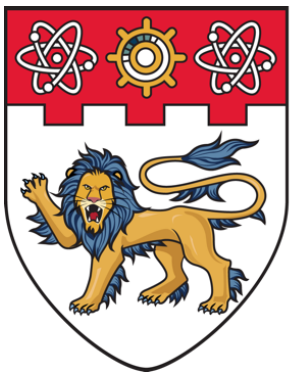

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

STRATEGIES TO MODULATE AMORPHOUS OXIDE SEMICONDUCTOR PROPERTIES FOR LOW TEMPERATURE TRANSPARENT TRANSISTORS

KULKARNI MOHIT RAMESHCHANDRA

SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

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A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2019

Statement of Originality

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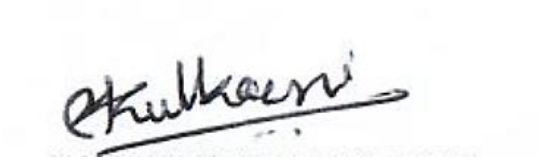

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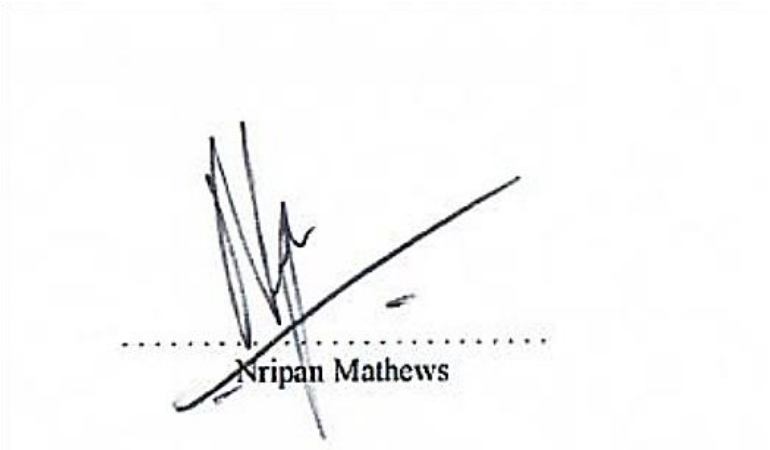

Authorship Attribution Statement

This thesis (chapter 6) contains material from a research article published in the following peer-reviewed journal in which I am listed an author.

Chapter 4 is currently being prepared as a manuscript-

Mohit Rameshchandra Kulkarni, Amoolya Nirmal, Rohit Abraham John, Nidhi Tiwari, Nripan Mathews. "Oxygen vacancies modulation using overlayer chosen from the Ellingham diagram for low-temperature Oxide Thin film transistor activation."

The contributions of the co-authors are as follows:

- A/Prof N. Mathews provided the initial project direction and edited the manuscript drafts.
- I prepared the manuscript draft, and the manuscript was revised by all the co-authors.
- I co-designed the study with A/Prof N. Mathews, Dr. Nidhi, Dr. Rohit
- I performed all the device fabrication and characterization at MSE, NTU, and ERIAN, NTU.

The first part of **Chapter 5** is currently being prepared as a manuscript-

Mohit Rameshchandra Kulkarni, Amoolya Nirmal, Rohit Abraham John, Nidhi Tiwari, Nripan Mathews. "Novel universal surface charge doping mechanism for manipulation of oxide thin film transistor properties."

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- I performed all the device fabrication and characterization at MSE, NTU, and ERIAN, NTU.

The second part of **Chapter 5** is currently being prepared as a manuscript-

Mohit Rameshchandra Kulkarni, Amoolya Nirmal, Rohit Abraham John, Nidhi Tiwari, Nripan Mathews. "Hydrogen peroxide assisted wet chemical treatment as a route for controlled passivation of oxygen vacancies for flexible thin film transistor application."

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- I performed all the device fabrication and characterization at MSE, NTU, and ERIAN, NTU.
- Dr. Rohit assisted with Neuromorphic data collection and analysis.

Chapter 6 is published as a manuscript

Mohit Rameshchandra Kulkarni, Rohit Abraham John, Nidhi Tiwari, Amoolya Nirmal, Si En Ng, Anh Chien Nguyen, Nripan Mathews "Field-Driven Athermal Activation Of Amorphous Metal Oxide Semiconductors For Flexible Programmable Logic Circuits And Neuromorphic Electronics" Small 2019, 1901457; DOI: 10.1002/smll.201901457

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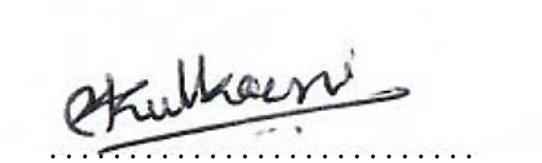

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Kulkarni Mohit Rameshchandra

Abstract

Amorphous Metal Oxide Semiconductors (AMOS) with properties such as high optical transparency, flexibility, and high electron mobility have emerged as a promising candidate over a-Si:H, poly-Si and organic semiconductor in the field of transparent and flexible electronics. However, the high processing temperature of AMOS constrains the fabrication process, including the choice of substrates, as the plastic substrates used for flexible electronics impose a limited thermal budget. In addition, unique novel applications such as oxide semiconductor-based logic gates, non-von Neumann architecture based neuromorphic devices and RRAM, require post-fabrication control over conductance of oxide semiconductor. Consequently, to achieve both athermal activations and better control over oxide conductivity, modulation of the charge carriers becomes vital. Typically, the carrier concentration of metal oxides is critically determined by the oxygen vacancies/ defects and external doping, where the increase in oxygen vacancies gives rise to higher conductivity/mobility. Oxygen vacancies are typically controlled during the growth of the thin films by modulating the partial pressure of oxygen during sputtering/ other vacuum deposition processes or through high-temperature post-deposition annealing. Such approaches increase the complexity of fabrication as well as allow less control over device behaviors. Hence the need for new post-fabrication techniques is manifested. The principal motivation of the thesis is to find alternate post-fabrication strategies to achieve the on-demand transformation of an oxide semiconductor for flexible electronics in order to avoid high-temperature annealing. In this work, the novel approaches to control oxygen vacancies concentration, and doping achieved through surface modification, which will decide charge carrier densities and charge transport in oxide semiconductors were investigated.

The feasibility of Ga/Zn-free Indium Tungsten Oxide (IWO) as a semiconducting channel layer for TFT was investigated. In-depth studies of various process parameters concluded that an IWO thickness of 20 nm, fabricated with an oxygen flow rate of 1sccm and annealed at 200 ^{o}C, yielded the best device performance. The work function of the electrode material had a significant impact on the performance of the TFT with ITO emerging as the best

candidate. Flexible TFTs on PI substrates with non-degraded device performance for a bending radius of up to 3 mm were also demonstrated. The prospect of athermal annealing with the inclusion of a reducing oxide layer carefully chosen from the Ellingham diagram used as an overlayer on the semiconducting oxide layer was also explored. From these studies, it was discovered that the current through the channel was increased after the deposition of the overlayer, which can be linked to the increased number of oxygen vacancies in the channel. The on-state current of the TFT was shown to increase with the thickness of overlayer oxide from 1 nm to 9 nm. As the demand for oxygen from overlayer rises with thickness, more oxygen is removed from the bottom layer of the semiconductor oxide, thus making it more metallic. Experiments with different overlayer oxides and semiconducting oxides were conducted, which concluded that oxide reduction through overlayer deposition could provide a universal method for athermally activating or transforming TFTs from enhancement mode operation into depletion mode operation as well as improving the environmental stability of the devices.

Another method for selective on-demand modification of TFT properties using chemical surface treatment was also explored in the dissertation. Herein, the possibilities of dipole induced and doping induced charge carrier modulation of oxide semiconductors were explored by grafting various self-assembled monolayers (SAMs) such as silane, thiol, polymers with amine groups and a few organic dopant molecules on IWO channel layer. Such surface modifications can achieve a change in the carrier concentration by change in work function or shifting- pinning of the Fermi level, or additional field generated due to dipoles created at the surface. This increase in carrier concentration can be utilized to achieve high-performance TFT. Hydrogen peroxide assisted wet chemical treatment was also explored as a route for controlled passivation of oxygen vacancies. Dynamic carrier modulation utilizing a novel field-driven athermal activation of AMOS channels via electrolyte gating was also implemented. The high electrostatic field provided by the ionic liquid gating facilitates reversible migration of the charged oxygen species. The study also gave critical insights into different parameters affecting oxygen vacancies generation.

Various material characterization techniques such as X-ray Photoelectron Spectroscopy (XPS), Ultraviolet photoelectron spectroscopy (UPS), Fourier-transform infrared spectroscopy (FTIR) and electrical characterizations were used to support these effects on oxide semiconductor. The above-mentioned techniques targeted the control of semiconductor conductance, thus altering the working mode of thin-film transistor from depletion-mode to enhancement mode and vice versa. This active programming of the operating mode of TFT is beneficial for the development of inverter logic gates. In addition, neuromorphic transistors, facilitated by field-induced activation, were also demonstrated. Hence, the ability to modify the electronic properties of amorphous metal oxide semiconductor precisely using oxygen vacancy modulation and surface chemical doping to unlock optimal electrical performances of electronic devices would be relevant for the development of the flexible and transparent electronics.

Lay Summary

Flexible and transparent electronics field is projected as the next-generation technology with applications such as flexible and foldable displays, wearable, and conformable electronics. The prerequisites of consumer electronics include highly reliable performance devices. Owing to an amorphous phase free from defects (called grain boundaries), which results in decreased obstacles (interfacial traps and scattering centers) for light to pass and electrical current to flow, amorphous Metal Oxide Semiconductors (AMOS) exhibit properties such as high optical transparency and high electron mobility. These properties make AMOS a promising candidate in comparison to its competitors, such as amorphous Silicon, polycrystalline Silicon, and organic semiconductors, for flexible and transparent electronics. However, the high processing temperature of AMOS constrains the fabrication process, including the choice of substrates, since the need of plastic substrates for flexible electronics imposes a thermal limit on the processes, due to low-temperature handling capability of plastics.

The principal motivation of the dissertation is the need to decrease the high process temperature required to activate the oxide semiconductor for flexible electronics. Apart from activation of the oxide semiconductor, various novel electronic applications such as oxide semiconductor-based logic gates, non-von Neumann architecture based neuromorphic devices and memory devices, require control over conductance of oxide semiconductor. Consequently, to achieve both goals, active modulation of the charge carriers responsible for the conduction in the oxide semiconductor becomes essential. Typically, the carrier concentration of metal oxides is critically determined by the defects called oxygen vacancies and external doping. Increase in oxygen vacancies gives rise to higher conductivity/mobility. Oxygen vacancies are usually controlled during the growth of the thin films by varying the partial pressure of oxygen during sputtering/ other vacuum deposition processes or through high-temperature post-deposition annealing. Such approaches increase the complexity of fabrication and modulate both bulk and surface properties at the same time, limiting the applicability of the oxides to novel architectures and to flexible substrates. Hence, this dissertation aims to explore avenues to achieve the

on-demand transformation of oxide semiconductor mainly for transistor configurations using novel approaches to athermally control concentration of oxygen vacancies and doping achieved through surface modification, which will decide charge carrier densities and charge transport in oxide semiconductors, thus unlocking optimal electrical performances of electronic devices revolutionizing the flexible and transparent electronics field.

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I am very grateful to all the friends in and outside of NTU without whom my journey would not behave been possible. I would especially like to thank Sneha and her family for making me feel at home in Singapore. They have always been a great help. I hope all this love and affection from friends continues to flourish.

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Last, but not the least I give my sincerest thanks to two of my most wonderful teachers - my beloved parents. Any amount of gratitude I express shall not be enough to quantify their love towards me. I would never have reached this stage in my life

without their blessings, sacrifices and constant support. I admire, love and respect them the most and their mere presence in my life is an inspiration to me.

To be honest, pursuing a PhD has been a roller-coaster ride with its fair share of ups and downs. It has been a journey filled with love and happiness while also serving as a great learning experience.

This journey is akin to a jigsaw puzzle with the aforementioned people being the puzzle pieces. This puzzle of mine would have remained incomplete if not for them, and for this I am eternally grateful.

Table of Contents

Table Captions

Figure Captions

Abbreviations

θ	Angle of Diffraction
λ	Wavelength
μ, μ_{FE}	Field Effect Mobility
Φ	Work Function
2D	Two Dimensional
AFM	Atomic Force Microscopy
Al_2O_3	Alumina
AMOS	Amorphous Metal Oxide
APTES	(3-AminoPropyl)TriEthoxySilane
Ar	Argon
Ca	Calcium
CaO	Calcium Oxide
CMOS	Complementary Metal Oxide Semiconductor
CNT	Carbon Nano Tube
DC	Direct Current
DDT	1-Dodecanethiol
EDL	Electrical Double Layer
EMIM TFSI	1-Ethyl-3-MethylIMidazolium bis(TriFluoromethylSulfonyl)Imide
F4TCNQ	2,3,5,6-TetraFluoro-7,7,8,8-TetraCyaNoQuinodimethane
FESEM	Field Emission Scanning Electron Microscope
FET	Field Effect Transistor
FTIR	Fourier-transform infrared spectroscopy
H_2O_2	Hydrogen Peroxide
HfO_2	Hafnium Oxide
HPA	High Pressure Annealing
I_D, I_{DS}	Drain to Source Current
I_{GS}	Gate Source current/ leakage current
IGZO	Indium Gallium Zinc Oxide
IL	Ionic Liquid
In_2O_3	Indium Oxide
I_{off}	Off Current
I_{on}	On Current
ITO	Indium Tin Oxide
IWO	Indium Tungsten Oxide
IZO	Indium Zinc Oxide
IZTO	Indium Zinc Tin Oxide
LED	Light Emitting Diode
LTD	Long Term Depression
LTP	Long Term potentiation
MoS_2	Molybdenum Disulphide

N_2	Nitrogen Gas
O_2	Oxygen Gas
OFET	Organic Field-Effect Transistor
PEDOT:PSS	Poly(3,4-EthyleneDiOxyThiophene) PolyStyrene Sulfonate
PEI	PolyEthylenImine
PEIE	PolyEthylenImine Ethoxylated
PESA	PhotoEmission Spectroscopy in Air
PFDT	1H,1H,2H,2H-PerFluoroDecaneThiol
RAM	Random Access memory
RF	Radio Frequency
RTA	Rapid Thermal Annealing
SAM	Self Assembled Monolayer
SiO_2	Silicon Dioxide
SS	Subthreshold Swing
STDP	Spike-Timing Dependent Plasticity
TFT	Thin Film Transistor
TiO_2	Titanium dioxide
TPPO	TriPhenylPhosphine Oxide
UPS	Ultraviolet photoelectron spectroscopy
UV	Ultra Violet
V	Voltage
V_D, V_{DS}	Drain Voltage
V_G, V_{GS}	Gate voltage
V_o, V_{ox}	Oxygen Vacancies
V_{th}	Threshold Voltage
W	Tungsten
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
Y_2O_3	Yttrium(III) oxide
ZrO_2	Zirconium dioxide
ZTO	Zinc Tin Oxide

Chapter 1

Introduction

This Chapter introduces the significance of oxide semiconductor and the motivation for the dissertation. The issues limiting the usage of oxide thin film transistors are identified and discussed, with a focus on the need to eliminate high temperature process during the fabrication of oxide semiconductors for the development of next generation transparent and flexible electronics. The research objective of this work is to investigate novel approaches towards controlling charge carrier densities and charge transport in oxide semiconductors through the modulation of oxygen vacancy concentration and doping/ workfunction modification. Following the discussion on research objectives and scope, general strategies to modulate the inherent properties of oxide semiconductors such as oxygen vacancies and charge carrier concentration are examined. The chapter also clarifies the necessity for modulation of TFT parameters and the effect of above-mentioned inherent features. Subsequently, the hypothesis and approaches are also specified; followed by an overview of the thesis with a brief introduction to each chapter. The significant findings and outcomes are provided in the last section.

1.1 Overview and motivation

The field of Flexible - transparent electronics is projected as a next - generation technology. It's potential applications include flexible and foldable displays, wearable and conformable electronics, fabrication of electronic circuits and devices on flexible and transparent substrates such as plastic is a primary criterion. Apart from the limited thermal budget imposed by the use of plastic substrates, the prerequisites of consumer electronics include highly reliable device performance. A comparison between available semiconductors suitable for flexible substrates is given in **Table 1-1**, and **Figure 1-1**. [1], [2] Organic semiconductors promise to be a prominent choice for such applications due to their low processing temperature. However, consistent low performance in terms of low mobility and high operating voltages, non-uniformity and instability has led the researchers to investigate other material systems, including poly-Si and a-Si. However, higher processing temperatures and opacity limit their usage for flexible and transparent devices.

Table 1-1: Comparison between available flexible semiconductors [1]

Sr. No.	Material	Deposition Technique	Mobility ($cm^2/V.s$)	Spatial Uniformity	Stability
1	Amorphous Silicon	PECVD	<1	High	Low
2	Nanocrystalline Silicon	PECVD	<10	Medium	Medium
3	Polycrystalline Silicon	Excimer LASER (on high-T annealing)	100	Low	High
4	Organics	Printing, vacuum evaporation), solution process	<20	Low	Low
5	Oxide semiconductor	Sputtering, Printing, spray coating, solution process	<50	High	High
6	CNT networks	Printing, spray coating, solution process	<10	Low	Low
7	Graphene	CVD graphene	50-9000	N/A	N/A

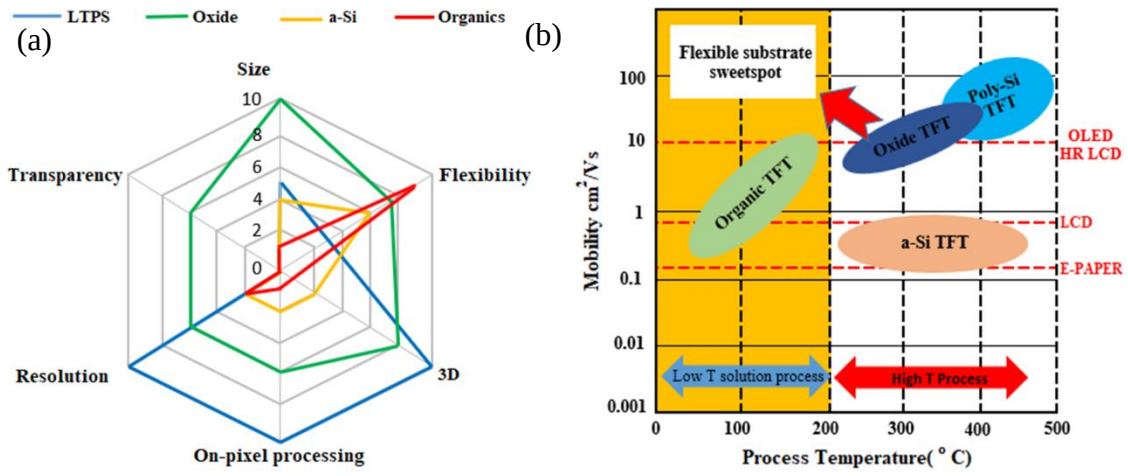

Figure 1-1: A comparison between available semiconductors suitable for flexible substrates.

It is evident from **Table 1-1**and **Figure 1-1** (inspired from [1], [2]), that amorphous oxide semiconductors of post-transition metals (such as In, Ga, Zn, Sn, W) with their thin-film processing capability, markedly different optoelectronic properties including electronic structure and defect states, have superior performance over Si and organic semiconductors with higher optical transparency, better electron mobility and ability to handle higher voltages and temperatures without breakdown. Owing to an amorphous phase, free from grain boundaries, which results in decreased interfacial traps and scattering centers, Amorphous Metal Oxide Semiconductors (AMOS) exhibit high optical transparency and high electron mobility[3]–[5]. The unique optical, electronic, and structural properties of oxide semiconductor enable conventional as well as novel and exotic applications such as neuromorphic electronics [6]. Deposition of the oxide thin films are done by either vacuum techniques such as sputtering, ALD, etc. or by ambient processes such as solution processing or spray pyrolysis. Solution-processed TFTs require relatively higher processing temperatures, high pressures for proper film formation, densification, and impurity removal; despite which they exhibit relatively low carrier mobilities (**Figure 1-2**) [7]. Although the vacuum-deposited AMOS exhibit enhanced device performance with higher mobilities, a high-temperature post-annealing treatment (temperatures>350 ^{o}C) is required, which is often incompatible with flexible substrates (which can typically handle temperatures <200^{O} C) [7].

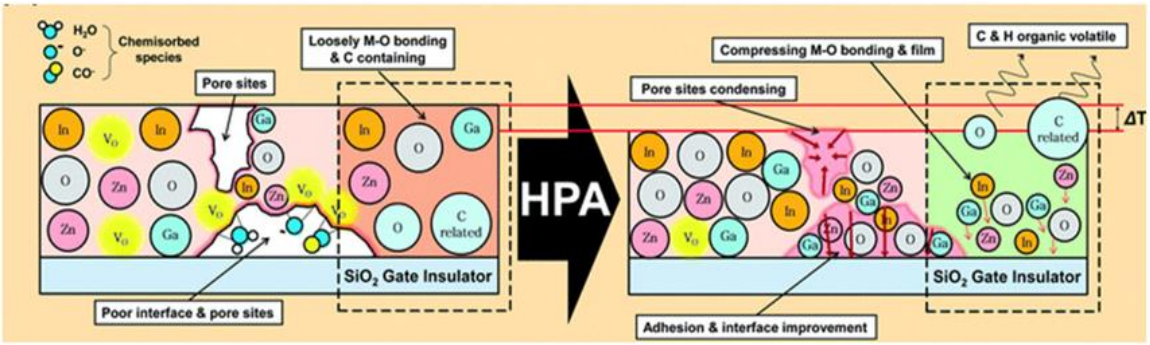

Figure 1-2: Illustration of high-pressure annealing utilized in the reduction in oxygen vacancies simultaneously in the bulk and interfaces. [7] Reproduced with permission from IOPscience.

Irrespective of the deposition techniques and apart from the uniform film formation, the properties of metal oxides are critically determined by the oxygen vacancies/defects that form in them.[1], [8] Oxygen vacancies are a special class of point defects, which have a marked influence on the behavior of oxide materials. Depending on the material, the structure and properties of oxygen vacancies can vary substantially. With fewer oxygen vacancies to carry out charge carrier transport, a less conducting semiconductor will result in a normally-off (deep enhancement region) TFT. In order to activate these transistors, a larger number of oxygen vacancies should be generated. Whereas in normally-on (deep depletion region) TFT the number of oxygen vacancies should be suppressed in order to operate the TFT within a smaller working voltage range. Oxygen vacancies are thus a fingerprint of the electronic properties of the oxide TFT. Oxygen vacancies are typically controlled during the growth of the thin films by modulating the partial pressure of oxygen during sputtering/ other vacuum deposition processes or through high-temperature post-deposition annealing[9]. Such approaches simultaneously modify both the bulk and the surface properties of all the devices on the given substrate thus limiting the range of applications that can be probed. In addition, conventional modulation techniques such as high temperature- high-pressure annealing are not always efficient or desirable for flexible device fabrication. Therefore, athermal, on-demand modulation of oxygen vacancies has tremendous potential. Post-treatment approaches could possibly accomplish a similar outcome as that of thermal treatments and need to be explored in order to discover new ways for oxygen vacancy modulation of an oxide semiconductor.

1.2 Objectives and scope

The concepts used in this dissertation for post-fabrication approaches of metal oxide semiconductor includes (i) reduction and oxidation of oxide semiconductor to increase or decrease oxygen vacancies respectively, (ii) field-induced manipulation of oxygen vacancies, (iii) surface chemical modifications used for controlling charge carrier concentration of oxide semiconductor. Surface dopants can mediate charge transfer through the chemisorbed species.[10] It has also been shown that the work function of metal/oxides can be changed through such surface doping techniques.[11]–[13] The details of these techniques are given below.

Specific objectives of this dissertation include:

1. *Study of process parameters and Ellingham diagram driven use of capping layer for semiconducting oxide reduction*:

The objective is to study the process parameters affecting the properties of tungsten doped Indium oxide TFT and obtain control over various TFT attributes. In addition, various novel processes for on-demand modulation of oxygen vacancies responsible for the properties of TFT will be evaluated. With the aid of post-fabrication techniques, the control over conductance of semiconductor is targeted, altering the working mode of TFT from enhancement mode to depletion mode and vice versa. These manipulations of oxygen vacancies can be done through chemical treatment via oxidation or reduction of the film. For reduction of film, well established Ellingham diagrams will be explored. These diagrams are widely used for extraction of metal from its oxides/sulfides. They suggest the viability of reduction of one oxide by others and the preferred conditions for the reaction. Reducing oxide overlayer can be used to modify the oxygen vacancies of the underlying oxide layer, thereby controlling the film's electronic properties. This approach will involve the utilization of judiciously chosen type of oxide overlayers. These overlayers will be used as capping layers for oxide semiconductors. **Figure 1-3** depicts the role of the capping layer in modulating the transport of oxygen vacancies (diffusion of oxygen) from and to

the active layer. These diffusion control layers can be designed and patterned to facilitate the transport of species from an atmosphere in and out of the active layer.

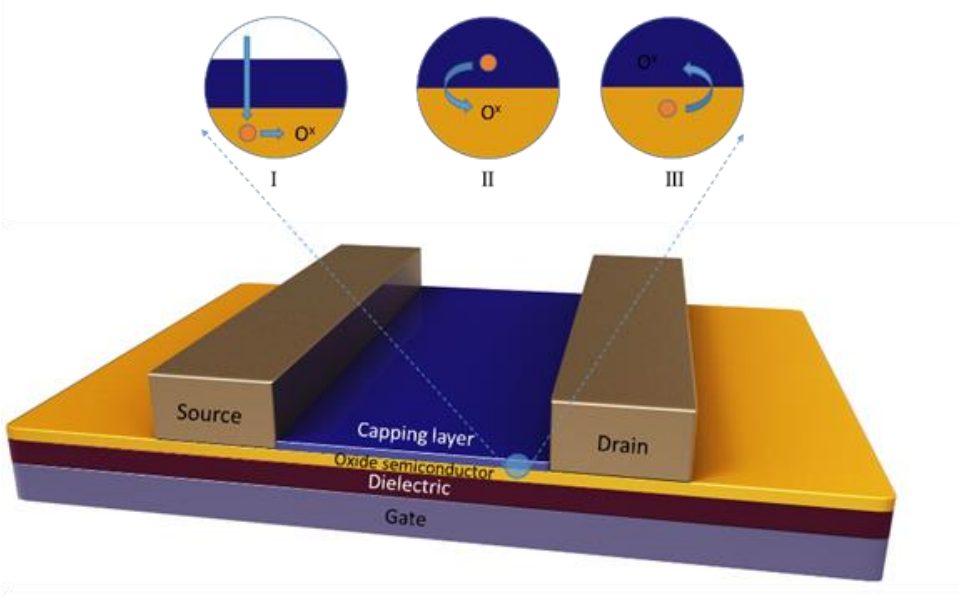

Figure 1-3: The mechanism of oxidation and reduction occurring between the semiconducting oxide and overlayer oxide in capped thin film transistor.

2. *Chemical modification to control carrier concentration in oxide thin films*:

Herein, the objective is to explore the possibility of surface chemical treatments in order to achieve the required attributes of the active device. Such surface treatments can account for the change in the carrier concentration through surface dopant mediated charge transfer, work function alteration, shift or pinning of the Fermi level and creation of an internal electric field to drive charge carriers, which can cumulatively be used to achieve high-performance in TFTs. This can be achieved through various surface treatments such as Silane, Thiol coatings, charge-neutral polymer coating, and doping molecules. However, some AMOS such as Indium oxide films fabricated at low temperatures are highly conducting because of the presence of excess oxygen vacancies, requiring high voltages to operate the TFT. In general, high thermal annealing usually is used to passivate these vacancies, which, as discussed in the previous section, is not feasible for flexible substrates.

Hence, an oxidizer (e.g., hydrogen peroxide) assisted wet chemical treatment was also explored as a route to athermally control the passivation of oxygen vacancies.

3. *Electric field-induced dynamic manipulation of oxygen vacancies*:

The aim is to investigate the effects of dynamically modifiable oxygen vacancy generation and annihilation in the oxide semiconductor. The objectives mentioned previously focused on a static modulation in the attributes. That is, the processes are irreversible due to permanent deposition of chemisorbed species on the oxide surface. There are some applications such as neuromorphic computing, which requires dynamic control on the conductivity of oxide. This can be achieved through controlled manipulation of oxygen vacancies. An on-demand field-induced modulation of oxygen vacancies can be used to achieve their reversible manipulation via electrolyte gating. The high electrostatic field provided by the ionic liquid gating facilitates reversible migration of the charged oxygen species.

4. *Employing the oxygen vacancy modulation to realize applications such as inverters and neuromorphic synapses:*

Utilization of the novel techniques discussed above in various applications is important to showcase their functionality. Transistors are fundamental building blocks of logic gates. An inverter is the basic logic gate. An exclusively n-type TFT inverter can be made which requires one TFT to be in enhancement mode and other in depletion mode. However, post-annealed samples usually are in enhancement mode and typically do not allow the customized modulation of semiconductor properties. However, these novel techniques can be used to modulate the electrical properties of the semiconductor to control these operating modes of TFT. Also, the control over conduction achieved through these techniques can be explored for applications such as athermal activation of flexible devices, and unique application such as neuromorphic circuits can be explored.

1.3 Hypothesis

1. The properties of oxide semiconducters can be modulated through the use of overlayer chosen with the help of Ellingham diagram. Ellingham diagram predicts how one oxide placed below in the diagram can be used to reduce the other oxide. Therefore, by deciding the overlayer composition, specifically chosen using the Ellingham diagrams, the oxide TFT properties can be controlled.

2. On-demand alteration of TFT properties is possible through various chemical modification using surface treatments. These treatments can be used to change the work function/Fermi level of semiconducting oxides through dipole creation at the surface or surface doping allowing the oxide film to increase or decrease charge carriers as required. The replacement of the annealing step required to transform inherently highly conductive indium-based oxides with high number of oxygen vacancies to low conductance state, by utilizing strong oxidizers such as hydrogen peroxide to increase oxygen content is also proposed.

3. Reversible characteristics of oxide TFT can be achieved through electric-field-driven migration of oxygen vacancies. This process will require a substantial electric field, for which the use of an electrical double layer formed at the interface of the ionic liquid and oxide is also propose.

4. The capability of athermal conductance manipulation achieved through dynamic variation of oxygen vacancies can be used in applications such as athermal activation of TFT, controlling modes of operation of TFT for logic gate operation and neuromorphic behavior.

1.4 Dissertation overview

Chapter 1 provides a brief introduction on the motivation for this work. The hypotheses and approaches are concisely explained. Then the structure of the dissertation is provided, followed by significant findings and novelty.

Chapter 2 discusses recent developments in the application of thin film transistor using oxide semiconductor. Various conventional strategies for modulating oxygen vacancies and various surface treatments used for conducting oxides and metals are included. Finally, the research gap in the oxygen vacancies creation-annihilation and surface chemical treatments is stipulated to justify the motivation for this work.

Chapter 3 elucidates the rationale behind the material selection, details of various fabrication processes, physical and electrical characterization techniques used and the detailed procedure for extraction of parameters.

Chapter 4 details the study of processing parameters affecting the performance of tungsten-doped indium oxide TFT acquired by the conventional method of air annealing. The chapter also addresses the source and drain electrode material selection. The material characterization techniques such as XRD, AFM were used to characterize the material. The chapter also probes the use of Ellingham diagram for capping the semiconducting oxide layer in order to modulate oxygen vacancies. The effect of thickness of the capping oxide layer and annealing temperature on the oxide film is explored. Various parameters of TFT are calculated and compared.

Chapter 5 inspects the possibility of charge carrier modulation of oxide semiconductors using various self-assembled monolayers (SAMs) such as silane, thiol, polymers with amine groups and dopant molecules responsible for creation of dipoles induced modulating the work function of oxide or surface dopant mediated charge transfer which in turn controlled the characteristics of TFT. The material characterization techniques such as XPS, UPS, FTIR were used to endorse the effect of surface treatment. The chapter also

investigates the oxidation of oxide semiconductor to achieve the modulation of TFT parameters from depletion mode to enhancement mode. The latter is characterized by various material characterization techniques such as XPS, UPS, Mott Schottky measurement, optical absorption spectroscopy, PESA to support the claim of decreased oxygen vacancies.

Chapter 6 studies the on-demand reversible oxygen vacancy variation using electric field achieved using EDL formed at the junction of ionic liquid and oxide. The effect of environment on oxygen vacancies generation is studied. A detailed analysis of factors affecting the generation and intercalation of oxygen vacancies, were described in this chapter. Applications such as activation of a normally-off transistor, modulation of oxygen vacancies on flexible TFT, dynamic modulation of TFT from enhancement mode to depletion mode and vice versa, inverter using ionic liquid gating and use of conductivity modulation in the neuromorphic synaptic device were investigated.

Chapter 7 summarizes and concludes the validation of hypotheses discussed in this chapter. The chapter also discusses the possible directions of future work for the extension of this dissertation.

1.5 Finding and outcomes

1. *Study of various process parameters on IWO TFT (conventional oxygen vacancies modulation technique):*

Ga/Zn-free Indium Tungsten Oxide (IWO) is investigated as an alternative to IGZO as a channel layer. The W dopant in an edge-sharing polyhedral structure enhances the stability of high mobility In_2O_3 matrix.[14] The variation in conduction of IWO layer through the controlling of oxygen vacancies was achieved through varying the oxygen flow rate at the time of deposition and by conventional thermal annealing technique on SiO_2 substrate. Various electrode materials were also tested (Al, Ag, Au, and ITO). It was concluded that an IWO thickness of 20 nm, annealed at 200 ^oC, and fabricated with an oxygen flow rate

of 1 sccm yielded the best device performance. The TFT had the mobility of 15.07 cm^2/V.s, the threshold voltage of 10.26 V and a subthreshold swing of 1.13 V/dec; with ITO selected as the best electrode. A TFT on flexible substrate also was demonstrated so as to illustrate the usefulness of tungsten doped Indium oxide TFT.

2. *Use of Ellingham diagram for modulation of oxygen vacancies:*

Ellingham diagram which dictated careful selection of capping layer for semiconducting oxide layer reduction is described in this chapter. It was noted that the deposition of an appropriate capping layer drastically altered the device performance. For thicker capping layers the transistors becomes conductive while for thinner capping layers, the threshold voltage undergoes a profound negative shift. Critically, it was found that through a post-capping annealing step, original device characteristics could be nearly restored. Crucially, the capped devices showed enhanced stability compared to the un-capped devices after one week in air. For an un-capped device, its threshold voltage negatively shifted by 12.09V. While for a device with a 3 nm-thick Al_2O_3 capping layer deposited with an oxygen flow rate of 1sccm, its threshold voltage negatively shifted only by 2.94V. Overall, a 3 nm-thick Al_2O_3 passivation layer deposited with an oxygen flow rate of 1 sccm yielded the best device stability. During the capping layer thickness study, it was confirmed that deposition of the alumina layer increased the resultant oxygen vacancy concentration in the channel. This phenomenon was also used to try to activate a deep IGZO transistor without the need for an annealing step. The IGZO TFT device left shifted the threshold voltage with improved mobility, proving that the method is universal and can be utilized for various applications.

3. *Selective modification of oxide TFT using chemical surface treatment:*

Surface chemical treatment was used to alter the electronic characteristics of the oxide semiconductor channel in order to modulate the TFT attributes. The investigation covered various types of surface treatments such as Silanes in the form of (3-AminoPropyl)TriEthoxySilane (APTES), Thiols in the form of 1-DoDecaneThiol (DDT)

and 1H,1H,2H,2H-Perfluorodecanethiol (PFDT) and dopant molecules such as TriPhenylPhosphine Oxide (TPPO) (n-type doping), and charge neutral polymers containing aliphatic amine groups PolyEthylenImine (PEI), PolyEthylenImine Ethoxylated (PEIE). It was evident that the strong electron-donating characteristics of the amine group in APTES, PEI, and PEIE allowed a significant enhancement in the mobilities as well as V_{th} control in a negative direction. Apart from that, the use of fluorinated chemicals such as PFDT also have shown potential for modulating the threshold voltage in a positive direction. The type of dopant is useful in controlling the threshold voltage; the n-type dopant can be used for negative V_{th} shift, whereas p-type dopant can be used for positive V_{th} shift. The electron donating capability of the surface dopant group such as amine group might help the shallow electron traps of semiconductor to be filled, hence improving the mobility. Eventually, this modification would help to achieve the next generation of flexible devices applications which demand low processing temperature and higher control over the conductance of the channel.

4. *Modulation of oxygen vacancies using wet chemical treatment:*

Surface state alteration through hydrogen peroxide assisted wet chemical treatment as a route for controlled passivation of oxygen vacancies determining the electrical properties of IWO for flexible thin film transistor application was investigated. This passivation was responsible for decreased carrier concentration which resulted in decreased conductivity of oxide TFT observed in terms of increased threshold voltage. The oxidized film characterization by XPS, UPS, Optical absorption spectroscopy, Mott-Schottky plot, and PESA measurements suggested increased oxide content in the film. The use of athermal oxidation of TFT devices was demonstrated; it would serve a basis for activation of flexible active devices without exceeding the thermal budget of flexible substrates.

5. *Electric field driven regulated conductance manipulation of oxide semiconductor:*

A novel field-driven athermal activation of AMOS channels via an electrolyte-gating approach was demonstrated. Large applied electric field facilitates the migration of charged

oxygen species across the semiconductor-dielectric interface. This approach modulates the local electronic structure of the channel thus generating sufficient carriers for charge transport and activating oxygen-compensated thin-films athermally.[15] An active surface modification using ionic liquid (IL) gating was explored for this approach due to its ability to apply a high electric field. Ionic liquid (IL) ions interact with the solid surface at the Electrical Double Layer (EDL) interface through electrostatic or van der Waals interaction without any chemical bonding due to their inert chemical reactivity within the electrochemical potential windows.

The thin-film-transistors (TFTs) investigated in this work depicted an enhancement of linear-mobility from 51 to 105.25 cm^2/Vs (ionic-gated) and 8.09 cm^2/Vs to 14.49 cm^2/Vs (back-gated), by creating additional oxygen vacancies.[15] The accompanying stochiometric transformations, monitored via spectroscopic measurements (XPS) corroborate the detailed electrical (TFT, current-evolution) parameter analyses, providing critical insights into the underlying oxygen-vacancy generation mechanism and clearly demonstrating field-induced activation as a promising alternative to conventional high-temperature annealing strategies while facilitating on-demand dynamic programming of the operation modes of transistors (enhancement vs. depletion). With this technique facile fabrication of logic circuits and neuromorphic transistors for bio-inspired computing was also achieved.[15]

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Chapter 2

Literature review

This chapter critically reviews the literature for thin film transistors for flexible devices from basics to recent advances. Crucial attributes that define the TFT operation are covered, with a discussion of the effect of oxygen vacancies on these attributes. A detailed review of various state of art annealing techniques for oxide semiconductors is given along-with the limitations of such techniques in flexible device applications. The need for controlled modulation of charge carriers is examined. Various non-conventional approaches used for oxygen vacancies modulation for oxide semiconductor is discussed. The research gap entailing the development of novel techniques for controlling attributes of thin film transistors is provided to justify the motivation of this work; the need for various low-temperature chemical techniques to modulate oxygen vacancies and charge doping mechanisms.

2.1 Overview and requirement of flexible electronics

Amorphous Metal Oxide Semiconductors (AMOS) exhibit properties such as high optical transparency and high electron mobility owing to an amorphous phase, free from grain boundaries resulting in decreased interfacial traps and scattering centers. [1]–[3] These properties make AMOS a promising candidate in comparison to a-Si:H and poly-Si for flexible and transparent electronics. The field has seen massive growth in the last 15 years after Hoffman et al. demonstrated a transparent ZnO transistor.[4], [5] Many different applications, mainly transparent display technologies, started booming with this development. As well as many new (**Figure 2-1**) cutting-edge, transparent and flexible electronic applications emerged such as flexible and transparent circuitry, e-skin, smart contact lenses. Neuromorphic flexible devices, e-paper, artificial-skin, the backplane of LED displays, mobile phones, etc.[2], [6]–[13]

Flexible electronics and need for low-temperature activation:

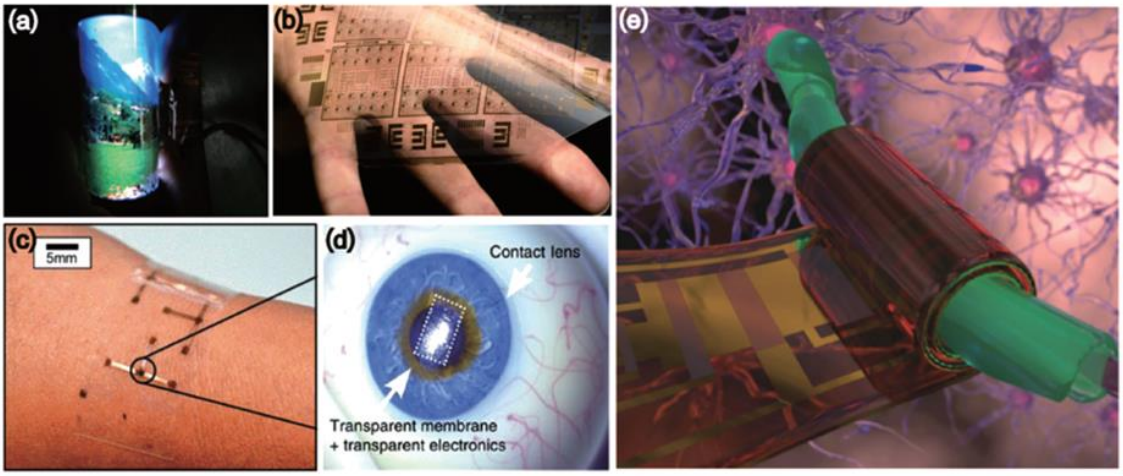

Figure 2-1: Flexible electronics applications (a) flexible display driven by IGZO [10] Reproduced with permission from AIP Publishing. (b) flexible transparent circuitry [11] Reproduced with permission from AIP Publishing. (c) electronic skin (d) smart contact lens [12] Reproduced with permission from Springer Nature (e) neuromorphic flexible devices. [13] Reproduced with permission from IOPscience.

In pursuit of a suitable material for these applications, various semiconducting amorphous oxides such as Tin oxide (SnOx), Indium Gallium Zinc Oxide (IGZO), Indium Oxide

(In_2O_3), Indium Gallium Oxide (IGO), Indium Zinc Oxide (IZO) and Zinc Tin Oxide (ZTO) are being extensively researched. [14]–[16] Deposition of these thin films are done by either vacuum techniques such as sputtering, ALD, etc. or by ambient processes such as solution processing or spray pyrolysis. Solution-processed TFTs require relatively higher processing temperatures for proper film formation, densification, and impurity removal; despite which they exhibit relatively low carrier mobilities[17]. Although the vacuum deposited AMOS exhibit better device performance with higher mobilities, a post-annealing treatment (temperatures>350 ^oC) is required, which is often incompatible with flexible substrates (which can typically handle temperatures <200^O C) [17]. Alternative annealing techniques such as photo-annealing [18], require high energy light source (e.g., ultraviolet light source) for annealing, and generates reactive and harmful gases such as ozone and other unstable oxygen radicals during the process. Therefore, new alternatives for activation/improvement of oxide thin film transistor's properties are being explored. With research focus on oxygen vacancies modulation of an oxide semiconductor for flexible electronics, the chapter gives an overview of flexible electronics and TFT devices, attributes of TFT that are affected by oxygen vacancies, followed by a summary of the state-of-the-art oxygen modulation techniques.

2.2 Thin film Transistor

Thin Film Transistors are three terminal devices where the flow of electrons between two terminals (source and drain) is controlled by the third terminal (Gate). TFT working principle is same as that of MOSFET, with slight variation in the structure. However, MOSFET uses single crystal Si wafer as a substrate and active area in the device. While expensive, high temperature (>1000 ^oC) and complex processes such as material diffusion/implantation of dopants, lithography, and etching are used in MOSFET manufacturing,[19] TFTs can be fabricated on cheaper insulating substrates (such as glass, polymer, paper, etc.) and the remaining layers can be grown by cheaper and low temperature (<650 ^oC) vacuum or sol-gel deposition techniques.[19] Owing to the manufacturing process, active layer of TFT are mainly polycrystalline or amorphous. This structural difference affects the carrier transport in the active layer as compared to that of

in single crystal. Another significant difference between these two field effect controlled transistors is that the TFT works in accumulation region whereas MOSFET works in the inversion region. From various device configurations for TFT such as bottom gate staggered TFT, Bottom gate coplanar TFT, top gate staggered TFT, top gate coplanar TFT, double-gate TFT and vertical TFT[20], bottom contact staggered TFT configuration is widely used due to ease of processing, enhanced performance, and lower leakage path.[15]

2.2.1 Operation of TFT

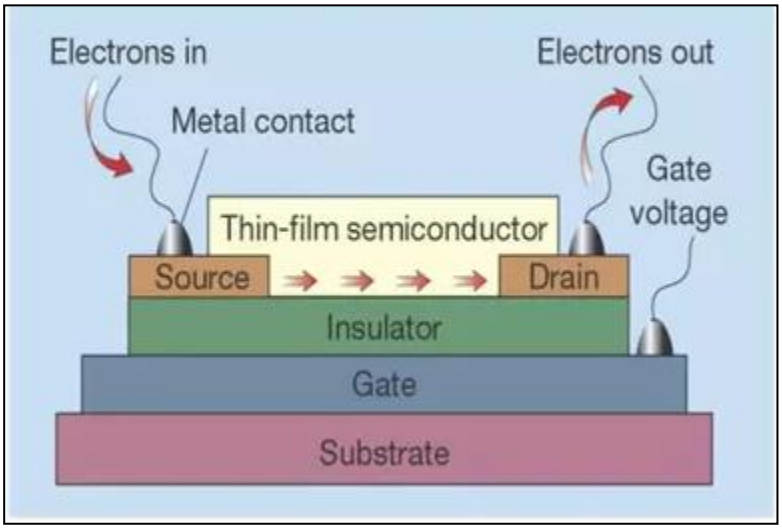

Figure 2-2: Typical TFT structure and operation. [21]

TFTs are three terminal field-effect devices (**Figure 2-2** [21]) which work by modulating the flow of current in a semiconductor placed between the source and drain electrodes [15]. A dielectric layer is placed between the semiconductor and a transversal gate electrode [15]. At a particular gate bias, current modulation is achieved by the capacitive injection of charge carriers close to the dielectric/semiconductor interface, known as field effect [22] and a channel is now created. TFT behavior is often characterized by two graphs. First, the transfer behavior is characterized by plotting the drain current against the gate voltage (**Figure 2-3** (a) [22]). It shows the behavior of the TFT in the "ON" and "OFF" state as well as the voltage needed to switch on the transistor. Secondly, the output behavior is characterized by plotting the drain current against the gate voltage (**Figure 2-3** (b) [22]). This graph shows the two regimes of charge transport in a TFT, either the linear regime or

the saturation regime. The magnitude of the drain bias, V_D, determines the regime of charge transport.

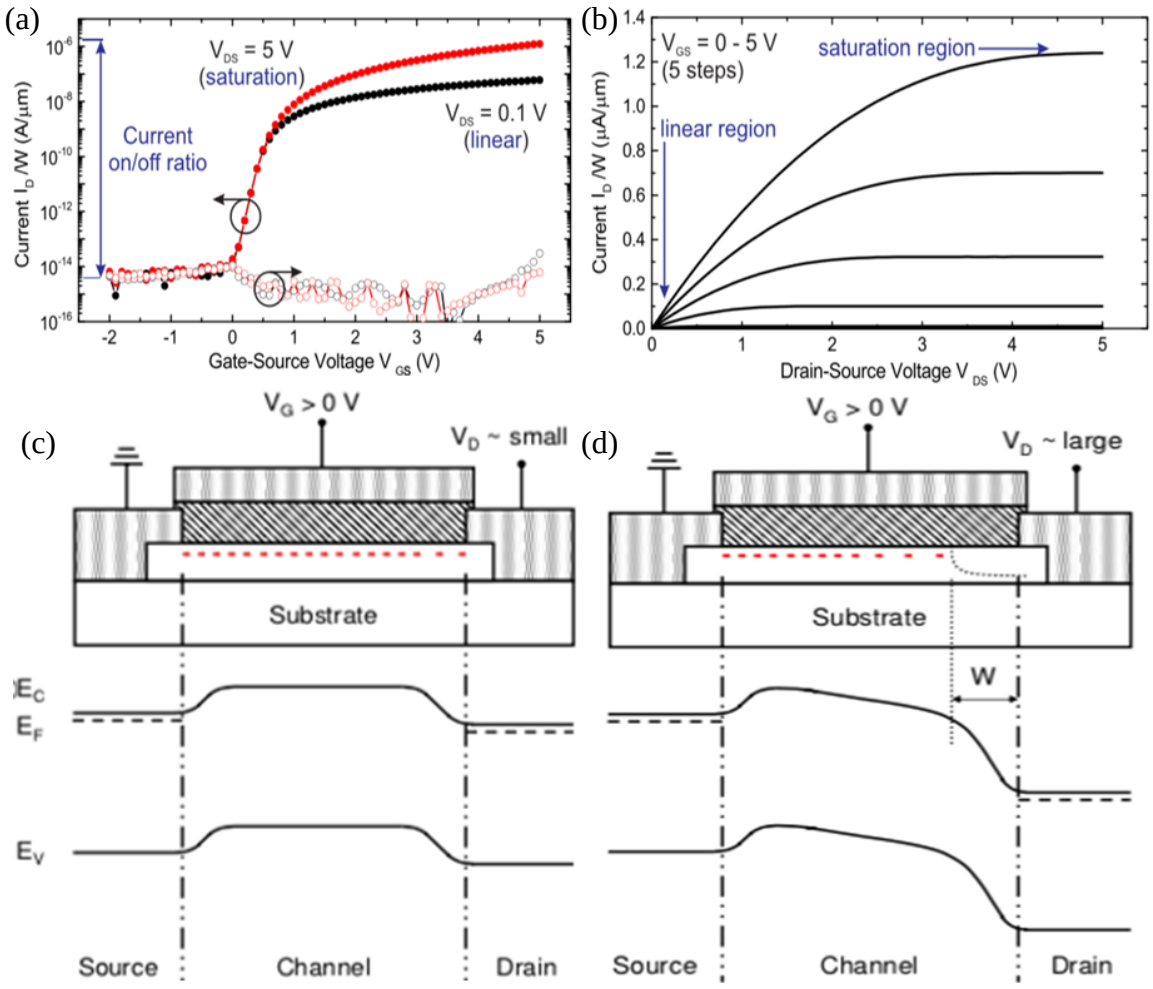

Figure 2-3: (a) Typical transfer characteristics of a TFT (b) typical output behavior of a TFT [22] reproduced with permission from AIP Publishing. cross-sectional and energy band diagrams for a TFT when V_{DS} is (c) small and (d) large. [23] Reproduced with permission from Oregon State University.

Two bias conditions (small and large V_D) are shown in **Figure 2-3** c,d [23], using cross-sectional views and energy band diagrams. The red "-" symbols in **Figure 2-3** c and d represent the flow of electrons in the channel. When the device is biased with significantly low V_D, the device operates in the linear region, where I_D increases linearly with respect to V_D. At sufficiently high V_D, I_D saturates, due to the formation of a depletion region close to the drain electrode, as shown by the region 'W' in **Figure 2-3** d. Essentially, as V*DS*

rises, the channel width reduces, i.e., the depletion region becomes wider. A decrease in channel width would potentially reduce $I_{D,}$ as fewer charge carriers reach the drain per unit time. However, when the depletion region gets more significant due to a larger drain bias, the strength of the electric field along the channel increases proportionally, hence the number of electrons that reach the drain per unit time remains the same, causing I_D to saturate.

2.2.2 The figure of merits for TFT

The key figures of merit to characterize the electrical performance of TFTs are Field-Effect Mobility (μ_{FE}), the Threshold voltage (V_{th}), Subthreshold Swing (SS), and the On/Off current ratio (I_{on}/I_{off}). These figures of merit are explained in detail below. And the procedure used to calculate is shown in experimental methodogy.

Mobility ($\mu_{FE)}$: This parameter quantifies the efficiency of charge carrier transport in the channel layer or simply put, how easily charge carriers can move through the semiconducting layer [15]. It affects the maximum drain current and the operating frequency of the device [22]. The operating frequency is a measure of how quickly the device can be turned "ON" and "OFF." Typically, high mobility is desired so that the device can switch between the "ON" and "OFF" state, as quickly as possible. This relationship between the mobility and the operating frequency (f) is represented by the equation 2-1 [24]:

$$f = \frac{\mu_{FE} V_D}{2\pi L^2} \text{.....Eq. 2-1}$$

where V_D is the drain voltage and L is the channel length.

Mobility depends on the inherent semiconductor properties and the quality of the film. The quality of the film is mainly determined by its crystallinity and defect density. Additional processing steps are often performed to improve the quality of the film [25]–[27] Mobility is also adversely affected by the various carrier scattering mechanisms, i.e., Lattice vibrations, impurities, defects, and grain boundaries [22]. In order to reduce scattering,

annealing is performed after deposition. Annealing provides the necessary thermal energy to facilitate atomic rearrangement, reducing disorder in the lattice and thus, reducing the extent of scattering [25]. In this case, the temperature of annealing would impact resultant mobility. It is anticipated that a rise in annealing temperature would improve mobility due to increased atomic rearrangement. Other factors that affect mobility include the number of charge carriers, which is influenced by channel thickness and the flow rate of oxygen during the semiconductor deposition. Thicker channel layers would mean more oxygen vacancies, resulting in more charge carriers and higher mobility. A lower oxygen flow rate during deposition would mean less oxygen is incorporated into the film, resulting in more oxygen vacancies and enhancing mobility.

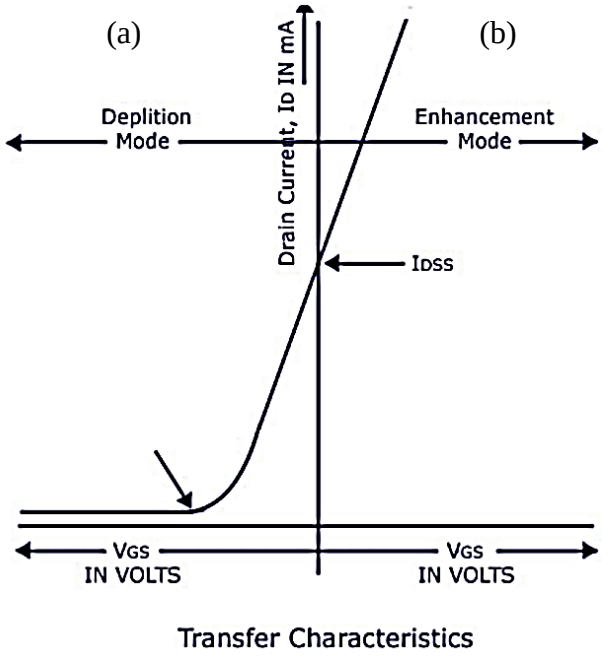

Figure 2-4: TFT working in the (a) depletion mode (b) enhancement mode. [29]

Threshold voltage (V_{th}): The gate voltage at which a channel is formed at the dielectric/semiconductor interface [22]. A positive/negative V_{th} would mean the device is operating in the enhancement /depletion mode, respectively. [28] A device working in the enhancement mode usually is "OFF" and requires a gate voltage to be turned "ON" (**Figure 2-4** a) [29]. A device in the depletion mode is usually "ON", and a gate voltage is supplied to turn the device "OFF" (**Figure 2-4** b [29]). Typically, devices operating in enhancement mode are desired as they do not require a gate voltage to be turned "OFF". This minimizes

power consumption and simplifies circuit design [15]. Usually, TFTs functioning in the enhancement mode are used for display application. This is intuitive as the displays are needed to be switched on when an appropriate voltage is applied and then switch "OFF" on the removal of the gate voltage.

ON-OFF ratio (I_{on}/I_{off}): It quantifies the difference in current flow when the device is "OFF" and when the device is "ON". Typically, a low off current and high on current is desired. A low off current implies a low leakage current [24], while a high on current indicates good transistor current and is advantageous when the device is used to drive some sort of circuitry. For example, a high ON current is needed if the transistor is to switch on another device [15]. ON-OFF ratio of 10^6 or larger is required for digital circuits, while a minimum of 10^4 is required for analog circuits [22]. I_{on}/I_{off} is affected by the number of charge carriers. Usually, a variation in the number of charge carriers tends to cause a more significant change in the off current. In this case, the channel thickness and the flow of oxygen during deposition can affect the $I_{on}/I_{off.}$

SS: SS is the change in gate voltage needed to change the drain current by an order of magnitude. It also functions as a measure of how quickly the device can be turned "OFF" and "ON" [22]. The quality of the dielectric/semiconductor interface directly affects the SS [22]. A low sub-threshold swing <100mV, together with a V_{th} close to 0 is desirable to reduce power consumption and the operating voltage in circuit applications. [22] SS has a theoretical limit of 60 mV/dec, originating from the electron density function. [30] This work does not look at methods to achieve a SS lower than the theoretical limit but focuses on the process parameters that affect the SS. Fundamentally, factors that affect the quality of the dielectric/semiconductor interface affects the SS. The impact of these factors, such as channel thickness and annealing temperature, on SS, will be investigated.

2.3 Available semiconductor comparison for flexible electronics

Flexibility and transparency of substrates are prerequisites for all flexible devices. Plastic substrates are commonly used for these purposes. These flexible substrates have very tight

thermal budget [17]; however semiconductors used for the above flexible applications require higher annealing temperature. Hence, low-temperature activation of semiconductor is necessary. The possibilities of a low thermal activation process are evaluated in this section.

Table 2-1: Comparison between oxide semiconductor, amorphous -Silicon, low-temperature polysilicon, and organic [15], [22], [31]–[36]

Sr.no.	TFT properties	Oxide semiconductor	a-Si	LTPS	Organic semiconductor
1	Microstructures	Amorphous	Amorphous	Poly-crystalline	Poly-crystalline
2	Mobility ($cm^2/V.s$)	1 to 100	0.1 to 1	50 to 100	0.1-10
3	Switching (V/dec)	0.1 to 0.6	0.4 to 0.5	0.2 to 0.3	0.1-1.0
4	Leakage current	$\sim10^{-13}$	$\sim10^{-12}$	$\sim10^{-12}$	$\sim10^{-12}$
5	Manufacturing cost	Low	Low	High	Low
6	Long term reliability	High	Low	High	Low in air
7	Yield	High	High	Medium	High
8	Process temperature	RT to 350	150-300	350- 500	RT to 250
9	Process complexity	Low	Low	High	Low
10	Large area scalability	High	High	Low	High
11	Device type	Mainly NMOS	NMOS	CMOS	Mainly PMOS

Table 2-1 summarizes the TFT properties for different semiconducting material classes available for flexible electronics. In the table Green, Yellow and Red color represents most desirable, moderate and least desirable property respectively. With amorphous nature of the film, superior carrier mobility, faster switching, lower leakage current, and stability along with cheaper, less complicated, high throughput, and low temperature processability the oxide semiconductors have emerged as the material system of choice for the flexible applications. Post-transition metals mainly Indium, Gallium, Tin, and Zinc are commonly used for oxide semiconductors. More details about these materials will be provided at the material selection section. In the next section, details about oxide semiconductor and origin of conductivity in oxides as well as charge transport mechanism will be discussed.

2.4 Oxide Semiconductor

2.4.1 Origin of charge transport in the metal oxide semiconductor

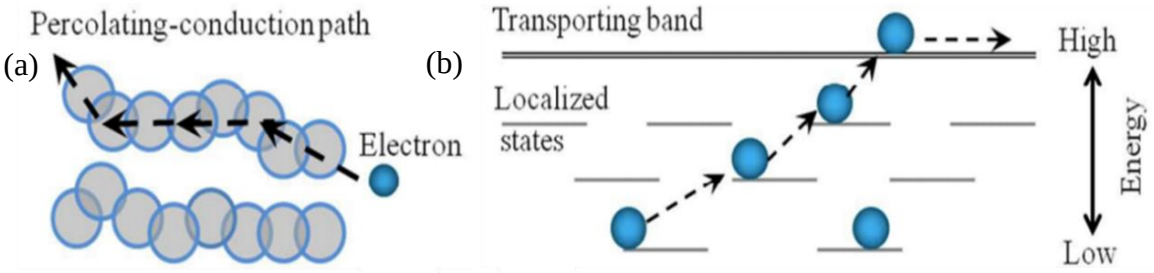

Figure 2-5: (a) Schematic of electron transport mode (b) energy band diagram in an amorphous oxide semiconductor. [37] Reproduced with permission from RSC Publishing.

Electron transport is governed by the hopping conduction mechanism between neighboring cations (**Figure 2-5** (a) [37]). Electrons jump to neighboring localized states, along a percolating electron path and increase its energy level until it reaches the conduction band (**Figure 2-5** (b) [37]). Despite an amorphous structure, metal oxide channel layers can boast excellent mobility compared to amorphous Si-based channel layers because of its electronic structure. In amorphous Si semiconductors, the covalent bonds consist of sp^3 or p orbitals (**Figure 2-6** (a) [2]) that have strong spatial directivity [38]. In the amorphous phase, the covalent bonds become strained, resulting in the formation of deep and high-density localized states between the conduction and valence band, this extends the percolating conduction path needed for the electron to reach the conduction band, causing carrier trapping, and hence, deteriorating mobility [38]. On the other hand, amorphous metal oxides consist of metal s orbitals, which are spherically extended. Crucially, their overlaps with neighboring metal s orbitals (**Figure 2-6** (b) [2]) are mostly unaffected by the disordered amorphous structure[39]. Thus, there is little change to the percolating conduction path, allowing metal oxide semiconductors to retain high mobility, even in the amorphous phase.

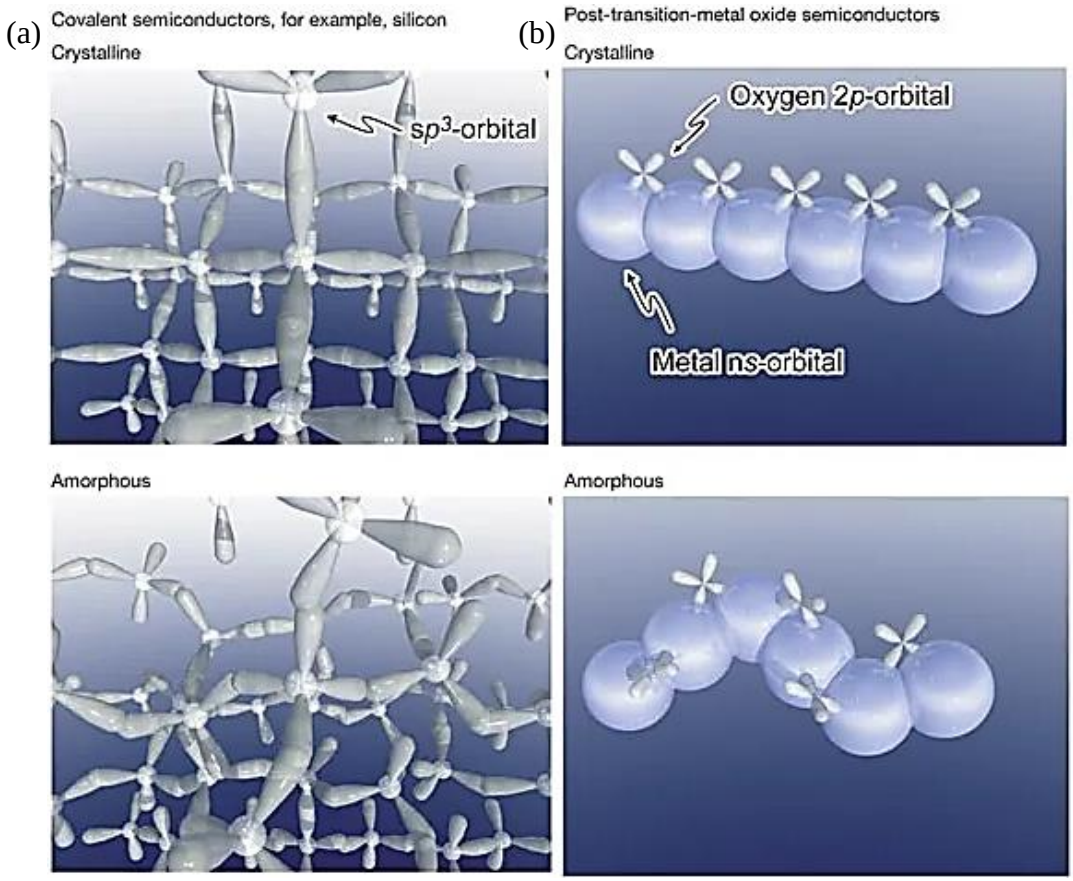

Figure 2-6: (a) Carrier transport paths of covalent Si bonds with strongly directive sp3 orbitals, hence structural randomness significantly degrades the magnitude of bond overlap, hence the carrier mobility as well (b) amorphous oxide semiconductors composed of post-transition-metal cations. Spheres denote metal s orbitals. The contribution of oxygen 2p orbitals is small. The direct overlap between neighbouring metal s orbitals is rather considerable and is not significantly affected even in an amorphous structure. [2] Reproduced with permission from Springer Nature.

2.4.2 Origin of charge carriers in metal oxide semiconductor: oxygen vacancies

In metal oxides, there are various types of traps present. Most essential defects at the surface of an oxide contains anion-cation vacancies, hydroxyl group, impurity atoms, oxygen radical, shallow and deep electron traps.[40] Oxygen vacancies and other defects can completely change the characteristics of the material. For example, MgO single crystal does not react with carbon monoxide, whereas polycrystalline form reacts with it.[41], [42]

In metal oxide TFTs, charge carriers originate from the formation of oxygen vacancies in the channel layer. The creation of these vacancies is governed by the following defect reaction equation [43]:

$$O_o^x \rightarrow \frac{1}{2}O_2(g) + V^{"} + 2e^-$$

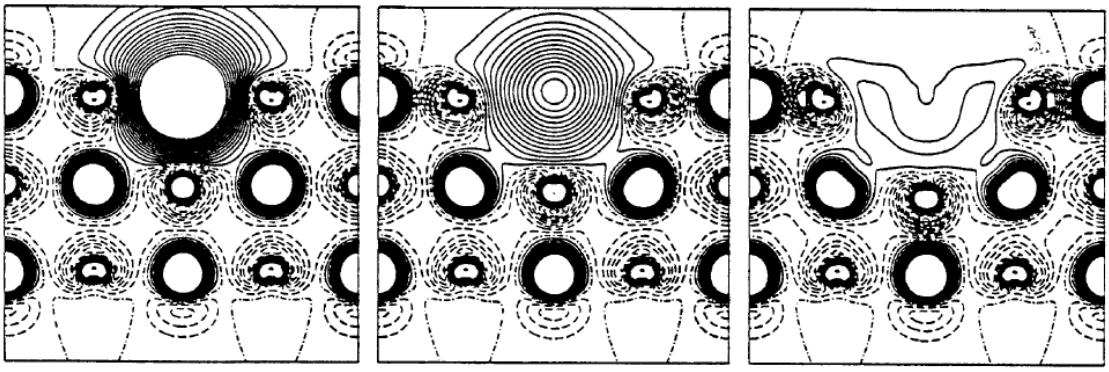

Figure 2-7: Electron density difference plot for V_{ox} at the surface of MgO (a) neutral oxygen vacancy with two trapped electrons (F center) (b) one electron trapped charged oxygen vacancy (F^+ center) (c) no trapped electron charged oxygen vacancy (F^{2+} center). [44] Reproduced with permission from AIP Publishing.

From the metal oxide matrix in **Figure 2-7**, it can be seen that a missing O atom creates two trapped electrons localized in the cavity. The creation of one oxygen vacancy contributes two electrons. Madelung potential of the highly ionic crystal is responsible for the localization of electrons.[44] Hence, instead of oxygen atoms, two electrons are positioned and this minimizes the energy loss in the formation of oxygen vacancy allowing only a very small structural relaxation.[40] Hence it is shown that one oxygen vacancy can accept two electrons. These neutral oxygen vacancies act as dormant deep trap states and get converted to shallow donors once an excitation is applied. The **Figure 2-8** shows the illumination effect on oxygen vacancy defect states, which resulted in persistent conductivity after removal of illumination stress, freed electrons being responsible for it. [45]

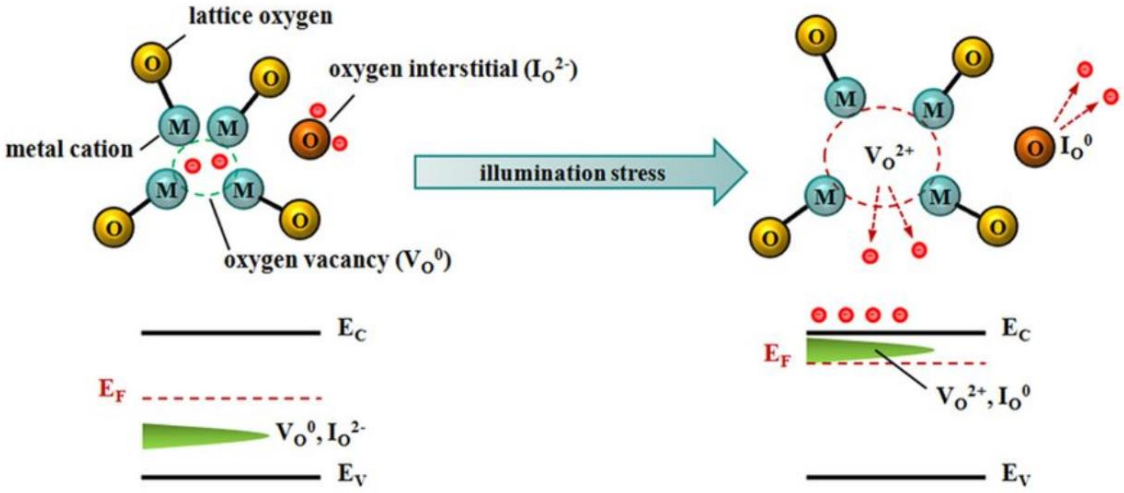

Figure 2-8: Illustration of oxygen defect ionization (ODI) to explain the increased energy level of the ionized oxygen defect states under illumination stress. [45] Reproduced with permission from Springer Nature.

Another example of defect creation in oxide such as IGZO can be seen from the schematic of the subgap DOS model illustrated in **Figure 2-9**. A Gaussian-distributed donor-like state located near the CBM can be attributed to oxygen vacancies (Vo) formation. The energy levels of Vo are generated in or near the CBM, allowing the Vo to act as a shallow donor. Solid curves within bandgap represent the exponentially-distributed band tail states, while the dashed curve near the conduction band gap represents the Gaussian-distributed donor-like oxygen vacancy states.[46]

It can be accepted that both deep state oxygen vacancies and shallow oxygen vacancies can take part in the conduction after sufficient energy is applied. From this section, it can be concluded that oxygen vacancies are a critical factor affecting the device attributes. Hence, it is essential to review the techniques to modulate these oxygen vacancies. The following section covers conventional approaches used to manipulate oxygen vacancies, many of which are not suitable for flexible substrates and does not allow localized manipulation of oxygen vacancies, which is important for new applications such as neuromorphic electronics.

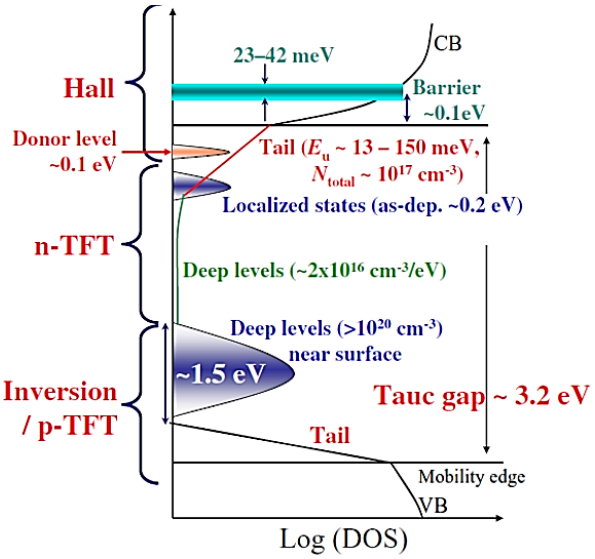

Figure 2-9: Proposed DOS model for a-IGZO. [46] Reproduced with permission from IOPscience.

2.4.3 Material selection for oxide semiconductor

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

Figure 2-10: Periodic table portion for selecting amorphous metal oxide semiconductor cation. Color coding: blue- most common cations employed in AMOS design, red- toxic; brown- p-type cations; orange- high cost cations; black- less investigated. [31] Reproduced with permission from Elsevier.

There are many metal oxide semiconductor trials done over the years and the most common are In, Ga, Zn, Sn. Hosono et al. promoted a selection of metal cation having a large ionic radius, spherical symmetric s-orbitals, from some specific elements from the periodic table (**Figure 2-10**). [47]

Table 2-2: Summary of literature related to flexible oxide TFT transistors

sr.no	Material	Technique	(Tdep./Tpost.)/(C)	Substrate	Dielectric	μ ($cm^2V^{-1}s^{-1}$)	On/off	Ref
1	GNS/IGZO	spin-coating	–/500	thin glass	Ta2O5	23.8	10^6	[48]
2	IGZO	PLD	RT/–	PET	parylene	3.2	10^7	[49]
3	IGZO	spin-coating	RT/350	PI	Al_2O_3	84.4	10^5	[50]
4	IGZO	spin-coating	–/$PN_2$54 nm	PI	Al_2O_3	5.41	10^8	[51]
5	IGZO	spin-coating	–/$PN_2$54 nm	PI	ZAO	11	10^9	[52]
6	IGZO	sputtering	–/$PN_2$54 nm	PAR	Al_2O_3	7	10^8	[53]
7	IGZO	sputtering	–/160	PEN	Al_2O_3	11.2	10^9	[54]
8	IGZO	sputtering	150/150	PEN	Al_2O_3	12.87	10^9	[55]
9	IGZO	sputtering	RT/180	PEN	Al_2O_3	15.5	10^9	[56]
10	IGZO	sputtering	RT/250	PI	Al_2O_3	14.88	10^8	[57]
11	IGZO	sputtering	RT/–	PI	Al_2O_3	17	10^5	[13]
12	IGZO	sputtering	RT/–	PI	Al_2O_3/SiO_2	4.93	5	[58]
13	IGZO	sputtering	RT/110	PET	c-PVP	10.2	10^6	[59]
14	IGZO	sputtering	RT/200	PI	HfLaO	22.1	10^5	[60]
15	IGZO	sputtering	RT/–	PEN	nanocomposite	5.13	10^5	[61]
16	IGZO	sputtering	RT/200	PDMS	P(VDF-TrFE)	21	10^7	[62]
17	IGZO	sputtering	RT/200	PDMS	P(VDF-TrFE)	0.35	10^4	[63]
18	IGZO	sputtering	RT/–	PEN	PVP	0.43	10^5	[64]
19	IGZO	sputtering	RT/–	PI	PVP	3.6	10^4	[65]
20	IGZO	sputtering	–/180	PEN	Si3N4	13	10^8	[66]
21	IGZO	sputtering	–/300	thin glass	Si3N4	9.1	10^8	[67]
22	IGZO	sputtering	RT/190	PEN	SiO_2	8	10^7	[68]
23	IGZO	sputtering	200/220	PI	SiO_2	19.6	10^9	[69]
24	IGZO	sputtering	RT/150	PVA	SiO_2/Si3N4	10	10^6	[70]
25	IGZO	sputtering	RT/RT	PC	$SiO_2/TiO_2/SiO_2$	76	10^5	[71]
26	IGZO/IZO	sputtering	40/200	PEN	SiO_2	18	10^9	[72]
27	IZO	SCS	275/–	polyester	Al_2O_3/ZrO_2	3.9/6.2	10^4	[73]
28	IZO	spin-coating	RT/350	PI	K-PIB	4.1	10^5	[74]
29	IZO	spin-coating	RT/280	PI	Zr-Al_2O_3	51	10^4	[75]
30	IZO	sputtering	–/300	PI	Al_2O_3	6.64	10^7	[76]
31	IZO	sputtering	RT/RT	PET	SiO_2	65.8	10^6	[77]
32	IZO:F	spin-coating	RT/200	PEN	Al_2O_3	4.1	10^8	[78]
33	ZITO	PLD	RT/–	PET	v-SAND	110	10^4	[79]
34	ZITO	sputtering	RT/–	polyarylate	Al_2O_3	16.93	10^9	[80]
35	ZITO	sputtering	300/200	PI	SiO_2	32.9	10^9	[81]
36	ZnO	ALD	150/–	PI	Al_2O_3	3.07	10v2	[82]
37	ZnO	hydrothermal	90/100	PET	PMMA	7.53	10^4	[83]
38	ZnO	PEALD	200/–	PI	Al_2O_3	12	10^8	[84]
39	ZnO	printing	–/250	PI	ion-gel	1.67	10^5	[85]
40	ZnO	spin-coating	–/160	PEN	Al_2O_3-ZrO_2	5	10^4	[86]
41	ZnO	spin-coating	–/200	PET	c-PVP	0.09	10^5	[87]
42	ZnO	spin-coating	–/150	PES	hybrid	0.142	10^4	[88]
43	ZnO	spin-coating	–/135	PEN	RSiO1.5	0.07	10^4	[89]
44	ZnO	spin-coating	RT/MW140	PES	SiO_2	0.57	10^3	[90]
45	ZnO	spin-coating	RT/200	PI	SiO_2	0.35	10^6	[91]
46	ZnO	sputtering	RT/RT	PEN	Al_2O_3	11.56	10^8	[92]
47	ZnO	sputtering	–/MW	PES	Al_2O_3	1.5	10^6	[93]
48	ZnO	sputtering	100/–	PET	HfO_2	7.95	10^8	[94]
49	ZnO	sputtering	–/225	PI	HfO_2	1.6	10^6	[95]
50	ZnO	sputtering	RT/350	PDMS	SiO_2	1.3	10^6	[96]
51	ZTO	Inkjet-print	30/300	PI	ZrO_2	0.04	10^3	[97]

Despite sizable on-going research effort for IGZO, In_2O_3, ZnO, ZTO in recent years [17] (**Table 2-2**), it still faces many challenges such as, reduced large area uniformity, threshold voltage shifts and thermal, light and environmental bias stress instabilities.[98], [99] A controlled carrier concentration, defined by oxygen vacancies are an essential characteristic

of a semiconductor, and oxide materials such as ZnO, SnO_2 and In_2O_3 possess very high carrier concentration, making them highly conducting without any post-annealing. [100] However, for a semiconducting amorphous oxide to be used in TFT applications, the carrier concentration should typically be $< 10^{17}$ cm^3 for good switching. [101] In general, mixing two or more metal cations will boost the formation of amorphous films thereby reducing the carrier concentration due to decreased grain boundaries present in polycrystalline samples.[102] However, these type of TFTs require higher annealing temperature, [103] which is not compatible with the thermal budget of flexible substrates. The proposed reasons for instability in oxide semiconductor are s photogenerated hole carriers, creation of oxygen defects, and desorption of oxygen and the effect of adsorbed moisture. [104]–[108] Trapping of hole carriers can be controlled by a suitable dielectric. However, to control the creation of oxygen defects and desorption of oxygen bonding strength dopants can be used. [99] Even in a-IGZO, the metal cation have different functions; In_2O_3 is the mobility enhancer, ZnO is the network former and GaO acts as the carrier suppressor. [38] GaO has better bonding strength than In and Zn quenching the oxygen-related defect creation/desorption. However higher amount of Ga substantially decreases the mobility. Hence suppressor metal ions concentration control is essential.

In conclusion, incorporation of high Lewis acid strength and strong oxygen binder dopants could suppress the formation of shallow oxygen vacancy defects as well as deep oxygen vacancy defects in the active channel layers. [109] **Table 2-3** summarizes some metal ions with high Lewis acid strength and M-O bond strength. According to studies, some primary constraints on choosing the dopants are the following: (i) The M-O bond strength should be higher than matrix metal ion. (ii)The dopant size should be smaller than the matrix host metal ion; else the dopant will act as a defect site. [78] (iii) high Lewis acid strength, as that results in higher mobility by suppressing scattering by oxygen interstitials. [109] (iv) the dopant should be in appropriate amount so as to accurately control the oxygen vacancies without a significant decrease in the mobility.

Table 2-3: Elemental analysis with electronegativity, Lewis acid strength and M-O bond strength. [109]–[113]

Elements	Electronegativity	Lewis acid strength	M-O bond strength (kJ/mol)
In^{3+}	1.445	1.026	320.1
Ga^{3+}	1.562	1.167	353.5
Mg^{2+}	1.208	1.402	363.2
Mn^{7+}	2.573	7.632	402.9
H^{+}	2.271	1.624	427.6
Cr^{6+}	2.29	8.203	429.3
Sb^{5+}	1.763	3.559	434.3
Se^{6+}	2.289	9.508	468.8
As^{5+}	2.035	6.22	481
Ba^{2+}	1.005	1.163	502.9
Al^{3+}	1.499	3.042	511
S^{6+}	2.479	21.362	521.7
Sn^{4+}	1.583	1.617	531.8
Sr^{2+}	1.004	1.417	549.5
Mo^{6+}	2.025	3.667	560.2
Ca^{2+}	1.032	1.593	589.8
P^{5+}	2.131	10.082	599.1
Ge^{4+}	1.799	3.059	659.4
W^{6+}	**2.132**	**3.158**	**672**
Ti^{4+}	1.577	3.064	672.4
Sc^{3+}	1.316	1.697	681.6
Gd^{3+}	1.272	0.788	719
Y^{3+}	1.209	1.465	719.6
Nb^{5+}	1.771	2.581	771.8
Zr^{4+}	1.476	2.043	776.1
La^{3+}	1.212	0.852	799
Ta^{5+}	1.881	1.734	799.1
Si^{4+}	1.769	8.096	799.6
Hf^{4+}	1.568	1.462	801.7
B^{3+}	1.966	10.709	808.8
C^{4+}	2.536	32.917	1076.5

Before discussing further studies on oxygen vacancies, a suitlable metal oxide is first selected. In_2O_3, as a matrix of metal-oxide, was chosen over ZnO as later experiences more instability problems as discussed before. In^{3+} cations also have a larger radius (94pm) compared to Zn^{2+} cation (88pm) [114], along with higher M-O bond dissociation energy for In_2O_3 (360 kJ/mol) than ZnO(284.1 kJ/mol). [112] W was chosen as the suppressant because of it's higher bond dissociation energy (672 kJ/mol) than indium oxide. W also has higher Lewis acid strength (3.158) and smaller size (60pm) than indium ion coupled with lower annealing temperature requirement (<200 ^{o}C) compared to other high M-O bond strength atoms such as carbon which require very high annealing temperature. [114] Also,

unlike ZnO, a-IWO can have a uniform amorphous phase because of tungsten acting as carrier suppressant in In_2O_3 while also promoting the amorphous phase formation. [109]

With lower operational voltages, higher mobility and a better resistance to moisture and acidic environments, indium tungsten oxide (IWO) thin films are promising alternatives to the intensively-researched indium gallium zinc oxide (IGZO) counterparts, justifying their selection as the reference prototypical AMOS system for this study. [25], [115]–[129] Akin to other AMOS, the oxygen stoichiometry-dependent transport properties enable probing of the local electronic structure via techniques that alter the oxygen vacancy concentration in such films.[25] A higher oxygen dissociation energy for W-O (653 kJ/mol) when compared to In-O (360 kJ/mol), Zn-O (284 kJ/mol) and Ga-O (285 kJ/mol), makes a good carrier suppressant and increases the stability of oxide. [130].

2.5 Oxygen vacancies modulation during deposition

For the sputtering technique, the oxygen partial pressure at the time of deposition can be varied in order to modulate the amount of oxygen present in the film. An example of IGZO TFT is shown in **Figure 2-11**. It can be noted that low oxygen content is useful for better-performing devices in terms of mobility near zero threshold voltage, better subthreshold swing and on-off ratio.[131] Variation of oxygen partial pressure also paves the way to control device attributes such as threshold voltage. The film goes from depletion mode to enhancement mode as the oxygen content increases. However, after annealing at 300 ºC the scale of the ability to control reduces due to atomic rearrangements leading to increased grain size as discussed in the previous section.

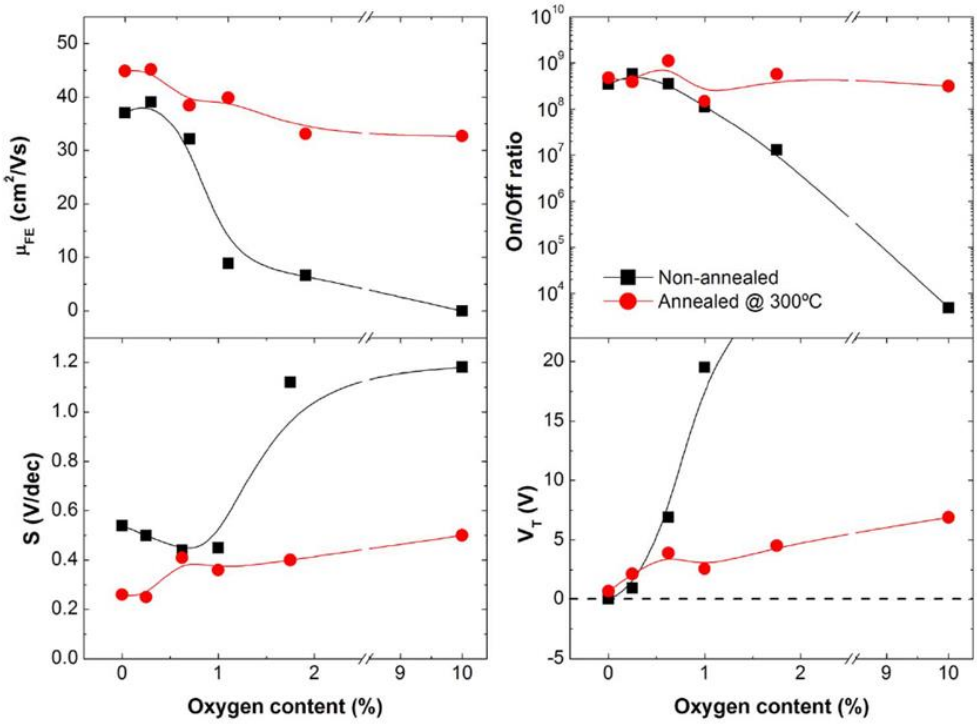

Figure 2-11: Change in field effect mobility, on/off ratio, subthreshold swing, the threshold voltage (from left in a clockwise direction) with respect to oxygen content used at the time of deposition. [131] Reproduced with permission from The Electrochemical Society.

2.6 Post deposition modulation

There are different post-deposition techniques explored in literature which change the oxygen content of the film.

2.6.1 Thermal Annealing

One of the most widely used conventional method is thermal annealing. Some of the significant factors affecting the oxygen content in thermal annealing are the temperature of annealing, annealing time, annealing environment (oxygen rich or oxygen deficient: annealing in water, O_2/O_3, N_2, vacuum), the gas pressure at the time of annealing, rate of annealing. The effect of these parameters on TFT are described briefly as follows.

Effect of Various environment, temperature

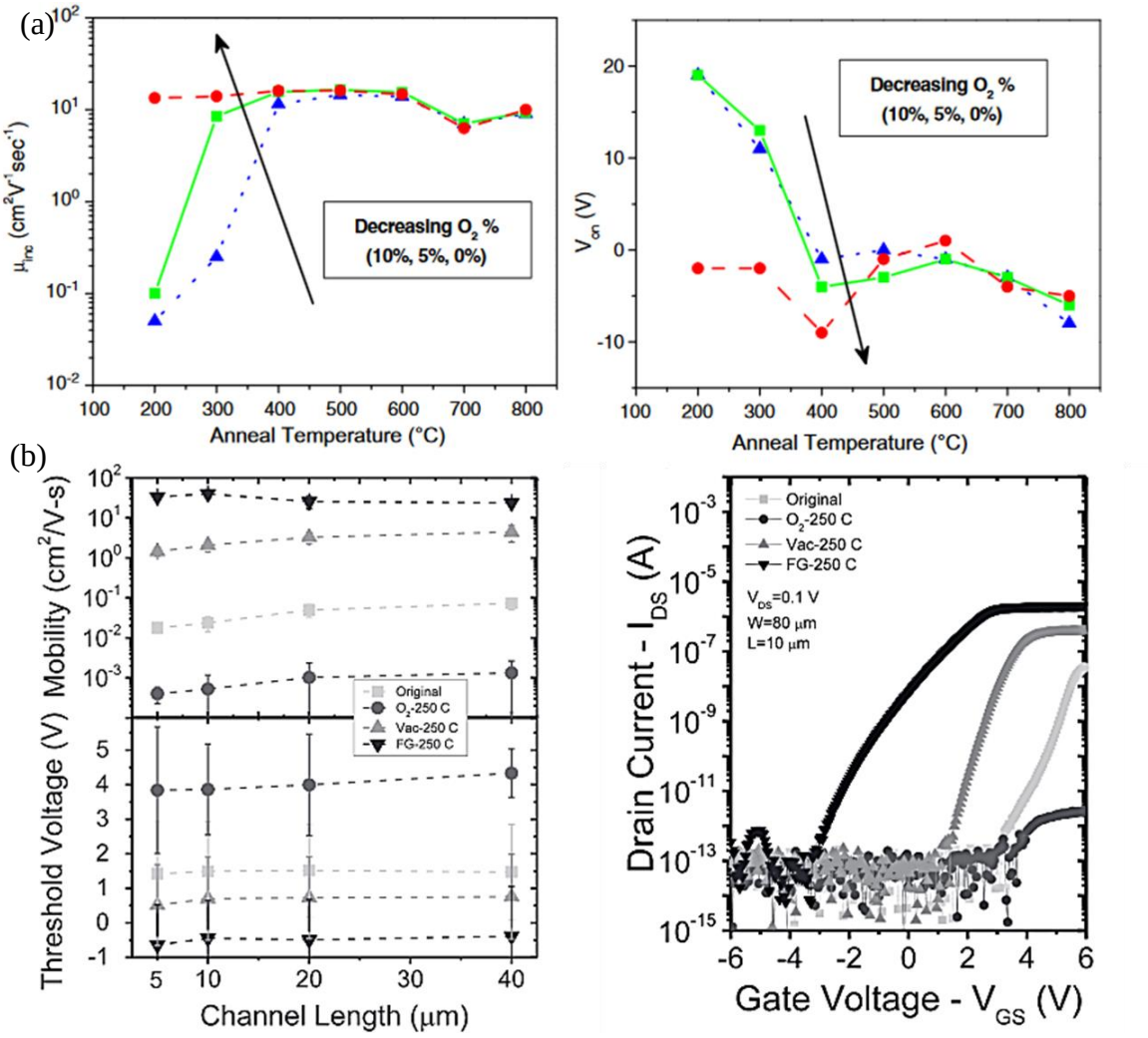

Figure 2-12: (a) Annealing temperature effect on mobility and Von of TFT [132] (b) annealing atmosphere (O_2,vacuum, forming a gas(FG)) effect on flexible IGZO TFT. [133] Reproduced with permission from Elsevier and IOPscience respectively.

As expected, the annealing temperature affects the film formation (**Figure 2-12**(a)), in turn, improving the device quality, with higher temperatures allowing the atoms to locally rearrange themselves, reducing the number of defects. Hence at higher temperature annealing, there is no effect of initial oxygen concentration in the film. But at lower temperatures, the effect is visible substantially in mobility and threshold voltage changes. With higher temperatures, the grain size growth decreases the grain boundary area, which acts as traping centers. These trapping centers are the cause of negative V_{th} shift, as explained in previous sections.

Figure 2-12(b) gives the effect of the annealing atmosphere on the flexible TFT. It can be anticipated that annealing in oxygen will cause more oxygen to be present in the film which positively shifts the threshold voltage.[134] similarly if compare O_2 vs. O_3 atmosphere was compared and O_3 will give more stability to the oxygen-deficient film[135]. Whereas, annealing in a vacuum will cause loss of oxygen, which will result in more oxygen vacancies and negative V_{th} shift. However, in the case of forming gas, the significant shift in V_{th} occurs owing to the presence of hydrogen. It has been reported that the hydrogen in oxide semiconductor film acts as a shallow donor and helps in conduction.[136]–[138] Hence, on annealing in forming gas which contains H_2 and N_2, the hydrogen content in the film increases, thus increasing the n-type doping of oxide semiconductor, while passivating the acceptor dopant and dangling bonds in cation vacancies.[138]

Rapid thermal annealing

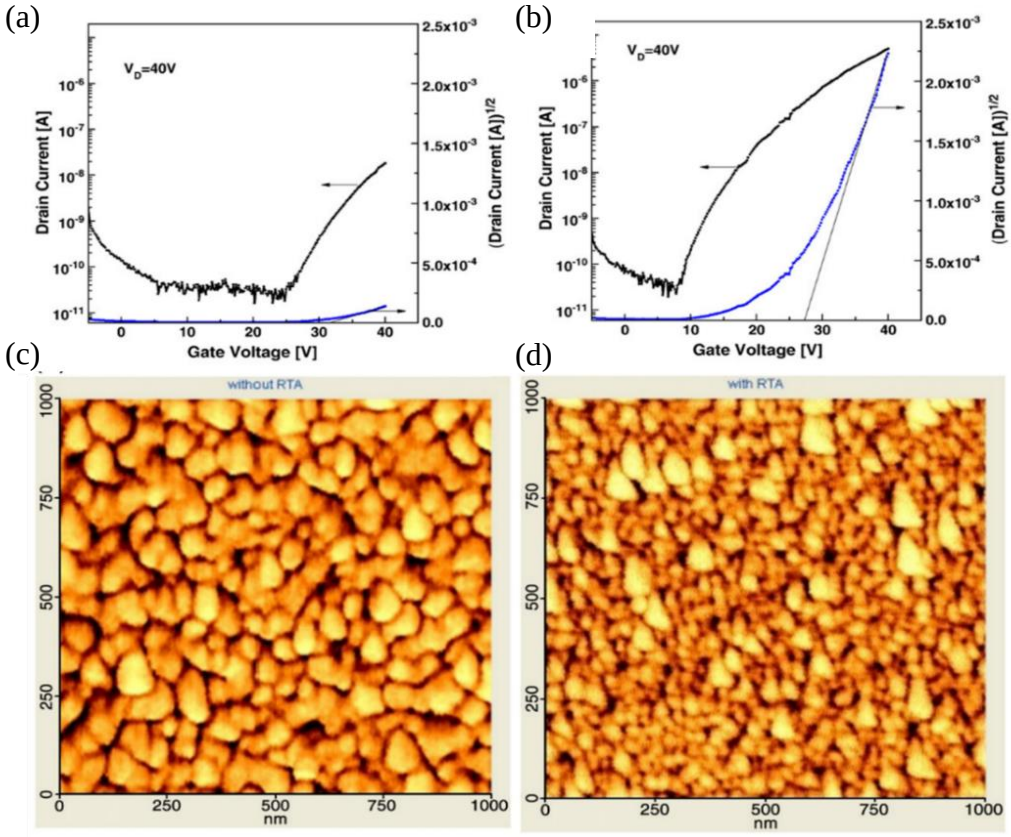

Figure 2-13: Transfer characteristics of (a) unannealed IGZO TFT (b) RTA annealed IGZO sample and AFM image of the film (c) without RTA and (d)with RTA. [139] Reproduced with permission from Elsevier.

Figure 2-13(a) and (b) compares the unannealed IGZO TFT to Rapid thermal annealed TFT. RTA shows incredible improvement in device threshold voltage and mobility. The main reason behind this improvement is the superior film formation. In RTA the atoms rearrange themselves in order to improve the roughness of film as seen from the **Figure 2-13** (c, d).

High-pressure annealing (HPA)

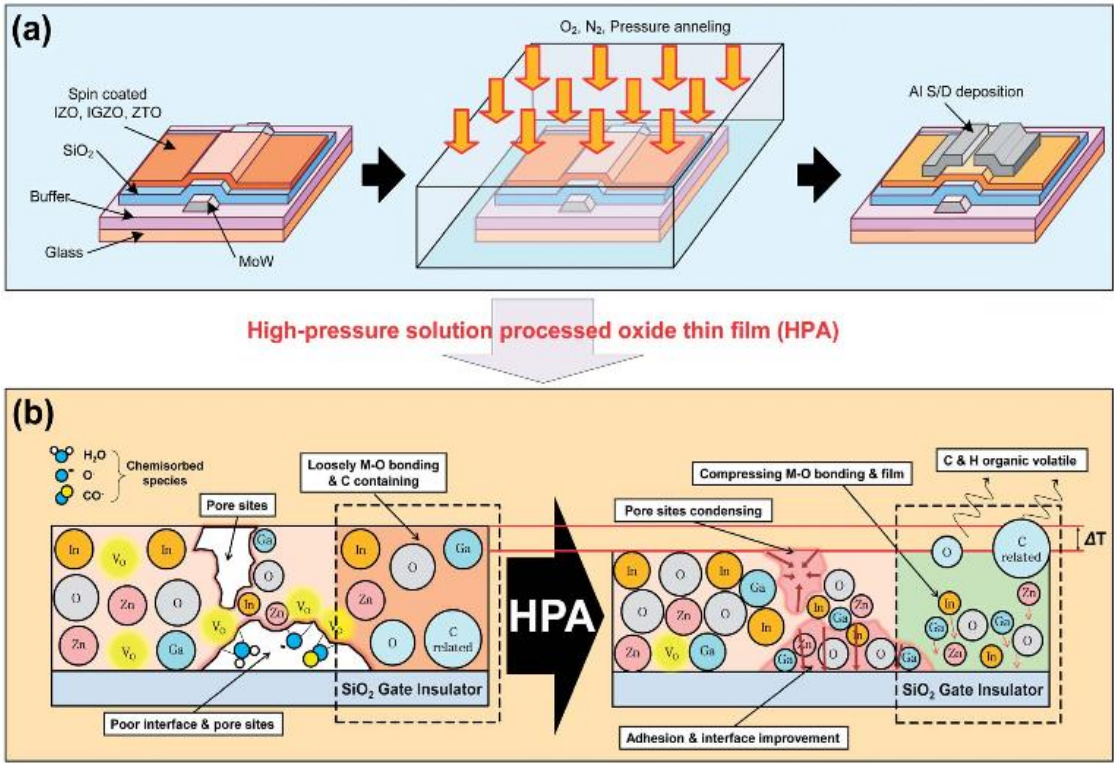

Figure 2-14: (a) Process flow for HPA (b) various processes occurring in HPA improving the film quality. [141] Reproduced with permission from RSC Publishing.

HPA is specifically useful for solution processed transistors as it simultaneously acts on thermal decomposition of elements and compression of film, while lowering annealing temperatures. **Figure 2-14** shows schematic of process flow for HPA and various processes occurring in HPA that are responsible for improving the film quality Thermal decomposition of residual organic chemicals from precursors used for oxide film formation helps reduce charge trapping and other defects. The film thickness is shown to decrease, this reduces all pin holes and improves the charge transport.[141] It is shown that high

oxygen pressure helps the IZO film to form a defect-free film which is visible in XPS data. Hence the V_{on} voltage decrease. However, as the oxygen pressure is increased, the film starts getting more oxygen. This again starts to shift the Von in a positive direction.

Other annealing techniques

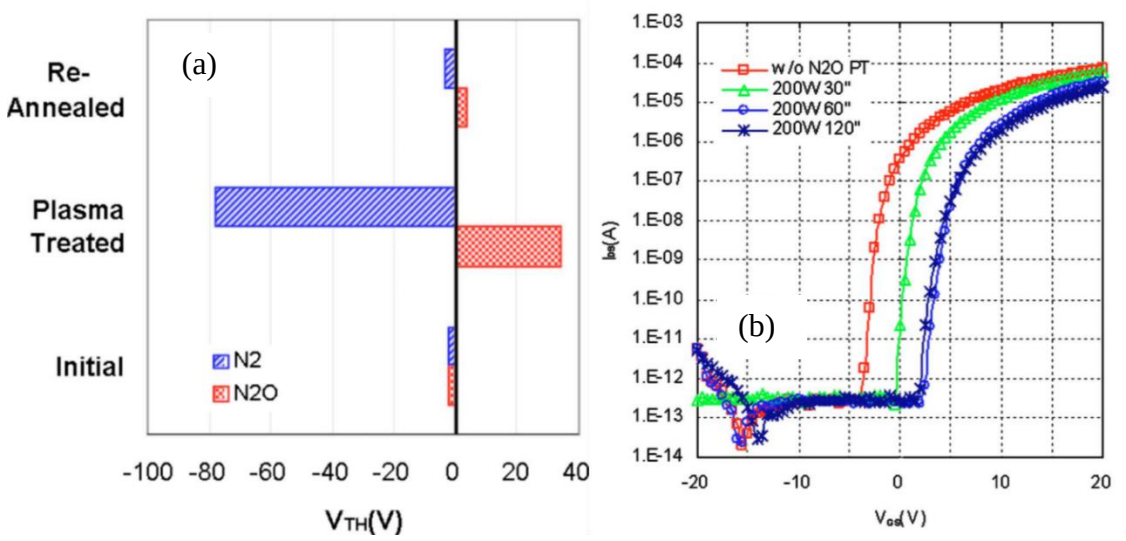

Figure 2-15: (a) Effect of N_2 vs. N_2O plasma on threshold voltage of devices (b) effect of N_2O is observed in a positive shift in V_{on}. [142] Reproduced with permission from IOP Publishing.

Various other annealing techniques such as Plasma annealing, UV photo-annealing, LASER annealing, microwave annealing etc., have also been reported. The effect of plasma annealing is demonstrated in **Figure 2-15** (a,b). In this research IGZO TFTs exposed to N_2 and N_2O plasma are compared. Acceptor like states originating from oxygen adsorbed on the IGZO back channel captures the electrons and shifts the threshold voltage to positive. Whereas nitrogen exposure creates oxygen vacancies, responsible for the negative shift in V_{th}. By performing plasma treatment in different atmosphere either enhancement or depletion mode TFT can be achieved.

Recently UV photo-annealing has been successfully used for activating solution processed TFT.[143] In this study (refer to **Figure 2-16**), UV annealing resulted in higher M-O-M bond, better removal of precursor impurities and transformation oxygen vacancies to act as shallow donors, demonstrated by Urbach studies as well.

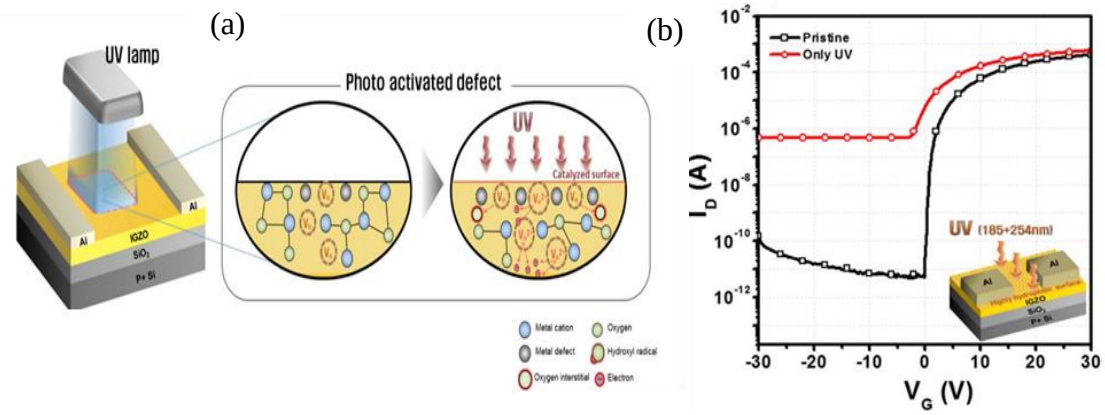

Figure 2-16: (a) Mechanism for photoactivated defects (b) increase in background charge carriers. [144] Reproduced with permission from Springer Nature.

However, in another study[144] , extended UV exposure created extra photo-activated defects in standard IGZO film, resulting in increased background carrier concentration, deteriorating the TFT attributes such as on-off ratio. There are also report of use of microwave energy of 5.8GHz for annealing.[145] It was noted that the threshold voltage stability of devices improved with the increase in exposure time and power. Also, the stability obtained was shown to be superior to samples annealed at 450 ^{o}C in N_2 atmosphere. The XPS spectra denoted in **Figure 2-17** shows that the M-O-M peak (A) improves and O_2^- ion peak is decreased owing to the localized annealing. The improved V_{th} stability indicates that the trap density has decreased which can be related to O_2^- peak. The selective heating avoids potential damage to materials near IGZO. [145] LASER annealing has also been shown to improve the crystallinity in IGZO sample. [146] It did improve the mobility of the device but did no V_{th} modulation was observed. Hence the use of this technique is limited, and it is also expensive due to usage of LASER.

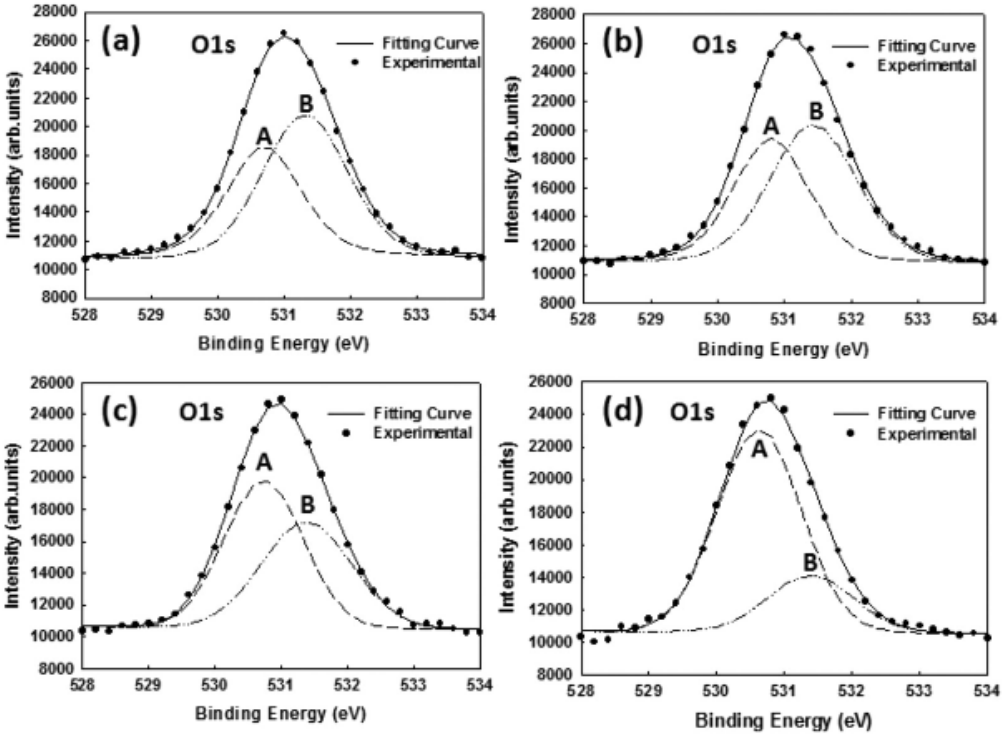

Figure 2-17: XPS analysis of O1s spectra after microwave annealing for treatment (a) 100s @600W (b) 300s @600W (c)600 s @600W (d) 100s @1200W. [145] Reproduced with permission from AIP Publishing.

2.6.2 Approaches to tuning electronic energy levels of oxide semiconductor through postprocessing modifications

The conventional approaches to modulate the attributes of TFT mostly focused on dry and physical techniques of annealing. The non-conventional approaches mainly focus on the chemical aspect and thermodynamics of the film in order to attain more tunability and spatial control at lower temperature or for activation without temperature.

Overlayers exploiting the Ellingham diagram

For TFTs, the effect of the environment on the channel layer can be detrimental to its electrical performance. Both oxygen and water vapor have the capacity to affect a device's performance. Adsorbed oxygen on the semiconducting layer would reduce oxygen

vacancies and thus reduce the number of charge carriers, causing a positive shift in V_{th} [38], [147]. While, adsorbed moisture at the back surface of the channel forms H_2O^+, which acts as an electron donor [148]. This reaction equation is as follows:

$$H_2O = H_2O^+ + e^- \text{.....eq. (2.2)}$$

With more electrons in the channel, V_{th} would be negatively shifted. These two effects highlight the importance of depositing a passivation layer on top of the semiconducting layer, to reduce the extent of oxygen/moisture adsorption. Materials used as passivation layers need to have excellent gas-barrier properties to reduce the environmental impact on device performance, as along with other properties, such as mechanical strength, chemical stability, and optical transparency so that the final application of the TFT is not compromised.[149] Y. Lin et al. researched various capping layers, including Al_2O_3, HfO_2, ZrO_2 ,TiO_2, AHO (Al_2O_3-HfO_2 stack) and ATO (Al_2O_3, TiO_2 stack). [149] J. Wu. Et Al. investigated four different oxides (SiO_2, Al_2O_3, Y_2O_3 & TiO_2 , all 100 nm thickness) as possible passivation layers in TFTs.[150] It was concluded that Al_2O_3 performed the best. [150] It yielded the best electrical properties (μ_{FE} = 5.26 $cm^2/V.s$) and possess excellent optical properties as well, which is critical for display applications. The excellent electrical properties of the Al_2O_3 – passivated TFT were attributed to the low roughness of the Al_2O_3 layer. [150]

Crucially, Al_2O_3 is also an excellent barrier material for preventing water and oxygen from penetrating. [151] However, a significant downside of Al_2O_3 was the relatively long deposition time, [150], which makes it less relevant to the industry. To remedy this, depositing a thinner layer of Al_2O_3 might be the way to go. To that end, H.Ning Et. Al. showed that an ultrathin (~3.5 nm) sputter deposited Al_2O_3 is capable of exhibiting excellent electrical properties as well, with μ_{sat} = 15.3 $cm^2/V.s$. [152]. It has been shown at many places that the TFT after capping undergo a negative shift [152]. These peculiar effects were pinned mostly on the damage caused by the plasma during deposition [150] and precursor reaction with oxide[149] for ALD based systems. However, similar behaviors were observed for sputtered samples as well. It has been reported that there is a

formation of the metallic layer at the interface of semiconducting oxide and more oxygen-rich layer at the capping oxide layer. [153] The same phenomena were observed in another study, including indium and europium monoxide, where the author noted that there is a formation of metallic indium phase. [154] All these studies concluded that the oxygen ion movement was responsible for the device modification. This phenomenon has been thermodynamically thoroughly studied by meteorologist for the extraction of a metal from ore, in various carbothermal reactions. [155], [156] These studies heavily depend on the Ellingham diagram for oxides [155], [156] and Ellingham-Richardson-Jeffes diagrams for nitride based reactions. [157] These diagrams govern the oxidation and reduction of oxide.

Ellingham diagram are plots of Gibbs free standard energy of formation against temperature, pressure, (CO/CO_2, H_2/H_2O) equilibrium Gas mixtures. An example of the Ellingham diagram is shown in **Figure 2-18**. In this diagram, the stability of oxide increases from top to bottom. These diagrams were first constructed by Harold Ellingham in 1944. [158] The diagram is used in metrology to evaluate ease in the reduction of metal oxide/sulfide/nitrides for extraction of metals from ore. Ellingham diagram depends on the Gibbs free energy change ($\Delta G = \Delta H - T\Delta S$, where ΔH and ΔS is enthalpy and entropy change respectively.) which tells how thermodynamically feasible a particular reaction will be. Few observations can be made from the diagram such as, the slope of lines in the diagram is proportional to ΔS. Most crucial observation for our work is that the oxide present below is thermodynamically more stable, hence if two metals are compared at a given temperature, the metal oxide with lower Gibbs free energy will reduce the metal oxide with higher Gibbs free energy. Hence most stable oxides which are Al_2O_3, CaO, MgO will reduce the oxides above. And oxides present on top such as CuO, Ag_2O, etc can oxidize the oxides positioned below in the diagram. Using this technique, fine tuning of TFT attributes such as threshold voltage to alter TFT working from enhancement mode to depletion mode by controlled oxidation and reduction can be achieved. The device can also be activated by increasing charge carrier concentration, which will occur due to the metal oxide reduction.

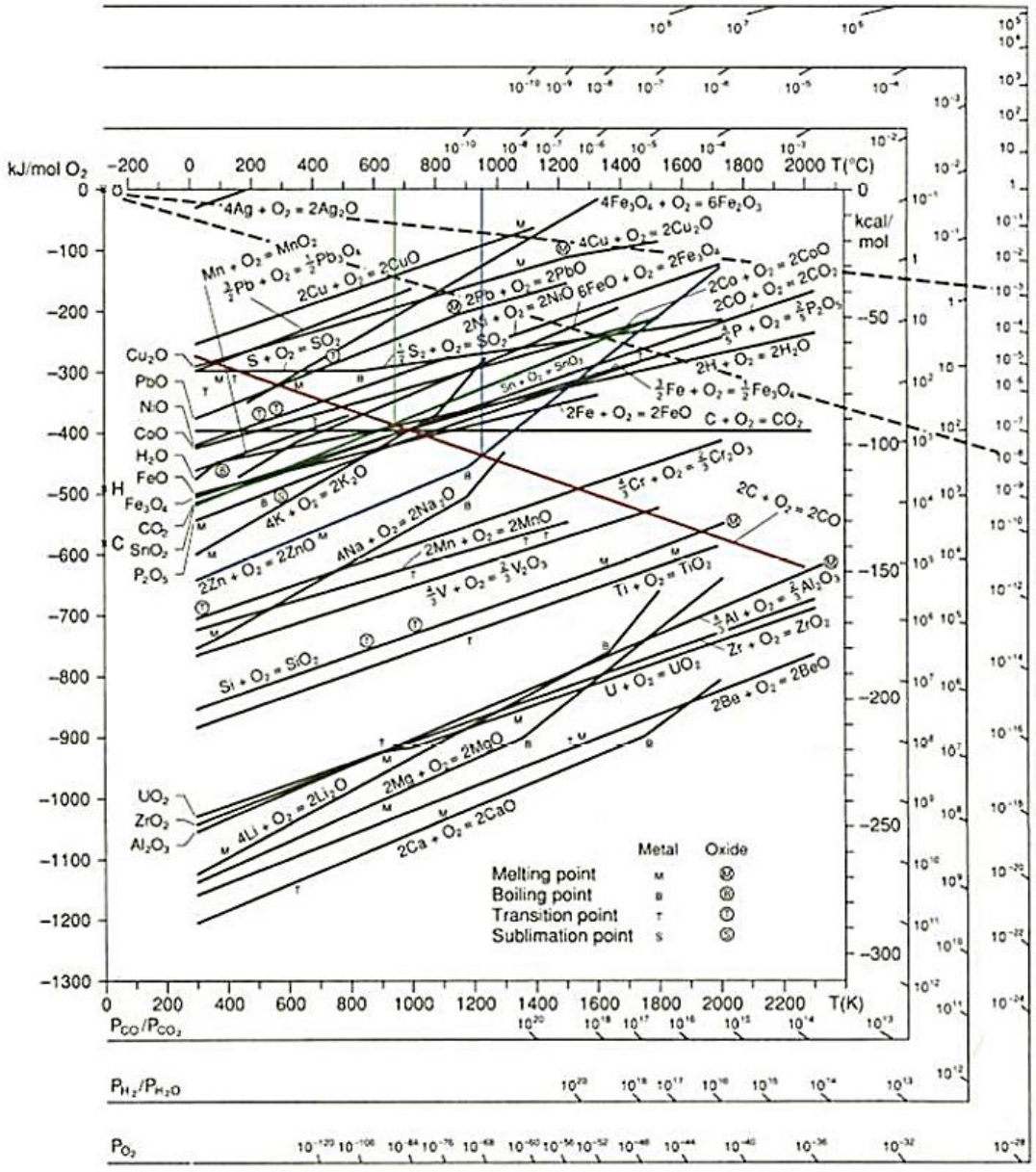

Figure 2-18: Ellingham diagram for metals with their free energy of formation of metal oxides with respect to temperature, oxygen partial pressure. [156] Reproduced with permission from Springer.

The reduction mechanism can be explained by a simple example. In the Ellingham diagram, In_2O_3 is placed above CO.[159] Hence, CO can be used to create reducing environment for In_2O_3. The reaction will occur as follows,

For carbon monoxide: $In_2O_3 + 3CO\ (g) = 2In + 3CO_2\ (g)$.... eq (2.3)

The diagram also shows that an oxide reduction by another oxide placed below in Ellingham diagram is valid for all temperatures. Hence this phenomenon can also be used to modulate oxygen vacancies without heating the substrate and will thus prove to be very useful for fabricating devices on a flexible substrate.

Organic surface modification of Oxide semiconductor

Researchers have used various chemical and physical treatments on organic devices in order to improve contact resistance between organic film and electrode. [160], [161] Such treatments helped to improve weak charge injection, a factor which severely limits the OFET performance. [162] Therefore, the contact engineering for improvement towards ohmic contact became an important area of research in organic semiconductor devices such as TFT's [160], LED's [161], [163] and solar cells [164]–[168]. However, the exploration of these surface modification techniques for oxide semiconductor TFT manipulation is minimal. [169], [170] This section will review the different surface modification techniques which are responsible for some electrical characteristics modifications in organic semiconductors. **Figure 2-19** gives an illustration of such mechanisms responsible for charge transfer. [171]

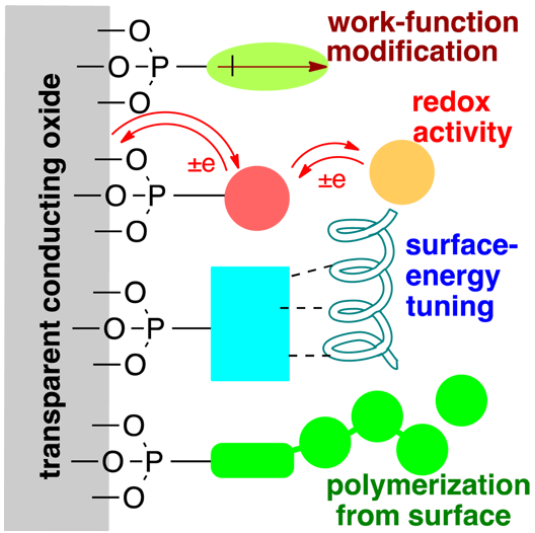

Figure 2-19: Different mechanism responsible for charge carrier concentration. [171] Reproduced with permission from ACS Publications.

The contact engineering of metal or transparent conducting oxide is typically achieved through alteration of work function, modulating surface energies, creating an internal electric field (dipole creation) to drive charge carriers to drift to the surface quickly or/and through charge transfer kinetics (surface dopant mediated charge transfer).[171]–[173] Such surface modifications are achievable through physical and chemical surface treatments. The physical treatments such as surface oxidation using Plasma etching, UV-ozone treatment, are some such examples of dry physical treatments as reviewed in earlier sections. The chemical treatments include surface treatments using organic self-assembled monolayers such as Silanes,[163] Thiols,[174] Carboxylic acids and Phosphonic acids[161] etc., wet inorganic treatments such as acids, bases and oxidants, viologen[118], *TPPO*[175] other organic layers capable of creating dipoles or surface doping such as PEI (polyethyleneimine) and PEIE (PolyEthylenImine-Ethoxylated),[176]–[178] PEDOT:PSS (poly(3,4-ethylene dioxythiophene) polystyrene sulfonate), etc., and some redox active molecules[179].

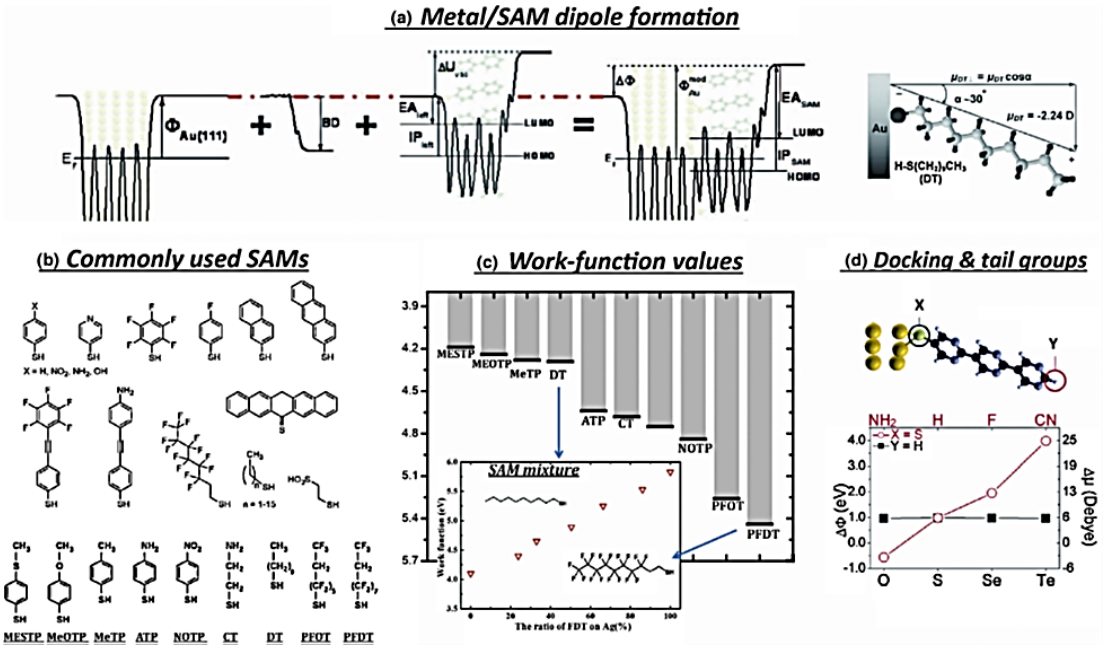

Figure 2-20: SAM modification of injection barriers (a) metal/SAM dipole formation (b) examples of some SAM (c) work function tuning using different SAM (d) effect of different docking and tail group on work function. [160] Reproduced with permission from Elsevier.

Different SAM modifications are described in **Figure 2-20**. The figure reviews the dipole formation, effect of docking and tail group, different SAM commonly used, and work function modulation depending on the surface modification group chosen. It can be noted that the fluorinated SAM changes the work function to a significant value, whereas small chain methyl group tailed SAM has smaller work function.

Electric field-based oxygen vacancies variation

The use of electric field effect for modulation of semiconductor has attracted tremendous interest, since the demonstrations of the insulator to superconductor phase transition with high charge carrier densities of the order of 10^{14} cm^{-2}, [180]–[182]. The extremely high electric field required is obtained through a capacitively coupled gate bias of an electrical double layer (EDL) transistor, which uses an electrolyte as the gate dielectric [181], [183], [184]. Use of electrolytes such as ionic liquids[185], [186] and polymer containing supporting salts[187], [188] have been reported. The electrolyte generates an EDL in the order of angstroms to 1 nm at the IL/solid interface, generating an extremely high electric field of ~ 50 MV/mm[18] . These large electrostatic fields have been shown to be capable of moving ions in/out of solid films, eg.VO_2, $SrTiO_3$ [180], [181]. Electric field-driven creation and manipulation of oxygen vacancies are well studied in deciding the switching characteristics in memristive devices. [184], [189], [190].

Ionic liquid gating has been used for manipulation of a carrier concentration of film leading to unexpected discoveries of the superconducting phase in $KTaO_3$ which was not observed before. EDL transistor devices were fabricated on $KTaO_3$ single crystals with an ionic liquid **Figure 2-21**.[180] A sharp increase in drain also was observed above 2.7 V, Ion/off > $1x10^5$ and a considerable leakage faradaic current as gate leakage current owing to an electrochemical reaction.

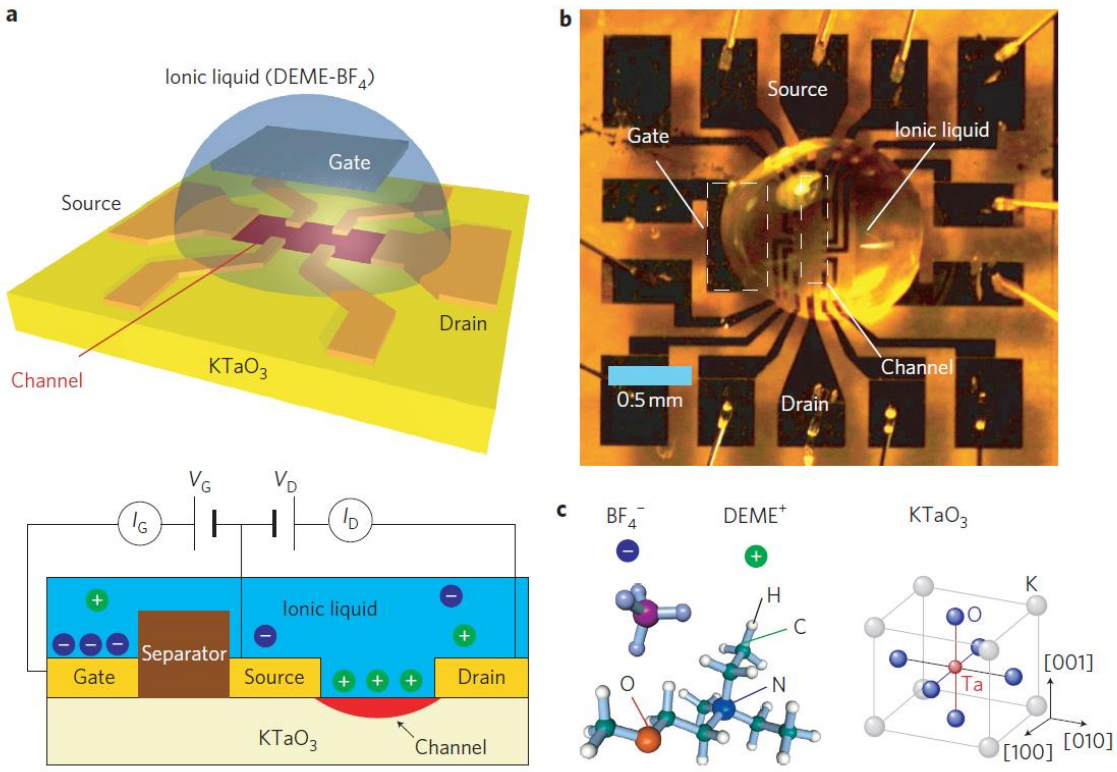

Figure 2-21: Schematics (a) and photograph (b) of device used (c) molecular structure of anion and cation of ionic liquid. [180] Reproduced with permission from Springer Nature.

After biasing ionic gated liquid, Electrostatic carrier doping could induce superconductivity in $KTaO_3$. Superconductivity was not previously observed for this material. The use of extensive electrical double layer helped to achieve a considerable improvement in carrier density compared to regular chemical doping.[180] This research clearly showed that electrostatic carrier doping could lead to new states of matter at the nanoscale. There is a lot of unexplored potential in ionic liquid gating.

2.7 Discussion

From the the literature survey done, it is evident that there is very little work done on athermal activation and manipulation of the oxide semiconductor film. Athermal activation paves the way for flexible and transparent electronics. The controlled manipulation of oxygen vacancies changes the conductance of film in a controlled manner which is of

interest for novel applications such as neuromorphic electronics. The control over enhancement mode and depletion mode have been of interest for a long time in order to realize the logic gates in electronics.

Until now, the majority of the research covererd annealing techniques such as thermal annealing, microwave annealing, rapid thermal annealing, high-pressure annealing, and laser annealing. All these processes have adverse effects on flexible substrates due to the small thermal budget. Apart from that, all of these techniques except for laser annealing are nonselective, i.e., all the TFTs on the substrates are affected by the process. If selective annealing is required a complex number of steps will be required, such as photolithography, to tune the attributes of thin film semiconductor selectively. Selective laser annealing is very expensive and cumbersome process due to the high-power laser.

Hence the need for other novel techniques which can selectively address the conduction of oxide semiconductor arises. The novel techniques which will be explored in this dissertation are mainly chemical treatments rather that physical treatments, which will pave a wave to selectively address individual oxide film conductance for new emerging applications.

The conclusion for the review of novel techniques which will be explored in the dissertation is as follows:

1. Engineering of capping layer using Ellingham diagram:

   As reviewed in previous sections, researchers have been using many different materials for capping layers, such as Al_2O_3, SiO_2, Y_2O_3 HfO_2,ZrO_2 ,TiO_2, AHO(Al_2O_3-HfO_2 stack) and ATO(Al_2O_3, TiO_2 stack) for addressing the issue of stability of oxide semiconductor in air and with higher temperature. It has been consistently noted that the V_{th} of the TFT shifts to negative values after the deposition of these insulating oxides. The effect was always either attributed to the chemical reaction of ALD precursors or damage due to plasma or oxygen ion motions; the phenomenon is not well addressed. The effect is

always suppressed by annealing. However, as discussed in section (2.6.3.1), the occurrence of this effect is not really new. It has been widely used for the extraction of metals from ore. Ellingham diagram is used to define the movement of oxygen, occuring due to Gibbs free energy difference between two oxides. Thermodynamically stable oxide, which is placed at a lower level in the Ellingham diagram, can reduce the oxides placed above in the diagram. Hence, the Ellingham diagrams can be used as a tool in order to oxidize or reduce the oxide semiconductor films selectively. The phenomenon can also be used to decrease the annealing temperature for activating oxide TFT and to alter operation to depletion mode from enhancement mode. This would be very beneficial in flexible electronics.

2. Use of chemicals to oxidize the surface of an oxide semiconductor for TFT applications:

   The chemical route of controlling conduction of semiconductor is to either oxidize or reduce the oxide film. Although hydrogen Peroxide has been long used for surface treatment of oxide semiconductors for photocatalytic reactions, the use of the chemical in oxide TFT is relatively unexplored. Hence, further exploration of H_2O_2 to oxidize the TFT film and measure the optical and electrical parameters of the oxide film is needed.

3. Charge carrier modulation of oxide semiconductor through various surface treatments.

   As discussed in the review, researchers have explored various chemical and physical treatments in organic devices in order to improve contact resistance between organic film and electrode. It helped to improve weak charge injection, a factor which severely affects the OFET, LED, and solar cell performance. As discussed in previous sections, these surface modifications are achievable through physical and chemical surface treatments. The chemical treatments have not been explored in detail for TFT application. The surface modifications using organic self-assembled monolayers such as Silanes, Thiols, Carboxylic acids, Phosphonic acids, etc., other organic layers capable of creating dipoles or surface doping such as PEI (polyethyleneimine), PEIE

(PolyEthylenImine-Ethoxylated), TPPO, etc. can be used to investigate the effect on TFT.

4. Electrostatic field driven modification of oxide semiconductor

As discussed before, inside the electrochemical potential window of ionic liquid, the ions interact electrostatically with the oxide interface without any chemical bonding. So far, ionic liquid electric field modulation is limited to charge modulation and accumulation for ionic liquid TFT. The high electric field of the order of 50 MV/mm present at the interface due to Helmholtz layers can be used to vary the oxygen ions present in the film. This should modify the TFT characteristics of back-gated TFT too. Hence further explorations in order to selectively change the TFT characteristics are needed. More detailed analysis in terms of ambient gas and biasing voltages are also needed in order to achieve controlled modulation of TFT attributes.

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Chapter 3

Experimental Methodology

This chapter explains the rationale behind the fabrication processes and characterization techniques used for inspecting the physical and electrical properties of materials and devices. Basic principles of these techniques with a detailed analysis of the acquired data from these techniques is described. The device fabrication of transistor on both rigid and flexible substrates is described in detail. Then post fabrication treatment protocol used in chapter 5 and 6 are explained. Next, principles of various deposition techniques and protocols used for dissertation are detailed. The details of physical characterization techniques (FESEM, XRD), surface characterization techniques (XPS, FTIR,AFM) and electronic level characterization techniques (UPS, Optical absorption, PESA) used to characterize the deposited film is described in this chapter as well.

3.1 Device Fabrication:

3.1.1 Fabrication of rigid transistors

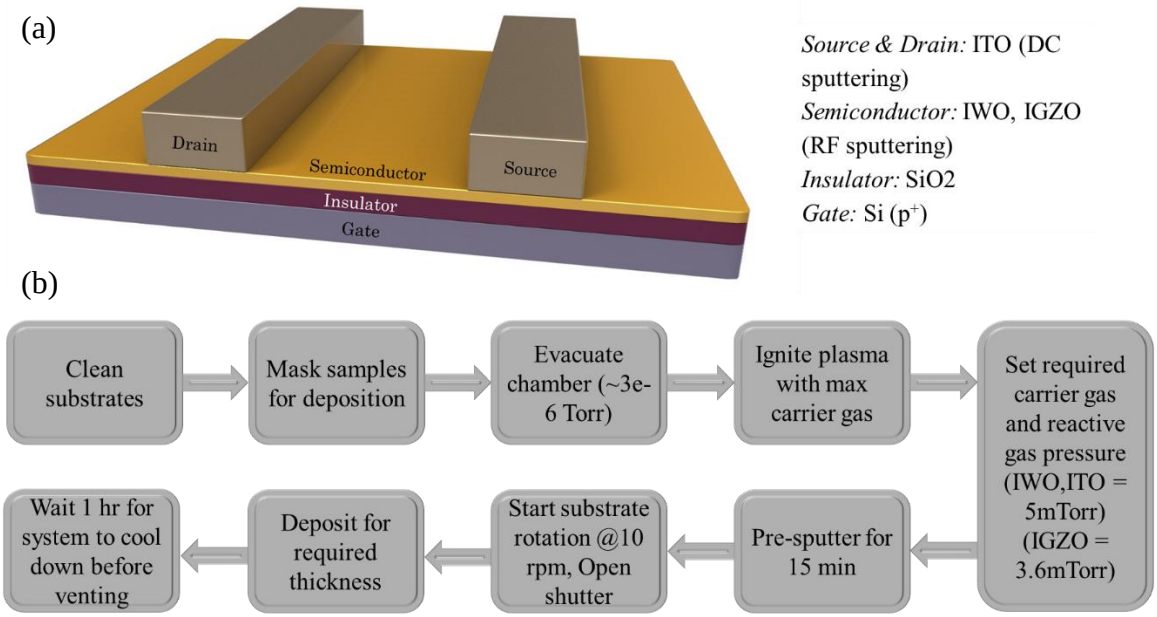


Figure 3-1: (a) Device structure of fabricated TFT (b) Fabrication process workflow.

Figure 3-1 gives a back gated device structure (a) and the workflow (b) used for rigid TFT fabrication. The semiconductor channel and electrodes of TFT were deposited by sputtering through the patterned hard mask. The details of masks are given in appendix information. The highly doped p-type Silicon acted as gate electrode whereas CVD grown SiO_2 acted as the gate insulator. For the study of various processing parameters described in chapter 4, the Si wafers with 300 nm SiO_2 were used and for chapter 5 and chapter 6, the Si wafers with 100 nm SiO_2 were used.

Cleaning Step

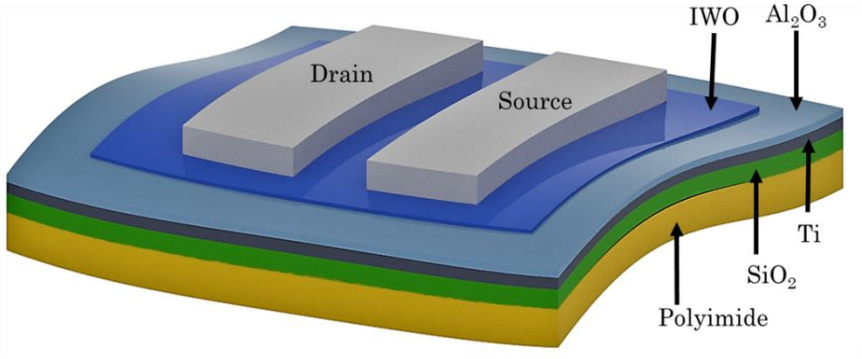
Highly doped p+ Si substrates with SiO_2 were cut into required size to be used as a gate electrode with dielectric. The substrates were ultrasonicated with Acetone, Ethanol, and Deionized Water for 15mins in sequence. Next, they were blow-dried with Nitrogen gas, followed by 30mins of plasma treatment.

Preparation of thin films by reactive r.f. magnetron sputtering

In this dissertation, most of the thin film deposition processes, including the IWO and IGZO channel layer, ITO S/D electrode, Al_2O_3 and SiO_2 capping layer were carried out by the magnetron sputtering machine. Before the deposition process, the chamber was pumped down to the high vacuum condition (background pressure ~ 3×10^{-6} torr) by the combination of the mechanical pump and turbopump. The sputtering system has three guns; one gun is reserved for dc sputtering for ITO. The remaining two guns are used for r.f. sputtering, one for semiconductor and other for the insulator. Each gun is equipped with a permanent magnet to magnetron control the plasma, and with a shutter to mechanically start/stop the deposition process. Each sputtering gun is water-cooled to prevent damage of equipment by overheating. The sample holder can be heated and can be rotated at a constant speed for better deposition uniformity. A DC generator, RF generator, and a matching network (box) are needed to carry out the sputtering process. The size of the target is 2" in diameter. The gas feedthrough consists of argon (Ar, 99.999 %, research-grade), oxygen (O_2, 99.993 %), and nitrogen (N_2, 99.999 %) gases. Each kind of gas has its own mass flow controller (MFC) to control the gas flow rate to the chamber. Therefore, the deposition ambient can be adjusted to three options, pure Ar, mixed Ar/O_2, and mixed Ar/N_2. In this dissertation, the maximum sputtering power used is 100 W. This is because the high-power process may cause the strong ion bombardment effect which can damage the sample surface, while the low power process may decrease the deposition rate and degrade the film quality due to the low energized sputtered atoms. The working pressure during the sputtering process for IWO and ITO was fixed at 5 mTorr, whereas for IGZO it was 3.6 mTorr. The IWO conductive oxide layer was sputtered from an ITO target (In_2O_3:WO_3 = 98:2 wt. %) at 5 mTorr using the pure Ar plasma, and the oxygen flow rate was varied from 1-5 sccm. The IGZO oxide semiconductor film was reactively sputtered from an IGZO target (In:Ga:Zn:O = 1:1:1:4 at%) using 40W RF power at 3.6 mTorr. The ITO conductive oxide layer was sputtered from an ITO target (In_2O_3:SnO_2 = 90:10 wt. %) at 5 mTorr using the pure Ar plasma. Pre-sputtering step of 15 min was also performed every time prior to deposition in order to clean the target surface.

3.1.2 TFT Fabrication on flexible substrate

(a)



(b)

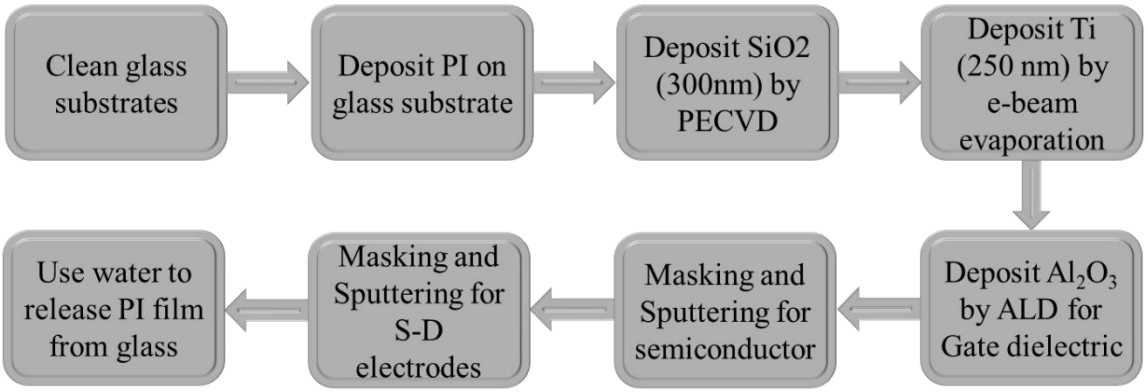


Figure 3-2: (a) Device structure of fabricated flexible TFT (b) Fabrication process workflow.

The flexible device contains various layers (**Figure 3-2:**), which are deposited by different methods. Initially, commercially available polyimide sheet is used as the substrates. However, our experiments with these substrates always failed, mainly because of the high roughness, which created pinholes in the dielectric, and the fabricated devices were always short-circuited with high gate current. Therefore, the polyimide substrates were prepared in house. In order to serve as the carrier substrates for the flexible TFTs, bare glass slides (Si wafer pieces) were cleaned using a procedure similar to that described above, followed by the deposition of PI precursor solution [poly (pyromellitic dianhydride-co-4,4-oxydianiline), amic acid solution] by spin-coating (2000 rpm for 30 s). The substrates were baked on a hot plate with a gradual increase in temperature from 100 to 300 °C, over 2 h (Ramping: 25 ^{o}C per 15 min). The cured PI film could be peeled off from the handle substrate and had a thickness of ~10 μm.

Then, a thick SiO_2 layer (~300 nm) was deposited using PECVD as a buffer layer to account for some of the bending strain and to achieve a smoother film. Ti deposited through e-beam evaporation was used as a gate electrode. For Ti, a higher thickness was chosen (~250 nm) again to act as a buffer for bending strain. 100 nm of Alumina was deposited as a gate dielectric by ALD. Then IWO of 7 nm and ITO electrodes were deposited using r.f. sputtering as described before.

3.2 Post fabrication treatment protocols

1. APTES, DDT, PFDT treatment: Substrates were submerged entirely into the container containing solutions in a nitrogen atmosphere. Solutions were prepared as follows APTES (1:10vol ratio with ethanol and later washed with ethanol), DDT & PFDT (12mM in ethanol solution), Substrates were washed with respective solvents to remove excess or species that are not chemisorbed.

2. PEI: PEI was heated to 100 ^oC in a vacuum chamber for 4 hrs before the solution was prepared (0.4 wt% 2methoxy ethanol). The solution was spin-coated at 4000 rpm for 1 min and annealed at 100 ^oC for 10 min.

3. PEIE: coated at 4000 rpm for 1 min, and heated at 100 ^oC for 10 min.

4. TPPO treatment: Substrates were submerged entirely into the container containing solutions in a nitrogen atmosphere. TPPO Solutions was prepared with a concentration of 1mg/ml in acetonitrile. Substrates were washed with Chlorobenzene to remove excess TPPO, which is not chemisorbed as described by Bao et.al.[1]

5. H_2O_2 treatment: Substrates were submerged entirely into a container containing 30% H_2O_2 kept under refrigeration.

6. Ionic liquid treatment: The ionic liquid 1-Ethyl-3-methylimidazolium bis-(trifluoromethylsulfonyl)imide (EMIM TFSI) was preheated for 3 h at 120 °C in a

vacuum oven to remove traces of moisture. Sample's channel areas were then laminated with ionic liquid for field-driven activation and its associated measurements. To probe the extent of oxygen extraction in the semiconducting channel, all traces of ionic liquid was thoroughly removed from the substrate surface (by ultrasonication with deionized (DI) water, acetone, and isopropyl alcohol, followed by drying with N_2 gas) prior to back-gated FET measurements. The measurements in different ambient were carried out by bleeding Ar, N_2, and dry air, respectively, into the vacuum measurement chamber at a pressure of 30 psi.

3.3 Brief principle and protocol of techniques used for deposition

3.3.1 Sputtering

Several techniques available for the preparation of oxide thin films include spray combustion synthesis [2], pulsed laser deposition [3], spin-coating [4], chemical vapor deposition (CVD) [5], D.C. and R.F. sputtering, etc. [6][7]. Among these, R.F. sputtering is popular, versatile, and suitable because of better process control, high deposition rate, and the possibility of yielding smoother film over a large area. The properties of R.F. sputtered films are determined by parameters such as gaseous atmosphere, target to substrate distance, substrate temperature, R.F. power, working pressure, thickness, and of course, the post-deposition treatment [8]. Sputtering is the process by which species are ejected from materials through positive ion bombardment via momentum transfer. It involves the interaction of the incident energetic (0.5-5 keV) inert positive ions with the solid surface leading to collision cascades and knocking/sputtering of species. After the collision, the solid species overcome the surface binding energy and the escaped matter condenses onto a substrate (held at a distance) as a thin film (**Figure 3-3**) [9].

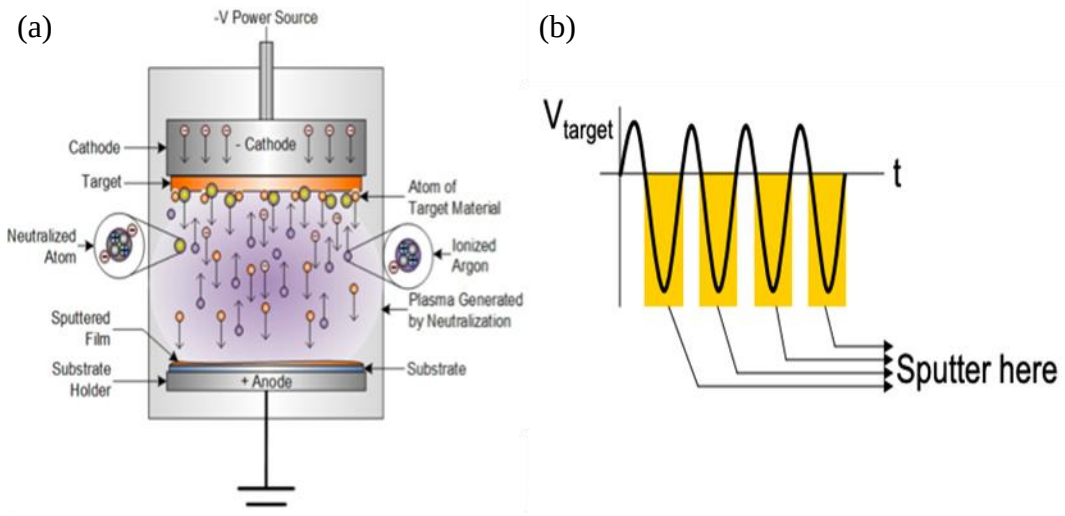


Figure 3-3: (a) Schematic of a Sputtering Process (b) Graph showing switching of polarities in RF Sputtering. [9]

Sputtering utilizes inert gas ions (usually Ar^+) to remove atoms from the source material, known as a sputter target. First, the chamber is evacuated to a vacuum state. Ar gas is then flowed in, and an electric field is applied. The electric field is high enough to extract electrons from the Ar in an ionization reaction: $Ar \rightarrow Ar^+ + e^-$. The combination of gaseous ions and electrons is known as plasma. The Ar^+ ions are accelerated to the negatively charged target where they bombard the source target, creating sputtered source atoms. These sputtered source atoms then travel and deposit on the positively charged substrate. A schematic of this process is shown in **Figure 3-3**a [10]. For the deposition of the semiconducting layer (IWO), Radio- Frequency (RF) sputtering is used. RF sputtering is typically used for depositing materials which are not conductive [11]. If RF sputtering was not used, electrons attracted to the positively charged substrate would inhibit the deposition of the sputtered material. Critically, positively charged ions would remain at the surface of the target, and when there is significant charge build-up, there would be a total cessation of atoms being sputtered from the target. Hence no deposition would occur [11]. In order to solve this, the polarities of the target and the substrate are switched periodically; this allows the electrons and the positively charged ions to be repelled of, which then facilitates the deposition of the sputtered material when the polarities switch back. The process of switching the polarities of the target and substrate is shown in **Figure 3-3**b. The substrate is also rotated to ensure that the film deposited is uniform and conformal.

3.3.2 Plasma-enhanced Chemical Vapour Deposition (PECVD)

Plasma-enhanced chemical vapor deposition (PECVD) is a chemical vapor deposition process used to deposit thin films from a gas state (vapor) to a solid-state on a substrate. Chemical reactions are involved in the process, which occur after the creation of a plasma of the reacting gases. For flexible device fabrication, a 300 nm SiO_2 interlayer was deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the PI film at 200 °C. This film is generally used in order to act as a buffer layer[5] to protect the active semiconducting layer from mechanical strain-induced due to flexing.

3.3.3 Atomic Layer Deposition (ALD)

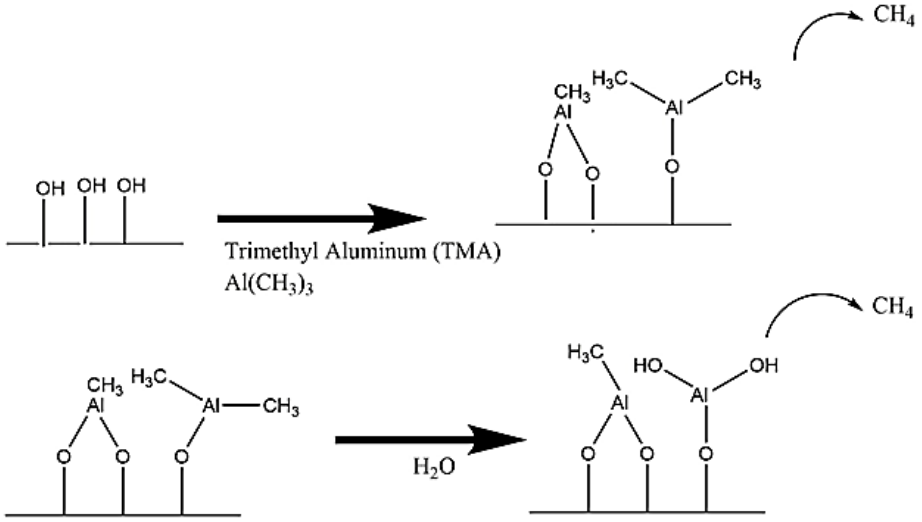


Figure 3-4: Proposed mechanism for Al_2O_3 ALD during the top- TMA reaction; bottom- H_2O reaction to generate hydroxyl group.

ALD is a subclass of CVD which uses a sequential and self-limiting gas-phase chemical reaction on the surface of the substrate. ALD allows high conformability, unprecedented thickness control to angstrom level and atomic level control on composition. With these characteristics, ALD is a powerful tool for deposition of thin films. The exceptional conformability allows ALD to deliver pinhole-free thin films which are really important for the gate dielectric of TFT. Hence, ALD was used as a method to deposit a dielectric layer on e-beam deposited Ti on flexible substrates. **Figure 3-4** displays the layer by layer deposition occurring in ALD. The first pulsed TMA precursor gets reacted with OH groups

present on the surface of substrates. Then the -ch_3 reacts in the next water pulse in the thermal ALD process, making the top layer hydroxyl group ready to react with next TMA pulse. Hence gradually preparing Aluminium oxide, one layer at a time.

The gate dielectric layer of Al_2O_3 (130 nm thick) was deposited by thermal atomic layer deposition (Cambridge Nanotech, Savannah S200) at 150 °C using a trimethylaluminum precursor and H_2O as a reactant. No additional heating/deposition temperature has been used. In order to measure capacitance values, aluminium circular electrodes (100 nm thick) were thermally evaporated on SiO_2 and Al_2O_3 to form capacitor devices with a metal−insulator-metal structure.

3.3.4 E-beam (electron beam) evaporation

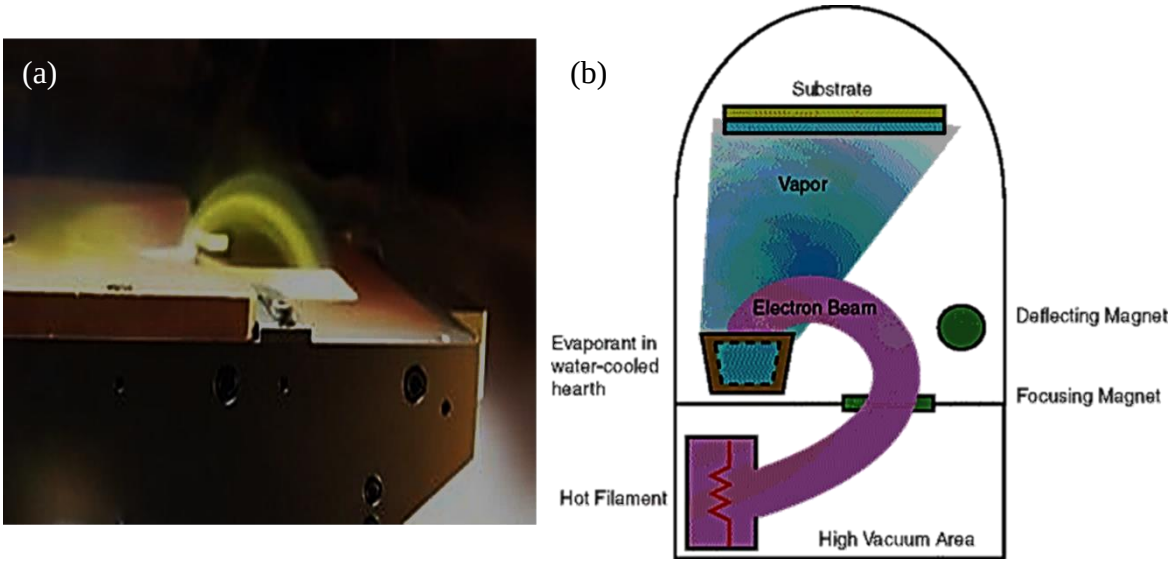


Figure 3-5: (a) Electron beam traveling from filament to the crucible [12] (b) Working principle of e-beam evaporation. [13]

E-beam evaporation is a type of physical vapor deposition. The targeted material kept in the crucible is bombarded with a high energy electron beam emitted from a tungsten filament **Figure 3-5**(a). Deflecting magnets are used to bend the e-beam. The working principle is demonstrated in **Figure 3-5**(b). The high cumulative energy of these electrons converts the material to the gaseous state, which then gets coated on substrates kept on the substrate holder. For flexible device fabrication, a Ti film (250 nm thick) was deposited by

e-beam on top of the SiO_2 interlayer to form the bottom gate contact. Thicker Ti film ensures a pinhole-free, strain buffering layer for device fabrication

3.3.5 Thermal evaporation

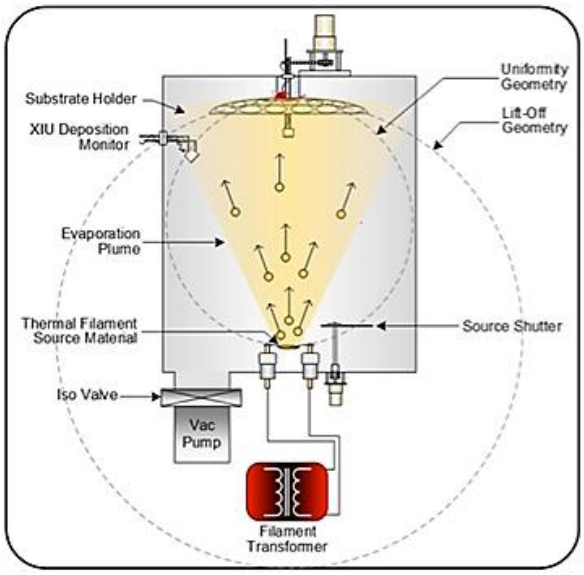


Figure 3-6: Schematic of the thermal evaporation process. [13]

Thermal evaporation is another PVD. This method involves heating a solid (usually metal) in vacuum by using joule heating to produce a small vapor pressure inside vacuum generating vapor cloud of the material. This vapor travels through the chamber and gets deposited on the substrates kept on substrate holders. **Figure 3-6** shows a schematic of the thermal evaporation process. For chapter 4, capping layers of Ca and Al as electrodes were deposited by the thermal evaporator.

3.4 TFT parameters extraction

The transfer and output characteristic of the devices were measured by a semiconductor parameter analyzer (Keithley 4200) in the dark at room temperature (RT). In the output characteristic (I_{DS}-V_{DS}), the V_{DS} was conventionally swept from 0 V to 30 V at the step V_{GS} (step = 5 V) to measure the corresponding I_{DS}. In the transfer characteristic (I_{DS}-V_{GS}), to ensure the devices operated in the linear and saturation regime, the V_{GS} was

conventionally swept from -30 V to 30V with the V_{DS} fixed at 1 V and 5 V, respectively (unless specified). For normal measurements the scanning rate was kept at 0.663 Vs−1 ionic liquid treatment the scanning rate was kept at 0.133 V s−1. The capacitance of the ionic liquid EMIM TFSI was measured (for frequencies from 0.1 Hz to 10 kHz) via impedance spectroscopy using autolab PG STAT 302N and that of SiO_2 was measured by E4980A Precision LCR Meter at a frequency of 10 kHz. The perturbation voltage used for capacitance measurement was V_{AC} = 45 mV.

The conventional n-type enhancement-mode TFTs have three operation regimes: (a) cutoff, (b) linear, and (c) saturation regime. (**Figure 3-7**)

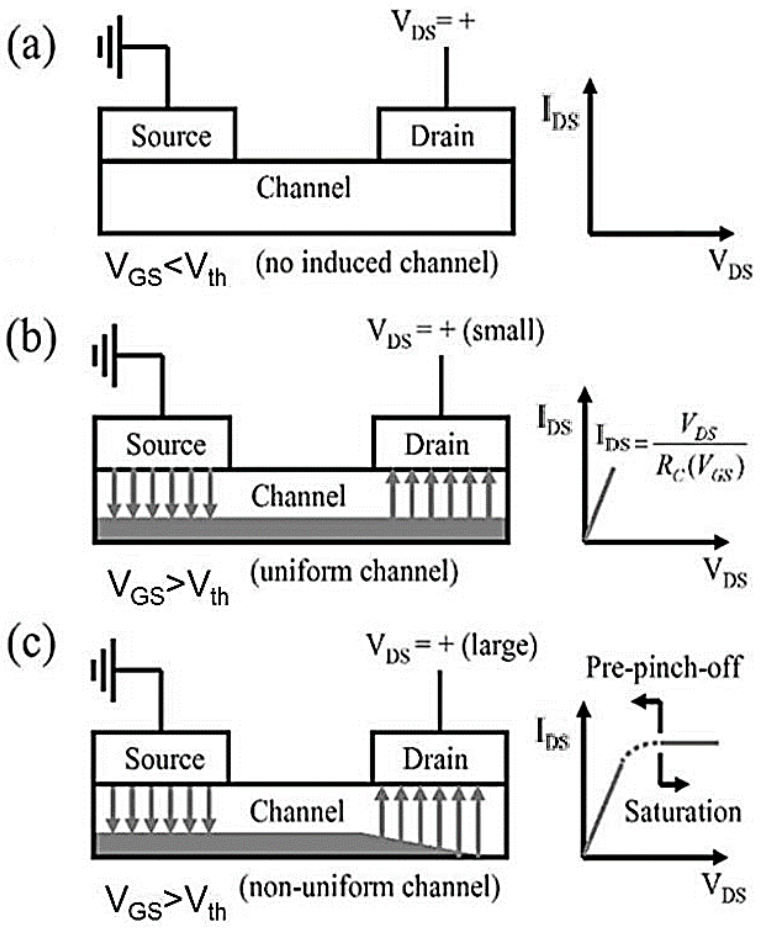


Figure 3-7: Operation principle of TFTs, (a) off state, (b) linear, and (c) saturation region, respectively. [14] Reproduced with permission from Springer.

Cutoff regime: When the gate-source voltage (V_{GS}) is lower than turn-on voltage (V_{th}), the electrons induced from source region are inadequate to generate a conductive channel. Consequently, TFTs is in off-state (**Figure 3-7**(a)).

Linear regime: When V_{GS} is larger than V_{th}, and the source-drain voltage (V_{DS}) is lower than V_{GS} - V_{th} ($V_{DS} \leq V_{GS} - V_{th}$), the electrons from source enter the channel and reach the drain. If V_{DS} is increased, the drain current (I_{DS}) flowing through the channel increases. Effectively, the TFTs act as a resistor in this regime, and the plot of I_{DS} versus V_{DS} is a straight line (**Figure 3-7**(b).

Saturation regime: When the V_{DS} is increased continuously and reaches the value of $V_{DS} = V_{GS} - V_{th}$, the width of channel approaches zero near the drain. This phenomenon is called pinch-off, which leads to a saturation of the drain current (I_{DS}). When the ($V_{DS} \geq$ VGS - V_{th}), the pinch-off point of the channel begins to move away from the drain region. Hence, IDS only depends on V_{GS} in the saturation regime (**Figure 3-7**(c)).

The electron mobility (μ_{FE}), the threshold voltage (V_{th}), and subthreshold swing (*S.S.*) are the TFT parameters commonly used for describing the electrical performance of TFT devices. Typically, the field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) in the linear region with applying low drain bias. The drain current of the TFT device in a linear region can be expressed as the following equation:

$$I_{DS} = \mu_{FE} C_{OX} \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \text{.....Eq. (3-1)}$$

where C_{ox} is the gate oxide capacitance per unit area, W is channel width, L is channel length, and V_{DS} is the drain voltage. If V_{DS} is much smaller than V_{GS}- V_{th} (i.e., $V_{DS} << (V_{GS} - V_{th})$) and $V_{GS} > V_{th}$, the drain current can be approximated as:

$$I_{DS} = \mu_{FE} C_{OX} \frac{W}{L} [(V_{GS} - V_{th}) V_{DS}] \text{ .....Eq. (3-2)}$$

The transconductance is defined as:

$$g_m = \mu_{FE} C_{OX} \frac{W}{L} V_{DS} \quad \text{.....Eq. (3-3)}$$

Thus,

$$\mu_{FE} = \frac{L}{C_{OX} W V_{DS}} g_m \quad \text{.....Eq. (3-4)}$$

In the saturation region, the drain current of the TFT device could be expressed as the following equation,

$$I_{DS} = \frac{1}{2} \mu_{FE} C_{OX} \frac{W}{L} (V_{GS} - V_{th})^2 \quad \text{.....Eq. (3-5)}$$

where μ_{sat} is the mobility in the saturation region. The saturation mobility could be extracted by the slope of $|I_{dS}|^{1/2}$-V_{GS} plot as an equation,

$$\mu_{sat} = \frac{2L}{W C_{OX}} \left(\frac{\delta \sqrt{I_{DS}}}{\delta V_{GS}} \right)^2 \quad \text{.....Eq. (3-6)}$$

The V_{th} is defined from the gate to source voltage while the TFT channel starts to turn on. The threshold voltage (V_{th}) is the critical figure of merit in TFT, which represents the onset of significant drain current flow. Therefore, V_{th} is strongly related to the gate insulator thickness and the flat band voltage. There are various methods to determine the value of V_{th} [15]. In this dissertation, the extrapolation method in the linear region is used, which uses the gate voltage axis intercept of the linear extrapolation of the transfer characteristics at its maximum first derivative (slope) point.

The subthreshold swing is a typical parameter to describe the control ability of the gate towards the channel, which is the speed of switching the device between on and off states. *S. S.* is affected by the total trap density, including interfacial trap density and bulk density. Therefore, it is commonly used for describing the quality of a TFT device. It determines the minimum V_{GS} required to turn a TFT from the off state to the on the state. It is defined

as the amount of gate voltage required to increase and decrease drain current by one order of magnitude as following [16]

$$S.S. = \frac{\delta V_{GS}}{\delta \log(I_{DS})} \quad \text{.....Eq. (3-7)}$$

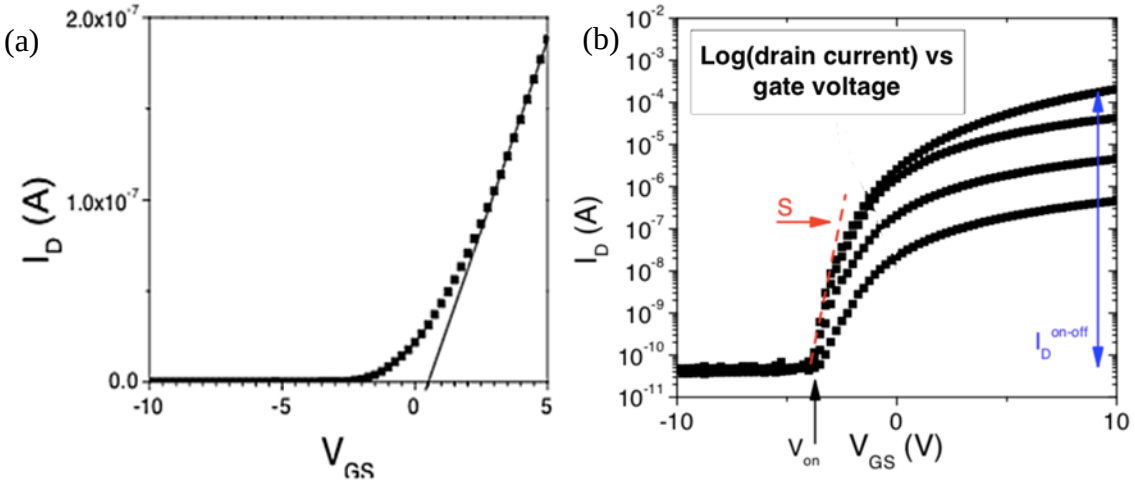


Figure 3-8: Determination of (a) g_m and V_{th} (b) S and I_{on}/I_{off}. [17] Reproduced with permission from Orgon State University.

The g_m is determined from the gradient of the linear portion of the I_D vs. V_{GS} graph at low V_D (**Figure 3-8**a).[17] where the device was operating in the linear region. Extrapolating this line to the horizontal axis would give us the V_{th}, as shown in **Figure 3-8**a and (I_{on}/I_{off}) is easily computed by dividing the I_{on} by I_{off}. These two values can be easily read off from the log (I_D) versus V_{GS} graph, as shown in **Figure 3-8** b. V_{on} can also be determined from the log (I_D) versus V_{GS} graph, as shown in **Figure 3-8** b. V_{on} is the gate voltage at which the device becomes conductive [17] and is identified by the point where there is a sharp rise in drain current, as shown in **Figure 3-8** b. In this study, The focus will be on V_{th} rather than V_{on}. This is because V_{th} gives us a better understanding of the voltage needed to form a channel layer in the semiconducting layer. Also, V_{th} indicates whether the device is operating in the enhancement mode or depletion mode, which is vital when deciding the device's potential application, as explained above. In terms of SS determination, the subthreshold slope (S) is extracted by calculating the gradient of the log (ID) versus VGS graph in the linear portion, as shown in **Figure 3-8** b and inverse of that will give SS.

3.5 Physical characterization

3.5.1 Field emission scanning electron microscopy (FESEM)

The scanning electron microscopy is a versatile, non-destructive technique that reveals detailed information about the morphology and the composition of materials. FESEM is a microscope that uses electrons instead of light for scanning the object under test. Electrons are emitted by the electron gun, which is a field emission source. These electrons are accelerated by high voltage within the high vacuum column. The focusing and deflection of this electron beam are done by electronic lenses. This focused beam of electrons is bombarded on a small spot of the sample while scanning. This results in secondary electron emission, which depends on the surface structures. A detector captures these electrons and converts it to a detectable electric signal which is processed to display an image. For this imaging, sample preparation is an essential step. For insulating samples, charging of sample takes place due to the electron bombardment, thus creating unclear images. Hence, such samples must be sputtered with a conducting material (Pt, Au) before FESEM imaging, so that the electrons will dissipate from the surface.

3.5.2 X-ray diffraction (XRD)

The X-ray diffractometry (XRD) analysis is the most common technique to obtain structural information such as the structure phase, preferred orientation, crystallinity, and average grain size. **Figure 3-9** shows the schematic mechanism of XRD analysis [18][19]. The XRD instrument utilized in this dissertation adopts the monochromatic Cu Kα X-ray (λ= 1.5418 Å). The Cu Kα X-ray incident on the sample with an angle (θ), can be reflected by the crystalline planes with different orientations. The reflected X-rays from the two consecutively parallel crystalline planes can form the constructive or destructive interference. Only the former can be detected by the detector, which reflects an XRD peak in the XRD pattern. By fitting this XRD pattern with the referred XRD peaks on Powder Diffraction Standards (JCPDS) database, the sample's crystalline structure, phase, and

orientation can be determined. The condition to form the constructive interference must meet the Bragg's law as followed:

$$2d \sin\theta = n \lambda \quad \text{.....Eq. (3-8)}$$

where d is the spacing between the two consecutively parallel crystalline planes, n is an integer, and λ is the wavelength of the Cu Kα X-ray.

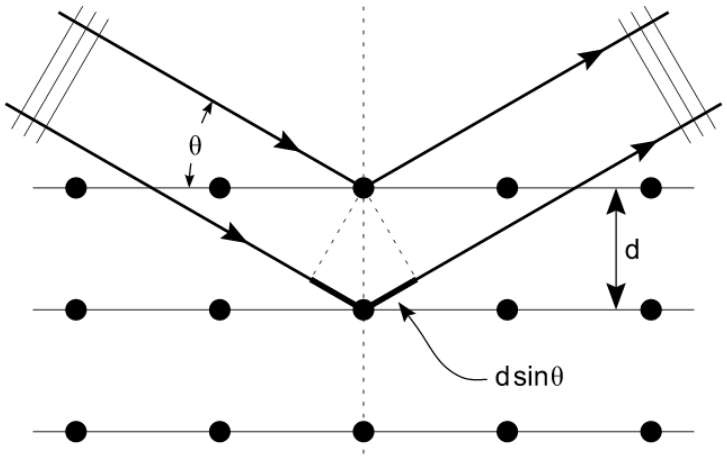


Figure 3-9: Schematic mechanism of XRD analysis. [18]

In this dissertation, the XRD is used to evaluate the phases and structures of various thin films. the amorphous phase of material is preferred, which plays a critical factor in maintaining better process uniformity in different positions on the glass/silicon substrates.

3.6 Surface characterization

3.6.1 X-ray photoelectron spectroscopy (XPS)

The X-ray photoelectron spectroscopy (XPS) (**Figure 3-10**(a)), also known as electron spectroscopy for chemical analysis (ESCA) is the most widely used surface analysis technique for material analysis. This surface-sensitive technique provides information such as elemental composition, chemical bonding energy, and depth profile of the samples virtually without any restriction on the type of material.

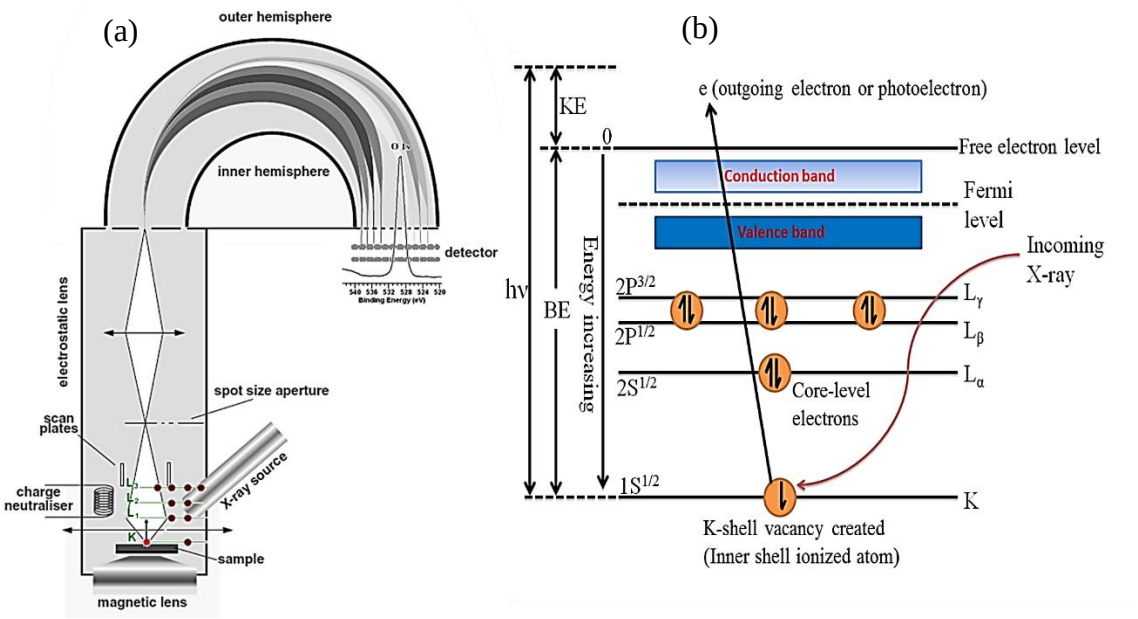


Figure 3-10: (a) Schematic diagram of the XPS analysis [20] (b) Illustration of XPS analysis. [21]

Figure 3-10 (b) shows the brief principle of the XPS, which is based on the photoelectric effect proposed by Einstein in 1905. This phenomenon could be expressed by the following equation [22]:

$$BE = h\nu - KE \quad \text{.....Eq. (3-9)}$$

Where BE is the binding energy of the electron in the atom, hν is the photon energy of X-ray source (Al Kα, 1486.6 eV and Mg Kα, 1253.6 eV), KE is the kinetic energy of the emitted electron that is detected by the analyzer. The chemical state of an atom alters the BE of a photoelectron resulting in a change in the measured KE. The different bonding states of the core level electrons correspond to the different binding energies, the chemical bonding states of an element can be determined by comparing the binding energy shift. Therefore, the element either in the neutral molecular state or in the charged compound state can be distinguished.

In this dissertation, the XPS analysis is employed as a material analysis method to investigate the atomic concentration and oxidation states of metal cations in oxide semiconductor thin film as well as a various bond for organic compounds in chapter 5. The bonding states of the oxygen can be realized from the oxygen (O1s) peak at about 531 eV

in the XPS spectrum. The oxygen deficiency in amorphous oxide semiconductor would generate excess carriers and form defect states, which strongly affects the electrical characteristics of TFT devices [21]. The peak deconvolution is usually required to separate several similar bonding states that generally have peaks close to each other. This analysis can help us to verify the bonding states of oxygen in IWO thin film fabricated under various process conditions. In consequent peaks such as C1s, N1s, Si2p, S2p, F1s would also be studied in detail in order to characterize surface adsorbed species.

3.6.2 Contact angle measurement

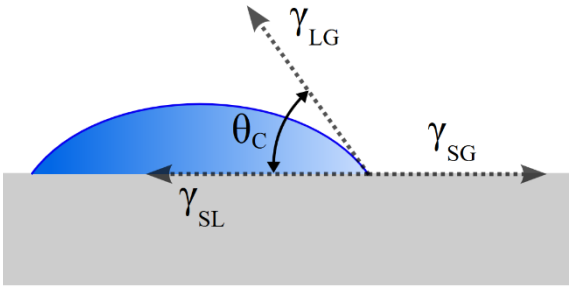


Figure 3-11: Schematic of liquid drop showing different energies in young's equation.

The contact angle is the angle conventionally measured at the solid-liquid interface and quantifies the wettability of solid surface by liquid via young equation[23]. If the surface free energy is denoted by γ_{SG}, the solid-liquid interfacial energy by γ_{SL}, and liquid-vapor interfacial energy by γ_{LG} then the equilibrium contact angle θ_C is determined by young equation[23] (**Figure 3-11**) [24].

$$\gamma_{SG} - \gamma_{SL} - \gamma_{LG} \cos \theta_C = 0 \quad \text{.....Eq. (3-10)}$$

From this equation, the surface energy can be estimated. In this dissertation, the contact angle studies were done for surface treated samples. The surface treatments change the surface free energy making the film either hydrophilic or hydrophobic. Hence to compare the various treatments and their effect on the surface, contact angle measurements were performed.

3.6.3 Fourier transform infrared (FTIR) spectroscopy

Most molecules absorb light in the infra-red region of the electromagnetic spectrum. This absorption explicitly corresponds to the bonds present in the molecule and is measured and analyzed in the FTIR study. The frequency range is denoted as wave numbers over a range of 4000 cm^{-1} - 400 cm^{-1}.

First a background emission spectrum of the IR source is recorded. Then the emission spectrum with the sample is recorded. The background spectrum is then subtracted from the obtained sample spectra. The absorption spectrum resulted from the natural vibration frequencies of bond indicates the presence of various chemical bonds and functional groups present in the sample. FTIR is very useful for identification of organic molecular groups and compounds due to various range of functional groups, side chains and cross-linking in these molecules. All of these will have characteristic vibrational frequencies in the infra-red range.

In this dissertation, FTIR is used to find the presence of various organic compounds on the oxide film after surface treatments as well as to detect ionic liquid residue on the oxide film after sample wash.

3.6.4 Atomic Force Microscopy (AFM)

The atomic force microscopy (AFM) is a high-resolution scanning probe microscopy. **Figure 3-12** shows the schematic configuration of the AFM system, which consists of a cantilever with a probe at its end to scan the morphology of the surface. The principle of the AFM is based on the van der Waals Force. When the probe is in close proximity to the detected surface (in the scale of angstroms), the interaction between the probe and sample induce a vertical shift. By calculating the displacement, the image of the detected surface can be obtained. In this dissertation, the tapping-mode AFM was adopted to scan the a-IWO sample in order to measure the thickness of the thin film and obtain the surface morphology. In this mode, the probe is oscillated and scanned at a height where it barely

taps the sample surface. The system monitors the variation of probe position and vibrational amplitude to obtain the image information. This method can lessen the damage of the sample and provide a better resolution (about 50 Å lateral and <1 Å height) compared with the other modes (contact and non-contact mode)[25].

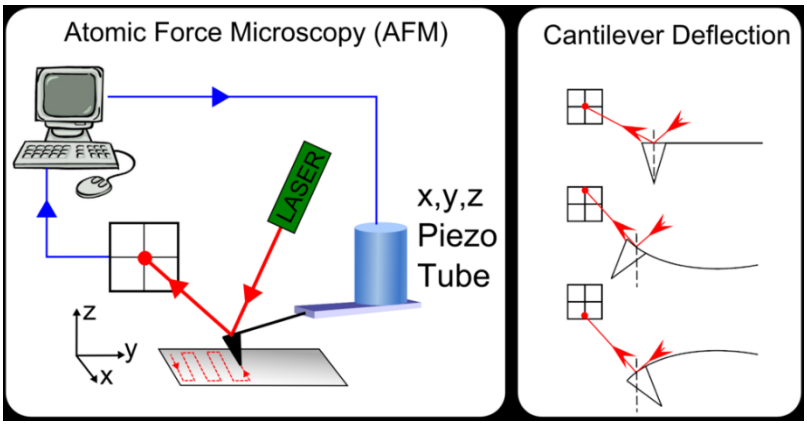


Figure 3-12: Schematic configuration of the AFM system. [26]

3.7 Electronic level characterization

3.7.1 Ultraviolet photoelectron spectroscopy (UPS)

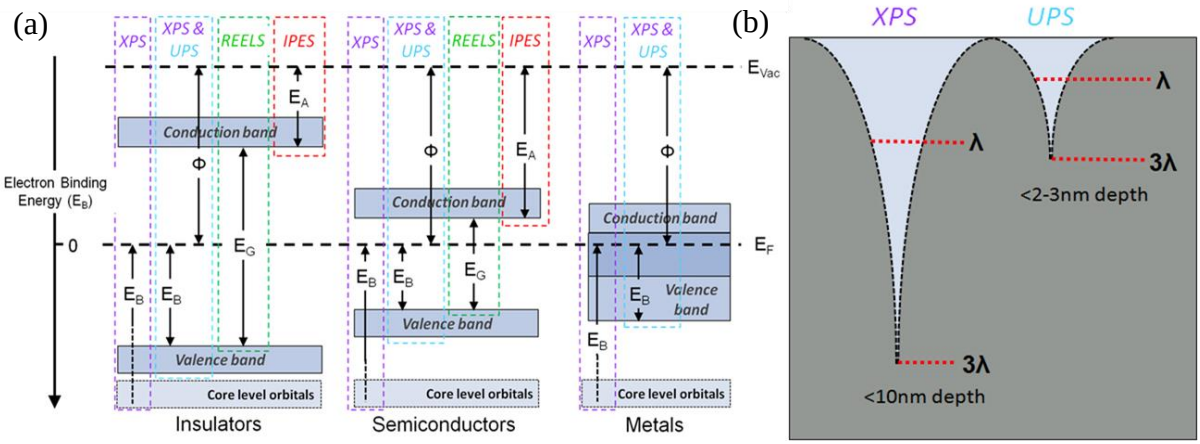


Figure 3-13: (a) Comparison with different characterization techniques[27] (b) difference in information depth for XPS and UPS. [27]

Ultraviolet Photoelectron Spectroscopy (UPS) operates on the same principle as the XPS. However, the excitation source is a helium discharge source. Depending on the operating conditions of the source, the photon energy can be optimized for He I = 21.22eV or He II

= 44.8eV which is significantly lower energy than Al Kα, 1486.6 eV and Mg Kα, 1253.6 eV used in XPS. The consequences of this lower photon energy is as listed: (i) only the low binding energy valence electrons will be excited using the He source, hence, spectral acquisition is limited to the valence band region (**Figure 3-13** (a) gives comparison with different characterization techniques and the electron binding energies which those techniques can address) (ii) UPS is more surface sensitive than XPS and thus very sensitive to surface contamination. (**Figure 3-13** (b) gives the depth comparison for the XPS and UPS)

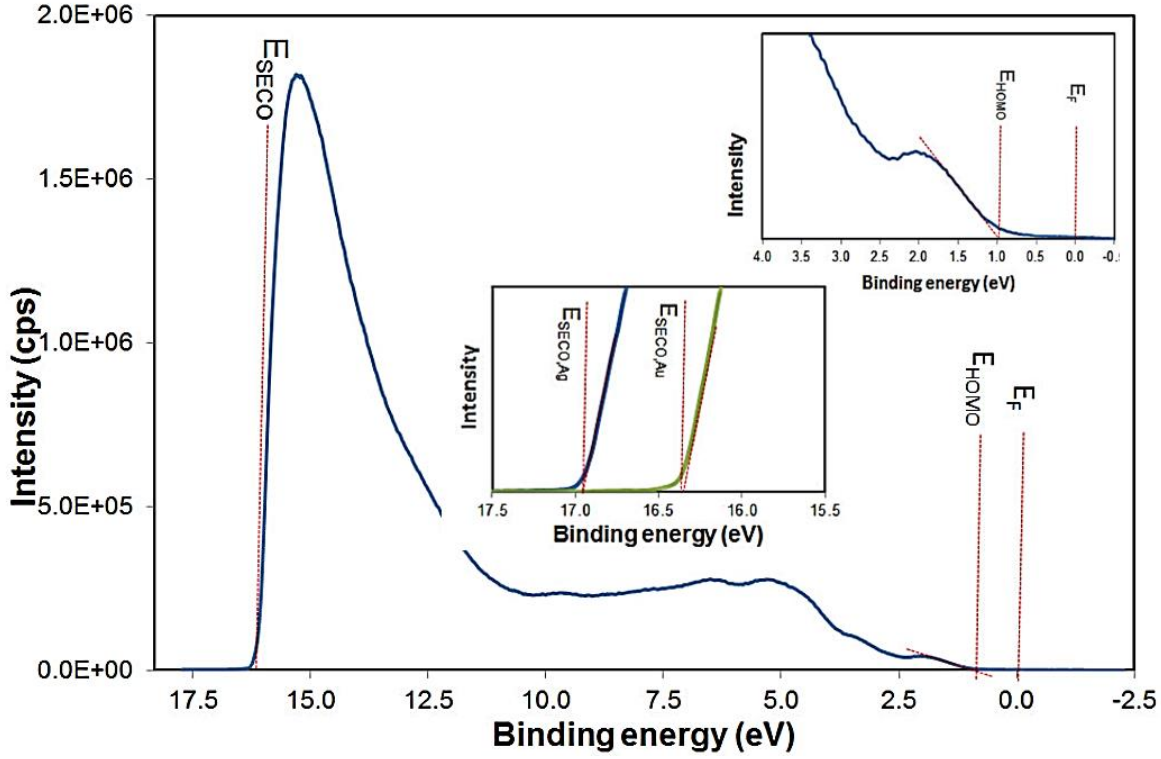


Figure 3-14: UPS spectra and the derivation of various energy levels. [28]

There are two types of experiments performed using UPS: Valence band acquisition and electronic work function measurement. The work function, Φ, and the Ionisation Potential, IP can be calculated using Equation eq. 3.10 and eq. 3.11 respectively.[28] The procedure to find E_{SECO} and E_{HOMO} is demonstrated in **Figure 3-14**

$$\Phi = h\nu - E_{SECO} \quad \text{.....Eq. (3.11)}$$

$$IP = h\nu - E_{SECO} + E_{HOMO} \quad .....Eq.\ (3.12)$$

where $h\nu$ = photon energy and E_{SECO} = Secondary Electron Cut Off Energy and E_{HOMO} = binding energy of the Highest Occupied Molecular Orbital.

In this dissertation, UPS is used primarily for finding the work function and HOMO energy level of oxide, and variation in these two parameters due to the surface modifications done using self-assembled monolayers formed by silanes, thiol, various organic compounds and charge neutral polymers with an amine group. The calculated shifts in these levels will help in analyzing the significant change in carrier concentration which leads to variation in device characteristics.

3.7.2 Optical absorption spectroscopy

An optical absorption spectroscopy is used to determine optical bandgap of the semiconductor. Tauc et al. proposed a method for determining the band gap using optical absorbance data plotted appropriately with respect to energy. It was further developed by Davis and Mott in order to find the optical band gap of the material using following equation.[29]

$$(\alpha h\nu)^{1/n} = A\,(h\nu - E_g) \quad .....Eq.\ (3.12)$$

Where h is Planck's constant, ν is the photon's frequency, α is the absorption coefficient, E_g is the band gap, and A is a proportionality constant. The value of the exponent denotes the nature of the electronic transition; allowed/forbidden and direct/indirect: for direct allowed transitions: n= 1/2, for direct forbidden transitions: n= 3/2, for indirect allowed transitions: n= 2, for indirect forbidden transitions: n= 3. Typically, the allowed transitions dominate the basic absorption processes, giving either n= 1/2 or n= 2, for direct and indirect transitions, respectively.[29][30]

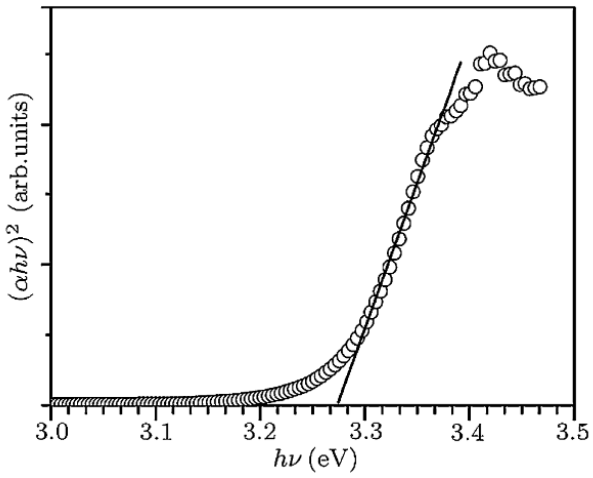


Figure 3-15: Example Optical absorption spectroscopy from UV–Vis analysis of a ZnO thin film that illustrates the method of fitting the linear region to evaluate the bandgap at the X-axis intercept, here about 3.27 eV. [29][30] Reproduced with permission from Wiley.

Tauc analysis is used to acquire optical absorbance data for the sample in a range of energies from below the bandgap transition to above it. Tauc analysis is doen by plotting the $(\alpha h\nu)^{1/n}$ versus $h\nu$. Plots with n= 1/2 and n= 2 can be compared to obtain the correct transition type (one providing the better fit). [29] **Figure 3-15** gives an example of Optical absorption spectroscopy for ZnO where n=1/2 was chosen; this was because ZnO is well known for direct transmission. In this dissertation, the Optical absorption spectroscopy is used to calculate the indirect band gap of tungsten-doped indium oxide subjected to different surface treatments. Hence n=2 was chosen.[31], [32] The required optical absorption spectra were collected by Ultraviolet-visible spectroscopy (UV-VIS) with UV–vis spectrometer (SHIMADZU UV-3600 UV–vis-NIR Spectrophotometer) with an integrating sphere (ISR-3100)

3.7.3 Photoelectron spectroscopy in air (PESA)

PESA can be used to detect homo levels of materials, measure the density of states, measure ionization potential and photoemission properties. The intensity of light emitted from the ultraviolet lamp enters into a nitrogen substitution chamber and then into the spectrometer. Spectrometer selects a wavelength of UV light and irradiates to the atmosphere through

the CaF2 window. Resulted photoelectrons emitted from the surface are counted by the open counter and processed.[33] In this dissertation, PESA was used to calculate ionization potential variation in the oxide. **Figure 3-16** shows a technique to measure the ionization potential of oxide.

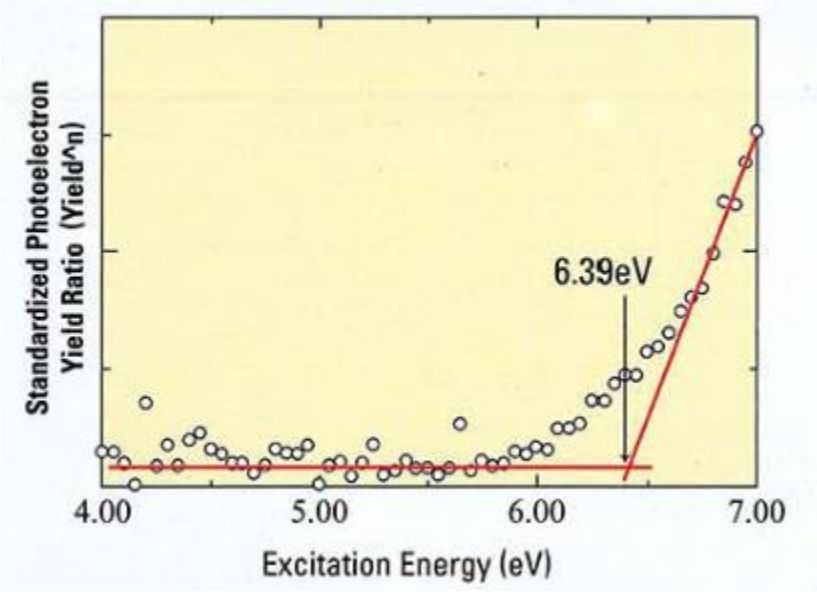


Figure 3-16: Ionization potential of oxide from PESA measurement.

3.7.4 Mott Schottky measurement

The Mott Schottky measurement is used to calculate the doping density of semiconductor and built-in potential for semiconductor, which can give a flat-band potential.[34] In semiconductor electrochemistry, a Mott-Schottky plot describes $1/C^2$ vs. potential difference between the bulk semiconductor and bulk electrolyte. The capacitance is measured through electrochemical impedance spectroscopy.

The formula to detect capacitance is derived from the depletion layer width considering semiconductor/ electrolyte junction. This capacitor can be approximated as two parallel plates with an area of electrode and depletion layer width as the distance between two plates. Capacitance C is calculated by the following formula

$$C^{-2} = \frac{2(V+V_{bi})}{qA^2\varepsilon N_D} \quad \text{.....Eq. (3.13)}$$

Where $\varepsilon = \varepsilon_r\varepsilon_0$ is the permittivity, q is the elementary charge, N_D is the doping density, V is applied bias potential, V_{bi} is the built-in potential, electrode area A.

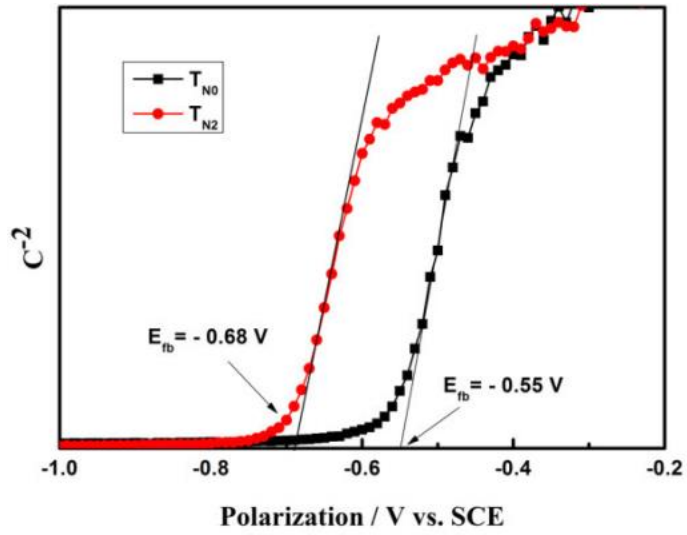


Figure 3-17: Mott Schottky plot derived from impedance spectroscopy of mesoscopic nitrogen-doped TiO_2. [35] Reproduced with permission from Springer.

Figure 3-17 gives the Mott Schottky measurement derived from impedance spectroscopy. The slope gives the doping density of semiconductor, the intercept to the x-axis provides the built-in potential, or the flat-band potential and allows establishing the semiconductor conduction band level with respect to the reference of potential. If standard SCE is not used, the x-axis values should be subtracted from the potential of a used standard electrode for accurate results. In this dissertation, Mott Schottky measurement was used for distinguishing the effect of oxidation on oxide semiconductor, using impedance spectroscopy, performed using electrochemical workstation (Autolab PGSTAT302N).

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Chapter 4 *

Influence of fabrication parameters and overlayer on TFT characteristics

The feasibility of Ga/Zn-free Indium Tungsten Oxide (IWO) as a semiconducting channel layer for TFT was investigated. The conduction of the IWO layer was varied through the control of oxygen vacancies via conventional annealing. In-depth studies of IWO film with respect to variation in oxygen flow rate during reactive sputtering, annealing temperature, and various electrode materials was performed for IWO TFT fabrication. Flexible TFTs on PI substrates were also demonstrated, with non-degraded device performance for a bending radius of up to 3mm. The prospect of athermal annealing with the inclusion of a reducing oxide capping layers was also explored based on their relative position in the Ellingham diagram. From the capping layer thickness studies, it was concluded that deposition of the alumina layer increased the oxygen vacancy concentration in the channel proving the utility of Ellingham diagram to transform TFTs from enhancement mode operation into depletion mode operation without high-temperature annealing.

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* This chapter is currently being prepared substantially as Kulkarni Mohit Rameshchandra, et al. “Oxygen vacancy modulation using overlayer chosen from Ellingham diagram for low temperature Oxide Thin film transistor activation,” (2019)

4.1 Introduction

In metal oxide semiconductors, the number of charge carriers greatly influence device characteristics. The number of charge carriers depends on the number of oxygen vacancies in the oxide [1]. For better device stability, a stronger metal-oxygen bond is desired to suppress the creation of oxygen vacancies. In IGZO TFTs, the low bond dissociation energy of Zn-O and Ga-O, facilitates the creation of oxygen vacancies, affecting the TFT's electrical performance [2]. Additionally, Gallium Oxide (Ga_2O_3) and Zinc Oxide (ZnO) are sensitive to humidity, affecting IGZO's stability [2]. Thus, there is a need to explore other oxides that can offer similar characteristics to an IGZO TFTs but offer enhanced stability. In this work, Ga-Zn-free IWO is studied as an alternative to IGZO. W acts as a much better charge suppressant [3], due to the higher oxygen dissociation energy for W-O (653 kJ/mol) when compared to In-O (360 kJ/mol), Zn-O (284 kJ/mol) and Ga-O (285 kJ/mol), makes a good carrier suppressant and increases the stability of oxide. [4] . It also reduces oxygen vacancy creation and facilitates the control of carrier concentration in the channel layer. With lower operational voltages, higher mobility and better resistance to moisture and acidic environments, indium tungsten oxide (IWO) thin films are promising alternatives to the intensively-researched indium gallium zinc oxide (IGZO) counterparts, justifying their selection as the reference prototypical AMOS system. [5]–[11] This chapter will study the effect of annealing temperature, oxygen flow rate during sputtering, and the type of source/drain electrode. Despite tungsten's role as a charge suppressant, the low doping of 2% results in the presence of a high number of the oxygen vacancies in tungsten-doped indium oxide, thus making it highly conducting with a large negative threshold voltage. The high value of V_{th} indicates the TFT to be in deep depletion mode, the requirement of sizeable operating voltage to turn off the TFT. Hence the as-deposited films of tungsten-doped indium oxide usually are highly conductive, and annealing in the presence of oxygen/air is needed for decreasing the conductance of film for lower operating voltages.

Capping layer selection using Ellingham diagram

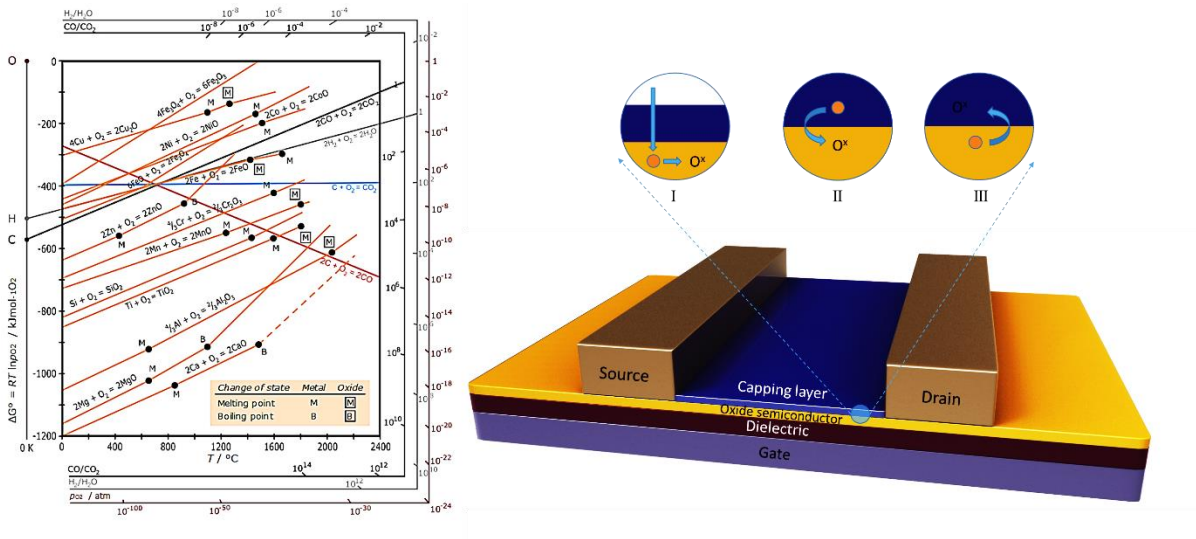

Figure 4-1: (a) Ellingham Diagram (b) Capping layer affecting the transport of oxygen in and out of the system modulation the concentration of oxygen vacancies inside the film. The three inset shows, oxygen diffusion from air to the oxide layer (I), oxygen transfer from capping layer to oxide semiconductor (II), oxygen transfer from oxide semiconductor to capping layer (III).

In the case of oxides with a smaller number of oxygen vacancies, the electronic properties of oxides are entirely different. In thin-film transistors (TFTs), the carrier concentration conductivity, mobility, on-off ratio decreases, and threshold voltage becomes positive.[12] With this, the TFT may be in deep enhancement mode, requiring high operational voltages in order to turn on the TFT. Capping layers can be designed using guidelines from the Ellingham diagram (**Figure 4-1**(a)) to selectively reduce/oxidize the oxide layers beneath them (more details in the literature review). The metal oxides with a relatively higher position in the Ellingham diagram can effectively oxidize those lying below it and vice versa.[13] The use of this concept to deposit capping layers through sputtering to act as local sources of oxygen for tuning the oxygen vacancy concentration of the underlying layers is proposed in this thesis. Sputtering is chosen over ALD in order to avoid interference of additional process of reduction due to highly reactive ALD precursors[14]. This approach can help to tune the oxygen vacancy concentration at lower temperatures without the need for a high-temperature post-annealing step. By depositing a capping layer, variable valence states at the interfaces of the underlying oxides can be achieved by tuning

the oxygen vacancy concentration in them. This can also enable low-temperature tuning of transport property in transition metal oxides. Capping layers could also be designed in such a way as to facilitate oxygen vacancy formation (reduction) in the active layer and helps to drive out these vacancies under an applied field. **Figure 4-1** (b) depicts the role of the capping layer in modulating the transport of oxygen vacancies from and to the active layer.

4.2 Study of process parameters for IWO TFT

4.2.1 Effect of Annealing Temperature

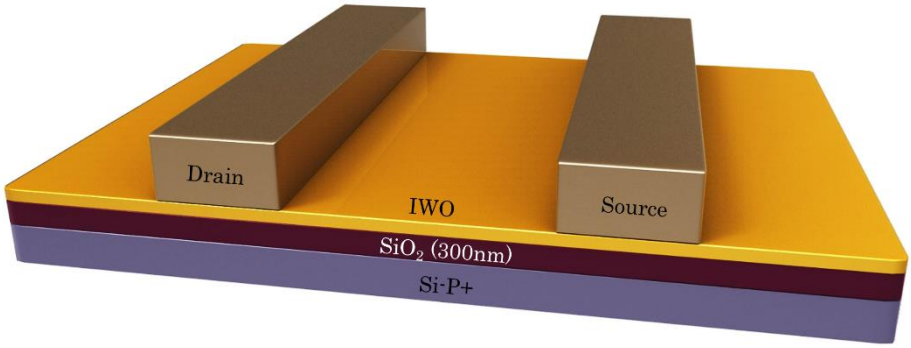

Figure 4-2: Device Structure used for the study of process parameters

In this segment, the effect of annealing on the electrical performance of the TFT was investigated. During sputter deposition, the oxygen flow rate was fixed at 1sccm. The figures of merit were used to characterize the TFT performance. The device structure used for this study is shown in **Figure 4-2**. The channel width and length were fixed at 400 and 800µm, respectively.

Table 4-1: Summary of device with IWO thickness of 20 nm annealed at 200 ^{o}C

T_{anneal} (^{0}C)	Unannealed	200 ^{o}C
Mobility (cm^2/V.s)	8.58	8.24
Subthreshold Swing (V/dec)	2.84	1.88
Threshold Voltage (V)	-22.33	1.47
I_{on} / I_{off}	2.0E+6	4.5E+6

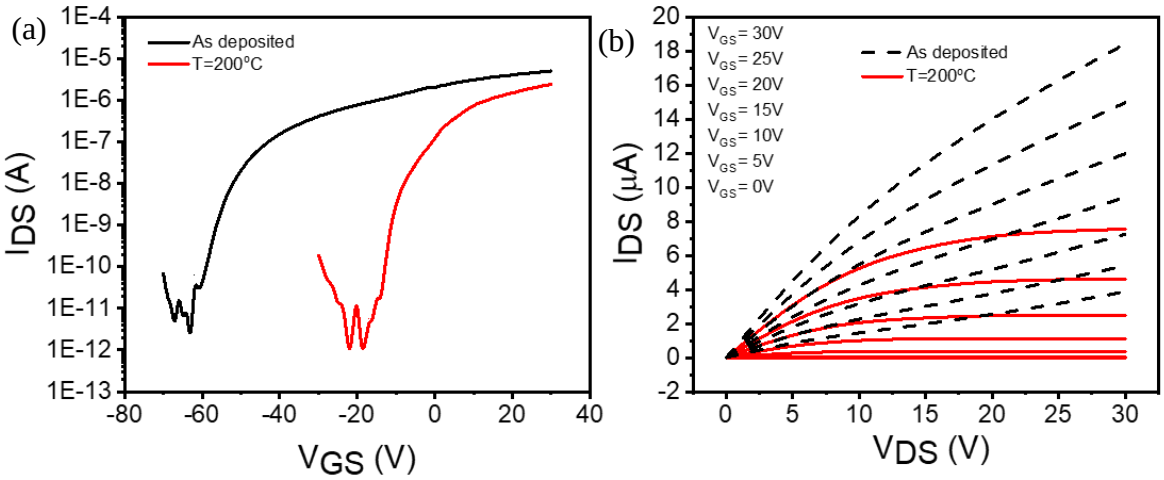

Figure 4-3: (a) Transfer characteristics (b) Output characteristics of as deposited and annealed samples. W=400 μm, L=800 μm V_{DS}=1V.

From **Figure 4-3**a and **Table 4-1**, The device annealed at 200 ºC for half an hour and with IWO thickness of 20nm offered the smaller subthreshold swing and smaller threshold voltage. The unannealed device possessed marginally high mobility, but its threshold voltage was very negative, which is highly undesirable, as higher threshold devices require larger switching voltage. Finally, the device annealed at 200 ºC had a mobility of 8.24 cm^2/V.s. It also possessed higher I_{on}/I_{off} ratio. Crucially, it had the lower subthreshold swing and a small positive threshold voltage, enabling it to operate in the enhancement mode and consume less power. Thus, the device with IWO thickness of 20 nm, annealed at 200 ºC is selected as the best device for further experiment. The output behavior of a device with IWO thickness of 20 nm annealed at 200 ºC is shown in **Figure 4-3**b.

XRD & AFM characterization

Figure 4-4 a shows the XRD scan of an as-deposited IWO and an IWO annealed at 200 ºC. The IWO remains in the amorphous phase even after annealing. This observation is similar to previous works on IWO TFTs [5][15]. **Figure 4-4** b shows the 3D AFM images of as-deposited IWO and an IWO annealed at 200 ºC. The films are of similar roughness. [16].

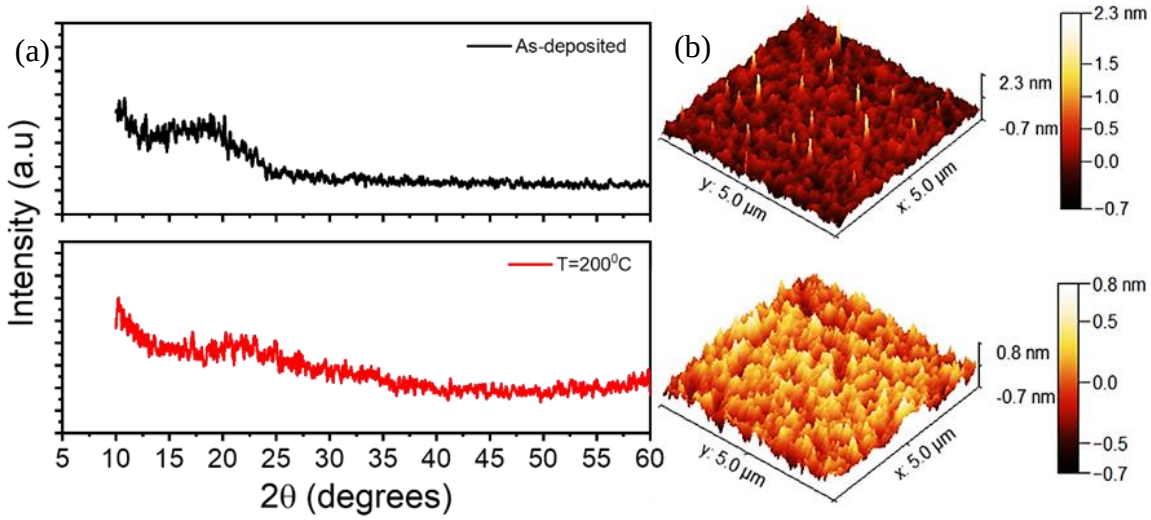

Figure 4-4: (a) XRD scan of an as-deposited IWO and annealed at 200 °C. (b) 3D AFM image of As-deposited IWO (top) and IWO annealed at 200 °C (bottom).

4.2.2 Effect of oxygen flow rate during sputter deposition

In this section, the effect of the oxygen flow rate on the electrical performance of the TFT was investigated. Oxygen flow rates of 0,1,2,3,4 & 5sccm were used. Based on the key figures of merit, the best oxygen flow rate was identified. The channel thickness and annealing temperature were fixed at 20 nm and 200 °C, respectively, as determined by the previous experiments.

Effect of oxygen flow rate on mobility and threshold voltage

A strong negative correlation was observed between the mobility and the oxygen flow rate, (**Figure 4-5** a) while a strong positive correlation was observed between the threshold voltage and the oxygen flow rate (**Figure 4-5** b). This was consistent with expectation. With a more significant oxygen flow rate, there would be a greater extent of oxygen incorporation into the channel layer. This results in a smaller number of oxygen vacancies, causing a decrease in the number of charge carriers and thus deteriorating mobility while elevating the threshold voltage. Both trends were reported by Chiang, Hai Q (IGZO [17]), and Liu et al. (IWO [18]). Overall, devices fabricated with an oxygen flow rate of 3, 4 & 5

sccm showed little promise due to their low mobilities of 3.53, 1.98 & 2.92 $cm^2/V.s$ respectively and high threshold voltages of 10.05, 13.8, and 12.66V respectively. Also, it is essential to note that at a flow rate of 0 sccm the devices no longer displayed transistor behavior but were instead conductive, this is likely to be due to a large number of charge carriers in the channel layer.

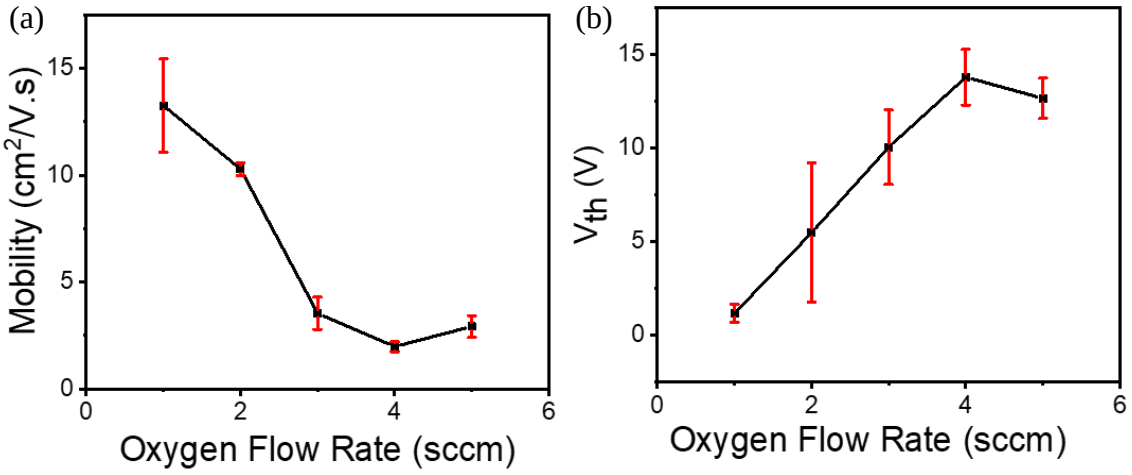

Figure 4-5: (a) Variation of mobility with an oxygen flow rate (b) Variation of threshold voltage with an oxygen flow rate.

Figure 4-6 shows the transfer characteristics of TFTs fabricated with an oxygen flow rate of 1-5sccm. From the figure, a clear rightward shift in V_{th} and the decrease in the on current is noted as of the oxygen flow rate rises. Overall, despite the reduced subthreshold swing for devices fabricated with an oxygen flow rate of 3-5sccm, they show little potential as they have poor mobilities and high threshold voltages. This narrows down the process to the devices fabricated with an oxygen flow rate of 1 and 2 sccm. 1sccm output characteristics was displayed in **Figure 4-6** b. Their key electrical parameters are captured in **Table 4-2**.

Table 4-2: Summary of devices fabricated with an oxygen flow rate of 1 and 2 sccm

Oxygen Flow Rate (sccm)	**1**	**2**
Mobility ($cm^2/V.s$)	13.26	10.28
Threshold Voltage (V)	1.17	5.49
Subthreshold Swing (V/dec)	1.88	1.47
I_{on}/ I_{off}	7.85e+05	3.22e+06

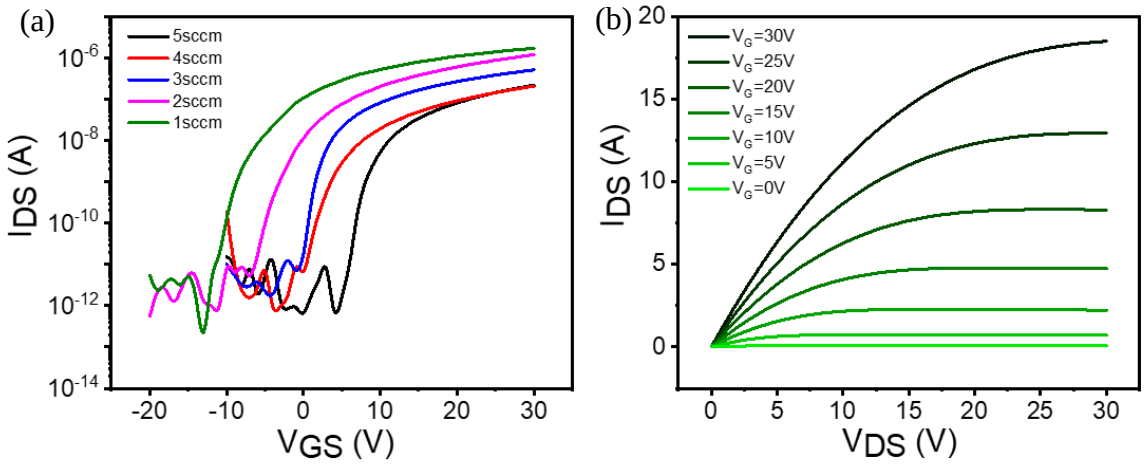

Figure 4-6: (a) Transfer characteristics of TFTs fabricated with an oxygen flow rate of 1-5 sccm (b) output behavior of a TFT fabricated with an oxygen flow rate of 1 sccm. W=400 μm, L=800 μm V_{DS}=1V.

The TFT fabricated with an oxygen flow rate of 1 sccm offers higher mobility, smaller threshold voltage and a better on/off current ratio. However, the TFT fabricated with an oxygen flow rate of 2 sccm offers an enhanced subthreshold swing. Intending to devise a recipe which can be used to fabricate TFTs for applications, where the subthreshold swing is essential, it is likely that an oxygen flow rate of 2 sccm might be optimal. For device used in digital circuits in transparent electronics, low operating voltage with high mobility is key factors. [19] Thus, the flow rate of 1 sccm is selected as the most optimal for our further experiments.

4.2.3 Selection of source/drain electrode material

In this segment, the effect of different source/drain electrodes on the electrical performance of the TFT was investigated. The IWO TFT was fabricated with a channel thickness of 20 nm and an oxygen flow rate of 1 sccm during sputter deposition. The materials explored were Aluminium (Al), Gold (Au), and Silver (Ag), Indium Tin Oxide (ITO). In this case, the annealing step was conducted before the deposition of the electrodes to avoid the electrode oxidation during the annealing process. The annealing temperature was set at 200 ^{o}C. Electron-beam evaporation was used to deposit the electrodes. The device structure

used is the same as the one depicted in **Figure 4-2**, with only the type of source/drain electrode varied. The TFTs with Ag and Au electrodes had very high threshold voltages (**Figure 4-7** a) and the Al, Ag, and Au devices had lower mobility compared to the ITO device (**Figure 4-7** b). Overall in the experiment performed, Al, Ag, and Au electrodes did not perform better than the ITO electrode. Hence for the remaining chapters, ITO was selected as the best electrode.

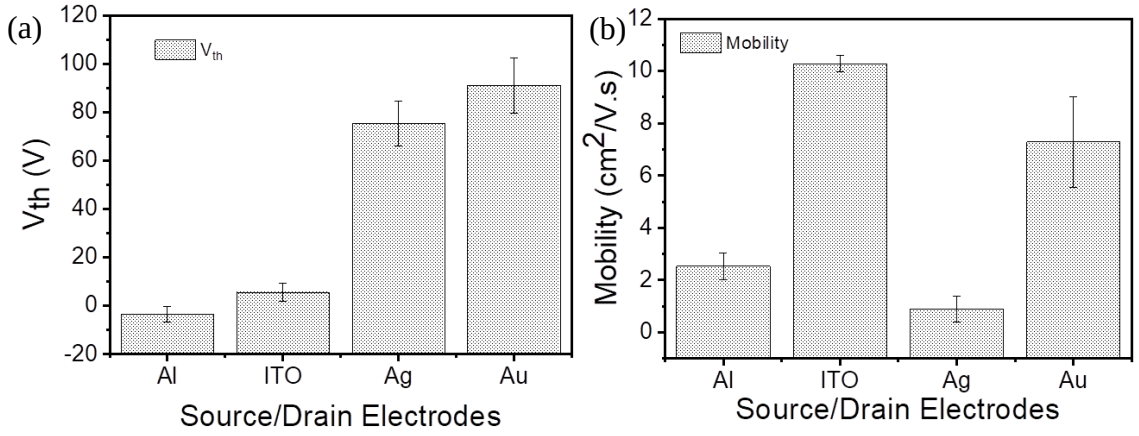

Figure 4-7: Effect of different source/drain electrodes on (a) threshold voltage, (b) mobility, W=400 μm, L=800 μm V_{DS}=1V.

4.2.4 Development of flexible devices

Electrical characterization before and after Flexing test on flexible transistor

Details about flexible TFT fabrication are provided in the experimental section. **Figure 4-8** (a) shows the structure of flexible TFT The thickness of each layer are PI= 10 um, SiO_2= 300 nm, Ti= 250 um, Al_2O_3= 100 nm, IWO= 7 nm was chosen because in future chapters thin films are needed) IWO was deposited at 1sccm oxygen partial pressure and 5mtorr Ar chamber pressure and annealed at 200 ºC. **Figure 4-8**(b) is the photo of fabricated flexible TFT mounted on the curved surface of 1.5 cm diameter.

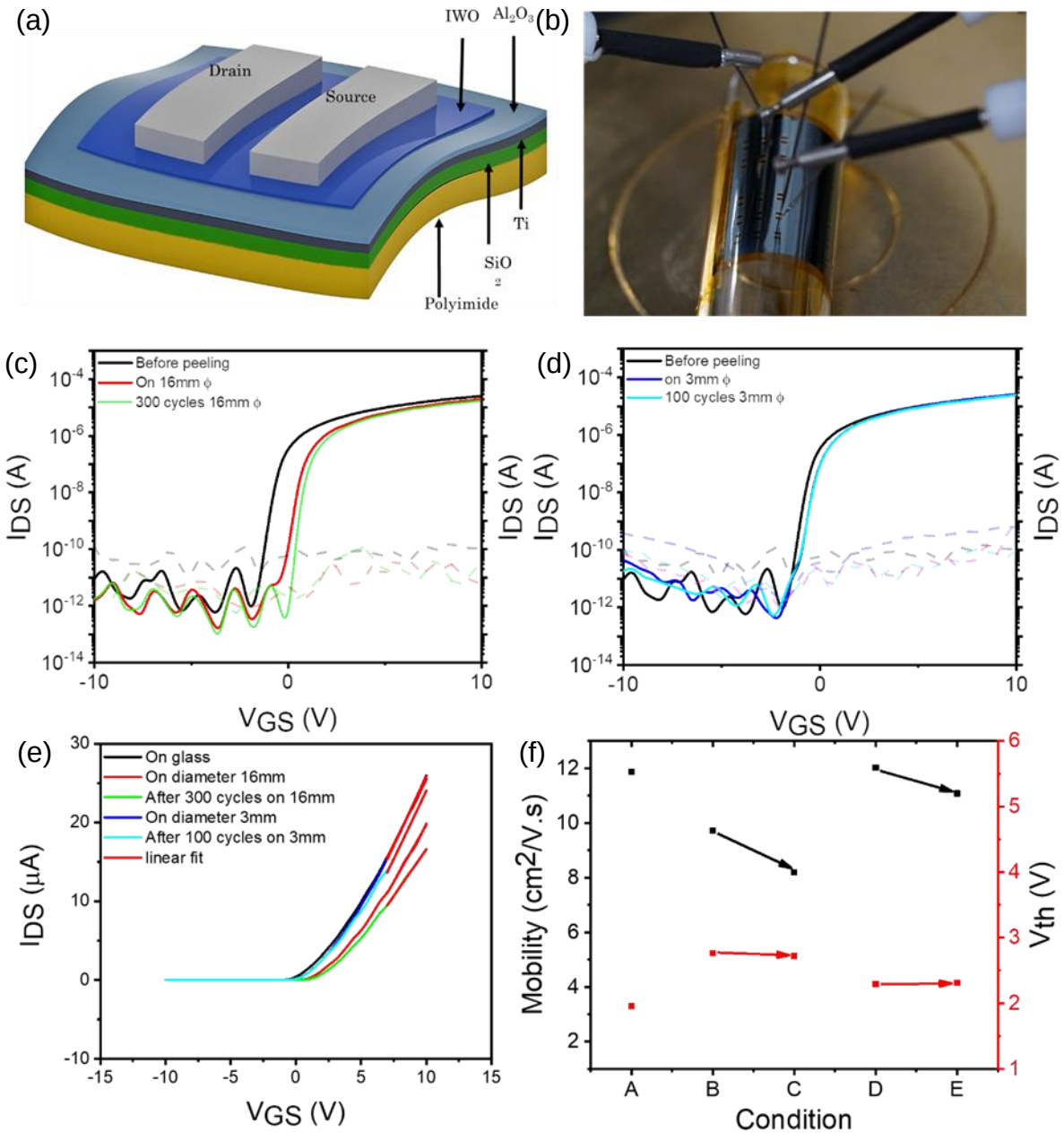

Figure 4-8: (a) Structure of flexible thin-film transistor (b) fabricated flexible TFT mounted on the surface of 1.5 cm diameter (c, d) transfer characteristics before and after flexing with a diameter of 16mm and 3mm respectively (e) linear fit for mobility and threshold voltage calculation (f) mobility threshold voltage and subthreshold swing calculations for TFT conditions (A. structure on the glass B. on 16mm diameter C. after flexing on 16mm diameter D. on 3mm diameter E. after flexing on 3mm diameter). W=1000 μm, L=300 μm V_{DS}=1V.

For strain durability measurements, the flexible transistors were attached on to tubes of diameter 16 mm and 3mm, corresponding to strains of 0.067 %, 0.36% respectively. The strain (ε) was calculated by the following formula[20]:

$$\varepsilon = (d_s + d_f)/2R \text{.....Eq. (4.1)}$$

where d_s is the thickness of the substrate, d_f is the thickness of the film, and R is the bending radius. The bending radius was kept below the 3mm limit of the critical strain (1%) of MOS thin films[21]. Electrical characterizations were performed on devices before, during, and after repetitive bending tests for up to 300 cycles for 16mm diameter and 100 cycles for 3mm diameter. The corresponding transfer characteristics of the devices are shown in **Figure 4-8** c and d, respectively. **Figure 4-8** e gives the linear curves used for plotting mobility, and **Figure 4-8** f summarizes TFT parameters. The mobility of transistor before removing from base glass substrate was measured to be 11.87 cm^2/Vs with V_{th} of 1.96 V. After removing from base substrate and transferring it to a 16 mm diameter surface which inflicted the strain of 0.067 % the mobility was measured to be 9.72 cm^2/Vs with V_{th} of 2.77 V. The transistor was then flexed 300 times from curved state to planar state and then measured again, and a mobility and threshold voltage of 8.2 cm^2/Vs and 2.72 V respectively was obtained. After removing from base substrate and transferring the TFT to a 3 mm diameter surface, which inflicted the strain of 0.36 %, the mobility was measured to be 12.03 cm^2/Vs with V_{th} of 2.29 V. The transistor was then flexed 100 times from curved state to planar state and then measured again and a mobility and threshold voltage of 11.08 cm^2/Vs and 2.31 V respectively was obtained. It can be noted that no significant changes were observed in the electrical behavior of flexible devices, demonstrating excellent stability with static bending deformation.

4.2.5 Summary and conclusion

It was concluded that an IWO thickness of 20 nm, annealed at 200 ^oC, and fabricated with an oxygen flow rate of 1sccm yielded the best device performance. The oxygen content was increased by increased reactive gas (O_2) pressure at the time of sputtering. The best

performing TFT had the mobility of 15.07 cm^2/V.s, the threshold voltage of 10.26 V and a subthreshold swing of 1.13 V/dec. ITO electrodes were selected as the best electrode for IWO TFT. A flexible TFT was also demonstrated with excellent stability til 3mm diameter bending radium. In the 5^{th} and 6^{th} chapters, focus is more on surface treatments of oxides which require a smaller thickness oxide TFT so that the real channel area is probed after the modifications which alter the properties of TFT to a great extent. Hence the smallest thickness of 7 nm was chosen for experiments. With the help of IWO as semiconducting material, the development of flexible TFT is successfully demonstrated. However, prior to use of IWO, IGZO was used to make flexible devices. The flexible devices using versatile IGZO systems were not of outstanding quality with a lot of nonuniformity. The IGZO film needs an adequate annealing temperature normally more than 300ºC for proper film formation. However, as noted in the literature review plastic substrates cannot handle this temperature level. Also, because of the difference in the coefficient of thermal expansion between two metals, the annealing and cooling process will generate interfacial stress. It will lead to more interface defects. It also leads to poor adhesion of flexible TFT with the substrate. Thus, although functioning flexible devices are demonstrated with IWO, in order to achieve the full potential of various semiconducting oxides in flexible devices, an athermal semiconductor activation still needs to be explored. In addition, as discussed in the literature review, it is essential for new applications to have an athermal, on-demand control after manufacturing on the conduction of oxide semiconductor.

4.3 Study of capping overlayers selected using the Ellingham diagram:

In this section, the effect of the capping layer on the electrical performance of the TFT was investigated. The preparation of TFT and capping layer used in this section was described in the methods section. First, 20 nm of IWO was deposited with an oxygen flow rate of 1 sccm, followed by the deposition of the ITO electrode. The devices were then annealed at 200 ºC for one hour. Next, the devices were measured to characterize their electrical performance prior to a capping layer. Al_2O_3 (1, 3, 5, 7 & 9 nm) was then sputter deposited as a capping layer, at a chamber pressure of 2mTorr and RF power of 120 W. The device structure is shown in **Figure 4-1** b.

4.3.1 Effect of an alumina capping layer on the electrical performance of the TFT

Across all Al_2O_3 thicknesses, the deposition of the capping layer led to a significant alteration in device characteristics. Apart from the device with a 1 nm thick capping layer, all other devices became conductive and no longer displayed transistor behavior. This showed that by depositing a capping layer, a large number of oxygen vacancies are created, generating a large number of free charge carriers created in the channel layer. A similar phenomenon was noted in a research where a metallic indium layer forms at the interface of EuO and ITO, as the latter gets reduced due to oxygen diffusing to EuO.[22] **Figure 4-9** a, b displays the mechanism of oxygen ion transfer and formation on metallic indium layer at the interface of IWO and alumina, which makes the TFT device characteristics resemble that of the conductor. In our experiment, it was also noted that as the capping layer thickness increased, the current of the conductive devices increased (**Table 4-3**) indicating an increase in oxygen vacancies. As the thickness of the capping layer increases, more oxygen diffuses from the channel layer to the capping layer, creating more charge carriers and enhancing the conductivity of the device. This occurrence is due to the alumina thin film growth process during sputter deposition. Initially, an O rich film forms, then as thickness rises, the film becomes Al-rich [23]. This means that higher alumina thicknesses are responsible for the higher reduction of the channel layer because of the abundant quantity of reducing oxide. This results in a more significant extent of oxygen diffusion from the channel layer to the capping layer, creating more oxygen vacancies in the channel layer.

Table 4-3: Relation between capping layer thickness and on current

Capping Layer Thickness (nm)	I_{on} after capping (A)
1	2.01E-06 [1]
3	6.01E-06
5	7.22E-05
7	9.45E-04
9	9.45E-04

[1] Still shows transistor behavior

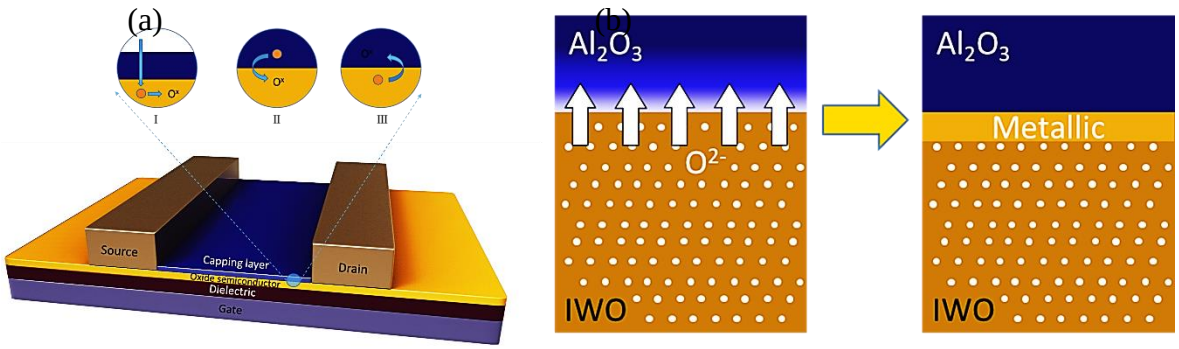

Figure 4-9: (a) Various proposed mechanism for oxygen transfer (b) Oxygen deficient alumina layer accepting oxygen ions from IWO.

4.3.2 Effect of post-capping annealing for the 1 & 3 nm-alumina capped devices

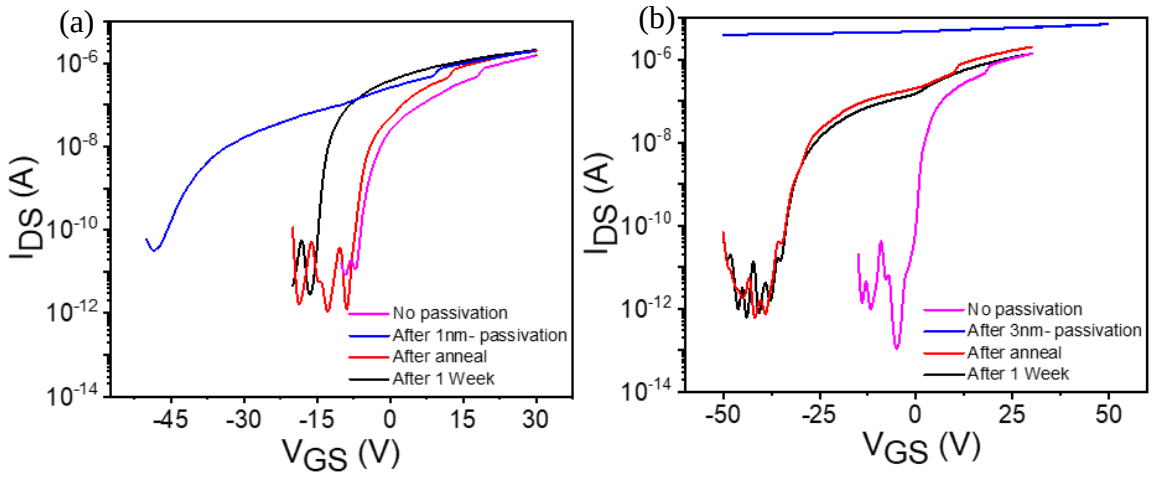

Figure 4-10: Transfer characteristics of (a) 1 nm-alumina passivated device (b) 3 nm-alumina passivated device. W=400 µm, L=800 µm V_{DS}=1V.

To investigate if the original, pre-capping device characteristics could be recovered, the devices were annealed for 60 mins on a hot-plate at 150^{o}C. This step proved successful for the 1 nm and 3 nm capped devices. The transfer characteristics of the 1 nm approached its original characteristics (**Figure 4-10**a). While for the 3 nm capped device, transistor behavior was restored (**Figure 4-10**b). **Table 4-4** compares the original and after-anneal electrical properties of the 1 and 3 nm capped devices. For the 1 nm capped device, the mobility and subthreshold swing deteriorated while its threshold voltage fell after capping. The negative shift in the threshold voltage is a consequence of the higher number of charge

carriers in the IWO, resulting in a smaller gate bias required to form the channel at the semiconductor/dielectric interface. Interestingly, the creation of more charge carriers suggests that the mobility would be enhanced, but this is not observed. The increase in the number of oxygen vacancies also resulted in a rise in the number of dangling bonds in the semiconducting layer. These dangling bonds act as charge trap states, inhibiting the flow of electrons, reducing mobility. In this case, the increased number of charge trap states outweighs the rise in the number of charge carriers, causing the mobility to fall, albeit only slightly by 2.84 $cm^2/V.s$. The reduced subthreshold swing (increase by ~ 4 times) also indicates that the effect of the rise in dangling bonds dominates, resulting in an inferior quality semiconductor/dielectric interface.

Table 4-4: Summary of electrical parameters of 1 and 3 nm, alumina capped devices

Mobility ($cm^2/V.s$)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	15.07	12.23	15.02	11.73
3 nm	12.83	NA	12.84	8.83
Subthreshold Swing (V/dec)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	1.13	4.42	1.09	1.02
3 nm	1.41	NA	2.35	1.81
Threshold Voltage (V)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	10.26	-0.58	4.26	-3.94
3 nm	9.05	NA	0.36	0.54
I_{on}/I_{off}				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	3.38E+05	6.69E+04	9.54E+06	9.54E+05
3 nm	6.31E+06	NA	7.94E+06	6.77E+06

Annealing helped to significantly improve the device characteristics of the 1 nm capped device. The mobility practically returns to its original value, while the subthreshold swing even improves compared to the original value. On this occasion, instead of oxygen diffusing from IWO to Al_2O_3, oxygen diffuses from air to Al_2O_3 to IWO as depicted in **Figure 4-1** a(I). This reduces the number of oxygen vacancies and reduces the number of dangling bonds in the semiconducting layer. The reduction in charge carriers is captured by the increase in the threshold voltage. However, it is still 6V less than its original value. This indicates that the total number of charge carriers in the semiconducting layer is still

more than the original device. With less charge trap states, the mobility elevates despite the fall in charge carriers. The improved subthreshold swing implies that the semiconductor/dielectric interface is of an even higher quality compared to the original device. This suggests that any other defects that were present at the interface were also annealed away in this step.

For the 3 nm capped device, transistor behavior was restored after annealing. However, the threshold voltage was 8.69 V lower than the original device; this indicates that the number of charge carriers in the semiconducting layer was still much higher than the original device. With more oxygen vacancies in the channel layer, it is likely that the number of dangling bonds present at the semiconductor/dielectric interface was significant, resulting in 1.6 times higher subthreshold swing. However, the mobility for the 3 nm-capped devices was restored, likely aided by the higher number of charge carriers in the channel layer.

4.3.3 Effect of post-capping annealing for the 5, 7 & 9 nm-alumina capped devices

For the 5,7 and 9 nm capped devices, post-capping annealing was unable to re-establish transistor performance. However, observations drawn from these results strongly correlate with what occurred for the 1 and 3 nm capped devices. For the 5, 7 & 9 nm-capped devices, post-capping annealing reduced the on the current of the conductive devices (**Table 4-5** and **Figure 4-11**). This substantiates the observation that annealing reduces the number of oxygen vacancies and hence, the number of charge carriers in the semiconducting layer.

Table 4-5: Change in I_{on} of 5,7,9 nm capped devices

Capping Thickness	Ion (A) after capping	Ion (A) after annealing	Ion (A) after one week
5 nm	7.22E-05	6.88E-06	1.17E-05
7 nm	9.45E-04	1.44E-05	5.45E-05
9 nm	9.45E-04	2.86E-05	2.86E-05

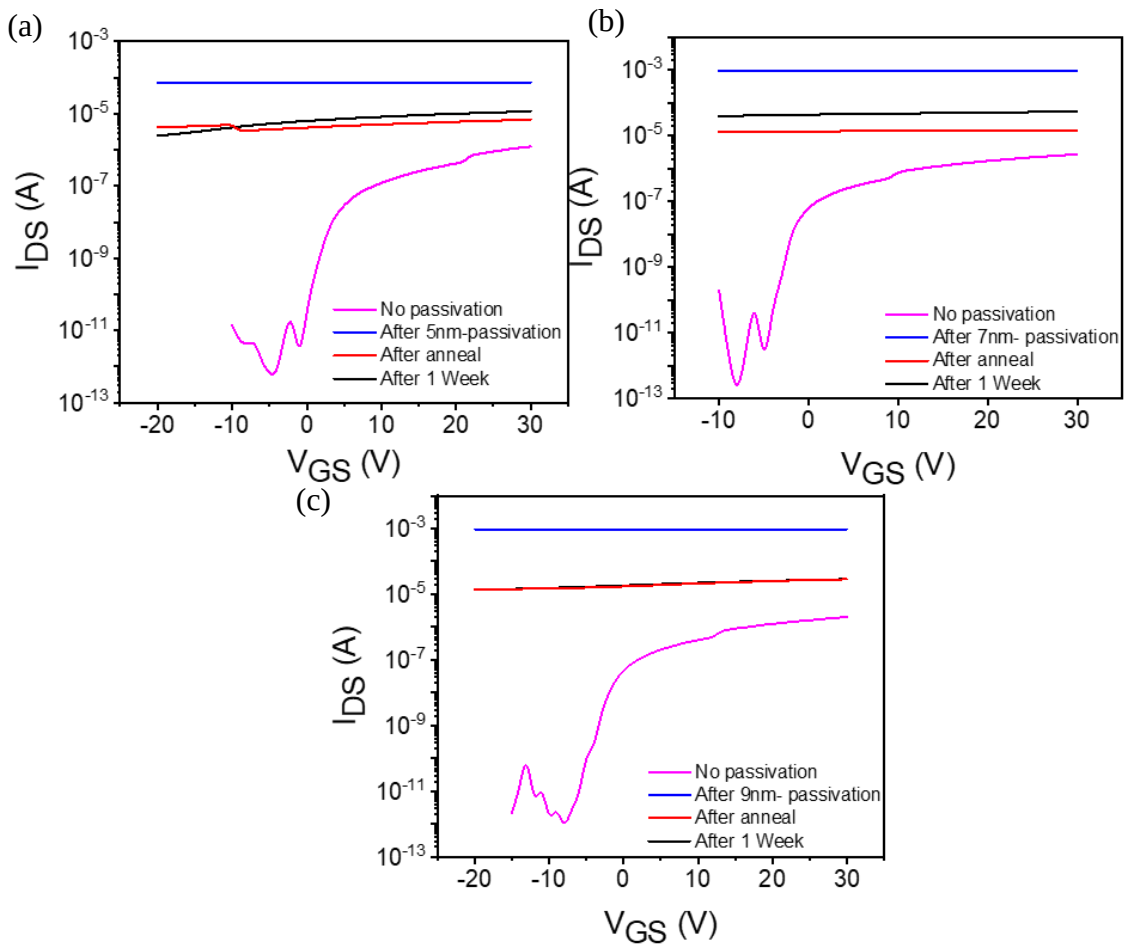

Figure 4-11: Transfer characteristics of the (a) 5 nm-alumina-passivated device (b) 7 nm-alumina-passivated device (c) 9 nm-alumina-passivated device. W=400 μm, L=800 μm V_{DS}=1V.

4.3.4 Summary and Conclusion

The 5,7 and 9 nm capped devices did not show promise as they are conductive even after post-capping annealing. Both the 1 nm-capped and 3 nm capped devices both have potential in capping layer studies. the stability of the devices needs improvement as their electrical properties after one week do not match closely with their original electrical properties or after annealing electrical properties. However, these devices have much more environmental stability than an uncapped layer. For example, after one week, there is a deterioration in the mobility of both the 1 and 3 nm capped devices (**Table 4-4**). Hence, to

identify the better capping conditions, further experimentation was performed for the 1, and 3 nm capped device.

4.3.5 Use of oxygen-rich Alumina as capping layer

In order to differentiate the 1 and 3 nm capped devices, the capping layer deposition process was altered. On this occasion, during sputter deposition of the capping layer, 1sccm of oxygen flow was utilized, with an intent to decrease the diffusion of oxygen from the channel to the capping layer. Providing more oxygen while forming the film will provide enough oxygen to the alumina layer hence decreasing the oxygen affinity of it. Hence, enabling more control on the device electrical properties.

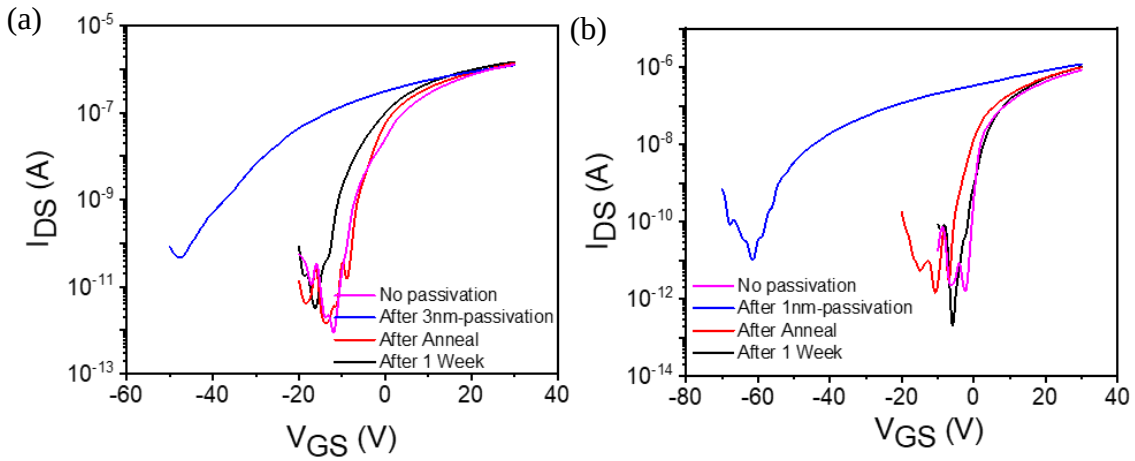

Figure 4-12: Transfer characteristics of alumina-capped devices fabricated with an oxygen flow rate of 1sccm, with a thickness of (a) 3 nm (b) 1 nm.

Overall, the 1 sccm of oxygen rate used during Al_2O_3 deposition enhanced the performance of the capping layer. Unlike the previous experiment where the 3 nm-capped device exhibited conductive behavior, for 1sccm flow rate, the device retained transistor behavior (**Figure 4-12** a). This showed that by flowing in oxygen during Al_2O_3 deposition, the extent of oxygen vacancy creation in the channel layer could be reduced. There are two possible mechanisms to explain this effect. First, by flowing in oxygen, the extent of oxygen incorporation into the capping layer can be increased. With more substantial oxygen content in the capping layer, the difference in concentration of oxygen between the channel and capping layer would be reduced. Hence, the driving force of oxygen diffusion from the

channel layer to the capping layer would be diminished. This means that fewer oxygen vacancies would be created after capping layer deposition. Alternatively, by flowing in oxygen during Al_2O_3 deposition, the oxygen content in the channel layer can be increased. Higher oxygen content in the channel layer would offset the effect of oxygen diffusion from the channel layer to the capping layer, reducing the number of oxygen vacancies created.

Table 4-6: Electrical parameters of 1/3 nm alumina capped devices deposited with an oxygen flow rate of 1sccm

Mobility (cm^2/V.s)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	7.83	6.67	8.34	9.15
3 nm	9.98	6.27	9.87	9.73
Subthreshold Swing (V/dec)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	0.84	3.59	1.29	1.63
3 nm	1.7	8.21	1.5	2.1
Threshold Voltage (V)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	9.61	-3.95	7.29	9
3 nm	2.84	-7.44	3.6	0.66
I_{on}/I_{off}				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	8.42E+05	1.32E+05	9.81E+05	2.53E+07
3 nm	2.97E+06	2.72E+04	9.89E+05	6.99E+05

In terms of electrical performance, differences can be observed in the after one-week device characteristics. Compared to the previous experiment, the mobility values remained closer to it's after annealing values (**Table 4-4**& **Table 4-6**). The after one-week threshold voltages also remained relatively close to the original device threshold voltages (**Table 4-6**). Importantly, for the 3 nm-capped devices, it's after one-week mobility was practically the same as its original mobility (**Table 4-6**). While for the 1 nm-capped device (**Figure 4-12** b), its mobility increased after one week. In terms of the subthreshold swing, the 3 nm-capped devices performed better again. Comparing the original and after one-week values, the 1 nm-capped device's subthreshold swing doubled, but the 3 nm-capped device's subthreshold swing only increased by 1.2 times (**Table 4-6**). Hence, the 3 nm-alumina

capped device is concluded to be better than the 1 nm-alumina capped device. Higher thickness Al_2O_3 layer, however, still showed conducting behavior. This again is owing to the Al_2O_3 layer's augmented need of oxygen. Hence according to the Ellingham diagram, the bottom In_2O_3 channel layer is reduced in order to obtain more oxygen by Al_2O_3, generating more oxygen vacancies making the In_2O_3 more conducting.

4.3.6 Extending the concept of overlayer-based charge carrier modulation to another capping oxide

Another available overlayer capable of reducing Indium oxide, according to the Ellingham diagram, is SiO_2. 1 and 3 nm-thick SiO_2 were also investigated as possible, reducing capping layers. The device structure is the same as the one in **Figure 4-1** b.

The 1 nm SiO_2 capped device continued to exhibit transistor behavior after capping (**Figure 4-13** a), but the 3 nm SiO_2 capped device became conductive (**Figure 4-13** b). This observation is consistent with what was observed earlier for the initial alumina capping layer study. After one week, the device characteristics of both thicknesses changed. Both devices experienced a rise in mobility (**Table 4-7**). This could indicate that the SiO_2 capping layer was unable to prevent the adsorption of water into the channel, causing the creation of more free carriers with more free carriers, mobility was enhanced.

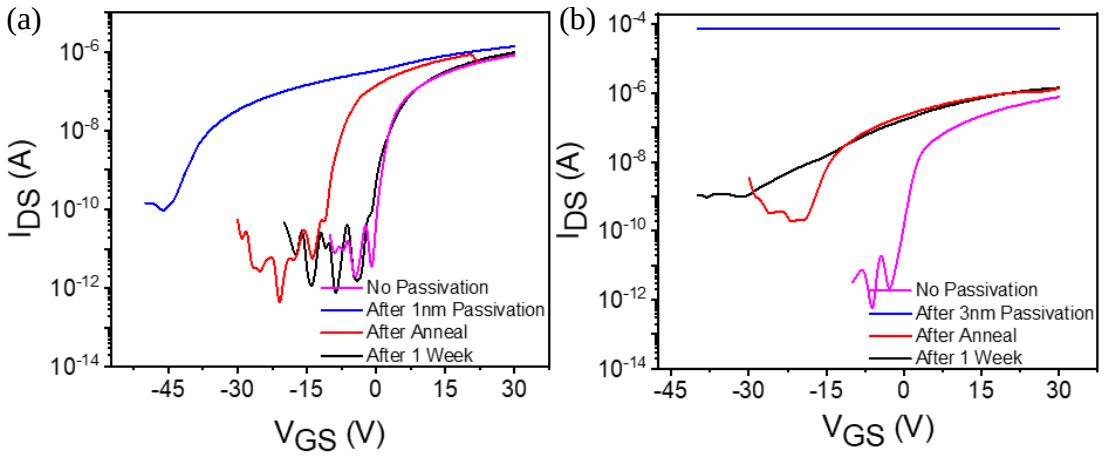

Figure 4-13: Transfer characteristics of SiO_2-capped devices fabricated with an oxygen flow rate of 1sccm, with a thickness of (a) 1 nm (b) 3 nm.

Table 4-7: Electrical parameters of 1/3 nm SiO_2 -capped devices fabricated with an oxygen flow rate of 1sccm

Mobility (cm^2/V.s)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	7	6.98	7.03	8.55
3 nm	7.72	NA	8.61	9.5
Subthreshold Swing (V/dec)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	0.99	4.24	1.6	1.43
3 nm	1.4	NA	2.66	13.63
Threshold Voltage (V)				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	7.56	-7.19	7.54	8.25
3 nm	10.72	NA	-2.55	0.05
I_{on}/I_{off}				
Capping Thickness	Original	After Capping	After Anneal	After 1 week
1 nm	1.13E+06	1.60E+04	5.61E+06	1.27E+06
3 nm	4.33E+06	NA	6.83E+03	1.65E+03

Considering the original and post-capping anneal characteristics, the 3 nm capped device suffered a significant drop in its I_{on}/I_{off} ratio (by three orders of magnitude), and its threshold voltage was negatively shifted (**Table 4-7**). For the 1 nm-capped device, its I_{on}/I_{off} ratio and threshold voltage returned close to its original value (**Table 4-7**). It is postulated that due to the longer deposition time of the 3 nm-capped device, the resultant plasma damage at the backchannel was more substantial. This resulted in a higher carrier concentration at the backchannel, causing a decrease in the threshold voltage [24]. These charge carriers are hardly depleted by negative gate voltages, causing a rise in the off-current, [24] depressing the I_{on}/I_{off} ratio. Hence, a 1 nm-SiO_2 capped device is determined to be better than a 3 nm-SiO_2 capped device. Although SiO_2 is placed above the Al_2O_3 in the Ellingham diagram, it is still capable of modifying device characteristics by reducing the semiconducting IWO.

4.3.7 Extending the concept of overlayer-based modulation to another semiconducting oxide

To prove that the capping layer selection for reducing semiconducting oxide layer of TFT devices using the Ellingham diagram is the universal method, capping for IGZO sputtered

enhancement-mode TFTwas employed. The thickness of the film was kept high so that the effect of oxygen vacancies created after alumina deposition was less at the interface of gate oxide and semiconductor.

Modulation of Oxygen-rich IGZO device

By inserting more oxygen ($Ar:O_2$ = 4:1) in the preparation of the IGZO film, the inherent oxygen vacancies present in the oxide are decreased, making it very less conducting and confining its operation to deep enhancement mode. Demonstrating that the threshold voltage and mobility of these films also changed, would strengthen our hypothesis of the use of Ellingham diagram for an oxide semiconductor reduction. **Figure 4-14**a shows the device structure used for this experiment. **Figure 4-14**b gives insights as to how the transfer characteristics of oxide semiconductor changed after capping with Alumina. **Table 4-8** details the parameter values before and after capping.

A substantial improvement in the threshold voltage can be seen. Mobility improvement is low as there were more scattering sites present in the unannealed IGZO sample, probably because of the unstructured pure amorphous film formed due to non annealed/less annealed samples. With temperature, atoms rearrange themselves thus improving bonding and semiconductor-dielectric interface.[31]

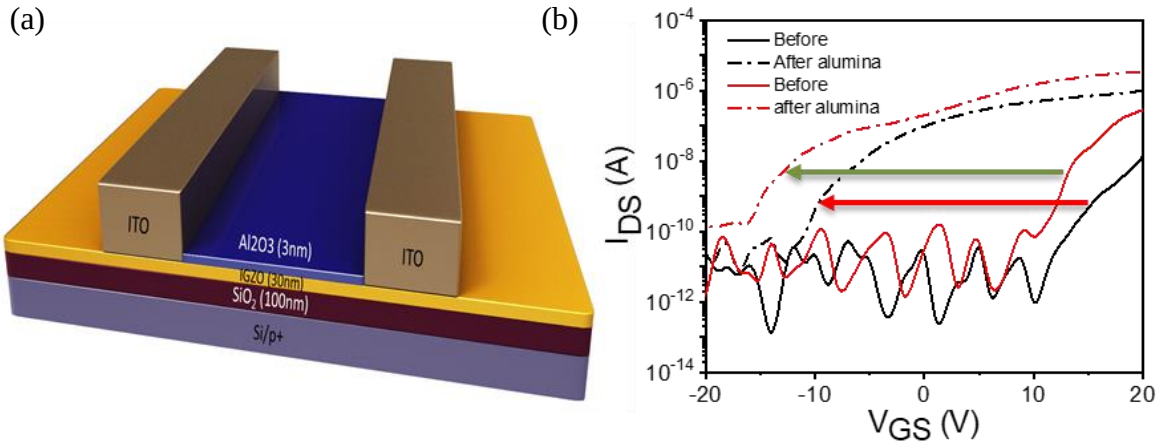

Figure 4-14: (a) IGZO TFT in less conducting state capped with sputtered alumina (b) change in transfer characteristics before and after alumina deposition. W=400 μm, L=800 μm V_{DS}=1V.

Table 4-8: Enhanced IGZO TFT manipulation

Parameter	Before	After Alumina sputtering
Mobility ($cm^2/V.s$)	0.18, 0.19	0.35, 0.48
V_{th} (V)	21.42,16	9, 2.02

Experiments on reducing IGZO with highly reducing metal Calcium were also performed. Calcium was deposited between the source and drain electrode for further reduction of IGZO. The details of the experiment and analysis are in appendix information (**Figure A-4**,**Table A-1**). Massive improvement in mobility and shift in threshold voltage was observed as the IGZO layer gets reduced by the Ca layer transforming Ca to CaO. The results were not included in this chapter as some unknown mechanism will be present as the channel created in the TFT will get affected by the changes in density of states occurred by deposited metal, Also if the Ca is not entirely oxidized at the interface then there is possibility of electrons flowing through the metal as well as the channel.

4.3.8 Additional use of capping layers to achieve device environmental stability

As discussed in the literature review, for TFTs, the effect of the environment on the channel layer can be detrimental to its electrical performance. Both oxygen and water vapor have the capacity to affect device performance. Adsorbed oxygen on the semiconducting layer would reduce oxygen vacancies and thus reduce the number of charge carriers, causing a positive shift in V_{th} [25], [26], while adsorbed moisture at the back surface of the channel forms H_2O^+, which acts as an electron donor [27]. With more electrons in the channel, V_{th} would be negatively shifted. In a humid environment like Singapore (humidity always >50%) negative shift in the characteristics is routinely observed, indicating that the effect of water is more pronounced.

Figure 4-15 compares an un-capped device after fabrication and after 1 week. Based on the properties of an un-capped TFT measured after one week, it was noted that the device mobility had doubled, and its threshold voltage negatively shifted by 12.1V (**Table 4-9**). This observation indicates that there was a large extent of water adsorption on the channel layer, which created more charge carriers, causing mobility to rise, and the threshold

voltage to fall. Hence, capping the layer as an overlayer on top of the IWO channel will provide an additional advantage of environmental stability.

Table 4-9: Electrical parameters of an un-capped device

Mobility ($cm^2/V.s$)		Subthreshold Swing (V/dec)		Threshold Voltage (V)		Ion/Ioff	
Original	After-1week	Original	After-1 Week	Original	After1 Week	Original	After1 Week
9.22	18.5	1.11	2.25	2.85	-9.24	3.45E+06	2.56E+07

Selection of best capping layer material and thickness for environmental stability

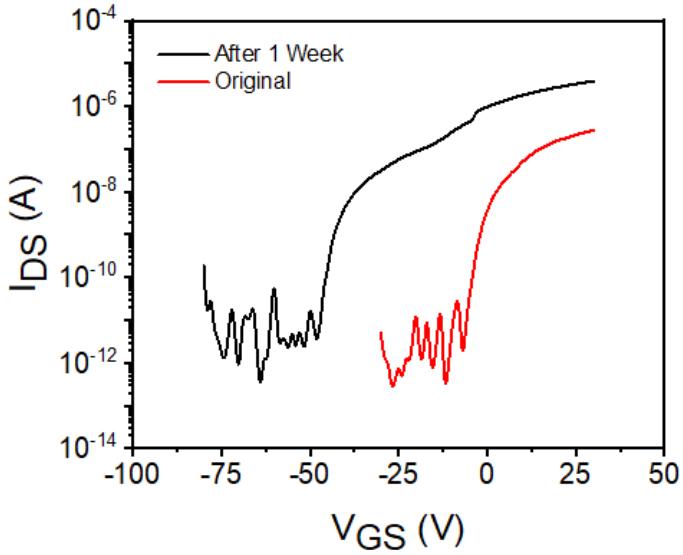

Figure 4-15: Transfer characteristics of an un-capped device. W= 400 µm, L= 800 µm V_{DS}= 1V.

The critical difference in the performance of the 3 nm-Al_2O_3 capped device compared with the 1 nm-SiO_2 capped device lies in the after one-week mobility. While the mobility of the 3 nm-Al_2O_3 capped device remains close to its original value (**Table 4-6**), the mobility of the 1 nm-SiO_2 capped device increases by 22% (**Table 4-7**). This shows that the 3 nm-Al_2O_3 capping layer is better able to shield the channel layer from the environment, particularly moisture. This is supported by other researchers who reported a Water Vapour Transmission Rate (WVTR) of 1-3x10^{-2} g/m^2/day for sputtered alumina [28], [29] and a WVTR of 4.2-7.6x10^{-1} g/m^2 for sputtered SiO_2 [30]. A 3 nm thick Al_2O_3 is thus selected as the best capping layer.

4.3.9 Summary and conclusion

Utilizing the best capping material and optimized thickness, it has been demonstrated that capping can be used to modulate device parameters athermally as well as to enhance environmental device stability, compared to an un-capped device. The measured properties of an un-capped TFT after one week displayed a drastic shift in the device's mobility and threshold. This observation indicates that there was a large extent of water adsorption on the channel layer, which created more charge carriers, causing mobility to rise, and the threshold voltage to fall. The fact that for an un-capped device, its threshold voltage negatively shifted by 12.1 V, while for a device with a 3 nm-thick Al_2O_3 capping layer selected using Ellingham diagram deposited with an oxygen flow rate of 1sccm, its threshold voltage only negatively shifted by 2.94V, proves that by depositing 3 nm of alumina as a capping layer, device stability, as well as performance, can be improved. Further experiments performed on the IGZO as channel layer and with alumina, SiO_2 and Ca capping layers proves that this method is universal. Ellingham diagram can thus be a very useful tool in flexible device fabrication, which requires a lower thermal budget and can pave the way for CMOS circuitry using oxide semiconductors.

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Chapter 5 *#

Surface chemical treatments for charge carrier modulation in oxide semiconductors

On-demand modulation of conductance of semiconducting devices is an additional requirement in applications such as neuromorphic electronics, logic gates, etc. However, the conventional annealing processes change the properties of all the TFTs on a given substrate and are unable to modulate the conductance of each device independently as required by these applications. This chapter proposes the use of two distinct chemical surface treatments as an alternative to achieve a selective on-demand alteration of TFT characteristics. In the first technique, the possibilities of charge carrier modulation were studied by grafting multiple self-assembled monolayers (SAMs) such as silane, thiol, amine-group polymers, and dopant molecules on the IWO channel layer. The second technique investigates surface chemical treatment to achieve oxygen vacancies reduction through wet chemical oxidation, thereby altering the electrical properties of semiconductor for TFT. Various material characterization techniques such as XPS, UPS, coupled with electrical characterizations were used to endorse the effect of surface chemical treatments on TFT.

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*# This chapter is currently being prepared in two manuscripts as * Kulkarni Mohit Rameshchandra, et al. “Novel universal molecular surface engineering of an oxide semiconductor for on-demand modulation of devices for flexible logic gates and neuromorphic devices,” (2019) and # Kulkarni Mohit Rameshchandra, et al. “Hydrogen peroxide assisted wet chemical treatment as a route for controlled passivation of oxygen vacancies for flexible thin-film transistor application” (2019).

5.1 Introduction

In this section, two surface treatment strategies (**Figure 5-1**) to modify charge carrier concentration in the oxide semiconductor will be introduced. One will cover SAMs, and other surface doping treatments and subsequently wet chemical oxidation treatment will be introduced.

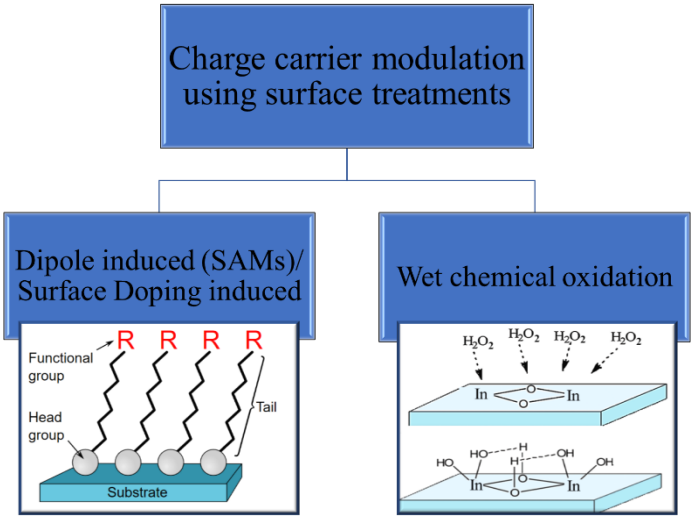

Figure 5-1: An Overview of surface treatments for charge carrier modulation.

Dipole induced/ Surface Doping induced: Previously, researchers have explored various chemical and physical treatments in organic devices in order to improve contact resistance between organic film and electrode.[1], [2] It helped to improve weak charge injection, a factor which severely limits the OFET performance.[3] Contact engineering for achieving ohmic contact became an important area of research in organic semiconductor devices such as TFT's [1], LED's [2], [4], solar cells.[5]–[9] The contact engineering of metal or transparent conducting oxide is typically achieved through alteration of work function, modulating surface energies, creating an internal electric field (dipole creation) to drive charge carriers to drift to the surface quickly or through charge transfer kinetics (surface dopant mediated charge transfer). Such surface modifications are achievable through physical and chemical surface treatments. The physical treatments include surface oxidation using Plasma etching, UV-ozone treatment, and Ar sputtering.[1] Moreover, the chemical treatments include surface treatments using organic SAM, wet inorganic

treatments such as acids, bases, and oxidants, other organic layers capable of creating dipoles or surface doping. [10]

The techniques were developed primarily for the conducting oxides, tackling the semiconductor-electrode interface to improve charge injection. However, efforts in the direction of changing the attributes of oxide semiconductor channel itself were negligible [11] even though it would be extremely beneficial to devise the ability to modulate the properties of semiconductor to achieve desired characteristics of oxide TFTs. Moreover, this is especially relevant in the era of flexible electronics, where the low-temperature processes become more critical. The thicker oxide semiconducting layers will be an important limiting factor for developments in this direction. As the oxide semiconductor used for this chapter is very thin (<10 nm), the surface treatments performed affect favorably on the work function of the channel formed near gate insulator during TFT operation. In general, work function change in oxide is attributed to change in surface dipole and Fermi level pinning at the surface due to surface adsorbed species.[4] Therefore, successful external surface modifications of the oxide semiconductor would achieve higher mobilities and unlock more ways to modulate the threshold voltage. The higher mobility is useful for faster speed of operation, which is useful in applications such as the backbone electronics of displays, and establishing better fabrication control is useful for building logic circuits. The chapter incorporates various electrical characterization and material characterization techniques such as XPS, UPS, FTIR to endorse the effect of surface modification.

Wet Chemical oxidation: As the interest in flexible and transparent electronics increases, the demand for high-performance amorphous oxide thin film transistor with the capacity to be processed on plastic substrates with low-temperature handling capabilities have increased. Studies have shown that the Indium-based semiconductors exhibit very high mobility; hence, they are of more interest. According to researchers, ions of a heavy transition metal cations such as Indium act as a high mobility matrix owing to unoccupied s - orbitals.[12]–[14] The origin of this property can be attributed to the edge-sharing polyhedral structure.[15] Hence, the matrix of Indium becomes unique for the doping

system providing higher mobility and carrier concentration due to the presence of oxygen vacancies.[16] However, the presence of excessive oxygen vacancies makes the TFT unstable and irreproducible. The high carrier concentration also results in highly negative threshold voltage of the device, requiring high-temperature annealing to reduce the concentration of oxygen vacancies.[17] However, for the use of flexible substrates (restricting the thermal budget), it is necessary to find athermal ways to decrease the oxygen vacancies so as to control the threshold voltage of the devices.

Hydrogen peroxide is an well established oxidizing agent in many areas including photocatalysis[18], as gate oxide treatment to improve device performance[19], [20], [21] and for controlling the conductivity of ZnO thin films[22]–[25], nanorods[26], [27]. The exploration of the effects, in terms of the attributes of TFT, is limited, except for few solution-processed TFT[28], [29] where H_2O_2 was used as an additive in precursor solution to improve the device performance by facilitating complete reaction and annihilation of carbon compounds present in the film at the time of fabrication. Therefore, the study of the effect of passivation of oxygen vacancies using hydrogen peroxide on TFT becomes essential. It will pave the way in the replacement of the high-temperature annealing process with simple H_2O_2 oxidation to neutralize the high conductance in thin-film transistors to enable a shift from depletion-mode operation to low voltage enhancement mode operation. Precise control of conductance value can also be useful in applications such as neuromorphic electronics and synaptic devices. The chapter investigates the effect of this oxidation on the IWO TFT devices in terms of TFT parameters such as mobility and threshold voltage, stability, the effect of time of deposition on TFT parameters. Then the films were characterized by XPS, UPS, UV-VIS, CV-measurement to create Mott–Schottky plot, PESA.

5.2 Use of SAMs for surface treatment to induce charge carrier modulation

As mentioned earlier, it is well known that by forming surface dipoles, SAMs change the working function of both metals and semiconductors. [1], [2], [30], [31] There will always be an inevitable interfacial charge transfer that can occur when silane binds to the metal/

semiconductor surface. [32] Consequently, the post-treatment measurement of resulting work function change helps to quantify SAM treatment in terms of band edge offset from Fermi level and correlates with modified carrier concentration levels of the semiconductor. UPS was used to measure the change in work function, while XPS validated the film formation through composition analysis. TFT characteristics were measured to probe the effect of dipole creation on the electronic semiconductor state before and after the treatments. To examine the effect of solvent, studies were carried out using the pure solvent (ethanol) under identical duration and dipping conditions at the same time. No changes were observed on the device performance and hence it was concluded that the solvent induced effects are absent during SAM treatments. The transfer characteristics data before and after treatment is depicted in appendix information (**Figure A-10**).

5.2.1 (3-Aminopropyl)triethoxysilane (APTES) treatment

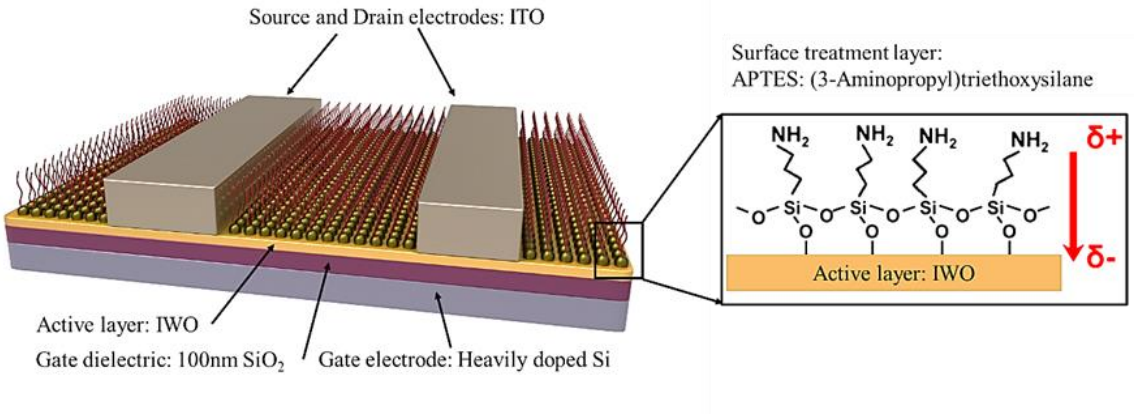

Figure 5-2: Schematic diagram of surface modification of IWO bottom gate-top contact TFT using APTES treatment.

The preparation of IWO TFT is already explained in the experimental section. The APTES treatment was done by dipping IWO-TFT in freshly prepared APTES solution (1:10vol ratio with ethanol and later washed with ethanol). The SAM layer was formed on the surface IWO through the hydrolysis process of triethoxy groups in APTES and hydroxyl groups. The layer formation is shown in **Figure 5-2**. A surface sensitive techniques, XPS was used to crosscheck the formation of the film.

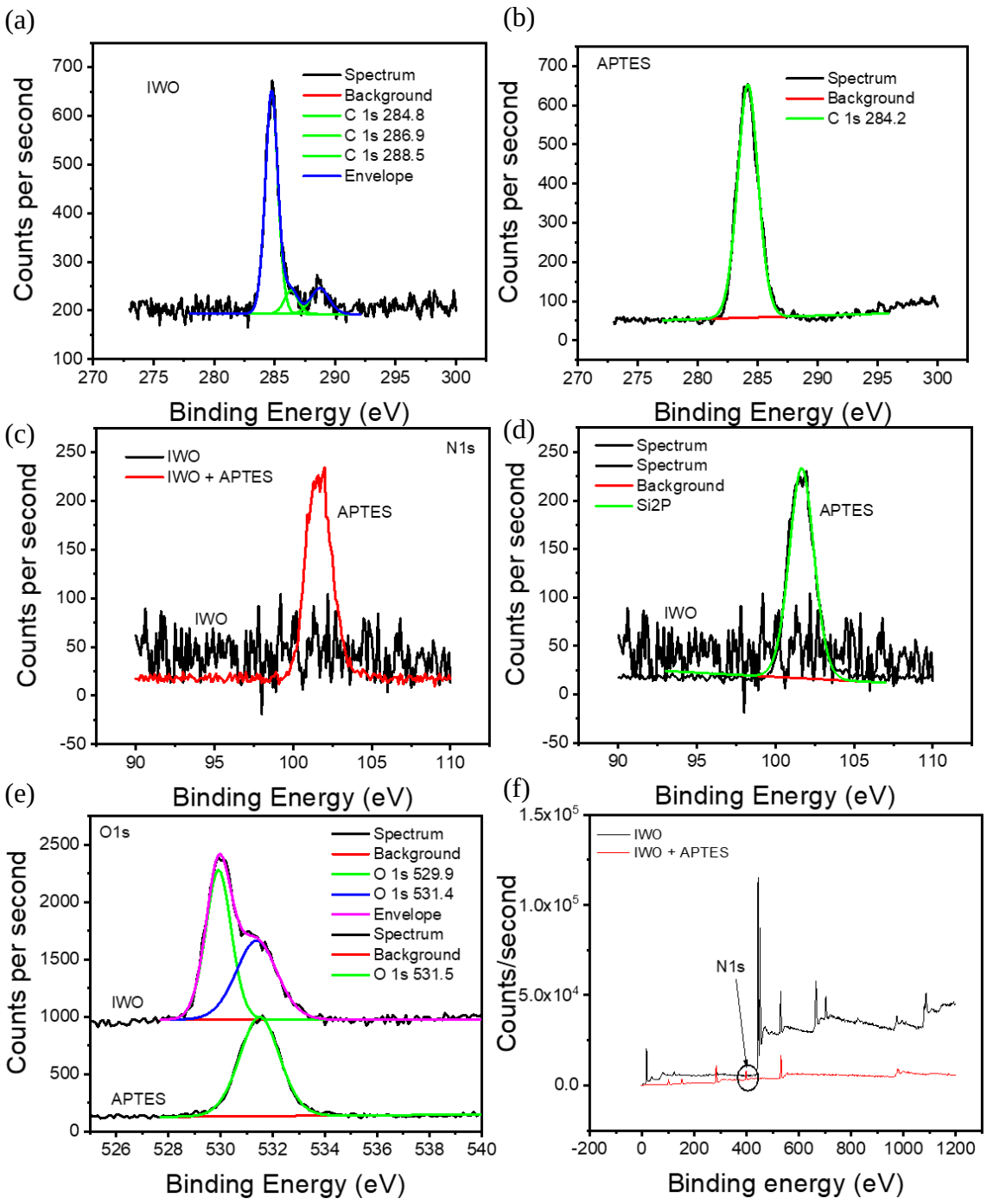

Figure 5-3: (a) C1s peak for IWO (b) C1s peak after APTES treatment (c) N1s peak with the without APTES treatment (d) Si2p peak with the without APTES treatment (e) O1s peak with the without APTES treatment (f) wide scan of film with the without APTES treatment.

Figure 5-3 depicts the comparison of the surface before and after two days of APTES treatment. **Figure 5-3** (a) C1s peak for IWO, this adventitious carbon peak is observed due

to various surface contaminations such as hydrocarbons due to ambient exposure or from oil diffusion vacuum pumps.[33] The first peak at 284.75eV confirms the presence of C-C bond, the next peak at 286.37eV confirms C-O-C bond and peak at 288.74eV confirms O-C=O bond present in hydrocarbon. Whereas, C1s peak (**Figure 5-3** (b)) after APTES treatment shows only the presence of C-C bond present in the alkyl groups. **Figure 5-3** (c) and (d) also clearly show the Formation of APTES with N1s peak resulting from -NH_2 and Si2p peak resulting from Si present in Silane whereas untreated samples do not show any presence of such compound. **Figure 5-3** e and f demonstrate O1s peak of the surface with and without APTES treatment. It can be noted that only the 531.38 eV O1S peak corresponding to M-O-M bond is present; the absorbed oxygen or oxygen vacancies peak present at 529.92eV for an untreated sample is not present in APTES treated sample. **Figure 5-3** (f) shows a wide scan of film with the without APTES treatment; it can be seen that the APTES treated IWO film shows shrunk In 3d or W 4f peak.

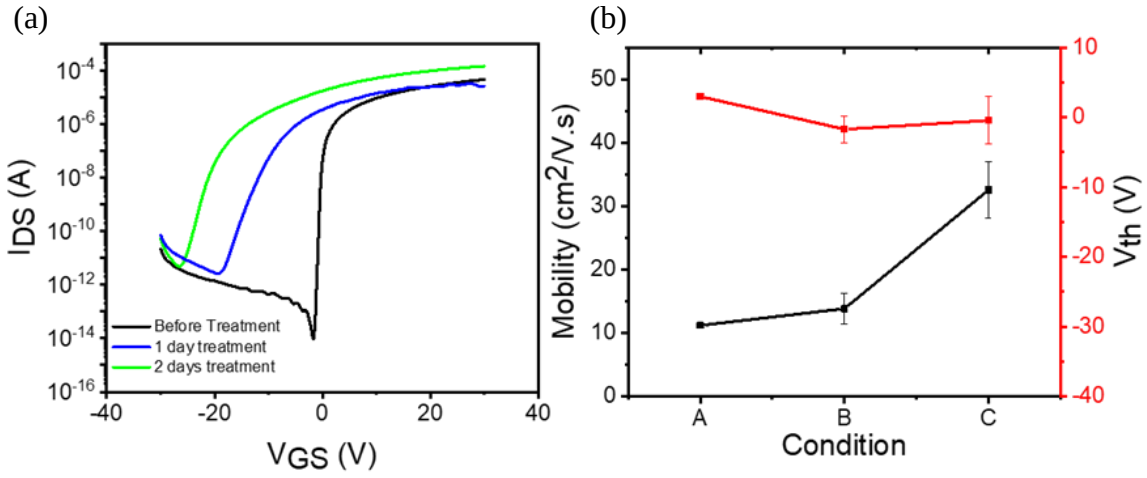

Figure 5-4: (a) APTES treatment with a drain voltage of 1V (b) variation of mobility and threshold voltage concerning treatment. A is before treatment, B is one day of treatment C is two days of treatment. W=1000 µm, L=250 µm V_{DS}=1V.

Figure 5-4a depicts the transfer characteristics of IWO TFT before and after APTES treatment. The devices were measured after one day of dipping in APTES, two days of dipping in APTES solution. The shift in the transfer characteristics is apparent. The mobility and threshold voltage variation is shown in **Figure 5-4** b. It is evident that the APTES treatment improves mobility and decreases the threshold voltage. The mobility

improves with more duration of treatment. It is successfully demonstrated that the attributes of TFT can effectively be modulated by dipole induced charge carrier modulation technique of self-assembled monolayer of Silanes.

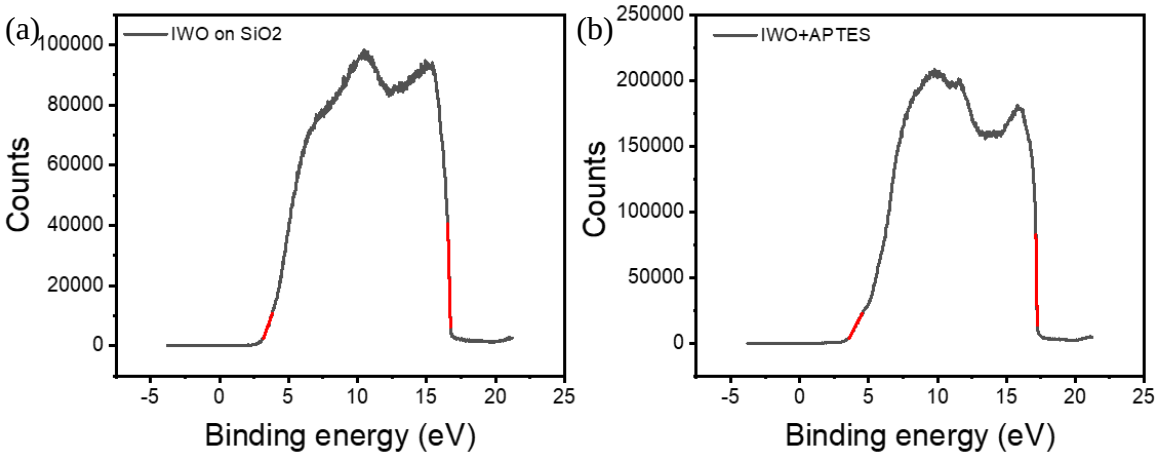

Figure 5-5: UPS to find work function and ionization potential of IWO (a) before and (b) after APTES treatment.

To further confirm that the modification indeed changes the electronic properties of the semiconductor, a UPS was performed. UPS result displayed in **Figure 5-5** was used to investigate the shift in work function and ionization potential of IWO by the APTES modification. The energy of He(I) photon source used for measurement is 21.2 eV. The HOMO energy level of IWO shifted from 2.8 eV to 3.42 eV; the secondary electron cut off energy shifted from 16.6 eV to 17.27 eV. The work function and ionization potential (VBM) changed from 4.61 to 3.94 eV and 7.40 to 7.36 eV, respectively, after APTES treatment. **Table 5-1** summarizes the changes after the treatment. Work function corresponds to Fermi level in the semiconductor. Hence decrease in fermi level indicates increased free electrons in the conduction band, which is observed in terms of change in device parameters, namely, increased mobility, increased off current and negatively shifted threshold voltage. This proves the doping of oxide semiconductor was successful.

Table 5-1: Work function and ionization potential derived from UPS

Surface	Energy of He	E_{homo}	E_{seco} (Secondary electron cut off energy)	Work function	Ionization potential
	B (eV)	C (eV)	D (eV)	B-D (eV)	B-D+C (eV)
IWO	21.2	2.8	16. 6	4.61	7.4
APTS	21.2	3.42	17.27	3.94	7.36

Based on the APTES's ability to change the semiconductor properties and control the TFT parameters, more surface treatments were briefly tested. The surface treatments were performed using chemicals such as 1-Dodecanethiol (DDT); 1H,1H,2H,2H-Perfluorodecanethiol (PFDT); Triphenylphosphine oxide (TPPO), Polyethylenimine (PEI) and polyethylenimine-ethoxylated (PEIE) and the results are discussed below.

5.2.2 1-Dodecanethiol (DDT) treatment

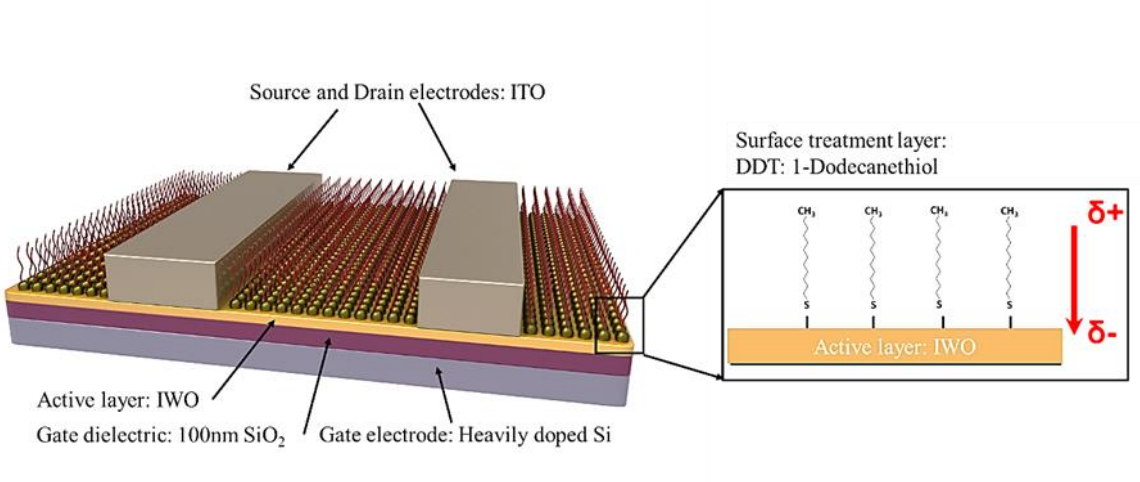

Figure 5-6: Schematic diagram of surface modification of IWO bottom gate-top contact TFT using DDT treatment.

Following Silane, Thiols are the another well studies molecules for the formation of the SAM layer. 1-Dodecanethiol was preferred because of its long chain, which restricts the interference of end group. The DDT treatment was done by dipping IWO-TFT in freshly prepared DDT solution (50hrs in a 12 mM ethanol solution and later washed with ethanol). The SAM layer was formed (**Figure 5-6**) on the surface IWO through the chemisorption of thiol head group on the surface of the oxide. XPS was done to crosscheck the formation of the film.

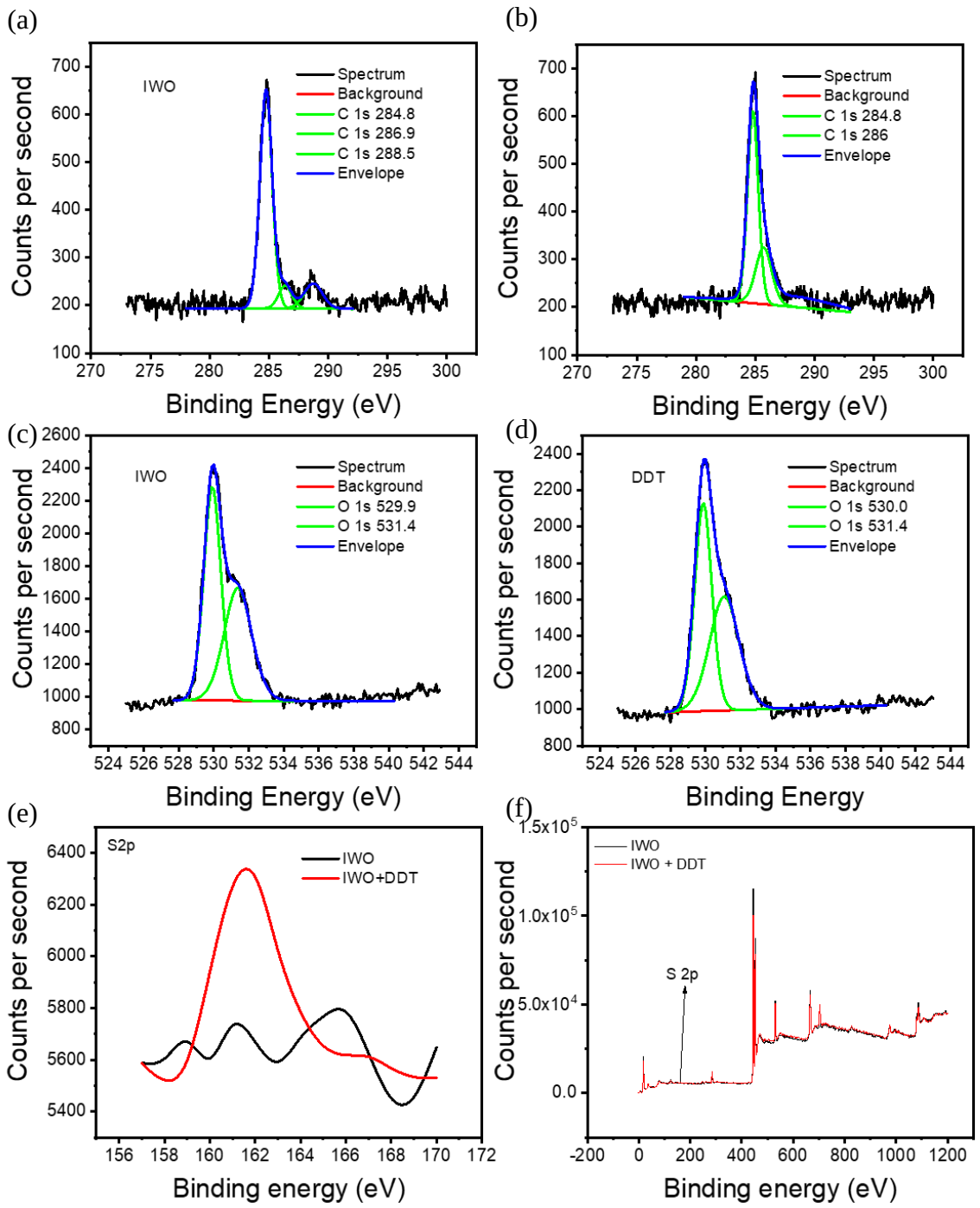

Figure 5-7: (a) C1s peak for IWO (b) C1s peak after DDT treatment (c) O1s peak without DDT treatment (d) O1s peak with the DDT treatment (e) S2p peak with and without DDT treatment (f) wide scan of film with the without DDT treatment.

Figure 5-7 depicts the comparison of XPS of the surface before and after two days of DDT treatment. **Figure 5-7** (a) gives Carbon (C1s) peak for IWO is deconvoluted as follows.

The first peak at 284.75eV confirms the presence of C-C bond, the next peak at 286.37eV confirms C-O-C bond and the peak at 288.74eV confirms O-C=O bond present in hydrocarbon. C1s peak (**Figure 5-7** (b)) after DDT treatment shows the primary presence of C-C bond from the alkyl groups with a percentage area of 73% and remaining area for the C-O-C bond maybe because of the previously adsorbed species. **Figure 5-7** (c) and (d) demonstrate the O1s peak of the surface with and without DDT treatment. It can be noted that only 531.38 eV O1S peak corresponding to M-O-M bond is present the absorbed oxygen or oxygen vacancies peak present at 529.92eV for an untreated sample with percentage area of 54.13% and 45.87% respectively and treated sample with 51.13% and 48.33%. This decrease can be due to the adsorbed Sulphur on the sample masking the M-O-M bond, allowing to have more percentage area for the adsorbed oxygen-oxygen vacancies peak. **Figure 5-7** (e) clearly shows the presence of DDT with S 2p peak resulting from sulfur in thiol, whereas untreated samples do not show any presence of such compound. **Figure 5-7** (f) shows a wide scan of film with the without DDT treatment; it can be seen that the DDT treated IWO film shows shrunken In 3d or W 4f peak which indicates the DDT film formation as the formation on the IWO surface, reduces the photoelectrons collected by surface-sensitive XPS..

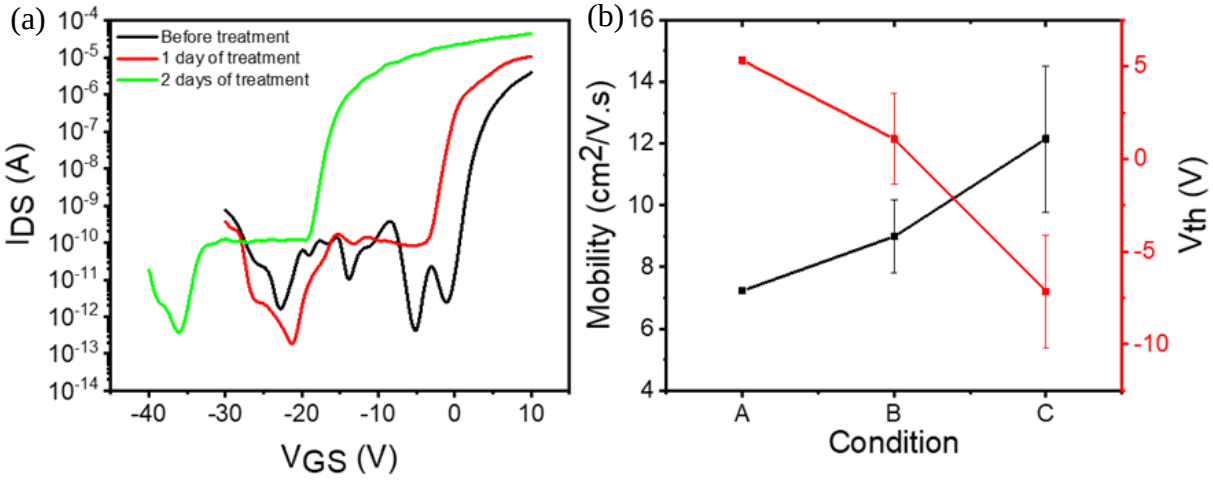

Figure 5-8: (a) Transfer characteristics before and after DDT treatment- A is before treatment, B is one day of treatment C is two days of treatment (b) mobility and threshold voltage before and after treatment. W=1000 µm, L=250 µm V_{DS}=1V.

Figure 5-8a depicts the transfer characteristics of IWO TFT before and after DDT treatment. The devices were measured after one day of dipping in DDT solution. The shift

in the transfer characteristics is apparent. The mobility and threshold voltage variations are shown in **Figure 5-8** b. It is evident that the DDT treatment improves the mobility and decreases the threshold voltage. The mobility improves with another day of treatment. It is successfully demonstrated that the attributes of TFT can effectively be modulated by dipole induced charge carrier using self-assembled monolayer with Thiol.

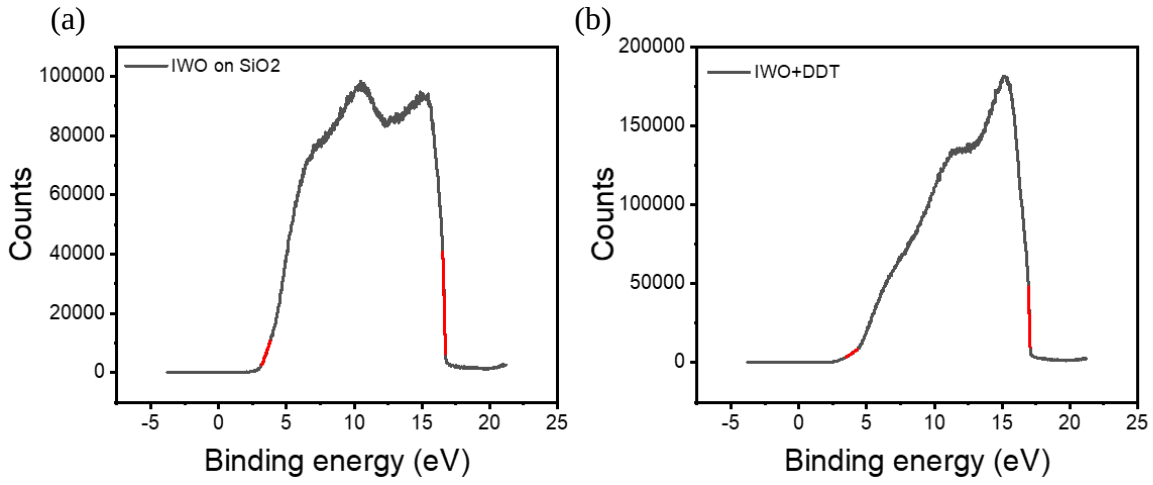

Figure 5-9: UPS before and after DDT treatment.

To further confirm that the modification indeed changes the electronic properties of the semiconductor, a UPS was performed. **Figure 5-9** compares UPS data for pristine, and DDT coated IWO film. From this figure, it is possible to calculate the shift in work function and ionization potential of IWO. The energy of He(I) used for measurement is 21.2 eV. The HOMO energy level of IWO shifted from 2.8 eV to 2.88 eV; The secondary electron cut off energy shifted from 16.6 eV to 17.10 eV. The work function and ionization potential (VBM) was changed from 4.61 to 4.1 eV and 7.40 to 6.98 eV, respectively, after DDT treatment. **Table 5-2** summarizes the changes after the treatment.

Table 5-2: Work function and ionization potential derived from UPS

Surface	Energy of He	E_{homo}	E_{seco} (Secondary electron cut off energy)	Work function	Ionization potential
	B (eV)	C (eV)	D (eV)	B-D (eV)	B-D+C (eV)
IWO	21.2	2.8	16. 6	4.61	7.4
DDT	21.2	2.88	17.10	4.1	6.98

5.2.3 1H,1H,2H,2H-Perfluorodecanethiol (PFDT) treatment

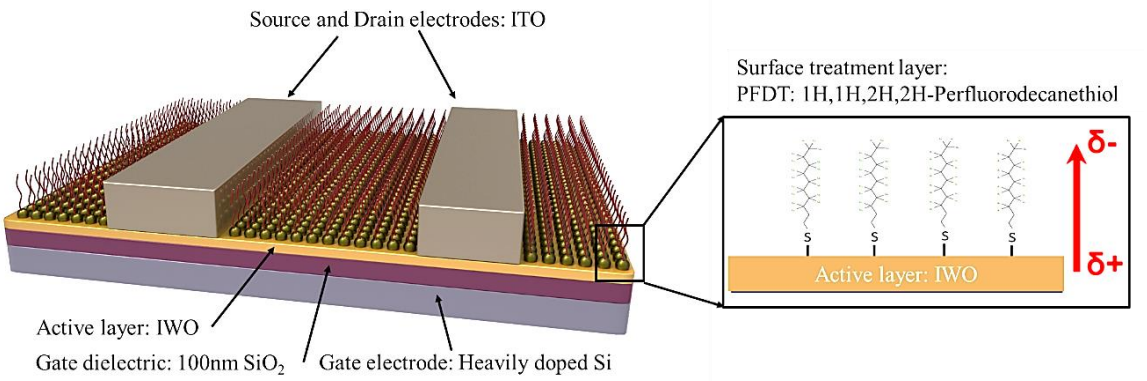

Figure 5-10: Schematic diagram of surface modification of IWO bottom gate-top contact TFT using PFDT treatment.

PFDT was chosen for this treatment because its long-chain will restrict the interaction from the end group. In addition,fluorine being an electron affinity element should be able to positively shift the threshold voltage, eventually hampering the mobility as well. The PFDT treatment was done by dipping IWO-TFT in freshly prepared PFDT solution (50hrs immersed in a 12 mM ethanolic solution, and later washed with ethanol). The SAM layer was formed on the surface IWO (**Figure 5-10**) through the chemisorption of the Sulphur head group on the surface of the oxide. XPS was done to crosscheck the formation of film. **Figure 5-11** depicts the comparison of XPS of the surface before and after two days of PFDT treatment. **Figure 5-11** (a) gives Carbon (C1s) peak for IWO is deconvoluted as follows. The first peak at 284.5eV confirms the presence of C-C bond the next peak at 285.3eV confirms C-O-C bond and peak at 288.4eV confirms O-C=O bond present in hydrocarbon. Whereas, C1s peak (**Figure 5-11** (b)) after PFDT treatment shows the primary presence of C-C bond (284.5 eV) from the alkyl groups, the C-O-C bond (285.3 eV) and O-C=O (288.4eV) bond present in hydrocarbon and at last another new peak is observed at 291.4 eV this peak corresponds to CF_2 bond which slightly electropositive carbon in CF2 due to electronegative F in the PFDT. **Figure 5-11** c and d demonstrate the O1s peak of the surface with the without PFDT treatment, shows a minor decrease in adsorbed oxygen peak. **Figure 5-11** (e) clearly shows the presence of PFDT with F1s peak resulting from fluorine in PFDT, whereas untreated samples do not show any presence of such compound. **Figure 5-11** (f) shows a wide scan of film with the without PFDT

treatment where the F1s peak is evident too.

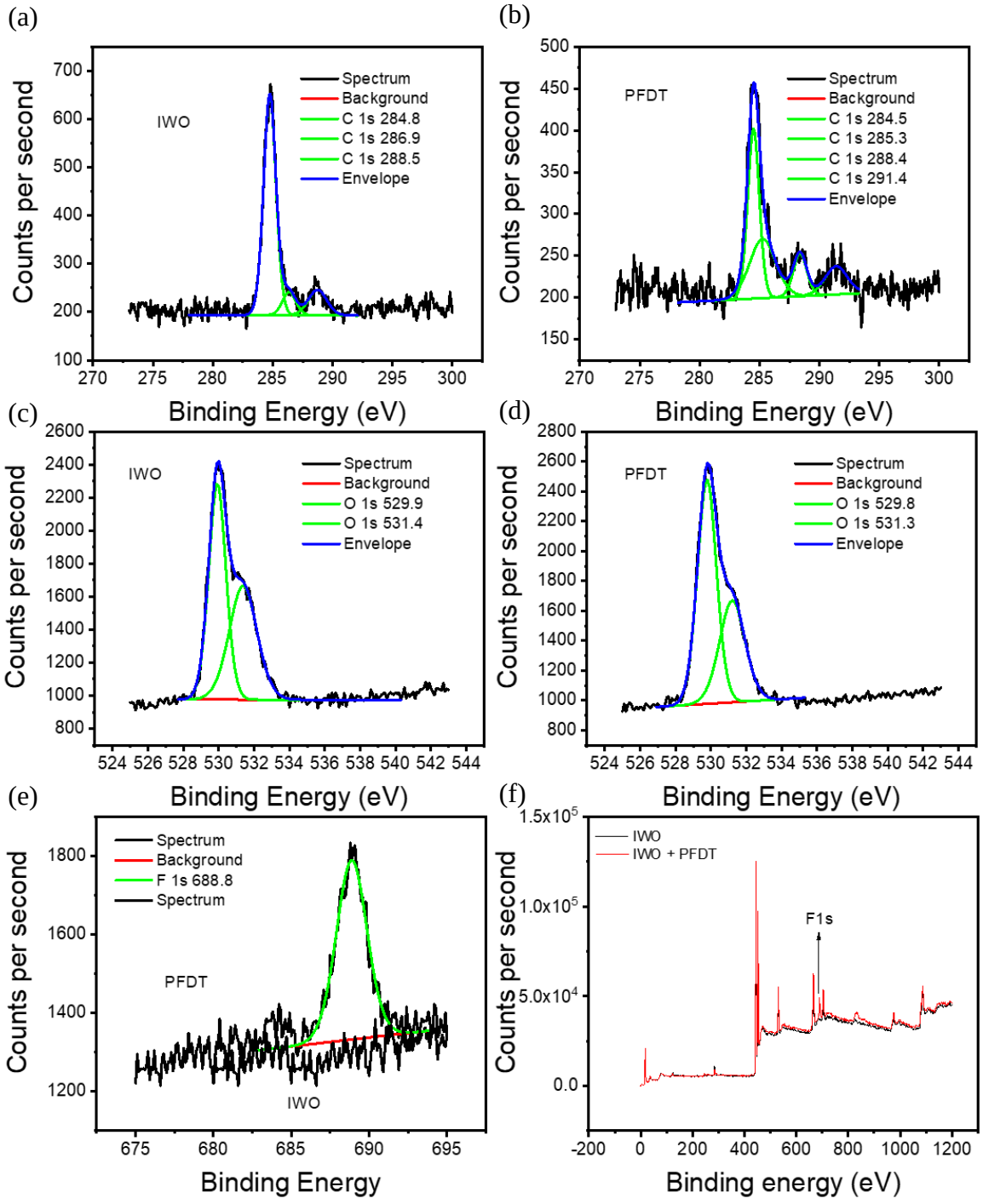

Figure 5-11: (a) C1s peak for IWO (b) C1s peak after PFDT treatment (c) O1s peak without PFDT treatment (d) O1s peak with the PFDT treatment (e) F 1s peak with and without PFDT treatment (f) wide scan of film with the without PFDT treatment.

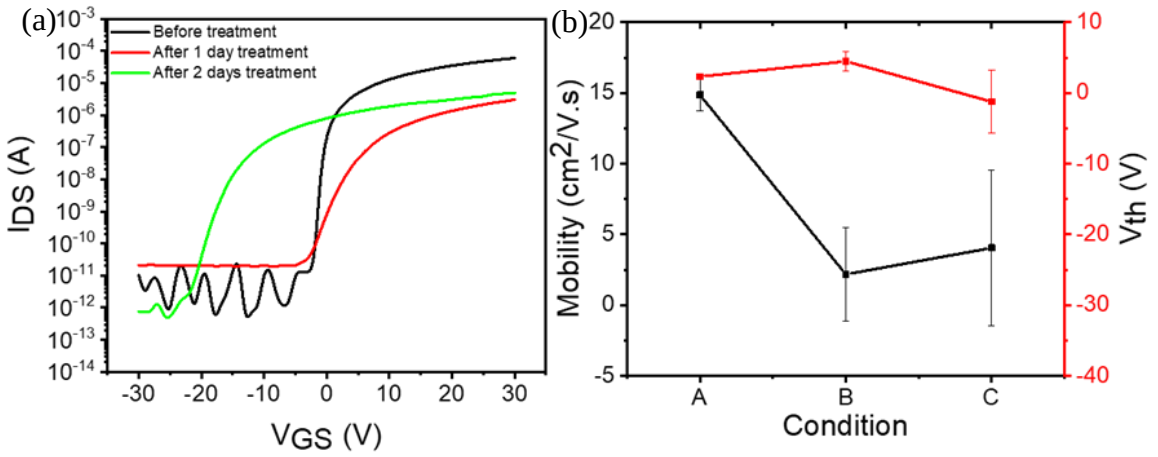

Figure 5-12: (a) Transfer characteristics before and after PFDT treatment: A is before treatment; B is one day of treatment C is two days of treatment (b) mobility and threshold voltage before and after treatment. W=1000 μm, L=250 μm V_{DS}=1V.

Figure 5-12a depicts the transfer characteristics of IWO TFT in DDT treatment. The devices were measured after one day of dipping in PFDT and two days of dipping in PFDT solution. The shift in the transfer characteristics is apparent. The mobility and threshold voltage variations are shown in **Figure 5-12**b. It was expected that the threshold voltage would shift to positive, and mobility will decrease due to the presence of electronegative fluorine atoms. However, for the sample after two days of treatment, the V_{th} shifts negative, implying that the previous shift is negated if the sample is kept in the PFDT solution for a long time. This might be due to hydroxyl ions passing through pinholes present in PFDT film, increasing the charge carriers in the film. The deteriorating effects of water are discussed in the literature review section. However, it is successfully demonstrated that the attributes of TFT can effectively be modulated by self-assembled monolayer dipoles of fluorinated - Thiol.

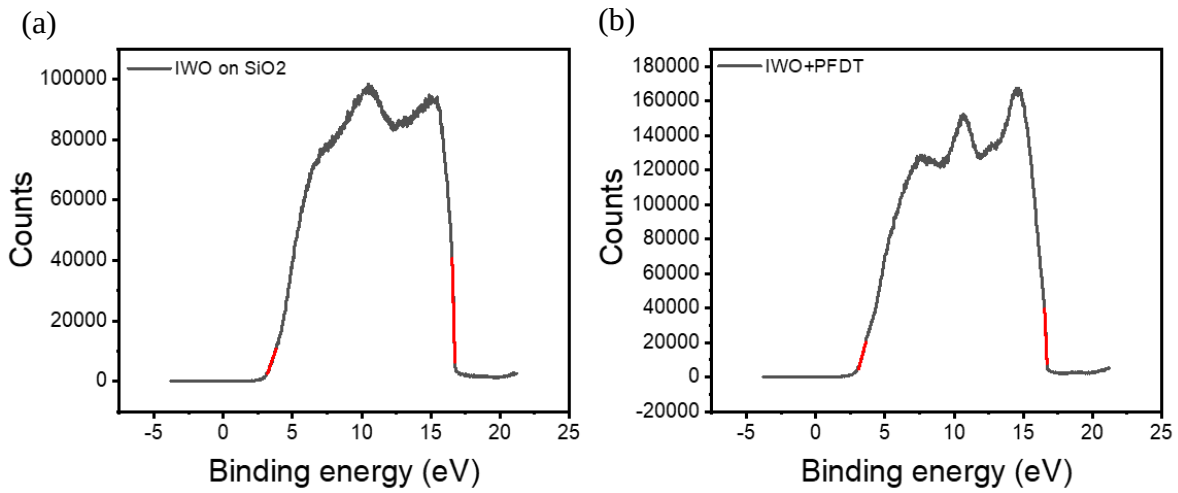

Figure 5-13: UPS of IWO film (a)before and (b) after PFDT treatment.

To further confirm that the modification indeed changes the electronic properties of the semiconductor, a UPS was performed. **Figure 5-13** compares UPS data for pristine, and PFDT coated IWO film. From this figure, it is possible to calculate the shift in work function and ionization potential of IWO. The energy of He(I) used for measurement is 21.2 eV. The HOMO energy level of IWO shifted from 2.8 eV to 2.94 eV; The secondary electron cut off energy shifted from 16.6 eV to 16.76 eV. The work function and ionization potential (VBM) was changed from 4.61 to 4.44 eV and 7.40 to 7.38 eV, respectively, after PFDT treatment. **Table 5-3** summarizes the changes after the PFDT treatment and compares it with DDT.

Table 5-3: Work function and ionization potential derived from UPS.

Surface	**Energy of He**	**E_{homo}**	**E_{seco} (Secondary electron cut off energy)**	**Work function**	**Ionization potential**
	B (eV)	C (eV)	D (eV)	B-D (eV)	B-D+C (eV)
IWO	21.2	2.8	16. 6	4.61	7.4
PFDT	21.2	2.94	16.76	4.44	7.38
DDT	21.2	2.88	17.10	4.1	6.98

5.2.4 Surface modification based on polymers containing aliphatic amine groups

Until now, Silane-based and thiol-based molecules were used for making the SAM layers to modify the surface. With the results, it can be concluded that silane-based APTES treatment resulted in better, more stable, and consistent results. However, it was suspected that the amine group from unreacted ligands might be a factor contributing to the increased carrier concentration of the semiconducting oxide. Therefore, to crosscheck the hypothesis, neutral polymers comprising aliphatic amine groups were chosen. The polymers PEI and PEIE were chosen for this experiment (chemical structure in **Figure 5-14**). Deposition of these polymer was done by spin coating PEIE directly (4000 rpm for 1 min) or PEI solution (0.4 wt% 2methoxy ethanol 4000 rpm for 1 min, 100 ºC for 10 min). Both the polymers were heated in a vacuum furnace for 3 hr at 80 ºC to get rid of the water content present prior to use. XPS was done to crosscheck the formation of the film.

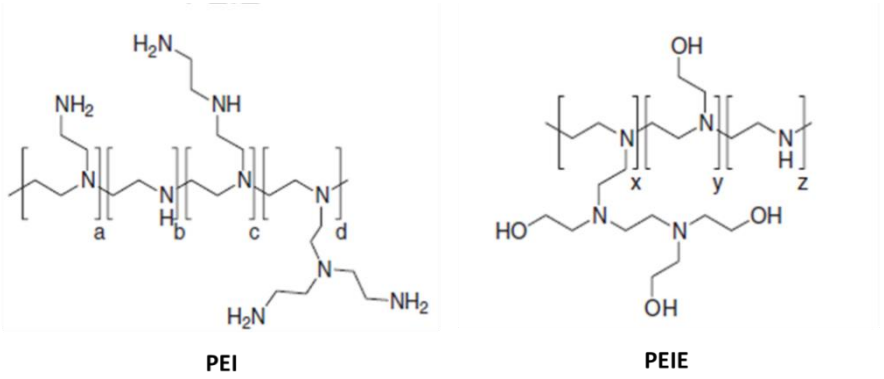

Figure 5-14: Chemical structure of PEI and PEIE.

Figure 5-15 depicts the comparison of XPS of the surface before and after spin coating PEI and PEIE on IWO surface. **Figure 5-15** a and b demonstrate the N1s peak of the surface with the without PEI and PEIE coating, respectively. The absence of nitrogen peak can be noted on bare IWO. The 398.6 eV peak belongs to N-H bond, and it is evident that the percentage area under the peak for PEIE (21.14%) is less than that of PEI (35.35%) as PEI have more N-H bonds compared to its ethylated counterpart. Whereas, the other peak of energy near 399 eV belongs to the N-C bond. Consequently, the PEI (64.65%) will have comparatively less percentage area than that of PEIE (78.86%) with less concentration on N-C bonds.

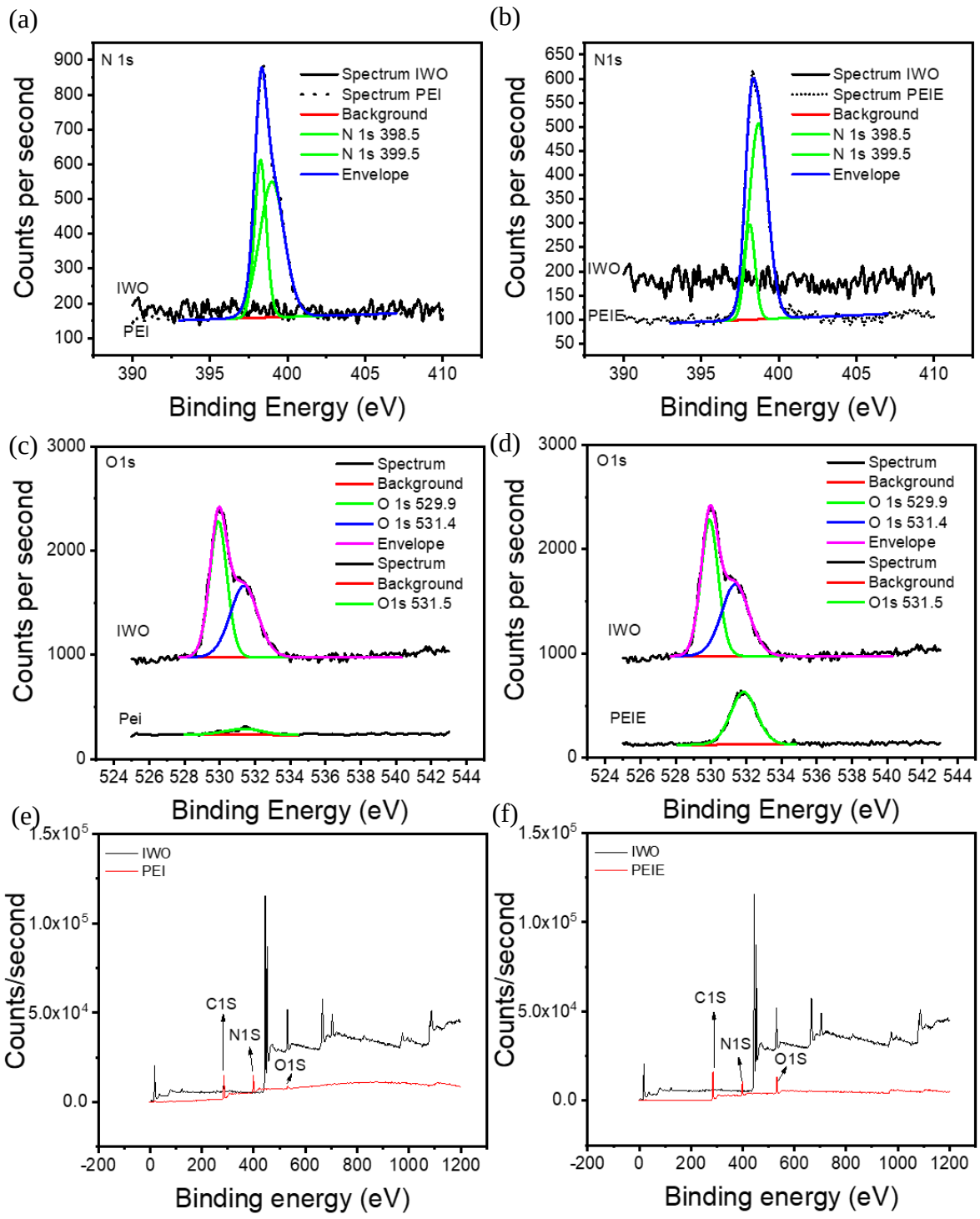

Figure 5-15: (a) N1s peak for IWO before and after PEI coating (b) N1s peak for IWO before and after PEIE coating (c) O1s peak for IWO before and after PEI coating (d) O1s peak for IWO before and after PEIE coating (e) wide scan of film with the without PEI treatment. (f) wide scan of film with the without PEIE treatment.

Figure 5-15 c and d demonstrate that the oxygen peak from M-O-M bond from IWO is entirely subsidized and is replaced by -OH bond peak of 531.85 eV. Being ethylated compound, the PEIE is expected to have more of -OH bonds compared to PEI. The same is observed in **Figure 5-15** c (PEI) and d (PEIE). **Figure 5-15** (e) and (f) clearly shows the presence of C 1s with N1s peak resulting from alkyl groups and amine group respectively whereas untreated samples do not show any presence of such compound. **Figure 5-15** (e) and (f) are wide scans of film coated with PEI and PEIE; Both the films give very sharp peaks for carbon (C 1s), Nitrogen (N 1s) and Oxygen (O 1s) and suppressed the indium and other peaks from semiconductor film.

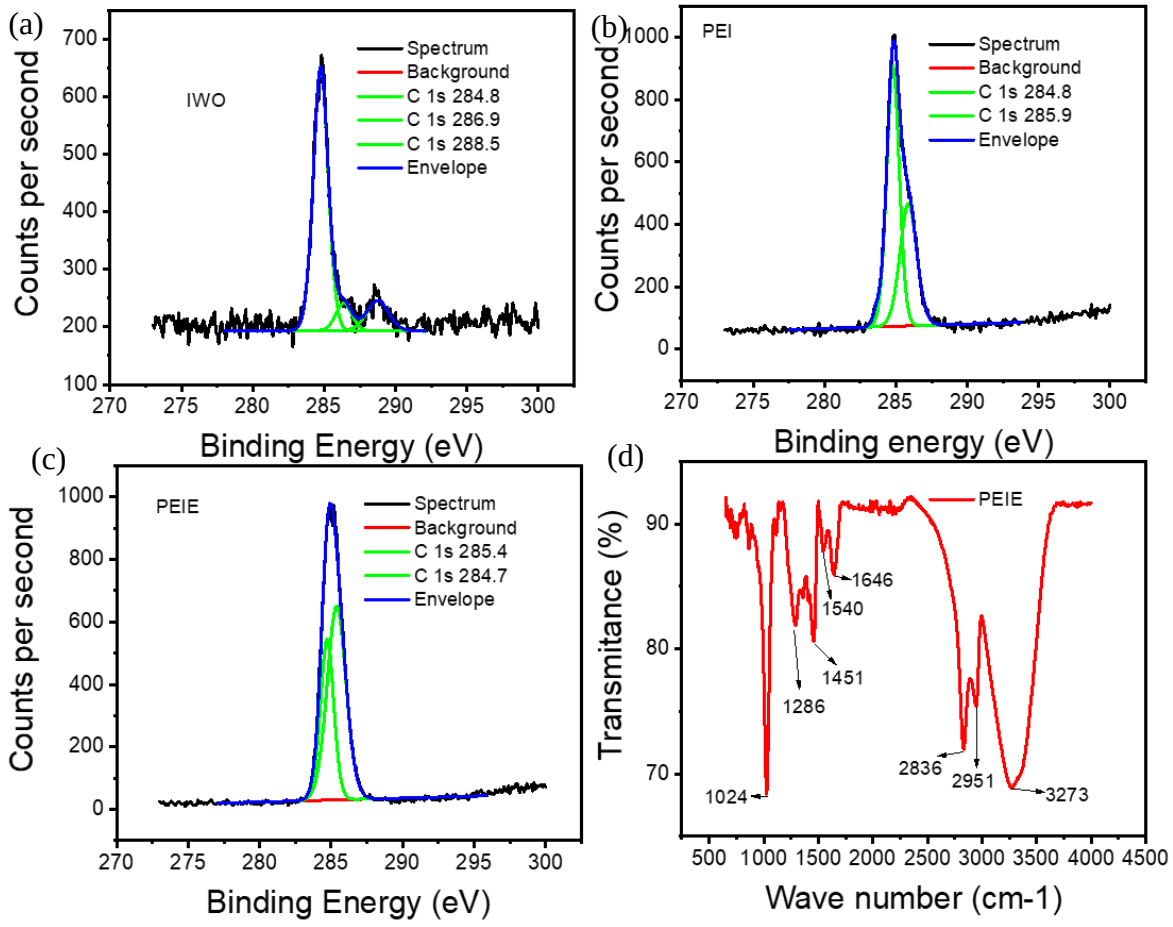

Figure 5-16: (a) C1s peak for IWO (b) C1s peak after PEI coating (c) C1s peak after PEIE coating (d) FTIR spectra of PEIE.

Figure 5-16a gives Carbon (C1s) peak for IWOis deconvoluted as follows. The first peak at 284.75eV confirms the presence of C-C bond the next peak at 286.37eV confirms C-O-C bond and at last 288.74eV confirms O-C=O bond present in hydrocarbon. Whereas C1s

peak in **Figure 5-16** b and c is of PEI, and PEIE coated samples, respectively. Apart from the first peak of 284.7 eV corresponding to C-C bond from the alkyl groups, the second peak belongs to C-N peak. Moreover, the increment in this second peak for PEIE again is due to ethylation. Hence, to crosscheck the proper ethylation of PEIE, an FTIR was performed on the IWO film coated with PEIE (**Figure 5-16** d). The observed peaks in FTIR are composed in **Table 5-4** with the group of the bond they belong to and compound class the specific wavenumber is represented.[34] From **Table 5-4**, the types of bond represented are for alkyl chain, nitro compound, amine group, alkane group, and -OH bond from alcohol. These all bonds are present in PEIE, confirming the ethylation of PEI in PEIE.

Table 5-4: IR Spectrum Table and corresponding peaks observed in FTIR of PEIE.

Sr. No.	Observed (cm^{-1})	Absorption (cm^{-1})	Appearance	Group	Compound Class
1	1024	1124-1087	strong	C-O stretching	secondary alcohol
2	1286	1342-1266	strong	C-N stretching	aromatic amine
		1310-1250	strong	C-O stretching	aromatic ester
		1275-1200	strong	C-O stretching	alkyl aryl ether
3	1451	1450	medium	C-H bending	alkane
4	1540	1550-1500	strong	N-O stretching	nitro compound
5	2836	3000-2840	medium	C-H stretching	alkane
6	2951	3000-2800	strong, broad	N-H stretching	amine salt
		3000-2840	medium	C-H stretching	alkane
		3200-2700	weak, broad	O-H stretching	alcohol
7	3273	3550-3200	strong, broad	O-H stretching	alcohol

Figure 5-17 a, c depicts the transfer characteristics of IWO TFT after PEI and PEIE coating, respectively. The devices were measured immediately after PEI and PEIE coating. The shift in the transfer characteristics is apparent. The mobility and threshold voltage variation is shown in **Figure 5-17** b, d. A negative shift was expected due to amine group present in the polymer. It can be seen that the change in threshold in PEI is more pronounced; this is because the PEI has more free amine groups compared to its ethylated counterpart PEIE.

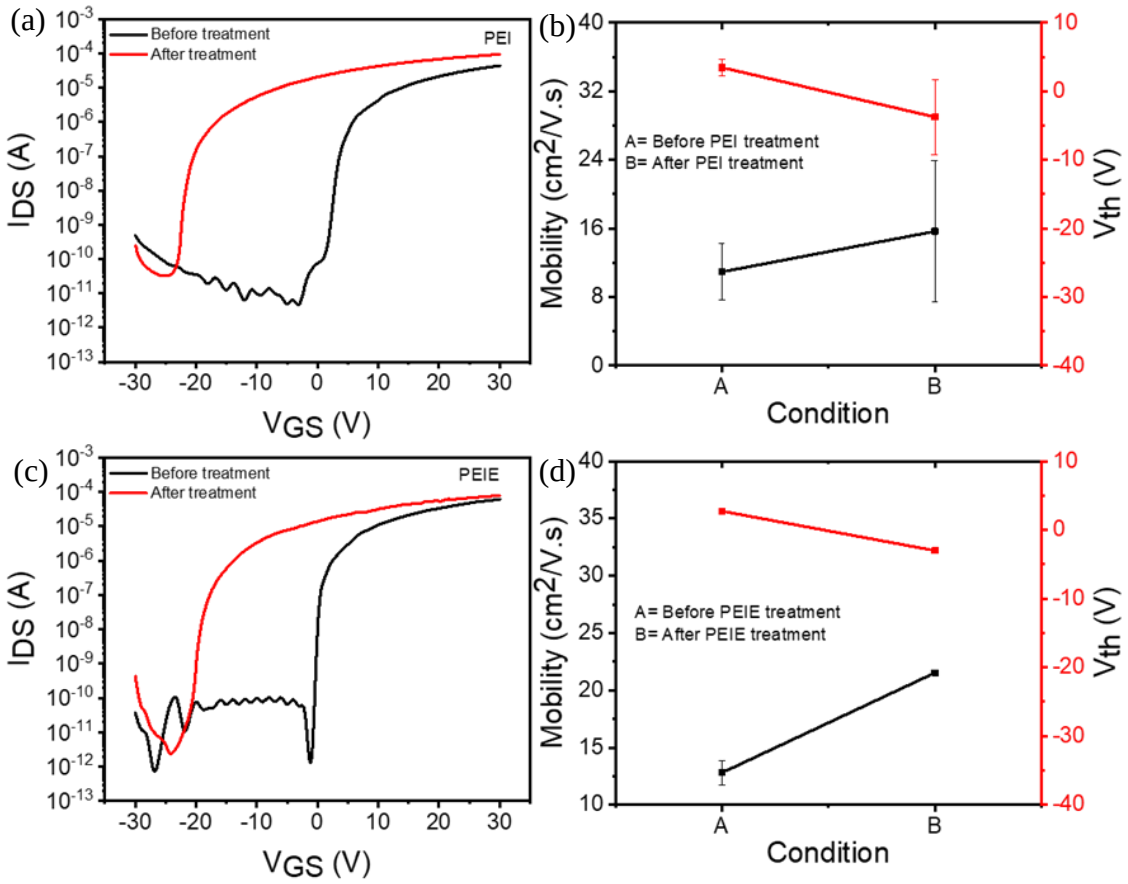

Figure 5-17: (a) and (c) transfer characteristics before and after PEI treatment and PEIE treatment, respectively. A is before treatment; B is after PEI treatment, (b, d) Mobility and threshold voltage before and after coating. W=1000 µm, L=250 µm V_{DS}=1V.

To further confirm that the modification indeed changes the electrical properties of the semiconductor, a UPS was performed. **Figure 5-18** is UPS data for PEI and PEIE coated IWO film. From this figure, it is possible to calculate the shift in work function and ionization potential of IWO. The energy of He(I) used for measurement is 21.2 eV. The HOMO energy level of IWO shifted from 2.8 eV to 2.84 eV for PEI and 2.56 for PEIE; The secondary electron cut off energy shifted from 16.6 eV to 17.59 eV for PEI and 17.44 for PEIE. The work function was modified from 4.61 to 3.61 eV for PEI, and 3.76 for PEIE and ionization potential (VBM) changed from 7.40 to 6.45 for PEI, and 6.32 eV for PEIE coated IWO film. **Table 5-5** summarizes the changes after the treatment.

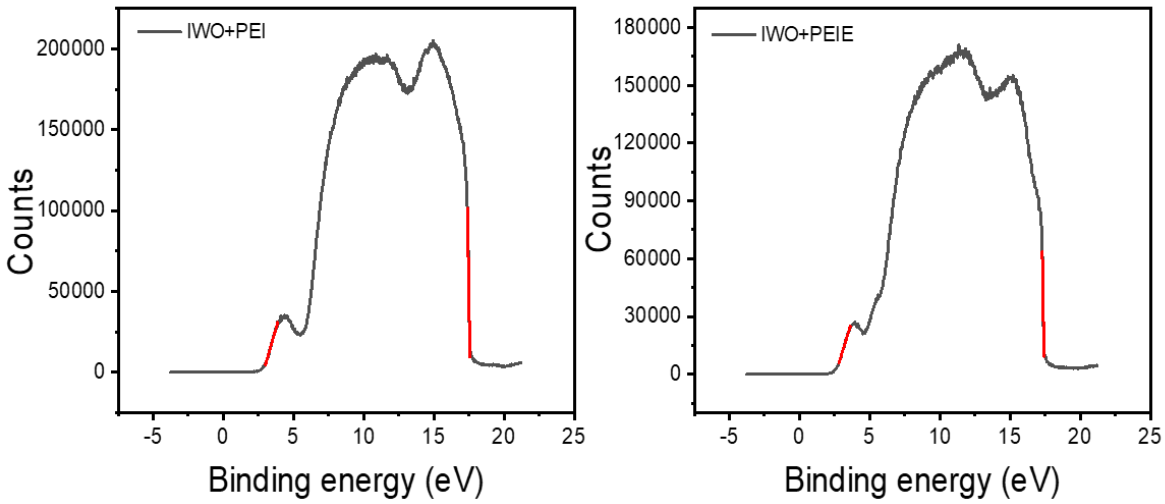

Figure 5-18: UPS of IWO samples with PEI and PEIE coating.

Table 5-5: Work function and ionization potential derived from UPS

Surface	Energy of He	E_{homo}	E_{seco} (Secondary electron cut off energy)	Work function	Ionization potential
	B (eV)	C (eV)	D (eV)	B-D (eV)	B-D+C (eV)
IWO	21.2	2.8	16. 6	4.61	7.4
PEI	21.2	2.84	17.59	3.61	6.45
PEIE	21.2	2.56	17.44	3.76	6.32

In conclusion, it is successfully demonstrated that the TFT attributes can be efficiently modulated by the surface doping technique utilizing neutral polymers containing aliphatic amine groups, where the presence of amine groups plays a vital role in shifting the work function of oxide semiconductors by around 1eV.

Thus far in this chapter, modulation of the charge carrier caused by surface dipole formation and molecular surface doping of inorganic oxide semiconductor using organic molecules to modulate the TFT features have been discussed. Recently one report showed the n-type doping of SnO_2 by a simple, air-robust, and cost-effective triphenylphosphine oxide molecule used as an electron transport layer for solar cell.[5] The effect of TPPO molecular doping on IWO oxide TFT was investigated and can be seen in appendix information (XPS- **Figure A-5**, TFT parameters- **Figure A-6**, UPS- **Figure A-7**). TPPO molecule did not show desirable effects the possibly due to the fact that complete film formation of these molecules did not occur as proven by XPS results.

5.2.5 Summary and Conclusion

In conclusion, a novel dipole induced charge carrier modulation technique to modulate TFT parameters was demonstrated. It was implemented through various surface treatments which alter the electronic characteristics of the TFT oxide semiconductor channel. Various types of surface treatments such as Silanes in the form of APTES, Thiols in the form of DDT and PFDT, charge-neutral polymers containing aliphatic amine groups PEI, PEIE and dopant molecules such as TPPO (n-type doping) were covered. Various parameters calculated for these surface-treated IWO samples are scripted in **Table 5-6**.

Table 5-6: Summary of various device parameters and physical properties

Surface	E_{homo}	E_{seco}	W.F.	I.P	μ_{lin}, (V_{th}) Before	μ_{lin}, (V_{th}) After
	eV	eV	eV	eV	$cm^2/V.s$, (V)	$cm^2/V.s$, (V)
APTS	3.42	17.27	3.94	7.36	11.21, (2.96)	32.54, (-0.46)
DDT	2.88	17.1	4.1	6.98	7.24, (5.33)	6.14, (1.09)
PFDT	2.94	16.76	4.44	7.38	14.86, (2.33)	2.16, (4.49)
PEI	2.84	17.59	3.61	6.45	10.94, (4.9)	15.66, (-3.76)
PEIE	2.56	17.44	3.76	6.32	12.80, (2.74)	21.53, (-3.02)

Figure 5-19 shows the postulated energy level alignment of the pristine IWO surface versus the SAM treated IWO surface. Pristine IWO's work function (WF-1) should reduce after treating with APTES / DDT(WF-2) leading in enhanced carrier concentration and left shift of threshold voltage owing to the proximity of the negative end of the dipole. The observed rise in mobility and left threshold shift can be ascribed to passivation of shallow trap states. On the other hand, the work function (WF-3) should increase with PFDT treatment, resulting in decreased carrier concentration and right-shift of the threshold voltage due to proximity of the positive end of the dipole. The use of fluorinated chemical such as PFDT (one-day treatment) also has shown potential for modulating the threshold voltage in a positive direction.

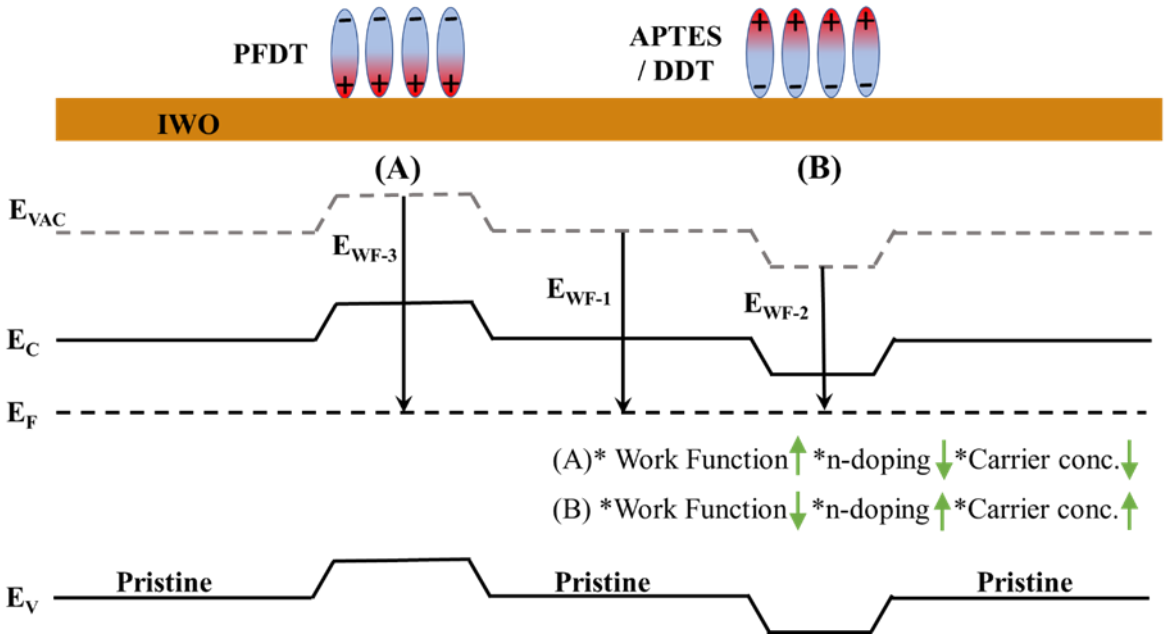

Figure 5-19: Energy Band diagram for pristine IWO and surface treated IWO. E_F= Fermi level, E_{VAC}= vacuum level, E_C= conduction band, E_V= valance band of the semiconductor. E_{WF1}= Work function of the pristine surface, E_{WF2}= Work function of APTES, DDT treated the surface, E_{WF3}= Work function of PFDT treated surface.

It is also evident that the strong electron-donating characteristics of the amine group in PEI, and PEIE significantly enhances the mobility and results in V_{th} modification in the negative direction. For APTES, the same group is accountable for positive NH_3^+ end, making a strong dipole that also helps to modify the V_{th}. Such SAM dipoles are therefore helpful for regulating the carrier concentration and threshold voltage; for example dipoles with the negative end near the IWO surface can be used for negatively shifting the V_{th} and increasing carrier concentration, whereas dipole with the positive end near the IWO surface can be used for positively shifting V_{th} and reducing the carrier concentration. The electron-donating capability of the surface dopant group (in case of PEI, PEIE) such as amine group and the excess charge carriers created due to SAM dipoles may enable the filling of the shallow electron traps of semiconductor, hence improving the mobility. **Figure 5-20** consolidates the variation achieved through the various surface coating. It can be seen from the figures that the amine-containing films, i.e., APTES, PEI, and PEIE, had the maximum amount of change in the work function followed by the DDT and TPPO. The film treated with PFDT had a higher work function than other surface treatments because positive end

of the dipole faces the surface. This is because of the presence of very high electron affinity fluorine atoms which make the other end of the dipole more negative. However, the measured work function of the two days PFDT treated IWO showed a lower value than pristine IWO. The presence of water in the ethanol is suspected to be the culprit. Its effect is evident in the TFT characteristics as well.

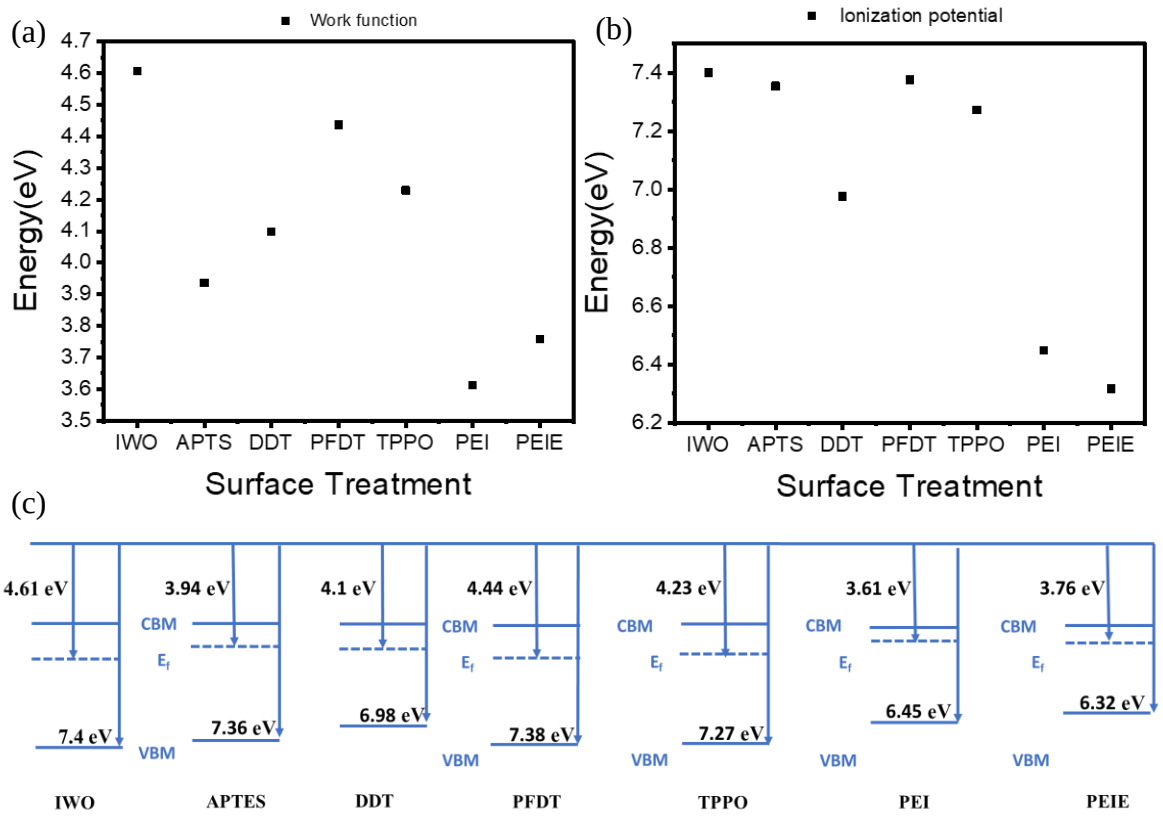

Figure 5-20: (a) Workfunction change for IWO with various surface modification, (b) ionization potential change for IWO with various surface modifications, (c) band diagram displaying valance band minimum and Fermi level energy.

With this, it can be concluded that the performance of TFT can be selectively manipulated via surface treatments. The method of drop on demand can be used to selectively apply these surface doping molecules on individual TFT to facilitate the selective modification of semiconductor parameters. Eventually, this modification would help to achieve the next generation of flexible devices applications which demand low processing temperature and higher control over conductance of channel.

5.3 Wet chemical oxidation as a route for controlled passivation of oxygen vacancies

The IWO film used for this section was prepared, as explained in the experimental section. The treatment with H_2O_2 was done by dipping the TFT substrate in 30% H_2O_2 for various durations.

5.3.1 Characterization of H_2O_2 treated samples

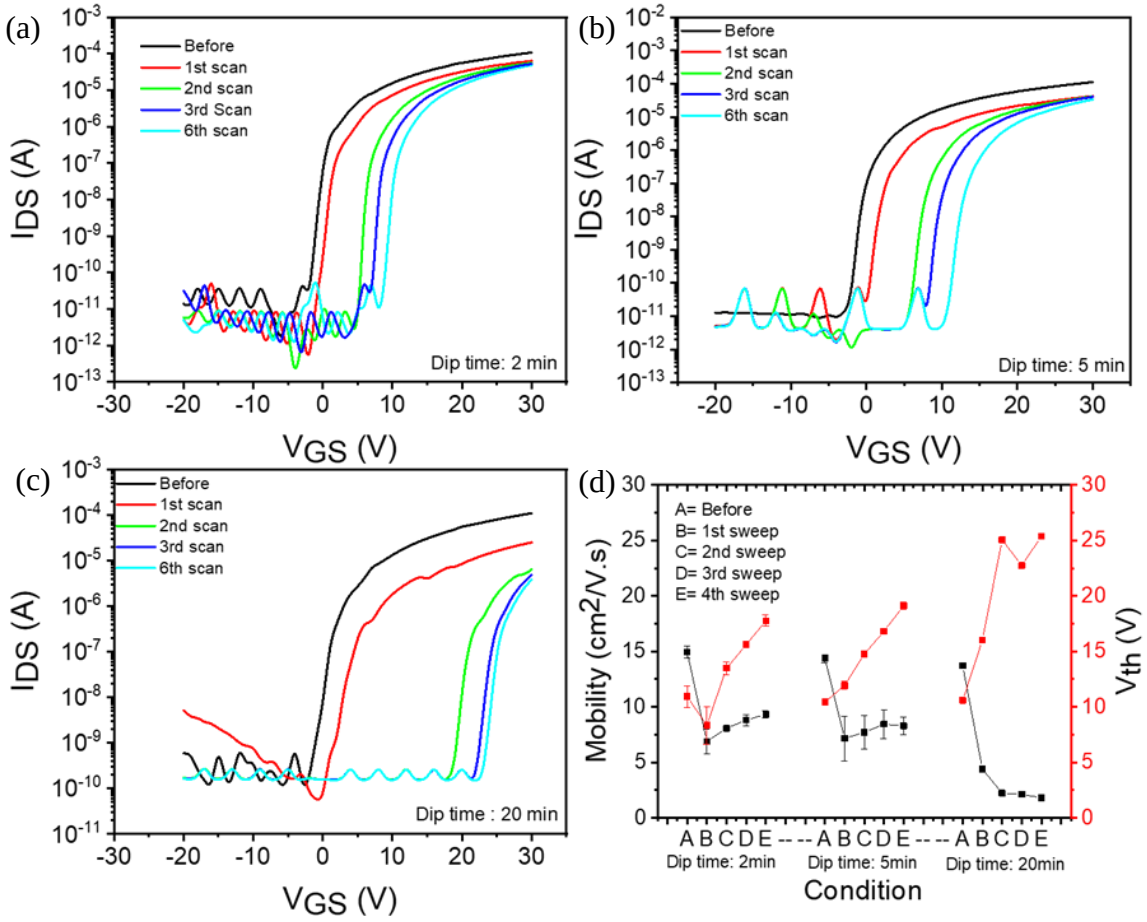

Figure 5-21: The instability for a few scans after the H_2O_2 treatment. (a) after 2 min of treatment (b) after 5 min of treatment (c) after 20 min of treatment (d) variation in parameters with consecutive sweep scans. W=1000 µm, L=250 µm V_{DS}=1V.

Figure 5-21 displays the variation of attributes of already annealed TFT with dipping time

in 30% H_2O_2. The changes in the threshold voltage and mobility are summarized in **Figure 5-21**(d). As the dip time increases, the threshold voltage shifts to more positive values. It can also be noted that with every sweep, the threshold shifts further. This shift relatively remains constant after the 6^{th} sweep. The reasons for this instability of the device will be discussed later in the section. Next, the XPS spectrum of various oxygen vacancies modulation techniques was compared.

Figure 5-22 demonstrates the XPS spectra of O 1s oxygen-peak for films as-deposited, H_2O_2 treated for 20 min after deposition, 200 ºC annealed, and H_2O_2 treated for 20 min after 200 ºC heat treatment. The as O 1s peaks are deconvoluted among three peaks named as M-O-M peak (around 529.8 eV), oxygen vacancies peak (531.4) and adsorbed species peak (533 eV). As expected, the oxygen vacancies peak (47.51%) for as-deposited sample was highest with M-O-M peak (50.91%) being lowest compared to other processes, whereas for the area percentage for oxygen vacancies of was decreased from only H_2O_2 treated (47.06%), 200 ºC (43.47%) annealed and H_2O_2 treated sample after 200 ºC annealing (38.9%). Consequently, the M-O-M peaks were increased from only H_2O_2 treated (52.71%), to 200 ºC (55.36%) annealed and H_2O_2 treated sample after 200 ºC annealing (60.58%).

This decrease in oxygen vacancies confirms the oxygen vacancies modulation through wet chemical oxidation of amorphous oxide using H_2O_2. It was also noted from **Figure 5-23**a that the plot of percentage area of adsorbed species containing OH ion peak in O 1s peak decreases for both the H_2O_2 treatment. This decrease in adsorbed oxygen deconvoluted peak suggests that H_2O_2 processing also helps to get rid of adsorbed contaminations. The phenomena can also be seen in XPS results of some other reports as well. [22], [35]

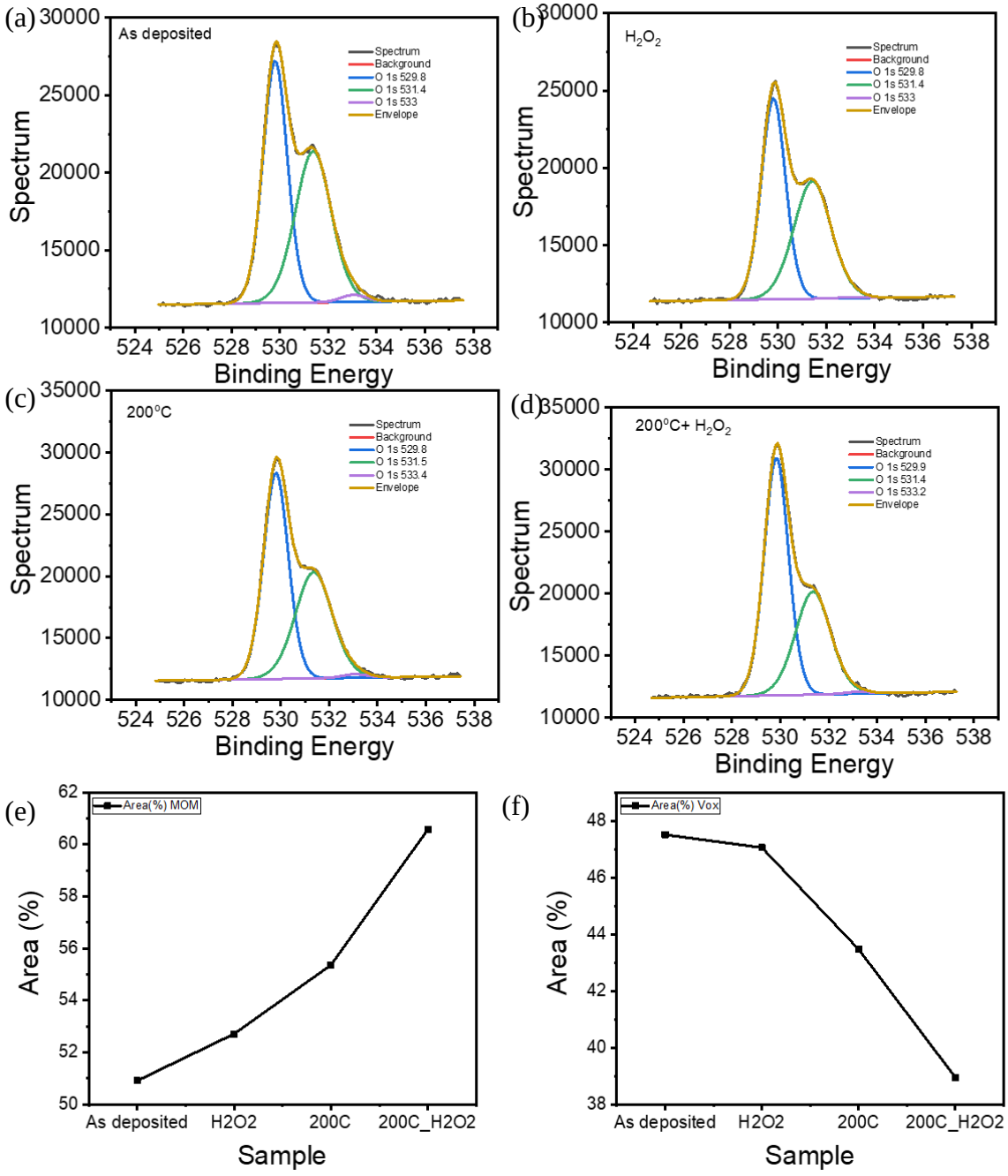

Figure 5-22: XPS O1s spectrum of treated samples and area of MOM peak, oxygen vacancies peak, and adsorbed OH group. (a) the o1s peak of the as-deposited sample (b) O1s peak of 20 min H_2O_2 treated sample (c) O1s peak of 200 ºC annealed sample (d) O1s peak of 20 min H_2O_2 treated sample after 200 ºC annealing. (e) the plot of percentage area of M-O-M peak in the O 1s peak concerning treatment type (f) plot of percentage area of oxygen vacancies peak in the O 1s peak concerning treatment type.

To reconfirm that the change in oxygen vacancies is affecting the TFT characteristics, UPS was performed on the films to detect modulation of work function due to the change of oxygen defects. **Figure 5-23** b displays the UPS of films processed in different ways. The work function and ionization potential were calculated from UPS spectra, detailed process of work functions calculations is given in the experimental section. The UPS results do not show the expected correlation with the amount of oxidation. As seen in **Figure 5-23** c, d there is an increase in work function and ionization potential from as-deposited to 200 ºC to H_2O_2 treatment after 200 ºC annealing except for the film with only H_2O_2 treatment without any annealing. The sample with H_2O_2 treatment alone has a higher work function than both as-deposited and 200 ºC annealed sample, which suggests that the Fermi level is lower than the 200 ºC sample. This should not be possible as the electric and XPS characterizations show that the sample of 200 ºC is more oxidized than only H_2O_2 treated sample. The answer to this anomaly lies in the limitation of the UPS measurement technique. The UPS technique is very surface sensitive. That means that any change at the surface will affect the readings form UPS. Moreover, when the samples were treated with H_2O_2, the reaction mainly occurs at the oxide surface, making the sample more oxidized at the surface compared to bulk. Such surface oxidation has been previously reported. [21], [36] This is another reason why the surface treatment experiments using H_2O_2 did not work with high k dielectrics such as with alumina. With high k dielectric, the channel forms further near the semiconductor-dielectric interface, which is away from the H_2O_2 exposed surface of the semiconductor. This surface oxidation also explains the UPS anomaly of higher work function for H_2O_2 treated sample compared to 200 ºC annealed sample. This also explains the instability of the device in the first few sweeps (as observed in **Figure 5-21**). The stability of the device while measuring the transfer characteristic is not excellent. The positive shift observed might be due to the filling of the metal cation traps created due to over-oxidation at the surface. These trap states occur due to the absence of metal cation in the M-O bond. This deficiency primarily occurs in the presence ofan excessive number of oxygen atoms. These defects are also called anti-site/ interstitial oxygen defects. [24] These deep trap states can easily accept and trap the electrons. These electrons require higher energy to activate during the next voltage sweep. After consecutive sweeps when these traps are filled the TFT transfer characteristics become stable. This also explains the

higher ionization potential of the film treated with only H_2O_2.

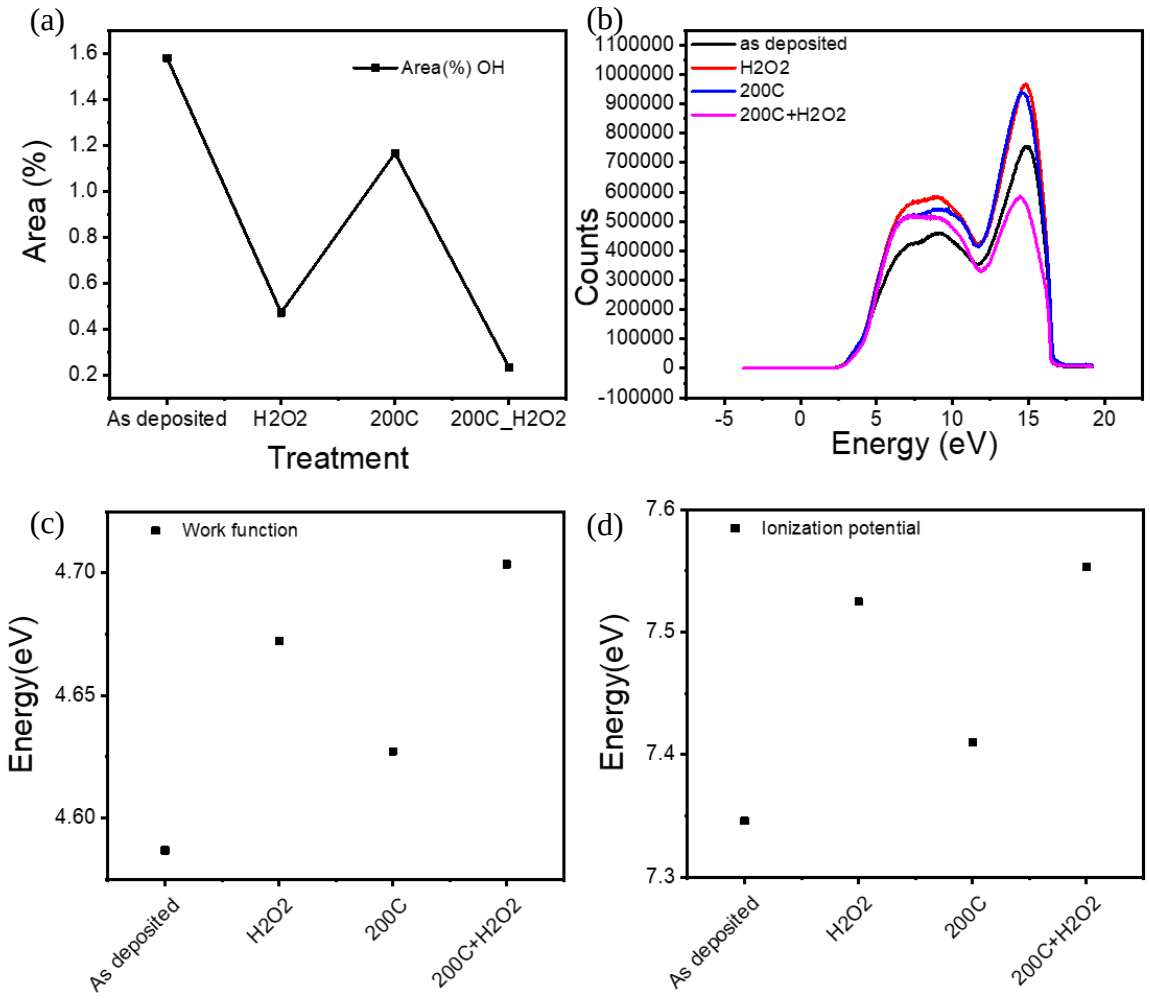

Figure 5-23: (a) Plot of percentage area of deconvoluted peak related to adsorbed oxygen associated with OH^- ion peak with respect to treatment type. (b) UPS spectra for different types of treatments. (c) work function changes with respect to types of treatments (d) ionization potential with respect to types of treatments.

The bandgap is needed to get the energy band diagram. **Figure 5-24**(a), displays the Optical absorption spectroscopy needed to calculate the optical bandgap of material the film used for this measurement was 100 nm thick as the 7 nm thick film was not providing consistent results. **Figure 5-24** b suggest that as the oxygen vacancies in the film decrease the bandgap also increases. The effect of anion defects might not be prominent in this measurement because of the higher thickness. This result is acceptable because majority defect

contribution must be from the 100 nm thick film which would have shadowed the effect from comparatively small numbers of anion defects.

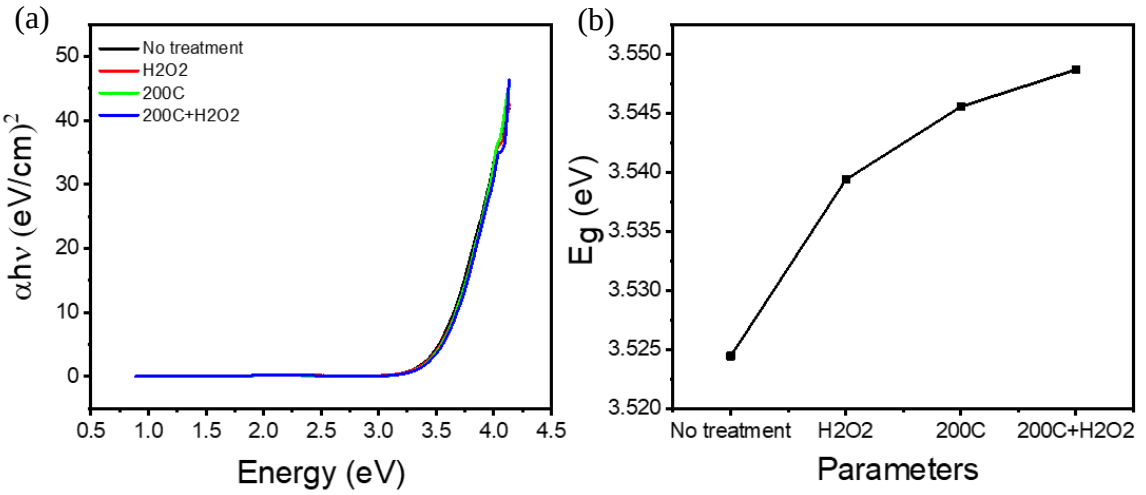

Figure 5-24: (a) Optical absorption spectroscopy using UV -VIS spectroscopy (b) bandgap for various treatments.

Table 5-7: Summarizes energy levels for various treatments

Parameter (unit)	**Bandgap(BG)** (eV)	**E_{homo}** (eV)	**E_{seco}** (eV)	**Fermi level (E_F)** (eV)	**VBM (E_V)** (eV)
Method (Instrument used)	**Optical absorption spectroscopy (UV VIS)**	**(UPS)**	**(UPS)**	**Work function (UPS)**	**Ionization potential (UPS)**
No treatment	3.52	2.72	16.61	4.59	7.35
H_2O_2	3.54	2.85	16.53	4.67	7.53
200 ºC	3.55	2.82	16.57	4.63	7.41
200 ºC+H_2O_2	3.56	2.89	16.51	4.69	7.58

Table 5-7 summarizes energy levels. HOMO energy level is obtained from UPS, Fermi level /work function, and ionization potential. Moreover, with the Optical absorption spectroscopy, the optical band gap was acquired. The corresponding band diagram is drawn in **Figure 5-25**. The changes in the Fermi level/ work function are visible from the diagram. The decrease in shallow trap density owing to decreasing oxygen vacancies can be seen from no treatment (leftmost) to 200 ºC + H_2O_2 treatment (rightmost).

Moreover, the deep traps away from CBM after the surface treatment with H_2O_2 can be shown to resemble the cationic traps present due to over-oxidation of the film surface. In shallow donor, states are metastable and can readily donate an electron to the conduction band. Initial sweeps at lower voltages will fill the deep states, and consequent sweep will require higher voltages to push electrons from these traps to the conduction band. These deep trap states are responsible for lower conductance of the film as the oxygen vacancies responsible for shallow states are minimum at this stage (for a sample of process 200 $^oC+H_2O_2$).

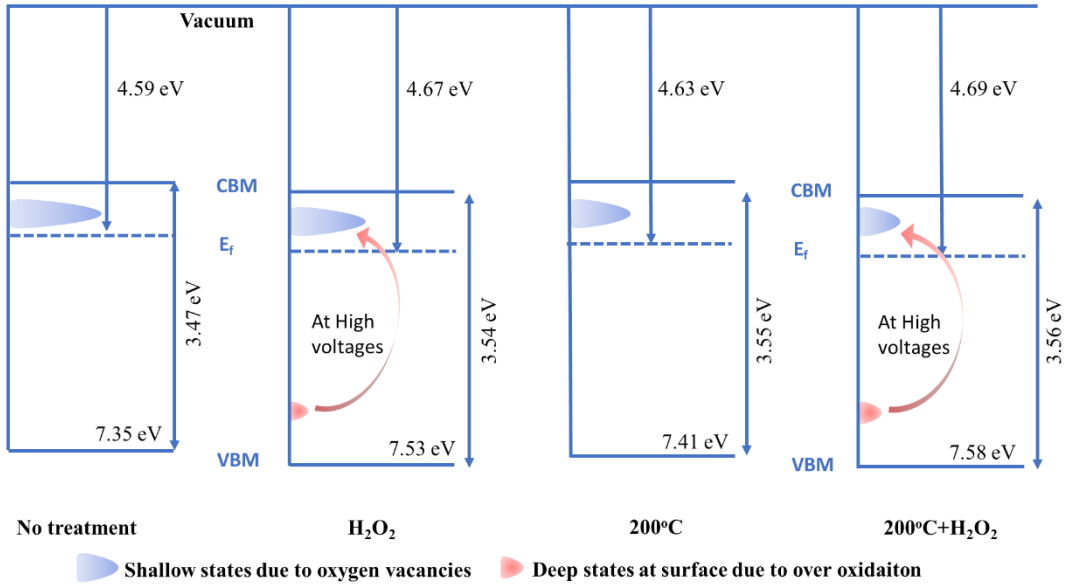

Figure 5-25: Derived band diagram from table 5-7 and explanations for the device instability.

The Mott Schottky measurement derived from CV measurement performed on the semiconductor film by electrochemical impedance spectroscopy (**Figure 5-26**) to measure charge carrier concentration. The slope obtained through measurement is used for calculating the charge carrier density. Moreover, x-intercept was used to obtain flat band potential. **Table 5-8** gives the details of these values.

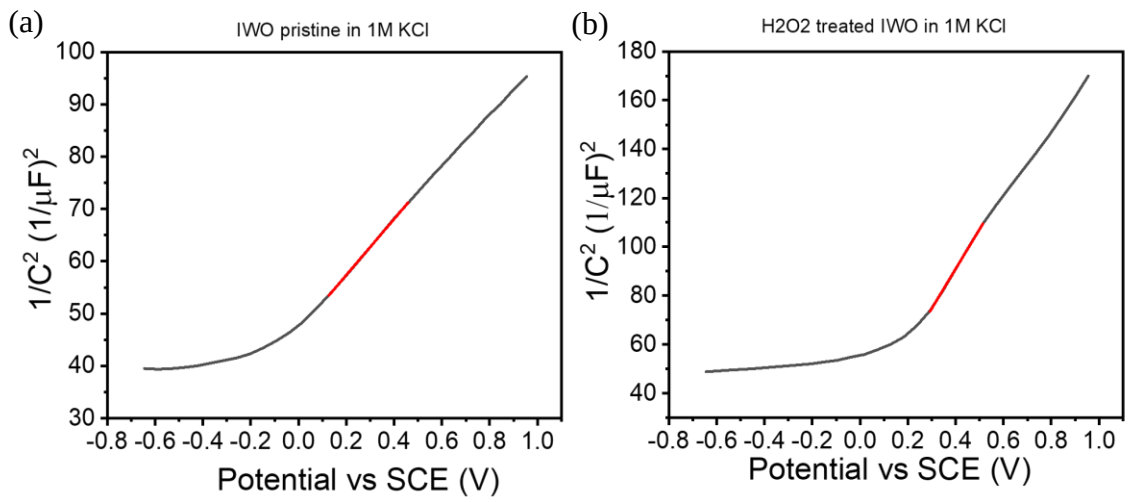

Figure 5-26: Mott Schottky measurement obtained through cyclic voltammetry measurement. (a) IWO pristine sample. (b) H_2O_2 treated IWO film.

Table 5-8: Values derived from Mott Schottky measurement

	Slope	N_D	X-intercept	V_{FB}
IWO pristine in 1M KCl	5.35E+13	2.283 e24	-0.87	-0.9
H_2O_2 treated IWO in 1M KCl	1.62E+14	7.539 e23	-0.16	-0.19

It is evident from **Table 5-8** that the charge carrier density decreases with H_2O_2 treatment. Which strengthens the fact that the oxygen vacancies are passivated, decreasing the number

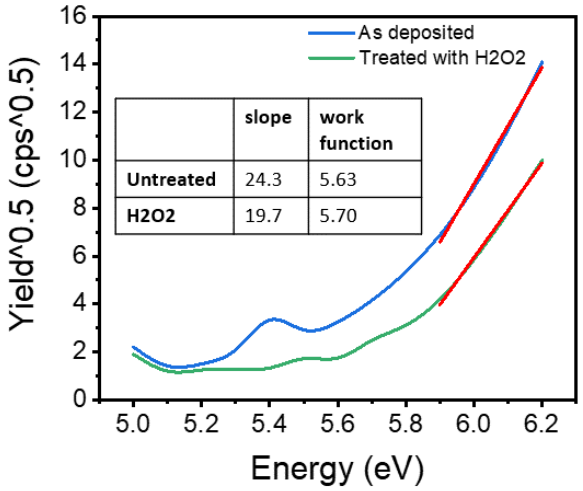

Figure 5-27: PESA measurement to measure work function.

In order to check the work function, PESA was used (**Figure 5-27**). The inset of the figure shows the calculated work function. Due to air-based measurements, the work function

seems very different from the UPS. However, it can be noted that the difference between the work function obtained from PESA (0.07 eV) and UPS (0.08 eV) is similar.

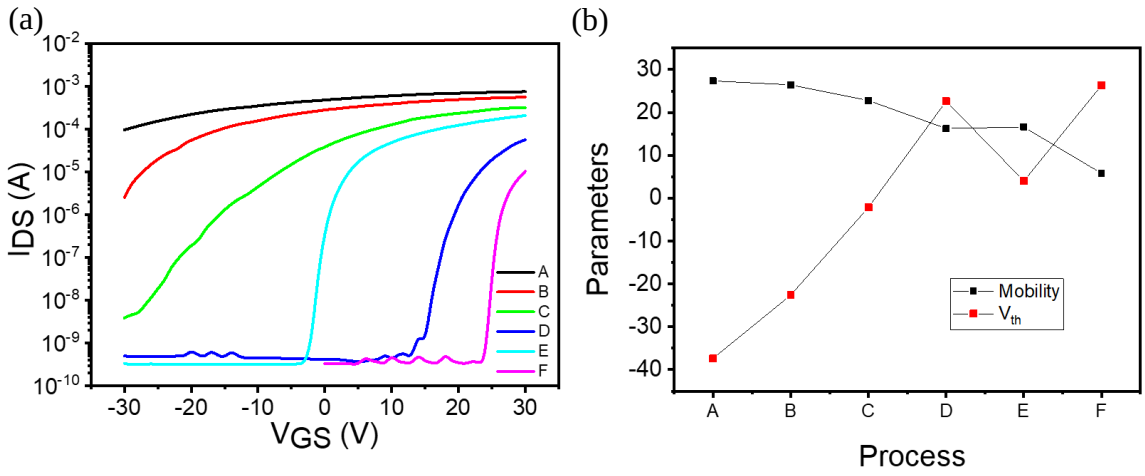

Figure 5-28: (a) Depletion to enhancement mode oxidation of thin-film transistor with W/L=1000/300 using H_2O_2, V_{DS}=1V. (b) variation in mobility and threshold voltage with the oxidation time. Where, A is sample before treatment, B is sample after 15 min in H_2O_2, C is sample after 45 min in H_2O_2, D is sample after 105 min in H_2O_2, E is sample annealed after 105 min in H_2O_2, F is sample after 20 min in H_2O_2 after annealing.

Based on the possibility of oxidation of film achievable through the Hydrogen peroxide assisted wet chemical treatment, the trial for shifting the threshold voltage using only hydrogen peroxide for replacing thermal annealing step was studied. **Figure 5-28** shows the controlled athermal passivation of oxygen vacancies in oxide semiconductor based thin film transistor using hydrogen peroxide assisted wet chemical treatment as a route. To show that the effect is universal and can be used on several different materials, experiments with oxidation using H_2O_2 on solution-processed samples made of IZO were performed details in Appendix (**Figure A-8**). The results showed similar conclusive results on these solution-processed TFTs as well.

5.3.2 Summary and Conclusion

Study of the effect of passivation of oxygen vacancies using hydrogen peroxide on TFT was performed to achieve athermal passivation of oxygen vacancies. It will pave the way for the replacement of the high-temperature annealing process with simple H_2O_2 oxidation

to control the very high conductance in thin-film transistors and enable the change from depletion-mode operation to low voltage enhancement mode operation. Precise control of conductance value can be useful in applications such as neuromorphic electronics and synaptic devices. From UPS, it was also noted that H_2O_2 could be responsible for the over-oxidation of the surface. This property can be used to achieve environmental stability. The decreased -OH peak from O1s spectra belonging to adsorbed species after H_2O_2 treatment also suggests the cleaned surface of the oxide. This cleaning can be useful for unique applications such as photocatalysis where the surface needs to be contaminant free.

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Chapter 6 *

Electric Field-Driven Athermal Activation of Amorphous Metal Oxide Semiconductors

One of the primary factors affecting the behavior and performance of TFT is the number of oxygen vacancies present in the channel material. Typically, for sputtered metal oxide thin films, the quantity of oxygen vacancies is controlled by the oxygen partial pressure during deposition and by the post-annealing process. Here, a novel field-driven athermal activation of AMOS channels via electrolyte gating was demonstrated. The high electrostatic field provided by the ionic liquid gating facilitates reversible migration of the charged oxygen species. These stoichiometric transformations are characterized through XPS and detailed electrical parameter analysis. The chapter gives critical insights on different parameters affecting oxygen vacancies generation. In addition, the chapter also covers various applications including active programming of operating mode of TFT, and neuromorphic transistors, facilitated by the field-induced activation.

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* This chapter is published substantially as as Kulkarni Mohit Rameshchandra, et al. “Field-Driven Athermal Activation of Amorphous Metal Oxide Semiconductors for Flexible Programmable Logic Circuits and Neuromorphic Electronics”, Small (2019). [1]

6.1 Introduction

As discussed in literature review with a highly hybridized conduction band minima (CBM) insensitive to local structural randomness, amorphous semiconducting oxides of post-transition metals [indium (In), gallium (Ga), tin (Sn), and zinc (Zn)] are superior alternatives to a-Si:H, poly-Si and organic semiconductors for applications that demand high-mobility, transparency, flexibility, and large-area uniformity.[2], [3] However, the high-temperature deposition and post-annealing processes required for high-mobility activation in these oxide semiconductors impede its realization on thermally-fragile flexible substrates, entailing significant research efforts in this direction.[4] Ideally, an athermal treatment optimized to modify the local electronic structure of AMOS to generate sufficient carriers for charge transport would ensure high-mobility devices at room temperature, overcoming conventional high-temperature processing challenges.

The use of electric field effect for modulation of semiconductor has attracted tremendous interest, since the demonstrations of the insulator to superconductor phase transition with high charge carrier densities of the order of 10^{14} cm^{-2}, [5]–[7]. The extremely high electric field required is obtained through a capacitively coupled gate bias of an electrical double layer (EDL) transistor, which uses an electrolyte as the gate dielectric [6], [8], [9]. Use of electrolytes such as ionic liquids [10], [11] and polymer containing supporting salts[12], [13] have been reported. The electrolyte generates an EDL in the order of angstroms to 1 nm at the IL/solid interface, generating an extremely high electric field of ~ 50 MV/mm[14] . These large electrostatic fields have been shown to be capable of moving ions in/out of solid films, eg.VO_2, $SrTiO_3$ [5], [6]. Electric field-driven creation and manipulation of oxygen vacancies are well studied in deciding the switching characteristics in memristive devices. [9], [15], [16].

Inspired from these previous advances and recent reports on electric field-induced TFT modulation [9][17], a novel field-driven electrolyte/ionic liquid gating approach to athermally modulate the local electronic structure of AMOS, favorably tuning the oxygen-stoichiometry at room temperature was adopted. The electrolyte acts as a permeable

membrane for oxygen extraction/intercalation from/into the semiconducting channel, modulating the available carriers for charge transport on-demand, thereby activating oxygen-compensated thin films at room temperature. Optimized biasing conditions (a function of the bias amplitude, duration, initial carrier concentration, and measurement ambient) enable fabrication of high-mobility (> 100 cm^2/V s) sputtered indium tungsten oxide (IWO)thin-film transistors (TFTs) on flexible polyimide substrates, mitigating high-temperature post-annealing processes.[1] Detailed electrical and spectroscopic characterizations provide novel insights into the mechanism of field-driven migration of oxygen vacancies, comprehensively establishing this technique as a promising alternative to conventional high-temperature processing. On-demand programming of operation modes (enhancement and depletion) is also demonstrated without any additional fabrication steps, facilitating the facile realization of logic circuits and neuromorphic transistors.

6.2 Study of field-induced oxygen vacancies variation

6.2.1 Manipulation of oxygen vacancies

The IL field-induced activation process was characterized on IWO TFTs deposited on Si-SiO_2 substrates (TFT fabrication process is described in the experimental section) **Figure 6-1** a illustrates the basic structure of the device fabricated for the study of oxygen vacancy manipulation. An ionic liquid with similar cation and anion size, EMIM TFSI (1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide) and SiO_2 serving as the top and bottom gate dielectrics respectively, were used in this process. The biasing field-application terminal was served by the top gate, while the bottom gate probed the electronic structure of the semiconducting channel, as detailed in further sections. As explained in previous chapters, IWO was used as the semiconducting layer since the W dopant in an edge-sharing polyhedral structure enhances the stability of high mobility In_2O_3 matrix[18]. Physical characterizations of films used for this chapter are displayed in appendix-Information (**Figure A-9**). **Figure 6-1** b-e depicts the transfer and output characteristics of the devices in both the top and bottom-gated configurations. The mobility was calculated

to be around 8 $cm^2\ V^{-1}\ s^{-1}$ for the electronic bottom-gated mode, and 51 $cm^2\ V^{-1}\ s^{-1}$ for the ionic top-gated mode.

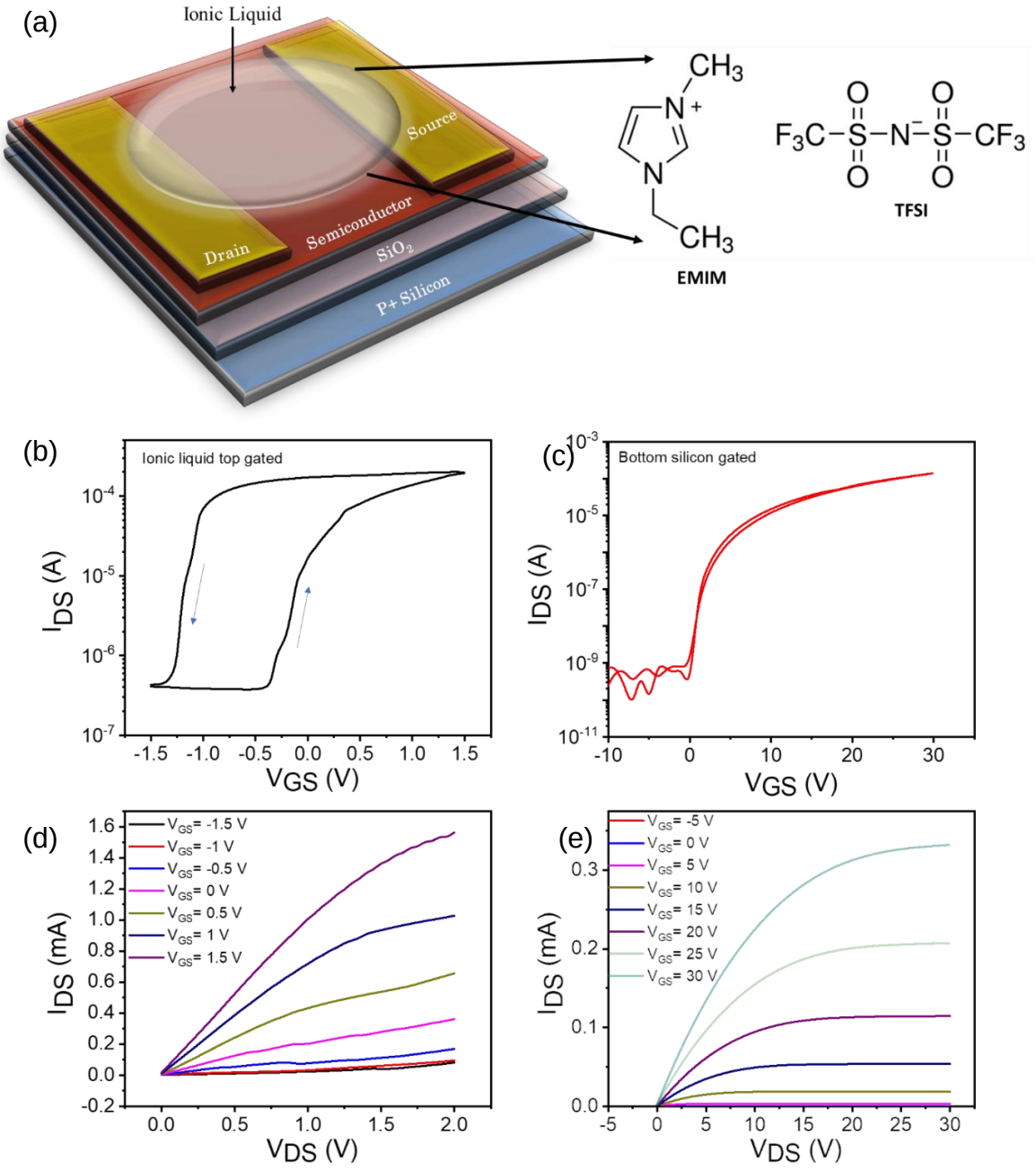

Figure 6-1: (a) Shows the double-gated FET configuration with EMIM TFSI (1-Ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide) and SiO_2 serving as the top and bottom gate dielectrics, respectively. (b-e) depicts the transfer and output characteristics of devices in the top (b, d) (V_{DS} of 0.3V) and bottom-gated configurations (c, e) (V_{DS} of 5V), respectively. W=1000 μm, L=150 μm. [1] Reproduced with permission from ACS Publications.

For mobility calculations, a measured specific capacitance value of 2.83 × 10^{-8} F/ cm^2 at 10 kHz and 1.99x10^{-6} F/ cm^2 at 20 Hz were selected for SiO_2 and EMIM TFSI (**Figure 6-2** a) respectively. The large EDL capacitance resulted in efficient carrier accumulation within the small electrochemical window of the ion liquid, resulting in an ultralow-voltage and power operation. Devices in the electronic back-gated mode clearly depicted a negligible clockwise hysteresis, while the ionic top-gated mode exhibited a larger anticlockwise hysteresis window of 1 V. In the ionic top-gated mode, the anticlockwise hysteresis was attributed to migration-relaxation kinetics of mobile ions in the dielectric. [19] Forward scan resulted in the migration of cations towards the ionic liquid-semiconductor interface, accumulating electrons in the IWO layer to form a conductive channel. This resulted in lower voltage requirements for the subsequent channel formation in the reverse scan, accounting for the anticlockwise hysteresis. To systematically examine field-driven vacancy creation, the devices were initially biased in the ionic top-gated configuration with the bottom-gate floated. In order to simplify the analysis, only the forward sweeps of the transfer characteristics were taken into consideration.

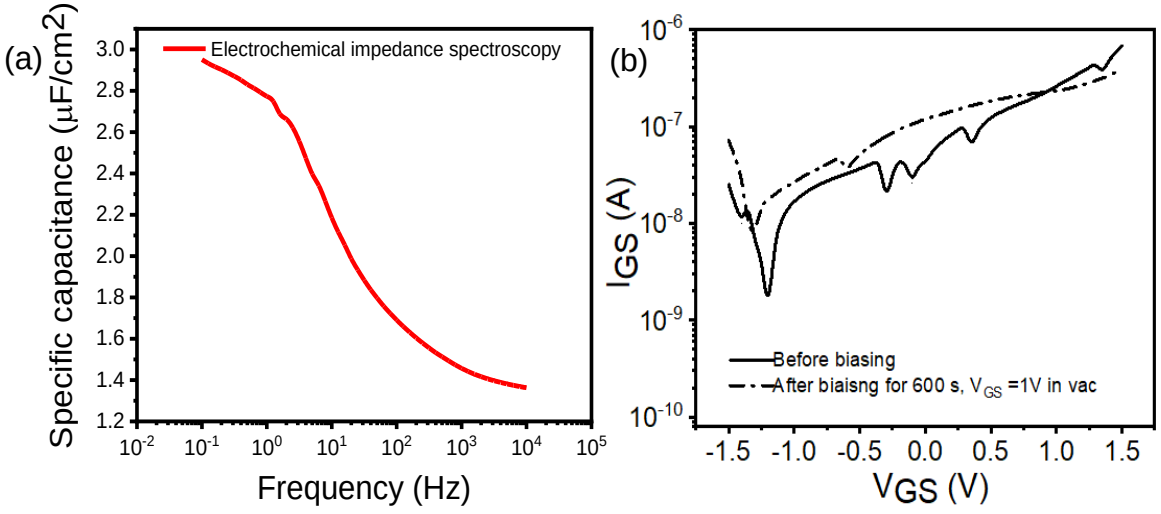

Figure 6-2: (a) The capacitance of the ionic liquid EMIM TFSI measured via impedance spectroscopy. The capacitance value of 1.99x10^{-6} F/cm^2 at 20 Hz was utilized in agreement with the literature[20] (b) the gate leakage currents for ionic liquid gate dielectric. [1] Reproduced with permission from ACS Publications.

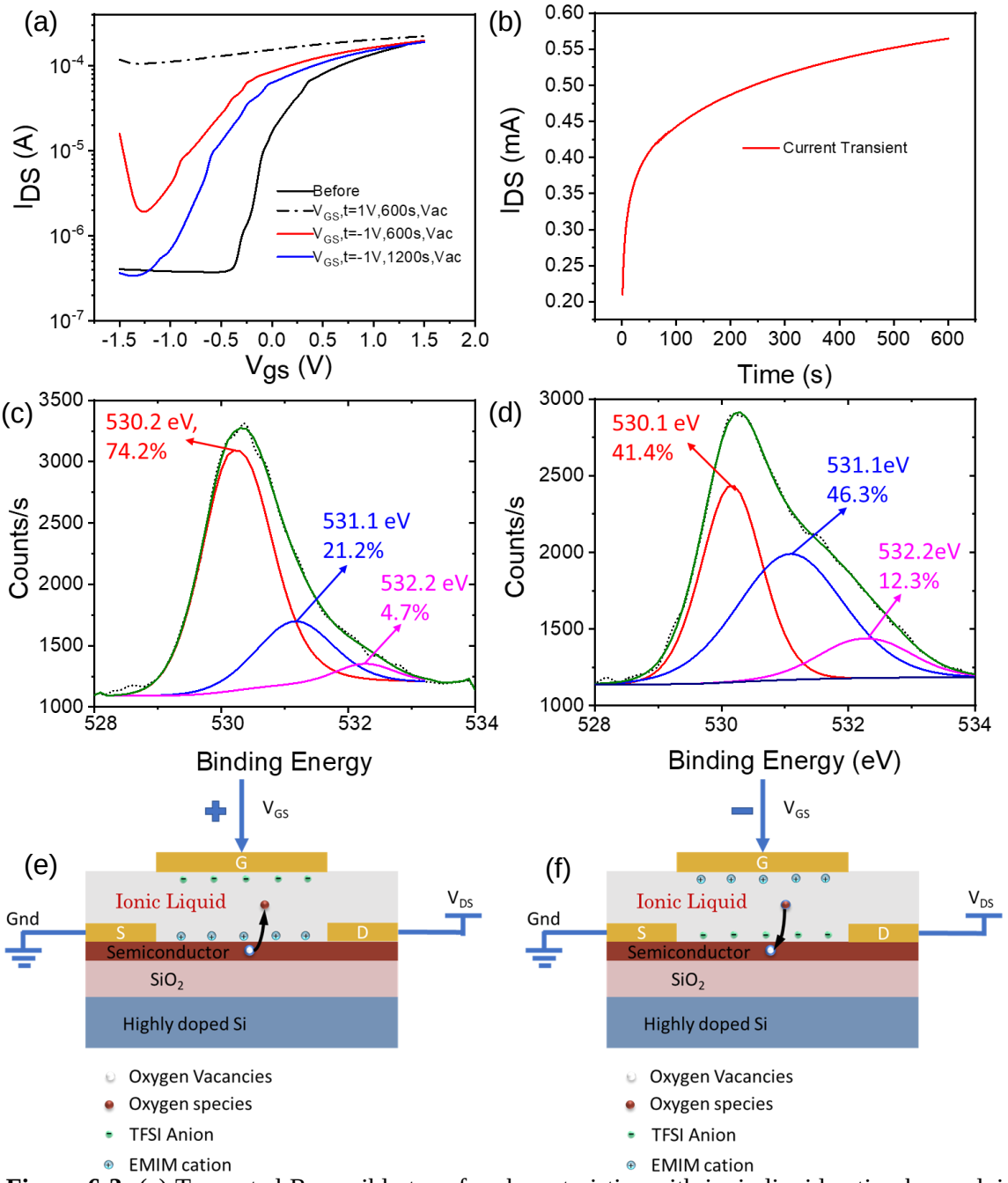

Figure 6-3: (a) Top-gated Reversible transfer characteristics with ionic liquid gating by applying positive and negative voltage. The solid black line indicates original device characteristics; dotted black line indicates after biasing of 1V for 600sec in a vacuum, the blue and red line represents after 600 s biasing and 1200 s biasing respectively on the same device, W=1000 μm, L=150 μm. (b) current transient for 600s of gate biasing voltage of 1 V and drain voltage of 0.3V (c) XPS of untreated sample (d)XPS after ionic liquid treatment (e) mechanism explaining creation of oxygen vacancy with application of positive gate voltage (f) mechanism for dissociation of oxygen vacancy with application of negative gate voltage. [1] Reproduced with permission from ACS Publications.

As can be observed from **Figure 6-3**a, the application of a positive bias of 1V for 600s (corresponding biasing current shown in **Figure 6-3**b), leads to an improvement in the ON-state current and a negative V_{th} shift, which indicates an increase in charge carriers which can in turn be linked to a rise in the number of oxygen vacancies. A reversal of the above-mentioned effect is expected with the application of a negative bias of the same amplitude and duration. However, from **Figure 6-3**a, it can be seen that although there is a reduction in the on-current and a shift in V_{th}, the threshold voltage does not return to its original value on the application of –1V bias for 600s. An additional negative bias of the 1200s results in more substantial V_{th} shift. However, a further increase in the duration of the negative bias does not result in a recognizable improvement in the threshold voltage. The mechanism of oxygen vacancy modulation was further investigated in order to understand the reason for these anomalies in the V_{th} shifts. It is biasing with higher fields, or longer durations resulted in a further programmed shift of V_{th}, $I_{on,}$ and I_{off}, confirming this observation.

Upon bias application, the biasing drain current transient (**Figure 6-3**b) first increased rapidly followed by gradual saturation, indicating the presence of two possible processes underplay. Under a bias of +1 V, the I_{ds} increased from 0.21 mA to 0.35 mA in 18 seconds, followed by a gradual saturation to 0.565 mA for bias durations greater than 600 seconds. It was suspected, first one process to be desorption of the surface oxygen species, which is a fairly facile process, thus requiring a relatively shorter duration of positive bias to achieve the desired level of carrier concentration. However, for longer durations, interior oxygen and deep oxygen vacancy variations are mainly involved, which are difficult to extract, resulting in a reduced rate of increase of current, contributing to the second process. In order to get more direct evidence of the underlying mechanism, XPS measurements were performed and analyzed for the metal-oxygen bonding (**Figure 6-3** c,d). Since the conduction pathways in these oxides are predominantly dictated by vacant spatially dispersed ns orbitals, the O1s peak was analyzed to estimate the modulation of oxygen vacancies. The O1s peak was deconvoluted to three individual peaks located around 530.1, 531.1, and 532.2 eV.[21] The peak at the lowest binding energy (~ 530.1 eV) was assigned to the oxygen atoms in the fully oxidized indium environment (lattice oxygen; M−O−M). The mid-peak at ~ 531.1 eV was assigned to oxygen ions in the oxygen-deficient region

(indicative of oxygen vacancy concentration). And the peak at high binding energy (~ 532.2 eV) was assigned to the presence of loosely bound oxygens (adsorbed oxygen) associated with the presence of hydroxyl groups on the surface.[22] The percentage area of M-O-M peak, oxygen vacancy peak, and adsorbed oxygen peak was changed from 74.2% to 41.4%, from 21.2% to 46.3%. from 4.7% to 12.3% respectively. XPS analyses revealed an increase in the concentration of oxygen vacancies for thin films that were biased at +1 V for 1200 s, authenticating the current transient measurements and hypothesis of oxygen vacancies modulation using the high electric field present due to EDL at the interface of the ionic liquid and channel. Films biased at lower dosages (1 V, 15 s) did not show any difference in the M-O bonding in the XPS analyses. Hence, the initial rapid increase in the current transients was attributed to the passivation of defects/trap centers like surface-adsorbed moisture/oxygen at the electrolyte-semiconductor interface, which may not alter the carrier concentration of the semiconducting channel permanently.

The electrical properties of amorphous oxide semiconductors, such as its transport properties, hinges on its electronic state, which in turn depends on its oxygen stoichiometry. Hence a variation in the oxygen concentration in the film will affect the electrical properties of an oxide semiconductor. When the positive bias is applied to the ionic liquid gate, the high electric field generated by the EDL, causes the negatively charged oxygen species (O_2^-, O^-) to move into and get dissolved in the ionic liquid, creating more oxygen vacancies in a thin film. The resultant increase in charge carriers is manifested as a negative V_{th} shift and an increase of the on-state current. **Figure 6-3** (e, f) illustrates the proposed mechanism of oxygen vacancies creation and dissociation with an applied gate voltage. The negatively charged oxygen species can be extracted from the channel layer into the ionic liquid using a positive IL gate bias, and with a negative IL gate bias, the process can be reversed.

Back-gated FET measurements were conducted subsequent to the IL field-induced activation process. All traces of the ionic liquid were washed away prior to these measurements to prevent further oxygen-getting reactions for a fair analysis. **Figure 6-4** depicts the back-gate FET characteristics of devices, post-application of the electric field. The unchanged back-gated transfer characteristics for IL field voltages of 1 V and duration 15 seconds supported the proposed hypothesis of surface defect passivation during the initial stages. However, prolonged (800 s blue curve in **Figure 6-4**) electric fields resulted in a shift of electrical parameters (V_{th}, I_{on}) for even the back-gated channels with an enhancement in mobility from 8 cm^2/Vs to 14.49 cm^2/Vs, re-validating the saturation in current transient measurements, and increased oxygen vacancy generation as reflected by the XPS measurements.

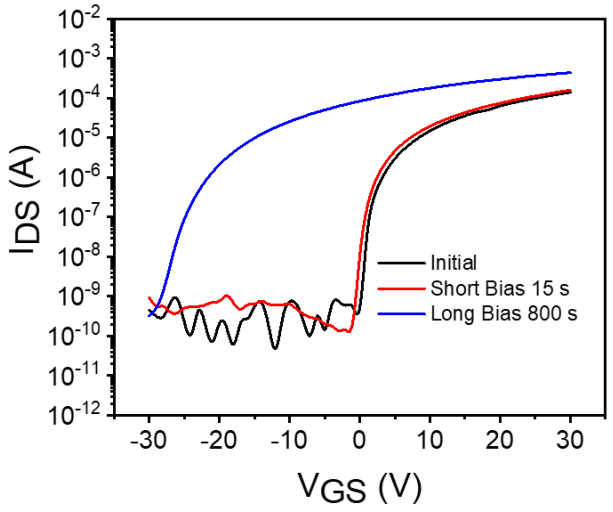

Figure 6-4: The back-gated FET characteristics of devices, post application of the bias voltage of 1 V, for 15 seconds (Short bias) and 800 seconds (long bias). W=1000 μm, L=150 μm. [1] Reproduced with permission from ACS Publications.

6.2.2 Effect of environment on biasing

Considering the oxygen vacancies modulation effect, a film with relatively higher oxygen concentration to modulate should show a more pronounced change in the maximum output current. Of the TFTs fabricated with different oxygen partial pressures (1sccm, 2sccm, 3sccm), the maximum relative improvement in on-state current was obtained with a 3sccm

oxygen partial pressure. **Figure 6-5**(a) demonstrates the normalized drain current variation, before and after biasing for 600 sec with respect to oxygen partial pressure at the time of IWO deposition. Hence 3sccm partial pressure was used for the IWO film formation for all further studies.

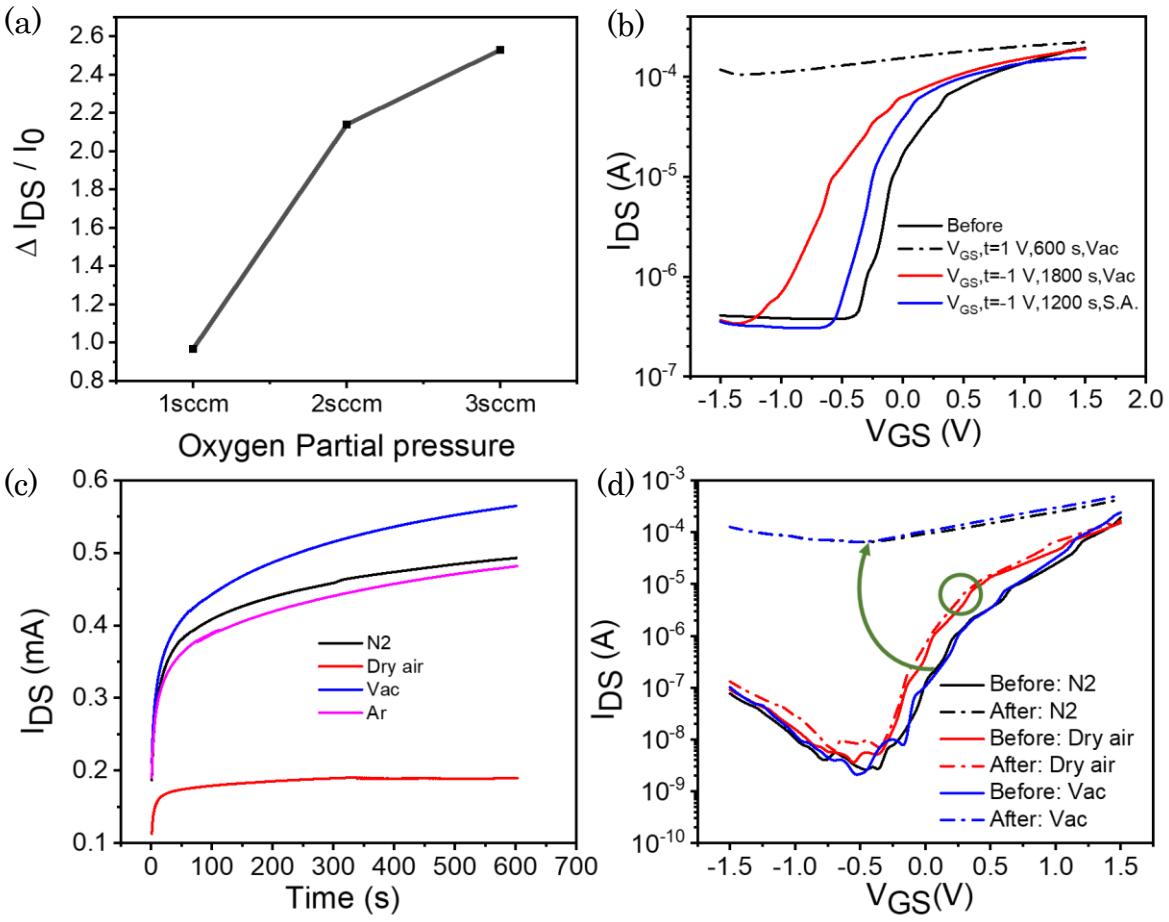

Figure 6-5: (a) Drain current variation with respect to oxygen partial pressure before and after biasing voltage for 600 sec. (b) effect of introduction of dry air on the transfer characteristics with ionic liquid gating by applying positive and negative voltage. The black solid line indicates original transfer characteristics; dotted black line indicates transfer characteristics after biasing of 1V for 600 s in a vacuum, the red and blue line represents transfer characteristics after 1800 s biasing in a vacuum and 1200 s biasing in synthetic air respectively on the same device. (c) effect of vacuum and various gaseous environments (Nitrogen, dry air, Argon) on the constant bias current (V_g = 1V) (d) Transfer characteristics before (Solid line) and after (dotted line) biasing in a different environment (V_d = 0.3V). Black color represents biasing in Nitrogen air, Red color represents biasing in dry air, and the blue curve represents biasing in a vacuum. W=1000 μm, L=150 μm. [1] Reproduced with permission from ACS Publications.

From our studies (displayed in **Figure 6-5**b), the modulation of oxygen vacancies is evident in terms of the shift in threshold voltage in the transfer characteristics curve of ionic liquid gated thin film transistor. However, it is essential to note in **Figure 6-5**b that the time required to shift threshold voltage to the left side (i.e., positive voltage biasing time) is much smaller than the time required to move it to the right side (i.e., negative voltage biasing time). This signifies that it is easier to remove the oxygen species than to reintroduce them back into the film matrix. The observed disparity may be explained as follows. On the application of the positive bias, the surface adsorbed oxygen species on the channel layer are removed initially followed by the oxygen species from the matrix of the thin film. However, the application of negative bias to return the dissolved oxygen species from the ionic liquid to the film is a more tedious process. This can be attributed to the low concentration of dissolved oxygen species in the ionic liquid, due to vacuum conditions in the measurement chamber.

In order to verify the hypothesis, dry air was introduced in the measurement chamber to increase the oxygen content. From **Figure 6-5**c it is clear that a dry synthetic air (pure oxygen (20%) with pure nitrogen (80%) to minimize the effect of water content in ionic the liquid) environment is more favorable than a vacuum for the application of negative bias to reintroduce oxygen species. Though there is a marked improvement in the positive shift of V_{th}, indicating increased oxygen concentration in the film, there is no return to the original V_{th}. The variation of V_{th} involves a combination of the variation of oxygen present in the matrix of oxide and the variation of surface adsorbed oxygen. A precise restoration of these oxygen levels is difficult to achieve. This experiment highlighted the need to investigate the effect of different gases present in the environment. Further experiments were performed, to substantiate the claim that the modulation of oxygen vacancies is indeed responsible for the variation in V_{th} and ON-state current during bias application. The rate of removal of oxygen species from the film is dependent on the number of oxygen species present in the ionic liquid. An abundance of dissolved oxygen in the ionic liquid will render the extraction of oxygen species from the film into the ionic liquid more difficult. In order to investigate this effect, the biasing current flowing through the TFT in vacuum was

compared to that in different gaseous environments, i.e., Argon, Nitrogen, and synthetic air.

From **Figure 6-5** (c), it can be observed that the increase in biasing current was highest for vacuum environment, while the current was lowest in synthetic air. This behavior confirms the effect of dissolved oxygen in ionic liquid. The oxygen present in synthetic air, saturated the ionic liquid with dissolved oxygen, hampering the oxygen extraction from the underlying oxide film. This, in turn, generated fewer oxygen vacancies in the film, leading to a lower rate of increase in drain current. In the case of vacuum, Argon and Nitrogen environment, where a minimal amount of oxygen is present, the amount of dissolved oxygen in the ionic liquid is lower which helps in easier extraction of oxygen from the oxide film, leading to a higher rate of increase in drain bias current. **Figure 6-5** (d) compares the before and after biasing transfer characteristics of thin-film transistors in the aforementioned environments. The negative shift in threshold voltage and increase in ON-state current in nitrogen, Argon, and vacuum environments is substantial when compared to the changes in these parameters in synthetic air, which is in agreement with the biasing current experiments.

6.2.3 Effect of biasing parameters: Biasing time, gate and drain voltage bias

From the previous experiments, it has been proven that the manipulation of TFT characteristics using the high electric field of the EDL is influenced by the high electric field and environmental conditions. The electric field is also dependent on various parameters such as biasing voltage at the gate and drain at the time of biasing. These parameters will affect the modulation of oxygen species, inevitably affecting the device behavior. **Figure 6-6**a depicts the shift in the transfer characteristics of ionic top-gated IWO TFTs with biasing time. The characteristics were recorded immediately after 100 s, 300 s, and 1200 s of application of the electric field (V_{GS}= 1 V, V_{DS} = 0.3 V). The corresponding shift in calculated mobility, V_{th}, $I_{on,}$ and I_{off} with respect to biasing time at the same gate voltage and drain voltage are summarized in **Figure 6-6**b. The values of V_{th} were extracted from the linear fit in I_{ds} versus V_{gs} curves in the linear region. It can be concluded that an

increase in bias time shifts the V_{th} negatively and increases the drain current, indicating increased generation of oxygen vacancies.

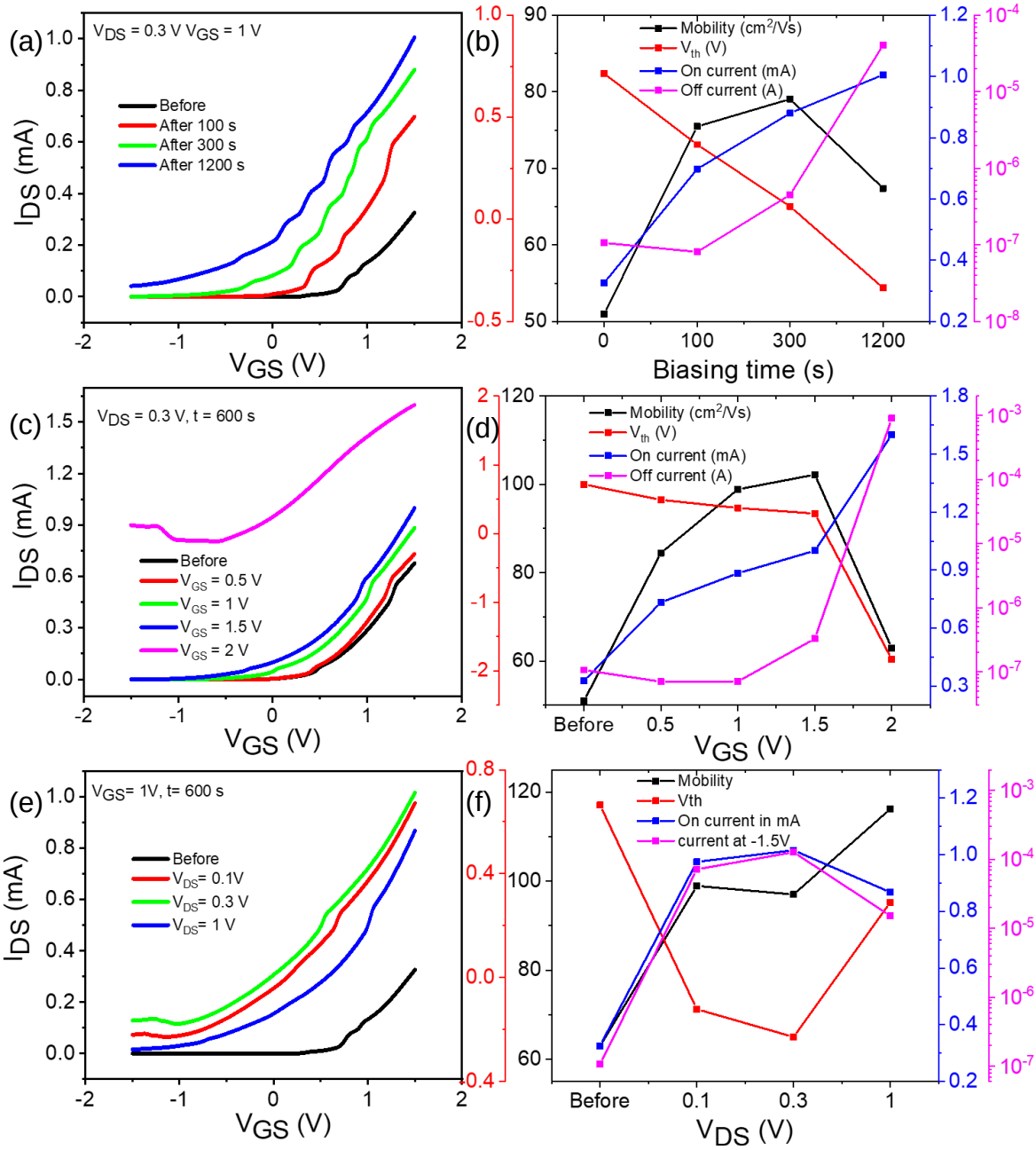

Figure 6-6: (a, c, e) Depicts the transfer characteristics of the transistors subjected to various dosages of the electric field (biasing time, biasing gate voltage at same drain voltage and biasing drain voltage at same gate voltage respectively) in the top-gated configuration. (b, d, f) summarizes the shift of mobility, threshold voltage, I_{on} and I_{off} as a function of the bias time and biasing gate and biasing drain voltage respectively. W=1000 μm, L=150 μm. [1] Reproduced with permission from ACS Publications.

Biasing voltages also influences the electric field induced oxygen modulation. **Figure 6-6**c illustrates the effect of a constant gate bias voltage on the transfer characteristics at a constant drain bias of 0.3 V and constant biasing time of 600 s. It is clear from the figure that, a higher gate voltage facilitates increased removal of negatively charged oxygen species. The 0.5 V gate bias has minimal effect, while a 2 V gate bias makes the film conductive. The corresponding shift in calculated mobility, V_{th}, $I_{on,}$ and I_{off} with respect to biasing gate voltage at the same drain voltage and biasing time are summarized in **Figure 6-6**d. Another parameter affecting the electric field is the drain voltage. Effect on transfer characteristics, due to variation in drain voltage, at a constant gate bias voltage of 1V is shown in **Figure 6-6**e. The transfer characteristics measured at Vd = 1 V, show a decrease in drain current, compared to that at Vd = 0.1 V. The larger drain voltage of 1 V can lead to an enhanced electron extraction from the channel near the drain terminal. This reduces the local electric field with the ionic liquid/channel interface near the drain terminal. A weaker electric field diminishes the yield of oxygen removal from the channel, resulting in lesser vacancies. The corresponding shift in calculated mobility, V_{th}, $I_{on,}$ and I_{off} with respect to biasing time at the same gate voltage and drain voltage are summarized in **Figure 6-6**f.

The effect of oxygen vacancy modulation on the performance of TFT is mainly manifested as an increase in ON-current. After biasing to modulate oxygen vacancies, the maximum mobility of the IL gated IWO TFT increased from 33.1 to 105.25 $cm^2/V.s$. The subthreshold swing reduced from 445 mV/dec to 230 mV/dec and V_{th} shifted from 0.4 V to 0 V. For transistors operating in the enhancement-mode or in the inactive state with low initial carrier concentration; this approach provides sufficient carriers exceeding trap densities resulting in increased mobilities. However, further increase in bias amplitude or time results in the creation of excess oxygen vacancies, increasing the effective carrier concentration by a significant amount as evidenced by substantial increases in off - and on-currents for devices. Such excessive increase in the carrier concentration results in the screening of the gate field, reducing the slope and hence, mobility in our devices. Such excess carrier-induced gate screening effects have been previously observed in several

devices, including oxide and organic semiconductors[23]–[25]. Other possibilities could include deleterious chemical reactions caused by impurities such as water in the ionic liquid.

6.2.4 Applications of oxygen vacancy variation using ionic liquid gating

Thus, in this work, the claim of field-driven oxygen vacancy generation is supported through systematic electrical parameter analyses and spectroscopic measurements. **Figure 6-7**(a) compares the conventional annealing parameters with EDL annealing parameters to modulate oxygen vacancies. To demonstrate the ultimate use of this approach as an alternative to conventional high-temperature deposition and annealing strategies in order to modulate device parameters using the EDL gating technique the possibility of activating a non-functional transistor was demonstrated in **Figure 6-7**(b) (with 1 V biasing voltage applied for 40 min). It can be clearly seen that the initially non-functioning TFT (black) was activated to a working transistor with mobility of 7.1 cm^2/Vs and the on-off ratio of 10^6. As indicated previously, the high temperatures required to access high performance in oxide semiconductors makes it incompatible with plastic substrates. Thus, efforts to modulate the local electronic structure and oxygen stoichiometry of oxygen-compensated thin films deposited on flexible polyimide substrates were also made. Thin films of IWO were sputtered under same conditions used for Silicon substrates on 130 nm Al_2O_3 (deposited via Thermal atomic layer deposition) with Titanium metal as a gate electrode. Al_2O_3 and EMIM TFSI served as the bottom and top gate dielectrics, respectively (structure of flexible TFT, **Figure 6-7** d,e). More details of fabrication and detailed characterization of flexible TFT are stated in the experimental section and chapter 4. To these flexible devices, the ionic liquid was used as gate dielectric and with the application of electric field (1 V, 600 seconds) generated additional carriers in the channel, resulting in depletion mode devices. The devices could be brought back close to its original state by biasing in synthetic air. The transfer characteristics of these ionic liquid gated TFT are shown in **Figure 6-7**c.

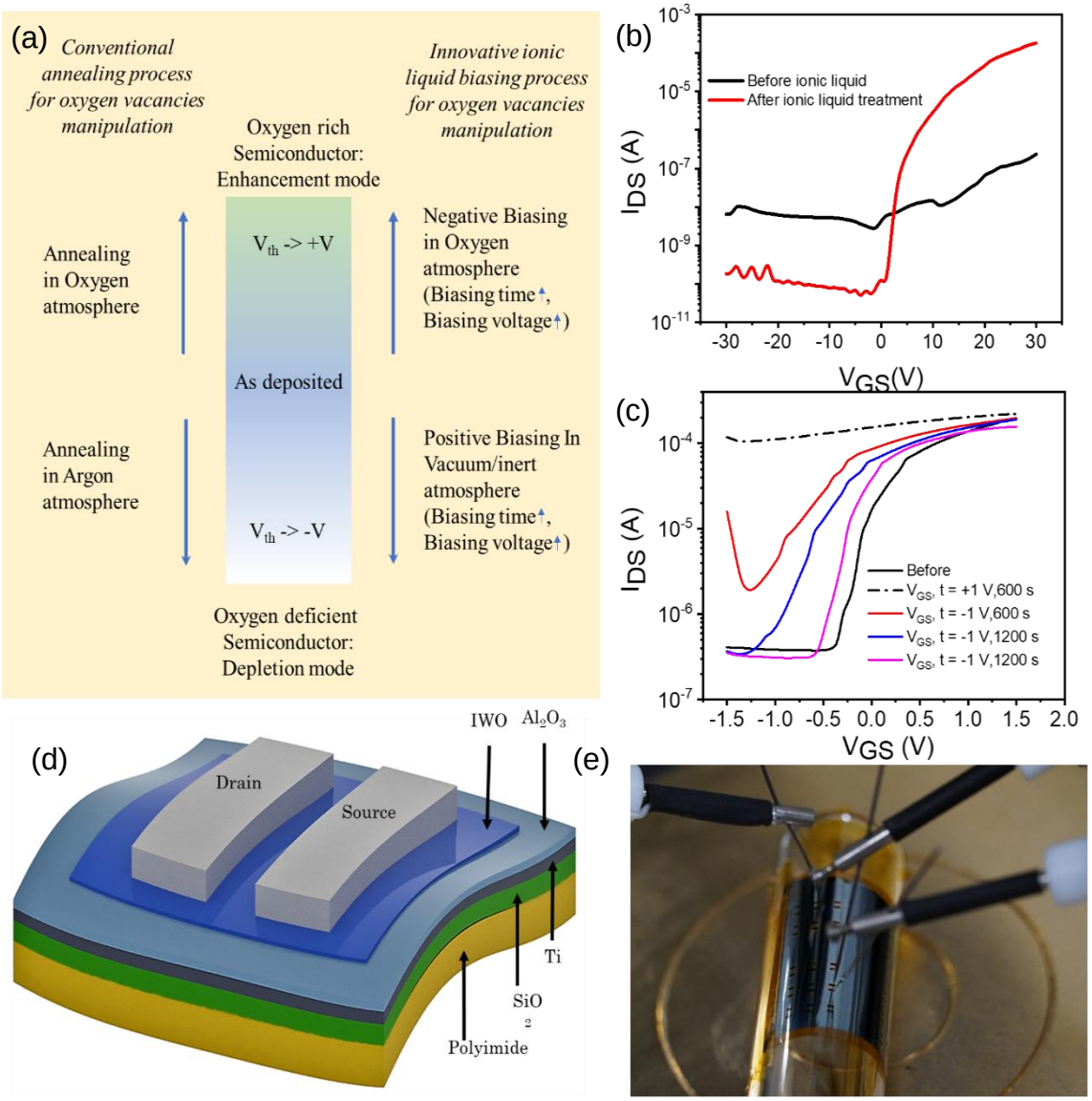

Figure 6-7: (a) Comparison between conventional vs. ionic liquid biasing for oxygen vacancies modulation (b) activation of not working bottom-contact thin film transistor, V_{DS} of 10 V W=1000 µm, L=150 µm (c) Reversible transfer characteristics of Ionic liquid-based flexible thin-film transistor with the applied electric field. Black solid line indicates original transfer characteristics, dotted black line indicates transfer characteristics after biasing of 1 V for 600 s in vacuum, the red line represents transfer characteristics after 600 s in vacuum, blue line corresponds to transfer characteristics after biasing for 1200 s in vacuum and magenta line corresponds to transfer characteristics after 1200 s biasing in synthetic air on the same device. (V_{DS} =0.3 V) W=1000 µm, L=150 µm (d) structure of flexible thin-film transistor, (e) fabricated flexible TFT mounted on the curved surface of 1.5 cm diameter. [1] Reproduced with permission from ACS Publications.

By creating additional oxygen vacancies in the semiconducting channel, this field-driven approach also enables selective activation and programming of TFTs to enhancement and depletion-modes in an on-demand manner, paving the way for the facile realization of logic circuits like inverters without additional fabrication steps. To demonstrate this, an array of 6 X 6 IWO TFTs (**Figure 6-8**a) were sputtered on a 2.5x2.5 cm^2 SiO_2 substrate (bottom) and the ionic liquid was top gated in a drop-on-demand manner (on TFTs showed in yellow color) and biased with positive voltage to create oxygen vacancies and form a depletion mode TFT. **Figure 6-8**b displays transfer characteristics of this depletion mode TFT and the original enhancement mode TFT. All the transistors depicted comparatively low carrier concentration in their back-gated channel before the field-driven activation process. The 1st column of transistors was allowed to remain in the enhancement mode, while the next column was programmed to the depletion mode by biasing 1 V for 800 seconds. The mobility and V_{th} of one of these back-gated enhancement devices were 8.09 cm^2/Vs and 11.81 V respectively while that for depletion devices were 14.49 cm^2/Vs and -2.11 V respectively. Conventional thermal annealing strategy is a global annealing technique that does not allow for selective activation. Fabricating depletion mode and enhancement mode transistors on the same substrate would need separate deposition and masking steps which can be avoided using the present approach. This active on-demand programmability of the operation mode of transistors facilitated facile fabrication and tuning of logic circuits like inverters.

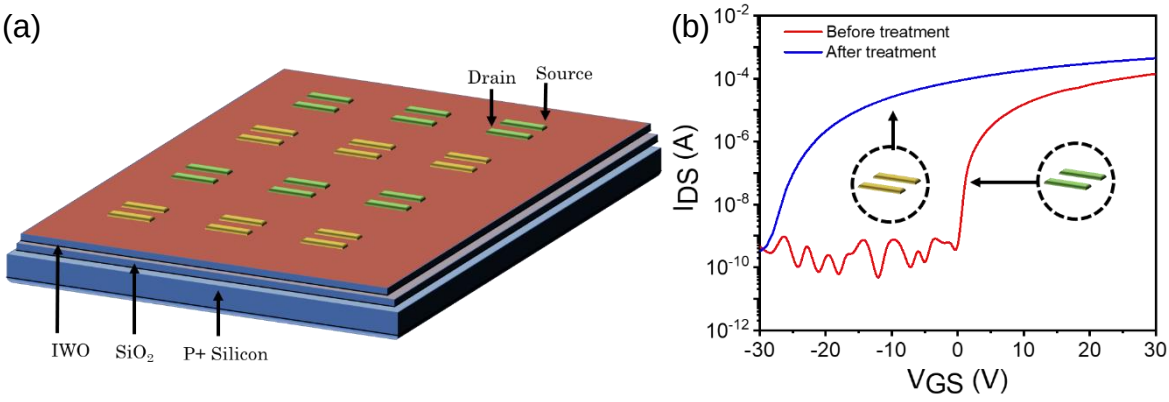

Figure 6-8: (a) Array of 6 X 6 IWO back-gated TFTs made into row-wise on demand depletion and enhancement TFTs (b) back gated transfer characteristics of on-demand depletion and enhancement TFTs in the array, V_{DS} of 5 V. W=1000 μm, L=150 μm. [1] Reproduced with permission from ACS Publications.

6.2.5 Double enhancement mode TFT inverter

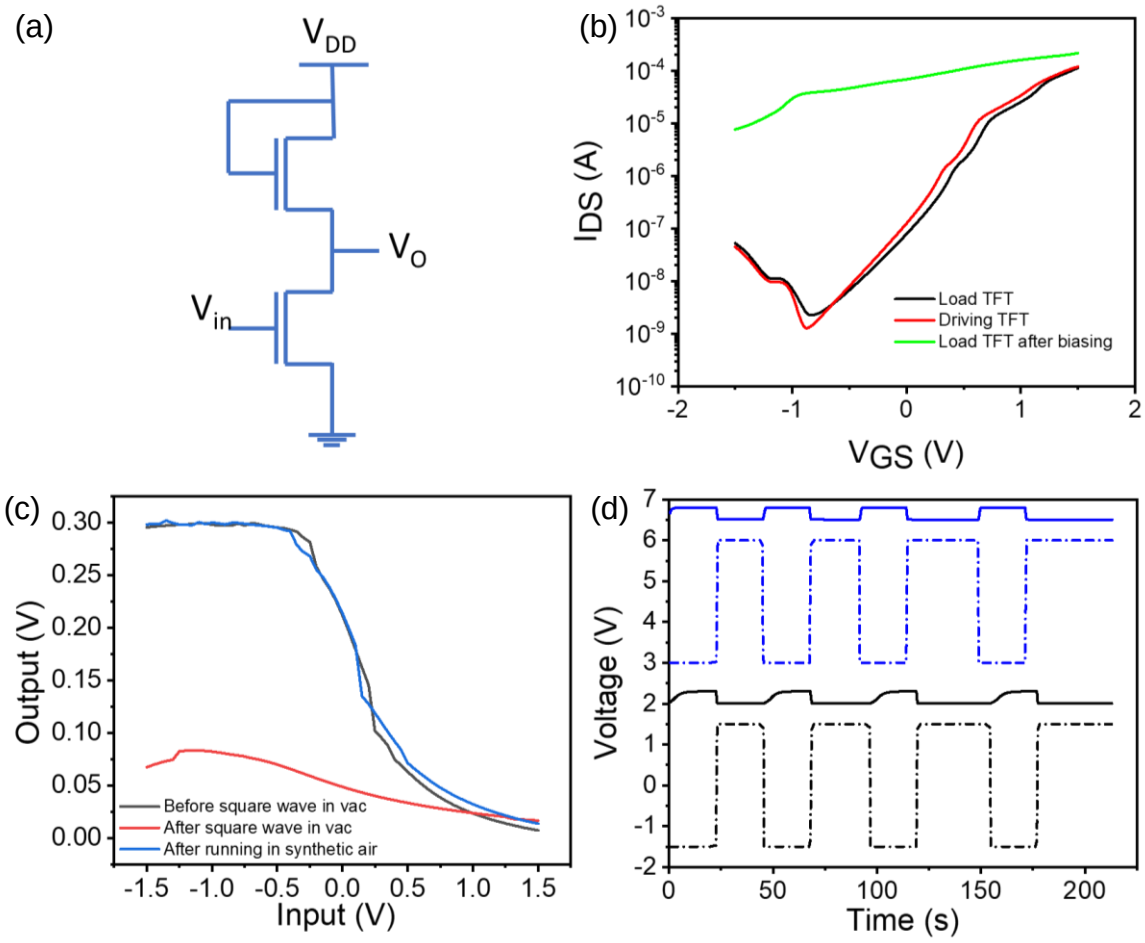

Figure 6-9: (a) Schematic illustration of the inverter using n-type thin film transistor (b) ionic liquid TFT used for inverter purpose (c) the static voltage inverter characteristics realized with ionic liquid biasing for different conditions. The black line corresponds to the original inverter characteristics. The red curve is inverter characteristics after operating inverter in a vacuum with a square wave. The blue curve shows the repaired characteristics of the same device after operating it in synthetic air with a square wave (d) stacked graphs of Output characteristics of the inverter with a square wave as input in synthetic air vs. vacuum. The dotted (solid) black curve is the input (output) square wave in the vacuum. And the dotted (solid) blue curve is the input (output) square wave in the synthetic air. [1] Reproduced with permission from ACS Publications.

In order to demonstrate this, ionic gated inverters were fabricated here via a single-step sputtering process. With its promising electrical performance, the ionic gated transistor was used in the fabrication of a double enhancement mode TFT inverter, for possible

application in logic gates. **Figure 6-9**a shows the schematic of a double enhancement mode TFT inverter. In this mode, the top TFT (Load TFT) works as a load to limit the current flowing through the bottom TFT. When a positive voltage is applied to the bottom TFT (Driving TFT), it turns on, shunting the output terminal to ground (state zero). When supplied with a negative voltage (state zero) the TFT is in an off state, allowing current to pass through the output terminal (state one), thus inverting the input. Prior to the field-activation process, both the load and driver transistors depicted an enhancement-mode operation with V_{on} around 0 V. The load transistors were then subjected to electric fields of 1 V for 1200 s to induce additional carriers in the channel shifting the V_{on} negative. Transfer characteristics for ionic gated load and driving TFT used for inverter are shown in **Figure 6-9**b. The load TFT has to be in normally-ON condition, and driving TFT should be in normally-OFF condition. Therefore, load TFT was biased for 1200 seconds, which shifted its threshold voltage from 0.89 V to -0.31 V. Thus, the Load TFT was in normally-ON condition at zero voltage. This can be seen from transfer characteristics. To our knowledge, this was the first ionic gated inverter demonstration.

Figure 6-9c demonstrates the static voltage transfer characteristics of the inverter with V_{DS} of 0.3V. Due to the high electric field imposed by the ionic liquid, on the application of voltage, the oxygen vacancies vary, resulting in degradation of the inverter transfer characteristics. **Figure 6-9**c shows the initial transfer characteristics in a vacuum with a gain of 0.61, that gets severely degraded to a gain of 0.09 after a square wave is run for 200 s from this inverter. However, with the introduction of dry air and a repeat of square wave measurement, this degradation is reversed, and the original transfer characteristics with a gain around 0.61 is recovered. Another important characterization parameter for an inverter is its output characteristics. **Figure 6-9**d shows the output characteristics of the inverter with a square wave as input in synthetic air vs. vacuum environment. It can be noted from the figure that the rise time and fall time is faster when operating in synthetic air. This can be attributed to the change in V_{th} due to variation of surface adsorbed oxygen on IWO as the interstitial oxygen species manipulation is a relatively slow process and it may not be able to react to a fast change occurring with square wave input. A constant current is flowing through the bottom TFT in the vacuum environment for a longer duration results

in increased carrier concentration due to decrease in the oxygen concentration on the surface of IWO, causing the negative V_{th} shift. The negative V_{th} shift of the bottom TFT does not allow the transistor to switch off completely, leading to the sluggish response. However, in synthetic air, the variation of carrier concentration is hugely suppressed because of the higher concentration of oxygen already present in the atmosphere of the synthetic air compared to vacuum. This is in agreement with the decrease in oxygen vacancy variation observed in the case of constant biasing applied in synthetic air (**Figure 6-5**). Hence, operating ionic gated transistors in synthetic/oxygen environment might be beneficial for stability and faster rise and fall time (**Figure 6-10** a and b shows a comparison between input-output characteristics of inverter in a vacuum vs. synthetic air depicting sharper turn off in synthetic air operation than in vacuum operation). The superior operation of the ionic liquid gated inverter in synthetic air can be attributed to the V_{th} stability of the bottom ionic liquid gated transistor characteristics while in operation.

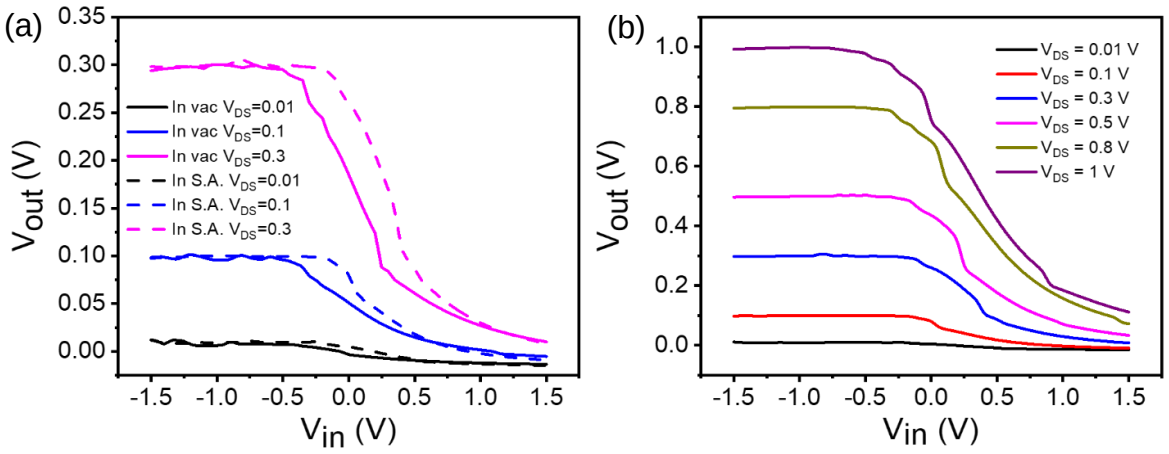

Figure 6-10: (a) Comparison between input-output characteristics of inverter in a vacuum and synthetic air. The solid line was before measurements and dashed line after measurements in synthetic air (b) the input-output curve for an inverter for different V_{DS} in synthetic air. [1] Reproduced with permission from ACS Publications.

6.2.6 Neuromorphic Synaptic device

As a final demonstration of the utility of this field-driven oxygen vacancy generation approach, neuromorphic transistors with programmable plasticity were realized in a comprehensive manner, correlating the above explanations with weight plasticity. Very recently, electrolyte-gated FETs have been extensively researched for hardware emulation of biological signal processing.[20], [26] Contrary to mass storage and conventional logic operations, emulation of biological signal-processing set unique requirements on the hardware switching devices, namely- a strong operational history, analog (non-abrupt) switching transitions, continuously distributed conductance states and programmable plasticity.[27] Although two-terminal memristive solutions have dominated this research area, three-terminal FET-based solutions have recently received significant scientific attention in this regard.[28]–[30] With a gated control of channel conductance exploiting time-dependent hysteresis and programmable shifts of threshold voltage (V_{th}), the thin-film transistor (TFT) configuration is promising in achieving programmable plasticity, compatible with spike-based computing algorithms.[28] Here, the hysteresis and field-driven oxygen-getting ability of electrolyte-gated TFTs was harness to demonstrate volatile and non-volatile switching characteristics, emulating short and long-term plasticity features respectively. Electrostatic doping due the large EDL capacitance caused volatile switching of memory states, accounting for short-term plasticity features, while the field-driven extrusion/intercalation of charged oxygen species created non-volatile changes in channel conductance, accounting for long-term plasticity features. Ionic migration-relaxation kinetics in the ionic liquid mimicking Ca^{2+} influx in dendritic spines modulated the electronic conductance-state of the semiconducting channel, while charge transport pathways emulated the synaptic cleft, and channel-conductance defined the synaptic weight. The pre- and post-synaptic potentials at the gate and source terminals tuned the post-synaptic channel conductance, read via the drain terminal (**Figure 6-11**a).

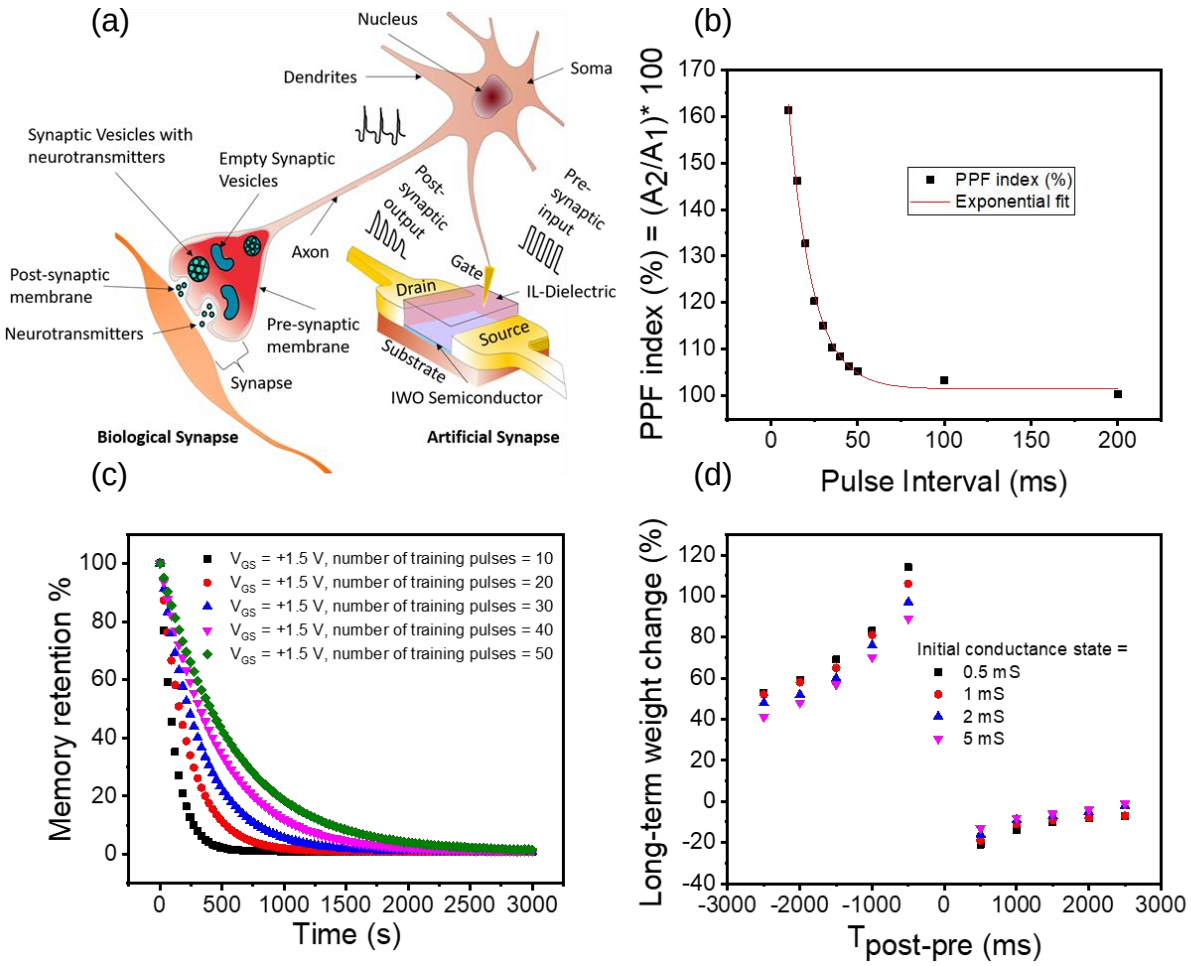

Figure 6-11: (a) Schematic of a biological synapse and an artificial synapse based on ionic liquid-gated IWO-based electric-double-layer (EDL) transistor (b) PPF index as a function of pulse interval reflecting the ion migration-relaxation dynamics at the semiconductor-dielectric interface (c) memory retention behavior as a function of the number of presynaptic pulses following a trend defined by Ebbinghaus's forgetting curve (d) Spike-Timing-Dependent-Plasticity (STDP) with respect to various conductance states. [1] Reproduced with permission from ACS Publications.

Classified based on the timescales of operation, short and long-term plasticity rules[31], [32] defining learning and memory were studied by recording excitatory postsynaptic currents (EPSCs)[33] in response to pre- and post-synaptic training sequences. A single pulse of (+ 1.5 V, 20 ms) at the gate terminal evoked a pulsed response of drain current (called Excitatory postsynaptic current (EPSC)) of 12.4 μA, which decayed back to its resting level of ~ 10 nA on the removal of the presynaptic pulse (**Figure 6-12**). A paired-pulse activation resulted in higher secondary EPSCs with an exponential dependence on

the pulse interval between the spikes, resembling a phenomenon called Paired-pulse facilitation (PPF). The PPF indices were strong (>> 100 %) for small pulse intervals (< 25 ms) and weakened with increasing pulse intervals up to 200 ms, indicating a strong temporal dependence (**Figure 6-11**b, **Figure 6-12**b).

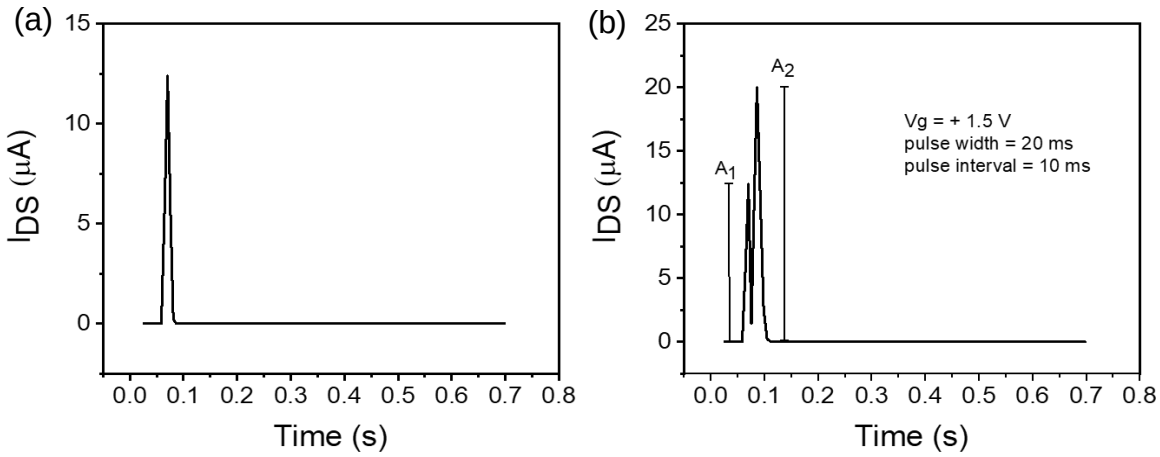

Figure 6-12: (a) A single presynaptic spike input induced an excitatory postsynaptic current (EPSC) response (b) a pair of presynaptic spikes (pulse width = 20ms, interval = 10ms) triggered a pair of EPSCs, with the amplitude of the 2nd (A_2) higher than the 1st (A_1). This indicated facilitation is due to ionic migration and relaxation at the semiconductor-dielectric interface. PPF index, defined as the ratio of A_2/A_1, that is [PPF = (A_2/A_1) * 100%]] is plotted as a function of the inter-spike interval to demonstrate facilitation decay. It quantifies the degree of facilitation and reflects the synaptic vesicular release probability. [1] Reproduced with permission from ACS Publications.

The maximum PPF index of ~ 161% was observed for a pulse interval of ~ 10 ms. This ratio decreased with increasing pulse interval and finally reached around 100 % for the largest pulse interval of 200 ms. In resemblance to the coupling of biological neurons, PPF variation with pulse interval fit well with an exponential decay function as shown below.

$$y = B_1 * \exp\left(-\frac{x}{t_1}\right) + y_0 \text{.....Eq. (3-8)}$$

where x is pulse interval time, y_0 is resting facilitation magnitude, B_1 is the facilitation constant, and t_1 is the characteristic time constant of decay phase. Detailed comparison of the decay time constants is presented in **Table 6-1** below. In all the above measurements,

short nature of the training sequences resulted in the decay of post-synaptic currents (PSCs) back to the initial state due to ion relaxation mechanisms, analogous to short-term plasticity.[34] With the ionic top-gated TFTs operating at 0.01 V (V_{ds}), the power consumption was calculated to be ~ 2.5 nJ per synaptic event (calculated from the peak value of the 1st EPSC) for the best-performing devices.

Table 6-1: Best fit values of PPF decay as a function of pulse interval

Mode	y0	A1	t1	Reduced Chi-Sqr	R-Square(COD)	Adj. R-Square
ExpDec1	101.42957	126.4018	13.78752	2.29455	0.99525	0.99406

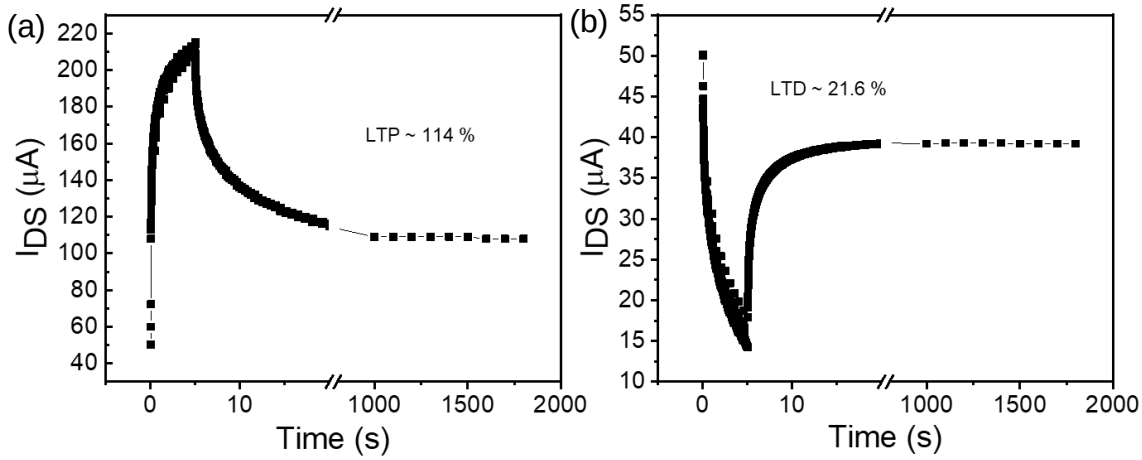

Figure 6-13: The pulse train of ten excitatory (+1.5 V) and inhibitory (-1.5 V) pulses of width 500 ms resulted in a non-volatile (a) weight potentiation of 114% and (b) weight depression of 22%. The devices were set to the same initial conductance state of 0.5 mS, and the final conductance is taken to be 30 minutes after the application of pulse trains. This non-volatile changes to the channel conductance are due to the creation of oxygen vacancies in the semiconductor channel. Long-term plasticity (LTP) signifies the physical changes of the structure of neurons with a retention characteristic from hours to years. [1] Reproduced with permission from ACS Publications.

Persistent training consolidated the weight changes, leading to precisely controlled non-volatile changes in channel-conductance, emulating long-term plasticity features.[31], [35] Application of 10 excitatory (+ 1.5 V) and inhibitory (- 1.5 V) pulses of pulse width 500 ms resulted in a non-volatile weight potentiation of 114 % and depression of 22 % starting from the same initial conductance state of 0.5 mS (**Figure 6-13**). For long-term weight analysis, the following approach was used in these experiments throughout. (i) Read the

channel conductance with V_{ds} = 0.1 V. (ii)Apply necessary voltage waveforms to induce non-volatile weight change/ long-term plasticity. (iii) Monitor the channel conductance 30 minutes after application of the waveforms and compare it to the initial conductance state to calculate weight %.

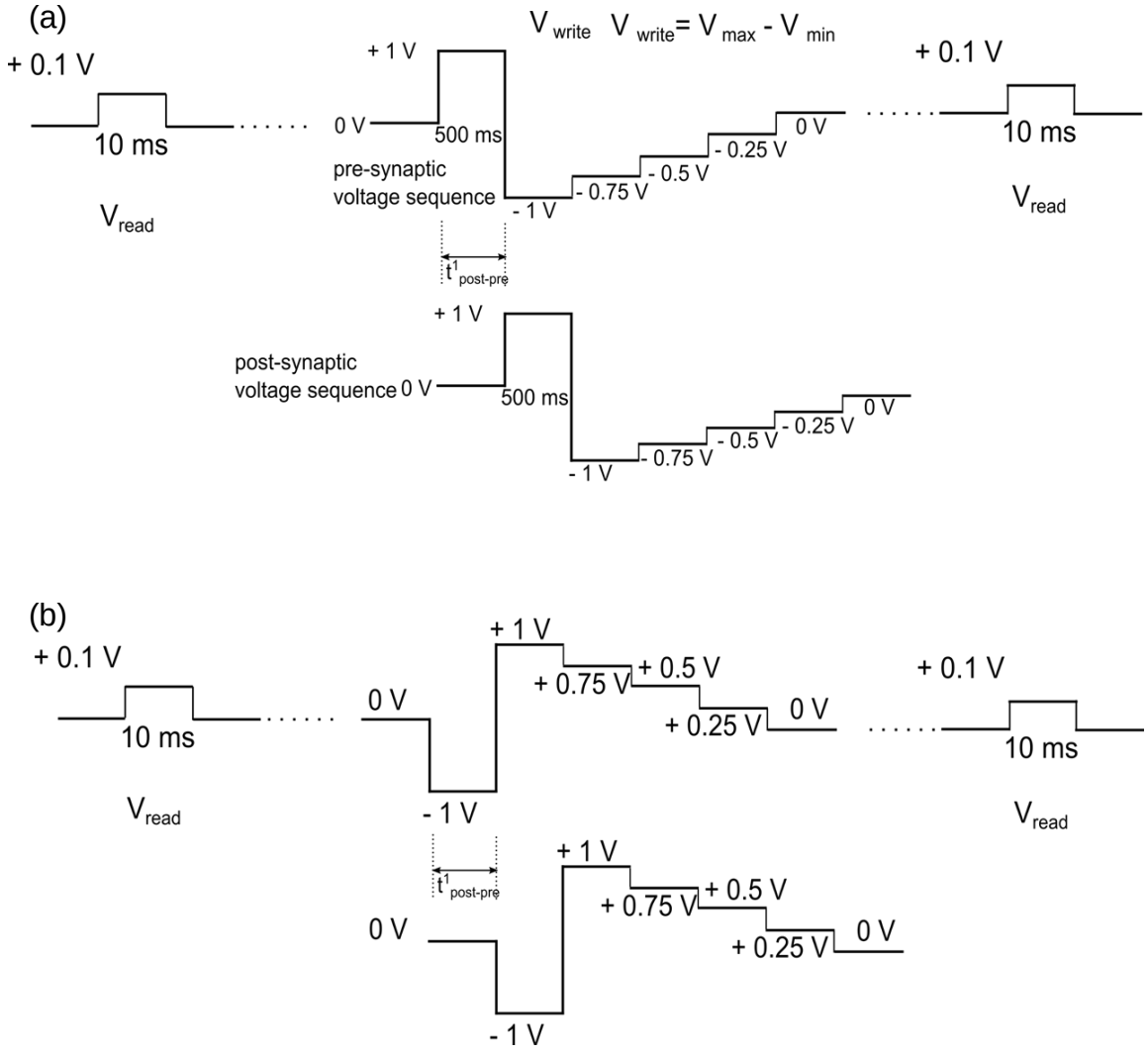

Figure 6-14: Input waveforms used to generate STDP data (a) the asymmetric anti-Hebbian and (b) asymmetric Hebbian. The pulse width used for this measurement= 500 ms. The resultant waveform is an interval-dependant function based on the pre-synaptic and post-synaptic waveforms, enabling temporal manipulatable weight changes by changing the pulse intervals. [1] Reproduced with permission from ACS Publications.

Directly proportional to the number, duration, and amplitude of the training pulses, these devices depicted enhanced learning rate and memory retention with repetitive training

sequences as depicted by Ebbinghaus's forgetting curves (**Figure 6-11** c). Spaced repetition resulted in softening of the downward slope of the forgetting curve, indicating modulation of the strength of memory and process of forgetting that occurs with the passage of time. Next, spike-based computing rules, also known as spike-timing-dependent plasticity (STDP) rules were emulated in these devices with the gate and source terminals acting as pre- and post-synaptic terminals and the drain terminal probing the change in channel conductance/weight. A refinement of Hebb's theory, STDP is considered to be the first law of synaptic plasticity and is believed to underlie learning and memory in neural networks.[36] In glutamatergic connections, strengthening/ long-term potentiation (LTP) occurs if the presynaptic spike precedes the post-synaptic spike ($t_{post-pre} > 0$, where δt is the relative time interval between the pre- and post-synaptic spikes), while presynaptic spikes following post-synaptic spikes ($t_{post-pre} < 0$) causes weakening/ long-term depression (LTD).

In these devices, spike patterns corresponding to **Figure 6-14** created interval-dependant net voltage changes across the device, resulting in temporally manipulatable weight changes following an asymmetric anti-Hebbian rule (**Figure 6-11**d, **Figure 6-15**), and asymmetric Hebbian behavior (**Figure 6-15**) analogous to biological systems [37], [38]. For example, an interval ($t_{post-pre}$) of + 500 ms resulted in a net voltage of V_{pre}-V_{post} = (-0.75) – (+0.75) = - 1.5 V developed across the device, triggering a permanent decrease in the channel conductance or LTD (~ 22 %). On arrival of presynaptic pulses after postsynaptic pulses, i.e. $t_{post-pre}$ of - 500 ms, the maximum net voltage developed across the device was V_{pre}-V_{post} = (+ 0.75) – (- 0.75) = + 1.5 V and this resulted in an increase in conductance or LTP (~ 114 %). These measurements were repeated for several combinations of spike intervals, and the weight changes were plotted as a function of $t_{post-pre,}$ as shown in **Figure 6-15**. Weight changes were predominant at small pulse intervals, and weakened with an increase in the interval, reflecting strong temporal correlations between the pre- and post-synaptic spikes. Interestingly, the magnitude of weight changes depicted a strong dependence on the initial channel concentration, as shown in **Figure 6-11**d. Devices with a lower initial channel conductance (0.5 mS, read at + 0.1 V) depicted larger weight changes compared to devices in the depletion-mode with a higher initial channel conductance (5 mS) for all temporal correlations between pre- and post-synaptic spikes.

This priming-like activity enhances the programmability of these artificial synapses, paving the way for highly-plastic neuromorphic circuits.[28]

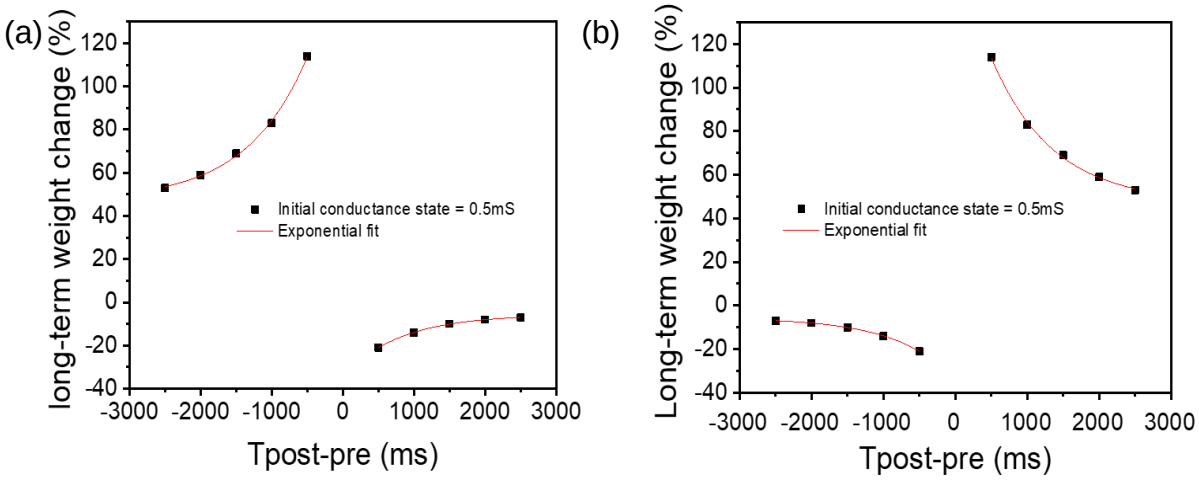

Figure 6-15: (a) The asymmetric anti-Hebbian and (b) asymmetric Hebbian characteristics of spike-time-dependant plasticity. The initial channel conductance state was set to be 0.5 mS before applying the waveforms. The characteristics show a strong temporal correlation between pre- and post-synaptic spikes. [1] Reproduced with permission from ACS Publications.

These non-volatile changes in conductance correlate to the creation of additional oxygen vacancies in the semiconducting channel, as detailed in the introductory sections of this study. Persistent stressing of the gate terminal with positive training pulses facilitate extraction of oxygen (creation of oxygen vacancies) from the semiconducting lattice to generate additional carriers for charge transport, resulting in a permanent shift of V_{th} and a long-term increase in channel conductance or in other words long-term potentiation. Higher electric fields or larger number of rehearsals (training pulses) accelerate this extraction process, shifting the channel conductance by more copious amounts, as depicted by the Ebbinghaus forgetting curves and strong temporal dependence of the STDP curves. Application of electric field in the opposite direction (negative biasing) intercalates oxygen back into the semiconducting channel, shifting the electrical parameters back to their original state and hence, causing long-term depression. The higher barrier for intercalation is again reflected by the lower numerical value of the depression indices in the STDP curve (**Figure 6-11** d).

6.3 Summary and Conclusion

In summary, field-driven athermal activation of AMOS is established comprehensively as a promising alternative to conventional high-temperature annealing techniques, enabling facile fabrication of flexible oxide electronics. The electric field-induced modulation of oxygen vacancies achieved in a Ga/Zn free a-IWO film by using an EDL formed at the interface due to ionic liquid gating was demonstrated. The controlled shifting of the threshold voltage demonstrates the tunability of the transistor characteristics. The effect of environmental gas, biasing time, and biasing voltages on the modulation of oxygen species using ionic liquid were systematically investigated. The results indicated that the presence of oxygen in the environment of IL gated TFT hampers the oxygen vacancy generation, decreasing the rate of increase in carrier concentration. The concentration of oxygen vacancies increases with increase in the biasing time, gate biasing voltage, and drain biasing voltage. However, for higher drain voltages, the decreased effective electric field in the channel leads to reduced oxygen vacancies creation. In addition, oxygen partial pressure at the time of deposition also influences the modulation of oxygen vacancies, with a relative increase in the modulation of oxygen vacancies observed for deposition at higher partial pressure. This control over oxygen vacancies manipulation enables not only selective activation of oxygen-compensated thin films without the need of high-temperature processing but also allows precise control over the carrier concentration and threshold voltage of active devices, facilitating on-demand programming of logic circuits and neuromorphic transistors. Also, the initially non-functioning TFT was activated to a working transistor with mobility of 7.1 cm^2/Vs and the on-off ratio of 10^6. High-performance ionic gated transistors with mobility of 105.4 cm^2/Vs were realized on flexible substrates using this technique at room temperature. A double enhancement-mode inverter utilizing the active modulation of the operational modes (enhancement and depletion) of TFT was also demonstrated. Finally, precise control of these conductance changes via active generation/depletion of oxygen vacancies were portrayed as synaptic weight changes in a neuromorphic TFT configuration, paving the way for ultrafast high-performance bio-inspired spike-based computing circuits.

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Chapter 7

Discussion and future work

This chapter draws together the threads of this dissertation. The extent to which the hypotheses were addressed and a summary of the results are also discussed. The drawbacks and implications are reflected, and new opportunities and strategies for future work are identified. The future work conveys suggestions for developing on this dissertation work essentially covering, extending Ellingham diagram study for CMOS circuitry, scalability of inkjet printing based low-temperature oxide semiconductor activation/modulation using "Drop on demand", d*etailed investigation of surface treatments in order to further fine-tuning of the properties of oxide semiconductor, and exploration of these surface modification and oxygen vacancies modulation techniques for other applications*.

7.1 Summary

Tapping on to the need for new flexible device technology, this dissertation attempts to find novel techniques for athermal activation of metal oxide semiconductors for thin-film transistors. The dissertation also addresses the modification of the electrical properties of the semiconductor, to enable the device operation to be fine-tuned for emerging applications of oxide TFT such as flexible devices, oxide logic gates, and neuromorphic electronics.

With respect to the selection of oxide for flexible TFT and study of various device and process parameters: It was concluded that for IWO thickness of 20 nm, annealed at 200 ^{o}C, and fabricated with an oxygen flow rate of 1 sccm yielded the best device performance in terms of mobility and threshold voltage. The IWO TFT had the mobility of 15.07 cm^2/V.s, the threshold voltage of 1.17 V and a subthreshold swing of 1.9 V/dec. ITO electrodes proved to be the best electrode for IWO TFT. Flexible TFT was also demonstrated with excellent stability even under the cyclic test of 3mm diameter bending radium. Even though well functioning flexible devices with IWO were demonstrated, in order to achieve the full potential of various semiconducting oxides in flexible devices, an athermal semiconductor activation still needs to be explored. In addition, it is essential for new applications to have an athermal, on-demand control after manufacturing on the conduction of oxide semiconductor. Hence various novel mechanisms were studied to modulate the charge carrier concentration such as (i) use of the Ellingham diagram dictated the selection of the overlayer to reduce the underlying oxide (increase in oxygen vacancies) (ii) various surface chemical treatments capable of creating surface dipoles and doping to modulate charge carrier concentration (iii)Passivation of oxygen vacancies by wet chemical oxidation. (iv) Electric field-driven modulation of oxygen vacancies.

Using the Ellingham diagram, a capping material can be selected to achieve better modulation for device fabrication at lower temperatures. The experiments were done to crosscheck the hypothesis and to select the best thickness. It is imperative to note that capping leads to enhanced device stability, compared to an un-capped device. The

properties of an un-capped vs. capped TFT were measured after one week. The uncapped device's threshold voltage negatively shifted by 12.1V with increased mobility. This observation indicates that there was a large extent of water adsorption on the channel layer, which created more charge carriers, causing mobility to rise, and the threshold voltage to fall. The fact that for an un-capped device, there was a drastic negative shift of threshold voltage, while for a device with a 3 nm-thick Al_2O_3 capping layer deposited with an oxygen flow rate of 1sccm, the negative shift of the threshold voltage was small, proves that a 3 nm of alumina capping layer improves device stability as well as performance. A thicker layer of Al_2O_3 deposition leads to conducting samples, indicating a complete oxide reduction of IWO as expected from the Ellingham diagram. Further experiments performed on the IGZO as channel layer and with various capping layers such as alumina, SiO_2, and Ca proves that this method is universal. Ellingham diagram can thus be very useful in low-temperature flexible device fabrication with and can pave the way for CMOS circuitry using oxide semiconductors. For all further studies, thinner semiconducting oxide layer (7nm) TFTs were used to allow surface treatments to influence the effective channel region.

Modification in charge carrier concentration by surface modification technique: Various surface modification techniques responsible for surface dipole creation and surface doping were used to alter the electronic characteristics of the oxide semiconductor channel in order to modulate the TFT characteristics. The investigation covered various types of surface treatments such as Silanes in the form of APTES, Thiols in the form of DDT and PFDT, charge-neutral polymers containing aliphatic amine groups PEI, PEIE, and dopant molecules such as TPPO (n-type doping). It was evident that the strong electron-donating characteristics of the amine group in PEI, and PEIE, as well as the dipole induced charge carriers in APTES and DDT, allowed a significant enhancement in the mobilities as well as V_{th} control in a negative direction. Apart from that, the use of fluorinated thiol, PFDT (one-day treatment) also has shown potential for modulating the threshold voltage in enhancement mode. The type of dopant is useful in controlling the threshold voltage the n-type dopant can be used for negative V_{th} shift, whereas p-type dopant can be used for positive V_{th} shift. The electron-donating capability of the surface dopant group such as amine group may enable the filling of the shallow electron traps of semiconductor, hence

improving the mobility. Eventually, this modification would help to achieve the next generation of flexible devices, applications which demand low processing temperature and selective control over conductance of channel.

Modulation of oxygen vacancies using wet chemical treatment for TFT results in a shift to enhancement-mode from depletion-mode: Surface state alteration through hydrogen peroxide assisted wet chemical treatment as a route for controlled passivation of oxygen vacancies that determine the electrical properties of IWO for flexible thin-film transistor application was investigated. The oxidized film characterization by XPS, UPS, Optical absorption spectroscopy, Mott-Schottky plot, and PESA measurements suggested the increased oxide content in the film. The use of athermal oxidation of TFT devices was demonstrated. This could enable the activation of fully depleted as-deposited TFT without exceeding the thermal budget of flexible substrates. Precise control on conductance value can be useful in applications such as neuromorphic electronics and synaptic devices. Apart from that, UPS studies indicated that H_2O_2 could be responsible for the over-oxidation of the surface. This function can be used to achieve environmental stability. The decreased -OH peak from O1s spectra belonging to adsorbed species after H_2O_2 treatment also suggests the cleaned surface of the oxide. This cleaning can be useful for unique applications such as photocatalysis.

Electric field-driven athermal activation of AMOS is established comprehensively as a promising alternative to conventional high-temperature annealing techniques, enabling facile fabrication of flexible oxide electronics. The electric field-induced modulation of oxygen vacancies achieved in a Ga/Zn free a-IWO film by using an EDL formed at the interface due to ionic liquid gating was demonstrated. The controlled shifting of the threshold voltage demonstrates the tunability of the transistor characteristics. The effect of environmental gas, biasing time, and biasing voltages on the modulation of oxygen species using ionic liquid were systematically investigated. The results indicated that the presence of oxygen in the environment of IL gated TFT hampers the oxygen vacancy generation thus decreasing the rate of increase in carrier concentration. The concentration of oxygen vacancies increases with increase in the biasing time, gate biasing voltage, and drain

biasing voltage. However, for higher drain voltages, the decreased effective electric field in the channel leads to reduced oxygen vacancies creation. In addition, oxygen partial pressure at the time of deposition also influences the modulation of oxygen vacancies, with a relative increase in the modulation of oxygen vacancies observed for deposition at higher partial pressure. This control over oxygen vacancies manipulation enables not only selective activation of oxygen-compensated thin films without the need of high-temperature processing but also allows precise control over the carrier concentration and threshold voltage of active devices thus, facilitating on-demand programming of logic circuits and neuromorphic transistors. Furthermore, the initially non-functioning TFT was activated to a working transistor with mobility of 7.1 cm2/Vs and the on-off ratio of 10^6. High-performance ionic gated transistors with mobility of 105.4 cm2/Vs were realized on flexible substrates using this technique at room temperature. A double enhancement-mode inverter utilizing the active modulation of the operational modes (enhancement and depletion) of TFT was also demonstrated. Finally, precise control of these conductance changes via active generation/depletion of oxygen vacancies were portrayed as synaptic weight changes in a neuromorphic TFT configuration, paving the way for ultrafast high-performance bio-inspired spike-based computing circuits.

In summary, the dissertation successfully investigated novel ways to modulate oxide TFT parameters athermally. The possible applications in flexible TFT, logic gates, and neuromorphic electronics were also explored with the help of the achieved modulation of oxide TFT.

7.2 Future work

1. Extending Ellingham diagram study for CMOS circuitry:

The capping layers chosen using Ellingham diagram[1] can also be designed and patterned to facilitate the transport of oxygen species from an oxidizing atmosphere in and out of the active layer, thereby selectively oxidizing certain areas of the active layer and reducing others. Such techniques would allow us to tune the transistor's threshold voltage. The

proposal is to form a p-type oxide and n-type oxide on the same substrate using this approach to facilitate CMOS fabrication based on oxide TFTs. For example, use of Ag_2O, CuO, Cu_2O, PbO, NiO, Fe_3O_4, etc. capping layers can serve as a local source of oxygen and help oxidize SnOx to SnO_2, as SnO_x will reduce Ag_2O because of its placement below the Ag_2O. Whereas SiO_2, TiO_2, Al_2O_3, MgO, CaO, etc. capping layer can help maintain an oxygen-deficient SnO state because their placement in the lowest region in the Ellingham diagram makes them stronger, reducing oxides. This could expedite the formation of CMOS logic circuits on the same substrate. Implementation of this requires precise control of the oxygen vacancy concentration and thickness of the oxygen-rich/ deficient overlayers. **Figure 7-1** shows complementary oxide semiconductor inverter structure (a) and process flow that can be used for deposition.

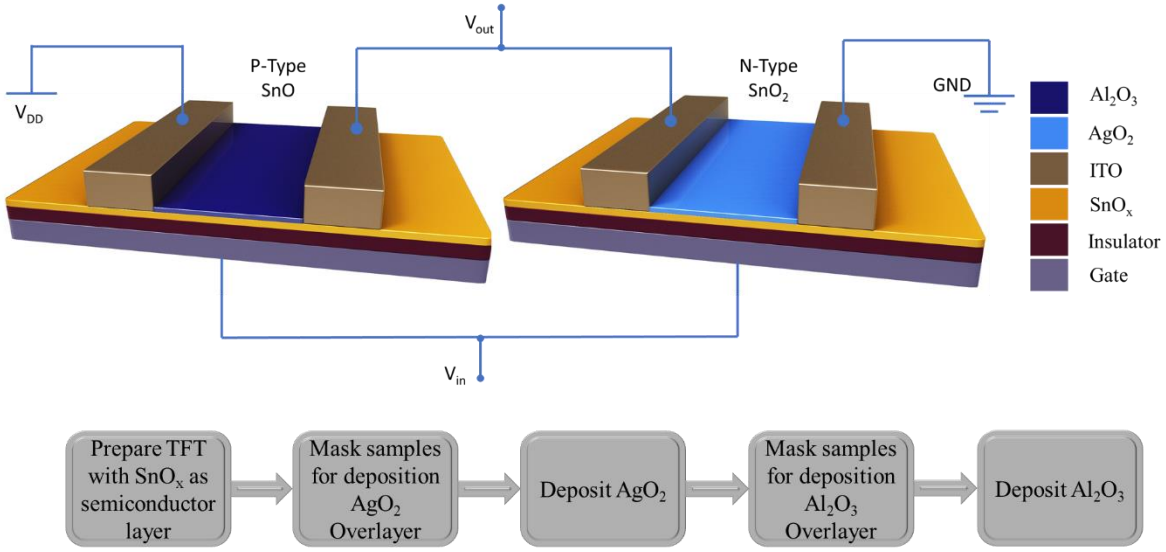

Figure 7-1: CMOS Inverter using p-type SnO and n-type SnO_2. And process flow for depositions to make CMOS inverter circuit.

2. Athermal passivation of oxygen vacancies for the flexible oxide semiconductor:

Use of oxidizing agent on flexible devices: The initial experiments done on the subject suggested demonstrated no effects on the channel formation on the flexible devices prepared with the H_2O_2 concentration and dip-time used in the experiment. This might be because of the higher dielectric constant of alumina compared to Silicon dioxide. Another technique, such as the use of H_2O_2 as a cosolvent in a supercritical fluid system can be

employed, which has been recently shown to affect the entire oxide thickness.[2] This would improve the effect of H_2O_2 on the entire oxide thickness, decreasing the charge carriers, and allowing more control over the TFT properties. In addition, various other highly oxidizing agents also can be used, such as Ag_2O, dichromate dianion ($Cr_2O_7^{2-}$), and Sodium superoxide (NaO_2). The depletion to enhancement mode conversion can be used for inverter configuration logic gates.

3. Scalability of inkjet printing based low-temperature oxide semiconductor activation/modulation using "Drop on demand":

The method of drop on demand can be used to selectively employ surface modification technique on the channel of specific TFT in order to facilitate the selective modulation of semiconductor parameters from the complete into row-wise on-demand depletion and enhancement TFTs. Eventually, this modification would help to achieve the next generation of flexible devices applications which demand low processing temperature and higher control over conductance of channel, which will, in turn, allow easier development of oxide-based logic gates. This method of semiconductor activation is beneficial for inkjet-

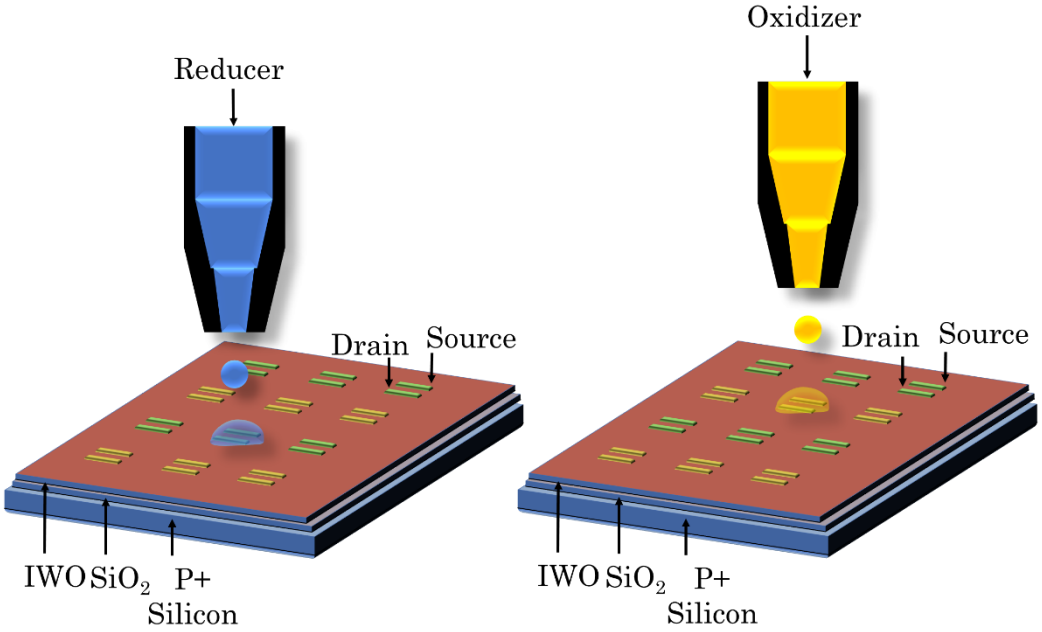

Figure 7-2: Drop on demand setup for changing the properties of oxide semiconductor from depletion to enhancement or vice versa.

printed oxide devices, as the athermal defect passivation or activation of TFT can be done on the go using inkjet printer using on-demand surface treatment **Figure 7-2**. This will also help in roll to roll processing of flexible devices which would be helpful in scalability and faster post-processing.

4. Detailed investigation of surface treatments in order to further fine-tuning of the properties of oxide semiconductor:

The dipole produced by SAMs will be influenced by the type of chain present (the number of fluorine atoms) and the length of the chain. This should further improve the threshold voltage modulation control. Other important factors that affect the dipole moment, such as the SAMs tilt angle and distance from the surface should also be studied {Governed mainly by the following equation: Dipole moment (M)= charging density (q)* distance between dipole(d)}. It is also possible to study in detail the impact of charge transfer happening at the moment of SAM binding with the surface, as it can also contribute to net available charge carriers and modulation of shallow traps. SAMs with similar binding chemistry with distinct dipoles and vice versa can be researched to distinguish these processes from each other. Many n-type and p-type dopants can also be studied, such as viologens that can also be used to modulate the concentration of the charge carrier.

5. Exploration of the surface modification and oxygen vacancies modulation techniques for other applications

The concepts for precise carrier concentration using oxidation control and manipulating vacancy concentration/ distribution to induce differences between bulk and surface electronic structure are novel. This approach can be explored for various applications, such as RRAM, Photoelectrochemical processes such as water splitting, ETL/HTL in Solar cell and LED, etc. Some of them are discussed below:

a. RRAM

In contrast to approaches where the modification is done during the synthesis process, approaches that modify the energy levels during the operation of the device itself would prove much more useful for novel applications such as neuromorphic synapse. This could involve a real-time adjustment of the threshold voltage/ mobility/ off-currents of a transistor, or the magnitude of the high resistance/ low resistance state as well as the switching voltages in a memristor. This would essentially allow the circuit to learn and adapt more closely to the input parameters to reach a more efficient solution. For this approach oxygen vacancy modulation using predefined nanostructures using a combination of Ellingham diagram and deposition methods like ALD can be used to generate oxygen vacancies reservoir in the device thickness which can be probed depending on the voltage applied. Apart from this ionic liquid gating can be used, in which , the addition of small size reactive ions like proton and hydroxyl ion will allow these ions to move across the ionic liquid helmholtz layer thus creating a proton memory behavior due to the reversible intercalation and removal of the protons as noticed in some of the TFT devices.[4] The oxygen vacancy generation effect of ionic liquids could be exploited here to generate oxygen vacancy in a gating like configuration. Such oxygen vacancy gating control would allow for switching between different device characteristics.

b. Photoelectrochemical processes:

Solar energy to drive the photoelectrochemical reaction for water cleavage into the molecular hydrogen and oxygen is of interest due to the possibility of direct generation of energy-rich fuels. However, after decades of research, efficient overall water splitting driven by a single photoelectrode has remained elusive due to stringent electronic and thermodynamic property requirements. Electronic modification of the surfaces of the oxide semiconductors through local doping/surface transformation methodologies can be investigated. Utilizing the oxidizing and reducing treatments, the dangling bonds at the semiconductor interface may be precisely controlled such that their performance in water splitting can be carefully monitored. Oxygen vacancies may play a decisive role by acting

as catalytic sites where the photoelectrochemical processes may occur, however an excess number could also affect the surface recombination processes. Hence control over oxygen vacancies is needed. Passivation of surface defects and reduction of charge recombination at electrode\electrolyte interface would be beneficial and worthwhile to explore for the photoelectrochemical process along with controlled and precise doping to improve conductivity and facilitate better charge transport. By carefully combining the ability of solution growth processes to grow nanostructures with various surface treatments, doped nanostructures/ films can be built up for improved charge transport.

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Appendix

A.1 Masks used:

1. Hard shadow Mask 1:

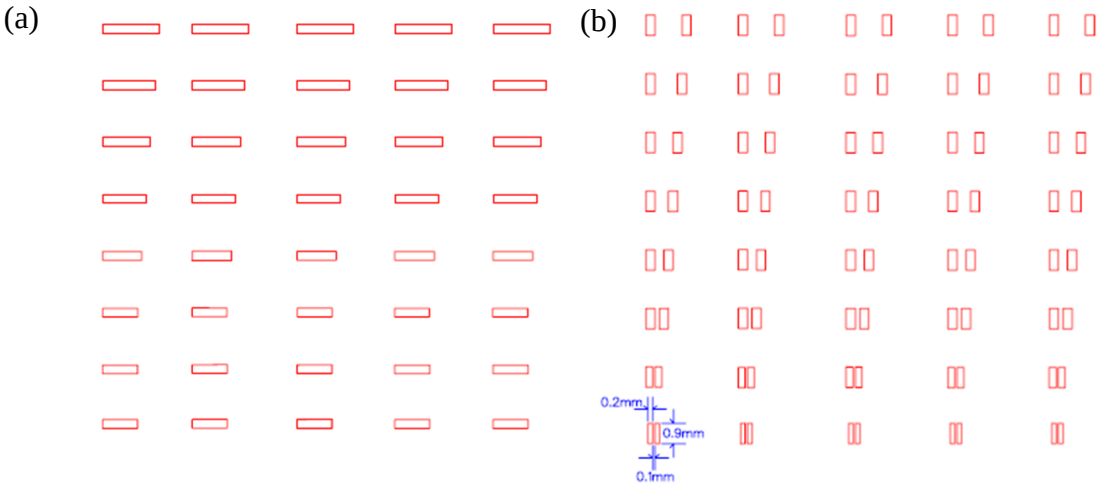

Figure A-1: (a) For Channel (b) for source drain electrodes.

2. Hard shadow Mask 2 for TFT:

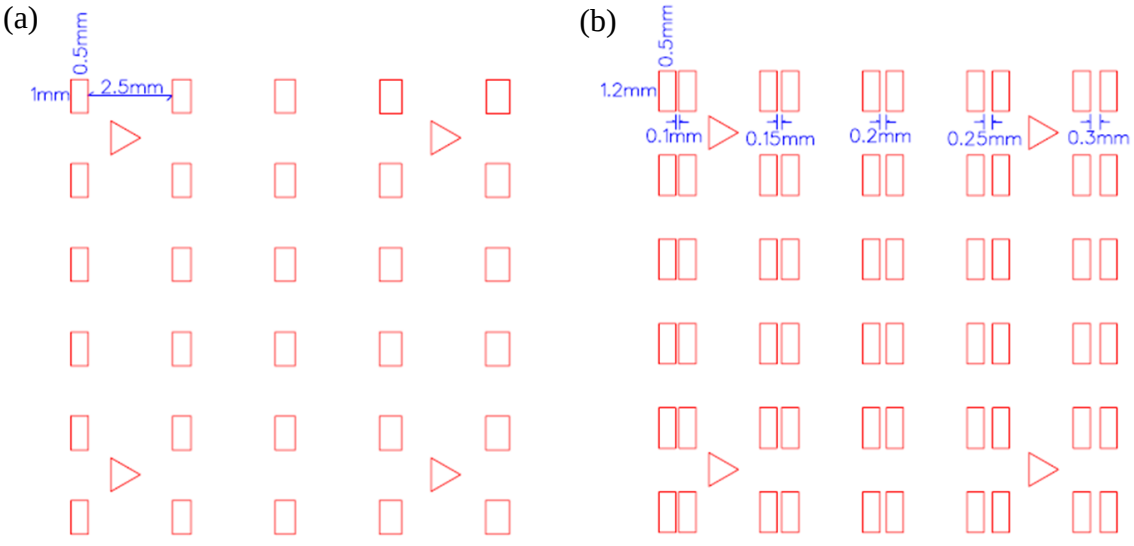

Figure A-2: (a) For Channel (b) for source drain electrodes.

3. Hard shadow Mask 3 for inverter and oscillator:

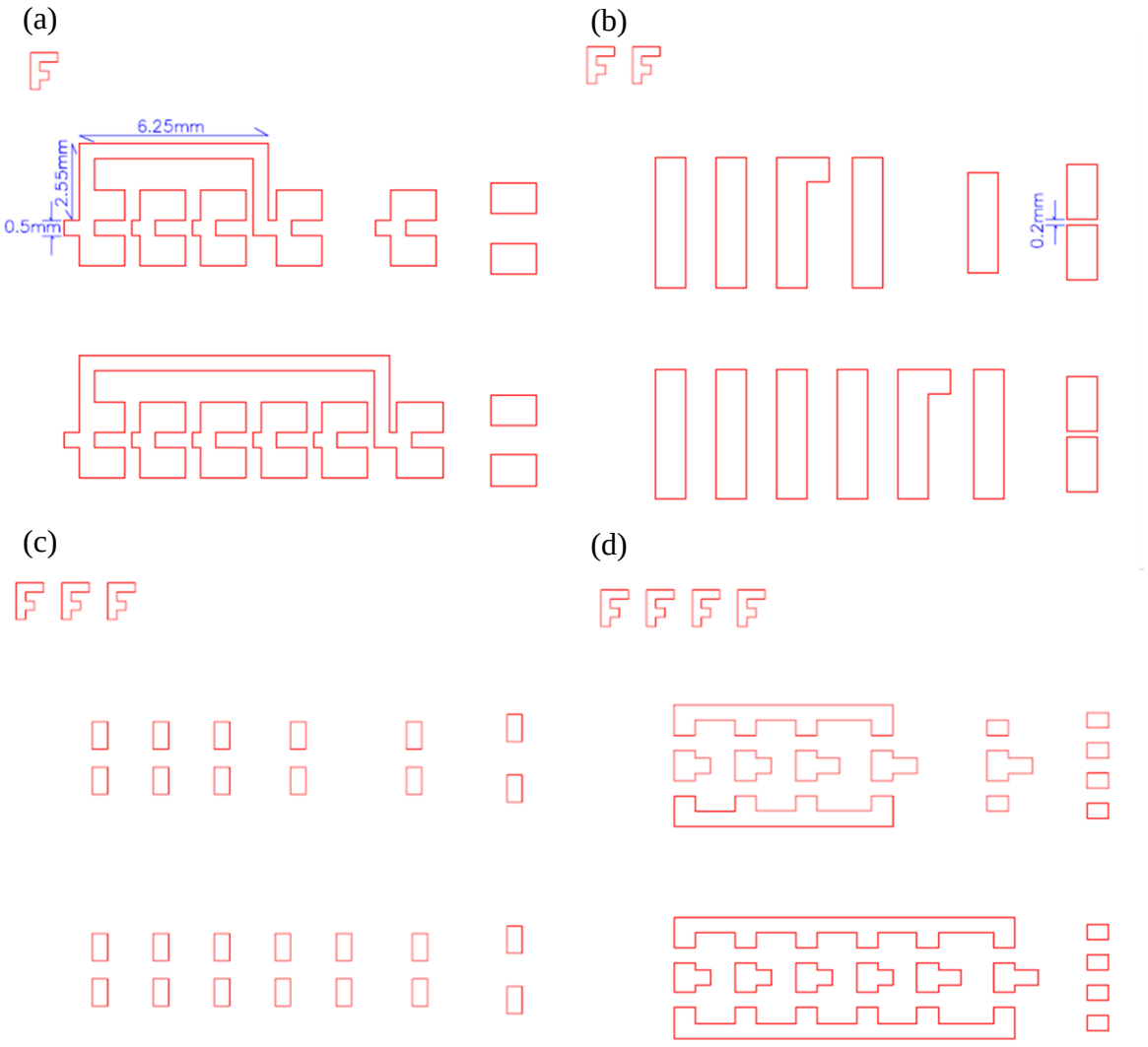

Figure A-3: (a) For Gate electrode (b) for Gate dielectric (c) for Channel (b) for source drain electrodes.

A.2 Appendix for Chapter 4

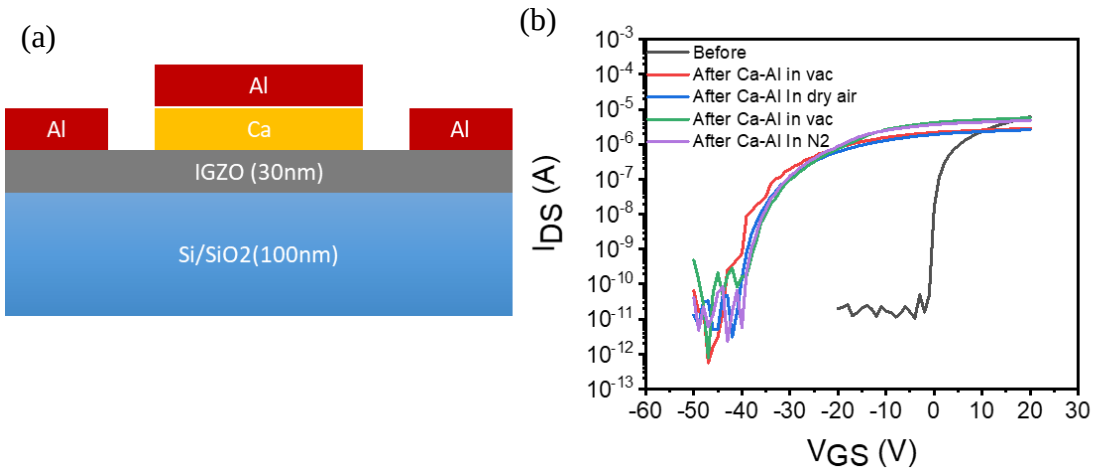

Figure A-4: (a) Structure of IGZO (b) Calcium layer deposition as capping layer on IGZO channel and effect of atmosphere. W=1000 µm, L=250 µm, V_{DS}= 1V.

Calcium layer deposition as capping layer on IGZO channel and effect of the atmosphere

Table A-1: Effect of Ca overlayer

Parameter	Before	After Ca-Al in vacuum	In dry air	After Ca-Al in vacuum	In N_2 gas
Linear slope	2.15E-07	7.98E-08	6.61E-08	2.05E-07	1.61E-07
Mobility	17.4	64.4	53.3	165	130
V_{th} (V)	0.7	-29.84	-29.28	-22.68	-25.56

A.3 Appendix for Chapter 5

A.3.1 TPPO treatment

N-type doping using triphenylphosphine oxide molecule

The Preparation of TPPO deposition was done by dipping IWO-TFT into freshly prepared TPPO solution (50hrs immersed in 1mg/ml in acetonitrile and washed with Chlorobenzene). The TPPO molecule bonds with oxide using the oxygen connected to P with a double bond. XPS was done to crosscheck the film formation.

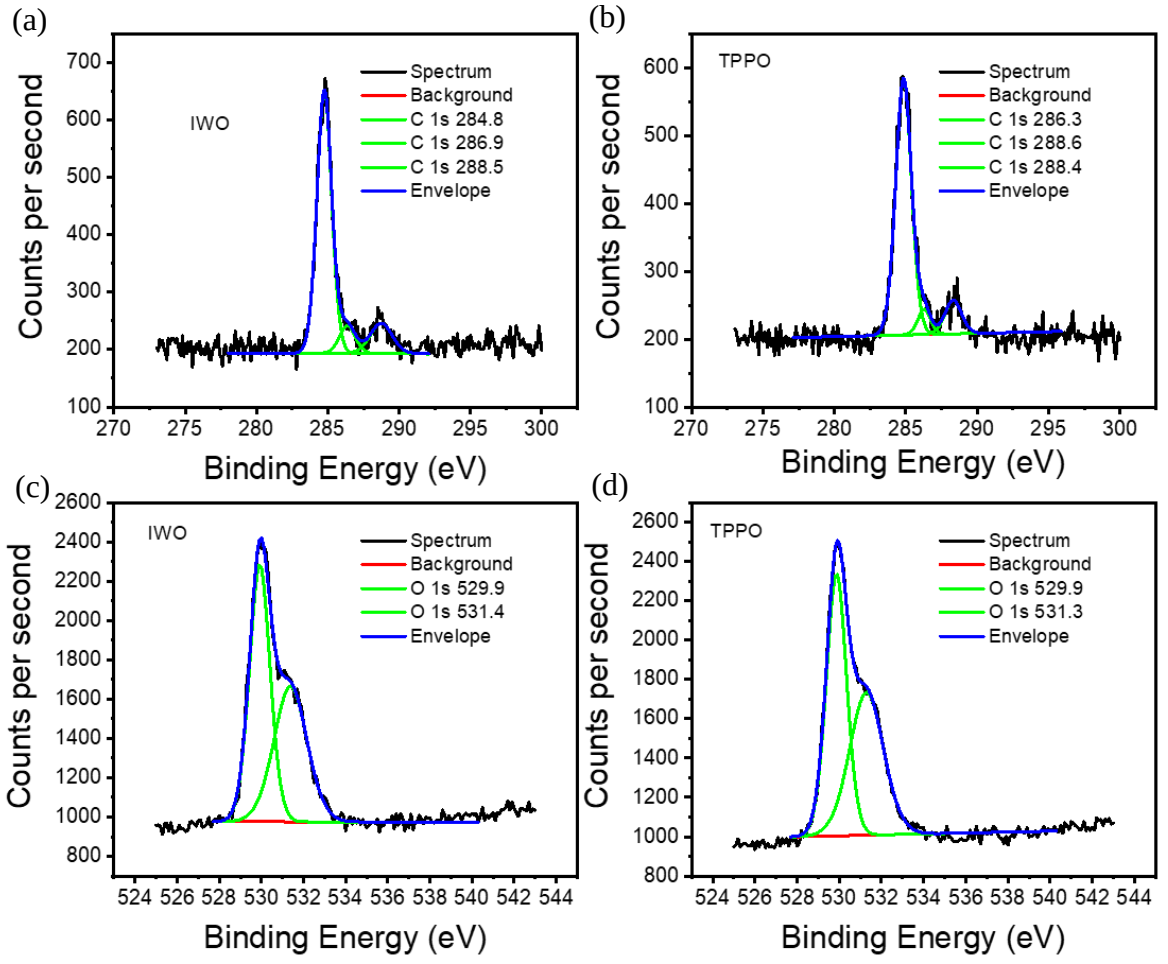

Figure A-5: (a) C1s peak for IWO (b) C1s peak after TPPO treatment (c) O1s peak without TPPO treatment (d) O1s peak with the TPPO treatment.

Furthermore, XPS was performed to confirm the existence of TPPO on the IWO film

(**Figure A-5**). A P 2p peak should give direct evidence of the presence of TPPO molecule on the film. However, the experiment showed that it is challenging to detect the phosphorus through the available XPS instrument. Apart from that, the C1s and O1s peaks also measured, but the variation among them was negligible; therefore, nothing could be concluded from XPS due to the instrument limitation. Hence, it can also be concluded that TPPO treatment did not provide positive results. It can safely be concluded that TPPO did not adsorbed properly to the surface.

Figure A-6 a depicts the transfer characteristics of IWO TFT after TPPO coating. The devices were measured immediately after TPPO coating and ten days after coating. The mobility and threshold voltage variations are shown in **Figure A-6** b. It was expected to get negative threshold voltage shift due to TPPO n-type doping through the electron transfer from the R3P+□O−σ-bond.[1] The threshold voltage shift indeed occurred; however, the mobility was surprisingly suppressed as well. The measurement after ten days shows improvement in mobility and an increase in threshold voltage. This suggests that the effect of TPPO was degraded inside the glovebox.

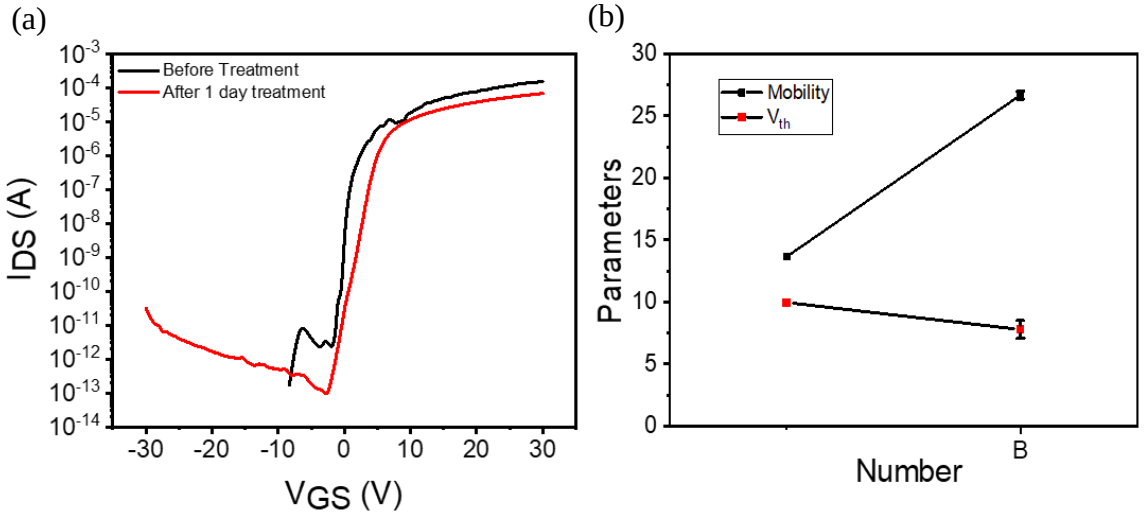

Figure A-6: A is before treatment, B is immediately after TPPO treatment, (a) Transfer characteristics of TFT before and after TPPO treatment (b) Mobility and threshold voltage before and after treatment. W=1000 µm, L=250 µm, V_{DS}= 1V.

To confirm that the modification indeed changes the electrical properties of the semiconductor, a UPS was performed. **Figure A-7** displays the obtained UPS results,

which can be used to calculate the work function and the ionization potential of IWO. The energy of He(I) used for measurement is 21.2 eV. The HOMO energy level of IWO shifted from 2.8 eV to 3.04 eV, and the secondary electron cut off energy shifted from 16.6 eV to 16.97 eV for TPPO treated samples. The calculated work function was modified from 4.61 to 4.23 eV, and ionization potential (VBM) changed from 7.40 to 7.27 for TPPO coated IWO film. **Table A-2** summarizes the changes after the treatment.

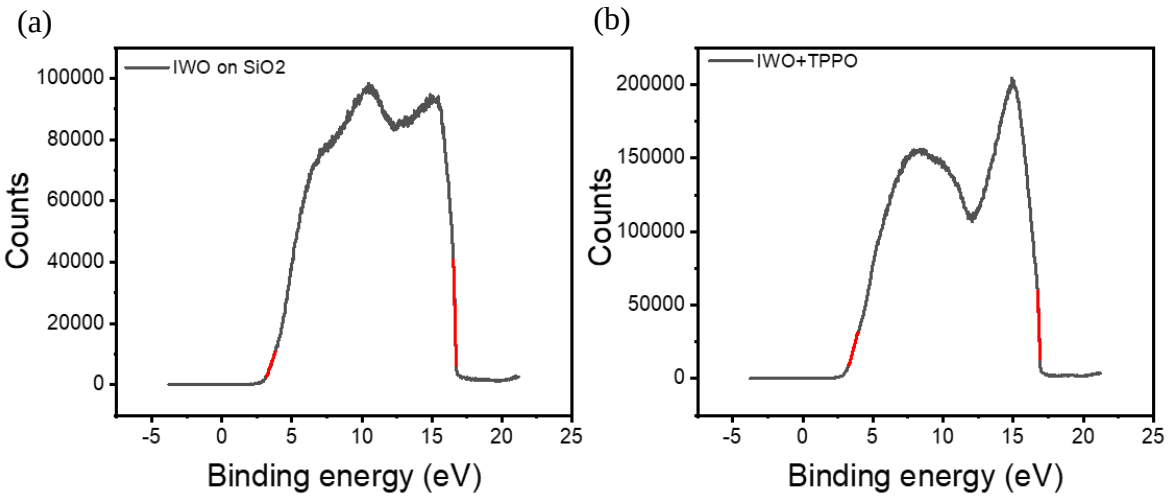

Figure A-7: UPS before (a) and after (b) TPPO treatment.

Table A-2: Work function and ionization potential derived from UPS

	Energy of He	**E_{homo}**	**E_{seco} (Secondary electron cut off energy)**	**Work function**	**Ionization potential**
	B	C	D	B-D	B-D+C
IWO	21.2	2.8	16. 6	4.61	7.4
TPPO	21.2	3.04	16.97	4.23	7.27

From these results for TPPO, it can be concluded that the TPPO treatment needs more study and optimization in order to dope the oxide semiconductor in order to change the attributes of TFT effectively.

A.3.2 H_2O_2 wet chemical oxidation of oxide films

The IZO TFT on P-type Silicon wafer with 300 nm thick SiO_2 substrate was prepared as follows:

Substrates were cleaned by the same process described in the experimental methodology section. Films were prepared by spin coating solutions at 3000 rpm for 1 min. Spin coated samples were baked at 110 ^oC for 5 min in order to remove excess solvent. The obtained films were subjected to deep-ultraviolet (DUV) irradiation for 15 min. [2] IZO solutions were prepared by dissolving indium nitrate hydrate ($In(NO_3)_3 \cdot xH_2O$) and zinc nitrate hydrate ($Zn(NO_3)_3 \cdot xH_2O$) salts in 2-methoxyethanol. The total cation concentration was kept constant at 0.2 M, and the In:Zn ratio was kept constant at 7:3 for IZO in this study. The solutions were stirred for 12 h to allow complete dissolution.

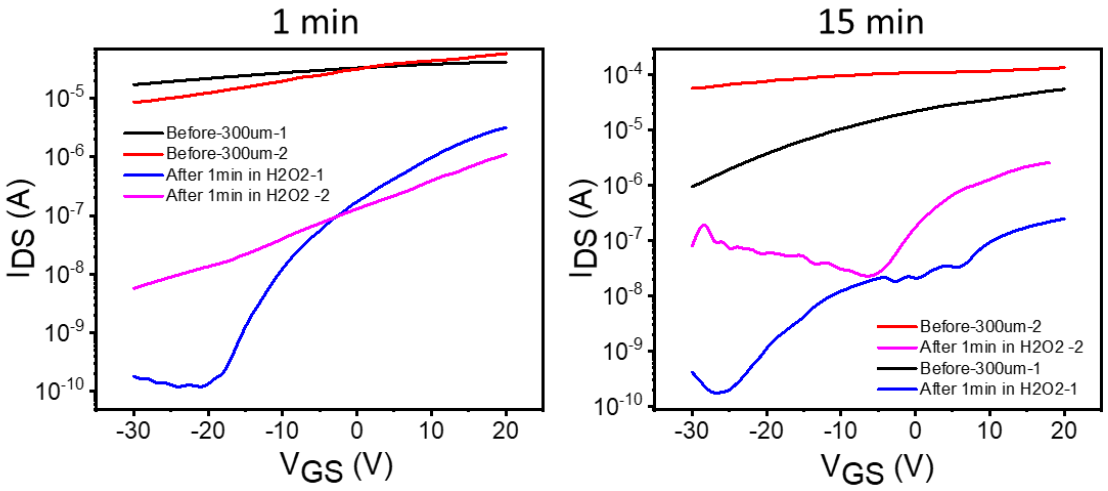

Figure A-8: Transfer characteristics of IZO solution processed TFT with ITO electrode with and without treatment (a) H_2O_2 treatment for 1 min, and (b) 15 min treated sample. (red and black are before treatment and pink and blue are after treatment).

From **Figure A-8** It can be seen that the H_2O_2 treatment works and decreases the charge carriers in the film bringing the threshold voltage to a smaller value.

A.4 Appendix for Chapter 6

Figure A-9 a and b show AFM images of the thin film before and after annealing IWO film. The roughness (Rrms value) without annealing and 200 ^{o}C annealing is 0.5 nm and 0.46 nm, respectively. This shows that the temperature improves the morphological characteristics of the film. **Figure A-9** c display XRD measurement of 50 nm thick films, and it can be noted that the films are amorphous.

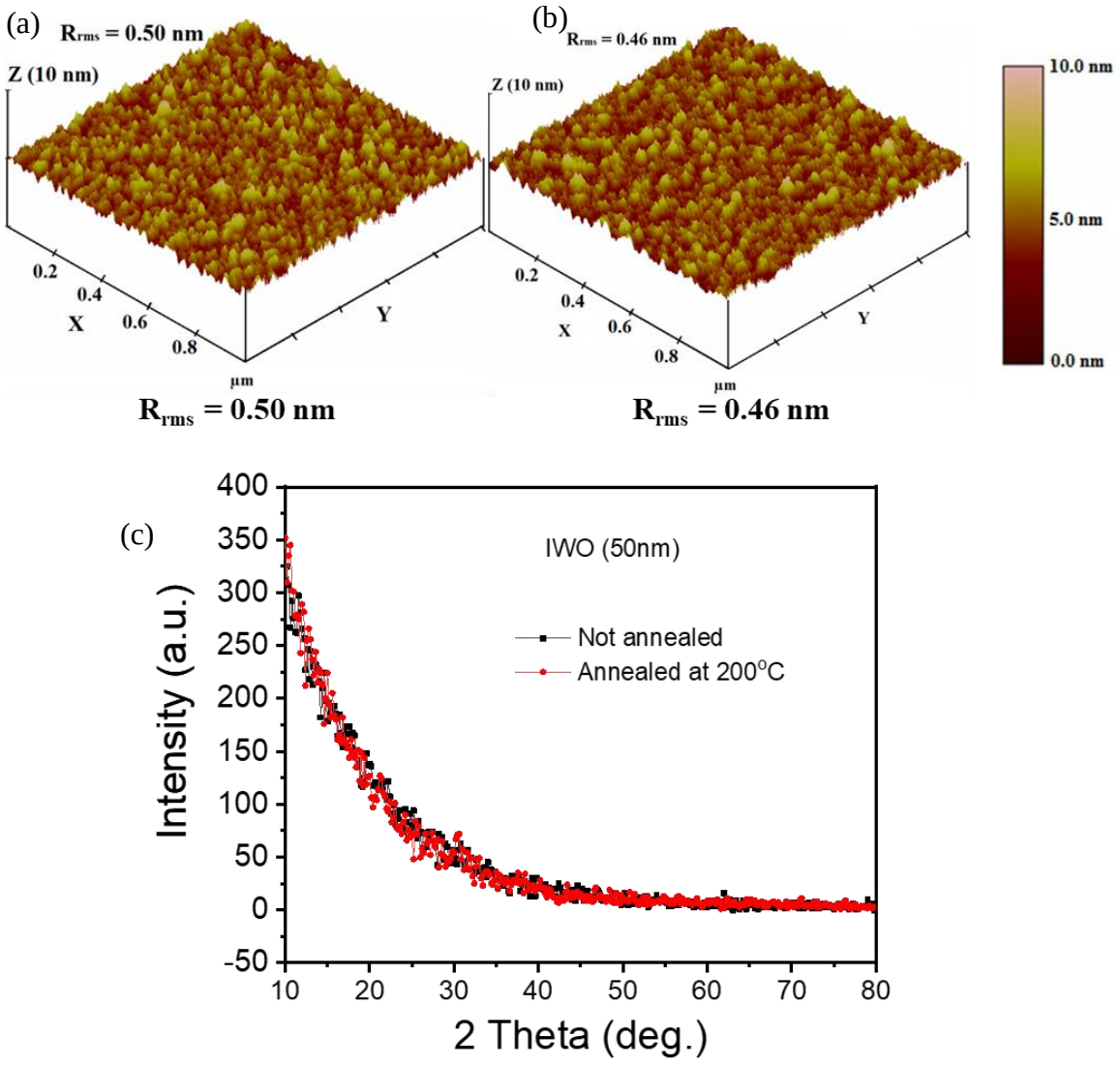

Figure A-9: 3D AFM images of IWO thin film (a) before and (b) after annealing at 200°C. (c) XRD spectra of IWO (50 nm) thin film deposited on SiO_2.

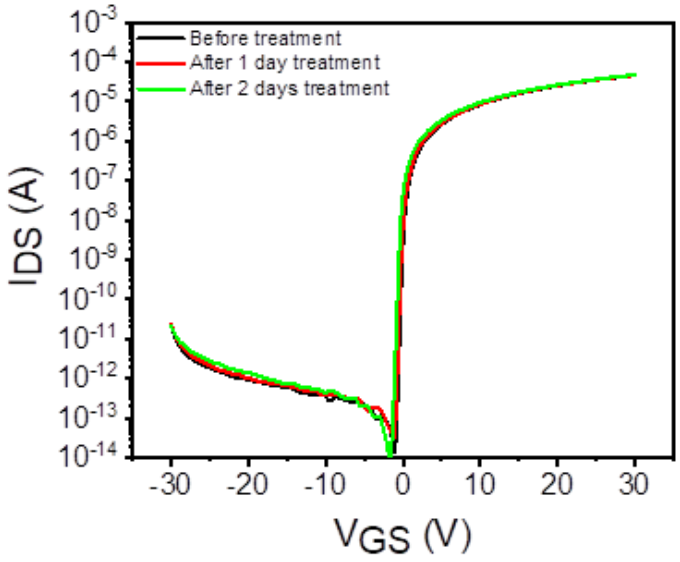

Figure A-10: Effect of dipping in ethanol solvent used for SAM treatment on the TFT transfer characteristics.

References

1. Tu, B. *et al.* Novel Molecular Doping Mechanism for n-Doping of SnO 2 via Triphenylphosphine Oxide and Its Effect on Perovskite Solar Cells. **1805944**, 1–9 (2019).
2. John, R. A. *et al.* Low-Temperature Chemical Transformations for High-Performance Solution-Processed Oxide Transistors. *Chem. Mater.* **28**, 8305–8313 (2016).