

# An Adaptive Beamforming Technique for UWB Impulse Transceiver

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**Abstract**—A two-channel beamforming ultra-wideband (UWB) impulse transceiver chip, which includes a beam steering TX controlled by a fractional delay locked loop and an adaptive RX that can self-tune the beamforming to the direction of incident pulses, is presented. The dual-channel timed array transmitter can generate UWB pulses in two separate transmitter paths with tunable path delay difference of 0~250 ps to achieve beam-steering capability. Each beamforming receiver channel has a measured continuous time delay between 0~250 ps. The proposed beamformer could provide maximum scan angle of up to  $\pm 60^\circ$  for two antennas with about 8-cm spacing. Fabricated in 0.18- $\mu\text{m}$  CMOS, the TX can beam steer across the full spatial range with resolution of  $4^\circ$ , and the RX can continuously scan the full range with resolution of  $3^\circ$ . The transmitter consumes 37 mA at 10 Mbps and receiver consumes 84 mA under 1.8-V power supply.

**Index Terms**—Beamforming, CMOS, impulse radio, pulse generator, receiver ultra, transmitter, ultra-wideband (UWB).

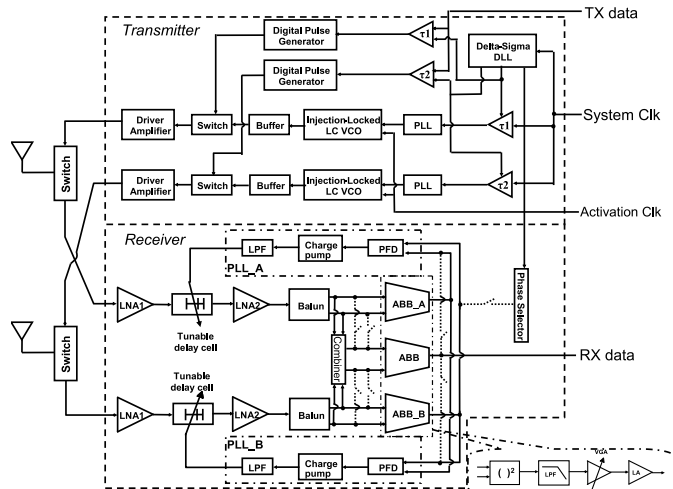


Fig. 1. Beam-forming UWB transceiver architecture.

## I. INTRODUCTION

UWB HAS been recognized as a promising radio technology for short-range wireless applications such as WPAN, WSN, and WBAN [1]–[3], [9]. Since UWB occupies a large bandwidth, it can achieve high data rates. However, the inherent problem of UWB is its limited range owing to low power transmission, multipath effects and interference. In order to overcome these problems, beamforming and beam steering techniques are employed in the UWB transceiver. These techniques enhance the reception of weak signals and increases the system immunity to jamming. Beamforming technique has been used in narrow band systems such as 802.11n WLAN to achieve higher data rate, strong interference rejection and range extension [4], [5]. Antenna array UWB receivers have been reported such as coherent combing of UWB pulses [6] and a  $2 \times 2$  dual-antenna transceiver for WiMedia UWB [7]. A beam-forming transmitter with fine resolution of  $1^\circ$  has been reported in [8].

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In this brief, we propose an adaptive beamforming technique for UWB transceiver, which includes a beam steering TX controlled by a fractional delay locked loop (FDLL) and an adaptive RX that can self-tune the beamforming. It can achieve high sensitivity for range extension without lowering the data rate. Based on the proposed phase detector (PLL\_A and PLL\_B in Fig. 1) in receiver, it could be beam-formed to desired angle adaptively and automatically without further digital processing. The brief is organized as follows. The UWB transceiver system architecture is described in Section II. The circuit implementation details of transmitter and receiver are given in Section III. The experimental results are reported in Section IV. Finally, the conclusion is drawn in Section V.

## II. SYSTEM ARCHITECTURE

The system architecture is briefly described as the following. First, a dual-channel IR-UWB timed array transmitter with beamforming capability is presented [15]. The proposed architecture utilizes injection-locking mechanism to achieve an accurate center frequency. Voltage controlled continuous true time delay (TTD) [15] is incorporated between the two channels to achieve fine time step resolution. Secondly, a fully integrated two-channel 3-5 GHz carrier-based IR-UWB beamforming receiver with adaptive angle tuning is proposed. High impedance artificial transmission line (ATL) is optimized [16] to provide maximum time delay and also acts as the matching network for the switch amplifier to minimize the cascaded loss.

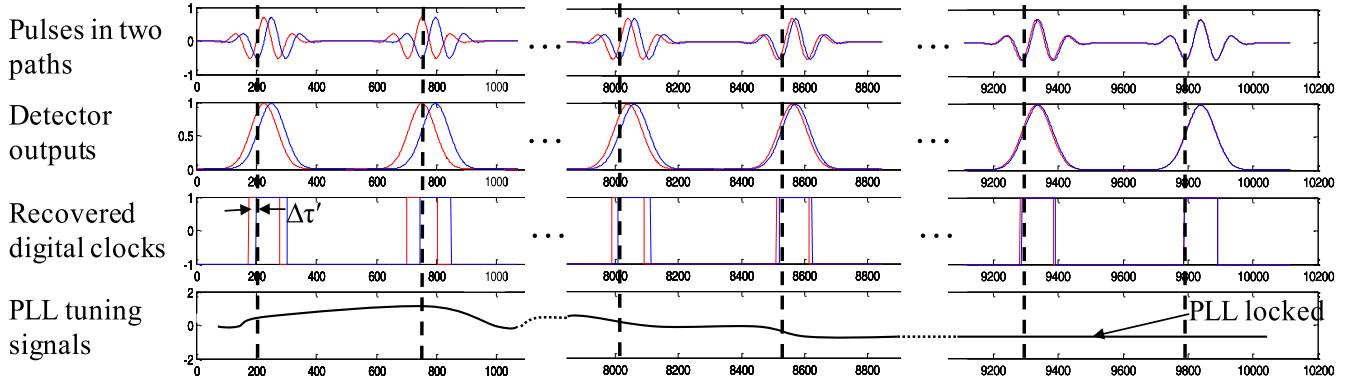


Fig. 2. Adaptive delay tuning for beam-forming.

Moreover, phase detector is adopted in each channel to monitor the phase difference and feedback to the front-end tunable delay cell accordingly. Finally, the FDLL is proposed to accurately control the TTD in transmitter paths and achieves fine time step resolution. In addition, the true time delay generated by this FDLL is used for offline calibration of the receiver to achieve fixed beamforming capability.

Fig. 1 shows the two-channel beamforming UWB impulse transceiver architecture. The transmitter generates two UWB pulses with a tunable delay difference for beam steering. A FDLL (delta-sigma DLL) is used to regulate two delay cells with delays of  $\tau_1$  and  $\tau_2$  respectively, using the 100 MHz reference clock. They are then applied to the reference clocks of the two PLLs to produce two 800 MHz injection signals. Two 4 GHz carriers with delay difference  $\tau = \tau_2 - \tau_1$  are then created through injection locked LC VCOs (IL-LCVCO). In addition, the clock signals with delays  $\tau_1$  and  $\tau_2$  trigger two pulse generators to output two short pulses with same delay difference  $\tau$ . They modulate the two carriers to create two UWB pulses with controllable true time shift  $\tau$ , which are then amplified by two driver amplifiers (DA) before going to the two antennas. The receiver has two independent receiving paths and a combination path. For each receiving channel, it consists of a RF front-end (RFFE) and an analog baseband (ABB\_A/ABB\_B). Each RFFE in the receiver path includes two LNAs separated by a tunable delay cell and a balun. In the combination path, ABB receives the combined signals of the two delay shifted UWB pulses. The ABB consists of a squarer, a VGA and a limiting amplifier to cater for both OOK and PPM signal demodulation. The two received pulses are shifted to the same phase through the delay cell to obtain coherent addition, which achieves diversity gain that can improve the receiver sensitivity. Conventionally, the amount of relative delay (phase) shift is chosen manually to obtain beam-forming. In this brief, a novel adaptive delay tuning scheme using PLLs with two operation modes is proposed, i.e., online tuning and offline calibration. For the online tuning (solid line), the control of the pulse delay is adaptively tuned throughout the receiving process. The recovered digital outputs from ABB\_A/ABB\_B are sent to PLL\_A/PLL\_B for phase comparison. Through the feedback loop, the PLL LPF outputs will adjust both the delay cells to eventually phase align the two incoming pulses, and achieve

locking. For the offline calibration (dotted line), one clock with desired delay is selected from the multiphase outputs of the FDLL and compared with the recovered digital output from path A (B) through ABB\_A (ABB\_B) and PLL\_A (PLL\_B). Once locked, the LPF outputs can be retained through DSP interface to achieve the desired delay (one way is to use an additional DAC to memorize the analog control voltage of the tunable delay cell). The proposed receiver can adaptively beam-form to the direction of incoming pulses, with the offline method provides additional fixed beam-forming capability.

The proposed receiver can tune the delays of received UWB pulses in the two paths adaptively through a PLL until constructive combination is achieved. Referring Fig. 2, assume the received two path pulses are

$$S_{d1}(t) = Ae^{-((t-\tau_1)/\Delta T)^2} \cos(\omega t + \varphi_1 - \omega\tau_1) \quad (1)$$

and

$$S_{d2}(t) = Ae^{-((t-\tau_2)/\Delta T)^2} \cos(\omega t + \varphi_2 - \omega\tau_2). \quad (2)$$

After the detectors (squarer and LPF), the delayed envelopes  $Ke^{-2((t-\tau_1)/\Delta T)^2}$  and  $Ke^{-2((t-\tau_2)/\Delta T)^2}$  are extracted, where  $K$  is the magnitude of envelopes.  $\Delta_\varphi = \varphi_2 - \varphi_1$  indicates the system delay mismatch from transmitter. Using matched limiting amplifiers with same threshold, the reconstructed digital signals have proportional linear delay of  $m + l\tau_1$  and  $m + l\tau_2$ , where  $m$  and  $l$  are the offset and gain coefficients of the delay, respectively. The relative delay  $\Delta\tau' = l(\tau_2 - \tau_1)$  is then employed to generate the tuning signals (through PLLs) to tune the UWB pulse delays until  $\Delta\tau' - > 0$ , i.e., the two pulses are in-phase aligned. Once locked, the combination of the two pulses equivalently generates a beam-forming to the original angle

$$\theta = \sin^{-1}\left(|\tau_1 - \tau_2| \frac{c}{d}\right), \quad (3)$$

where  $d$  is the spacing of the two antennas. Conventionally, the amount of relative phase shift is chosen manually in discrete steps to obtain beam-forming with limited beam-forming range and resolution. Compared to conventional methods, the proposed method achieves significant performance, because the path delay is adaptively tuned and changed continuously. The beam-forming resolution is only limited by the jitter of the PLL.

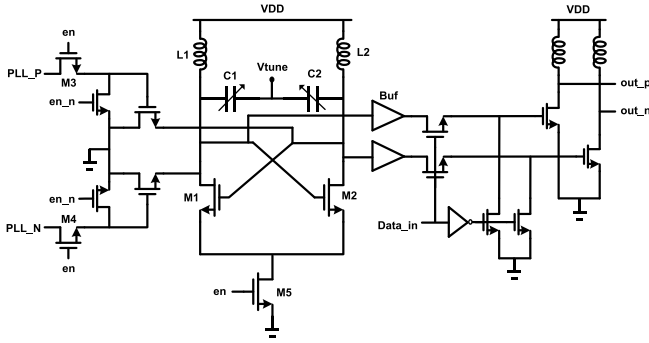


Fig. 3. The schematic of a single channel transmitter circuits.

### III. TRX CIRCUITS AND SYSTEMS

The single-channel transmitter circuits are shown in Fig. 3. During “on” time, the transmitter consumes 37 mA. In the schematic of Injection locked (IL)-LCVCO, the window pulse ‘en’ and its inverted signal ‘en\_n’ are used to activated the oscillator [15]. The IL-LCVCO consists of NMOS cross-coupled pair (M1, M2), PLL output gating switches (M3, M4), LC Tank (L1, L2, C1 and C2) and tail current transistor M5. The IL-LCVCO locks to the 5th harmonic of the 800 MHz from PLL differential outputs. The reference clock is set to be 100 MHz to generate 800 MHz PLL output. This reference frequency is also chosen to be the digital baseband frequency.

A dual loop DLL is shown in Fig. 4. It generates 0~250 ps relative time delay with around 8 ps tuning resolution. The two loop duplicate the same blocks except the reference DLL takes the last output of the delay line (P10) as the feedback clock, while the tuning FDLL uses a Delta-Sigma modulator to control the multiplexer and select the feedback clock among (P7-P11).  $\Delta\Sigma$  DLL with pico-second delay tuning and good jitter performance has been reported in [12]. Both DLLs will finally lock with the control voltage V1 and V2, which correspond to the time delay as desired. The reference delay is  $\tau_1 = T/10$  with  $T = 10$  ns. Employing a 2<sup>nd</sup> order delta-sigma modulator, a 7-bit code (*mod\_in*) and the control signal (*mod\_ctrl*) determine the probability of the 5-bit selection, and this reflects a fractional amount of delay cells, from 8 to 10, and hence generates a tunable time delay as  $\tau_2 = T/(10 - S_{ctl} - i/128)$ , where  $i$  is the integer representation of *mod\_in* ( $i = 0, 1, \dots, 127$ ) and  $S_{ctl}$  represents *mod\_ctrl* ( $S_{ctl} = 0, 1$ ). The delay cell consist of differential NMOS input pair (M1, M2), resistive loading which are represented by using M3, M4 in linear region and M5, M6 in saturation region. Replica bias is employed to provide the control voltage  $V_p$  and the current bias  $V_b$  for the delay cells. The main structure is two duplicated circuits of half the delay cell. A differential op-amp keeps tracking  $V_p$  to the input control voltage  $V_{ctrl}$  through a negative feedback. The phase detector of DLL is improved to overcome the limitation of initial phase condition and false locking problem. It takes three control signals: START, OVER and UNDER. The START signal ensures the phase comparison begins within one clock period. The OVER and UNDER signals come from the lock detector and enable the phase detector only when the delay between the reference clock and the feedback clock is within  $0.5T \sim 1.5T$ . The outputs are UP and DOWN, indicating the leading or

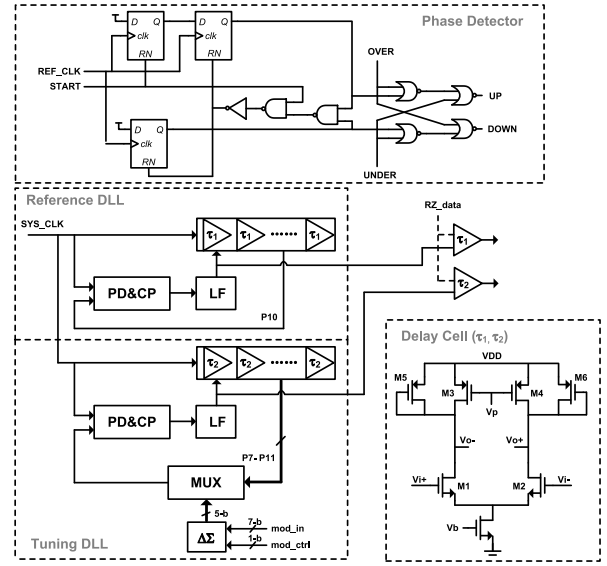


Fig. 4. Schematic of the FDLL.

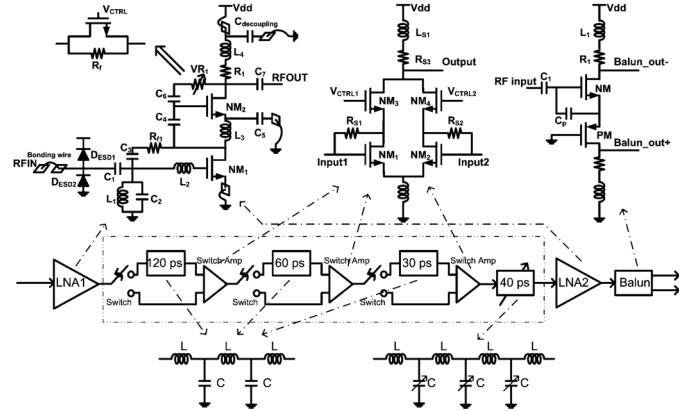


Fig. 5. Receiver RF front-end circuits.

lagging phase relationship. The 2<sup>nd</sup> order delta-sigma modulator is designed and synthesized. A 7-bit code (*mod\_in*) and the control signal (*mod\_ctrl*) determine the probability of the 5-bit selection, and this reflects a fractional amount of delay cells, from 8 to 10, and hence generates a tunable time delay as  $\tau_2 = T/(10 - S_{ctl} - i/128)$ , where  $i$  is the integer representation of *mod\_in* ( $i = 0, 1, \dots, 127$ ) and  $S_{ctl}$  represents *mod\_ctrl* ( $S_{ctl} = 0, 1$ ). The delay cell consist of differential NMOS input pair (M1, M2), resistive loading which are represented by using M3, M4 in linear region and M5, M6 in saturation region. Replica bias is employed to provide the control voltage  $V_p$  and the current bias  $V_b$  for the delay cells. The main structure is two duplicated circuits of half the delay cell. A differential op-amp keeps tracking  $V_p$  to the input control voltage  $V_{ctrl}$  through a negative feedback. The phase detector of DLL is improved to overcome the limitation of initial phase condition and false locking problem. It takes three control signals: START, OVER and UNDER. The START signal ensures the phase comparison begins within one clock period. The OVER and UNDER signals come from the lock detector and enable the phase detector only when the delay between the reference clock and the feedback clock is within  $0.5T \sim 1.5T$ . The outputs are UP and DOWN, indicating the leading or

The single-channel RX front-end circuits are shown in Fig. 5 [16]. The 3-5 GHz two-stage current-reuse LNA includes LC input matching networks with high/low gain mode. The tunable delay cell consists of three fixed delay stages (120 ps, 60 ps, 30 ps), and a continuous tunable delay stage (0-40 ps), which employs 2-stage and 3-stage cascaded LC transmission line. Switch amplifier is used to toggle between paths and compensates the loss of the passive delay cell. The active current sharing balun minimizes the power consumption. The 3-5 GHz variable gain LNA is a three-stage cascaded resistive feedback amplifier. A switch amplifier is designed to provide path switching and insertion loss compensation. The delay cell is included as part of the amplifier input matching circuit to facilitate the impedance matching with previous stages.

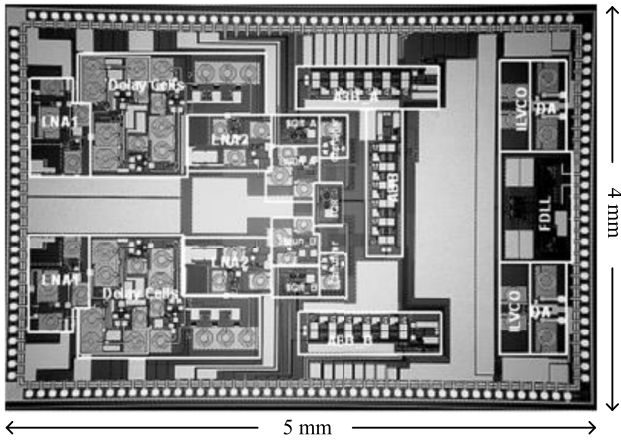


Fig. 6. TRX chip microphotography.

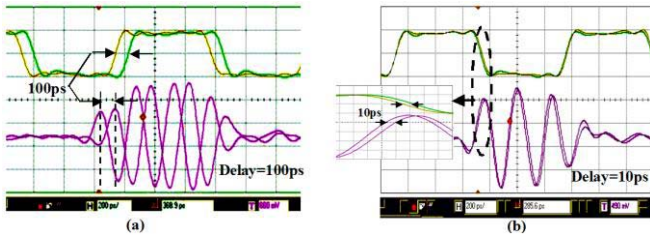


Fig. 7. Injection locking performances at delay of (a) 100 ps and (b) 10 ps: UWB pulse delay versus input clock delay.

#### IV. EXPERIMENT RESULTS

The transceiver is integrated on standard 0.18- $\mu\text{m}$  CMOS technology. The chip shown in Fig. 6 occupies an area of 4 mm  $\times$  5 mm. The chip is housed in a QFN132 package and mounted on a Rogers Printed Circuit Board (PCB) and tested. For the purpose of beam steering in transmitters, the delay between two UWB pulses at ILVCO's output should be equal to the delay between two 800 MHz clocks at ILVCO's input (and the delay between two 800 MHz clocks is controlled by the FDLL). The measured ILVCO performance is shown in Fig. 7. With 10 Mbps baseband input data, the generated UWB pulse occupies 2 GHz bandwidth (measured at  $-10$  dB cut-off). As illustrated in the figure, the transmitted pulses exhibit pulse width of 1 ns and peak swing of 2V with 50  $\Omega$  load. The path delay difference can vary between 0~250 ps. The spectrum centered at 4 GHz and meets the FCC mask requirement except for the lower frequency portion. However, this should be easily suppressed by the external band-pass filter or antenna. Fig. 8 shows the beamforming measurement setup. Before the beam steering pattern testing, the system mismatch caused delay between two channels is measured and compensated through post-processing. A measured transmitter beam steering pattern, with 0 degree ( $\tau_1 - \tau_2 = 0$  ps) and 30 degree ( $\tau_1 - \tau_2 = 62.5$  ps) angle tuning, is shown in Fig. 9. Fig. 10 (a) shows the measured S11 and S21 of the combined LNA/TTD block. Over the 3-5 GHz range, the measured S21 is between 16.5-18.5 dB with  $\pm 1$  dB variation, whereas the measured S11 is always below  $-10$  dB. Fig. 10 (b) shows the measured gain and noise figure of LNA1+TTD+LNA2+Balun. Over the 3-5 GHz range, the measured gain is between 14-22 dB, the measured noise

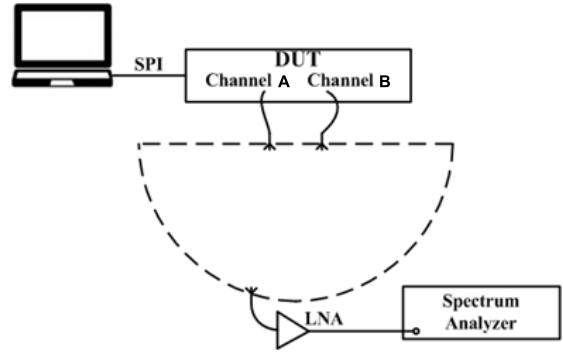


Fig. 8. Measurement set up.

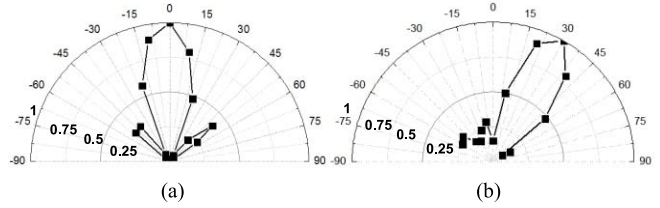


Fig. 9. Beamforming pattern at different angles (a) 0 degree (b) 30 degree.

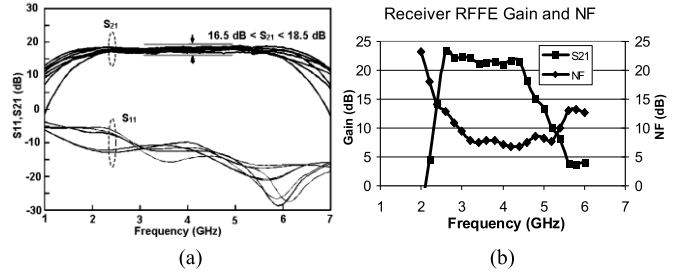


Fig. 10. Measured RF front-end performance: (a) LNA1+TTD S11, S21 in various coarse delay tuning settings, (b) LNA1+TTD+LNA2+Balun.

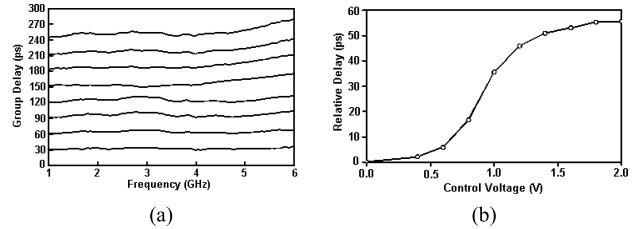


Fig. 11. Measured delay. (a) Coarse delay block delay for various delay settings (b) Fine delay block delay versus varactor control voltage.

figure (NF) is always below 8 dB. The measured group delay of the coarse tuning block for different settings with analog tuning block fixed at 30 ps is illustrated in Fig. 11 (a). The maximum achievable delay is 250 ps in 3-5 GHz band. The measured delay time versus frequency of the continuous analog fine tuning block is shown in Fig. 11(b). The varactor biasing voltage between 0 - 1.0 V is used to cover the full 30 ps delay range continuously. A measured FDLL delayed outputs by different control codes are demonstrated in the Fig. 12. The measured delays (triangles) versus the theoretical calculated delays (lines) match well. The performance summary of the TRX is given in Table I. In addition, the performance

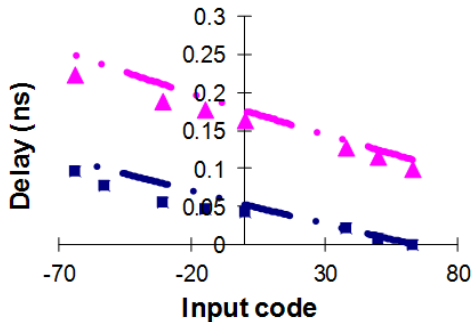


Fig. 12. Measured FDLL performance: delay versus input code.

TABLE I  
TRX PERFORMANCE SUMMARY

Transmitter	Receiver	Overall
Pulse width: 0.5~1ns	Receiver gain: 10-85 dB	VDD: 1.8V
Center freq: 4 GHz	Noise Figure: 8 dB	Technology: 0.18 $\mu$ m CMOS
BW: 1 GHz	Sensitivity: -85 to -91 dBm	FDLL max time delay: 250 ps
Modulation: OOK/PPM	Tunable delay: 0-250 ps	FDLL time delay resolution: <10 ps
3dB beamwidth: 20°	Min True delay resolution: 8 ps	Beamforming gain: 6 dB
Max beam angle: 60°	Max beam angle: 60°	Die Size: 12.45 mm <sup>2</sup>
Beamsteering resolution: < 4°	Beamforming resolution: <3°	
Current consumption: 37 mA	Current consumption: 84 mA	

TABLE II  
PERFORMANCE COMPARISON

Reference	[10]	[11]	[13]	[14]	<b>This work</b>
Technology	0.13 $\mu$ m CMOS	0.13 $\mu$ m CMOS	65nm CMOS	140nm CMOS	<b>0.18<math>\mu</math>m CMOS</b>
TRX	TX only	TRX	RX only	RX only	<b>TRX</b>
Freq (GHz)	4~6	23-29	0.1~10	0.5~3	<b>3 - 5</b>
Antenna spacing (cm)	30	0.6	3	-	<b>8</b>
No. of TX channels	4	4	-	-	<b>2</b>
TX delay res (ps)	180	3	-	-	<b>10</b>
TX max delay (ps)	880	55	-	-	<b>250</b>
TX phase res	10	9	-	-	<b>4</b>
TX power	-	-	-	-	<b>67</b>
No. of RX channels	-	4	4	4	<b>2</b>
RX delay res (ps)	-	-	7	14	<b>8</b>
RX max delay (ps)	-	-	224	550	<b>250</b>
RX phase res	-	-	4	4.6	<b>3</b>
RX adaptive beam-forming	-	No	No	No	<b>Yes</b>
RX Power (mW)	-	68	192	250	<b>151</b>

of the proposed UWB TRX is compared with the state-of-the-art designs as listed in Table II. To our best knowledge, the proposed design is among the first fully integrated UWB beam-forming TRX with adaptive beam-forming receiver.

## V. CONCLUSION

A dual-channel IR-UWB timed array transceiver with FDLL for delay generation and adaptive beamforming is presented in this brief. The chip has been implemented in 0.18- $\mu$ m CMOS process and demonstrated a controllable path delay difference of 0~250 ps between the two channels. The measured results demonstrate a scan range of  $\pm 60^\circ$  can be achieved for a two-element array with 8 cm antenna spacing. The proposed design has been validated and proved to be well suited for IR-UWB phased-array applications.

## ACKNOWLEDGMENT

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