



**ADVANCED GAN HEMT DEVICE MODELING AND
HIGH EFFICIENCY MMWAVE POWER AMPLIFIER
DESIGN FOR BEYOND 5G APPLICATION**

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School of Electrical & Electronic Engineering

2024

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School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2024

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

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Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Zheng Yuanjin

Authorship Attribution Statement

This thesis includes material from two papers currently under review by peer-reviewed journals, one paper in preparation for submission to peer-reviewed journals, and one paper accepted at a conference, all with me as the first author.

Part of Chapter 3 is published as Z. Lu, H. Xie, J. Piao, W. Zhengzhe, N. G. Ing and Y. Zheng, “A Wideband GaN HEMT Modelling with Comprehensive Hybrid Parameter Extraction for 5G Power Amplifiers,” 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5.

The contributions of the co-authors are as follows:

- Prof. Yuanjin Zheng provided essential guidance and direction throughout the research process and revised the manuscript.
- I conducted the research, analyzed the data, and wrote the manuscript, and I coordinated with co-authors, integrated their contributions, and ensured the overall quality and coherence of the paper.
- Hanlin Xie provided the DC testing results and Jiaming Piao helped with the measurement system setup.

The revised version of Chapter 3 is accepted as Z. Lu, H. Li, H. Xie, Y. Zhang, W. Wang, N. G. Ing and Y. Zheng, “A Hybrid GaN HEMT Model Merging Artificial Neural Networks and ASM-HEMT for Parameter Precision and Scalability”, in IEEE Transactions on Electron Devices (2024).

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- Prof. Yuanjin Zheng provided essential guidance and direction throughout the research process and revised the manuscript.
- • I conducted the research, analyzed the data, and wrote the manuscript, and I coordinated with co-authors, integrated their

contributions, and ensured the overall quality and coherence of the paper.

- Hanchao Li and Yihao Zhuang provided the DC testing results.

Chapter 4 is published as T. Guo, Z. Lu, K. Tang, C. Yang, B. Yu and Y. Zheng, “A Floating-Body Transistor-Based Power Amplifier for Sub-6-GHz 5G Applications in SOI CMOS 130-nm Process,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 10, pp. 4088-4092, Oct. 2022.

The contributions of the co-authors are as follows:

- Prof. Yuanjin Zheng provided essential guidance and direction throughout the research process and revised the manuscripts.
- I helped with the layout design, simulation and experiment, and I also helped with the revision of the manuscript.
- Ting Guo designed the circuit and wrote the manuscript.

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The contributions of the co-authors are as follows:

- Prof. Yuanjin Zheng provided essential guidance and direction throughout the research process and revised the manuscripts.
- I conducted the research, analyzed the data, and wrote the manuscript, and I coordinated with co-authors, integrated their contributions, and ensured the overall quality and coherence of the paper.
- Yanshu Guo helped with the layout design of the work.

Chapter 6 is in preparation as Z. Lu, Y. Wang, G. Fan, C. Wan, K. Hong, and Y. Zheng, “An 8-shaped-transformer based power amplifier for D-band FMCW radar application”. IEEE Transactions on Circuits and Systems I:

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The contributions of the co-authors are as follows:

- Prof. Yuanjin Zheng provided essential guidance and direction throughout the research process and revised the manuscripts.
- I conducted the research, analyzed the data, and wrote the manuscript, and I also built the corresponding testing platforms of each block in FMCW radar system.
- Yange Wang was in charge of PLL and VCO design of the radar system, Guanghao Fan was in charge of multiplier and mixer design.
- Cao Wan and Kaidong Hong provided some guidance and experience in using software efficiently like HFSS and Cadence.

01-Aug-2024

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Summary

Advancements in wireless communication demand high-performance components operating at higher frequencies and efficiencies. The evolution from 4G to 5G has significantly improved data rates and user experience. As we move towards B5G and 6G, requirements for communication systems rise, driven by IoT, autonomous vehicles, smart cities, and high-speed internet connectivity. High-frequency, high-power devices, especially power amplifiers (PAs), are crucial for meeting these demands. Gallium Nitride (GaN) HEMTs are leading in high-frequency, high-power applications due to their superior properties like high electron mobility and thermal conductivity. Accurate modelling of GaN HEMTs is essential for predicting performance and optimizing integration into communication systems. Challenges include capturing physical phenomena such as charge-conservation, trapping effects, and thermal management. In this thesis, a novel GaN model integrating the ASM-GaN HEMT model with artificial neural network (ANN) techniques was proposed, retaining the ASM model's scalability and leveraging ANN's nonlinear modelling capabilities. This model led to the innovative design of a matching network for GaN device packaging, resulting in a packaged GaN PA.

Additionally, for CMOS technology, a sub-6GHz two-stage differential push-pull PA structure for 5G applications was designed, incorporating on-chip baluns for matching. Research also focuses on designing PAs for mmWave frequencies, crucial for radar applications. In the automotive radar bands of 60GHz and 77GHz, a novel dual-frequency matching structure based on coupled lines was proposed, achieving simultaneous impedance matching at different frequencies by adjusting the electrical lengths of the coupled and transmission lines. This resulted in a dual-band PA operating efficiently at both 60GHz and 77GHz.

In the emerging field of terahertz research, several PAs and driver amplifiers (DAs) for sub-terahertz (sub-THz) radar transceivers used in environmental sensing were designed. A T-shaped embedding network was employed to enhance maximum gain ($G_{\max}$), and an 8-shape transformer was introduced for impedance matching. This novel transformer design facilitated realizing extreme parameters compared to traditional transformers while significantly reducing the overall chip area.

Finally, the proposed methods and theories were thoroughly supported by extensive simulations and experimental results, demonstrating their effectiveness and practical applicability.

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List of Acronyms

4/5/6G	4 th /5 th /6 th generation of cellular network technology
IoT	Internet of Things
PA	Power Amplifier
GaN	Gallium Nitride
HEMT	High Electron Mobility Transistor
ASM-GaN-HEMT	Advanced SPICE Model for GaN HEMTs
ANN	Artificial Neural Network
ASM	Advanced SPICE Model
B5G	Beyond fifth generation of cellular network technology
Si	Silicon
GaAs	Gallium Arsenide
CMOS	Complementary Metal-Oxide Semiconductor
mmWave	Millimeter Wave
DA	Driver Amplifier
Sub-THz	Sub-Terahertz
$G_{\max}$	Maximum achievable Gain
SOI	Silicon on Insulator
PAE	Power Added Efficiency
P1dB	Output 1 dB compression point
VHT80	Very High Throughput channel at 80MHz
MCS9	Modulation and Coding Scheme 9
256-QAM	256-quadrature amplitude modulation
EVM	Error Vector Magnitude
UWB	Ultra-Wideband

P_{sat}	Output Saturated Power
FET	Field Effect Transistor
C_{pgi}	interelectrode and crossover capacitances between gate and source
C_{pdi}	interelectrode and crossover capacitances between drain and source
C_{gdi}	interelectrode and crossover capacitances between gate and drain
C_{gg}	Added Outer capacitance in gate side
C_{dd}	Added Outer capacitance in drain side
R_{gg}	Added Outer resistance in gate side
R_{dd}	Added Outer resistance in drain side
C_{gp}	Outer capacitance in gate side
C_{dp}	Outer capacitance in drain side
G_{gsf}	Intrinsic conductance between gate and source
G_{gdf}	Intrinsic conductance between gate and drain
G_{ds}	Output conductance
τ_{ds}	Time delay
AlGaN	Aluminum Gallium Nitride
I_{ds}	Drain current
V_{ds}	Drain voltage
R_{ch}	Channel Resistance
R_y	Diode differential resistance
V_{pk}	Gate voltage at which the maximum of the trans-conductance occurs
I_{pk}	Gate current at which the maximum of the trans-conductance occurs
ψ_p	A power series function centred at V_{pk}
K_{bg}	Dispersion via the intrinsic gate voltage at RF
ΔP_1	fundamental harmonic dependence with V_{ds}

$\Delta P_{2/3}$	$2^{\text{nd}}/3^{\text{rd}}$ harmonic dependence with V_{ds}
$P_1(f(T))$	Temperature dependence of the carrier velocity
I_{pk0}	Thermal effect on the carrier's concentration.
α_r	Saturation parameters
α_s	Saturation parameters
λ	Channel length modulation
MVSG	MIT Virtual-Source Gallium-nitride
$I_{d,rs}$	Self-consistent current in access region
I_d	Self-consistent current in intrinsic gated region
$I_{d,gfp}$	Self-consistent current for gate field plate (GFP)
$I_{d,sfp}$	Self-consistent current for source field plate (SFP)
$I_{d,rd}$	Self-consistent current in drain access region.
C_g	Gate capacitance per unit area
v_{sat}	Saturation velocity
ϕ_t	Thermal voltage in MVSG
μ	Mobility
ΔT	Temperature rise
T	Nominal temperature
n	Subthreshold factor
$\theta_i(T)$	Fitting parameters
E_F	Quasi-Fermi level
n_s	Charge density
V_{th}	thermal voltage in ASM-GaN-HEMT
D	density of states
E_0	sub-band within the quantum well

E_1	sub-bands within the quantum well
γ_0	parameters determined through experiments
γ_1	parameters determined through experiments
V_{go}	Gate Overdrive voltage
V_{gs}	Gate voltage
V_{off}	Pinch off voltage
d	Thickness of the AlGaIn barrier
V_x	channel potential at a given point x in the transistor
DynaFET	Dynamic FET model
EMLP	Evolutionary multilayer perceptron
DNN	Dynamic neural network
ADAS	Advanced driver assistance systems
DBA	Differential bi-directional amplifier
PAPR	Peak-to-average power ratio
TBFC	Transformer-based folded-cascode
RFSOI	Radio Frequency Silicon-on-Insulator
DAT	Distributed active transformers
MAG	Maximum available gain
FDSOI	Fully depleted silicon-on-insulator
BEOL	Back-end-of-line
φ_s	Surface potential at source terminal
φ_d	Surface potential at drain terminal
MOPSO	Multi-objective particle swarm optimization
TEM	Transmission Electron Microscopy
MOCVD	Metal-Organic Chemical Vapor Deposition

2DEG	2-dimensional electron gas
PECVD	Plasma-enhanced chemical vapor deposition
Q_{gi}	Intrinsic gate charges
Q_{di}	Intrinsic drain charges
ΔC_y	Infinitesimal capacitance of Shottky barrier
ΔR_y	Infinitesimal resistance of Shottky barrier
C_y	Equivalent lumped capacitance of Shottky barrier
R_y	Equivalent lumped resistance of Shottky barrier
ΔC_{ch}	Infinitesimal capacitance of channel barrier
ΔR_{ch}	Infinitesimal resistance of channel barrier
C_{ch}	Equivalent lumped capacitance of channel barrier
R_{ch}	Equivalent lumped resistance of channel barrier
ECPs	Equivalent circuit parameters
$\varepsilon_{ij}(S)$	Extraction error for each of the four elements of the S parameters
K_B	Boltzmann constant
PSO	Particle swarm optimization
CPW	coplanar waveguide
SoP	System-on-Package
BVR	Bandgap voltage reference
CSCG	Common source common gate
ADS	Advanced Design System
VCO	Voltage Controlled Oscillator
FMCW	Frequency-modulated continuous-wave
U	Unilateral power gain
LLR	Linear-lossless-reciprocal

Chapter 1. Introduction

Firstly, this chapter briefly introduces the background and motivation of the research, focusing on advanced GaN HEMT models and mmWave power amplifiers for 5G and Beyond 5G (B5G) applications. Subsequently, section 1.2 outlines the objectives of the research. Additionally, the major contributions, including theoretical and practical innovations and achievements, are listed, followed by the organization and outline of the entire thesis.

1.1. Background and Motivation

The rapid advancement in wireless communication technologies has brought about an unprecedented demand for high-performance electronic components capable of operating at higher frequencies with greater efficiency. The evolution from 4G to 5G has significantly enhanced data rates, reduced latency, and improved overall user experience. However, as the world moves towards B5G and even 6G, the expectations and requirements for communication systems continue to escalate. The primary drivers for these next-generation systems include the proliferation of the Internet of Things (IoT), the emergence of autonomous vehicles, the expansion of smart cities, and the increasing reliance on high-speed, reliable internet connectivity[1-4].

At the heart of these advancements are high-frequency, high-power devices that can efficiently manage the increasing demands for data transmission and reception. Among these devices, PAs play critical roles. Power amplifiers are essential components in the transmission chain of communication systems, as they amplify the signal to the required power level before transmission. The performance of PAs directly impacts the efficiency, range, and reliability of wireless communication systems.

GaN HEMTs have emerged as a leading technology in high-frequency and high-

power applications due to their superior material properties. GaN, a wide bandgap semiconductor, offers significant advantages over traditional silicon (Si) and gallium arsenide (GaAs) technologies. These advantages include high electron mobility, high breakdown voltage, and excellent thermal conductivity, which enable GaN HEMTs to operate at higher voltages, temperatures, and frequencies. These properties make GaN HEMTs particularly suitable for use in high-frequency applications, providing the performance needed for modern communication systems. However, accurate device modeling is crucial for predicting the performance of GaN HEMTs in real-world applications and for optimizing their integration into communication systems. The challenge lies in capturing the various physical phenomena that occur within the device, including charge-conservative, trapping effects, thermal management, and reliability under high-stress conditions[5-7].

In parallel, the design of PAs operating at mmWave frequencies, specifically within the 60GHz, 77GHz, and 110-170GHz bands, is another critical area of research. These frequency bands are essential for radar applications due to their ability to support high data rates and dense sensor networks. The 60GHz and 77GHz dual-band PAs are specifically designed for automotive radar systems, enhancing vehicle safety and autonomous driving capabilities [8-10]. These dual-band PAs enable both short-range applications, such as parking assistance and blind-spot detection, and long-range functions, including adaptive cruise control and collision avoidance. Additionally, the D-band PAs aim to improve environmental sensing in automotive radar systems, further advancing autonomous driving technology [11-14]. CMOS technology, with its scalability and integration capabilities, offers a promising platform for mmWave PA design. However, designing efficient PAs in CMOS at these frequencies requires innovative circuit topologies and design techniques.

1.2. Research Objectives

The significance of this research lies in its potential to advance the state-of-the-art in GaN HEMT device modeling for 5G applications and the design of high efficiency mmWave power amplifiers using CMOS technology for B5G applications. The research objectives are listed below:

1. **Develop Advanced GaN HEMT Device Models:** Create accurate and scalable models for GaN HEMTs that account for complex physical phenomena such as charge-conservation, trapping effects, and self-heating effects. These models will be essential for understanding and optimizing the performance of GaN HEMTs in high-frequency applications. A packaged PA is designed based on the proposed models to verify the effectiveness of the proposed model.

2. **Design High-Efficiency mmWave Power Amplifiers:** Design power amplifiers for the 60GHz, 77GHz, and 110-170GHz bands, focusing on innovative circuit topologies and design techniques to enhance efficiency and performance using CMOS technology. Thorough testing and validation of the designed PA are conducted.

By achieving these objectives, the research aims to contribute significantly to the advancement of high-frequency communication systems, addressing the critical demands of the emerging B5G and 6G technologies.

1.3. Major Contributions

My research work during Ph.D. period primarily focuses on the design of power amplifiers for 5G and B5G applications. Given the necessity for accurate GaN models in high-frequency PA design, this research initially aims to develop precise and scalable GaN models. To address this, a novel GaN model that integrates the Advanced SPICE

Model for GaN HEMT (ASM-GaN HEMT) with artificial neural network (ANN) techniques is proposed. This hybrid model not only retains the dimensional scalability of the ASM model but also leverages the nonlinear modeling capabilities of ANNs. Based on this model, I innovatively designed a matching network for the GaN device packaging, resulting in a packaged GaN PA.

Additionally, for CMOS technology, I designed a sub-6GHz two-stage differential push-pull PA structure for 5G applications, incorporating on-chip baluns for matching. In the widely used automotive radar bands of 60GHz and 77GHz, I proposed a novel dual-frequency matching structure based on coupled lines. This innovative structure achieves simultaneous impedance matching at different frequencies by adjusting the electrical lengths of the coupled lines and transmission lines. This resulted in the development of a dual-band PA that operates efficiently at both 60GHz and 77GHz.

Furthermore, in the emerging field of terahertz research, I designed several PAs and driver amplifiers (DAs) for sub-terahertz (sub-THz) radar transceivers used in environmental sensing. A T-shaped embedding network is employed to enhance maximum gain ($G_{\max}$), and an 8-shape transformer is introduced for impedance matching. This novel transformer design allows for easier realization of extreme parameters compared to traditional transformers while significantly reducing the overall chip area.

Finally, the proposed methods and theories have been thoroughly supported by extensive simulations and experimental results, demonstrating their effectiveness and practical applicability.

1.4. Organization of the thesis

The organization of this thesis is as follows:

Chapter 2 presents the current state-of-the-art GaN model types, and the different equivalent circuits for GaN HEMT and various GaN models are introduced. Then it summarizes the trend of using ANN technologies for GaN modeling. Additionally, this section reviews and summarizes the state-of-the-art Beyond 5G power amplifiers, describes some of the more special design methods in detail, especially at 60GHz, 77GHz, and D-band frequencies. Furthermore, various design methods mentioned in these research articles are summarized and classified according to different research purposes and finally lists the performance of most PAs in a table, providing guidance for research in this field.

Chapter 3 introduces a novel GaN model design method that combines the ASM-GaN-HEMT with ANN techniques. This innovative approach not only retains the dimensional scalability of the ASM model but also leverages the powerful nonlinear modeling capabilities of ANN technology. The chapter demonstrates the effectiveness of this hybrid method by modeling two GaN HEMTs fabricated in-house. Detailed comparisons are made between the performance of the models derived from the new method and those obtained using the traditional ASM-GaN approach. Sufficient experimental results indicate that the new hybrid model outperforms the conventional method, providing more accurate and reliable predictions of the device's behavior under various operating conditions.

Chapter 4 presents a power amplifier design based on 130nm CMOS Silicon-on-insulator (SOI) process at sub-6GHz. This design employs a differential push-pull structure to achieve higher output power than the single-ended configuration. On-chip transformer baluns are investigated and utilized as the anti-phase splitter and combiner for input and output impedance matching networks. The proposed PA achieves a maximum power gain of 25.6 dB, an output power of 22.2 dBm, and a power added

efficiency (PAE) of 28% at the output 1 dB compression point (OP_{1dB}). It shows a 3 dB bandwidth spanning from 4.3 GHz to 6.4 GHz and occupies a core area of 0.59 mm². When tested under IEEE 802.11ac standards and VHT80 MCS9 conditions (80MHz, 256-QAM), the PA provides an output power of 21.4 dBm and a PAE of 24.8% at 5.5 GHz, with an error vector magnitude (EVM) of -36 dB.

Chapter 5 introduces a novel dual-band power amplifier, specifically designed for beyond 5G applications, operating efficiently at 60GHz and 77GHz. A detailed theoretical analysis of dual-band impedance converters based on couple-lines has been conducted, along with specific design methodologies. The proposed unique coupler design employs the varying electrical lengths of couplers and transmission lines at different frequencies, resulting in distinct impedance characteristics at 60GHz and 77GHz, thus could fulfil the matching at both frequency points. The simulation results reveal impressive performance, achieving power gains of 12.4 dB at 60GHz and 9.8 dB at 77GHz, with output powers of 12 dBm at 60GHz and 10 dBm at 77GHz, and power-added efficiencies of 24.4% and 13.85%, respectively. This advancement in power amplifier design marks a significant step towards improving the efficiency and effectiveness of radar applications beyond 5G.

Chapter 6 introduces the system structure of a sub-THz Ultra-Wideband (UWB) radar transceiver operating at D-band frequency (110-170 GHz) with a bandwidth of over 30 GHz. Based on the system's specifications, several PAs and DAs were designed. These amplifiers employ a dual-peak G_{max} -core gain boosting technique, which enhances the transistor's small-signal gain by adding a T-shaped embedding network around the transistor. Additionally, an innovative figure-eight-shaped transformer is used in the matching network of these PAs and DAs. This transformer shape offers higher design flexibility and significantly reduces the area compared to traditional

stacked transformers. The final design of the three-stage PA achieves a 13 dB gain, a 3 dB bandwidth ranging from 113 GHz to 130 GHz, a $P_{1\text{dB}}$ of 5 dBm, and a saturated output power (P_{sat}) of 8.4 dBm.

Finally, in Chapter 7, conclusions are drawn, and future work plans are presented.

Chapter 2. Review of GaN HEMT modeling and B5G PA designs

This chapter presents the literature review of the GaN device modeling and power amplifier design at mmWave frequency. The commonly utilized PA structure for efficiency and linearity improvement are briefly illustrated.

2.1 GaN Device Modeling

2.1.1 Equivalent Circuits of GaN HEMTs

Since the successful development of GaN HEMT devices in the 1990s, due to the unique advantages of GaN materials in terms of band gap, electron mobility, thermal conductivity and relative permittivity, the process fabrication, electrical properties, Device models and other aspects have always been the research hotspots of domestic and foreign researchers. GaN HEMTs are well-suited for high-power microwave and millimeter-wave applications, but their high-frequency large-signal performance is limited by trap-related dispersion effects, which have been a key focus in recent research. [15]. There are three main models of GaN HEMT devices: physical-based model, behavior-based model, and equivalent circuit model. The equivalent circuit model is the most widely used device model at present, and an accurate small-signal model is the basis for characterizing the large-signal model of GaN HEMT devices. Therefore, different methods have been proposed for small-signal equivalent circuit modeling. In the literature, the small-signal modeling methods proposed by researchers can be divided into three types: cut-off condition method[16-19], test structure method and electromagnetic simulation method[20]. For different processes of GaN HEMT devices, topologies require different parameter extraction techniques for modeling. G. Crupi and researchers have proposed different circuit topologies for modeling. Different circuit D. M.M.-P. Schreurs et al. through in-depth research on Field Effect Transistor (FET) and

summarizing the modeling work of related researchers, in their book “Microwave de-embedding from theory to applications” give a typical small-signal circuit topology for a FET device is shown, as shown in Fig. 2.1[21]. The model proposed by other related researchers can be regarded as an extension of the circuit topology shown in Fig. 2.1 to take into account the effects introduced by different fabrication processes, such as the 22-element model[16, 17], 19 Component model[18], 26-component model[22], 20-component model[23], etc.

A. Jarndal et al. proposed two different 22-element small-signal equivalent circuit models in 2006 and 2011, respectively, to account for the effects of device process. In the literature [19], A. Jarndal et al. added circuit elements C_{pgi} , C_{pdi} and C_{gdi} based on

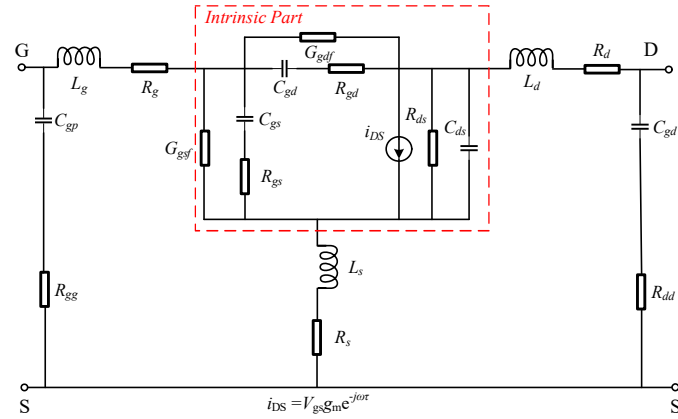


Fig. 2.1 Small-signal typical equivalent circuit topology for microwave FET devices [21].

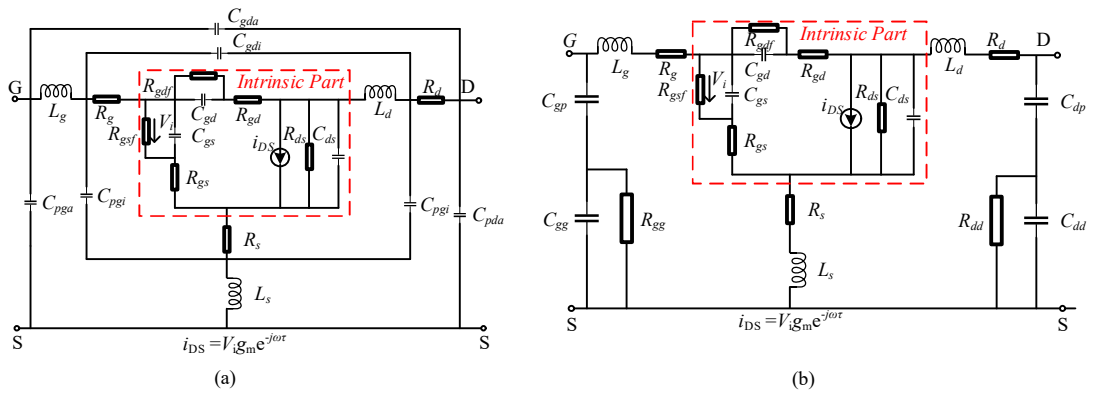


Fig. 2.2 (a) 22-element model considering interpole distributed capacitance [16]; (b) 22-element model considering parasitic conduction [17].

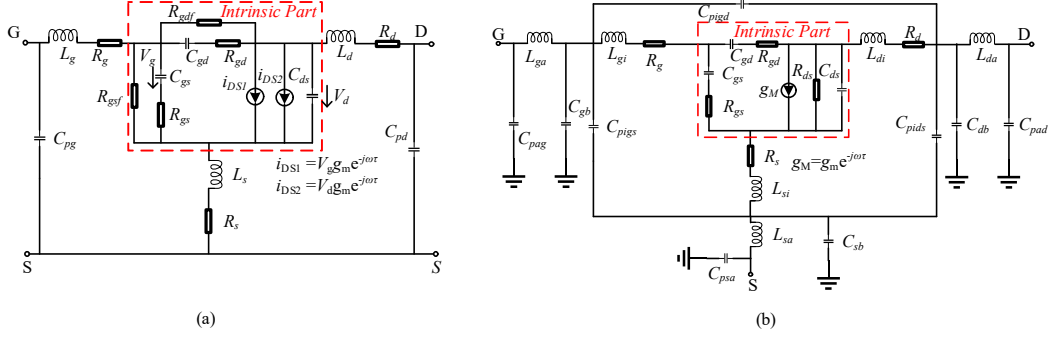


Fig. 2.3. (a) 19-element model considering time delay [18]. (b) 26-element model for broadband 0.1 to 110GHz [22].

the traditional small-signal equivalent circuit model to consider the effect of distributed capacitance between electrodes introduced by the air bridge. The circuit model is shown in Fig. 2.2 (a). In, GaN HEMT devices based on Si substrates have parasitic turn-on problems. To characterize this phenomenon, A. Jarndal et al. pointed out that two RC branches (C_{gg} , C_{dd} , R_{gg} , R_{dd}) can be connected in series with parasitic capacitances C_{gp} and C_{dp} , as shown in Fig. 2.2 (b)[24]. Since the 20-element model proposed by G. Crupi et al. ignores differential conductance G_{gsf} and G_{gdf} , it can be seen as a simplification of the 22-element model proposed by A. Jarndal et al.

R. G. Brady et al. reported a small-signal equivalent circuit model of 19 elements in 2008. In order to consider the negative value of the output conductance G_{ds} in the high frequency band caused by the phase delay, a time delay τ_{ds} was introduced to the output conductance G_{ds} , as shown in Fig. 2.3(a)[18]. In 2013, D. Schwantuschke et al. established a fully scalable small-signal equivalent circuit model for AlGaIn/GaN HEMTs, and proposed a 26-element equivalent circuit model, as shown in Fig. 2.3 (b), the model takes into account the characteristics of parasitics as a function of device geometry, and proposes an 18-element distributed parasitic network[22].

2.1.2 Compact GaN Models in Industry

2.1.2.1 Anglov Model

As can be seen in Fig. 2.4, the existing GaN compact models can be classified as table-based, empirical and physics-based models. Anglov model is one of the most famous empirical models that has been widely used as the mode standard in the present industry[25].

The equivalent circuit of the GaN HEMT is shown in Fig. 2.5, this model employs $\tanh()$ function in current I_{ds} and $\sinh()$ function in ψ_p to make the fit easier, the main equations are given as follow:

$$I_{ds} = I_{PK0} (1 + \tanh(\Psi_p) \cdot \tanh(\alpha_p V_{ds}) \cdot (1 + \lambda_p V_{ds} + L_{SB0} \cdot \exp(V_{dg} - V_{TR}))) \quad (2.1)$$

$$\Psi_p = \sinh(P_{1m}(V_{gs} - V_{pk}) + P_{2m}(V_{gs} - V_{pk})^2 + P_{3m}(V_{gs} - V_{pk})^3) \quad (2.2)$$

$$P_1 = g_{m \max} / I_{pk0} \quad (2.3)$$

$$V_{pk}(V_{ds}) = V_{pk} - \Delta V_{pks} + \Delta V_{pks} \tanh(\alpha_s V_{ds} + K_{BG} V_{bgate}) \quad (2.4)$$

$$\begin{aligned} P_{1m} &= P_1(f(T)) [(1 + \Delta P_1)(1 + \tanh(\alpha_s V_{ds}))] \\ P_{2m} &= P_2 [(1 + \Delta P_2)(1 + \tanh(\alpha_s V_{ds}))] \\ P_{3m} &= P_3 [(1 + \Delta P_3)(1 + \tanh(\alpha_s V_{ds}))] \\ \alpha_p &= \alpha_R + \alpha_S (1 + \tanh(\psi_p)) \end{aligned} \quad (2.5)$$

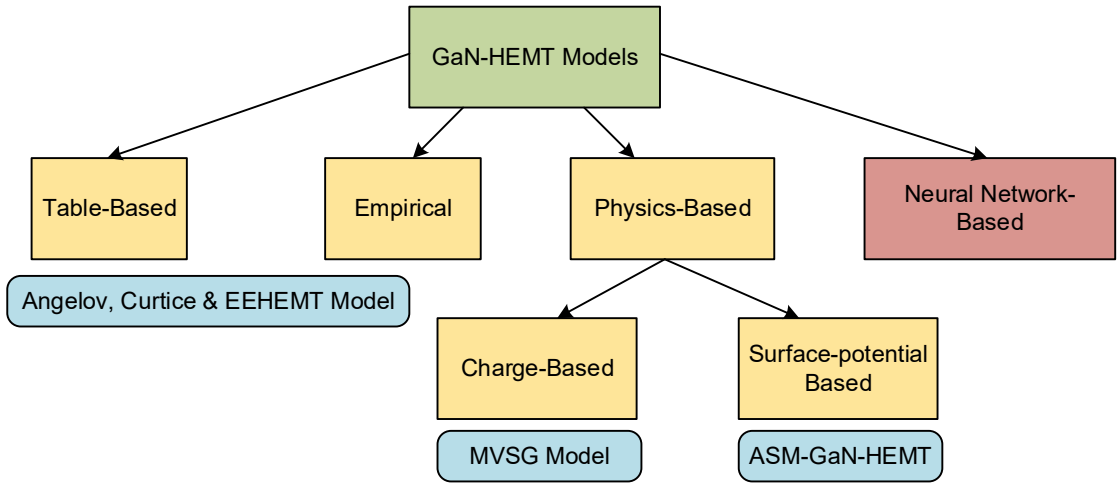


Fig. 2.4. Classifications of various GaN HEMT models.

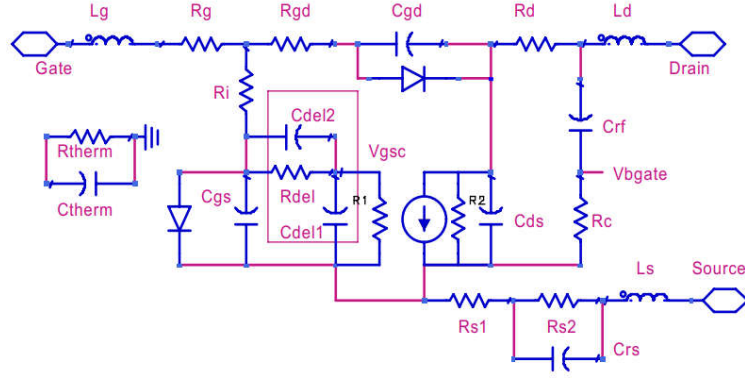


Fig. 2.5. Equivalent circuit model of Angelov GaN HEMT model[25].

2.1.2.2 MVSG Model

The MVSG model is one of the two strong physical based models for both RF and power switching applications that were chosen as industry standard. The MVSG model is a charge-based model for GaN HEMTs, utilizing the concept of virtual source "top-of-barrier" transport of carriers in field-effect devices. Fig. 2.6 shows the equivalent circuit of the MVSG model, it employs five-transistor-sub-circuits to capture the static and dynamic behavior through self-consistent current and charge expressions, where $I_{d,rs}$ stands for access region, I_d means intrinsic gated region, $I_{d,gfp}$ for gate field plate (GFP), $I_{d,sfp}$ for source field plate (SFP) and $I_{d,rd}$ represents drain access region[26]. A more detailed equivalent circuit is given on Fig. 2. 7.[27] Moreover the key mode equations which capture currents and charges are given as follow[26, 27]:

$$I_D/W = \frac{(Q_{inv,s} + Q_{inv,d})}{2} v_{sat} F_{Vsat} \quad (2.6)$$

$$Q_{inv,s(d)} = 2C_g n\phi_t \ln \left(1 + \exp \left(\frac{(V_G - V_{S(D)}) (V_T - \alpha\phi_t F_{f,S(D)})}{2n\phi_t} \right) \right)$$

$$F_{Vsat} = \frac{(Q_{inv,s} - Q_{inv,d})/C_g V_{DSAT}}{\left((1 + ((Q_{inv,s} - Q_{inv,d})/C_g V_{DSAT}))^\beta \right)^{1/\beta}} \quad (2.7)$$

$$\mu = \mu_0 \left(1 + \frac{\Delta T}{T_0} \right)^{-\varepsilon}; v_{sat} = v_{sat0} (1 + Z\Delta T)^{-1}; V_{DSAT} = \frac{L_g v_{sat}}{\mu}$$

$$Q_{S(D)} = \frac{2WL_g}{(Q_{inv,s}^2 - Q_{inv,d}^2)^2} \left[(+) \frac{Q_{inv,s}^5 - Q_{inv,d}^5}{5} - (-) Q_{inv,d(s)}^2 \frac{Q_{inv,s}^3 - Q_{inv,d}^3}{3} \right] \quad (2.8)$$

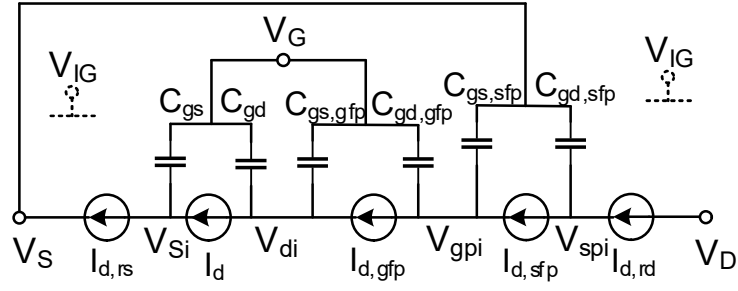


Fig. 2.6. The simplified equivalent circuit for MVSG model [26].

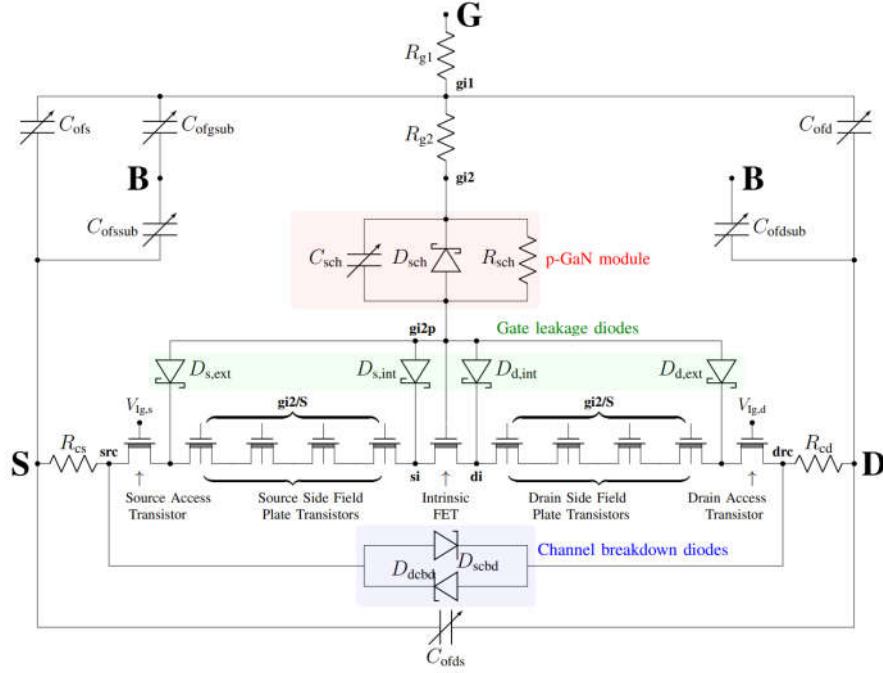


Fig. 2.7. The equivalent circuit for MVSG model [27].

$$f(V_{DS}) = \theta_1(T)V_{DG} + \theta_2(T)\exp\left(\frac{V_{DG} - V_{TRAP}}{\theta_3(T)}\right) \quad (2.9)$$

Where C_g is gate capacitance, v_{sat} is saturation velocity, ϕ_t is thermal voltage, μ is mobility, ΔT is temperature rise, T is nominal temperature, n is subthreshold factor, $\theta_1(T)$, $\theta_2(T)$ and $\theta_3(T)$ are fitting parameters.

2.1.2.3 ASM-GaN-HEMT Model

Another physics-based model that has been chosen to be the GaN HEMT model standard is the ASM-GaN-HEMT model. The ASM-GaN-HEMT model considers most of the nonlinear device effects, such as self-heating, mobility degradation, DIBL and so on to build a completed drain current model, shown in Fig. 2.7. The core principle is to

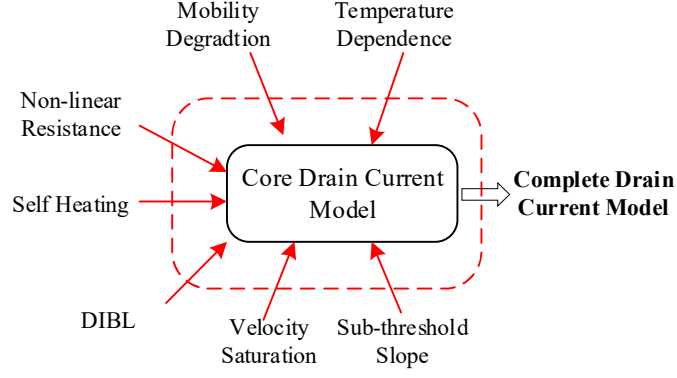


Fig. 2.7. Core surface-potential-based drain current model with various nonlinear effects [28].

evaluate the quasi-Fermi level (EF) as a function of bias within the triangular quantum well formed at the AlGaIn/GaN heterojunction. [28, 29]. The following expressions relate EF and the charge density n_s , which are an outcome of Schrodinger's equation and voltage balance across the AlGaIn/GaN heterojunction respectively[30-33].

$$n_s = DV_{th} \left[\ln \left[\exp \left(\frac{E_F - E_0}{V_{th}} \right) + 1 \right] + \ln \left[\exp \left(\frac{E_F - E_1}{V_{th}} \right) + 1 \right] \right] \quad (2.10)$$

$$n_s = \frac{\epsilon}{qd} (V_{go} - E_F - V_x) \quad (2.11)$$

$$E_{0/1} = \gamma_{0/1} n_s^{2/3} \quad (2.12)$$

where V_{th} denotes the thermal voltage, D represents the density of states, E_0 and E_1 refer to the two sub-bands within the quantum well, γ_0 and γ_1 are parameters determined through experiments, V_{go} is the gate overdrive (calculated as $V_{gs} - V_{off}$), d is the thickness of the AlGaIn barrier and V_x is the channel potential at a given point x in the transistor.

2.1.2.4 ANN-based GaN HEMT Model

ANN based GaN device modeling is also a popular approach that uses machine learning techniques to create accurate models without the need for extensive physical knowledge. ANN models can capture non-linear and complex device behaviors like self-heating and trapping effects and are computationally efficient [34, 35]. However, their effectiveness depends on the availability of large, high-quality datasets for training,

and their accuracy is sometimes constrained by the quality of the input data. ANN models are typically used in combination with other modeling approaches to improve accuracy. Recent years have seen a surge in the application of ANN in GaN HEMT modeling. Research has explored various innovative approaches, such as Dynamic FET model (DynaFET) [36], evolutionary multilayer perceptron (EMLP) based modeling [37], gate charge model based on neural networks [38], and electrothermal modeling approach using ANN applied to GaN devices [39]. Further research has investigated machine learning techniques for temperature-dependent small signal modeling [38, 40, 41], compared different ANN architectures for behavioral modeling [42], and explored the innovative use of a hybrid multilayer perceptron-random forest model for precise estimation of device parameters [43]. Additionally, novel methodologies like Wiener-type dynamic neural network (DNN) structures for nonlinear device modeling have also been put forth [44]. Although ANN models adeptly replicate device behavior, their lack of physical interpretability obscures the understanding of underlying physical principles. This gap has catalyzed the exploration of hybrid models combining ANN and physical modeling approaches [45]. Such hybrid models promise enhanced accuracy and computational efficiency over standalone ANN models. They adeptly capture complex physical phenomena while curtailing the volume of training data required.

2.2. Review of 60GHz and 77GHz power amplifiers

The rapid advancement in wireless communication and automotive radar technologies has driven the demand for high-frequency PAs operating at 60 GHz and 77 GHz. These frequency bands are crucial for various applications, including high-speed wireless communication systems, advanced driver assistance systems (ADAS), and autonomous vehicles. This section provides a systematic review of recent

advancements in power amplifiers designed for these frequency bands, highlighting their design innovations, performance metrics, and application suitability.

Ref. [46] presents a two-stage PA designed at 54-68 GHz frequency range in 40 nm CMOS process. The circuit diagram is shown on Fig. 2.8, two built-in linearizers are added in the second stage to further improve the linearity of the PA. The initial linearizer functions as a pre-distortion circuit, whereas the second linearizer operates as a body-biased post-linearizer located between transistors M_4 and M_6 .

Besides using lumped components for matching network design, some researchers also focused on transformer-based or coupler-based unique matching networks design. Ref. [47] introduces a two-stage differential bi-directional amplifier (DBA) for 60GHz applications in a 65-nm CMOS process. This work utilizes a differential neutralized common-source gain cell, enhanced by a cross-coupled g_m -boosting technique for enhanced stability and gain. The circuit diagram and chip photo are given in Fig. 2.9.

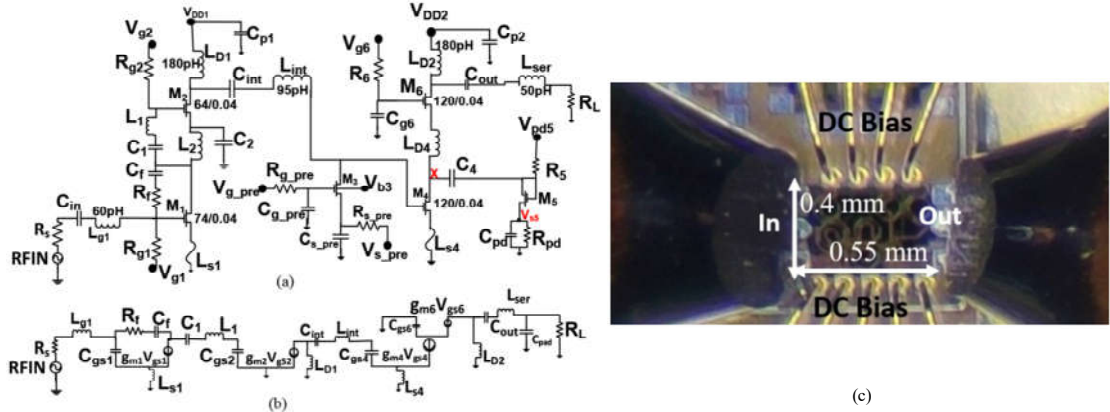


Fig. 2.8 (a) Circuit schematic of the proposed PA, and (b) the small-signal equivalent circuit. (c) The two-stage PA die photograph [46].

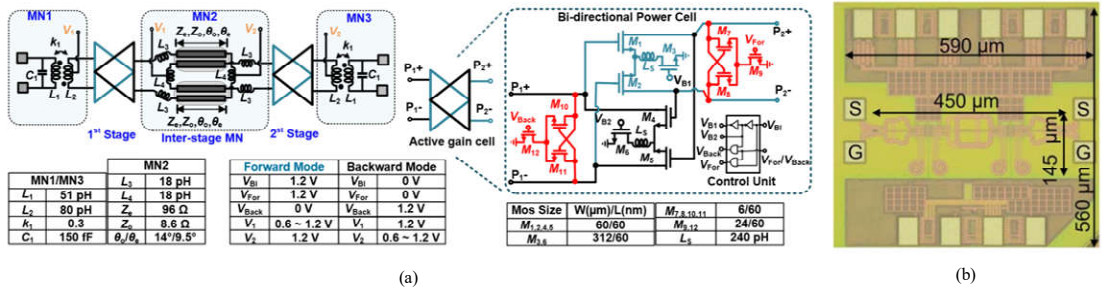


Fig. 2.9 (a) Symmetrical DBA topology. (b) Die micrograph [47].

To address the power consumption problems existing in 60GHz short-range applications, Ref. [48] presents two designs of low-power balanced front-end amplifiers in 65nm PD-SOI CMOS technology, the circuit diagram and chip photo are given in Fig. 2.10. The circuit adopts resistive feedback neutralized common-source differential pair architecture with 90° twisted hybrid couplers to achieve power combining and enhanced robustness against load variations.

High-frequency communication systems often utilize complex modulation schemes (e.g., QAM) that necessitate linear operation of PAs across a broad range of output power levels. These modulation schemes typically exhibit a high peak-to-average power ratio (PAPR), which can degrade the average efficiency of the PA. In practical applications, the PA frequently operates below its maximum output power, a condition known as power back-off. Maintaining high efficiency during power back-off is crucial

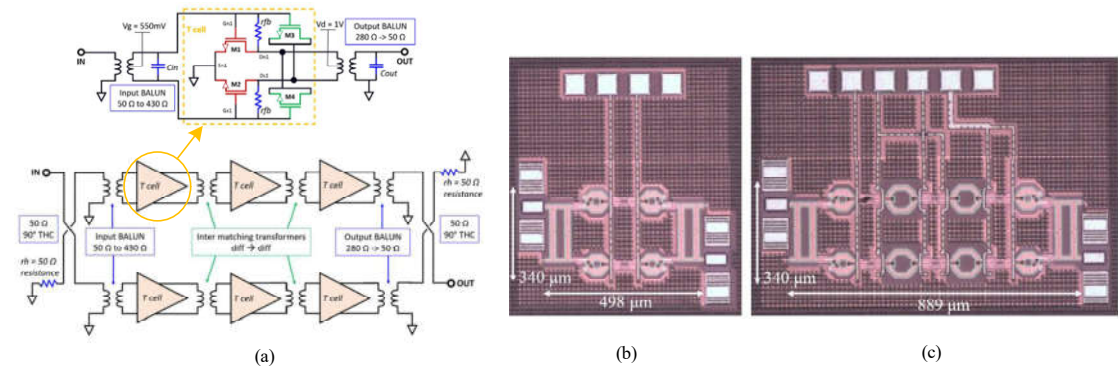


Fig. 2.10 (a) Detailed transistor cell (T cell) architecture and diagram of the three-stage proposed PA. (b) The 1-stage balanced amplifier die photograph and (c) 3-stages balanced amplifier die photograph [48].

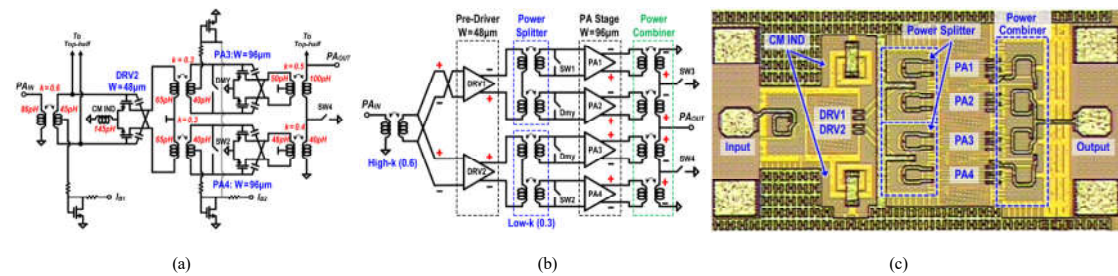
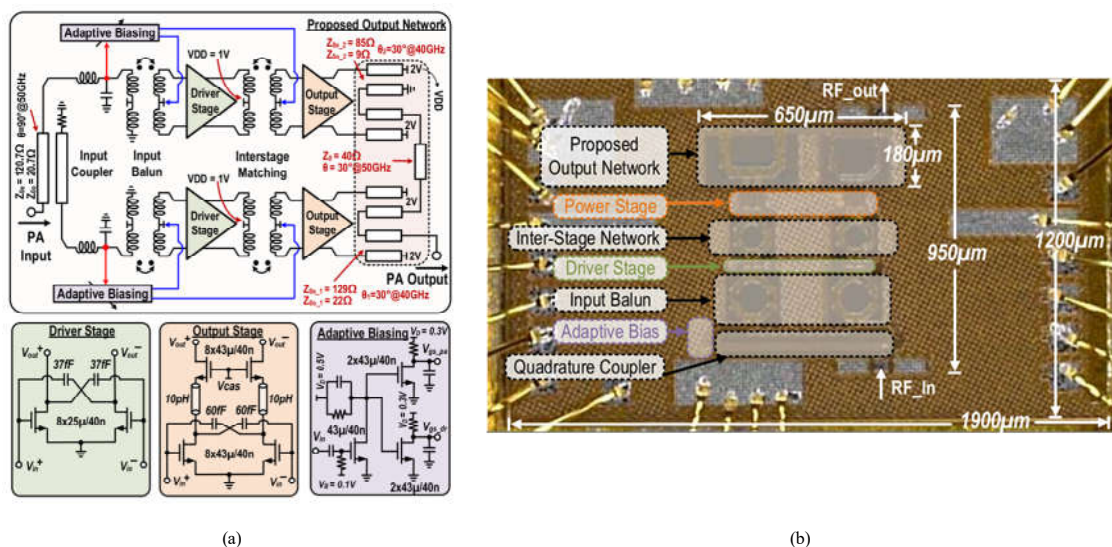


Fig. 2.11 (a) Transistor-level schematic of the proposed PA. (b) The proposed PA structure with a reconfigurable 4-way series-parallel power combiner. (c) Die photographs of the PA core [49].

to ensure linear PA operation, preserving the integrity of the transmitted signal and minimizing distortion. Ref. [49-53] have proposed different methods to enhance the PBO efficiency of the power amplifier.



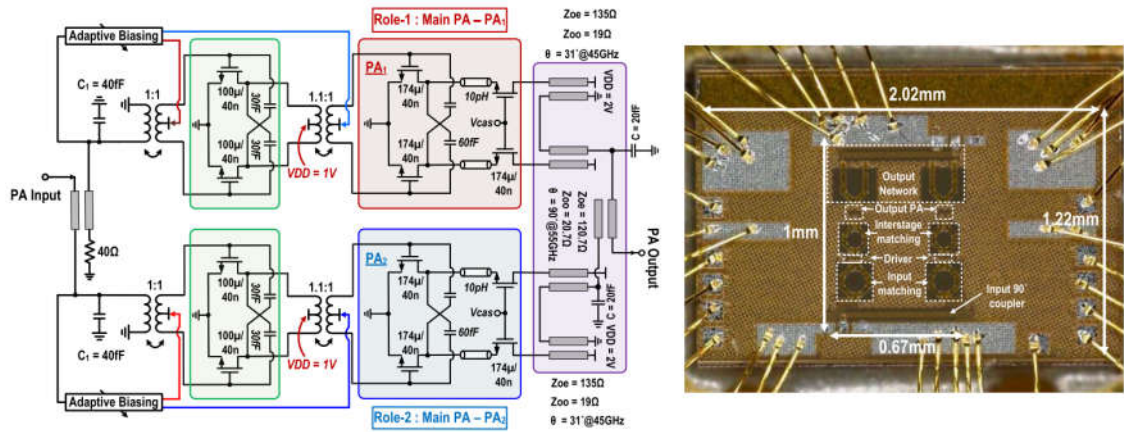


Fig. 2.13 PA architecture and chip microphotograph [53].

Table 2.1 Comparison to prior art 60GHz PA designs.

	[46]	[47]	[49]	[55]	[56]	[52]
Technology	40nm CMOS	65nm PD-SOI	16nm FF	45nm CMOS SOI	45nm CMOS SOI	45nm CMOS SOI
Topology	Single-ended	Balanced CS diff. (THC)	2/4 way Non-Uni Power Comb.	Cascaded Asym. DAT	On-Antenna Doherty	Coupler-Based Doherty
Frequency (GHz)	54-68	60	65	60	65	60
Supply (V)	2	1	0.95	2	1.9	2
Power Gain	14±1.5	21	21.4	23.9	12	12.9
P _{SAT} (dBm)	15	6.95	17.9	29.1	19.4	20.1
P _{1dB} (dBm)	14	3.7	13.5	24.7	19.2	19.3
Peak PAE	26%	8.4%	26.5%	18.4%	28.3%	26%
PAE@P _{1dB}	20%	5.1%	15%	8% ¹	27.5%	25.9%
PAE@PBO	NA	NA	18.4% @4.5dB PBO	NA	20.1% @6dB PBO	16.6% @7dB PBO
Modulation	NA	NA	64-QAM	64-QAM	64-QAM	64-QAM
Date Rate	NA	NA	6Gb/s	12Gb/s	6Gb/s	3Gb/s
RMS EVM	NA	NA	-23.2dB	-27.1dB	-23dB	-23.1dB
Average Pout	NA	NA	9.8dBm	20.9dBm	14.2dBm	13.8dBm
Average PAE	NA	NA	7.2%	5% ¹	20.2%	15.7%
Active Area (mm ²)	0.2	0.3	0.107	6.6	3.23*	0.76

¹Estimate from figures. *Including pads and on-chip antenna.

The performance of the 60GHz PAs mentioned above is summarized in Table 2.1.

77 GHz band is widely used in automotive radar applications for long-range detection and high-resolution imaging. Most power amplifiers in CMOS process employ differential structure in 77GHz, these designs employ transformer-based matching networks and neutralizing capacitors to expand the bandwidth and improve stability. Ref. [57] details a 77-GHz PA in a 28nm CMOS process, the PA features a digital power control scheme that adjusts the width of the RF MOS transistors to optimize PAE. The design incorporates a two-way power combiner and maintains performance from -45 to 125°C, making it suitable for long-range, middle-range, and

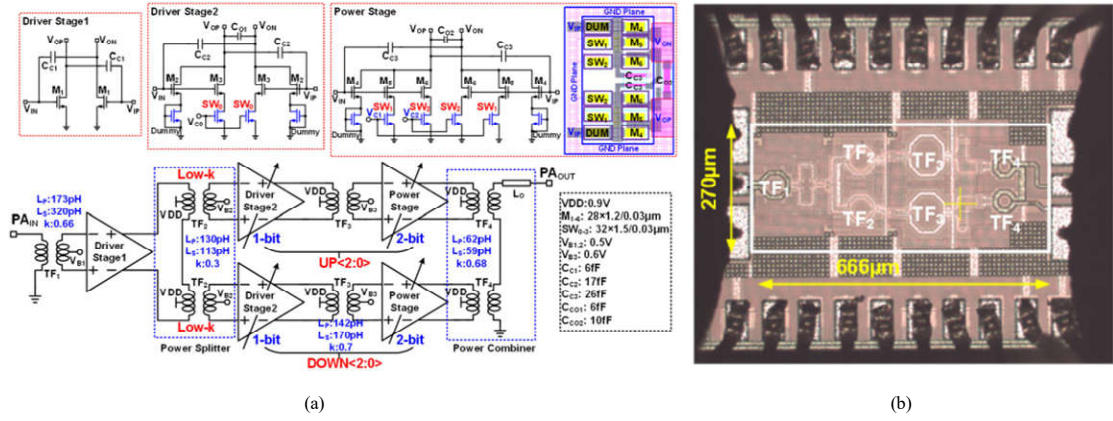


Fig. 2.14 (a) The schematic of proposed digital controlled PA. (b) Chip photograph [57].

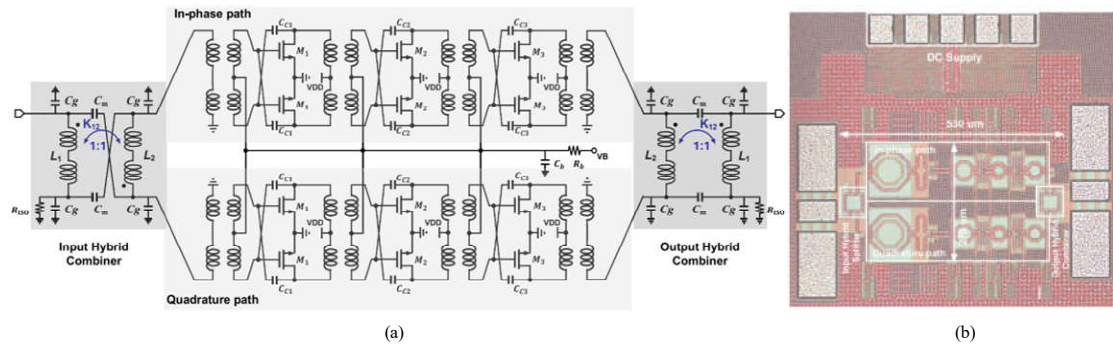


Fig. 2.15 (a) Schematic of the proposed power combining PA. (b) Die photograph [58].

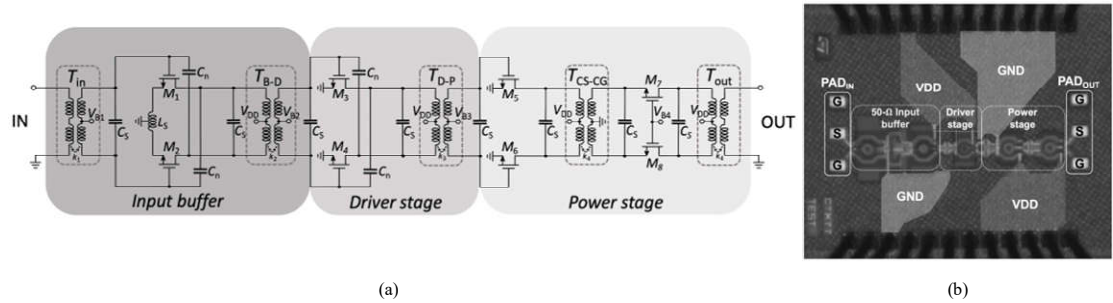


Fig. 2.16 (a) Simplified schematic of the 77-GHz PA. (b) Die photograph [59].

short-range radar applications in ADAS. The circuit diagram and chip photograph are given in Fig. 2.14. Ref. [58] features a novel transformer-based quadrature coupler used as the power splitter and combiner, achieving low loss and wide bandwidth in 65nm CMOS technology. The circuit diagram and chip photograph are given in Fig. 2.15. And Ref. [59] utilizes a pseudo-differential architecture incorporating coupling transformers and a transformer-based folded-cascode (TBFC) design, achieving a P_{sat} of 13.5 dBm,

Table 2.2 Comparison to prior art 77GHz PA designs.

	[57]	[58]	[59]	[60]
Technology	28nm CMOS	65nm CMOS	28nm CMOS	22nm FDSOI
Frequency (GHz)	72.9-89	77	77	76-81
Supply (V)	0.9	1.2	1	1.3
Power Gain	11.4-17	26.4	26.5	23.9
P_{SAT} (dBm)	12.15	15.82	14.5	9.5
P_{1dB} (dBm)	14	11.5	10	NA
Peak PAE	7.2-12%	15.9%	14.5%	10%
Active Area (mm ²)	0.178	0.143	0.14	0.065

and a PAE of 14.5% at 77 GHz while operating under the power supply of 1V. The circuit diagram and chip photograph are given in Fig. 2.16.

Besides these power amplifier block level designs, there are also many 77GHz radar system designs [61-63]. Table 2.2 has listed the performance of the prior art 77GHz PAs.

2.3. Review of D Band Power Amplifiers

The D-band frequency range offers significant opportunities for high-speed communication, imaging, and radar systems due to its wide available bandwidth. However, designing PAs that can operate efficiently and effectively in this range presents unique challenges. Recent advancements in semiconductor technologies, particularly in CMOS and FinFET processes, have enabled significant progress in D-band PA designs. This review provides an overview of recent advancements in D-band PA design, categorizing the efforts into a few strategies: power combining techniques, adaptive biasing, and wideband performance enhancements.

To achieve high output power level as required, most of the D band PA design employs transformer-based power combining techniques [64-67]. Among them, Ref [65] discusses multiway power combined amplifiers using 45nm CMOS RFSOI technology, focusing on enhancing both efficiency and output power. The proposed eight-way power combining network integrates a four-way balun with a short transmission line combiner and a traditional quarter-wavelength transmission line combiner. The circuit diagram, and 3-D layout of the four-way combiner and the chips photograph are shown

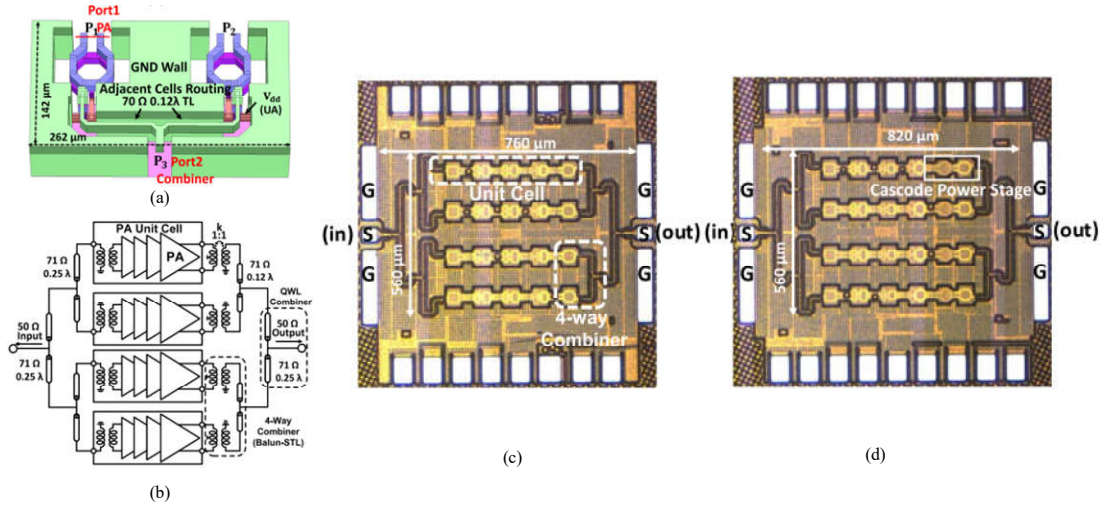


Fig. 2.17 (a) 3-D layout of the four-way combiner. (b) Circuit diagram of eight-way PA utilizing four-stage PA unit cells. Chip micro-photographs of (c) eight-way C.S. PA and (d) eight-way cascode PA [65]. in Fig 2.17. Ref. [66] features an on-chip current combining transformer integrated into a linearized PA for wireless chip-to-chip communications in 65nm CMOS process. This design addresses amplitude and phase mismatch issues that can degrade transformer performance. Furthermore, a diode-connected linearization method is implemented at the power stage to counteract the gate bias voltage degradation as input power rises. The circuit diagram and die photograph are shown in Fig. 2.18.

Ref. [67] presents a four-stage differential common-source PA using 28nm bulk CMOS. Significant enhancements include choosing transistors that offer superior efficiency and output power, integrating compensating inductors within the distributed active transformer (DAT) network to reduce insertion loss, and refining interstage matching to maximize efficiency, gain, and minimize chip area consumption. The PA employs a four-way power combining architecture, achieving a P_{sat} of 15.4 dBm, a peak PAE of 14.25%, a power gain of 19.2 dB, and a power density of 381 mW/mm². The analysis and design methods of this article are very instructive. The circuit diagram and die photograph are shown in Fig. 2.19.

Besides power combining techniques, there are some researchers focusing on boosting the power gain of transistors by adding embedding network in the transistor[68, 69]. Ref. [68] showcases a high-gain broadband amplifier designed with a T-shaped embedding network, which includes two series capacitors and a single shunt inductor. This network provides dual-peak maximum available gain (MAG) and broad gain-bandwidth with fewer stages. This design leverages the high degree of freedom in the

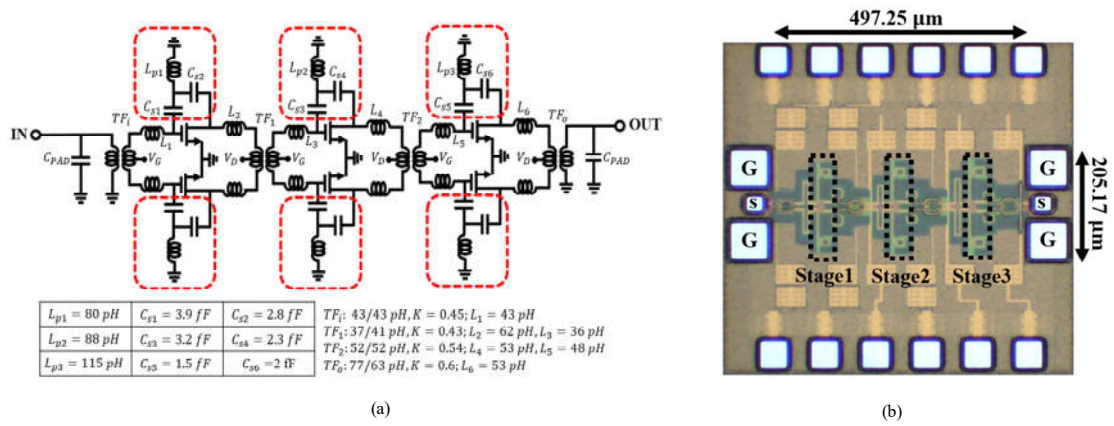


Fig. 2.20 (a) Schematic and (b) die photograph of the proposed D-band amplifier [68].

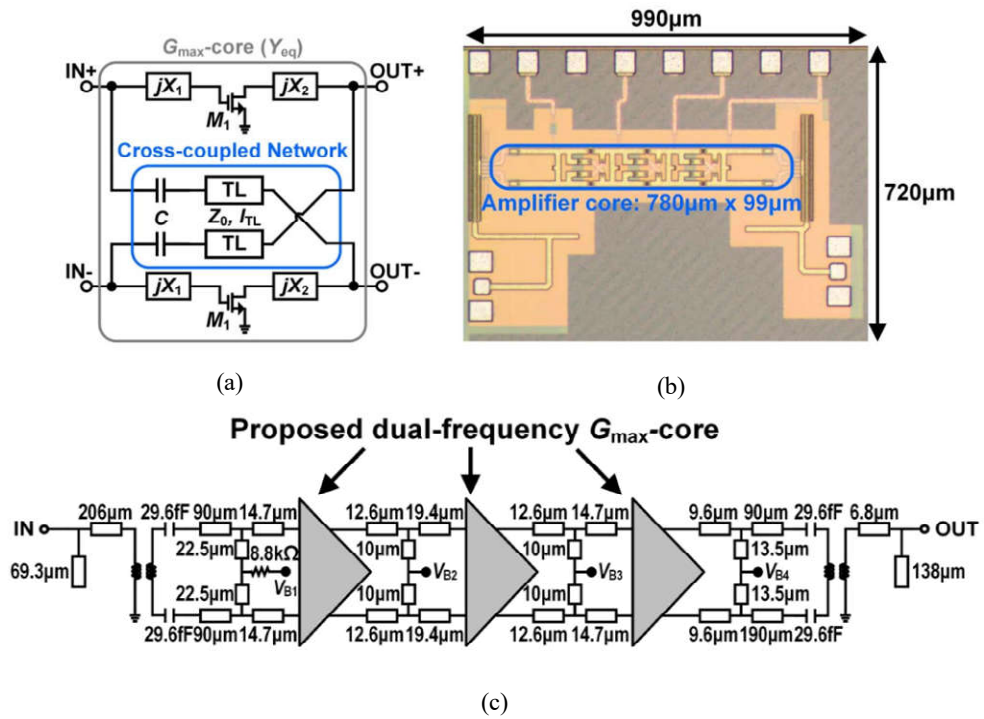


Fig. 2.21 (a) A cross-coupler-based differential G_{max} -core (b) Chip micrograph and (c) schematic of the designed 3-stage D-band PA [69].

T-shaped network to optimize the gain profile and input/output impedances, achieving an impressive gain-bandwidth product relative to power dissipation, outperforming many contemporary amplifiers operating at comparable frequencies. The circuit diagram and chip photograph are given in Fig. 2.20. Ref. [69] introduces a D-band differential amplifier featuring a cross-coupled capacitor and a transmission line-based dual-band core to minimize feedback and improve linearity. By using series-connected capacitors to neutralize gate-drain capacitance and incorporating a dual-frequency core, the design enhances gain across multiple frequencies. Fig. 2.21 (a) presents the differential $G_{\max}$ -core featuring a cross-coupled network, along with its corresponding two-port single-ended equivalent representation. Fig. 2.21 (b) and (c) show the circuit diagram and chip photograph.

Based on the characteristics of transistors under different process conditions, these articles implement specific changes to achieve better performance [70-74]. Ref. [70] describes two D-band PAs integrated in 22 nm fully depleted silicon-on-insulator (FDSOI) technology, aimed at achieving low DC-power consumption and high efficiency. Both PAs incorporate capacitive neutralization to boost gain and improve stability. The designs feature distinct matching networks: one employs a transformer-

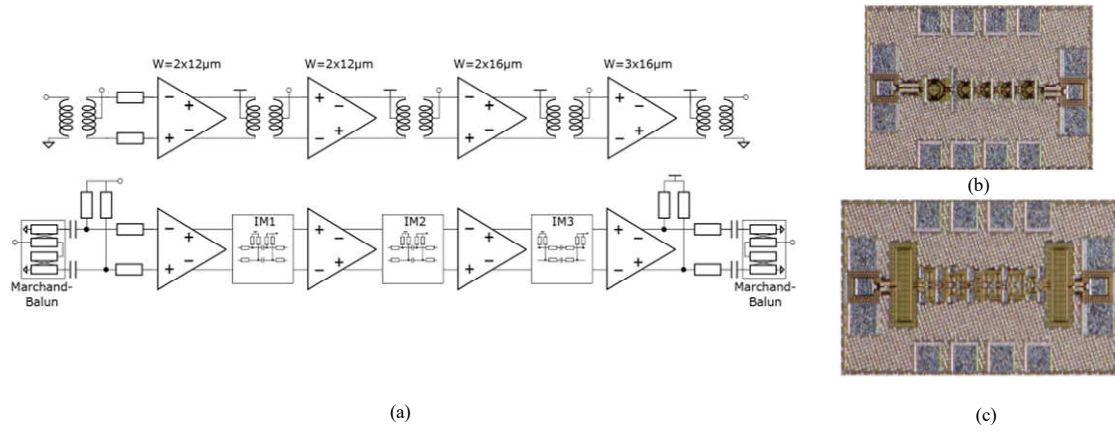


Fig. 2.22 (a) Simplified block diagram of TB-PA at the top and LB-PA at the bottom. Chip photographs of (b) TB-PA and (c) LB-PA [70].

based (TB) approach, while the other uses a line-based (LB) method, each presenting specific advantages and drawbacks. The circuit diagram and chip photograph are given in Fig. 2.22. Ref. [71] presents a solution to design challenges posed by transitioning to 16nm FinFET technology for D-band PAs. It addresses three fundamental limitations: increased parasitic capacitance and interconnect resistance, self-heating effects, and size constraints of PA power stages due to total input/output capacitance. The proposed design uses small transistors with a high-k sandwiched transformer for output matching, reducing performance degradation and improving heat dissipation. The PA employs a differential common-source neutralized amplifier with a two-way power-combining approach to enhance output power. Measurements indicate that the PA consistently achieves high gain and efficiency across a broad frequency spectrum. It surpasses the performance of other FinFET designs operating at double the frequency, positioning it as a highly promising solution for high-speed D-band communication systems. The circuit diagram and chip photograph are given in Fig. 2.23.

Ref. [72] presents a 2-way, 3-stage PA in 22nm FD-SOI technology designed for D-band applications. The PA employs an innovative dynamic bias scaling technique that

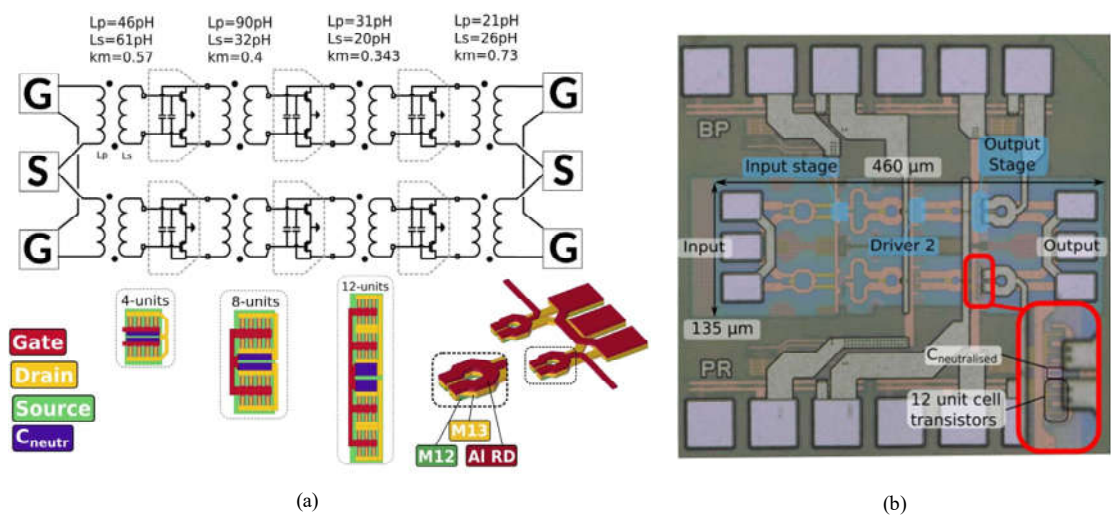


Fig. 2.23 (a) Circuit diagram of the 2-way, 3-stage power-combining PA, including the detailed layout of each stage and the output matching transformer. (b) Chip photograph [71].

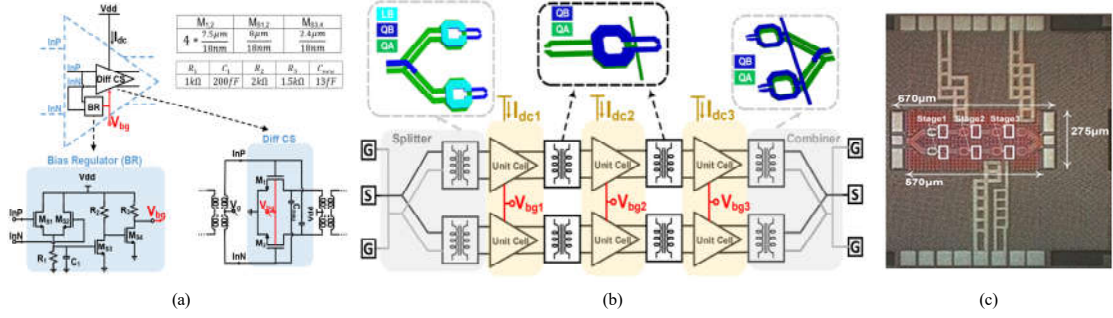


Fig. 2.24 (a) Unit cell of the PA. (b) Architecture and (c) Chip photograph [72].

uses the back-gate terminal in FD-SOI technology to adaptively optimize power consumption in response to varying input power levels, as depicted in Fig. 13. This method greatly improves power-added efficiency within the linear operating range. The circuit diagram and chip photograph are given in Fig. 2.24. Ref. [73] details the design of an F-band PA utilizing novel back-end-of-line (BEOL) techniques in Intel 16 FinFET technology. This PA employs skip-layer vias to directly connect transistors to thick metal layers, reducing parasitic capacitance and resistance, and thus enhancing performance. Fig. 2.25 (a) shows the 3D view of an assembled 4x1 neutralized transistor array. The circuit diagram and chip photograph are given in Fig. 2.25 (b) and (c).

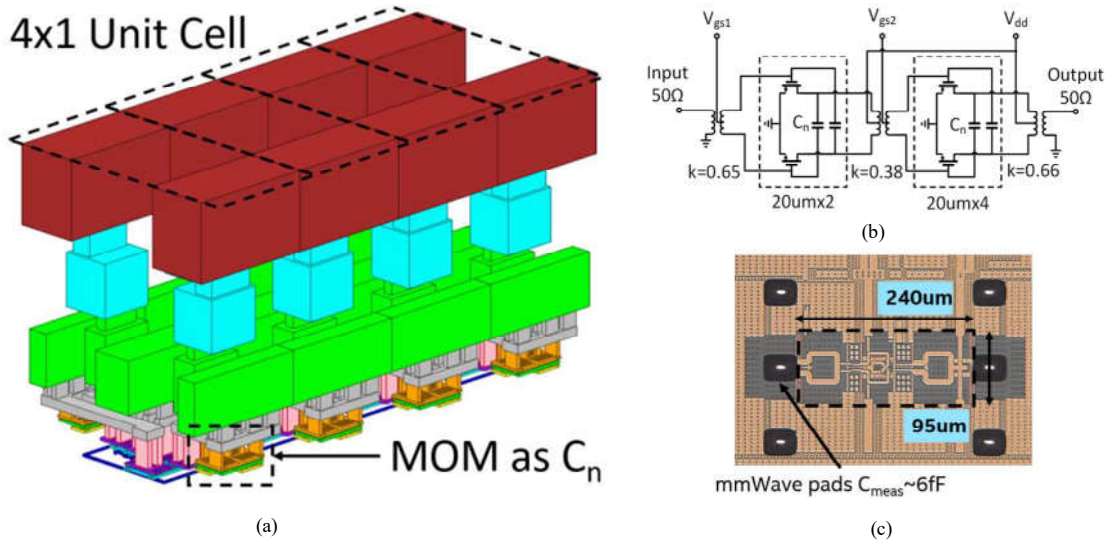


Fig. 2.25 (a) Neutralized transistor array in mmWave optimized BEOL. (b) Schematic and (c) photograph of the 2-stage PA [73].

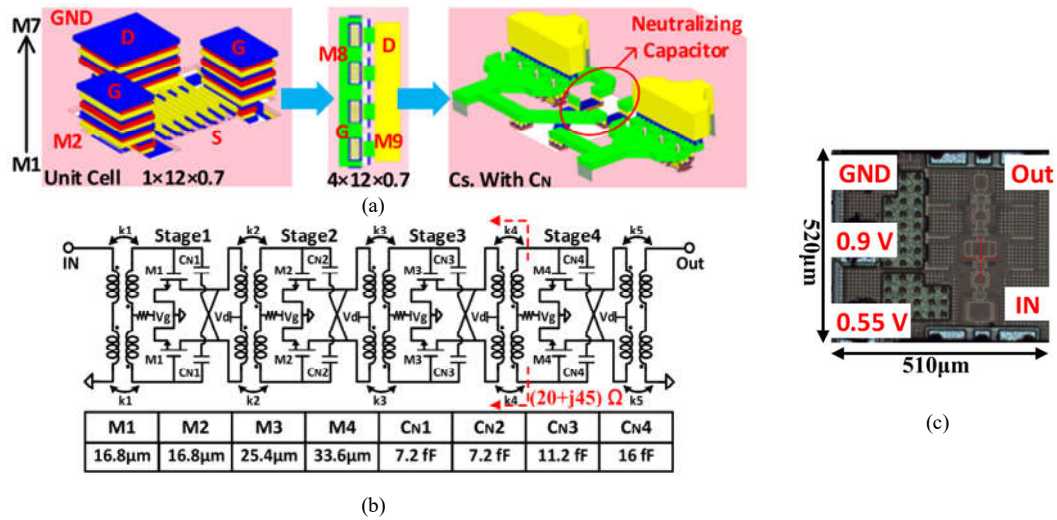


Fig. 2.26 (a) Layout of unit cell and output stage. (b) Schematic and (c) Die micrograph of the proposed PA [74].

Table 2.3 Comparison to prior art D band PA designs.

	[65]	[67]	[68]	[69]	[71]	[74]
Technology	45nm CMOS SOI	28nm CMOS	28nm FDSOI	40nm CMOS	16nm FinFET	28nm CMOS
Topology	8-Way C.S. (4-Way Diff.)	3-stage C.S. 2-Way Diff.	3-stage C.S. Diff.	Cross-coupled Diff.	2-Way C.S Diff.	4-stage C.S. 1-Way Diff.
Frequency (GHz)	140	138	130	144	135	140
Supply (V)	1/1.2	1	0.95	2	1	0.9
Power Gain	22.2/24	19.2	14.5	14.2	20.5	21.9 @160GHz
P _{SAT} (dBm)	16/17.5	15.4	0 ¹	5.7	15	9.5
P _{1dB} (dBm)	12.5/14.2	14.25	-2 ¹	1.9	9.2	4.6
Peak PAE	12.5/13.4	11.2%	NA	5.5%	12.8%	7.6%
Active Area (mm ²)	0.43	0.091	0.102	0.078	0.041	0.26
FoM*	92.2/95.7	88.9	-	-	89.2	-

*FoM = Gain [dB] + Psat [dBm] + 20*log (Fc (GHz)) + 10*log (peak PAE (%)).

Ref. [74] presents a four-stage differential PA in 28nm CMOS, focusing on achieving broadband performance and high efficiency. presents a four-stage differential common-source (CS) PA designed in 28-nm bulk CMOS technology. To enhance the PA's large-signal bandwidth and efficiency, the design optimizes the transistor size and layout, shown in Fig. 2.26 (a). Transformer-based matching networks are introduced to achieve wideband output matching and a multistage staggering scheme. The circuit diagram and chip photograph are given in Fig. 2.26 (b) and (c). The PA demonstrates the broadest large-signal bandwidth among D-band PAs fabricated in CMOS technology. The performance of the D-band PAs are listed in Table 2.3.

In conclusion, the advancements in D-band power amplifier design have significantly pushed the boundaries of what is achievable in terms of gain, efficiency, and bandwidth. These innovations are crucial for the development of next-generation wireless communication and radar systems. Key design points include enhancing gain through advanced embedding networks, improving efficiency with adaptive biasing, and increasing output power by power combining techniques. Future research should focus on addressing thermal management, improving linearity, and exploring scalable designs to further advance the field. The promising directions and solutions provided by these papers lay a solid foundation for ongoing and future developments in D-band power amplifier technology.

2.4. Summary

This chapter offers a comprehensive review of GaN device modeling and mmWave power amplifier design, emphasizing the evolution of modeling techniques from physical to empirical and ANN-based approaches. It underscores the significance of GaN HEMT devices in microwave and mmWave applications and discusses industry-standard models like Anglov and MVSG. The review also highlights the different characteristics in various ANN-based GaN HEMT models. Future research directions inferred from the review suggest a push towards hybrid modeling combines ANN and physical modelling for enhanced accuracy and scalability of the model.

Advancements in 60GHz, 77GHz, and D-Band PAs are examined, with a focus on topologies, linearization, and matching networks. Innovative techniques for boosting performance, such as embedding networks and adaptive biasing, are noted. These innovative technologies provide new ideas for PA design, including but not limited to new power combining technologies, more optimized matching structures or layout

designs with lower parasitics. The performance of start-of-art PAs for beyond 5G applications is summarized, providing a benchmark for future PA designs.

Chapter 3. A Hybrid GaN HEMT Model Merging Artificial Neural Networks and ASM-HEMT for Parameter Precision and Scalability

As mentioned in Chapter 1, GaN technology is at the forefront of semiconductor technology, particularly in microwave application. Their advantages are manifold, including power density, operation capabilities extending to millimeter-wave frequencies, and exceptional efficiency—attributes owed to their high electron mobility, elevated cutoff frequency, and minimized on-resistance and capacitance. Consequently, GaN device modeling is crucial in designing circuits as it accurately predicts device performance, allows for circuit simulation and optimization, and enables parameter extraction essential for accurate simulation and optimization. However, the complexity of the electrical behavior of GaN HEMT devices poses a challenge in accurately predicting their performance, necessitating a robust device model. To address this issue, ANN based GaN device modeling is a popular approach that uses machine learning techniques to create accurate models without the need for extensive physical knowledge. Though substantial advancements have been achieved in ANN-based modeling of GaN HEMTs, the field still confronts formidable challenges. A primary issue is the substantial data requirement for effective model training. Another significant hurdle is the development of more refined physical models that can serve as a foundation for training data generation. Although ANN models adeptly replicate device behavior, their lack of physical interpretability obscures the understanding of underlying physical principles. This gap has catalyzed the exploration of hybrid models combining ANN and physical modeling approach.

This chapter introduces an innovative hybrid physical model that leverages ANN to precisely characterize the surface potentials (ψ_s , ψ_d) of the GaN HEMT, which are the key parameters in the ASM-GaN-HEMT model [28, 31-33]. In addition, this article

employs parameter extraction and multi-objective particle swarm optimization (MOPSO) methodology designed for the hybrid model [75]. Moreover, this hybrid model exhibits enhanced scalability relative to traditional ANN-based models [76], as evidenced by its integration of dimensional parameters within the modeling process. Experimental validations demonstrate a strong concordance between the hybrid model's predictions and the empirical data across a range of tests, including current-voltage (IV) characteristics, S-parameters, and load-pull power sweeps. The proposed method significantly improves the accuracy of the S parameter compared to traditional models, reducing the large signal performance error to within 5%.

3.1. Working Principle

3.1.1. Description of in-house fabricated GaN HEMTs

In this section, we detail the structural and electrical characterization of AlN/GaN-on-Si HEMTs, shown in Fig. 3.1(a), (c) and (d), which combines a cross-sectional schematic and a Transmission Electron Microscopy (TEM) image of the fabricated device. Fabricated on a 6" high-resistivity ($>6000 \text{ } \Omega\cdot\text{cm}$) Si (111) substrate, the III-nitride materials were epitaxially grown via Metal-Organic Chemical Vapor Deposition (MOCVD). The epitaxial stack includes a $1.5 \text{ } \mu\text{m}$ GaN buffer, a 6 nm AlN barrier, and a 4 nm in-situ SiN cap layer, which together enable a 2-dimensional electron gas (2DEG) with a density of $2.06 \times 10^{13} \text{ cm}^{-2}$, electron mobility of $1060 \text{ cm}^2/\text{Vs}$, and a sheet resistance of $285 \text{ } \Omega/\square$, as derived from Hall measurements.

The device fabrication commenced with mesa isolation using Cl_2/BCl_3 plasma dry etching to achieve a mesa height of approximately 120 nm. Subsequent steps involved the formation of ohmic contacts by the deposition of a Ti/Al/Ni/Au metal stack with respective thicknesses of 20/120/40/50 nm, of 20/120/40/50 nm, and rapid thermal

potential-based framework, is designed for GaN HEMTs and adeptly evaluates the quasi-Fermi level as a function of bias, having met the rigorous benchmarks of the CMC standard. A key aspect of this model is the precise calculation of intrinsic capacitances. In this framework, the intrinsic gate (Q_{gi}) and drain (Q_{di}) charges are determined based on the surface potential at both ends of the channel (ψ_s, ψ_d).

The hybrid physical and ANN-based GaN model method proposed here is applied. In ASM-GaN-HEMT model, due to the difference in barrier thickness under the field plate, the V_{off} will be different from the intrinsic transistor, Since the GaN-on-Si HEMTs to be modeled in this paper are designed for low voltage 5G applications, there is no field plate in the structure, which will simplify the three equivalent transistors in ASM into one equivalent transistor in this section.

3.1.2. Extrinsic parameter extraction of the GaN HEMTs

From the analysis above, the equivalent circuit for in-house GaN on Si HEMT is shown in Fig 3.1 (b) [24]. And Fig. 3.2 presents the equivalent circuit for GaN HEMT on Si subtraction under pinch-off condition. To address the unique RF characteristics of the Si substrate, especially under low-frequency pinch-off conditions, an RC branch comprising parameters such as $C_{gg}, C_{dd}, R_{gg}, R_{dd}, C_{pg}, C_{pd}$ is integrated, From the diagram, the Y-parameters of this circuit can be listed as follow:

$$\begin{aligned} Y_{11} &= Y_{gg} + j\omega(C_{gs} + C_{gd}) \\ Y_{22} &= Y_{dd} + j\omega(C_{ds} + C_{gd}) \\ Y_{12} &= Y_{21} = -j\omega C_{gd} \end{aligned} \quad (3.1)$$

Where

$$\begin{aligned} Y_{gg} &= \frac{j\omega C_{pg}(1 + j\omega C_{gg} R_{gg})}{1 + j\omega R_{gg}(C_{pg} + C_{gg})} \\ Y_{dd} &= \frac{j\omega C_{pd}(1 + j\omega C_{dd} R_{dd})}{1 + j\omega R_{dd}(C_{pd} + C_{dd})} \end{aligned} \quad (3.2)$$

The values of the components are scanned with certain ranges to minimize the error

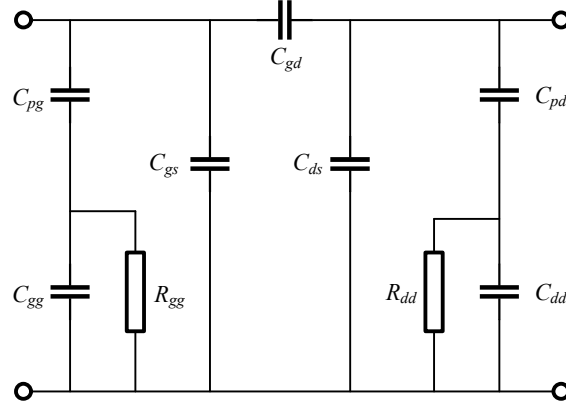


Fig. 3.2 Equivalent circuit under pinch off condition [24].

Table 3.1 Extracted Pad Parameters

Parameter	Value	Parameter	Value
C_{gp}	52.099 fF	C_{pd}	51.167 fF
C_{gg}	0 fF	C_{dd}	0 fF
R_{gg}	38.3115 Ω	R_{dd}	38.8598 Ω
C_{gs}	4.5774 fF	C_{ds}	4.3141 fF
C_{gd}	16.322 fF		

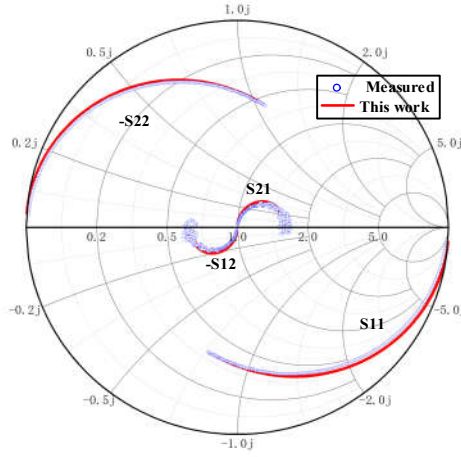


Fig. 3.3 Measured and simulated S-parameter results under pinch off condition ($V_{DS}=0V$, $V_{GS}=-5V$).

between the calculated results and measurement results. Table 3.1 illustrates the extracted pad parameters of GaN HEMT under pinch-off condition, Fig. 3.3 shows the measured and simulated S-parameters from 0.1 to 40 GHz under $V_{gs} = -5V$ and $V_{ds} = 0V$. Apparently, the measured results and simulated results are well matched, which verifies the correctness of the extracted pad parameters.

After removing the determined extrinsic capacitance networks from the measured data in Y-parameter format, the data is transformed into Z-parameter format. The

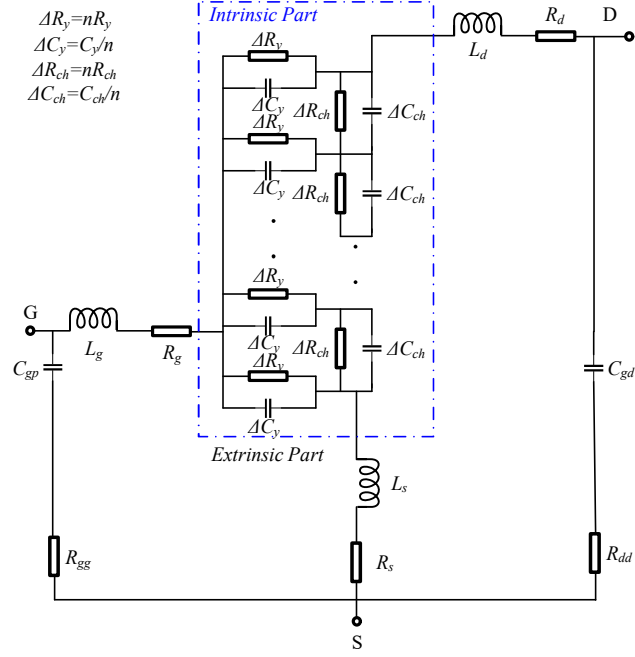


Fig. 3.4. Small-signal equivalent cold-FET circuit[77], [78].

extraction of extrinsic elements follows the methodology outlined in the cold-FET model by Jeon et al. [78], which utilizes a distributed approach for a precise representation of the intrinsic channel and barrier regions. This process is illustrated in the intrinsic section of Fig. 3.4.

Thus subtract the pad parameters (C_{pg} , R_{pg} , C_{pd} , R_{pd}), the Z-parameter of the instinct part can be expressed as

$$\begin{aligned}
 & \begin{bmatrix} S_{11,meas} & S_{12,meas} \\ S_{21,meas} & S_{22,meas} \end{bmatrix} \\
 & \Downarrow S \rightarrow Y \\
 & \begin{bmatrix} Y_{11,meas} - \frac{j\omega C_{pg}}{1 + j\omega C_{pg} R_{pg}} & Y_{12,meas} \\ Y_{21,meas} & Y_{22,meas} - \frac{j\omega C_{pd}}{1 + j\omega C_{pd} R_{pd}} \end{bmatrix} \\
 & \Downarrow Y \rightarrow Z \\
 & Z = \begin{bmatrix} \frac{R_s + R_g + j\omega(L_g + L_s) + \frac{R_{ch}}{3(1 + j\omega C_{ch} R_{ch})} + \frac{R_y}{1 + j\omega C_y R_y}}{R_s + j\omega L_s + \frac{\alpha R_{ch}}{1 + j\omega C_{ch} R_{ch}}} & \frac{R_s + j\omega L_s + \frac{\alpha R_{ch}}{1 + j\omega C_{ch} R_{ch}}}{R_d + R_s + j\omega(L_d + L_s) + \frac{R_{ch}}{1 + j\omega C_{ch} R_{ch}}} \\ \frac{R_s + j\omega L_s + \frac{\alpha R_{ch}}{1 + j\omega C_{ch} R_{ch}}}{R_d + R_s + j\omega(L_d + L_s) + \frac{R_{ch}}{1 + j\omega C_{ch} R_{ch}}} & \frac{R_d + R_s + j\omega(L_d + L_s) + \frac{R_{ch}}{1 + j\omega C_{ch} R_{ch}}}{R_s + j\omega L_s + \frac{\alpha R_{ch}}{1 + j\omega C_{ch} R_{ch}}} \end{bmatrix}
 \end{aligned} \tag{3.3}$$

Sweep the value of α from 0 to 1 and calculate the standard derivation of $\text{Re}(Z_{12}) - \alpha \text{Re}(Z_{22})$, then the value of α can be settled with the minimum standard

derivation. From (3.3) the real part of Z_{12} and Z_{22} can be written in the form of a polynomial as follows:

$$\begin{aligned} \text{Re}(Z_{12}) = \text{Re}(Z_{21}) &= a_1 + \frac{\alpha b}{1 + \omega^2 b^2 c^2} \\ \text{Re}(Z_{22}) &= a_2 + \frac{b}{1 + \omega^2 b^2 c^2} \end{aligned} \quad (3.4)$$

Where $a_1 = R_s$, $a_2 = R_d + R_s$, $b = R_{ch}$, $c = C_{ch}$.

By employing the polynomial fitting in MATLAB, the value of R_s , R_d , R_{ch} , C_{ch} can be obtained, Fig. 3.5 shows the results of polynomial fitting curve. In this case, $\alpha = 0.4951$, $R_s = 0 \Omega$, $R_d = 0.0528 \Omega$, $R_{ch} = 35.91 \Omega$, $C_{ch} = 85.785 \text{ fF}$. With these settled parameters, it will greatly simplify the optimization procedure in the next step.

From the equation (3.3), the initial value of the elements in the equivalent circuit can be given by:

$$\begin{aligned} Z_{11} &= R_s + R_g + j\omega(L_g + L_s) + \frac{R_{ch}}{3(1 + j\omega C_{ch} R_{ch})} + \frac{R_y}{1 + j\omega C_y R_y} \\ Z_{12} = Z_{21} &= R_s + j\omega L_s + \frac{0.4951 \cdot R_{ch}}{1 + j\omega C_{ch} R_{ch}} \\ Z_{22} &= R_d + R_s + j\omega(L_d + L_s) + \frac{R_{ch}}{1 + j\omega C_{ch} R_{ch}} \end{aligned} \quad (3.5)$$

$$\begin{aligned} L_d + L_s &\approx \frac{1}{\omega_H} \text{Im} \left(Z_{22} \Big|_{f_H} - \frac{R_{ch}}{1 + j\omega_H C_{ch} R_{ch}} \right) \\ R_s &\approx \text{Re} (Z_{12} \Big|_{f_H}) \\ L_s &\approx \frac{1}{\omega_H} \text{Im} \left(Z_{12} \Big|_{f_H} - \frac{\alpha R_{ch}}{(1 + j\omega_H C_{ch} R_{ch})} \right) \\ R_g + R_s &\approx \text{Re} (Z_{11} \Big|_{f_H}) \\ C_y &\approx -\frac{1}{\omega_L} \text{Im} \left(Z_{11} \Big|_{f_L} - \frac{R_{ch}}{3(1 + j\omega_H C_{ch} R_{ch})} \right)^{-1} \\ R_y &\approx \frac{1}{(\omega_L C_y)^2} \text{Re} \left(Z_{11} \Big|_{f_L} - \frac{R_{ch}}{3(1 + j\omega_H C_{ch} R_{ch})} \right)^{-1} \\ L_g + L_s &\approx \frac{1}{\omega_H} \text{Im} \left(Z_{11} \Big|_{f_H} - \frac{R_{ch}}{3(1 + j\omega_H C_{ch} R_{ch})} - \frac{R_y}{1 + j\omega C_y R_y} \right) \end{aligned} \quad (3.6)$$

The optimization criteria are defined through the following process. First, after performing the initial direct extraction, the device's S parameters are simulated using

the obtained equivalent circuit parameters (ECPs) via the inverse procedure outlined in step 4. The extraction error for each of the four elements of the S parameters, denoted as $\varepsilon_{ij}(S)$, is then computed as follows:

$$\varepsilon_{ij}(S) = \frac{1}{N} \sum_{n=1}^N \frac{|S_{ij_sim_n} - S_{ij_mea_n}|}{|S_{ij_mea_n}|} \quad (3.7)$$

Fig.3.6 compares the difference between measured and simulated S-parameter results, obviously the extracted parasitic parameters could well reflect the Cold-FET characteristic of GaN HEMT.

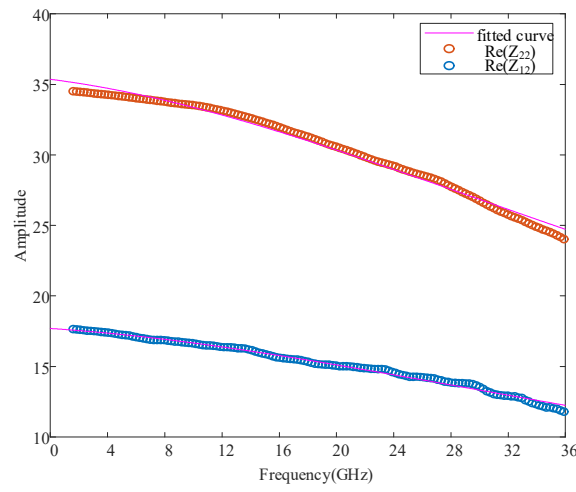


Fig. 3.5. Polynomial fitting results.

Table 3.2 Extracted Passive Components

Parameter	Value	Parameter	Value
L_g	11.92 pH	R_g	42 Ω
L_d	109.84 pH	R_d	0.3034 Ω
L_s	113.061 pH	R_s	3.524 Ω
C_{ch}	87.56 fF	R_{ch}	36.27 Ω
C_y	51.95 fF	R_y	3336.76 Ω

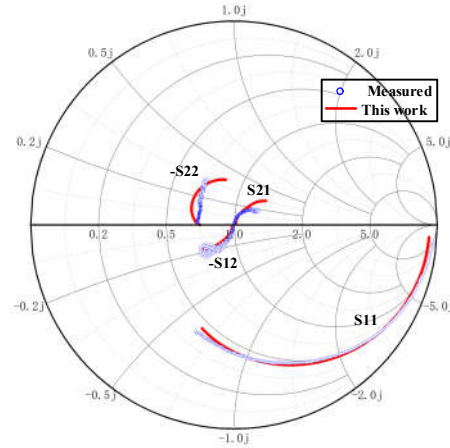


Fig. 3.6. Measured and simulated S-parameter results under cold-FET condition ($V_{DS}=V_{GS}=0V$).

3.1.3. Intrinsic parameter extraction of the GaN HEMTs

After obtaining the parasitic parameters from small-signal equivalent circuit, the intrinsic parameter could be derived from multi-bias S-Parameter measurement results, the intrinsic Y-parameter expression could be derived after the following steps:

Step 1: De-embed the pad parameter (C_{pg} , R_{gg} , C_{pd} , R_{dd}):

$$\begin{aligned} & \begin{bmatrix} S_{11,meas} & S_{12,meas} \\ S_{21,meas} & S_{22,meas} \end{bmatrix} \\ & \Downarrow S \rightarrow Y \\ & \begin{bmatrix} Y_{11,meas} - \frac{j\omega C_{pg}}{1 + j\omega C_{pg} R_{gg}} & Y_{12,meas} \\ Y_{21,meas} & Y_{22,meas} - \frac{j\omega C_{pd}}{1 + j\omega C_{pd} R_{dd}} \end{bmatrix} \end{aligned} \quad (3.8)$$

Step 2: De-embed the parasitic parameters (R_s , L_s , R_g , L_g , R_d , L_d):

$$\begin{aligned} & \Downarrow Y \rightarrow Z \\ & Z_{intr} = \begin{bmatrix} Z_{11} - R_s - R_g - j\omega(L_g + L_s) & Z_{12} - R_s - j\omega L_s \\ Z_{12} - R_s - j\omega L_s & Z_{22} - R_d - R_s - j\omega(L_d + L_s) \end{bmatrix} \\ & \Downarrow Z \rightarrow Y \\ & \begin{bmatrix} Y_{11,intr} & Y_{12,intr} \\ Y_{21,intr} & Y_{22,intr} \end{bmatrix} \end{aligned} \quad (3.9)$$

And then the intrinsic Y parameter could be expressed as:

$$Y_{intr_raw} = \begin{bmatrix} j\omega C_{gs} \| R_{gs}^{-1} + j\omega C_{gd} \| R_{gd}^{-1} + G_{gsf} + G_{gdf} & -j\omega C_{gd} \| R_{gd}^{-1} - G_{gdf} \\ g_m e^{-j\omega\tau} - j\omega C_{gd} \| R_{gd}^{-1} - G_{gdf} & G_{ds} + G_{gsf} + j\omega C_{ds} + j\omega C_{gd} \| R_{gd}^{-1} \end{bmatrix} \quad (3.10)$$

G_{gsf} and G_{gdf} could be extracted from the low frequency measurement results, where the intrinsic capacitor branch could be regarded as open circuit, then

$$\begin{aligned} G_{gsf} &= \text{Re}(Y_{11}^{intr_raw} + Y_{12}^{intr_raw}) \\ G_{gdf} &= -\text{Re}(Y_{12}^{intr_raw}) \end{aligned} \quad (3.11)$$

The Y-parameter of the rest elements after de-embedding G_{gsf} and G_{gdf} could be expressed as:

$$Y_{intr} = \begin{bmatrix} j\omega C_{gs} \| R_{gs}^{-1} + j\omega C_{gd} \| R_{gd}^{-1} & -j\omega C_{gd} \| R_{gd}^{-1} - G_{gdf} \\ g_m e^{-j\omega\tau} - j\omega C_{gd} \| R_{gd}^{-1} & G_{ds} + j\omega C_{ds} + j\omega C_{gd} \| R_{gd}^{-1} \end{bmatrix} \quad (3.12)$$

From (3.13), the value of each component could be illustrated as follow:

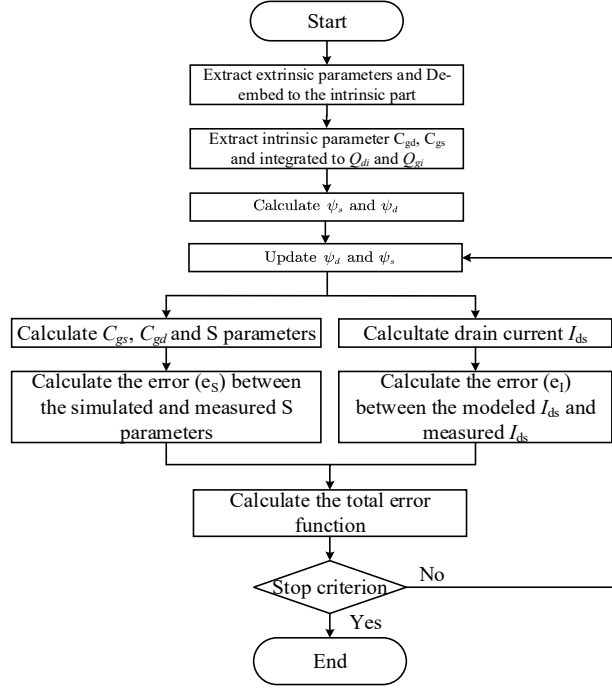


Fig. 3.7 Optimization flowchart of ψ_s and ψ_d .

$$\begin{aligned}
 R_{gs} &= \text{Re} \left(\frac{1}{Y_{11}^{intr} + Y_{12}^{intr}} \right) \\
 R_{ds} &= \frac{1}{\text{Re}(Y_{12}^{intr} + Y_{22}^{intr})} \\
 C_{gs} &= - \frac{1}{\omega \text{Im} \left(\frac{1}{Y_{11}^{intr} + Y_{12}^{intr}} \right)} \\
 R_{gd} &= - \text{Re} \left(\frac{1}{Y_{12}^{intr}} \right) \\
 C_{gd} &= - \frac{1}{\omega \text{Im} \left(\frac{1}{Y_{12}^{intr}} \right)} \\
 C_{ds} &= \frac{\text{Im}(Y_{12}^{intr} + Y_{22}^{intr})}{\omega} \\
 g_m &= \left| \frac{(Y_{11}^{intr} + Y_{12}^{intr})(Y_{21}^{intr} - Y_{12}^{intr})}{\text{Im}(Y_{11}^{intr} + Y_{12}^{intr})} \right| \\
 \tau &= - \frac{1}{\omega} \text{phase} \left\{ (Y_{21}^{intr} - Y_{12}^{intr}) \left[1 + j \frac{\text{Re}(Y_{11}^{intr} + Y_{12}^{intr})}{\text{Im}(Y_{11}^{intr} + Y_{12}^{intr})} \right] \right\}
 \end{aligned} \tag{3.13}$$

It is imperative to acknowledge that the intrinsic capacitances within the GaN HEMT model, specifically C_{gs} , C_{gd} , C_{ds} , exhibit variations in response to changes in the extrinsic voltages V_{GS} and V_{DS} . To accurately derive the intrinsic charge model and the nonlinear drain-source current model, a crucial step involves the elimination of the

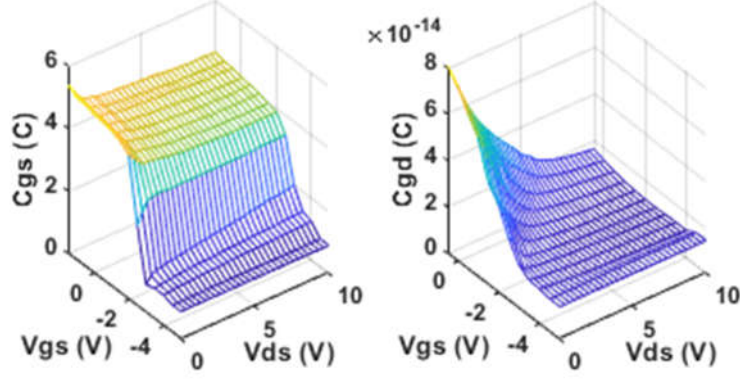


Fig. 3.8 The derived C_{gd} and C_{gs} values under different bias conditions.

voltage drops across the parasitic resistances, namely R_g , R_d and R_s from the extrinsic voltages V_{GS} and V_{DS} . This adjustment is essential to accurately determine the intrinsic voltages, V_{gs} and V_{ds} . This expression listed below plays a pivotal role in ensuring that the model accurately reflects the intrinsic electrical characteristics of the GaN HEMT.

$$\begin{bmatrix} V_{gs} \\ V_{ds} \end{bmatrix} = \begin{bmatrix} V_{GS} \\ V_{DS} \end{bmatrix} - \begin{bmatrix} R_g + R_s & R_s \\ R_s & R_d + R_s \end{bmatrix} \begin{bmatrix} I_{gs} \\ I_{ds} \end{bmatrix} \quad (3.14)$$

Numerical integration of the intrinsic capacitance C_{gs} and C_{gd} from (3.15) as a function of the intrinsic voltage enables the derivation of charge expression.

$$\begin{aligned} Q_{gs}(V_{gs}, V_{gd}) &= \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{gd})} C_{gs} dV_{gs} \\ Q_{gd}(V_{gs}, V_{gd}) &= \int_{(V_{gs0}, V_{ds0})}^{(V_{gs}, V_{gd})} C_{gd} dV_{gd} \end{aligned} \quad (3.15)$$

In alignment with the ASM-GaN-HEMT model description and reflecting the specific characteristics of our in-house GaN HEMT, the expressions for intrinsic gate charge (Q_{gi}) and drain (Q_{di}) charges are as follows [28].

$$\begin{aligned} Q_{gi} &= WLC_g \left\{ V_{go} - \frac{1}{2}(\psi_s + \psi_d) + \frac{1}{12} \frac{(\psi_d - \psi_s)^2}{V_{goT}} \right\} \\ Q_{di} &= -\frac{1}{2} WLC_g \left\{ V_{go} - \frac{1}{3}(\psi_s + 2\psi_d) + \right. \\ &\quad \left. \frac{1}{12} \frac{V_{DS}^2}{V_{goT}} \left(1 + \frac{1}{10} \frac{V_{DS}}{V_{goT}} \right) + \frac{V_{DS}^3}{120V_{goT}^2} \right\} \end{aligned} \quad (3.16)$$

where W and L means the gate width and length of the GaN HEMT, C_g denotes the

gate capacitance per unit area, $C_g = \frac{\epsilon}{d}$. V_{go} symbolizes the gate override voltage

$V_{GS} - V_{off}$, and the expression of V_{goT} is given below, and K_B is the Boltzmann constant.

$$V_{goT} = V_{go} + \frac{K_B T}{q} - \frac{1}{2}(\psi_s + \psi_d) \quad (3.17)$$

MATLAB is employed to compute the surface potentials ψ_s and ψ_d using the equations (3.17). Yet, these initially calculated values require fine-tuning to negate influences from non-ideal factors such as instrumental errors or interference. In adherence to the ASM-GaN-HEMT model's theoretical framework, the conditions that $\psi_s = E_F$ and $\psi_d = E_F + V_{ds}$, must be satisfied, ensuring ψ_d exceeds ψ_s whenever V_{ds} is positive. The refined values of ψ_s and ψ_d should comply with these rules, signifying their critical role within the ASM-GaN-HEMT model by impacting several device characteristics. The surface potential dictates the drain current by modulating the transconductance g_m and influences the high-frequency response through its effects on intrinsic capacitances. This article seeks to establish precise models for both DCIV and RF performance of GaN HEMTs, utilizing ANNs. Therefore, as shown in Fig. 3.7, the value of ψ_s is derived from the intrinsic gate and drain charges. ψ_d is then computed by incrementing ψ_s by the V_{DS} , aligning the model with the applied bias conditions. Subsequently, two parallel streams of calculations proceed.

The first stream involves the computation of gate-to-source (C_{gs}) and gate-to-drain (C_{gd}) capacitances, key parameters that affect the transistor's frequency response. Following this, the S-parameters are obtained, which are essential for characterizing the high-frequency behavior of the device. An error metric (es) is then calculated by quantifying the deviation between the simulated S-parameters and the empirical S-parameters obtained from measurements, the calculation equation is same with (3.8).

Concurrently, the second stream addresses the direct current characteristics by

obtaining the I_{ds} from the model. The value of I_{ds} could be calculated using the physical equations (3.22) given in Section 3.1.4.1. The error (e_I) in this stream is defined by

$$e_I = \frac{1}{N} \sum_{n=1}^N (I_{ds,meas}^{(n)} - I_{ds,sim}^{(n)})^2 \quad (3.18)$$

where N is the total number of bias points, $I_{ds,meas}^{(n)}$ is the measured drain current at the n^{th} bias point, $I_{ds,sim}^{(n)}$ is the simulated or modeled drain current at the same condition. e_I and e_S from the parallel streams are then amalgamated to formulate a total error function, $e_{total} = w_I e_I + w_S e_S$. w_I and w_S are the weights of e_I and e_S , both are 0.5 in this paper. This composite error function serves as an indicator of the overall discrepancy between the model's predictions and the measured data across both frequency-dependent and static operational regimes. The iterative cycle involves updating ψ_s and ψ_d to minimize the total error function, refining the model with each iteration. This process is repeated until a predefined stopping criterion is satisfied. Such a criterion could be a minimal threshold for the error function or a maximum number of iterations, ensuring convergence to an optimal solution within practical computational limits.

Based on the principles of the particle swarm optimization (PSO) algorithm, the MOPSO [75] is a nature-inspired metaheuristic algorithm used to solve multi-objective optimization problems, which has many advantages, such as diversity preservation, efficient exploration. Like PSO, particles in MOPSO adjust their positions based on their own best position found so far and the global best position found by the entire swarm. These updates aim to guide the search toward better solutions in the multi-objective space. In multi-objective optimization, the goal is to find a set of solutions that represent a trade-off between different objectives, forming a Pareto front. In this work, MOPSO is employed to optimize the value of ψ_s and ψ_d for global accuracy. The optimization is carried out in Matlab. Then, the ANN-based ψ_s and ψ_d model is

illustrated in Section 3.1.4.

3.1.4. Nonlinear effects modeling of the GaN HEMTs

In this section, a neural network architecture featuring two hidden layers is utilized to encapsulate the nonlinear interdependencies between the surface potential ψ_s , ψ_d and the intrinsic voltages V_{ds} , V_{gs} . This approach diverges from the conventional lookup table-based large-signal models, where intrinsic voltages are discretized at uniformly distributed intervals. Due to the non-uniform spacing of the intrinsic voltages in this context, interpolation methods are necessitated to facilitate the rasterization of V_{gs} and V_{ds} . In contrast, when leveraging ANNs for the modeling of large-signal behaviors, it becomes feasible to train the model directly using the intrinsic voltages V_{gs} and V_{ds} , thereby obviating the need for rasterization. The ANNs inherently select either a sigmoid or a linear activation function, which ensures the preservation of data continuity and the retention of higher-order differentiability within the model. The ANNs inherently select either a sigmoid or a linear activation function, which ensures the preservation of data continuity and the retention of higher-order differentiability within the model. Consequently, the formulations for the ANN-based ψ_s and ψ_d are posited as follows, integrating the considerations to provide a robust framework for the predictive simulation of transistor characteristics.

The tanh function is selected due to its effectiveness in modeling non-linearities and its smooth, bounded output, which helps stabilize the training process. The tanh function is known to provide better performance compared to other activation functions like the sigmoid, especially when dealing with both positive and negative values. This property makes tanh particularly useful for this application, as it allows for more symmetric output scaling, which was necessary for accurately capturing the variations in our

dataset. Moreover, the tanh function has been widely adopted in similar non-linear modeling tasks because of its ability to approximate complex behaviors while maintaining smoothness and differentiability, making it an ideal candidate for the proposed neural network model [34, 79].

It is well-established that neural networks with one or more hidden layers are effective at capturing complex, non-linear relationships between input and output variables. We opted for two hidden layers in this case because, for the specific complexity of the dataset and the target application, this architecture provides an adequate balance between model accuracy and computational efficiency. While a single hidden layer can model non-linear relationships, multiple hidden layers enable the network to learn hierarchical features more effectively, which improves its ability to model complex functions. This configuration utilizes a backpropagation (BP) neural network with dual hidden layers [79-81]. Therefore, the functional representation of ψ_s and ψ_d as a response to V_{gs} and V_{ds} could be articulated as follows.

$$\psi_k(V_{gs}, V_{ds}) = b_3 + \sum_{i=1}^M w_{3i} \tanh(\varphi_{2i}) \quad (3.19)$$

Where φ_{2i} is defined by

$$\varphi_{2i} = b_{2i} + \sum_{j=1}^N w_{2ij} \tanh(\varphi_{1j}) \quad (3.20)$$

Where φ_{1j} is specified by

$$\varphi_{1j} = b_{1j} + w_{1j1} V_{gs} + w_{1j2} V_{ds} \quad (3.21)$$

Here, φ_{2i} and φ_{1j} are the output function of the second and the first hidden layer, respectively. Specifically, we trained and evaluated three different configurations of the neural network: (7, 5), (9, 7), and (11, 9). The training time for each configuration and the corresponding Mean Squared Error (MSE) are provided in Table 3.3. The (7, 5) configuration required 3.6 seconds, (9, 7) took 4.2 seconds, and (11, 9) took 5.4 seconds.

As demonstrated, increasing the number of neurons improves the fitting performance but also increases the computational time.

However, selecting too many neurons can significantly increase the complexity of the system, extend the simulation time on the ADS platform, and lead to overfitting. After considering the trade-off between model complexity and fitting performance, we determined that the (9, 7) configuration offers the best balance between these factors. This selection allows for improved accuracy while maintaining reasonable computational efficiency. The notations w and b signify the weights and biases of the neurons within the hidden layers and the output layer, respectively. A total of 714 observations are employed, of which 70% were allocated to the training set 15% to the validation set and 15% to the testing set. This split ensured that the model was trained on enough data while also maintaining a robust validation process to evaluate its performance. The data was initially cleaned by removing any outliers or missing values to ensure data integrity. Afterward, normalization was applied to rescale the input features to a range between [0, 1], which is a common practice to improve neural network performance. The convergence criterion of the neural network is based on the minimization of the MSE on the validation set. The training process was set to run for a maximum of 10000 epochs, but early stopping was employed to prevent overfitting. The metric was the MSE for both the training and validation sets, providing a measure of the model's accuracy [79-81]. The technique employed here constructs a nonlinear connection between the surface potential and bias voltages, noting that the ANN model does not convey any direct physical meaning but rather serves as a computational tool for simulation and prediction. To make the trained ANN model conform to some physical rules of the surface potential model, such as the ψ_s and ψ_d will increase with the increasing V_{gs} , the ANN need to be trained multiple times and carefully selected.

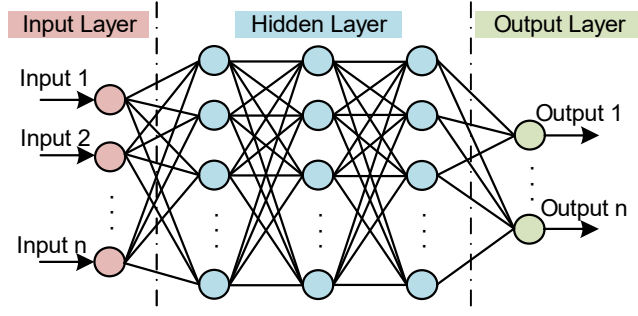


Fig. 3.9 Two hidden layers ANN framework for ψ_s and ψ_d model.

Table 3.3 Comparison of training time and MSE for different neural network configurations

Neuron numbers	Computational Time	MSE
7,5	3.58s	0.0551
9,7	4.23s	0.0275
11,9	5.4s	0.0159

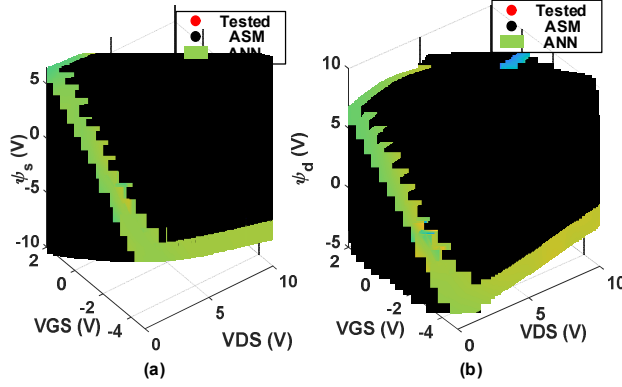


Fig. 3.10. ASM-based (black dots) and ANN-based (surface) results of (a) ψ_s and (b) ψ_d . VDS ranges from 0 to 10 V and VGS from -5.0 to 1.5 V.

Fig. 3.10 shows the extracted and optimized ψ_s and ψ_d results in different bias conditions. V_{gs} is selected from -5 to 1.5 V and V_{ds} is selected from 0 to 10 V.

3.1.4.1 Drain Current Modeling

Within the framework of the ASM-GaN HEMT model, the drain current I_{ds} is expressed by the following equation.

$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1 + \theta_{sat}^2 V_{ds}^2}} \frac{W}{L} C_g N_f V_{goT} V_{ds} (1 + \lambda V_{ds}) \quad (3.22)$$

Where μ_{eff} symbolizes effective mobility, and θ_{sat} is a fitting parameter. N_f represents the number of fingers, and λ signifies the channel length modulation coefficient.

The effective mobility μ_{eff} is further described by the relation.

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + UA \cdot E_{\text{avg}} + UB \cdot E_{\text{avg}}^2} \quad (3.23)$$

where E_{avg} is the average vertical electric field computed as

$$E_{\text{avg}} = \frac{V_{\text{gs}} - \psi_{\text{m}}}{T_{\text{bar}}} \quad (3.24)$$

In this context, UA and UB are parameters from the ASM-HEMT model, with typical values being in the order of 10^{-9} and 10^{-18} , respectively. E_{avg} denotes the average vertical electric field and ψ_{m} is the average surface-potential which is obtained by averaging the surface potential at the source and the drain ends of the channel. T_{bar} is the barrier layer thickness.

3.1.4.2 Nonlinear effects Modeling

In GaN HEMTs, two critical nonlinear phenomena, self-heating and trapping effects, are observed. These effects are instrumental in influencing the operational stability and efficiency of the devices. The self-heating effect is caused by the power dissipation within the device, leading to a temperature rise that affects the electrical characteristics. The trapping effect, on the other hand, refers to the capture of charge carriers in the gate area, modifying the threshold voltage and, consequently, the drain current.

Self-heating refers to the thermal elevation within the transistor structure due to power dissipation, which can lead to a degradation of electron mobility and a shift in device characteristics. To capture this phenomenon, an RC network comprising a thermal resistance (R_{th}) and a thermal capacitance (C_{th}) is employed. The equations are listed below.

$$\begin{aligned} i_{\text{DS}} &= I_{\text{ds}} \times (1 + K_{\text{T}} \Delta T) \\ K_{\text{T}} &= \alpha_0 + \alpha_1 [1 + \tanh(\alpha_2 + \alpha_3 V_{\text{ds}})] \\ T &= T_{\text{ref}} + \Delta T, \quad \Delta T = P_{\text{diss}} R_{\text{th}} + T_{\text{amb}} - T_{\text{ref}} \\ \tau_{\text{th}} &= R_{\text{th}} C_{\text{th}} \end{aligned} \quad (3.25)$$

The self-heating effect is represented by modifying the drain current I_{ds} with a factor (K_{T}), and α_0 , α_1 , α_2 and α_3 are fitting parameters. This configuration accounts for the temporal evolution of the device temperature due to power dissipation. The elevation in

temperature at the thermal node is quantified by a temperature increase (ΔT), which is superimposed on a predefined reference temperature, $T_{\text{ref}} = 25^\circ\text{C}$. The product of R_{th} and C_{th} defines the thermal time constant τ_{th} , which dictates the rate of thermal transients within the device. C_{th} is selected to establish a thermal time constant of approximately 0.1ms, ensuring that the model captures the rapid thermal dynamics characteristic of GaN HEMTs.

The trapping effect in GaN HEMTs, which involves charge carriers getting caught in defects, presents a significant design challenge by altering device performance, causing issues like threshold voltage shifts and current collapse. To measure this effect and obtain accurate device characteristics, pulsed I-V testing is employed. This method applies voltage pulses to minimize self-heating and avoid the impact of charge trapping, offering a clearer view of the transistor's behavior. As shown in the provided graph, Fig. 3.11(a) shows a DC I-V test where the voltage (V_{ds}) steadily increases over time and the drain current (I_{d}) decreases accordingly. The inserted window shows a specific voltage pulse and its width (t_{sw}). Fig. 3.11(b) shows the pulsed I-V (PIV) test. Here, the V_{ds} voltage is applied in pulses with an off time (t_{off}) between each pulse to allow the device to cool down and reduce the effects of charge trapping. The inset detail shows the duration (t_{on}) and off time (t_{off}) of a voltage pulse. Pulsed I-V testing contrasts with DC I-V testing by using a series of voltage pulses and observing the corresponding current response, which avoids the steady-state conditions that can mask the true performance of the GaN HEMT due to thermal effects and charge trapping. This technique is essential for developing models that predict device behavior and ensure the reliability of GaN HEMTs in high-frequency, high-power applications.

The trapping effects are quantitatively accounted for by incorporating two resistive-capacitive (RC) subcircuits, shown in Fig. 3.12. These subcircuits are designed to emulate

the alterations in the gate- source voltage induced by the trapping effects within both the surface states and the subsurface buffer layer [35].

$$\begin{aligned}
 V_{GS_eff} &= V_{gs} + \gamma_{surf} + \gamma_{subs} \\
 \gamma_{surf} &= k_{g1} (V_{gs} - V_{gsq0}) (V_{gsq} - V_{gsq0}) \\
 \gamma_{subs} &= \begin{cases} \tanh(k_{g2} (V_{ds} - V_{dsq}) (V_{gs} - V_{gsq1})) \\ + k_{g3} V_{dsq} (V_{gs} - V_{gsq2}), & V_{ds} \leq V_{dsq} \\ k_{g3} V_{dsq} (V_{gs} - V_{gsq2}), & V_{ds} > V_{dsq} \end{cases} \quad (3.26)
 \end{aligned}$$

The effective gate-source voltage V_{GS_eff} is formulated by adjusting V_{gs} with two terms γ_{surf} and γ_{sub} , which represent the surface and buffer-related trapping effects, respectively. The fitting parameters k_{g1} , k_{g2} and k_{g3} are calibrated to encapsulate the complex dynamics of charge trapping and de- trapping, which are instrumental in the accurate prediction of the device's transient and steady-state responses. The quiescent voltages V_{gsq0} , V_{gsq1} and V_{gsq2} serve as the reference points for these trapping-induced potential shifts. Through this meticulous formulation, the model aspires to closely replicate the GaN HEMT's performance characteristics, accounting for the nuanced interplay between electrical operation and the trapping mechanisms intrinsic to the device architecture.

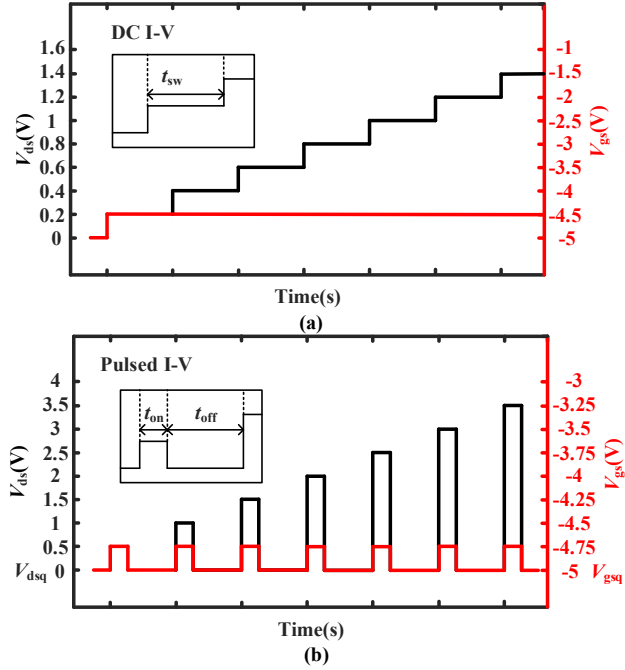


Fig. 3.11. Diagram of (a) DC IV, $V_{DS} = 0-10$ V in 0.2V step and $V_{GS} = -5.0$ to 1.5 V in 0.5V step (b) Pulsed IV, $V_{dsq} = 0$ V, $V_{gsq} = -5$, $V_{DS} = 0-10$ V in 0.5V step and $V_{GS} = -5.0$ to 1.5 V in 0.25V step.

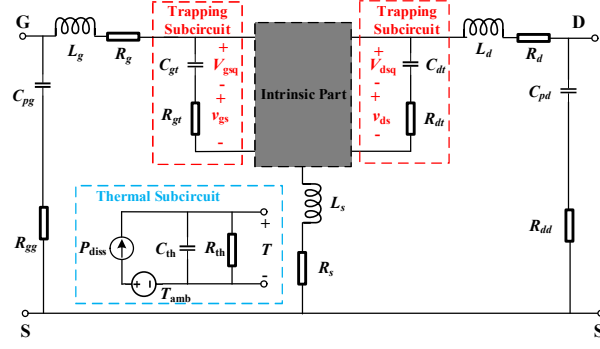


Fig. 3.12. Large signal equivalent circuit for GaN HEMTs with thermal and trapping subcircuits [35].

3.1.4.3 Gate Current Modeling

The gate currents I_{gs} and I_{gd} epitomize the behavioral characteristics of the Schottky contacts present in the device architecture. These currents can be accurately modeled by either utilizing an artificial neural network that captures the nonlinearities associated with the Schottky barrier or by employing a traditional Schottky diode model equation. The latter is mathematically represented as [82].

$$\begin{aligned} I_{gs} &= I_{sgs} \left(e^{\frac{qV_{gs}}{kTN_{gs}}} - 1 \right) \\ I_{gd} &= I_{sgd} \left(e^{\frac{qV_{gd}}{kTN_{gd}}} - 1 \right) \end{aligned} \quad (3.27)$$

Where q is the charge of an electron, k is the Boltzmann constant, T is the absolute temperature, and N_{gs} and N_{gd} are the ideality factors of the gate-source and gate-drain Schottky diodes, respectively. I_{sgs} and I_{sgd} are the saturation currents for the gate-source and gate-drain junctions, respectively, and serve as fitting parameters to align the model with empirical observations.

These expressions are instrumental in defining the gate leakage behavior under different biasing conditions and are crucial for the prediction of the off-state leakage currents in GaN HEMT devices. The accurate estimation of these currents is paramount for the assessment of device reliability and the optimization of its performance, particularly in high-frequency and high-power applications where Schottky barriers play

a vital role in the overall device behavior.

3.2. Experimental results and Model verification

In this paper, a comprehensive suite of experimental evaluations, namely DCIV, Pulsed I-V, and load-pull measurements—were conducted on two in-house fabricated GaN HEMT devices. The objective of these experimental analyses was to substantiate the precision and scalability of the advanced model delineated herein. The two GaN HEMT devices both use in-situ technology with 100-nm gate length and 100- μm total gate width (2 fingers $\times$ 50 μm), 200- μm total gate width (2 fingers $\times$ 100 μm), respectively. Employing the outcomes from these experimental evaluations and the proposed modeling technique, a novel GaN HEMT model was constructed within the ADS by employing symbolically defined device. For comparative purposes, the conventional ASM-GaN-HEMT model was also instantiated to predict upon the empirical data. Notwithstanding the differences in handling of ψ_s and ψ_d both models-maintained congruity in other aspects, encompassing the extraction of direct current parameters and the modeling of both self-heating and trapping effects. To corroborate the fidelity of the self-heating and trapping effect representations within the proposed model, DCIV characterizations were performed under varied temperature conditions, alongside PIV characterizations under diverse non-zero quiescent bias states. Fig. 3.13 illustrates the platform utilized for testing the DC IV and the pulsed IV characteristics of the device. Enclosed within the orange frame, the Accent Diva 265 is employed for Pulse IV testing, featuring a pulse period of 1 ms, a pulse length of 0.2 μs , and a duty cycle of 0.02%. Within the blue frame, the Kesight B1505A is used for DC IV testing, with V_{DS} settings ranging from 0 to 10 V in 0.2 V steps and V_{GS} settings from -5.0 to 1.5 V in 0.5 V steps. Additionally, temperature-dependent DC IV tests were conducted

using the ERS AirCoolPlus SP72-300-T at three distinct temperatures: 25°C, 65°C, and 100°C. Fig 3.14(a) and (b) illustrate measured versus modeled DCIV responses at disparate temperatures for the GaN HEMT with $2 \times 50 \mu\text{m}$ gate width, thereby affirming the accuracy of the self-heating model. Fig 3.14(c) demonstrates the alignment of measured and simulated PIV characteristics, which was influenced by different quiescent drain-source and gate-source voltages, indicating a satisfactory model of the

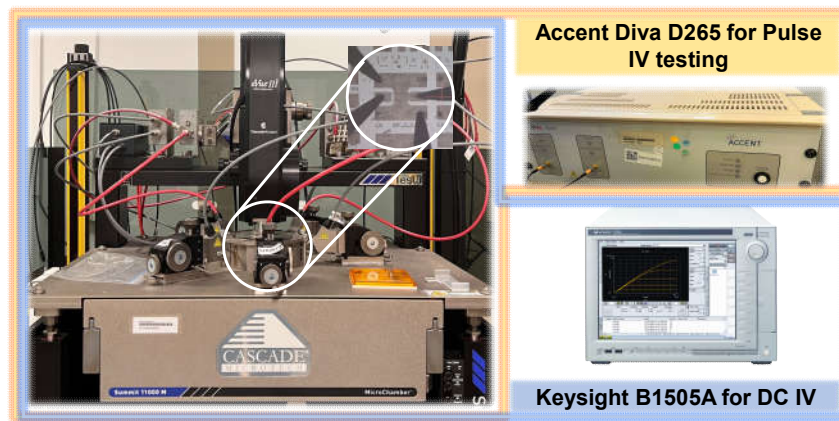


Fig. 3.13. (a) Pulsed IV testing an DC IV testing platforms.

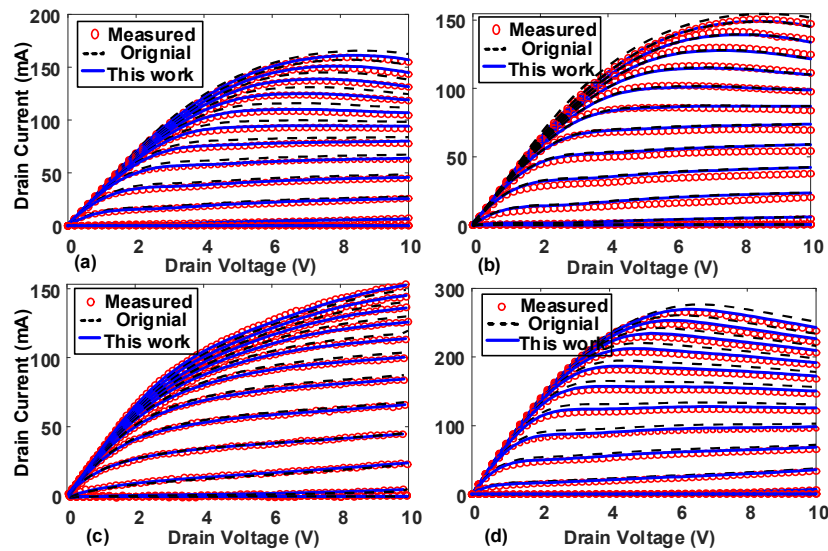


Fig. 3.14. Measured (red symbols), ASM model simulated (black dashed lines) and hybrid model simulated (blue lines) IV characteristics of (a) $2 \times 50 \mu\text{m}$ device, DCIV at 25°C, (b) $2 \times 50 \mu\text{m}$ device, DCIV at 65°C, (c) $2 \times 50 \mu\text{m}$ device, PIV testing, $V_{\text{dsq}} = -5 \text{ V}$, $V_{\text{gsq}} = 10 \text{ V}$, (d) $2 \times 100 \mu\text{m}$ device, DCIV at 25°C.

trapping effects. Fig 3.14(d) contrasts the measured and modeled DCIV curves for the GaN HEMT with a $2 \times 100 \mu\text{m}$ gate width, validating the model's scalability. Subsequently, Fig. 3.14 also shows the outcomes of the ASM-GaN-HEMT model with those of the proposed hybrid physical model, with the latter exhibiting marginally superior congruence with empirical data. Fig. 3.15 shows the gate current simulated and measured results.

To substantiate the large-signal model delineated in this section, a comprehensive load-pull characterization spanning the frequency range of 10 to 67 GHz was executed to assess the performance attributes of the GaN-based device. Fig. 3.16 provides a visual depiction and schematic layout of the load-pull testbed. The apparatus integrates the Cascade Elite 300 probe station as its foundational platform, harnessing a Keysight PNA-X N5247B network analyzer for signal generation, complemented by a Keysight B1500A unit supplying DC power for gate and source biasing. The system incorporates

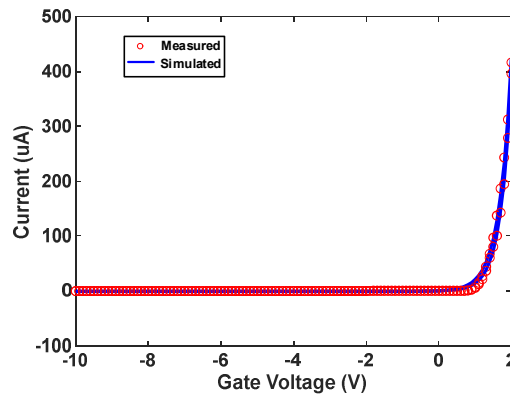


Fig. 3.15. The measured (red symbols) and simulated (blue line) gate current of the $2 \times 50 \mu\text{m}$ device.

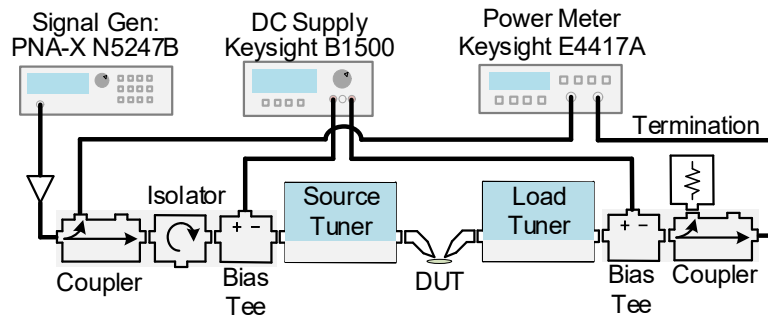


Fig. 3.16. Structure diagram of Load pull system.

a wideband coaxial programmable impedance tuner, specifically the iCCMT-67100 from Focus Microwave, facilitating load and source tuning across the specified frequency spectrum. Power measurements were executed using a dual-channel power meter, the Keysight E4417A. The load-pull configuration further includes ancillary components such as input preamplifiers, couplers, and bias Tees, among others.

Fig. 3.17 shows both the measured and simulated small-signal S-parameters for the two disparate GaN HEMT devices, revealing a strong concordance between simulation and measurement across a frequency range from 0.1 GHz to 40 GHz. Due to the bandwidth constraints of the coupler and isolator, which operate within the 26.5 GHz to 40 GHz range, this study presents large-signal test results exclusively at 28 GHz. Consequently, measurement and comparative analysis for harmonic and intermodulation distortion could not be conducted. Fig. 3.18 and 3.19 present the measured and simulated contours of the output power and PAE derived from the load-pull analysis. These contours were acquired for two GaN HEMT devices with varying geometries, which are pertinent to 5G communication technologies. In Fig. 3.18, the optimal matching impedance is $0.409 \angle 68^\circ$ in simulation, compared to $0.433 \angle 66.4^\circ$ as observed in measurement. For the peak power-added efficiency (PAE), the optimal matching impedance is $0.612 \angle 60.6^\circ$ in simulation, whereas it measures at $0.7 \angle 62.4^\circ$. Fig. 3.19 presents a similar comparison: the optimal matching impedance is $0.546 \angle 84.7^\circ$ in simulation and $0.58 \angle 90^\circ$ in measurement. Similarly, the best PAE matching impedance is $0.55 \angle 86^\circ$ in simulation and $0.562 \angle 90^\circ$ in measurement. By comparing the S parameters with these optimal matching impedances, it can be concluded that the model proposed in this paper effectively captures both the small signal and large signal characteristics of the in-house device.

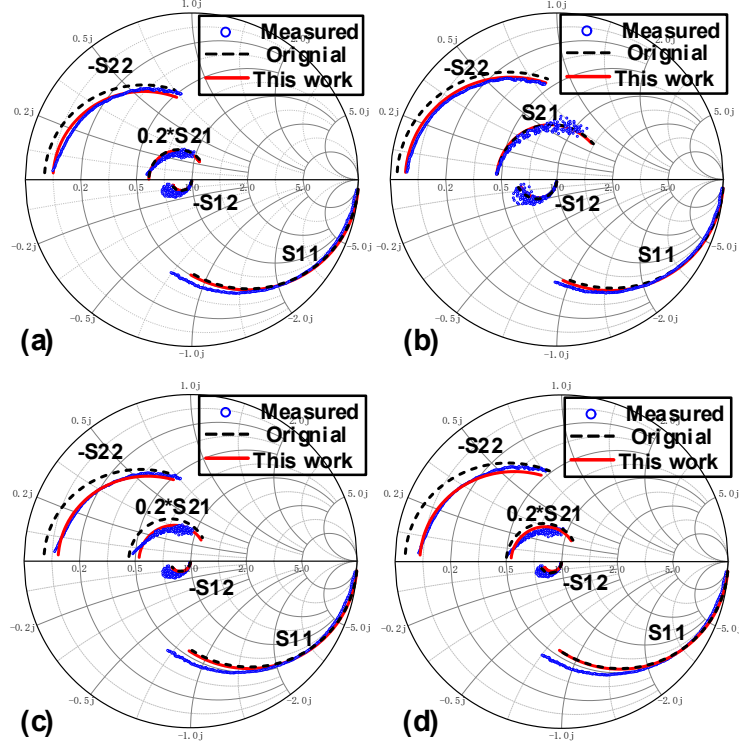


Fig. 3.17. Measured (blue symbols), ASM model simulated (black dashed lines) and proposed hybrid model simulated (red lines) S-parameters in 1-40 GHz of (a) $2 \times 50 \mu\text{m}$, $V_{\text{GS}} = -2.0 \text{ V}$, $V_{\text{DS}} = 10 \text{ V}$ (on-state); (b) $2 \times 50 \mu\text{m}$, $V_{\text{GS}} = 1.5 \text{ V}$; $V_{\text{DS}} = 10 \text{ V}$ (on-state), (c) $2 \times 100 \mu\text{m}$, $V_{\text{GS}} = -2 \text{ V}$, $V_{\text{DS}} = 10 \text{ V}$ (on-state), and (d) $2 \times 100 \mu\text{m}$, $V_{\text{GS}} = -1.5 \text{ V}$, $V_{\text{DS}} = 10 \text{ V}$ (on-state).

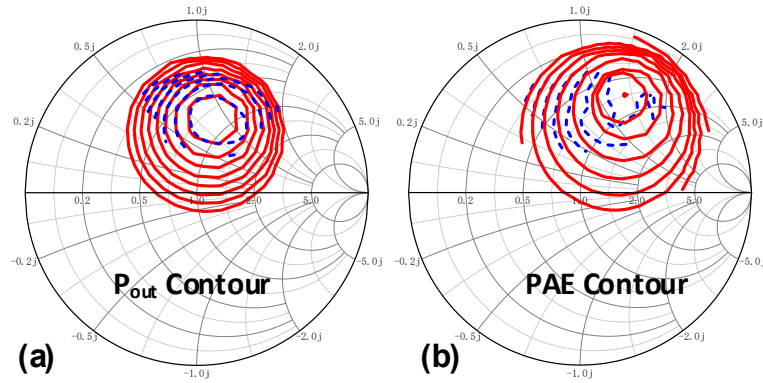


Fig. 3.18. Measured (blue dashed lines) and simulated (red solid lines) loadpull contours: (a) P_{out} contour, and (b) PAE contour of the $2 \times 50 \mu\text{m}$ device at 28.0 GHz. The device is biased at $V_{\text{GS}} = -2 \text{ V}$ and $V_{\text{DS}} = 10 \text{ V}$ with an input power of 10.9 dBm. The source reflection coefficient is $1.13 + j0.628$.

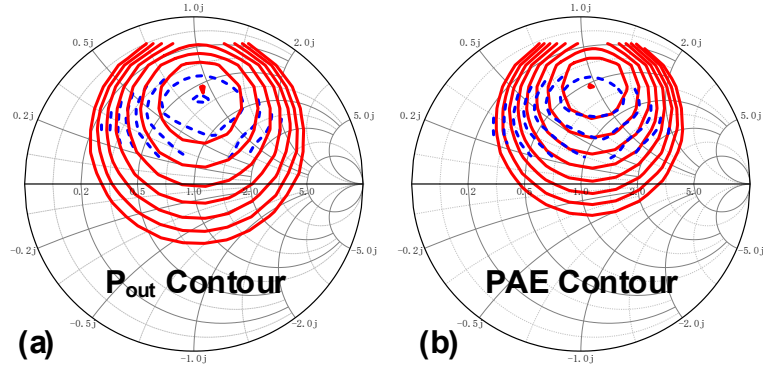


Fig. 3.19. Measured (blue dashed lines) and simulated (red solid lines): (a) P_{out} contour and (b) PAE contour of the $2 \times 100 \mu\text{m}$ device at 28.0 GHz. The device is biased at $V_{GS} = -2 \text{ V}$ and $V_{DS} = 10 \text{ V}$ with an input power of 15.7 dBm. The source reflection coefficient is $1.31 + j0.816$.

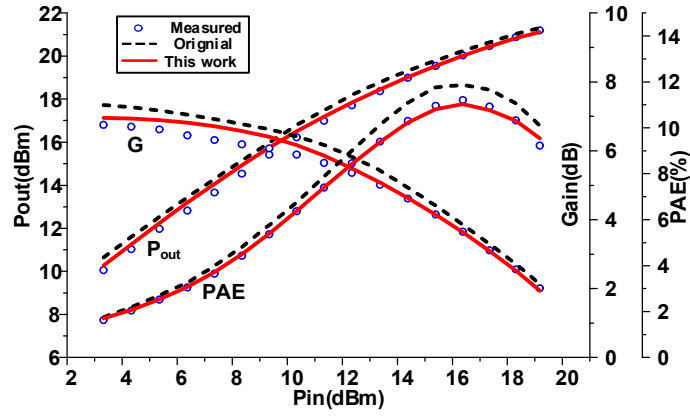


Fig. 3.20. Measured (blue symbols), ASM model simulated (black dashed lines) and hybrid model simulated (red lines) power gain (G), P_{out} , and PAE of the $2 \times 50 \mu\text{m}$ device at 28.0 GHz. The device is biased at $V_{GS} = -2 \text{ V}$ and $V_{DS} = 10 \text{ V}$.

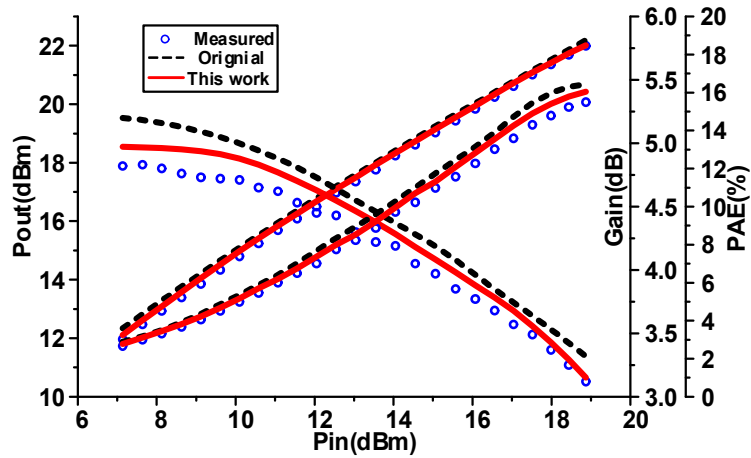


Fig. 3.21. Measured (blue symbols), ASM model simulated (black dashed lines) and hybrid model simulated (red lines) power gain (G), P_{out} , and PAE of the $2 \times 100 \mu\text{m}$ device at 28.0 GHz. The device is biased at $V_{GS} = -2 \text{ V}$ and $V_{DS} = 10 \text{ V}$.

To further compare the large-signal performance of the theoretical model against the real-world device, a power sweep was conducted within the 10-67GHz loadpull architecture. This exercise yielded insights into the power gain (G), P_{out} , and PAE across varying levels of input power. Fig. 3.20 shows the measured (blue symbols), ASM model simulated (black dashed lines) and hybrid model simulated (red lines) values of P_{out} , G , and PAE curves. Additionally, the large-signal performance parameters of the device model with $2 \times 100 \mu\text{m}$ gate width were also scrutinized and depicted in Fig. 3.21, demonstrating a robust concordance between the measured data and simulation outputs. It is important to note that the proposed ASM-ANN model is developed based on a low-voltage GaN HEMT without a field plate. Therefore, it does not account for the additional charge effects in field-plated regions. While acceptable accuracy is achieved for the tested device, extending the model to field-plated structures is considered future work.

3.3. Packaged PA implementation

To further validate the proposed model, a flip-chip packaged PA implementation is on process. The proposed packaged PA structure is given in Fig. 3.22. In this design, the input and output matching networks are integrated on the Si-interposer. At this

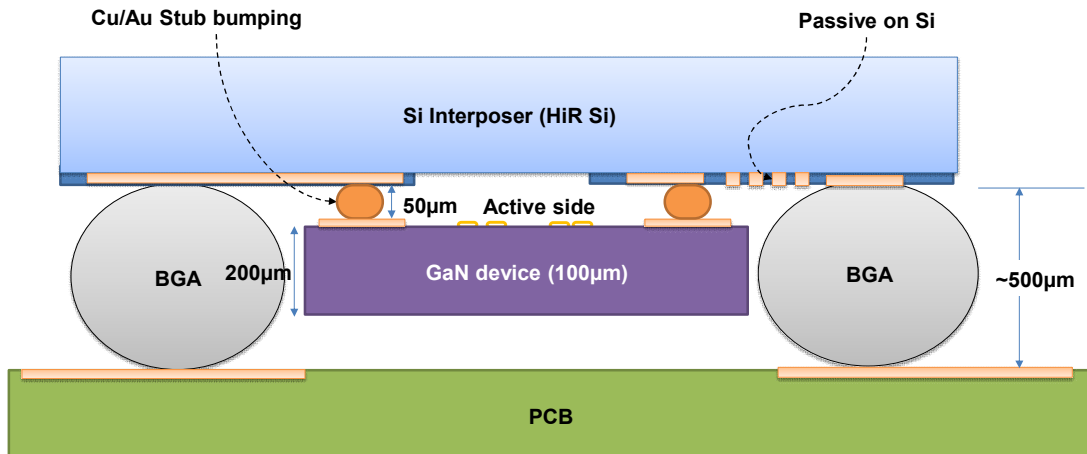


Fig. 3.22. Cross section of the proposed packaged PA.

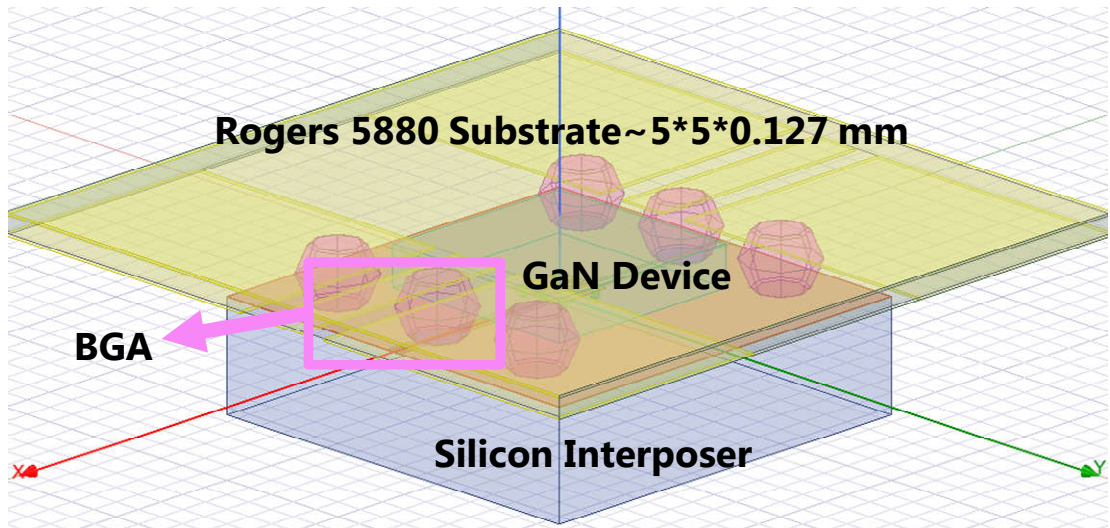
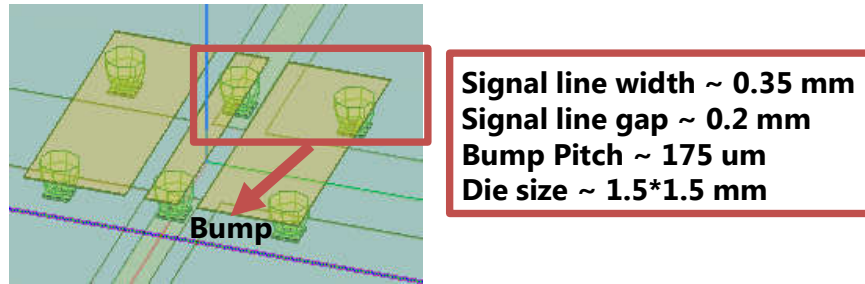


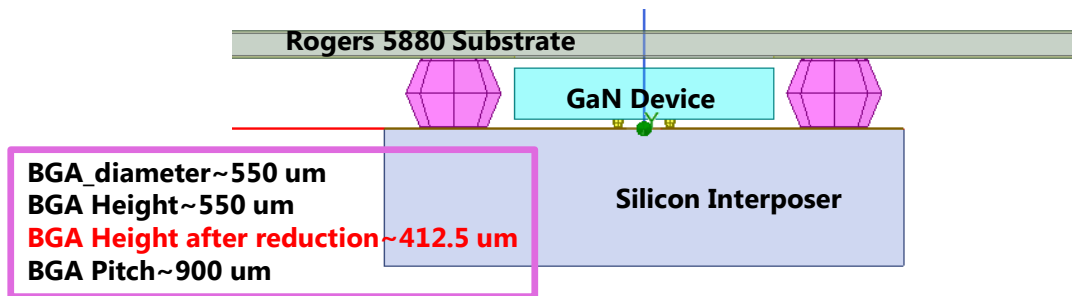
Fig. 3.23. 3D layout of the packaged PA.

frequency range, it is crucial to minimize the impedance mismatch of the interconnects and the loss of the silicon substrate through the co-design of the package and GaN MMIC. In addition to developing the mmWave interposer, an accurate model of the interconnects, including the passive components, is required.

Based on the dimension of the package structure, the 3D model of the whole package is built in HFSS software, shown in Fig. 3.23. The detailed parameters are also shown



(a)



(b)

Fig. 3.24. (a) Bump structure in HFSS. (c) Cross section of the packaged PA in HFSS.

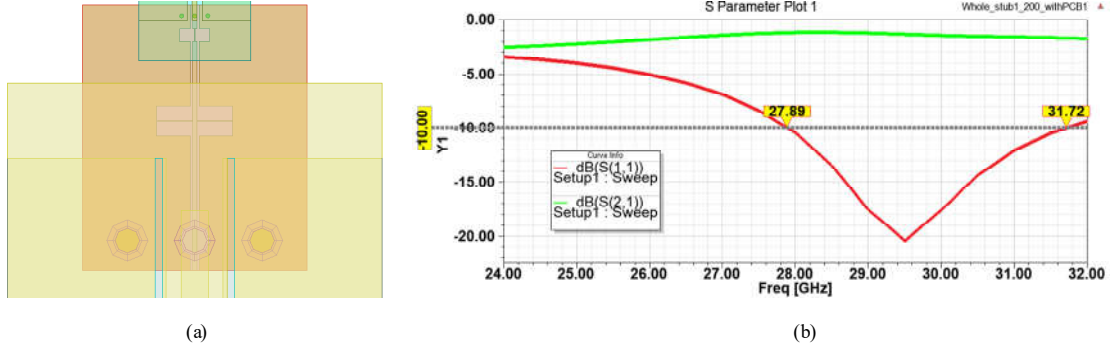


Fig. 3.25. (a) Proposed input matching network structure. (b) Simulation results.

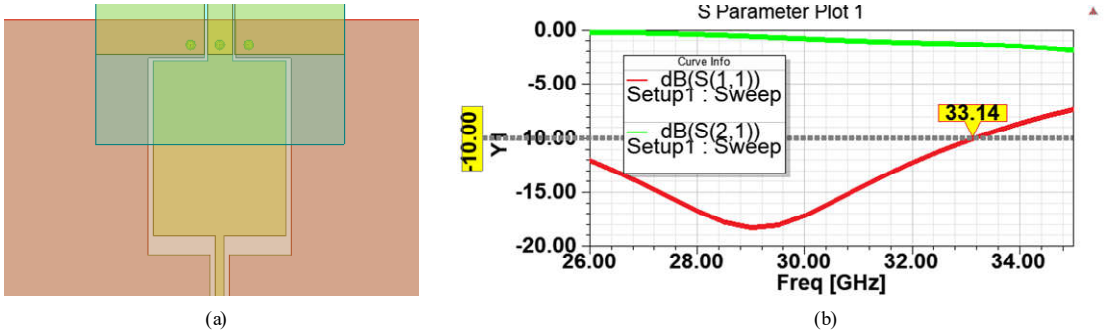


Fig. 3.26. (a) Proposed output matching network structure. (b) Simulation results.

in Fig. 3.24 (a) and (b). As there is only one metal layer on the Si interposer, coplanar waveguide (CPW) is employed to complete input and output matching. The structure and simulation results of the input and output matching are given in Fig. 3.25 and 3.26. The simulation results indicate that the proposed matching network meets the requirements, allowing for subsequent design, production, and iterative refinement.

3.4. Summary

In this work, we introduce an ANN-based modeling framework for GaN HEMTs that synergistically integrates physical concepts. This framework is particularly tailored for the next generation of 5G power amplifiers. The modeling paradigm employs parameter extraction procedure and a sophisticated optimization technique, Multi-Objective Swarm Particle Optimization (MOSPO), to efficiently characterize the surface potential. This ensures a globally accurate model that harmonizes the DC and RF characteristics based on the Advanced-SPICE-Model (ASM) theoretical constructs.

The integration of ANN in the modeling process alleviates the complexities traditionally encountered in the ASM characterization of surface potential, thereby retaining the integrity of the ASM's physical principles within the hybrid architecture. This fusion model surpasses the scalability limitations of conventional ANN-based models and demonstrates enhanced accuracy in predicting large-signal operations when benchmarked against standard ASM-derived physical models. The model also encompasses comprehensive treatments of self-heating and trapping phenomena, pivotal to the emulation of real-world device behavior. Developed within the ADS for a 100-nm GaN HEMT, the hybrid model's validity is evidenced by the close alignment of simulation results with empirical measurements, signifying the model's exceptional precision. The agreement between the theoretical predictions and measured data substantiates the efficacy of the proposed hybrid model, marking a significant stride in the nuanced field of GaN HEMT device modeling.

Chapter 4. A two stages power amplifier in a 130 nm Silicon-On-Insulator (SOI) CMOS process for sub-6GHz 5G applications

Having established a compact and scalable modelling framework for GaN HEMT devices using both ASM-based and ANN-augmented surface potential models in Chapters 2 and 3, the focus of this thesis now shifts toward circuit-level implementations using silicon CMOS technology. Although the modelling and circuit design parts employ different semiconductor platforms, they are unified under the broader objective of developing high-performance mmWave systems for next-generation communication and sensing applications. The GaN-based modelling methodology provides essential insights into device-level behavior, while the CMOS-based power amplifier designs demonstrate practical realization of broadband, efficient mmWave front ends. This transition from physical modelling to circuit design represents a holistic and multidisciplinary approach that spans the entire mmWave design chain, from device physics to tape-out-ready circuit implementations.

Power amplifiers play a vital role in 2G/3G/4G/5G RF/mmWave applications. A PA dominates the power dissipation of the transceiver system. The future of 5G applications at sub-6GHz push a great demand in PAs that combine low power dissipation, high linearity, output power and PAE for high reliability and stability massive deployment [83, 84]. III-V compound and CMOS process are two main choices according to different applications. In the area of high-performance requirements such as communication stations, military fields of radar system, ship and aviation etc where high linearity, high PAE, high output power, and the most important, reliability and stability are required, III-V compound processes such as GaAs, GaN, InP etc are highly recommended for their high breakdown voltage, high electron mobility and high heat performance process characteristic [85-87]. Improved process preparation, cost down,

and the yield of III-V compound process will lead to more consumer opportunities. In the area of low cost and low power commercial electronics, CMOS processes are competitive though it is still a challenging task to implement PA performances such as linearity, efficiency and stability in CMOS process due to the low breakdown voltage and low resistance substrate limitation [88, 89]. Thanks to process, circuit and package technology improvements, the development of PAs in silicon CMOS process and its derivative processes such as SiGe, BiCMOS and SOI CMOS processes are thriving with performance optimization techniques are adopted in CMOS PAs to reduce performance disparities in recent years. Average power tracking (APT) which is used in [90] improved the PAE to 50%. PA with both envelop tracking (ET) mode and APT mode in [91] provides 88.2% PAE. Digital pre distortion (DPD) which is used in [92] improved the linearity performance ACPR from -42dBc to -58dBc. Antenna tuner technique which is used in [93] improved the PAE from 15% to 45 %. The PAs based on CMOS SOI process have the potential to be widely used comparing to the existing high-cost process PAs, and can deliver the combined benefits of high performance, high integration as well as low cost [94, 95]. Though System-on-Package (SoP) solutions make it easier to combine RF frontend and baseband processor in different processes, the integration of RF and the baseband blocks, high power and its control blocks is still critical for cost down and form-factor reasons. As such, SOI CMOS is a good choice to design and fabricate the PAs for low cost 5G applications.

In SOI CMOS process, digital baseband processors are normally realized using floating body transistors because body-contacted areas can be reduced in layout and the chip area will be smaller. But for RF frontend blocks such as LNAs, PAs and switches, body-contacted transistors are recommended to achieve superior noise figure, linearity and isolation performance [96, 97]. To investigate better integration between RF

frontend and digital baseband, a two stages PA is presented using floating-body transistors. In order to achieve wide bandwidth, high gain and high output power, on chip wideband impedance matching networks and two stages PA configuration are used with inter-stage impedance matching network [98, 99]. Two-stage configuration is used for sufficient power gain of the PA including input matching networks, input amplifier stage, inter-stage matching networks, output amplifier stage and output matching networks. The input amplifier stage is working as a driver stage, and the output amplifier stage is a power stage. Fig.4.1 shows the proposed two stages PA. On-chip transformer baluns are employed as anti-phase signal splitter and combiner, which are also used for impedance matching at the input and output. Differential push-pull structures are adopted for higher output impedance and output power compared to the single-ended structure. On-chip bandgap voltage reference (BVR) is also adopted, and it generates the temperature independent voltage bias for the drivers and power amplifiers. What is more, to minimize the multi-physics affects, especially to minimize the thermal effect, over temperature gain compensation technique is used in the proposed PA.

4.1 PA Structure

As shown in Fig. 4.1, the proposed floating-body based two stage power amplifier with on-chip BVR voltage bias circuit. In PA part, common source common gate (CSCG) structure is utilized in both the driver amplifier and power amplifier to improve transmitting gain. The difference of the two stages is that there is a negative RC shunt feedback network between the input and output of driver amplifier which can improve the stability and linearity.

Differential push-pull structure instead of single-ended structure is adopted with a supply voltage of 3.3 V. By using this structure, the amplifier output impedance will be higher so that higher output power can be achieved. What's more, heat radiation is the

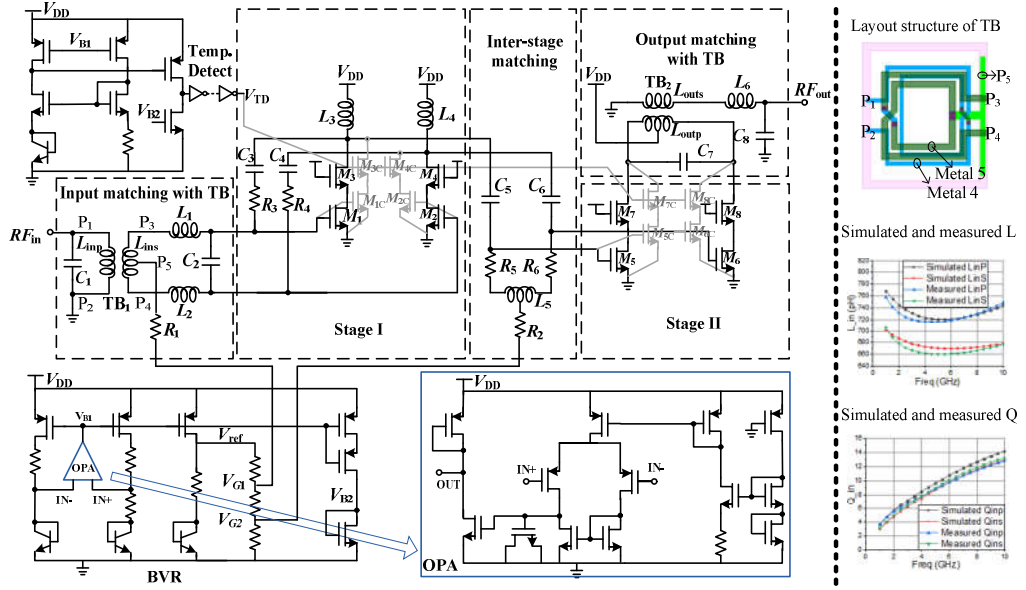


Fig. 4.1. The proposed two-stage push-pull power amplifier circuit with input and output matching network.

crux especially in high power applications and differential push-pull structure is a good on-chip circuit solution. Input high pass matching network is mainly composed of L_1 , L_2 and an on-chip transformer balun TB_1 , together with L_3 , L_4 composed low pass network in stage I will realize wideband matching for input. TB_1 turns the single RF input signal into a pair of differential signals as a splitter. C_5 , C_6 , R_5 , R_6 and L_5 are used for inter-stage matching. Transformer balun TB_2 combines the differential signal of stage II power amplifier to single output, and with L_6 and L_8 , constitute the output matching network. The fundamental blocks and circuit design considerations are described in the following subsections.

4.2 SOI Floating-body Transistor and Transformer Balun Consideration

Thin floating-body transistor will be used to investigate the possibility and reliability of high-performance PAs with smaller chip size. Fig. 4.2 (a) is the cross-section graph of floating-body (FB) and body-contacted (BC) NMOS in 130nm SOI CMOS process. To estimate the current variation of floating-body and body-contacted transistors, Fig. 4.2 (b) shows the variation of drain current at length L of $0.13 \mu\text{m}$, width W of $240 \mu\text{m}$

and $960\mu\text{m}$ at V_{GS} of 0.75 V and 1 V , respectively. When $V_{ds} > 1\text{ V}$, I_{ds} of FB NMOS is about 20% lower than that of BC NMOS. Therefore, it is possible to use FB NMOS instead of body contacted NMOS to realize PA if reasonable DC is chosen. Transformers for the input and output matching are designed based on EM simulation using ADS (Advanced Design System) Momentum to compensate for the effect of the parasitic passive components. Both input and output transformer baluns share a similar structure, as shown in Fig. 4.1, where M_4 is used for the primary coil while M_5 is used for the secondary coil which is split into 2 halves to generate differential outputs. The comparison of simulated and measured characteristics of the proposed TB are discussed. Regarding measurement results, inductance L and Q value variation are less than 10%, the insertion loss of S_{21} and S_{31} are -5.1 dB and -7.2 dB at 5 GHz , and phase imbalance gap is less than 5° in the pass band. The variation of TB inductance around $5\text{-}6\text{ GHz}$ is acceptable and Q value is reasonable for wideband application and according to the results, the performance of the proposed transformer balun could be satisfied the requirements for the design of this two stage PA.

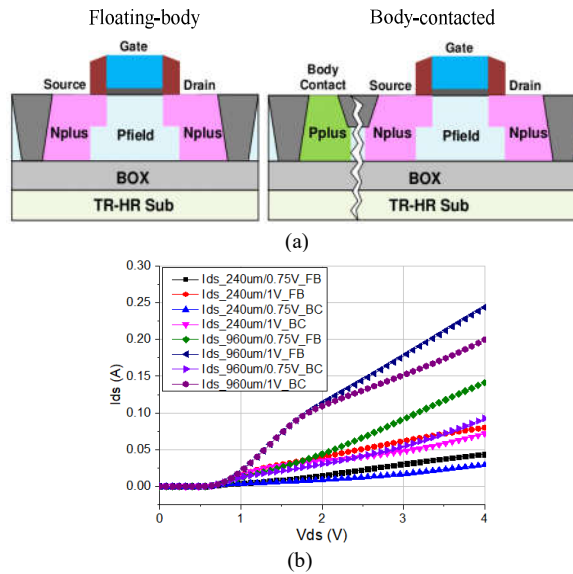


Fig. 4.2. SOI floating-body and body-contacted NMOS comparison (a) cross section structure (b) DC results at $L=0.13\mu\text{m}$, $W=240\mu\text{m}$ and $960\mu\text{m}$.

4.3 Amplifier Design and Impedance Matching

Cascaded common source common gate structure is used in two stages of amplifiers at 3.3 V power supply for power dissipation optimization. The proposed PA consists of two stages of CSCG structure amplifier to achieve high gain of > 20 dB and RC compensation is used for stability design. As shown in Fig. 4.1, transistors M_1 - M_4 are used for the driver amplifier stage as well as M_5 - M_8 are adopted for the power amplifier stage. To improve the linearity, negative feedback composed of R_3 , C_3 and R_4 , C_4 is used to control the gain. Metal-insulator-metal (MIM) capacitors are adopted for the feedback circuits and matching networks since the capacitance value is more accurate, and it does not change with the bias voltage. To trade-off the output power and the power gain of the designed PA, the optimization for the device size which is controlled by the gate width and multiplication number of the unit cell in the implementation [100].

As discussed in [99], the single-ended output power and power gain could be expressed as equation (4.1) and (4.2) from the small signal equivalent circuit of half-circuit of the proposed cascoded CSCG push-pull structure.

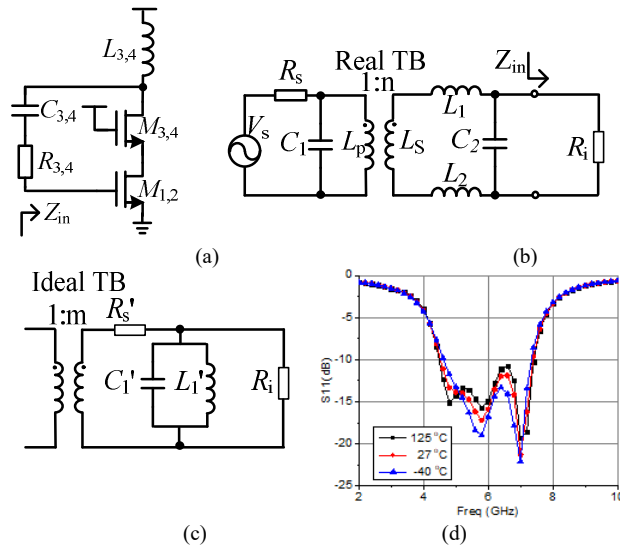


Fig. 4.3. Impedance matching consideration: (a) RC shunt feedback, (b) schematic of input matching, (c) equivalent circuit of input matching, (d) simulated results of input matching at -40°C , 27°C and 125°C .

$$P_{\text{out},s} = \frac{V_{\text{out}}^2}{R_{\text{out}}} \text{ and } P_{\text{in}} = \frac{V_{\text{in}}^2}{R_{\text{in}}} \quad (4.1)$$

$$P_G = \frac{2mnP_{\text{out},s}}{P_{\text{in}}} \propto \frac{2mnV_{\text{out}}^2}{V_{\text{in}}^2} \quad (4.2)$$

where m and n are the turn ratios of input and output transformer balun TB₁, TB₂, respectively, V_{in} and V_{out} present the input and output voltage as well as R_{in} and R_{out} are the input and output impedance, respectively. To get larger gain, the lengths of common gate transistors M_3, M_4, M_7 and M_8 are set larger than those of common source transistors M_1, M_2, M_5 and M_6 . Additionally, the bias of the driver stage CS transistors V_{G1} is injected through TB₁ while that of the power stage is injected through L₅.

In this PA design, device size of the driver stage and power stage are optimized using source-pull and load-pull simulation. The device size for M_1 and M_2 of the driver stage is a gate width of 240 μm and a gate length of 130 nm while the device size for M_5 and M_6 of the power-stage is a width of 960 μm and a length of 130 nm. The difference between driver stage amplifier and power stage amplifier is that there is a negative RC shunt feedback network in driver stage which can improve the stability, linearity and bandwidth between input and output, as shown in Fig. 4.3(a). To realize wideband matching, input matching network is based on a band-pass filter with passive TB. Fig. 4.3 (b) (c) is the schematic and equivalent model. The band-pass filter has two poles ω_1 and ω_2 :

$$\omega_1 = -\frac{X}{2} + \sqrt{\frac{X^2}{4^2} + \omega_0^2}; \omega_2 = \frac{X}{2} + \sqrt{\frac{X^2}{4^2} + \omega_0^2} \quad (4.3)$$

$$X = \frac{1}{C'_1} \cdot \sqrt{\frac{1}{R'_s} \cdot \left(\frac{1}{R_i} - \frac{1}{R'_s} \right)} \quad (4.4)$$

Where

$$\omega_0 = \sqrt{\omega_1 \cdot \omega_2} = \frac{1}{C'_1 \cdot L'_1} \quad (4.5)$$

$$C_1' = \frac{C_1}{m^2} + C_2 \quad (4.6)$$

$$L_1' = \frac{k^2 L_p \cdot L_1}{k^2 L_p + L_1}, (L_1 = L_2) \quad (4.7)$$

where ω_0 is the medium frequency, and $1:m = k \cdot \sqrt{L_p/L_s}$, $R_s' = m^2 R_s$, R_i is input impedance at driver stage amplifier. The minimum return loss is achieved at ω_0 and it can be derived as:

$$S_{11} = \sqrt{1 - \frac{4R_s' \cdot R_i}{R_s' + R_i}} \quad (4.8)$$

Under the discussion, Fig. 4.3(d) shows its input matching results at different temperatures. There is a 3.6 dB variation when the temperature is from -40°C to 125°C at the other same simulation setup and impedance matching conditions. In output power stage, the gate width of M_5 and M_6 is 4 times that of M_1 and M_2 in driver stage to provide enough output power.

The reliability caused by multi-physics effects are also considered for optimization of the proposed PA. Like the previous work in [97], electrical parasitic and field distribution effects of bonding wires are modelled and co-simulated with the circuits. The electrical performance degraded due to the parasitic parameters of bonding wires such as parasitic capacitance C_{bd} , resistance R_{bd} and inductance L_{bd} , where L_{bd} is the decisive factor which is proportional to the length of the bonding wires. Based on the co-simulated SP results, the input and output matching performance are degraded due to the L_{bd} mainly since the C_{bd} and R_{bd} are small. Minimum the length of the bonding wire with optimized input and output matching network are adopted for this design.

Besides electrical parasitic effects simulation, electric energy density response, electric potential response and thermal response of bonding wires are also modelled and co-simulated, as shown in Fig.4.4, 1 mil diameter Au bonding wire is adopted in the co-

simulation according to package or bonding requirement. Due to the 735 μ m thickness silicon substrate, the shortest length of bonding wires is estimated to be 32-35 mils at input and output ports. When the surface charge is set to 0.00001 C, the simulated electric energy density is about 10^{17} J/m³ (Fig. 4.4(a)) and the electric potential is 1.6×10^9 V (Fig. 4.4(b)) in the case of interconnect Al Metal 5 of the PA die to PCB copper-island. The simulation result shows there is field stress concentration at Metal 5 of S PAD (signal pad of GSG), but it can be ignored because the edge terminations and dual passivation are used in the proposed 130nm CMOS SOI process to avoid high electrical field stress. The thermal response result in Fig. 4.4 (c) shows that the temperature of the top surface of drain electrode (S PAD) is 203°C at 27°C environment temperature with 100W heat power. When the heat power ranges from 10W to 0.1W, the surface temperature will range from 44.6°C to 27.4°C at 27 °C environment temperature, shown in Fig. 4.4 (d) and (e). The electro-thermal responses results indicate that when chip heat-dissipation is ignored, the electro-thermal effects of bonding wires are less important than electrical parasitic effect at low output power applications. Besides bonding wire, temperature and heat problem for the PA kernel circuit is also important and discussed. There is a 5.7dB gain degradation of the PA when the simulated temperature is increased to 120°C. To solve this problem, auxiliary CSCG structures M_{1C} - M_{4C} in driver stage and M_{5C} - M_{8C} in power stage are adopted to compensate for the gain, as shown in Fig. 4.1. The CS part of auxiliary CSCG is controlled by the same bias as the major CS pairs. The CG part is controlled by an over temperature detector as shown in Fig. 4.1. When the PA temperature is low, the lateral NPN is off and the over temperature detector output is 0, so that the auxiliary CSCG is off. In contrast, the lateral NPN will be on and the overtemperature detector output is 1 when the PA temperature increased, and then the auxiliary CSCG is on which will

provide extra gain to compensate the gain degradation. In simulation, there is a 3-5 dB gain compensation via the temperature gain compensation technique for the proposed.

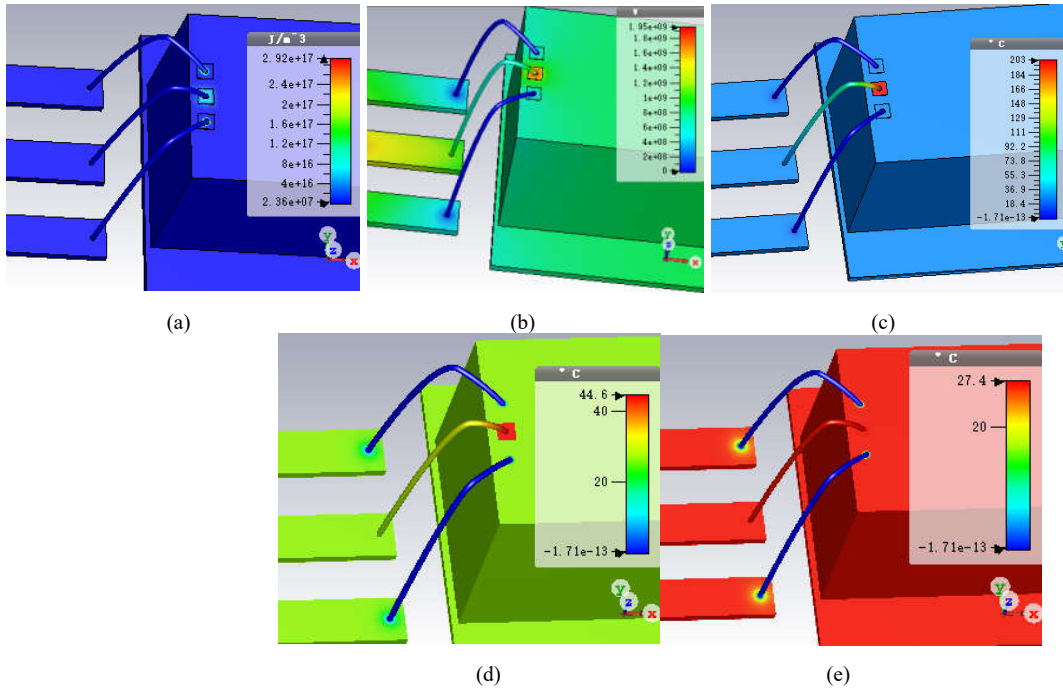


Fig. 4.4 Simulated electric energy density response, electric potential response and thermal response of bonding wires (a) electric energy density response, (b) electric potential response, thermal response (c) at 100 W heat power, (d) at 10 W heat power and (e) at 0.1 W heat power.

4.4 Experimental Results

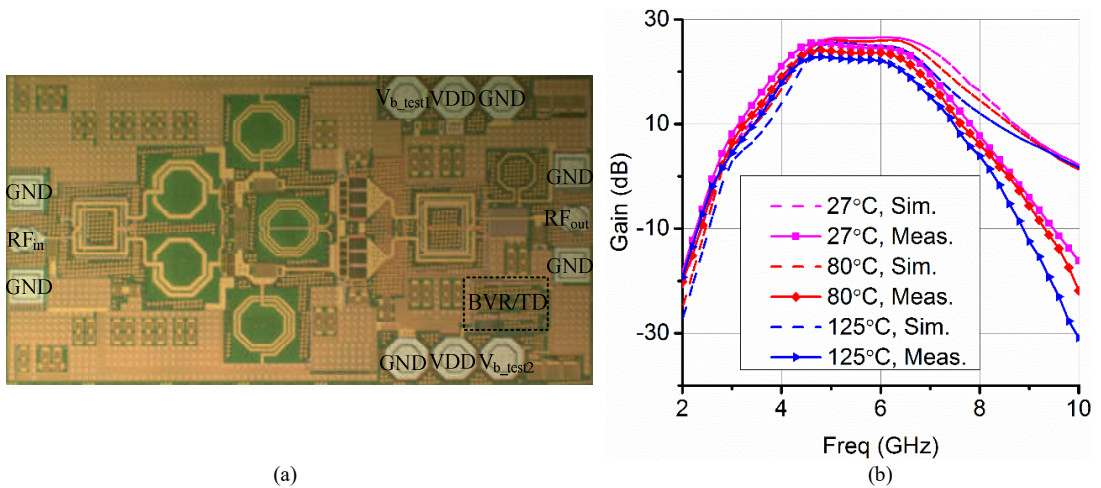


Fig. 4.5. (a) Chip micrograph of the proposed PA and (b) measurement and simulation comparison of gain.

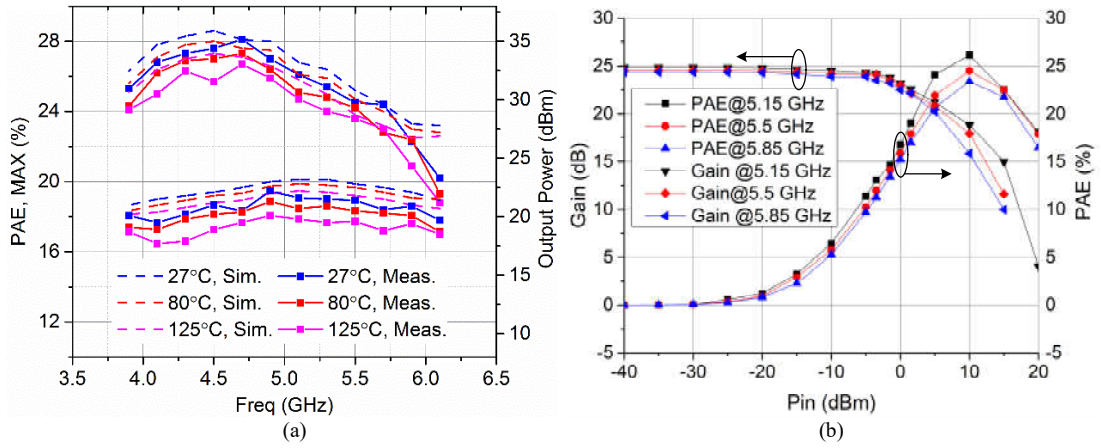


Fig. 4.6. (a) Measured PAE and output power versus frequency and (b) measured PAE and power gain versus input power.

The PA is fabricated in a 130nm SOI CMOS process and wire bonded to PCB implemented using RO4350 substrate with 20- mil thickness. The overall chip size of the implemented PA circuit is 1.21 mm $\times$ 0.65 mm including bias circuit and Input/Output (IO) pads, testing pads as shown in Fig. 4.5 (a). The core size of the chip is only 0.59 mm². Fig. 4.5(b) shows the comparison of the simulated and measured gain. Wide band input matching has been achieved with 3 dB bandwidth from 4.3 GHz to 6.4 GHz while the gain is up to 25.6dB. The gain drop over a temperature range of 27°C to 125°C is 1.9 dB on average, which validates the robustness of the proposed techniques. The measured output power and PAE performance versus operating frequencies are depicted in Fig. 4.6(a). The maximum output power is 22.2 dBm at around 4.9 GHz and the highest PAE is 28% at around 4.7 GHz for the temperature of 27°C. When the temperature is increased to 125°C, the output power decreases less than 2 dB, while there is a decrease of only 6% in the PAE. The measured power gain and PAE versus input power at 5.15 GHz, 5.5GHz and 5.85 GHz are displayed in Fig. 4.6(b). To evaluate its performance practically for IEEE 802.11ac 5G application, the proposed PA was measured using VHT80 MCS9 (80 MHz, 256-QAM) signals without digital predistortion. At satisfying the specification of EVM <-36 dB, the PA delivers power

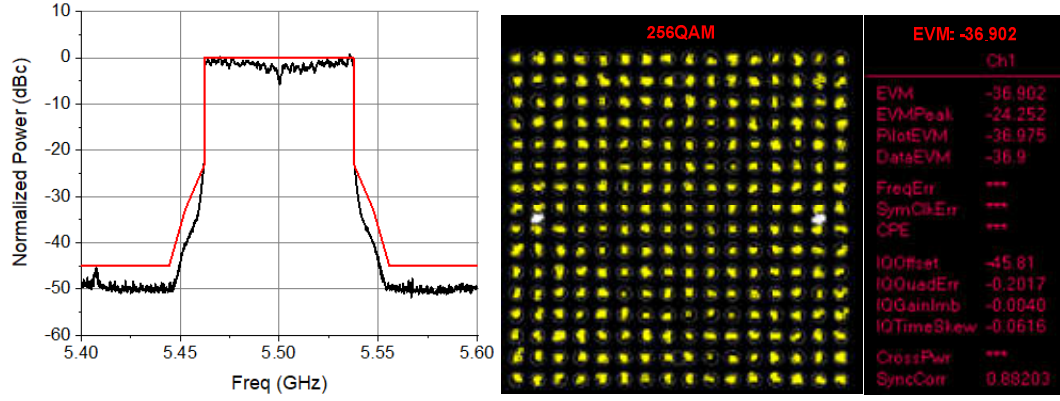


Fig. 4.7. The EVM measurement @5.5 GHz.

Table 4.1. Performance Summary and Comparison

Ref.	This work	[94]	[99]	[100]	[101]
Process	130nm SOI CMOS	55nm SOI CMOS	130nm SOI CMOS	130 nm SOI CMOS	GaN HEMT
BW (GHz)	4.3-6.4	4.9-5.9	5.15-5.85	3.1-3.9	5.5-6.5
Gain (dB)	25.6	26	14.7	17	12.5
$P_{out-1dB}$ (dBm)	22.2	20	24	23	44
PAE@ P_{out} (%)	28	12	40	60	42
Supply (V)	3.3	3.3	3.6	4	30
Area (mm ²)	0.59	1.04	0.62	-	2.256

gain of 24.6-25 dB and PAE of 23.8-26.9 %. The measured EVM results for VHT80 MCS9 at 5.5GHz are shown in Fig. 4.7.

In Table 4.1, the measured performance of the proposed PA which has achieved wideband and high gain are summarized and compared with other state-of-the-arts. PAs in [94, 99] and [101] share good OP-1dB and PAE performance. PA in [100] demonstrates good gain and OP-1dB performance. The proposed two-stage push-pull PA is a good choice for the reasonable trade-off of these three important performances compared to CMOS or other process PAs. What is more, the chip area is smallest and is suitable for low cost, temperature adaptable sub-6GHz 5G applications.

4.5 Summary

This chapter proposed a floating-body transistor based two-stage PA in 130 nm SOI CMOS process, which has achieved maximum power gain of 25.6 dB with 3 dB

bandwidth from 4.3 GHz to 6.4 GHz. The output power is up to 22.2 dBm at 4.9 GHz. The maximum PAE is 28% at 4.7 GHz. This work has proved the feasibility of using floating-body SOI CMOS devices to achieve advanced PAs as well as small chip area and has been ready for better integration with baseband processors in sub-6GHz 5G applications.

Chapter 5. A mm-Wave coupler-based dual-band power amplifier for beyond 5G application

The rapid advancement of wireless communication and automotive technologies has led to an increasing demand for high-frequency, high-performance components in various applications. Automotive radar systems, essential for ADAS and autonomous driving, particularly benefit from operating in the 60GHz and 77GHz frequency bands. These bands offer significant advantages in resolution, data transmission speed, and interference reduction, making them ideal for precise and reliable object detection and distance measurement. Developing dual-band power amplifiers for 60GHz and 77GHz applications provides several notable benefits. High-frequency operation allows for smaller antenna sizes, which is beneficial for integrating radar systems into vehicles without taking up too much space. Additionally, the higher frequency bands are less crowded, leading to reduced interference and improved signal quality. The wider bandwidths available at these frequencies support high data rates, essential for the rapid processing and transmission of radar signals. These characteristics are crucial for enhancing the functionality and reliability of automotive radar systems, supporting advanced features like collision avoidance, adaptive cruise control, and parking assistance, as well as paving the way for fully autonomous driving technologies.

The focus of this section is on the design and development of dual-band power amplifiers operating at 60GHz and 77GHz, using a coupled-line dual-frequency matching structure. The innovation of this amplifier is mainly seen in its input and output matching networks. A unique coupler design, capable of matching at both frequency points, is implemented. This design takes advantage of the varying electrical lengths of couplers and transmission lines at different frequencies, resulting in distinct impedance characteristics at 60GHz and 77GHz. By carefully simulating the transistor

at these frequencies, optimal input and output matching impedances for both bands are determined. Consequently, the coupler is tailored to simultaneously match the transistor at both frequencies, achieving a well-matched power amplifier across the dual bands. The simulation results demonstrate impressive performance metrics, with P_{out} of 12 dBm at 60GHz and 10 dBm at 77GHz, with the power added efficiency of 24.4% and 13.85%, respectively.

5.1. Dual band impedance converter

In the design of RF and microwave circuits, impedance matching is a crucial concept and step that must be considered when designing devices and modules. For instance, in the design of RF power amplifiers and microwave oscillators, matching circuits are an essential part of the design process. Passive networks are typically inserted into almost all active devices to achieve proper impedance matching.

The practical function of a dual-frequency impedance converter is fundamentally like that of a single-frequency impedance converter, with the key difference being its application to two frequencies instead of one. However, achieving this extension poses significant challenges in circuit analysis and design. Analyzing a circuit at two different frequencies is considerably more complex than in the single-frequency case.

Dual-band transmission line converters utilize transmission lines designed to operate at two distinct frequencies. By carefully selecting the lengths and characteristic impedances of the transmission lines, efficient impedance transformation can be achieved. These converters are commonly used in RF power amplifiers and antenna matching networks where dual-band operation is required. They offer a simple structure and ease of integration into existing circuit designs, though precise control over transmission line parameters is necessary to achieve accurate impedance matching.

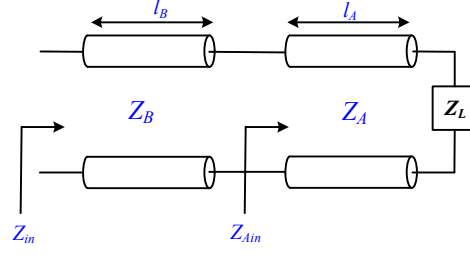


Fig. 5.1 Two transmission line dual-band impedance converter.

Fig. 5.1 shows a dual-frequency matching structure composed of two transmission lines with different characteristic impedances. Each transmission line segment has corresponding lengths l_A and l_B , and characteristic impedances Z_A and Z_B . By adjusting these four parameters, impedance matching can be achieved. Z_{Ain} is the input impedance of the transmission line segment with characteristic impedance Z_A , and Z_{in} is the input impedance of this part of the matching circuit.

The principle of the impedance converter with two transmission line segments can be analyzed as follows. Since $\beta = 2\pi f/\mu_p$ where μ_p is the phase velocity, the input impedance of the first transmission line segment at two different frequencies is given by:

$$Z_{Ain}(f_1) = Z_A \frac{Z_{L1} + jZ_A \tan(\beta_1 l_A)}{Z_A + jZ_{L1} \tan(\beta_1 l_A)} \quad (5.1)$$

$$Z_{Ain}(f_2) = Z_A \frac{Z_{L2} + jZ_A \tan(\beta_2 l_A)}{Z_A + jZ_{L2} \tan(\beta_2 l_A)} \quad (5.2)$$

Since the above impedance becomes the load impedance of the second transmission line segment, the input impedance of the matching circuit can be obtained through the following formulas:

$$Z_{in}(f_1) = Z_B \frac{Z_{Ain}(f_1) + jZ_B \tan(\beta_1 l_B)}{Z_B + jZ_{Ain}(f_1) \tan(\beta_1 l_B)} \quad (5.3)$$

$$Z_{in}(f_2) = Z_B \frac{Z_{Ain}(f_2) + jZ_B \tan(\beta_2 l_B)}{Z_B + jZ_{Ain}(f_2) \tan(\beta_2 l_B)} \quad (5.4)$$

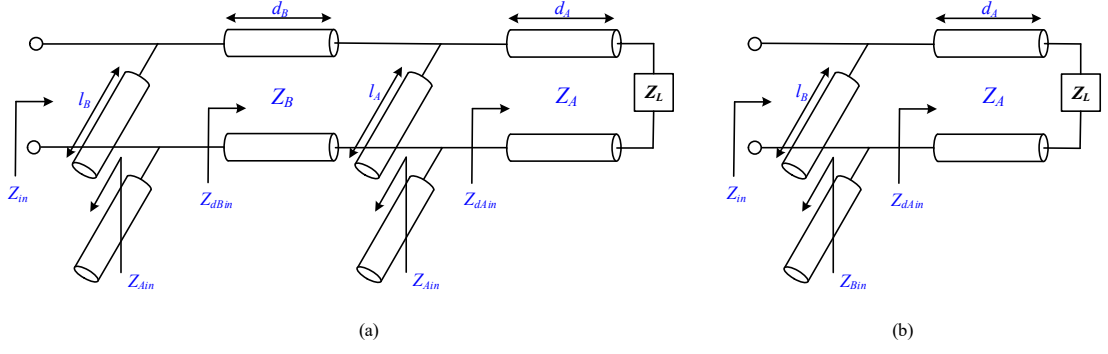


Fig. 5.2 (a) Two transmission lines and two branch dual-band impedance converter, (b) Single transmission line and single branch dual-band impedance converter.

Separating the real and imaginary parts of the impedance, and matching the real part to a system reference impedance Z_0 , the following set of equations is obtained:

$$\begin{aligned} \operatorname{Re}(Z_{in}(f_1)) - Z_0 &= 0 \\ \operatorname{Re}(Z_{in}(f_2)) - Z_0 &= 0 \\ \operatorname{Im}(Z_{in}(f_1)) &= 0 \\ \operatorname{Im}(Z_{in}(f_2)) &= 0 \end{aligned} \quad (5.5)$$

These equations ensure that the impedance is correctly matched at both frequencies, providing an effective dual-band impedance transformation. Also, there are other kinds of dual-band transmission line converters, their principle and design methods are similar, the diagrams are shown as Fig. 5.2(a) and (b).

Lumped element dual-band converters use discrete inductors and capacitors to create resonance at two different frequencies. The component values are chosen to provide the desired impedance transformation at each frequency, making them suitable for applications where space constraints prevent the use of transmission lines, such as compact RF modules. These converters are compact and flexible in design but are sensitive to component tolerances and may experience performance degradation due to parasitic effects. Fig 5.3 gives some examples of lumped element dual-band converters.

Dual-band Wilkinson power dividers are designed to split power equally at two frequencies while providing impedance matching and isolation between output ports.

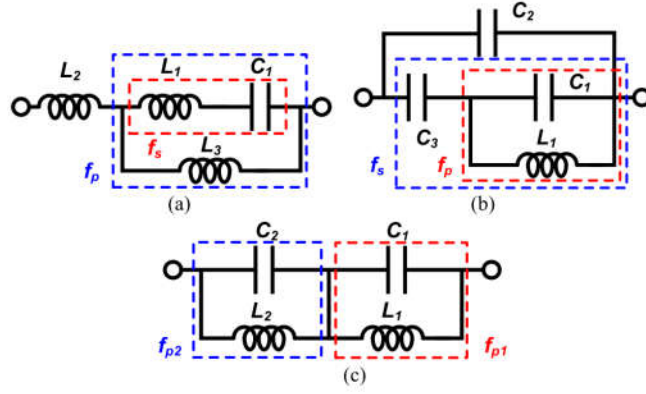


Fig. 5.3 Schematic of dual-band lumped element. (a) dual band inductor, (b) dual-band capacitor, and (c) dual-band reactance.

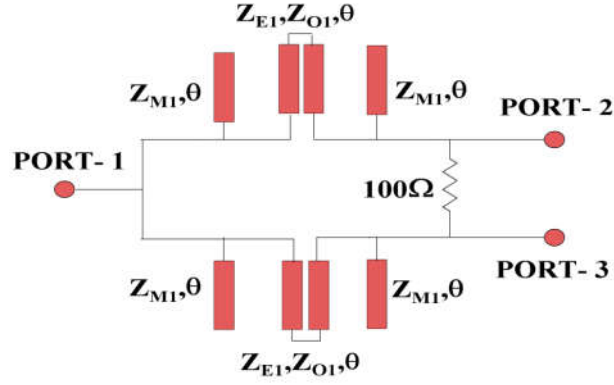


Fig. 5.4 Dual-band Wilkinson power divider.

They typically use a combination of transmission lines and reactive components and are widely used in phased array radar systems and multi-band communication systems. These dividers provide excellent isolation and matching at both frequencies, but their design is complex, and they may require additional reactive components, increasing their size. Fig. 5.4 has shown the structure of a dual-band Wilkinson power divider.

5.2. Dual-band coupled-line converters for impedance matching networks

Based on the analysis in the previous section, a dual-frequency computation and dual-frequency dual-reactance branch method using coupled lines has been adopted. The proposed dual-band coupled-line converters leverage coupled transmission lines to achieve impedance transformation, resulting in a compact wideband coupled line dual-

frequency impedance converter. The electrical lengths and coupling coefficients are designed to match the desired impedance at two frequencies. This section begins with a detailed analysis of the main components that make up the coupled line dual-frequency impedance converter. Subsequently, the basic principles of single-frequency coupled line impedance converters and the dual-frequency dual-reactance branches are analyzed and derived separately. Based on the combination and application of these key components, the dual-band coupled-line converters discussed in this paper is realized.

Fig. 5.5 gives the diagram of the proposed dual-band coupled-line impedance converters, in this design, the main structure of the circuit consists of two parts. One part is a section of coupled line, and the other part is a dual-frequency dual-reactance element connected to the two ends of the coupled line. The even-mode and odd-mode characteristic impedances of the coupled line are Z_{0o} and Z_{0e} , respectively. At the first operating frequency f_1 , the electrical length is θ_1 . At the second operating frequency f_2 , the electrical length is θ_2 .

The dual-frequency dual-reactance element exhibits different impedances at the two frequencies f_1 and f_2 , specifically jX_{T11} and jX_{T12} . These characteristics enable the dual-frequency impedance converter to transform the load impedance Z_L to two arbitrary complex impedances Z_{in1} and Z_{in2} at frequencies f_1 and f_2 .

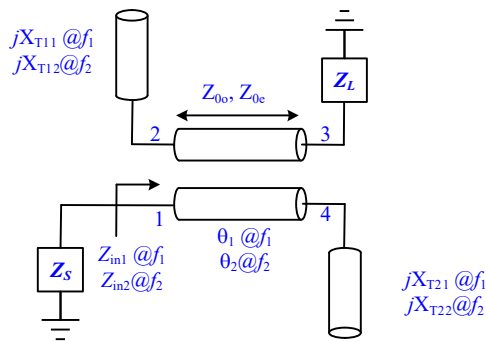


Fig. 5.5 Proposed dual-band coupler-based impedance converter.

In couple-line based impedance converters, symmetric coupled lines can meet most application requirements. Therefore, this section focuses only on the even-odd mode analysis method for symmetric networks. The matrix elements of the open-circuit impedance matrix for symmetric coupled lines can be expressed using the following equations:

$$\begin{aligned}
Z_{11} = Z_{22} = Z_{33} = Z_{44} &= -j \frac{Z_{0e} + Z_{0o}}{2} \cot(\theta) = \frac{-jZ_a}{\tan(\theta)} \\
Z_{12} = Z_{21} = Z_{34} = Z_{43} &= -j \frac{Z_{0e} - Z_{0o}}{2} \cot(\theta) = \frac{-jZ_b}{\tan(\theta)} \\
Z_{13} = Z_{31} = Z_{42} = Z_{24} &= -j \frac{Z_{0e} - Z_{0o}}{2} \csc(\theta) = \frac{-jZ_b}{\sin(\theta)} \\
Z_{14} = Z_{41} = Z_{23} = Z_{32} &= -j \frac{Z_{0e} + Z_{0o}}{2} \csc(\theta) = \frac{-jZ_a}{\sin(\theta)}
\end{aligned} \tag{5.6}$$

$$\text{Where } Z_a = \frac{Z_{0e} + Z_{0o}}{2}, Z_b = \frac{Z_{0e} - Z_{0o}}{2}.$$

Since the reactance elements X_{T1} and X_{T2} must be real numbers. Their values can be zero, positive, or negative, and they can be equal or unequal depending on the specific circuit requirements. These reactance elements can be adjusted based on the practical needs of the circuit. When these two reactance elements are connected to ports 2 and 4 of the coupled line, the four-port network simplifies to a two-port network. Then the impedance matrix elements at ports 1 and 3 can be expressed as follows:

$$\begin{aligned}
Z_{11} &= j \frac{Z_a(Z_a^2 - Z_b^2 - X_{T1}X_{T2})\sin(\theta)\cos(\theta) - Z_a^2X_{T1}\sin^2(\theta) + (Z_a^2 - Z_b^2)X_{T2}\cos^2(\theta)}{[Z_a\cos(\theta) - X_{T2}\sin(\theta)][Z_b\cos(\theta) - X_{T1}\sin(\theta)] - Z_b^2} \\
Z_{13} = Z_{31} &= j \frac{Z_b\sin(\theta)(Z_b^2 - Z_a^2 - X_{T1}X_{T2})}{[Z_a\cos(\theta) - X_{T2}\sin(\theta)][Z_b\cos(\theta) - X_{T1}\sin(\theta)] - Z_b^2} \\
Z_{33} &= j \frac{Z_a(Z_a^2 - Z_b^2 - X_{T1}X_{T2})\sin(\theta)\cos(\theta) - Z_a^2X_{T2}\sin^2(\theta) + (Z_a^2 - Z_b^2)X_{T1}\cos^2(\theta)}{[Z_a\cos(\theta) - X_{T2}\sin(\theta)][Z_b\cos(\theta) - X_{T1}\sin(\theta)] - Z_b^2}
\end{aligned} \tag{5.7}$$

By transforming the relationship between the impedance matrix and the ABCD matrix, the ABCD matrix for ports 1 and 3 can be derived as follows:

$$\begin{aligned}
A &= \frac{Z_a(Z_a^2 - Z_b^2 - X_{T1}X_{T2})\sin(\theta)\cos(\theta) - Z_a^2X_{T1}\sin^2(\theta) + (Z_a^2 - Z_b^2)X_{T2}\cos^2(\theta)}{Z_b\sin(\theta)(Z_b^2 - Z_a^2 - X_{T1}X_{T2})} \\
B &= \frac{j}{2} \frac{Z_a^2X_{T1}X_{T2} + (Z_a^2 - Z_b^2)^2 - 2Z_b^2X_{T1}X_{T2} + [Z_a^2X_{T1}X_{T2} - (Z_a^2 - Z_b^2)^2]\cos(2\theta) + (X_{T1} + X_{T2})Z_a(Z_a^2 - Z_b^2)\sin(2\theta)}{Z_b\sin(\theta)(Z_b^2 - Z_a^2 - X_{T1}X_{T2})} \\
C &= -j \frac{[Z_a\cos(\theta) - X_{T2}\sin(\theta)][Z_b\cos(\theta) - X_{T1}\sin(\theta)] - Z_b^2}{Z_b\sin(\theta)(Z_b^2 - Z_a^2 - X_{T1}X_{T2})} \\
D &= \frac{Z_a(Z_a^2 - Z_b^2 - X_{T1}X_{T2})\sin(\theta)\cos(\theta) - Z_a^2X_{T2}\sin^2(\theta) + (Z_a^2 - Z_b^2)X_{T1}\cos^2(\theta)}{Z_b\sin(\theta)(Z_b^2 - Z_a^2 - X_{T1}X_{T2})}
\end{aligned} \tag{5.8}$$

To achieve the ideal match for the impedance converter, the following condition must be satisfied:

$$R_S - jX_S = \frac{AZ_L + B}{CZ_L + D} \tag{5.9}$$

Substituting $Z_L = R_L + jX_L$ into equation, and separating the real and imaginary parts, we get:

$$\begin{aligned}
jCX_LR_S - jCR_LX_S + DR_S - AR_L &= 0 \\
B + jX_LA - R_SR_LC - X_SX_LC + jX_SD &= 0
\end{aligned} \tag{5.10}$$

In these equations, R_S , R_L , X_S and X_L are known quantities determined by practical needs, and Z_a , Z_b , θ , X_{T1} and X_{T2} are the values to be calculated. Fortunately, once Z_a , Z_b , and θ are manually selected, the values of X_{T1} and X_{T2} can be calculated through the following analytical formulas:

$$\begin{cases} X_{T1} = \frac{C_1 + C_3 + \sqrt{2C_2}}{C_4}, \\ X_{T2} = \frac{C_5 + C_6 + \sqrt{2C_2}}{C_7}, \end{cases} \tag{5.11}$$

$$\begin{cases} X_{T1} = \frac{C_1 + C_3 - \sqrt{2C_2}}{C_4}, \\ X_{T2} = \frac{C_5 + C_6 - \sqrt{2C_2}}{C_7}, \end{cases}$$

where

$$\begin{aligned}
C_1 &= \\
&-4R_SX_LZ_a^2Z_b^2 - 2R_LX_SZ_a^2Z_b^2 + 4R_SX_LZ_b^4 - R_LX_SZ_b^4 \\
&+ 8R_SX_LZ_a^4\cos(2\theta) - 12R_SX_LZ_a^2Z_b^2\cos(2\theta) \\
&+ 4R_LX_SZ_a^2Z_b^2\cos(2\theta) + 4R_SX_LZ_b^4\cos(2\theta) \\
&- 2R_LX_SZ_a^2Z_b^2\cos(4\theta) + R_LX_SZ_b^4\cos(4\theta)
\end{aligned} \tag{5.12}$$

$$\begin{aligned}
C_2 = & -R_L R_s [Z_b^2 - 2Z_a^2 + Z_b^2 \cos(2\theta)]^2 \{8R_L R_s Z_a^4 - 4R_L^2 R_s^2 Z_b^2 - 4R_s^2 X_L^2 Z_b^2 \\
& - 4R_L^2 X_s^2 Z_b^2 - 4X_L^2 X_s^2 Z_b^2 - 16R_L R_s Z_a^2 Z_b^2 - 8X_L X_s Z_a^2 Z_b^2 - 4Z_a^4 Z_b^2 \\
& + 11R_L R_s Z_b^4 + 8X_L X_s Z_b^4 + 8Z_a^2 Z_b^4 - 4Z_b^6 \\
& + 4Z_b^2 [R_s^2 X_L^2 + R_L^2 (R_s^2 + X_s^2) - R_L R_s Z_b^2 + (X_L X_s + Z_a^2 - Z_b^2)^2] \cos(2\theta) \\
& + R_L R_s Z_b^4 \cos(4\theta) \}
\end{aligned} \tag{5.13}$$

$$\begin{aligned}
C_3 = & -4R_L^2 R_s Z_a^3 \sin(2\theta) - 4R_s X_L^2 Z_a^3 \sin(2\theta) + 4R_s Z_a^5 \sin(2\theta) \\
& + 4R_s Z_a R_L^2 Z_b^2 \sin(2\theta) - 2R_L R_s^2 Z_a Z_b^2 \sin(2\theta) \\
& + 4R_s X_L^2 Z_a Z_b^2 \sin(2\theta) - 2R_L X_s^2 Z_a Z_b^2 \sin(2\theta) + 2R_L Z_a^3 Z_b^2 \sin(2\theta) \\
& - 8R_s Z_a^3 Z_b^2 \sin(2\theta) - 2R_L Z_a Z_b^4 \sin(2\theta) \\
& + 4R_s Z_a Z_b^4 \sin(2\theta) + R_L R_s^2 Z_a Z_b^2 \sin(4\theta) + R_L X_s^2 Z_a Z_b^2 \sin(4\theta) \\
& - R_L Z_a^3 Z_b^2 \sin(4\theta) + R_L Z_a Z_b^4 \sin(4\theta)
\end{aligned} \tag{5.14}$$

$$\begin{aligned}
C_4 = & -4R_L^2 R_s Z_a^2 - 4X_L^2 R_s Z_a^2 - 4R_s Z_a^4 + R_L R_s^2 Z_b^2 + R_L X_s^2 Z_b^2 + 3R_L Z_a^2 Z_b^2 \\
& + 8R_s Z_a^2 Z_b^2 - 4R_s Z_b^4 \\
& + 4[R_L^2 R_s Z_a^2 - R_L Z_a^2 Z_b^2 + R_s X_L^2 Z_a^2 - R_s (Z_a^2 - Z_b^2)^2] \cos(2\theta) \\
& - R_L (R_s^2 + X_s^2 - Z_a^2) Z_b^2 \cos(4\theta) + 8R_s X_L Z_a^3 \sin(2\theta) \\
& - 8R_s X_L Z_a Z_b^2 \sin(2\theta) + 4R_L X_s Z_a Z_b^2 \sin(2\theta) - 2R_L X_s Z_a Z_b^2 \sin(4\theta)
\end{aligned} \tag{5.15}$$

$$\begin{aligned}
C_5 = & -2R_s X_L Z_a^2 Z_b^2 - 4R_L X_s Z_a^2 Z_b^2 + 4R_L X_s Z_b^4 - R_s X_L Z_b^4 \\
& + 8R_L X_s Z_a^4 \cos(2\theta) - 12R_L X_s Z_a^2 Z_b^2 \cos(2\theta) \\
& + 4R_s X_L Z_a^2 Z_b^2 \cos(2\theta) + 4R_L X_s Z_b^4 \cos(2\theta) \\
& - 2R_s X_L Z_a^2 Z_b^2 \cos(4\theta) + R_s X_L Z_b^4 \cos(4\theta)
\end{aligned} \tag{5.16}$$

$$\begin{aligned}
C_6 = & -4R_s^2 R_L Z_a^3 \sin(2\theta) - 4R_L X_s^2 Z_a^3 \sin(2\theta) + 4R_L Z_a^5 \sin(2\theta) \\
& + 4R_L Z_a R_s^2 Z_b^2 \sin(2\theta) - 2R_s R_L^2 Z_a Z_b^2 \sin(2\theta) \\
& + 4R_L X_s^2 Z_a Z_b^2 \sin(2\theta) - 2R_s X_L^2 Z_a Z_b^2 \sin(2\theta) \\
& + 2R_s Z_a^3 Z_b^2 \sin(2\theta) - 8R_L Z_a^3 Z_b^2 \sin(2\theta) - 2R_s Z_a Z_b^4 \sin(2\theta) \\
& + 4R_L Z_a Z_b^4 \sin(2\theta) + R_s R_L^2 Z_a Z_b^2 \sin(4\theta) + R_s X_L^2 Z_a Z_b^2 \sin(4\theta) \\
& - R_s Z_a^3 Z_b^2 \sin(4\theta) + R_s Z_a Z_b^4 \sin(4\theta)
\end{aligned} \tag{5.17}$$

$$\begin{aligned}
C_7 = & -4R_s^2 R_L Z_a^2 - 4X_s^2 R_L Z_a^2 - 4R_L Z_a^4 + R_s R_L^2 Z_b^2 + R_s X_L^2 Z_b^2 + 3R_s Z_a^2 Z_b^2 \\
& + 8R_L Z_a^2 Z_b^2 - 4R_L Z_b^4 \\
& + 4[R_s^2 R_L Z_a^2 - R_s Z_a^2 Z_b^2 + R_L X_s^2 Z_a^2 - R_L (Z_a^2 - Z_b^2)^2] \cos(2\theta) \\
& - R_s (R_L^2 + X_L^2 - Z_a^2) Z_b^2 \cos(4\theta) + 8R_L X_s Z_a^3 \sin(2\theta) \\
& - 8R_L X_s Z_a Z_b^2 \sin(2\theta) + 4R_s X_L Z_a Z_b^2 \sin(2\theta) - 2R_s X_L Z_a Z_b^2 \sin(4\theta)
\end{aligned} \tag{5.18}$$

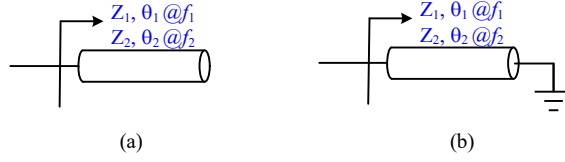


Fig. 5.6 Dual-band dual-reactance branch in different situations. (a) Open circuit. (b) Short circuit.

Equation (5.10) provides two possible solutions for X_{T1} and X_{T2} , to ensure these values are real, the condition $C_2 > 0$ must be met. For dual-band operation, parameters must consider both frequency bands. Setting Z_{0e} , Z_{0o} and θ_1 at frequency f_1 determines the parameters at f_2 as Z_{0e} , Z_{0o} and $\theta_2 = n\theta_1$ (where $n = f_2/f_1$). Then, X_{T1} and X_{T2} can be calculated.

A dual-band dual-reactance branch is created using either an open-circuit transmission line T_1 or a short-circuit transmission line T_2 . Each transmission line has different electrical lengths at two frequencies, resulting in different reactance at those frequencies. To choose between open-circuit or short-circuit lines, the shortest branch length should be selected. For designing the reactance components for a dual-frequency coupled line impedance converter, the first dual-frequency reactance branch must satisfy:

$$Z_{T1}(f) = \begin{cases} jX_{T11} @ f_1 \\ jX_{T12} @ f_2 \end{cases} \quad (5.19)$$

X_{T11} , X_{T12} , X_{T21} and X_{T22} are calculated using given parameters. The following sections explain the principles of using open-circuit and short-circuit transmission lines for these branches.

For an open circuit transmission line, the impedance of transmission line T_1 (electrical length θ_1 at frequency f_1) and transmission line T_2 (electrical length θ_2 at frequency f_2) will be:

$$\begin{aligned} Z_{T1}(f_1) &= -jZ_1 \cot \theta_1 @ f_1 \\ Z_{T1}(f_2) &= -jZ_1 \cot n\theta_1 @ f_2 \end{aligned} \quad (5.20)$$

Similarly, the impedance parameters for a short-circuit transmission line will change

to:

$$\begin{aligned} Z_{T2}(f_1) &= jZ_2 \tan \theta_2 @ f_1 \\ Z_{T2}(f_2) &= jZ_2 \tan n\theta_2 @ f_2 \end{aligned} \quad (5.21)$$

The final step in designing a dual-band couple-line impedance converter is to connect the two dual-band dual-reactance branches to the two junctions of the couple-line, as shown in Fig. 5.5. When the two junctions of the coupled line are connected to the reactance loads corresponding to the two frequencies, the remaining two ports can perform the required impedance transformation. Specifically, at the first frequency f_1 , the load impedance Z_L is converted to Z_{in1} , and Z_L is converted to Z_{in2} at f_2 . This achieves the dual-band impedance matching network.

5.3. 60GHz and 77GHz power amplifier design

In designing a PA, it is crucial to start by determining the size of the MOSFET and the bias voltage based on the specific application requirements. For our design, utilizing the TSMC 40nm CMOS technology, we aim to achieve an output power of 10dBm for signal transmission at 77GHz. Accordingly, we have selected a transistor for the output amplification stage with a gate width of 72 μ m.

To ensure optimal performance, we conducted load pull simulations for the transistor at two frequencies: 60GHz and 77GHz. These simulations enabled us to identify the optimal matching impedances for each frequency, which are essential for maximizing the PA's efficiency and output power. The optimal impedance at 60GHz is (22.1+j18.5) Ω , and the optimal impedance at 77GHz is (19.5+j19.35) Ω .

Based on the optimal impedance values obtained from the load pull simulations, we proceeded with the design of the coupled transmission lines. We selected an odd-mode characteristic impedance of 40 Ω and an even-mode characteristic impedance of 120 Ω . Through careful calculations, we determined θ_1 to be 40° and θ_2 to be 51.3°. Using these

Table 5.1. Parameter of Coupler-based Dual-band Matching Network

	Z_{0e}	Z_{0o}	$\theta_1 @ f_1$	$\theta_2 @ f_2$	X_{T11}	X_{T12}	X_{T21}	X_{T22}
Input matching	120 Ω	40 Ω	45	57.75	-45.03	-13.17	-50.07	-31.59
Output matching	120 Ω	40 Ω	40	51.3	-47.15	-18.22	-53.21	-21.71

Table 5.2. Parameter of Dual-band Dual-reactance Branch

	Z_0	$\theta_1 @ f_1$	$\theta_2 @ f_2$	Width/length (μm)
Input matching T_1	90.6	63.6	81.62	1.55 / 622.5
Input matching T_2	49.5	44.7	57.36	6.57/437.4
Output matching T_1	82	60	77	2.13 / 615.6
Output matching T_2	92	60	77	1.46 / 623.5

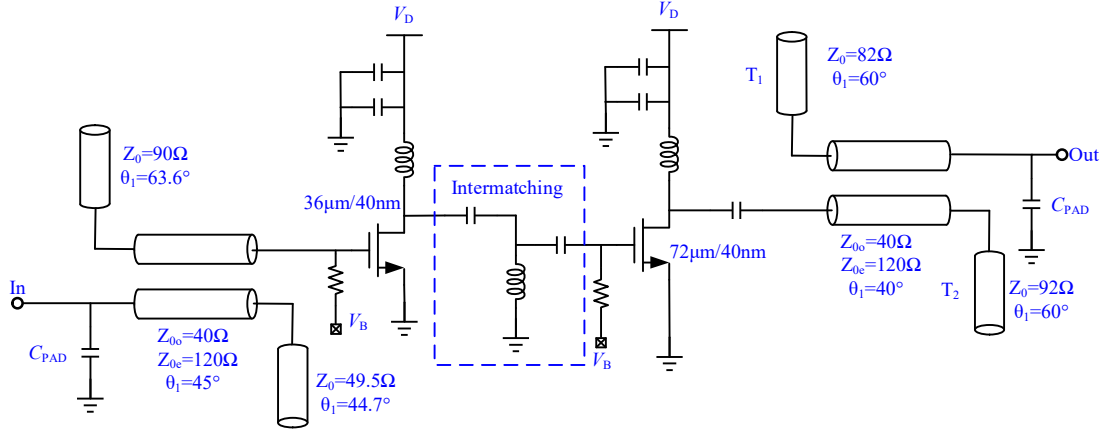


Fig. 5.7 Circuit diagram of the proposed dual-band PA.

angles and the previously established formulas, we computed the values for X_{T11} , X_{T12} , X_{T21} , and X_{T22} , which are detailed in Table 5.1.

Additionally, the design includes single-section transmission lines, with specific values listed in Table 5.2. For instance, T_1 has a characteristic impedance of 82 Ω and an electrical length of 60°, while T_2 has a characteristic impedance of 92 Ω and an electrical length of 60°. We used metal layer M_6 for the design of the coupling lines, with metal layer M_1 serving as the ground. Based on TSMC's substrate material and metal layer information, we determined the width of the designed coupling line to be 1.6 μm , with T_1 and T_2 having widths of 2.1 μm and 1.5 μm , respectively. For input matching, we employed a conjugate matching approach, utilizing a similar design method for the coupling line as used for the output matching.

The complete circuit diagram of the designed two-stage PA is illustrated in Fig. 5.7.

Furthermore, the post-simulation of S-parameter and large-signal results are presented in Fig. 5.8 and Fig. 5.9.

The simulation results exhibit impressive performance metrics, showcasing power gains of 12.4 dB at 60GHz and 9.8 dB at 77GHz. In the S parameter results, two obvious troughs can be seen in S_{11} and S_{22} at 60 GHz and 77 GHz, which validates the theory of coupler-based dual-band matching structure proposed in this section. The saturated output power achieved are 12 dBm at 60GHz and 10 dBm at 77GHz, with the power added efficiency of 24.4% and 13.85%, respectively. These results confirm the PA's capability to meet the design specifications and deliver the required output power.

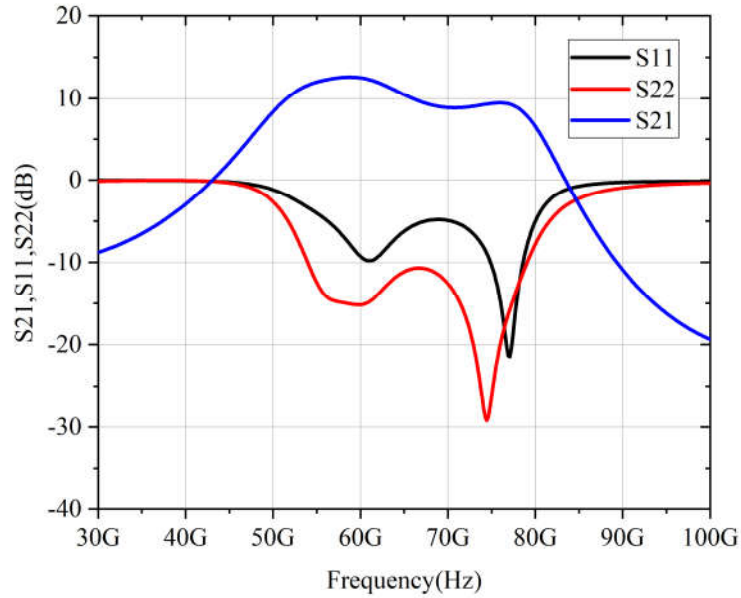


Fig. 5.8. Simulation S parameter results of the proposed PA.

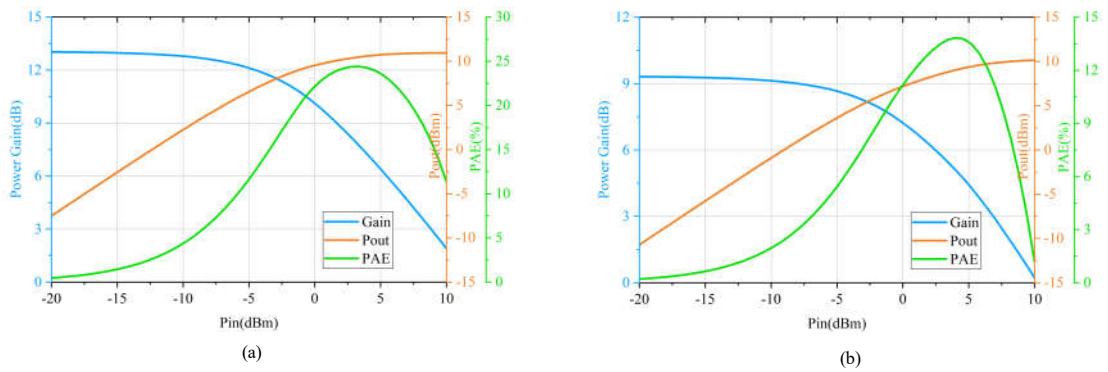


Fig. 5.9. Simulation Large signal performance of the proposed PA. (a) 60GHz. (b) 77GHz.

5.4. Experimental results

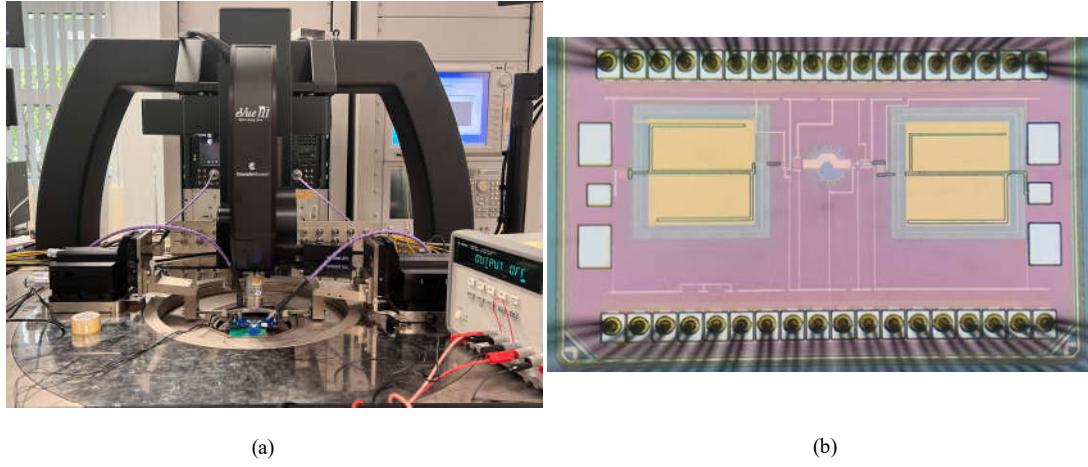


Fig. 5.10. Measurement platform and chip photograph.

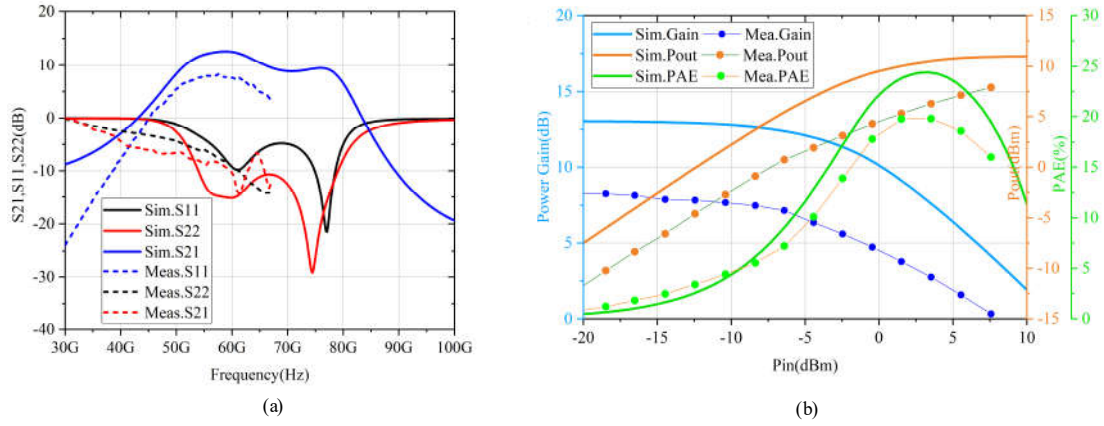


Fig. 5.11. (a) S parameter measurement results (b) large signal measurement results below 67GHz.

Table 5.3. Performance Summary and Comparison

	This work	[47]	[55]	[57]
Technology	40nm	65nm	45nm	28nm
Frequency (GHz)	52-64	60	60	72-89
Supply (V)	1.1	1	2	0.9
Power Gain (dB)	9	21	23.9	11.4-17
P_{sat} (dBm)	8	6.95	29.1	12.15
P_{1dB} (dBm)	4	3.7	24.7	14
Peak PAE	18%	8.4%	18.4%	7.2-12%
Active Area (mm ²)	0.45	0.3	6.6	0.178

To test the designed PA, a small-signal test system was constructed, as illustrated in the figure. The Keysight PNA-X N5247B was used as the signal generator, and the probes employed were infinity probes with GSG of 150 μ m pitch. After calibrating the VNA and the probes, the system was capable of measuring S-parameters in the frequency range of 10MHz to 67GHz. However, due to the absence of a VNA extender

for the 67GHz-110GHz range, testing beyond 67GHz was not feasible. Therefore, this section presents test results only for frequencies below 67GHz.

Fig. 5.10 shows the setup of the test platform and the die photograph of the chip. The chip has an area of $0.7\text{mm} \times 1.1\text{mm}$, with a core area of $0.5\text{mm} \times 0.9\text{mm}$. Fig. 5.11 presents the small-signal test results of the chip. From the results, it is evident that the power gain exhibits a significant decline, which could be attributed to several factors:

1) Substrate modeling accuracy: As this was the first time using this process for fabrication, the substrate modeling might not be entirely accurate. This could lead to discrepancies between the designed and actual performance of the couple-line impedance converter, affecting the matching results.

2) Transmission line design: The designed transmission lines may have widths that are too narrow, and the addition of metal dummies could introduce substantial losses, leading to a considerable deviation in the final power gain.

The small-signal test results indicate that the peak power gain of the PA is 8dB, with a 3dB bandwidth ranging from 52GHz to 64GHz. Due to testing limitations, results for frequencies above 67GHz were not obtained. The proposed PA shows a P_{sat} of 8dBm, PAE of 18% in the large signal measurement.

Based on the results, this design method presents several issues that need to be clarified:

- 1) Lack of Differential Structure: This design does not employ a differential structure, which means it cannot effectively suppress common-mode noise, resulting in poor interference immunity.
- 2) Large Circuit Size: The use of transmission line structures for matching leads to a relatively large overall circuit size, thereby reducing the power density of the

entire chip.

- 3) Limitations in CMOS Process: In the CMOS process, the DRC rules and metal width limitations restrict the characteristic impedance of the transmission lines that can be designed. The structure mentioned in the document may not be feasible.

Table 5.3 has listed the comparison between this work and prior art works. As shown in the table, this work supports dual-band operation at both 60GHz and 77GHz, which are critical for automotive radar applications, while most previous works focus on a single frequency band. The proposed design utilizes a novel dual-band coupled-line impedance matching structure, offering efficient impedance transformation and compact layout. The amplifier achieves comparable output power and PAE with a smaller chip area (0.45 mm^2), which is advantageous for dense integration in multi-channel radar systems.

After simulation and testing, we believe that this structure is more suitable for GaN technology. Since GaN technology typically has only two metal layers, transmission lines are commonly used for matching in GaN PA designs.

Moreover, GaN materials offer high power density and gain, which can effectively address the losses caused by the coupler-based structure mentioned in the document and achieve wideband matching.

5.5. Summary

This chapter discusses the design and development of dual-band PAs for 60GHz and 77GHz, crucial for automotive radar systems in ADAS and autonomous driving. The design utilizes a coupled-line dual-frequency matching structure, with innovative input and output matching networks. Impedance matching is critical, achieved through dual-

frequency impedance converters that operate at two distinct frequencies, transforming load impedance for optimal performance. The layout of the coupled microstrip line for output matching is illustrated, with electromagnetic simulation results. The two-stage PA shows power gains of 12.4 dB at 60GHz and 9.8 dB at 77GHz, with output power of 12 dBm at 60GHz and 10 dBm at 77GHz, and power-added efficiencies of 24.4% and 13.85%, respectively. A small-signal test system was constructed using the Keysight PNA-X N5247B and infinity probes with a GSG spacing of 150 μ m. Testing was limited to below 67GHz due to equipment constraints. Test results indicated a decline in power gain due to substrate modelling inaccuracies and transmission line design issues. The PA's peak power gain was 8dB, with a 3dB bandwidth from 52GHz to 64GHz, P_{sat} of 8dBm and the peak PAE of 18%.

Chapter 6. D band Power Amplifiers Design for FMCW radar system

The advent of millimeter-wave technology has opened new horizons in the field of radar systems, offering exceptional resolution and precision that are essential for modern applications. The D-band, in particular, presents a compelling frequency range for the development of advanced radar systems due to its unique propagation characteristics and potential for high data rate transmission. However, the design of PAs for operation in the D-band is fraught with challenges, including the need for high linearity, efficiency, and output power within the constraints of modern semiconductor processes.

FMCW radar systems modulate a continuous wave signal in frequency and analyze the beat frequency of the transmitted and received signals to determine the range and velocity of targets. The PA is a key component in this process, as it must provide the necessary amplification to ensure the transmitted signal has the power required to penetrate the environment, illuminate the target, and return with sufficient strength for detection.

The primary purpose of this chapter is to present a comprehensive approach to the design of D-band power amplifiers for FMCW radar systems. This chapter introduces innovative concepts, such as T-shape embedding networks for gain boosting in millimeter-wave amplifiers, which are critical for optimizing the bandwidth and performance of the PAs. It also presents a detailed design of a D-band power amplifier, incorporating an 8-shaped transformer for impedance matching, which is a novel solution to the impedance matching challenges at high frequencies. Simulation and experimental results are given to validate the designed PAs against the benchmarks of high-frequency radar applications. These results are essential for ensuring that the designed PAs can meet the demanding requirements of FMCW radar systems.

6.1. System Requirements and Amplifier Design Overview

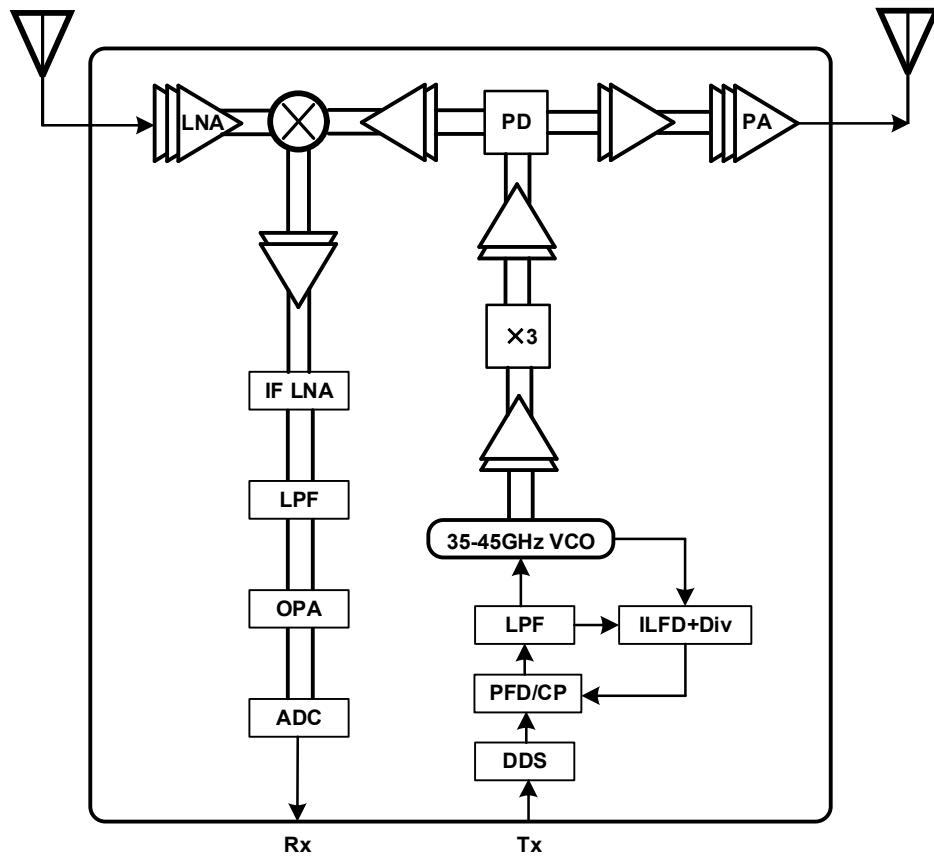


Fig. 6.1 A standard FMCW radar system structure.

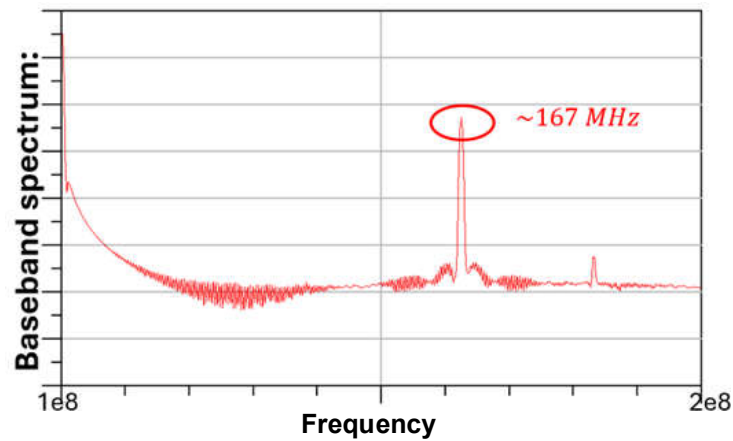


Fig. 6.2. Simulated performance of the standard FMCW radar system with 50 m target.

The architecture of a standard FMCW radar system shown in Fig. 6.1 is elegant in its simplicity, featuring a single transmitter and receiver. This configuration is widely adopted in radar engineering due to its efficiency and reliability. The system is

engineered to operate at millimeter-wave and high frequencies, which are crucial for achieving the precision and resolution required for modern radar applications. ADS is utilized to simulate the radar system's performance with a target at a specified distance, for instance, 50 meters. These simulations are critical as they offer insights into the system's detection and tracking capabilities in a controlled environment. A crucial aspect of these simulations is the relationship between the de-chirped spectrum frequency and the target distance, encapsulated by (6.1), where c means speed of light. With a chirp slope set at 500 MHz/ μ s, the resultant baseband frequency f_{Baseband} is determined to be 167 MHz, which is vital for signal processing and analysis.

$$f_{\text{Baseband}} = \frac{(2 \times \text{Distance})}{c} \times \text{Chirp}^\circ \text{slope} \quad (6.1)$$

In the context of short- to mid-range FMCW radar systems, the transmitted signal typically spans a wide frequency sweep (e.g., 20–30 GHz), and the PA must therefore maintain sufficiently flat gain and efficient power delivery across the entire sweep. Considering the limited power gain and high output impedance of nanoscale CMOS transistors operating at D-band, the design must employ multi-stage amplification and careful matching to achieve acceptable power output and energy efficiency.

To address these requirements, this work targets a three-stage D-band power amplifier architecture designed and fabricated using a 28-nm CMOS process. The design goals are tailored for integration into a radar transmitter front-end with the following key specifications:

Output Power Target: ≥ 5 dBm across 110–140 GHz

Power-Added Efficiency (PAE): $\geq 10\%$ at peak output

Small-Signal Gain: ≥ 13 dB to ensure sufficient drive for radiation

3-dB Bandwidth: ≥ 15 GHz, covering full FMCW sweep.

6.2. Gain boosting principle of T-shape embedding networks

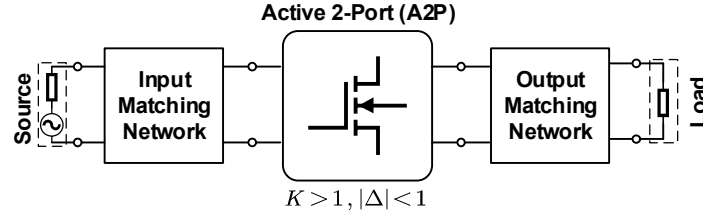


Fig. 6.3. Simplified diagram of the power amplifier.

The pursuit of high gain mmWave amplifiers has led to significant advancements in embedding network designs that enhance the power gain of amplifiers. Traditional gain-boosting techniques involve embedding networks that leverage the inherent properties of transistors to achieve maximum gain. When analyzing different impedance conditions for the transistor's 2-port network, three fundamental power gains are defined: Maximum Achievable Gain ($G_{\max}$), Maximum Available Gain (MAG), and Unilateral Power Gain (U). Below gives the detailed definition and expressions of them.

MAG is defined as the ratio of the available power from the output port of the two-port to the available power from the source and is the highest gain that a transistor can achieve when it is conjugately matched at both the input and output. It assumes the device is unconditionally stable (i.e., it remains stable for all possible passive source and load impedances). Fig. 6.3 presents the circuit diagram of a transistor-based two-port network with its matching network, designed to be unconditionally stable. The black box in the center represents the active part composed of the transistor. The conditions for unconditional stability, given as $k > 1$ and $|\Delta| < 1$, are provided below the diagram.

Once these conditions are satisfied, the expression for the MAG is given as:

$$MAG = \frac{|S_{21}|^2 (1 - |\Gamma_s|^2)}{(1 - |\Gamma_{out}|^2) |1 - S_{11} \Gamma_s|^2} \quad (6.2)$$

U is the gain of a transistor when the reverse transmission coefficient S_{12} is assumed

to be zero. This simplifies the design process by neglecting the feedback from the output to the input. The calculation of U is straightforward, as it does not take into account the feedback path. This gain parameter is often used for a preliminary evaluation of a transistor's gain performance. Although this assumption simplifies the analysis and design process, it may not always be accurate in real-world applications where feedback effects are present.

$$U = \frac{(1 - |\Gamma_L|^2) |S_{21}|^2 (1 - |\Gamma_S|^2)}{|1 - S_{22}\Gamma_L|^2 |1 - S_{11}\Gamma_S|^2} \quad (6.3)$$

$G_{\max}$ represents the highest possible gain that a transistor can achieve, considering stability constraints and potential mismatch at the input or output. In other words, when the core satisfies

$$\cos(\theta^A) = -1, \quad k = 1 \quad (6.4)$$

Which means embedding a tunable linear-lossless-reciprocal (LLR) embedding network and match the input and output, $G_{\max}$ can be conducted as:

$$G_{\max} = (2U - 1) + 2\sqrt{U(U - 1)} \quad (6.5)$$

From the equation, we can see that $G_{\max}$ is a function of U , is an inherent characteristic of any active 2-port network. $G_{\max} \approx 4U$ when $U \gg 1$. Fig. 6.4 has shown the MAG, U and $G_{\max}$ of the $45\mu\text{m}$ transistor biased in linear region in TSMC 28nm CMOS process. In the sub-THz frequency range, the difference between $G_{\max}$ and U becomes more pronounced and significant. This indicates that at such high frequencies, techniques for gain enhancement are not only necessary but also hold great potential.

Fig 6.5 has presented the gain plane of $G_{\max}$ to U/A , to design a suitable LLR network to achieve $G_{\max}$, this involves moving the green spot of a given MOSFET on the gain plane to the black spot at $(-1/4, 0)$. But in [61], a simple parallel passive network cannot achieve $G_{\max}$ from an arbitrary transistor. The necessary condition for high gain

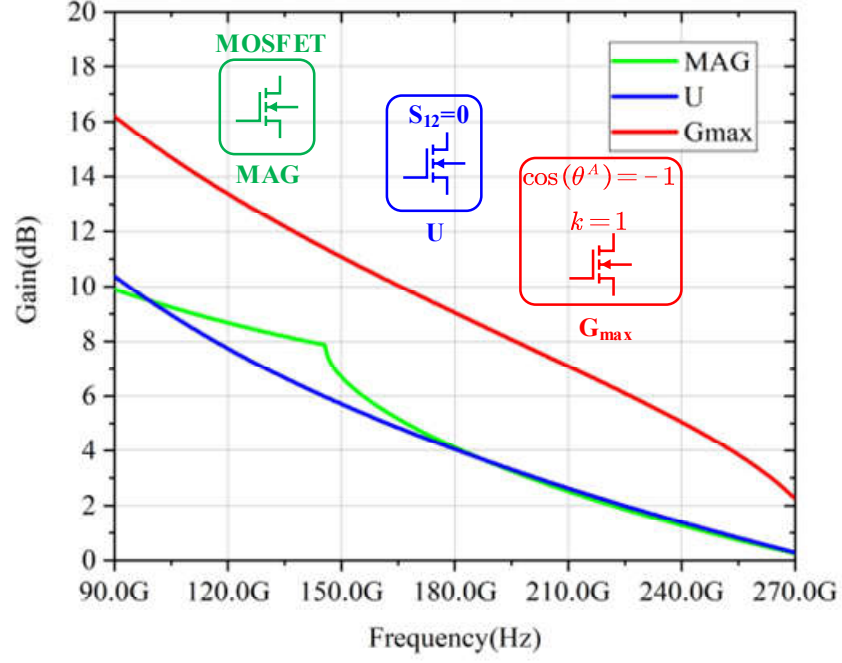


Fig. 6.4 The MAG, U and $G_{\max}$ of the 45 μ m transistor in TSMC 28nm CMOS process.

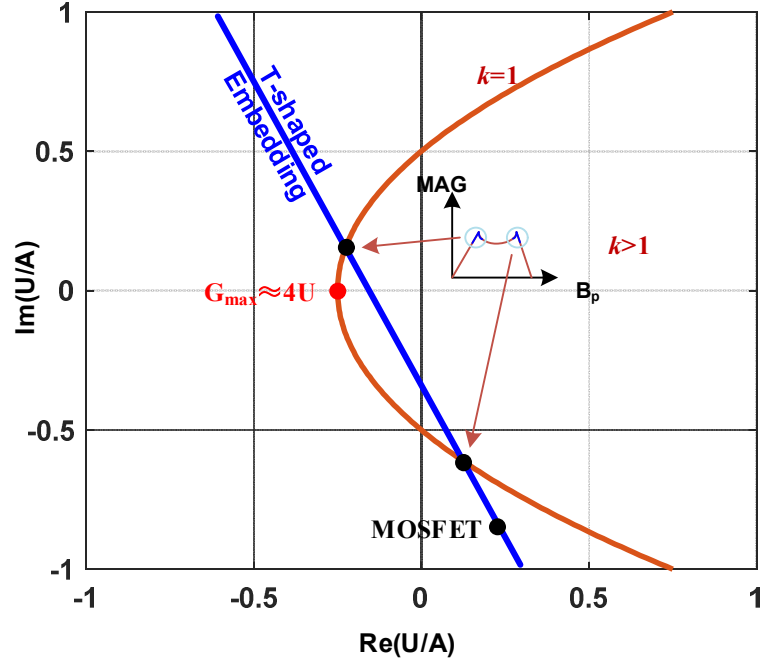


Fig. 6.5 Gain plane and dual-peak conditions of the embedding network.

amplifiers are represented by a blue parabola, with the transistor's movement depicted as a red line based on the assumption $Y_{21}^{LLR}/Y_{21}^{mos} \ll 1$, then the gain plane equation is:

$$\left(\operatorname{Im}\left(\frac{U}{A}\right)\right)^2 = \operatorname{Re}\left(\frac{U}{A}\right) + \frac{1}{4} \quad (6.6)$$

The relationship involving U/A for the LLR embedding network, is $\frac{U}{A} \approx \frac{UY_{12}^{\text{mos}}}{Y_{21}^{\text{mos}}} + \frac{jUB_p}{Y_{21}^{\text{mos}}}$, where $Y_{21}^{\text{LLR}} = jB_p$. Traditional single-peak designs often fall short in bandwidth performance. A novel approach involves the use of T-shaped embedding networks to create dual-peak G_{max} cores.

The T-shaped embedding network provides significant flexibility in design, allowing for manipulation of both the gain profile and input/output impedances. This flexibility is critical for achieving broadband matching and optimizing amplifier performance across a wide frequency range. The dual-peak condition for the T-shaped network is derived from the Y-parameters of the amplifier core, ensuring that the network meets specific impedance and admittance criteria at different frequencies. For a T-shaped embedding network, the dual-peak conditions can be derived from the following quadratic equations:

$$\begin{aligned} B_{p1} &= \frac{-b - \sqrt{b^2 - 4ac}}{2a} \\ B_{p2} &= \frac{-b + \sqrt{b^2 - 4ac}}{2a} \end{aligned} \quad (6.7)$$

where

$$\begin{aligned} a &= \left(\operatorname{Re}\left(\frac{U}{Y_{21}^{\text{mos}}}\right)\right)^2 \\ b &= 2\operatorname{Im}\left(\frac{UY_{12}^{\text{mos}}}{Y_{21}^{\text{mos}}}\right)\operatorname{Re}\left(\frac{U}{Y_{21}^{\text{mos}}}\right) + \operatorname{Im}\left(\frac{U}{Y_{21}^{\text{mos}}}\right) \\ c &= \left(\operatorname{Im}\left(\frac{UY_{12}^{\text{mos}}}{Y_{21}^{\text{mos}}}\right)\right)^2 - \left(\frac{1}{4} + \operatorname{Re}\left(\frac{UY_{12}^{\text{mos}}}{Y_{21}^{\text{mos}}}\right)\right). \end{aligned} \quad (6.8)$$

These conditions ensure that the network can support two distinct gain peaks at frequencies ω_1 and ω_2 , enhancing the overall bandwidth, shown by (6.7) and (6.8). The

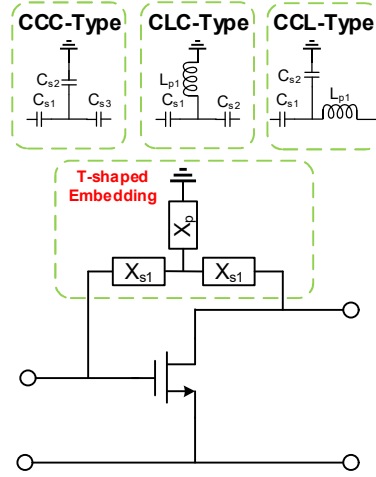


Fig. 6.6. Schematic of three types of the T-shaped embedding network.

choice of these reactance is critical in determining the dual-peak behavior of the amplifier.

$$Y_{12}^{\text{LLR}}(\omega_1) = jB_{p1} \text{ and } Y_{12}^{\text{LLR}}(\omega_2) = jB_{p2} \quad (6.9)$$

$$Y_{12}^{\text{LLR}}(\omega_2) = jB_{p1} \text{ and } Y_{12}^{\text{LLR}}(\omega_1) = jB_{p2} \quad (6.10)$$

The proposed T-shaped embedding networks are shown in Fig 6.7. The Y_{12} of the T-shaped embedding network is calculated as:

$$Y_{12}^{\text{LLR}} = j \frac{X_p}{X_p X_{s1} + X_p X_{s2} + X_{s1} X_{s2}} \quad (6.11)$$

Where X_{s1} , X_{s2} , and X_p are the reactance of the two series components and one shunt component, respectively. We exclude configurations with two or more inductors due to the need for additional components to separate the bias for the gate or drain. Based on this equation, the Y_{12}^{LLR} for each case is calculated.

For $C_{s1} - C_p - L_{s2}$ case, by using the dual-peak conditions, C_{s1} , C_p , and L_{s2} can be determined through the following relationships:

$$L_{s2} + \frac{L_{s2} C_p}{C_{s1}} = \frac{1}{\omega_1 B_{p1}} + \frac{1}{\omega_1^2 C_{s1}} \quad (6.12)$$

$$C_{s1} = \frac{1/\omega_1^2 - 1/\omega_2^2}{1/(\omega_2 B_{p2}) - 1/(\omega_1 B_{p1})} \quad (6.13)$$

For $C_{sl} - C_p - C_{s2}$ case, using a similar derivation method, the dual-peak conditions for this configuration are simplified to:

$$\frac{\omega_1}{B_{p1}} = - \left(\frac{1}{C_{s1}} + \frac{1}{C_{s2}} + \frac{C_p}{C_{s1}C_{s2}} \right) \quad (6.14)$$

$$\frac{\omega_1}{B_{p1}} = \frac{\omega_2}{B_{p2}} \quad (6.15)$$

For $C_{s1} - L_p - C_{s2}$ case, the dual-peak conditions for this configuration are derived as follows:

$$\frac{1}{C_{s1}} + \frac{1}{C_{s2}} = \frac{B_{p1}\omega_2^3 - B_{p2}\omega_1^3}{B_{p1}B_{p2}(\omega_1^2 - \omega_2^2)} \quad (6.16)$$

$$\frac{1}{L_p} = C_{s1}C_{s2} \left(\frac{\omega_1^3}{B_{p1}} + \frac{\omega_1^2}{C_{s1}} + \frac{\omega_1^2}{C_{s2}} \right) \quad (6.17)$$

By considering these conditions, we can effectively design an LLR embedding network that achieves the desired dual-peak MAG, enhancing the overall gain and bandwidth performance of the amplifier.

Based on the provided descriptions, the $C_{s1} - L_p - C_{s2}$ configuration is chosen over the $C_{s1} - C_p - L_{s2}$ and $C_{sl} - C_p - C_{s2}$ configurations due to its practical and feasible solutions for achieving dual-peak Gmax. The $C_{sl} - C_p - C_{s2}$ configuration limits the designer's flexibility because the ratio of the peak gain frequencies is dictated by formula (6.15), and it fails to provide a general solution when B_{p1} can be negative. On the other hand, the $C_{s1} - C_p - L_{s2}$ configuration requires a C_{sl} value of approximately 1.4 fF at D-band frequencies for the chosen 28-nm CMOS transistor, which is impractical due to fabrication tolerances. In contrast, the $C_{s1} - L_p - C_{s2}$ configuration allows for the adjustment of the inductance and capacitance ratios to achieve dual-peak Gmax and provides flexibility in tuning the input and output

impedances, which is beneficial for broadband matching circuit design. Therefore, the $C_{s1} - L_p - C_{s2}$ configuration is preferred for its ability to overcome manufacturing and design limitations while offering greater design flexibility and implementable component parameters.

In $C_{s1} - L_p - C_{s2}$ configuration, the Y_{11} and Y_{22} of the T-shaped embedding network are given by:

$$Y_{11}^T = j \frac{\omega C_{s1} (\omega^2 C_{s2} L_p - 1)}{\omega^2 C_{s1} L_p + \omega^2 C_{s2} L_p - 1} \quad (6.18)$$

$$Y_{22}^T = j \frac{\omega C_{s2} (\omega^2 C_{s1} L_p - 1)}{\omega^2 C_{s1} L_p + \omega^2 C_{s2} L_p - 1} \quad (6.19)$$

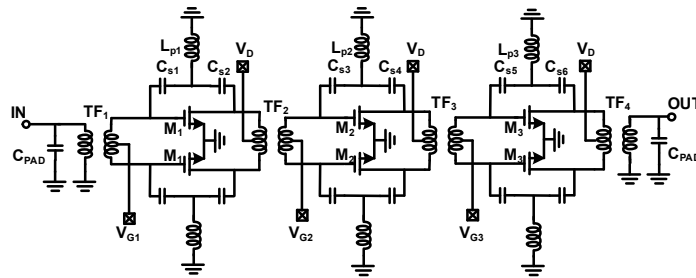
Therefore, the input and output admittances of the dual-peak core are expressed as:

$$Y_{in} = Y_{11}^{mos} + Y_{11}^T - \frac{(Y_{21}^{mos} + Y_{12}^T)(Y_{12}^{mos} + Y_{22}^T)}{Y_{22}^{mos} + Y_{22}^T + Y_o} \quad (6.20)$$

$$Y_{out} = Y_{22}^{mos} + Y_{22}^T - \frac{(Y_{21}^{mos} + Y_{12}^T)(Y_{12}^{mos} + Y_{22}^T)}{Y_{11}^{mos} + Y_{11}^T + Y_o} \quad (6.21)$$

Based on the analysis above, the PA design will be presented in Section 6.3.

6.3. D Band Power Amplifier Design



$L_{p1}=55p$	$C_{s1}=12.2f$	$C_{s2}=5.7f$	$M_1:21.6um/30nm$
$L_{p2}=60p$	$C_{s3}=7.8f$	$C_{s4}=4.7f$	$M_2:21.6um/30nm$
$L_{p3}=65p$	$C_{s5}=5.7f$	$C_{s6}=6.8f$	$M_3:45um/30nm$
$TF_1:34p/46p \quad k=0.6$		$TF_2:32p/34p \quad k=0.68$	
$TF_3:45p/37p \quad k=0.27$		$TF_4:18p/19p \quad k=0.7$	

Fig. 6.7. Schematic and design parameters of the proposed D band power amplifier.

In this section, we detailed the design of the PAs that the radar transceiver required in a 28nm TSMC CMOS process. The first step is to determine the size and bias voltage of the MOSFETs based on the specific application requirements. According to the previous section's description of the entire radar transceiver and its parameters, our PA design aims to deliver an output power of 5dBm with an input P_{1dB} of -5dBm for signal transmission in TSMC 28nm CMOS process. Therefore, we selected a transistor with a gate width of 45 μ m for the output amplification stage.

Given the high-frequency operation in the D band, where the G_{max} of the transistor is inherently low, designing an efficient PA poses significant challenges. To address this, careful selection of the transistor's finger width is crucial to achieve the maximum G_{max} . Based on the simulations, we determined that the optimal finger width for the transistor in the output amplification stage is 500nm. And also, we have selected 0.6V as the gate voltage. This value was chosen to ensure optimal performance, balancing between achieving a high G_{max} and maximizing the g_m of the transistor.

According to the requirements of the radar transceiver, we have chosen 110 GHz and 130 GHz as the dual frequencies for our design. Following the analysis and formulas of the CLC embedding network discussed in the previous section and literature [61], we designed the corresponding CLC embedding network for each stage of the transistor. Fig. 6.8 shows the post-simulation results of G_{max} for each stage of the three-stage power amplifier we designed.

In designing this power amplifier, we employ magnetically coupled resonator (MCR) matching network for impedance matching. After the optimal load impedance is determined by the load pull simulation under certain input power and bias voltages, a symmetrical MCR is designed following the method from literature [102]. Then the coupling coefficient (k), the primary coil inductance (L_1), and the secondary coil

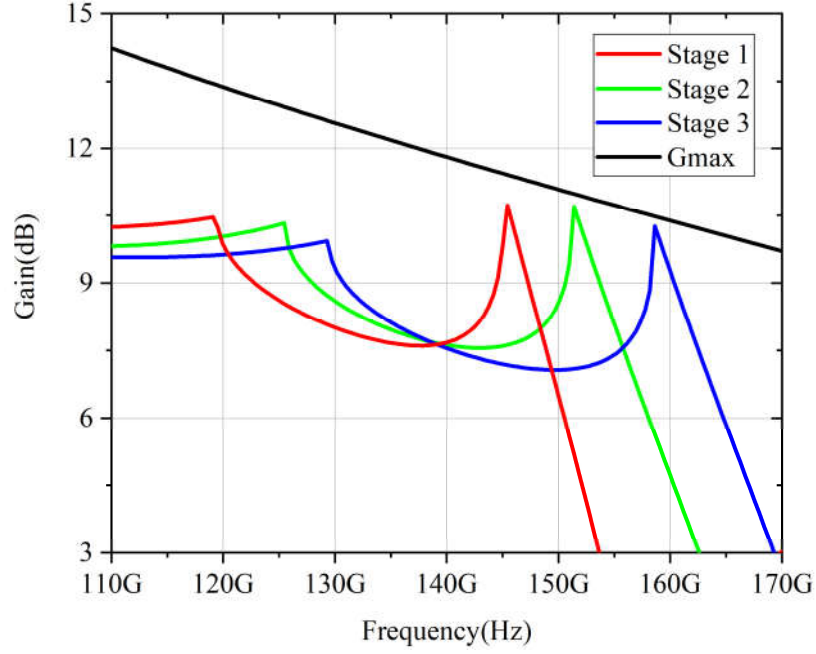


Fig. 6.8 post-layout simulation results of $G_{\max}$ for each stage of the three-stage power amplifier.

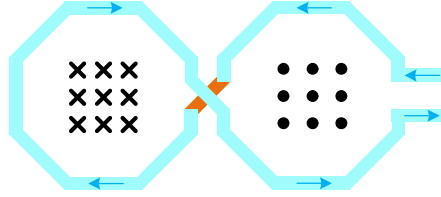


Fig. 6.9. Magnetic field distributions of a typical 8-shaped inductor.

inductance (L_2) of the MCR is determined. The design of sub-THz PAs, particularly in the D-band, imposes stringent requirements on impedance transformation structures. These requirements include broadband impedance matching, high magnetic coupling, minimal insertion loss, and compact layout suitable for mmWave application. Traditional stacked transformers based on octagonal or circular inductors often face several limitations when pushed into the sub-THz regime: narrow bandwidth due to limited coupling flexibility, increased insertion loss from long interconnects, and inefficient use of silicon area.

To address these constraints, recent studies, notably by Jia *et al.*, have introduced and analyzed the 8-shaped inductor as a superior alternative. This geometry inherently provides opposite magnetic flux paths within the same layout footprint,

shown in Fig. 6.9. 8-shaped inductor also enables better field confinement, shows enhanced immunity to electromagnetic interference (EMI), and the ability to modulate coupling coefficients by geometric shaping alone.

In this work, we propose a novel transformer topology that integrates the 8-shaped inductor into a vertically stacked transformer configuration. Specifically, one layer comprises an 8-shaped inductor while another layer maintains a conventional octagonal winding. This arrangement retains the mutual inductive benefits of the stacked transformer while leveraging the field-shaping and coupling flexibility of the 8-shaped geometry. By adjusting the lateral offset and loop dimensions, the coupling coefficient can be finely tuned without increasing interlayer spacing, thereby maintaining layout compactness.

To validate the proposed structure, EM simulations were carried out using ANSYS HFSS for both the proposed stacked 8-shaped transformer and a conventional stacked octagonal transformer, each with comparable metal layer definitions and target inductance values. Fig.6.10 (a) and (b) show the layout comparison between the two topologies, which a 40% reduction in layout area can be calculated by $[1 - (59.4 \times 37.4) / (77 \times 50.6)]$. Fig.6.10 (c), (d), (e) present the parameters of the two transformers from 110 to 170GHz.

Fig. 6.11 illustrates the simulated insertion loss of the two transformer structures. While the 8-shaped transformer exhibits a slightly higher loss of approximately 0.3 dB compared to the conventional design, this is primarily due to the slightly lower Q -factor of the 8-shaped inductor. However, this drawback is offset by a substantial 40% reduction in layout area, making it highly advantageous for dense integration. The smaller footprint also reduces parasitic coupling to surrounding structures and simplifies the layout of interstage and output matching networks.

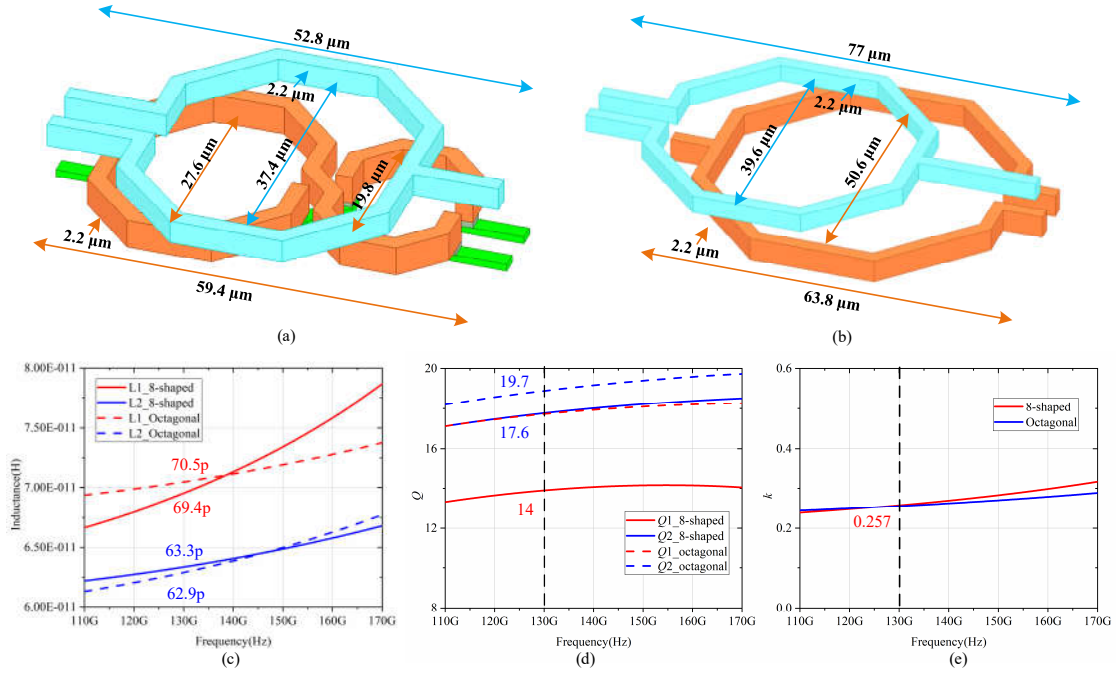


Fig. 6.10. 3-D layout of (a) 8-shaped transformer, (b) Octagonal transformer, and EM simulation results of an 8-shaped transformer and an octagonal transformer, (c) $L_1 = 69.4\text{pH}$ and $L_2 = 63.3\text{pH}$, (d) Q value, (e) $k=0.257$.

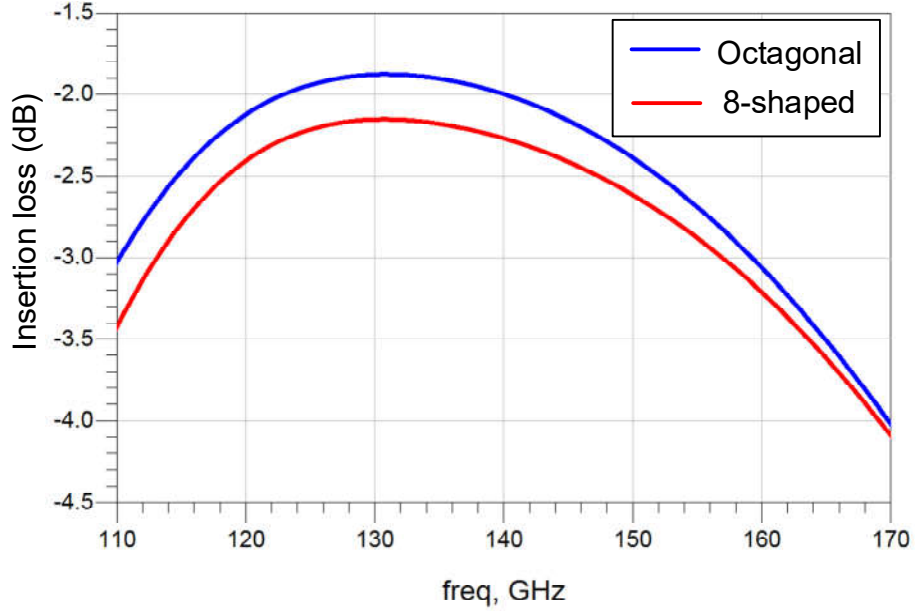


Fig. 6.11. Insertion loss of the 8-shaped transformer and the octagonal transformer.

Beyond the mentioned senerio above, the proposed 8-shaped stacked transformer is also particularly well-suited for scenarios requiring big difference between the primary and secondary inductors while maintaining large coulping factors. In conventional

transformer designs, achieving high coupling under large inductance mismatch is challenging. Normally auxiliary leakage inductors or complex layout folding will be added, which increase design effort and chip area.

In contrast, the 8-shaped transformer architecture allows the primary and secondary inductors to be independently shaped and laterally offset, enabling precise control over the inductance ratio while preserving strong magnetic coupling. This flexibility greatly simplifies the design process for impedance networks requiring unbalanced transformation. Fig. 6.12 shows the 3D layout and simulation results of an 8-shaped transformer with $L_1 = 30\text{pH}$ and $L_2 = 70\text{pH}$, $k=0.7$. While no direct comparison with conventional transformers is provided for this asymmetric case, the resulting structure demonstrates similar advantages to the former scenario. The proposed 8-shaped transformers are integrated into a three-stage D-band PA in later sections, demonstrating broadband matching and enhanced power gain over a wide frequency span.

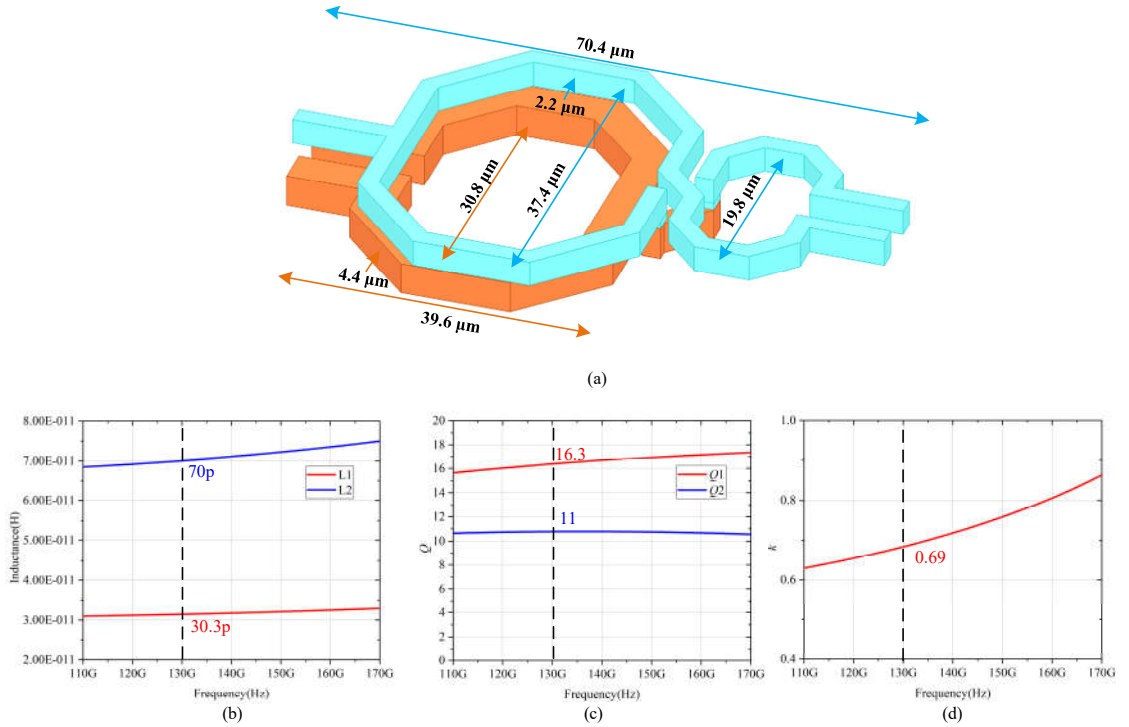


Fig. 6.12. 3-D layout and EM simulation results of an 8-shaped transformer, $L_1 = 30\text{pH}$ and $L_2 = 70\text{pH}$, $k=0.7$.

6.4. Simulation and experimental results

To test the designed PAs, a small-signal testing system was set up, as illustrated in Fig. 6.13. The Keysight PNA-X N5247B was used as the signal generator. The system upconverted the test frequency from 10 MHz to 67 GHz to a range of 110-170 GHz using the VNAX waveguide 6.5. After calibrating the VNAX and probes, as well as performing power calibration, the system could provide an input power range of -10 to 6 dBm. However, this output power was too high to accurately test the large-signal characteristics of the PAs. Therefore, a dedicated load-pull test setup was constructed for large-signal testing of the designed PAs.

The load-pull testing setup, also shown in Fig. 6.14, utilized the PNA-X N5247B as the signal generator with an additional attenuator to manage input power levels. The VNAX 2985 was used as the power receiver to measure the output power. This setup is primarily designed to test the large-signal performance of semiconductor transistors used in the PA designs. It includes computer-controlled source and load tuners to adjust the input and output impedances, allowing for both large-signal and small-signal testing.

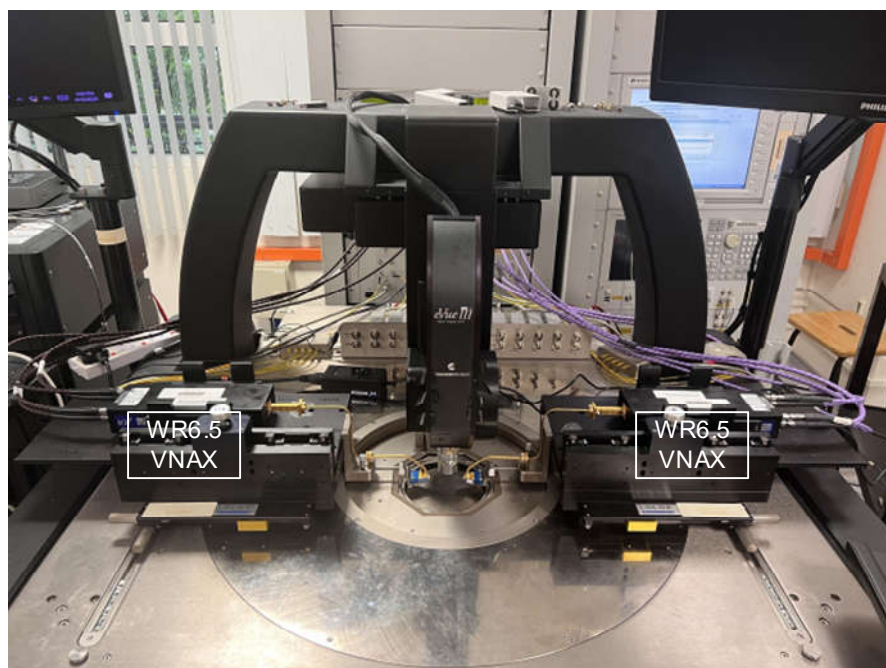


Fig. 6.13. Small signal testing platform.

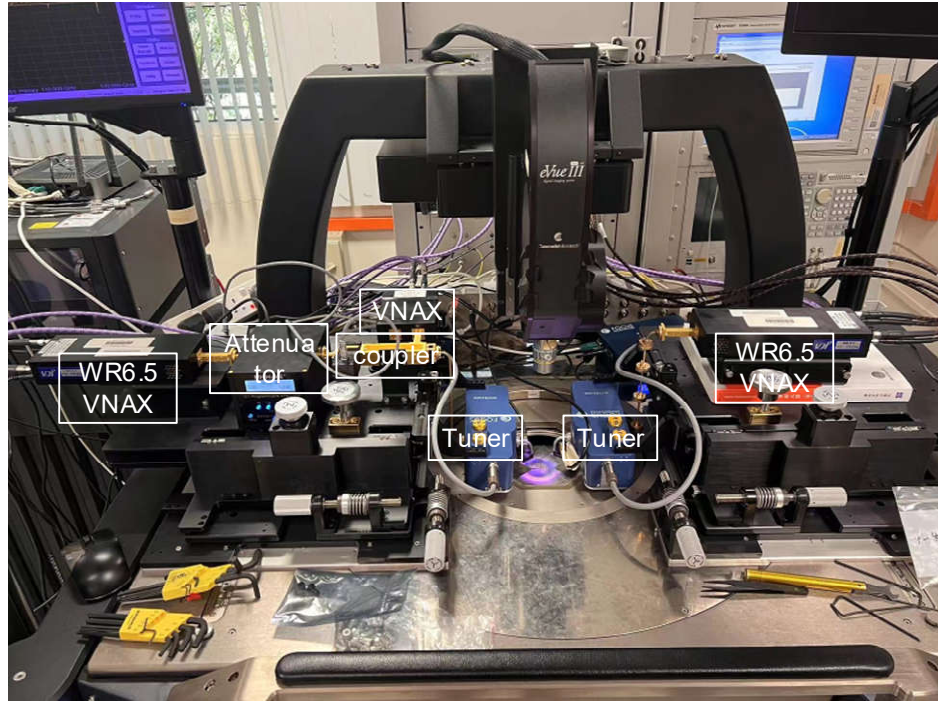


Fig. 6.14. Large signal measurement system set up.

Fig. 6.15 shows the chip photograph. Fig. 6.16 shows the measured and simulated S-parameters of the proposed D-band power amplifier. The measured peak small-signal gain reaches approximately 15.8 dB, which is higher than the simulated peak gain of 15 dB. This improvement is attributed to a slightly higher than expected magnetic coupling in the fabricated transformer, resulting in enhanced impedance transformation near the center frequency. However, this also leads to a narrower bandwidth, as the gain rapidly drops on both sides of the peak. The measured 3 dB bandwidth spans from 113 GHz to 130 GHz, whereas the simulated result shows a wider bandwidth of 112–138 GHz. This mismatch can be primarily attributed to EM-modeling inaccuracies of the transformer, including deviation in the extracted inductance and interwinding capacitance during post-layout simulation. The measured $|S_{11}|$ and $|S_{22}|$ also show consistent frequency shift compared to the simulation, further validating the hypothesis of mismatch due to layout-extracted inductor parameter deviations.

Fig. 6.17 presents the large-signal performance of the PA under continuous-wave

excitation at 130 GHz. The measured output power and gain follow the simulation trends but are slightly lower due to high-frequency loss in the measurement path and transistor model limitations above 120 GHz. The PA delivers a peak measured output power of 8.4 dBm, with a 1 dB gain compression point at about -1 dBm.

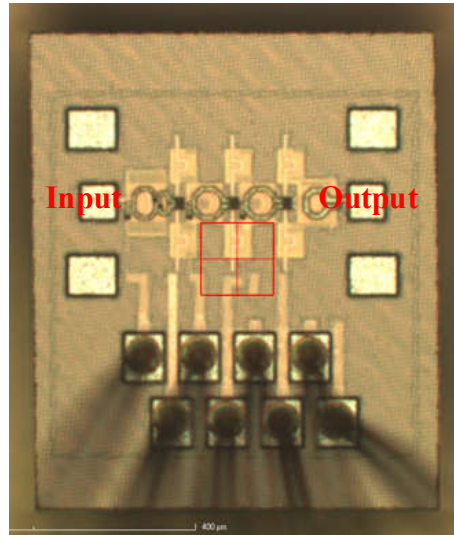


Fig. 6.15 Chip photograph.

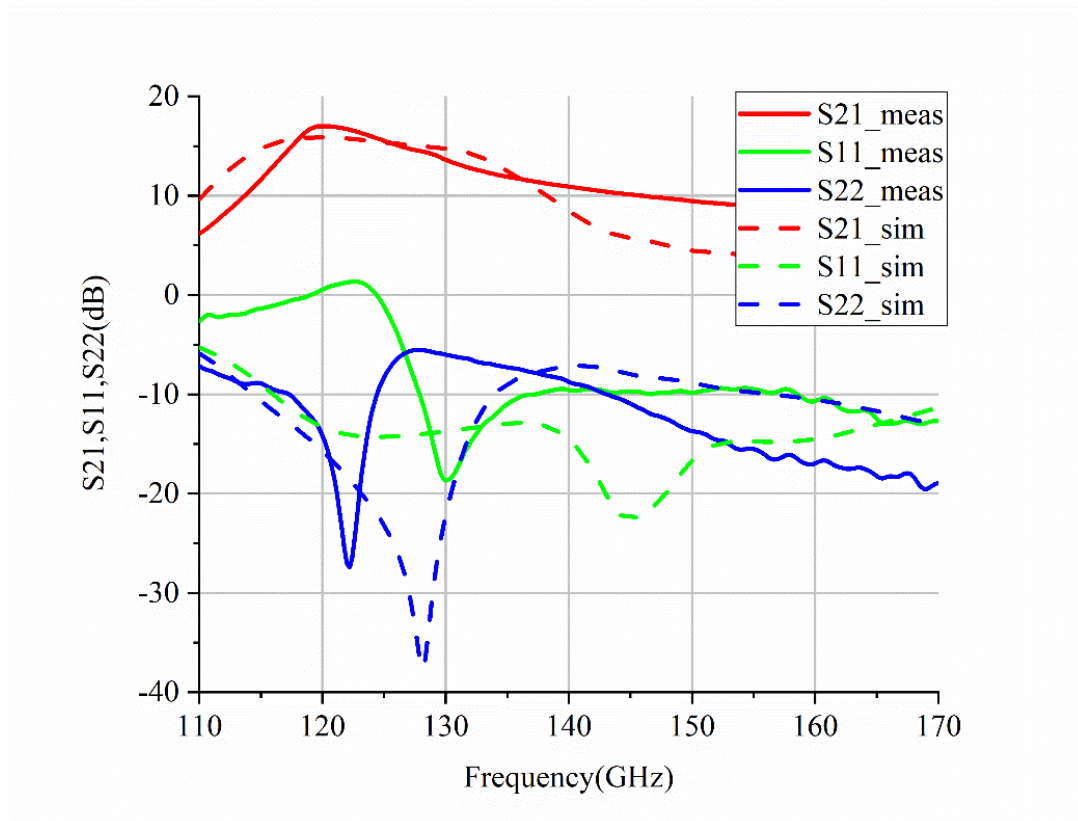


Fig. 6.16. S parameter post-simulation and measurement results of D band 3-stage PA.

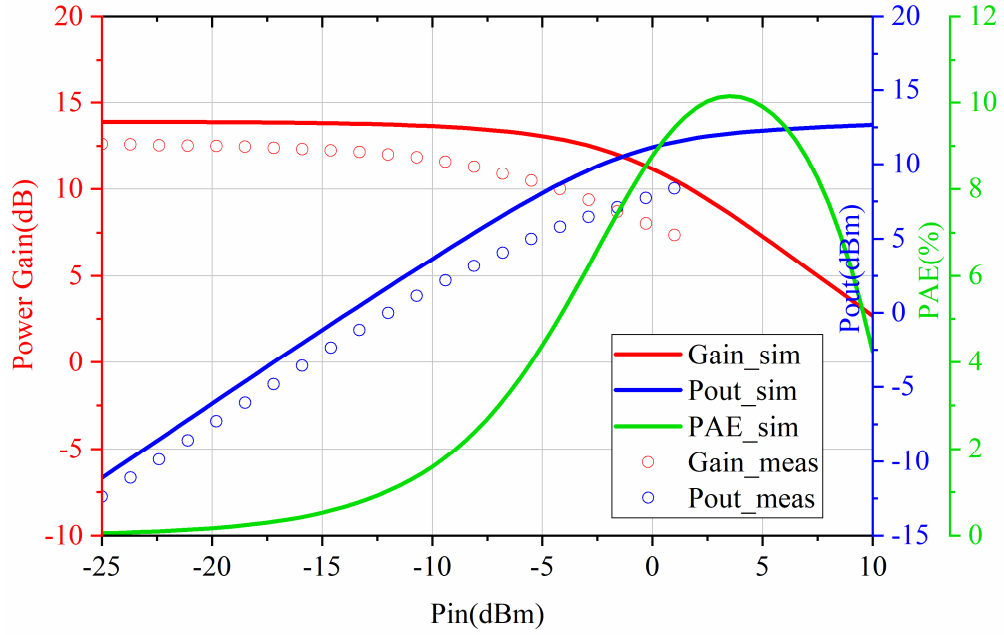


Fig. 6.17 Large-signal post-simulation and measurement results of D band 3-stage PA.

Table 6.1 Comparison to prior art D band PA designs.

	This work	[67]	[68]	[73]	[74]
Technology	28nm CMOS	28nm CMOS	28nm FDSOI	40nm CMOS	28nm CMOS
Topology	3-stage Diff.	3-stage C.S. 2-Way Diff.	3-stage C.S. Diff.	Cross-coupled Diff.	4-stage C.S. 1-Way Diff.
Frequency (GHz)	130	138	130	144	140
Bandwidth (GHz)	113-130	130-146	120-134	130-158	110-170
Supply (V)	1	1	0.95	2	0.9
Power Gain	13.2	19.2	14.5	14.2	21.9 @160GHz
P_{SAT} (dBm)	8.4	15.4	0 ¹	5.7	9.5
P_{1dB} (dBm)	5	14.25	-2 ¹	1.9	4.6
Active Area (mm ²)	0.0387	0.091	0.102	0.078	0.26

Due to hardware constraints, the maximum input power during measurement was limited to 1 dBm, as it was supplied through a front-end driver amplifier with finite gain and linearity. Moreover, the PA's DC power was provided via the PCB, which lacks direct access to on-chip current measurement. As a result, the actual DC current consumption could not be monitored during the large-signal test, and measured PAE data is therefore unavailable. All PAE values discussed are based on simulation.

Table 6.1 summarizes the measured performance of the proposed D-band PA in the context of recent CMOS implementations. The design achieves a saturated output power of 8.4 dBm and a peak gain of 13.2 dB, while maintaining a wide 3 dB bandwidth of 17GHz (113–130 GHz). These results are realized within a compact core area of only

0.0387 mm², demonstrating excellent area efficiency. The use of a stacked 8-shaped transformer enables wideband impedance matching and contributes to the flat gain response across the target band. Additionally, the differential 3-stage architecture ensures robust linearity, stable gain compression, and ease of integration for sub-THz applications. Compared with prior works, the proposed PA offers a favorable trade-off among gain, output power, bandwidth, and integration compactness, making it highly suitable for broadband D-band communication and radar systems.

6.5. Summary

In this chapter, we have proposed an 8-shaped-transformer based broadband dual-peak $G_{\max}$ -core PA for FMCW radar system. Innovative 8-shaped transformers were designed to address impedance matching challenges at high frequencies. These transformers use the unique magnetic field distribution of the 8-shaped inductor to offer adjustable coupling coefficients by varying loop sizes without changing the distance between inductors. Simulations showed these transformers achieve primary and secondary inductance values of 70pH and 30pH, respectively, with a coupling coefficient of 0.7, offering significant integration advantages.

The measured results validate the effectiveness of the proposed PA architecture and transformer design in achieving broadband and compact sub-THz performance. The fabricated chip exhibits a peak small-signal gain of 13.2 dB with a measured 3 dB bandwidth spanning 113–130 GHz, confirming the wideband matching capability enabled by the stacked 8-shaped transformer. The return loss remains below -10 dB across most of the operating band, indicating good input and output matching.

Large-signal measurements show a saturated output power of 8.4 dBm, with a 1 dB gain compression point occurring near -1 dBm input power. The gain compression

behavior is smooth and consistent with simulation trends. Due to testbench limitations, the maximum available input power was capped at 1 dBm, and direct DC current measurements were unavailable because the PA was biased through a PCB-based supply path, preventing extraction of measured PAE data. Nevertheless, simulated PAE results indicate up to 11.6% peak efficiency, and the overall measured characteristics confirm the design's suitability for compact, wideband D-band radar systems.

Chapter 7. Conclusion and Recommendations

7.1. Conclusion

This thesis has made significant contributions to the field of GaN device modeling and the design of mmWave power amplifiers, which are pivotal for the progression towards beyond 5G technologies. Chapter 2 provided a foundational review of GaN device modeling, highlighting the evolution from physical to empirical and ANN-based approaches. The significance of GaN HEMT devices in microwave and mmWave applications was underscored, with a focus on industry-standard models such as Anglov and MVSG. The chapter also did a comprehensive review of power amplifiers in beyond 5G application and summarizes some promising research directions in PA design.

Chapter 3 introduced an innovative ANN-based modeling framework for GaN HEMTs, tailored for next-generation 5G power amplifiers. This framework, developed within the ADS environment, demonstrated exceptional precision by integrating ASM-GaN-HEMT physical concepts with ANN, ensuring a globally accurate and scalable model that characterizes DC and RF characteristics. The good agreement between simulation results and measurement results have validated the correctness of the proposed model.

Chapter 4 proposed a floating-body transistor-based two-stage PA designed in a 130 nm SOI CMOS process. This PA achieves impressive performance metrics, including a maximum power gain of 25.6 dB and a PAE of 28%. The work demonstrates the feasibility of using floating-body SOI CMOS devices for advanced PA designs, offering small chip areas and better integration with baseband processors for sub-6GHz 5G applications, showcasing the potential for compact and efficient designs.

Chapter 5 focused on the design and development of dual-band PAs for 60GHz and

77GHz applications, crucial for automotive radar systems in ADAS and autonomous driving. The innovative coupled-line dual-frequency structure was proposed, and the design process was detailed, simulation results of the proposed structure demonstrated the capability to achieve conjugate matching in two different frequencies at the same time.

Chapter 6 presented an 8-shaped-transformer based broadband dual-peak Gmax-core PA for radar systems. The innovative design of the 8-shaped transformers addressed impedance matching challenges at high frequencies, offering adjustable coupling coefficients and significant integration advantages for sub-THz applications. This work highlights the potential of novel transformer designs in enhancing PA performance for radar systems.

In summary, this thesis has successfully developed a hybrid ANN-based GaN HEMT model with enhanced accuracy and scalability, designed and tested state-of-the-art PAs for sub-6GHz and mmWave frequencies, and proposed innovative matching techniques that offer new insights and solutions for beyond 5G applications. The findings and designs presented in this thesis lay a solid foundation for future research and development in the field of mmWave power amplifiers and contribute to the ongoing advancements in wireless communication and radar technologies.

7.2. Recommendations for further research

As the field of GaN HEMT device modeling and mmWave PA design continues to evolve, there remain several areas ripe for further exploration and enhancement. The integration of advanced modeling techniques and innovative design strategies will be crucial in addressing the challenges and meeting the demands of beyond 5G applications. This section outlines potential future work and improvements that can significantly

advance the current state of technology.

1. Enhanced GaN Modeling with Physics-Informed Neural Networks (PINNs)

Future work in GaN modeling can benefit significantly from integrating ANN technology with physical models. Traditional ANN models often lack physical significance, but this can be addressed by incorporating Physics-Informed Neural Networks (PINNs). By embedding physical laws and parameters within the neural network, PINNs can design corresponding loss functions that respect physical constraints. This approach can revolutionize traditional physical modeling by introducing AI-driven methods, thereby mitigating the need for extensive formula derivations and complex computations. The hybridization of AI and physical modeling can lead to more efficient and accurate GaN device models, optimizing performance predictions and real-world applicability.

2. Implementation of 60-77GHz Dual-Frequency PA Design on GaN Technology

The dual-frequency PA design based on coupled lines for 60-77GHz applications can be implemented using GaN technology. This approach, while accepting a certain level of power gain loss, can achieve wideband matching. This implementation would leverage GaN's superior properties to enhance the performance and efficiency of dual-frequency PAs, making them suitable for high-frequency applications such as automotive radar and advanced communication systems.

3. Advanced Power Combination Designs for D-Band Power Amplifiers

For D-band PA design, future research can explore advanced power combination techniques. By reviewing current advancements, new strategies can be developed for 2-way to 4-way power amplifiers, tailored to meet the requirements of future 4-channel radar systems. Innovative power combination methods will be crucial for enhancing the performance and efficiency of D-band PAs, potentially leading to breakthroughs in

high-frequency radar systems.

4. Optimization of Differential Structures and Embedding Networks

In the current differential structure with a CLC embedding network, each transistor is accompanied by large inductors both above and below, resulting in a considerable width for each PA path. This design poses challenges in multi-way power combining, potentially leading to either an excessively large overall PA area, which reduces power density, or a highly complex design for the multi-way power combiner, thus limiting design flexibility. To address these issues, two approaches can be considered:

Integrating inductors into the matching network: Embedding the inductors into the matching network could allow coupling with transformers, optimizing the overall layout. This might involve overlapping the inductors with transformers on a separate metal layer, the coupling effects must be considered in the matching and theoretical analysis is needed in the design.

Multi-coil matching structure: Another approach is to redesign the matching network by overlapping the inductors with the 8-shaped transformers. Considering the opposing magnetic fields in the 8-shaped inductor, a novel structure could be proposed to minimize the coupling effect between the L_p (the inductor in CLC embedding network) with the 8-shaped transformer matching network.

5. Improving Power Amplifier Linearity

As communication systems demand higher linearity from power amplifiers, future designs must balance efficiency with linearity enhancements. Incorporating predistortion networks and circuit architectures like Doherty amplifiers can significantly improve PA linearity. Predistortion techniques can pre-compensate for non-linearities, ensuring the output signal remains within acceptable distortion limits. Meanwhile, Doherty amplifiers, known for their high efficiency and linearity over a wide output

power range, could be integrated into PA designs to meet stringent linearity requirements. Continued innovation in these areas will be essential for developing next-generation PAs capable of supporting advanced communication systems.

Author's Publications

Journal papers:

1. **Zhongzhiguang Lu**, Hanchao Li, Hanlin Xie, Yihao Zhuang, Wensong Wang, Ng Geok Ing and Yuanjin Zheng, “A Hybrid GaN HEMT Model Merging Artificial Neural Networks and ASM-HEMT for Parameter Precision and Scalability”, in IEEE Transactions on Electron Devices (2024). (under review)
2. **Zhongzhiguang Lu**, Yanshu Guo, Yange Wang, and Yuanjin Zheng, “A mm-Wave coupler-based dual-band power amplifier for beyond 5G application,” in IEEE Transactions on Circuits and Systems II: Express Briefs. (under review)
3. **Zhongzhiguang Lu**, Yange Wang, Guanghao Fan, Cao Wan, Kaidong Hong, and Yuanjin Zheng, “An 8-shaped-transformer based power amplifier for D-band FMCW radar application”. IEEE Transactions on Circuits and Systems I: Regular Papers. (in preparation, waiting for experimental results in September 2024)
4. Ting Guo, **Zhongzhiguang Lu**, Kai Tang, Chuanshi Yang, Bo Yu and Yuanjin Zheng, “A Floating-Body Transistor-Based Power Amplifier for Sub-6-GHz 5G Applications in SOI CMOS 130-nm Process,” IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 10, pp. 4088-4092, Oct. 2022.

Conference papers:

1. **Zhongzhiguang Lu**, Hanlin Xie, Jiaming Piao, Wei Zhengzhe, Ng Geok Ing and Yuanjin Zheng, “A Wideband GaN HEMT Modelling with Comprehensive Hybrid Parameter Extraction for 5G Power Amplifiers,” 2023 IEEE International

- Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5.
2. **Zhongzhiguang Lu**, Hanchao Li, Yihao Zhuang, Ng Geok Ing, Yuanjin Zheng, “An ANN-Physical Hybrid GaN HEMT Model for 5G Power Amplifiers”, 2024 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), 2024. (under review)
 3. Wenwen Zhang, Zhengyuan Zhang, **Lu Zhongzhiguang**, Zhiping Lin and Yuanjin Zheng, “Gas/Odor Qualitative and Quantitative Estimation Methodology for a Bionic Electronic Nose,” 2023 IEEE Biomedical Circuits and Systems Conference (BioCAS), Toronto, ON, Canada, 2023.
 4. Zhengzhe Wei, Junjie Mu, **Zhongzhiguang Lu**, Yuanjin Zheng, Tony Tae-Hyoung Kim and Bongjin Kim, “A Graph-Based Accelerator of Retinex Model with Bit-Serial Computing for Image Processing,” 2023 IEEE International Symposium on Circuits and Systems (ISCAS), Monterey, CA, USA, 2023, pp. 1-5.

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