GATE-ALL-AROUND VERTICAL SILICON NANOWIRE (GAA-VSiNW) FETS: JUNCTION AND THRESHOLD VOLTAGE ENGINEERING FOR OPTIMUM PERFORMANCE AND SCALABILITY

LU WEIJIE

LU WEIJIE

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

A thesis submitted to the Nanyang Technological University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

2017

ACKNOWLEDGEMENT

The author would like to express his gratitude to Nanyang Technological University (NTU), particularly School of Electrical and Electronics Engineering, and GLOBALFOUNDRIES Singapore Inc. for the financial support as well as the opportunity to pursue this post-graduate degree.

This report was made possible with the help of many people who have assisted the author throughout the project. First and foremost, the author would like to take this opportunity to express his heartfelt appreciation to Prof. Pey Kin Leong (research co-supervisor, NTU) who has inspired and encouraged the author to pursue a higher degree for his interest in the field of advanced semiconductor devices. During the second year into the author's PhD candidature, Prof. Pey was hand-picked by Ministry of Education (Singapore) to be the vice-Provost of Singapore University of Technology and Design (SUTD). Despite his busy schedule, Prof. Pey always make time to review the project progress and give the author invaluable guidance and suggestions towards the completion of this work.

The author would like to thank Prof. Tan Chuan Seng (research supervisor, NTU) for accepting the author into his research group and giving the author guidance and logistical support throughout the project. Thanks to Dr. Wang Xinpeng, Mr. Chen Zhixian, Dr. Li Xiang and Dr. Navab Singh from Institute of Microelectronics (IME), A*STAR, Singapore, for their guidance and support. They have provided the author with the experience of working in a full-fledged semiconductor industry standard clean room where the device fabrication is done and fruitful discussions in device analysis. Special thanks to the IME clean room staff for their help in fabricating the devices.

The author would also like to show his appreciation to Dr. Lap Chan, Dr. Ng Chee Mang and Mr. Leong Kam Chew from GLOBALFOUNDRIES Singapore for their mentorship, valuable lectures and discussions every week which broadens the author's

knowledge on many different aspects concerning the semiconductor industry. Thanks to Assoc. Prof. Zhou Xing and Mr. Zhang Junbin for their support in nanowire device simulation used in this work.

Special thanks to fellow colleagues Dr. Chin Yoke King, Dr. Peng Jianwei, Dr. Dexter Tan Xueming, Dr. Ong Chio Yin, Dr. Ong Beng Sheng, Dr. Anson Heryanto, Dr. Lim Dau Fatt, Dr. Liu Wenhu, Dr. Guai Guan Hong, Dr. Leiw Ming Yian, Dr. Li Yida, Dr. Zhang Lin, Dr. Peng Lan and Dr. Rahmat Agung Susantyoko. Their company, moral support and the shared fun had been important to cheer up the author when he was down.

Last but not least, the author would like to thank his family for their unconditional love and support and to his lovely wife, Rebecca, for her encouragement and for giving birth to three adorable and lovely sons.

"Genius is one per cent inspiration and ninety-nine per cent perspiration."

- Thomas Edison

Table of Contents

CHAPTER 4

CHAPTER 5

CHAPTER 6

CHAPTER 7

CHAPTER 8

ABSTRACT

Gate-All-Around (GAA) Silicon nanowire (SiNW) is a structure with virtually "infinite" number of gates in close vicinity to the channel to provide the best gate-to-channel electrostatic control, and therefore drastically reduces the parasitic short channel effects leading to lower power dissipation when the transistor is turned off. Generally, GAA-SiNW devices are demonstrated in either the lateral or vertical direction. With the limited estate area per wafer, GAA vertical SiNWs (GAA-VSiNWs) are preferred to fully utilize the advantages of the nanowire infrastructure while maximizing the number of transistors per unit area. Due to the one dimensional nature of vertical nanowire, 2 problems arise: (1) Threshold Voltage (V_T) of gated nanowire transistors are incorrectly set due to the work function difference between the gate and the undoped channel and (2) high series resistance of the source/drain regions.

In this work, to address issue (1), two methods are employed. In the first method, dopants of opposite polarity to the intended device type are used as the gate implant. For example, the gate of nMOS transistor will be implanted with high dosage of p-type dopant and vice versa. From our measurement results, we demonstrate that there is a positive V_T shift of ~ 1.5V across different diameters while the short channel effect characteristics remain similar for small diameter GAA-VSiNWs. In the second method, poly-Si gate is replaced with doped fully-silicided (FUSI) gate using nickel silicide (Ni_xSi_y) as the gate material.

To tackle issue (2), Ni_xSi_y Schottky S/D is introduced. However, 2 challenges are associated with Ni_xSi_y Schottky S/D: (1) Ni_xSi_y intrusion into the silicon nanowire channel during silicidation and (2) the existence of a Schottky barrier which leads to increased contact resistance.

By using a two-step rapid thermal annealing (RTA) silicidation methodology, Ni_xSi_y intrusion into nanowire can be controlled. VSiNW diodes and Transmission Electron Microscopy (TEM) imaging were used to characterize intrusion lengths into VSiNWs. A low temperature RTA was first used to control the intrusion length and subsequently, a higher temperature RTA was used, after removal of un-reacted Ni, to form the desired nickel silicide phase. From our results, the two-step RTA silicidation showed a 5 times reduction in silicide intrusion length compared to one-step RTA silicidation. At the same time, the two-step RTA silicidation method demonstrated 2 orders in magnitude of reduction in $I_{reverse}$, ~14% reduction in ideality factor (from 2.25 to 1.75) and ~28% reduction in effective electron Schottky Barrier Height (SBH) (from 0.7eV to 0.51eV).

Dopant Segregated Schottky (DSS) contact was employed to reduce the SBH and in turn, improve the S/D contact resistance. Through the use of silicidation induced dopant segregation (SIDS) method, boron or phosphorus atoms were implanted into the S/D regions before the occurrence of silicidation to segregate the dopants at the Ni_xSi_y/Si interface. Using two-step RTA silicidation as standard throughout the experiments, DSSB-VSiNW diodes higher $I_{forward}$ and lower $I_{reverse}$ than SB-VSiNW diodes. In addition, DSSB-VSiNW diodes showed ideality factor close to unity (a 61% reduction from 2.25 to 1.15) and ~10% reduction in effective electron SBH (from 0.5eV to 0.45eV).

Moreover, the fabricated DSS-VSiNW MOSFETs demonstrated excellent electrical characteristics with an increase of 8% to 29% in drive currents over the SB-VSiNW MOSFETs. From our low temperature measurements, DSS-VSiNW MOSFETs showed ~ 50% reduction in SBH as compared to SB-VSiNW MOSFETs. In addition, DSS-VSiNW MOSFETs demonstrated lower Drain-Induced Barrier Lowering (DIBL) and Sub-threshold swing (SS) short channel effect characteristics over SB-VSiNW MOSFETs.

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1
INTRODUCTION

1.1 Motivation

Classical transistor or **M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor (MOSFET) architecture has been the preeminent choice for fabrication. As the semiconductor industry progresses into deep sub-micrometer regime and beyond, classical MOSFETs are reaching the scaling limits confined by the physical laws of nature. These limits include higher sub-threshold off-state leakage current ($I_{d,leak}$) due to reduced threshold voltage (V_T), gate oxide leakage, lithography variation, degraded performance induced by Short Channel Effects. Apart from conventional scaling, other various techniques and new transistor architectures are explored to enhance MOSFET performance.

Strain techniques are widely adopted by today’s semiconductor industry to enhance hole and electron mobility, which in turn, boost transistor performance. For instance, Intel Corporation used SiN liner stressor for nMOS and embedded SiGe S/D stressors, coupled with Σ-shaped S/D architecture for pMOS at the 90nm technology node. Besides the reduction of gate dielectric thickness, nitridation of SiO_2 gate dielectric [1.1 – 1.4] and replacing with high-κ dielectric [1.5 – 1.11] are other methods to increase gate oxide capacitance to boost transistor performance. However, the use of high-κ dielectric requires a mandatory switch from poly-gate to metal gate due to the poly-gate depletion effect on gate capacitance.

Another significant development is the introduction of fin field-effect transistors (FinFETs) [1.12 – 1.14]. FinFETs are three-dimensional (3D) MOSFETs with tri-gate infrastructure. They give better electrostatic control of the channel which helps to suppress SCEs, reduce leakage current and improve sub-threshold performance. In 2011, Intel Corporation presented a transition from 2D to 3D architecture with FinFETs starting from 22nm and TSMC followed suit starting from 16nm in 2013. These are two prominent examples that clearly depict the shift of semiconductor foundries from single-gate to Multi-Gate MOSFET (MuGFET) architecture to combat inherent scaling limits as technology node shrinks. Other examples of MuGFET include double-gated FinFET [1.15, 1.16], SOI π-gated FET [1.17, 1.18] and SOI Ω-gated FET [1.19]. These MuGFETs are schematically depicted in Figure 1.1.

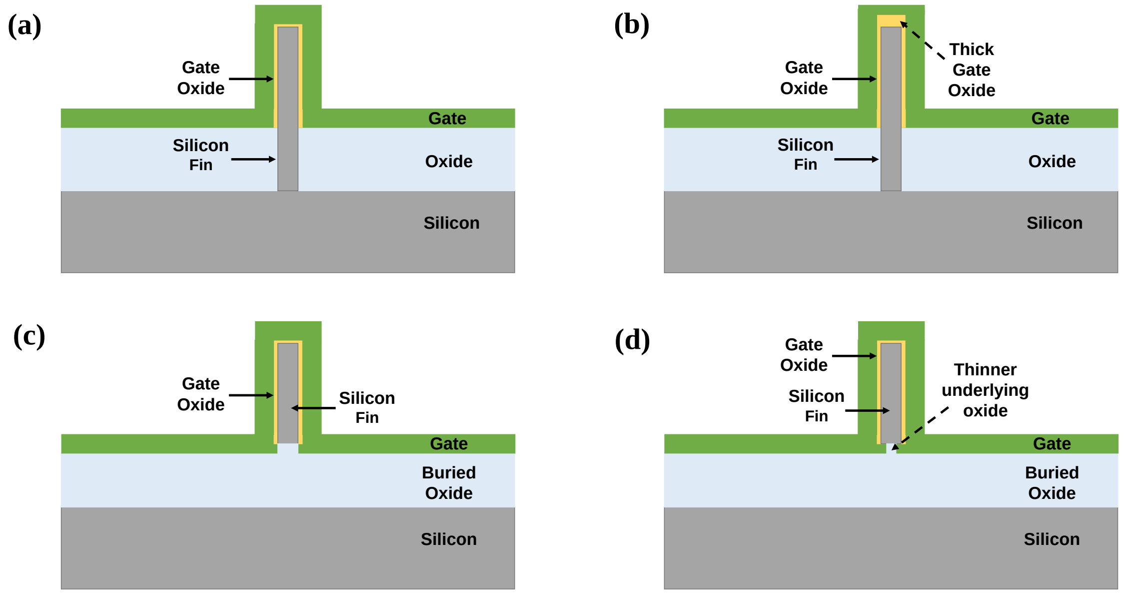


Figure 1.1 (a) Cross-section schematic of FinFET, (b) double-gated FinFET , (c) π-gated FET and (d) Ω-gated FET.

An ideal yet extreme case of MuGFET is **G**ate-**A**ll-**A**round (GAA) MOSFET whereby the gate completely surrounds an ultra-narrow cylindrical Si nanowire (SiNW) channel. This architecture provides the best possible electrostatic control resulting in greatly reduced SCEs and improved drive current. There are two typical orientations for GAA MOSFET: lateral [1.20, 1.21], shown in Figure 1.2 (a) and vertical [1.22, 1.23], shown in Figure 1.2 (b).

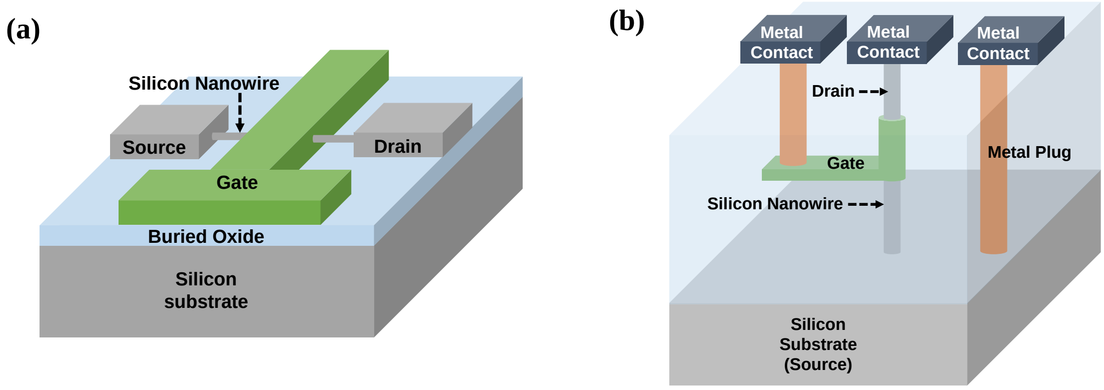
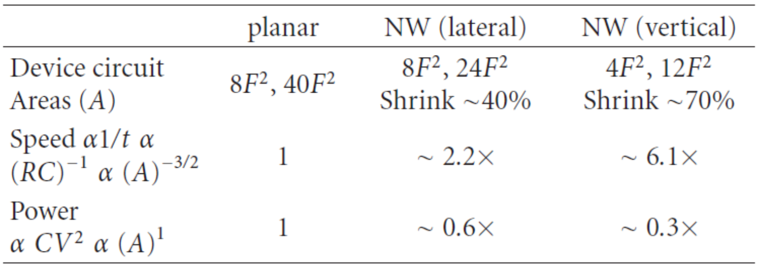


Figure 1.2 Schematic of GAA-SiNW MOSFET. This structure provides the best possible gate electrostatic control over the channel since the channel body is completed surrounded by the gate material.

Using *ab-initio* calculations on device circuit fabricated via lateral and vertical NW GAA MOSFET, Kwong et al. [1.24] summarized the various aspects of each GAA-MOSFET architecture. The results, tabulated in Table 1.1, illustrated vertical NW GAA-MOSFET (VNW-GAA-MOSFET) occupied ~ 50% less area and use ~ 50% less power while perform ~ 300% faster than lateral NW GAA MOSFET (LNW-GAA-MOSFET). It is evident that VNW architecture outperforms LNW architecture in terms of area occupied by circuit, circuit speed and circuit power consumed. Therefore, VSiNW is a very promising candidate as the main device architecture beyond the 22nm node and is the focus of the work in this thesis.



	planar	NW (lateral)	NW (vertical)
Device circuit Areas (A)	$8F^2$, $40F^2$	$8F^2$, $24F^2$ Shrink ~40%	$4F^2$, $12F^2$ Shrink ~70%
Speed $\alpha 1/t$ α $(RC)^{-1}$ α $(A)^{-3/2}$	1	~ 2.2×	~ 6.1×
Power α CV^2 α $(A)^1$	1	~ 0.6×	~ 0.3×

Table 1.1 Various advantages, in terms of device area, speed and power consumption, gained by device circuit fabricated via vertical silicon nanowires over those of planar bulk substrate and lateral nanowires [1.24].

Despite the advantages of VNW architecture, there are underlying issues associated with VNW-GAA-MOSFET. The external series resistance is one of the issues for VNW-GAA-MOSFET. The schematic in Figure 1.3 (b) is representative of the TEM micrograph shown in Figure 1.3 (a) where the external resistance consists of: 1) metal to SiNW contact resistance ($R_{contact}$), 2) nanowire tip resistance (R_{tip}), 3) nanowire bottom resistance (R_{bottom}) and 4) substrate sheet resistance (R_{sub-sh}). For conventional highly-doped S/D nanowire FETs, the main challenge in external resistance comes from R_{tip}, R_{bottom} and $R_{contact}$ due to the narrow dimensions of source/drain.

Another issue is the incorrect threshold voltage (V_T) value associated with nanowire transistor. Doped poly-Si gates give too low V_T value for n- and p-MOS and this causes the fabricated inverters to have very small noise margin (NM). The problem can be attributed to the Fermi level of the intrinsically doped channel and the incorrect work-function (Φ_m) values of the doped poly-Si gate.

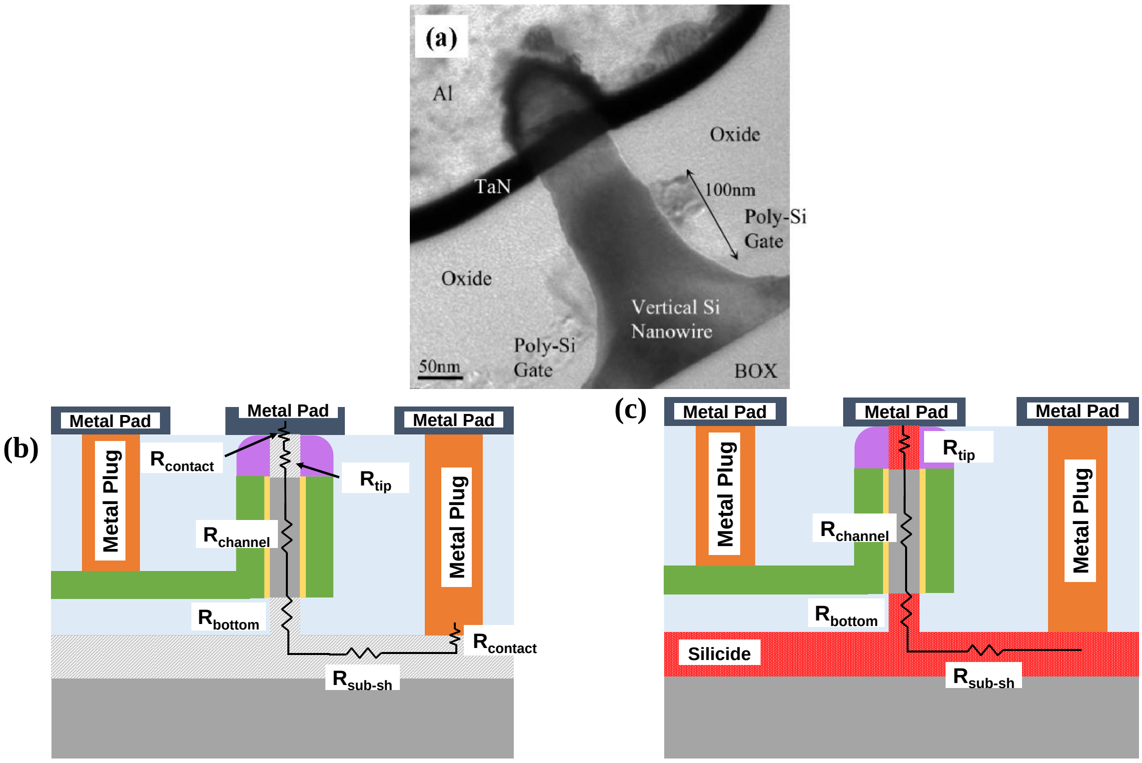


Figure 1.3 (a) Cross-sectional TEM of VNW-GAA-MOSFET embedded in oxide dielectric with polySi gate and Al metal contact. Schematics of different resistance components for (b) doped VNW-GAA-MOSFET and (c) silicided VNW-GAA-MOSFET.

In recent literature, silicided S/D was successfully implemented in planar [1.25, 1.26] and nano-scaled [1.27, 1.28] devices and has been proven to effectively reduce R_{ext} with the formation of abrupt junctions. This inspires us to integrate S/D metallization with VNW-GAA-MOSFET, shown in Figure 1.3 (c), and study the possibility of junction scaling of silicided S/D. Furthermore, dopant segregation with fully silicided (FUSI) S/D was introduced [1.29, 1.30] to improve carrier injection, short channel effect immunity and to achieve very low S/D resistance due to Schottky Barrier Height (SBH) lowering. This motivates us to incorporate the dopant segregation technique, for the first time, on VNW-GAA-MOSFET to study the possibility of junction engineering. Lastly, alternative gate options, such as FUSI or doped-FUSI gate, have been proposed to tune V_T [1.29, 1.31, 1.32] by adjusting the gate work function. This propels us to explore the possibility of integrating alternative gate options with VNW-GAA-MOSFET and to study the relative performance improvement.

1.2 Objectives of Dissertation

The project focuses to (i) integrate S/D metallization, (ii) analyze the effect of dopant segregation at S/D regions and (iii) explore the effect of various alternative gate options, on GAA-VSiNW MOSFET. This will be achieved in the following 5 phases:

1) To fabricate VSiNW as starting infrastructure using standard CMOS processes.

2) To investigate the effect of silicide intrusion and dopant segregation on (i) silicidation and (ii) electrical parameters of VSiNW Schottky diodes.

3) To study and analyze the electrical characteristics of GAA-VSiNW MOSFETs with poly-gate and highly doped S/D.

4) To study and analyze the electrical characteristics of GAA-VSiNW MOSFETs with Schottky Barrier (SB) S/D and GAA-VSiNW MOSFETs with Dopant Segregated SB (DSSB) S/D.

5) To tune V_T of FUSI GAA-VSiNW MOSFETs using different gate implants and investigate the effect of SiNW diameter on V_T.

1.3 Scope of Dissertation

This project involves fabricating free-standing VSiNW, as the basic building block for subsequent device development, on bulk Si substrate using conventional CMOS processes. A major contribution of this work is providing well-documented procedures of fabricating VSiNW and the related VSiNW transistors used for this work. Another important contribution is the understanding of nickel silicide formation in nanostructures encapsulated within thick oxide layer. To investigate the effect of silicide intrusion, Transmission Electron Microscopy (TEM) and Energy-Dispersion X-ray (EDX) techniques are employed to study and characterize the silicide intrusion into the vertical nanowire. Concurrently, electrical measurements are performed on VSiNW Schottky diodes to investigate the effect of silicide intrusion on diode electrical characteristics.

The third contribution of this work is the understanding of dopant segregation in VSiNW structure. To realize dopant segregation, low energy, high dose dopant implant was performed at the VSiNW tip at the silicide/Si interface before silicidation. Firstly, the effect of segregated dopants will be studied via VSiNW Schottky diodes. This is followed by the electrical characterization and analysis of SB MOSFETs to demonstrate the effect of dopant segregation on device performance and effective SBH. TEM is utilized for the physical characterization of SB and DSSB MOSFETs.

The last contribution of this dissertation is the study of V_T tuning using different gate materials via various VSiNW MOSFET. Ni FUSI, doped-Ni FUSI, n-doped and p-doped gate materials were used to tune V_T of VSiNW MOSFETs. Electrical measurements were performed to understand the effect of different gate materials on the device electrical characteristics.

1.4 Organization of Dissertation

Chapter 1 introduces the background and motivation for this project.

Chapter 2 gives the literature review covering the synthesis of Si nanowires, the operating principles of Schottky Barrier MOSFETs and the concept of Schottky Barrier Height tuning. The challenges of nanowire transistors are also reviewed.

Chapter 3 reports the detailed experimental methodologies that include the fabrication of VSiNW, SB/DSSB-VSiNW diodes as well as GAA-VSiNW MOSFETs with SB/DSSB S/D.

Chapter 4 investigates the silicide intrusion and the impact of RTA temperatures on the electrical performance of VSiNW Schottky and DSSB diodes. The effect of interfacial segregated dopants on diode performance are presented and discussed.

Chapter 5 studies the electrical characteristics and Short Channel Effect (SCE) performance of GAA-VSiNW MOSFETs with highly-doped S/D and the various V_T tuning methodologies, as well as their impact on the MOSFET electrical performance.

Chapter 6 investigates the feasibility of integrating Schottky Barrier (SB) S/D and FUSI gate with VSiNW to form FUSI-GAA VSiNW SB MOSFETs. The electrical performance and SCEs of the modified transistor are analyzed.

Chapter 7 explores the concept of dopant segregation SB S/D and its incorporation in device fabrication. The electrical characteristics of FUSI-GAA VSiNW DSSB MOSFETs are also presented and compared against MOSFETs with SB S/D. In addition, various V_T tuning methods and their impact on MOSFET electrical and SCE characteristics are analyzed.

Chapter 8 summarizes the major findings and results of this project. Possible future directions with regards to VSiNW MOSFETs are also proposed.

1.5 References

[1.1] J. R. Shallenberger, D. A. Cole, and S. W. Novak, "Characterization of silicon oxynitride thin films by x-ray photoelectron spectroscopy," *J. Vac. Sci. Technol. A*, vol. 17, pp. 1086-1090, Jul. 1999.

[1.2] S. Inaba, T. Shimizu, S. Mori, K. Sekine, K. Saki, H. Suto, H. Fukui, M. Nagamine, M. Fujiwara, T. Yamamoto, M. Takayanagi, I. Mizushima, K. Okano, S. Matsuda, H. Oyamatsu, Y. Tsunashima, S. Yamada, Y. Toyoshima, and H. Ishiuchi, "Device performance of sub-50 nm CMOS with ultra-thin plasma nitrided gate dielectrics," *IEEE Int. Electron Devices Meeting – Tech. Dig.*, pp. 651-654, Dec. 2002.

[1.3] P. A. Kraus, K. Z. Ahmed, C. S. Olsen, and F. Nouri, "Physical models for predicting plasma nitrided Si-O-N gate dielectric properties from physical metrology," *IEEE Electron Device Lett.*, vol. 24, pp. 559-561, Sep. 2003.

[1.4] F. N. Cubaynes, V. C. Venezia, C. van der Marel, J. H. M. Snijders, J. L. Everaert, X. Shi, A. Rothschild, and M. Schaekers, "Plasma-nitrided silicon rich oxide as an extension to ultrathin nitrided oxide gate dielectrics," *Appl. Phys. Lett.*, vol. 86, no. 17, 172903, Apr. 2005.

[1.5] H. R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G. A. Brown, C. D. Young, P. M. Zeitzoff, J. Gutt, P. Lysaght, M. I. Gardner, and R. W. Murto, "High-k gate stacks for planar, scaled CMOS integrated circuits," *Microelect. Eng.*, vol. 69, pp. 152-167, Sep. 2003.

[1.6] F. Chen, X. Bin, C. Hella, X. Shi, W. L. Gladfelter, and S. A. Campbell, "A study of mixtures of HfO2 and TiO2 as high-k gate dielectrics," *Microelect. Eng.*, vol. 72, pp. 263-266, Apr. 2004.

[1.7] O. Auciello, W. Fan, B. Kabius, S. Saha, J. A. Carlisle, R. P. H. Chang, C. Lopez, E. A. Irene, and R. A. Baragiola, "Hybrid titanium-aluminum oxide layer as alternative high-k gate dielectric for the next generation of complementary metal-oxide-semiconductor devices," *Appl. Phys. Lett.*, vol. 86, no. 4, 042904, Jan. 2005.

[1.8] N. Umezawa, K. Shiraishi, T. Ohno, H. Watanabe, T. Chikyow, K. Torii, K. Yamabe, K. Yamada, H. Kitajima, and T. Arikado, "First-principles studies of the intrinsic effect of nitrogen atoms on reduction in gate leakage current through Hf-based high-k dielectrics," *Appl. Phys. Lett.*, vol. 86, no. 14, 143507, Apr. 2005.

[1.9] J.-P. Locquet, C. Marchiori, M. Sousa, J. Fompeyrine, and J. W. Seo, "High-K dielectrics for the gate stack," *J. Appl. Phys.*, vol. 100, 051610, Sep. 2006.

[1.10] H. Wong and H. Iwai, "On the scaling issues and high-κ replacement of ultrathin gate dielectrics for nanoscale MOS transistors," *Microelect. Eng.*, vol. 83, pp. 1867-1904, Oct. 2006.

[1.11] J. Robertson, "Maximizing performance for higher K gate dielectrics," *J. Appl. Phys.*, vol. 104, 124111, Dec. 2008.

[1.12] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor, and C. M. Hu, "FinFET - A self-aligned double-gate MOSFET scalable to 20 nm," *IEEE Trans. Electron Devices*, vol. 47, pp. 2320-2325, Dec. 2000.

[1.13] J. Kedzierski, E. Nowak, T. Kanarsky, Y. Zhang, D. Boyd, R. Carruthers, C. Cabral, R. Amos, C. Lavoie, R. Roy, J. Newbury, E. Sullivan, J. Benedict, P. Saunders, K. Wong, D. Canaperi, M. Krishnan, K. L. Lee, B. A. Rainey, D. Fried, P. Cottrell, H. S. P. Wong, M. Ieong, and W.

Haensch, “Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation,” *IEEE Int. Electron Devices Meeting – Tech. Dig.*, pp. 247-250, Dec. 2002.

[1.14] J. Kedzierski, M. Ieong, E. Nowak, T. S. Kanarsky, Y. Zhang, R. Roy, D. Boyd, D. Fried, and H.-S. P. Wong, “Extension and source/drain design for high-performance FinFET devices,” *IEEE Trans. Electron Devices*, vol. 50, pp. 952-958, Apr. 2003.

[1.15] H. Xuejue, L. Wen-Chin, C. Kuo, D. Hisamoto, L. Chang, J. Kedzierski, *et al.*, "Sub-50 nm P-channel FinFET," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 880-886, 2001.

[1.16] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, *et al.*, "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," *Electron Devices, IEEE Transactions on*, vol. 47, pp. 2320-2325, 2000.

[1.17] P. Jong-Tae, J. P. Colinge, and C. H. Diaz, "Pi-Gate SOI MOSFET," *Electron Device Letters, IEEE*, vol. 22, pp. 405-406, 2001.

[1.18] P. Jong-Tae and J. P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," *Electron Devices, IEEE Transactions on*, vol. 49, pp. 2222-2229, 2002.

[1.19] Y. Fu-Liang, C. Hao-Yu, C. Fang-Cheng, H. Cheng-Chuan, C. Chang-Yun, C. Hsien-Kuang, *et al.*, "25 nm CMOS Omega FETs," in *Electron Devices Meeting, 2002. IEDM '02. International*, 2002, pp. 255-258.

[1.20] K. Nayak, S. Agarwal, M. Bajaj, K. V. R. M. Murali, and V. R. Rao, "Random Dopant Fluctuation Induced Variability in Undoped Channel Si Gate all Around Nanowire n-MOSFET," *Electron Devices, IEEE Transactions on*, vol. 62, pp. 685-688, 2015.

[1.21] S. K. Sinha, K. Kumar, and S. Chaudhury, "Si/Ge/GaAs as channel material in nanowire-FET structures for future semiconductor devices," in *Electron Devices and Solid-State Circuits (EDSSC), 2015 IEEE International Conference on*, 2015, pp. 527-530.

[1.22] K. Tomioka, J. Motohisa, and T. Fukui, "III-V nanowire channel on Si: From high-performance vertical FET to steep-slope devices," in *VLSI Technology, Systems and Application (VLSI-TSA), 2015 International Symposium on*, 2015, pp. 1-2.

[1.23] Z. Yujia, L. Mathew, R. Rao, M. Palard, S. Chopra, J. G. Ekerdt, *et al.*, "High-Performance Vertical Gate-All-Around Silicon Nanowire FET With High-k/Metal Gate," *Electron Devices, IEEE Transactions on*, vol. 61, pp. 3896-3900, 2014.

[1.24] D.-L. Kwong, X. Li, Y. Sun, G. Ramanathan, Z. X. Chen, S. M. Wong, *et al.*, "Vertical Silicon Nanowire Platform for Low Power Electronics and Clean Energy Applications," *Journal of Nanotechnology*, vol. 2012, 2012.

[1.25] L. Knoll, Q. T. Zhao, R. Luptak, S. Trellenkamp, K. K. Bourdelle, and S. Mantl, "20nm Gate length Schottky MOSFETs with ultra thin NiSi/epitaxial $NiSi_2$ source/drain," in *Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, 2011, pp. 1-4.

[1.26] J. L. Padilla, L. Knoll, F. Gamiz, Q. T. Zhao, A. Godoy, and S. Mantl, "Simulation of Fabricated 20-nm Schottky Barrier MOSFETs on SOI: Impact of Barrier Lowering," *Electron Devices, IEEE Transactions on*, vol. 59, pp. 1320-1327, 2012.

[1.27] K. Zhaoyi, Z. Liangliang, W. Runsheng, and H. Ru, "A comparison study of Silicon Nanowire Transistor with Schottky-Barrier source/drain and doped source/drain," in *VLSI Technology, Systems, and Applications, 2009. VLSI-TSA '09. International Symposium on*, 2009, pp. 133-134.

[1.28] C. Wei, S. Chun-Hsing, W. Wen-Fa, and L. Chenhsin, "P-channel Schottky barrier nanowire SONOS memory with low-voltage operations and excellent reliability," in *VLSI Technology, Systems, and Applications (VLSI-TSA), 2012 International Symposium on*, 2012, pp. 1-2.

[1.29] C. Sung-Jin, H. Jin-Woo, K. Sungho, D.-I. Moon, M. Jang, and Y.-K. Choi, "Dopant-Segregated Schottky Source/Drain FinFET With a NiSi FUSI Gate and Reduced Leakage Current," *Electron Devices, IEEE Transactions on*, vol. 57, pp. 2902-2906, 2010.

[1.30] Z. Yi-Bo, S. Lei, X. Hao, X. Yu-Qian, W. Yi, and Z. Sheng-Dong, "Comparative study of dopant-segregated Schottky barrier germanium nanowire transistors," *Japanese Journal of Applied Physics*, vol. 53, p. 04EN03, 2014.

[1.31] J. Kedzierski, D. Boyd, C. Cabral, P. Ronsheim, S. Zafar, P. M. Kozlowski, *et al.*, "Threshold voltage control in NiSi-gated MOSFETs through SIIS," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 39-46, 2005.

[1.32] N. Yoshida, H. Keping, H. Peng-Fu, M. Beach, L. Xinliang, R. Hung, *et al.*, "Threshold voltage tuning by metal gate work function modulation for 10 nm CMOS integration and beyond," in *VLSI Technology, Systems and Application (VLSI-TSA), Proceedings of Technical Program - 2014 International Symposium on*, 2014, pp. 1-2.

CHAPTER 2
LITERATURE REVIEW

This chapter briefly overviews the background physics required to facilitate the understanding of the rest of this thesis. In Section 2.1, the two important parameters to quantify short channel effects (SCEs) will be introduced and it will be followed by methodologies in Section 2.2. The various methods to synthesize silicon nanowires are briefly discussed in Section 2.3. Section 2.4 presents the fundamentals related to Schottky barrier, operating principles of Schottky MOSFETs and methodologies to tune Schottky barrier height. Use of nickel (Ni) to form metal silicide is reviewed in Section 2.5. Finally, Section 2.6 will sum up this chapter by giving a brief summary.

2.1 Challenges in device scaling

Before we explore the benefits and types of MuGFETs, we need to understand the challenges in scaling down planar transistors that lead to the need for MuGFETs. The semiconductor industry has been revolutionized with a mission or objective to fulfill ever since the birth of Moore’s Law in 1965. Thereafter, transistor size starts to shrink by a factor of 0.7 every 2 years. As the size of transistor shrank, two fundamental problems related to short channel effects (SCEs) start to surface. These problems and their effect on device performance are discussed in Sections 2.1.1 and 2.1.2.

2.1.1 Drain-Induced Barrier Lowering (DIBL) effect and V_T roll-off

Scaled transistors suffer from Drain-Induced-Barrier-Lowering (DIBL) effect [2.1-2.3] caused by the penetration of the depletion regions of the S/D regions into the channel region beneath the gate and this will result in energy band lowering. It causes the gate to lose the sole dominance over the formation of the inversion layer beneath it, which serves as the 'channel' for carriers to flow between S/D, to the drain region. Furthermore, DIBL is worsened with the increase in drain voltage (V_{DS}) and the decrease in distance between S/D. Secondary effects caused by DIBL are V_T reduction as L_G decreases and increase off-state leakage current (I_{off}). DIBL can be explained in terms of energy band, as shown in Figure 2.1.

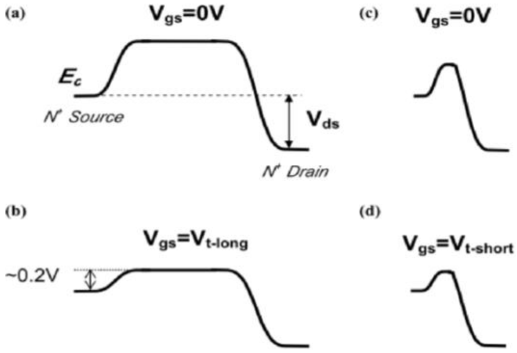


Figure 2.1 Conduction energy band (E_c) diagrams of long- and short-channel nMOS to explain the DIBL effect.

Figure 2.1(a) shows the conduction energy band (E_c) of a long-channel nMOS at V_{GS} = 0V and a certain voltage V_{DS} is applied across the S/D. When V_{GS} is equivalent to the V_T of the long-channel nMOS is applied (Figure 2.1(b)), the channel E_c is lowered and an inversion layer of electrons is formed in the channel. With the lowering of E_c, a 0.2eV potential barrier exists between the source and channel and this is sufficient for the electrons to flow from the source into the channel and then into the drain.

From Figure 2.1(c), it is observed that the channel E_c is much lower than that of the long-channel counterpart in Figure 2.1(a) at V_{GS} = 0V due to the extension of the depletion region of the drain side into the intrinsic region underneath the gate. This is termed as DIBL. Hence, a smaller V_T is required to pull the barrier down to 0.2eV. Therefore, V_T for short-channel devices is much smaller than that of long-channel. Figure 2.2 shows I_{DS}-V_{GS} data for nMOS, at low and high V_{DS}, suffering from the DIBL effect. From the electrical characteristics, the DIBL effect will shift the I_{DS} curve to the left and results in lower V_T and higher I_{off} (indicated by red and blue dots).

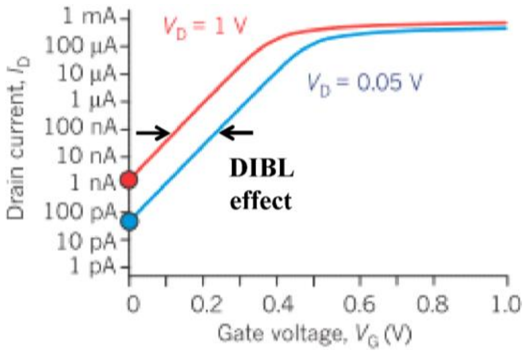


Figure 2.2 Illustration of the electrical characteristics of nMOS suffered from DIBL. Blue curve is extracted at low V_{DS} = 0.05V and red curve is extracted at high V_{DS} = 1V [2.1].

Figure 2.3 shows the V_T roll-off phenomenon observed in nMOS and pMOS devices gathered from experimental data [2.4]. V_T roll-off is caused by charge sharing between the gate and source/drain. From Figure 2.3, it can be seen that the V_T values for both types of devices decreases significantly with reducing gate length and the degradation increases faster with high V_{DS} (1V) as compared to low V_{DS} (0.05V). With the prominence of the V_T 'roll-off' phenomenon in short-channel devices, MOSFET switching on and off becomes more difficult as the noise margin becomes substantially smaller and proper circuit functions will be impeded.

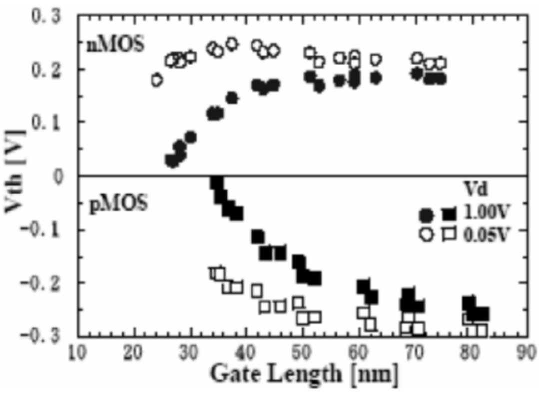


Figure 2.3 V_T decreases with L_G, depicting a phenomenon known as V_T roll-off [2.4].

2.1.2 Degradation of Sub-threshold swing (SS)

Another SCE is the degradation of sub-threshold swing (SS). SS defines the rate of increase of current below the threshold voltage for a particular MOSFET device and is defined in Equation (1):

$$SS = \frac{dV_{GS}}{d(\log(I_{DS}))} \qquad Equation\ (1)$$

where V_{GS} is the voltage between gate and source and I_{DS} is the current between drain and source. Equation (1) is usually used in extracting SS from experimental data. Typically, SS is extracted from the slope of log I_{DS}-V_{GS} curve below threshold voltage. A graphic representation of SS extraction is shown in Figure 2.4. Another definition of SS, used in analytical calculation, is given by Equation (2):

$$SS = \eta\left(\frac{k_B T}{q}\right)(ln10) \qquad Equation\ (2)$$

where k_B is the Boltzmann constant, T is the temperature in Kelvin, q is the electronic charge and η is the effectiveness of gate-to-channel coupling. Looking at Equation (2), the ideal SS, achieved with 100% electrostatic gate-to-channel coupling at 300K, is ~ 59.6 mV/decade. However, in practice, due to the electrostatic coupling of gate and channel region through the depletion layer, η has a typical value between 1.2 and 1.5 in bulk MOSFETs which results in SS values of 70 – 90 mV/decade.

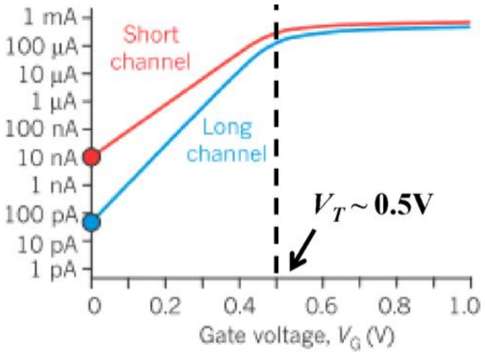


Figure 2.4 Sub-threshold swing (SS), extracted from the linear portion of the red (short channel device) and blue (long-channel device) below threshold, increases as channel length decreases. I_{off} (indicated by the red and blue dots) increases as SS degrades [2.1].

Looking at Figures 2.2 and 2.4, the I_{off} increases for the short-channel MOSFET as compared to the long-channel MOSFET. Thus, it can be said that DIBL and SS degradation has an additive effect for MOSFET I_{off}. Increase in I_{off} has a detrimental effect on the total power consumed per microprocessor [2.5, 2.6]. The total power consumption is found in Equation (3),

$$P = ACV^2f + VI_{off} \quad Equation\ (3)$$

where P is total power consumption per microprocessor, A is the fraction of gates actively switching, C is the total capacitive load of all gates, V and f is the operating voltage and frequency, respectively. It is observed that the overall power consumed consists of dynamic power (first term) and static power (second term). Assuming I_{off} per transistor increases from 10pA to 15 pA and there are 10 million transistors per processor, the processor's leakage current will increase by 50% from 0.1mA to 0.15mA. From this example, it can be understood that the increase in I_{off} will impede the scaling of MOSFETs.

2.2 Reducing Short Channel Effects

In the previous section, we can see that the lack of efficient electrostatic gate-to-channel coupling causes the gate to gradually lose control over the channel formation as the device structure reduces in size and SCEs start to appear. Hence, to counter the SCEs, we need to reinstate the gate with the dominant control of the channel formation. This can be done through the methods, but not limited to, discussed below in Sections 2.2.1 to 2.2.3.

2.2.1 Fully-Depleted (FD) Silicon-On-Insulator (SOI)

First method is to utilize Fully-Depleted (FD) Silicon-On-Insulator (SOI) technology where the entire channel is depleted due to the thin Si body. Moreover, using FD-SOI technology also reduces the S/D to bulk capacitive parasitic and the halo implant damage associated with bulk Si. Furthermore, random dopant fluctuations are significantly minimized in FD-SOI technology as lightly doped or un-doped Si body is used and thus V_T variation is also decreased. Figure 2.5 shows the schematic and TEM micrograph of an ultra-thin FD-SOI nMOS.

Experimental results [2.7, 2.8] have shown that SCEs in FD-SOI MOSFETs can be suppressed significantly through the reduction of the thin Si body. However, the FD-SOI technology also has some drawbacks such as carrier mobility reduction due to the inefficient heat removal caused by the buried oxide beneath the thin Si body [2.9] and enhanced drain leakage currents due to impact ionization and band-to-band tunneling in FD-SOI MOSFETs with slight spacer width variations and lateral doping profiles [2.10].

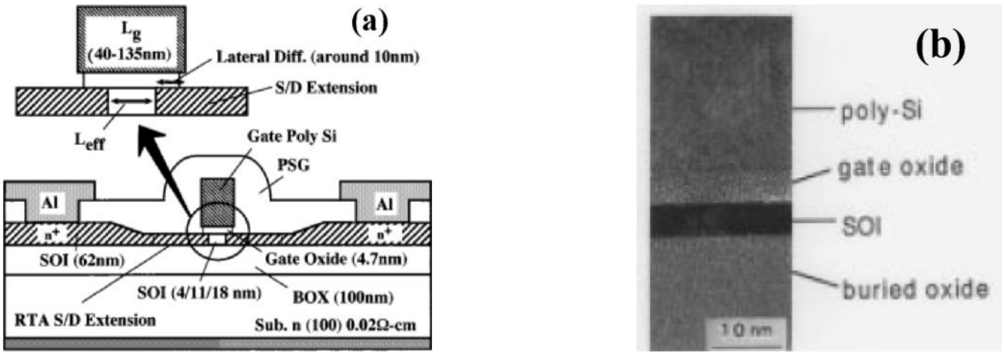


Figure 2.5(a) Cross-sectional schematic of nMOS with ultra-thin SOI layer of 4, 11 and 18nm directly beneath the gate stack that serves as the channel region and (b) shows the Transmission Electron Micrograph (TEM) of the gate region. [2.7]

2.2.2 Reducing gate oxide thickness (T_{ox}) and use of high-K/metal gate stacks

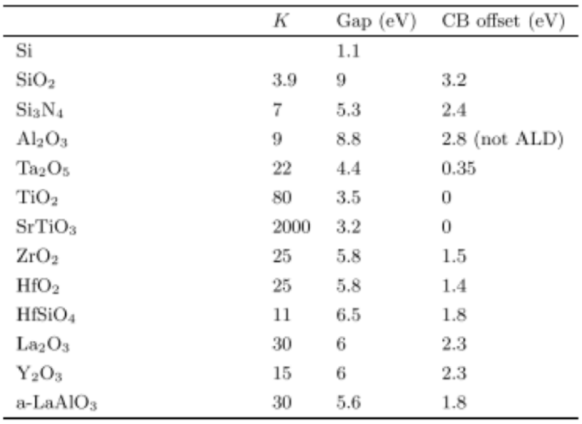
Second method to overcome SCEs is by reducing the gate oxide thickness (T_{ox}) and thus increasing the gate oxide capacitance (C_{ox}) which will enhance the gate-to-channel electrostatic coupling. This method is widely accepted in bulk Si or FD-SOI technology. However, there is a limit to how thin the gate oxide can be reduced since thinner T_{ox} will lead to the increase in gate leakage current (I_{GS}) due to enhanced electronic charge tunneling through the gate oxide. As a consequence, the total power consumption will rise. Typically, the gate leakage current density increases around ten times for every two Å reduction in T_{ox} [2.11].

High-κ dielectrics are thus introduced to replace the conventional SiO_2 as the gate insulator. By using high-κ dielectric as the gate oxide, T_{ox} becomes thicker and I_{GS} reduced drastically. The ability to make use of thicker T_{ox} stems from the idea that the capacitance of high-κ dielectric is equivalent to that of thin SiO2 and the effect of large dielectric constant ratio between high-κ material and SiO2 is shown in Equations (4) and (5):

$$\frac{K_{SiO_2}\varepsilon_o A}{T_{SiO_2}} = \frac{K_{HK}\varepsilon_o A}{T_{HK}} \qquad Equation\ (4)$$

$$T_{HK} = \frac{K_{HK}}{K_{SiO_2}} T_{SiO_2} \qquad Equation\ (5)$$

where K_{SiO2} is the dielectric constant for SiO_2, T_{SiO2} is the thickness of SiO_2 layer, K_{HK} is the dielectric constant for the high-K layer, T_{HK} is the thickness of high-K layer, ε_o is the permittivity of free space and A is the gate area.



	K	Gap (eV)	CB offset (eV)
Si		1.1	
SiO_2	3.9	9	3.2
Si_3N_4	7	5.3	2.4
Al_2O_3	9	8.8	2.8 (not ALD)
Ta_2O_5	22	4.4	0.35
TiO_2	80	3.5	0
$SrTiO_3$	2000	3.2	0
ZrO_2	25	5.8	1.5
HfO_2	25	5.8	1.4
$HfSiO_4$	11	6.5	1.8
La_2O_3	30	6	2.3
Y_2O_3	15	6	2.3
a-$LaAlO_3$	30	5.6	1.8

Table 2.1 Dielectric constants, experimental band-gap and conduction band offsets of various high-κ materials and SiO_2 [2.12]

Table 2.1 shows a list of high-κ materials with their respective dielectric constants, experimental band-gaps and conduction band offset [2.12]. Even though high-κ dielectric is a viable solution to reducing I_{GS} issue, it is incompatible with the use of poly-silicon as the high-κ material can easily react with poly-silicon to form metal silicides within the gate oxide [2.13, 2.14]. This can cause electrical shortage between the gate electrode and the Si substrate. Furthermore, there is interfacial reaction between the high-κ material and poly-silicon which causes an interfacial layer to be formed beneath the high-κ material [2.15-2.17] and Equivalent Oxide Thickness (EOT) of the high-κ layer will increase which reduces the gate oxide capacitance. Hence, high-K dielectric is always used with metal gate stacks such as TiN [2.18-2.20] and TaN [2.19].

2.2.3 Single- to multiple-gated FETs and bulk to nanostructures

The third alternative is to increase the number of gates surrounding the channel region to overpower the influence the effect of the drain. To do so, a third dimension, z, is needed to be introduced to the traditional planar FETs which only constitutes of two dimensions, x and y. This new kind of gated FETs is termed as Multi-Gated FETs or MuGFETs where the gate electrode wraps around several sides of the channel region. Some examples of MuGFETs include vertical double-gate FinFET [2.21-2.24], triple-gate (Tri-gate) MOSFET [2.25, 2.26], Π-gate MOSFET [2.27-2.29], Ω-gate MOSFET [2.30, 2.31] and Gate-All-Around (GAA) transistor [2.32-2.35], are shown in Figure 2.6.

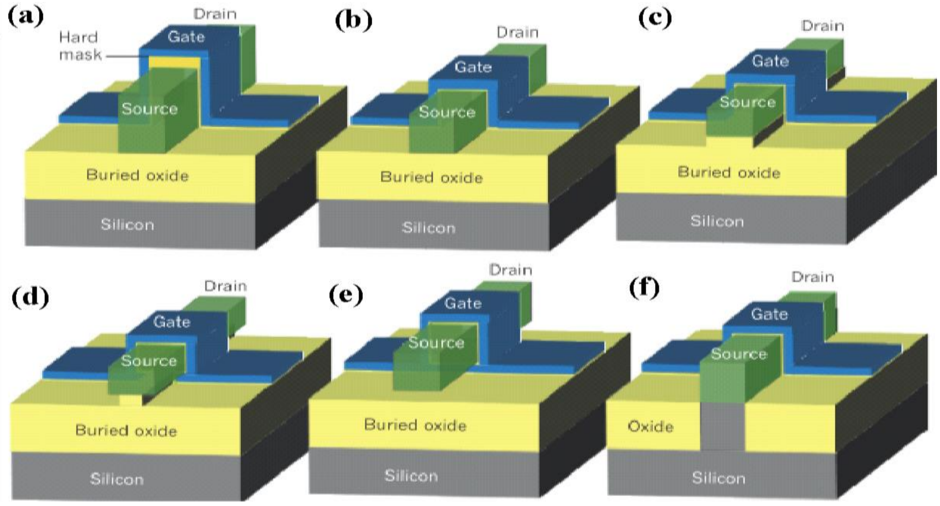


Figure 2.6 Different types of multi-gate MOSFETs include (a) SOI vertical double-gate FinFET, (b) SOI tri-gate FinFET, (c) SOI Π-gate MOSFET, (d) SOI Ω-gate MOSFET, (e) SOI GAA MOSFET and (f) tri-gate FinFET fabricated on Si substrate.

To have reasonable electrostatics and control SCEs at a given gate length (L_G), the critical Si channel thickness, t_{si}, must be one third of L_G [2.8, 2.36]. By replacing single, top-gated MOSFETs with MuGFETS, the effective channel thickness is reduced through the strengthening of gate control over the channel. This will imply the criterion for critical Si thickness is relaxed. Figure 2.7 shows the cross-sectional view of the gate stacks of (a) planar Ultra-Thin-Body (UTB) FD-SOI, (b) double-gate FinFETs, (c) tri-gate FinFETS and (d) GAA nanowire FETs. The critical Si channel thickness criterion is also included for the different gate stacks to demonstrate that GAA nanowire FETs can be considered as a potential candidate for future technology nodes due to the more relaxed channel dimension as compared to the other structures.

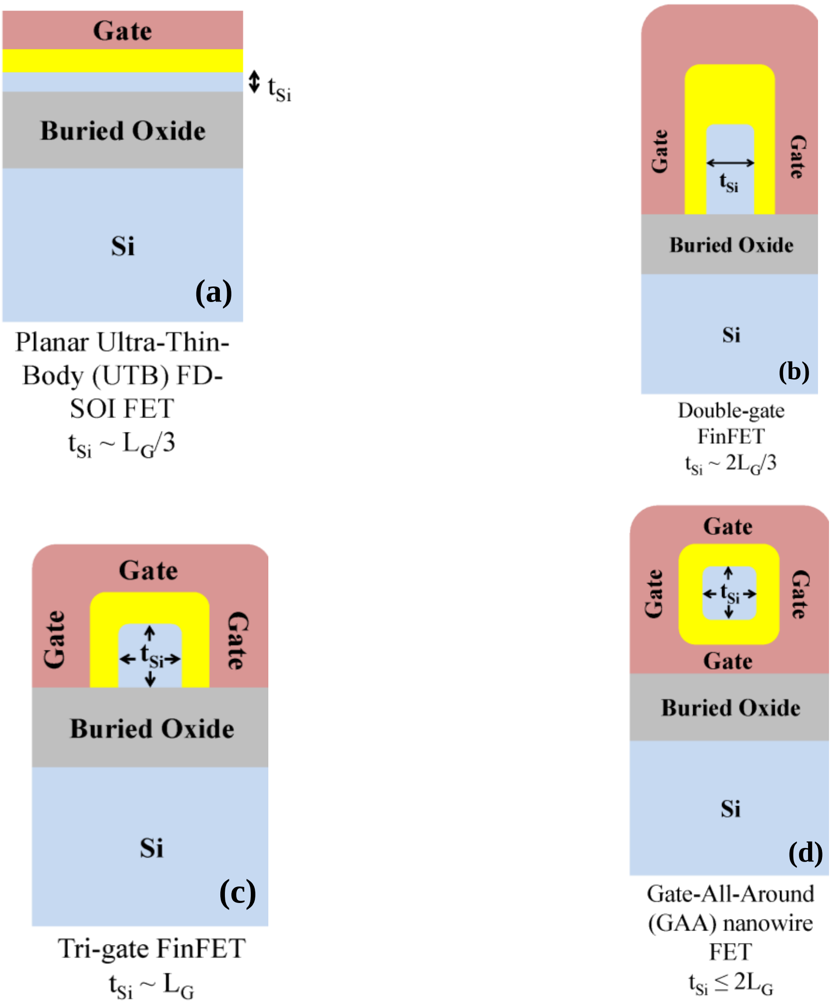
Furthermore, with the increase in the number of gates surrounding the channel, the natural length, λ, a parameter which represents the encroachment of electric field lines from the S/D into the channel, will be significantly reduced [2.36, 2.37]. This implies that, in devices with short-channel lengths, the SCEs can be better controlled or even reduce with the increased number of gates surrounding the channel. The generalized relationship between λ and number of gates, N, is:

$$\lambda_N = \sqrt{\frac{\varepsilon_{Si}}{N\varepsilon_{ox}} t_{ox} t_{Si}} \qquad Equation\ (6)$$

where λ is the natural length, N is the number of gates, ε_{si} is the electrical permittivity of silicon, ε_{ox} is the electrical permittivity of the gate oxide, t_{ox} is the gate oxide thickness and t_{si} is the silicon film thickness.

From the critical Si thickness criterion and the natural length parameter requirement, it is clear that the best architecture to minimize SCEs is Gate-All-Around (GAA) MOSFET where the gate fully surrounds the silicon substrate. To achieve this structure, the logical method is to reduce the dimensions of a Si fin in both lateral and vertical directions. By doing so, we will achieve a free-standing Si nanowire (SiNW) that may come in various shapes such as elliptical [2.35], triangular [2.38], cylindrical [2.39, 2.40] or square [2.41]. No matter what cross-sectional shape the Si nanowire has, the main result is number of gate has increased and the gate length is much larger than the surrounded silicon thickness. Therefore, the free-standing SiNW structure surpasses the requirements for critical t_{si} and natural length.

Currently, there are two main options to fabricate nanowires: (a) bottom-up approach and (b) top-down approach. Each of these approaches has their own pros and cons. The following two sections are dedicated to the discussion of both approaches.



Planar Ultra-Thin-Body (UTB) FD-SOI FET
$t_{Si} \sim L_G/3$

Double-gate FinFET
$t_{Si} \sim 2L_G/3$

Tri-gate FinFET
$t_{Si} \sim L_G$

Gate-All-Around (GAA) nanowire FET
$t_{Si} \leq 2L_G$

Figure 2.7 Cross-sectional schematics of (a) planar Ultra-Thin-Body (UTB) FD-SOI FET with single, top-gate, (b) double-gated FinFET, (c) Tri-gate FinFET and (d) Gate-All-Around (GAA) nanowire FET. The Si thickness, tsi, for each architecture is also shown and it can be seen that the critical Si thickness criterion is relaxed by increasing the number of gates wrapped around Si.

2.3 Silicon nanowire synthesis methods

2.3.1 Bottom-up approach

Typically, SiNWs are synthesized using two different approaches. The first approach is dubbed as the bottom-up approach. Several methods of fabricating nanowires using bottom-up approach had been reported by research groups. In general, these methods consist of: (a) template-directed growth [2.42-2.46], (b) vapor-liquid-solid (VLS) synthesis [2.47-2.51], (c) vapor-solid (VS) growth [2.52-2.55], (d) laser-ablation [2.56-2.59] and (e) electrochemical deposition [2.60-2.63]. In this section, only VLS growth will be discussed as it is the most well-studied and reported fabrication method for nanowire synthesis.

In VLS growth method, nanowires are grown on clean and defect-free semiconductor substrates or insulators such as sapphire or glass. The process normally takes place in a vacuum chamber to greatly reduce contamination issues. Using Si substrate as an example, the VLS process starts by depositing a layer of metal catalyst (for example, Au) onto the Si substrate. Subsequently, the substrate is heated such that the temperature is higher than the eutectic point of the Au-Si system, which can be referred from the binary phase diagram, such that Au-Si liquid alloy droplets are formed on the surface of Si substrate.

Following that, precursor gas carrying Si atoms will be flown into the chamber and the Si atoms dissolve into the droplets. These droplets lower the activation energy of normal vapour-solid growth and thus, they are energetically favoured sites for the incoming Si atoms. The adsorption of Si atoms by the alloy droplets continue until a super-saturated state of Si in Au is reached. Upon which, Si atoms will start to precipitate out of the Au-Si alloy at the liquid alloy/solid Si interface. This process is illustrated in Figure 2.8. With the continuation of adsorption and precipitation of Si atoms at the liquid/solid interface, the Si nanowire grows in height.

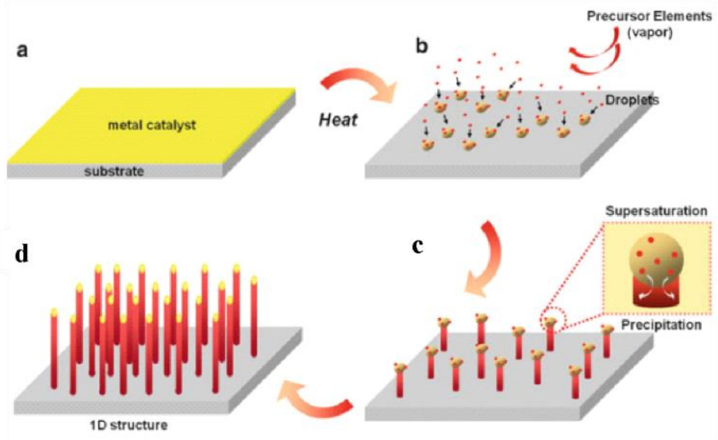


Figure 2.8 Growth of 1D-nanowires by Vapour-Liquid-Solid mechanism whereby (a) the metal catalyst film is deposited onto the substrate and agglomerate to form liquid alloy droplets upon subjected to high temperature. Following that, (b) precursor gases are released into the system and the reactant atoms are absorbed by the droplets and (c) the reactant atoms start to precipitate out of the liquid alloy at the liquid alloy/substrate interface and form crystalline nanostructure when the droplet becomes super-saturated with the reactant atoms. As the process continues, the nanowires increase in height as shown in (d) [2.64].

The metal catalyst is one of the major components in the VLS synthesis. However, the choice of metals needs to fulfill some requirements before the VLS synthesis of nanowires is able to succeed. First, it must be able to form liquid solution with a solid phase component. Second, the catalyst component in liquid phase must have a much higher solubility limit than that in solid phase such that liquid alloy with little contamination can form at ease. Third, vapour pressure of the catalyst component is much smaller as compared to the liquid alloy. Fourth, the metal is chemically inert such that no intermediate solid is formed [2.64]. So far, noble and transition metals are suitable for VLS growth. For example, Au is the most frequently used metal to grow Group IV and III-V nanowires. Some transition metals such as Ni and Fe are also used by research groups [2.65-2.67]. Phase diagrams of Au-Si, Fe-Si and Ni-Si systems are shown in Figure 2.10.

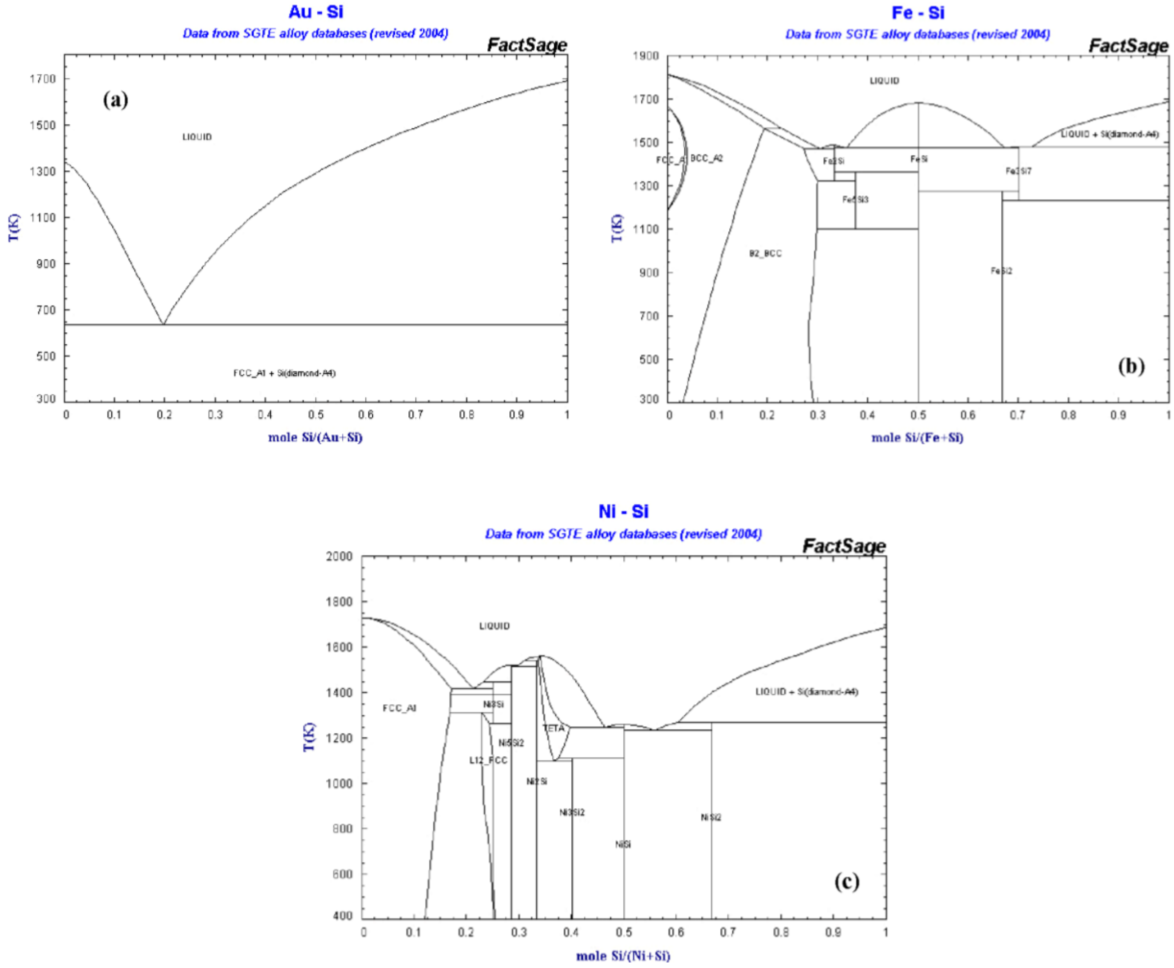


Figure 2.10 Binary phase diagrams of (a) Au-Si, (b) Fe-Si and (c) Ni-Si systems [2.65].

The advantages of the VLS synthesis method are (a) the size of the nanowires is determined by the size of the alloy droplet formed on the starting substrate. The droplet size is, in turn, determined by the initial thickness of the deposited metal catalyst layer [2.68]; (b) uniform in-situ doping [2.69-2.71] can be obtained via the inclusion of doping gases, such as PH_3 or B_2H_6, during the growth process; (c) atomically abrupt junctions are achievable by switching the gas sources [2.72, 2.73]. Moreover, the bottom-up VLS synthesis approach is free of photo-lithography and photo-masks. This will, in turn, allow the VLS process to be highly cost effective and attain high economy of scale.

However, the main challenge posed by this method is finding an economical yet reliable path to successfully integrate the synthesized nanowires into functional Integrated Circuits (ICs) in large scale. Generally, the synthesized nanowires are randomly dispersed over the substrate wafer since there is no control over the location where the alloy droplet will form and furthermore, complex techniques are required to organize the nanowires into specific device architectures to achieve certain functionalities. Some of these techniques include the use of Atomic Force Microscopy (AFM) tip for ‘pick-and-place’ [2.74, 2.75], liquid suspension [2.76] and electric- or magnetic-field methodologies [2.77-2.79]. These techniques lack repeatability and have low throughput, both of which are critical criteria in industry production. Therefore, there are very limited opportunities for the nanowires realized by the bottom-up approach to be commercialized.

2.3.2 Top-down approach

The top-down approach is a more feasible alternative for the commercialization of nanowires because the fabrication steps used are compatible to the standard CMOS processes found in the industry. Typically, the top-down methodology involves photo-lithography, dry and/or wet chemical etching and oxidation steps. Due to the high cost involved in photo-lithography and writing photo-masks, some research groups have successfully replaced it with a new technique known as nano-imprint lithography (NIL) [2.80-2.82]. In NIL, patterns are created by deforming the imprint resist mechanically and then they are transferred to the underneath substrate through dry etching.

Photo-lithography will be used for the discussion in the remaining section since it is highly utilized by many research groups. In general, there are four basic steps, involved in the top-down approach, to achieve nanowires. First, the wafer substrate, for example Si, is coated with photo-resist (PR), exposed and lastly developed. The intended patterns are imprinted onto the PR that remains on the wafer substrate. Optional Reactive Ion Etch (RIE) trimming of the PR is performed to achieve smaller PR dimension. Second, using PR as the hard-mask, physical dry etching of Si is done to remove the unwanted Si regions and depending on the initial mask design, a lateral Si fin or a vertical Si pillar is obtained.

Third, thermal oxidation is performed to reduce the size of the vertical Si pillar or lateral fin. In the case of vertical Si pillar, due to the effect of self-limiting oxidation, there is a lower limit on the diameter of the final nanowire. For the lateral Si fin, depending on the fin height, 2 or more nanowires may be formed stacked one on top of the other. The self-limiting oxidation effect will also occur in the case of lateral Si fin. Lastly, free-standing nanowires are achieved via the removal of the SiO_2 shell (from the previous step) by dipping the wafer into Diluted Hydro-Fluoric acid (DHF).

Self-limiting oxidation effect is first reported by Liu *et al.* [2.83] in 1993. In his work, thick vertical Si columns are first fabricated via electron-beam lithography (EBL) and NF_3 plasma RIE etching. Following that, the Si columns are subjected to the first round of thermal oxidation to grow ~ 9nm of SiO_2 around the Si columns. This is to remove the Si sidewall damage caused by RIE and impurity residual effects such that a clean Si surface is available for subsequent oxidation studies. The oxidation studies using Si columns are done at 800 ^{0}C and 850 ^{0}C with varying time (1.5 to 44hrs). Figure 2.11 shows the Si columns prior to the oxidation studies.

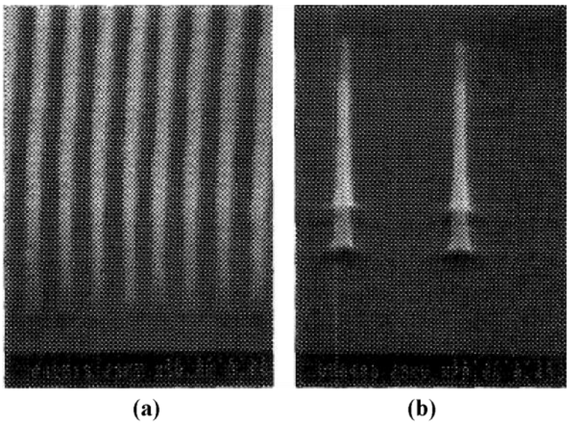


Figure 2.11 SEM micrographs of NF_3 plasma etched Si nanocolumns. (a) Large areas dense array of 60 nm wide x 0.7 µm tall Si columns. (b) A 2 x 2 matrix of Si columns about 43nm in diameter and 0.7 µm in height [2.83].

It was found that the final Si core diameter achieved was self-limited to 11nm for 800 ^{0}C after 15hrs of oxidation and 6nm for 850 ^{0}C after 8hrs of oxidation, prolonged oxidation duration has no effect in further reducing the Si core diameter. There is substantial reduction in the diameter variation along the non-uniform region of the column as shown in Figure 2.12.

Another observation seen in Figure 2.12 is the bottom portion of Si column near the substrate has larger diameter and it oxidizes faster than the middle portion of Si column. This showed that the oxidation rate depends on the column diameter. The smaller (larger) the diameter (curvature), the slower the column oxidizes. Apart from the column diameter dependency, the oxidation rate was also found to be dependent on the column oxide thickness. For a given column diameter, thicker column oxide reduced the oxidation rate.

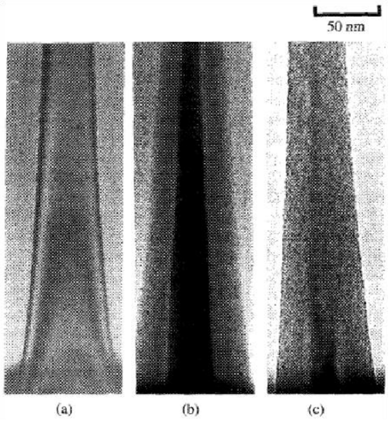


Figure 2.12 TEM micrographs of the bottom non-uniform regions of Si columns after (a) 0hr, (b) 8hrs and (c) 16hrs of thermal oxidation at 850 ^{o}C [2.83].

The cause of self-limiting oxidation effect seen in Si nanowire (SiNW) is believed to be the result of the retarded oxidation of the Si core induced by the stress normal to the Si/SiO$_2$ interface. Using the basic mechanism in a dry oxidation process, Liu et al. [2.83] explained that oxygen atoms need to diffuse through the already formed oxide layer to react with the Si at the interface and form SiO$_2$. This newly formed SiO$_2$ layer then pushes out the old oxide to allow for volume expansion. Importing this idea to SiNW with large curvature, Liu et al. [2.83] further explained that the old oxide layer needed to expand more to make room for the increase in volume and given that SiO$_2$ is extremely viscous below 960 ^{0}C [2.88], the expansion of the old oxide layer would cause a great stress normal to the Si/SiO$_2$ interface and hence, the process of further oxidation was impeded.

By modifying the Deal-Grove's planar oxidation model with the appropriate boundary conditions in cylindrical coordinates and model the oxidation kinetics as diffusion-limited:

$$\frac{dx_0}{dt} = \frac{1}{N}\frac{C^*}{[(\frac{x_0}{D})r_c ln\,(\frac{r_0}{r_c})\,]} \qquad Equation\ (7)$$

Liu et al. [2.84] to express the oxidation rate (dx_0/dt) for a SiNW (Equation 7) in terms of N (oxide density), C* (the oxidant solubility in the oxide), D (the diffusivity of oxidant in the oxide), r_c (SiNW core radius) and r_0 (the outer radius of an oxidized SiNW).

Furthermore, by plotting the diffusivity activation energies (ED) as a function of γ ($\gamma \equiv r0/rc$), which is related to oxide stress through the oxide strain energy, it can be observed that ED increases with increasing γ as shown in Figure 2.13 (a). This implied that an increase in ED in a highly stressed oxide reduces the diffusion of the oxidizing species and this could be a possible cause for the oxidation rate of SiNW to slow down in the self-limiting regime. In addition, from the experimental data, the dependence of final SiNW core diameter on the starting Si column diameter was also observed in Figure 2.12 (b).

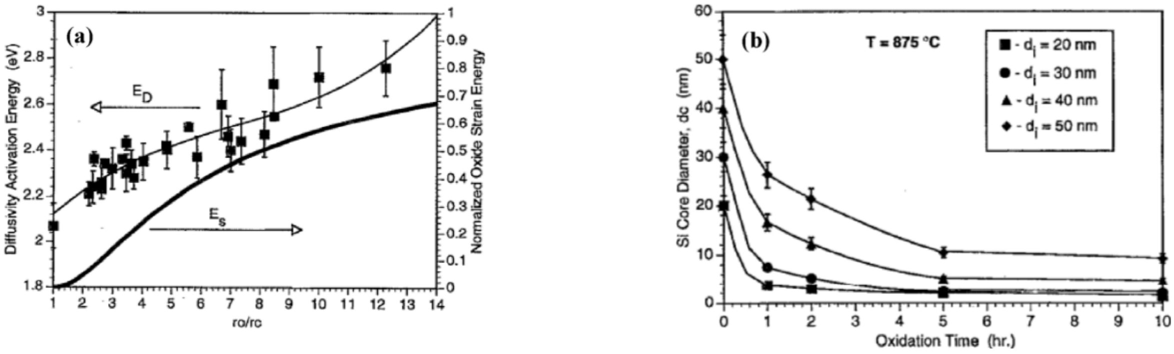


Figure 2.13 (a) illustrates the increase of diffusivity activation energy (ED) with the increase of γ and the oxide strain energy also shows the same trend. Figure 2.13 (b) shows that the final Si core diameter at the self-limited regime is dependent on the initial Si column before oxidation.

The oxidation kinetics model was further enhanced by Cui et al. [2.85] whereby in their kinetic model, they assumed that the diffusion of the oxidizing species dominates the oxidation of SiNWs. Furthermore, they also suggested that there is a region (~1nm) of high density oxide near the Si/SiO_2 interface and the oxide density increases monotonically with oxidation. Interfacial stress caused a change in the distribution of ED in the high density oxide and resulted in self-limiting oxidation behavior in SiNWs. Consequently, their model was in close agreement with the initial fast oxidation regime, which was attributed to the higher surface Si atom ratio and the enhancement of the equilibrium concentration of the oxidant and with the self-limiting regime, which was caused by the suppressed diffusion of oxidants due to the existence of the high density oxide region near the Si/SiO_2 interface as shown in Figure 2.14.

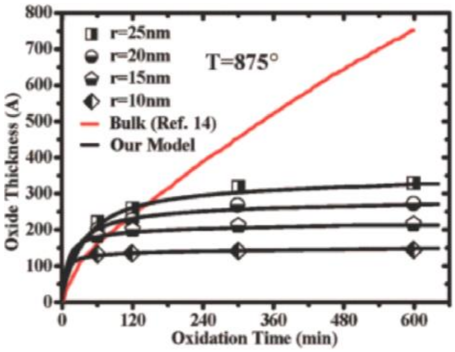


Figure 2.14 Close agreement between the experimental data from Lui et al. [2.84] and the simulation data from Cui et al. model [85]. The model successfully replicates the exponential increase in the oxidation thickness from 0 min to ~ 120 mins and the self-limiting oxidation effect from 120 mins onwards.

Besides the modeling of oxidation kinetics to find the root cause of self-limiting oxidation in SiNWs, Ma et al. [2.86] extended the idea and incorporated SiNW shape engineering into his model. In his experiment, SiNWs are fabricated from the oxidation of Si fins, with (100) orientation at the top surface and (110) orientation at the side-walls, built on SOI wafers. Similar to the previous models discussed, Ma et al. attributed the self-limiting effect in oxidizing SiNWs to the extremely reduced diffusivity of oxidants as a result of the high compressive hydrostatic pressure near the Si/SiO_2 interface. In addition, the retardation of oxidant diffusivity is orientation-dependent with (100) plane suffering more severe stress retardation than (110) plane. Furthermore, Ma et al. also used his model to predict the final shape of the SiNW after oxidation. Figure 2.15 illustrates the close agreement of the final SiNW cross-sectional shape from TEM and simulation results using Ma et al.'s model.

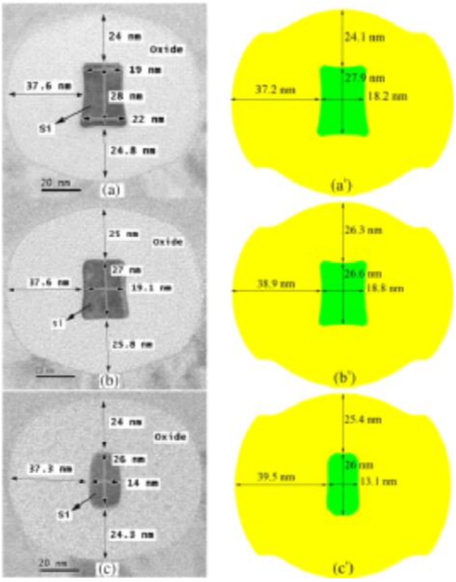


Figure 2.15 Simulation and TEM results showing close agreement with one another. (a)-(a') 850 ºC after 22hrs, (b)-(b') 875 ºC after 15hrs, (c)-(c') 975 ºC after 2hrs [2.86].

2.4 Schottky barrier (SB) Source/Drain (S/D) transistors

2.4.1 Fundamentals of Schottky barrier

Schottky barrier is a potential barrier formed at a metal-semiconductor (MS) junction. The barrier can be identified in the energy diagram shown in Figure 2.16. According to Schottky-Mott rule, Schottky barrier height (SBH) or Φ_B is predicted to be the difference between metal work function (Φ_m) and the electron affinity (χ_s) of the semiconductor and is expressed as follows

$$\Phi_B \approx \Phi_m - \chi_S \quad Equation\ (8)$$

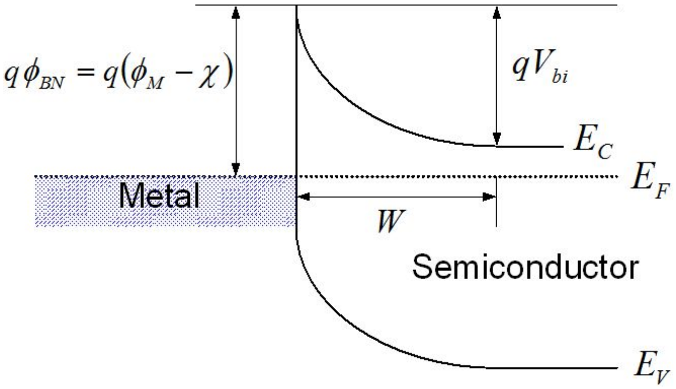


Figure 2.16 Φ_B band diagram of an arbitrary MS Schottky diode.

The Schottky Barrier Height (SBH) is dependent on the work function of the metal used and the semiconductor material listed in [2.87]. Φ_B calculated in Equation (8) assumes that there are zero metal-induced gap states (MIGS) or surface states such as surface dangling bonds and impurities [2.89-2.91]. However, in practice, Φ_B is strongly influenced by Fermi level pinning caused by MIGS and surface states. Taking into account of Fermi level pinning, the general form of Φ_B is [2.92]:

$$\Phi_B \approx \Phi_m - \chi_S + qV_{int} \qquad Equation\ (9)$$

where V_{int} is the voltage drop across the dipoles and/or charge re-distribution between the metal and semiconductor during the MS interface formation, and q is the electronic charge.

Mönch attempted to explain the dependence of Φ_B of a MS junction through adding charge density from MIGS into the charge neutrality equation in [2.89]:

$$Q_M = Q_S + Q_{MIGS} \qquad Equation\ (10)$$

where Q_M is the charge density on metal side, Q_S is the space charge density of semiconductor and Q_{MIGS} is the charge density contributed by MIGS. In addition, Φ_B can be correlated to the electronegativity difference between the metal and semiconductor by assuming a charge neutrality level whereby MIGS above and below this level have acceptor-like and donor-like behaviors, respectively. Hence, the relationship between SBH and electronegativity difference, assuming the MS junction is abrupt, defect-free and laterally homogeneous, can be given as

$$\Phi_B = \Phi_{CNL} + S_X(X_M - X_S) \qquad Equation\ (11)$$

where Φ_{CNL} corresponds to charge neutrality level, X_M and X_S denote the electronegativity of metal and semiconductor and S_X is a fitting parameter called the slope parameter. Figure 2.17 depicts Fermi level pinning as a result of MIGS.

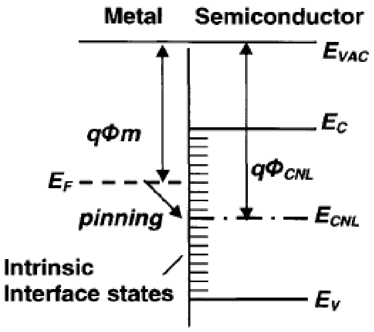


Figure 2.17 Energy band diagram showing Fermi level pinning at MS interface.

Another school of thought by Tung suggested the cause of Fermi level pinning is due to the chemical bonding to achieve thermodynamic equilibrium at the MS interface [2.92, 2.93]. The nature and morphology of the very first interfacial layer of the MS contact when metal first comes into contact with semiconductor is highly dependent on the chemical reactions, surface diffusion and inter-diffusion. Therefore, interfacial defects are created and dominate Φ_B. Through experiments [2.94], the effect of interfacial structure on Φ_B can be observed as Φ_B becomes dependent on the epitaxial orientation of $NiSi_2$.

2.4.2 Operating principles of Schottky Barrier S/D transistors

The operating principles of Schottky Barrier MOSFET are illustrated and compared with those of conventional MOSFET in Figure 2.18.

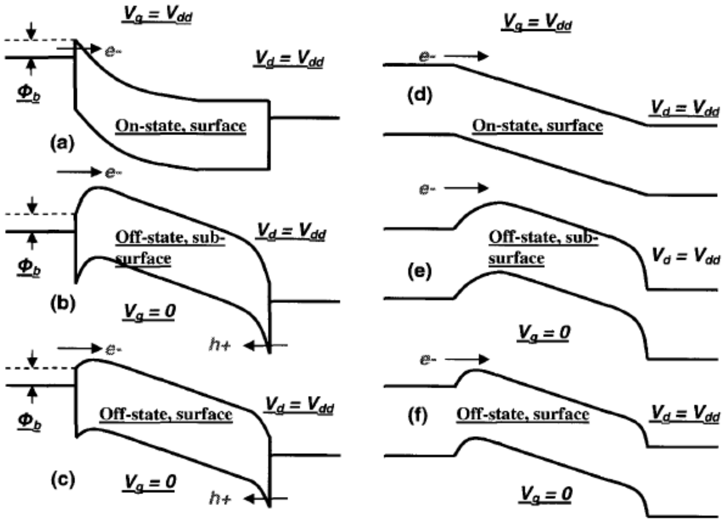


Figure 2.18 Band diagram on surface and sub-surface of (a-c) SB-NMOS and (d-f) conventional NMOS [2.95].

When a positive gate voltage is applied, the semiconductor channel is bent downwards. This causes the barrier to electron injection from the source into the channel to be lowered and thermionic emission (TE) occurs. As the gate voltage increases, the barrier is further lowered. When the barrier is lowered to be equal to Φ_B, the drive current is limited by Thermionic Field Emission (TFE), i.e., tunneling through the Schottky barrier. The main carriers, in this case, are electrons. In theory, hole current can also be conducted by the same mechanisms from the drain side but because of the V_{bi}, the effective Φ_B to holes is high and hole current is suppressed. By increasing the gate and/or drain bias, the effective Φ_B to electrons can be substantially reduced by image force barrier lowering [2.96, 2.97]. At the same time, the barrier width is thinned significantly as a result of high electric field at source to channel junction [2.91, 2.95] and tunneling of electrons is enhanced. Hence, current is increased by increasing gate/drain bias.

SB MOSFET exhibits ambipolar conduction whereby the flow of current for both positive and negative gate biases is contributed by both the electron current from the source and hole current from the drain. Thus, whether the MOSFET behaves as NMOS or PMOS depends entirely on the bias conditions and not on the Fermi level of semiconductor (as in the case of conventional MOSFET) or Φ_B of MS junction. It is worthwhile to take note that SB MOSFET has two main disadvantages compared to conventional MOSFET: (1) SB MOSFET has lower drive (on-state) current since the current is TFE-limited. (2) SB MOSFET has higher leakage (off-state) current due to ambipolar conduction.

2.4.3 Schottky Barrier Height Tuning

In the previous section, the current transport mechanism of SB MOSFET has been discussed. Clearly, SB MOSFET performance is hindered by the existence of Φ_B and it is vital to have low electron SBH (n-SBH) for NMOS and hole SBH (p-SBH) for PMOS. In this section, various SBH tuning methodologies will be discussed.

To implement complementary performance in SB MOSFET, both NMOS and PMOS are required. This can be achieved by using two different silicides, one having low p-SBH for PMOS and one having low n-SBH for NMOS. $ErSi_{2-x}$ with n-SBH between ~ 0.27eV to 0.32 eV [2.95, 2.98, 2.99] and PtSi with p-SBH between ~ 0.15 eV to 0.24 eV [2.100-2.102] are used for NMOS and PMOS, respectively. Apart from $ErSi_{2-x}$ and PtSi, $YbSi_{2-x}$ and IrSi have been proposed to give lower n-SBH and p-SBH, respectively. Zhu *et al.* [2.103] fabricated SB-NMOS using $YbSi_{2-x}$ as S/D material and reported higher drive current and lower leakage compared to $ErSi_{2-x}$. They attributed the improved performance to lower n-SBH and smoother $YbSi_{2-x}$/Si interface. Through empirical calculations, IrSi presents the lowest p-SBH with an extracted value of ~ 0.11 eV [2.104]. However, IrSi has not been applied experimentally to SB-PMOS.

The stumbling block to use 2 different materials for NMOS and PMOS separately is the need for additional processing steps. This means silicide for NMOS has to be formed first followed by the formation of silicide on PMOS. This incurs extra costs since additional masking layers are required. In retrospect, research has since been re-focused on mid-gap silicides, including $TiSi_2$, $CoSi_2$, NiSi with SBH ~ 0.6 eV as a result of the simplicity in process steps [2.105-2.108]. Therefore, the SBH tuning methods used must focus on these mid-gap silicides to achieve low effective SBH.

2.4.4 Dopant Segregation Technique – a viable solution to tune Schottky Barrier Height of mid-gap silicide

Dopant segregation works on the principle of difference in solid solubility of dopants in silicide and silicon. When silicidation occurs on a doped silicon substrate, dopants are found to “pushed” out of the silicide where they are piled up at the silicide/silicon interface to form a very thin, high concentration doping layer with a very steep profile [2.100-2.110]. A typical SIMS profile of dopant segregation on bulk Si substrate is shown in Figure 2.19.

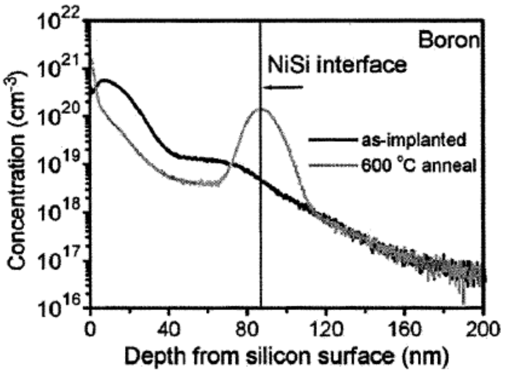


Figure 2.19 Typical SIMS profile of boron doped Si substrate before and after NiSi formation. High concentration of boron atoms is found at the NiSi/Si interface [2.100].

Currently, there are two methods to engineer dopant segregation. The first option is known as silicidation induced dopant segregation (SIDS) which is described above. This method will also be used for the work in this dissertation. The second option is silicide as diffusion source (SADS) where dopants are pre-implanted into the silicide and subsequently, thermal annealing is employed to diffuse the dopants to the silicide/silicon interface [2.100].

Kinoshita et al. first attempted to integrate dopant segregation into silicided S/D regions of SB MOSFET in an effort to reduce Φ_B, so as to achieve higher device drive current with lower leakage. The term Dopant Segregated Schottky (DSS) MOSFET was thus coined [2.106]. The DSS MOSFET architecture was illustrated in Figure 2.20. There are two important aspects to keep in mind in order to achieve SBH modulation without losing the merits of Schottky junctions: (1) the dopant layer must be sufficiently thin (< 5nm) to be fully depleted and (2) the dopant layer must have concentration > 1 x 10^{20} atoms/cm^3.

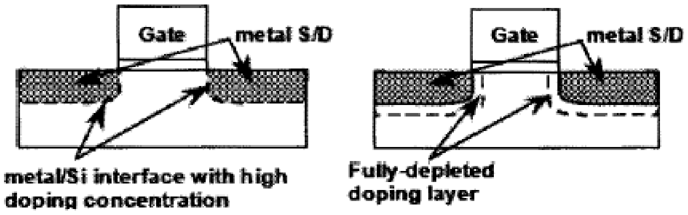


Figure 2.20 Schematics of (a) ideal DSS MOSFET with ultra-thin segregated regions and (b) a practical DSS MOSFET with finite yet fully depleted segregated regions [2.106].

The beauty of utilizing DSS is the additional contact potential at the metal-silicon junctions, which effectively increase the barrier height for off-state carriers and reduce the barrier width for on-state carriers. The working mechanisms of on- and off-state carrier transport is shown in Figure 2.21 with band diagrams.

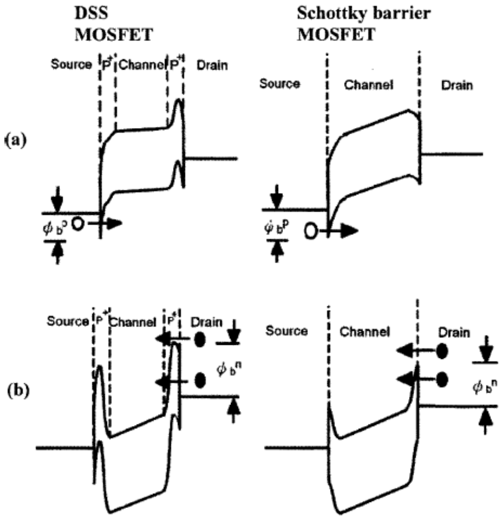


Figure 2.21 Energy band diagrams during (a) on-state and (b) off-state of DSS and Schottky PFETs [2.111].

When the device operates in on-state as shown in Figure 2.21 (a), the segregated dopant region reduces the depletion width of the source and channel which enhances the tunneling of holes through the barrier. Furthermore, the drain receives additional built-in potential from the distorted energy band. Therefore, electrons 'see' a higher barrier height and electron current is reduced. Hence, the effective drive current is improved by hole injection from the source side. On the contrary, when the device is in the off-state, the additional built-in potential at the drain side prevented electron tunneling. Hence, the overall leakage current is greatly suppressed. Figure 2.22 depicts the transfer characteristic of DSS MOSFET reported in [2.111].

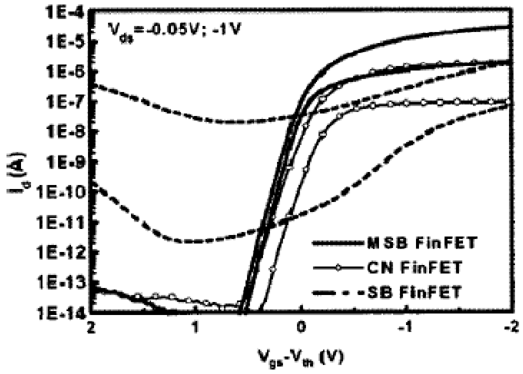


Figure 2.22 Transfer characteristics of DSS MOSFET shown as Modified Schottky Barrier (MSB) FinFET, conventional MOSFET (CN FinFET) and Schottky Barrier MOSFET (SB FinFET) in [2.111].

2.5 Nickel Silicide

Nickel silicide shows several advantages over $TiSi_2$ and $CoSi_2$ and this propels the industry to switch to nickel silicide for contact metallization. Amongst the three silicides, nickel silicide is formed at very low temperature (~ 400 ^{0}C), has the least silicon consumption, smooth silicide/Si interface, lowest specific resistivity, insensitivity to Si substrate doping and no “fine-line effect” [2.112-2.114]. Based on binary phase diagram, there are six stable nickel silicide phases at room temperature (Ni_3Si, $Ni_{31}Si_{12}$, Ni_2Si, Ni_3Si_2, NiSi and $NiSi_2$).

In the case of thin film reaction between Ni and Si, it is discovered that there is a sequential phase. In situations where $T_{Ni} << T_{Si}$ (T_{Ni} = Ni thickness, T_{Si} = Si thickness), the silicides are formed in the order of $Ni_2Si \rightarrow NiSi \rightarrow NiSi_2$. However, in the case where $T_{Ni} >> T_{Si}$, the silicides are formed in the order of $Ni_2Si \rightarrow Ni_5Si_2 \rightarrow Ni_3Si$. Despite its numerous advantages, NiSi was not the first candidate of choice due to its low morphological and thermal stability. NiSi agglomeration issue is reported to occur between 550 ^{0}C and 600 ^{0}C [2.115, 2.116]. In addition, at 700 ^{0}C, NiSi phase becomes unstable and transforms into $NiSi_2$ phase which has three times higher specific resistivity [2.117]. On top of that, $NiSi_2$ phase is accompanied by 1.7 times volume expansion which implies higher Si consumption and $NiSi_2$ typically has a rough surface and interface [2.118]. These observations are deem $NiSi_2$ undesirable for junction integration.

2.6 Summary

The background and relevant theories of short-channel effects (SCEs) have been covered, together with the options to suppress SCEs. Also, the relevant concepts of SiNW formation by bottom-up and top-down approaches have been discussed. In addition, concepts on Schottky barrier formation, the operation and architecture of Schottky barrier MOSFET have been discussed. Lastly, dopant segregation technique has also been introduced and discussed.

2.7 References

[2.1] I. Ferain, C. A. Colinge, and J. P. Colinge, "Multigate transistors as the future of classical metal-oxide-semiconductor field-effect transistors," Nature, vol. 479, pp. 310-6, Nov 17 2011.

[2.2] R. R. Troutman, "VLSI Limitations from Drain-induced Barrier Lowering," IEEE Journal of Solid-State Circuits, vol. SC-14, p. 9, 1979.

[2.3] M. J. Deen and Z. X. Yan, "DIBL in short-channel NMOS devices at 77 K," Electron Devices, IEEE Transactions on, vol. 39, pp. 908-915, 1992.

[2.4] K. Goto, Y. Tagawa, H. Ohta, H. Morioka, S. Pidin, Y. Momiyama, et al., "High performance 25 nm gate CMOSFETs for 65 nm node high speed MPUs," in Electron Devices Meeting, 2003. IEDM '03 Technical Digest. IEEE International, 2003, pp. 27.1.1-27.1.4.

[2.5] N. S. Kim, T. Austin, D. Baauw, T. Mudge, K. Flautner, J. S. Hu, et al., "Leakage current: Moore's law meets static power," Computer, vol. 36, pp. 68-75, 2003.

[2.6] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage Current Mechanisms and Leakage Reduction Techniques in Deep-Submicrometer CMOS Circuits," Proceedings of the IEEE, vol. 91, p. 23, 2003.

[2.7] E. Suzuki, K. Ishii, S. Kanemaru, T. Maeda, T. Tsutsumi, T. Sekigawa, et al., "Highly suppressed short-channel effects in ultrathin SOI n-MOSFETs," Electron Devices, IEEE Transactions on, vol. 47, pp. 354-359, 2000.

[2.8] K. K. Young, "Short-channel effect in fully depleted SOI MOSFETs," Electron Devices, IEEE Transactions on, vol. 36, pp. 399-402, 1989.

[2.9] P. T. Tran, "Overview of fully depleted silicon-on-insulator (SOI) technology," in University/Government/Industry Microelectronics Symposium, 2003. Proceedings of the 15th Biennial, 2003, pp. 370-371.

[2.10] R. J. Luyken, M. Specht, W. Rosner, J. Hartwich, F. Hofmann, L. Dreeskornfeld, et al., "Drain leakage mechanisms in fully depleted SOI devices with undoped channel [MOSFETs]," in European Solid-State Device Research, 2003. ESSDERC '03. 33rd Conference on, 2003, pp. 419-422.

[2.11] G. C.-F. Yeap, "Leakage current in low standby power and high performance devices: trends and challenges," presented at the Proceedings of the 2002 international symposium on Physical design, San Diego, CA, USA, 2002.

[2.12] J. Robertson, "High dielectric constant oxides," The European Physical Journal - Applied Physics, vol. 28, pp. 265-291, 2004.

[2.13] D.-G. Park, K.-Y. Lim, H.-J. Cho, J.-J. Kim, J.-M. Yang, J.-K. Ko, et al., "Boron penetration and thermal instability of p[sup +] polycrystalline-Si/ZrO[sub 2]/SiO[sub 2]/n-Si metal-oxide-semiconductor structures," Journal of Applied Physics, vol. 91, pp. 65-68, 2002.

[2.14] M. Gutowski, J. E. Jaffe, C.-L. Liu, M. Stoker, R. I. Hegde, R. S. Rai, et al., "Thermodynamic Stability of High-K Dielectric Metal Oxides ZrO2 and HfO2 in Contact with Si and SiO2," MRS Online Proceedings Library, vol. 716, pp. null-null, 2002.

[2.15] W. Xuguang, J. Peterson, P. Majhi, M. I. Gardner, and K. Dim-Lee, "Impacts of gate electrode materials on threshold voltage (Vth) instability in nMOS HfO2 gate stacks under DC and AC stressing," Electron Device Letters, IEEE, vol. 26, pp. 553-556, 2005.

[2.16] G. Bersuker, C. S. Park, J. Barnett, P. S. Lysaght, P. D. Kirsch, C. D. Young, et al., "The effect of interfacial layer properties on the performance of Hf-based gate stack devices," Journal of Applied Physics, vol. 100, pp. 094108-6, 2006.

[2.17] M. H. Hakala, A. S. Foster, J. L. Gavartin, P. Havu, M. J. Puska, and R. M. Nieminen, "Interfacial oxide growth at silicon/high-k oxide interfaces: First principles modeling of the Si--HfO2 interface," Journal of Applied Physics, vol. 100, pp. 043708-7, 2006.

[2.18] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, and M. Metz, "High-k / metal-gate stack and its MOSFET characteristics," Electron Device Letters, IEEE, vol. 25, pp. 408-410, 2004.

[2.19] L. Å. Ragnarsson, T. Chiarella, M. Togo, T. Schram, P. Absil, and T. Hoffmann, "Ultrathin EOT high-κ/metal gate devices for future technologies: Challenges, achievements and perspectives (invited)," Microelectronic Engineering, vol. 88, pp. 1317-1322, 2011.

[2.20] K. Choi, H. Jagannathan, C. Choi, L. Edge, T. Ando, M. Frank, et al., "Extremely scaled gate-first high-k/metal gate stack with EOT of 0.55 nm using novel interfacial layer scavenging techniques for 22nm technology node and beyond," in VLSI Technology, 2009 Symposium on, 2009, pp. 138-139.

[2.21] D. Hisamoto, L. Wen-Chin, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," Electron Devices, IEEE Transactions on, vol. 47, pp. 2320-2325, 2000.

[2,22] H. Xuejue, L. Wen-Chin, K. Charles, D. Hisamoto, C. Leland, J. Kedzierski, et al., "Sub 50-nm FinFET: PMOS," in Electron Devices Meeting, 1999. IEDM '99. Technical Digest. International, 1999, pp. 67-70.

[2.23] C. Yang-Kyu, K. Tsu-Jae, and H. Chenming, "Nanoscale CMOS spacer FinFET for the terabit era," Electron Device Letters, IEEE, vol. 23, pp. 25-27, 2002.

[2.24] Y. Bin, C. Leland, S. Ahmed, W. Haihong, S. Bell, Y. Chih-Yuh, et al., "FinFET scaling to 10 nm gate length," in Electron Devices Meeting, 2002. IEDM '02. International, 2002, pp. 251-254.

[2.25] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, et al., "High performance fully-depleted tri-gate CMOS transistors," IEEE Electron Device Letters, vol. 24, pp. 263-265, 2003.

[2.26] B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, et al., "Tri-Gate fully-depleted CMOS transistors: fabrication, design and layout," in VLSI Technology, 2003. Digest of Technical Papers. 2003 Symposium on, 2003, pp. 133-134.

[2.27] P. Jong-Tae, J. P. Colinge, and C. H. Diaz, "Pi-Gate SOI MOSFET," Electron Device Letters, IEEE, vol. 22, pp. 405-406, 2001.

[2.28] P. Jong-Tae and J. P. Colinge, "Multiple-gate SOI MOSFETs: device design guidelines," Electron Devices, IEEE Transactions on, vol. 49, pp. 2222-2229, 2002.

[2.29] J. P. Colinge, X. Weize, C. R. Cleavelin, T. Schulz, K. Schrufer, K. Matthews, et al., "Room-Temperature Low-Dimensional Effects in Pi-Gate SOI MOSFETs," Electron Device Letters, IEEE, vol. 27, pp. 775-777, 2006.

[2.30] Y. Fu-Liang, L. Di-Hong, C. Hou-Yu, C. Chang-Yun, L. Sheng-Da, H. Cheng-Chuan, et al., "5nm-gate nanowire FinFET," in VLSI Technology, 2004. Digest of Technical Papers. 2004 Symposium on, 2004, pp. 196-197.

[2.31] C. Jahan, O. Faynot, M. Casse, R. Ritzenthaler, L. Brevard, L. Tosti, et al., "ΩFETs transistors with TiN metal gate and HfO2 down to 10nm," in VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on, 2005, pp. 112-113.

[2.32] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight, et al., "Measurement of Carrier Mobility in Silicon Nanowires," Nano Letters, vol. 8, pp. 1566-1571, 2008/06/01 2008.

[2.33] S. Sung Dae, L. Sung-Young, K. Sung-Min, Y. Eun-Jung, K. Min-Sang, L. Ming, et al., "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk Si wafer, characteristics, and reliability," in Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International, 2005, pp. 717-720.

[2.34] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, et al., "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance," in Electron Devices Meeting, 2006. IEDM '06. International, 2006, pp. 1-4.

[2.35] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. Fuller, et al., "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in Electron Devices Meeting (IEDM), 2009 IEEE International, 2009, pp. 1-4.

[2.36] R. H. Yan, A. Ourmazd, and K. F. Lee, "Scaling the Si MOSFET: from bulk to SOI to bulk," Electron Devices, IEEE Transactions on, vol. 39, pp. 1704-1710, 1992.

[2.37] J. P. Colinge, "Multi-gate SOI MOSFETs," Microelectronic Engineering, vol. 84, pp. 2071-2076, 2007.

[2.38] J. W. Peng, S. J. Lee, G. C. A. Liang, N. Singh, S. Y. Zhu, G. Q. Lo, et al., "Improved carrier injection in gate-all-around Schottky barrier silicon nanowire field-effect transistors," Applied Physics Letters, vol. 93, p. 073503, 2008.

[2.39] K. H. Cho, K. H. Yeo, Y. Y. Yeoh, S. D. Suk, M. Li, J. M. Lee, et al., "Experimental evidence of ballistic transport in cylindrical gate-all-around twin silicon nanowire metal-oxide-semiconductor field-effect transistors," Applied Physics Letters, vol. 92, pp. 052102-3, 2008.

[2.40] C. Keun Hwi, S. Sung Dae, Y. Yun Young, L. Ming, Y. Kyoung Hwan, K. Dong-Won, et al., "Temperature-Dependent Characteristics of Cylindrical Gate-All-Around Twin Silicon Nanowire MOSFETs (TSNWFETs)," Electron Device Letters, IEEE, vol. 28, pp. 1129-1131, 2007.

[2.41] X. Lu and J. Chu, "Lattice thermal conductivity in a silicon nanowire with square cross section," Journal of Applied Physics, vol. 100, pp. 014305-6, 2006.

[2.42] W. Wang, D. Li, M. Tian, Y.-C. Lee, and R. Yang, "Wafer-scale fabrication of silicon nanowire arrays with controllable dimensions," Applied Surface Science, vol. 258, pp. 8649-8655, 2012.

[2.43] W. Sun-Hwak and W. Dongmok, "Template-assisted CVD growth of silicon nanowires on a gram scale," Journal of the Korean Physical Society, vol. 54, pp. 152-6, 2009.

[2.44] M. S. Sander, M. J. Cote, W. Gu, B. M. Kile, and C. P. Tripp, "Template-assisted fabrication of dense, aligned arrays of titania nanotubes with well-controlled dimensions on substrates," Advanced Materials, vol. 16, pp. 2052-2057, Nov 2004.

[2.45] H. J. Fan, W. Lee, R. Hauschild, M. Alexe, G. Le Rhun, R. Scholz, et al., "Template-assisted large-scale ordered arrays of ZnO pillars for optical and piezoelectric applications," Small, vol. 2, pp. 561-568, Apr 2006.

[2.46] G. Z. Cao and D. W. Liu, "Template-based synthesis of nanorod, nanowire, and nanotube arrays," Advances in Colloid and Interface Science, vol. 136, pp. 45-64, Jan 2008.

[2.47] D. Shakthivel and S. Raghavan, "Vapor-liquid-solid growth of Si nanowires: A kinetic analysis," Journal of Applied Physics, vol. 112, pp. 024317-14, 2012.

[2.48] A. Mao, H. T. Ng, N. Pho, M. McNeil, and M. Meyyappan, "Silicon nanowire synthesis by a vapor-liquid-solid approach," Journal of Nanoscience and Nanotechnology, vol. 5, pp. 831-5, 2005.

[2.49] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, "Growth of silicon nanowires via gold/silane vapor--liquid--solid reaction," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 15, pp. 554-557, 1997.

[2.50] W. Tang, S. A. Dayeh, S. T. Picraux, J. Y. Huang, and K.-N. Tu, "Ultrashort channel silicon nanowire transistors with nickel silicide source/drain contacts," Nano Letters, vol. 12, pp. 3979-3985, 2012.

[2.51] U. Herr, B. Riedmueller, M. Haddad, K. Abushgair, M. Madel, J. B. Jakob, et al., "Investigation of Si nanowires from VLS growth," Physica Status Solidi (C) Current Topics in Solid State Physics, vol. 9, pp. 1912-1915, 2012.

[2.52] J. Zhang, L. Zhang, X. Peng, and X. Wang, "Vapor-solid growth route to single-crystalline indium nitride nanowires," Journal of Materials Chemistry, vol. 12, pp. 802-804, 2002.

[2.53] S. V. Thombare, A. F. Marshall, and P. C. McIntyre, "Size effects in vapor-solid-solid Ge nanowire growth with a Ni-based catalyst," Journal of Applied Physics, vol. 112, p. 054325 (6 pp.), 2012.

[2.54] J. Li, Q. Zhang, H. Peng, H. O. Everitt, L. Qin, and J. Liu, "Diameter-controlled vapor-solid epitaxial growth and properties of aligned ZnO nanowire arrays," Journal of Physical Chemistry C, vol. 113, pp. 3950-3954, 2009.

[2.55] C. Y. Wen, M. C. Reuter, J. Tersoff, E. A. Stach, and F. M. Ross, "Structure, growth kinetics, and ledge flow during vapor-solid-solid growth of copper-catalyzed silicon nanowires," Nano Letters, vol. 10, pp. 514-519, 2010.

[2.56] B. Eisenhawer, D. Zhang, R. Clavel, A. Berger, J. Michler, and S. Christiansen, "Growth of Doped Silicon Nanowires by Pulsed Laser Deposition and Their Analysis by Electron Beam Induced Current Imaging," Nanotechnology, vol. 22, p. 075706 (7 pp.), 2011.

[2.57] A. M. Morales and C. M. Lieber, "A Laser Ablation Method for the Synthesis of Crystalline Semiconductor Nanowires," Science, vol. 279, pp. 208-211, January 9, 1998 1998.

[2.58] Y. F. Zhang, Y. H. Tang, N. Wang, D. P. Yu, C. S. Lee, I. Bello, et al., "Silicon nanowires prepared by laser ablation at high temperature," Applied Physics Letters, vol. 72, pp. 1835-1837, 1998.

[2.59] D. P. Yu, C. S. Lee, I. Bello, X. S. Sun, Y. H. Tang, G. W. Zhou, et al., "Synthesis of nano-scale silicon wires by excimer laser ablation at high temperature," Solid State Communications, vol. 105, pp. 403-407, 1998.

[2.60] C. Fournier and F. Favier, "Zn, Ti and Si nanowires by electrodeposition in ionic liquid," Electrochemistry Communications, vol. 13, pp. 1252-1255, 2011.

[2.61] J. Mallet, M. Molinari, F. Martineau, F. Delavoie, P. Fricoteaux, and M. Troyon, "Growth of silicon nanowires of controlled diameters by electrodeposition in ionic liquid at room temperature," Nano Letters, vol. 8, pp. 3468-3474, 2008.

[2.62] F. Martineau, K. Namur, J. Mallet, F. Delavoie, F. Endres, M. Troyon, et al., "Electrodeposition at room temperature of amorphous silicon and germanium nanowires in ionic liquid," IOP Conference Series: Materials Science and Engineering, vol. 6, p. 012012, 2009.

[2.63] D. Xu, Y. Xu, D. Chen, G. Guo, L. Gui, and Y. Tang, "Preparation of CdS single-crystal nanowires by electrochemically induced deposition," Advanced Materials, vol. 12, pp. 520-522, 2000.

[2.64] H.-J. Choi, "Vapor–Liquid–Solid Growth of Semiconductor Nanowires," in Semiconductor Nanostructures for Optoelectronic Devices, G.-C. Yi, Ed., ed: Springer Berlin Heidelberg, 2012.

[2.65] N. Wang, Y. Zhang, and J. Zhu, "Growth of silicon nanowires via nickel/SiCl4 vapor-liquid-solid reaction," Journal of Materials Science Letters vol. Volume 20, pp. 89-91, 2001.

[2.66] F. Qian, Y. Li, S. Gradečak, D. Wang, C. J. Barrelet, and C. M. Lieber, "Gallium Nitride-Based Nanowire Radial Heterostructures for Nanophotonics," Nano Letters, vol. 4, pp. 1975-1979, 2004/10/01 2004.

[2.67] J. Zhou, S. Z. Deng, J. Chen, J. C. She, and N. S. Xu, "Synthesis of crystalline alumina nanowires and nanotrees," Chemical Physics Letters, vol. 365, pp. 505-508, 2002.

[2.68] Y. Wu, R. Fan, and P. Yang, "Block-by-Block Growth of Single-Crystalline Si/SiGe Superlattice Nanowires," Nano Letters, vol. 2, pp. 83-86, 2002/02/01 2002.

[2.69] E. Koren, J. K. Hyun, U. Givan, E. R. Hemesath, L. J. Lauhon, and Y. Rosenwaks, "Obtaining Uniform Dopant Distributions in VLS-Grown Si Nanowires," Nano Letters, vol. 11, pp. 183-187, 2011/01/12 2010.

[2.70] D. E. Perea, E. R. Hemesath, E. J. Schwalbach, J. L. Lensch-Falk, P. W. Voorhees, and L. J. Lauhon, "Direct measurement of dopant distribution in an individual vapour-liquid-solid nanowire," Nat Nano, vol. 4, pp. 315-319, 2009.

[2.71] C. Celle, C. l. Mouchet, E. Rouvière, J.-P. Simonato, D. Mariolle, N. Chevalier, et al., "Controlled in Situ n-Doping of Silicon Nanowires during VLS Growth and Their Characterization by Scanning Spreading Resistance Microscopy," The Journal of Physical Chemistry C, vol. 114, pp. 760-765, 2010/01/21 2009.

[2.72] A. L. Vallett, S. Minassian, P. Kaszuba, S. Datta, J. M. Redwing, and T. S. Mayer, "Fabrication and Characterization of Axially Doped Silicon Nanowire Tunnel Field-Effect Transistors," Nano Letters, vol. 10, pp. 4813-4818, 2010/12/08 2010.

[2.73] C.-Y. Wen, M. C. Reuter, J. Bruley, J. Tersoff, S. Kodambaka, E. A. Stach, et al., "Formation of Compositionally Abrupt Axial Heterojunctions in Silicon-Germanium Nanowires," Science, vol. 326, pp. 1247-1250, November 27, 2009 2009.

[2.74] X. Hui, H. Dogan Sinan, and R. Stéphane, "A versatile atomic force microscope for three-dimensional nanomanipulation and nanoassembly," Nanotechnology, vol. 20, p. 215301, 2009.

[2.75] X. Hui, J. C. Acosta, D. S. Haliyo, and S. Regnier, "Pick-and-place nanomanipulation with three-dimensional manipulation force microscopy," in Intelligent Robots and Systems, 2009. IROS 2009. IEEE/RSJ International Conference on, 2009, pp. 1333-1338.

[2.76] M. Marczak, D. Hourlier, T. Melin, L. Adamowicz, and H. Diesinger, "Frequency dependent rotation and translation of nanowires in liquid environment," Applied Physics Letters, vol. 96, pp. 233502-3, 2010.

[2.77] E. M. Freer, O. Grachev, X. Duan, S. Martin, and D. P. Stumbo, "High-yield self-limiting single-nanowire assembly with dielectrophoresis," Nat Nano, vol. 5, pp. 525-530, 2010.

[2.78] P. A. Smith, C. D. Nordquist, T. N. Jackson, T. S. Mayer, B. R. Martin, J. Mbindyo, et al., "Electric-field assisted assembly and alignment of metallic nanowires," Applied Physics Letters, vol. 77, pp. 1399-1401, Aug 2000.

[2.79] M. Tanase, L. A. Bauer, A. Hultgren, D. M. Silevitch, L. Sun, D. H. Reich, et al., "Magnetic alignment of fluorescent nanowires," Nano Letters, vol. 1, pp. 155-158, Mar 2001.

[2.80] S. Y. Chou, P. R. Krauss, and P. J. Renstrom, "Imprint Lithography with 25-Nanometer Resolution," Science, vol. 272, pp. 85-87, April 5, 1996 1996.

[2.81] M. D. Austin and S. Y. Chou, "Fabrication of 70 nm channel length polymer organic thin-film transistors using nanoimprint lithography," Applied Physics Letters, vol. 81, pp. 4431-4433, 2002.

[2.82] S. Zankovych, T. Hoffmann, J. Seekamp, J. U. Bruch, and C. M. S. Torres, "Nanoimprint lithography: challenges and prospects," Nanotechnology, vol. 12, p. 91, 2001.

[2.83] H. I. Liu, *et. al.*, "Self-limiting oxidation of Si nanowires," Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, vol. 11, p. 2532, 1993.

[2.84] H. I. Liu, D. K. Biegelsen, F. A. Ponce, N. M. Johnson, and R. F. W. Pease, "Self-limiting oxidation for fabricating sub-5 nm silicon nanowires," Applied Physics Letters, vol. 64, pp. 1383-1385, 1994.

[2.85] H. Cui, C. X. Wang, and G. W. Yang, "Origin of Self-Limiting Oxidation of Si Nanowires," Nano Letters, vol. 8, pp. 2731-2737, 2008/09/10 2008.

[2.86] M. Fa-Jun, S. C. Rustagi, G. S. Samudra, Z. Hui, N. Singh, L. Guo-Qiang, et al., "Modeling of Stress-Retarded Thermal Oxidation of Nonplanar Silicon Structures for Realization of Nanoscale Devices," Electron Device Letters, IEEE, vol. 31, pp. 719-721, 2010.

[2.87] W. E. Beadle, J. C. C. Tsai, and R. D. Plummer, Quick reference manual for silicon integrated circuit technology. New York: Wiley, 1985.

[2.88] R. E. and Raider, S. I., “Insitu measurements of SiO(g) production during dry oxidation of crystalline silicon”, Applied Physics Letters, vol. 53, pp. 888-890, 1988.

[2.89] W. Monch, "Barrier heights of real Schottky contacts explained by metal-induced gap states and lateral inhomogeneities," J. Vac. Sci. Technol. B, vol. 17, p. 1867, 1999.

[2.90] W. Mönch, "Role of virtual gap states and defects in metal-semiconductor contacts," Phys. Rev. Lett., vol. 58, no. 12, pp. 1260–1263, Mar. 23, 1987.

[2.91] J. Tersoff, "Schottky barrier heights and the continuum of gap states," Physical Review Letters, vol. 52, p. 465, 1984.

[2.92] R. T. Tung, "Chemical bonding and Fermi level pinning at metal-semiconductor interfaces," Phys. Rev. Lett., vol. 84, pp. 6078 - 6081, Jun. 2000.

[2.93] R. T. Tung, "Recent advances in Schottky barrier concepts," Mat. Sci. Eng. Rep., vol. 35, pp. 1-138, Nov. 2001.

[2.94] R. T. Tung, "Schottky-Barrier Formation at Single-Crystal Metal-Semiconductor Interfaces," *Physical Review Letters*, vol. 52, pp. 461-464, 1984.

[2.95] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Transactions on Electron Devices*, vol. 53, pp. 1048-1058, 2006.

[2.96] V. L. Rideout and C. R. Crowell, "Effects of image force and tunneling on current transport in metal-semiconductor (Schottky barrier) contacts," Solid-State Electronics, vol. 13, pp. 993-1009, 1969.

[2.97] G. P. Lousberg et al., "Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs," IEEE Elec. Dev. Lett., vol. 28, p. 123, 2007.

[2.98] M. Jang et al., "Characteristics of erbium-silicided n-type Schottky-barrier tunnel transistors,” " Appl. Phys. Lett., vol. 83, pp. 2611–2613, 2003.

[2.99] M. Jang et al., "Formation of erbium-silicide as source and drain for decananometer-scale Schottky barrier metal-oxide-semiconductor field-effect transistors," Materials Science and Engineering B, vol. 114-115, pp. 51-55, 2004.

[2.100] Z. Qiu et al., "A Comparative Study of Two Different Schemes to Dopant Segregation at NiSi/Si and PtSi/Si Interfaces for Schottky Barrier Height Lowering," IEEE Trans. Elec. Dev., vol. 55, p. 396, 2008

[2.101] J. P. Snyder et al., "Experimental investigation of a PtSi source and drain field-emission transistor," Appl. Phys. Lett., vol. 67, pp. 1420–1422, 1995.

[2.102] G. P. Lousberg et al., "Schottky-Barrier Height Lowering by an Increase of the Substrate Doping in PtSi Schottky Barrier Source/Drain FETs," IEEE Elec. Dev. Lett., vol. 28, p. 123, 2007.

[2.103] S. Zhu et al., "N-type Schottky barrier source/drain MOSFET using ytterbium silicide," IEEE Electron Dev. Lett., vol. 25, pp. 565-567, 2004.

[2.104] G. Larrieu, E. Dubois, X. Wallart, J. Katcki, “Kinetics, stoichiometry, morphology, and current drive capabilities of Ir-based silicides”, Journal of Applied Physics, vol. 102, pp. 094504, 2007.

[2.105] A. Kaneko et al., "High-Performance FinFET with Dopant-Segregated Schottky Source/Drain," IEDM Tech. Dig., Dec. 2006.

[2.106] A. Kinoshita et al., "Solution for High-Performance Schottky-Source/Drain MOSFETs: Schottky Barrier Height Engineering with Dopant Segregation Technique," VLSI Tech. Dig., pp. 168-169, 2004.

[2.107] Q. T. Zhao et al., "Tuning of Silicide Schottky Barrier Heights by Segregation of Sulfur Atoms," Proc. IEEE, pp. 456-459, 2004.

[2.108] H. S. Wong et al., "Schottky Barrier Height Modulation for Nickel Silicide on n-Si(100) using Antimony (Sb) Segregation," Ext. Abstr. SSDM, pp. 366-367, 2007.

[2.109] C. Zaring et al., "Boron redistribution during formation of nickel silicides," applied surface science, vol. 53, pp. 147-152, 1991.

[2.110] I. Ohdomari et al., "Low-temperature redistribution of As in Si during Ni silicide formation," J. Appl. Phys., vol. 56, p. 2725, 1984.

[2.111] B.-Y. Tsui and C.-P. Lin, "Process and Characteristics of Modified Schottky Barrier (MSB) p-Channel FinFETs," IEEE Trans. Elec. Dev., vol. 52, p. 2455, 2005.

[2.112] Z. Shi-Li and M. Östling, Crit. Rev. Sol. State Mat. Sci., vol. 28, 1 2003.

[2.113] D.-X. Xu et al., "Material aspects of nickel silicide for ULSI applications," Thin Solid Films, vol. 326, pp. 143-150, 1998.

[2.114] D.-X. Xu et al., "Process windows of nickel and platinum silicides in deep sub-micron regime," Silicide Thin Films - Fabrication, Properties, and Applications. Symposium, pp. 59-64, 1996.

[2.115] Q. Z. Hong et al., "Thermal stability of silicide on polycrystalline Si," Thin Solid Films, vol. 253, p. 479, 1994.

[2.116] S. Nygren et al., "Morphological instabilities of nickel and cobalt silicides on silicon," Appl. Surf. Sci. , vol. 53, p. 87, 1991.

[2.117] K. Maex and M. Van Rossum, "Properties of Metal Silicides," ed: Institution of Engineering and Technology, p. 277.

[2.118] F. M. d'Heurle, "Nucleation of a new phase from the interaction of two adjacent phases: some silicides," J. Mater. Res. , vol. 3, p. 167, 1988.

CHAPTER 3
DEVICE DESIGN AND FABRICATION PROCESS FLOW[a]

3.1 Introduction

The continuous and aggressive scaling of MOSFETs for higher integration to realize performance improvements in large-scale integrated circuits have led to the aggravation of Short Channel Effects (SCEs), such as Drain-Induced Barrier Lowering (DIBL), sub-threshold swing (SS) and Threshold Voltage (V_T) roll-off, which instigated an increase in the off-state leakage current (I_{off}).

One solution to reduce the SCEs in scaled MOSFETs is to boost the electrostatic control of the gate electrode over the channel by increasing the number of gates surrounding the channel. Three-dimensional structures including FinFETs, multiple gate FETs and nanowire (NW) FETs are proposed to achieve this objective. Among them, NWFET is the most promising candidate owing to the ease of fabricating Gate-All-Around (GAA) architecture around it and the best electrostatic control.

In reported literature, many successful cases whereby LNW-GAA-MOSFETs [3.1-3.3] have shown to mitigate the SCE challenges. However, LNW-GAA-MOSFETs suffer from two fundamental issues.

[a] Reproduced in part from L. Weijie, P. Kin Leong, W. Xinpeng, L. Xiang, C. Zhixian, N. Singh, *et al.*,"Vertical Silicon Nanowire Diode with Nickel Silicide Induced Dopant Segregation," *Japanese Journal of Applied Physics*, vol. 51, p. 11PE08, 2012.
Copyright (2016) with permissions from The Japan Society of Applied Physics

The first issue is "parasitic gate" effect.. A trail of poly-Si underneath the S/D extension is left behind after the gate etching process, commonly known as the poly-Si stringer [3.4]. The presence of poly-Si stringer boosts the parasitic leakage paths and in turn, higher leakage current. An illustration is provided in Figure 3.1 to better depict the "parasitic gate" effect.

The second issue is estate area per wafer and limited capability of lithography optics. With identical gate orientation as planar devices, LNW-GAA-MOSFETs will need to scale down its gate length to accommodate more devices per unit area and this leads to the same scaling issues faced by the planar counterparts.

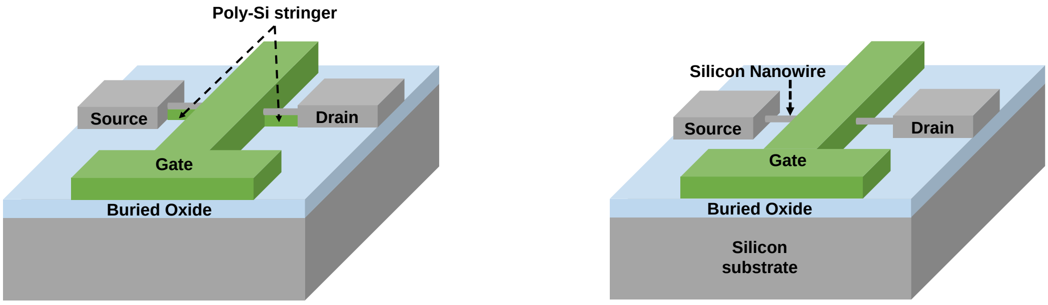


Figure 3.1 Demonstration of LNW-GAA-MOSFET with (left) and without (right) trail of poly-Si stringer underneath S/D extension [3.4].

VNW-GAA-MOSFETs are able to alleviate the issues faced by LNW-GAA-MOSFETs while harnessing the benefits of 1D SiNWs. Essentially, VNWs are identical to LNWs in every aspect, except the channel and gate regions are vertically-oriented. Figure 3.2 (a) [3.5] shows a schematic of VNW-GAA-MOSFET and Figure 3.2 (b) shows colored cross-sectional Transmission Electron Microscope (TEM) image of VNW-GAA-MOSFET [3.6].

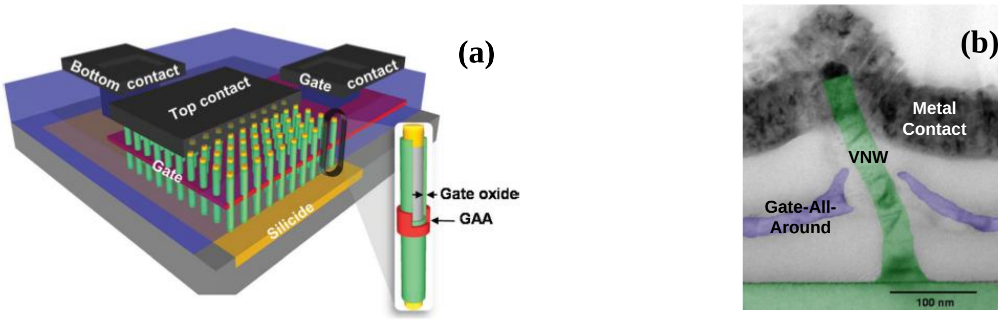


Figure 3.2 (a) Illustration of VNW-GAA-MOSFET array connected to metal contacts. Inset of (a) shows the zoomed-in cross-sectional view of a nanowire with gate stack composed of gate oxide and gate surrounding the nanowire [3.5]. (b) Transmission electron micrograph of VNW-GAA-MOSFET [3.6].

In this chapter, the feasibility of fabricating VNWs on Si substrate using standard CMOS processes is studied and the fabrication of devices such as Schottky Barrier (SB), Dopant-Segregated Schottky Barrier (DSSB) VNW diodes and transistors using VNW as the fundamental platform are discussed in detail.

Section 3.2 details every fabrication step of VNW using standard CMOS processes with tilted Scanning Electron Microscope (SEM) images. Section 3.3 discusses the fabrication of VNW SB and DSSB diodes. Section 3.4 examines the fabrication of GAA-VNW SB and DSSB transistors. Lastly, Section 3.5 provides a short summary of the essential concepts discussed.

3.2 Fabrication of Vertical Silicon Nanowire using standard CMOS processes

VNWs are fabricated on 200mm p-type (~ 10^{15}cm^{-3}) Si (100) wafers using fully CMOS-compatible processes. The main reason to use CMOS-compatible processes is for ease of integration into the industry mainstream in the future.

3.2.1 Details of fabrication process

The cross-section schematics of the fabrication process can be found in Figure 3.3. Firstly, nitride (SiN) hard-mask layer (~1000Å) was deposited using Low Pressure Chemical Vapour Deposition (LPCVD) furnace method onto the Si wafers. Subsequently, photoresist (PR) nanodots with diameters from 170nm to 450nm were patterned using 248nm KrF lithography Nikon stepper. The patterned PR nanodots were then trimmed down to between 60nm - 300nm via Deep Reactive Ion Etch (DRIE) process step in STS-DRIE CMOS etcher. Subsequently, the PR nanodots were transferred to the hard-mask by etching away exposed nitride surfaces in TEL-RIE etcher with over-etch (OE). This OE step is critical because it ensures that there is no nitride residue remaining on the Si wafer surface which may serve as micro-masks in the later process steps.

Following the hard-mask layer etch, the Si wafers were subjected to DRIE process again whereby 300nm of exposed Si was etched away to form thick vertical Si pillars. Figure 3.4 (a) shows the tilted Scanning Electron Microscope (SEM) image of a single vertical Si pillar taken from center of the wafer and Figure 3.4 (b) shows the tilted SEM image of a single vertical Si pillar taken from the wafer edge. From Figures 3.4 (a) and (b), it is observed that regardless of the wafer measurement location, there is negligible difference, in terms of pillar height (~ 340nm) or diameter (~65nm). At the same time, we observe that the shape of the vertical pillar is not perfectly straight but is slightly tapered near the bottom of the pillar as shown in Figure 3.4 (c). This is due to the Si etching process that inherently produced a tapered pillar profile.

In the DRIE process, deep vertical Si etch was achieved at a fast rate via alternating passivation and etching steps, also known as the Bosch process. Firstly, C_4F_8-based plasma was used to produce a conformal layer of polymer, with a thickness of a few monolayers, which serves as a protecting layer across all surfaces exposed to the plasma. Subsequently, the gas switched to SF_6 to create a plasma chemistry that etches Si anistropically. Lastly, with the use of DC biasing to the plate, the plasma ions bombard the exposed Si surface parallel to the surface of the wafer at a much higher rate. This etching was done by fluorine-based species while the polymer protects the pillar sidewall from etching.

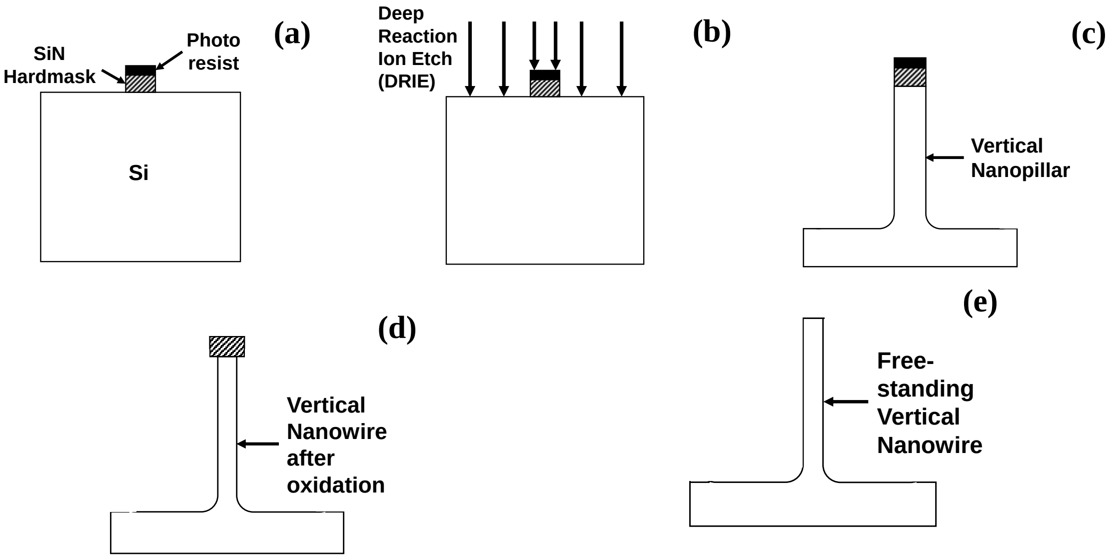


Figure 3.3 Cross-sectional schematics showing (a) nanodots formed on blanket Si wafers using 246nm KrF lithography and resist trim, (c) vertical Si pillar formed after DRIE process in (b) with a film stack consisting of photoresist and SiN as hardmask, (d) vertical SiNW after dry thermal oxidation of Si pillar in (c) and oxide release, (e) vertical SiNW without hardmask.

After the vertical Si pillars ~ 300nm in height was achieved, the PR was removed using a combination of wet process steps using diluted hydrofluoric acid (DHF) (HF: H_2O) with a ratio of (1:100) and Sulfuric-Peroxide Mixture (SPM) (H_2SO_4: H_2O_2) with a ratio of (4: 1). Firstly, the wafers were immersed in DHF for 10 sec to soften the PR for easy removal. Subsequently, the wafers were immersed in SPM for 10 mins to remove the PR and any PR residue on the wafers. This is followed by a 10 cycle de-ionized (DI) water rinse and 100 rotations per minute (RPM) spin-dry with N_2 flow to dry the wafers.

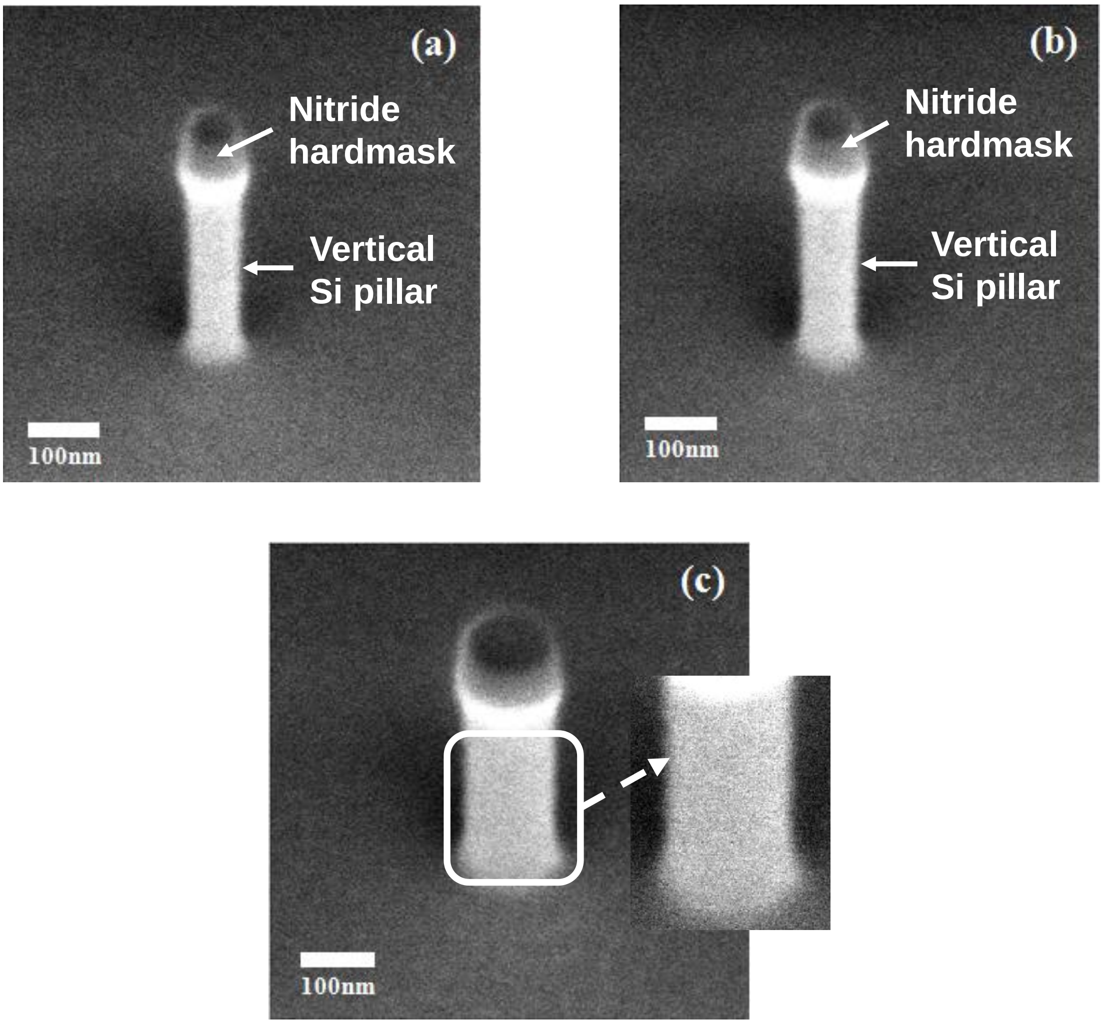


Figure 3.4 Tilted Scanning Electron Microscopy (SEM) images of vertical Si pillars, before thermal oxidation, located at the (a) center and (b) edge of the wafer. Both pillars exhibited heights of ~ 340nm and ~ 342nm and widths of ~ 64nm and ~ 66nm, respectively. (c) shows the SEM image of a fat vertical Si pillar with obvious tapering at the bottom of the pillar (Inset shows the zoom-in image with dotted white lines to serve as guide for the eye).

To obtain vertical Si nanowires (VSiNWs) of the desired size, self-limited oxidation is required to reduce the diameter of the vertical Si pillars. Before loading the Si wafers into the thermal oxidation furnace, the wafers were immersed into SC1 ($NHOH_4$: H_2O_2: H_2O) solution with a ratio of (1: 1: 5) for 5 mins at 750^{o}C. This was followed by a 10 cycle de-ionized (DI) water rinse. This step is to remove organic residue. Subsequently, the wafers were immersed in DHF with a ratio of (1: 200) for 2 mins, followed by a 10 cycle DI water rinse. This step is to remove any native oxide found on the Si surface. Lastly, the wafers were dried by N_2 flow and loaded immediately into the thermal oxidation furnace.

Dry thermal oxidation process, with 10% O_2 and 90% N_2, was used to oxidize the Si nanopillars. DHF solution with a ratio (1: 25) was then used to release the VSiNWs formed. Following that, the wafers went through a 10 cycle Di water rinse and 100 RPM low spin-dry. SEM images of VSiNWs released after the thermal oxidation process are shown in Figure 3.5. VSiNWs with diameter of 20 nm to 200 nm were achieved. After VSiNW release, the SiN hard-mask was removed via hot H_3PO_4 solution wet etch. Figure 3.6 depicts the flow-chart detailing the whole fabrication process.

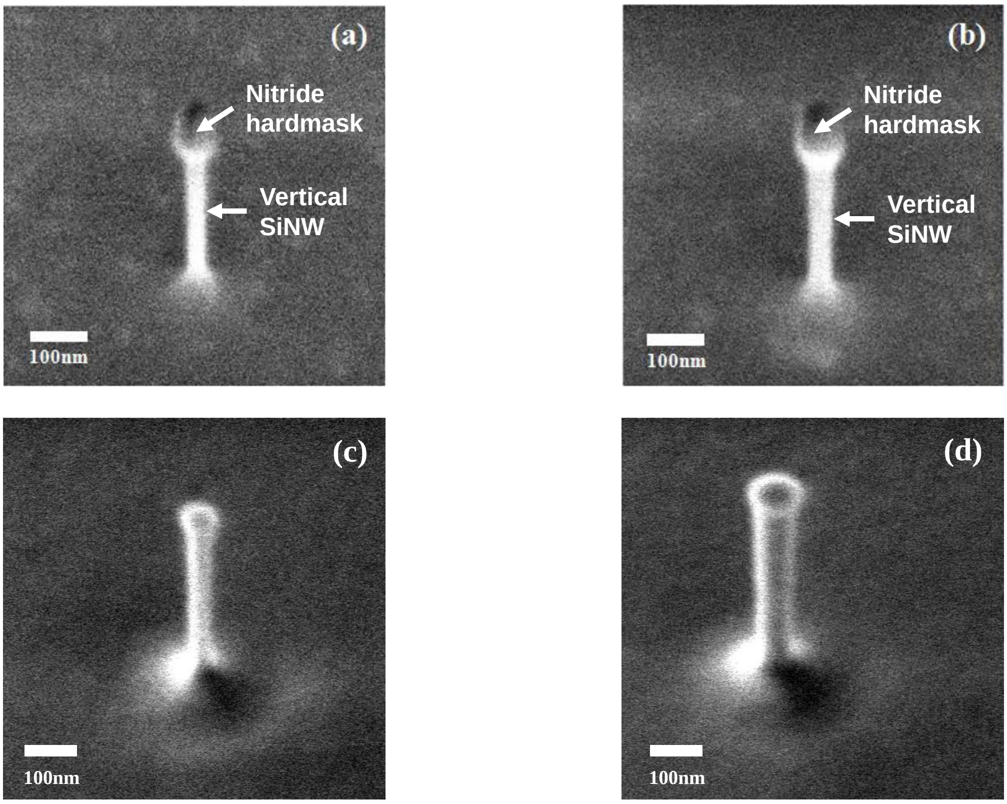


Figure 3.5 (a) and (b) shows the SEM images of vertical SiNWs (VSiNWs) after the Si pillars, shown in Figure 3.4, have undergone thermal oxidation to reduce the pillar diameter. The VSiNW diameter in (a) is ~ 30nm and (b) ~ 34nm while the VSiNW height remains ~ 340nm. Figure 3.5 (c) and (d) shows free-standing VSiNWs after undergoing nitride hard-mask removal.

3.2.2 Summary of whole fabrication process

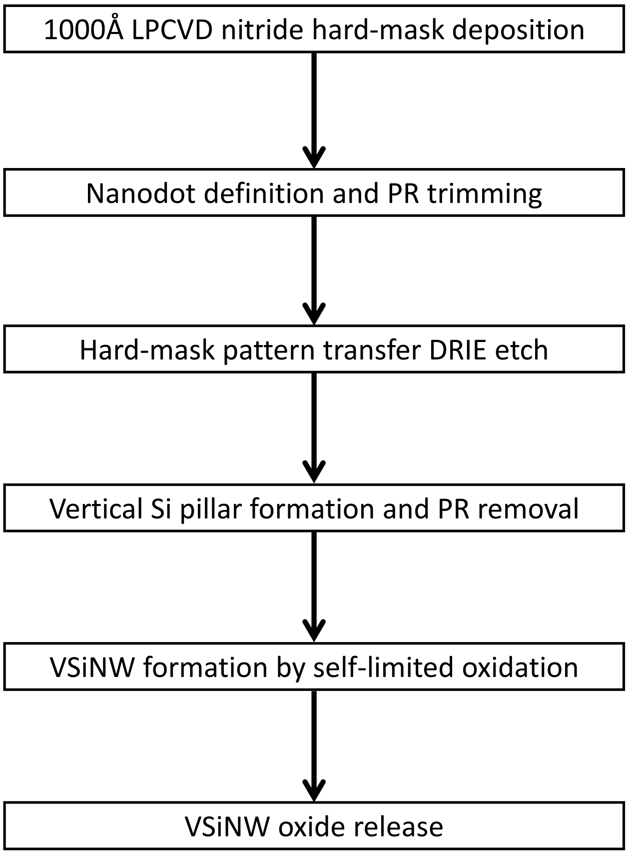


Figure 3.6 Process flow for fabricating Vertical Silicon Nanowire via CMOS-compatible processes

3.3 Fabrication of VSiNW Schottky Barrier and VSiNW Dopant Segregated Schottky Barrier diode

The diodes studied in this work made use of VSiNW as the starting infrastructure and are fabricated on 200mm Si substrates. There were 2 splits of the diode of interest, namely, VSiNW Schottky (VSiNWSB) diode, whereby only the top portion of VSiNW is metallized with nickel silicide and VSiNW Dopant Segregated Schottky (VSiNWDSSB) diode, whereby a thin layer of implanted dopants segregates at nickel silicide/silicon interface within the top portion of VSiNW.

3.3.1 Fabrication details of VSiNW-SB diode

After obtaining the VSiNWs described in Section 3.2, non-conformal high density plasma (HDP) oxide deposition followed by RIE oxide etch back was done to obtain a 40 nm oxide spacer around the VSiNWs (Figure 3.7d). The substrate was subsequently doped with BF_2 (10 keV/ 4 x 10^{15} cm^{-2}/ 0^o tilt; activation 1000^0C/ 5s) to achieve an Ohmic contact to the substrate. HDP oxide deposition followed by chemical and mechanical polishing (CMP) and DHF etch-back were used to expose only the VSiNW tip for metallization.

<u>Silicide formation</u>

To silicidize the top portion of VSiNW, 300Å Ni was deposited followed by rapid thermal annealing (RTA) in nitrogen ambient. During the RTA process, Ni will intrude into the VSiNW and thus silicidizing only the top portion of ViSNW to form Ni_xSi_y (Figure 3.7f). Finally, aluminum metal contacts were formed and sintering (10% H_2: 90% N_2) was performed at 420^0C for 30 min (Figure 3.7g).

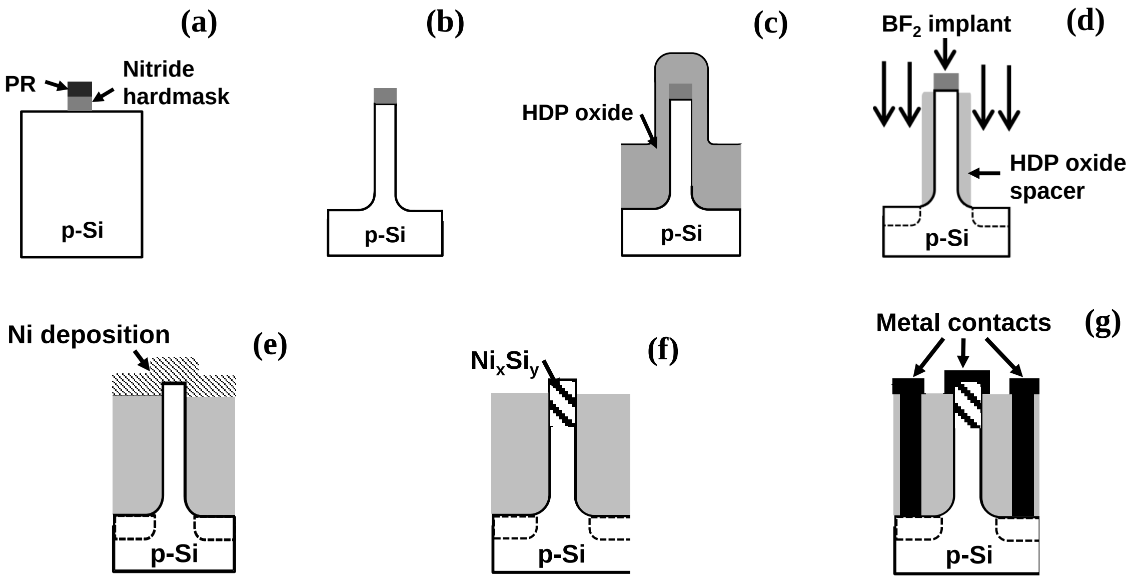


Figure 3.7 Schematics of fabrication process for VSiNWSB diodes: (a) Formation of SiN hardmask on p-Si substrate for subsequent etching of vertical Si pillar and formation of VSiNW upon thermal oxidation in (b). (d) Formation of substrate Ohmic contacts via implantation with VSiNW remaining intrinsic due to the presence of HDP oxide spacer formed in (c). (e) Deposition of Ni layer to form Ni_xSi_y in (f) using appropriate metallization conditions such that only the top VSiNW portion becomes silicided. Finally, Al contacts formation in (g) for device electrical probing.

3.3.2 Vertical Silicon Nanowire Dopant Segregated Schottky Barrier diode (VSiNW-DSSB) splits

In the study of VSiNW-DSSB diodes, p- and n-substrates were used. To achieve n-substrate, 50 Å of oxide was grown via dry thermal oxidation on the p-type Si wafers in Section 3.2.1 to serve as screening oxide before the wafers were subjected to phosphorus (P) implantation with implant and annealing conditions simulated using Synopsys TSUPREM4 simulation software.

The P implantation was simulated using 170keV / 7° tilt / 0 rotation and 2 different doses, 5×10^{12} cm^{-2} and 1×10^{13} cm^{-2}. Different implant dose was used to study the effect of substrate doping on ideality factor and Schottky Barrier Height (SBH) of the diodes. After the implant process, the annealing condition was simulated using 1100 ^{0}C for 300 mins.

From the simulation results shown in Figures 3.9 and 3.10, the annealed wafers were successfully n-doped with uniform concentration of 4 x 10^{16} cm^{-3} and 1 x 10^{17} cm^{-3}.

After getting the required starting p- and n-substrates, VSiNW diodes were fabricated on the wafers as described in Section 3.3.1. To achieve Ohmic contact, the n-substrates were doped with Arsenic (10keV / 4 x 10^{15} cm^{-2} / 0^{o} tilt / 0 rotation; activation 1000^{o}C for 5 s) while the p-substrates were doped with BF_2 (10 KeV/ 4 x 10^{15} cm-2/ 0^{o} tilt; activation 1000^{o}C/ 5s).

VSiNW tips were then exposed through HDP oxide deposition, CMP and chemical oxide etch back process steps. An additional implant step was inserted before the nickel silicidation process to segregate the implanted dopants at the silicide/silicon interface during the silicide formation. BF_2 (four orthogonal implants: 10keV / 1 x 10^{15} cm^{-2} per rotation / 7^{o} tilt) was implanted into the n-doped VSiNWs and Arsenic (four orthogonal implants: 10keV / 1 x 10^{15} cm^{-2} per rotation / 7^{o} tilt) was implanted into the p-doped VSiNWs.

Subsequently, Al contacts were formed for device electrical probing. The fabrication process steps for VSiNW-DSSB diodes are depicted in Figure 3.8.

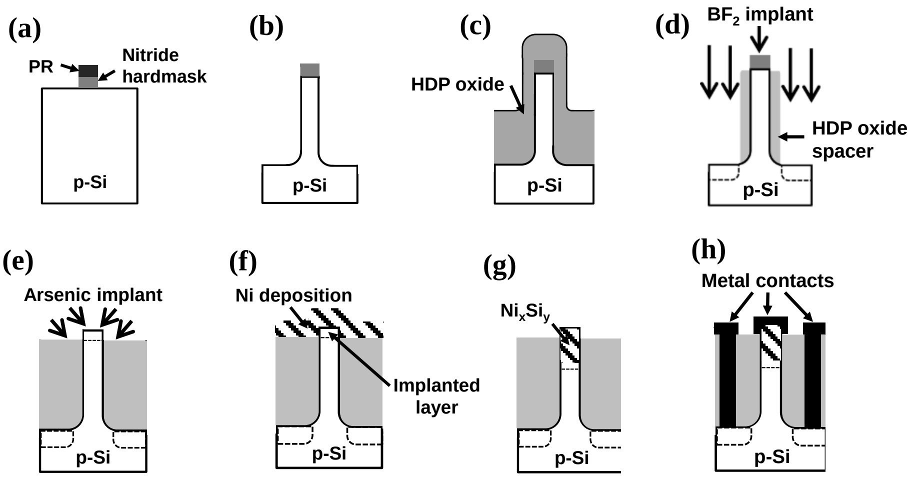


Figure 3.8 Cross-sectional schematics of device: (a) Nitride hard-mask definition on p-substrate. (b) Nanowire etch using DRIE and thermal oxidation. (c) Oxide spacer formation. (d) Vertical BF_2 implant for bottom contact. (e) Arsenic implant to exposed SiNW top for dopant segregation. (f) 30 nm Ni layer deposition. (g) Ni_xSi_y formation using RTA anneal. (h) Aluminium contact formation.

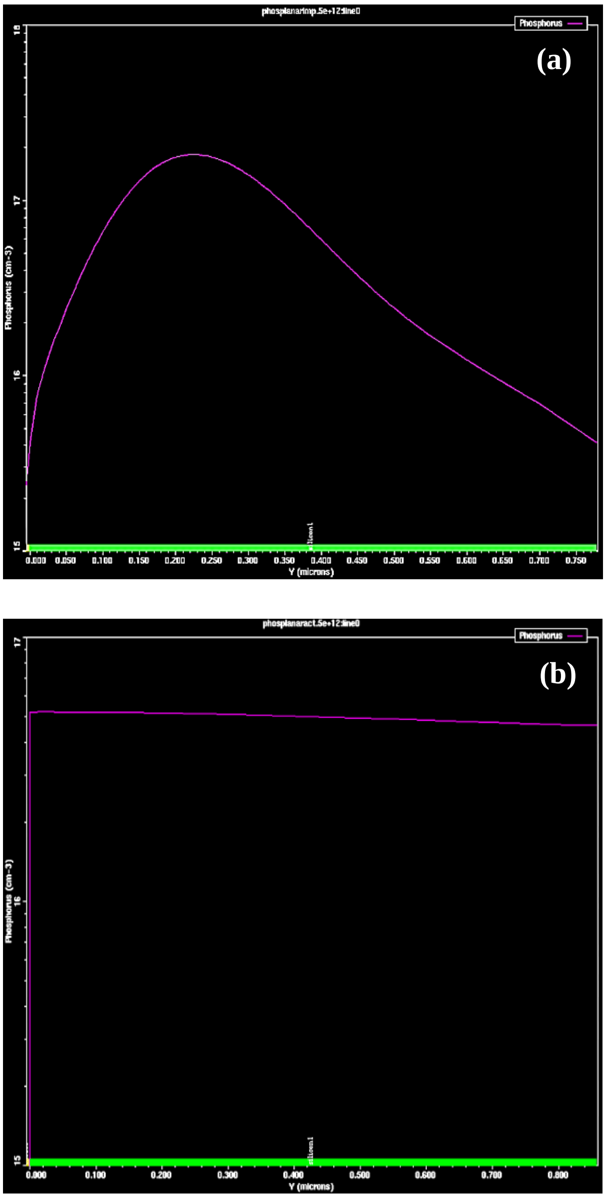


Figure 3.9 TCAD simulation results of dopant distribution profiles for (a) as-implanted (Phosphorus/ 170keV/ 5 x 10^{12} cm^{-2}/ 7º tilt/ 0º rot) and (b) after thermal annealing (1100ºC, 300 mins).

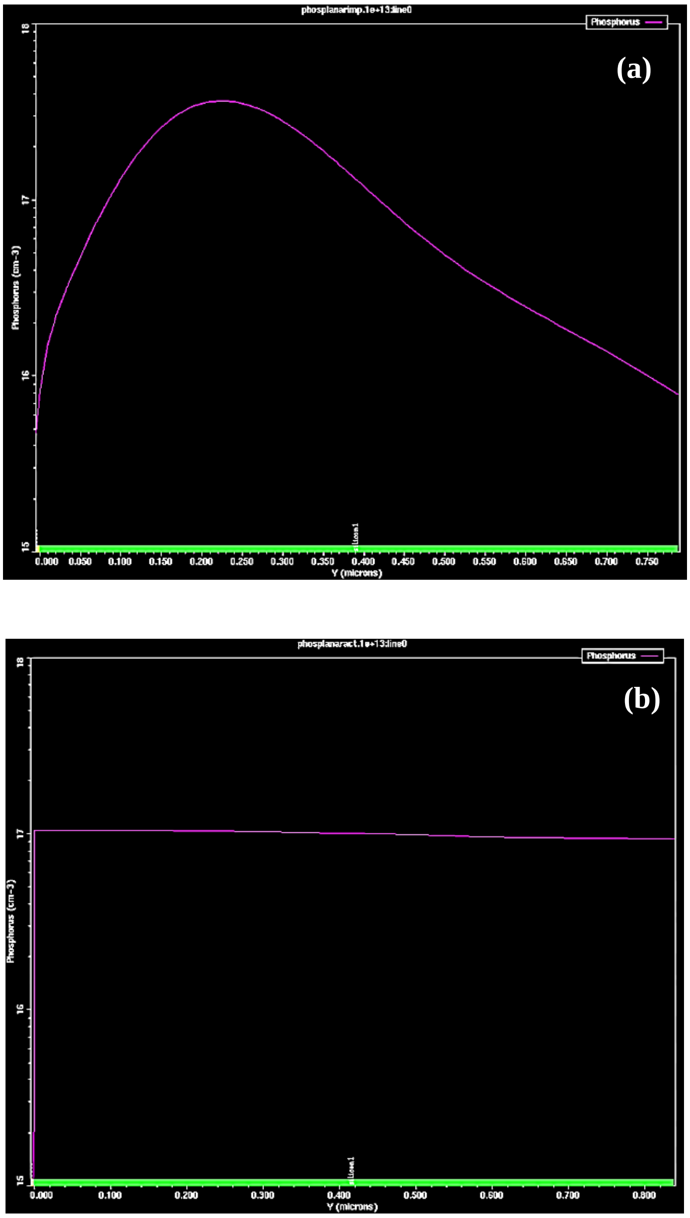


Figure 3.10 TCAD simulation results of dopant distribution profiles for (a) as-implanted (Phosphorus/ 170keV/ 1 x 10^{13} cm^{-2}/ 7^{o} tilt/ 0^{o} rot) and (b) after thermal anneal (1100^{o}C, 300 mins).

3.3.3 Summary of VSiNW diode splits

A summary of the different diode fabrication processes is depicted in Figure 3.9 for easy comparison.

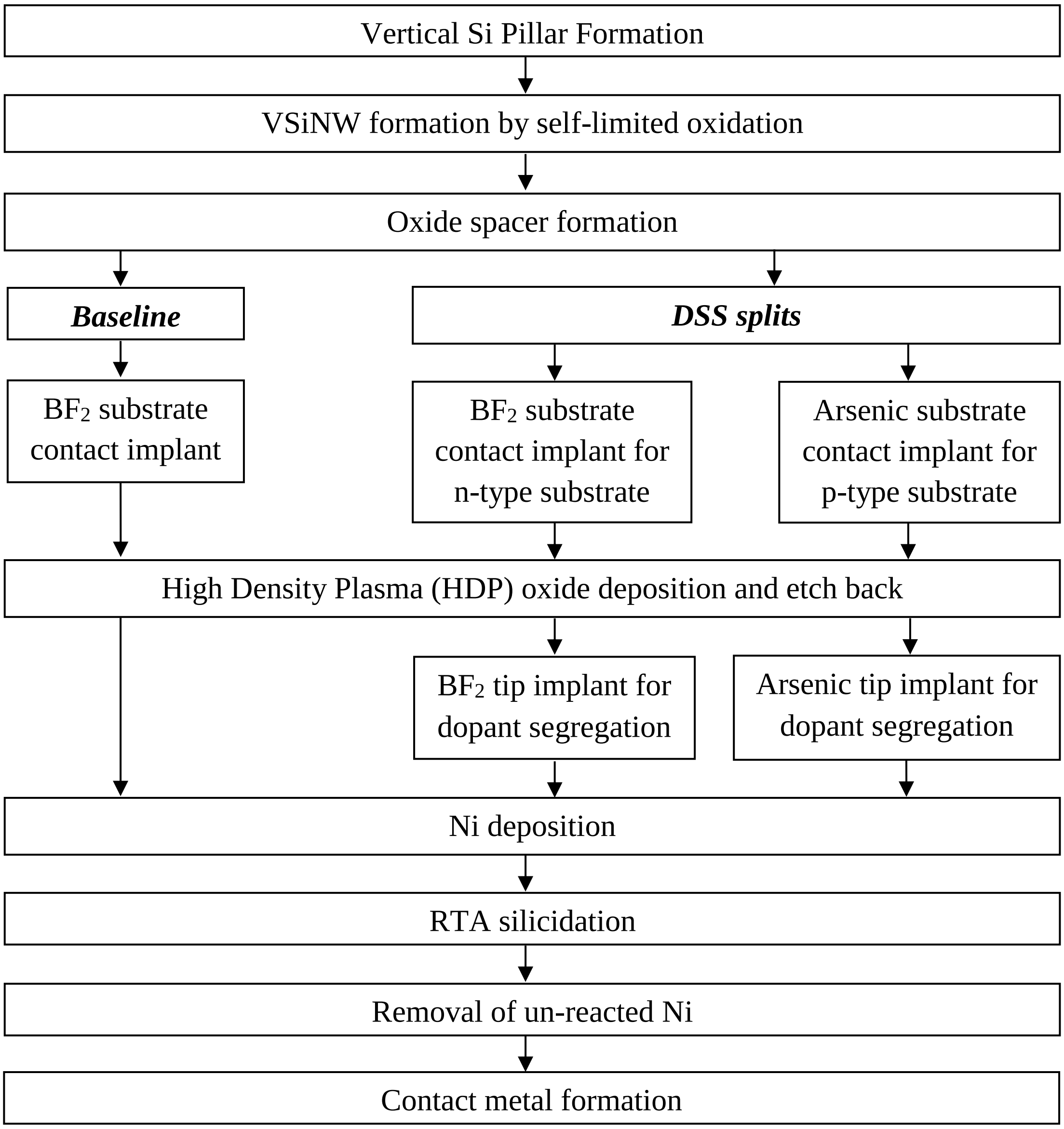


Figure 3.11 Process flow for VSiNW-SB and -DSSB diodes

3.4 Gate-All-Around Vertical Silicon Nanowire (GAA-VSiNW) Transistor Fabrication

This section gives an overview of the CMOS processing of GAA-VSiNW *p*- and *n*-MOS transistors used in this work. There are three experimental splits, namely, baseline MOSFET with poly-gate and doped source/ drain (S/D), Fully Silicided (FUSI) MOSFET with tuned-FUSI gate and Schottky S/D, and FUSI MOSFET with tuned-FUSI gate and DSS S/D. Figure 3.12 shows the fabrication schematics of GAA p- and n-MOS transistors with highly doped S/D and poly-Si gate.

3.4.1 Baseline GAA-VSiNW MOSFET fabrication flow

Freestanding VSiNWs were used as the basic infrastructure to fabricate the GAA p- and n-MOS transistors. The fabrication of freestanding VSiNWs was explicitly discussed in Section 3.2.1 under Chapter 3. After achieving the VSiNWs, screening oxide ~ 100Å was deposited using Applied Materials Plasma Enhanced Chemical Vapour Deposition (AMAT-PECVD) system followed by arsenic implant (30keV / 5 x 10^{15} cm^{-2} / 0^o tilt / 0 rotation) for n-MOS and BF_2 implant (15keV / 5 x 10^{15} cm^{-2} / 0^o tilt / 0 rotation) for p-MOS. The wafers were then annealed at 1100°C for 10 sec in N_2 environment using Rapid Thermal Annealing (RTA) process. Now, the substrate becomes highly-doped and will serve as the source region of the MOSFET.

Gate stack formation

After the RTA process, bottom isolation oxide (~800Å), using oxide PECVD deposition and DHF etch back, was formed to isolate the gate and substrate regions. Subsequently, the remaining nitride hard-mask on top of the VSiNWs were removed in H_3PO_4 (180 °C) solution before the dry thermal growth of ~45Å gate oxide. Following the growth of gate oxide, 500Å of α-Si layer was deposited using LPCVD furnace process and this was succeeded with Phosphorus and BF_2 implants (5keV / 1 x 10^{15} cm^{-2} / 20^o tilt/ 4 rotations) and annealed at 950^oC for 10 sec to achieve poly-Si gates for n-and p-MOS, respectively.

Gate Length definition

To achieve gate length of 1000Å, gate isolation oxide formation and poly-Si RIE etch was used. Firstly, ~ 950Å of low temperature high density plasma (HDP) oxide was formed on top of the poly-Si via HDP-PECVD deposition and wet chemistry etch-back. Subsequently, the exposed poly-Si was removed using RIE etch and nitride spacer (~500Å) was formed around the sidewall of the exposed poly-Si. The purpose of the nitride spacer will be explained later in Section 3.4.2. Now, only the VSiNW top surface is exposed.

Drain formation

The exposed VSiNW top surface was heavily doped with vertical Phosphorus or BF_2 implants (5keV / 4 x 10^{15} cm^{-2} / 0^o tilt/ 0^o rotation) for n- and p-MOSFET, respectively. The wafers were then RTA-annealed 1050^oC for 5 sec to activate the dopants. The gate isolation oxide was then removed by immersing the wafers in DHF (1: 100) solution. Following that, 248nm KrF lithography and RIE etch were used to pattern the gate. The VSiNW tip will be the drain region of the MOSFET.

Contact formation

Quadruple layer, consisting of nitride, PECVD oxide, HDP oxide and PECVD oxide, was deposited onto the wafers and CMP (Chemical Mechanical Polishing) to flatten the surface. Following that, contact holes were patterned and etched and metallization was done to complete the fabrication process.

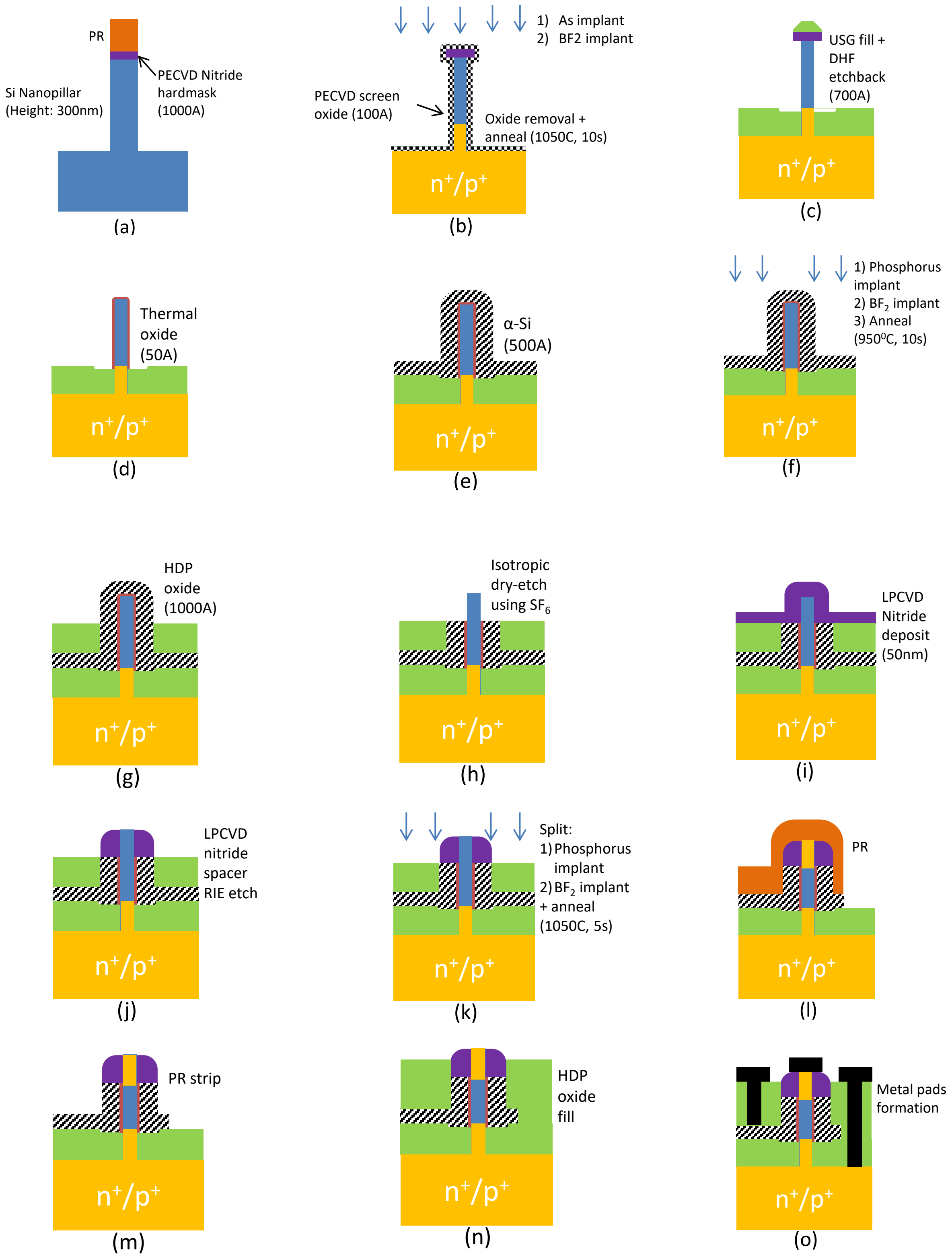


Figure 3.12 Fabrication schematics of GAA p- and n-MOS transistors with highly-doped S/D and poly-Si gate

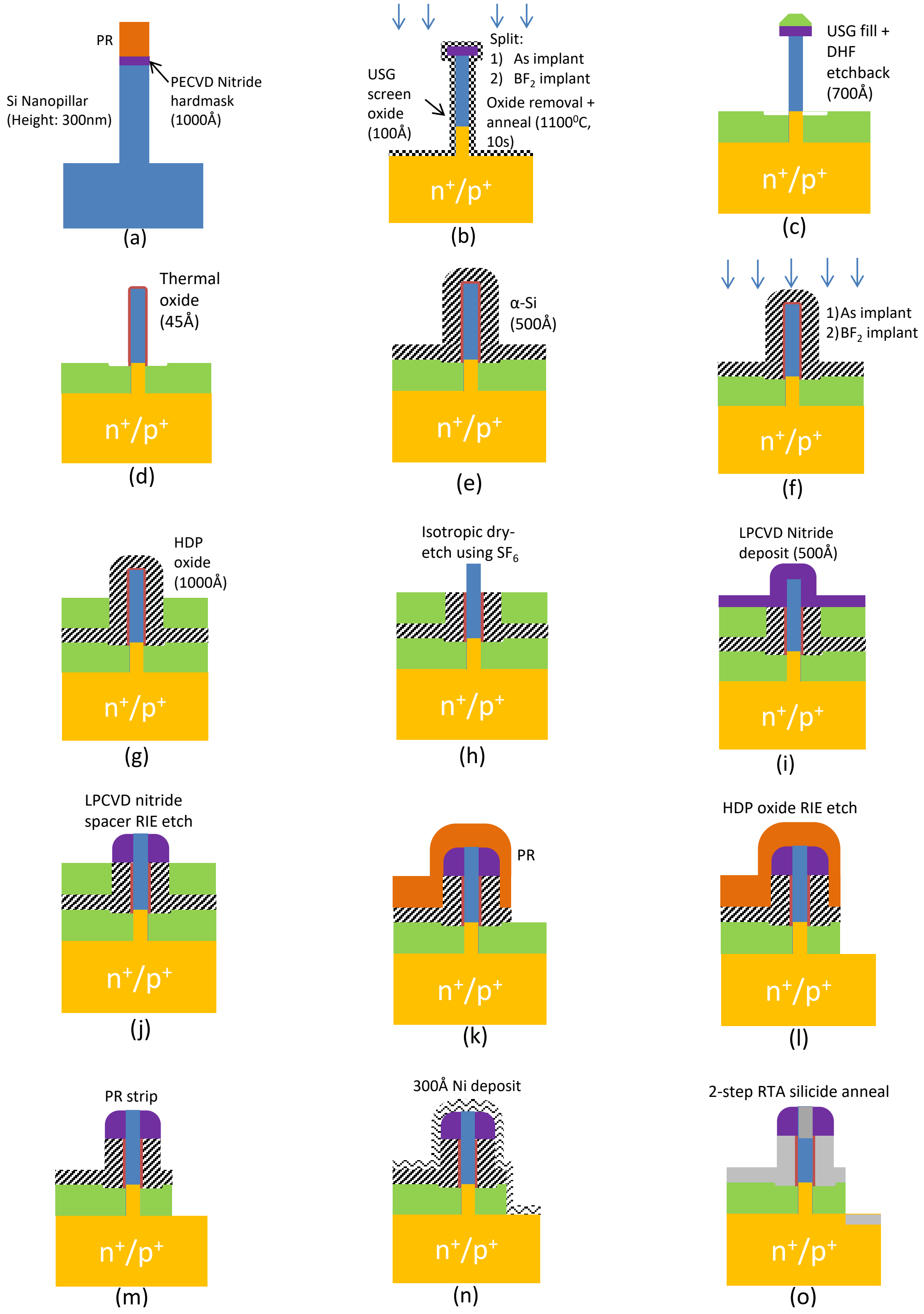
3.4.2 Tuned FUSI GAA-VSiNW MOSFET Schottky split

In this section, the process flow for GAA-VSiNW MOSFET with tuned FUSI gate and Schottky S/D is discussed. Figure 3.13 illustrates the detailed fabrication schematics.

After defining the gate length discussed in Section 3.4.1, the gate isolation oxide was removed by immersing the wafers into DHF (1:100) solution. Do note that no implant step was performed. Gate patterning was done using 248nm KrF lithography and RIE etch. During the RIE etch, exposed bottom isolation oxide was also removed with photoresist (PR) serving as the etching hard-mask.

<u>Schottky S/D and FUSI gate formation</u>

After PR removal, 300Å Ni was deposited using Physical Vapour Deposition (PVD) method. The wafers were then sent for 2-step RTA silicidation to form the desired Ni silicide phase, as discussed in Section 3.5. By doing so, the VSiNW tip (Drain), bottom (Source) and poly-Si (Gate) layer will be silicided together. Since nickel silicide cannot be formed over silicon oxide or nitride layers, the nitride spacer prevents the drain and gate regions being electrically connected. Following which, the quadruple layer of nitride, PECVD oxide, HDP oxide and PECVD oxide was deposited and CMP was performed before contact holes etch and metallization.


PR
Si Nanopillar
(Height: 300nm)
PECVD Nitride
hardmask
(1000Å)
(a)
USG
screen
oxide
(100Å)
Split:
1) As implant
2) BF$_2$ implant
Oxide removal +
anneal (1100^{0}C,
10s)
n$^+$/p$^+$
(b)
USG fill +
DHF
etchback
(700Å)
n$^+$/p$^+$
(c)
Thermal
oxide
(45Å)
n$^+$/p$^+$
(d)
α-Si
(500Å)
n$^+$/p$^+$
(e)
1)As implant
2)BF$_2$ implant
n$^+$/p$^+$
(f)
HDP
oxide
(1000Å)
n$^+$/p$^+$
(g)
Isotropic dry-
etch using SF$_6$
n$^+$/p$^+$
(h)
LPCVD Nitride
deposit (500Å)
n$^+$/p$^+$
(i)
LPCVD nitride
spacer RIE etch
n$^+$/p$^+$
(j)
PR
n$^+$/p$^+$
(k)
HDP oxide RIE etch
n$^+$/p$^+$
(l)
PR strip
n$^+$/p$^+$
(m)
300Å Ni deposit
n$^+$/p$^+$
(n)
2-step RTA silicide anneal
n$^+$/p$^+$
(o)

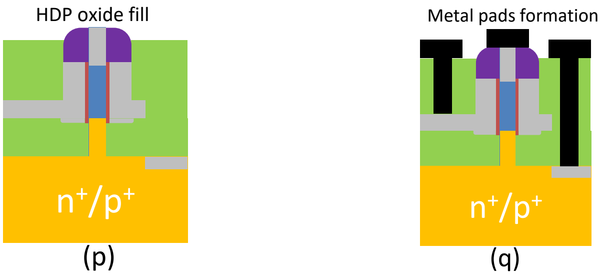
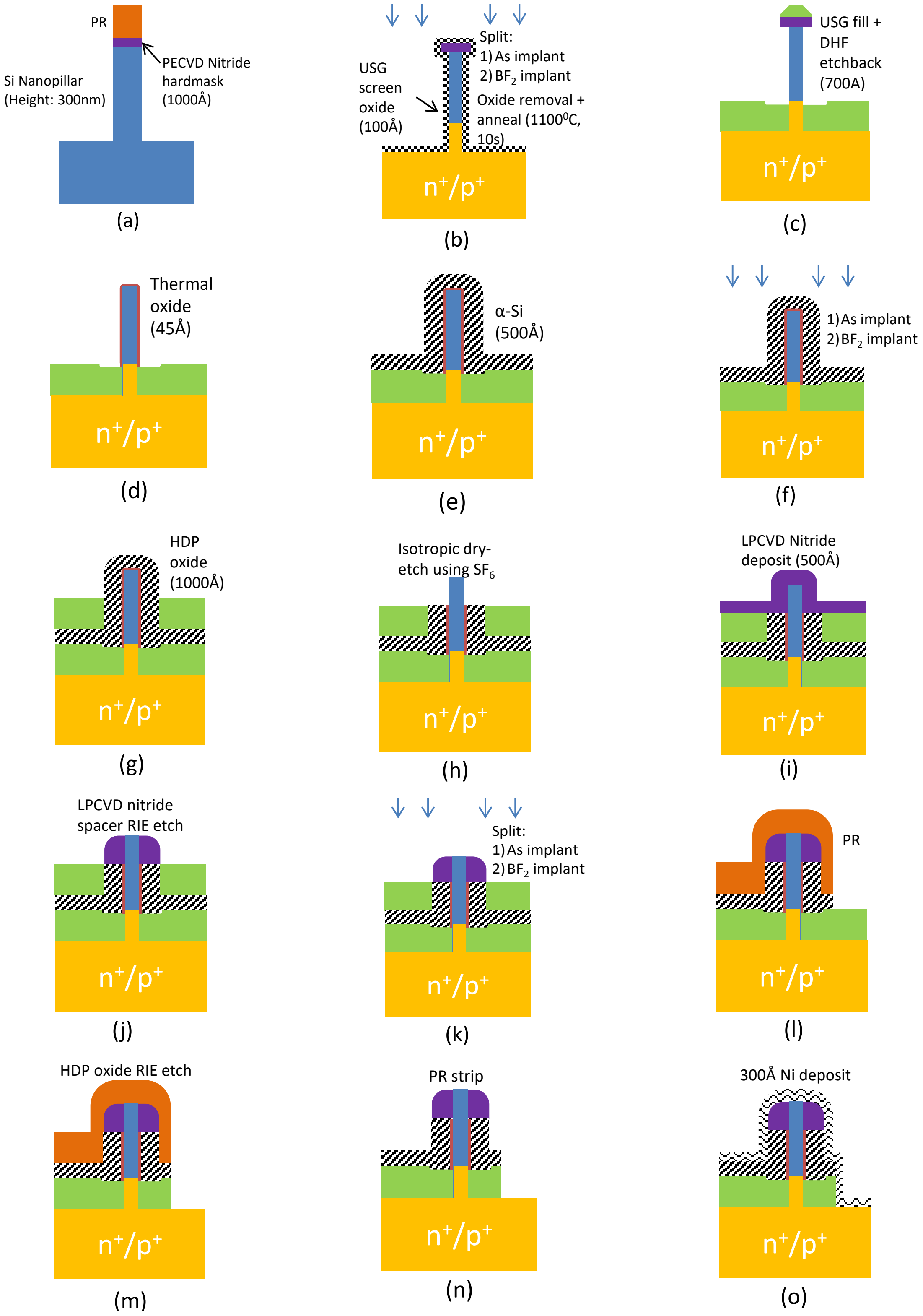


Figure 3.13 Fabrication schematics for Tuned FUSI gate GAA-VSiNW Schottky transistor

3.4.3 Tuned FUSI GAA-VSiNW MOSFET DSS split

The process flow for DSS split is a combination of the baseline and Schottky split process flows. Figure 3.14 details the fabrication schematics of the tuned FUSI GAA-VSiNW DSS transistors.

In the DSS split, the fabrication started with a process flow identical to the baseline. A small change in the flow occurred during the RIE gate patterning etch process. The bottom isolation oxide was removed together with the exposed poly-Si layer. Subsequently, the PR was removed and 300Å Ni was deposited using PVD method. A 2-step RTA silicidation was used to form the nickel silicide, same as the process flow for Schottky split. Following that, the quadruple layer of nitride, PECVD oxide, HDP oxide and PECVD oxide was deposited and CMP was performed before contact holes etch and metallization.


PR
Si Nanopillar
(Height: 300nm)
PECVD Nitride
hardmask
(1000Å)
(a)
USG
screen
oxide
(100Å)
Split:
1) As implant
2) BF_2 implant
Oxide removal +
anneal (1100^{0}C,
10s)
n^+/p^+
(b)
USG fill +
DHF
etchback
(700A)
n^+/p^+
(c)
Thermal
oxide
(45Å)
n^+/p^+
(d)
α-Si
(500Å)
n^+/p^+
(e)
1) As implant
2) BF_2 implant
n^+/p^+
(f)
HDP
oxide
(1000Å)
n^+/p^+
(g)
Isotropic dry-
etch using SF_6
n^+/p^+
(h)
LPCVD Nitride
deposit (500Å)
n^+/p^+
(i)
LPCVD nitride
spacer RIE etch
n^+/p^+
(j)
Split:
1) As implant
2) BF_2 implant
n^+/p^+
(k)
PR
n^+/p^+
(l)
HDP oxide RIE etch
n^+/p^+
(m)
PR strip
n^+/p^+
(n)
300Å Ni deposit
n^+/p^+
(o)

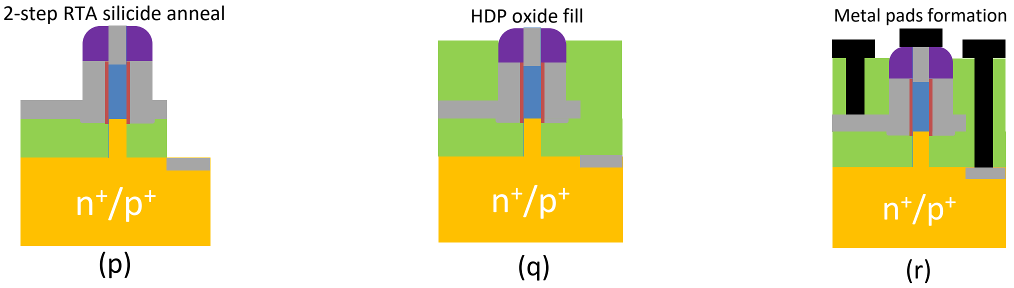


Figure 3.14 Detailed fabrication schematics of tuned FUSI GAA-VSiNW DSS transistors

3.4.4 Summary of GAA-VSiNW MOSFET splits

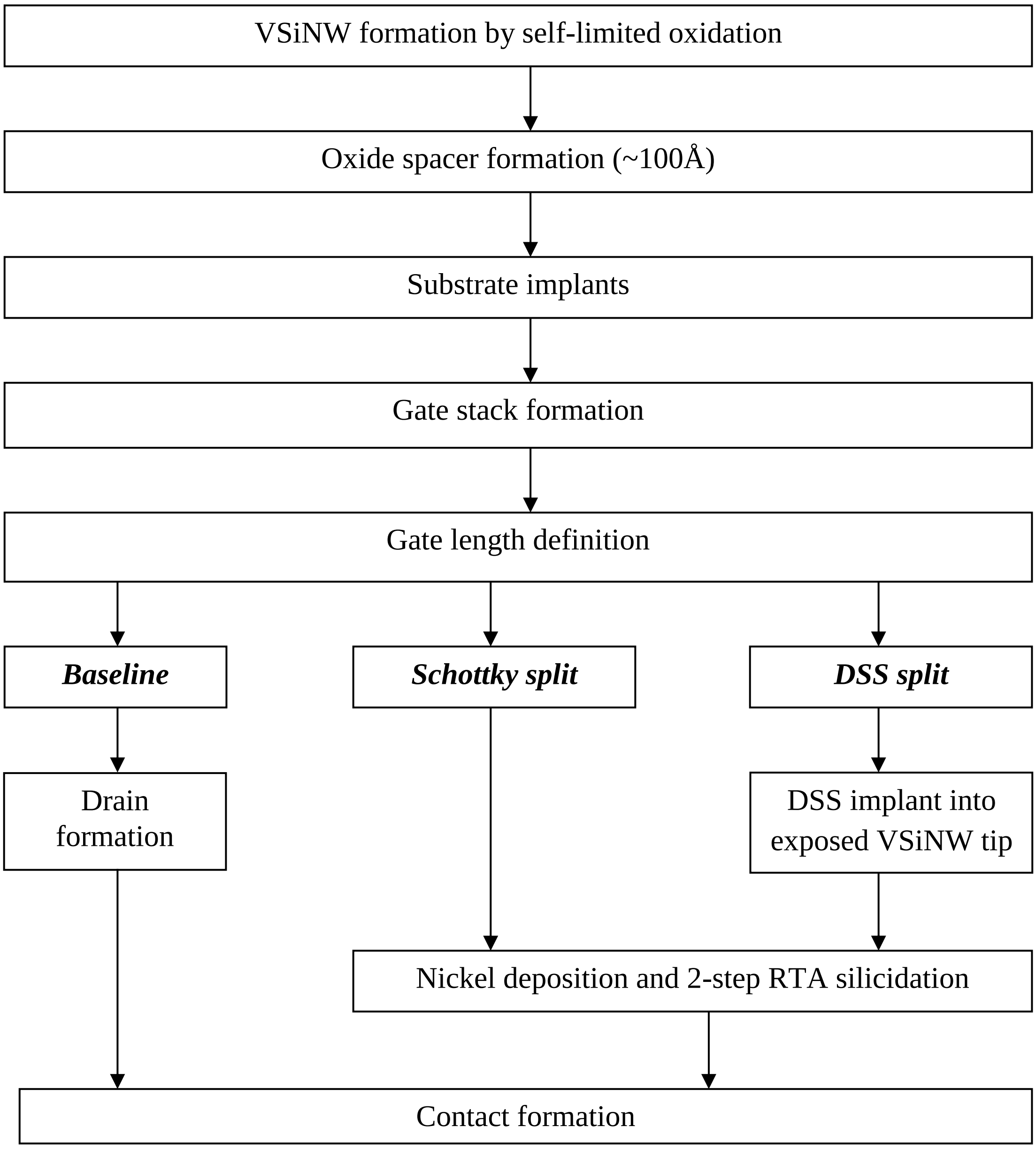


Figure 3.15 Process flow for baseline, Schottky and DSS GAA-VSiNW MOSFETs

Figure 3.15 depicts the overall process flow for the various experimental splits of GAA-VSiNW transistors.

3.5 Summary

VSiNW is the central and most critical infrastructure in this work because it replaces the bulk Si substrate as the starting material to build devices such as diodes and transistors. The process flow to fabricate VSiNW was discussed in great detail. The different fabrication processes for diodes and transistors studied in this work were also described with emphasis on several key process steps. Unless otherwise stated, the experimental procedures described in this chapter would be used in the subsequent chapters.

3.6 References

[3.1] L. Knoll, A. Schafer, S. Trellenkamp, K. K. Bourdelle, Q. T. Zhao, and S. Mantl, "Nanowire and planar UTB SOI Schottky Barrier MOSFETs with dopant segregation," in *Ultimate Integration on Silicon (ULIS), 2012 13th International Conference on*, 2012, pp. 45-48.

[3.2] Z. Yi-Bo, S. Lei, X. Hao, X. Yu-Qian, W. Yi, and Z. Sheng-Dong, "Comparative study of dopant-segregated Schottky barrier germanium nanowire transistors," *Japanese Journal of Applied Physics,* vol. 53, p. 04EN03, 2014.

[3.3] Z. Yi-Bo, S. Lei, X. Hao, H. Jing-Wen, W. Yi, and Z. Sheng-Dong, "Comparative study of silicon nanowire transistors with triangular-shaped cross sections," *Japanese Journal of Applied Physics,* vol. 54, p. 04DN01, 2015.

[3.4] Y. K. Chin, K. L. Pey, N. Singh, L. Guo-Qiang, T. Khing Hong, O. Chio-Yin, *et al.*, "Dopant-Segregated Schottky Silicon-Nanowire MOSFETs With Gate-All-Around Channels," *Electron Device Letters, IEEE,* vol. 30, pp. 843-845, 2009.

[3.5] G. Larrieu and X. L. Han, "Vertical nanowire array-based field effect transistors for ultimate scaling," *Nanoscale,* vol. 5, pp. 2437-2441, 2013.

[3.6] V. Schmidt, H. Riel, S. Senz, S. Karg, W. Riess, and U. Gösele, "Realization of a Silicon Nanowire Vertical Surround-Gate Field-Effect Transistor," *Small,* vol. 2, pp. 85-88, 2006.

CHAPTER 4

Vertical SiNW Schottky and Dopant Segregated Schottky Diodes[a]

4.1 Introduction

With the downscaling of field effect transistor (FET) geometry to meet Moore's Law scaling, silicon nanowires (SiNWs) are viewed as a serious contender to provide Gate-All-Around (GAA) transistor architecture to boost the gate electrostatic control over the channel inversion. In order to take full advantage of the GAA nanowire geometry, vertical SiNWs (VSiNWs) are preferred over lateral nanowires because of their reduced device circuit area, increased circuit speed and reduced circuit power consumption as shown in Table 4.1 [4.1]. Major assumptions used in Table 4.1 are:

1) At a given technology node, the half-pitch "F" is equivalent to the minimum lithographic printable feature size
2) Circuit speed calculation: Speed α 1/RC α $(\mathrm{Area})^{-3/2}$
3) Circuit power consumption calculation: Power α CV^2 α (Area)
4) Parasitic effect is not taken into account for the calculation

---

[a] Reproduced in part from L. Weijie, P. Kin Leong, W. Xinpeng, L. Xiang, C. Zhixian, N. Singh, *et al.*,"Vertical Silicon Nanowire Diode with Nickel Silicide Induced Dopant Segregation," *Japanese Journal of Applied Physics,* vol. 51, p. 11PE08, 2012.

Further details pertaining to the device circuit area, circuit speed and circuit power consumption can be found in [4.1].

	Planar	**Lateral NW**	**Vertical NW**
Device circuit area	$8F^2$, $40F^2$	$8F^2$, $24F^2$ Shrink: ~ 40%	$4F^2$, $12F^2$ Shrink: ~70%
Circuit speed	1	~ 2.2x	~ 6.1x
Circuit power consumption	1	~ 0.6x	~ 0.3x

Table 4.1 Comparison of device circuit area, circuit speed and power consumption between planar bulk devices, lateral and vertical nanowire devices [4.1].

Since the transistor source/drain (S/D) and channel regions are encompassed within the VSiNW, Schottky Barrier (SB) junctions are proposed to replace the conventional doped S/D to alleviate the contact resistance and short channel effects. Currently, PtSi and rare earth silicides, such as $ErSi_x$ or $YbSi_x$, provided the lowest known Schottky Barrier Height (SBH) for p- and n-type SB-MOSFETs (Metal Oxide Semiconductor Field Effect Transistors), respectively [4.2]. Dopant segregation (DS) technique was introduced to overcome the issue of using different metals for different types of MOSFETs and to further reduce SBH. In VSiNW structures, the S/D silicide intrusion length and silicide shape are important for minimizing the gate to S/D parasitic capacitance and the modulation of SBH.

4.2 Silicide intrusion length and silicide interface morphology

The effect of different silicide formation process flow on (i) silicide intrusion length and (ii) silicide/silicon interface morphology will be discussed in this section. Two types of silicidation process flow were used in this work, namely, 1-step RTA and 2-step RTA.

In the 1-step RTA process, the wafers were annealed at $450^{O}C$ for 30 secs after nickel deposition and subsequently, the un-reacted nickel was removed by SPM. In the 2-

step RTA process, the wafers were firstly annealed at 275^{O}C for 30 secs, followed by the removal of un-reacted nickel using SPM and then annealed again at 450^{o}C for 30 secs. The fabrication of the diodes used in this work is described in Chapter 3.

4.2.1 Effect of silicidation process on silicide intrusion length

Figures 4.1 (a) and (b) show the cross-sectional transmission electron microscopy (XTEM) images of SB-VSiNW (diameter ~ 50nm) diodes annealed under different RTA anneal schemes, namely 1-step RTA (450^{O}C) 30 secs and 2-step RTA (275^{O}C, 30 secs followed by 450^{O}C, 30 secs with the removal of un-reacted Ni after first anneal), both with a layer of 30nm Ni. From Figure 4.1 (a), the silicide intrusion length into VSiNW is ~ 95nm after 1-step RTA anneal (measurement is taken with reference to TaN layer). As opposed to 1-step RTA anneal scheme, the 2-step RTA anneal scheme in Figure 4.1 (b) shows no obvious silicide intrusion into VSiNW through XTEM imaging but from in-situ TEM-EDX (Energy Dispersion X-ray) analysis shown in Figure 4.2, Ni signals are collected around the VSiNW tip and TaN areas in Figure 4.3.

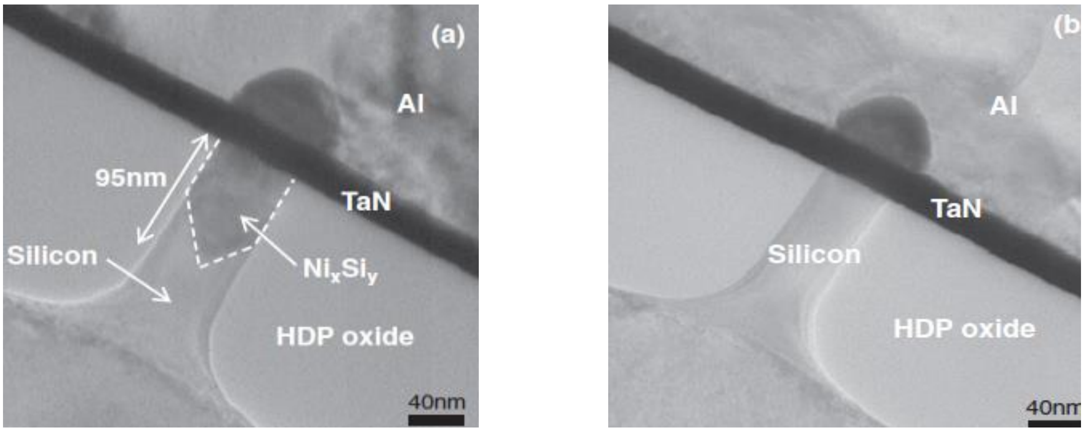


Figure 4.1 XTEM images of SB-VSiNW diodes fabricated via (a) 1- and (b) 2-step silicidation methods. Silicide intrusion was ~ 95 nm after 1-step RTA silicidation. Although no obvious Ni_xSi_y intrusion was observed from the image, Ni signal was detected near VSiNW tip and TaN regions through in-situ TEM–EDX scan. White-dotted lines denote Ni_xSi_y/Si interface.

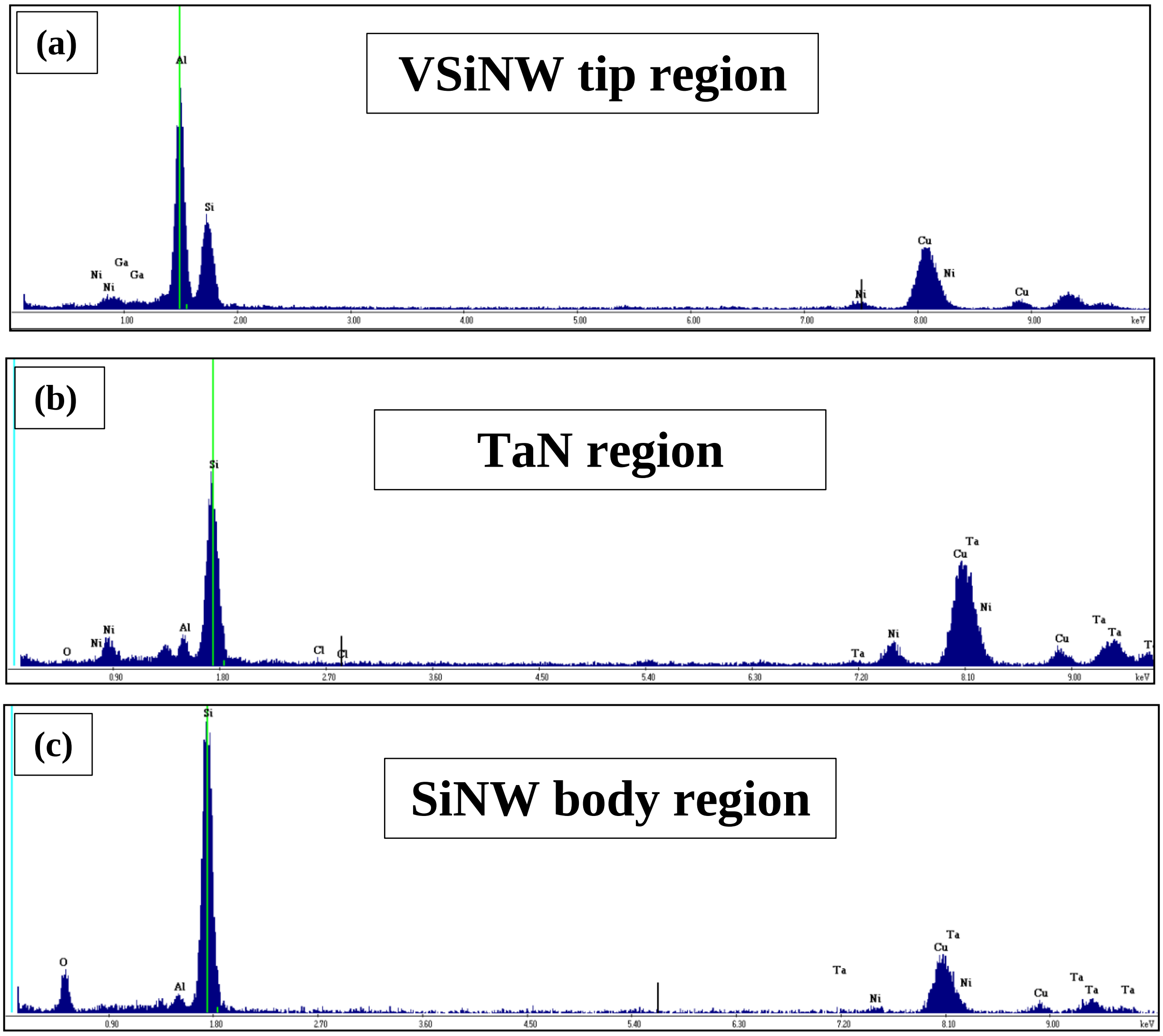


Figure 4.2 TEM-EDX micrographs of (a) VSiNW tip region, (b) TaN region and (c) SiNW body region.

From Figure 4.2, Ni signals are detected in all in-situ TEM-EDX scan regions. The Ni signal intensity increases between VSiNW tip (Figure 4.2 (a)) and TaN (Figure 4.2 (b)) regions with a peak Ni signal intensity in the TaN region and the signal intensity becomes negligible as the EDX scan region approaches the silicon body (Figure 4.2 (c)). This signifies that Ni has successfully silicidized into VSiNW using 2-step RTA anneal and the intrusion length is substantially shorter than 1-step RTA anneal.

For DSSB-VSiNW diodes, the silicide intrusion lengths of both 1-step RTA and 2-step RTA anneal schemes are observed in XTEM images as shown in Figure 4.3. After 1-

step RTA anneal, the silicide intrusion length is ~ 113nm while that of 2-step RTA anneal is ~ 22nm (measurements are taken with reference from the TaN layer). This is about 5 times reduction in length. The intrusion length is confirmed by the in-situ TEM-EDX analysis results. The suppression of silicide intrusion length by using two-step silicide annealing process is consistent with reported literature using planar [4.3] and lateral nanowire [4.4] structures.

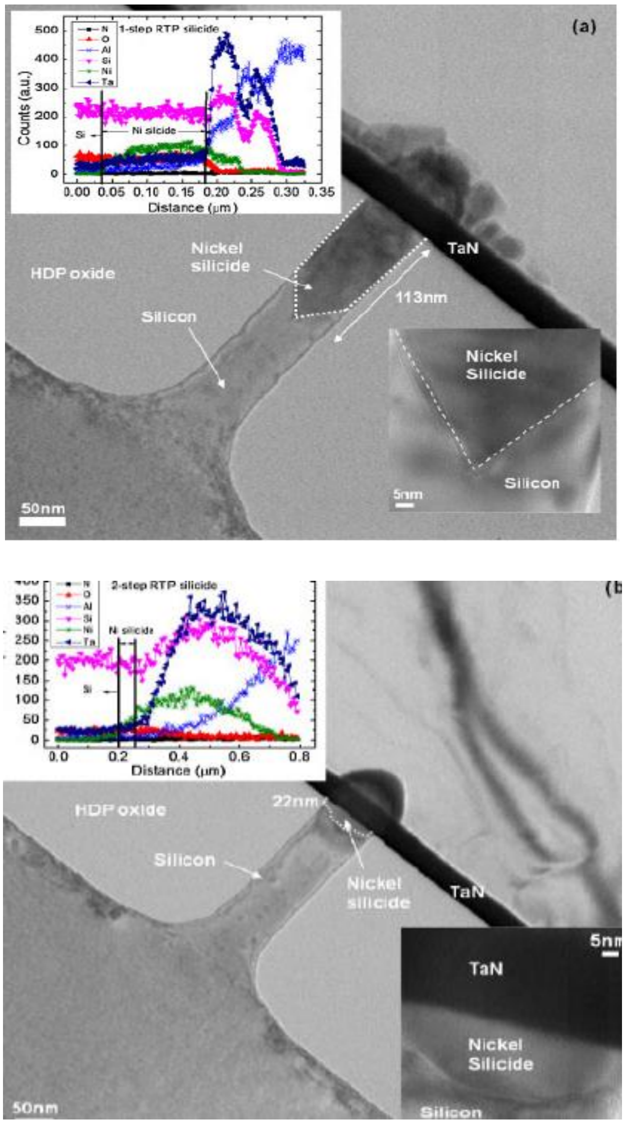


Figure 4.3 XTEM images of DSSB-VSiNW diodes fabricated via (a) 1- and (b) 2-step silicidation methods. Insets are the magnified view of Ni_xSi_y/silicon interface and the in-situ TEM–EDS data. White-dotted lines denote Ni_xSi_y/silicon interface.

4.2.2 Effect of silicidation process on silicide/silicon interface morphology

A common observation from the XTEM micrographs in Figures 4.1 and 4.3 is the formation of a V-shaped silicide interface after one-step silicidation at 450 ^{0}C. From the in-situ TEM-EDX analysis [inset of Figure 4.3 (a)], the Ni to Si ratio is found to be 1:2 and this confirms that $NiSi_2$ is formed within the VSiNW after 450 ^{0}C anneal. The angle of V-shaped silicide facets within VSiNW is identical to the epitaxial growth of $NiSi_2$ pyramidal facets along Si <111> planes in Si (100) thin film [4.6] and this further verifies the existence of $NiSi_2$ in our sample. This is an unexpected result because $NiSi_2$ usually occurs at temperatures above 550 ^{0}C [4.5]. A possible explanation for the formation of $NiSi_2$ pyramidal facets at reduced temperature is proposed.

Firstly, the local temperature within the VSiNW is enhanced due to the low thermal conductivities of the surrounding oxide [4.7] (1.12 $WK^{-1}m^{-1}$) compared to SiNW [4.8] (~25$WK^{-1}m^{-1}$). The phonon transport in SiNWs are reduced due to enhanced boundary scattering as discussed by Li et al., we believe that the thermal conductivity of our VSiNWs could have further reduced due to the SiNW rough sidewalls which increases boundary scattering [4.9]. Therefore, the thermal conductivity of VSiNWs fabricated in this work is lower than those discussed in literature [4.8]. Hence, the phonons are trapped by the oxide surrounding the VSiNWs and within VSiNWs. In turn, the local temperature within VSiNW can easily increase above 550^{0}C. This provides sufficient energy for $NiSi_2$ to be formed directly without passing through other phases.

Secondly, the deposited HDP oxide isolation layer exerts high compressive stress onto the surrounded VSiNW and coupled with the low surface energy level of the Si <111> planes [4.10], Ni atoms tend to precipitate along the Si <111> planes [4.11]. Therefore, $NiSi_2$ phase is formed with pyramidal facets within VSiNW at reduced temperature.

Following the above argument, the local temperature within the VSiNW during the first RTA temperature (275^{0}C) of the two-step anneal should be enhanced to 375 – 450^{0}C, the formation temperature range for NiSi phase. This results in a smooth silicide interface.

After the second RTA (450^{0}C), we should observe the formation of $NiSi_2$ pyramidal facets as in the case of one-step anneal but from the TEM micrograph [Fig. 4(b)], only smooth silicide interface parallel to Si <100> plane is observed. This implies that besides the local heat confinement and surrounding oxide stress, some other effects could play important roles. More experiments must be performed before solid conclusions can be drawn.

4.3 Effect of silicidation process and segregated interfacial dopants on VSiNW diode *I-V* characteristics

In this section, the main discussion will be (i) the impact of different silicidation process and (ii) the effect of segregated interfacial dopants, on diode *I-V* characteristics. Electrical performance of diodes was usually benchmarked using several parameters such as current rectification ratio (R_C), ideality factor (η) and effective SBH for electrons ($\Phi_{B_{n.eff}}$) and holes ($\Phi_{B_{p.eff}}$).

4.3.1 Effect of silicidation process on VSiNW diode *I-V* characteristics

This section examines the effect of 1-step RTA anneal scheme against 2-step RTA anneal scheme on the electrical performance of SB- and DSSB-VSiNW diodes. The nanowire diameter used in measurements is ~ 50nm. Voltage is applied to the silicided nanowire tip and the substrate is connected to 0V. Figure 4.4 shows the measurement setup.

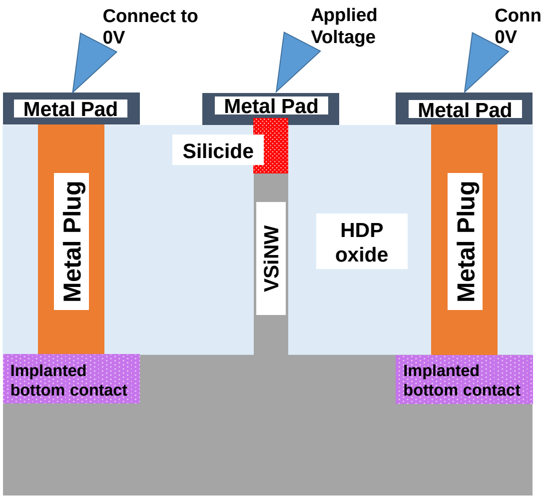


Figure 4.4 SB-VSiNW *I-V* measurement setup. Voltage is applied to silicided VSiNW tip and the substrate is connected to ground.

Figure 4.5 (a) depicts the *I-V* characteristics of SB-VSiNW diodes annealed at the two RTA silicidation processes. From the *I-V* results, we can observe the fabricated SB-VSiNW diode is p-type since higher current is measured when negative voltage applied and lower current is measured when positive voltage is applied. The $I_{forward}$, measured at V = -2V, after both RTA anneals is ~ 10^{-6} A but the $I_{reverse}$ after 1-step RTA anneal (8 x 10^{-9} A), measured at V = 2V, is 2 orders of magnitude higher than that of 2-step RTA anneal (10^{-11} A).

From Figure 4.5 (b), DSSB-VSiNW p-type diodes showed $I_{forward}$, measured at V = -2V, after both RTA schemes is ~ 10^{-6} A and $I_{reverse}$, measured at V = 2V, after 1-step RTA anneal is ~ 10^{-11} A while that of 2-step RTA anneal is ~ 4 x 10^{-13} A. The 2-step RTA anneal demonstrated an improvement of 2 orders in magnitude for $I_{reverse}$, identical to SB-VSiNW diodes.

For DSSB-VSiNW n-type diodes, shown in Figures 4.5 (c) and (d), we can observe the $I_{forward}$, measured at V = 2V, peaks at ~ 10^{-5} A. Compared to the $I_{forward}$ value of DSSB-VSiNW p-type diodes, it is increased by ten times. This boost in $I_{forward}$ can be attributed to the different current carrier types, namely, electrons for n-type diodes and holes for p-type diodes and the use of nanowire infrastructure. Electron mobility (1400 $cm^2/(V{\cdot}s)$) in silicon is three times higher than that of hole mobility (450 $cm^2/(V{\cdot}s)$) in silicon, it is expected n-type VSiNW has at least three times higher $I_{forward}$ than p-type VSiNW diodes. In our study, n-type VSiNW diodes showed ten times increase over p-type VSiNW diodes. This implies that the additional increase in $I_{forward}$ can be attributed to a combination of various factors such as (i) VSiNW architecture, (ii) strain induced by surrounding oxide, (iii) decrease in Schottky Barrier width by dopants segregated at silicide/Si interface to increase carrier injection. From Figures 4.5 (c) and (d), we can also observe $I_{reverse}$, measured at V = -2V, after 2-step RTA is 1 to 2 orders in magnitude lower than 1-step RTA.

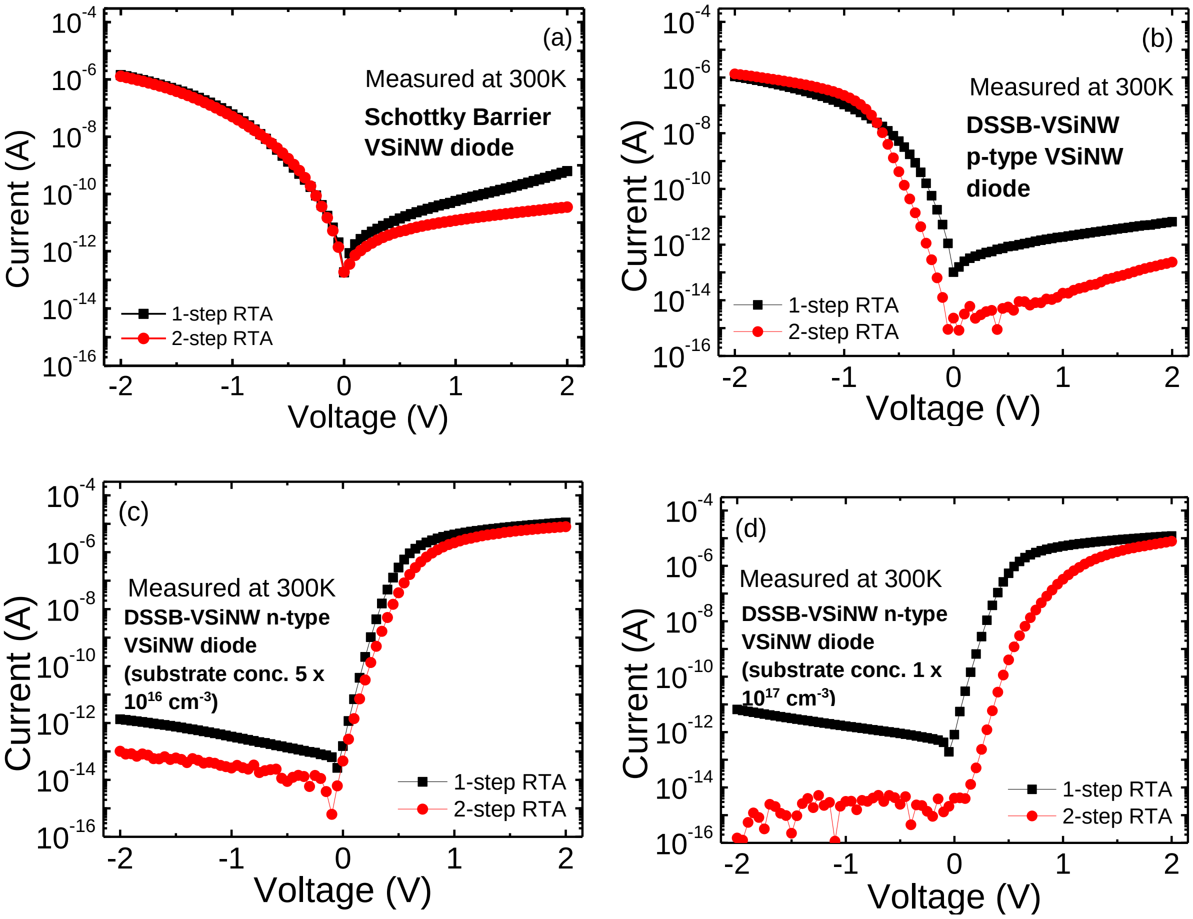


Figure 4.5 *I–V* measurement data of (a) SB-VSiNW diode, (b) DSSB-VSiNW p-type diode with As implant on 10^{15} cm^{-3} p-type substrate, (c) DSSB-VSiNW n-type diode with BF_2 implant on 4 x 10^{16} cm^{-3} n-type substrate and (d) DSSB-VSiNW n-type diode with BF_2 implant on 10^{17} cm^{-3} n-type substrate fabricated separately via 1- and 2-step RTA silicidation methods.

We proposed a plausible hypothesis to explain why measured $I_{reverse}$ after 1-step RTA anneal is much higher than that of 2-step RTA anneal. It is well-documented that nickel atoms are the dominant diffusion species in the formation of nickel silicide and Ni is a fast diffusion species verified by its high diffusion coefficient. During the annealing process, Ni atoms diffuse rapidly into Si to form nickel silicide and some Ni atoms will diffuse into Si to cause various defects and Ni-related deep level defects were reported in literature18-19). In general, nickel silicide will undergo three sequential transformation phases: (i) Ni_2Si, (ii) NiSi and (iii) $NiSi_2$, depending on the annealing temperature and annealing duration [4.12].

Tian [4.21] *et al.* and Qu [4.14] *et al.* reported that the amount of deep-level defects is reduced when nickel silicide is formed at higher temperature above 450^{o}C [4.13]. In addition, Qu *et al.* [4.14] and Foggiato [4.5] *et al.* discussed that a primary low temperature annealing followed by a secondary higher temperature annealing could also help to lower the deep level defects and improve device leakage.

In our study, we have confirmed that the nickel silicide phase formed via 1-step RTA anneal process is $NiSi_2$ as discussed in Section 4.2.2. This increases the concentration of interfacial and Ni-related deep-level defects due to the rough $NiSi_2$ interface [4.15] and the continuous supply of Ni atoms (un-reacted Ni is removed only after the RTA anneal). Therefore, $I_{reverse}$ for 1-step annealed SB-VSiNW diodes is expected to be higher.

In retrospect, for the 2-step RTA silicidation anneal process, the first stage low temperature (275^{o}C, 30 secs) RTA anneal could have induced large amounts of the deep-level defects but the subsequent removal of un-reacted nickel removal and high temperature (450^{o}C, 30 secs) RTA anneal has helped to eliminate the deep-level defects [4.13]. In our study, regardless of SB- or DSSB-VSiNW diodes, $I_{reverse}$ values for the 2-step annealed VSiNW diodes are consistently lower than the 1-step annealed counterparts. This result is consistent with literature.

Figure 4.6 illustrates the rectification (R_C) characteristics of SB- and DSSB-VSiNW diodes. DSSB-VSiNW diodes are further separated into n- and p-type diodes in Figure 4.6 (b), (c) and (d). R_C is defined as the maximum-to-minimum current ratio where the bias voltage for maximum/minimum current is extracted at ± 2V. In general, diodes should possess relatively high R_C values. This means at forward bias, there should be large forward current and at reverse bias, there should be very small leakage current.

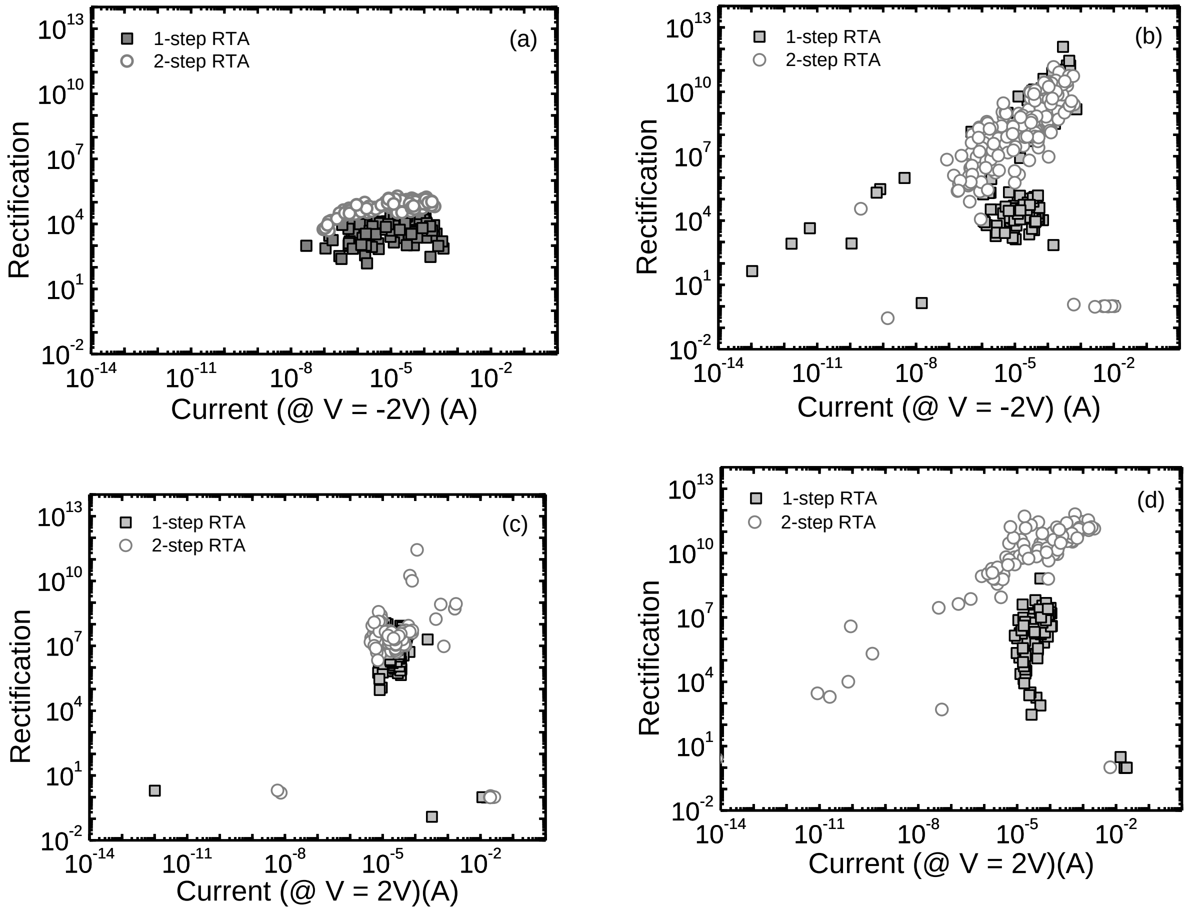


Figure 4.6 Rectification (*R_C*) values plotted as a function of forward current for (a) SB-VSiNW diode, (b) DSSB-VSiNW p-type diode, (c) DSSB-VSiNW n-type diode with substrate concentration = 4 x 10^{16} cm^{-3} and (d) DSSB-VSiNW n-type diode with substrate concentration = 1 x 10^{17} cm^{-3}.

From Figure 4.6 (a), SB-VSiNW diodes processed using 2-step silicidation RTA show higher R_C value (~ 4 x 10^4) in contrast to the same type of diodes processed using 1-step silicidation RTA (~ 10^3). This represents more than 1 order of magnitude increase. In the case of DSSB-VSiNW n-type (with substrate concentration = 1 x 10^{17} cm^{-3}) diodes shown in Figurer 4.6 (d), R_C values of the diodes annealed using 2-step RTA (~ 10^{10}) are ~ 3 orders of magnitude higher than those annealed using 1-step RTA (~ 6.5 x 10^6).

From Figures 4.6 (b) and (c), the R_C values for DSSB-VSiNW p-type and n-type (with substrate concentration = 4 x 10^{16} cm^{-3}) diodes, fabricated under different silicide annealing processes are very similar with 2-step RTA having slightly higher values than 1-

step RTA. In general, 1-step silicide RTA anneal achieve lower R_C values than 2-step silicide RTA anneal due to the higher $I_{reverse}$ caused by the increased concentration of interfacial and Ni-related deep level defects along Si <111> planes.

4.3.2 Impact of interfacial segregated dopants on VSiNW diode *I-V* characteristics

The impact of silicide RTA scheme on diode *I-V* characteristics is discussed in the Section 4.3.1. It is understood that $I_{reverse}$ of VSiNW diodes with or without segregated dopants fabricated using 2-step silicide anneal process are lower than those fabricated using 1-step silicide anneal process.

In this section, the *I-V* measurements of SB-VSiNW diodes and DSSB-VSiNW p-type diodes fabricated using the same RTA anneal scheme are compared to explore the effect of interfacial segregated dopants on VSiNW diode performance.

The *I-V* performance of SB-VSiNW and DSSB-VSiNW p-type diodes fabricated under 1-step RTA anneal scheme is shown in Figure 4.7 (a). The results showed $I_{forward}$ of DSSB-VSiNW p-type diodes is ~ 6 times higher than that of SB-VSiNW diodes. In addition, $I_{reverse}$ of DSSB-VSiNW p-type diode showed reduction of 1 order (from 3 x 10^{-11}A to 2 x 10^{-12}A) in magnitude.

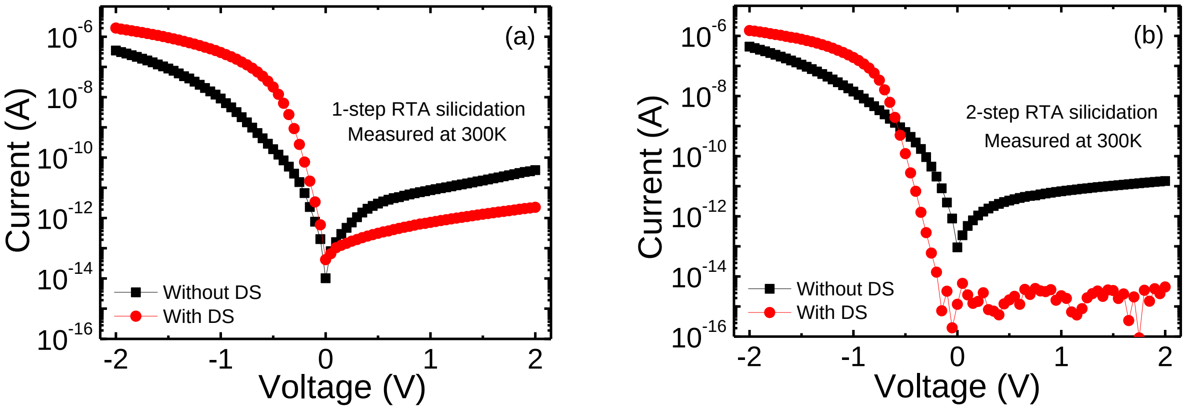


Figure 4.7 ***I-V*** **measurements of SB-VSiNW and DSSB-VSiNW p-type diodes fabricated using (a) 1-step RTA anneal and (b) 2-step RTA anneal.**

Figure 4.7 (b) illustrates the *I-V* performance of SB-VSiNW and DSSB-VSiNW p-type diodes fabricated under 2-step RTA anneal. $I_{forward}$ of DSSB-VSiNW p-type diodes is ~ 5 times higher than that of SB-VSiNW diodes. The result is almost identical to that of 1-step RTA anneal. This implies that the underlying mechanism that causes increase in $I_{forward}$ is very likely to be the same. More details will be discussed later. Furthermore, $I_{reverse}$ of DSSB-VSiNW p-type diode is found to be 4 orders in magnitude lower than SB-VSiNW (from 2 x 10^{-11}A to 5 x 10^{-15}A). Compared to 1-step RTA anneal, the reduction in $I_{reverse}$ is much higher and is consistent with the findings discussed in previous Section 4.3.1.

Inferring to Yamauchi et al. first-principle simulation which uses boron (B) as the implant [4.17], we postulate a simple hypothesis the impact of segregated dopants for our VSiNW diodes. The implanted As atoms used in this work, combined with the use of nickel silicide to segregate the dopants at silicon/silicide interface, occupy the substitutional sites within the first Si monolayers in close vicinity to the silicide/silicon interface and are positively charged by the interface states. As a result, electric dipoles are formed across the interface. With the formation of electric dipoles, Si energy band adjacent to the silicide/silicon interface experiences severe downward band bending and reduction of depletion layer thickness. During forward bias operation, when negative voltage is applied to silicided VSiNW tip and 0V is applied to VSiNW body, the thermal emission of hole from Si to Ni_xSi_y and tunneling of electron from Ni_xSi_y to Si substrate are enhanced. This in turn increases the $I_{forward}$ of DSSB-VSiNW diodes in contrast to SB-VSiNW diodes.

Simultaneously, the segregated dopants also help to reduce the $I_{reverse}$. During the reverse bias operation, the Si energy band bends upwards when positive voltage is applied to the silicided tip and VSiNW body remains at 0V. Electron tunneling is impeded and this leads to low leakage current. The hypothesis is proven in Section 4.4.2.

4.4 Effect of silicidation process and segregated interfacial dopants on diode ideality factor and effective Schottky Barrier Height

4.4.1 Impact on diode ideality factor (η)

Thus far, the choice of silicidation process and the incorporation of DS technique have demonstrated to affect the VSiNW diode *I-V* characteristics. In this section, the diode ideality factor (η) and effective SBH ($\Phi_{B_{eff}}$) are studied. Figure 4.8 (a) shows η of SB- and DSSB-VSiNW p-type diodes fabricated using different silicidation process. Ideality factor is extracted from the slope of the linear region of the forward bias ln *I-V* plot [4.16]

From Figure 4.8 (a), the 2-step silicided SB-VSiNW diodes generally exhibited a reduction ~ 14% in η values, as compared to 1-step silicided SB-VSiNW diodes before the integration of the segregated dopants. This can be attributed to the reduction in the deep-level defects previously mentioned. Furthermore, the η values of SB-VSiNW diodes maintained above 2.0 for every measurement temperature.

With the inclusion of the DS technique, η of DSSB-VSiNW p-type diodes dropped by 42% to ~ 1.5 and 61% to ~ 1.2, for 1-step and 2-step RTA schemes, respectively. In addition, the η values of DSSB-VSiNW p-type diodes remain under 1.5 for every measurement temperature. Since it is known that deep-level interface defects are introduced into silicon during nickel silicide formation by RTA [4.13], DS implant is able to passivate these interfacial defects and causes η to improve closer to unity. This is confirmed by examining the η values extracted from DSSB-VSiNW n-type diodes fabricated under 1-step and 2-step RTA schemes shown in Figure 4.8 (b). The average η value of DSSB-VSiNW n-type diode is ~ 1.6 and ~ 1.3 after 1-step RTA and 2-step RTA anneal, respectively. Furthermore, we can observe that the lowest η value is achieved when the combination of DS technique and 2-step RTA silicide anneal are used to form DSSB-VSiNW diode.

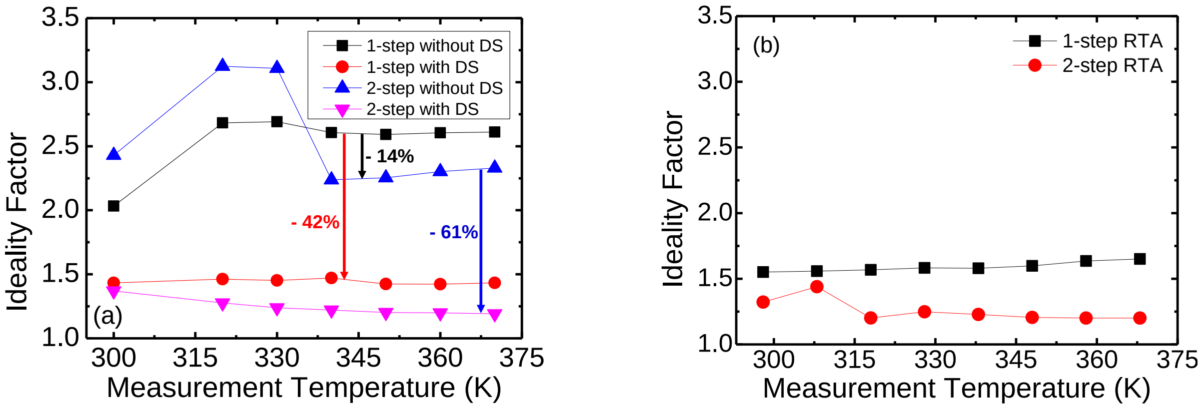


Figure 4.8 η as a function of measurement temperatures taken from VSiNW diodes with and without DS implant, fabricated under different RTA anneal schemes.

4.4.2 Impact on effective Schottky Barrier Height (Φ_{Beff})

Figures 4.9 (a) and (b) show the extracted $\Phi_{B_{p,eff}}$ and $\Phi_{B_{n,eff}}$ values for SB-VSiNW and DSSB-VSiNW p-type diodes plotted against measurement temperatures. $\Phi_{B_{p.eff}}$ is extracted using Richardson plot at a forward bias voltage V = -0.3V. $\Phi_{B_{n.eff}}$ is calculated by using the relationship, $\Phi_{B_{p.eff}} + \Phi_{B_{n.eff}} = E_g$, where E_g is the bandgap energy of Si (1.12 eV).

From Figure 4.9 (a), we can observe that by replacing the 1-step silicide anneal (black line) with the 2-step anneal (green line), $\Phi_{B_{p.eff}}$ of SB-VSiNW diodes increase by 31% from 0.42 eV to 0.61 eV. With the introduction of segregated dopants, $\Phi_{B_{p.eff}}$ of DSSB-VSiNW p-type diodes increase by 19% and 7.5% for 1-step anneal and 2-step anneal, respectively. Similarly, combining DS technique with different RTA anneal scheme, we can see an increase of 21% in $\Phi_{B_{p.eff}}$.

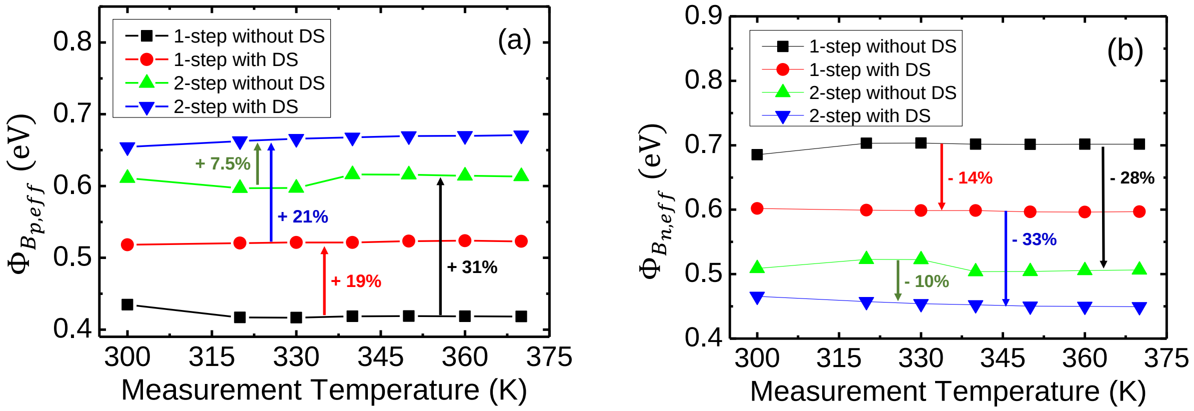


Figure 4.9 (a) $\Phi_{Bp,eff}$ and (b) $\Phi_{Bn,eff}$ as a function of measurement temperatures taken from VSiNW p-type diodes with and without DS implant for different silicide anneal RTA schemes.

Figure 4.9 (b) shows the $\Phi_{B_{n.eff}}$ values of the same diodes used to extract $\Phi_{B_{p.eff}}$. In conjunction with Figure 4.9 (a), an increase (decrease) in $\Phi_{B_{p.eff}}$ will result in a decrease (increase) in $\Phi_{B_{n.eff}}$. From Figure 4.9 (b), based on SB-VSiNW diode, changing of RTA anneal scheme from 1-step to 2-step will result in a 28% drop in $\Phi_{B_{n.eff}}$ from 0.70 eV to 0.51 eV. With dopant segregation at the silicon/silicide interface, $\Phi_{B_{n.eff}}$ is reduced by 14% and 10% for 1-step and 2-step anneals, respectively. This reduction in $\Phi_{B_{n.eff}}$ confirms our initial hypothesis postulated in Section 4.3.2.

Figures 4.10 (a) and (b) shows the $\Phi_{B_{n.eff}}$ and $\Phi_{B_{p.eff}}$ values extracted from DSSB-VSiNW n-type diodes. Results from Figures 4.9 and 4.10 co-relate well with the measured *I-V* data in Section 4.3.

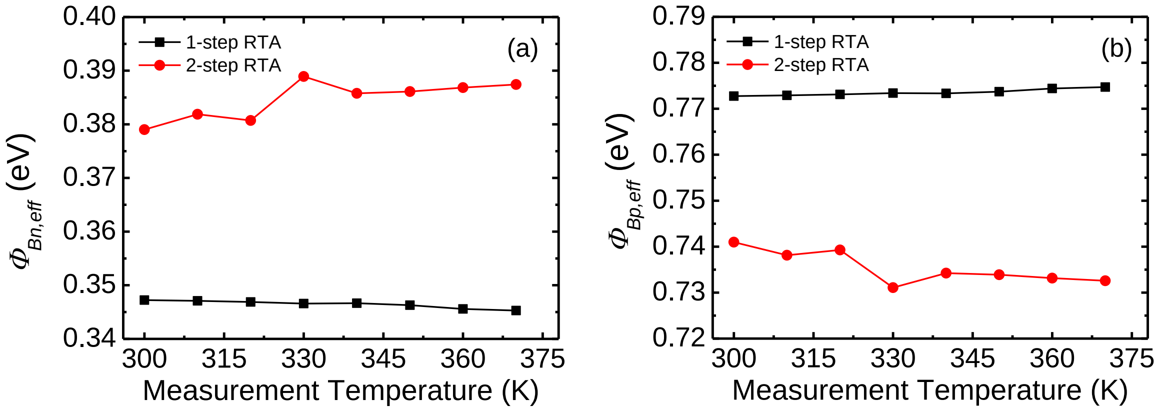


Figure 4.10 (a) $\Phi_{Bn,eff}$ and (b) $\Phi_{Bp,eff}$ of DSSB VSiNW n-type diodes fabricated under different RTA schemes as a function of measurement temperature.

Based on the experimental results, $\Phi_{Bn,eff}$ of SB-ViSNW diodes can be tuned by using the appropriate silicidation process and the incorporation of DS further enhances the lowering of $\Phi_{Bn,eff}$. Although $\Phi_{Bn,eff}$ is reduced in the present work, the values obtained are still unable to position SB MOSFETs favorably with respect to the conventional technology [4.18]. Therefore, further optimization in reducing $\Phi_{Bn,eff}$ is required. Possible solutions include optimization of the dopant segregation technique (with plasma doping) and optimization of the silicide formation.

4.5 Summary

The impact of silicide formation and segregated interfacial dopants in VSiNW diodes is studied. The optimal combination of 2-step silicidation and DS technique offers shallow silicide with intrusion length of ~ 22 nm and relatively flat silicide/silicon interface morphology. Based on the findings of DSSB-VSiNW p-type diode, low $\Phi_{Bn,eff}$ ~ 0.47 eV, $I_{forward}$ ~ 40 µA/µm and extremely low $I_{reverse}$ ~ 40 fA/µm can be achieved. However, $\Phi_{Bn,eff}$ must be further reduced and optimized for future integration of Schottky Barrier nanostructures in future CMOS circuit.

4.6 References

[4.1] D.-L. Kwong, X. Li, Y. Sun, G. Ramanathan, Z. X. Chen, S. M. Wong, Y. Li, N. S. Shen, K. Buddharaju, Y. H. Yu, S. J. Lee, N. Singh, and G. Q. Lo: *J. Nanotechnol.*, pp. 492121, 2012.

[4.2] Z. Qiu, Z. Zhang, M. O¨ stling, and S. L. Zhang: *IEEE Trans. Electron Devices*, vol. 55, pp. 396, 2008.

[4.3] A. Lauwers, J. A. Kittl, M. Van Dal, O. Chamirian, R. Lindsay, M. de Potter, C. Demeurisse, C. Vrancken, K. Maex, X. Page`s, K. Van der Jeugd, V. Kuznetsov, and E. Granneman: *Microelectron. Eng.*, vol. 76, pp. 303, 2004.

[4.4] H. Arai, H. Kamimura, S. Sato, K. Kakushima, P. Ahmet, K. Tsutsui, N. Sugii, K. Natori, T. Hattori, and H. Iwai: *ECS Trans.*, vol. 25, no. 7, pp. 447, 2009.

[4.5] J. Foggiato, W. S. Yoo, M. Ouaknin, T. Murakami, and T. Fukada: *Mater. Sci. Eng. B*, vol. 56, pp. 114–115, 2004.

[4.6] S. Migita, Y. Morita, W. Mizubayashi, and H. Ota: *Ext. Abstr. Int. Workshop Junction Technology*, pp. 1, 2010.

[4.7] M. B. Kleiner, S. A. Ku¨hn, and W. Weber: *Proc. European Solid State Device Research Conf.*, pp. 473, 1995.

[4.8] D. Li, Y. Wu, P. Kim, P. Yang, and A. Majumdar: *Appl. Phys. Lett.*, vol. 83, 2934, 2003.

[4.9] A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar, and P. Yang: *Nature*, vol. 451, pp. 163, 2008.

[4.10] R. J. Jaccodine: *J. Electrochem. Soc.*, vol. 110, pp. 524, 1963.

[4.11] A. Lauwers, P. Besser, T. Gutt, A. Satta, M. de Potter, R. Lindsay, N. Roelandts, F. Loosen, S. Jin, H. Bender, M. Stucchi, C. Vrancken, B. Deweerdt, and K. Maex: *Microelectron. Eng.*, vol. 50, pp. 103, 2000.

[4.12] F.F. Zhao, J.Z. Zheng, Z.X. Shen, T. Osipowicz, W.Z. Gao, L.H. Chan: *Microelectron. Eng.*, vol. 71, pp. 104–111, 2004.

[4.13] Y. Tian, Y.-L. Jiang, Y. Chen, F. Lu, and B.-Z. Li: Semicond. Sci. Technol., vol. 17, pp. 83, 2002.
[4.14] X. P. Qu, Y. -L. Jiang, G. -P. Ru, F. Lu, B. -Z. Li, C. Detavernier, R.L. Van Meirhaeghe, Thin Solid Films, vol. 462–463, pp. 146-150, 2004.
[4.15] J. Foggiato and W. S. Yoo: Ext. Abstr. Advanced Semiconductor Manufacturing Conf. Workshop, pp. 205, 2005.
[4.16] E. H. Rhoderick and R. H. Williams: Metal Semiconductor Contacts (Clarendon Press, Oxford, U.K., 1988).
[4.17] T. Yamauchi, A. Kinoshita, Y. Tsuchiya, J. Koga, and K. Kato: IEDM Tech. Dig., pp. 1, 2006.
[4.18] D. Connelly, C. Faulkner, and D. E. Grupp: IEEE Trans. Electron Devices, vol. 50, pp.1340, 2003.

CHAPTER 5

PERFORMANCE AND THRESHOLD VOLTAGE ENGINEERING OF GAA-VSINW WITH HIGHLY DOPED SOURCE/DRAIN FOR CMOS CIRCUIT INTEGRATION

5.1 Introduction

With the continuous scaling of CMOS technology to extend Moore's Low, Gate-All-Around Nanowire Field-Effect Transistor (GAA-NW FET) is considered as one of the promising candidates. GAA-NW FET demonstrates the natural progression after the multi-gate (FinFET) structure since the GAA architecture offers the best gate electrostatic control to scale the channel region. Hence, GAA-NW FET exhibit close-to-ideal sub-threshold swing (SS), very low DIBL (Drain-Induced Barrier Lowering) and threshold voltage roll-off characteristics [5.1 - 5.8].

In GAA-SiNW FETs, SiNW replaces conventional bulk Si substrate as the starting platform in which the channel, source and drain will be formed. The SiNW can be fabricated via two orientations – lateral or vertical, illustrated in Figures 5.1 (a) and (b), respectively. Despite its advantages, the lateral GAA-SiNW (GAA-ℓSiNW) transistors encounter process-related issues that could possibly limit its scalability.

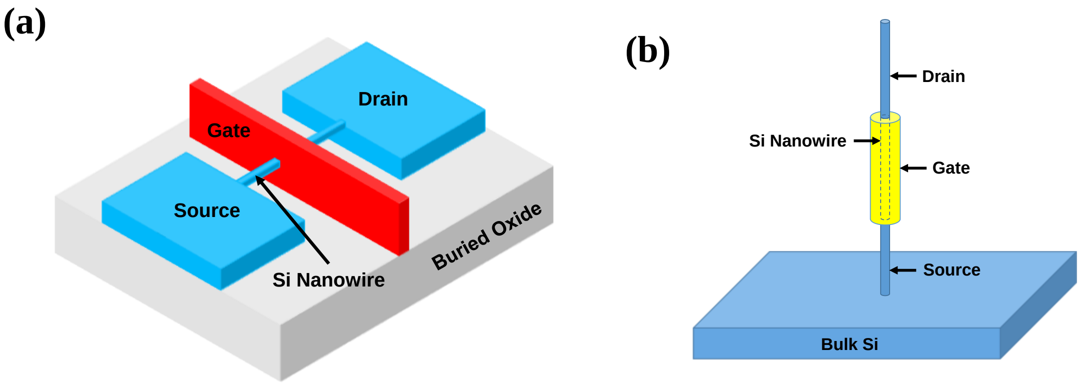
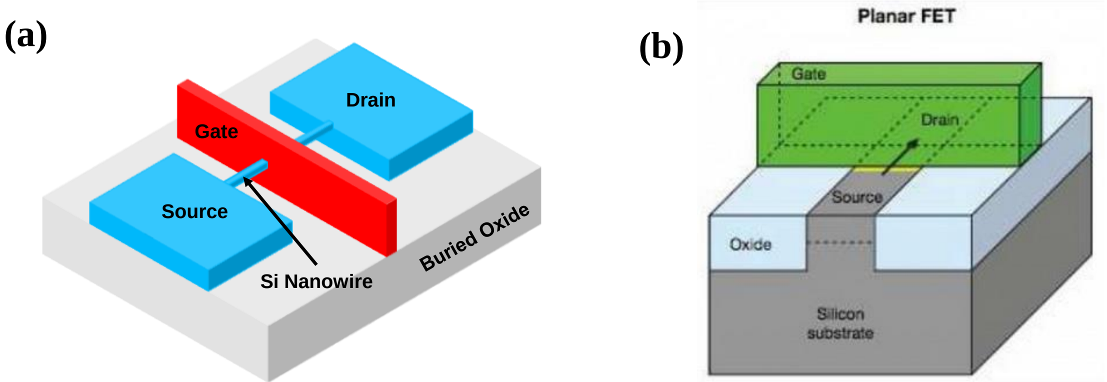


Figure 5.1 Schematic diagrams show the (a) GAA-lSiNW FET and (b) vertical GAA-SiNW (GAA-VSiNW) FET. Process related issues such as (i) defining uniform gate and (ii) high source/drain extension resistance could hinder the scalability of lateral GAA-VSiNW. On the other hand, vertical GAA-VSiNW FET is regarded as the most promising alternative while still capitalizes on conventional CMOS fabrication process.

Defining a uniform gate over the channel region is a serious challenge encountered by GAA-ℓSiNW FETs. The shadowing effects during the plasma etch of the poly-Si gate may cause the formation of un-wanted poly stringers beneath the lateral non-gated regions along the SiNW. This will result in the increase of overall effective gate length and renders the physical gate length as an unreliable representation of the effective gate length.

Another issue faced by GAA-ℓSiNW FET is to obtain small channel lengths out of relatively long nanowires. The use of expensive lithography process tools such as 193nm ArF immersion or EUV (Extreme-UV) steppers and elaborate lithography techniques, such as double-patterning and LELE (Litho-Etch-Litho-Etch), will be involved and higher cost per device is expected.

Lastly, GAA-ℓSiNW architecture will eventually encounter the same process lithography problem of printing the gate region with adequate resolution as its planar counterpart, when the gate length shrinks down to reduce individual device estate while increasing the packing density per unit floor area. This is because both GAA-ℓSiNW and planar transistors are oriented in the same manner on the wafer. A simple illustration is shown in Figure 5.2 to offer a detailed explanation.



(Image courtesy of Intel Corporation)

Figure 5.2 Illustrations of (a) GAA-ℓSiNW FET and (b) conventional planar 2D FET comparing their respective orientation on wafer. As shown, both architectures have the same lateral on-wafer orientation and this suggests that GAA-lSiNW FET will eventually experience the same process lithography difficulty of printing the gate region with good resolution

Vertical SiNW with GAA architecture (GAA-VSiNW) presents itself to be the prominent alternative to GAA-ℓSiNW to fully leverage on the benefits of GAA-SiNW infrastructure and mitigate the issues faced by GAA-ℓSiNW. As observed in Figure 5.1, the design of GAA-VSiNW is very similar to GAA-ℓSiNW except that the drain, gate and source are positioned on top of one another and the current flow is perpendicular to the wafer surface.

In this chapter, the feasibility of fabricating GAA-VSiNW pFET and nFET with highly-doped S/D via conventional CMOS processes is first explored. This is followed by the study of the electrical characteristics and the short channel effects of the fabricated devices, comparing with the values obtained from literature. Finally, two threshold voltage (V_T) tuning methods, (1) varying VSiNW diameter and (2) introduction of opposite polarity dopant species to the device gate region, to optimize the incorrect device V_T values are investigated.

5.2 Experimental Details

The fabrication process details for the vertical GAA-SiNW PFET and NFET devices studied in this chapter had been outlined in Section 3.4.1 in Chapter 3.

In summary, GAA-VSiNW pMOS was constructed on a single VSiNW with height ~ 300nm, gate length (L_{gate}) ~ 100nm and varying diameters. The VSiNW tip and wafer substrate will serve as the drain (D) and source (S) regions, respectively. Both S/D regions are heavily doped with BF_2 implant. The gate region comprises of 50nm poly-Si deposited via Chemical Vapour Deposition (CVD) method on top of an isolation oxide spacer layer that separates the gate and source, followed by BF_2 implantation (5 KeV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations). In the case of GAA-VSiNW nMOS, the entire process flow is identical to that of vertical GAA-SiNW pMOS except the implant species used is As (Arsenic) instead BF_2. Finally, electrical contacts to S/D and gate regions are done through patterned metal layers consisting of TaN/Al/TaN layers.

For the V_T tuning splits, the gate implant conditions are shown in the table below.

Device	**Implant conditions**
GAA-VSiNW nMOS (control)	P/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations
GAA-VSiNW nMOS (tuned V_T)	BF_2/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations

Table 5.1 List of gate implant conditions for V_T tuning splits

From the Table 5.1, it can be observed that the implant conditions are kept constant and the only difference is the dopant species used for the implant process. GAA-VSiNW nMOS is chosen as the test vehicle for the device V_T tuning study because from literature, the V_T value for GAA-VSiNW FETs tends to be negative.

Figure 5.3 shows the TEM (Transmission Electron Micrograph) image of a single GAA-VSiNW FET with TaN/Al/TaN metal layers taken on larger diameter (50nm) device for the ease of sample preparation. From Figure 5.3, we can see that the VSiNW side-wall is relatively rough and this might cause the carrier mobility to decrease. The carrier mobility will be studied in the subsequent section.

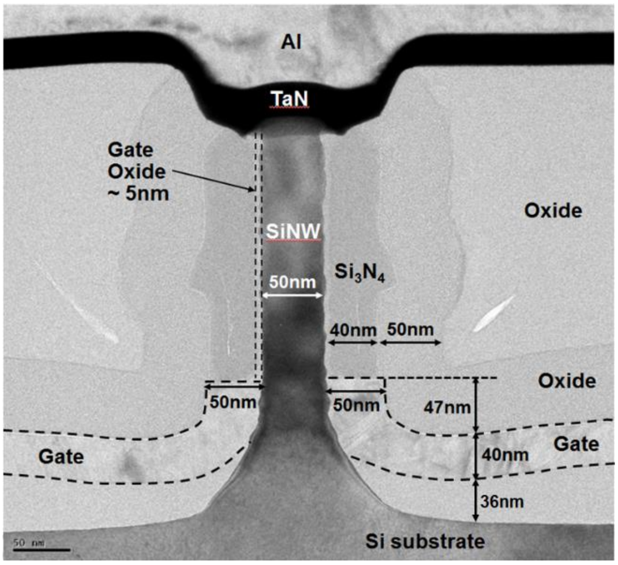


Figure 5.3 Cross-sectional TEM image showing the GAA-VSiNW FET with metal layers for probing. Side-wall of fabricated VSiNW is relatively rough and the carrier mobility might be affected. The measured L_{gate} is ~ 87nm as compared to the intended 100nm. Gate oxide is ~ 5nm and Si_3N_4 spacer surrounding the VSiNW body is ~ 40nm. The oxide isolation between the gate and source (wafer substrate) regions is ~ 36nm. Dotted lines are used for the ease of viewing.

5.3 GAA-VSiNW pMOSFET with BF$_2$-doped poly-gate and S/D regions

5.3.1 Output and Transfer Electrical Characterization

Figure 5.4 illustrates the $I_{DS} – V_{GS}$ and $I_{DS} – V_{DS}$ characteristics of the GAA-VSiNW pFET with BF$_2$-doped poly-gate and S/D. The gate length (L_G) is ~ 100 nm, the SiNW height and diameter are about 300 nm and 23 nm, respectively. It is worthwhile to note that the wire tip is used as drain (D) and substrate side is used as source (S) during the device measurement.

Figure 5.4 (a) shows the $I_{DS} – V_{GS}$ curve of the fabricated GAA-VSiNW pFET. Due to the band bending of valence and conduction bands, high drive current is observed with increasing negative V_G region and low current in the positive V_G region. This electrical behavior is characteristic of enhancement mode pFET with p^+ gate and S/D.

The fabricated device showed an extremely low DIBL of ~ 9 mV/V, measured at 0.1 nA and sub-threshold swing of ~ 66 mV/decade at V_{DS} = -1.2V. The sub-threshold swing is very close to the theoretical predicted value of 60mV/decade [5.9]. I_{on} of ~ 113 µA/µm is achieved at V_{DS} = -1.2V and V_{GS} = -2V while I_{off} of ~ 0.1 µA/µm is obtained at V_{DS} = -1.2V and V_{GS} = 2V. The I_{on}/I_{off} ratio, measured at V_{DS} = -0.2V, is ~ 10^7 and the fabricated device V_T is ~ 0.832V. This positive V_T is undesirable and is due to the work-function mis-match between the gate and the intrinsic VSiNW body. Optimal V_T can be achieved using the technique detailed in Section 5.3.3.

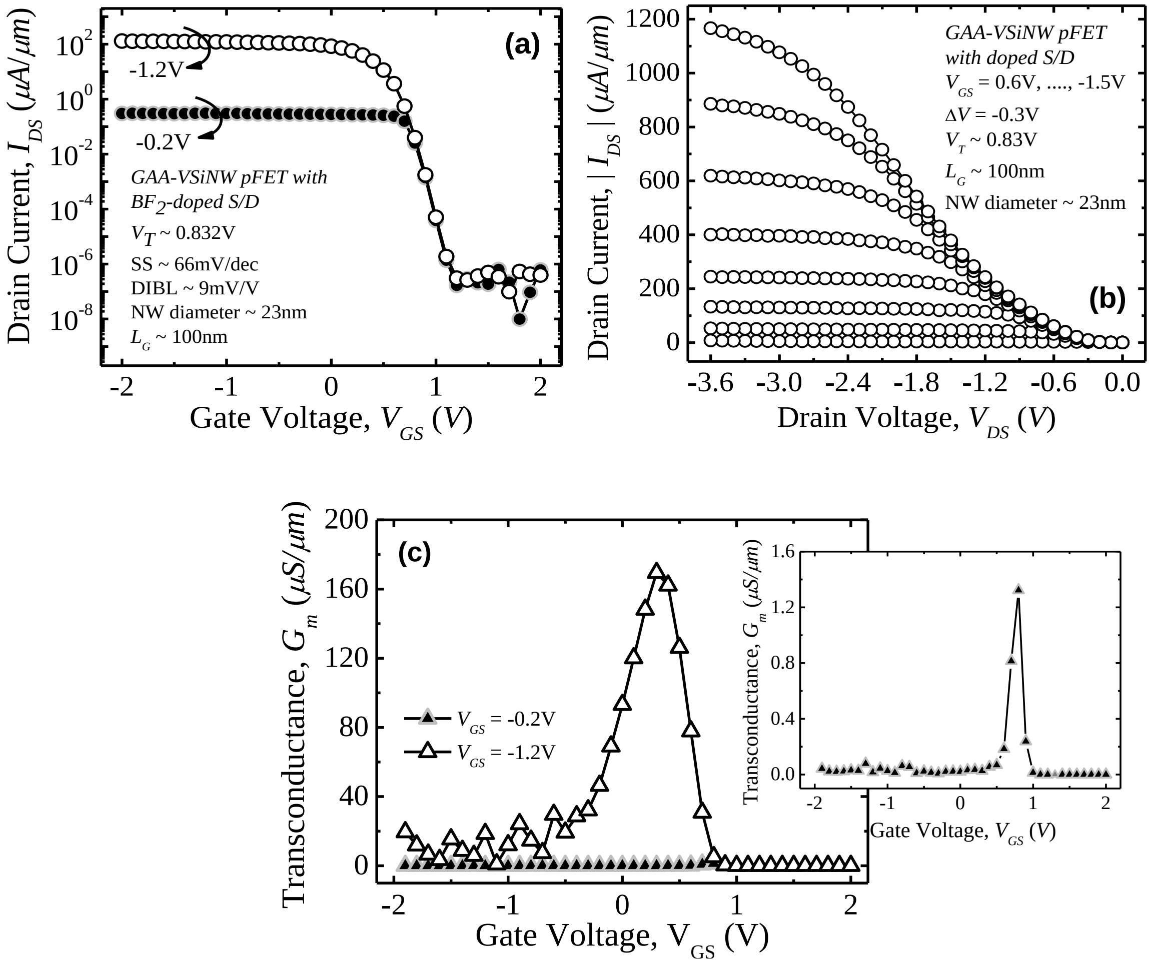


Figure 5.4 (a) I_{DS} – V_{DS} and (b) I_{DS} – V_{GS} plots of GAA-VSiNW pMOS with BF_2-doped gate and S/D regions. Excellent SCE parameters, SS ~ 66mV/dec and DIBL ~ 9mV/V, are obtained. Extracted V_T ~ 0.832V is undesirable and can be rectified using V_T tuning methods to be introduced in later section. Despite sub-linear turn-on at low V_{DS}, there is a clear distinction between saturation and linear regions in the I_{DS} – V_{DS} plot. The extracted $G_{m,sat}$ and $G_{m.lin}$ are plotted in Figure 5.4(c).

The extracted DIBL and SS values, in our measured device, are much lower than the reported values of SS = 96mV/decade and DIBL = 25mV/V that are measured on Vertical GAA SiNW with Al_2O_3/TiN gate stack and L_G = 320 nm [5.10]. In addition, the reported I_{on} is significantly lower (11.8 µA/µm at V_{DS} = -1V and V_{GS} = -2V with 25 nanowires connected in parallel).

The lower DIBL, SS and larger I_{on} values extracted in our study can be attributed to the intrinsic channel region (~ 10^{15} cm^{-3}) in our fabricated device whereby, there is much lower ionized impurity scattering as compared to the implanted channel (~ 10^{17} cm^{-3})

reported in literature. Furthermore, better gate-to-channel electrostatic coupling is achieved in our device since much thinner gate oxide (4.5nm) is used in our study as compared to the thick Al_2O_3 layer (20nm) used in literature.

Figure 5.4 (b) plots the I_{DS} – V_{DS} characteristics of the same device. The fabricated pFET exhibits a high drive current (I_{Dsat}) of ~ 400 µA/µm measured at V_{DS} = -3V and V_{GS} = -0.6V. An upward gradual sloping super-linear turn-on with is observed in Figure 5.3(b) between V_{DS} = 0V to V_{DS} = -0.3V. In addition, the saturation region is only apparent at large V_{DS} bias (V_{DS} = ~ -1.8V). This suggests there's a high external series resistance path in the fabricated pFET due to the mis-alignment of doping regions between the source side and gate. Despite this problem, there is a clear distinction between the linear and saturation regions for all V_{GS} biases, indicating that the channel pinch-off has been reached.

This is an inherent problem with the fabrication of VSiNW MOSFETs in this study because the source (substrate side of the wire) is implanted first while the drain (wire tip) and gate regions are implanted together in the subsequent implant step. However, this issue can be resolved through process optimization.

Figure 5.3 (c) shows the extracted trans-conductance (G_m) of fabricated pMOSFET at V_{DS} = -0.2V and -1.2V. The inset presents the zoom-in view for V_{DS} = -0.2V because the G_m values are too small as compared to V_{DS} = -1.2V. The maximum G_m occurs at V_{GS} = 0.8V for V_{DS} = -0.2V and V_{GS} = 0.3V for V_{DS} = -1.2V.

5.3.2 Short-Channel Effect Characteristics

Important SCE parameters for MOSFETs are (1) DIBL (Drain-Induced Barrier Lowering), which reduces the device V_T as V_{DS} increases due to the drain-junction depletion region penetrating the channel region and causes the gate to lose control over the channel, and (2) SS (Sub-threshold swing) degradation, which reduces the rate of increase of drain current below V_T. Both effects are additive and in consequence, causes circuit power consumption and MOSFET off-state leakage current to increase. Since the fabricated pMOS L_G is fixed at 100nm, it would be interesting to illustrate the impact of nanowire diameter with regards to DIBL and SS.

Figure 5.5 (a) shows the extracted DIBL values plotted against the VSiNW diameter. For smaller nanowire diameters 20nm and 23nm, DIBL remains almost constant around 225mV/V while larger nanowire diameters 32nm and 40nm, DIBL increases almost doubly to 400mV/V. Much smaller DIBL values have been reported experimentally for GAA-VSiNW pFET with nanowire diameter = 25nm (DIBL ~ 25 mV/V) [5.11] and nanowire diameter = 8µm (DIBL ~ 72mV/V) [5.12].

The considerably higher DIBL observed in this study can be attributed to the un-optimized implantation and annealing process conditions since both gate and drain regions are implanted in a single step. This enabled the applied drain bias to influence potential barrier on the source side electric potential.

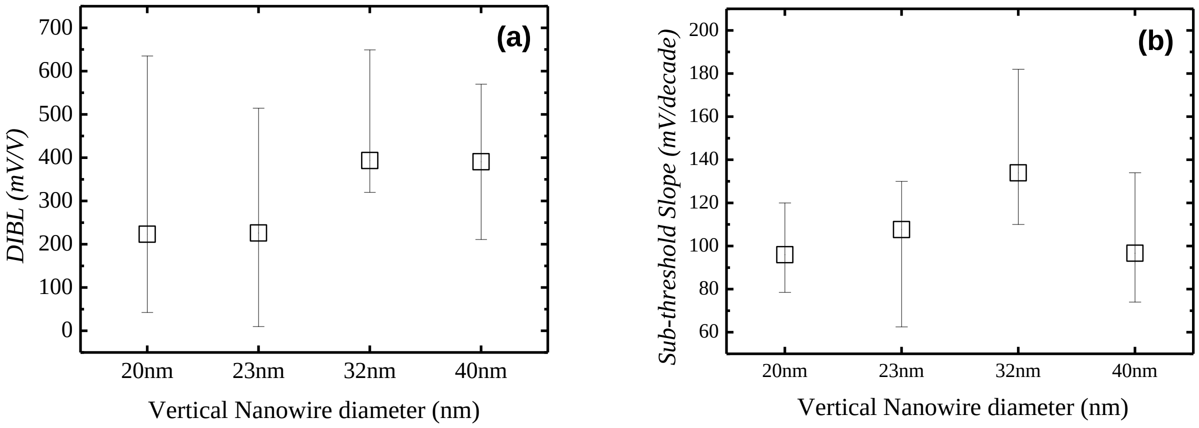


Figure 5.5 Extracted (a) DIBL and (b) Sub-threshold swing (SS) measurements plotted against VSiNW diameter. DIBL values increase ~ 2 times and SS values remain below 190mV/decade as the VSiNW diameter varies from 20nm to 40nm.

Figure 5.5(b) shows the extracted SS plotted against VSiNW diameter. The SS increases from ~ 95mV/decade to ~ 135mV/decade as the nanowire diameter increases from 20nm to 32nm. However, the SS drops to below 100mV/decade for nanowire diameter = 40nm. These SS values are comparable with those reported in conventional planar pMOS with L_G = 100nm (SS < 90mV/decade) and in GAA-VSiNW pMOS (SS ~ 85mV/decade) [5.11]. For a given L_G, it is expected that as the channel width (or nanowire diameter, in this study) increases, the gate electrostatic control over the channel weakens and hence, the SS will degrade.

5.3.3 I_{on} - I_{off} current characteristics and Threshold Voltage (V_T) tuning

Figure 5.6 (a) plots the I_{on}/I_{off} ratio against the measured VSiNW diameters. The I_{on}/I_{off} ratio shows an average value of ~ 2 x 10^8, much higher than that recorded for planar pMOS with similar L_G. High I_{on}/I_{off} ratio is expected for GAA-VSiNW FETs as the GAA architecture greatly suppresses the leakage current, thus, making GAA-VSiNW a much promising candidate for ultra-low leakage applications.

Figure 5.6 (b) illustrates the I_{off} vs I_{on} characteristics of GAA-VSiNW pMOS with BF_2-doped poly-gate and S/D. Also included in Figure 5.6 (b) are the I_{off} vs I_{on} characteristics of reported SiNW devices. At $I_{off} = 10^{-3}$ µA/µm, the drive current of fabricated pMOS devices in this study is ~ 3 times lower than reported lateral SiNW devices but ~ 50 times higher than reported VSiNW devices. The reason for the reduced I_{on} is believed to be the result of (1) VSiNW sidewall roughness (shown in Figure 5.3) or (2) high external series resistance present in device due to mis-alignment between the source dopant profile and gate. Fortunately, issue (1) can be resolved via sequential hydrogen annealing followed by high-temperature annealing and issue (2) can be mitigated by implanting the gate and S/D regions concurrently which involves process step modification.

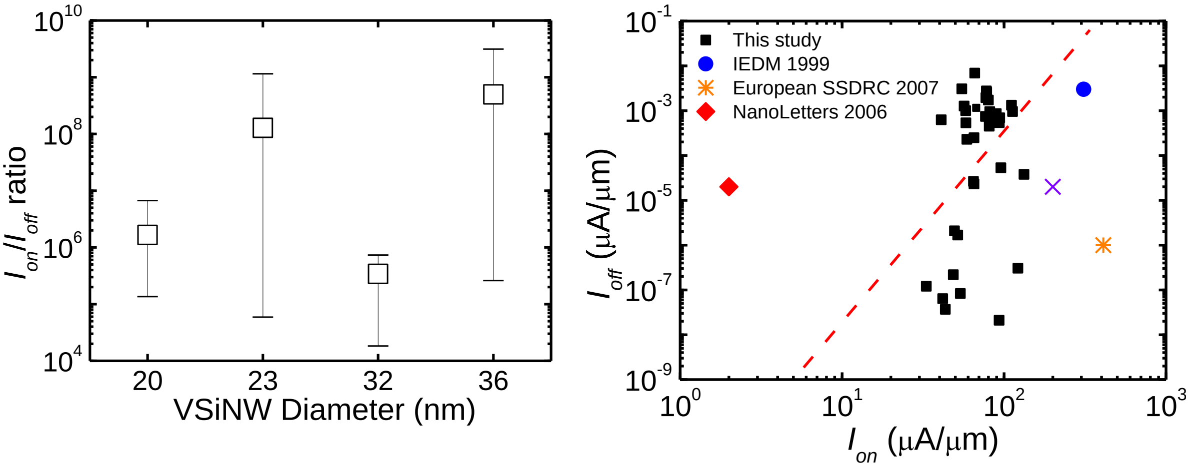


Figure 5.6 (a) I_{on}-I_{off} ratio of GAA-VSiNW pMOS with various diameters and (b) Ioff vs Ion characteristics of GAA-VSiNW pMOS compared with reported devices.

In previous section 5.3.1, the measured pMOSFET shows a V_T of ~ 0.832V, which is undesirable as this signifies that the device will not “turn-off” until $V_{GS} > 0.832$V is applied to the gate. In terms of an inverter circuit, this leads to smaller static noise margin (SNM) since the voltage noise margins become smaller and the circuit will start to lose noise immunity which results in higher power consumption. Hence, it is imminent to tune the pMOSFET V_T in order to achieve a large SNM.

Figure 5.7 shows the variation of pMOSFET threshold voltage (V_T) with respect to the different vertical nanowire diameter used to fabricate the device. V_T is extracted from the $I_{DS} - V_{GS}$ measurement data using the trans-conductance extrapolation method in the linear region (GMLE).

From the plot, it is observed that the device V_T generally decreases with increasing nanowire diameter size. This observation implies that the device V_T can be tuned to the desired value range without additional fabrication processes or materials and V_T tuning can be achieved simply by changing the nanowire size. This provides an additional invaluable benefit for GAA-VSiNW architecture to the numerous advantages discussed earlier.

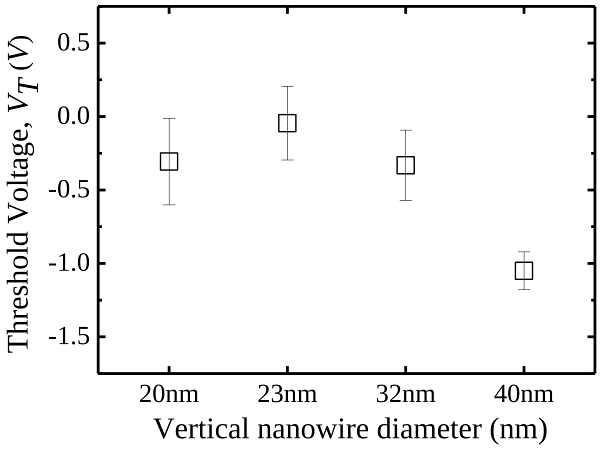


Figure 5.7 Threshold Voltage (V_T) variation across the various VSiNW diameters fabricated in this work. In general, the extracted V_T shows a decreasing trend when the VSiNW diameter increases from 20 nm to 40 nm.

5.4 GAA-VSiNW nMOSFET with Phosphorus-doped poly-gate and S/D regions

5.4.1 Output and Transfer Electrical Characterization

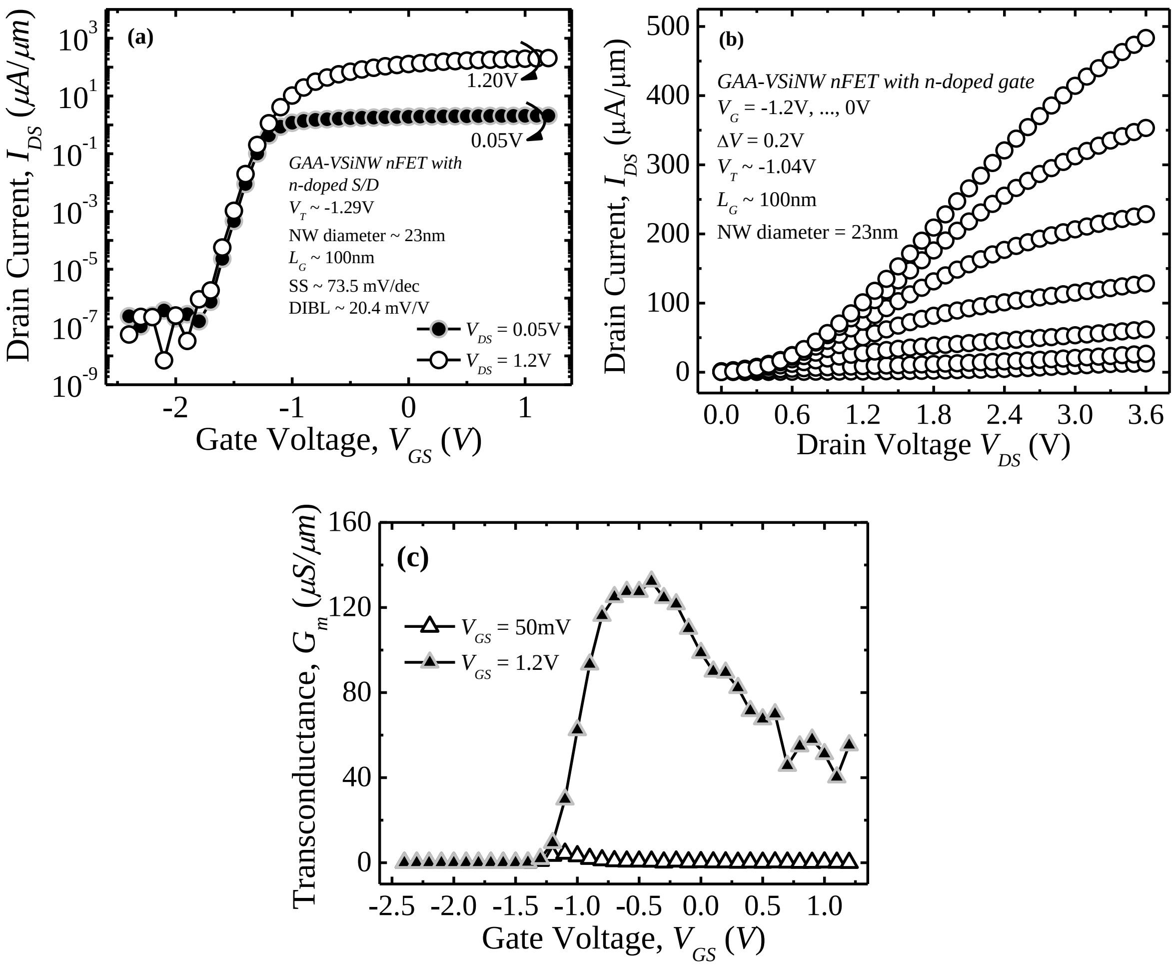


Figure 5.8 (a) I_{DS} – V_{DS} and (b) I_{DS} – V_{GS} plots of GAA-VSiNW nMOS with As-doped gate and S/D regions. Excellent SCE parameters, SS ~ 66mV/dec and DIBL ~ 9mV/V, are obtained. Extracted V_T ~ -1.29V is undesirable and can be rectified using V_T tuning methods to be introduced in later section. Despite sub-linear turn-on at low V_{DS}, there is a clear distinction between saturation and linear regions in the I_{DS} – V_{DS} plot. The extracted $G_{m,sat}$ and $G_{m.lin}$ are plotted in Figure 5.8(c).

Figure 5.8 presents the output, transfer and trans-conductance characteristics of GAA-VSiNW nMOSFET with As-doped poly-gate and S/D regions. The gate length is ~ 100nm, the SiNW height and diameter are ~ 300nm and ~ 23nm, respectively. The I_{DS} – V_{GS}

curve in Figure 5.8 (a) demonstrates typical output characteristics of enhancement mode nMOS with high I_{on} for positive V_{GS} and low I_{off} for negative V_{GS}.

In addition, the fabricated nMOS exhibits DIBL of 20.4mV/V and SS of 73.5mV/dec. These values are comparable with those reported by H. S. Wong et. al. The I_{on}/I_{off} ratio for this measured device is ~ 10^7 at V_{DS} = 50mV and the extracted V_T is ~ -1.29V. The negative V_T measured is undesirable for nMOS and can be attributed to the work function mis-match between the VSiNW body and the poly-gate. Optimal V_T can be achieved using the techniques detailed in Section 5.4.3.

Figure 5.8 (b) shows the $I_{DS} – V_{DS}$ plot for the measured nMOS. The device exhibits saturation current (I_{Dsat}) of ~ 300 µA/µm at V_{DS} = 3V and V_{GS} = -0.2V. An upward gradual sloping sub-linear turn-on is observed, similar to the results from GAA-VSiNW pMOS in Section 5.3.1. This can be attributed to the existence of a high external series resistance path due to the source dopant profile mis-alignment between poly-gate and source regions. However, there is a clear presence of linear and saturation regions for low V_{GS} biases, indicating that the channel pinch-off has been reached. Figure 5.8 (c) illustrates the measured trans-conductance (G_m) of the fabricated nMOS. The maximum G_m of 135µS/µm is achieved at V_{GS} = -0.3V for V_{DS} = 1.2V.

5.4.2 Short-Channel Effect Characteristics

Figure 5.9 illustrates the short-channel characteristics of GAA-VSiNW nMOSFET with n-doped poly-gate and S/D regions. As shown in Figures 5.9 (a) and (b), DIBL and SS values demonstrated an increase trend with increasing VSiNW diameter. The lowest DIBL and SS values extracted are ~ 6mV/V and ~ 70mV/decade, respectively. Similar DIBL (15mV/V) and SS (75 mV/decade) values are reported for lateral NW nMOSFETs with poly-Si/SiO2 gate stack (yy) and metal/high-κ gate stacks. Larger DIBL and SS values are expected for VSiNW with larger diameters since the gate electric field coupling to the channel weakens.

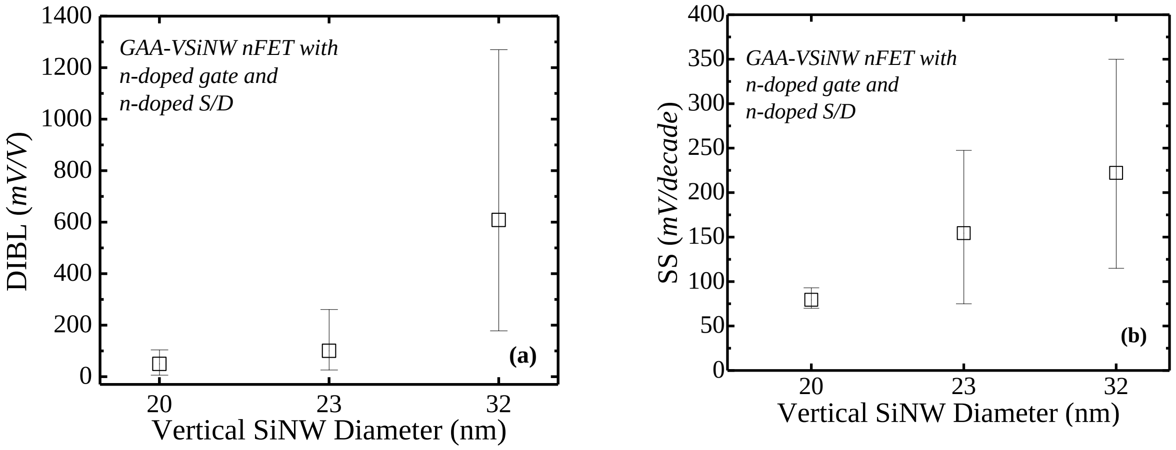


Figure 5.9 (a) DIBL distribution of GAA-VSiNW nMOS with various diameters The lowest value is ~ 6mV/V and (b) SS distribution of GAA-VSiNW nMOS with various diameters. The lowest value is ~ 70 mV/decade.

5.4.3 I_{on} - I_{off} current characteristics and V_T tuning

Figure 5.10 illustrates the I_{on} vs. I_{off} characteristics of the measured devices with various VSiNW diameters. Included in the diagram are some reported I_{on} and I_{off} values for nMOSFETs with planar, GAA-VSiNW and lateral SiNW with GAA architectures. The I_{on} values of GAA-VSiNW nMOSFET fabricated in this study are much higher than 2 of the reported devices. The reason for much higher I_{on} values is believed to be a result of reduced Columbic scattering due to a close-to-fully depleted channel region enabled by GAA design.

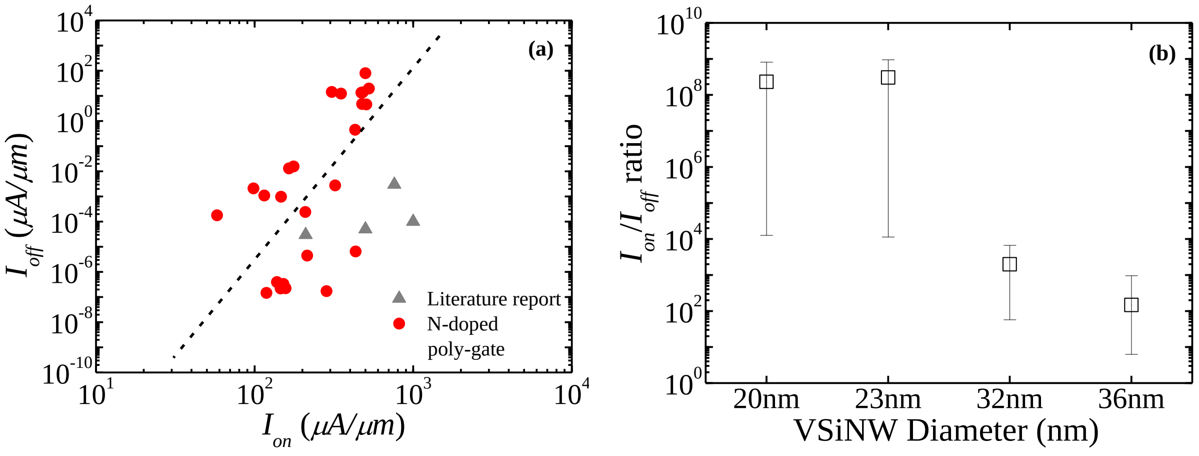


Figure 5.10 (a) I_{off} vs I_{on} characteristics of GAA-VSiNW nMOS fabricated in this study. Results from literature are also included. (b) I_{on}/I_{off} ratio of GAA-VSiNW nMOS measured in this study. Bigger diameter VSiNW shows lower I_{on}/I_{off} ratios than smaller diameter VSiNWs.

From Section 5.4.1, the measured nMOS shows a negative V_T which is undesirable for circuit operation. In this section, 2 methods are studied to tune or optimize the device V_T. The first method makes use of the various VSiNW diameter size while the second method employs the change of gate dopant type. Figure 5.11 (a) shows the V_T box plot of measured doped GAA-VSiNW nMOS with n^+ - polysilicon gate for various VSiNW diameters (Method 1). The results indicate that the device V_T decreases from ~ -0.9V to ~ -2.7V as the diameter of VSiNW increases from 20nm to 36nm. ΔV_T ranges from ~ 0.3V to 1V across the measured VSiNWs. With bigger VSiNW diameter, larger V_T is required to fully deplete and invert the SiNW body. Similar to GAA-VSiNW pMOS in Section 5.3.3, the desired device V_T can be easily achieved by changing the diameter of VSiNW. This simplifies the overall fabrication process and significantly reduces fabrication cost.

An alternative option to tune V_T is to switch the gate dopant species from Phosphorus (n-type) to BF_2 (p-type). Figure 5.11 (b) shows the V_T comparison of measured devices with n^+ - polysilicon vs. p^+ - polysilicon gates for various VSiNW diameters (Method 2). From the measurements, the V_T of GAA-VSiNW nMOS with BF_2-doped polysilicon gate exhibits a positive shift of ~ 1.5V as compared to Phosphorus-doped polysilicon gate for all the VSiNW diameters measured. A plausible reason for the positive V_T shift is that the work function difference between p-type and n-type polysilicon gate, which is larger than 1.1 eV.

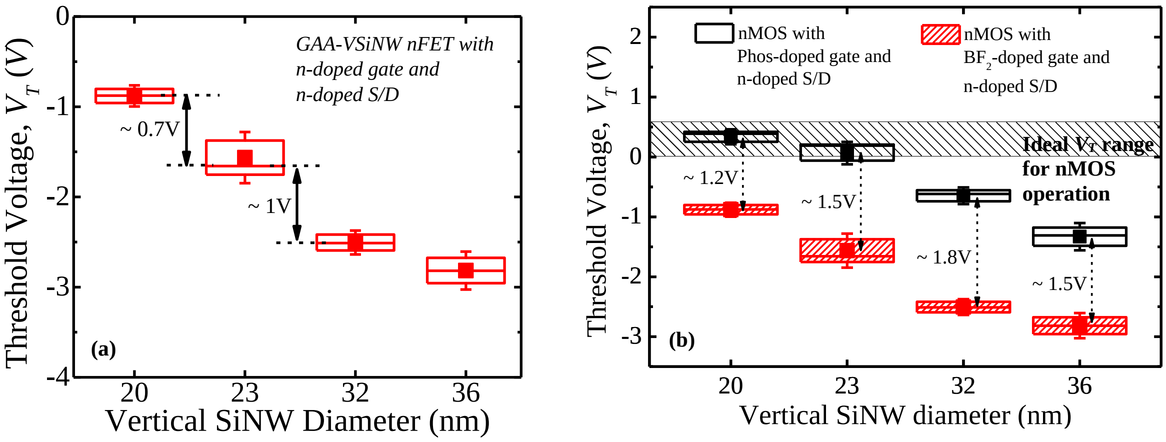


Figure 5.11 (a) Threshold Voltage (V_T) distribution of GAA-VSiNW nMOS fabricated in this study. Smaller diameter VSiNW attains less negative V_T and larger diameter VSiNW achieves more negative V_T. Δ V_T between measured devices varies from 0.3V to 1V. (b) A positive shift in V_T distribution for all the measured GAA-VSiNW nMOS accomplished using BF_2-doped poly-gate instead of As-doped poly-gate. The ideal V_T range for normal nMOS operation is included/

5.5 Electrical characteristics comparison between GAA-VSiNW nMOS with p^+ - polysilicon gate vs GAA-VSiNW nMOS with n^+ - polysilicon gate

5.5.1 Output and transfer characteristics

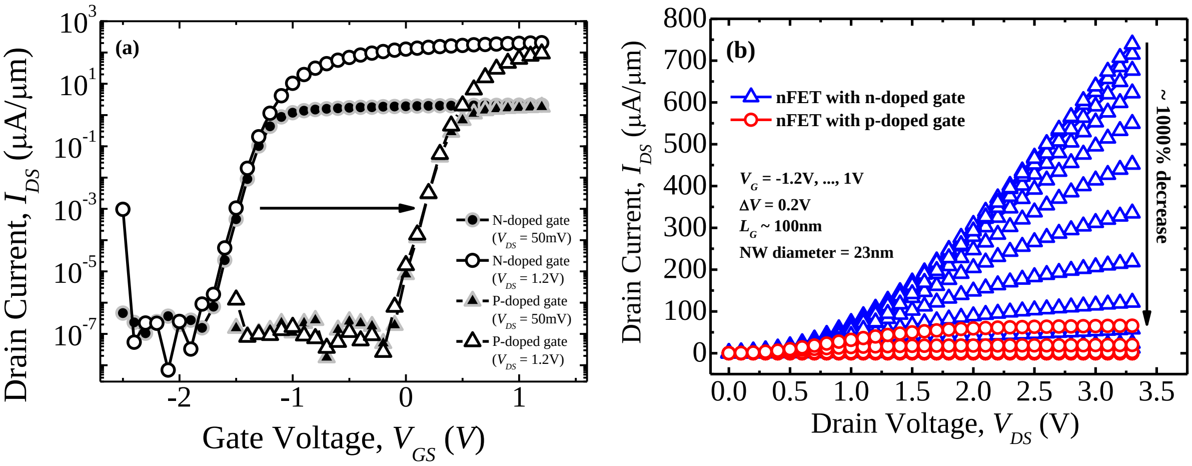


Figure 5.12 (a) I_{DS} - V_{GS} graph of GAA-VSiNW nMOS with BF_2-doped poly-gate and As-doped poly-gate. Devices with BF_2-doped poly-gate showed a positive shift of +1.5V. The I_{DS} - V_{DS} graphs of GAA-VSiNW nMOS devices with As-doped poly-gate and BF_2-doped poly-gate are shown in (b) and (c), respectively.

From Section 5.4.3, there are 2 plausible methods to tune/optimize the nMOS V_T value. A combination of the 2 proposed methods is able to achieve the ideal V_T range for nMOS operation. Figure 5.12 (a) compares the I_{DS} – V_{GS} characteristics between GAA-VSiNW nMOS devices with BF_2-doped poly gate and Phosphorus-doped poly gate (VSiNW diameter = 23nm, L_{gate} = 100nm) and Figures 5.12 (b) shows the corresponding I_{DS} – V_{DS} curves of the same measured devices. From Figure 5.12 (a), there is a +1.5V rightward shift in the slope of the I_{DS} - V_{GS} curve which corresponds well with the ΔV_T value shown in Figure 5.11 (b). From Figure 5.12 (b), there is a distinct drop in I_{DS} (~ 1000% decrease) between the two device types. This observation is expected due to the increase in V_T (+ 1.5V) as a result of opposite doped poly-gate. Furthermore, the I_{off} value remains constant at ~ 10^{-7}

µA/ µm for both types of nMOS. This implies that the change in gate doping species has no impact on the leakage current.

5.5.2 Short-Channel Effect Characteristics

Figure 5.13 compares the (a) SS and (b) DIBL values between GAA-VSiNW nMOS with n^+ vs. p^+ - polysilicon gate. From the comparison results, GAA-VSiNW nMOS with p^+ - polysilicon gate and n^+ - polysilicon gate exhibited similar SS and DIBL values for VSiNW diameter = 20nm. However, for bigger VSiNW diameters, GAA-VSiNW nMOS with p^+ - polysilicon gate showed significantly lower SS and DIBL values than those with n^+ - polysilicon gate.

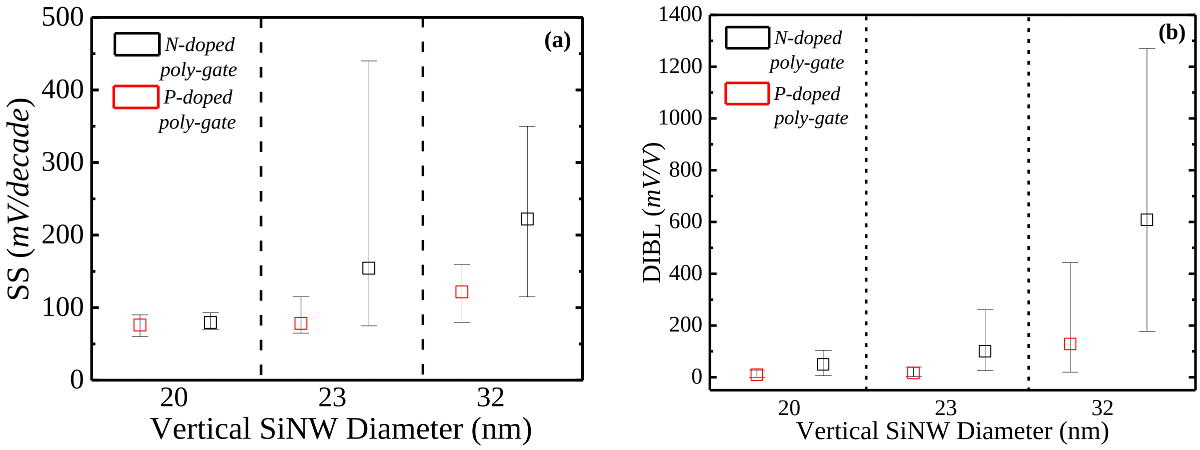


Figure 5.13 (a) SS comparison between GAA-VSiNW nMOS with n^+-polysilicon gate vs p^+-polysilicon gate. GAA-VSiNW nMOS with p^+-polysilicon gate showed lower SS values than its counterpart. (b) illustrates the DIBL comparison of the same devices in (a). Similarly, devices with p^+-polysilicon gate showed lower values than its opposition.

A plausible reason is with the penetration of B atoms into the channel region, the barrier height between the source and channel increases and causes DIBL values in devices with p+ - polysilicon gate to be lower than those of n+ - polysilicon gate. Moreover, the channel N_A (acceptor ion) concentration will increase and reduce C_{dep} (depletion capacitance). This will result in lower SS values, as shown in Eqns (2) and (3). Hence, the integration of BF_2 - doped polysilicon gate with GAA-VSiNW nMOS will bring about reduction in both SS and DIBL.

$$C_{dep} = \frac{\varepsilon_{Si}}{W_{dep}} \propto \sqrt{\frac{1}{N_A}} \quad [\boldsymbol{Eqn\ 5.1}]$$

$$S \equiv n\left[\frac{kT}{q}\right]\ln(10) \quad [\boldsymbol{Eqn\ 5.2}]$$

$$where\ n = 1 + \frac{C_{dep}}{C_{ox}}$$

5.5.3 I_{on} - I_{off} Characteristics

Figure 5.14 shows the I_{off} vs I_{on} characteristics of GAA-VSiNW nMOS with n^+- and p^+-polysilicon gate. It is observed that at I_{off} = 1nA/µm, I_{on} of GAA-VSiNW nMOS with p^+-polysilicon gate increases by 50% as compared to the same nMOS devices with n^+-polysilicon gate. In addition, results from literature are included for reference. The devices in our study are yet to be fully optimized but our results are comparable with some of the reported SiNW cases.

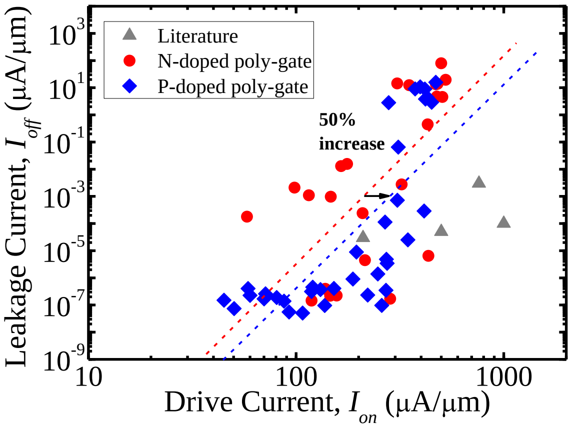


Figure 5.14 I_{off} vs I_{on} characteristics of GAA-VSiNW nMOS with n^+-doped (●) and p^+-doped poly-gate (◆). At I_{off} = 1nA/µm, I_{on} of nMOS with p^+-doped poly-gate increases by 50%.

5.5 Chapter Summary

We have fabricated pMOSFET and nMOSFET via GAA-VSiNW architecture. For GAA-VSiNW pMOS with diameters 20nm to 23nm, the extracted DIBL is ~ 225mV/V and it increases to ~ 400mV/V for VSiNW with larger diameters 32nm to 40nm. The corresponding SS values increase from ~ 95mV/decade to ~ 135mV/decade as the nanowire diameter increases from 20nm to 32nm but the SS value of pMOS with diameter of 40nm drops below 100mV/decade. We have also showed that our fabricated pMOS achieves 50 times higher drive current (I_{on}) than reported VSiNW devices at fixed I_{off} = 1nA/µm. Furthermore, pMOS V_T tuning is also demonstrated. V_T tuning is achieved through varying the VSiNW diameter with bigger VSiNW having more negative V_T as compared to smaller VSiNW.

Excellent electrical characteristics (I_{on}/I_{off} ratio of > 10^8, DIBL = 6mV/V to 104mV/V, SS = 70mV/decade to 93 mV/decade) are achieved by GAA-VSiNW nMOS with diameter = 20nm. Apart from this, negative V_T values are extracted from the fabricated nMOS devices. Reducing VSiNW diameter helped to create a positive shift in V_T but there is a limit to how small the nanowire diameter can get. Alternatively, implanting the poly-gate with p^+ dopants instead of n^+ dopants will produce a larger positive shift in V_T than reducing VSiNW diameter. Hence, we showed that V_T tuning for nMOS is achievable through two methods.

Lastly, GAA-VSiNW nMOS with p^+-doped poly-gate showed better electrical characteristics (I_{on}/I_{off} ratio of > 10^8, DIBL = 4mV/V to 28mV/V, SS = 65mV/decade to 90 mV/decade) as compared to GAA-VSiNW nMOS with n^+-doped poly-gate. In addition, at fixed I_{off} = 1nA/µm, GAA-VSiNW nMOS with p^+-doped poly-gate demonstrated 50% higher drive current than GAA-VSiNW nMOS with n^+-doped poly-gate.

5.6 References

[5.1] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High Performance Silicon Nanowire Field Effect Transistors," *Nano Letters*, vol. 3, pp. 149 - 152, 2003.

[5.2] Y. Fu-Liang, C. Haur-Ywh, C. Fang-Cheng, C. Yi-Lin, Y. Kuo-Nan, C. Chih-Jian, et al., "35 nm CMOS FinFETs," in *VLSI Technology, Digest of Technical Papers*. 2002 Symposium on, 2002, pp. 104-105.

[5.3] S. Sung Dae, L. Sung-Young, K. Sung-Min, Y. Eun-Jung, K. Min-Sang, L. Ming, et al., "High performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET) : fabrication on bulk si wafer, characteristics, and reliability," in *Electron Devices Meeting*, 2005. *IEDM Technical Digest*. IEEE International, 2005, pp. 717-720.

[5.4] S. Bangsaruntip, G. M. Cohen, A. Majumdar, Y. Zhang, S. U. Engelmann, N. Fuller, et al., "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," in *Electron Devices Meeting (IEDM)*, 2009 IEEE International, 2009, pp. 1-4.

[5.5] B. S. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, et al., "High performance fully-depleted tri-gate CMOS transistors," *IEEE Electron Device Letters*, vol. 24, pp. 263-265, 2003.

[5.6] Y. Jiang, T. Y. Liow, N. Singh, L. H. Tan, G. Q. Lo, D. Chan, et al., "Nanowire FETs for low power CMOS applications featuring novel gate-all-around single metal FUSI gates with dual fm and VT tune-ability," in *Electron Devices Meeting*, 2008. *IEDM* 2008. IEEE International, 2008, pp. 1-4.

[5.7] N. Singh, F. Y. Lim, W. W. Fang, S. C. Rustagi, L. K. Bera, A. Agarwal, et al., "Ultra-Narrow Silicon Nanowire Gate-All-Around CMOS Devices: Impact of Diameter, Channel-Orientation and Low Temperature on Device Performance," in *Electron Devices Meeting*, 2006. IEDM '06. International, 2006, pp. 1-4.

[5.8] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, et al., "High-performance fully depleted silicon nanowire (diameter ≤ 5 nm) gate-all-around CMOS devices," *Electron Device Letters, IEEE*, vol. 27, pp. 383-386, 2006.

[5.9] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *Electron Device Letters, IEEE*, vol. 18, pp. 74-76, 1997.

[5.10] Z. Yujia, L. Mathew, R. Rao, M. Palard, S. Chopra, J. G. Ekerdt, et al., "High-Performance Vertical Gate-All-Around Silicon Nanowire FET With High-k/Metal Gate," *Electron Devices, IEEE Transactions* on, vol. 61, pp. 3896-3900, 2014.

[5.11] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong, "Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET," *IEEE Electron Device Letters*, vol. 29, p. 4, 2008.

[5.12] H. Takato, K. Sunouchi, N. Okabe, A. Nitayama, K. Hieda, F. Horiguchi, et al., "High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs," in *Electron Devices Meeting*, 1988. IEDM'88. Technical Digest., International, 1988, pp. 222-225.

CHAPTER 6
DEMONSTRATION OF SCHOTTKY BARRIER MOSFET USING VSiNW ARCHITECTURE

6.1 Introduction

In Chapter 5 we have successfully demonstrated NMOSFET and PMOSFET with excellent electrical performance using VSiNW architecture. The fabricated transistors have un-optimized V_T values and V_T tuning is achieved through varying VSiNW diameter and/or implanting gate region with opposing dopant species with respect to S/D regions. However, the extracted I_{on} for n- and PMOSFETs are lower than literature reports for nanowires at fixed I_{off} = 1nA/µm.

In order to improve I_{on}, two requirements need to be fulfilled: (i) low S/D sheet resistance and (ii) abrupt junction within S/D regions. Schottky Barrier (SB) MOSFET is one of the promising options whereby metalized S/D regions are in direct contact with transistor channel can reduce parasitic resistance significantly and provide abrupt junction interfaces.

While work on lateral nanowire with nickel silicidized S/D has been investigated, integration of nickel silicide (Ni_xSi_y) into VSiNW and its impact on transistor's performance by method of conventional lithography has not been well studied. In this chapter, we aim to demonstrate the feasibility of achieving GAA-VSiNW MOSFET with Ni_xSi_y S/D regions (GAA-VSiNW SB MOSFET) and extract the respective electrical characteristics.

6.2 Experimental Details

In this chapter, the devices under study are: (i) GAA-VSiNW SB PMOS with tuned FUSI gate and (ii) GAA-VSiNW SB NMOS with tuned FUSI gate. In addition, V_T tuning splits will be done using GAA-VSiNW SB NMOS. The fabrication process details for the devices studied in this chapter had been outlined in Section 3.4.2 in Chapter 3.

GAA-VSiNW SB MOSFETs with tuned FUSI gate were fabricated on single VSiNWs with height ~ 300nm, gate length (L_{gate}) ~ 100nm and varying diameters (from 20nm to 60nm). The VSiNW tip and wafer substrate will serve as the drain (D) and source (S) regions, respectively. To attain tuned FUSI gate, 50nm poly-Si was deposited via Chemical Vapour Deposition (CVD) method on top of an isolation oxide spacer layer that separates the gate and source, followed by BF_2 implantation (5 KeV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations) for PMOS and Phosphorus implantation (5 KeV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations) for NMOS and RIE etch to expose VSiNW tip.

Subsequently, 30nm Ni was deposited using Physical Vapour Deposition (PVD) after SC1 wet clean. Following nickel deposition, a 2-step RTA process was used to form nickel mono-silicide (NiSi) on the gate and S/D regions. Finally, electrical contacts to S/D and gate regions are done through patterned metal layers consisting of TaN/Al/TaN layers.

Due to the complexity of gate last process and the risk of metal cross contamination between different process equipment used during the VSiNW transistor fabrication, the gate first process is adopted but a drawback of this process is the formation of asymmetrical SB S/D regions. In order to achieve low substrate resistivity, the substrate is subjected to a pre-implant step with high dose and low implant energy before the Ni deposition. Unless specified otherwise, the devices studied in this chapter will consist of doped FUSI gate and asymmetrical SB S/D regions.

For the V_T tuning splits, the gate implant conditions are shown in the table below. GAA-VSiNW NMOS is chosen as the test vehicle for the V_T tuning study because from literature, the V_T value for GAA-VSiNW FETs tends to be negative.

Device	**Implant conditions**
GAA-VSiNW Schottky NMOS (control)	P/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations
GAA-VSiNW Schottky NMOS (tuned V_T)	BF_2/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations

Table 6.1 List of gate implant conditions for V_T tuning splits to be used in conjunction with GAA-VSiNW SB NMOS

6.3 Physical Characterization

Figure 6.1 (a) shows the TEM (Transmission Electron Micrograph) image of a single GAA-VSiNW SB MOSFET with contact metal layers taken using low magnification. Figure 6.1 (b) shows the same TEM image taken using higher magnification. The VSiNW height (269.2nm) and diameter (~ 47nm) and the thickness of the bottom isolation oxide layer (~ 28 nm) are also measured. Different VSiNW diameters (from 20nm to 80nm) were fabricated in this study but for ease of TEM sample preparation, a large diameter was chosen.

It is evident in Figure 6.1 (a) that the silicide-silicon interface in the Si substrate is right below the edge of the gate region and there is no sign of nickel silicide intrusion beneath the gate region or into the VSiNW bottom in Figure 6.1 (b). From the dark contrast labelled as Ni_xSi_y intrusion in Figure 6.1 (b) the VSiNW tip is fully silicidized. This observation demonstrates the S/D regions of the fabricated transistor is silicidized asymmetrically and correlates well with the fabrication process. Also shown in Figure 6.1 (b), the silicide-silicon interface in the VSiNW is not align to the edge of the gate region. Coupled with the lack of un-silicidized VSiNW bottom, fabricated SB transistor will have low drive current due to large internal resistance.

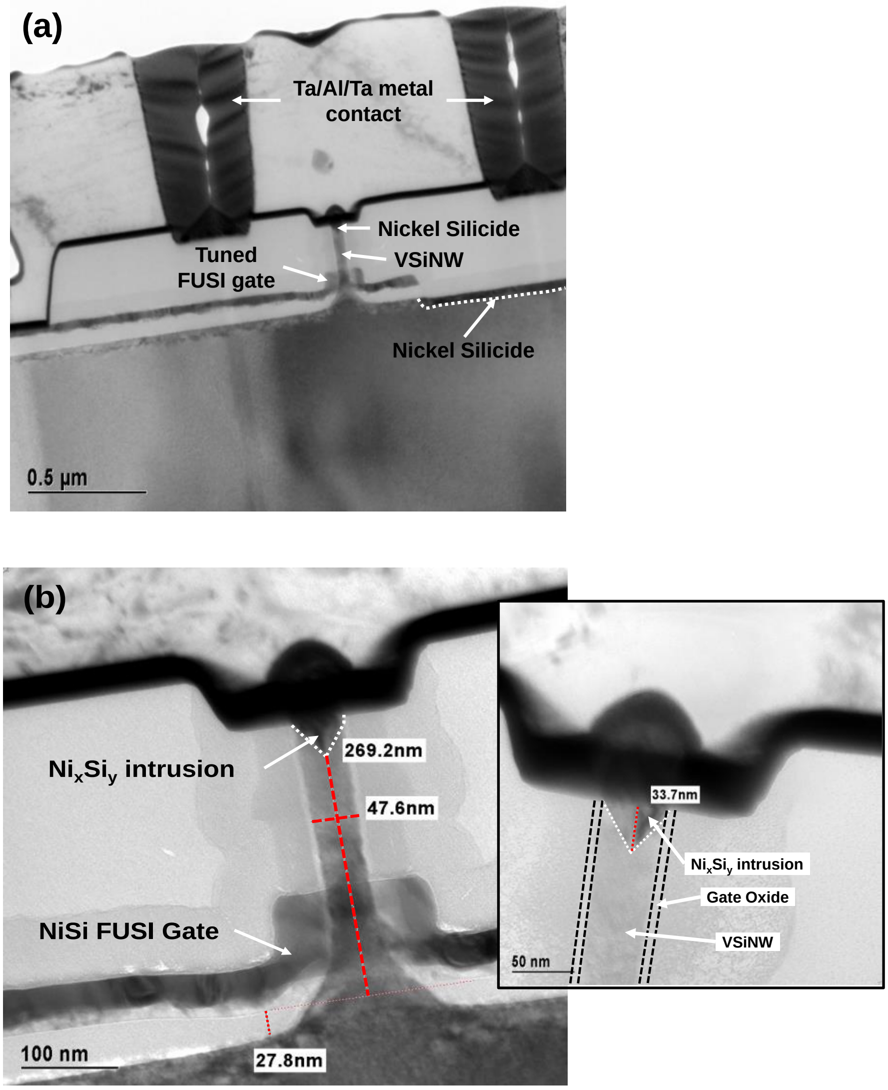


Figure 6.1 Cross-sectional TEM image showing the GAA-VSiNW SB MOSFET (diameter ~ 48nm) with metal layers for probing. Gate oxide is ~ 5nm and Ni_xSi_y intrusion length is ~ 34nm. Bottom isolation oxide layer thickness is ~ 28nm. The gate region is observed to be fully-silicidized.

6.4 GAA-VSiNW Schottky barrier PMOSFET

6.4.1 Output and Transfer Electrical Characterization

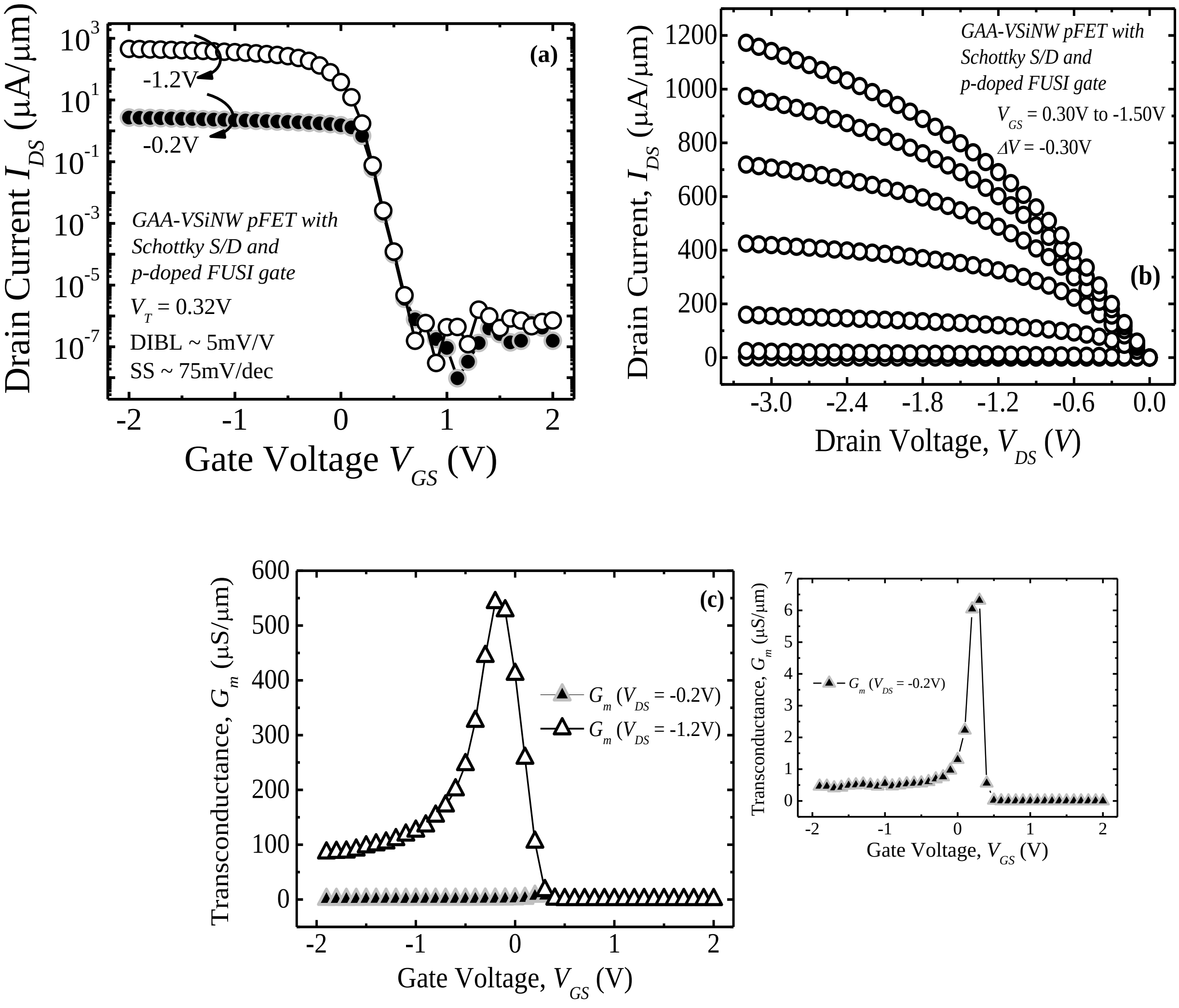


Figure 6.2 (a) I_{DS} – V_{GS}, (b) I_{DS} – V_{DS} and (c) G_m of GAA-VSiNW SB PMOS.

Figure 6.2 (a) shows the I_{DS} – V_{GS} curve of the fabricated GAA-VSiNW SB PMOSFET with p-doped FUSI gate. During measurement, gate voltage of ± 2V and drain voltage of -1.2V and -0.2V are applied to the device under test while the source is maintained at 0V. It is worthwhile to take note that the VSiNW tip is denoted as ‘Drain’ and the VSiNW bottom is denoted as ‘Source’.

High drive current (~ 650 µA/µm at V_{DS} = -1.2V, V_{GS} = -2V) is observed in the negative V_G region and low leakage current (~ 10^{-6} µA/µm at V_{DS} = -1.2V, V_{GS} = +2V) in the positive V_G region. These features are very similar to those of doped S/D PMOSFET instead of the ambipolar characteristics of SB-MOSFET, due the asymmetrical SB S/D regions mentioned in Section 6.2. The Drain-Induced Barrier Leakage (DIBL) is ~ 5mV/V and sub-threshold swing (SS) is ~ 75mV/decade. The excellent SCE characteristics are attributed to the Gate-All-Around structure and the thin gate oxide thickness of 5nm which enhance the gate electrostatic control. The I_{on}/I_{off} ratio, measured at V_{DS} = -200mV, is ~ 2 x 10^8 and V_T is ~ 0.32V.

The I_{DS} - V_{DS} characteristics in Figure 6.2 (b) shows the absence of an upward sloping sublinear turn-on due to the low Φ_{beff}. In most SB MOSFET, the upward sloping sublinear turn-on behavior can be found in their I_{DS} - V_{DS} characteristics. There is also clear presence of linear and saturation regions for all V_{GS} biases, indicating that channel pinch-off has been reached.

Figure 6.2 (c) shows the extracted trans-conductance (G_m) of the fabricated device at V_{DS} = -0.2V and -1.2V. The inset presents the zoom-in view for V_{DS} = -0.2V because the G_m values are too small as compared to V_{DS} = -1.2V. Maximum G_m of ~ 550 µS/µm is achieved at V_{GS} = -0.25V for V_{DS} = -1.2V. Compared to GAA-VSiNW PMOS with doped S/D, for V_{DS} = -1.2V, the maximum G_m for GAA-SB PMOS is ~ 3 times higher. This is expected since at the same V_{GS}, the drive current for GAA-VSiNW SB-PMOS is higher than that of GAA-VSiNW with doped S/D.

Based on literature, SB transistors should exhibit ambipolar behavior whereby the drain current I_{DS} attains the similar magnitude level regardless of the applied V_{GS}. This is attributed to the near mid-gap SBH of NiSi-silicided S/D regions due to Fermi level pinning, which has a SBH of 0.67eV for electrons and 0.45eV for holes. As shown in Figure 6.2 (a), the fabricated SB transistor does not exhibit ambipolar characteristics. The reason is due to the asymmetrical SB S/D regions inherent from the fabrication process. This could be better illustrated by the energy band diagram shown in Figure 6.3.

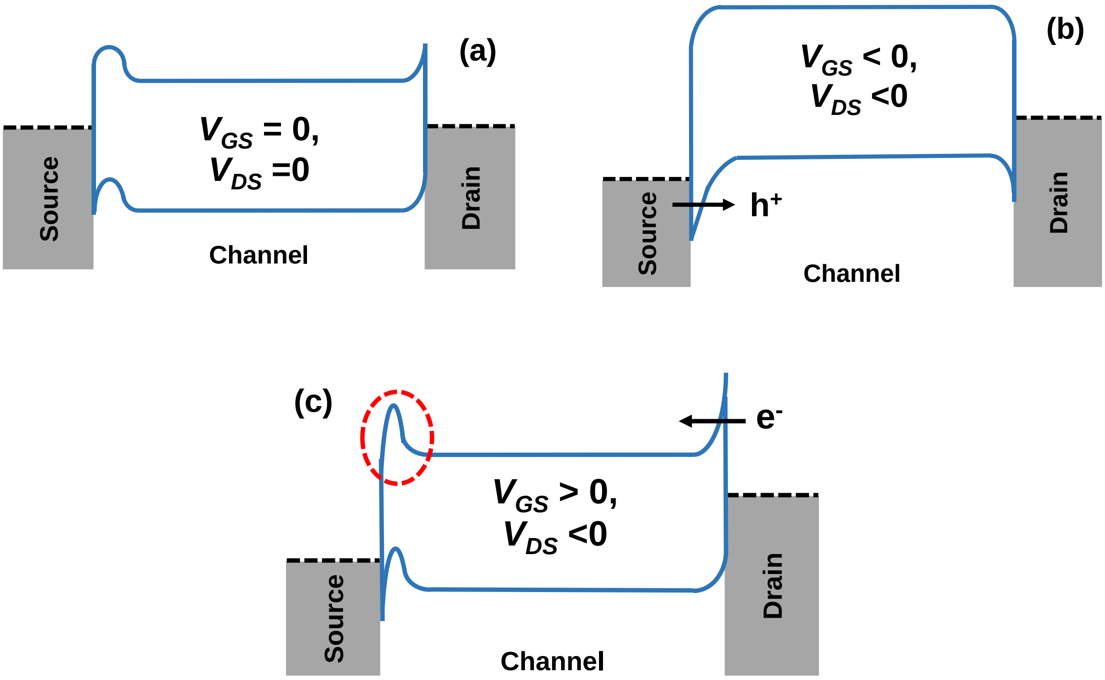


Figure 6.3 Energy Band Diagram of VSiNW SB-PMOS fabricated in this study.

Figure 6.3 (a) shows the energy band diagram of VSiNW SB-PMOS fabricated in this study without the application of external bias to the gate and drain. Due to the p-type implant at the source side, the energy band within close vicinity of the source is pushed up. At negative V_{GS}, shown in Figure 6.3 (b), the energy band is pushed up by the gate bias which leads to tunnel hole current at the source side. At the drain side, the electron Schottky barrier thickens such that there is negligible electron current at the drain side. Thus, the predominant transport carriers at this stage are holes and this is well-reflected by the high drive current I_{DS} in Figure 6.2 (a). As V_{GS} increases, the energy band is pushed downward and the Schottky barrier for holes at the source side thickens while the Schottky barrier at the drain side for electrons starts to thin down. This results in tunnel electron current at the drain side. At large positive V_{GS} in Figure 6.3 (c), the energy band is pushed further downwards and the Schottky barrier at the drain side becomes very thin which allows more electrons to tunnel through it and this leads to increased electron current at the drain side. Concurrently, at the source side, the electron Schottky barrier thickens (red circle) due to the p-type implant and leads to reduced electron tunneling at the source side. Thus, the leakage current observed is contributed only by the thermionic electron current having sufficient thermal energy to surmount the Schottky barrier at the source side. This is reflected by the very low leakage current at positive V_{GS} in Figure 6.3 (a). Therefore, the SB-VSiNW transistors fabricated in this study do not exhibit the typical ambipolar transfer output behavior of SB-MOSFET [6.9].

6.3.2 Short-Channel Effect Characteristics

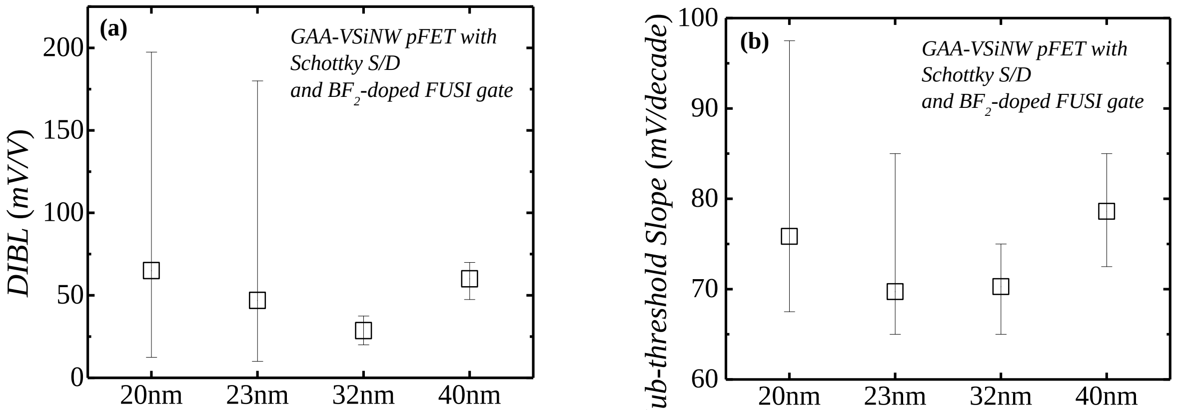


Figure 6.4 Extracted (a) DIBL and (b) Sub-threshold swing (SS) measurements plotted against VSiNW diameter. DIBL values remain below 75mV/V and SS values remain below 80mV/decadeade as the VSiNW diameter varies from 20nm to 40nm.

Figure 6.4 (a) shows the extracted DIBL values plotted against the VSiNW diameter. The average DIBL value decreases, from ~ 65mV/V to a minimum of ~ 27mV/V, as the nanowire diameter increases from 20nm to 32nm and rebound back to ~ 60mV/V as the nanowire diameter further increases to 40nm. The overall DIBL performance across all the measured nanowire diameters is almost constant ~ 50mV/V. The constant DIBL observed is due to the presence of Schottky barriers at the source and drain ends, even though the fabricated transistors have asymmetrical SB S/D regions, which reduce the bending of the VSiNW channel potential. Furthermore, compared to GAA-VSiNW doped PMOSFET with same nanowire diameter, the SB counterpart demonstrates DIBL values more than 400% lower. This remarkable result can be attributed to the steep, well-defined metallized S/D interface in the SB transistors since no diffusion of dopants are required and this helped to minimize the effect of drain bias on the energy band barrier on the source side.

Figure 6.4 (b) shows the extracted SS values plotted against the VSiNW diameter. The average SS value decreases, from ~ 76 mV/decade to ~ 71 mV/decade, with VSiNW diameter increases from 20nm to 32nm but it rebounds back to ~ 79mV/decade at VSiNW diameter = 40nm. The overall SS performance across all the measured nanowire diameter is almost constant at ~ 75mV/decade. The constant SS extracted indicates that the leakage current is suppressed and this can be attributed to the existence of an $NiSi_{2-x}$/Si Schottky barrier at the source which is immune to the drain bias applied at the various VSiNW diameter measured. Compared to GAA-VSiNW doped PMOSFET with the same diameter, the measured SB PMOSFET exhibits ~ 30% reduction in value. This is expected since no dopant implantation is needed, which, in turn, reduces the depletion layer capacitance and lowers SS.

6.3.3 I_{on}/I_{off} current characteristics and Threshold Voltage (V_T) tuning

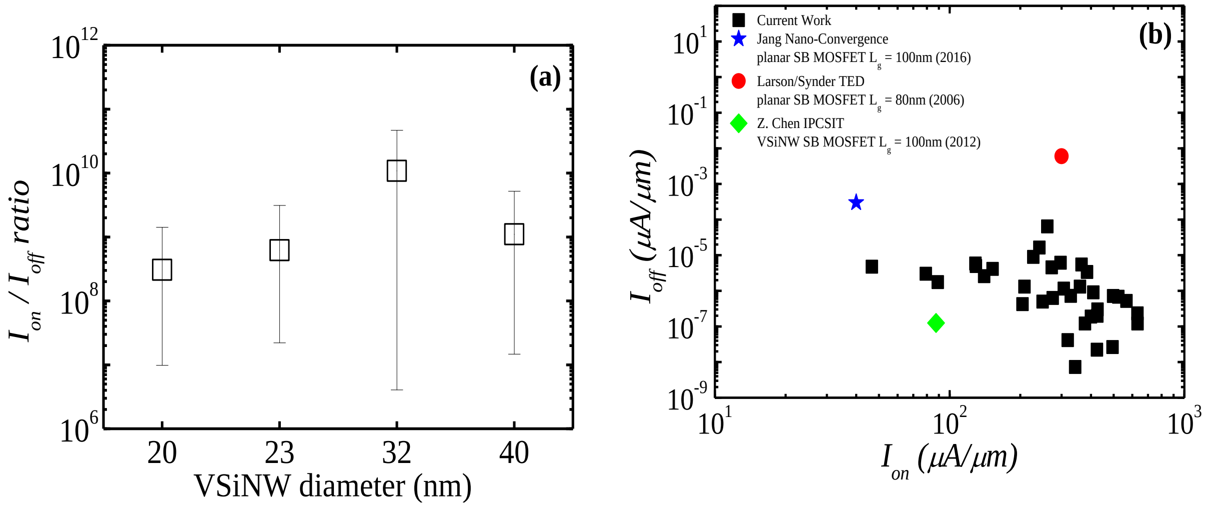


Figure 6.5 (a) I_{on} - I_{off} ratio of GAA-VSiNW PMOS with various diameters and (b) Ioff vs Ion characteristics of GAA-VSiNW PMOS compared with reported devices.

Figure 6.5 (a) plots the I_{on}/I_{off} ratio against VSiNW diameter characteristics of GAA-VSiNW SB PMOS. The I_{on}/I_{off} ratio shows an average value of ~ 10^9 for all VSiNW diameters, one order of magnitude higher than GAA-VSiNW doped PMOS. Since the absolute values of I_{on} and I_{off} are independent of VSiNW diameters, it implies that the variations in the I_{on}/I_{off} ratio is due to the slight differences in Φ_{beff} and not due to the difference in VSiNW diameter. This is contrary to the belief that with larger VSiNW diameter, the gate electrostatic potential control over the channel is reduced and results in higher leakage current. With the help of GAA architecture, I_{on}/I_{off} ratio is expected to be higher than the planar counterparts.

Figure 6.5 (b) illustrates the I_{off} versus I_{on} characteristics of GAA-VSiNW SB PMOS for various VSiNW diameters. Also included in Figure 6.5 (b) are the I_{off} versus I_{on} characteristics of some reported planar and VSiNW SB PMOS. A comparison owith the report in recent literature frames the results of the fabricated devices in favorable terms even against planar counterparts [6.2-6.4]. At $I_{off} = 10^{-7}$ µA/µm, the VSiNW SB PMOS in this study have 5 times higher I_{on} than that reported by Chen et al [6.1]. At I_{on} = 300 µA/µm, leakage current of the PMOS devices in this study is 4 orders of magnitude lower than those reported in [6.3].

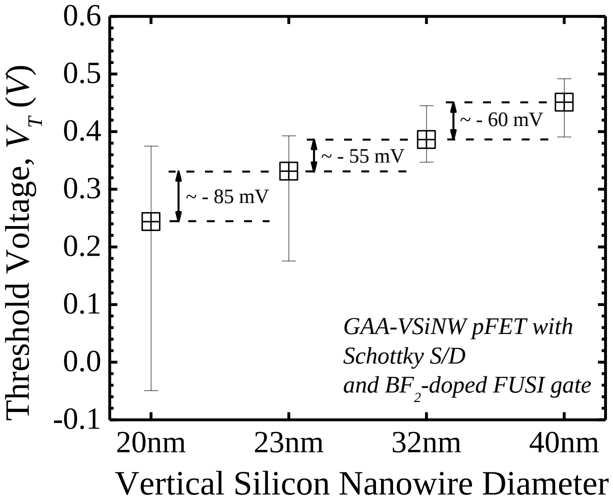


Figure 6.6 Threshold Voltage (V_T) variation across the various VSiNW diameters fabricated in this work. The extracted V_T shows an increasing trend when the VSiNW diameter increases from 20 nm to 40 nm.

Figure 6.6 shows the variation of threshold voltage (V_T) with respect to the different measured VSiNW diameter. V_T is extracted from the I_{DS} – V_{GS} measurement data using the trans-conductance extrapolation method in the linear region (GMLE). The average extracted V_T values from the measured GAA-VSiNW SB PMOS devices are in the positive range above 0V. This can be attributed to the work function mis-match between the gate and the channel. Moreover, the overall V_T trend decreases as the VSiNW diameter decreases with an average V_T reduction of 67 mV. In addition, it is observed that the reduction in V_T is bigger when the difference in VSiNW diameter is larger. This implies that V_T can be adjusted to the desired value by changing the size of VSiNW without the need of additional V_T adjustment implants or the use of different gate materials (such as Er for PMOS and Pt for NMOS) [6.6, 6.10] for different transistors.

6.5 GAA-VSiNW Schottky barrier NMOSFET

6.5.1 Output and Transfer Electrical Characterization

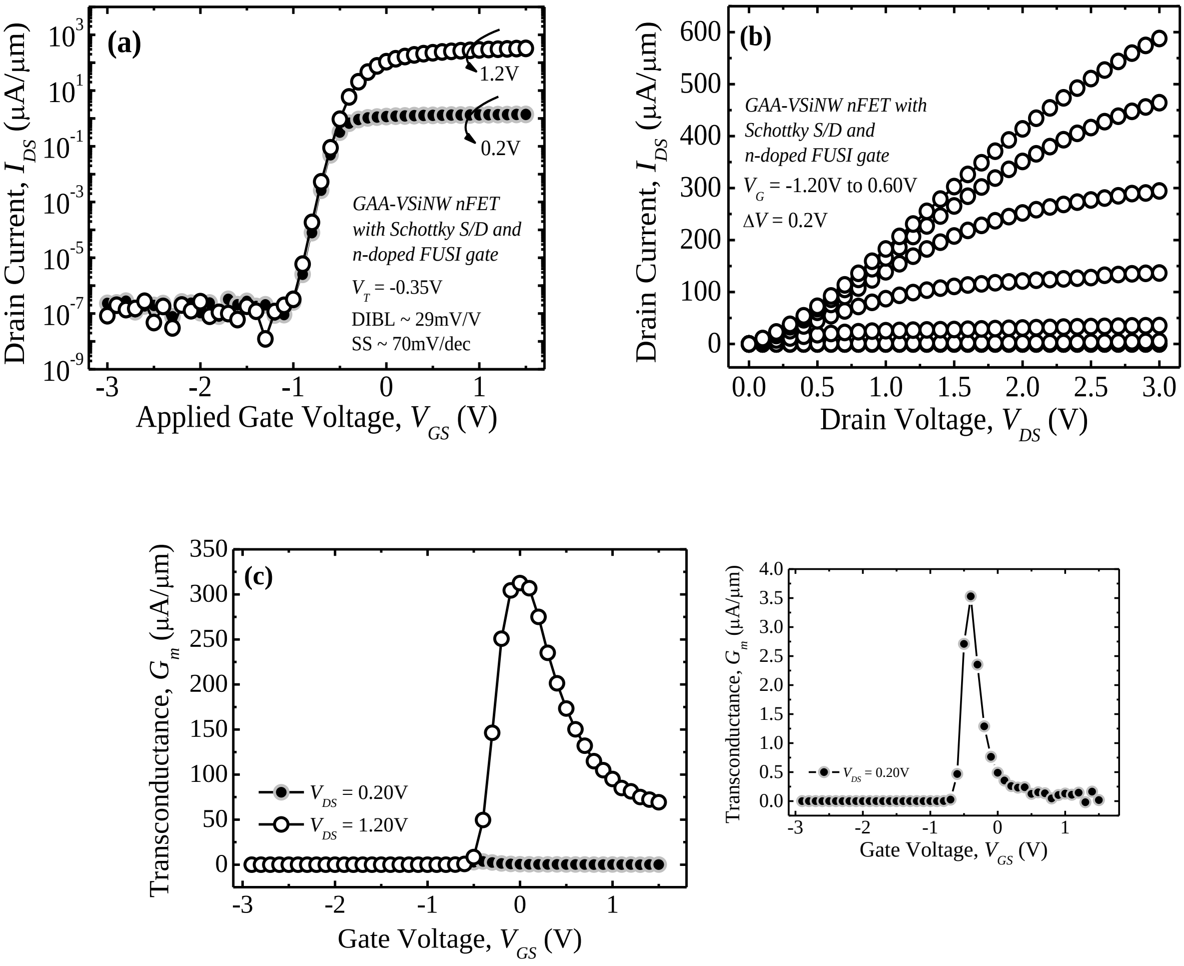


Figure 6.7 (a) I_{DS} – V_{GS} and (b) I_{DS} – V_{DS} plots of GAA-VSiNW NMOS with As-doped gate and S/D regions. The extracted $G_{m,sat}$ and $G_{m.lin}$ are plotted in Figure 6.7(c).

Figure 6.7 illustrates the output, transfer and trans-conductance characteristics of GAA-VSiNW NMOS with FUSI gate and asymmetrically silicided S/D regions. The gate length is ~ 100nm, the SiNW height and diameter are ~ 300nm and ~ 23nm, respectively. The I_{DS} – V_{GS} curve in Figure 6.7 (a) exhibits high I_{on} for positive V_{GS} region (~ 1000 µA/µm at V_{GS} = 1.5V and V_{DS} = 1.2V) and low leakage current, I_{off}, for negative V_{GS} region (~ 10^{-14} µA/µm at V_{GS} = -2V and V_{DS} = 1.2V). This behavior closely resembles the typical output characteristics of enhancement mode NMOS instead of Schottky Barrier NMOS. The root cause can be attributed to the asymmetrically silicided S/D regions as explained in Figure 6.3.

In addition, the fabricated NMOS exhibits excellent SCEs with DIBL ~ 29 mV/V and SS ~ 70 mV/decade. These values are comparable with those reported by E. J. Tan et. al. [6.11]. The I_{on}/I_{off} ratio for this measured device is ~ 10^6 at V_{DS} = 200mV and the extracted V_T is ~ -0.35V. From Figure 6.7 (b), there is a slight upward sloping sublinear turn-on, found in most SB MOSFET, due to the existence of Φ_{beff}. However, there is clear presence of linear and saturation regions for all V_{GS} biases, indicating that channel pinch-off has been reached.

Figure 6.7 (c) shows the extracted trans-conductance (G_m) of the fabricated device at V_{DS} = 0.2V and 1.2V. The inset presents the zoom-in view for V_{DS} = 0.2V because the G_m values are too small as compared to V_{DS} = 1.2V. Maximum G_m of ~ 325 µS/µm is achieved at V_{GS} = 0V for V_{DS} = 1.2V. Compared to GAA-VSiNW NMOS with doped S/D, for V_{DS} = 1.2V, the maximum G_m of GAA-VSiNW SB NMOS is ~ 2 times higher.

6.5.2 Short-Channel Effect Characteristics

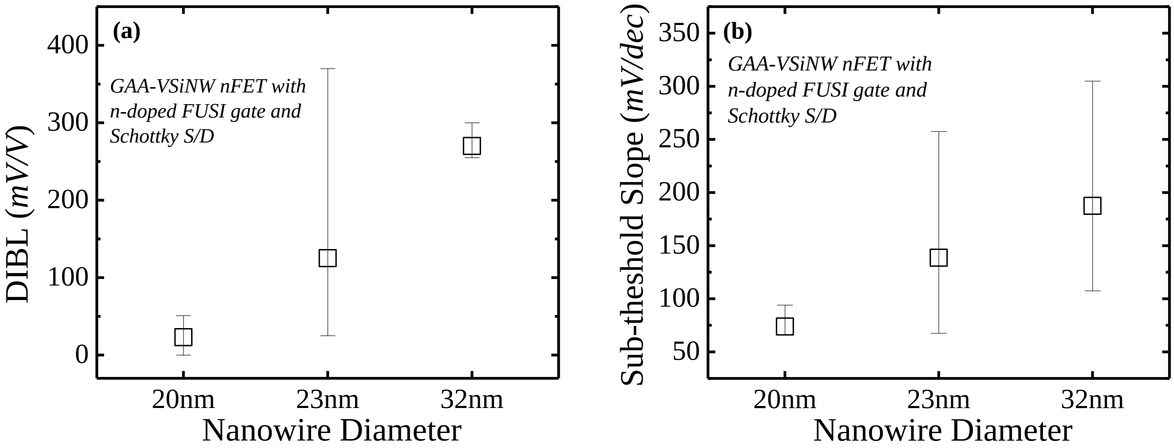


Figure 6.8 (a) and (b) depict the SCE characteristics, SS and DIBL, for various VSiNW diameters measured.

Figure 6.8 displays the SCEs (DIBL and SS) distribution of GAA-VSiNW SB NMOS with FUSI gate across various VSiNW diameters. As shown in Figure 6.8, DIBL and SS values both demonstrate an increasing trend as VSiNW diameter increases in size. The lowest DIBL and SS extracted are ~ 5 mV/V and ~ 66 mV/decade, respectively, where VSiNW diameter = 20nm. These values are amongst the lowest ever extracted with respect to reported literature [6.11]. Larger DIBL and SS values are expected for bigger VSiNW diameter size because the gate electric field coupling to the channel weakens and the drain starts to exert greater influence on the channel and source. This is similar to the degradation of SCEs in classic planar MOSFETs as the gate length shortened.

6.5.3 I_{on}/I_{off} current characteristics and V_T tuning

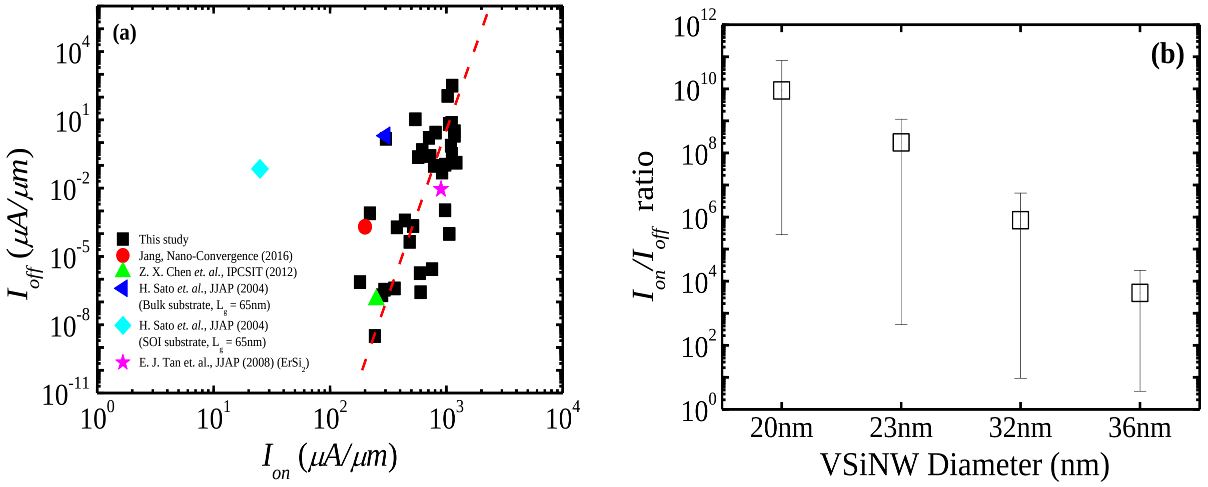


Figure 6.9 (a) I_{off} vs I_{on} characteristics of GAA-VSiNW NMOS fabricated in this study. Results from literature are also included. (b) I_{on}/I_{off} ratio of GAA-VSiNW NMOS measured in this study. Bigger diameter VSiNW shows lower I_{on}/I_{off} ratios than smaller diameter VSiNWs.

Figure 6.9 (a) illustrates the I_{on} vs. I_{off} characteristics of the measured devices with various VSiNW diameters. Included in the diagram are some reported I_{on} and I_{off} values for NMOSFETs with planar, GAA-VSiNW and lateral GAA-SiNW architectures. A comparison between the fabricated devices and those from reported literature [6.3-6.6] frames the devices in this study in favorable terms even against the planar counterparts [6.5]. The GAA-VSiNW SB NMOSFET I_{on} values are higher than the reported I_{on} values of planar SB NMOSFETs with shorter gate length or similar GAA-SiNW. The higher I_{on} values can be attributed to the enhanced tunneling current due to a possible thinning effect of the Schottky Barrier caused by smaller metal-silicon junction size [6.1].

Figure 6.9 (b) shows the I_{on} / I_{off} ratio of the fabricated GAA-VSiNW SB NMOS against various VSiNW diameters. The average I_{on} / I_{off} ratio decreases as the VSiNW diameter increases. For VSiNW diameter = 20nm, the average I_{on} / I_{off} ratio is ~ 10^{10} while the average I_{on} / I_{off} ratio reduces by 7 orders of magnitude to ~ 3.7 x 10^3 for VSiNW diameter = 36nm. The decrement of I_{on} / I_{off} ratio is consistent at approximately 2 orders of magnitude. The decreases in I_{on} / I_{off} ratio with increasing VSiNW diameter is expected because the electrostatic coupling of the gate weakens with larger VSiNW and as a result, the I_{off} values increase as a faster rate than the I_{on} values.

Figure 6.10 (a) shows the V_T box plot of measured GAA-VSiNW SB NMOS for various VSiNW diameters (Method 1). Negative V_T, which ranges from ~ -0.6V to ~ -2.75V with smaller VSiNW diameter having more positive V_T values (close to 0V) and larger VSiNW diameter having more negative V_T values, are extracted from the fabricated devices. This is a result of small work function difference between the gate and channel regions. Looking closer at the measurements, it is observed that the measured V_T values exhibit an increasing trend (V_T values are getting closer to or above 0V) with decreasing VSiNW diameter with an average ΔV_T of ~ 72 mV. This implied that the work function difference between the gate and channel regions can be engineered to the desired value simply by adjusting the VSiNW diameter, thus providing an effective yet highly efficient method of optimizing device V_T.

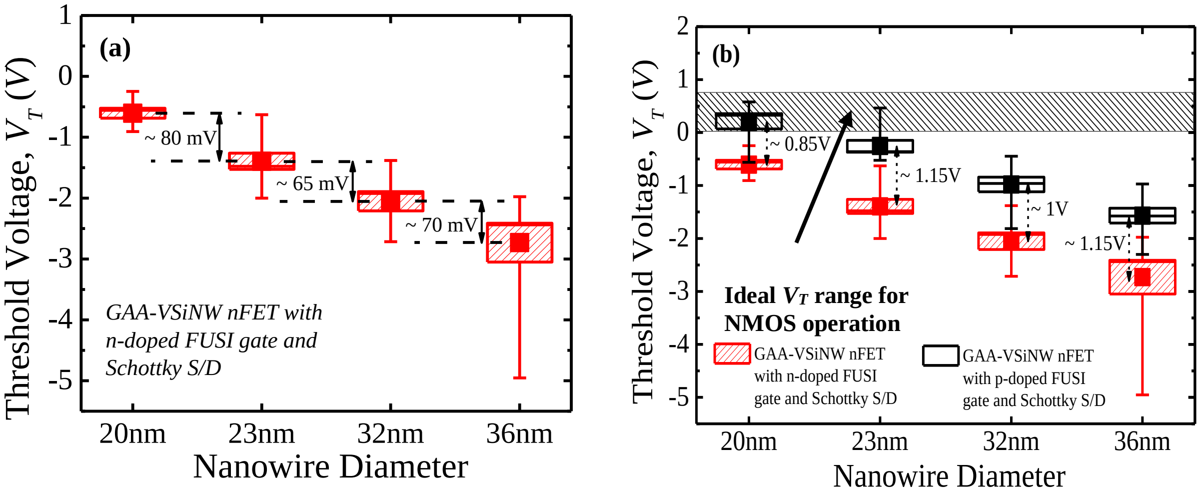


Figure 6.10 (a) Threshold Voltage (V_T) distribution of GAA-VSiNW SB NMOS. Smaller diameter VSiNW attains less negative V_T. ΔV_T varies from 65mV to 80mV. (b) A positive shift in V_T distribution for all measured GAA-VSiNW SB NMOS accomplished using BF_2-doped FUSI-gate. The ideal V_T range for normal NMOS operation is included

In this study, we have studied another option to optimize V_T. The second method (Method 2) is to implant the BF_2 (p-type) dopant species, instead of Phosphorus (n-type) dopant, into the gate region, before nickel deposition, to form tuned FUSI gate. Figure 6.10 (b) shows the V_T comparison of measured devices between n-doped and p-doped FUSI gates for various VSiNW diameters. From the measured results, the V_T values of GAA-VSiNW NMOS with BF_2-doped FUSI gate are consistently higher than those of Phosphorus-doped FUSI gate. The increment in V_T values ranges from 0.85V to 1.15V and there is an average positive V_T shift of ~ 1.04 V when all measured VSiNW diameters are taken into consideration. This positive shift in V_T can be attributed to the larger work function difference between the gate and channel regions due to BF_2 dopant species. Furthermore, it is observed that, with VSiNW diameters smaller than 23nm and BF_2 gate implant, the V_T

value of fabricated GAA-VSiNW SB NMOS can be tuned to above 0V (the ideal V_T range for NMOS operation).

In the next section, the different electrical aspects between GAA-VSiNW SB NMOS with Phosphorus - doped FUSI gate and GAA-VSiNW SB NMOS with BF_2 - doped FUSI gate will be compared.

6.6 Electrical characteristics comparison between GAA-VSiNW SB NMOS with BF_2 – doped FUSI gate and GAA-VSiNW SB NMOS with Phosphorus – doped FUSI gate

6.6.1 Output and transfer characteristics

From Section 6.5.3, there are 2 plausible methods to tune/optimize the NMOS V_T value. A combination of the 2 proposed methods is able to achieve the ideal V_T range for NMOS operation. In this section, detailed analysis is performed to investigate the impact of BF_2 gate doping on the various electrical characteristics and associated SCEs.

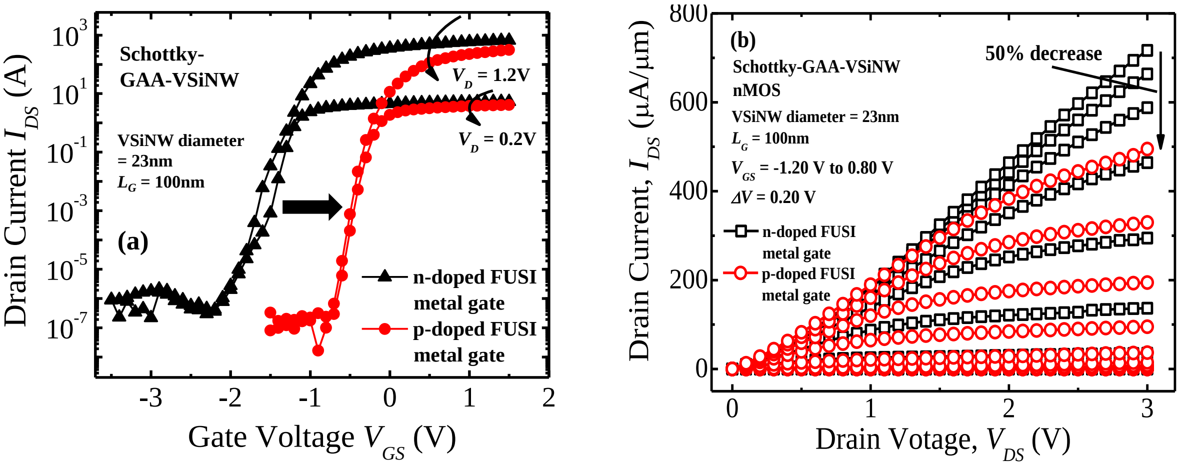


Figure 6.11 (a) I_{DS} - V_{GS} graph of GAA-VSiNW NMOS with n- and p-doped FUSI gate. Devices with p-doped FUSI gate showed a positive shift of +1V. The corresponding I_{DS} - V_{DS} graphs are shown in (b). There is a 50% decrease in drive current at V_{DS} = +3 V, V_{GS} = +0.80 V.

Figure 6.11 (a) compares the I_{DS} – V_{GS} characteristics between GAA-VSiNW SB NMOS with BF_2 – doped FUSI gate and GAA-VSiNW SB NMOS with Phosphorus – doped FUSI gate (VSiNW diameter = 23nm, L_{gate} = 100nm). From Figure 6.11 (a), it is observed that there is a +1 V rightward shift in the slope of the I_{DS} - V_{GS} curve which corresponds well with the ΔV_T value shown in Figure 6.10 (b). There is also a slight decrease in drive current for GAA-VSiNW SB NMOS with p-doped FUSI metal gate at V_{GS} = + 1.50 V, V_{DS} = + 1.20 V. This can be attributed to the increases in V_T. Furthermore, the I_{off} value remains constant at ~ 6.5 x 10^{-6} µA/ µm for both types of NMOS. This implies that the change in gate doping species has no impact on the leakage current.

Figure 6.11 (b) illustrates the I_{DS} – V_{DS} characteristics of both types of GAA-VSiNW SB NMOS. There is a clear presence of linear and saturation regions for all V_{GS} biases, indicating that the channel pinch-off has been reached. Clearly, from Figure 6.11 (b), NMOS device with BF_2 – doped FUSI metal gate demonstrated a 50% drop in I_{DS} at V_{DS} = +3 V, V_{GS} = +0.80 V. This substantiates the drive current observation seen in Figure 6.11 (a).

6.6.2 Short-Channel Effect Characteristics

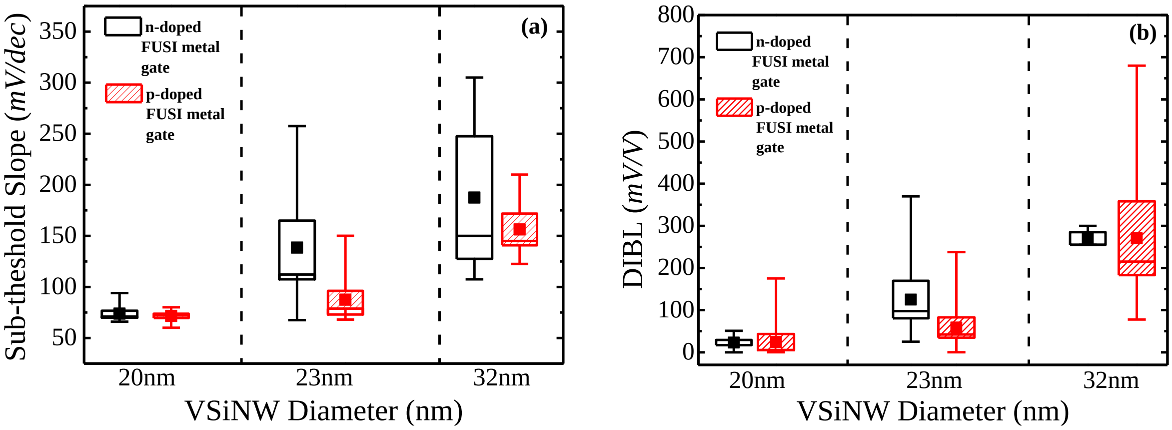


Figure 6.12 (a) SS comparison between GAA-VSiNW SB NMOS with n- vs p-doped FUSI gate. (b) illustrates the DIBL comparison of the same devices in (a).

Figure 6.12 compares the (a) SS and (b) DIBL characteristics between GAA-VSiNW SB NMOS with n-doped FUSI metal gate and GAA-VSiNW SB NMOS with p-doped FUSI metal gate. From Figure 6.12 (a), at VSiNW diameter = 20nm, good SS performance (~ 70 mV/decade) is achieved for both types of NMOS devices. The SS performance degrades with larger VSiNW diameters. This is expected because full depletion of VSiNW is hard to achieve at large VSiNW diameters, resulting in sub-threshold leakage which leads to SS degradation. At VSiNW diameter > 23nm, the SS values of devices with p-doped FUSI metal gate is consistently lower than those of devices with n-doped FUSI metal gate. This may suggest that increasing the work function difference between the gate and channel regions will aid in the slowdown of SS degradation to VSiNW diameters larger than those fabricated in this study.

From Figure 6.12 (b), excellent DIBL characteristic (~ 20mV/V) is achieved for both types of NMOS devices at VSiNW diameter = 20nm. However, the DIBL performance degrades with VSiNW diameters > 20nm. Unlike the corresponding SS performance, DIBL values remain fairly consistent between both device types.

6.6.3 Effective Schottky Barrier Height

The total injection current from the drain can be approximated by the aggregation of thermionic (I_{TE}) and tunneling (I_{TN}) currents (i.e. $I = I_{TE} + I_{TN}$) which can be expressed in the forms of

$$I_{TE} = AA^{*}T^{2}exp\left(-\frac{q(\Phi_b+\Psi_c)}{kT}\right) = I_s exp\left(-\frac{q\Psi_c}{kT}\right) \quad \text{(Equation 6.1)}$$

and

$$I_{TN} = \frac{Aq^{2}E^{2}}{8\pi h\Phi} exp\left[-\frac{8\pi}{3hqE}\{2m^{*}(q\Phi_b)^{3}\}^{\frac{1}{2}}\right] \quad \text{(Equation 6.2)}$$

where Φ_b is the SBH, Ψ_c is the channel potential (conduction band across the channel modulated by the external gate voltage), k is the Boltzmann constant, T is the measurement temperature, q is the electronic charge, A is the diode area, A^* is the Richardson constant, E is the electric field across Φ_b, h is the Planck's constant and m^* is the effective mass.

Hence, to determine the SBH, the I_{TE} or I_{TN} would need to be evaluated first and then solve for SBH. In practice, it is more straightforward to measure the total current and solve for an 'effective' SBH via the thermionic equation (see Equation 6.1) since the total current encompasses both I_{TE} and I_{TN} components. In this study, we employed the modified method by Zhang et. al. [6.7] and Peng et. al. [6.8] to evaluate the effective SBH of SB and DSSB (to be introduced in Chapter 7) nanowire transistors. The equation is expressed as:

$$I = wA^{**}T^2 exp\left(-\frac{q\Phi_{eff}}{kT}\right)\left[exp\left(\frac{qV_D}{kT}\right) - 1\right] \qquad \text{(Equation 6.3)}$$

where w is a suitable geometric factor e.g. the nanowire diameter.

The device $I_{DS} - V_{GS}$ is measured at relatively low V_{DS} across several temperatures where I_{DS} is simply the total current across the MS junction. For every point of V_{GS}, a corresponding effective SBH is extracted as the activation energy from the Arrhenius plot using Equation 6.3. A typical Arrhenius plot is shown in Figure 6.13 where the measurement was done between 300K to 100K. Only the shaded region is used for the extraction of the activation energy due to good linearity.

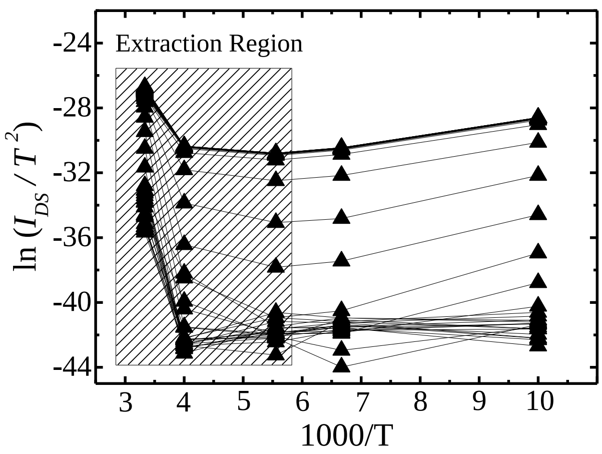


Figure 6.13 Arrhenius plot of SB GAA-VSiNW nMOS from which the effective SBH is extracted from the linear region of the plot.

Figure 6.14 shows the extracted effective SBH (*Φ*$_{beff}$) of GAA-VSiNW SB NMOS with n-doped FUSI metal gate and GAA-VSiNW SB NMOS with p-doped FUSI metal gate as a function of the applied V_{GS}. The extracted Φ_{beff} takes into account both thermionic (I_{TE}) and tunneling current (I_{TN}). Therefore, it is a measure of Schottky Barrier Height (SBH) and Schottky Barrier thickness. Disparity in Φ_{beff} is observed between the two types of devices at $V_{GS} < -0.5$ V. This is due to the different V_T values where devices with n-doped FUSI metal gate has more negative V_T than devices with p-doped FUSI metal gate.

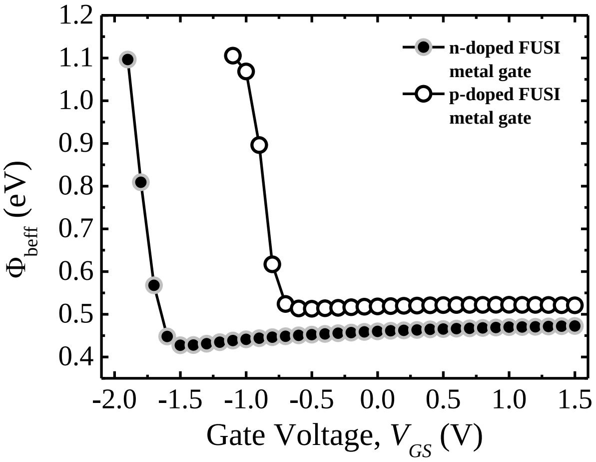


Figure 6.14 Effective SBH (Φ_{beff}) of devices with n-doped FUSI metal gate and p-doped FUSI metal gate.

From Figure 6.14, for n-doped FUSI metal gate, between V_{GS} = -1.90 V to -1.70 V, the current transport mechanism is dominated by TE with a slope of ~ 2.6 eV/V. In this region, V_{GS} modulates the SBH to ~ 0.56 eV. Between V_{GS} = -1.70 V to V_{GS} = -1.50 V, V_{GS} modulates the Schottky Barrier thickness and the current flow is now controlled by thermionic field emission (TFE) with the Φ_{beff} modulation is reduced to ~ 0.70 eV/V. Thus, the change in Φ_{beff} is due to the different current conduction mechanisms. At larger V_{GS} (V_{GS} > -1.50V), V_{GS} is unable to reduce the Schottky Barrier thickness further and the current flow is limited by the VSiNW resistance. This occurs for V_{GS} > -1 V whereby Φ_{beff} remains constant ~ 0.45 eV.

For p-doped FUSI metal gate, the Φ_{beff} modulation is ~ 2.2 eV/V, between V_{GS} = -1 V to -0.80 V, very similar to n-doped FUSI metal gate. Hence, the current transport in this region is dominated by TE. Between V_{GS} = -0.80 V to -0.60V, Φ_{beff} modulation is reduced to ~ 0.52 eV/V and the current transport mechanism has changed from TE to TFE whereby V_{GS} adjusts the Schottky Barrier thickness. At V_{GS} > -0.60 V, Φ_{beff} is equal to 0.51 eV, slightly higher than n-doped FUSI metal gate devices. Both Φ_{beff} values are near Si mid-gap which exemplifies Fermi level pinning.

6.5 Chapter Summary

We have fabricated Schottky Barrier PMOSFET and NMOSFET via GAA-VSiNW architecture. GAA-VSiNW SB PMOS exhibited high I_{DS} (~ 650 µA/µm at V_{DS} = -1.2V, V_{GS} = -2V) with low leakage (~ 10^{-6} µA/µm at V_{DS} = -1.2V, V_{GS} = +2V). In addition, GAA-VSiNW SB PMOS fabricated in this study exhibited 5 times higher drive current than reported literature at I_{off} = 10^{-7} µA/µm. Furthermore, our devices showed excellent SCE performance.

There is slight upward sloping sub-linear slope shown in GAA-VSiNW SB NMOS and the SCE performance is degraded as compared to GAA-VSiNW SB PMOS. In terms of I_{on}-I_{off} characteristics, GAA-VSiNW SB NMOS fabricated in this study still outperforms those reported in literature.

For V_T tuning, GAA-VSiNW SB NMOS with p-doped FUSI gate showed an average positive V_T shift of ~ 1.04V and NMOS devices with diameters 20nm and 23nm able to meet the V_T requirement for LSTP application. Despite this advantage, GAA-VSiNW SB NMOS with p-doped FUSI gate demonstrated a 50% drop in drain current. This observation is due to the increase in device V_T. At the same time, GAA-VSiNW SB NMOS with p-doped FUSI gate also exhibited better SCE performance than that of n-doped FUSI gate and both types of device achieve almost identical effective SBH for electrons.

6.6 References

[6.1] G. D. J. Smit, S. Rogge and T. M. Klapwijk, “Scaling of nano-Schottky-diodes”, *App. Phys. Lett.*, vol. 81, pp. 3852-3854 (2002).

[6.2] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1048-1058, May 2006.

[6.3] Z. Chen, X. Li, A. Kamath, X. Wang, K. Buddharaju, J. Wang, R. Sayanthan, K. T. Win, N. Singh, G. Q. Lo, and D. -L. Kwong, “Vertical Silicon Nanowire CMOS Inverter”, *IPCSIT*, vol. 32, pp. 92, 2012.

[6.4] M. Jang, "Scalability of Schottky barrier metal-oxide-semiconductor transistors," *Nano Convergence*, vol. 3, pp. 1-7, 2016.

[6.5] H. Sato, H. Sato, T. Iguchi, and M. Asada, "Increase drive current by Pt/W protection on short-channel Schottky S/D metal-oxide-semiconductor field-effect transistors with metal gate", *Jpn. J. Appl. Phys.*, vol. 43, no. 9A, pp. 6038–6039, 2004.

[6.6] E.J. Tan, K. L. Pey, N. Singh, D. -Z. Chi, G. -Q. Lo, P. S. Lee, K. -M. H, Y. K. Chin and G. D. Cui, "Erbium silicided Schottky Source/Drain Silicon Nanowire N-Metal–Oxide–Semiconductor Field-Effect Transistors", *Jpn. J. Appl. Phys.*, vol. 47, No. 4, pp. 3277–3281, 2008

[6.7] M. Zhang, J. Knoch, Q. T. Zhao, A. Fox, S. Lenk and S. Mantl, "Low temperature measurements of Schottky barrier SOI-MOSFETs with dopant segregation," *Electronics Letters*, vol. 41, no. 19, pp. 1085-1086, Sep. 2005.

[6.8] J. W. Peng, S. J. Lee, G. C. A. Liang, N. Singh, S. Y. Zhu, G. -Q. Lo and D. -L. Kwong, "Improved carrier injection in gate-all-around Schottky barrier silicon nanowire field-effect transistors," *App. Phys. Lett.*, vol. 93, p. 073503, 2008.

[6.9] D. Sacchetto, G. De Micheli, and Y. Leblebici, “Ambipolar Si Nanowire Field Effect Transistors for low current and temperature sensing”, *16th International Solid-State Sensors, Actuators and Microsystems Conference*, Beijing, 2011, pp. 2562-2565, 2011

[6.10] C. Wang, J. P. Snyder, and J. R. Tucker, “Sub-40 nm PtSi Schottky source/drain metal–oxide–semiconductor field-effect transistors,” *Appl. Phys. Lett.*, vol. 74, no. 8, pp. 1174–1176, Feb. 1999

[6.11] E. J. Tan, K. L. Pey, N. Singh, G. Q. Lo, D. Z. Chi, Y. K. Chin, L. J. Tang, P. S. Lee and C. K. F. Ho, “Nickel-Silicided Schottky Junction CMOS Transistors With Gate-All-Around Nanowire Channels”, *IEEE Electron Device Letters*, Vol. 29, No. 8, pg. 902 – 905, August 2008.

CHAPTER 7

JUNCTION ENGINEERING WITH DOPANT-SEGREGATED SCHOTTKY BARRIER VSiNW MOSFETs

7.1 Introduction

In Chapter 6, we have investigated the electrical and SCE characteristics of GAA-VSiNW SB MOSFETs. Furthermore, we have successfully demonstrated SB transistors with superb electrical and SCE performance. Concurrently, we are able to tune the device V_T through replication of the V_T tuning methods first discussed in Chapter 5.

Although GAA-VSiNW SB MOSFETs have attained high drive current (I_{on}), we would like to further increase I_{on} while maintaining low leakage current (I_{off}) levels. To help achieve this goal, a technique known as dopant segregation is integrated into GAA-VSiNW SB n- and p-MOSFETs. Dopant segregation is attained by forming metal silicide on an ultra-shallow doped region to accumulate or ‘snow-plow’ the dopants at the Metal-Silicon (MS) interface. An advantage of this method is the use of a single metal for both NMOS and PMOS and the metal does not necessary has to be rare earth material.

In this chapter, we will also explore the implementation of Dopant Segregated Schottky Barrier (DSSB) S/D regions in VSiNW MOSFET (GAA-VSiNW DSSB MOSFET), determine their electrical characteristics and compare them against those from GAA-VSiNW SB MOSFET. At the same time, we will also include V_T tuning splits for NMOS devices and measure the corresponding electrical characteristics.

7.2 Experimental Details

In this chapter, the devices under study are: (i) GAA-VSiNW DSSB PMOS with doped FUSI gate and (ii) GAA-VSiNW DSSB NMOS with doped FUSI gate. The fabrication process details for the devices studied in this chapter had been outlined in Section 3.4.2 in Chapter 3.

GAA-VSiNW DSSB MOSFETs with doped FUSI gate were fabricated on single VSiNWs with height ~ 300nm, gate length (L_{gate}) ~ 100nm and varying diameters (from 20nm to 60nm). The VSiNW tip and wafer substrate will serve as the drain (D) and source (S) regions, respectively. To obtain the dopant accumulation effect, a pre-silicidation implant step was done before Ni deposition. For PMOS, the pre-silicidation implant conditions are BF_2 / 5KeV / 4 x 10^{15} cm^{-2} / 0^o tilt / 0^o twist and for NMOS, the pre-silicidation implant conditions are As / 5KeV / 4 x 10^{15} cm^{-2} / 0^o tilt / 0^o twist. Finally, S/D and gate electrical contacts are done through patterned metal layers consisting of TaN/Al/TaN layers.

Due to the complexity of gate last process and the risk of metal cross contamination between different process equipment used during the VSiNW transistor fabrication, the gate first process is adopted but a drawback of this process is the formation of asymmetrical SB S/D regions. In order to achieve low substrate resistivity, the substrate is subjected to a pre-implant step with high dose and low implant energy before the Ni deposition. Unless specified otherwise, the devices studied in this chapter will consist of doped FUSI gate and asymmetrical DSSB S/D regions.

For the V_T tuning splits, the gate implant conditions are shown in the table below. In Table 7.1, the implant conditions for dopant segregation are kept constant except for the dopant species used. GAA-VSiNW NMOS is chosen as the test vehicle for the V_T tuning study because from literature, the V_T value for GAA-VSiNW FETs tends to be negative.

Device	**Implant conditions**
GAA-VSiNW DSSB NMOS (control)	P/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations
GAA-VSiNW DSSB NMOS (tuned V_T)	BF_2/5 keV/ 1 x 10^{15} cm^{-2}/ 20^0 tilt/ 4 rotations

Table 7.1 List of gate implant conditions for V_T tuning splits to be used in conjunction with GAA-VSiNW DSSB NMOS

7.3 Electrical Characteristics of GAA-VSiNW DSSB PMOS measured against GAA-VSiNW SB PMOS

7.3.1 Transfer and Output Electrical Characterization

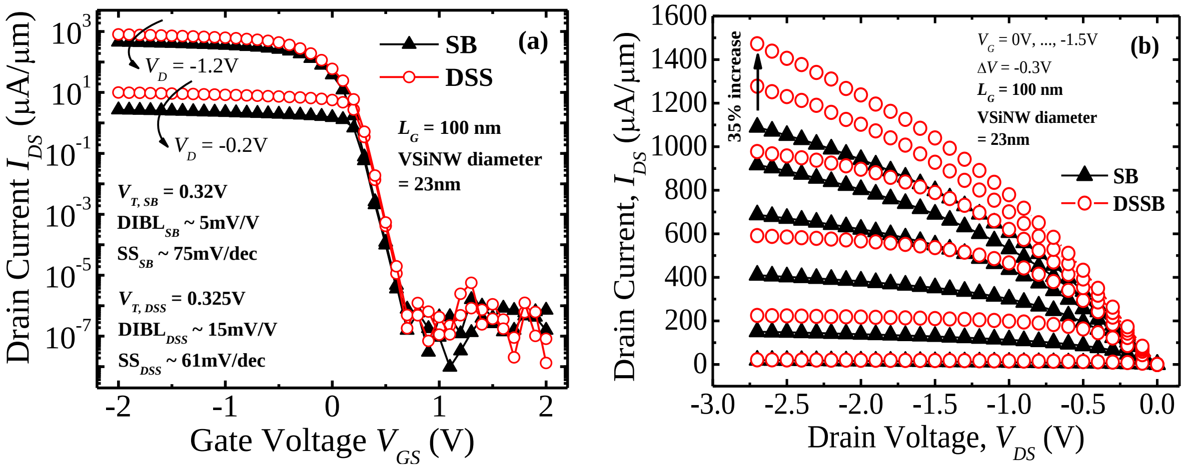


Figure 7.1 (a) I_{DS} – V_{GS} transfer characteristics of GAA-VSiNW DSSB PMOS compared against GAA-VSiNW SB PMOS. (b) shows the corresponding I_{DS} – V_{DS} output characteristics of the same devices.

Figure 7.1 (a) shows the I_{DS} – V_{GS} curve of GAA-VSiNW SB PMOS measured against that of GAA-VSiNW DSSB PMOS. During measurement, gate voltage of ± 2V and drain voltage of -1.2V and -0.2V are applied to the device under test while the source is maintained at 0V. It is worthwhile to take note that the VSiNW tip is denoted as ‘Drain’ and the VSiNW bottom is denoted as ‘Source’ and the gate is BF_2 – doped FUSI metal gate.

High I_{on} are achieved, at V_{DS} = -1.2V and V_{GS} = -2V, for both SB and DSSB PMOS. For DSSB PMOS, the drive current, at V_{DS} = -1.2V and V_{GS} = -2V, is ~ 800 µA/µm which is 77% higher as compared to 450 µA/µm achieved by SB PMOS under same testing condition. The Drain-Induced Barrier Leakage (DIBL) for DSSB PMOS is ~ 15mV/V, three times higher than SB PMOS (~ 5 mV/V) but the Sub-threshold swing (SS) for DSSB PMOS is ~ 19% lower than SB PMOS (61 mV/decade for DSSB against 75 mV/decade for SB). Note that the DIBL of DSSB PMOS is very close to ideal SS (60 mV/decade).

The increase is DIBL can be attributed to the diffusion of small amounts of dopants, caused by thermal steps during the fabrication, closer to the channel region. However, the improvement in SS is due to the presence of accumulated dopants at MS interface which altered the energy bands as explained in Chapter 2. Despite the enhanced I_{on}, the I_{off} for both devices remained constant at 6.5 pA/µm.

From Figure 7.1 (b), it is observed that there is absence of upward sloping sublinear turn-on due to the low Φ_{beff} to holes. There is clear presence of linear and saturation regions of all V_{GS} biases, indicating channel pinch-off has been reached. Furthermore, DSSB PMOS exhibits higher measured I_{DS} than SB PMOS for every V_{GS}. At V_{GS} = -1.5 V and V_{DS} = -2.7 V, DSSB PMOS shows a 39% increase in I_{DS} over SB PMOS.

7.3.2 Device current characteristics, Short Channel Performance and Threshold Voltage Tuning

Figure 7.2 (a) shows the I_{DS} behavior with respect to various VSiNW diameters. From Figure 7.2 (a), the extracted I_{DS}, at V_{GS} = -2V and V_{DS} = -1.2V, of DSSB GAA-VSiNW PMOS is clearly much higher than that of SB GAA-VSiNW PMOS for all the measured VSiNW diameters. The enhancement in drive current can be attributed to thinning of Schottky Barrier thickness and Fermi level de-pinning caused by segregating dopants at the MS interface. This is supported by the consistency of drive current value of DSSB PMOS.

From Figure 7.2 (b), DSS GAA-VSiNW PMOS exhibit consistently higher I_{on} than SB GAA-VSiNW PMOS even at larger VSiNW diameter. This is consistent with the observation seen in Figure 7.2 (a). At I_{off} = 10 pA/µm, DSS GAA-VSiNW PMOS (1160 µA/µm) showed a 66% increase in I_{on} with respect to SB GAA-VSiNW PMOS (700 µA/µm).

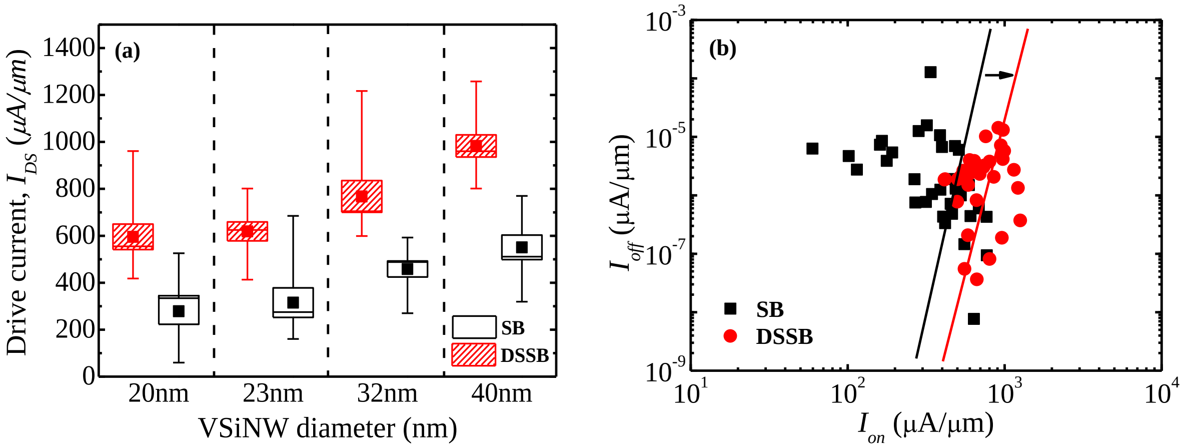


Figure 7.2 (a) I_{dsat} of GAA-VSiNW PMOS increase with increasing VSiNW diameter. Devices with DSS S/D show higher *Idsat* than those with SB S/D. Figure 7.2 (b) I_{on} vs I_{off} characteristics of GAA-VSiNW PMOS with DS S/D and DSS S/D.

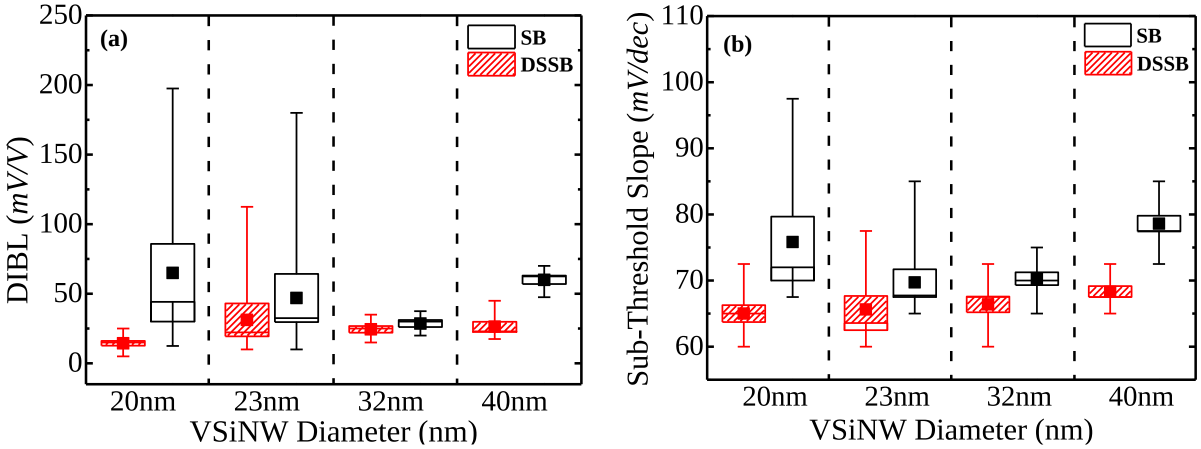


Figure 7.3 (a) DIBL and (b) SS values of DSSB GAA-VSiNW PMOS are consistently smaller than SB GAA-VSiNW PMOS. This implies segregated dopants at MS interface helped to alleviate SCE.

Figure 7.3 illustrates the short channel performance DSSB GAA-VSiNW PMOS plotted as a function of VSiNW diameter. Setting as a benchmark, the DIBL and SS characteristics of SB GAA-VSiNW PMOS are compared against those of DSSB GAA-VSiNW PMOS in Figure 7.3. It is clear that the short channel performance of DSSB GAA-VSiNW PMOS is much better than SB GAA-VSiNW PMOS as shown in Figures 7.3 (a) and (b). Both DIBL and SS characteristics of DSSB GAA-VSiNW PMOS exhibit lower values as compared to SB GAA-VSiNW PMOS.

It is easy to notice the similarities in the trends between the two plots in Figure 7.3. The short channel performance of DSSB GAA-VSiNW PMOS improves with smaller VSiNW diameters. This implies that smaller VSiNW diameters coupled with dopant segregation technique is beneficial to the further scaling of GAA-VSiNW.

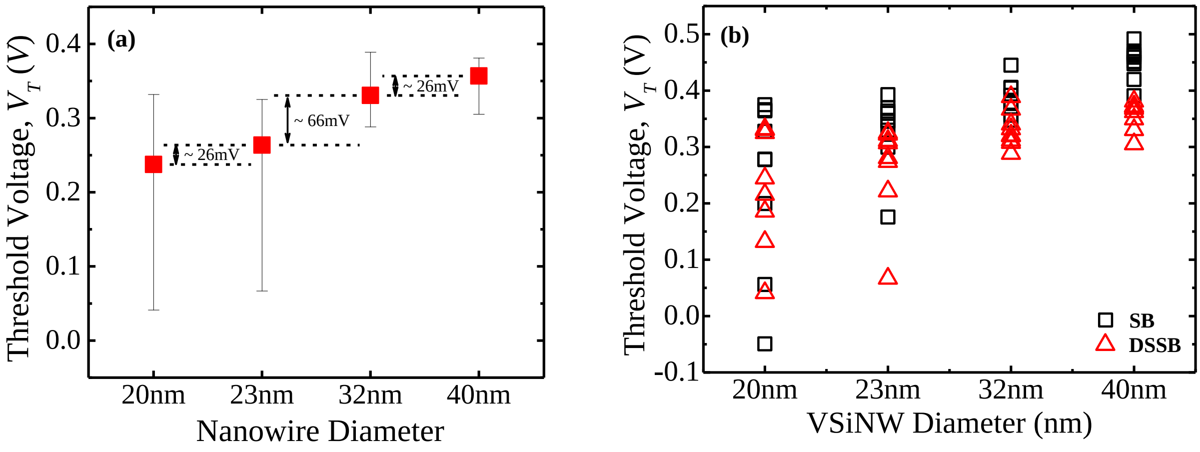


Figure 7.4 (a) Threshold Voltage (V_T) of DSSB GAA-VSiNW PMOS as a function of VSiNW diameter and (b) V_T comparison of DSSB GAA-VSiNW PMOS with respect to SB GAA-VSiNW PMOS.

Figure 7.4 (a) shows the V_T of DSSB GAA-VSiNW PMOS as a function of VSiNW diameter while Figure 7.4 (b) shows the V_T comparison between DSSB GAA-VSiNW PMOS and SB GAA-VSiNW PMOS. From Figure 7.4 (a), it is clear that fine-tuning of V_T, for GAA-VSiNW devices, is achievable by reducing or increasing the VSiNW diameter. This provides a simple yet cost-efficient method to optimize device performance and is definitely beneficial to further scaling of VSiNW devices.

From Figure 7.4 (b), there is minimal difference in the extracted V_T values for both DSSB and SB GAA-VSiNW PMOS devices. This implies that the segregated dopants did not diffuse into the channel region (underneath the gate) but only to regions close to the channel. Thus, there is no large impact on device V_T.

7.4 Electrical Characteristics of DSSB GAA-VSiNW NMOS measured against SB GAA-VSiNW NMOS

7.4.1 Transfer and Output Electrical Characterization

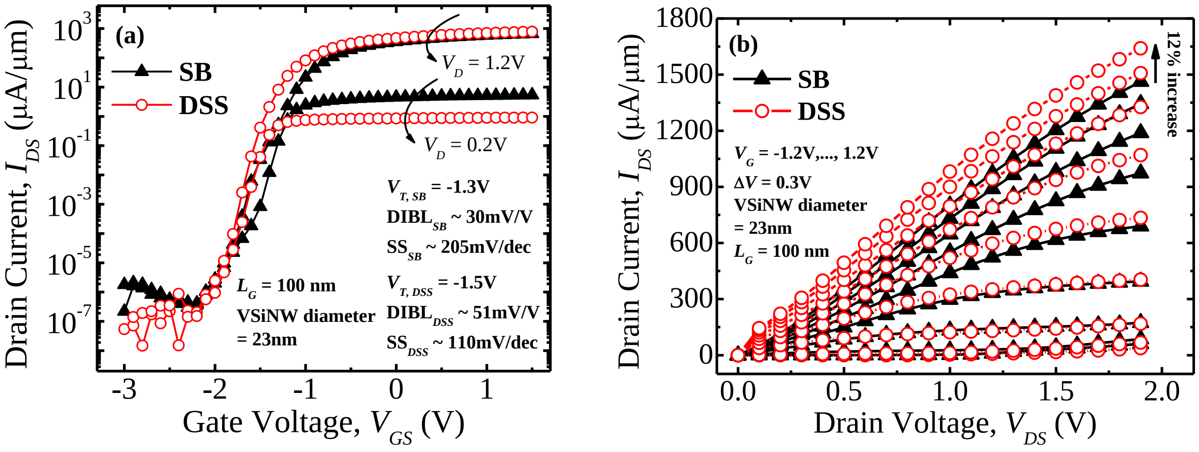


Figure 7.5 (a) I_{DS} – V_{GS} transfer characteristics of DSSB and SB GAA-VSiNW NMOS and (b) I_{DS} – V_{DS} output characteristics of the same devices.

In this section, the electrical characteristics of DSSB GAA-VSiNW NMOS are compared against SB GAA-VSiNW NMOS. It is worthwhile to take note that the gate is Arsenic – doped FUSI metal gate and the sole difference between both types of devices is the segregation of dopants at the MS interface.

Figure 7.5 depicts the I_{DS} – V_{GS} transfer and I_{DS} – V_{DS} output characteristics of DSSB GAA-VSiNW NMOS with respect to SB GAA-VSiNW NMOS. From Figure 7.5 (a), high I_{DS} is achieved for both SB and DSSB NMOS. At V_{GS} = 1.5 V and V_{DS} = -1.2 V, DSSB NMOS (~ 778 µA/µm) demonstrated a 17% increase in drive current (I_{DS}) as compared to SB NMOS (~ 664 µA/µm). The enhancement in I_{DS} can be attributed to the successful reduction of Φ_{beff} to electrons due to the segregated Arsenic dopants at the MS interface. Although there is an increase in drive current, the leakage current (I_{off}) remains constant at ~ 6.5 x 10^{-6} µA/µm for both DSSB and SB GAA-VSiNW NMOS. This implies that the accumulated dopants at MS interface do not pose detrimental impact to the transistor performance.

Furthermore, extracted DIBL for DSSB NMOS (~ 51 mV/V) is ~ 1.7 times higher than that of SB NMOS (~ 30 mV/V) but SS for DSSB NMOS is 86% lower than SB NMOS (110 mV/decade for DSSB against 205 mV/decade for SB).

From Figure 7.5 (b), there is an absence of an upwardly sloping sublinear turn-on, an indication of low Φ_{beff} to electrons. There is clear presence of linear and saturation regions for low V_{GS} biases, indicating that the channel pinch-off has been reached. Furthermore, DSSB NMOS showed higher I_{DS} than SB NMOS for every measured V_{GS}. At V_{GS} = 1.2 V and V_{DS} = 1.9 V, DSSB NMOS demonstrated 12% increase in I_{DS} over SB NMOS.

7.4.2 Device current characteristics, Short Channel Performance and Threshold Voltage Tuning

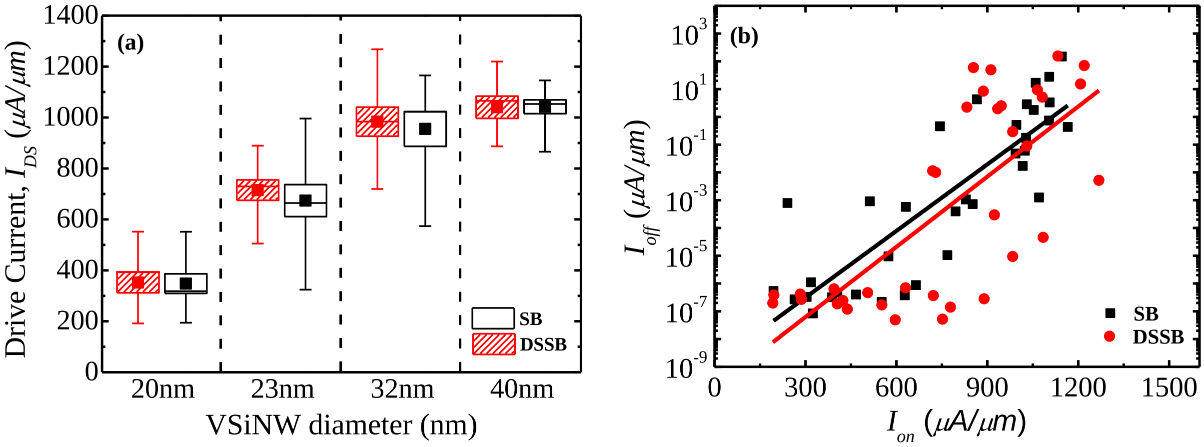


Figure 7.6 (a) I_{DS} of DSSB and SB GAA-VSiNW NMOS increase with increasing VSiNW diameter. DSSB devices show higher I_{DS} than SB devices. (b) I_{on} vs I_{off} characteristics of DSSB and SB GAA-VSiNW NMOS.

Figure 7.6 (a) depicts the extracted I_{DS} characteristics as a function of VSiNW diameter. Clearly, DSSB GAA-VSiNW NMOS has slightly higher I_{DS} than SB GAA-

VSiNW NMOS. In terms of $I_{on} - I_{off}$ characteristics, at I_{off} = 10 pA/µm, there is a 15% increase in I_{DS} for DSSB GAA-VSiNW NMOS with respect to SB GAA-VSiNW NMOS. This enhancement in I_{DS} can be attributed to the modification of the Schottky Barrier thickness due to the segregated dopants at the MS interface.

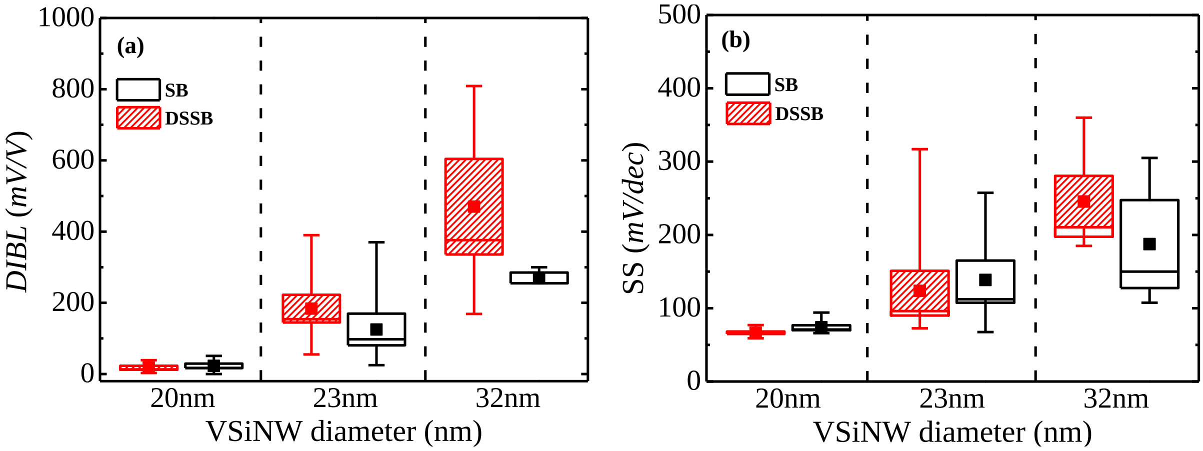


Figure 7.7 (a) DIBL and (b) SS of DSSB GAA-VSiNW NMOS are higher than SB GAA-VSiNW NMOS.

Figure 7.7 illustrates the DIBL and SS characteristics comparison between DSSB GAA-VSiNW NMOS and SB GAA-VSiNW NMOS. For VSiNW diameter = 20nm, it is clear that the DIBL and SS performance for DSSB GAA-VSiNW NMOS is better than SB GAA-VSiNW NMOS but for VSiNW diameter > 20nm, DIBL performance of SB GAA-VSiNW NMOS is better than its counterpart. However, for SS performance, SB GAA-VSiNW exhibit lower values only when VSiNW diameter is > 23nm. Process fluctuations might be the reason for these mixed results.

Figure 7.8 shows the threshold voltage (V_T) variation as a function of VSiNW diameter. From Figure 7.8 (a), it is clear that V_T of DSSB GAA-VSiNW NMOS exhibits an increasing trend as VSiNW diameter reduces. ΔV_T ranges from 900mV to 26mV whereby the larger VSiNW diameter (reduction from 40nm to 32nm) gets smaller ΔV_T value while smaller VSiNW diameter (reduction from 23nm to 20nm) gets larger ΔV_T value. This implies that V_T of DSSB GAA-VSiNW NMOS is more sensitive to VSiNW diameter variation than DSSB GAA-VSiNW PMOS (Figure 7.4 (a)). Looking at Figure 7.8 (b), the integration of dopant segregation into SB GAA-VSiNW NMOS has little impact on V_T since there is very slight difference in the extracted V_T values between DSSB and SB GAA-VSiNW NMOS.

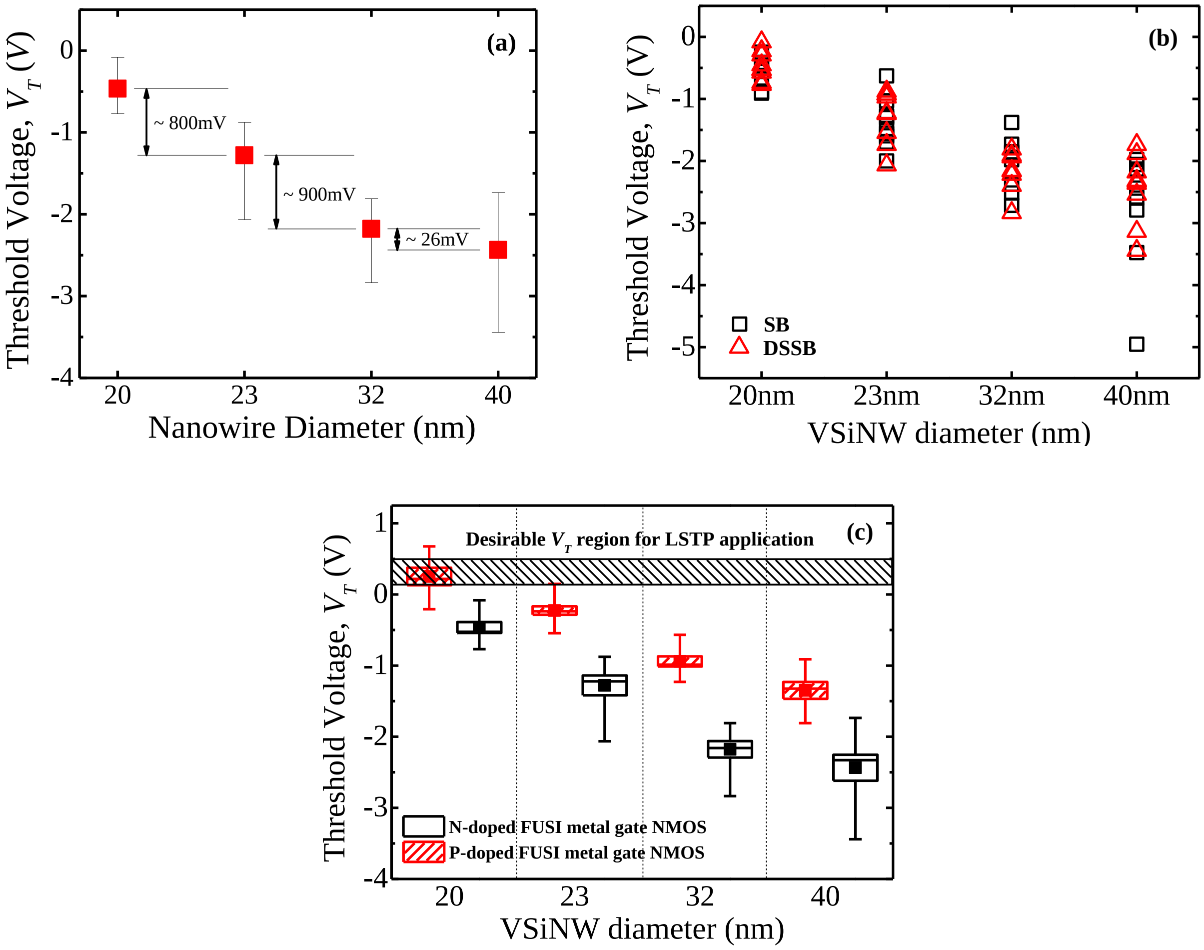


Figure 7.8 (a) Threshold Voltage (V_T) variation as a function of VSiNW diameter and (b) comparison of V_T between DSSB and SB GAA-VSiNW NMOS.

From Figure 7.8, it can be observed that it is feasible to tune the device V_T by varying the VSiNW diameter. As mentioned in Section 7.2, we study another method to optimize V_T of DSSB GAA-VSiNW NMOS. In this new method, for the first time, we attempt to coalesce opposite doped FUSI metal gate and VSiNW diameter variation to obtain the ideal

V_T range for Low Standby Power (LSTP) applications. The results are shown in Figure 7.8 (c). P–doped (specifically BF_2 – doped) FUSI metal gate increase the V_T between 0.72 V to 1.05 V. Moreover, DSSB GAA-VSiNW NMOS with p – doped FUSI gate is able to attain the desired V_T values for LSTP application at VSiNW diameter = 20nm and some devices with VSiNW diameter = 23nm also manage to realize the minimum V_T requirement for LSTP application. Thus, through further fine-tuning, the range of VSiNW diameter required to achieve LSTP application can be expanded.

7.4.3 Effective Schottky Barrier Height

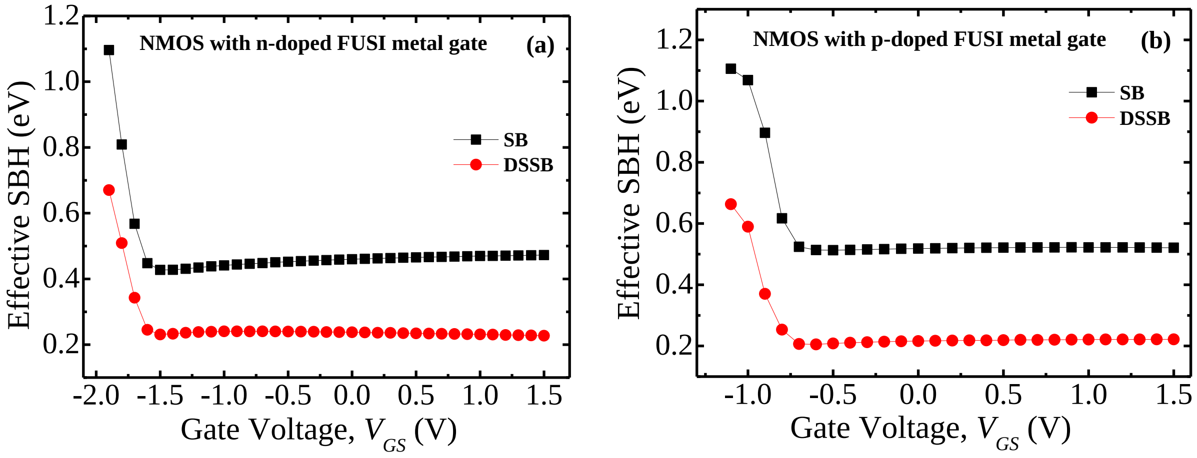


Figure 7.9 Effective plotted as a function of gate voltage, V_{GS}, for SB GAA-VSiNW NMOS and DSSB GAA-VSiNW NMOS. Both devices have n-doped FUSI metal gate.

The extracted effective SBH (Φ_{beff}) for SB GAA-VSiNW and DSSB GAA-VSiNW NMOS are depicted in Figure 7.9. In Figure 7.9 (a), both devices have n-doped FUSI metal gate and in Figure 7.9 (b), both devices have p-doped FUSI metal gate. All devices are measured with VSiNW diameter = 40nm. Generally, the Φ_{beff} of both devices decrease rapidly at the start of a raising V_{GS}. Upon reaching threshold voltage, V_T, the modulation of Φ_{beff} becomes more gradual and converges to a small value of 0.45 eV (SB NMOS) and 0.23

eV (DSSB NMOS) for V_{GS} > -1.0V in Figure 7.9 (a). From Figure 7.9 (b), Φ_{beff} converges to 0.52 eV (SB NMOS) and 0.22 eV (DSSB NMOS) for V_{GS} > -0.5V. Regardless of gate doping species used, dopant segregation technique managed to achieve ~ 0.2 to 0.3 eV reduction in Φ_{beff}. The drop in Φ_{beff} corresponds well with the increase in I_{DS} observed in Figure 7.6 (a).

The reduction in Φ_{beff} can be attributed to the de-pinning of Fermi level through the replacement of silicon atom at the MS interface with a foreign atom. The new electronegativity difference between the metal silicide and the foreign atoms result in a different dipole moment [7.1]. Besides changing the dipole moment, foreign atoms with extra valence electron (Group V element) or lacking of a valence electron (Group III element) can induce image charges on the metal side. Therefore, due to additional electrons, Si surface becomes negatively charged when Si atoms are replaced by Group V atoms. At the same time, positive charges on the metal side are formed and this leads to an electrostatic field between the charge pair that tends to reduce Φ_{beff} of electrons. The same is true for Group III atoms whereby negative charges are induced in the metal side which helps in lowering Φ_{beff} of holes.

7.5 Electrical Characteristics of GAA-VSiNW DSSB NMOS with p – doped FUSI metal gate measured against GAA-VSiNW DSSB NMOS with n – doped FUSI metal gate

7.5.1 Transfer and Output Electrical Characterization

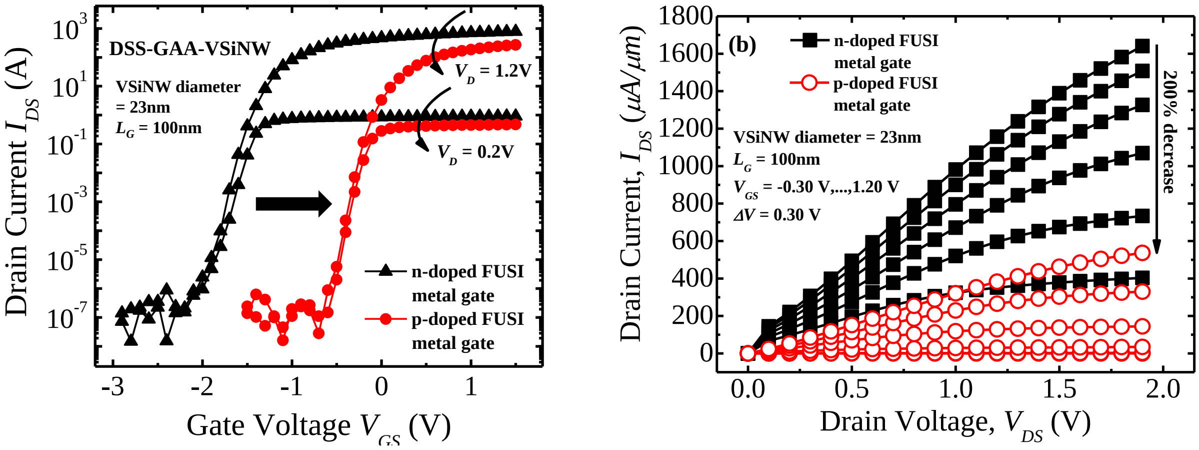


Figure 7.10 (a) I_{DS} – V_{GS} and (b) I_{DS} – V_{DS} electrical characteristics comparison of DSSB GAA-VSiNW NMOS with n-doped FUSI metal gate and p-doped FUSI metal gate.

In this section, we will analyze the results of devices fabricated using the new method and compare the same results with the devices fabricated using the original method.

Figure 7.10 depicts the output and transfer electrical characteristics of DSSB GAA-VSiNW NMOS with (i) n-doped FUSI metal gate and (ii) p-doped FUSI metal gate. Clearly, devices with p-doped FUSI gate exhibited a positive shift of ~ 1.5V as shown in Figure 7.10 (a). This coincides well with the shift in device V_T from Figure 7.8 (c). Due to the increase in V_T, there is a corresponding decrease in the drive current at the same V_{GS}. From Figure 7.10 (b), I_{DS} of DSSB GAA-VSiNW NMOS with p-doped FUSI gate decreases by 200% from ~ 1640 μA/μm to ~ 537 μA/μm at V_{GS} = 1.2V and V_{DS} = 1.9V. In addition, there is clear presence of linear and saturation regions in the I_{DS} - V_{DS} measurements and there is no sub-linear turn-on. This indicates that the channel pinch-off has been reached and Φ_{beff} to electrons is low.

7.5.2 Device current characteristics, Short Channel Performance and Effective Schottky Barrier Height

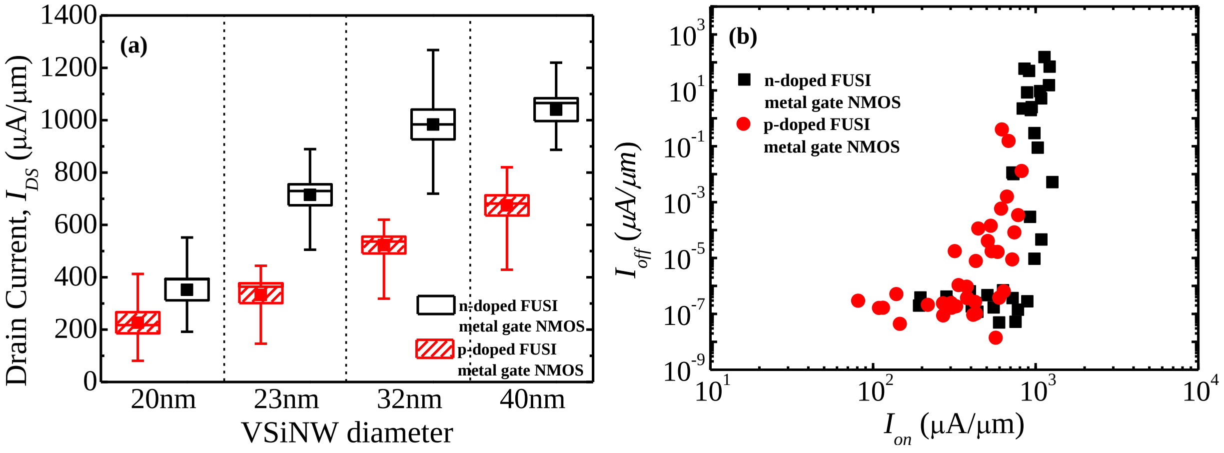


Figure 7.11 (a) Drain current (I_{DS}) of n-doped FUSI metal gate NMOS and p-doped FUSI metal gate NMOS as a function of VSiNW diameter. I_{on}-I_{off} characteristics of both device types are shown in Figure 7.10 (b).

Figure 7.11 (a) plots the extracted I_{DS} of n-doped FUSI metal gate NMOS and p-doped FUSI metal gate as a function of different VSiNW diameter. It is clear that n-doped FUSI metal gate NMOS exhibits higher I_{DS} than p-doped FUSI metal gate NMOS across all the measured VSiNW diameters. This observation is expected since the V_T of p-doped FUSI metal gate NMOS is higher than n-doped FUSI metal gate NMOS as shown in Figure 7.8 (c). In addition, ΔI_{DS} between VSiNW diameter increases with increasing VSiNW diameter.

Figure 7.11 (b) illustrates the $I_{on} - I_{off}$ electrical characteristic of NMOS with p-doped FUSI metal gate compared against NMOS with n-doped FUSI metal gate as a benchmark. It can be observed that the I_{on} values of NMOS with n-doped FUSI gate demonstrated a right shift to higher values even at smaller VSiNW diameter. At 10 pA/µm, p-doped FUSI metal gate NMOS attains I_{on} of ~ 700 µA/µm while its counterpart achieves I_{on} of ~ 1000 µA/µm. This substantiates the findings in Figure 7.11 (a).

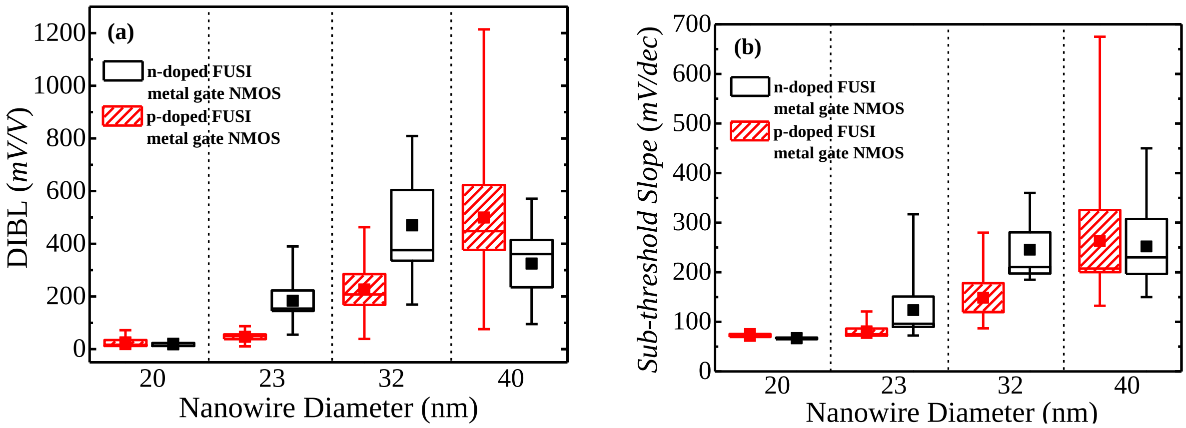


Figure 7.12 (a) DIBL and (b) SS performance of NMOS with p-doped FUSI metal gate compared to NMOS with n-doped FUSI metal gate as benchmark. Both SCE characteristics are plotted as a function of VSiNW diameter.

In Figure 7.12, SCE performance is plotted as a function of VSiNW diameter. Setting NMOS with n-doped FUSI metal gate as a benchmark, NMOS with p-doped FUSI metal gate exhibits better performance in terms of both DIBL (Figure 7.12 (a)) and SS (Figure 7.12 (b)) characteristics across all the measured VSiNW diameters. At VSiNW diameter = 20nm, excellent SCE performance is achieved with DIBL ~ 3 mV/V and SS ~ 63 mV/decade. The SS values are better than reported in literature [7.2, 7.3].

Coupled with the alteration of Schottky barrier shape due to MS junction scaling [7.4]., the dopant segregation technique further aids in Schottky barrier thinning. Thus, it is not surprising that small VSiNW diameter is able attain such outstanding results.

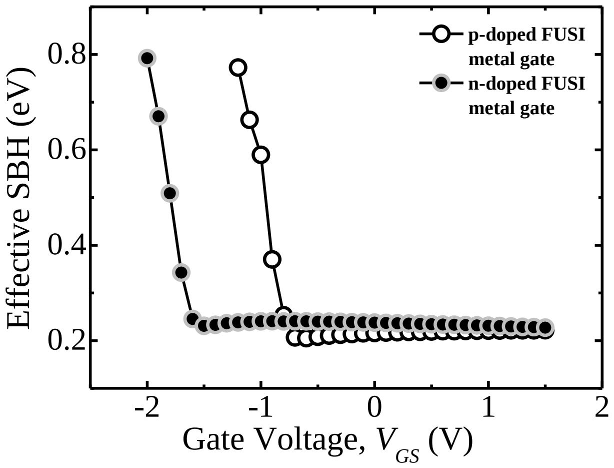


Figure 7.13 Effective SBH (Φ_{beff}) comparison between NMOS with p-doped FUSI metal gate and NMOS with n-doped FUSI metal gate (benchmark).

Figure 7.13 shows the extracted Φ_{beff} of NMOS with p-doped FUSI metal gate compared with NMOS n-doped FUSI metal gate as benchmark. Disparity in Φ_{beff} is expected since both devices have different V_T value. Clearly, both devices demonstrated a rapid decrease in Φ_{beff} as V_{GS} begins to rise and upon reaching V_T, Φ_{beff} modulation gradually decreases and Φ_{beff} eventually converges at 0.22 eV. This implies that the change in gate doping species has no impact on Φ_{beff} and the process is well controlled.

7.6 Chapter Summary

We have fabricated DSSB PMOSFET and NMOSFET using GAA-VSiNW architecture. In the first part of this chapter, setting SB GAA-VSiNW PMOS as benchmark, the electrical characteristics, SCE performance and V_T tuning of DSSB GAA-VSiNW PMOS are measured. It is found that DSSB GAA-VSiNW PMOS demonstrated a 39% increase in I_{DS} measured at V_{GS} = -1.5 V and V_{DS} = -2.7 V. In terms of I_{on} – I_{off} characteristics, at I_{off} = 10 pA/µm, DSS GAA-VSiNW PMOS (1160 µA/µm) showed a 66% increase in I_{on} with respect to SB GAA-VSiNW PMOS (700 µA/µm).

Furthermore, DSSB GAA-VSiNW PMOS is able to achieve SS performance close to ideal while DIBL shows consistently better performance than SB GAA-VSiNW PMOS. In addition, V_T fine-tuning is achieved through alteration of VSiNW diameter with smaller VSiNW diameter giving more negative V_T and larger VSiNW diameter giving more positive V_T. Moreover, minimal difference is discovered in the extracted V_T values for both DSSB and SB GAA-VSiNW PMOS devices.

In the second part of this chapter, using SB GAA-VSiNW NMOS as benchmark, we have explored the electrical characteristics and SCE performance of DSSB GAA-VSiNW NMOS. We discovered that, from electrical transfer characteristics, the drive current (I_{DS}) of DSSB GAA-VSiNW NMOS improves by only 12% at V_{GS} = 1.2 V and V_{DS} = 1.9 V but the improvement is lower than DSSB GAA-VSiNW PMOS. At the same time, leakage current (I_{off}) is constant at 6.5 x 10^{-6} µA/µm for both DSSB and SB GAA-VSiNW NMOS. In terms of DIBL and SS performance, DSSB GAA-VSiNW NMOS presented mixed results with smaller VSiNW diameter providing better SCE performance but vice versa for larger VSiNW diameter.

Furthermore, it is discovered that VSiNW diameter < 20nm, DSSB GAA-VSiNW NMOS with p-doped FUSI gate is able to achieve the ideal V_T range for LSTP application. We have also demonstrated that Φ_{beff} to electrons, regardless of gate doping species, reduces by ~ 0.2 eV (from 0.45 eV to 0.22 eV) by integrating dopant segregation technique with SB S/D.

In the last part of this chapter, we have investigated the impact of opposite gate doping on the electrical and SCE performance of DSSB GAA-VSiNW NMOS. It is found that, due to the increase in V_T, DSSB GAA-VSiNW NMOS with p-doped FUSI gate showed lower drive current than DSSB GAA-VSiNW NMOS with n-doped FUSI gate across all measured VSiNW diameters and ΔI_{DS} increases with increasing VSiNW diameter. In terms of SCE performance, NMOS with p-doped FUSI gate revealed improvements over NMOS with n-doped FUSI gate. Lastly, Φ_{beff} to electrons for both types of device converged to the same value of 0.22 eV.

7.7 References

[7.1] L. Geng, B. Magyari-Kope and Y. Nishi , "Image Charge and Dipole Combination Model for the Schottky Barrier Tuning at the Dopant Segregated Metal/Semiconductor Interface," *IEEE Electron Device Letters* , vol. 30, p. 963, 2009.

[7.2] Y. K. Chin, K. L. Pey, N. Singh, G. -Q. Lo, K. H. Tan, C. -Y. Ong and L. H. Tan, "Dopant-Segregated Schottky Silicon-Nanowire MOSFETs With Gate-All-Around Channels," *IEEE Electron Device Letters*, vol. 30, no. 8, pp. 843-845, 2009.

[7.3] J. W. Peng, S. J. Lee, G. C. A. Liang, N. Singh, S. Y. Zhu, G. -Q. Lo and D. -L. Kwong, "Improved carrier injection in gate-all-around Schottky barrier silicon nanowire field-effect transistors," *App. Phys. Lett.*, vol. 93, p. 073503, 2008.

[7.4] G. D. J. Smit, S. Rogge, and T. M. Klapwijk, “Scaling of nano-Schottky-diodes”, *App. Phys. Lett.*, vol. 81, pp. 3852-3854, 2002.

CHAPTER 8
CONCLUSIONS AND RECOMMENDATIONS FOR FURTHER RESEARCH

8.1 Conclusions

This work is dedicated to the study of VSiNW MOSFETs with a focus on junction scaling and S/D engineering for advancing MOSFET technology. To achieve GAA-VSiNW MOSFET, it is of great importance to research on the feasibility of fabricating VSiNW infrastructure via conventional CMOS process methodology. This research project began with detailed process steps to illustrate the fabrication procedure to achieve VSiNW structure on bulk Si substrate. Furthermore, fabrication details of producing VSiNW Schottky Barrier (SB) and Dopant Segregated SB (DSSB) VSiNW diodes are revealed.

Following that, discussion is focused on gate stack formation for GAA-VSiNW MOSFETs and subsequently, fabrication steps to create SB and DSSB GAA-VSiNW MOSFETs with tuned FUSI metal gate are discussed.

To investigate silicide intrusion into VSiNW and silicide surface morphology, nickel was used to silicide VSiNW tip by using 2 different RTA methods, namely 1-step RTA at 450^0C and 2-step RTA at 275^0C followed by 450^0C, to form SB and DSSB VSiNW diodes. It is found that RTA temperature is a crucial factor in determining silicide intrusion length and silicide morphology whereby a 2-step RTA method produces shorter intrusion length with a relatively flat silicide/silicon interface but a 1-step RTA method produces longer intrusion length with a V-shaped silicide/silicon interface. The silicide formed using either of the RTA methods is identified to be $NiSi_2$. From our analysis, we found that SB and DSSB VSiNW diodes fabricated using 1-step RTA produces higher reverse current and lower forward current than 2-step RTA. Furthermore, VSiNW diodes fabricated using 2-step RTA coupled with DS technique produces ideality factor, closer to ideal value, and lower effective SBH (Φ_{beff}) to electrons.

GAA-VSiNW MOSFET of various diameter with highly-doped S/D and poly-gate were fabricated using ‘top-down’ CMOS compatible technology. PMOS devices exhibited high I_{on}/I_{off} ratio > 10^5 and high drive current ~ 400 µA/µm. Relatively large DIBL and SS values are extracted but SCE performance improves with smaller VSiNW diameter. Furthermore, fine-tuning of device V_T can be achieved by altering VSiNW diameter. With regards to NMOS devices, excellent electrical characteristics were observed with high I_{on}/I_{off} ratio > 10^8, DIBL value of 6 mV/V and SS value of 70 mV/decade. The SB GAA-VSiNW NMOS is comparable to reported NMOSs with planar, GAA-VSiNW and lateral SiNW with GAA architectures. V_T tuning of NMOS is achieved by combining small VSiNW diameter and opposite doped poly gate. Average positive V_T shift of ~ 1V is extracted from devices with various VSiNW diameter and largest V_T shift (+1.5 V) occurs at VSiNW diameter = 23nm.

To achieve junction scaling and drive current enhancement, GAA-VSiNW MOSFET with SB S/D is developed. SB PMOS with p-doped FUSI gate demonstrated high drive current ~ 650 µA/µm with low leakage current ~ 10^{-6} µA/µm and outstanding SCE characteristics with DIBL ~ 5mV/V and SS ~ 75mV/decade. A comparison of $I_{off} - I_{on}$

characteristics with the report in recent literature frames the results of the fabricated devices in favorable terms even against planar counterparts. Varied V_T values can be achieved through VSiNW diameter adjustment. SB NMOS with n-doped FUSI gate exhibited drive current ~ 1000 µA/µm with leakage current ~ 10^{-14} µA/µm. Good SCE performance with DIBL ~ 29 mV/V and SS ~ 70 mV/decade. Enhanced tunneling current caused by small metal junction size is the cause of high drive current. Coupled with small VSiNW diameter, opposite doped (p-doped) FUSI gate is used to create positive shift in device V_T to attain Low Standby Power (LSTP) V_T range. However, more positive V_T value resulted in lower drive current and SCE characteristics remains fairly similar between both gate types. Extracted Φ_{beff} to electrons is ~ 0.45 eV for n-doped FUSI gate and 0.51 eV for p-doped FUSI gate.

To further enhance drive current of SB GAA-VSiNW MOSFETs, dopant segregation is introduced into SB GAA-VSiNW MOSFETs. With segregated dopants, DSSB PMOS devices exhibited 39% increase in drive current (~ 1500 µA/µm) and better SCE characteristics than SB PMOS devices. In addition, the use of dopant segregation did not have an adverse effect on the device V_T. DSSB NMOS showed a lower 12% increase (~ 1640 µA/µm) in drive current with aggravated SCE performance as compared to SB NMOS. Similar to PMOS devices, segregated dopants at MS interface have no impact on device V_T. In terms of Φ_{beff} to electrons, DSSB NMOS showed a reduction of ~ 0.2 eV in SBH. Concurrently, DSSB GAA-VSiNW NMOS with p-doped FUSI gate is developed to attain the desired V_T for LSTP application. But the opposite doped FUSI gate caused a positive V_T shift and resulted in 200% decrease in drive current (~ 1640 µA/µm vs. ~ 537 µA/µm). Apart from the low drive current, excellent DIBL ~ 3 mV/V and SS ~ 63 mV/decade is achieved and Φ_{beff} to electrons did not suffer any adverse effect due to change in gate doing species.

8.2 Recommendations for Further Research

Several areas of research related to vertical Si nanowire Schottky Barrier MOSFETs can be studied to enhance the possibility of integration into the mainstream process in the semiconductor industry. These include:

1) Analysis of gate oxide charges, VSiNW defects and localized electron density

Additional electrical measurements using split C-V method, Kelvin probe force microscopy (KPFM) and scanning tunneling spectroscopy (STS) to further investigate the intrinsic properties of SB GAA-VSiNW and DSSB GAA-VSiNW MOSFETs. By using the split C-V method, possible VSiNW defects and gate oxide charges can be measured and analyzed. Mobility and ballistic efficiency in the SiNW channel can be calculated from the C-V curves.

Furthermore, KPFM can be used to map out the work function variation of the NiSi far away from the MS interface to region close to MS interface. This could help to understand the composition and electronic state of the local structures at the MS interface, especially for DSSB devices. In addition, STS technique is able to map out the localized density of electrons at the MS interface and at the VSiNW sidewall. This allows us to understand how the electron density varies between SB and DSSB devices.

However, the main challenge to implementing these techniques on VSiNW comes from the VSiNW landscape. Instruments must be customized to accommodate to the SiNW vertical sidewalls instead of the horizontal or planar planes in conventional SiNW and planar devices. Additional measurements would include reliability and failure analysis measurements to determine VSiNW MOSFETs' failure modes.

2) *Ab-initio simulation study of dopant interaction and diffusion at metal/Si interface*

Dopant atoms interaction with Si defects such as self-interstitial and vacancy can be studied using ab-initio simulation. Furthermore, detailed simulation, subject to simulation fine-tuning, of various dopants before experiments to establish the efficiency of various dopant segregation can be performed to reduce resource wastage. Ab-initio simulations can also be used to investigate the dopant atom diffusion since the VSiNW is subjected to various temperature-related processes during fabrication. In addition, simulations can provide information about the random dopant fluctuation effect on VSiNW device performance when small VSiNW diameter is used.

3) *SBH engineering using other elements or methods*

Strain engineering, coupled with VSiNW architecture, can be viewed as a method to lower Φ_{beff}. To achieve global strain, strained capping nitride can be used through additional of wafer processing steps. To attain localized tensile or compressive strain in S/D regions, SiGe stressors through epitaxial growth can replace Si S/D. In addition, forming germanosilicide on SiGe S/D would also result in lower Φ_{beff}. Another method to obtain localized strain in S/D is to implant Ge into PMOS and C into NMOS S/D before silicidation to enhance electron mobility. Besides strain engineering, exotic elements, such as sulphur, selenium and chlorine have been researched as dopant segregation species.

4) Dopant activation in Si nanowire

Dopant activation has been studied extensively in bulk Si substrate but little research is done on nanowires. Compared to bulk Si substrate, Si nanowire has large surface to volume ratio. This implies that surface states can have considerable effect on nanowire performance. Therefore, it is of interest to look into the surface effects and to explore the choices of dopants that are most beneficial to nanowire semiconductor devices.

5) Enhancement of drain current performance of VSiNW transistors with opposite gate doping type

It has been established from the current study that short channel effects can be mitigated by having opposite gate doping type compared to channel doping. However, this will increase the threshold voltage and reduce the drain current performance. Therefore, it will be important to discover methods to improve the drain current to levels similar to state-of-the art MOSFETs.

6) *Integration of other metals with VSiNW structure to further improve device performance and study of high frequency performance*

The choice of metal for this study is Ni. However, there are other possibilities to explore other rare earth metals such erbium, platinum and ytterbium to further improve the device performance. Studies of high frequency performance can also be initiated to analyze the effect of overlap capacitance between gate and source/drain due to the non-self-aligned process.

AUTHOR’S PUBLICATIONS

Journal publications:

1. Weijie Lu, Kin Leong Pey, Xinpeng Wang, Xiang Li, Zhixian Chen, Singh Navab, Kam Chew Leong, Chee Lip Gan, and Chuan Seng Tan, “Vertical Silicon Nanowire Diode with Nickel Silicide Induced Dopant Segregation”, Japanese Journal of Applied Physics, vol. 51, pp. 11PE08, 2012.

Conference presentations:

1) Y. K. Chin, K. L. Pey, N. Singh, W. J. Lu, G. Q. Lo, L. H. Tan, X. C. Wang, H. Y. Zheng, “Si Nanowire Gate-All-Around FET with Excimer-Laser Annealed Dopant Segregated Schottky (DSS) Source Drain”, CACS 2010 (poster).
2) W. J. Lu, K. L. Pey, N. Singh, K. C. Leong, G. Q. Luo, D. L. Kwong, “Vertical silicon nanowire Schottky Barrier diodes with Dopant Segregation”, ICMAT 2011 (poster)
3) W. J. Lu, K. L. Pey, N. Singh, K. C. Leong, G. Q. Luo, D. L. Kwong, “Vertical Silicon Nanowire Diode with Schottky Barrier Tip: Effect of Dopant Segregation”, ICYRAM 2012 (poster)
4) W. Lu, K. L. Pey, N. Singh, K. C. Leong, Q. Liu, C. L. Gan, G. Q. Lo and D. -L. Kwong, “Analysis of vertical nanostructure diode performance: Effect of nickel silicide formation process and dopant segregation”, MRS 2012 (presentation)
5) W. Lu, K. L. Pey, Z. X. Chen, X. P. Wang, K. C. Leong and C. S. Tan, “Reducing contact resistance of nickel silicided vertical silicon nanowire tip with titanium capping layer”, ICMAT 2013 (poster)
6) W. Lu, K. L. Pey, X. P. Wang, K. C. Leong, C. S. Tan, G. Q. Luo, D. L. Kwong, “Demonstration of VT tuning in Gate-All-Around (GAA) Vertical Silicon Nanowire (SiNW) Transistor with Schottky Barrier source/drain (SB-S/D)”, INEC 2013 (poster)