# SRAM Devices and Circuits Optimization toward Energy Efficiency in Multi-$V_{th}$ CMOS

**Bo Wang[a,b], Jun Zhou[b], and Tony Tae-Hyoung Kim[a]**

[a]School of Electrical and Electronic Engineering, Nanyang Technological University

Address: 50 Nanyang Avenue, Singapore, Singapore 639798

[b]Institute of Microelectronics, Agency for Science, Technology and Research

Address: 11 Science Park Road, Singapore Science Park II, Singapore 117685

**Corresponding author: Bo Wang**

School of Electrical and Electronic Engineering, Nanyang Technological University

Address: 50 Nanyang Avenue, Singapore, Singapore 639798

Phone: (65) 6592-1844, fax: (65) 6316-4416, email: bwang6@e.ntu.edu.sg

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## ABSTRACT

Minimum-energy-driven circuit design is highly required in numerous emerging applications such as mobile electronics, wireless sensor nodes, implantable biomedical devices, etc. Due to high computing capability requirements in such applications, SRAMs play a critical role in energy consumption. This paper presents SRAM energy analysis utilizing multi-threshold (multi-$V_{th}$) voltage devices and various circuit techniques for power reduction and performance improvement, and suggests optimal device combinations for energy efficiency improvement. In general, higher-$V_{th}$ devices are preferred in the cross-coupled latches and the write access transistors for reducing leakage current while lower-$V_{th}$ devices are desired in the read port for implementing higher performance. However, excessively raised $V_{th}$ in the write paths, i.e. the cross-coupled latches and the write access transistors, leads to slower write speed than read, quickly nullifying improved energy efficiency. In this work, the energy efficiency improvement of 6.24× is achieved only through an optimal device combination in a commercial 65 nm CMOS technology. Employing power reduction and performance boosting techniques together with the optimal device combination enhances the energy efficiency further up to 33×.


## 1. INTRODUCTION

Recently emerging micro-watt applications, such as micro-sensor networks, handset electronics, implantable biomedical devices, etc place a primary criterion on minimum energy consumption or high energy efficiency to prolong battery life time [1]-[5]. To improve the energy efficiency, operating voltage (VDD) in these applications is positioned

near or below threshold voltage ($V_{th}$), known as the near- or sub-threshold region. However, design of ultra-low voltage digital and memory circuits is highly required for achieving this ultra-low energy goal. Particularly, the design of ultra-low voltage SRAMs remains significantly challenging due to the additional constraints such as high sensitivity to process-voltage-temperature (PVT) variations, smaller cell stability, smaller voltage margin, and prevailing leakage current [6].

Various design techniques have been developed for ultra-low voltage SRAM design. SRAM cells with decoupled cell nodes from read bitlines have been widely accepted as an SRAM cell solution due to their improvement in cell stability [7]-[15]. Elimination of disturbing current from the read bitlines to the cell nodes makes the read-mode cell stability identical to the hold-mode stability. Half-select is another challenging issue pertinent to cell stability. A half-select-free wordline driver scheme and a write-back scheme were proposed at the cost of additional devices in each local wordline driver and data path [10], [11]. To minimize the impact of the half-select problem without sacrificing too much silicon area, a pulsed wordline scheme has been proposed [12]. The pulsed wordline reduces the time period where SRAM cell nodes are disturbed, accordingly improving dynamic cell stability. To improve write margin, a boosted wordline voltage scheme is commonly adopted in design to strengthen the write devices [13]. Another design constraint to be considered is readability, which is mainly limited by the read bitline swing. To improve bitline sensing capability, design techniques including bitline leakage reduction [13]-[15], bitline equalization [16], [17], bitline leakage compensation [18], and bitline sensing with redundant sense amplifiers [19] have been published. Standby leakage reduction is also critical in enhancing energy efficiency. Bitline leakage elimination

techniques [19], [20], leakage reduction schemes using sleep transistors [21], [22] and multi-$V_{th}$ devices [23], [24] have been introduced.

SRAMs can dissipate significant power and consume high energy in numerous applications, such as DSP, MCU and etc. Consequently, energy efficiency is a topmost parameter for SRAMs embedded in micro-watt systems. While numerous research works have been conducted for minimizing SRAM energy consumption, research on the utilization of multi-$V_{th}$ devices for minimum energy-driven SRAMs has been rarely executed. The main challenge in the design of ultra-low voltage SRAMs with multi-$V_{th}$ is to reduce leakage and dynamic current without degrading performance. In decoupled SRAM cells, higher-$V_{th}$ devices are preferred in write paths and data storage to reduce leakage current, and lower-$V_{th}$ devices are used in read paths to achieve better performance. However, this can generate excessively slower write operation than read operation if $V_{th}$ of the devices in the write paths is too high compared to that of the devices in the read ports. This work examines how to improve the energy efficiency of SRAMs with multi-$V_{th}$ devices. Optimal device combinations will be analyzed for maximizing energy efficiency. We will also present the effects of various SRAM design techniques on enhancing the energy efficiency with multi-$V_{th}$ devices. The rest of the paper is organized as follows. In section 2, we will analyze the energy consumption of SRAMs. The optimal $V_{th}$ for maximum energy efficiency will be discussed in section 3. Section 4 explains design techniques that can enhance the energy efficiency. Finally, we will draw summary and conclusion in section 5.

## 2. ANALYSIS OF SRAM ENERGY

Energy efficiency is a paramount design criterion in emerging ultra-low power applications. Supply voltage scaling has been the most widely accepted method for energy efficiency improvement. SRAMs, however, require additional considerations such as array structures, active-switching, and leakage energy. Although dual-$V_{th}$ and multi-$V_{th}$ schemes have been utilized for power reduction [23], [24], minimum energy-driven device selections have been rarely visited. In this section, we will analyze SRAM energy minimization considering the option of multi-$V_{th}$ devices. The functionality of all SRAMs is guaranteed by simulation, even at the condition of the lowest supply voltage.

### *2.1. SRAM Energy Modeling*

The occurrence of minimum energy operating point is determined by the correlation of power and performance. Energy consumption of an SRAM can be separated into two components: switching energy, also known as dynamic energy, and leakage energy known as static energy. Fig. 1 shows a simplified SRAM array with highlighted critical parameters relevant to the energy analysis. An 8T decoupled SRAM cell [25] is employed due to its popularity in ultra-low voltage SRAM design. The effect of an optimal device selection on the energy of SRAM peripheral circuits is insignificant compared to that on SRAM arrays. Therefore, peripheral circuits such as decoding blocks, column multiplexers for read and write operations, sense amplifiers and write drivers are excluded in this energy analysis.

The total energy ($E_{total}$) of the SRAM array can be expressed by

$$E_{total} = E_{switching} + E_{leakage} \quad (1)$$

Here, $E_{switching}$ represents the dynamic energy consumed by switching activities. $E_{leakage}$ is the static energy consumption coming from the leakage current in the SRAM cells. $E_{switching}$ is the summation of the switching energies during read operation and write operation, which can be expressed as below.

$$\begin{aligned} E_{switching} &= P_{Read}\left(C_{RWL} \times V_{DD}^{2} + k \times P_{Low} \times C_{RBL} \times V_{DD}^{2}\right) \\ &+ P_{Write}\left(C_{WWL} \times V_{DD}^{2} + \frac{k}{m} C_{WBL} \times V_{DD}^{2}\right) \end{aligned} \quad (2)$$

Here, $P_{Read}$ is the probability of read operation, $P_{Low}$ is the probability of reading data '0' during read operation, and $P_{Write}$ is the probability of write operation. Note that no switching activity occurs in the read bitlines when the read data is '1'. As shown in Fig. 1, the read energy is associated with the wordline capacitance ($C_{RWL}$) and the bitline capacitance ($C_{RBL}$). Note that multiple read bitlines ($k$) will be discharged during read operation due to the shared read wordline. Read data also affects the switching energy since the read bitlines are only discharged with the read data of '0'. Similarly, the write energy is primarily determined by the write wordline capacitance ($C_{WWL}$) and the write bitline capacitance ($C_{WBL}$). The switching write bitline capacitance is determined by the number of columns ($k$) and the multiplexing ratio ($m$). One write bitline in a pair switches regardless of write data. Therefore, the write energy is independent of the write data.

The static energy ($E_{leakage}$) of the SRAM array is given by

$$\begin{aligned} E_{leakage} &= V_{DD} \times I_{Leakage} \times T \\ &= V_{DD} \times N \times \left[ I_{SN} \times e^{\frac{|V_{GS}|-|V_{thn}|}{nV_T}} + I_{SP} \times e^{\frac{|V_{GS}|-|V_{thp}|}{nV_T}} \right] \\ &\times (1 - e^{\frac{-V_{DS}}{V_T}}) \times T \end{aligned} \quad (3)$$

where, $I_{Leakage}$ is the total leakage current, $N$ is the number of SRAM cells, $I_{SN}$ and $I_{SP}$ are technology scaling parameters for the NMOS and PMOS devices, $V_{GS}$ is the gate-to-source voltage, $V_{DS}$ is the drain-to-source voltage, $V_{thn}$ and $V_{thp}$ are the device threshold voltage of the NMOS and PMOS transistors, $n$ is related to the sub-threshold slope, $V_T$ is the thermal voltage, and $T$ is the time to finish a computation. For simplicity, we assume that the sub-threshold current only consists of the drain current in the sub-threshold region.

### *2.2. Effects of Supply Voltage Scaling and Threshold Voltage on Energy Efficiency*

As shown in the above equations, the energy consumption is highly sensitive to the supply voltage (VDD) and device threshold voltage. In circuit designers' point of view, the simplest method of improving energy efficiency is to scale supply voltage (VDD). Lowering VDD improves energy efficiency when the dynamic energy is dominant over the static energy. However, the static energy becomes significant when the supply voltage becomes near or below the device threshold voltage level. In this region, even though the leakage current still decreases by lowering VDD, the exponentially degraded performance quickly increases the overall static energy. As a result, the combination of the dynamic energy and the static energy generates an operating point that minimizes the total energy consumption. This point is generally found in the region where VDD is below the device threshold voltage.

Higher-$V_{th}$ devices have been utilized in the design of ultra-low power SRAMs due to the exponentially decreased leakage current. The ultra-low power is obtained at the cost of degraded performance. However, compared to the effect of the supply voltage scaling on the energy efficiency, the effect of the threshold voltage on the energy efficiency is not straightforward. Increasing the threshold voltage decreases the amount of leakage current

exponentially. However, increased threshold voltage degrades performance exponentially, too. Consequently, the impact of the threshold voltage alteration on the static energy is determined by the ratio of the reduced leakage current to the increased operating delay. If the gain in the leakage reduction is larger than the loss in the performance, the overall energy efficiency improves by replacing with higher-$V_{th}$ transistors. Contrarily, if the impact of delay degradation exceeds the gain in leakage suppression, the energy efficiency improves when lower-$V_{th}$ devices are adopted.

### *2.3. Effects of Multi-$V_{th}$ Devices on SRAM Energy*

Circuit design using multi-$V_{th}$ devices have been widely used in digital circuits. Critical paths are preferred to be designed using lower-$V_{th}$ devices while higher-$V_{th}$ devices are favored in non-critical paths. The higher-$V_{th}$ devices in non-critical paths reduce the leakage current and the lower-$V_{th}$ devices maintain the required performance. However, this cannot be easily employed in conventional 6T SRAMs since the SRAM performance is directly related to the amount of leakage current. Instead, multi-$V_{th}$ devices have been usually adopted to achieve balanced design parameters such as cell stability, performance, and write margin. Unlike the conventional 6T SRAMs, decoupled SRAM cells with separated read and write ports can accomplish the energy efficiency improvement by employing higher-$V_{th}$ devices in the data storage and low-$V_{th}$ devices in the performance limiting read port.

Fig. 2 illustrates a sample 8T dual-port SRAM cell designed with higher-$V_{th}$ devices in the cross-coupled latch and the write access transistors, and lower-$V_{th}$ devices in the read port. This is straightforward when considering that read operation is slower than write operation. In this case, the energy model described in Section 2.1 has to be modified. The

energy equation for the switching energy remains the same while the leakage energy equation is written by

$$\begin{aligned} E_{leakage} &= I_{Leakage} \times V_{DD} \times T \\ &= \begin{bmatrix} I_{SN_HV} \times e^{\frac{|V_{GS}|-|V_{thn_HV}|}{nV_T}} + I_{SP_HV} \times e^{\frac{|V_{GS}|-|V_{thp_HV}|}{nV_T}} \\ + I_{SN_LV} \times e^{\frac{|V_{GS}|-|V_{thn_LV}|}{nV_T}} \end{bmatrix} \\ &\times (1 - e^{\frac{-V_{DS}}{V_T}}) \times N \times V_{DD} \times T \end{aligned} \quad (4)$$

where $I_{SN\text{-}HV}$, $I_{SP\text{-}HV}$, and $I_{SP\text{-}LV}$ are technology scaling parameters for the higher-$V_{th}$ NMOS, higher-$V_{th}$ PMOS and lower-$V_{th}$ NMOS, $V_{thn\text{-}HV}$, $V_{thp\text{-}HV}$ and $V_{thn\text{-}LV}$ are the device threshold voltage of the higher-$V_{th}$ NMOS, higher-$V_{th}$ PMOS and lower-$V_{th}$ NMOS. Compared to the previous leakage energy equation, three different types of devices (two types in NMOS and one type in PMOS) determine the cell leakage current. In addition to the leakage current, the time to finish a computation has to be rewritten as

$$T = \max(T_{read},\ T_{write}) \quad (5)$$

where $T_{read}$ is the time to finish a read operation and $T_{write}$ is the time to complete a write operation. If the write operation with higher-$V_{th}$ devices takes longer time that the read operation with lower-$V_{th}$ devices, $T_{write}$ has to be used in the energy estimation. This indicates that increasing the threshold voltage of the higher-$V_{th}$ devices over an optimal point quickly lose the energy efficiency improvement. In the following section, we will discuss the optimal SRAM cell design toward energy minimization using multi-$V_{th}$ devices.

## 3. MINIMUM ENERGY-DRIVEN SRAM DESIGN USING MULTI-$V_{TH}$ DEVICES

SRAM energy consumption is determined not only by supply voltage selection but also by device selection. It has been demonstrated that minimum energy of an SRAM is found in the sub-threshold region. In this section, we will investigate the impact of device selection on minimum energy consumption. Table I summarizes the relevant design parameters used in the analysis. An SRAM array in commercial 65nm CMOS technology is simulated over various combinations in device selection. We use three device types (LVT, SVT, and HVT) available in the selected CMOS technology. Read delay is measured at points of crossing '$0.5 \times VDD$'. Write delay to data flip point is used in the analysis. Instant read-after-write operation is not considered and it could be solved by [26]. Process and temperature variations affect device characteristics. However, they are not included and this work will primarily focus on the effect of multi-$V_{th}$ devices on SRAM energy minimization.

### *3.1. Analysis of SRAM Energy without Multi-$V_{th}$ Devices*

To minimize the leakage power consumption, SRAM cells have employed higher-$V_{th}$ devices at the cost of performance degradation. However, the degraded performance caused by the selection of higher-$V_{th}$ devices also affects energy consumption. Therefore, careful device selection has to be considered for improving energy efficiency using multi-$V_{th}$ devices. Fig. 3 demonstrates the SRAM energy consumption designed by different device types sweeping supply voltage. When the supply voltage is in the super-threshold region, dynamic energy is dominant compare to leakage energy. Therefore, lowering supply voltage reduces overall energy consumption. As expected, the minimum point of each device selection is formed at a point where the supply voltage is around the threshold voltage of the devices. However, the minimum energy level using HVT (0.16) or SVT (0.12)

is higher than that of using LVT (0.08), which explains that selecting SVT or HVT for improving power dissipation is not the best choice in terms of energy efficiency. This result can be explained as follows. Compared to LVT, SVT and HVT decrease leakage current and increase read delay. However, since the increase in the read delay is more significant than the decrease in the leakage, the SRAM arrays using SVT and HVT consume more energy overall.

### *3.2. Analysis of SRAM Energy with Multi-$V_{th}$ Devices*

Transistors with different threshold voltages are offered in recent CMOS technologies. This provides circuit designers with more opportunities to optimize circuits in performance, power, and energy. While higher energy efficiency can be achieved through a proper device selection, an undesirable device selection will produce lower energy efficiency. Fig. 4 shows the impact of undesirable device selections on SRAM energy. HVT devices are employed in the read port to limit the overall performance. In this case, using SVT and LVT devices does not improve the energy efficiency because SVT and LVT devices in write paths dissipate more power without improving the overall performance.

In general, higher-$V_{th}$ devices are employed in non-critical paths for reducing power while lower-$V_{th}$ devices are adopted in critical paths for achieving high performance [27]. Conventionally, read paths are considered as critical paths, limiting overall performance as shown in Fig. 5. Write paths are non-critical due to the faster operation speed than read paths. Therefore, lower-$V_{th}$ devices have to be incorporated in read operation, and higher-$V_{th}$ devices can be employed in write paths. However, as supply voltage decreases, the write speed with higher-$V_{th}$ devices degrades faster than the read speed with lower-$V_{th}$,

eventually making the write paths critical. In this case, overall energy consumption needs to be estimated carefully since the degraded critical path delay from write operation becomes more substantial. Fig. 6 explains the impacts of device selection on the critical path delay. Using the result of Fig. 3, LVT devices are used in the read port for enhancing the SRAM performance. When SVT devices are used in the write paths, the delay of the write paths is still smaller than that of the read paths using LVT devices. As a result, using SVT in the write paths will decrease leakage current while maintaining the same performance, consequently reducing energy consumption. However, when HVT devices are adopted in the write paths, the delay of the write paths will be larger than that of the read paths at lower supply voltages. This occurs because the write delay increases exponentially from a higher supply level while the read delay starts to augment exponentially at lower VDD. Specifically, read delay is larger than write delay in a single $V_{th}$ SRAM cell. For this MTCMOS cell, read delay is larger initially. However, HVT devices have higher $V_{th}$ than LVT devices. Thus current from the write paths degrades sharply when VDD is near the $V_{th}$ of HVT devices (~0.6V) whereas it is still super-threshold for LVT devices. The significantly degraded write performance will lose the benefit of utilizing higher-$V_{th}$ for enhancing energy efficiency. Fig. 7 demonstrates simulated SRAM energy of various device combinations. As expected from Fig. 6, the minimum energy of an SRAM array using SVT in write paths shows better efficiency due to the reduced leakage current. However, in case of using HVT in write paths, the minimum energy point is formed at the supply voltage of 0.4V and the energy increases dramatically. Fig. 8 demonstrates the leakage current of the SRAM arrays under different device combinations. Although the selection of SVT in the write

paths and LVT in the read paths has the lowest minimum energy level, it consumes the second largest leakage current.

Fig. 9 summarizes the normalized energy consumption of various device combinations. The energy variation of up to 6.24× exists, which emphasizes the importance of careful device selection. Apart from energy efficiency, leakage reduction by device selection is equally important. SRAMs with less leakage power dissipation are more demanded in battery-powered applications, especially in sleep mode. The corresponding leakage currents of the devices combinations described in Fig. 9 are shown in Fig. 10. Note that the device combination for the highest energy efficiency (SVT(W)-LVT(R)) is not the best in terms of leakage. In addition, the device combination with the highest leakage (LVT(W)-LVT(R)) has the second highest energy efficiency. Therefore, careful device selections have to be made depending upon the system requirements. If an SRAM stays in an idle or sleep mode for majority of the life time, the leakage current becomes more significant than the energy efficiency during computational operations. However, the energy efficiency will be more significant if the SRAM workload becomes substantial. A design option is implementing the write paths with different device types. By separating the write access transistors and the latch with individual $V_{th}$ devices, write delay and leakage current can be both improved. Similarly, MTCMOS methodology is also applicable to 6T SRAM cell. But the transistor size has to be carefully selected to maintain cell stability.

## 4. DESIGN TECHNIQUES FOR SRAM ENERGY EFFICIENCY IMPROVEMENT UTILIZING MULTI-$V_{TH}$ DEVICES

As discussed earlier, SRAM energy is determined by multiple parameters such as leakage current, dynamic current and critical path delay. Various SRAM design techniques have been proposed to improve the above parameters. In this section, we will explore the effects of various SRAM design techniques on energy efficiency under multi-$V_{th}$ devices. Design techniques such as a column-interleaved scheme and a read buffer foot control scheme for leakage reduction, and boosting schemes for performance improvement will be considered. The energy overhead of utilizing the two techniques is negligible compared to the improvement they make. Other write performance boosting techniques such as data retention voltage collapsing and negative bitline scheme are also effective and applicable.

### *4.1. Effect of Power Reduction Techniques on SRAM Energy*

Fig. 11 illustrates 8T decoupled SRAMs employing the column-interleaved scheme [28] and the read buffer foot control scheme [14]. In Fig. 11 (a), CSL is shared by SRAM cells in each column. During non-read operation CSL is held to VDD to eliminate the read bitline leakage from pre-charged RBL to CSL. During read operation, CSL in selected columns is pulled down to GND and RBL is conditionally discharged based upon the stored cell data. However, in unselected columns, CSL remains at VDD, which eliminates not only the bitline leakage in the read port but also the unwanted RBL discharging. Read buffer foot technique was proposed to reduce bitline leakage and enhance read bitline sensing margin. As Fig. 11 (b) depicts, FOOT is shared by SRAM cells in each row. It can be either pulled-up to VDD to eliminate leakage current flowing to the read bitline or statically connected to GND to form a discharging path from read bitline to ground. During non-read operation, FOOT is connected to VDD to eliminate the leakage through the read port. During read operation,

only FOOT in the selected row is pulled down to GND, and all RBLs are conditionally discharged based upon the data in the selected row. Compared to the column-interleaved scheme, the key advantage of the read buffer foot control scheme is to provide enhanced RBL sensing margin at low supply voltage. However, the column-interleaved scheme demonstrates better performance in point of power reduction since it eliminates the unwanted dynamic discharging as well as the RBL leakage. Therefore, in this analysis, we will estimate the effect of the column-interleaved scheme on the overall SRAM energy. The combination of SVT in write paths and LVT in read paths as shown in Fig. 7 is also assumed in the analysis.

While the RBL leakage is avoided in both of the column-interleaved scheme (Fig. 11 (a)) and the read buffer foot control scheme (Fig. 11 (b)), the dynamic energy reduction is more significant in the column-interleaved scheme, which is primarily determined by the multiplex ratio. Although the selected column dissipates more power due to the discharging of CSL and the internal node in the read port, the elimination of discharging RBL in unselected columns improves the overall SRAM energy. Fig. 12 demonstrates the effectiveness of the column-interleaved scheme on energy efficiency. Simulation shows the energy reduction is proportional to the multiplex ratio. A multiplex ratio of 32 improves the energy efficiency by ~5× compared to the reference design whose device combination has the highest energy efficiency (Fig. 7). In addition, raising the multiplex ratio moves the minimum energy points to higher supply voltages, which is more desirable when considering the larger device variations at lower supply voltages.

*4.2. Effect of Performance Boosting Techniques on SRAM Energy*

At a given SRAM array architecture, device selection has to be made for maximizing performance and minimizing leakage to achieve better energy efficiency. In Fig. 7, the highest energy efficiency is achieved by the combination of SVT in the write paths and LVT in the read paths. Although HVT in the write paths can reduce the leakage more substantially, the exponentially degraded performance in write operation deteriorates the overall energy efficiency much faster. Boosted voltage schemes can be employed for enhancing write performance over read performance (Fig. 13). In this scheme, the voltage of WWL is boosted to a higher voltage than VDD. Consequently, the $V_{GS}$ of the write access transistors increases and the write speed is enhanced accordingly. Fig. 14 demonstrates the change in the SRAM array after utilizing a boosted voltage scheme. As expected, the significant boosting in write performance eliminates the increase in the SRAM energy below the previous minimum energy point and improves the energy efficiency continuously even at lower supply voltages. The gain in the energy reduction expands as the supply voltage decreases. For example, 9.4× improvement was achieved at the supply voltage of 0.2 V. Fig. 15 summarizes the effectiveness of the boosted voltage scheme on various device combinations. The boosting voltage scheme is only useful in HVT(W)-LVT(R) and HVT(W)-SVT(R) whose write operation is slower than read operation at lower supply voltages. It is worth noting that the largest energy reduction is realized in HVT(W)-LVT(R) because the leakage in the write paths is the smallest and the performance is the highest. Compared to SVT(W)-LVT(R) whose energy efficiency is the highest before performance boosting, HVT(W)-LVT(R) consumes 11 % less energy. The relatively small improvement is due to the fact that although significant amount of leakage is reduced from the array by

using HVT, the RBL leakage caused by the LVT devices dominates the overall leakage current. This limits the overall improvement in the energy efficiency.

### *4.3. Combination Effect of Power Reduction and Performance Boosting Techniques*

To maximize the energy efficiency of an SRAM, both leakage reduction and performance improvement need to be achieved at the same time. In this work, the maximum energy efficiency can be obtained from HVT(W)-LVT(R) after adopting the column-interleaved scheme (Fig. 11 (a)) for power reduction and the boosted voltage scheme (Fig. 14) for performance improvement. Fig. 16 illustrate the SRAM energy of HVT(W)-LVT(R) after employing the aforementioned design techniques. Note that two design techniques improve the normalized minimum energy from 0.131 to 0.006 (~22×). Finally, the benefit of multi-$V_{th}$ devices incorporated with the power reduction and performance boosting techniques are summarized in Fig. 17. When additional circuit techniques are not employed, the SRAM with the optimal device selection (SVT(W)-LVT(R)) consumes 31 % of the SRAM energy designed solely by HVT devices. However, the optimal device selection moves from SVT(W)-LVT(R) to HVT(W)-LVT(R) after adopting the power reduction and performance boosting techniques. Consequently, the energy efficiency improvement of 33× is achieved, which is larger than the energy saving from voltage scaling as shown in Fig. 7.

## 5. CONCLUSION

This paper presents the comprehensive energy analysis of SRAMs under multi-$V_{th}$ devices. Although higher-$V_{th}$ devices are preferred in the write paths for reducing power and energy consumption, a careful device type selection has to be considered to maximize the benefit of utilizing multi-$V_{th}$ devices. Using higher-$V_{th}$ devices in the SRAM write paths

improve energy efficiency when VDD is in the strong inversion region where the write speed with higher-$V_{th}$ devices is still higher than the read speed with lower-$V_{th}$ devices. However, lowering supply voltage degrades the write speed faster than the read speed, eventually leading to slower write operation and losing the benefit of using higher-$V_{th}$ devices in the write paths for power and energy reduction. Therefore, there exists a limitation in the $V_{th}$ difference of the devices used in the write paths and the read paths. In this analysis, using the devices (HVT, SVT, and LVT) available in a commercial CMOS technology, the best device combination for energy minimization is to use SVT devices in the write paths and LVT devices in the read ports. We also explored the effects of several power reduction and performance boosting techniques on SRAM energy efficiency. After employing these techniques, the optimal device combination moves to HVT devices in the write paths and LVT devices in the read paths. This optimal combination improves energy efficiency by 33× compared to the device combination of HVT devices in the write and read paths.

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**Figure Captions**

Figure 1. Simplified SRAM array diagram for energy analysis.

Figure 2. Schematic of an 8T decoupled SRAM cell with multi-$V_{th}$ devices.

Figure 3. Normalized energy of three SRAMs designed by three different device types (i.e. HVT, SVT and LVT) available in the commercial 65nm CMOS technology. All transistors in one SRAM have the same $V_{th}$.

Figure 4. Impact of device selection on normalized energy of three SRAMs. Note that HVT devices are employed for read port in all three SRAMS. Rest transistors in each SRAM cell adopt one device type.

Figure 5. Normalized delay values of SRAM read and write operations designed with HVT devices.

Figure 6. Comparison of read delay (LVT) with write delay implemented with multi-$V_{th}$ devices (SVT and HVT).

Figure 7. Normalized energy of SRAMs utilizing three different device types (i.e. HVT, SVT, and LVT) for data storage and write paths. Note that LVT devices are used in read port.

Figure 8. Comparison of leakage current over various device combinations.

Figure 9. Summary of normalized minimum energy consumption over various device combinations.

Figure 10. Summary of normalized leakage current over various device combinations.

Figure 11. 8T decoupled SRAM cells with leakage reduction techniques: (a) column-interleaved, and (b) read buffer foot control.

Figure 12. Effect of column-interleaved scheme on SRAM energy. The reference design is using SVT devices in the write paths and LVT devices in the read path, which is also shown in Fig. 7.

Figure 13. Simplified 8T SRAM schematic adopting boosted wordline scheme.

Figure 14. Improvement of energy efficiency by boosting write performance. Additional energy overhead induced by the boosting voltage generation is not considered in this simulation.

Figure 15. Comparison of normalized minimum energy consumption with write performance techniques.

Figure 16. Improvement of minimum energy after adopting the column-interleaved scheme (Fig. 11 (a)) and the boosted voltage scheme (Fig. 13). Multiplex ratio of 32 is assumed.

Figure 17. Comparison of normalized SRAM minimum energy consumption.

**Table Captions**

Table I. Parameter summary for energy analysis simulation.

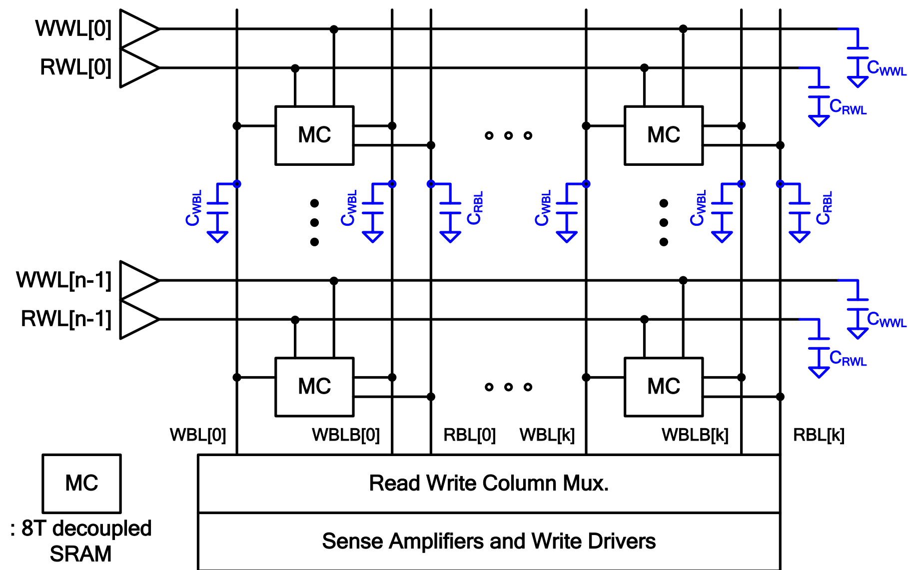


**Fig. 1.** Simplified SRAM array diagram for energy analysis.

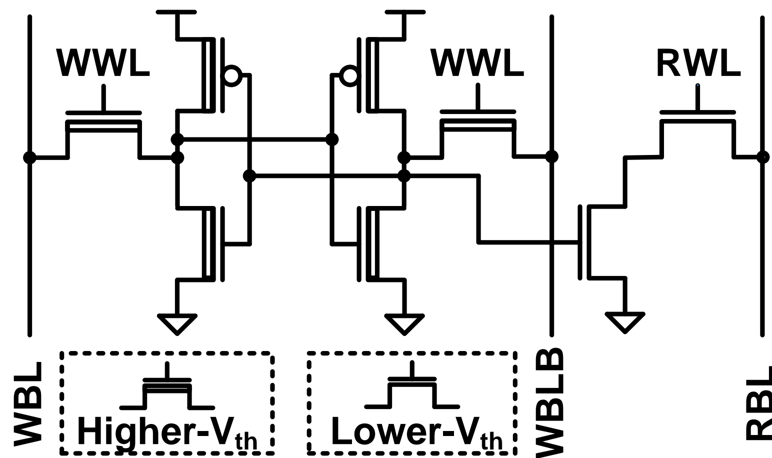


**Fig. 2.** Schematic of an 8T decoupled SRAM cell with multi-$V_{th}$ devices.

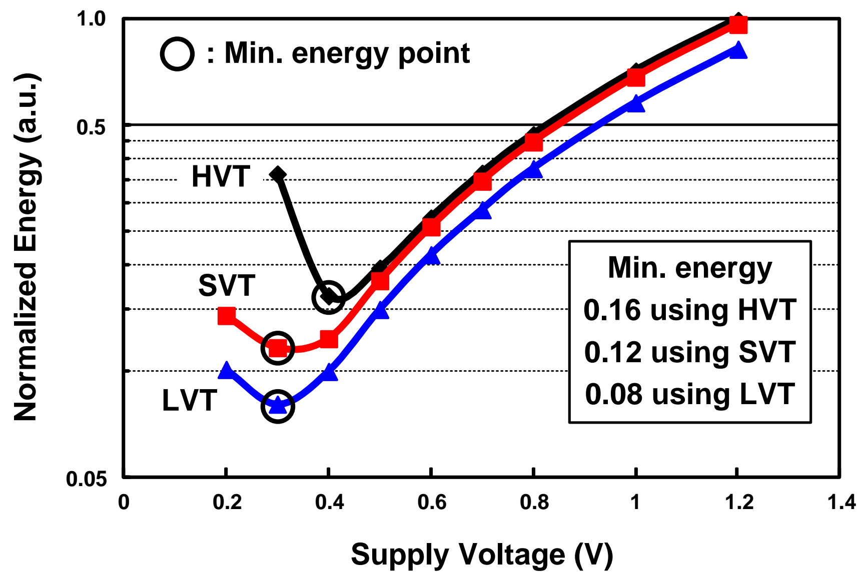


**Fig. 3.** Normalized energy of three SRAMs designed by three different device types (i.e. *HVT*, *SVT*, and *LVT*) available in the commercial 65nm CMOS technology. All transistors in one SRAM have the same $V_{th}$.

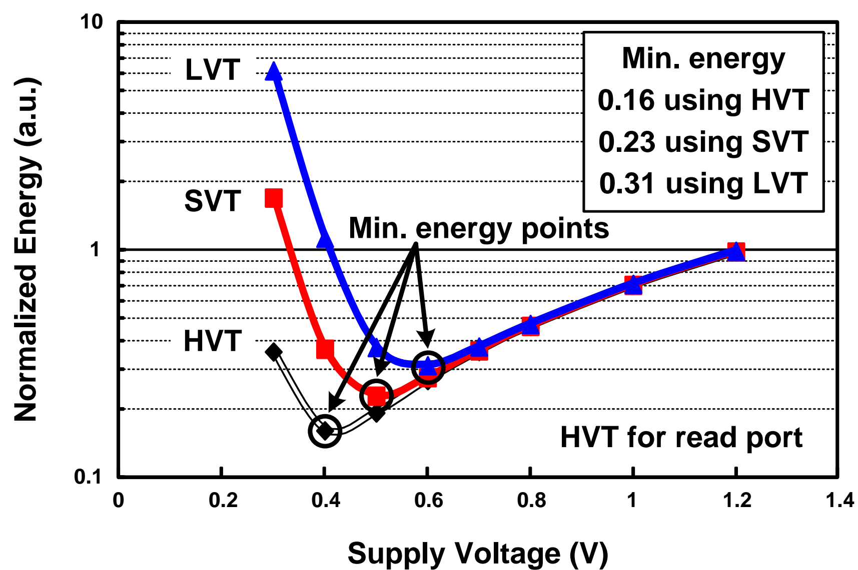


**Fig. 4.** Impact of device selection on normalized energy of three SRAMs. Note that *HVT* devices are employed for read port in all three SRAMS. Rest transistors in each SRAM cell adopt one device type.

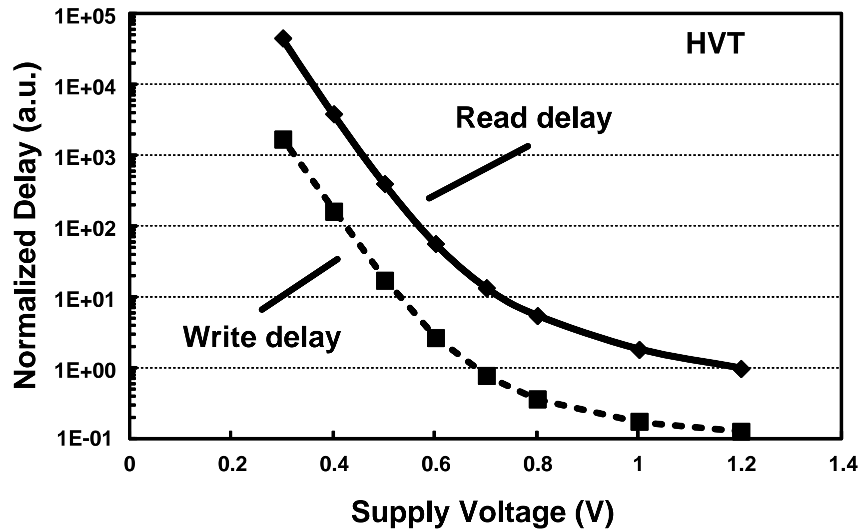


**Fig. 5.** Normalized delay values of SRAM read and write operations designed with *HVT* devices.

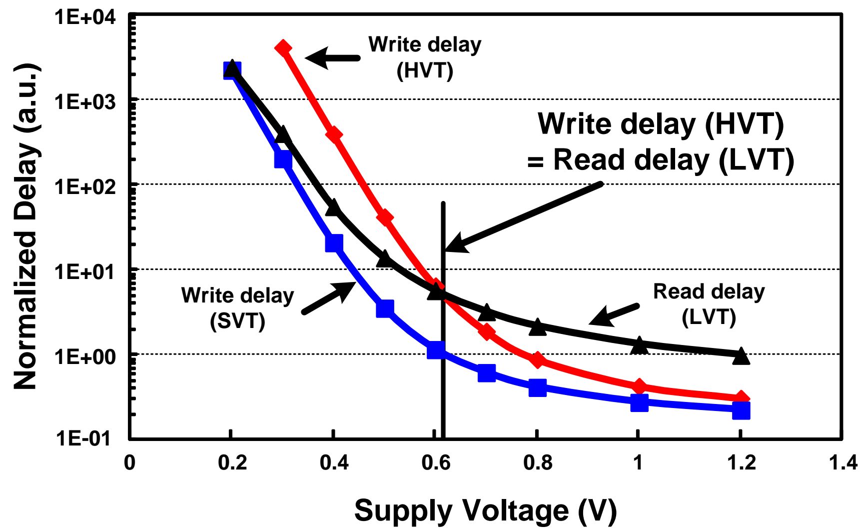


**Fig. 6.** Comparison of read delay (*LVT*) with write delay implemented with multi-$V_{th}$ devices (*SVT* and *HVT*).

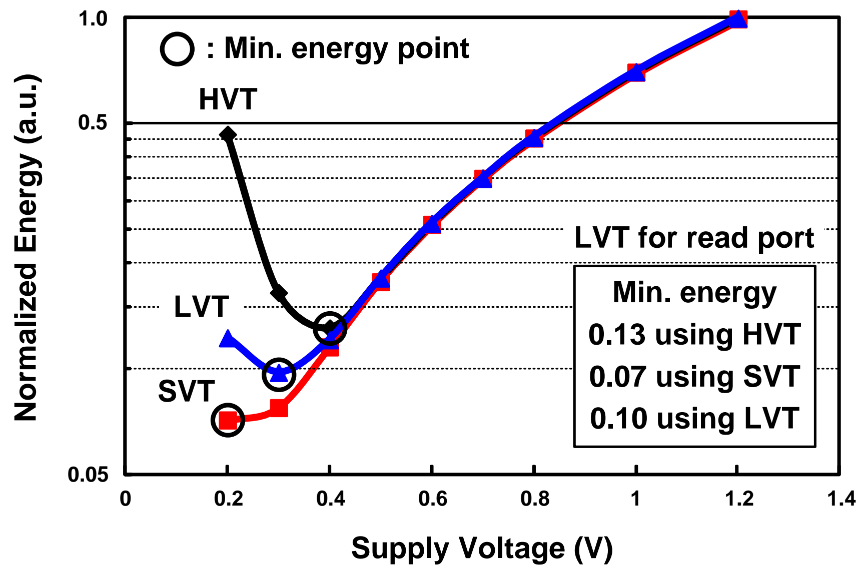


**Fig. 7.** Normalized energy of SRAMs utilizing three different device types (i.e. *HVT*, *SVT*, and *LVT*) for data storage and write. Note that *LVT* devices are used in read port.

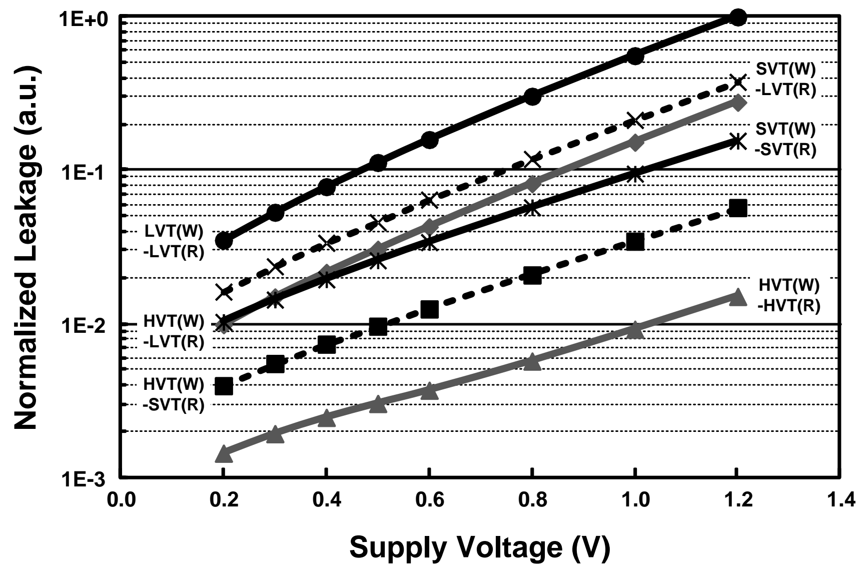


**Fig. 8.** Comparison of leakage current over various device combinations.

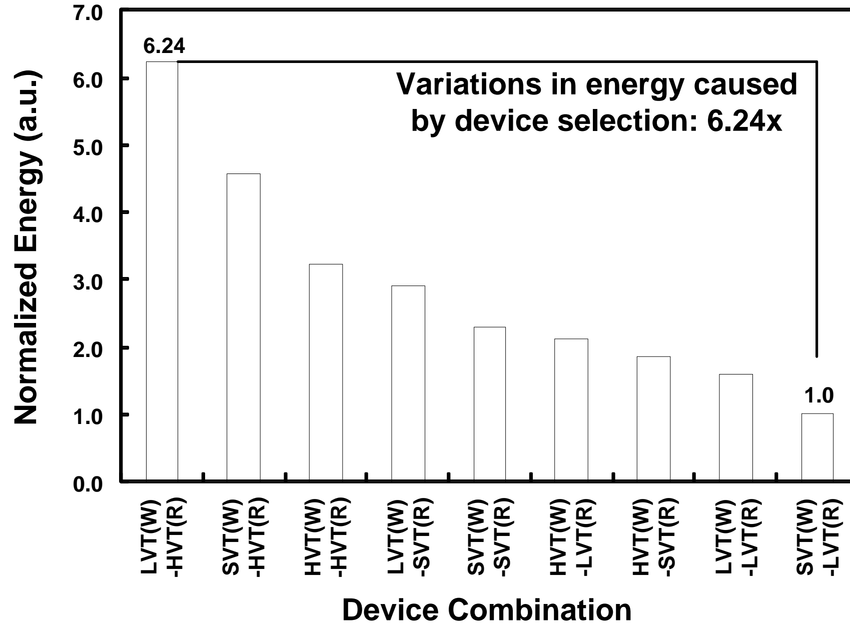


**Fig. 9.** Summary of normalized minimum energy consumption over various device combinations.

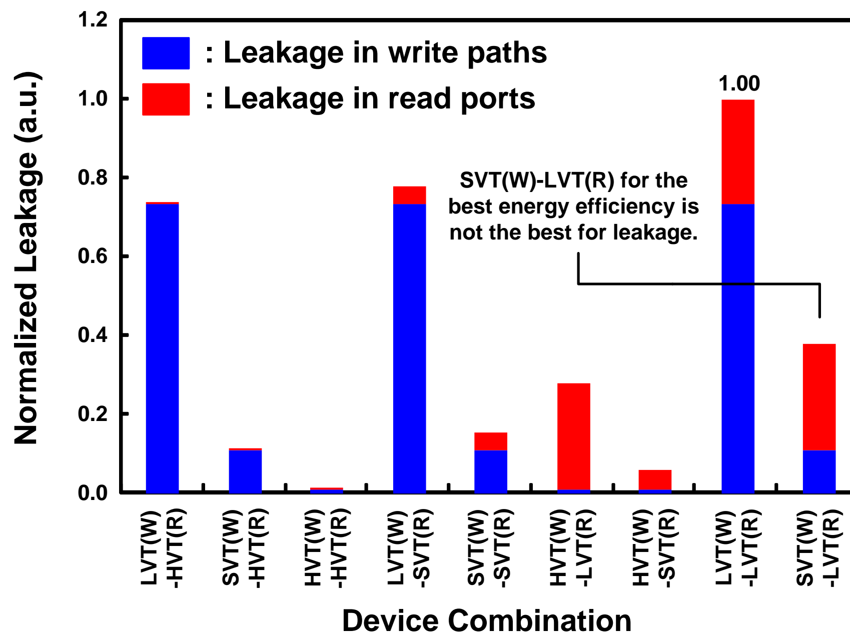


**Fig. 10.** Summary of normalized leakage current over various device combinations.

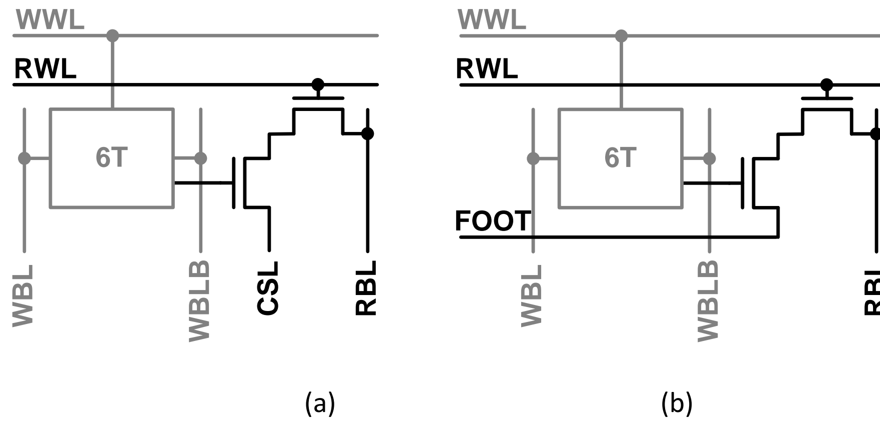


**Fig. 11.** 8T decoupled SRAM cells with leakage reduction techniques: (a) column-interleaved, and (ii) read buffer foot control.

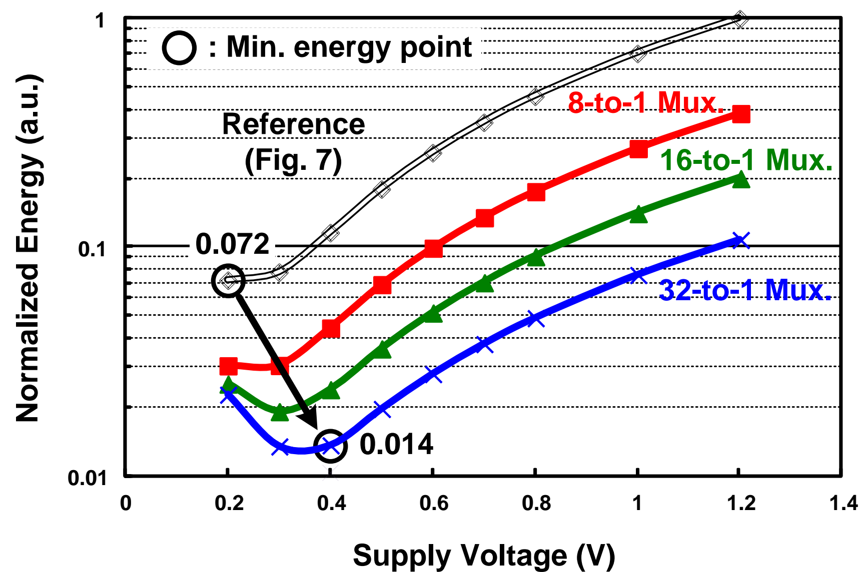


**Fig. 12.** Effect of column-interleaved scheme on SRAM energy. The reference design is using *SVT* devices in the write paths and *LVT* devices in the read path, which is also shown in Fig. 7.

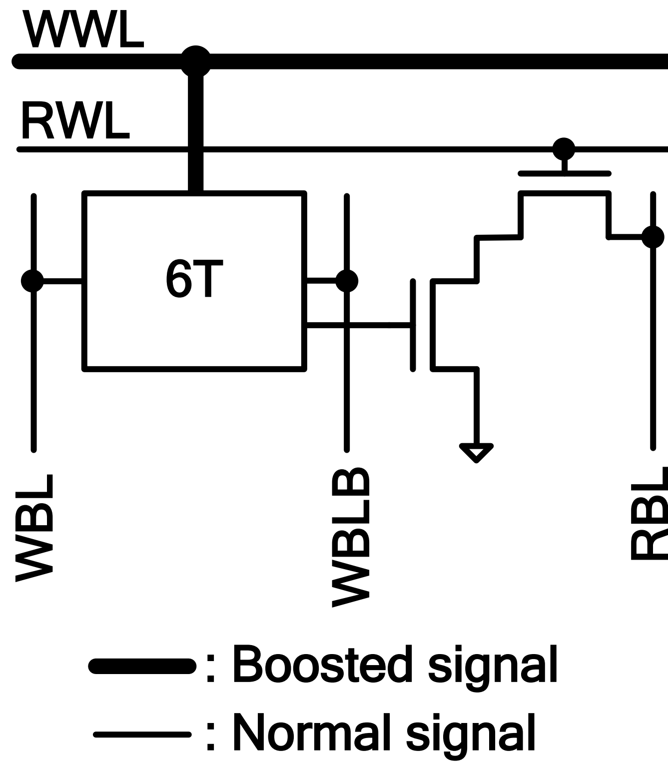


**Fig. 13.** Simplified 8T SRAM schematic adopting boosted wordline scheme.

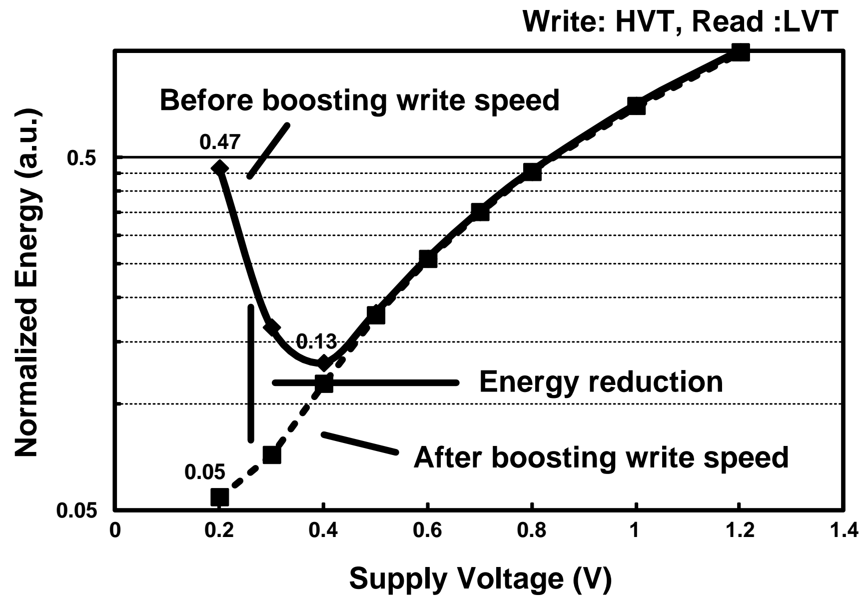


**Fig. 14.** Improvement of energy efficiency by boosting write performance. Additional energy overhead induced by the boosting voltage generation is not considered in this simulation.

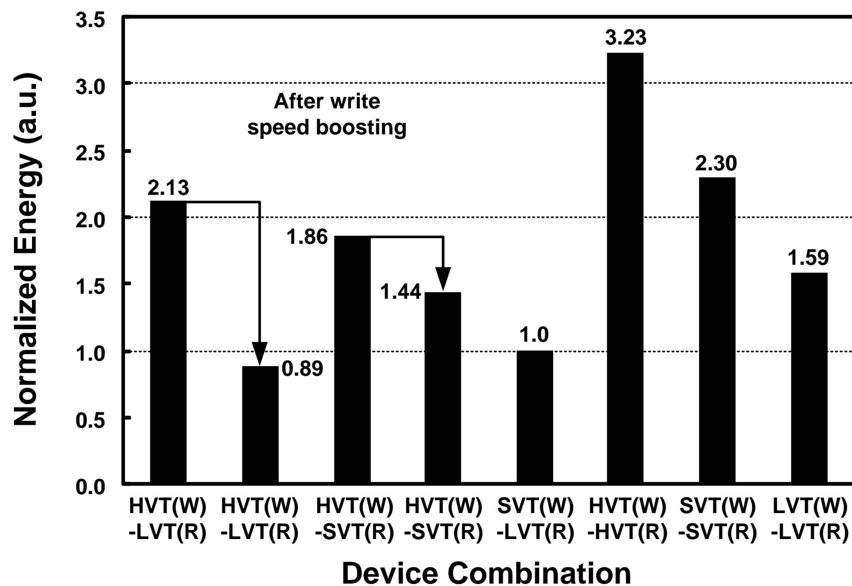


**Fig. 15.** Comparison of normalized minimum energy consumption with write performance techniques.

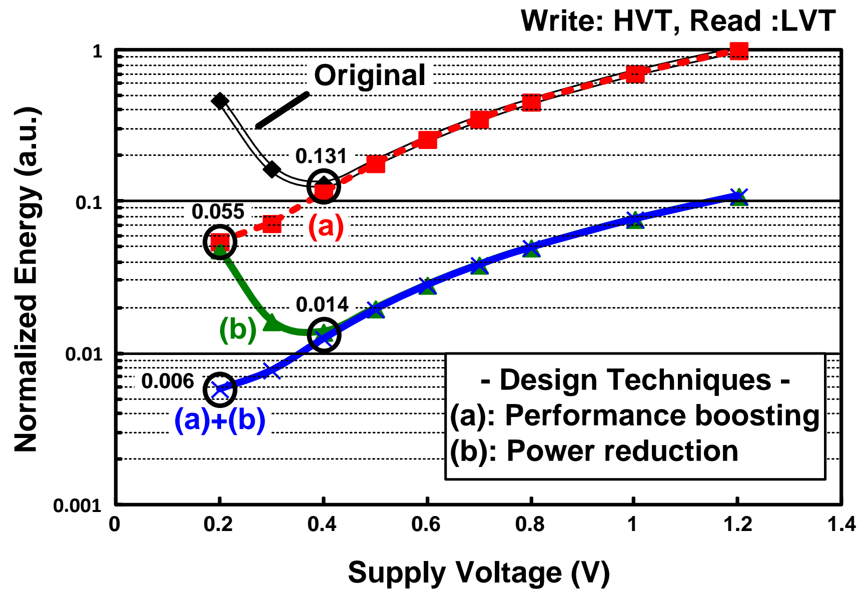


**Fig. 16.** Improvement of minimum energy after adopting the column-interleaved scheme (Fig. 11 (a)) and the boosted voltage scheme (Fig. 13). Multiplex ratio of 32 is assumed.

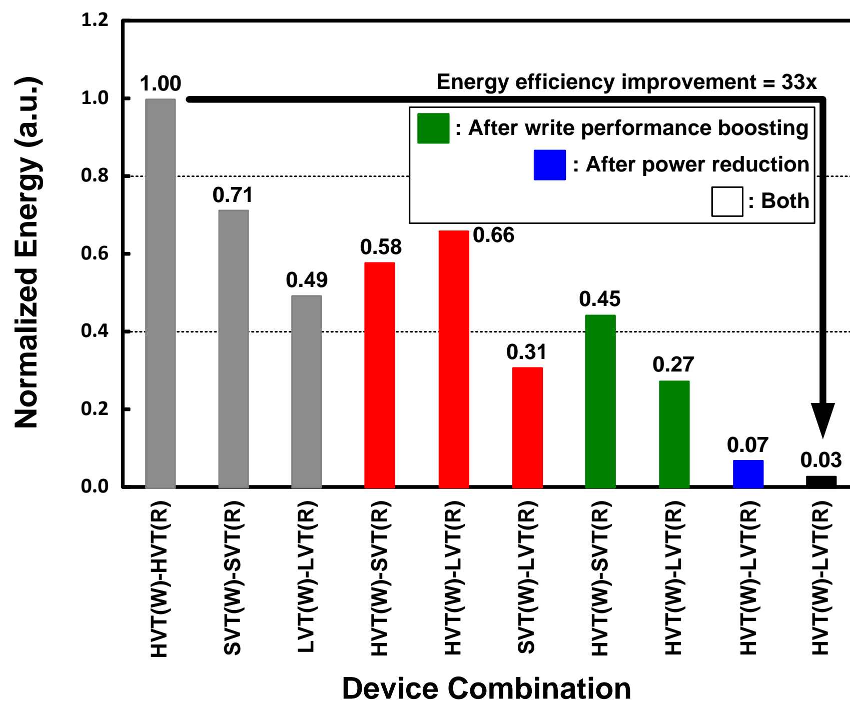


**Fig. 17.** Comparison of normalized SRAM minimum energy consumption.

## Table I

PARAMETER SUMMARY FOR ENERGY ANALYSIS SIMULATION

| Items | Remarks |
|---|---|
| Technology | Commercial 65nm CMOS |
| Array structure | 256 rows × 128 columns |
| SRAM bitcell | 8T decoupled SRAM |
| Devices | LVT, SVT, HVT |
| $V_{th}$ | LVT: 0.28V/–0.2V SVT: 0.37V/–0.31V HVT: 0.61V/–0.56V |
| Read delay | From clock to RBL at $0.5 \times V_{DD}$ |
| Write delay | From clock to data flip point |
| SRAM operation | Read probability = 0.5, (data ‘1’ = 50%, data ‘0’ = 50%), write probability = 0.5 |