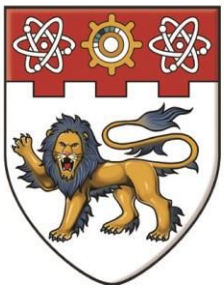

NANYANG TECHNOLOGICAL UNIVERSITY

RF TRANSMITTER USING 33% DUTY CYCLE LO SIGNAL FOR HARMONIC SUPPRESSION

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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RF Transmitter Using 33% Duty Cycle LO Signal for Harmonic Suppression

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ABSTRACT

Due to the increasing demand for communication bandwidth combined with scarceness of free spectrum, spectral efficiency has been a challenge to the development of 4th generation RF communication system. In particular, the Long-Term-Evolution (LTE) standard groups the OFDM subcarriers into Resource Blocks to dynamically allocate within the channel bandwidth. However, during this process, due to the limited linearity of transmit path, harmonic distortion components named counter intermodulation products (CIM) are generated. The CIM products may fall directly or through cross-modulation into the receiver (RX) band, thus degrading the frequency division duplexing performance. CIM products may also fall into the protected bands and violate spectral emission requirement. Recently, CIM products, especially for counter 3rd-order intermodulation products (CIM3) due to 3rd-order nonlinearity in the transmit path, has been recognized as an important design parameter for LTE RF system.

Two main contributors of the CIM3 have been identified in the previous literatures. The first and minor contributor comes from the baseband 3rd-order nonlinearity; the second and major contributor is due to the intermodulation between the wanted signal and the local oscillator (LO) signal's 3rd-order harmonic component. Targeting for the solution of the second contributor, an RF transmitter (TX) employing passive mixer based architecture is demonstrated in previous literature. The 33% duty cycle LO scheme is used since it intrinsically does not have 3rd-order harmonic. Thus the intermodulation with 3×LO (3LO) frequency component is avoided. As a result, CIM3 is suppressed at the RF output. This technique is not sensitive to device matching and calibration is not a pre-requisite. Since 3LO filtering requirement can be alleviated, the bill-of-material cost is reduced.

This thesis is the continuous work of the previous literature to explore the 33% duty cycle LO scheme. An RF transmitter employing 33% duty cycle LO is proposed in this thesis. The implementation of the system in this thesis is based on active mixer approach which is different from previous literature. A wide band test frequency range is also provided in this thesis. Besides, each block design are explained in details in the thesis. This TX prototype was fabricated in GlobalFoundries (GF) RF CMOS 180 nm

process. The TX active core occupies 1.4 mm × 0.5 mm including RF front-end as well as analog baseband. The design was tested on PCB with Rogers 4350. The measurement result shows that the designed TX achieves a power gain of 11 dB when VGA is set to the lowest bit. The operation frequency is from 350 MHz to 1.35 GHz. The output 1 dB compression point is measured at -0.7 dBm and the output 3^{rd}-order intercept point is 8.3 dBm at the frequency of 782 MHz. The measured CIM3 and 3LO frequency component are less than -60 dBc and -45 dBc respectively up to output 1 dB compression point. The designed circuit also shows the consistency for the suppression of CIM3 to be less than -60 dBc over whole operating frequency. The power consumption of this TX is 190.8 mW with 1.8 V supply voltage.

ACKNOWLEDGEMENTS

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CHAPTER 1

Introduction

1.1 Background

Recently the integrated multi-band multi-mode cellular transceivers (TRX) have become a great commercial success. This trend drives the demand for the development of small size RF modules with a higher degree of integration. As the number of bands/modes increases, module counts also increase. As a consequence, surface accusative wave (SAW) filter in transmit path which aims to reduce the out-of-band noise must be removed because it is off-chip, bulky and difficult to configure for multiple bands. To allow removal of SAW filter, the transmitter (TX) out-of-band noise emissions in the receiver (RX) band as well as the protected bands must be minimized. Many efforts have been made to meet the TX out-of-band noise requirement of SAW-less transmitter [1] - [7].

In the 4^{th} generation (4G) cellular system, the requirement for out-of-band noise emissions has become very stringent. RF systems are challenged to afford superior "error vector magnitude" (EVM) which indicates in-channel signal-to-noise ratio (SNR) and low "adjacent channel leakage ratio" (ACLR) which implies out-of-channel emissions. As the data rate continues to increase, second-order circuit impairments, which were not a major design consideration, have become significant in system design.

One example is the Long Term Evolution (LTE) [8]. Several major modifications have been applied to increase spectral efficiency and accommodate the growing demand data rate. Compare with the previous generation, channel bandwidth (BW) of 4G LTE has been expanded to 9 MHz in sub-GHz range (e.g. LTE 10) and 18 MHz in GHz range (LTE 20). Take 4G LTE 20 as an example, for the spectral allocation (Figure 1), transmitter orthogonal frequency division multiplexing (OFDM) subcarriers are grouped into Resource Blocks (RBs). Each RB bandwidth equals to 15 kHz × 12 = 180 kHz. One type of transmitted baseband signal can be a wideband signal which occupies 18 MHz bandwidth. In this case, 100 Resource Blocks of 180 kHz are fully

used (100 RB/full-RB) and the transmitting power at RF are spreading over 18 MHz. The other type of baseband signal can be narrow band, in this case, only single RB (1 RB) or a few consecutive RBs are occupied. When a single RB or a few RBs are transmitted, the transmitter output power is concentrated in a very narrow bandwidth instead of spreading across the whole channel as full-RB transmitting. The spectrum power density thus can be very high.

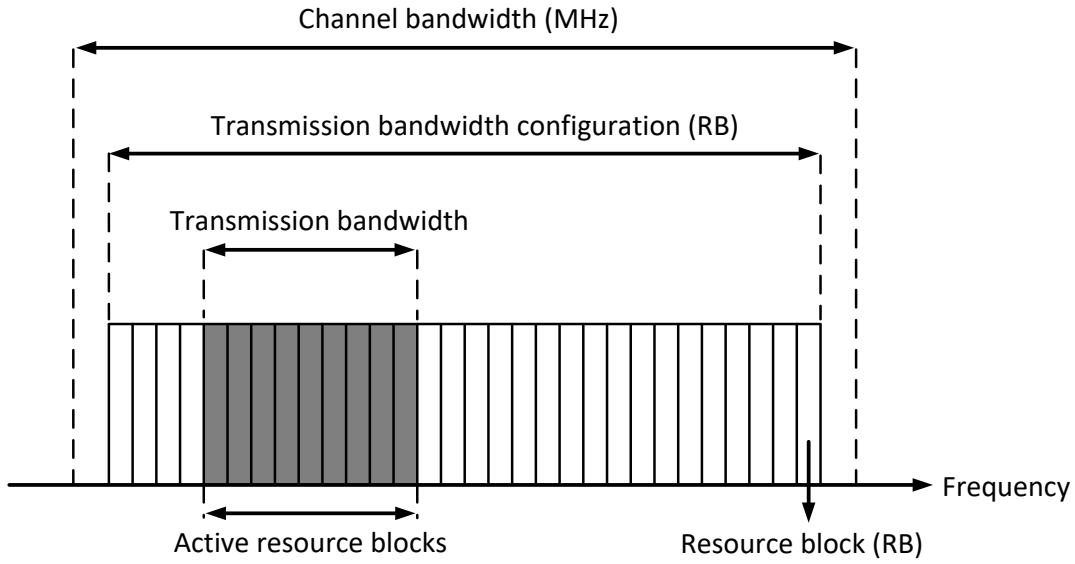


Figure 1. Resource Block allocation in LTE system [8]

The second-order impairment exists owing to high spectrum power density. Due to nonlinearity in TX path, there is the generation of undesired spurs named counter intermodulation products (CIM) such as counter 3rd-, 5th- and 7th-order intermodulation products (CIM3, CIM5, and CIM7) [9] [10]. Suppose the carrier frequency is LO and baseband bandwidth is BB, then CIM3 will locate at LO – 3BB, CIM5 and CIM7 will locate at LO + 5BB and LO - 7BB respectively. Details of generation of CIM products will be discussed in the following chapter. If this single RB or a few RBs are located within the channel bandwidth, it will increase the in-channel noise. On the other hand, if they are located at the channel edge, the strong CIM products may fall into adjacent bands. As a consequence, the transmitter can violate the spurious emission specification. In addition, for frequency division duplexing (FDD) system, the transmitter and receiver are operating at the same time. If the out-of-band noise of TX falls into RX band, the RX sensitivity will be degraded and noise figure is worsened consequently.

1.2 Objectives

This thesis is the continuous work of the previous literatures [11] [12] to explore the application of 33% duty cycle scheme in RF transmitter system for CIM products suppression. Different from the reference work, active mixer based architecture is employed in the proposed RF transmitter (TX) system. 33% duty cycle scheme is also applied targeting at suppression of undesirable counter 3rd-order intermodulation. In this thesis, the detailed design, layout, test and measurement procedure are presented. Besides, the designed system has a broad band test frequency range to verify the theory in active mixer based architecture. Overall, the system is designed towards to simplicity, low cost, easy implementation and adaptable to existing environments.

To be more specific, this work:

1) Designs an RF transmitter which is fabricated with GlobalFoundries (GF) RF CMOS 180nm technology and tested on PCB. The max routing layer used in the design is metal 5 and top power/ground layer is metal 6.
2) Implements an RF transmitter with 33% duty cycle LO signal. The suppression of 3rd-order harmonic of LO signal is validated in the system. The measurement result indicates counter 3rd-order intermodulation product is sufficiently suppressed at the output stage for a large frequency range.
3) Adopts active mixer based architecture. Unlike typical power mixer topology, more stages of PA driver are directly cascaded after the upconverter stage. PA driver is designed for gain and bandwidth optimization. There is no excessive generation of CIM3 caused by intermodulation at PA driver stage. This type of design targets to mitigate the design effort for gain and bandwidth requirements and power consumption of the transmitter.
4) Designs an easily implementable divider circuit to generate the required 33% duty cycle LO signals. This circuit is able to produce 6-phase differential clocks with quadrature phases. The effort is put in both the block and top circuit layout to minimize potential mismatch.

1.3 Organization

The rest of the thesis is organized as follows:

Chapter 2 gives a brief review of the state-of-the-art cellular transmitter architectures including passive mixer based voltage-mode transmitter and active mixer based current-mode transmitter. After that, generation of counter intermodulation products is explained in details, followed by the previous art of harmonic suppression techniques.

Chapter 3 describes the architecture of the designed RF front-end with 33% duty cycle LO signal. The theory of harmonic suppression technique of the proposed architecture is explained.

Chapter 4 presents the design of transmitter core blocks. Mixer element schematic and layout design are firstly discussed. It is followed by the divider circuit design to generate 33% duty cycle LO. Divide-by-2 and divide-by-3 circuits are combined to generate 6-phase differential 33% duty cycle LO signals. Optimization of parasitic parameters in the layout is provided in details. Finally, it presents the design of PA driver and the considerations for the output stage,

In Chapter 5, test and measurement of designed circuit are discussed. It shows the overall layout design and PCB design. It also presents the simulation and measurement results in this chapter.

The final chapter concludes this thesis and gives further suggestions of the transmitter design.

CHAPTER 2

Literature Review

2.1 Cellular Transmitter Architecture

An RF transmitter processes modulation, upconversion and power amplification. A generic modern direct-conversion RF transmit chain is shown in Figure 2. It composes of baseband and RF front-end. Baseband can be further divided into digital baseband and analog baseband. Digital baseband performs digital modulation and this signal is then transformed into analog domain by digital/analog converter (DAC). The output from DAC goes through analog baseband which includes a variable gain amplifier and a low pass filter to adjust signal power and filter the out-of-band noise. RF front-end includes mixers, PA driver, and power amplifier. Mixers serve as up-converter that translates the baseband spectrum into the RF carrier. For modern cellular communication, quadrature upconversion is used to reduce the bandwidth. Quadrature mixers are employed to up-convert quadrature baseband to RF carrier and combine the signal for transmitting. PA driver is used to drive the large input transistor of the power amplifier. Finally, PA delivers the adequate power to the antenna for transmitting.

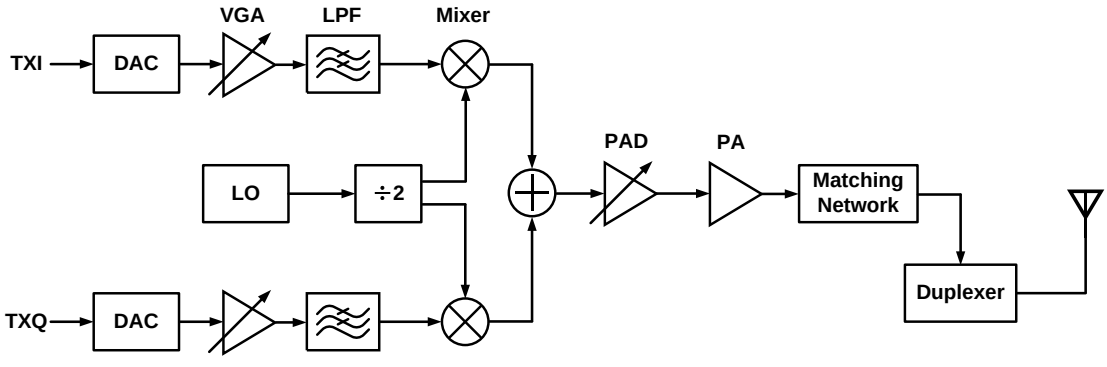


Figure 2. Typical modern direct-conversion transmitter with quadrature modulation

Additionally, if PA output and LO frequency are the same, the strong PA output power will couple back to LO through PCB board, package parasitics and the silicon substrate. Therefore in most of the today's modern transmitters, the LO frequency,

ω_{LO}, is set to be far from the PA output carrier frequency, ω_C, to avoid injection pulling effect [13]. Figure 2 also depicts a common example, where LO frequency passes through a divide-by-2 circuit to generate carrier frequency with quadrature phases obtaining $\omega_C = \omega_{LO} \div 2$. This comes to be today's popular architecture because it reduces injection pulling significantly and provides quadrature outputs through a single module [13].

Nowadays there are two popular architectures used in cellular transmitter design which are the voltage-mode passive mixer based driver amplifier (PA driver) structure [4] [5] [9] [14] - [20] and the current-mode active mixer (also known as power mixer) based design [21] - [26].

Figure 3 depicts a traditional current mode transmitter employing active mixers [26]. The baseband signal is obtained from DAC as a current and converted to a voltage by a resistor. The signal is buffered before reaching a biquad low-pass filter. The output of baseband filter is transformed to current using a voltage-to-current converter (V2I) which also incorporates a passive RC filter to further reject the noise generated by the filter. The V-I outputs are routed to current-mode IQ mixers for frequency upconversion. The V-I path is designed for high linearity to suppress baseband harmonics. Normally the 50% duty cycle LO signal is used for power mixers. The up-converted signal can be further attenuated by passive RF VGA and finally delivered to external PA through a differential to single-ended on-chip balun.

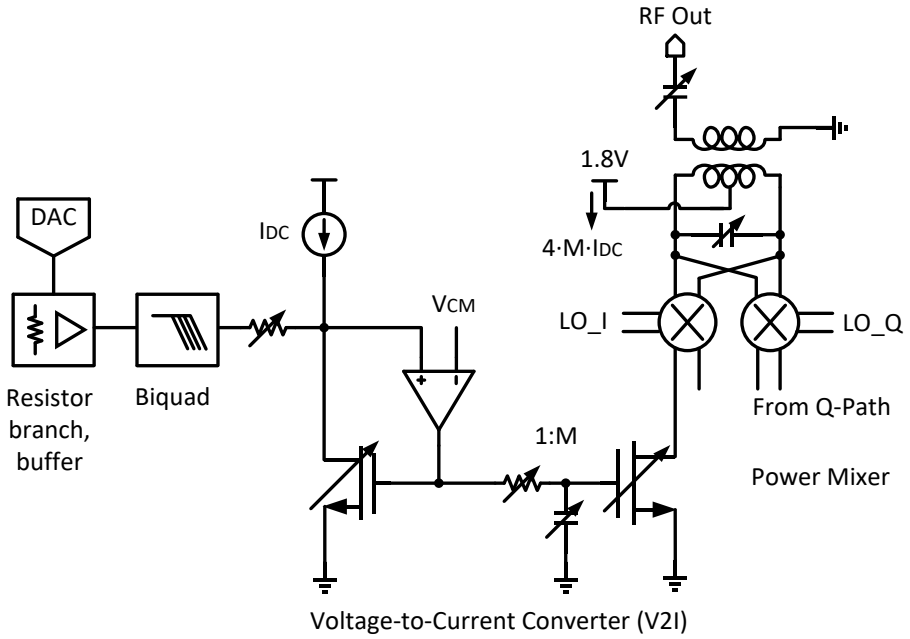


Figure 3. Traditional power mixer based transmitter architecture [25]

Figure 4 shows an example of passive mixer based voltage-mode transmitter [7]. In this design, the current signal first passes through a transimpedance low pass filter which is used to tune the bandwidth for multimode. Then the out-of-band noise of output voltage is further filtered out by a passive pole before reaching passive switches. The baseband voltage is sampled with 25% duty cycle LO for both I and Q channel. The final stage, pre-power amplifier, aka. PA driver, takes the up-converted signal from the mixers, provides a configurable differential to single-ended gain and feed it to the power amplifier. It consists a group of parallel common-source amplifiers which can be turned on or off by cascade thick-oxide transistors. The thick transistors also provide protection for pseudo-differential input transistors from 2.5V supply voltage in this publication. For LO signal, 25% duty cycle is most popular for passive mixers. It is because 25% duty cycle LO has 4 phases and can turn on the 4 switches (2 for I path, 2 for Q path) alternatively to avoid turning on the switches concurrently like 50%. This method is able to improve the linearity of the sampling mixer [4] [27].

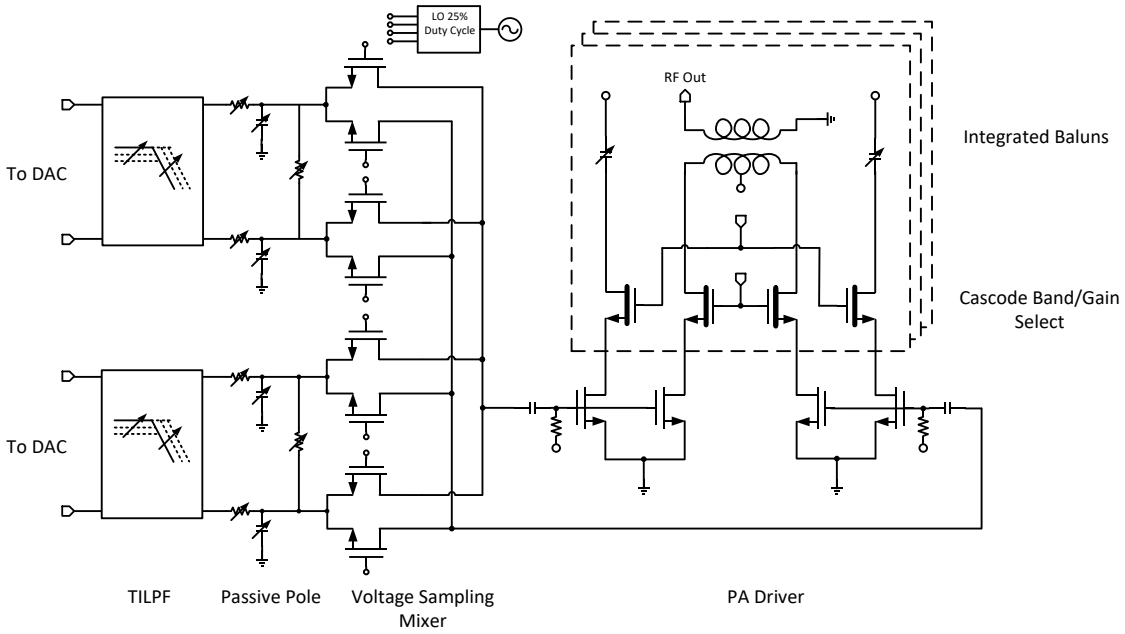


Figure 4. Example of passive mixer based transmitter architecture [7]

2.2 Generation of Counter Intermodulation Products

As mentioned in Section 1.1, CIM products have become a major design consideration for 4th generation cellular transmitter. Several dominating causes have been identified for the generation of CIM3 components in Figure 5 [9] [10].

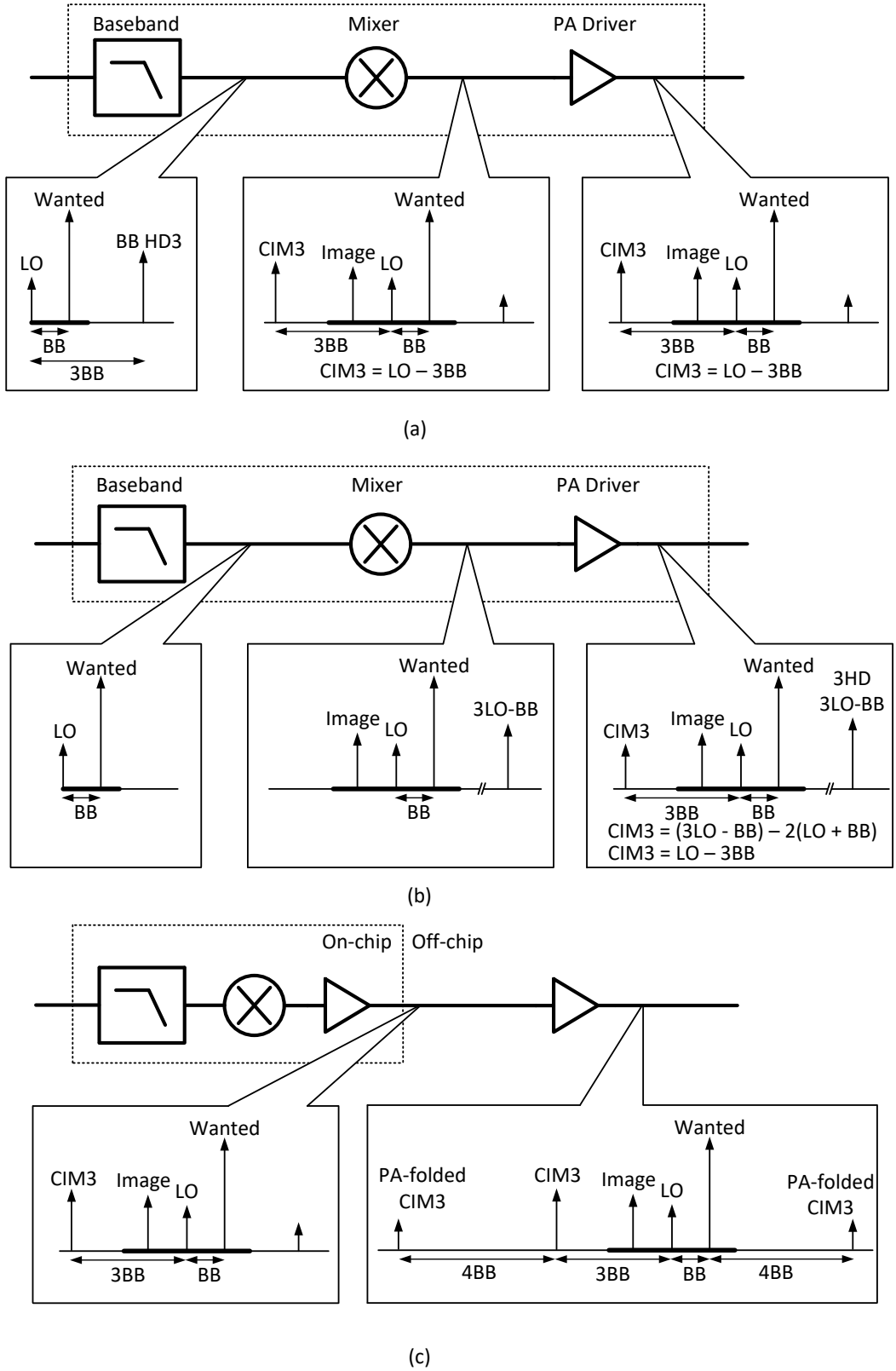


Figure 5. Generation of CIM products [9] [10], (a) CIM3 due to BB HD3, (b) CIM3 due to intermodulation between LO+BB and 3LO-BB, (c) generation of CIM5 and CIM7

The first contributor originates from the baseband 3rd-order nonlinearity which is depicted in Figure 5(a). The baseband signal with frequency BB is applied to a nonlinear baseband circuit which generates baseband 3rd-order harmonic distortion (BB HD3) at 3BB. During mixing at upconverter, BB HD3 is up-converted to LO – 3BB as part of CIM3. This will remain in the following transmit chain because LO – 3BB is so close to wanted signal and it can be hardly filtered out. In a typical transmit baseband chain, the signal level is kept rather high to obtain good signal to noise ratio (SNR), together with low supply voltage applied, it is difficult to obtain an extremely linear baseband circuit. Therefore, the resulting generation of CIM3 at LO - 3BB due to baseband HD3 remains a critical issue.

The second important contribution originates in the mixer shown in Figure 5(b). Due to mixing with a large LO signal, which is not a pure sine wave, harmonics of LO signal is created such as 3rd harmonics at 3×LO frequency (3LO). Upconversion with this 3LO creates a component at 3LO – BB at the mixer. This undesirable signal can generate CIM3 product due to intermodulation with the wanted signal at LO + BB in the non-linear PA driver as illustrated in Equation 2.1,

$$(3LO - BB) - 2 \times (LO + BB) = LO - 3BB \qquad \text{(Equation 2.1)}$$

This especially raises challenge for extensively used passive mixers in modern modulators since LO signals acts more like a square wave in these mixers. The desired signal at LO + BB and the CIM3 product at PA driver may further generate intermodulation products in the power amplifier as shown in Figure 5(c), Equation 2.2 and 2.3,

$$2\,(LO + BB) - (LO - 3BB) = LO + 5BB \qquad \text{(Equation 2.2)}$$

$$2\,(LO - 3BB) - (LO + BB) = LO - 7BB \qquad \text{(Equation 2.3)}$$

The products located at LO + 5BB and LO – 7BB are known as counter 5th intermodulation product (CIM5) and counter 7th intermodulation product (CIM7). CIM3 together with CIM5, especially for CIM3 since it has stronger power, significantly challenge system noise and spurious emission requirements.

In summary, the CIM3 product is the major counter intermodulation product, which originates from both baseband nonlinearity and LO harmonics.

2.3 Harmonic Suppression Techniques for RF Transmitter

As the development of LTE network, CIM3 has been recognized as an important issue and only a few publications deal with this problem. There are mainly two approaches to deal with this issue.

2.3.1 Power Mixer Approach

One conventional way to improve CIM3 is applying a power mixer architecture discussed in Section 2.1 [21]. Targeting at first contributor, the baseband's intrinsic linearity is improved by using a highly linear voltage-to-current converter before mixing. And the signal is processed and up-converted in current domain to keep good linearity and suppress the generation of baseband harmonics. However, the drawbacks of this design are more design efforts and power penalties. And the baseband pre-distortion [28] to compensate the non-linearity is not appropriate due to required wider filter bandwidths and the associated penalty in out-of-band noise. In addition, in order to maintain a sufficient baseband linearity to avoid direct CIM3 generation, a 2.8V power supply is applied to baseband circuits.

After the mixing, targeting at the 2nd contributor listed in Section 2.2, PA driver is removed to avoid generation of CIM products close to wanted signal. However, 3LO or higher order harmonic component originating from mixer still exists in spectrum and CIM3 will be produced at PA instead. Thus an off-chip notch filter is required to eliminate 3LO – BB before PA as shown in Figure 6 [11]. As a consequence, the use of notch filter results in a significant area increase and more importantly, a limitation of RF operation frequency range. The limitation of the frequency range is a major disadvantage, especially for 3GPP standards [8], which requires the coverage of multiple RF bands. Due to the off-chip filter, the level of integration and bill-of-material of the circuit are both compromised significantly.

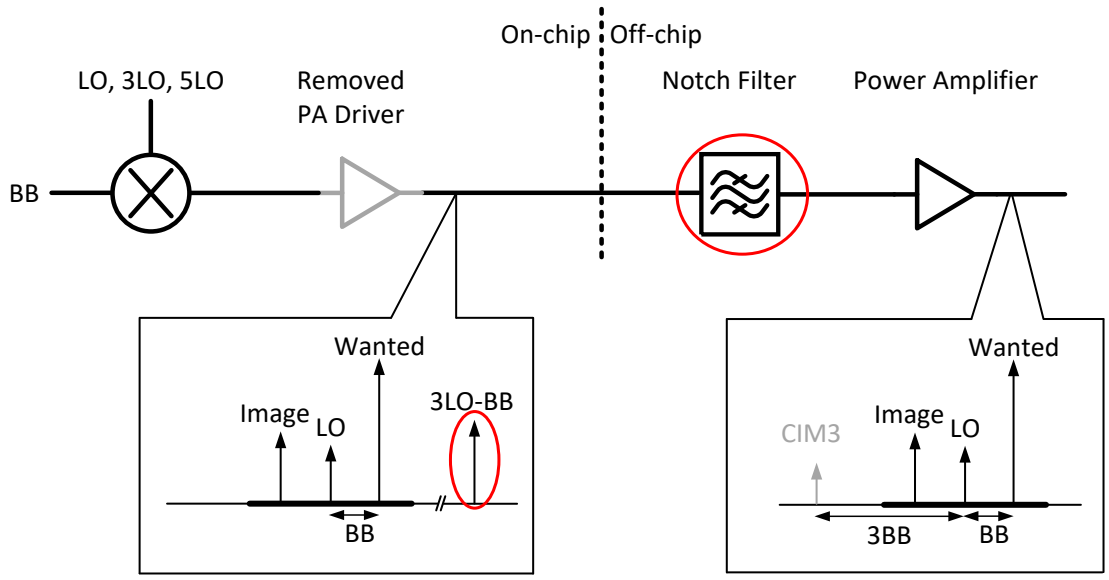


Figure 6. Power mixer approach to suppress harmonic generation [11]

Several techniques have been proposed to minimize the power consumptions by applying Class A/B topology [22] [23]. A dynamically biased transmitter [25] [26] is also proposed to further minimize power consumption and improve circuit efficiency. Nonetheless, the filtering of 3LO component is a must which considerably complicates the RF system design. Furthermore, the baseband linearity still needs to be sufficiently high to avoid direct CIM3 generation.

2.3.2 Harmonic Cancellation Approach

For a typical nonlinear system, suppose the input signal is a single-tone sine wave,

$$x(t) = A\cos\omega t \qquad \text{(Equation 2.4)}$$

If only consider up to the 3rd-order nonlinearity, the output waveform is

$$y(t) = \alpha_1 A\cos\omega t + \alpha_2 A^2 cos^2\,\omega t + \alpha_3 A^3 cos^3\,\omega t \qquad \text{(Equation 2.5)}$$

$$y(t) = \frac{1}{2}\alpha_2 A^2 + (\alpha_1 A + \frac{3}{4}\alpha_3 A^3)\cos\omega t + \frac{1}{2}\alpha_2 A^2 cos\,2\omega t + \frac{1}{4}\alpha_3 A^3 cos\,3\omega t$$

(Equation 2.6)

For a differential system, only odd order terms are retained, thus

$$y(t) = (\alpha_1 A + \tfrac{3}{4}\alpha_3 A^3)\cos\omega t + \tfrac{1}{4}\alpha_3 A^3 cos\,3\omega t \qquad \text{(Equation 2.7)}$$

If there are multi-phase signals are input into system, for a phase difference of θ,

$$y(t) = (\alpha_1 A + \frac{3}{4}\alpha_3 A^3)\cos(\omega t + \theta) + \frac{1}{4}\alpha_3 A^3 cos(3\omega t + 3\theta) \qquad \text{(Equation 2.8)}$$

It is shown that for an input signal with a phase difference of θ, the output 3rd-order harmonic distortion has a phase difference of 3θ.

Harmonic cancellation technique was proposed in [29] by applying harmonic rejection mixer (HRM) to reject the 3rd-order baseband harmonics. The principle of the harmonic cancellation is upconverting the baseband signal with same LO frequency of different phases (Figure 7) i.e. 0°, 45°, 90°, and the amplitude ratio of 1:√2:1. The different phases can be generated from polyphase filter and the amplitude ratio is obtained by carefully adjusting transistors' size of upconversion mixers.

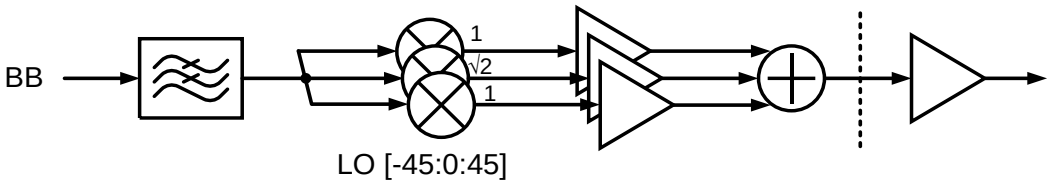


Figure 7. Block diagram of transmitter proposed in [29]

The harmonic cancellation procedure is illustrated in Figure 8 (only in-phase signal is used for ease of illustration). Suppose the baseband signal has a phase of 0° (Figure 8(a)), then according to Equation 2.7, its 3rd-order harmonic product have the same phase with the baseband signal (Figure 8(b)). Then the LO frequency with the same amplitude but different phases of 0°, 45°, 90° are applied (Figure 8(c)). The active mixer is used and the tail current is scaled by 1:√2:1. Thus, the wanted signal is scaled by 1:√2:1 and combined constructively in RF domain with the total phase of 45° (Figure 8(d)). According to Equation 2.8, the LO 3rd-order harmonics are located at 0°, 135°, 270° (Figure 8(e)), with an amplitude ratio of 1:√2:1. It can be found that the RF HD3 are canceled out, as a result, the BB is not upconverted to 3LO, and 3LO – BB product is not generated (Figure 8(g)). Thus the related CIM3 mechanism which is the 2nd contributor explained in Section 2.2 is suppressed.

However, this scheme has no impact on the CIM3 baseband nonlinearity related generation. As a consequence, the CIM3 product due to the presence of BB HD3 component is not eliminated (Figure 8(f)). In addition, there may be a phase mismatch of the multi-paths since the polyphase filter is used to generate 45° difference.

Furthermore, the amplitude ratio of 1:√2:1 has a residual error of harmonic cancellation which sets the rejection limit.

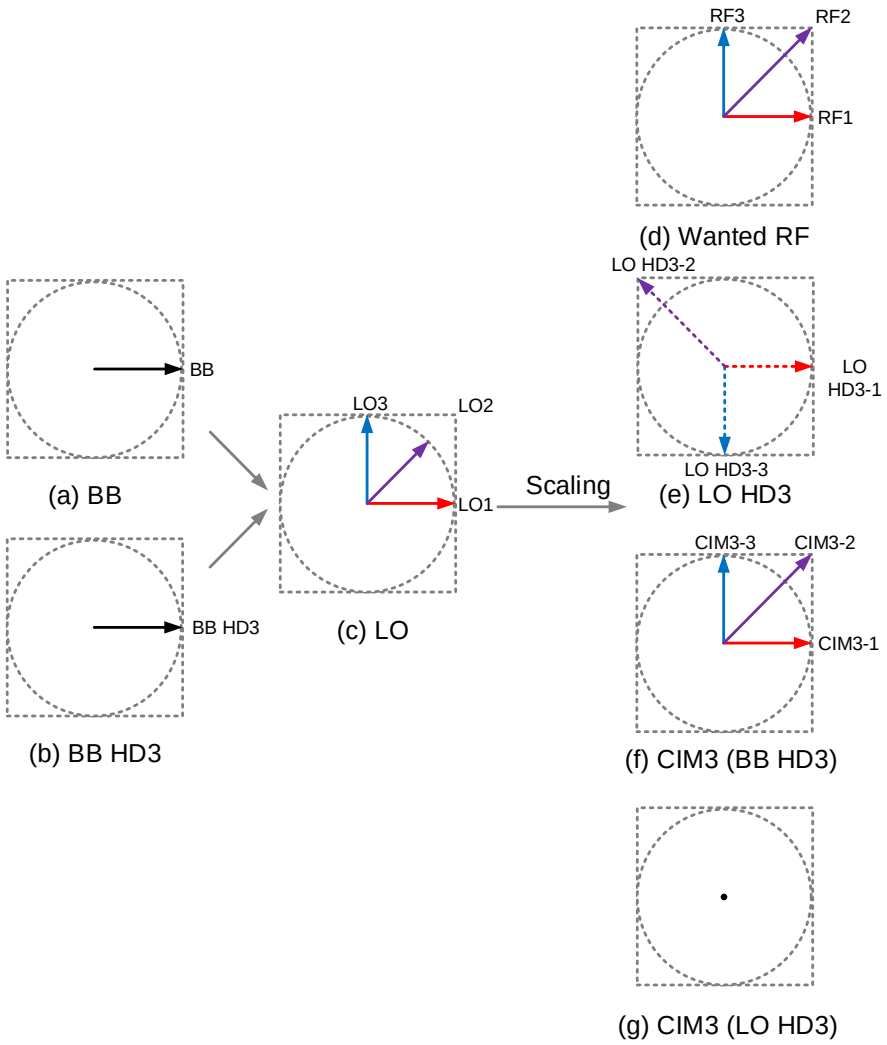


Figure 8. Harmonic cancellation technique proposed in [29]

An improved harmonic cancellation technique is exploited in [9]. The corresponding circuit diagram is shown in Figure 9.

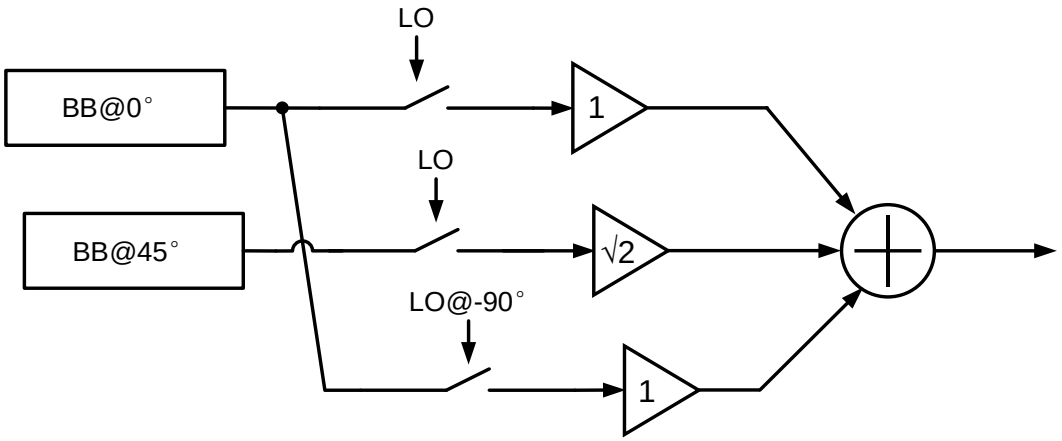


Figure 9. Block diagram of transmitter proposed in [9]

It proposed a harmonic rejection transmitter by using a baseband signal with 2 different phases upconverting with an LO signal with 2 phases. The upconverted signal is then scaled by PA driver respectively and combined to reject baseband harmonics at RF. The design is implemented with voltage mode passive mixer architecture where the sampling mixers (passive mixers) are used. The outputs of all the mixers are combined at the input transistor of PA driver. 50% duty cycle LO is no longer to be used since signal overlapping will occur in the time domain. Instead, 25% duty cycle LO is used to ensure the non-overlapping in this design.

The harmonic cancellation procedure is illustrated in Figure 10 (only in-phase signal is used for ease of illustration). Baseband signal with the phase of 0° (Figure 10(a)) is mixed by LO and LO@-90° (Figure 10(e)) and baseband signal with the phase of 45° (Figure 10(c)) is mixed by LO (Figure 10(f)). The upconverted RF signal is combined constructively and scaled in Figure 10(g) and Figure 10(k) respectively. The final RF signal has finite amplitude with a total phase of 0°. For the baseband 3rd-order harmonic distortion, the BB@0° HD3 (Figure 10(b)) and BB@45° HD3 (Figure 10(d)) are upconverted with respective LO signals and combined in Figure 10(i) as CIM3 product. After scaling by the PA driver, the CIM3 are removed (Figure 10(m)).

However, CIM3 caused by 3LO – BB still exists since neither LO HD3 (Figure 10(h) and Figure 10(l)) nor the combined phase of BB and LO HD3 (Figure 10(j) and Figure 10(n)) are canceled. As a result, the off-chip filter is still needed to notch the spurs at 3LO – BB.

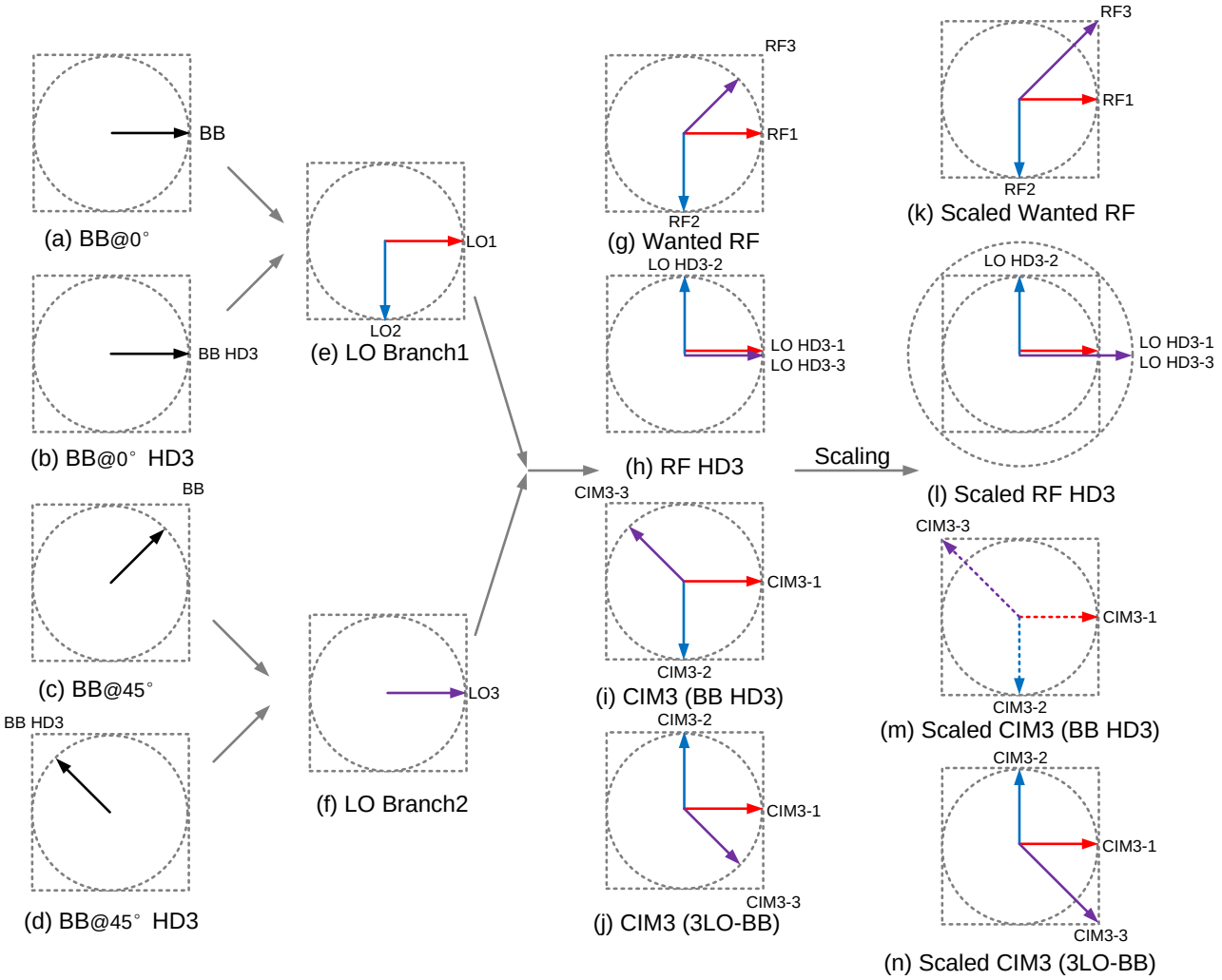


Figure 10. Harmonic cancellation technique proposed in [9]

Another drawback of this design is that BB circuit has to be doubled to provide both 0° and 45° phase baseband signal at a cost of doubling BB area and power.

One idea of complete rejection of both the 1st and 2nd causes is illustrated in [10]. 2-phase BB path same as [9] together with mixer arrays originating from [29] are combined. In this way, BB HD3 are removed by the techniques in [9] while harmonic rejection mixer [29] is used to eliminate LO 3rd-order harmonics completely. However, the proposed idea is limited by its LO generation circuit complexity since a phase difference of 45° is required instead of 90° of 25% duty cycle LO. It is also not possible to avoid turning on switch together so that the linearity of the mixer is compromised. Moreover, scaling ratio of 1:√2:1 is still used which sets the limitation of rejection.

Recently, one innovative technique focused on LO harmonic cancellation is proposed in [11]. Shown in Figure 11, 33% duty cycle LO signal is used for signal upconvertion in the transmitter design. The basic theory of the design is that LO signal with 33% duty cycle intrinsically does not have 3rd-order harmonics, so CIM3 caused by 3LO component is suppressed at the RF output. The harmonic cancellation procedure is demonstrated in Figure 12 (only in-phase signal is used for ease of illustration). As shown in Figure 12(h) and Figure 12(j), CIM3 caused by 3LO component is not presented in the final output signal. Besides, signal scaling is not applied in this design which can reduce the phase mismatch in the design. Furthermore, this technique is not sensitive to device matching and calibration is not a pre-requisite. 3LO filtering is not required as a result BOM cost is saved. Without filtering, the broadband application can also employ this technique.

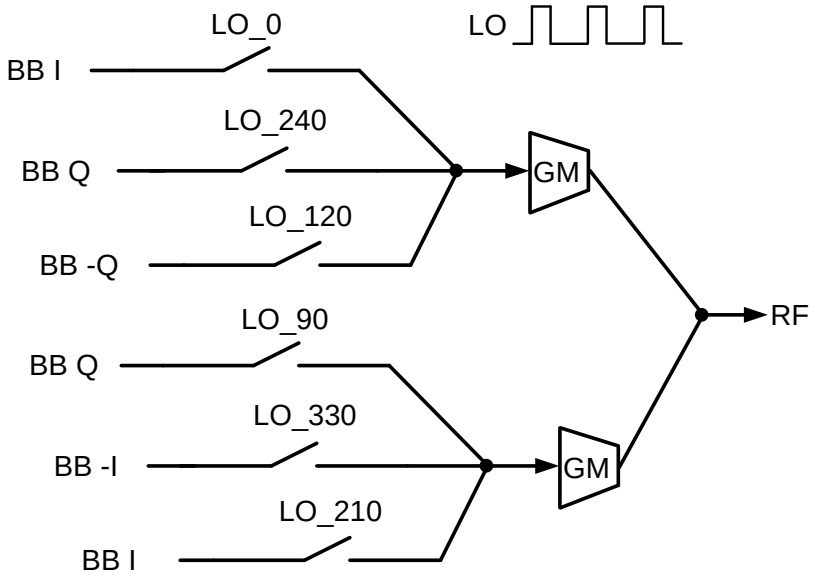


Figure 11. Block diagram of transmitter proposed in [9]

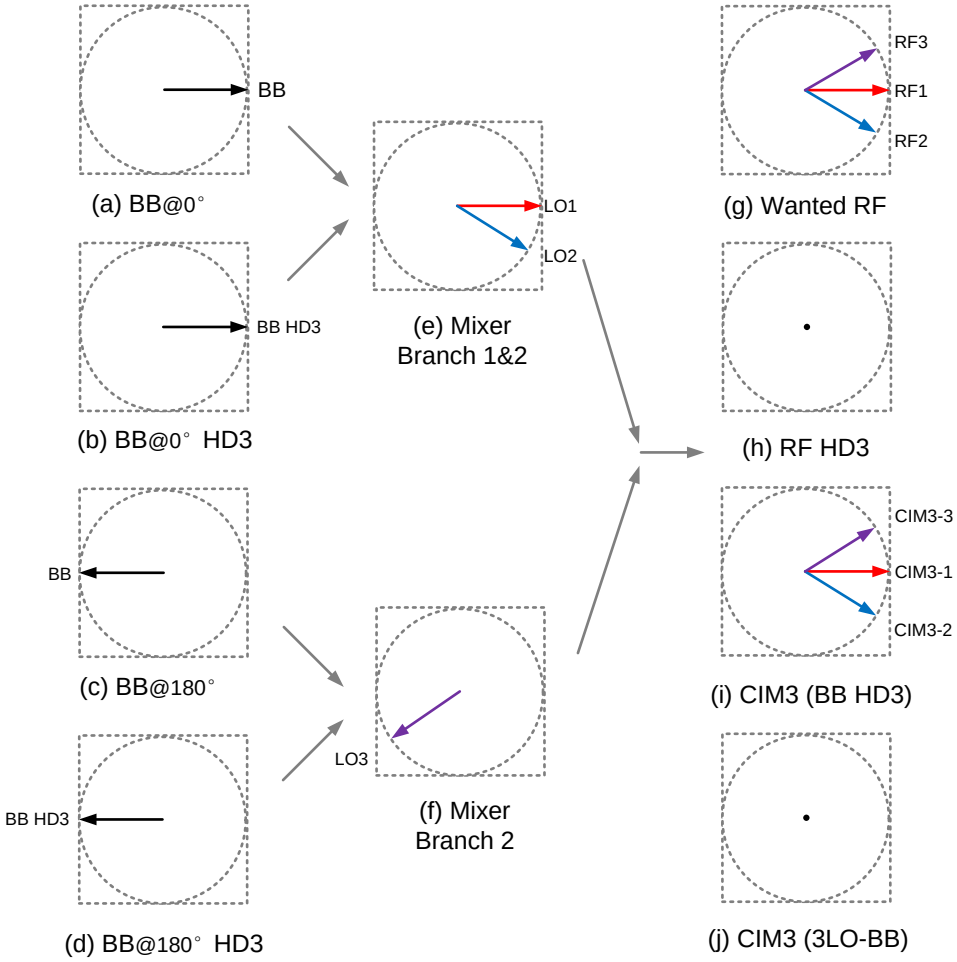


Figure 12. Harmonic cancellation technique proposed in [9]

This thesis is the continuation of the previous literature [11] to explore the application of 33% duty cycle scheme for CIM products suppression. The reference work studies the property of 33% duty cycle of LO signal and provides an innovative solution for harmonic suppression in passive mixer based TX system. Different from the reference work, active mixer based architecture is employed in the proposed RF transmitter (TX) system. 33% duty cycle scheme is also applied targeting at suppression of undesirable counter 3rd-order intermodulation. Besides, the designed system has a wide band test frequency range to further verify the attenuation of 3LO component. Overall, the system is designed towards to simplicity, low cost, easy implementation and adaptable to existing environments. The detailed explanation and circuit implementation will be discussed in following chapters.

CHAPTER 3

Design of Transmitter RF Front-End With 33% Duty Cycle LO

In this chapter, theory and circuit architecture will be presented in the following sections.

3.1 Theory

Figure 13 shows the timing diagram of an ideal 33% duty cycle signal. The single-ended signal is shown here.

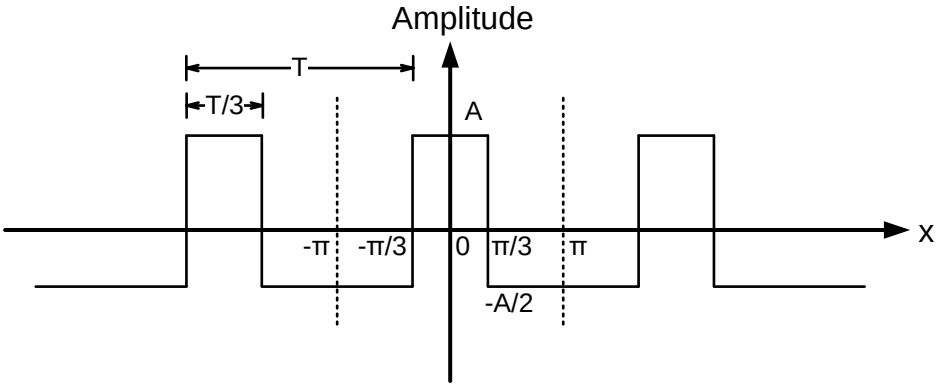


Figure 13. 33% duty cycle LO waveform

The Fourier transform of the 33% duty cycle waveform is shown below,

$$f(t) = a_0 + \sum_{n=1}^{\infty} a_n \cos nx \qquad \text{(Equation 3.1)}$$

where n is the harmonic number. Let $a_0 = 0$ by assuming the average DC amplitude is 0 in the waveform for simplicity. So,

$$a_n = \frac{2}{\pi}\int_0^{\pi} f(x)\cos nx\ dx$$

$$= \frac{2}{\pi}\left[\int_0^{\frac{\pi}{3}} A\cos nx\ dx + \int_{\frac{\pi}{3}}^{\pi}\left(-\frac{A}{2}\right)\cos nx\ dx\right]$$

$$= \frac{3}{\pi}\frac{A}{n} \sin n\frac{\pi}{3} \quad \text{(Equation 3.2)}$$

Therefore,

$$f(x) = \sum_{n=1}^{\infty} \frac{3}{\pi}\frac{A}{n} \sin(\frac{n\pi}{3}) \cos nx \quad \text{(Equation 3.3)}$$

Equation 3.3 can be converted to the following equation when the x-axis is in the time domain,

$$LO(t) = \sum_{n=1}^{\infty} \frac{3}{\pi}\frac{A}{n} \sin(\frac{n\pi}{3}) \cos(n\omega_{LO}t) \quad \text{(Equation 3.4)}$$

Equation 3.4 indicates that the waveform's 3rd-order harmonic term is nulled due to $\sin(n\pi/3)$. When n equals integer multiples of 3, $\sin(n\pi/3)$ equals to 0. If LO signal has a duty cycle of 33%, it intrinsically does not have the 3rd-order harmonic product. Thus the CIM3 due to LO HD3 can be suppressed.

Since the harmonic suppression technique is based on LO waveform, it is not sensitive to device matching of the upconverter, and calibration is not required for robust performance. Most importantly, adopting 33% duty cycle LO can eliminate the use of 3LO component notch filter to reduce CIM3 generation, which allows the circuit to cascade a PA driver stage without considering intermodulation of 3LO – BB and LO + BB.

3.2 Initial Design

The design starts with applying the 33% duty LO signals to a multi-path active mixer. Differential LO signal with 3 phases are provided as shown in Figure 14(a), each of signal has a phase difference of 120°. The LO signals are all differential and only the single-ended waveform is shown in the figure for simplicity. A three-phase mixer depicted in Figure 14(b) is used to eliminate the undesired harmonic components at 3LO, the consequential LO - 3BB, and I-Q quadrature image signal. The in-phase differential baseband input is upconverted with 0° phase LO and the quadrature-phase input signal is upconverted with 120° and 240° phase LO signals. The upconverted I and Q signals are then combined in the current domain. With the vector summation, the in-phase signal is aligned at a phase of 0° while the quadrature-phase signals are constructively summed at a phase of 90° as shown in Figure 14(c).

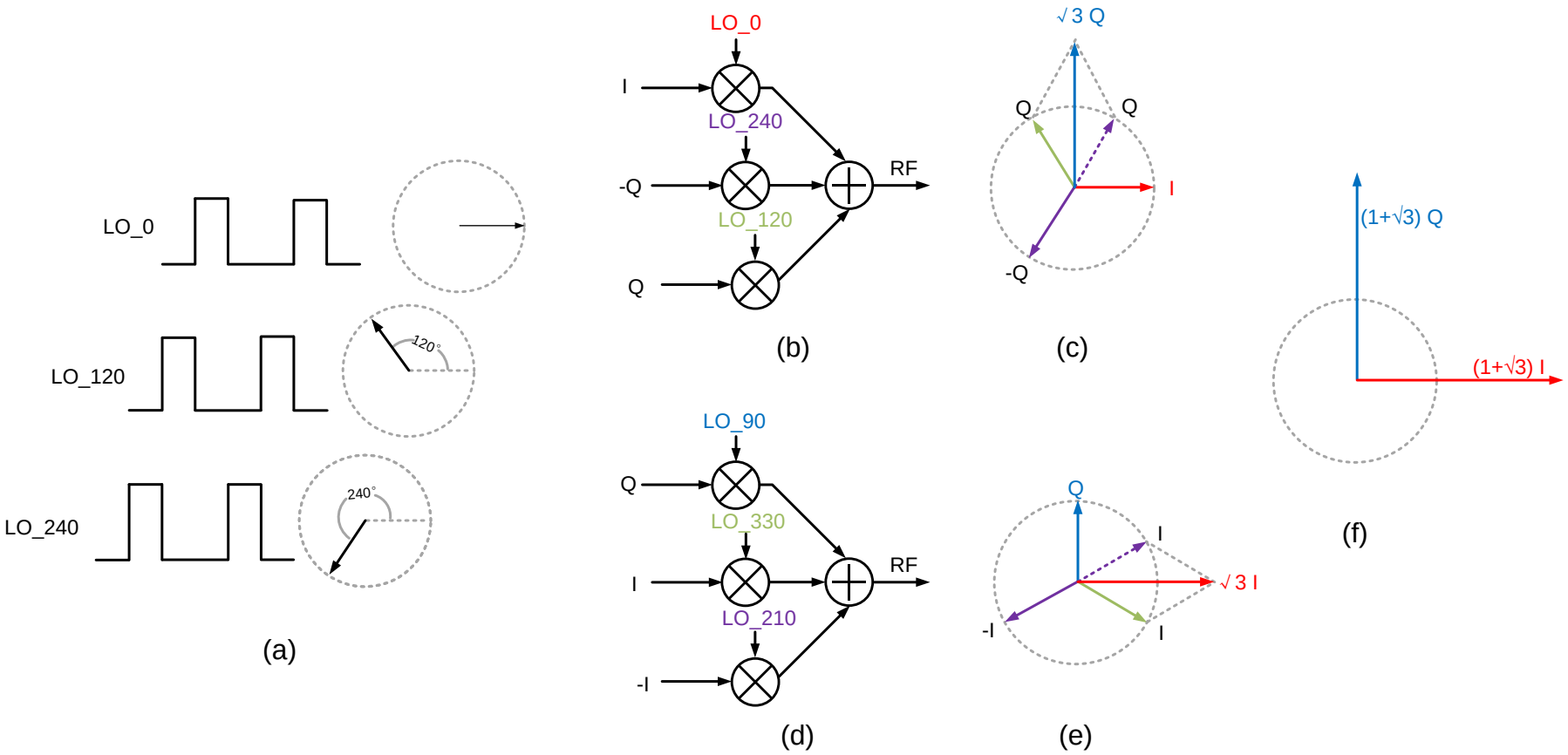


Figure 14. Cartesian direct upconversion and I-Q balance without gain scaling, (a) LO signal with 33% duty cycle, (b) 3-phase mixer I, (c) vector summation for I/Q signal upconverted by 3-phase mixer I, (d) 3-phase mixer II, (e) vector summation for I/Q signal upconverted by 3-phase mixer II, (f) final vector summation

However, there is an obvious amplitude mismatch between I and Q signals with the ratio 1:√3. One solution to minimize the mismatch is properly adjusting transistor size of mixers but there is a rejection limit for √3 in circuit design as discussed in Chapter 2. Besides, the input IF I path and Q path are not balanced because input I drives 1 pair of mixers while input Q drives 2 pairs. The I-Q imbalance can degrade the I-Q image rejection. To address this issue, an identical mixer element with 2 I paths and 1 Q path is added to construct a symmetric topology as shown in Figure 14(d). To make I-Q signal locate at the correct phase, LO signals with phases of 90°, 210°, 330° are applied as shown in Figure 14(e). The outputs from 2 mixer elements are coupled to an output network where the differential outputs of the 2 mixer elements are added constructively. As is seen in Figure 14(f), the summed output has equal I-Q amplitude. With this type of circuit, the undesired harmonic contents at 3LO and the resultant CIM3 at LO – 3BB are suppressed and the circuit is also balanced for the baseband signals. Furthermore, the scaling of √3 can be avoided in this design.

3.3 Architecture Design

The overall architecture is shown in Figure 15. The designed transmitter composes of mixer elements, a divide-by-6 circuit, an analog baseband circuit, PA drivers, and an off-chip balun.

Different from previous literature [11], in this design, the topology adopting active mixers is explored. The mixers are designed to have moderate gain thus relatively good linearity can be obtained. PA driver is employed to drive the capacitive and resistive load of various type of testing equipment such as oscilloscope and spectrum analyzer. The off-chip balun is provided on PCB to convert differential signal into a single-ended signal. Analog baseband circuit is from the pre-designed group project and the details will be shown in Section 3.4.

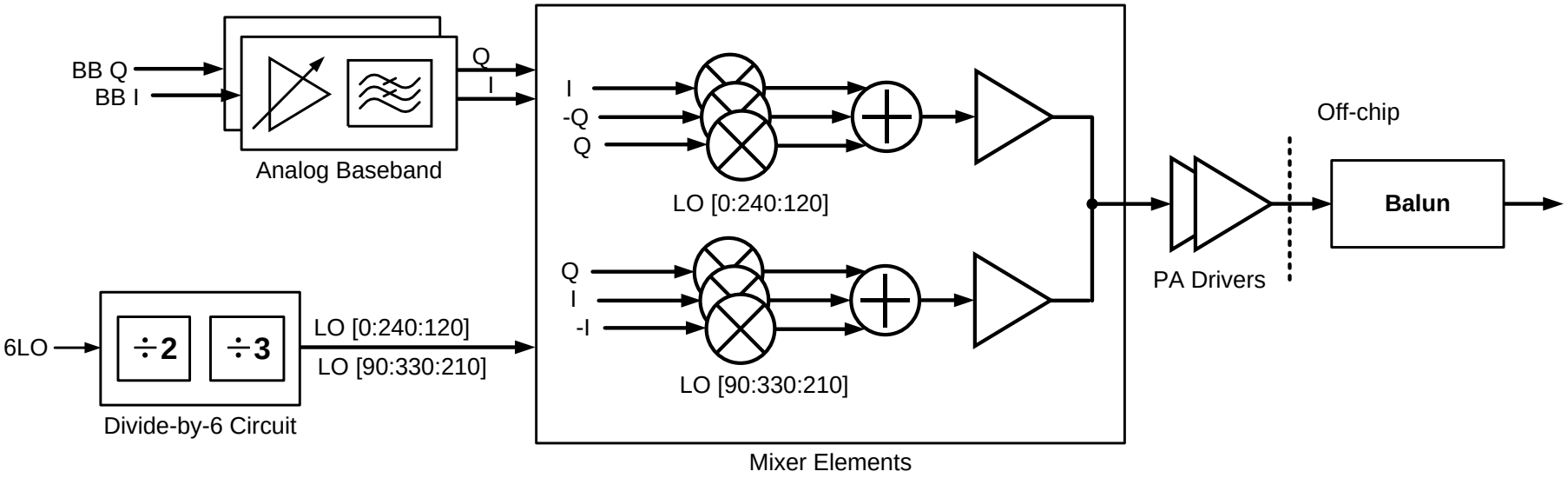


Figure 15. Block diagram of designed RF transmitter with 33% duty cycle LO

3.4 Pre-designed Analog Baseband

The gain and frequency range of pre-designed analog baseband circuit are shown in Figure 16. The baseband circuit is composed of a variable gain amplifier (VGA) and a low pass filter. The simulated gain range is from 0 to 32 dB and the -3 dB bandwidth is 5.6 MHz.

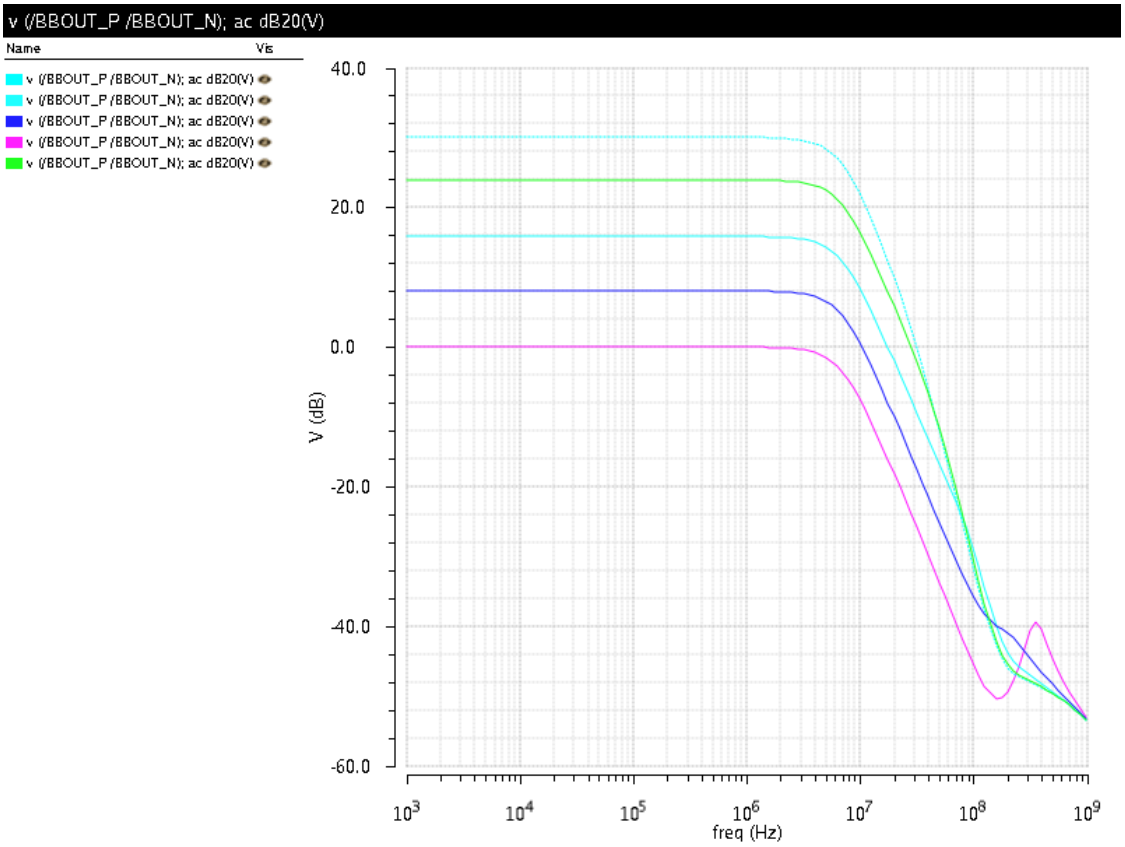


Figure 16. Analog baseband circuit gain and bandwidth simulation results

CHAPTER 4

Design of Transmitter Blocks

In this chapter, the core blocks of the transmitter including mixer element, divider circuit and output stage circuit will be discussed in details.

4.1 Design of Mixer Element

4.1.1 General Considerations

In general, the mixers designed in a transmitter should translate the baseband spectrum to a high output frequency while providing sufficient gain. It must be able to drive the input capacitance of the PA and deliver the necessary swing to the PA input. Moreover, it cannot limit the linearity of the whole TX.

There are different types and structures of mixer design in the transmitter. The mixers used in RF transmitter can be classified in 2 main structures: active mixer as used in [1] [21] and passive mixer as illustrated in [7] [9] [11]. These 2 types of mixer are firstly reviewed in the following parts [13].

4.1.2 Passive Mixers

The circuit diagram of double-balanced passive mixer is shown in Figure 17. It consists of 2 pairs of CMOS switches to modulate the signal at the carrier frequency while rejecting LO-to-RF feedthrough compared with single balanced structure.

Regarding the gain of the mixer switches, if the square wave is used as LO signal, it provides a conversion loss instead of a conversion gain, which is

$$A_{CL} = \frac{2}{\pi} \approx -4\ dB \qquad \text{(Equation 4.1)}$$

Even though it doesn't provide a positive gain, it can switch the IF signal directly in the voltage domain without the voltage-to-current (V-I) conversion. This will increase the circuit linearity significantly. The other attractive properties of this mixer topology are the low power consumption. Ideally, the passive switches consume no DC power.

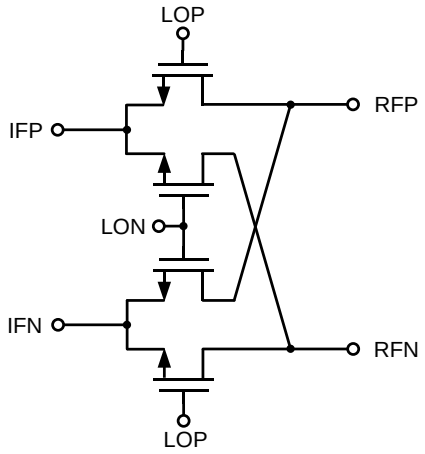


Figure 17. Circuit diagram of double-balanced passive mixer

One issue of the passive mixer is that the rail-to-rail LO signals are required to drive the switches, which is a disadvantage with respect to the active mixer. LO buffer should be provided at a cost of additional power consumption. The other issue related to the use of passive mixer topology is that for quadrature upconverter, the outputs from 2 mixers must be summed. However, passive mixers sense and produce voltages at the output, which makes the direct summation difficult. Therefore, a summation stage followed the passive mixers should be added to convert the voltage to current, sum the currents and convert the current to voltage as the output. However, this stage will increase the power consumption and degrade the linearity due to V-I conversion at the transconductance transistor.

In a summary, the passive mixers have advantages of power and linearity performance in the transmitter design, but the gain needs to be compensated by the I-Q summation stage and the linearity will be degraded due to V-I conversion of this stage. The passive mixer also requires large LO swing which will increase the power budget when designing divider output buffers. In order to have more gain and relax the divider output buffer power consumption, and the noise requirement for RF transmitter is quite relaxed compared with RF receiver, we focused on the active mixer in the transmitter design.

4.1.3 Active Mixers

The second type of mixer reviewed is the active mixer. The most popular active mixer currently in use is Gilbert cell mixer. The circuit diagram of Gilbert cell active mixer

is shown in Figure 18. It consists of two single-balanced mixers with cross-coupled outputs in the current domain. M_2 and M_3 form the transconductor stage of the mixer and convert the input IF signal into current. The upper two pairs of transistors, M_4 - M_7 are cross-coupled and driven by LO signal, forming the switching stage of the mixer. At the output, the RF signal is taken differentially between V_{RFP} and V_{RFN}. Moreover, the double-balanced structure is capable of providing excellent LO-to-RF isolation because the LO signals appears as common mode signals at the RF output and are thus cancelled after subtracting.

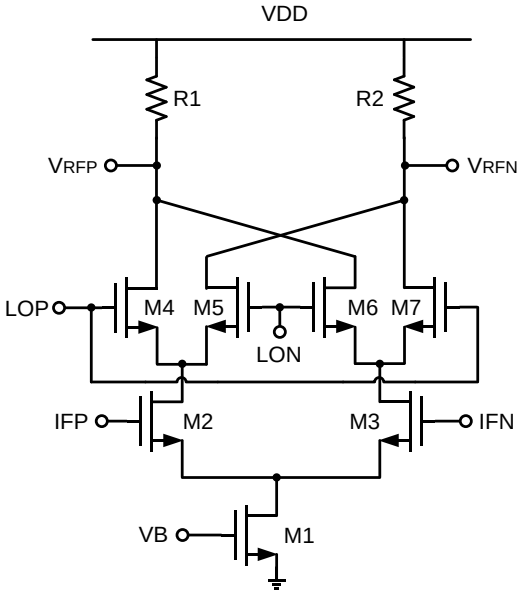


Figure 18. Circuit diagram of Gilbert cell active mixer

The active mixer has many advantages compared with the passive mixers. It can have broad bandwidth and provide positive conversion gain. Figure 19(a) depicts a typical single-balanced realization of the active mixer. M_1 acting as transconductor converts the input IF voltage to a current; switching pairs M_2 and M_3 commutates this current to the left and to the right; R_1 and R_2 convert the currents to voltage. As shown in Figure 19(b), M_1 produces a small-signal drain current equal to $g_{m1}V_{IF}$. M_2 and M_3 act as switches if abrupt LO signal is provided. Suppose M_2 multiplies I_{RF} by $S(t)$ and M_3 multiplies I_{IF} by $\overline{S(t)}$, where $S(t)$ and $\overline{S(t)}$ are complementary signals toggling between 0 and 1, e.g. 50% duty cycle LO signal as shown in Figure 19(c). It follows that:

$$I_1 = I_{IF} \cdot S(t) \qquad \text{(Equation 4.2)}$$

$$I_2 = I_{IF} \cdot \overline{S(t)} \quad \text{(Equation 4.3)}$$

Since $V_{out} = V_{DD} - I_1R_1 - (V_{DD} - I_2R_2)$ and $R_1 = R_2 = R_D$,

$$V_{out}(t) = I_{IF}R_D\left[S(t) - \overline{S(t)}\right] \quad \text{(Equation 4.4)}$$

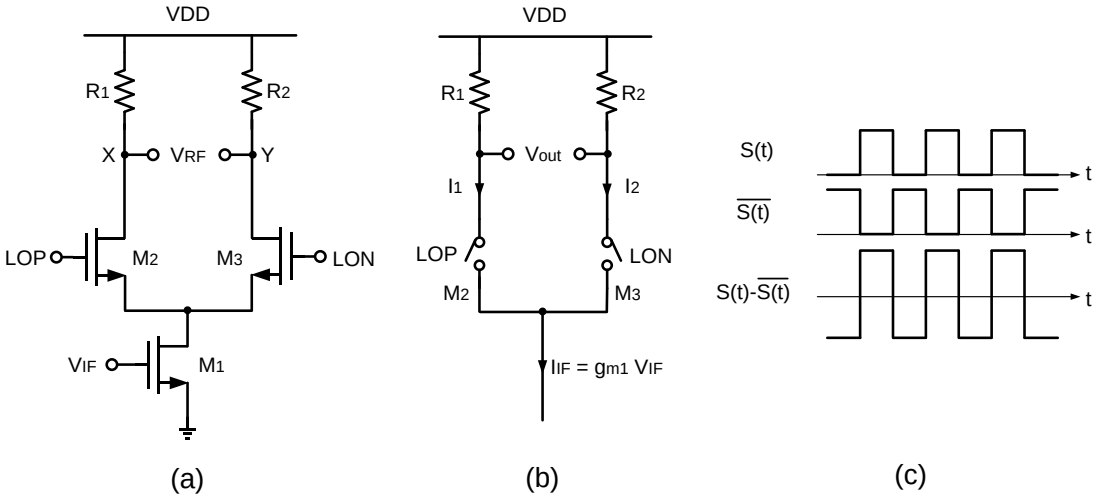


Figure 19. Circuit diagram of single-balanced mixer and LO waveform (a) Single-balanced mixer (b) equivalent circuit of single-balanced mixer (c) switching waveform

From Figure 19(c) that the switching operation shown in the above equation is equivalent to multiplying I_{IF} by a square wave toggling between -1 and 1. Such a waveform exhibits a fundamental amplitude equal to $4/\pi$, which gives an output given by:

$$V_{out}(t) = I_{IF}(t)\, R_D \cdot \frac{4}{\pi} \cos \omega_{LO} t + \cdots \quad \text{(Equation 4.5)}$$

If $I_{IF}(t) = g_{m1}V_{IF} \cos \omega_{IF} t$, then the RF component at $\omega_{IF} + \omega_{LO}$ is equal to

$$V_{RF}(t) = \frac{2}{\pi}\, g_{m1}R_D V_{IF} \cos(\omega_{IF} + \omega_{LO})t \quad \text{(Equation 4.6)}$$

Then the voltage gain is equal to

$$\frac{V_{RF,p}}{V_{IF,p}} = \frac{2}{\pi}\, g_{m1}R_D \quad \text{(Equation 4.7)}$$

Similar analysis can be made for the double-balanced topology like Gilbert cell mixer (Figure 18, Figure 20). However, the current in each resistor is doubled because the currents from two branches are summed. Thus the load resistors should be $R_D/2$ to

maintain same voltage headroom for the transistors. The currents and output voltage are

$$I_1 = I_{IF} \cdot S(t) + (-I_{IF}) \cdot \overline{S(t)} \quad \text{(Equation 4.8)}$$

$$I_2 = I_{IF} \cdot \overline{S(t)} + (-I_{IF}) \cdot S(t) \quad \text{(Equation 4.9)}$$

$$V_{out}(t) = \left(I_1 \frac{R_D}{2} - I_2 \frac{R_D}{2}\right) = I_{IF} \cdot 2\left[S(t) - \overline{S(t)}\right] \cdot \frac{R_D}{2} = I_{IF} R_D \left[S(t) - \overline{S(t)}\right]$$

(Equation 4.10)

which is same as the single-balanced mixer. So the gain will be related to the waveform of $\left[S(t) - \overline{S(t)}\right]$ and the value is same as single-balanced mixer.

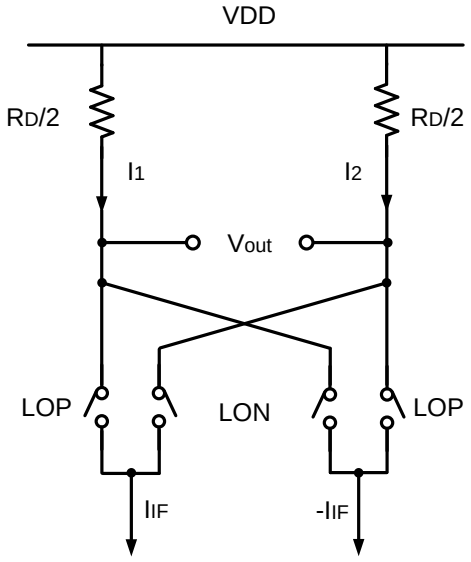


Figure 20. Equivalent circuit of double-balanced mixer

Similarly, for the mixer with 33% duty cycle LO signal, according to Equation 3.4, Equation 4.4, and Equation 4.5, the gain of the mixer is should be proportional to the fundamental of the LO waveform, thus

$$A_{CG} = \frac{3}{2\pi} g_m R_D \quad \text{(Equation 4.11)}$$

where g_m is the transconductance of the transconductance transistor.

The noise analysis of Gilbert cell mixer is difficult due to time invariance and frequency translation. Generally, there are three noise sources in a Gilbert cell mixer

[30]. The first noise source originates from transconductor, which determines the base noise floor. The second source is from switching pair. Non-ideal switching pairs will attenuate signal current and thus degrade noise figure. Additionally, switching pairs contribute additional noise if the rising and falling edge of LO signal are not ideal sharp transition. It is because that there exists a time interval that all the switching transistors are on and conducts current. The third noise source is the resistive load which will add noise directly to the output signal. The inductive load can be used to replace resistive load to get rid of this noise source if necessary.

There is a number of method proposed to minimize the noise figure [30]. High bias current can improve the transconductance of the mixer which will improve conversion gain and noise figure. An enough LO drive is preferred since it can further improve gain and noise performance. In addition, the minimum channel length is desirable for both the switching and transconductance transistor to improve conversion gain.

The linearity of the Gilbert cell mixer is primarily determined by the input transistors' overdrive voltage and the input transistor imposes a direct trade-off between the nonlinearity and noise given by Equation 4.12 and Equation 4.13 [13],

$$IP_3 \propto V_{GS} - V_{TH} \qquad \text{(Equation 4.12)}$$

$$\overline{V_{n,in}^2} = \frac{4kT\gamma}{g_m} = \frac{4kT\gamma}{2I_D}(V_{GS} - V_{TH}) \qquad \text{(Equation 4.13)}$$

Therefore, in order to increase circuit linearity while maintaining relative small noise, the bias current can be increased.

In this thesis, only basic mixer structure and moderate power consumption are required since the purpose is to explore the application of 33% duty cycle technique in active mixer based RF transmitter. This technique should be only dependent on the LO signals instead of mixer structure. Therefore, a conventional Gilbert cell structure mixer is chosen for the design of mixer element.

4.1.4 Mixer Element Design

Each of the mixer elements shown in Figure 21(a) composes of 3 active mixers with outputs connected together shown in Figure 21(b) and one current mode differential buffer shown in Figure 21(d). The active mixer is implemented as Gilbert cell which is

shown in Figure 21(c). Each mixer cell has a pair of differential baseband inputs clocked by differential LO signals. 3 active mixers' differential outputs are coupled together with a resistive load. There are two reasons to use resistive load instead of inductor in mixer element:

1) The target frequency is around 700 MHz to 1 GHz which is at sub-GHz range and the parasitic capacitance of the buffer input transistor is relatively small, thus the use of resistive load is acceptable;
2) The area can be saved significantly by using resistors instead of inductors.

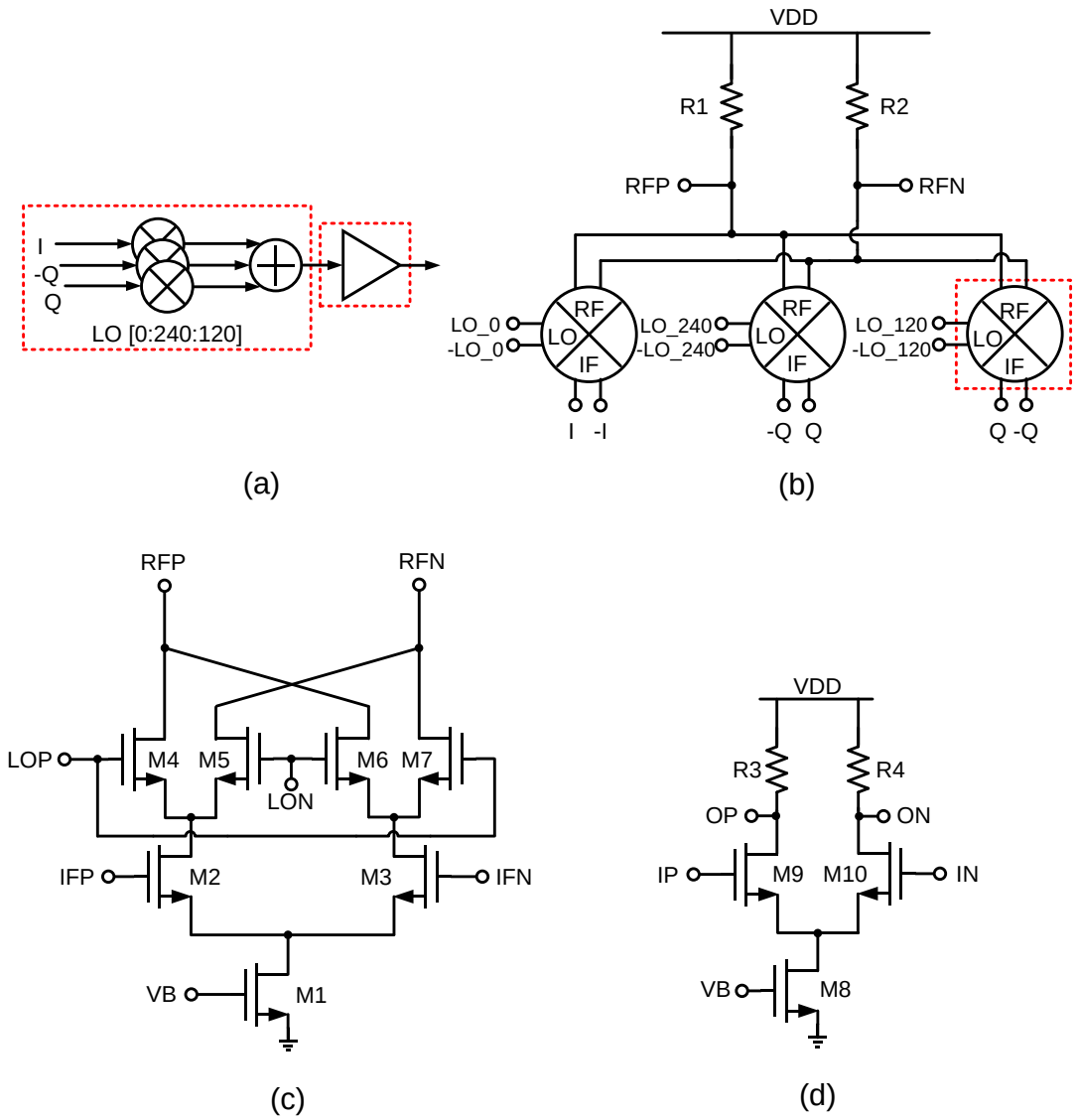


Figure 21. Circuit diagrams related to mixer element, (a) single mixer element, (b) connection of mixers' outputs, (c) single Gilbert cell mixer without load, (d) output buffer

A single Gilbert cell as shown in Figure 21(c) is simulated. In the simulation, the value of loading resistor is $1/3$ of the resistor value shown in Figure 21(b) to obtain same DC condition. The simulated gain is shown in Figure 22 which is 5.1 dB at the frequency of 1 GHz. The input referred 1 dB compression point is located at -3.1 dBm shown in Figure 23 and input referred 3rd-order intercept point is at 6.9 dBm shown in Figure 24. The power allocated for each Gilbert mixer is 2.3 mA.

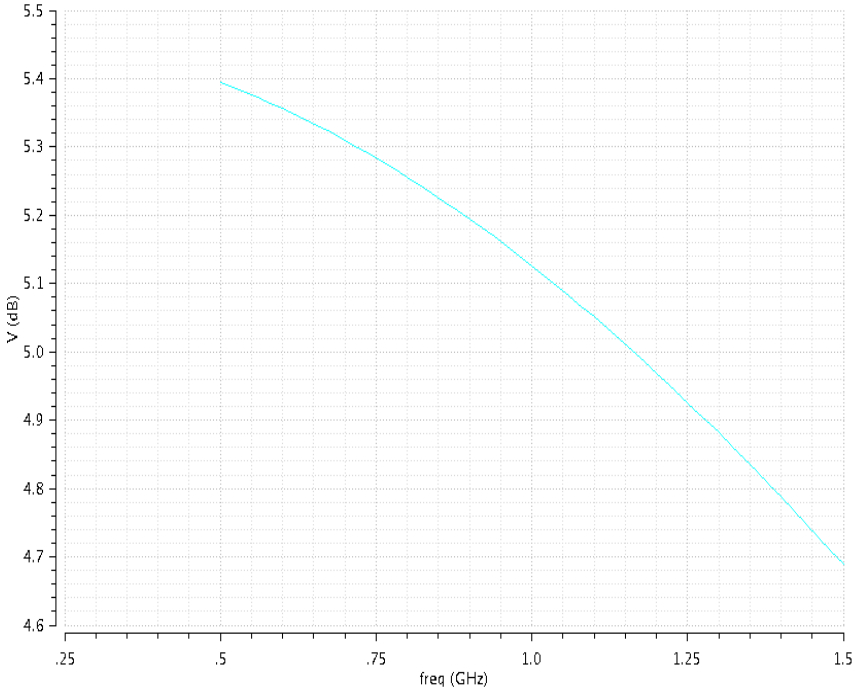


Figure 22. Simulation result of mixer gain

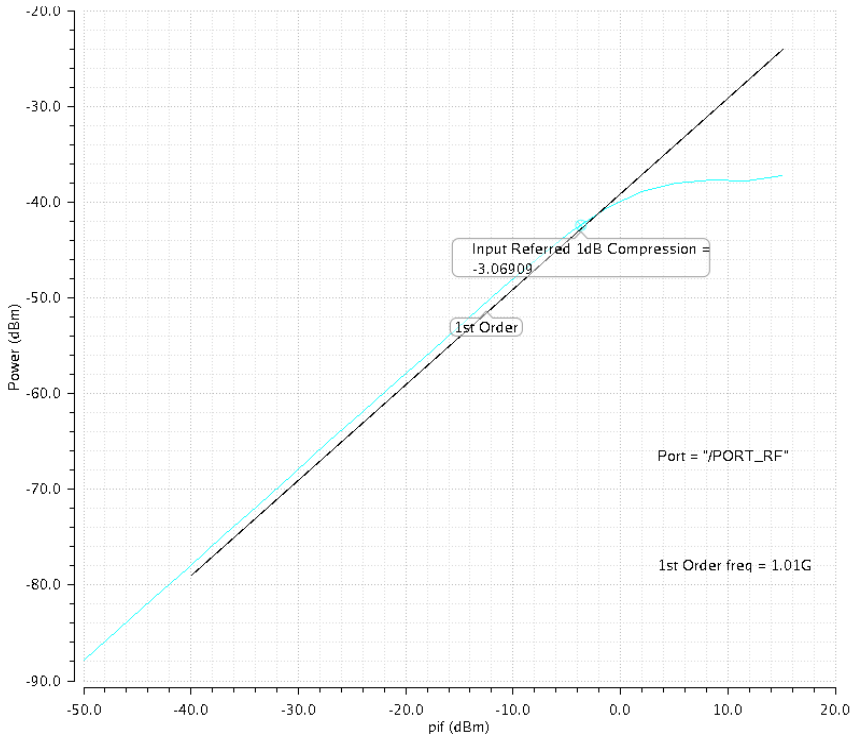


Figure 23. Simulation result of mixer IP1dB

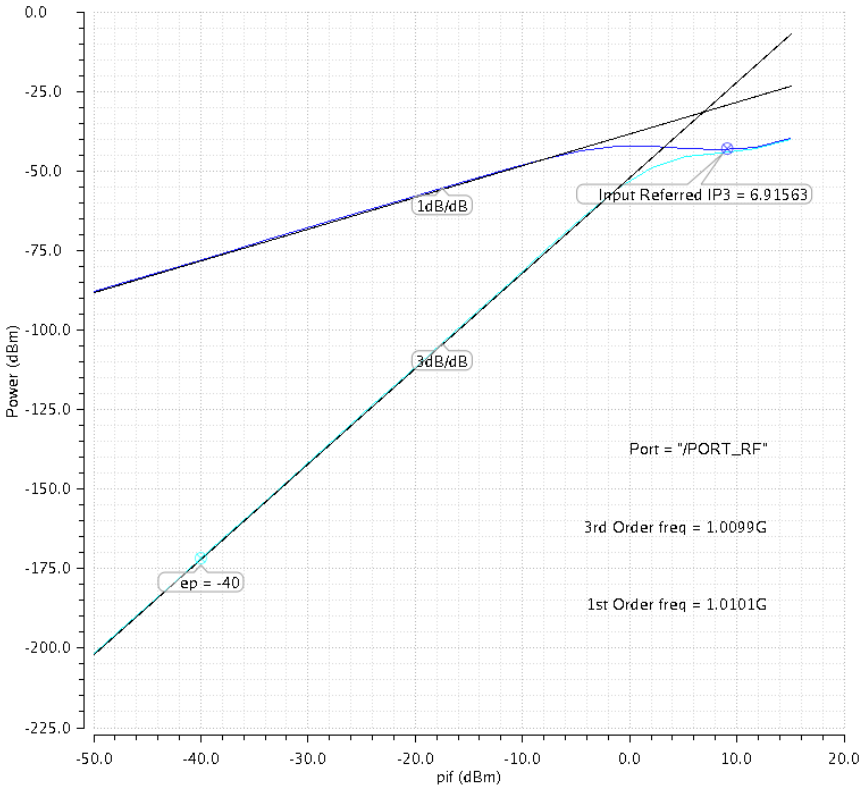


Figure 24. Simulation result of mixer IIP3

The circuit layout of one mixer element is shown in Figure 25. All the 3 LO signals are placed on the right-hand side horizontally with equal distance from each other in

order to minimize mismatch in this stage of design. The 2 pairs of baseband I-Q signal are placed vertically. Suppose the baseband I signal is given from top while the baseband Q signal is given from bottom. It can be seen that for each mixer, the distance of baseband signal path is different. The difference will become larger when stacking more than one mixer element. However, this type of placement can be accepted since the baseband signal is at relatively low frequency i.e. less than 10 MHz.

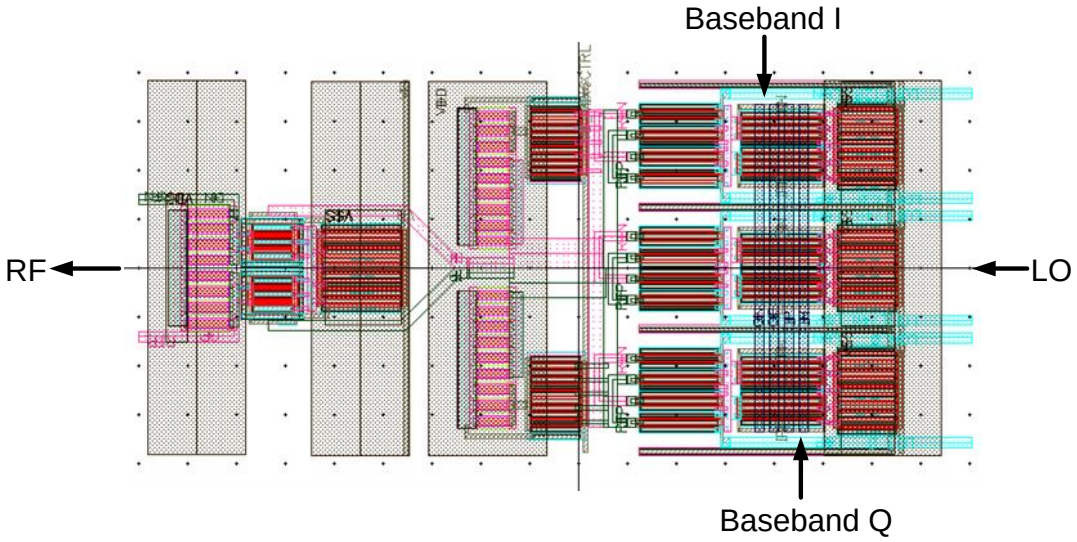


Figure 25. Layout of one mixer element

In summary, this section firstly investigates several common mixer structures and chooses Gilbert cell structure to explore the 33% duty cycle LO scheme. Each Gilbert cell has moderate gain and linearity. Three Gilbert cell mixers are combined, together with an output buffer, forms a mixer element. For each mixer element, it will upconvert one baseband I (or Q) signal and two baseband Q (or I) signals. The layout optimization of one mixer element has also been discussed in this chapter.

The designed transistors' size, resistor and capacitor values shown in Figure 21 are listed in Table 1.

Table 1. Designed values for the mixer element

Instance in Figure 21	Value
R1,R2	126Ω
M1	W/L=60/0.3μm, F=10, M=1
M2,M3	W/L=32/0.18μm, F=4, M=1
M4-M7	W/L=16/0.18μm, F=2, M=1
R3,R4	365Ω
M8	W/L=80/0.3μm, F10, M=1

M9,M10	W/L=16/0.18μm, F=4, M=1

4.2 Design of Divide-by-6 Circuit

4.2.1 General Considerations

The target of this block is to provide the differential quadrature LO signals with 33% duty cycle. There are several approaches shown in Table 2 to meet the requirements.

Table 2. Divider design comparison table

	FF based divide-by-3 circuit (this work)	TSPC divide-by-3 circuit [31]	Transfomer-feedback injection locking divider [32]	Specifications
Duty cycle	33%	33%	33%	33%
Differential phase	differential	single	differential	yes
I/Q output	no	no	yes	yes
Multi-phase	yes	yes	no	yes
Operating freq. (after dividing)	< 2GHz	1 GHz	7.5 – 8.7 GHz	0.7 - 1 GHz
Input freq. ratio	3×	3×	3×	-
max locking range	large	not reported	1.3 GHz	-
Area	small	small	large	small
Power consumption	> 10 mW	2.7 mW	1.7 mW	medium
Easy implementation	yes	yes	no	-

The first approach to realize 33% duty cycle signal is the traditional flip-flop based digital divider. The principle of this circuit has been mentioned in [11]. The approach is based on digital circuit design and 33% duty cycle can be easily achieved. It can also output multiple phases (e.g. 120°, 240°) by a digital method. The operating frequency is normally lower than 2 GHz which is dependent on the process and supply voltage used. The locking frequency range is large which can be improved by adjusting power and transistor size. Another benefit is the small die area since only flip-flops are used. However, a divide-by-3 circuit with single phase 50% duty cycle input clock is not able to provide quadrature outputs after dividing by 3. Instead, quadrature input clocks for divide-by-3 circuit should be provided to meet the requirement. This can be implemented by a divide-by-2 circuit. As a consequence, the total dividing ratio is 6 which will set the upper limit of operating frequency. Another

drawback is high power consumption since the static power consumption of flip-flop is high. Additionally, multi-phase outputs will consume additional power based on the number of phases needed.

Similar to the first approach, using true single phase clock (TSPC) circuit to implement a divide-by-3 circuit with 33% duty cycle is published in [31]. It has similar specifications of the digital flip-flop based divider. The advantage compared with the first approach is it has lower power consumption. Since it is digital based, it can provide a multi-phase output based on digital design method. However, it does not provide differential phase which is not suitable to meet the requirement for this prototype.

Another approach of quadrature output signal with 33% duty cycle can be realized by transformer-feedback injection-locked divide-by-3 frequency divider [32]. It enjoys the advantage of lower power consumption and low phase noise. However, it has two transformers which consume large die area and it is difficult to cover the target low-frequency range, i.e. below 3 GHz for input frequency. Moreover, it suffers from limited input locking range. After the dividing, additional circuits should be provided to implement multi-phase signals which will add more power budget in the design.

In this design, considering the priority of area efficiency and transmitter operating frequency, i.e. sub-GHz, the first approach, flip-flop-based digital divider, will be used and optimized in this design. In order to be differential and quadrature, the output signal is required to have 6 phases, i.e. 0°, 120°, 240°, 90°, 210°, and 330° (Figure 26). The circuit will be implemeted in the following sections to meet this requirement.

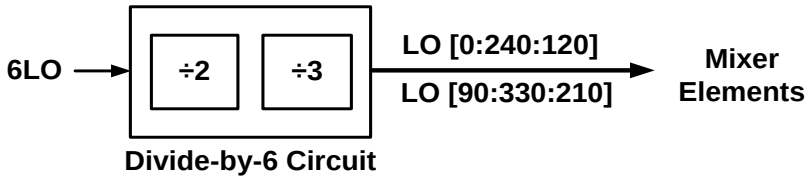


Figure 26. Circuit diagram of divide-by-6 circuit

Considering the output, the output V_{PP} should be around 0.6 V which will provide maximum gain for active mixers based on simulation. Buffers will be added before the mixers to achieve this requirement at a cost of certain power consumption.

For the output frequency, it should cover the range from 700 MHz to 1 GHz. Therefore, the divide-by-2 circuit should be able to divide the frequency up to 1 GHz × 6 = 6 GHz. In practical, considering the temperature and process variation, at least 1.2 times this frequency should be considered during simulation.

Besides, it is also important to have a compact and symmetric layout for this divider to minimize the routing distance and difference for each differential LO signal.

4.2.2 Divide-by-2 Circuit Design

The traditional CML based divide-by-2 circuit is used in this design which is realized by placing two D latches in a negative feedback loop as shown in Figure 27(a) and Figure 27(b). Suppose the input frequency is differential 6LO, after the divider circuit, differential in-phase and quadrature-phase 3LO will be generated at the output as shown in Figure 27(c).

The layout of this divide-by-2 circuit is shown in Figure 28. In order to have maximum symmetry, the clock path and feedback signal path are routed in 90 degree. The benefits of this type of layout are:

1) The circuit is complete symmetry for both input and output clock signals;
2) The differential inputs are close to each other and pointed at the same direction, which will benefit the overall layout;
3) The feedback signal path is minimized, the length is only slightly more than two times of the loading resistor length;
4) The differential outputs are close to each other and pointed at the same direction, which will minimize the mismatch before reaching the next stage;
5) Last but not least, the vertical length of a single latch is minimized. This layout method is applicable to all latch based designs.

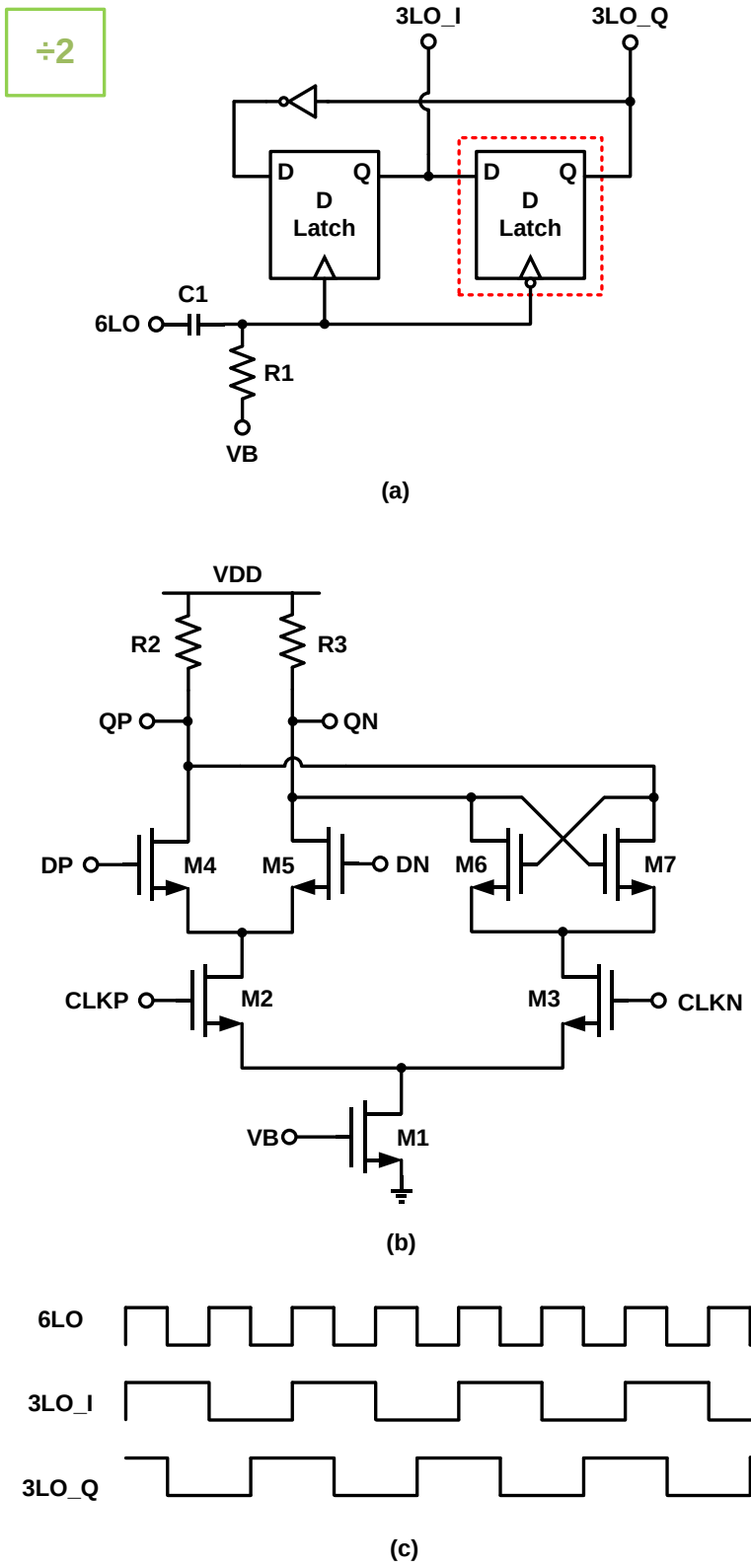


Figure 27. Circuit and timing diagram of divide-by-2 circuit, (a) circuit diagram of divide-by-2 circuit, (b) D latch, (c) divide-by-2 circuit I/Q outputs

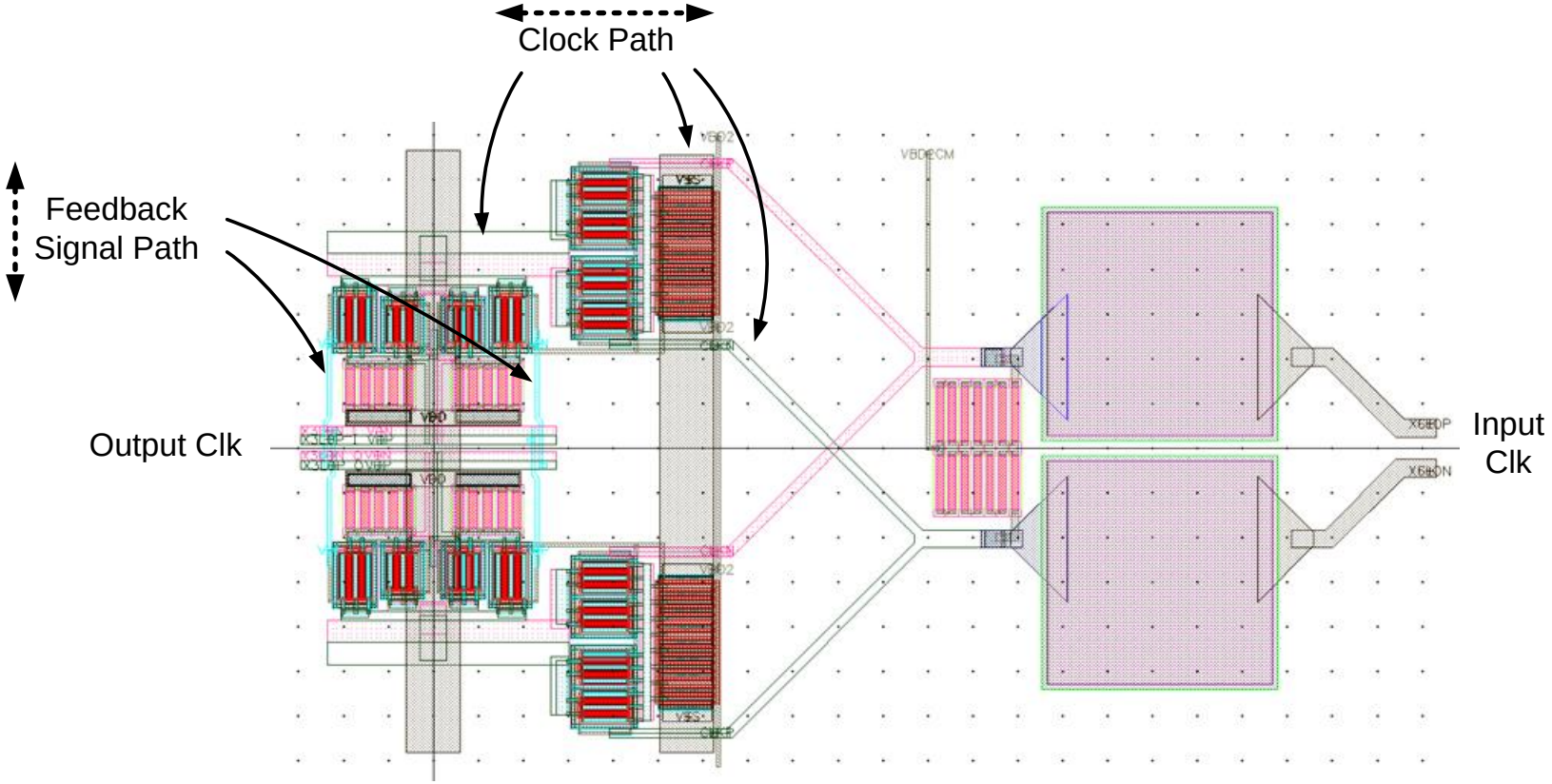


Figure 28. Layout of divide-by-2 circuit

4.2.3 Divide-by-3 Circuit Design

The conventional CML based divide-by-3 circuit is shown in Figure 29(a). It is composed of 2 D flip-flops (DFF) and 1 NOR logic. The DFF circuit and D-latch are shown in Figure 29(b) and Figure 29(c). The DFFs are clocked by 3LO and this circuit will generate 33% duty cycle LO signal. Suppose this signal has a phase of 0° and labeled as LO_0. More DFFs can be cascaded after the LO_0 to generate LO signals with phases of 240° and 120°. One dummy latch is placed at the last stage to provide a proper parasitic load for LO_120.

However, this kind of design suffers from excessive parasitic capacitance at node X. The load at X includes 2 DFF input transistors, input transistor of NOR logic, and input transistor of the output buffer.

An improved design to alleviate loading capacitance at node X is shown in Figure 30. Firstly, the NOR logic is placed at the input of the leftmost DFF. Secondly, one DFF is cascaded after node X and the LO_0 is defined at the output of this inserted DFF. As a result, the contribution of the parasitic load at node X is only from one NOR logic input, one DFF input, and buffer input.

The further improvement is shown in Figure 31. The NOR logic is merged into a D latch to become an OR-Latch in Figure 32(a). The detailed circuit diagram is depicted in Figure 32(b). Thus the circuit can be simplified.

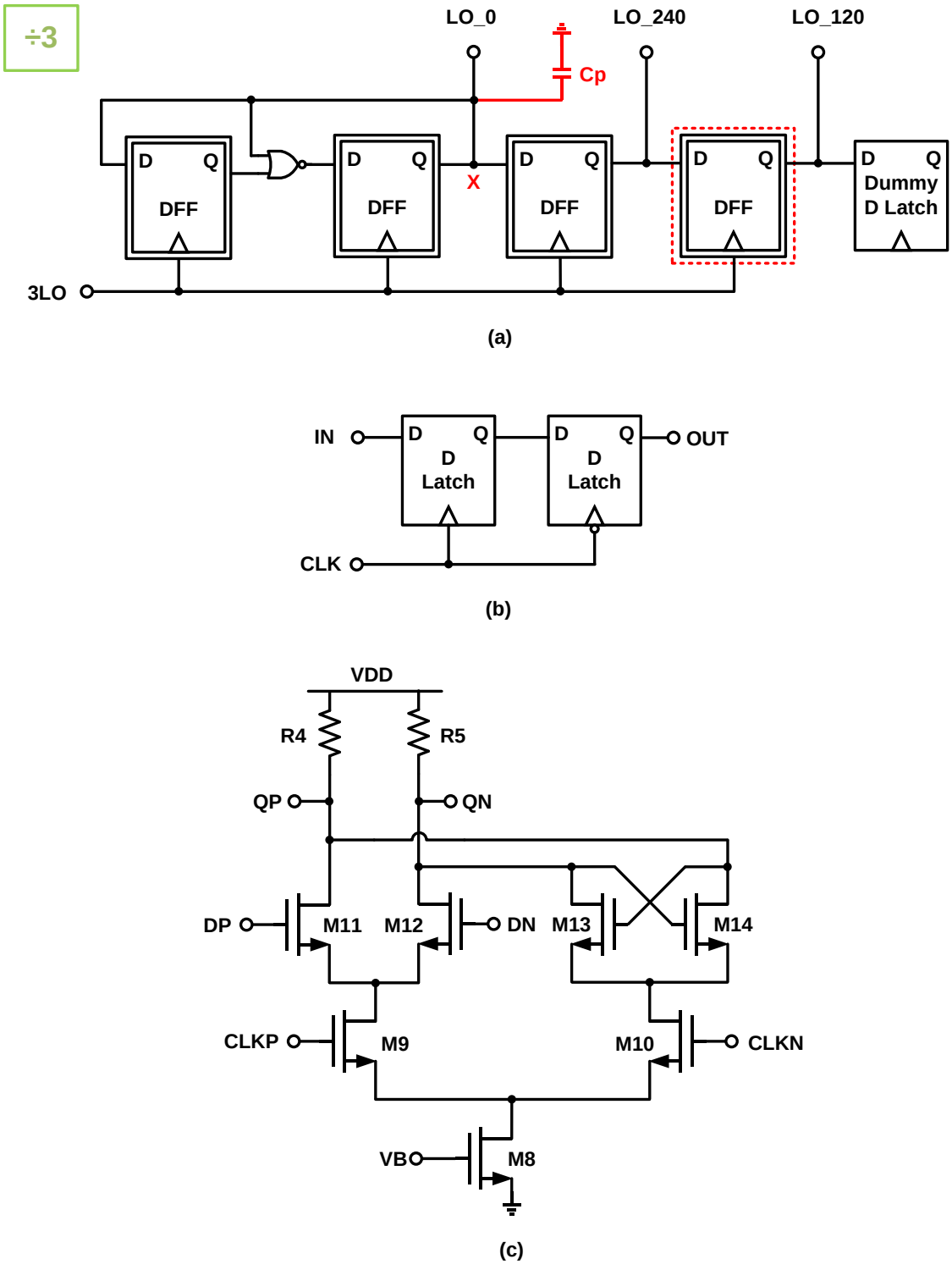


Figure 29. Circuit diagram of conventional divide-by-3 circuit (Ver.1), (a) divide-by-3 circuit, (b) DFF, (c) D latch

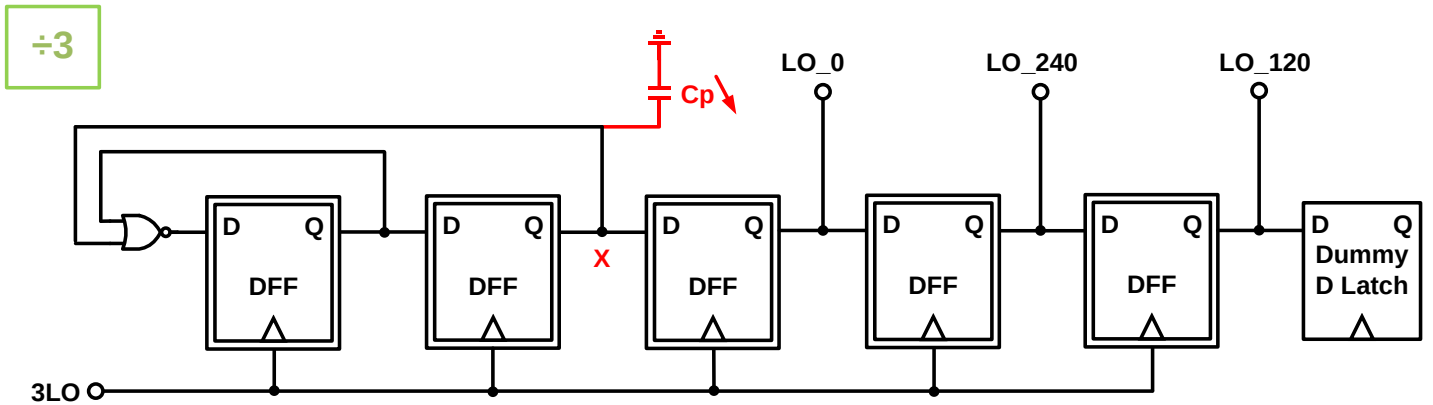


Figure 30. Circuit diagram of divide-by-3 circuit (Ver.2)

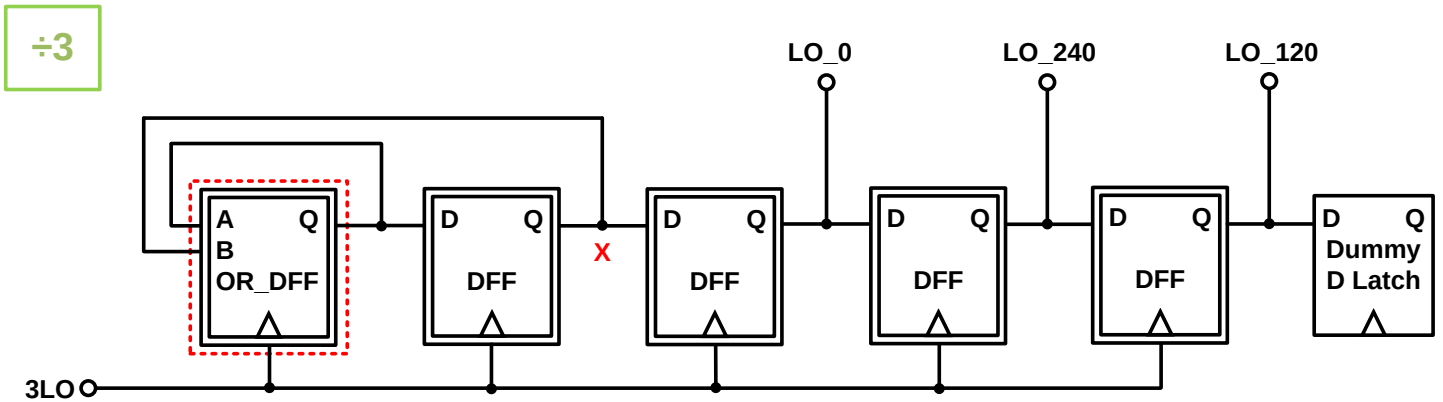
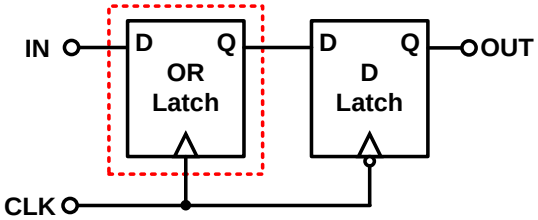
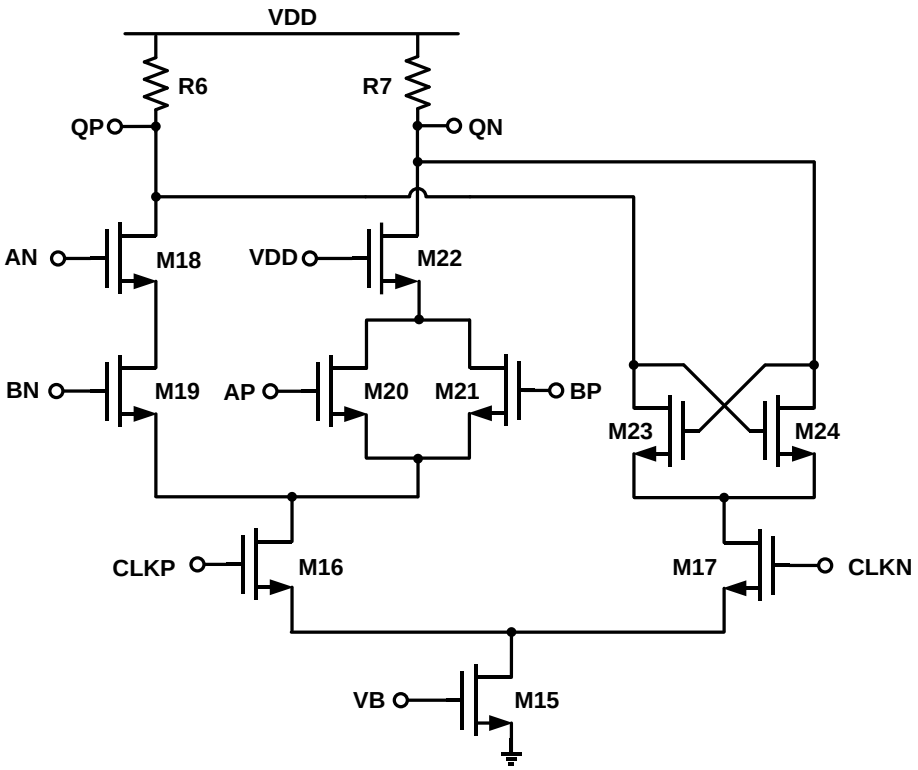


Figure 31. Circuit diagram of divide-by-3 circuit (Ver.3)



(a)



(b)

Figure 32. Circuit diagram of divide-by-3 circuit (Ver.3) (Conti.), (a) OR_DFF, (b) OR_Latch

For the real application, the quadrature LO signals are required. This is implemented by feeding quadrature 3LO from divide-by-2 circuit into cascade DFFs. The circuit is depicted in Figure 33. The first 2 DFFs are "initiation blocks", together with the following 3 DFFs, the first 5 DFFs are clocked by 3LO_Q. Then the LO_120 is input into the 6^{th} DFF which is clocked by 3LO_I. The LO signal with a phase of 90° can be obtained at the output of 6^{th} DFF. As shown in the timing diagram in Figure 34, the $\pi/2$ phase difference of 3LO signal will result in a $\pi/6$ difference of LO signal. Therefore, the I-Q divide-by-3 circuit is completed.

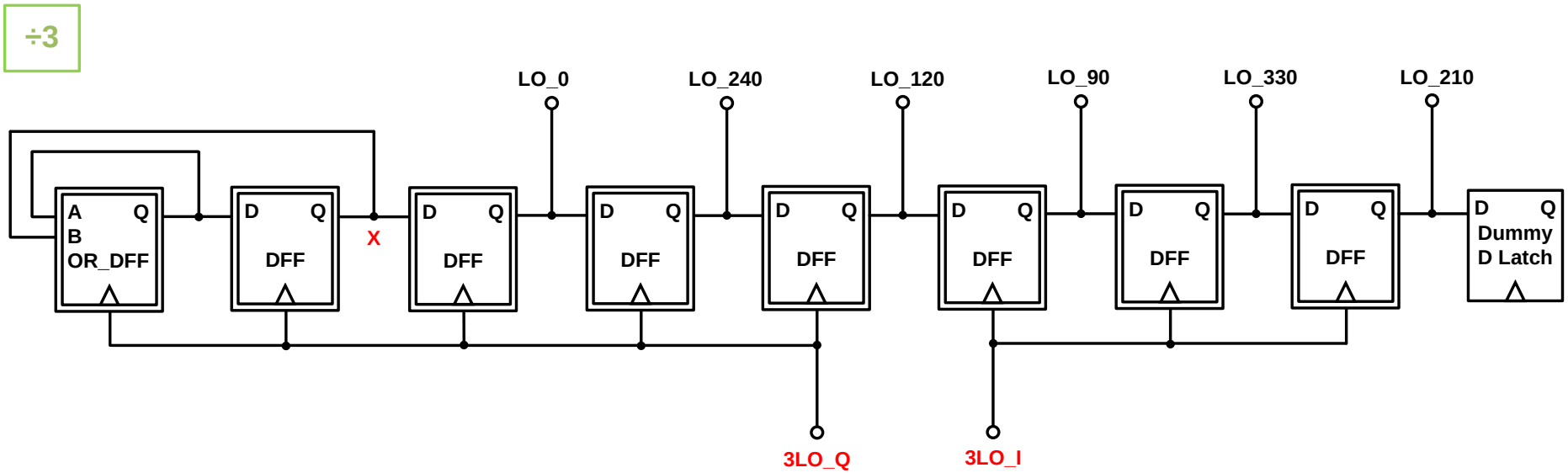


Figure 33. Circuit diagram of divide-by-3 circuit with quadrature phases (Ver.4)

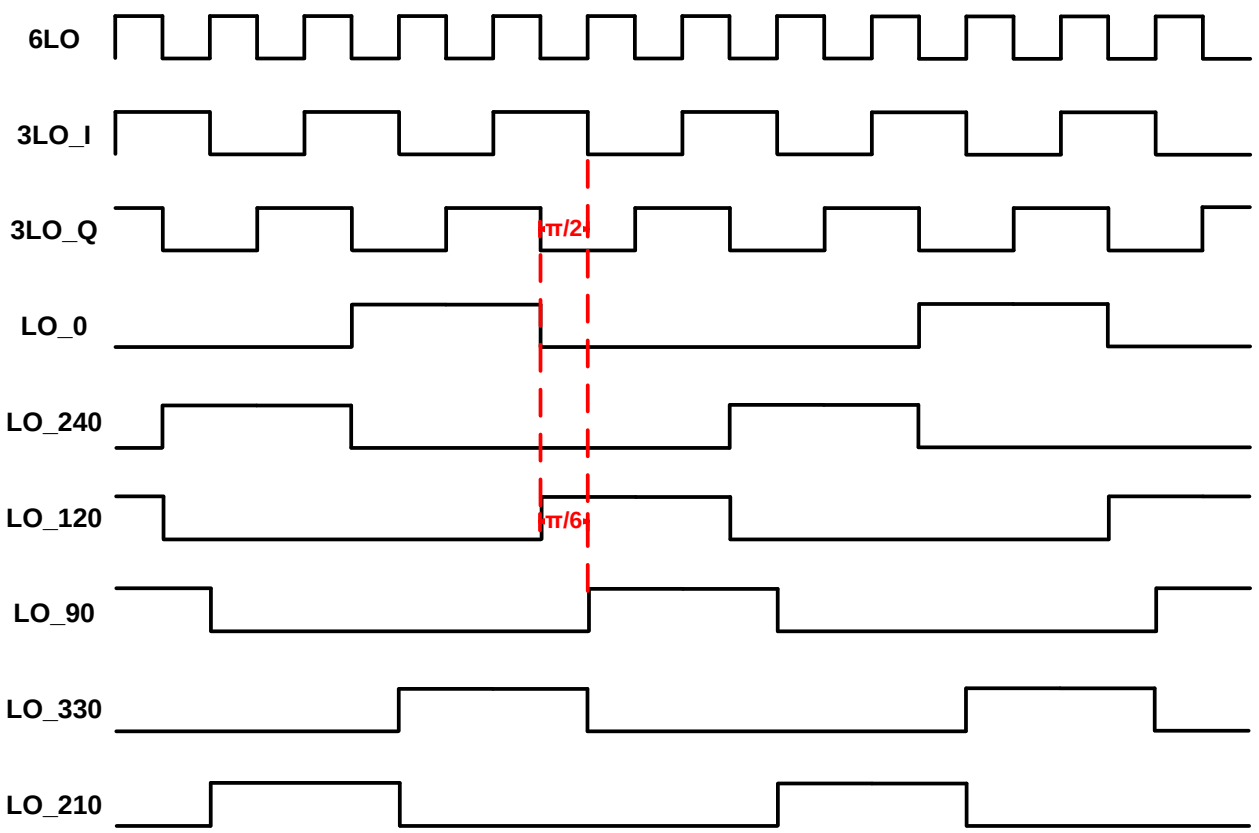


Figure 34. Timing diagram of divide-by-3 circuit with I-Q phases

The following paragraphs will discuss the layout technique for the proposed divide-by-3 circuit. For both DFF and OR-DFF, since they are latch based structure, same layout technique as divide-by-2 can be applied.

Figure 35 displays a layout of a DFF which is composed of 2 latches. Similar to divide-by-2 circuit layout, the clock path and signal path are routed with an angle of 90 degree. It also has similar benefits when applying this type of layout technique:

1) The circuit is symmetry for both input and output clock signals;
2) The differential inputs are close to each other and pointed at the same direction, which will benefit the overall layout;
3) The length of the signal path is shortened, which is about 4 times the width of one routing metal line as shown in Figure 35. So if more DFF stages need to be cascaded as shown in Figure 33, the overall vertical length can be minimized;
4) The differential outputs are close to each other and pointed at the same direction, which will minimize the mismatch before reaching the next stage.

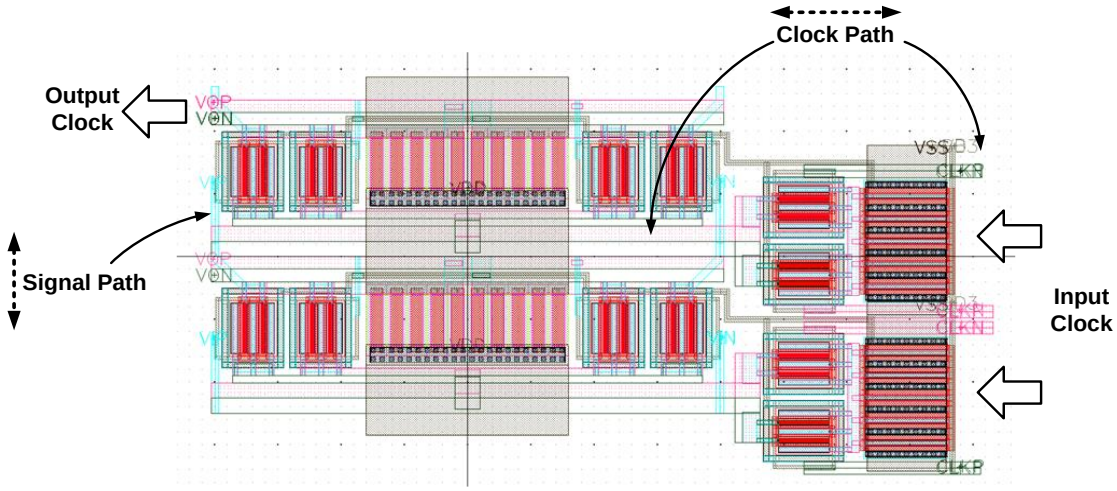


Figure 35. Layout of DFF

Figure 36 depicts the overall divide-by-3 circuit layout. The "initiation blocks" are placed at the bottom and all the 6 outputs are aligned on the top. By applying the layout technique mentioned before, the minimized vertical length is achieved.

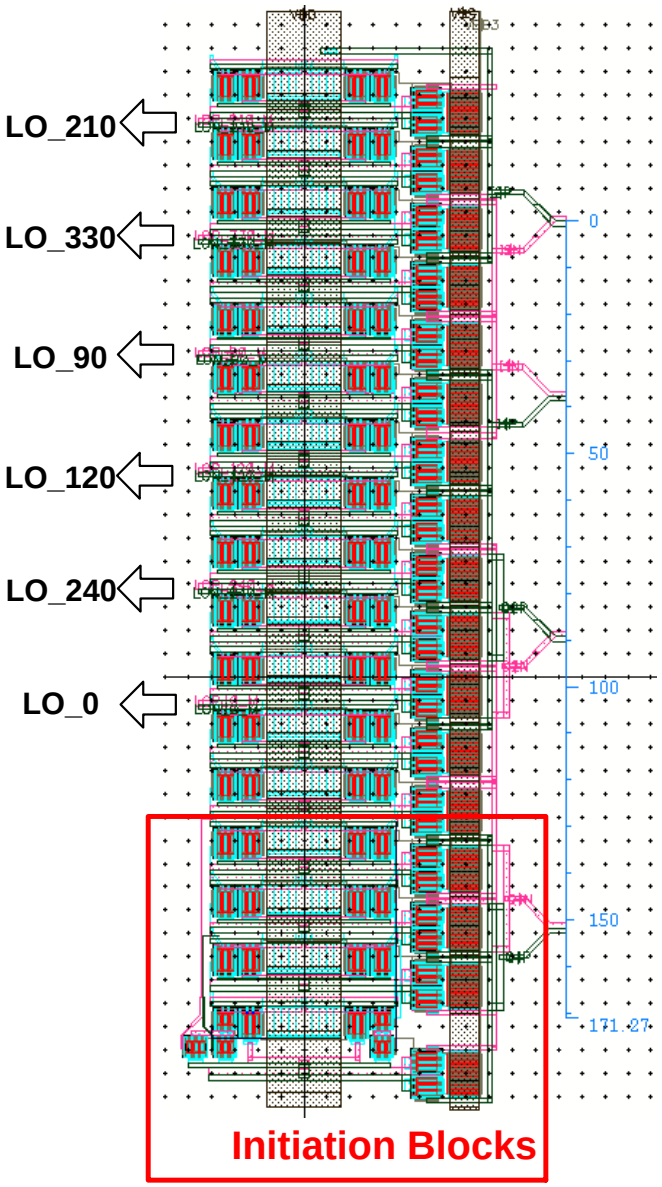


Figure 36. Layout of divide-by-6 circuit

4.2.4 Divide-by-6 Circuit Design

The overall divide-by-6 circuit is shown in Figure 37. The connection between divide-by-2 and divide-by-3 circuit is discussed in this section. It is found that single stage driver is not able to drive up to 6 numbers of DFF input in the divide-by-3 circuit. To realize the good driving capability, cascade buffer technique is used where 2 stages of buffers are connected in a tree structure. The number of the second stage buffer is doubled to ensure the driving capability. In addition, the 2 latches in the 3rd and the 7th DFFs are clocked with the same clock but from different 2nd stage buffers. The purpose is to balance the loading of 2nd stage buffer. However, there will still be a

mismatch between Q path and I path since each 2nd stage 3LO_Q buffer drives 5 latches while 3LO_I buffer drives only 3 latches. This can be solved by cascading more dummy DFFs for 3LO_I but which is not necessary. The difference can be minimized by slightly increasing the power of 2nd stage buffer.

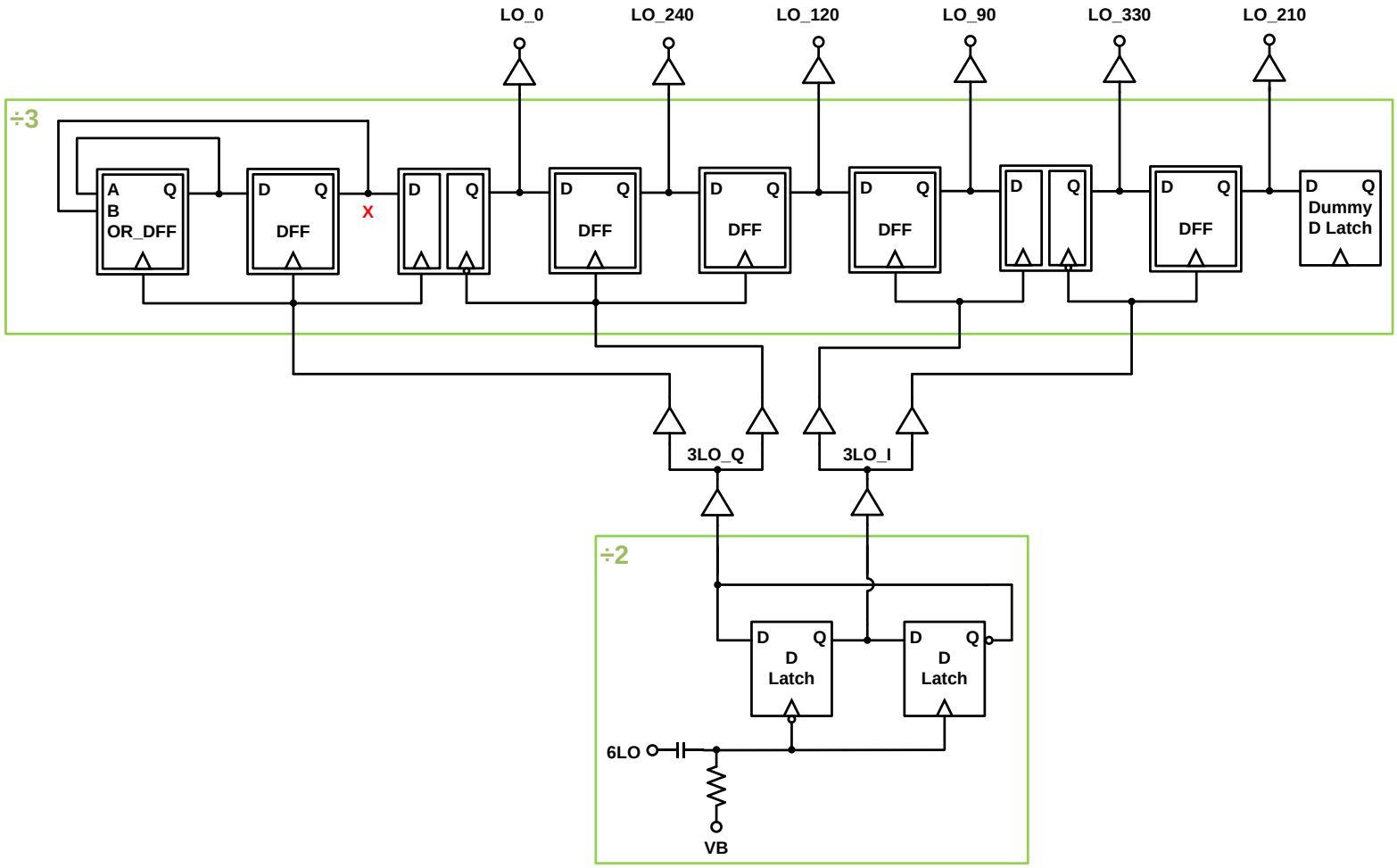


Figure 37. Circuit diagram of divide-by-6 circuit

The layout of the overall divide-by-6 circuit is shown in Figure 38. The 6-phase LO outputs are placed on the left side with equal spacing. Thick and wide metal is used for power and ground path to tolerate the high current consumption of this block.

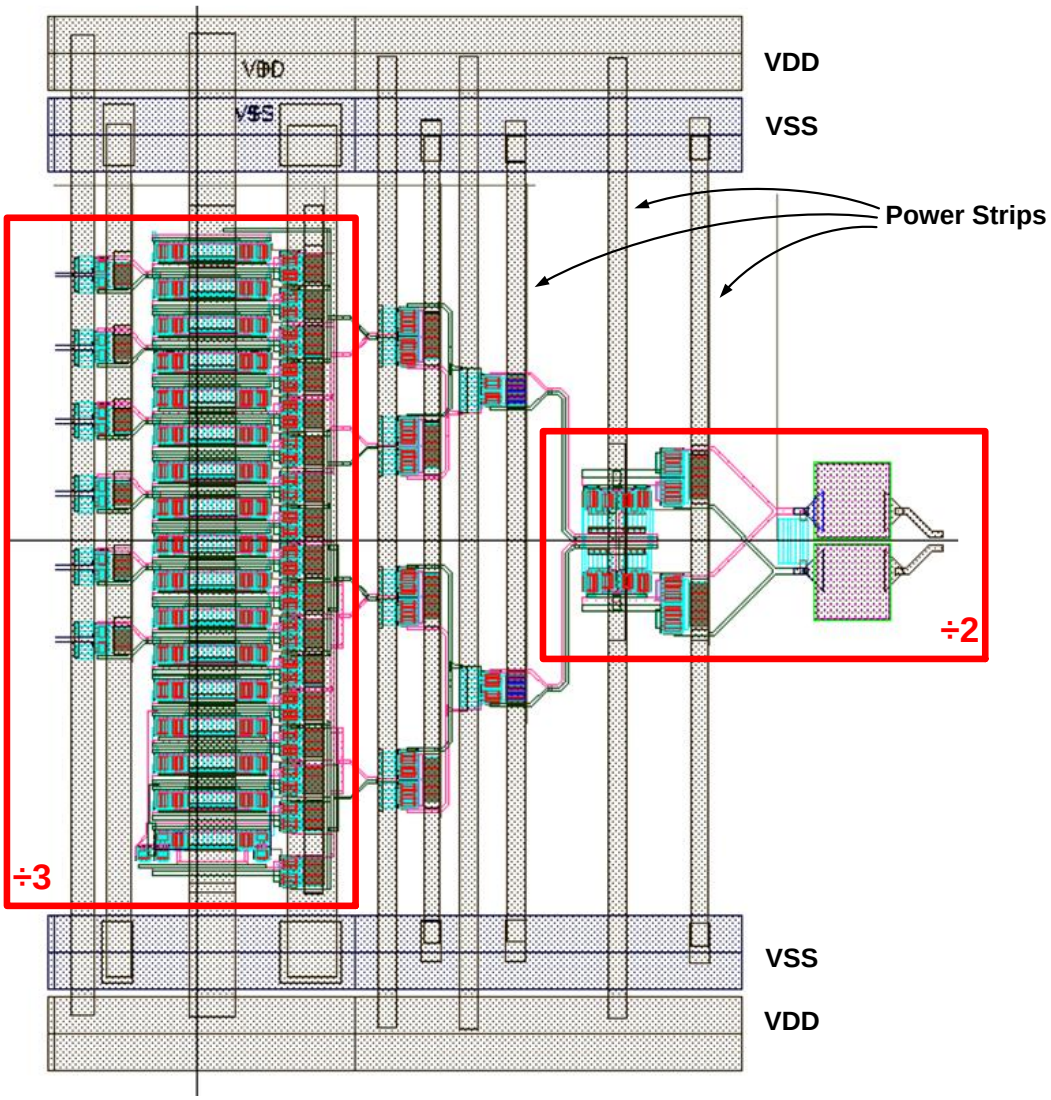


Figure 38. Layout of divide-by-6 circuit

Simulation result of this divide-by-6 circuit is shown in Figure 39 to Figure 42. 1 GHz frequency is used as an example. In this version of design, 6 phases are used. Simulation of one phase differential LO signal is shown in Figure 39. The peak-to-peak voltage is around 0.7 V. Its spectrum in Figure 40 shows that it has more than 45 dB attenuation for the signal's 3rd-order harmonic component compared to fundamental frequency component. 3 phase outputs e.g. 0°, 120°, 240° are shown in Figure 41 and quadrature outputs are shown in Figure 42, e.g. 0°, 90°.

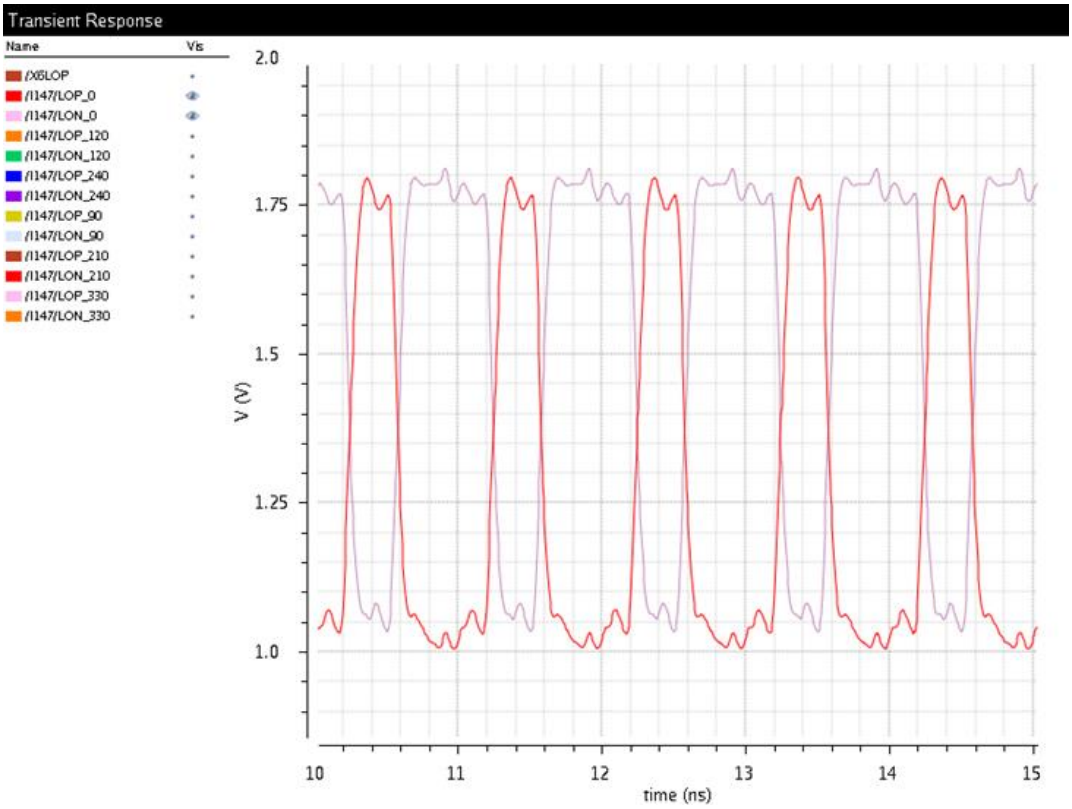


Figure 39. Simulation result of divide-by-6 circuit single phase differential outputs

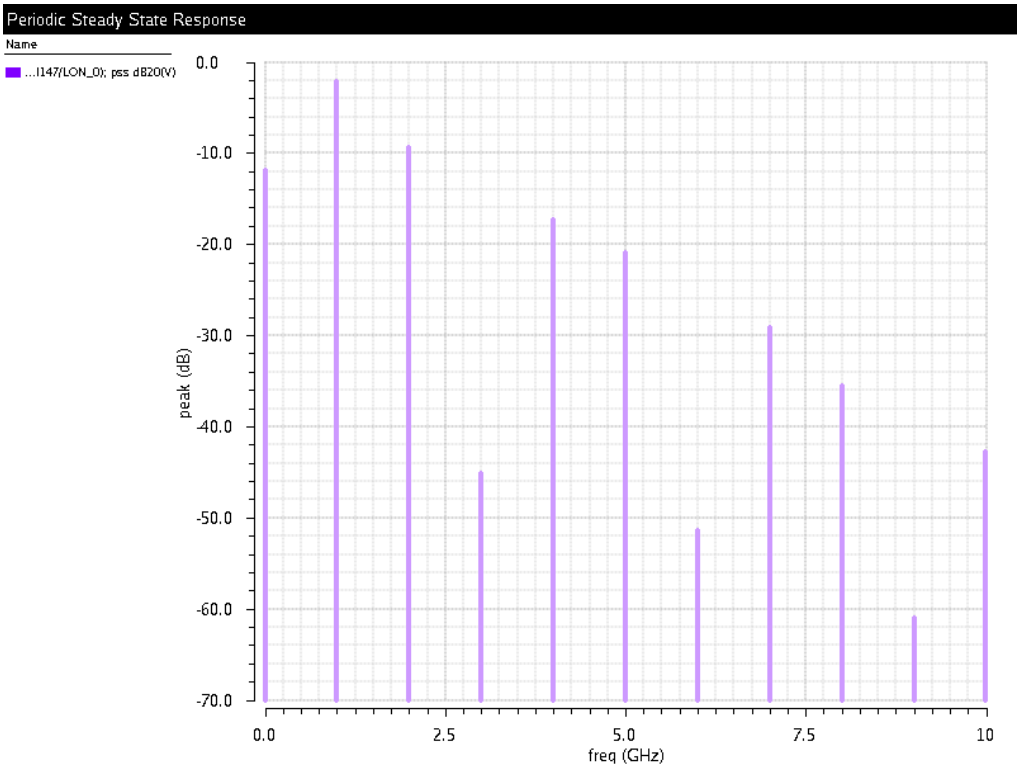


Figure 40. Simulation result of divide-by-6 circuit output spectrum

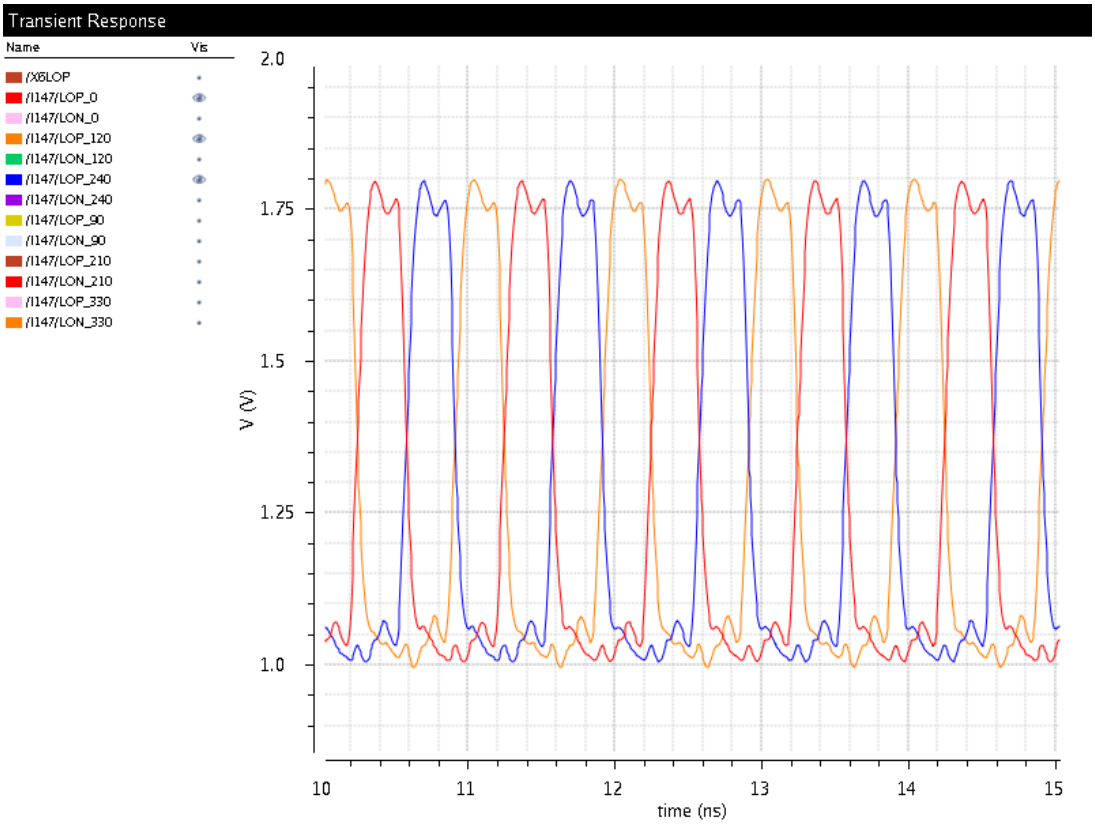


Figure 41. Simulation result of divide-by-6 circuit 3-phase outputs

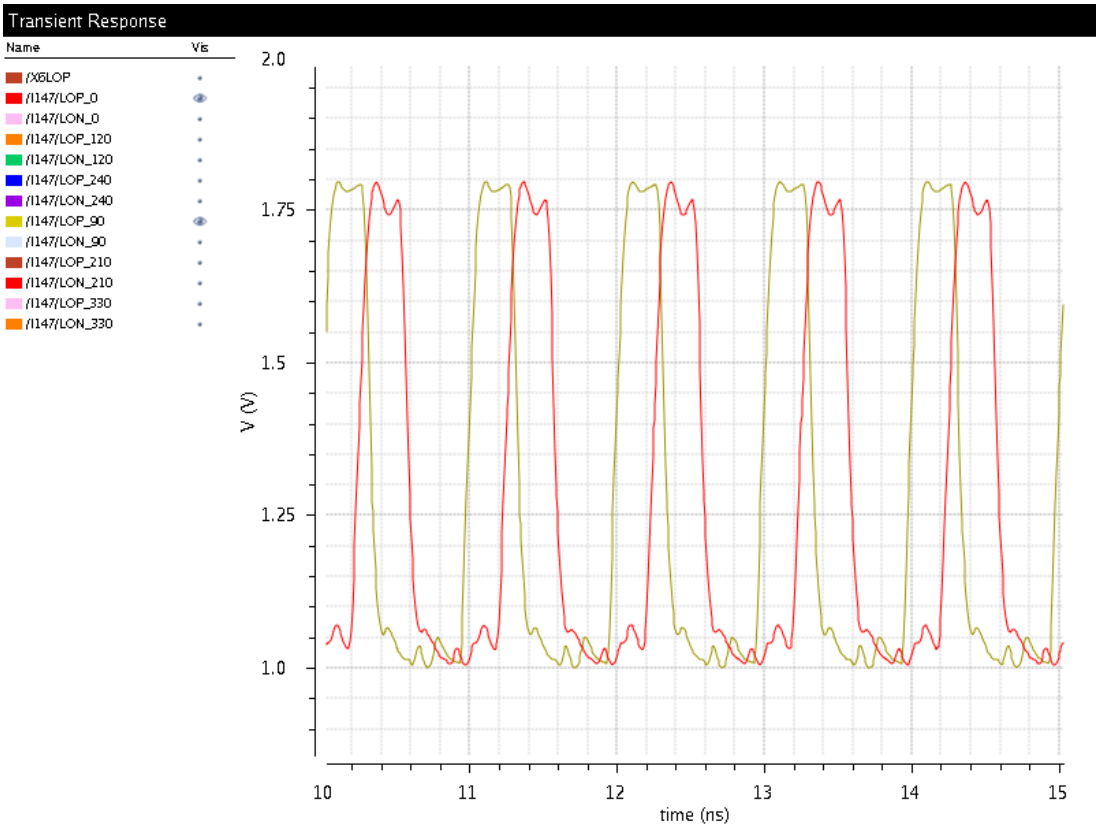


Figure 42. Simulation result of divide-by-6 circuit quadrature outputs

To summarize, this section describes the design procedure to produce required quadrature LO signals. It is implemented by a divide-by-6 circuit which is composed of a divide-by-2 circuit and a divide-by-3 circuit. The parasitic effect is the focus of study and has been fully discussed. The outputs of this module are 6-phase differential signals which are buffered and will be connected to mixer elements. The simulation result proves that the integer multiples of 3rd-order harmonics are greatly suppressed which is coincide with the theory. In addition, the layout techniques for each block along with the top module have been depicted in detail.

The designed transistors' size, resistor and capacitor values for divider circuits are listed in Table 3.

Table 3. Designed values for divide-by-6 circuit

Instance in Figure 27	**Value**
R1	15.9kΩ
C1	0.64pF
R2,R3	292Ω
M1	W/L=96/0.36μm, F=16, M=1
M2,M3	W/L=40/0.18μm, F=4, M=2
M4,M5	W/L=20/0.18μm, F=4, M=1
M6,M7	W/L=16/0.18μm, F=4, M=1
Instance in Figure 29	**Value**
R4,R5	292Ω
M8	W/L=64/0.36μm, F=10, M=1
M9,M10	W/L=16/0.18μm, F=4, M=1
M11,M12	W/L=16/0.18μm, F=4, M=1
M13,M14	W/L=16/0.18μm, F=4, M=1
Instance in Figure 32	**Value**
R6,R7	292Ω
M15	W/L=64/0.36μm, F=10, M=1
M16,M17	W/L=16/0.18μm, F=4, M=1
M18	W/L=8/0.18μm, F=4, M=1
M19	W/L=8/0.18μm, F=4, M=1
M20,M21	W/L=8/0.18μm, F=4, M=1
M22	W/L=8/0.18μm, F=4, M=1
M23,M24	W/L=16/0.18μm, F=4, M=1

4.3 Design of Output Stage

Basically, the output stage in a transmitter has the function to provide the driving capability of the large input transistor of the power amplifier. In this design, the output of RF front-end circuit is directly connected to the testing equipment instead of power amplifier, so it needs to provide 50 Ω matching for the testing. Figure 43(a) depicts the output stage circuit diagram which is composed of 2 cascaded PA drivers.

The 1st PA driver is shown in Figure 43(b). It is a current mode differential pair with source degeneration to have a moderate gain and good linearity. The outputs from mixer elements are coupled to the input of first PA driver. A resistive load is used for this stage of PA driver since the input transistor size of 2nd stage PA driver is relatively small.

In the 2nd stage of PA driver shown in Figure 43(c), an inductive load is used to drive the large parasitic capacitance of PA input transistor. Even through PA is not included in testing, the input port loading of test equipment and PCB components still need to be taken into account. The loading can be as large as pF in parallel with 50 Ω. In this design, the inductor is designed for area efficiency with low Q value. Shunt peaking of the inductor with one triode region biased PMOS transistor will further decrease Q value of the load. Together, the inductor and the transistor are used as load to cover the frequency range from 700 MHz to 1 GHz and match for 50 Ω.

The block of output stage has been simulated individually and the simulation results are recorded. The overall voltage gain is around 6 dB from 700 MHz to 1 GHz as shown in Figure 44. The input referred 1 dB compression point is -2.5 dBm for the frequency of 1 GHz. The most important specification is the output reflection, S22, which is < -15 dB from 200 MHz to 1.45 GHz shown in Figure 45 (Note that the balun used in the simulation is ideal).

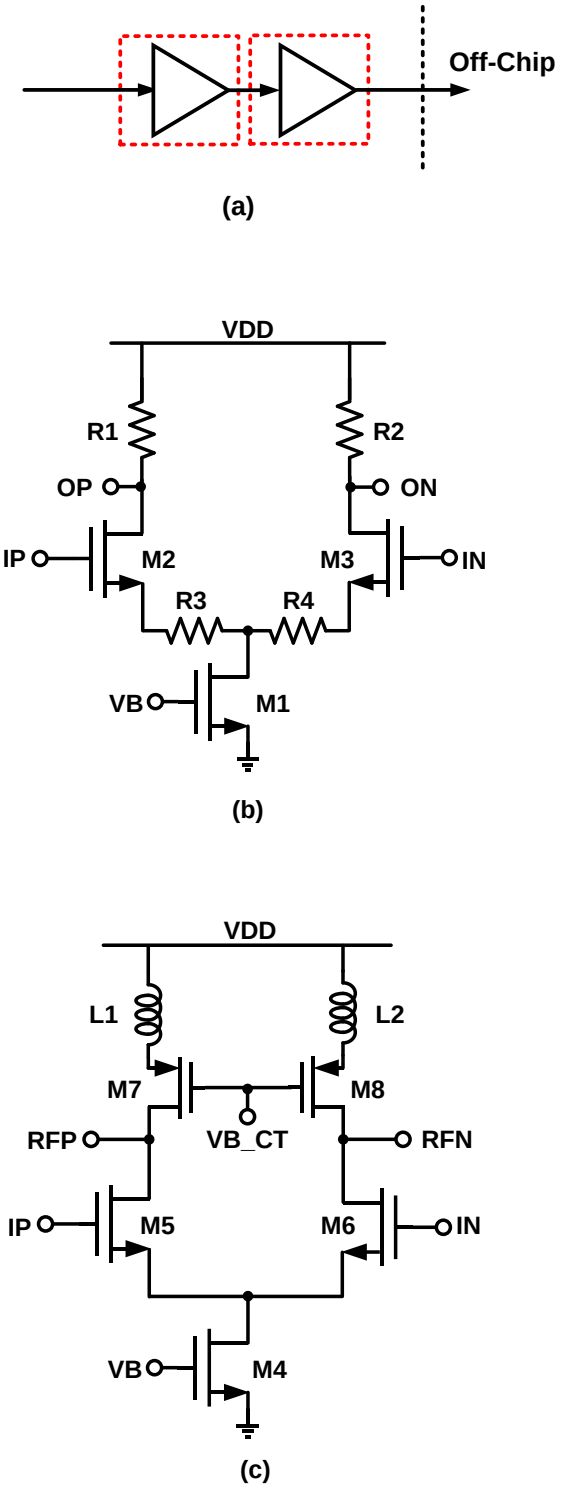


Figure 43. Circuit diagram of output stage PA drivers, (a) 2-stage PA driver, (b) 1st stage PA driver, (c) 2nd stage PA driver

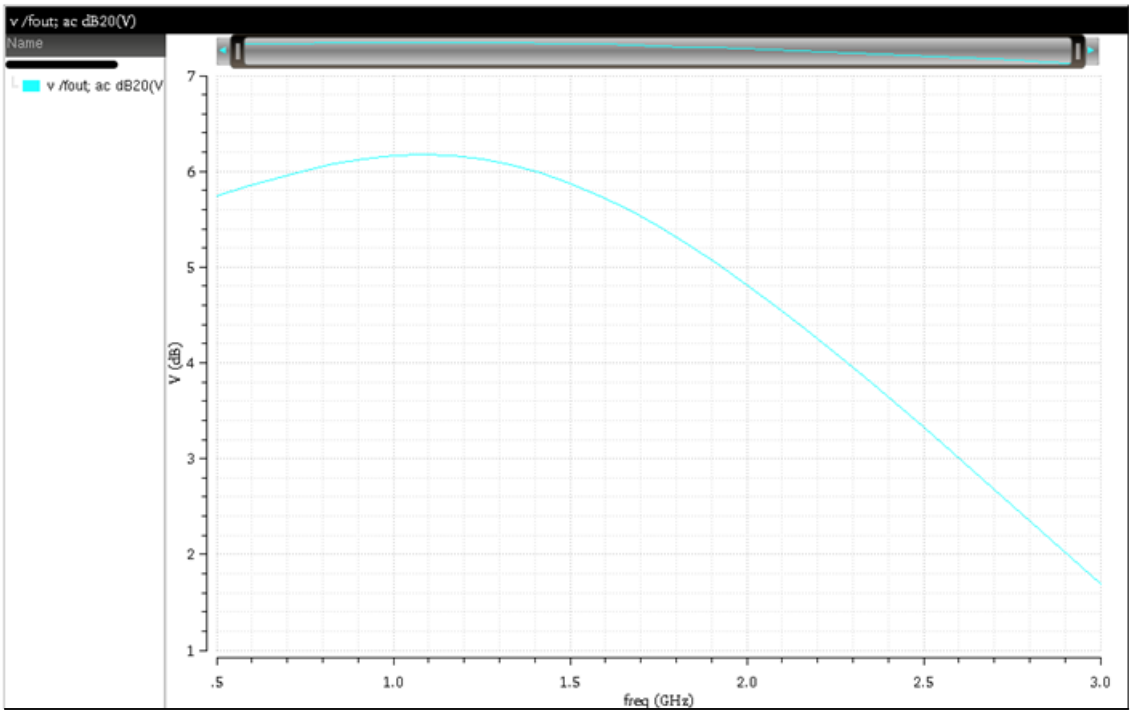


Figure 44. Simulation result of output stage gain

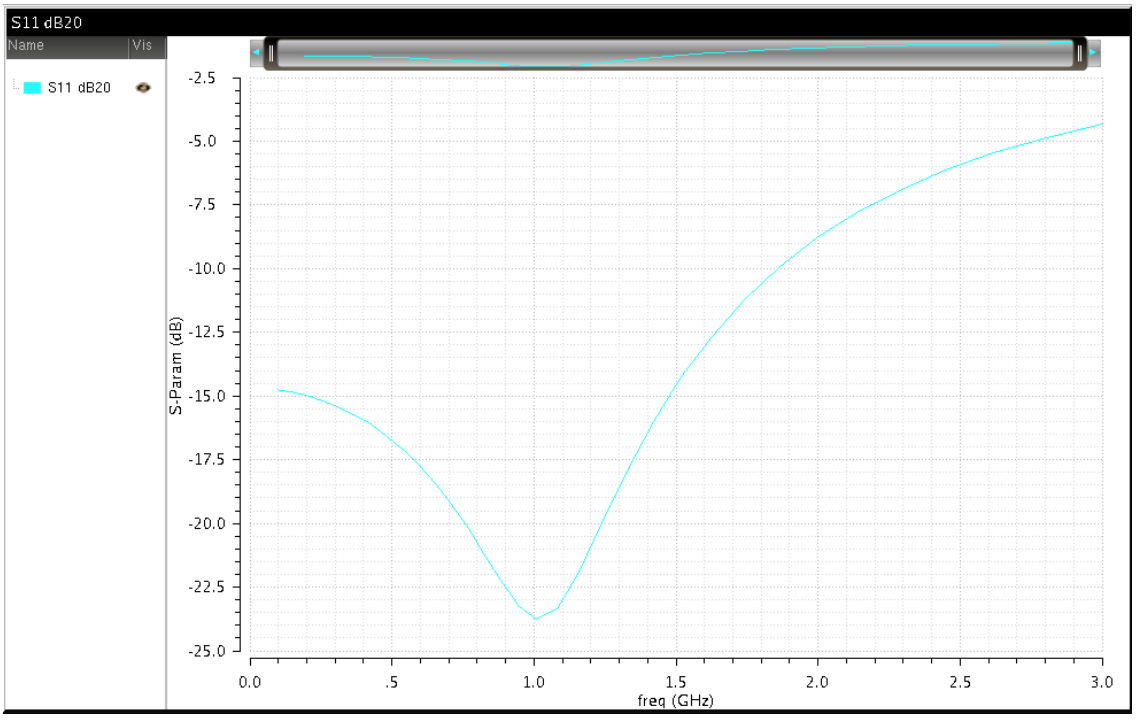


Figure 45. Simulation result of output stage S22

In a conclusion, the design of output buffer stage is discussed in this section. It consists of 2 stages and designed for 50 Ω match at the output. It is designed to meet the matching requirement, <-10 dB, in the frequency range from 700 MHz to 1 GHz.

The designed transistors' size, resistor and capacitor values for the output stage are listed in Table 4.

Table 4. Designed values for output stage circuit

Instance in Figure 43	Value
R1,R2	325Ω
R3,R4	12Ω
M1	W/L=64/0.18μm, F=16, M=1
M2,M3	W/L=16/0.18μm, F=4, M=1
L1,L2	4nH
M4	W/L=700/0.36μm, F=50, M=1
M5,M6	W/L=128/0.18μm, F=4, M=4
M7,M8	W/L=160/0.18μm, F=23, M=1

CHAPTER 5 Test and Measurement

In this chapter, layout, test and measurement of the designed transmitter will be discussed. The top level chip layout is firstly discussed to accommodate for testing on PCB. It is followed by PCB design. Finally, the measurements result will be presented and compared.

5.1 Top Level Chip Layout Design

The overall die micrograph for the designed transmitter is shown in Figure 46. The figure highlights the placement of each circuit block, VDD/GND pads, input and output ports and chip size.

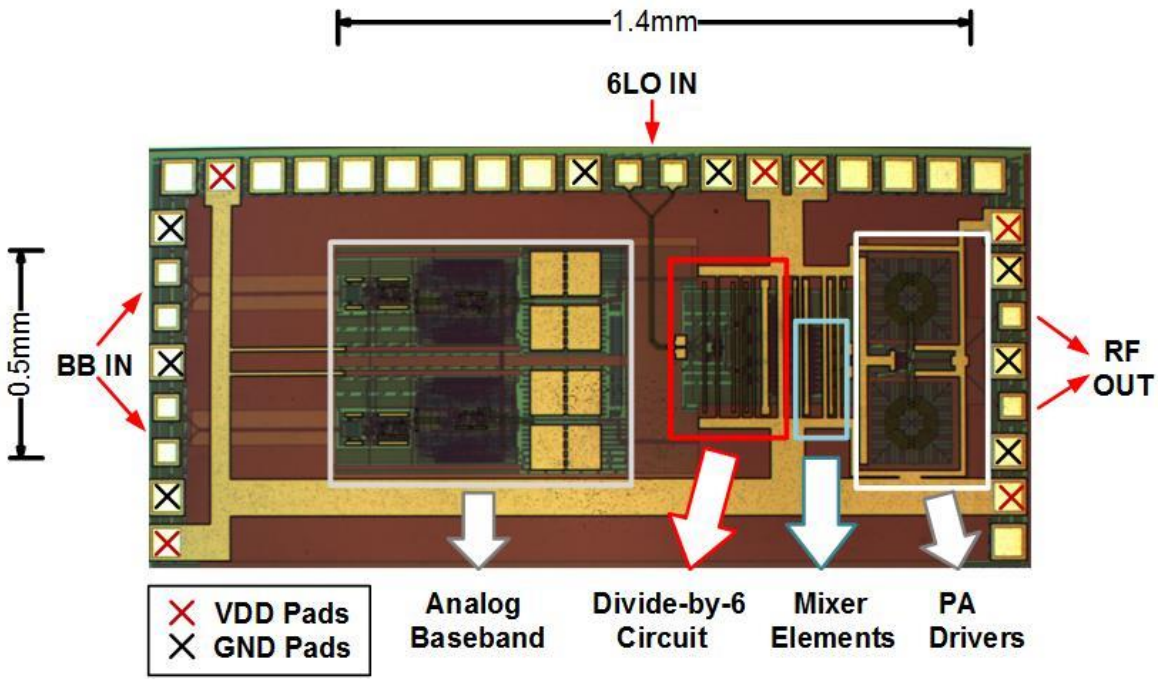


Figure 46. Die micrograph of designed transmitter

The first design consideration is the balance of power nets. In this design, both divider block and PA driver block consume tens of mAs. For such high current, thick and wide VDD/GND metal should be considered to reduce IR-drop. In addition, multiple VDD and GND pads are also placed at different corners to balance the power and ground nets. As shown in Figure 46, the VDD pad is labeled by a red cross and GND

pad is labeled by a black cross. There are totally 6 VDD pads and 8 GND pads used for TX circuit.

The second design consideration is the directions of signal ports. Baseband inputs, 6LO inputs, and RF outputs occupy 3 different directions. Such placement will benefit the PCB design and minimize signal paths.

The third consideration is to increase the testability and tolerance of temperature and process variation. Each block will have its own bias and input common mode voltage control. As a cost, more bias pins are used.

Last but not least, in this design, all the signal transistors are implemented with RF CMOS transistor model. Poly type resistors, Metal-Insulator-Metal (MIM) type capacitor, inductor model with calculation tool are used to further improve design accuracy over process and temperature variation.

The active area of the designed TX is 1.4 mm × 0.5 mm = 0.7 mm^2.

5.2 PCB Design and Chip Connection

5.2.1 PCB Design

The designed transmitter chip is sliced together with a receiver chip which is positioned at the bottom of the transmitter (Figure 47). In order to be compatible with the sliced chip, the PCB is designed for the testing of both the transmitter and the receiver circuit. However, the RX circuit will not be discussed in this thesis.

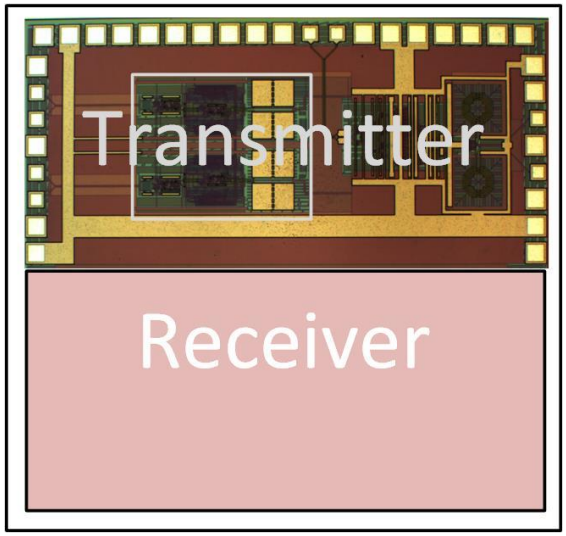


Figure 47. Die micrograph of DUT

The top layer of the designed PCB is shown in Figure 48. It shows the input ports and output ports of TX and RX.

The PCB is fabricated with Rogers 4305 to achieve good frequency performance up to several GHz. The top layer of fabricated PCB with soldering components is shown in Figure 49. DUT and other components are labeled in the figure.

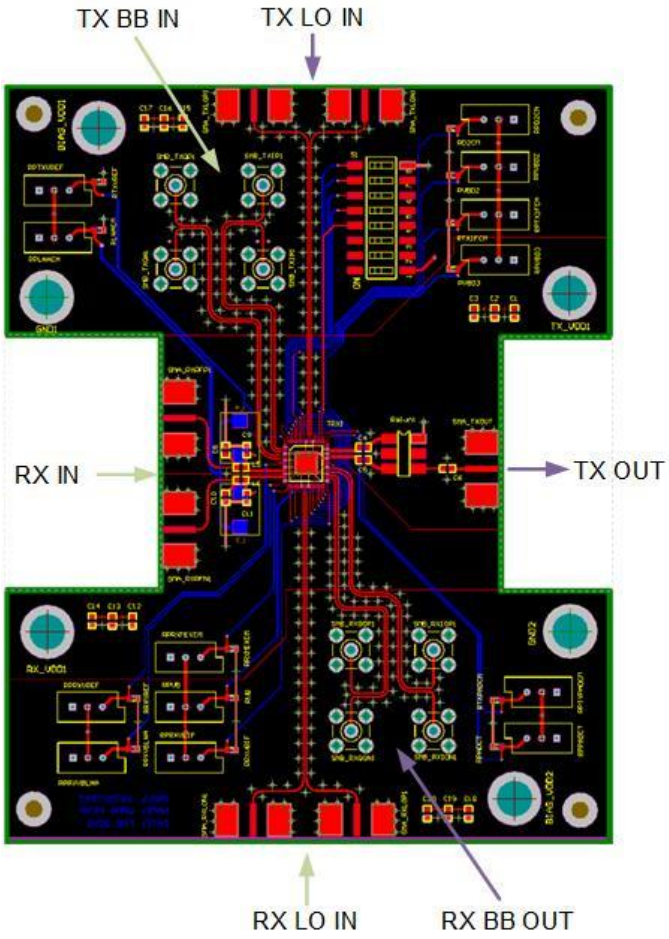


Figure 48. Layout of designed transceiver PCB

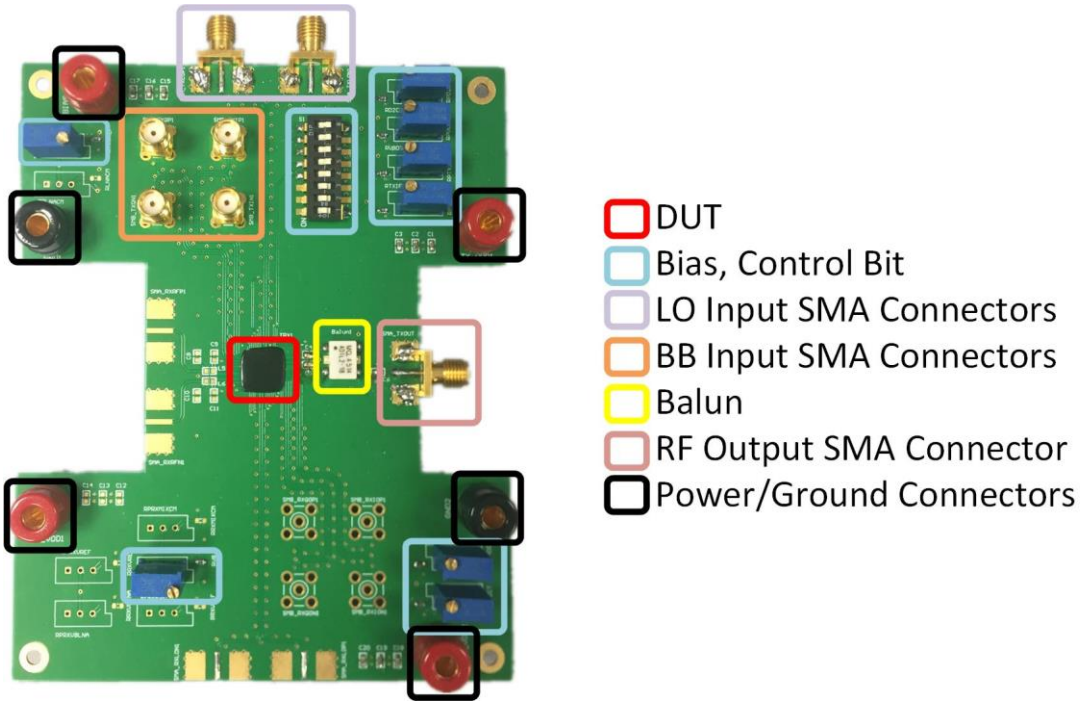


Figure 49. Fabricated PCB with soldering components

There are totally four layers of PCB used in this design, which includes 1 power plane and 1 ground plane as middle layers. The power plane is split into 4 parts to isolate TX and RX VDD nets. The 4 VDD nets include power net for TX, bias net for TX, power net for RX and bias net for RX. The purpose of isolating TX and RX VDD nets is to ease the debugging of testing and minimize the mutual influence. The isolation of power net and bias net is to avoid the possible strong ripple from TX output influencing the bias condition. The 4 VDD inputs are connected with the red colored banana connector shown in Figure 49. The ground nets for both the TX and RX are shared so that there is only one ground plane. Two black banana connectors are used to balance the ground voltage and reduce IR-drop due to the large current.

The DUT is wire-bonded in the middle of the PCB as highlighted with a red square. In order to minimize the high-frequency signal path, i.e. RX input and TX output, a special shape of the PCB is used as shown in Figure 49. The PCB is cut towards the inside in the directions of RX input and TX output. The shorter path used for the high-frequency signal will help minimize the parasitic resistance and mismatch of differential signals.

Two types of SMA connectors are chosen in this design. The horizontal SMA connectors are used for LO input ports and RF output port. Since the frequency is in

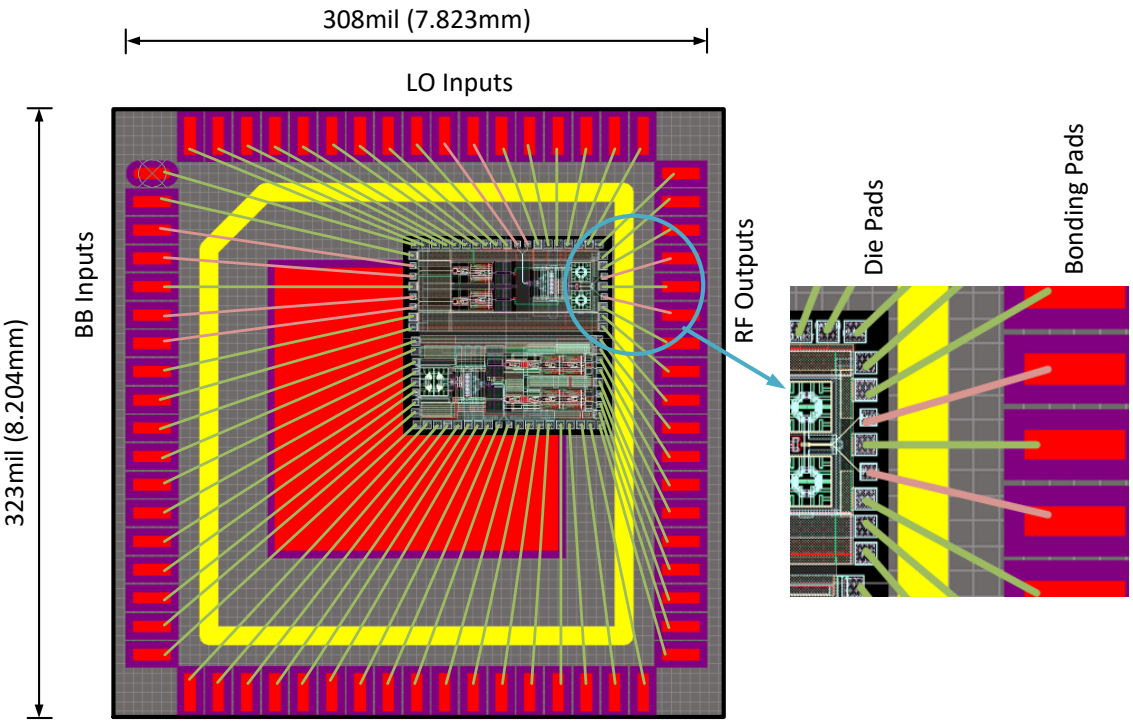
GHz range for these signals, the horizontal SMA connectors generally have better frequency performance. For the baseband inputs, since the signal frequency is below 10 MHz, vertical SMA connectors are used to save board area and minimize signal path from BB input ports to the chip.

Even though the power nets are isolated as mentioned before, several voltage bias controls are shared between TX and RX circuits. The biasing pin is always connected to the gate of the transistor and the gate resistance is normally in MΩ range. The bias voltage will be accurate when testing TX or RX alone.

At the RX input, a matching network is reserved. At the output of TX, a balun is used to convert differential signal into a single-ended signal. The balun used in this design is Mini-circuits ADTL2-18. This product has a frequency range from 30 MHz to 1.8 GHz. The typical insertion loss for the range from 100 MHz to 1.5 GHz is around 1 dB. The impedance ratio of secondary to primary port is 2. If the test equipment has 50 Ω input resistance, this balun will convert it into 100 Ω differential impedance for the designed chip.

5.2.2 Chip Connection and Wire-bonding

As shown in Figure 50, the test chip is wire-bonded on the PCB. The bonding wires connect the die pads and PCB bonding pads directly. To ensure the circuit performance, gold bonding wire (AW-99) with diameter of 20μm (0.8 mils) is used. The surface of bond pad is electroplated with NiPdAu to accommodate gold bonding wire. Take the 2 RF output signals as an example, the bonding wires are labelled in pink color in the zoomed figure (Figure 50(a)). And the die pad pitch is 254 μm (10 mils) for 2 signals and the PCB bond pad pitch is 762 μm (30 mils).



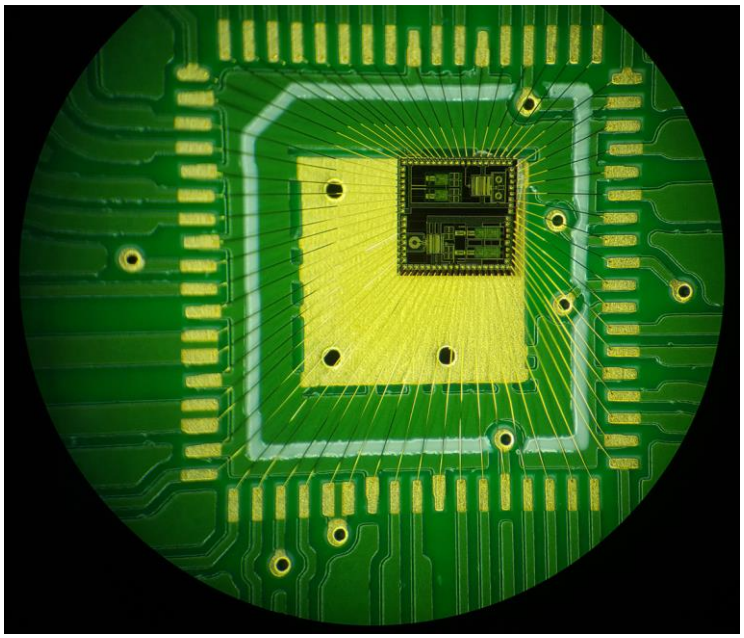


Figure 50. PCB wire-bonding diagram, (a) suggested bonding diagram sent to vender company, (b) actual bonding diagram

The primary concern of wire-bonding is the bonding wire length at RF output ports. The 2 ports are close to each other and the bonding wires may affect transmitter performance. As shown in Figure 51, the bonding wire can be modeled as series inductor and mutual capacitor. In order to minimize the effect of bonding wire and

benefit transmitter testing, the die is placed close to RF output bond pads on the right side as shown in Figure 50 (a). The microscope view of actual bonding is shown in Figure 50 (b).

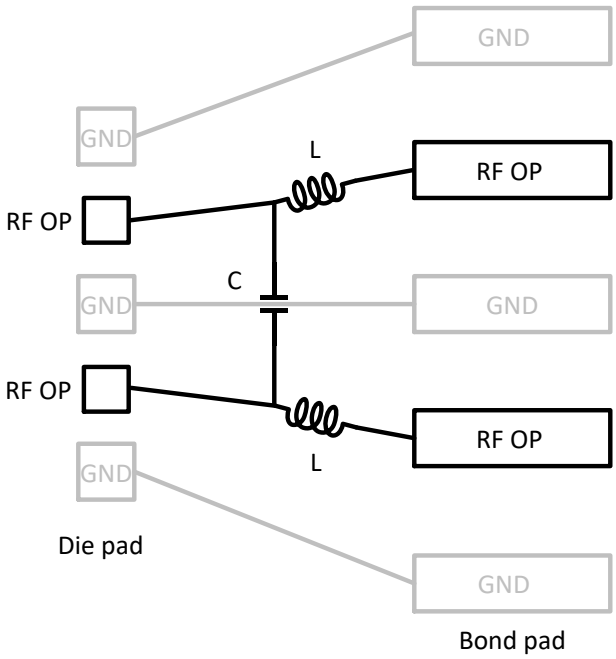


Figure 51. Modeling of bonding wires

The less important concern of bonding wire effect is at LO and BB input ports. Since the LO signal is driven by external equipment and the bonding wire length difference is very small, the effect is minimized. For BB input ports, the BB signal is at low frequency, thus the bonding wire will also have minor influence on these ports.

5.3 Simulation and Measurement Results

5.3.1 TX Output Matching

The RF output will be connected to a spectrum analyzer which has an input impedance of 50 Ω. Therefore the output matching should be done before testing of TX output spectrum. To perform the testing, the output RF port is connected to a vector network analyzer (VNA). The measurement setup is shown in Figure 52. The model of VNA used is Rohde&Schwarz ZVA 67.

The first step of testing is calibration. This is due to the non-ideality of SMA adaptor and cable loss. The SMA connectors used on the PCB and cable have a diameter of 3.5 mm and the SMA connector of equipment is 1.8 mm. Thus an adaptor is used to

convert the diameters of connectors. The SMA cable is not ideal which has a loss smaller than 1 dB. The calibration can optimize the cable and SMA adaptor. 2 port calibration is programmed and 2 ports of equipment are calibrated. For the testing of S22, only one port is needed. The second step of testing is turning the power on and bias the circuit at the correct bias condition. For simplicity, the DC supply is not shown in Figure 52.

The measurement result is taken down which is shown in Figure 53. It is shown that S22 is below -10 dB from 770 MHz to 1.16 GHz. The minimum output reflection is near 1 GHz which has an S22 smaller than -22 dB. The measured S22 is slightly worse than that in the simulation result of output stage S22 in Chapter 6. The difference can be the cause of process and temperature variation, bonding wire effect, parasitic effect of the chip and testing PCB board.

For the LTE, the sub-GHz uplink operating band bands includes band 5 (824 MHz – 849 MHz), band 8 (880 MHz – 915 MHz), band 12 (698 MHz – 716 MHz), band 13 (777 MHz – 787 MHz), band 14 (788 MHz 798 MHz), band 18 (815 MHz – 830 MHz), band 19 (830 MHz – 845 MHz) and band 20 (832 MHz – 862 MHz) [8]. For the S22 that is below -10 dB, the frequency range can cover band 5, 8, 13, 14, 18, 19 and 20, from 777 MHz to 915 MHz. This frequency range has been highlighted in the yellow color shown in Figure 53. Besides, the testing of transmitter performance will not be limited in this frequency range, it will be tested in all the operating frequency as explained in following sections.

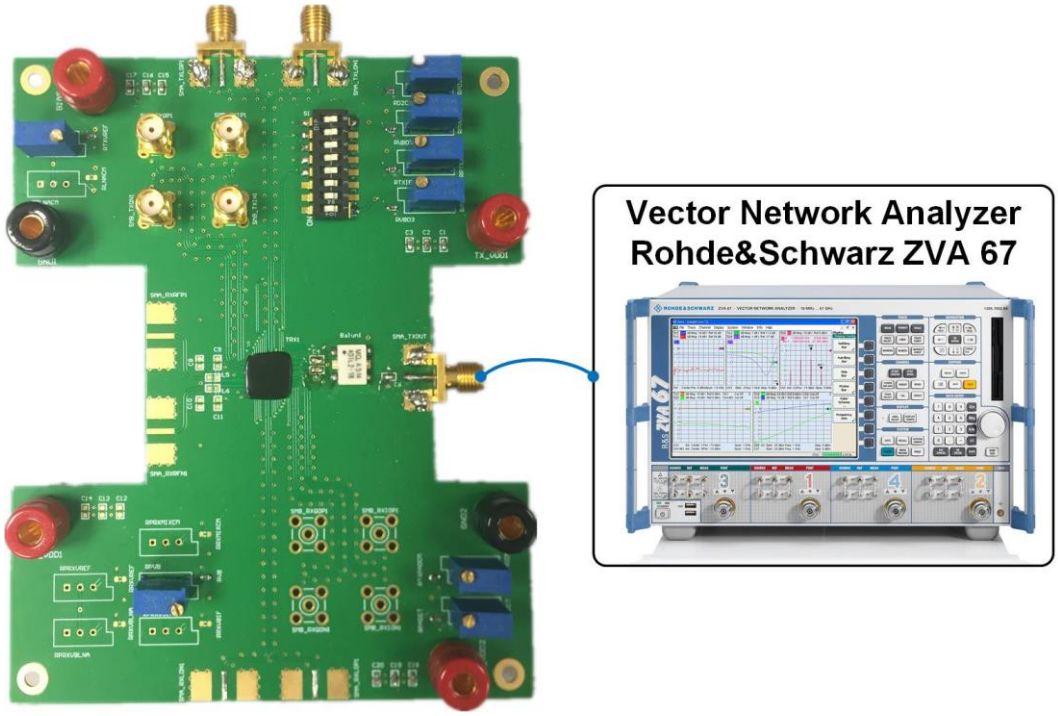


Figure 52. Equipment setup for testing TX output matching

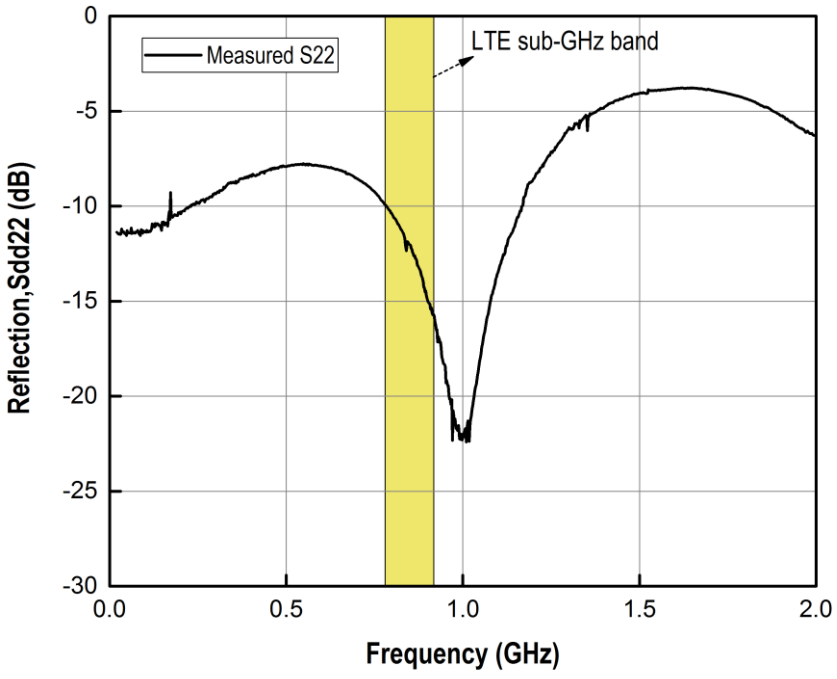


Figure 53. Measurement result of S22

5.3.2 TX RF Output Spectrum

The equipment setup for transmitter RF output spectrum is shown in Figure 54. The DC supply for PCB board is not shown in the figure for simplicity. The LO signal is generated by a signal generator which is Agilent N5183A. The first testing LO frequency used for the transmitter is 782 MHz (band 13). The signal frequency is calculated by:

$$6LO = LO \times 6 = 782\ MHz \times 6 = 4.692\ GHz$$

And the signal power is set at 0 dBm. The LO signal passes through an off-chip balun (SigaTek SH15555) to generate a differential LO signal. The balun has an input operating frequency range from 2 GHz to 12 GHz and a loss of -3 dB when converting the single-ended signal to differential signal. After the on-chip divide-by-6 circuit, the testing range limited by the balun for the transmitter is from 334 MHz to 2 GHz.

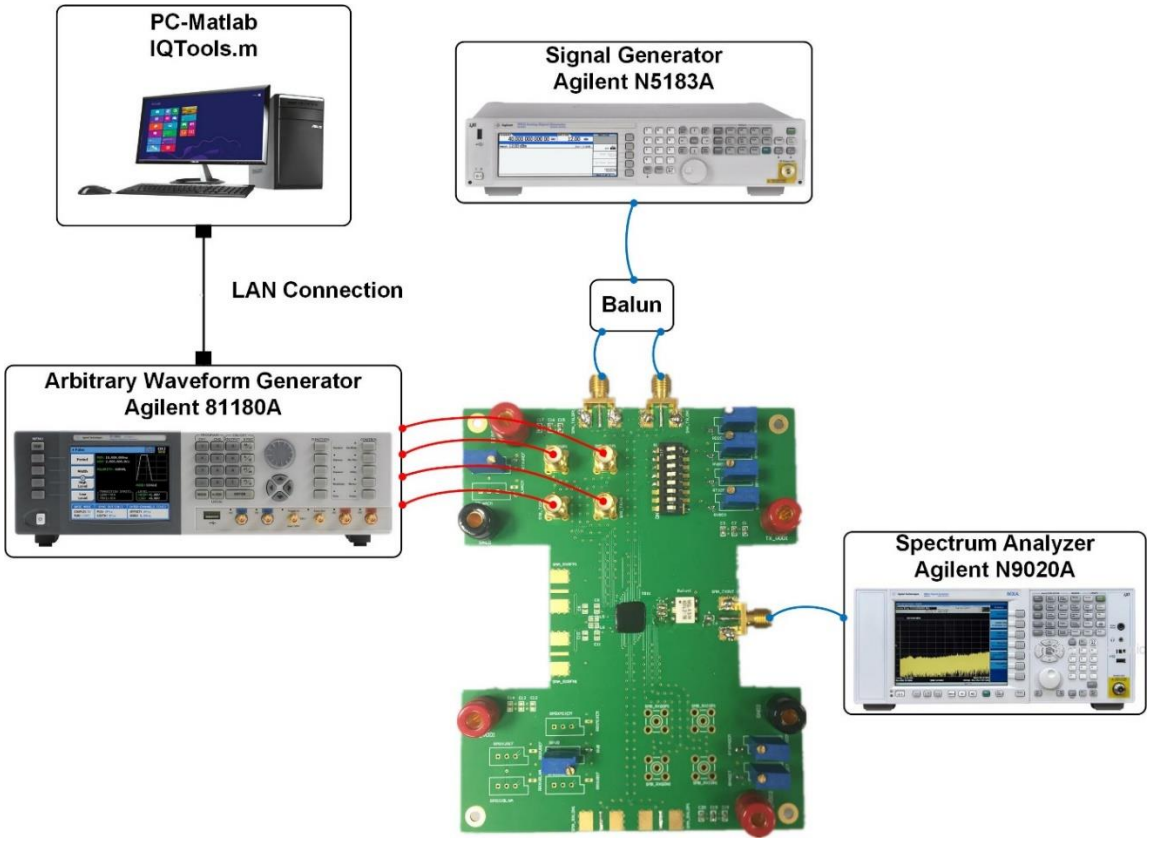


Figure 54. Equipment setup for testing transmitter output spectrum

The baseband input signal port is connected to an arbitrary waveform generator (AWG), Agilent 81180A. Four ports of the equipment are used to generate baseband differential I/Q signals. The AWG is controlled through LAN connection by a Matlab

program on PC. The program used is iqtools.m which is an open source Matlab program. As shown in Figure 55, the signal amplitude and DC offset can be controlled in the program. The multi-tone test is selected as shown in Figure 56. The number of tones and signal frequency can be selected in this interface. The single-tone test with signal frequency 3.5 MHz is set for the testing of the spectrum.

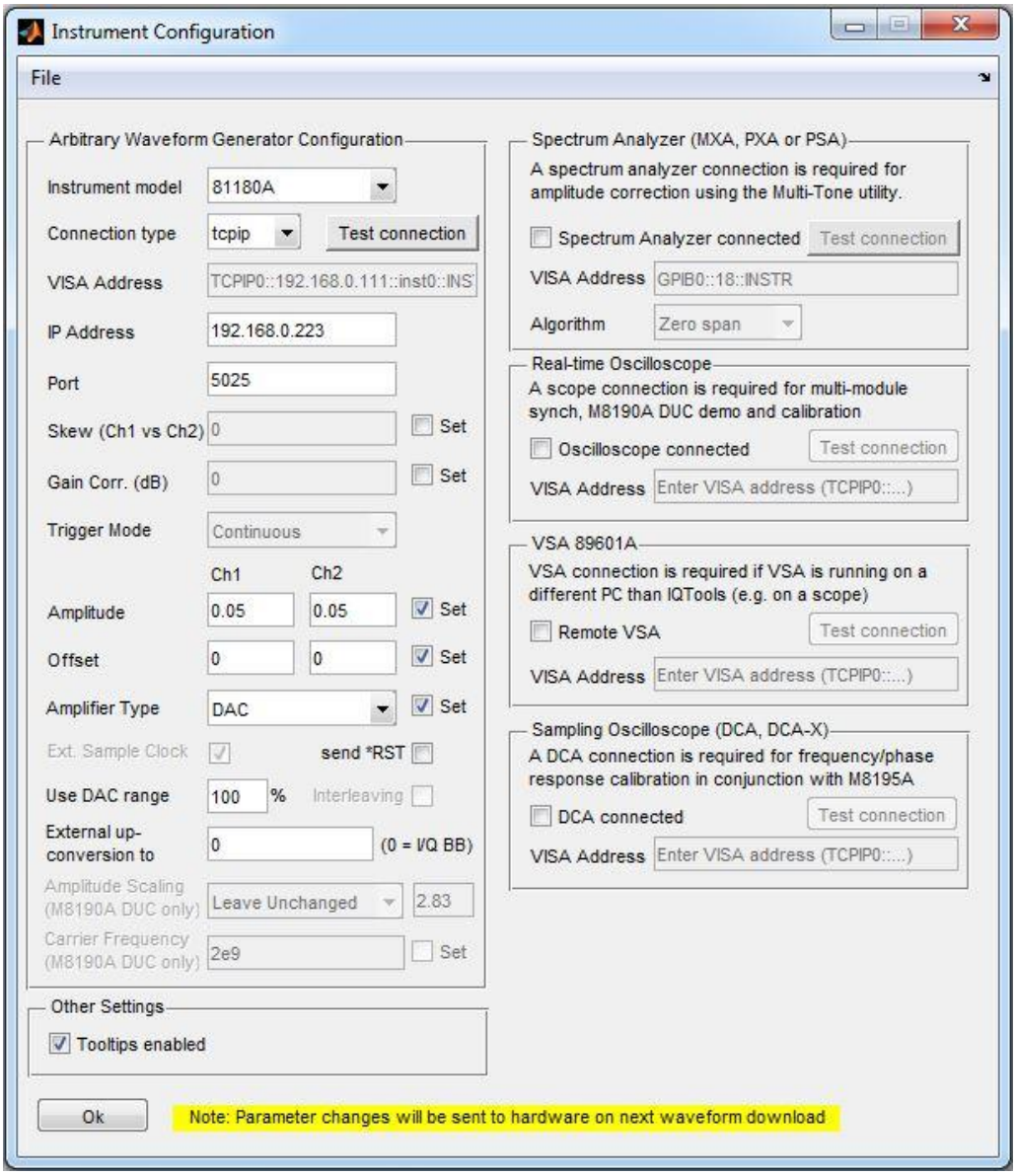


Figure 55. Instrument configuration of Matlab iqtools.m

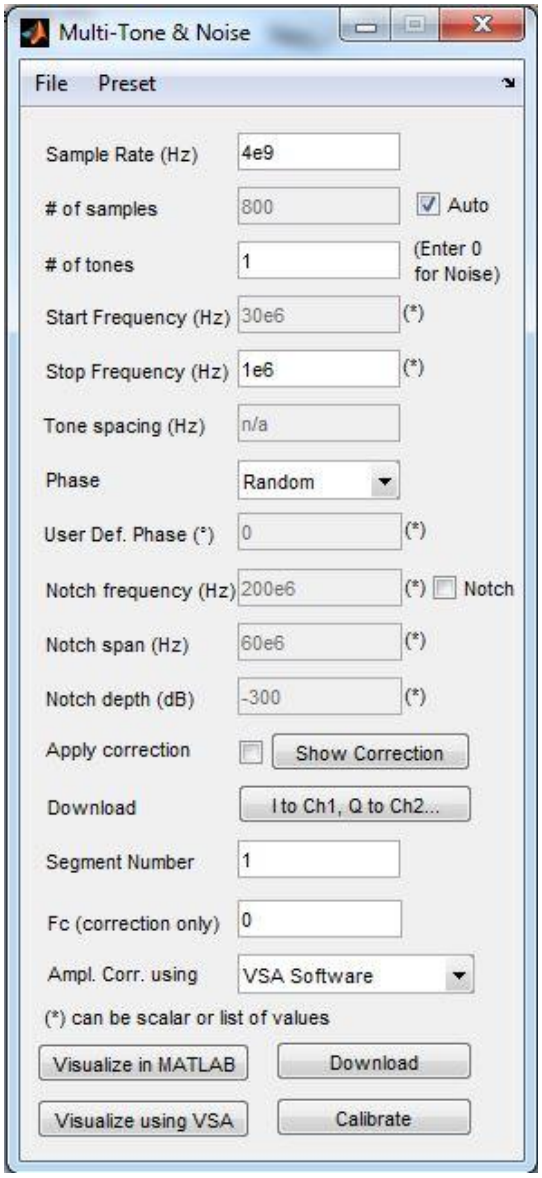


Figure 56. Single-tone setting of Matlab iqtools.m

The output port is connected to a spectrum analyzer (Agilent N9020A). The cable used is individually tested and verified to find it has a loss of 0.6 dB. The loss will be added in the final testing result together with the loss of the off-chip balun used on the PCB.

The spectrum result for LO frequency of 782 MHz and BB frequency of 3.5 MHz is shown in Figure 57 and Figure 58. The input baseband amplitude is chosen at 100 mV_{PP} for both I and Q channels. In Figure 57, the frequency is centered at 782 MHz and has a span of 35 MHz. The measurement result shows that the output power located at LO + BB is -8.6 dBm without compensation of cable and balun loss. The CIM3, image, LO leakage and CIM5 located at LO – 3BB, LO – BB, LO, LO + 5BB are -62.9 dBc, -27 dBc, -21.5 dBc and -65.1 dBc.

The other phenomenon shown in the spectrum is there is a notch located near LO frequency. This is due to the inserted DC coupling capacitor between baseband circuit and mixer elements. Since the baseband circuit and RF-front end circuit are designed separately, the output voltage of baseband circuit is designed at 0.9 V which is different from mixer input common mode voltage that is 1.1 V. Therefore, the inserted capacitor is necessary to individually bias the mixer input common mode voltage. However, at the baseband frequency, the capacitor, the on-chip bias resistors, and the off-chip bias resistors form a high pass filter (HPF) as shown in Figure 59. The spectrum due to this HPF will reject the baseband frequency close to DC and the mixers in the RF front-end circuit will upconvert this spectrum to the frequency at LO. Together with the LO leakage coming from RF front-end circuit, the final spectrum near LO thus behaves as shown in Figure 57.

The other important parameter is 3LO component which is located at 3LO – BB. As shown in Figure 58, 3LO – BB is located at:

$$3LO - BB = 3 \times 782\ MHz - 3.5\ MHz = 2.3425\ GHz$$

The power of this spurious tone is -50.4 dBm which is -41.8 dBc compared with wanted signal at LO + BB. If there is a power amplifier after the PA driver, this component will further mix with wanted signal LO + BB to generate CIM product at LO – 3BB at the RF output.

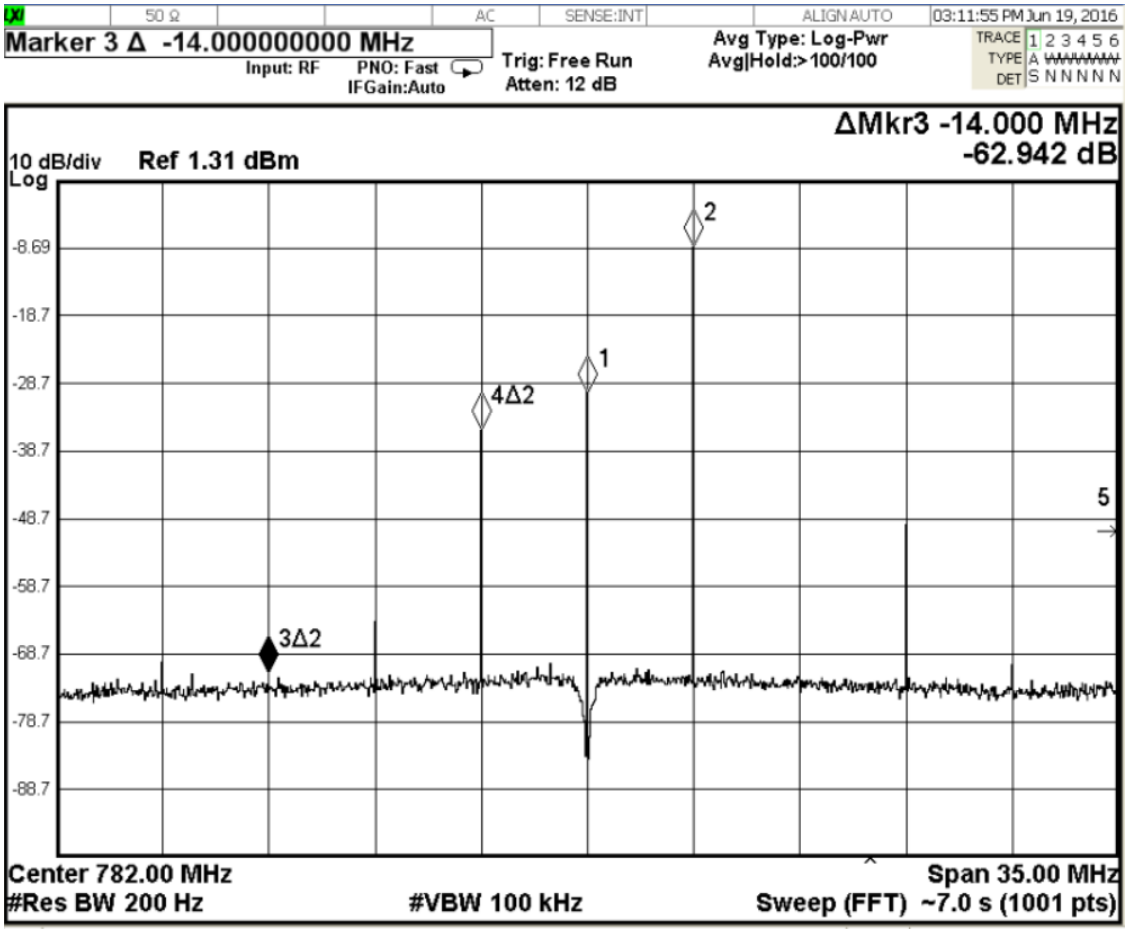


Figure 57. Measurement result of transmitter output spectrum near LO

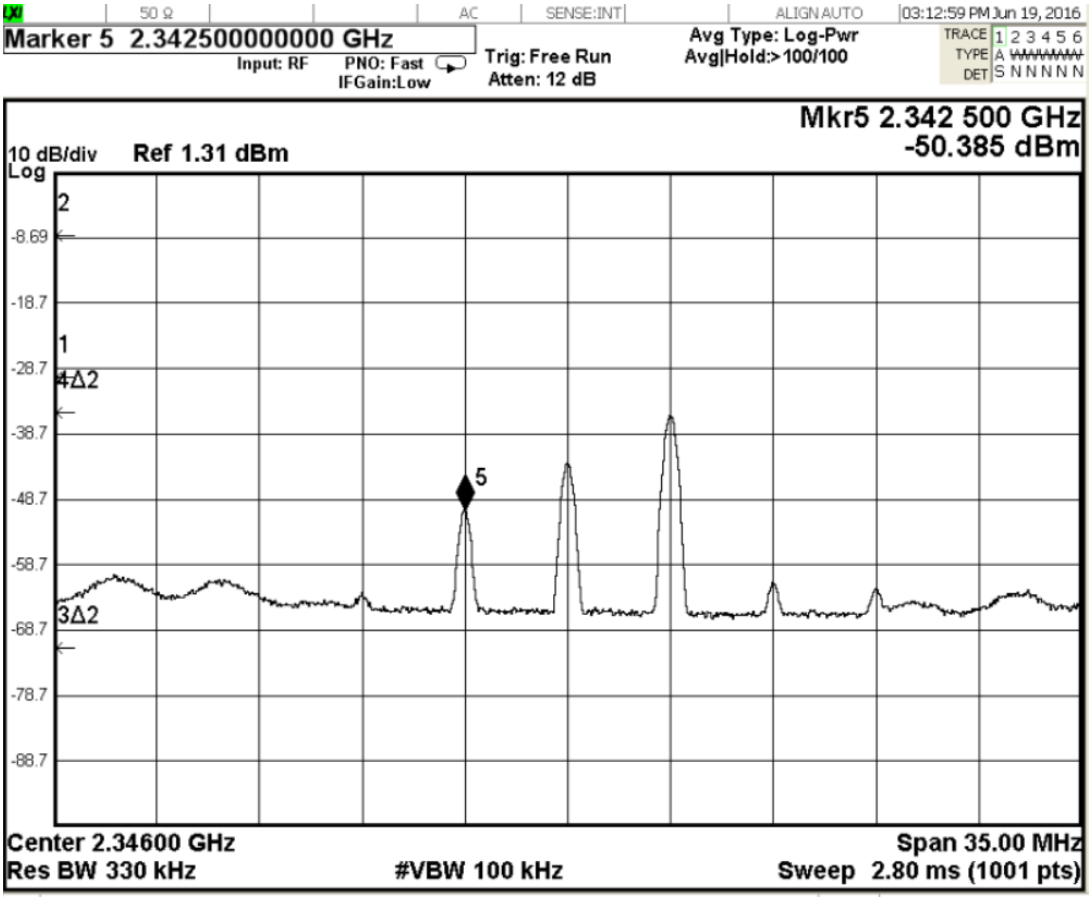


Figure 58. Measurement result of transmitter output spectrum near 3LO

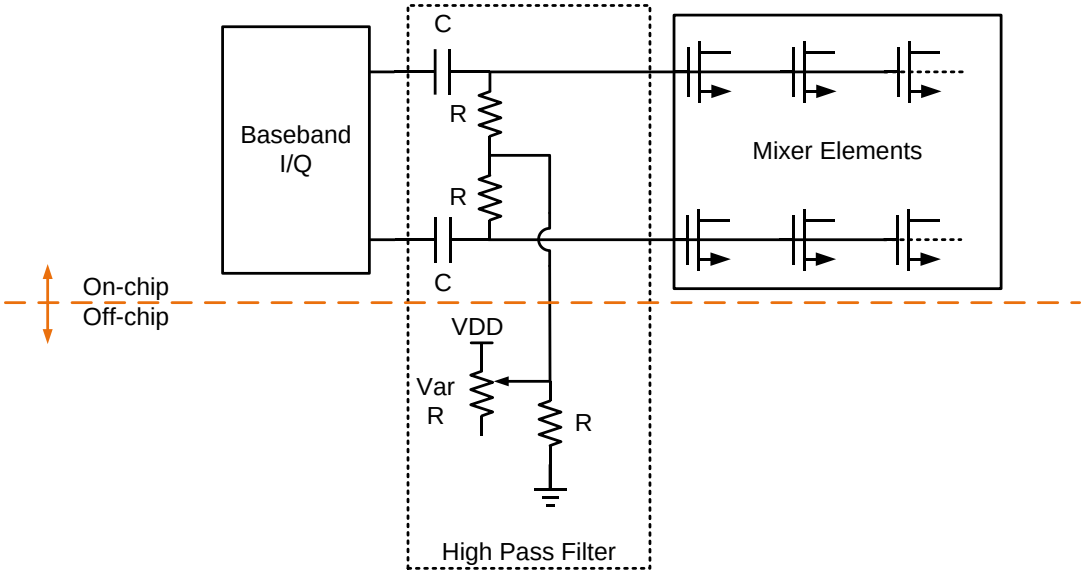


Figure 59. Circuit diagram showing consequence due to inserted capacitor

5.3.3 TX Performance vs Baseband Swing

The testing equipment setup for the testing of TX performance with respect to baseband swing is same as the Figure 54. The selected LO frequency is 782 MHz. For

the baseband signal, the single-tone test is firstly chosen. The baseband frequency is set at 1 MHz. According to the data sheet of output off-chip balun, it has an insertion loss of 0.8 dB. Together with the cable loss of 0.6 dB, 1.4 dB will be added for the final testing result. In the rest part of this thesis, 1.4 dB compensation is added to the signal spectrum if there is no further explanation.

Figure 60 shows the transmitter gain versus baseband swing. The baseband swing is single-channel differential peak-to-peak voltage. The differential voltage is 100 mV and source resistance is 50 Ω. The input power is calculated by:

$$10\log\left(\frac{(0.05V)^2}{2\ \times 50\Omega}\times 1000\right) = -16.02\ dBm$$

Since the single-side band modulation is applied, the total gain is calculated by:

$$Gain = \ Output\ Power - Input\ Power - 3\ dB$$

It shows that when the input swing is 0.1 V, the gain is 11 dB. As the baseband swing increases, the gain decreases gradually and passes the 1 dB compression point.

Figure 61 shows the output 1 dB compression point (O1dB). When the input swing is 185 $mV_{PP,diff}$, the O1dB is -0.7 dBm.

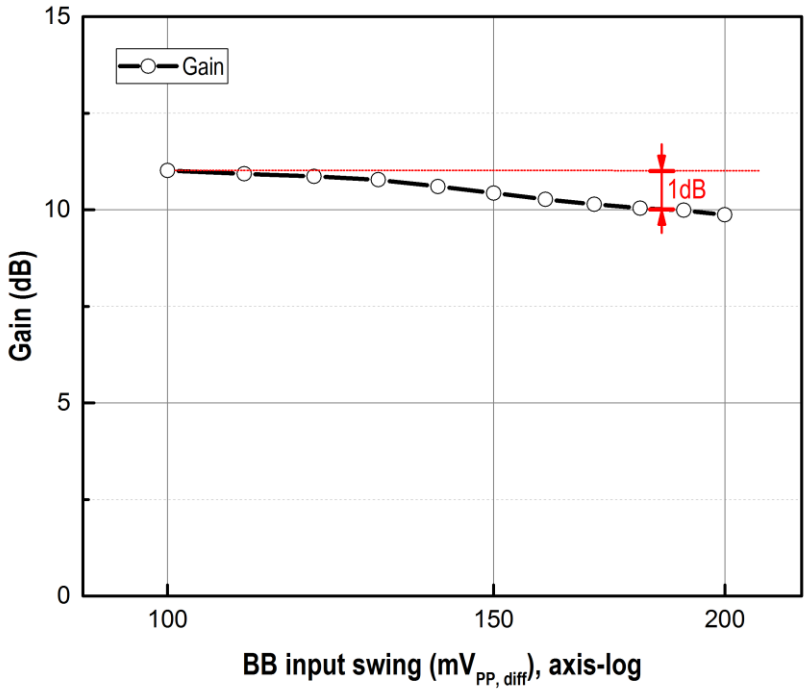


Figure 60. Measurement results of transmitter gain vs BB input swing

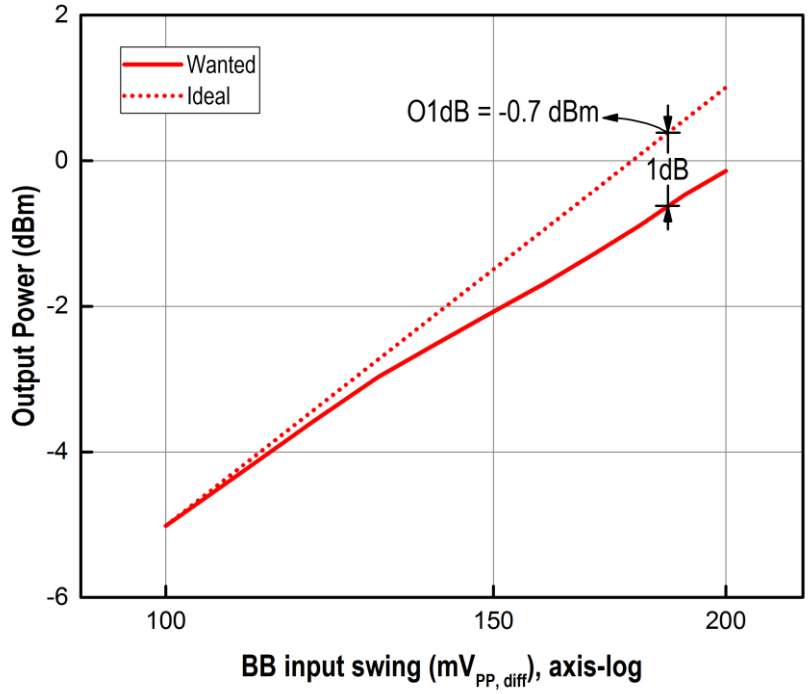


Figure 61. Measurement result of transmitter output 1 dB compression point

The equipment setup for the measurement of OIP3 is same as the one of O1dB measurement. The Matlab setup is slightly different in the multi-tone test interface. The two-tone test is selected with the first tone at 1 MHz and second tone at 1.1 MHz (Figure 62). The output wanted signal and IM3 are plotted in Figure 63. The result shows that the output 3rd-order intercept point (OIP3) is measured at 8.3 dBm.

To justify this measurement result, the difference between the OIP3 and O1dB is calculated by:

$$OIP3 - O1dB = 8.3 - (-0.7) = 9\ dB$$

This result is close to the ideal difference between OIP3 and O1dB, i.e. 9.6 dB [13].

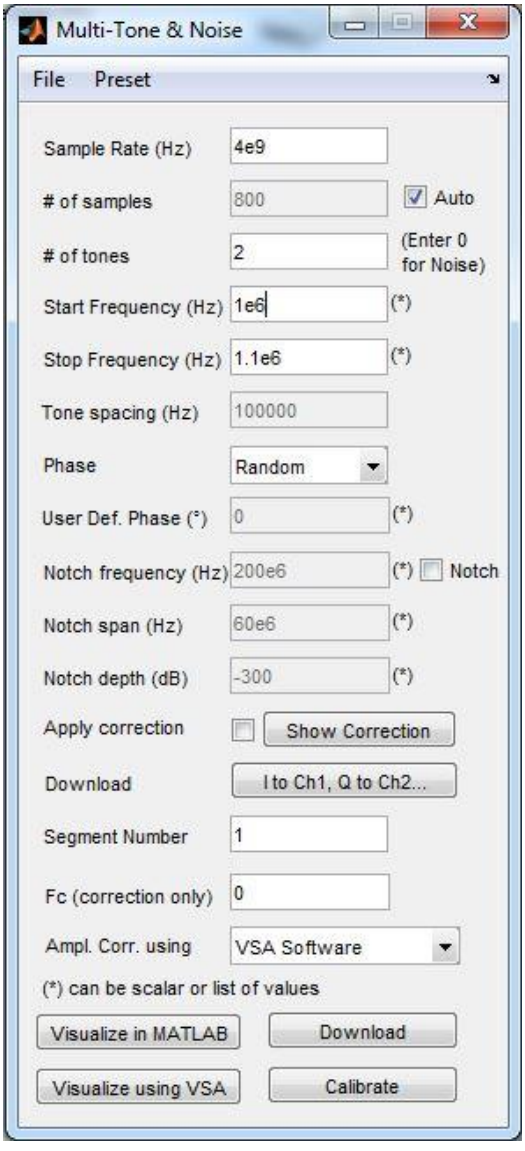


Figure 62. Multi-tone setting of Matlab iqtools.m

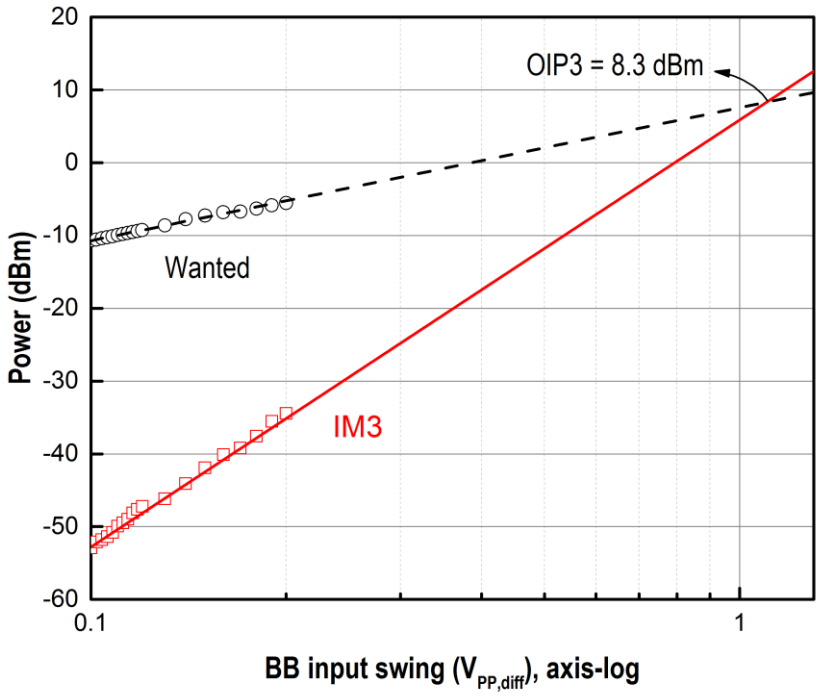


Figure 63. Measurement result of transmitter output 3rd-order intercept point

Apart from the gain, O1dB, and OIP3, other transmitter quality parameters such as CIM products, image, LO leakage and 3LO component versus baseband input swing are also measured and plotted. The test methodology and measurement setup is same as spectrum measurement in Section 5.3.2. The baseband input voltage is increased gradually and the output spectrum is recorded and plotted.

Figure 64 shows the measurement results of the CIM products including CIM3 and CIM5 located at LO – 3BB and LO + 5BB respectively. Wanted output signal located at LO + BB is plotted for reference. The signal power is in dBm as shown in the left y-axis. CIM3 and CIM5 products are plotted with reference to wanted signal and the unit is dBc as shown in the right y-axis. It is shown in the figure that as the input baseband swing increases from 100 $mV_{PP.diff}$ to 200 $mV_{PP,\ diff}$, the output power is gradually approaching 1 dB compression point. CIM3 is slightly increased from -64 dBc to -60 dBc as input increases. And CIM5 is slightly increased in the range from -60 dBc to -50 dBc as input signal power approaches 1 dB compression point.

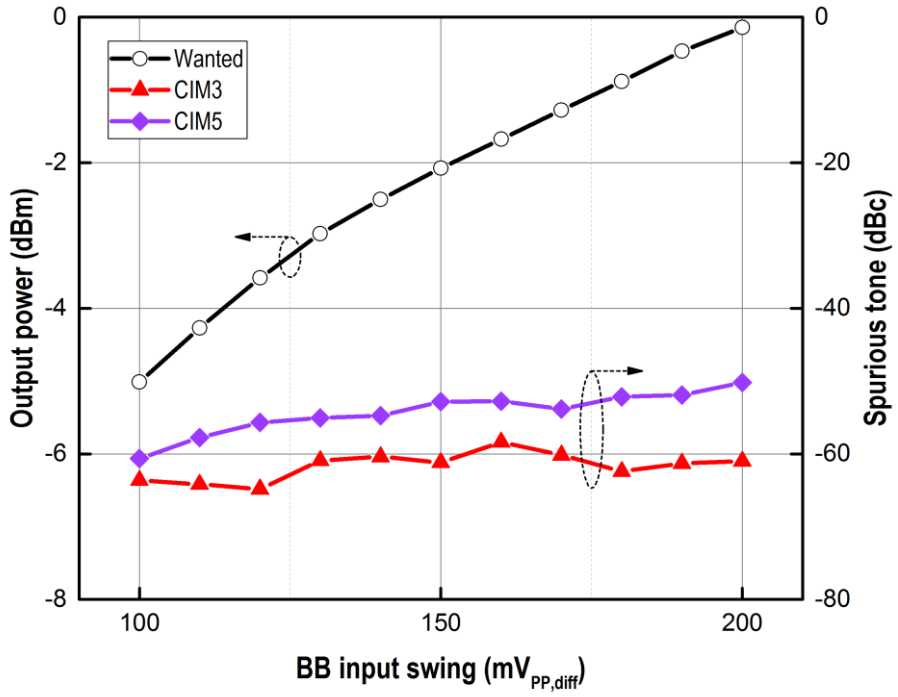


Figure 64. Measurement results of CIM products vs BB input swing

Figure 65 shows the measurement result of the image and the LO leakage. It shows that the LO leakage is relatively independent of input/output power. The image is in the range from -25 dBc to -34 dBc. There is no obvious dependence between the image and input/output signal power.

Figure 66 shows the measurement result of the 3LO component at 3LO – BB. As the output increases from -5 dBm to 0 dBm, the 3LO – BB is decreased from -46 dBc to -54 dBc. This means that when the wanted signal approaches 1 dB compression point, the absolute value of 3LO component is decreased by 3 dB. This measurement result indicates that the power of 3LO component is relative independent of the input/output power when the wanted signal approaching 1 dB compression.

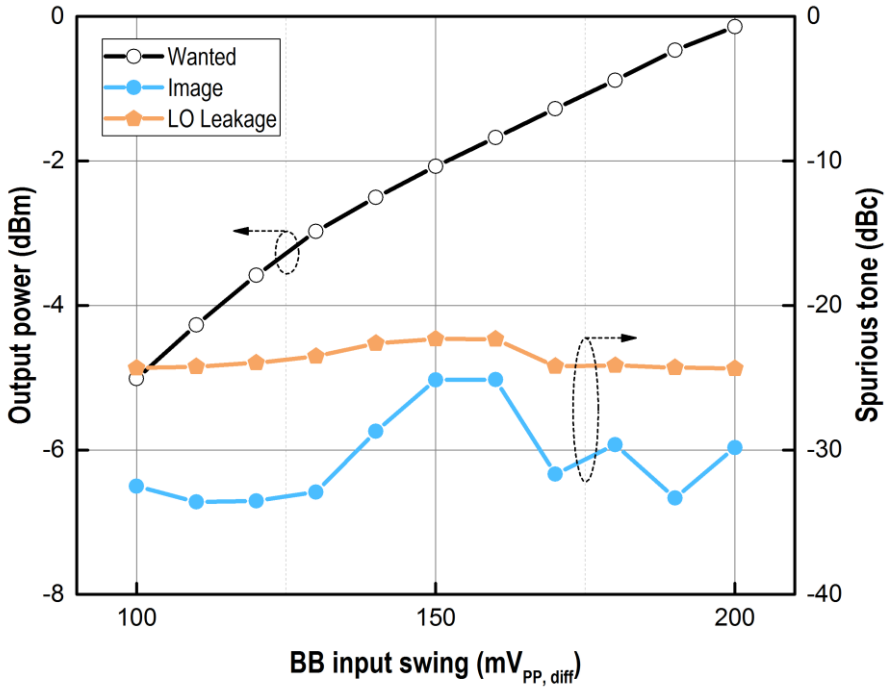


Figure 65. Measurement results of image and LO leakage vs BB input swing

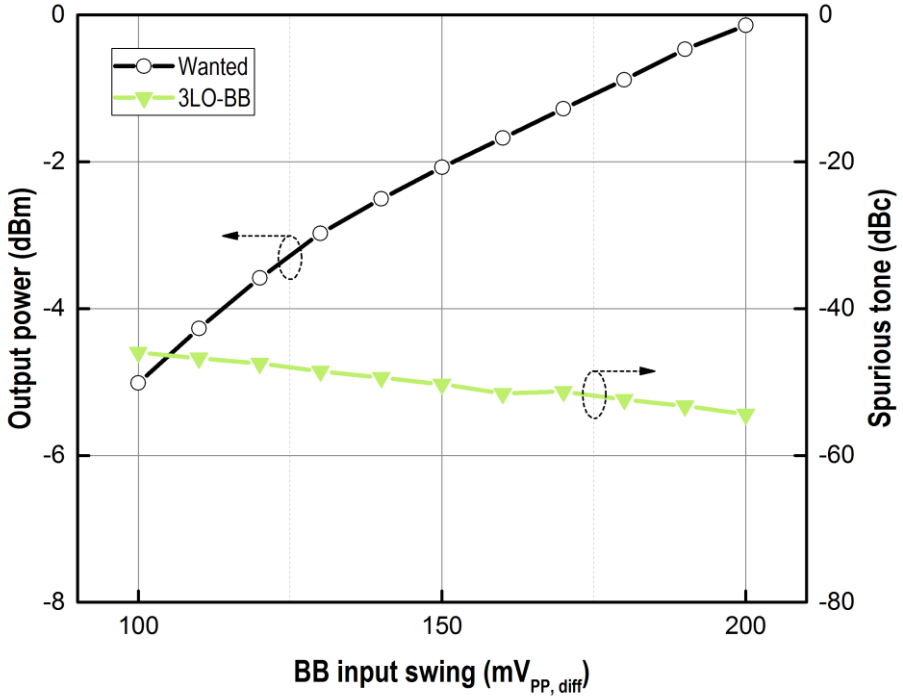


Figure 66. Measurement results of 3LO component vs BB input swing

5.3.4 TX Performance vs LO Frequency

The frequency response of the designed transmitter is also measured. The equipment setup is same as the measurement of the output spectrum. The baseband frequency and amplitude are 1 MHz and 100 $mV_{PP,diff}$. Due to the operating frequency range (2 GHz to 12 GHz) of off-chip balun used for LO signal, the minimum testing frequency for the transmitter should be larger than 2G ÷ 6 = 333 MHz. Thus 350 MHz is chosen for minimum testing frequency and it is increased by 50 MHz each step until -3 dB point is reached.

Figure 67 shows the schematic simulation result and measurement result of transmitter power gain. The simulation result shows that the transmitter has a gain of 11.5 dB to 12.3 dB in the frequency range from 350 MHz to 2 GHz. The peak frequency is around 1.1 GHz. For the measurement result, the transmitter is only testable up to 1.4 GHz. Due to the parasitic resistance and capacitance, the divide-by-6 circuit reaches its maximum operating frequency with 0 dBm LO signal and -3 dB off-chip balun loss. The divider is able to work when increasing the LO input power but it is not necessary. The transmitter gain increases gradually and reaches its maximum gain at 1 GHz. The -3 dB point is around 1.35 GHz. The maximum gain is located at 1 GHz which is because the reflection of the transmitter is minimum at 1 GHz as shown in Section 5.3.1. This result is coincident with the measurement result of S22 testing.

CIM products measurement are shown in Figure 68. It is shown that CIM3 is in the range from -64 dBc to -60 dBc and CIM5 is in the range from -67 dBc to -55 dBc.

Image and LO leakage with respect to LO frequency are shown in Figure 69. LO leakage is measured around -25 dBc and image is measured in the range from -34 dBc to -25 dBc for the frequency from 350 MHz to 1.4 GHz. In the LTE sub-GHz bands, LO leakage is -24 dBc and image is -34 dBc to -32 dBc.

3LO component is measured and the testing result is shown in Figure 70. The measurement result shows a decreasing tendency of this spurious tone when the testing frequency increases. In the LTE sub-GHz bands, 3LO component is in the range from -51 dBc to -43 dBc.

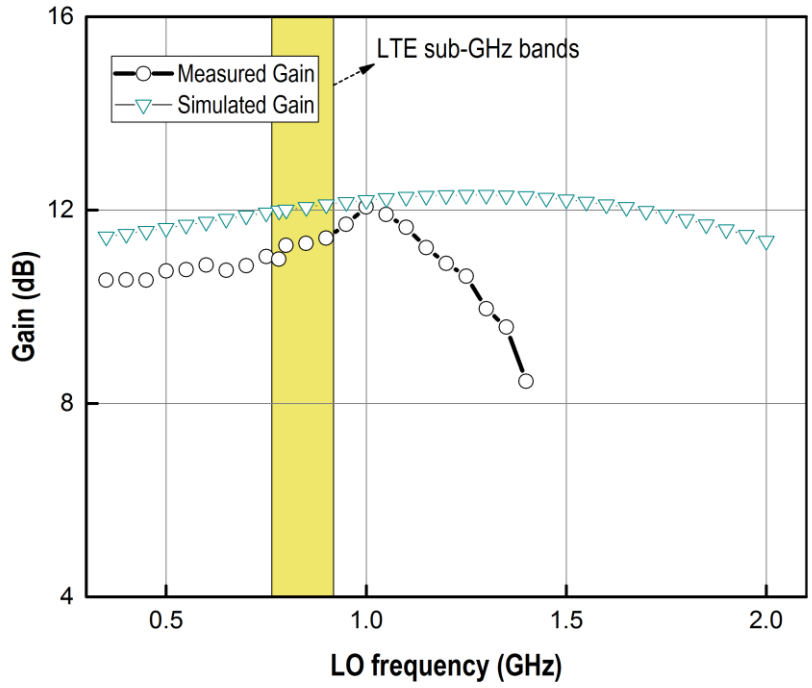


Figure 67. Measurement and simulation results of gain vs LO frequency

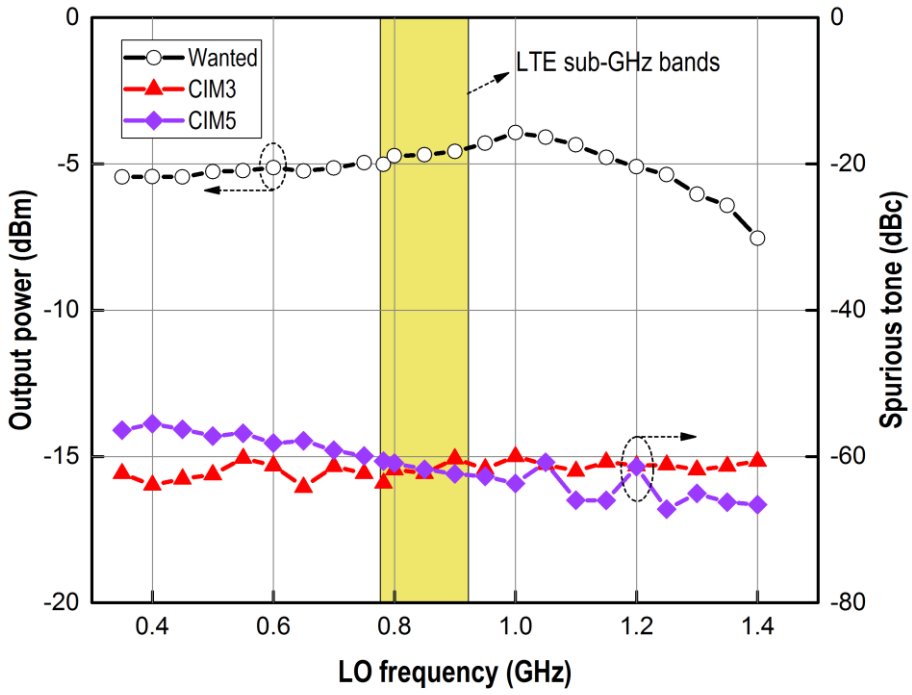


Figure 68. Measurement results of CIM products vs LO frequency

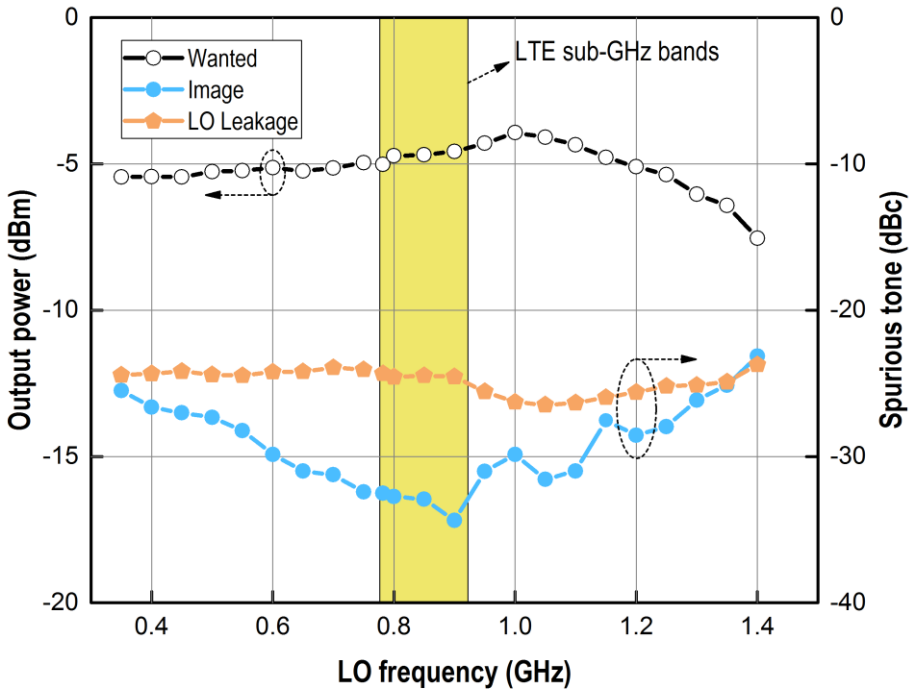


Figure 69. Measurement results of image and LO leakage vs LO frequency

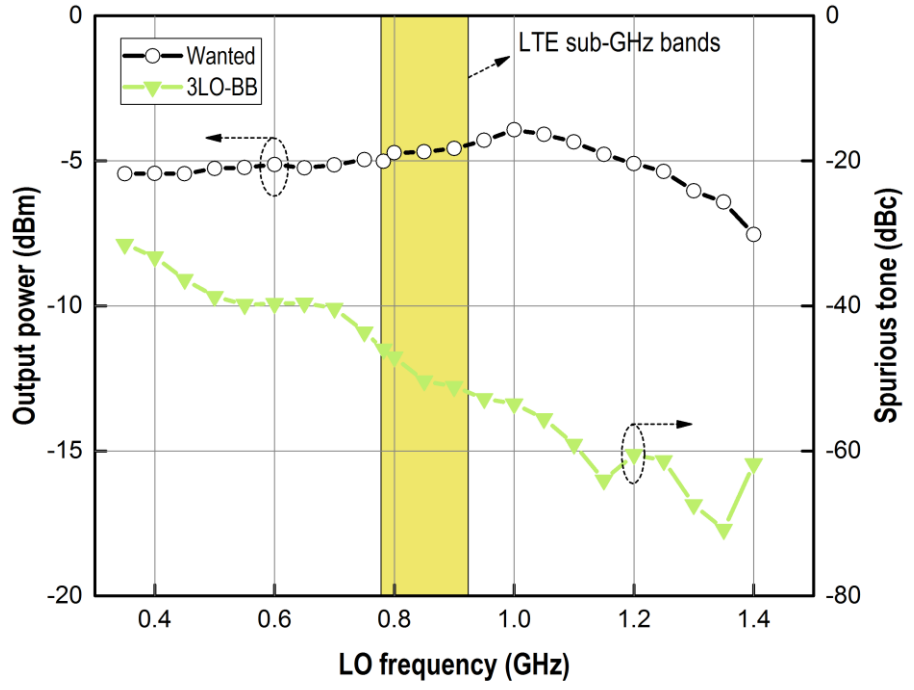


Figure 70. Measurement results of 3LO component vs LO frequency

5.3.5 TX Performance vs Baseband Frequency

Transmitter response with respect to baseband frequency is tested with the same setup as output spectrum testing. LO frequency of 782 MHz is chosen and baseband frequency is variable. The measurement result is recorded and plotted in the following figures.

Figure 71 shows the gain of the transmitter which has a maximum gain of 11 dB around 1 MHz. The gain decrease as with the increment of baseband frequency. -3 dB point is reached at baseband frequency of 4 MHz. The testing result is smaller than post simulated result of baseband bandwidth which is 5.6 MHz. Another observation is the transmitter gain is decreased as the baseband frequency approaches 0 Hz. The reason is explained in the Section 5.3.2, which is due to the inserted DC coupling capacitor between baseband circuit and RF front-end circuit. This issue can be resolved by making the level of the output voltage of baseband circuit and input common mode voltage of mixers same. Thus the capacitor can be removed. The mixers should be redesigned to meet this requirement.

CIM result is plotted in Figure 72 with wanted signal power as a reference. It is shown that CIM3 and CIM5 are over -60 dBc and -58 dBc respectively when baseband frequency is equal and larger than 0.3 MHz. CIM degrades below 0.3 MHz due to the decreasing of wanted signal power at LO + BB.

Image and LO leakage performance are shown in Figure 73. LO leakage is measured in the range from -22 dBc to 28 dBc. Image is from -25 dBc to -36 dBc.

3LO component is shown in Figure 74. It is from -46 dBc to -41 dBc.

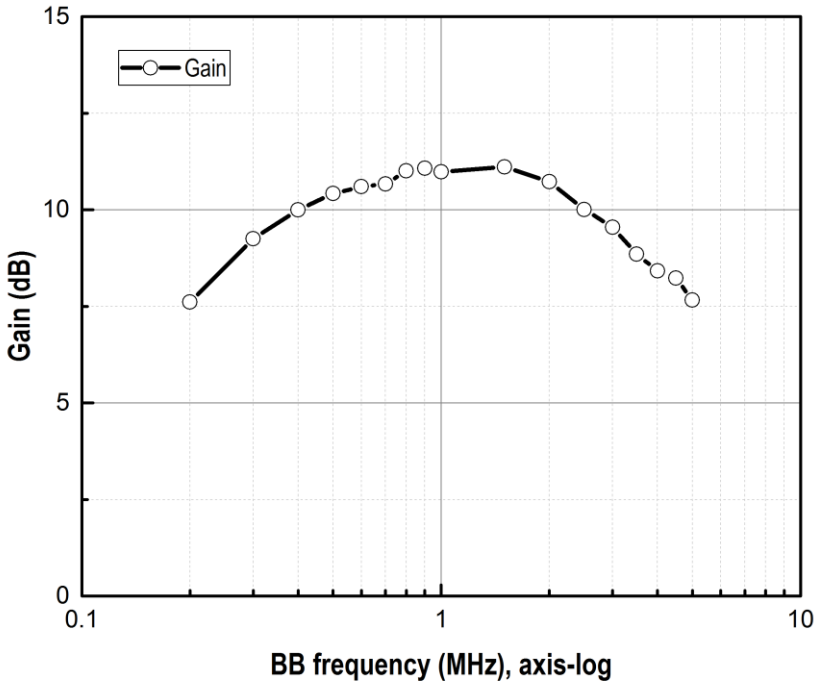


Figure 71. Measurement results of gain vs BB frequency

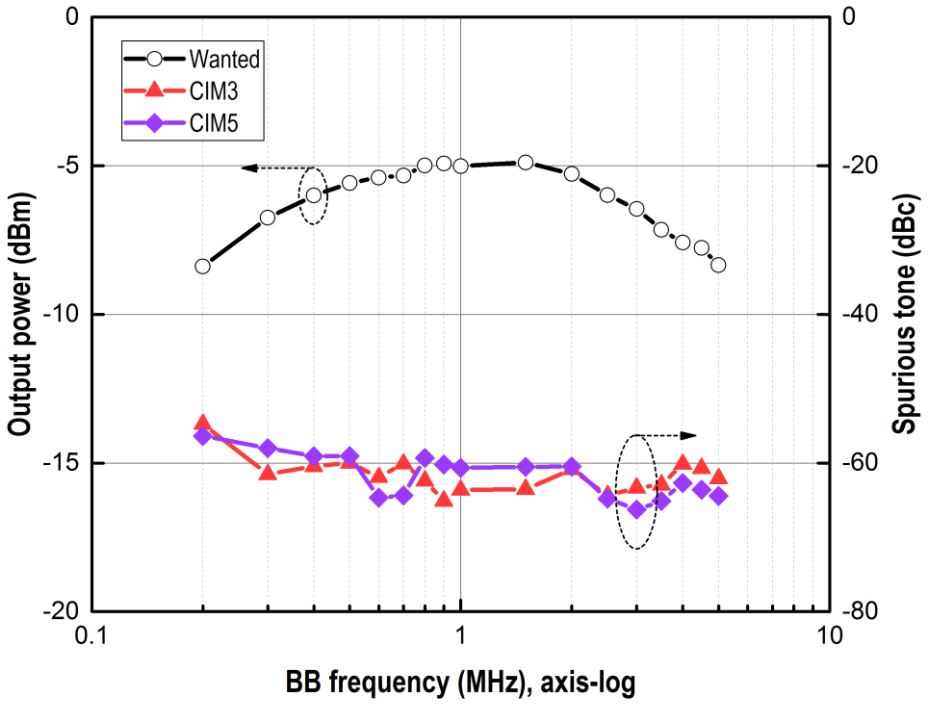


Figure 72. Measurement results of CIM products vs BB frequency

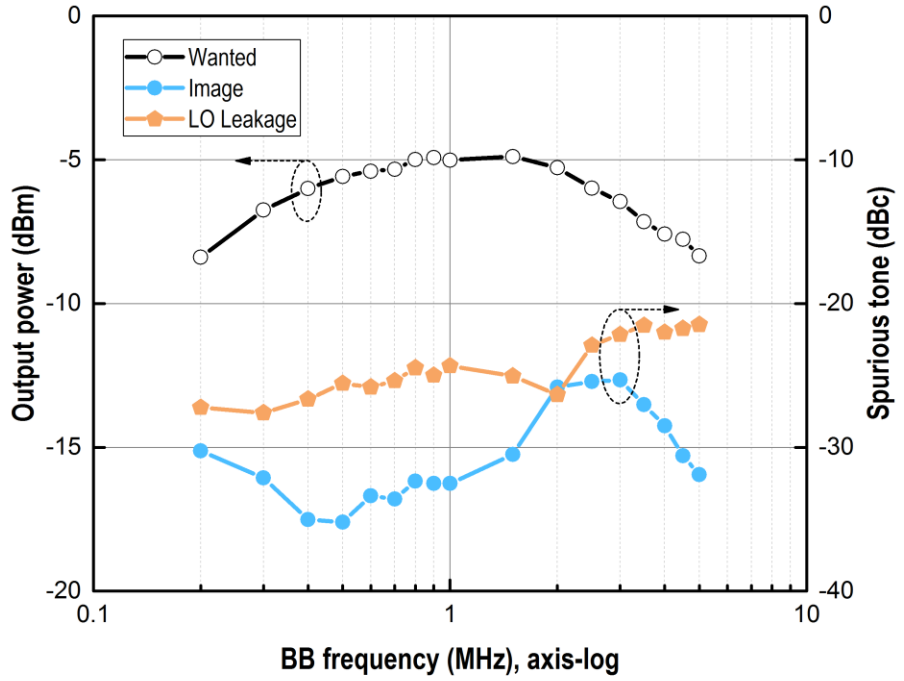


Figure 73. Measurement results of image and LO leakage vs BB frequency

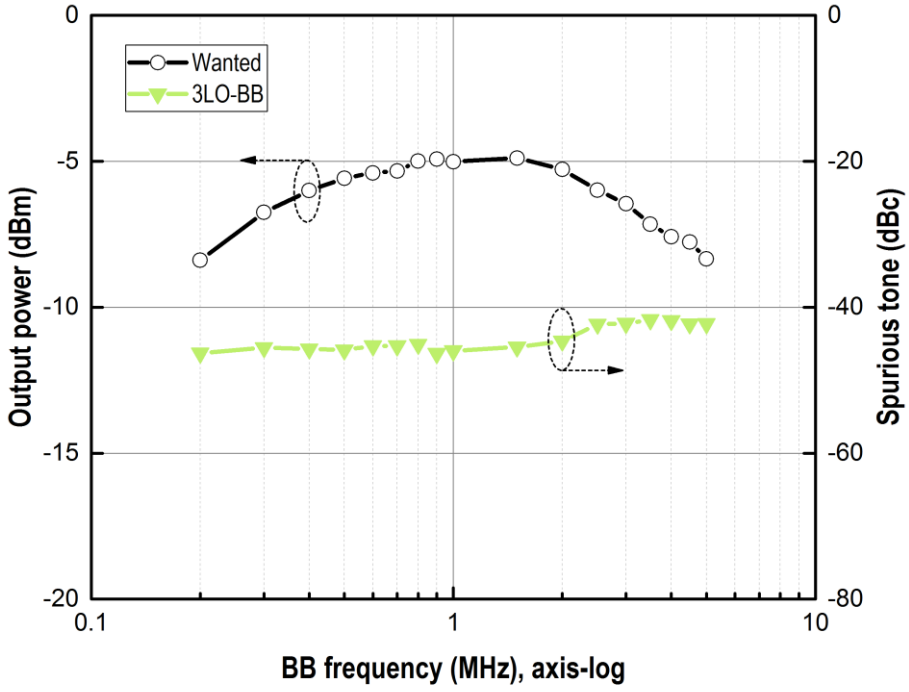


Figure 74. Measurement results of 3LO component vs BB frequency

5.4 Transmitter Performance Summary

Table 5. RF transmitter performance summary

Items	Unit	[20]	[23]	[11]	This work
Mode/BW	-	LTE/20MHz	LTE/20MHz	LTE/10MHz	LTE/5MHz
Carrier	GHz	2.5	1.95	0.782	0.782
Process	nm	130	55	40	180
Pout	dBm	1.3	5.5	2	-
O1dB	dBm	-	-	-	-0.7
OIP3	dBm	-	-	-	8.3
Duty Cycle	-	25%	50%	33%	33%
Mixer Type	-	Passive	Active	Passive	Active
CIM3	dBc	-50.6 Single-Tone	-57.1 1 RB	-70 1 RB	-60 Single-Tone
3LO Component	dBc	-	-	-	-45
3LO Component Filter	-	Yes	Yes	No	No
Supply Voltage	V	1.2/3	1.8	1.8	1.8
Power: Divider	-	Off-chip	Off-chip	On-chip	58mA@1.8V
Power: Analog baseband	-	16mA@1.2 V	-	-	8mA@1.8V
Power: Modulator	-	15mA@1.2 V	-	-	17mA@1.8V
Power: PPA	-	30mA@3V	-	-	23mA@1.8V
Power: Overall	mW	127.2	101	216	190.8
Chip Area	mm^2	1.04	1.3	0.93	0.7

The RF transmitter performance is summarized in Table 5. In this work, an RF system of transmitter targeting at suppression of counter 3^{rd}-order harmonic is designed and taped out in 180 nm process. Transmitters with different duty cycles and mixer types are compared in the table. Transmitters with 33% duty cycle LO have better CIM3 performance compared with the transmitters with 25% and 50% duty cycle LO. No linearization technique and frequency trap technique are used in [11] and this work, but it still outperforms [20] and [23]. It is concluded by [11] and this work that both passive and active mixer based architecture can be applied to the transmitter design with 33% duty cycle LO. [11] achieves better performance but it uses 1.8 V supply for 40 nm process. By increasing the PA driver stage supply voltage to 2.5 V, this design is expected to achieve better performance. Due to power consumption reason, 2.5 V is not adopted in this prototype. However, high voltage like 2.5 V can be applied to the system if the overall current consumption is kept small to protect the circuit.

CHAPTER 6

Conclusion and Future Work

6.1 Conclusion

In this thesis, previous literatures are studied and two main contributors of the CIM3 have been identified. The first and minor contributor comes from the baseband 3rd-order nonlinearity; the second and major contributor is due to the intermodulation between the wanted signal and the local oscillator (LO) signal's 3rd-order harmonic component. In the previous literature, targeting for the solution of the second contributor, an innovative 33% duty cycle LO signal has been proposed and successfully applied in the RF passive mixer based transmitter. In this thesis, as the continuation of previous literature, an RF transmitter (TX) employing active mixer approach with 33% duty cycle LO is designed, fabricated and successfully tested. The 33% duty cycle LO scheme is used because it intrinsically does not have 3rd-order harmonic. Thus the intermodulation with 3LO frequency component is avoided. As a result, CIM3 is suppressed at the RF output. This technique is not sensitive to device matching and calibration is not a pre-requisite. Since 3LO filtering requirement can be alleviated, the bill-of-material cost is reduced.

The TX prototype adopting 33% duty cycle LO is fabricated in GlobalFoundries (GF) RF CMOS 180 nm process. The TX active core occupies 1.4 mm × 0.5 m and this design is successfully tested on PCB. The measurement result shows that the designed TX achieves a power gain of 11 dB when VGA is set to the lowest bit. The operation frequency is from 350 MHz to 1.35 GHz. The output 1 dB compression point is measured at -0.7 dBm and the output 3rd-order intercept point is 8.3 dBm at the frequency of 782 MHz. The measured CIM3 and 3LO frequency component are less than -60 dBc and -45 dBc respectively up to output 1 dB compression point. The designed circuit also shows the consistency for the suppression of CIM3 to be less than -60 dBc over whole operating frequency. The power consumption of this TX is 190.8 mW with 1.8 V supply voltage.

In a summary, the designed system has explored the use of 33% duty cycle LO signal in active mixer based RF transmitter system. The counter 3rd-order intermodulation products has been suppressed in the output. The system achieves:

1) Simplicity: the harmonic suppression technique originates from the novel 33% duty cycle LO signal, which does not need calibration circuitry.
2) Cost effective: inductors are only required at the output stage. only a pair of inductors the system is optimized for minimized area;
3) Easy implementation: there is no extra effort required for the existing blocks in a typical transmitter except divider design. The traditional Gilbert cell active mixer is used in this design and this technique is also applicable for the passive mixers and other types of mixers like switched transconductance mixers. This technique can apply to the design with the different process without extra design effort.

6.2 Future Work

The prototype can be improved in terms of following aspects:

1) Solution for the frequency notch at LO frequency

It is shown in the measured spectrum that there is a frequency notch at LO frequency. This is due to the inserted capacitor and bias resistors forming a high pass filter. This issue can be solved by removing the DC coupling capacitor. As a result, the output voltage must be aligned with the common mode voltage for the mixers. The mixer can be modified as shown in Figure 75(a). Other mixer structures compatible with baseband output voltage level are also recommended since 33% duty cycle LO technique is not limited by the choice of mixer types.

2) LO's 2nd-order harmonic component suppression.

As shown in the LO output spectrum from Section 4.2.4, the 2nd-order LO is not suppressed. A 12-phase single-ended LO signal instead of 6-phase differential LO signal with 33% duty cycle can be implemented in the transmitter design. One mixer with 2-phase single-ended LO signal is shown as an example in Figure 75(b). Compared with the transmitter with 6-phase LO, the equivalent LO signal in the 12-phase transmitter intrinsically does not have even order harmonics as well as integer

multiples of 3rd-order harmonics. The simulated RF front-end output spectrum is shown in Figure 76. The cost of this design is the increasing complexity of divide-by-3 circuit design. Instead of digital FF based divider, TSPC divider can be chosen for single-ended mixer design but 12 phases will still burden the power and layout complexity. Further research regarding this topic will be focused in the future.

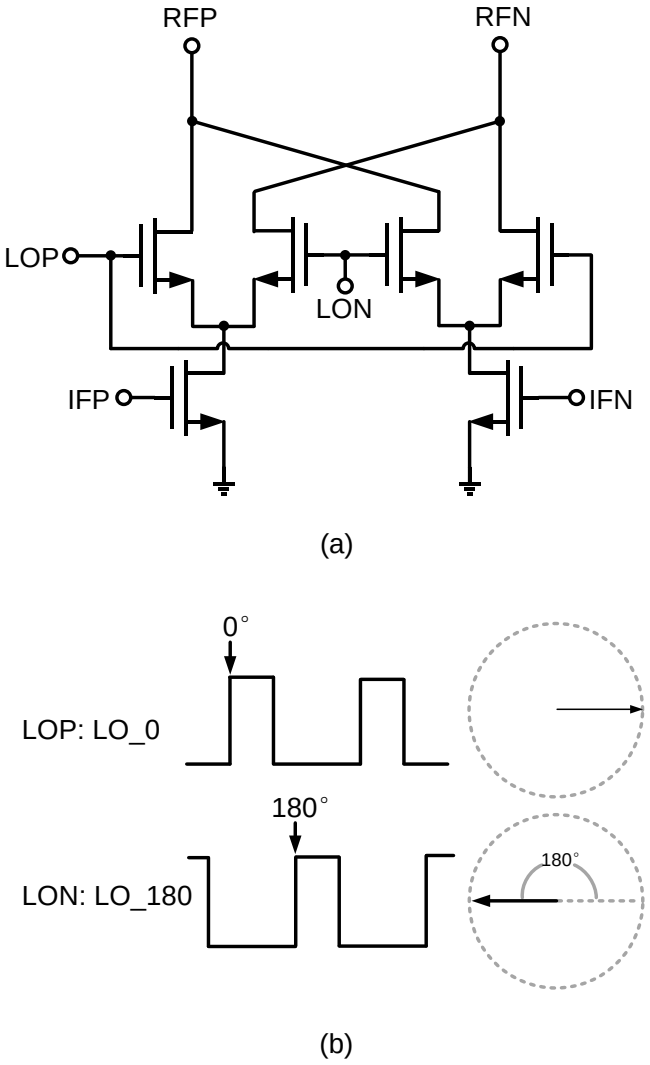


Figure 75. Circuit improvement of transmitter design, (a) improved mixer structure, (b) improved LO signal design

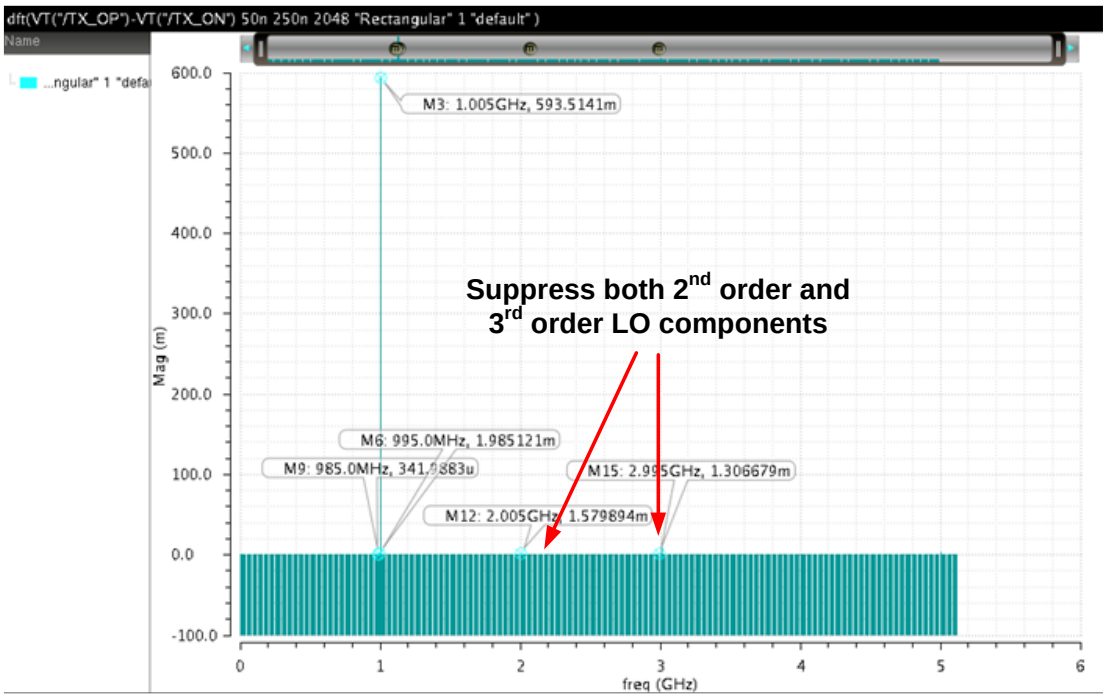


Figure 76. Simulation result of the 12-phase LO transmitter

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