Indium Tungsten Oxide Thin Films for Flexible High Performance Transistors and Neuromorphic Electronics

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Abstract

Thin film transistors (TFTs) with high electrical performances (mobility > 10 cm^2 /Vs, V_{th} < 1 V, SS < 1 V/decade, on/off ratio ~ 10^6) obtained from the silicon and oxide-based single-crystalline semiconductor materials require high processing temperature and hence not suitable for flexible electronics. Amorphous oxide based transparent electronic devices are attractive to meet emerging technological demands where crystalline oxide/silicon-based architectures cannot provide a solution. Here, we tackle this problem by using a novel amorphous oxide semiconducting material—namely indium tungsten oxide (IWO)—as the active channel in flexible thin film transistors (FTFTs). Post-annealing temperature at as low as 270°C for a-IWO thin films deposited by RF sputtering at room temperature could result in smooth morphology (R_{rms} ~ 0.42 nm), good adhesion and high carrier density (n ~7.19 × 10^{18} cm^{-3}). Excellent TFT characteristics of flexible devices could be achieved with linear field effect mobility μ_{FE} ~ 25.86 cm^2/Vs, sub-threshold swing SS ~ 0.30 V/decade, threshold voltage V_{th} ~ -1.5 V, on/off ratio I_{on}/I_{off} ~ 5.6×10^5 at 3V and stable operation during bending of the FTFT. Additionally, IWO TFTs were implemented as synapses, the building block for neuromorphic computing. Paired-pulse facilitation (PPF) up to 138% was observed and showed an exponential decay resembling chemical synapses. Utilizing this characteristic, high-pass dynamic temporal filter was devised providing increased gain from 1.55 to 21 when frequency was raised from 22 to 62 Hz. The high performance and stability of flexible TFTs obtained with IWO films demonstrate their promise for low voltage electronic applications.

1. Introduction

Transparent amorphous oxide semiconductors (TAOSs) have been considered as a potential candidate for application in thin-film transistors (TFTs) for backplanes in flat-panel displays based on active matrix organic light-emitting diodes[1–3] and liquid-crystal displays.[4,5] Besides, oxide semiconductor TFTs can display excellent device performance because of their high mobility and low leakage current attributed to their wider band gap compared to that of low temperature processed polycrystalline/amorphous silicon.[6] Park and co-workers developed crystalline IGZO (c-IGZO) thin films after annealing at 600°C in air environment for 1h to fabricate TFT with high field effect mobility[7] of 14.59 cm^2/V s. A lot of oxide semiconductors, e.g., zinc oxide (ZnO), IGZO, IZO, ZTO, have been prepared with various deposition techniques at high temperatures and studied for possible TFT applications.[8–12]

However, high processing temperatures to unlock good device performance like impressive linear field effect mobility, turn-on voltage, on/off ratio and degradation in acidic environments are challenges to be overcome when fabricating electronic devices on flexible substrates such as polyethersulphone, polyethylene naphthalate, polyethylene terephthalate, and polycarbonate[13–19]. In 2004, Nomura et al. demonstrated an amorphous –IGZO TFTs on inexpensive polymer films and displayed good performance—such as saturation mobilities of ,6–9 cm^2/V-s , a low leak current of ,10^{-10}A, and an on-to-off ratio of 10^3 — even during and after bending.[20]

The archetypical TAOS is InGaZnO (IGZO) which is well explored due to its deposition at low temperatures, good uniformity (root mean square roughness, $R_{rms} < 2$ nm), decent mobility (μ_{FE} ~10-100 cm^2/Vs), and high optical transparency (T > 80%) in the visible region compared to polycrystalline silicon.[18, 20–25]

Recently, InZnO,[26] Sn-InZnO,[27] Hf-InZnO,[28] Si-InZnO,[29] Zr-InZnO[30] and InGaO[31]

have been deposited at low substrate temperature and explored to improve the device performance. However, TFT devices associated with Zn/Ga-containing channel layer have been reported to be very sensitive to moisture, which results in poor performance and stability.[30,32] Several passivation strategies have been implemented to improve the stability of the devices.[19, 33–35]

To address the above issues, Ga /Zn free TAOS such as indium tungsten oxide (IWO) can be examined for making high performance and stable flexible TFTs. In IWO, In_2O_3 acts as matrix to provide high electron mobility due to band conduction originating from an edge-sharing polyhedral structure while W (tungsten) as dopant enhances its stability in most acidic environments.[36–38] IWO has been utilized as transparent conductive electrodes as well as semiconducting layers [39–43] for devices on rigid substrates. However there has been no attempt to address the challenges of developing semiconducting IWO channel layers for flexible TFT. In the present study, we demonstrate usage of IWO for flexible TFTs and the role of its physical and optical characteristics on the performance and stability of the devices. Additionally we have utilized IWO TFTs as synapses, the building block for neuromorphic computing. Synaptic transistors may have a wide range of applications, such as bendable smart tags and low-power neuromorphic chips for use in pattern recognition and other learning tasks.

IWO-based TFTs were fabricated on both rigid (Si wafer) and flexible (Polyimide film) substrate for comparison. Optimized fabrication process for semiconducting IWO channel, high-k dielectric and low contact resistance electrode that results in high performance flexible TFTs are presented.

2. Experimental

2.1 Material synthesis and TFT fabrication process

The top-contact bottom-gate (TCBG) staggered structure was adopted for both of rigid and flexible TFT fabrication shown in **Figure 1a**. For rigid TFTs, Si wafer with 100 nm thick SiO_2 oxide layer was used and cleaned with acetone, methanol and deionized (DI) water in ultrasonic bath prior to sputtering deposition. The procedure to fabricate flexible polyimide substrate is described as follows.

To serve as the carrier substrates for the flexible TFTs , bare glass slides (Si wafer pieces) were cleaned using similar procedure described above followed by the deposition of polyimide (PI) precursor solution (Poly (pyromellitic dianhydride-co-4,4-oxydianiline), amic acid solution) by spin coating (2000 rpm for 30 seconds). The substrates were baked on a hot plate with temperatures gradually increased from 100 to 300°C over 2 hours. The cured PI film could be peeled off from the handle substrate and had a thickness of ~10 µm. A 300 nm SiO_2 inter layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) onto the PI film at 200°C. Titanium film (250 nm thick) was deposited by sputtering on top of the SiO_2 inter layer for bottom gate contact. Gate dielectric layer of Al_2O_3 (130 nm thick) was deposited by thermal Atomic Layer Deposition (ALD) (Cambridge Nanotech, Savannah S200) at 150°C using Trimethylaluminum (TMA) precursor and H_2O as reactant. No any additional heating/ deposition temperature has been carried out. To measure capacitance values, aluminum circular electrodes (100 nm thick) were thermally evaporated on SiO_2 and Al_2O_3 to form capacitor devices with metal-insulator–metal (MIM) structure (**Figure S1**).

IWO thin films (thickness ~7 nm) were deposited on SiO_2 (Si substrate) and on Al_2O_3 (PI substrates) at room temperature using RF magnetron sputtering with an

$In_2O_3:WO_3$ (98:2 wt%) target (Kurt J. Lesker, 99.99% purity). The sputtering system was initially evacuated to 3×10^{-6} mbar followed by the deposition of IWO at a chamber pressure of 5 mtorr, RF power of 50W, and a mixed Ar : O_2 (20:1) gas flow. Source and drain contacts (thickness ~100 nm) were sputter deposited (rate of 0.27Å/s) through a shadow mask by using In_2O_3: SnO_2 (90: 10 wt%) target (Kurt J. Lesker, 99.99% purity) with RF power and Argon gas pressure maintained at 50W, 5 mtorr, respectively. Before TFT measurement, all devices were annealed at two different conditions 200°C and 270°C on a hot plate for 30 minutes in air ambient. The measured devices have an electrode width (W) of 4000 μm and a channel length (L) of 200 μm. For the bending tests, fabricated devices were gently released from the glass (Si) handle substrates and transferred onto curved surface with a pre-determined radius.

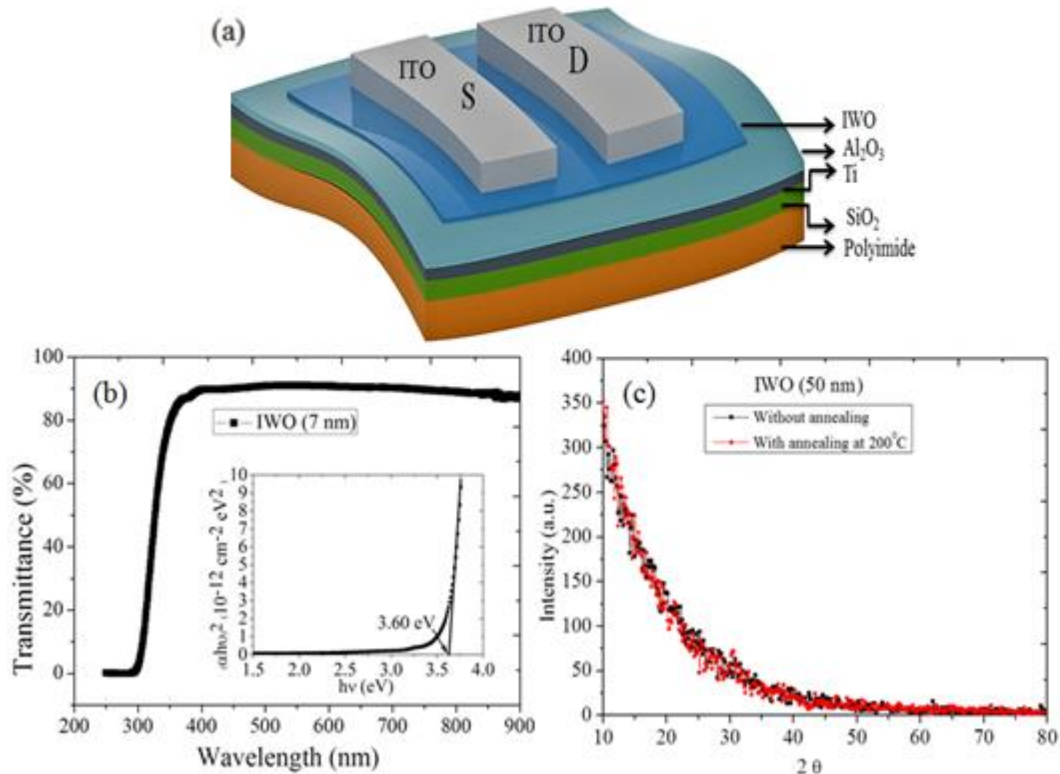

Figure 1. (a) Schematic diagram of the experimental procedure for the flexible TFTs (b) Transmittance plot of the IWO film, inset showing $(\alpha h\nu)^2$ versus hν plots of IWO thin films annealed at 200°C for 30 min in air environment (c) XRD pattern of IWO (50 nm) film.

2.2 Characterization

2.2.1 Electrical Characterization

The output and transfer characteristics of the transistors devices were measured under ambient condition using Keithley 4200 semiconductor characterization system. The transfer characteristics (I_{DS}-V_{GS}) are employed to extract the electrical performance parameter such as like field effect mobility (μ_{FE}), threshold voltage (V_{th}), sub-threshold slope (SS), and on/off current ratio (I_{on}/I_{off}). The threshold voltage (V_{th}) calculated from the intercept of the extrapolated $\sqrt{(I_{DS}-V_{GS})}$ plot with the horizontal, V_{GS} axis. The μ_{FE} value was calculated using the following equation:

$$\mu_{FE} = \frac{L}{C_{ox}W\ V_{DS}} \text{.......................................[1]}$$

where L and W are the channel length and width, respectively, g_m and C_{ox} is the transconductance and capacitance per unit area. For mobility calculation the capacitance value of SiO_2 (2.8 x 10^{-8} F/cm^2) and Al_2O_3 (0.53 x 10^{-7} F/cm^2) were measured from capacitor device using Agilent E4980A precision LCR meter. Dielectric constant was estimated to be 3.2 and 7.8 for SiO_2 and Al_2O_3, respectively

2.2.2 Material Characterization

Surface morphology of IWO films on Al_2O_3 / Ti / SiO_2 / Si were analyzed by Atomic Force Microscopy measurements. X-ray photoelectron spectroscopy (XPS) measurements were obtained by PHI Quantera II (Al Kα 1486.6 eV source) at pressure of 4.5×10^{-10} torr . The XPS depth-profile of the thin films was also recorded by etching the film via Ar^+ ion sputtering at the rate 2.5 nm/min. XRD pattern of 50 nm thick IWO layer annealed at 200°C was collected by X-ray diffraction (GIXRD) (Bruker D8 Advance Diffractometer). Contact angle of the annealed IWO film was measured using

distilled water (Dataphysics; OCA 15 Pro). The IR spectra of the IWO thin film on Si/SiO_2 substrate were obtained using an Attenuated total reflection (ATR) spectrophotometer (ATR spectrum GX; PerkinElmer) and transmittance of IWO thin film by Lambda 950 UV/Vis Spectrophotometer.

3. Results and discussion

3.1 Physical Characteristics

IWO thin films exhibit high optical transmittance (T ~ 90%) in the visible region as shown in **Figure 1b**. The transmittance spectrum can be used to determine the absorption coefficient (α), (defined by—[lnT]/t; T is the transmittance, t is film thickness) for calculating the optical band gap (E_g) from the equation:

$$(\alpha h\upsilon)^2 = A\ (h\upsilon - E_g) \qquad [2]$$

where hυ is the incident photon energy and A is the proportionality constant.[44] The optical band gap is calculated to be 3.60 eV for the annealed IWO film (inset of **Figure 1b**). XRD measurement of 50 nm thick films (**Figure 1c**) indicated amorphous nature with or without annealing at 200°C, in agreement with previous reports.[43, 45] However, annealing was shown to improve morphological characteristics of the film as observed by AFM (**Figure S2**). The roughness (root mean square, R_{rms}) values of the film without annealing was 0.5 nm, which after annealing at 200 and 270°C reduced to 0.46 and 0.42 nm, respectively.

The surface composition of IWO thin films annealed at 200 and 270°C were investigated by XPS. The O1s spectra of the annealed films were fitted by three Gaussian distributions, approximately centered at 529.71, 531.29, and 532.54 eV (**Figure 2a** and **b**). The low binding energy (O_L) peak at 529.71 eV is attributed to

metal–oxygen (M-O) bonds. The medium binding energy (O_M) peak at 531.29 eV is attributed to O^{2-} ions that are in oxygen-deficient region within the indium oxide

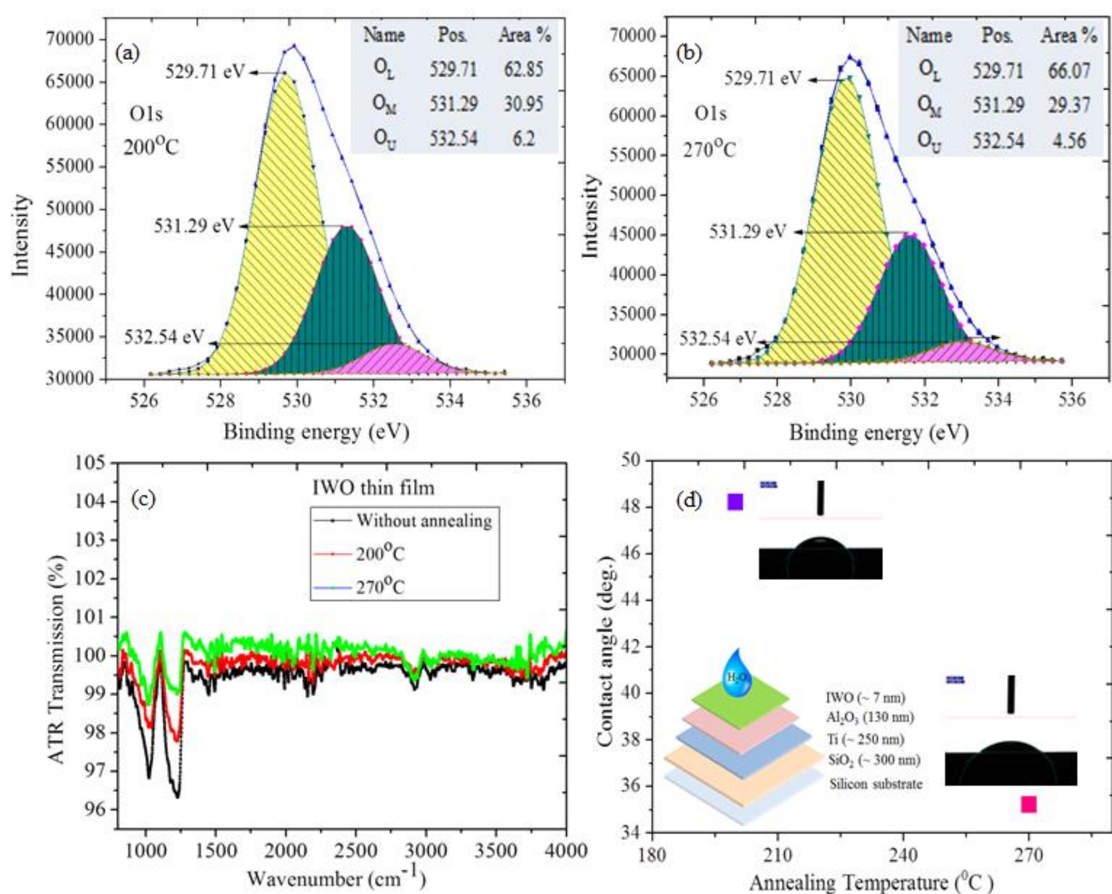

Figure 2. XPS spectra with Gaussian fitting curves for O1s of IWO annealed thin film annealed at (a) 200°C and (b) 270°C (c) Attenuated total reflection Fourier transform infrared (ATR-FTIR) spectrum of IWO thin film at different annealing temperature (d) Contact angle of IWO thin film annealed at 200 and 270°C.

matrix. The higher binding energy (O_U) peak at 532.6 eV is associated with loosely bonded oxygen such as chemisorbed $–CO_3$, adsorbed OH^-, or absorbed H_2O/ O_2, on the surface of IWO thin films.[46] The area percentage distribution of each species in both films is shown in inset of **Figure 2a** and **b**. The M-O bonding was enhanced in the film annealed at 270°C (66.07%) in comparison to annealing at 200°C (62.85%) while the loosely bonded oxygen species are slightly reduced for film annealed at 270°C. The ratio of the peak areas of V_O (oxygen vacancy) and O_O (lattice oxygen) gives an estimate

of oxygen deficiency, which is estimated to be 0.49 and 0.44 in the films annealed at 200 and 270°C, respectively. Lower oxygen vacancies in IWO film annealed at 270°C is possibly due to the increased complete oxidation of metal atoms on the film surface. The value of carrier concentration (n) measured from Hall effect was estimated to be 2.72×10^{18} and 7.19×10^{18} cm^{-3} for the films annealed at 200 and 270°C, respectively. A slight increase in carrier concentration at higher annealing temperature is possibly due to reduction of trap states, and relaxation of the film. Attenuated total reflectance (ATR) spectra of the IWO films with and without annealing exhibited three absorption peaks at 1020, 1227 and 2918 cm^{-1} (**Figure 2c**) associated with loosely bonded oxygen species of C-O,-OH, and C-H, respectively.[47] The absorption of all peaks decreases with increasing annealing temperature in-line with the observations from XPS analysis.

Surface energy estimations of the films were carried out by performing contact angle measurements of the IWO films as shown in **Figure 2d**. The film annealed at 270 °C exhibits smaller contact angle ($\theta_o \approx 35.2°$) than the film annealed at 200°C ($\theta_o \approx 48.2°$). This is possibly due to lowered surface roughness (R_{rms} ~ 0.42 nm) and lower concentration of adsorbed organic molecules (**Figure S2** and **Figure 2c**) after annealing at higher temperature. Surface energy (γ_p) was estimated from contact angle following the equation:

$$\gamma p = \frac{\gamma w}{4} \times (1 + \cos\theta_o)^2 \quad \text{..[3]}$$

where θ_o is the contact angle at equilibrium and γ_W is the water surface free energy (73 mJ/m^2).[48] The values of γ_P of the films annealed at 200 and 270°C were determined to be 50.48 and 60.25 mJ/m^2, respectively. Higher surface energy of the film annealed

at 270°C can indicate better adhesion between the semiconductor and the ITO S/D contacts for TFTs.

3.2. Transistor Performance characteristics

The electrical characteristics of the IWO TFT on rigid Si/SiO_2 substrate are shown in **Figure 3a**.The TFT exhibited field effect mobility (μ_{FE}) of 7.1 $cm^2.V^{-1}s^{-1}$, threshold voltage (V_{th}), -0.6 V, and sub-threshold swing (SS) of 0.28 V/dec .The output

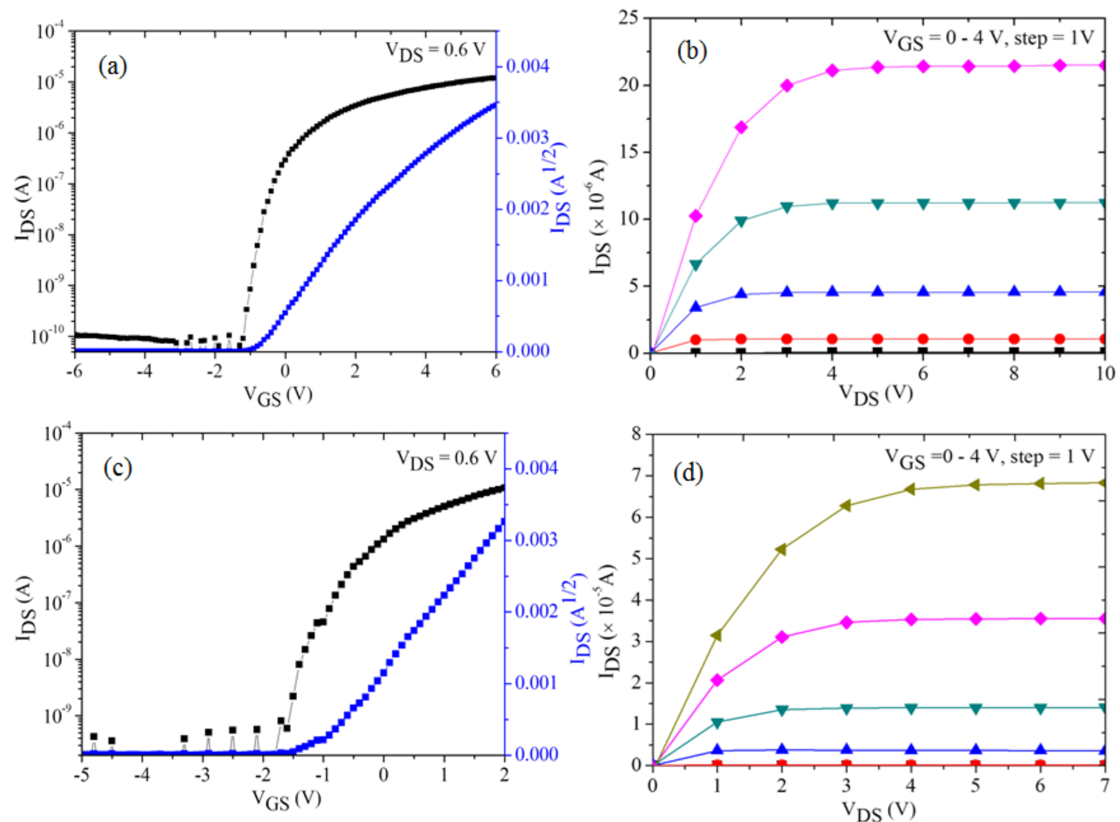

Figure 3. (a) Transfer characteristics of IWO TFT (W =4000 μm, L = 200 μm, W/L = 20:1) on SiO_2 dielectric layer with annealing at 200°C. The applied drain voltage, V_D is 0.6 V, inset showing $\sqrt{I_{DS}}$-V_G for V_{th} calculation. (b) Output characteristics. (c) Transfer characteristics of flexible IWO TFT annealed at 200°C (d) Output characteristics.

characteristics (I_D-V_{DS}) show the clear saturation behavior from the onset of V_{DS} ~ 3V and V_{GS} ~ 4V (**Figure 3b**). The stability of semiconductor material upon light illumination has been performed with 445 nm (blue light), 693.06931 W/m^2 (intensity).

Upon Light illumination graph shifted toward left direction and recovered back to the original position within 30 min, which shows that material have good stability as shown in **Figure S2**.

To test the electrical stability of the devices, positive gate bias stress (PGBS) was applied in the dark with gate bias at 20 V and zero bias at source and drain electrodes in order to keep a uniform potential through the channel layer (see **Figure S3).** Threshold voltage shift, ΔV_{th}, was analyzed as the indicator of stability in devices. The threshold voltage shift after PGBS stressing is obtained using the equation:

$$\Delta V_{th} = [V_{th}(1000\ s) - V_{th}(0\ s)] \quad [4]$$

where V_{th} (0 s) is the threshold voltage without stressing and V_{th} (1000 s) is the threshold voltage at stressing of 1000 s. The original threshold voltage V_{th} (0 s) was extracted to be -0.6 V as shown in **Figure 3a**. The PGBS-induced variation showed very little threshold voltage shifting (ΔV_{th} = + 0.8 V) in our IWO TFT. This value is better than IGZO devices with ΔV_{th} ~ 2.0 V.[35, 50] The parallel shifting of I_{DS}-V_{GS} curves under positive gate biased conditions in IWO device is associated with charge trapping rather than defect creation within the semiconductor. The maximum trapped charge density (N_{max} ~ 0.76×10^{12} cm^{-3} eV^{-1}) is 1-order smaller than the reported IGZO (N_{max} ~ 1.05×10^{13} cm^{-3} eV^{-1}), possibly due to large optical band gap and better binding ability of W in IWO than Ga and Zn in IGZO.[49]

For realization of flexible IWO TFTs, a thin interlayer of SiO_2 (roughness ~ 0.135 nm) (see **Figure S4**) was deposited on top of the PI substrate (roughness ~ 0.365 nm) by PECVD. The reduced roughness in SiO_2 layer helped to improve the substrate morphology for the subsequent deposition of good quality gate electrode and high-k dielectric layer. The cross-section image of the various stacking was obtained by

FESEM showing the thickness of each layer and interfacial adhesion as shown in **Figure S1**. Al_2O_3 film exhibits high capacitance value of 0.53 x 10^{-7} F/cm^2 with high dielectric constant value of 7.8 (see **Figure S1**). The electrical characteristics of the flexible TFT are shown in **Figure 3c, d** and **Figure 4a, b**. The TFT output characteristics exhibit a clear pinch-off and current saturation, as described by standard field-effect transistor theory. The flexible TFT annealed at 200°C for 30 minutes on hot plate exhibited good linear field effect mobility of 10.25 cm^2/V·s,

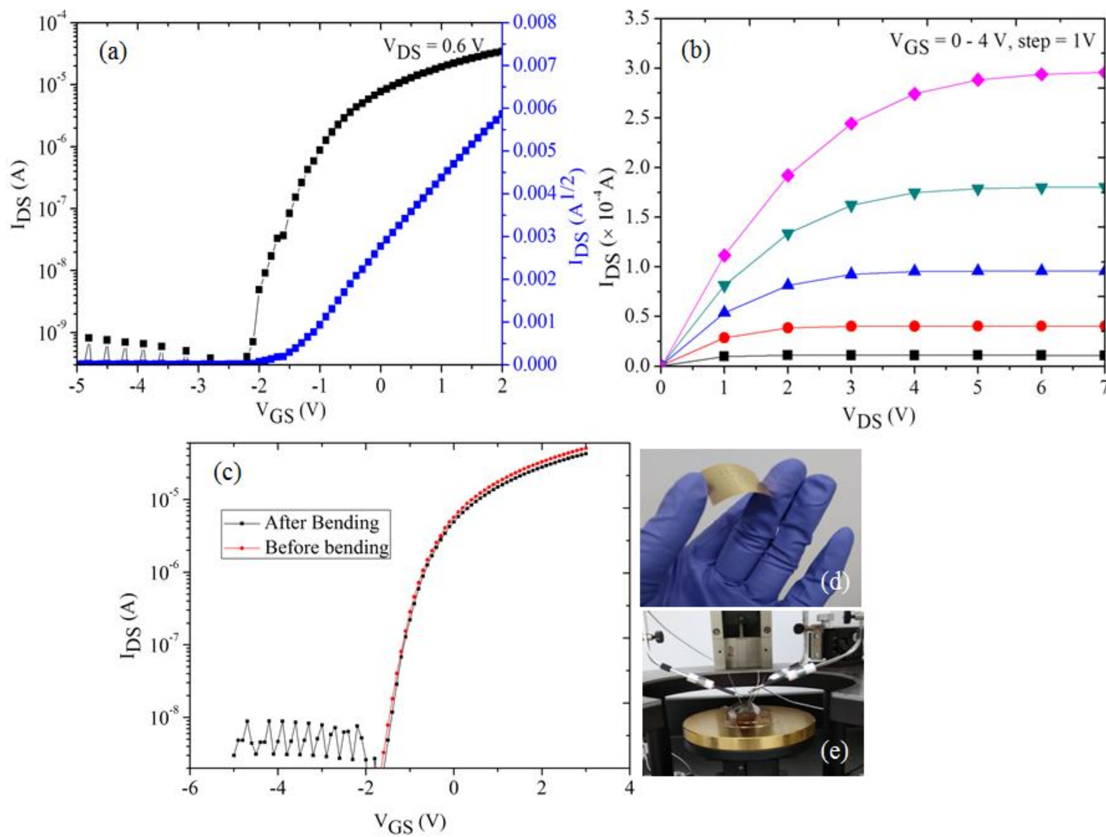

Figure 4. (a) Transfer characteristics of flexible IWO TFT (W = 4000 μm, L = 200 μm, W/L = 20:1) annealed at 270°C . The applied drain voltage, V_D is 0.6 V, and gate voltage, V_G is −5 to 3 V (b) Output characteristics (c) Transfer characteristics of flexible IWO TFT annealed at 270°C before and after bending (d) optical image of flexible TFT (e) bending test (R = 20 mm).

subthreshold swing (SS) of 0.47 V/decade, threshold voltage (V_{th}) of -1.15 V and on/off current ratio (I_{on}/ I_{off}) of 2.09 × 10^5. The device performance improved further

(μ_{FE} ~ 25.86 cm^2/Vs, SS ~ 0.30 V/decade, V_{th} ~ -1.5 V and I_{on}/I_{off} ~ 5.6×10^5) upon annealing at 270°C for 30 minutes (see **Figure 4a** and **b**). The transfer characteristics of all devices annealed at 200 and 270°C exhibited clockwise hysteresis (**Figure S5**) indicating the dominance of interfacial charge trapping between dielectric and semiconducting layers. The values of hysteresis were determined from the difference of gate voltages between the forward and reverse sweep traces at drain current of 10^{-9} A. The hysteresis of the TFT annealed at 200°C was 0.5 V at V_{DS} = 0.6 V, while this value reduced to 0.3 V for the TFT annealed at 270°C. The lowered hysteresis is possibly attributed to the i) decreased electron trap centers owing to better interface of insulator/channel and electrodes/semiconductor layers quality (**Figure 2d**) ii) lower charge trapping by the adsorbed water (**Figure 2a,b** and **Figure S2**) on the semiconductor surface annealed at 270°C. Clearly, the carrier mobility of the TFT annealed at higher temperature is improved and the threshold voltage shift in the negative direction. Annealing temperature as low as 270°C, which can improve the interfacial adhesion without altering the amorphous nature (**Figure 1d**) of the semiconductor film, is critical for devices built on flexible substrate platform. These results are associated with higher surface energy effects and thus the higher adhesion properties (**Figure 2d**) of IWO films annealed at 270°C. It can enable more compact structure, better atomic relaxation and fewer electron traps to yield higher field effect mobility. Gate leakage current of transistors are shown in **Figure S6**.

To demonstrate the flexibility of IWO-TFT, test samples were released from the handle substrate and attached to convex curved surface with radius of 20 mm as shown in **Figure 4c**. The transfer characteristics measured during bending showed excellent flexibility and mechanical stability of the IWO semiconducting channel. Carrier mobility during bending state maintained over 92% of the initial value for a bending

radius of 20 mm, while no adverse effects on OFF-state current, threshold voltage and subthreshold swing could be observed (μ_{FE} ~ 24.86 cm^2/Vs, SS ~ 0.28 V/decade and V_{th} ~ -1.3 V). Our results indicate that the IWO-based TFTs showed great potential for applications in various flexible devices.

3.3. Synaptic Transistor

In addition, IWO TFTs were implemented as synapses, the building block for neuromorphic computing. The presence of defects at the semiconductor-dielectric

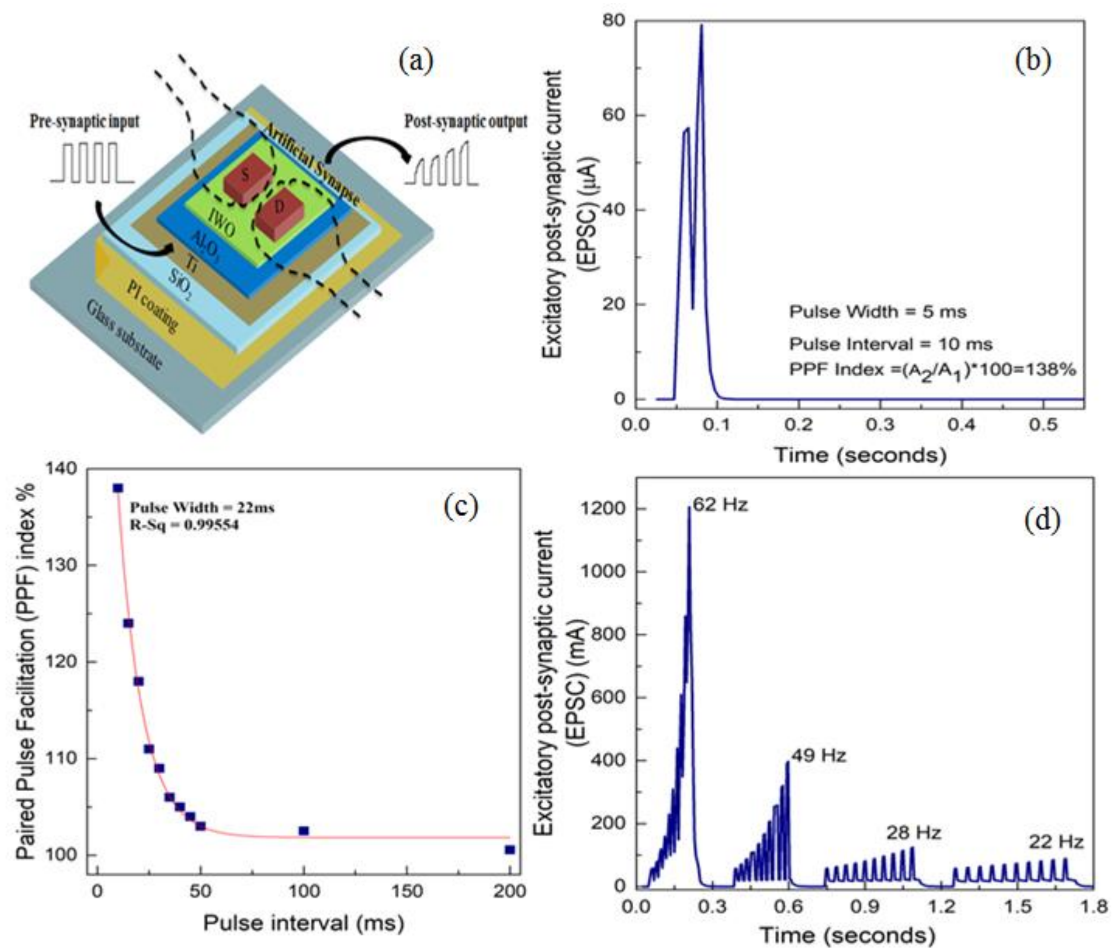

Figure 5. (a) Schematic diagram of artificial synapse . (b) Pair of input spikes (pulse width = 5 ms) with a time interval of 10 ms. (c) Paired pulse facilitation (PPF) index vs. pulse interval. (d) Excitatory postsynaptic currents (EPSCs) results from the presynaptic stimulus trains of different frequencies.

interface was utilized to create time-varying electronic properties allowing emulation of short-term synaptic functionalities, such as paired pulse facilitation (PPF) and dynamic temporal filtering.[51] For these synaptic transistors, gate terminal served as the presynaptic input while the semiconducting IWO channel with source/drain electrodes functioned as post-synaptic output terminals as shown in **Figure 5a**. Interfacial traps mimicked neurotransmitters, while channel conductance served as the synaptic weight. When stimulated by paired pulses in rapid succession, the second excitatory post-synaptic current (EPSC) was observed to be larger than the first - a phenomenon called neural facilitation or paired-pulse facilitation (PPF). Analogous to the residual Ca^{2+} hypothesis by Katz and Miledi,[52] PPF index could be used to quantify facilitation of EPSCs and is an easy measure of synaptic vesicular release probability. In our study, when the pulse interval was kept below 50 ms, the PPF index was observed to be much higher than 100 %, indicating a strong facilitation. The maximum PPF index observed was ~138% and this ratio continued to decrease with increasing pulse interval and finally reached around 100 % for the largest pulse interval of 500 ms. This observed decay of PPF index with pulse interval was fitted with an exponential function (**Figure 5c**) in resemblance to chemical synapses. This temporal behaviour was further extended to create high-pass dynamic temporal filters [51] (**Figure 5d**) showing an increasing gain as a function of frequency. The gain, obtained from the ratio of amplitudes of the tenth EPSC (A_{10}) and first EPSC (A_1), increased from 1.55 to 21 with increasing stimulus frequency from 22 to 62 Hz. These results indicate the potential of building artificial synapses and neural networks using IWO TFT devices. .

4. Conclusion

In summary, we have fabricated high-performance flexible IWO TFT at low temperature. Al_2O_3 used as dielectric layer provides a high capacitance to enhance the

transistor performance. Post-annealing of devices at low temperature of 270°C improves linear field effect mobility, sub-threshold swing and reduced device hysteresis. Moreover, synaptic behaviors can be extracted from IWO TFT indicating its possible usage as a building block of next generation neural circuits. Among other TAOS-based candidates, amorphous indium–tungsten oxide (a-IWO) as an active layer featuring low-temperature manufacture can exhibit great potential for flexible electronics/display applications.

Supporting Information.

Details of material such as capacitance vs frequency measurement of Al_2O_3,cross sectional SEM image, 3D AFM images IWO films without and with annealing, positive gate bias stress test, 3D AFM images IWO films on PI / Glass (Si) and SiO_2 /PI / Glass (Si) and stability test of TFTs supplied as supporting information.

Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

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