An Injection-Nulling Switch for Switched-Capacitor Circuit Applications

W. F. Lee and P. K. Chan

***Abstract*—This paper presents a new switch, the injection-nulling switch (INS), for minimizing both the charge injection error and the clock feedthrough error in switched-capacitor circuits. Comprised of two identically designed MOS transistors and a capacitor, INS benefits from using matching transistor characteristics, which result in an improvement in the reduction of switch errors on the conventional techniques. In this paper, the working mechanism of the INS technique and the analysis of the impact of nonideal effects on the switch are described. A comparison with other switch employments using sample-and-hold circuit implementation in AMS 0.6-μm CMOS technology is also discussed. The simulation results have verified that the proposed method is insensitive to the nonideal effects. Besides, its effectiveness has also been validated by the experimental results.**

***Index Terms*—Analog switch, charge injection, clock feedthrough, integrated circuits, switched-capacitors circuits, switched-networks.**

I. Introduction

SWITCHED-CAPACITOR (SC) circuits have been widely used for decades. Not only are they being employed in both integrated circuits (IC) [1]–[4] and discrete component implementation [5], but they also play a very important role in the instrumentation circuits, such as sensor interfacing [6], [7] and capacitance sensing [8]. Although they possess many advantages over the conventional resistive circuits, for example, low power consumption and better temperature invariance, they have their own fundamental problems, that is, the charge injection (CI) error and the clock feedthrough (CKFT) error. These nonideal switch errors, which originate from MOS switches, greatly limit the performance of precision measurements. Hence, it is important to minimize these errors so that the accuracy and the resolution can be improved.

To reduce these errors, the use of either a CMOS switch [9] or a dummy switch (DS) [1] is common. The CMOS technique aims to cancel out the CI error of the NMOS transistor by using that of the PMOS transistor, and vice versa. However, in a typical CMOS switch, the vast difference in their threshold voltages causes the two transistors to turn off at different time instances, which results in an unavoidable CI error. In addition, the presence of large parasitic capacitance mismatch also makes the compensation of the CKFT error ineffective. In many SC circuits, the DS is more desirable. It employs a main MOS transistor either in series with a dummy MOS transistor or sandwiched between the two. As the DS is half of the size, upon turning off of the main transistor, the dummy transistors are assumed to absorb half of the channel charge. However, in practice, it is difficult for the two transistors to establish an exact half-ratio proportion on all their characteristics, especially on the parasitic capacitance. Therefore, it is normal to observe the existence of some residual switch errors.

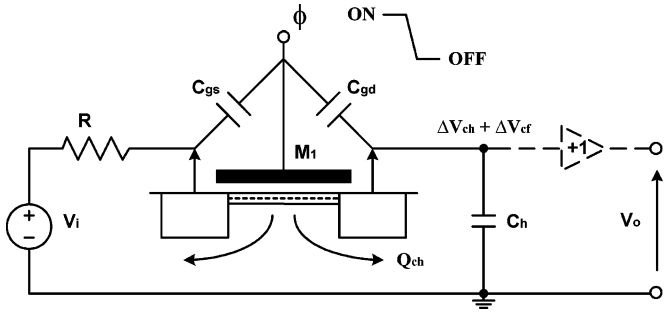

Fig. 1. Charge injection and clock feedthrough mechanism of a single MOS transistor.

This paper presents an approach using the new injection-nulling switch (INS) [10] to circumvent the above-mentioned problems. A considerable improvement in the reduction of the switch errors will be shown using two identically designed MOS transistors and a capacitor. Following this introduction, the mechanisms of both the CI error and the CKFT error are illustrated. Section III proposes the INS technique in conjunction with the derivation of its error. The analysis of the nonideal effects on the switch, such as the geometry mismatch and the threshold voltage mismatch, is given. Then a comparison with the conventional switch methods implemented on the sample-and-hold (S/H) circuit is presented in Section V. Finally, the conclusions drawn are presented in Section VI.

II. Charge Injection and Clock Feedthrough

This section illustrates the mechanism of CI error and CKFT error using a single NMOS transistor switch in a simple S/H circuit (Fig. 1). When the NMOS transistor M_1, driven by a clock signal ϕ, is switched on (i.e., the gate-to-source voltage V_{GS} is larger than the threshold voltage V_T), it operates in the triode region with approximately zero voltage across its drain and source terminals. The channel of M_1 is then inverted, and the amount of accumulated channel charge is given by [1]

$$Q_{ch} = -\mathrm{WLC}_{OX}\left(V_{GS} - V_T\right) \quad \text{for} \quad V_{GS} > V_T \qquad (1)$$

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where L and W are the effective channel length and width of M_1, respectively, and C_{ox} is the gate capacitance per unit area. Note that the accumulation of electrons in the channel accounts for the negative sign.

Subsequently, when M_1 is turned off, due to the fact that there is no longer an electrical force attracting the channel charge, the charge starts to flow to both the drain and the source terminals. The fraction (α) of it that is eventually stored in the holding capacitor C_h gives rise to the CI error voltage V_{CI}, which is written as

$$V_{CI} = \frac{\alpha Q_{ch}}{C_h} = \frac{-\alpha \mathrm{WLC}_{OX}\left(V_{GS} - V_T\right)}{C_h} \text{ for } V_{GS} > V_T. \tag{2}$$

This will cause some nonlinear distortion in the input signal [1] because of the signal-dependent parameters α, V_{GS}, and V_T. Incidentally, α depends on the transition rate of the driving clock [11]. If the rate is high (in fast switching condition), owing to the lack of time for charge distribution that results in an equal spreading on both terminals, α can be approximated to 50%. But, if the rate is slow enough to allow a charge distribution such that a higher proportion of the charge goes to the side with lower impedance, α will take a different value. Despite the possibility that a slow transition rate can minimize α for reducing the CI error, because of the increase in the power dissipation due to the long rise and fall time of the clock edges, it is often not considered. This makes the high clock rate popular in most applications.

In contrast, CKFT error does not cause any distortion as it relies only on the ratio of capacitances and the difference in clocking voltages. Basically, through the parasitic capacitance C_p between the gate and either of the terminals, the abrupt transition change in the clocking voltages causes a sudden flow of charge toward the holding capacitor C_h. This produces the CKFT error voltage V_{CKFT}, which is given by

$$V_{\mathrm{CKFT}} = \frac{-\left(V_{DD} - V_{SS}\right) C_p}{C_h + C_p} \tag{3}$$

where V_{DD} and V_{SS} are high and low voltage levels of the clock signal, respectively, and C_p is the parasitic capacitance seen by C_h. Note that the negative voltage step, due to the falling-edge of the clock, gives the result of the negative sign.

More generally, the total error voltage is expressed by

$$V_E = V_{CI} + V_{\mathrm{CKFT}}. \tag{4}$$

III. Injection-Nulling Switch

As mentioned earlier, the INS comprises two identically designed NMOS transistors and a capacitor. Fig. 2 shows how these components (M_i, M_n, and C_n in the dotted box) are connected in a S/H circuit together with the clocking scheme. In particular, terminal H is joined to the high-impedance MOS-gated opamp input, which is prone to switch errors. Although the clock signal ϕ_n (switching M_n) is a phase-shifted signal of ϕ_i (switching M_i), ϕ_n and ϕ_i are of the same frequency and can be easily realized using digital clock dividers. Based on this clocking scheme and the principle of charge distribution, the mechanism of the INS technique is described as follows.

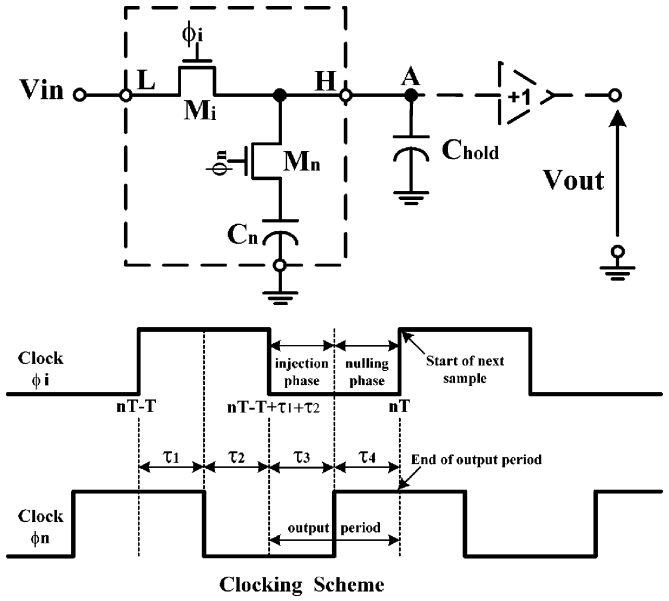

Fig. 2. Novel general structure and clocking sequence of INS to cancel charge injection and clock feedthrough errors.

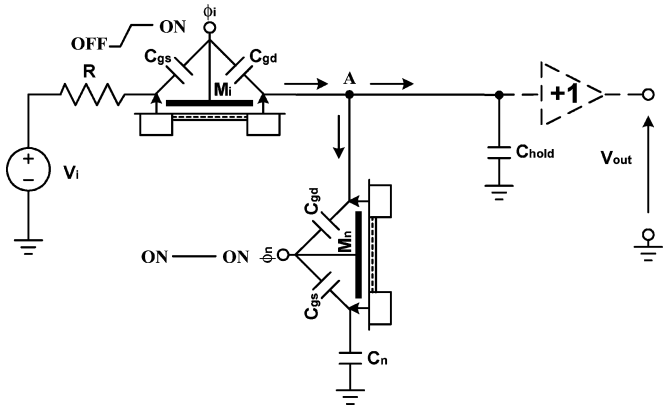

Fig. 3. Operation of INS during time interval τ_1.

The operation starts from τ_1, the interval when both M_i and M_n are turned on (Fig. 3). During this time, the two capacitors C_{hold} and C_n are directly connected to the input signal with voltage $V_i\left(nT - T + \tau_1^-\right)$, where nT represents the n^{th} sampling instance of the clock period T, and τ_1^- signifies the interval from the beginning to the end of τ_1 just before going into τ_2. By definition, when the voltage across a capacitor, with capacitance C, changes from 0 to V, the amount of charges Q stored in the capacitor is expressed as $Q = \int_0^V C dv = CV$. Accordingly, given that the clocking period has been designed to ensure sufficient settling time for the charge transfer, the charge stored in C_{hold} and C_n are given by

$$Q_{\mathrm{hold}}\left(nT - T + \tau_1^-\right) = V_i\left(nT - T + \tau_1^-\right) C_{\mathrm{hold}} \tag{5}$$

$$Q_n\left(nT - T + \tau_1^-\right) = V_i\left(nT - T + \tau_1^-\right) C_n \tag{6}$$

where

$Q_{\mathrm{hold}}\left(nT - T + \tau_1^-\right)$ charge stored during τ_1^- in the holding capacitor C_{hold};

$Q_n\left(nT - T + \tau_1^-\right)$ charge stored during τ_1^- in the nulling capacitor C_n;

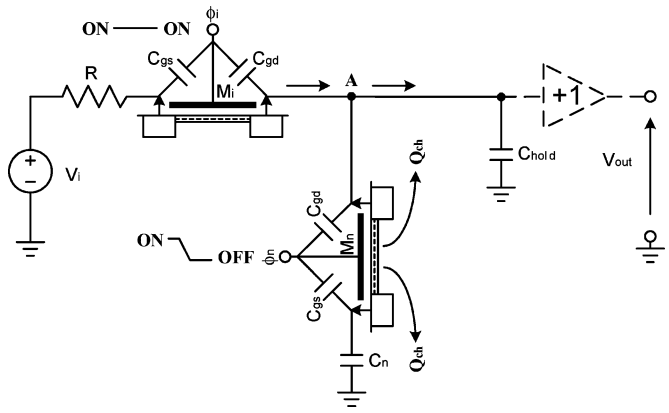

Fig. 4. Operation of INS during time interval τ_2.

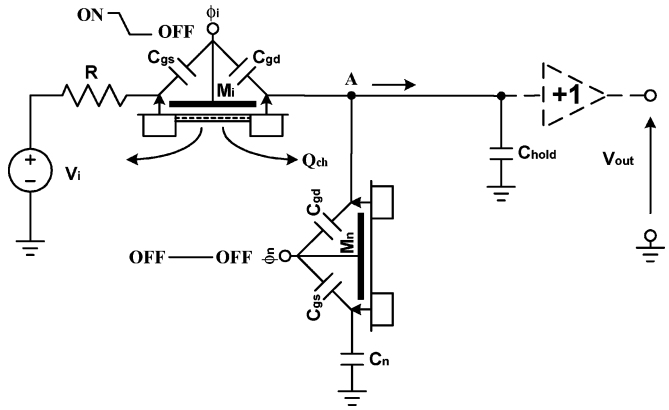

Fig. 5. Operation of INS during time interval τ_3 (injection phase).

$V_i\left(nT-T+\tau_1^-\right)$ input voltage sampled into the circuit during τ_1^-.

Upon entering τ_2, transited from the high supply voltage V_{DD} (ON) to the low supply voltage V_{SS} (OFF), ϕ_n switches off M_n (Fig. 4). The switch error charges from M_n are then injected into both C_n and node A. As the charges injected into node A are absorbed by the input source through the on-state M_i, they are not stored in C_{hold}. Hence, assuming that the input signal does not change between τ_1 and τ_2, at the end of τ_2, the respective charge in C_{hold} and C_n are

$$Q_{\text{hold}}\left(nT-T+\tau_1+\tau_2^-\right)=V_i\left(nT-T+\tau_1\right)C_{\text{hold}} \tag{7}$$

$$\begin{aligned}Q_n\left(nT-T+\tau_1+\tau_2^-\right)=&V_i\left(nT-T+\tau_1\right)C_n-\alpha_{n\_\tau 2}\text{WLC}_{OX}\\&\cdot\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]\\&-\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_n+C_p}C_n\end{aligned} \tag{8}$$

where $\alpha_{n\_\tau 2}$ is the fraction of M_n's channel charge stored in C_n during τ_2, and $[V_{DD}-V_i(nT-T+\tau_1)]$ is the V_{GS} of M_n before it is switched off. Note that, in (8), the quantity of charge in the second term and the third term are caused by the CI error and the CKFT error respectively.

Nonetheless, the source of errors in the output arises when M_i is being switched off by ϕ_i (Fig. 5) during τ_3 (the injection phase). At this point, due to the off-state M_n, instead of flowing to C_n, the error charges are either stored in C_{hold} or absorbed by the input source. This results in the following charge distributions:

$$\begin{aligned}&Q_n\left(nT-T+\tau_1+\tau_2+\tau_3^-\right)\\&=V_i\left(nT-T+\tau_1\right)C_n\\&\quad-\alpha_{n\_\tau 2}\text{WLC}_{OX}\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]\\&\quad-\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_n+C_p}C_n\end{aligned} \tag{9}$$

$$\begin{aligned}&Q_{\text{hold}}\left(nT-T+\tau_1+\tau_2+\tau_3^-\right)\\&\quad=V_i\left(nT-T+\tau_1\right)C_{\text{hold}}+\varepsilon_{\text{switch}}C_{\text{hold}}\end{aligned} \tag{10}$$

where $\varepsilon_{\text{switch}}$ is the well-known uncompensated switch error voltage defined by

$$\begin{aligned}\varepsilon_{\text{switch}}=&\frac{-\alpha_{i\_\tau 3}\text{WLC}_{OX}}{C_{\text{hold}}}\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]\\&-\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_{\text{hold}}+C_p}.\end{aligned} \tag{11}$$

Here, $\alpha_{i\_\tau 3}$ is the fraction of M_i's channel charge stored in C_{hold} during τ_3, and similarly, $[V_{DD}-V_i(nT-T+\tau_1)]$ is the V_{GS} of M_i before it is turned off.

The final phase τ_4 (the nulling phase) is the main emphasis of the whole operation because it is when the errors are minimized while generating an almost precise replica of the input signal to the output. The uniqueness of this phase lies in the turning-on of M_n. This produces the error-compensating CI and CKFT charges in view of the fact that electrons from C_{hold} and C_n are drawn into M_n to form the inverted channel (Fig. 6), whilst CKFT charges are generated in the reverse polarity (on both sides of M_n) by the positive transition of ϕ_n (from V_{SS} to V_{DD}). These two error-compensating charges counteract those error charges produced in τ_2 and τ_3. In other words, the charge distributions on the two capacitors at the end of the nulling phase are as follows:

$$\begin{aligned}&Q_{\text{hold}}\left(nT-T+\tau_1+\tau_2+\tau_3+\tau_4^-\right)\\&=V_i\left(nT-T+\tau_1\right)C_{\text{hold}}-\alpha_{i\_\tau 3}\text{WLC}_{OX}\\&\cdot\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]-\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_{\text{hold}}+C_p}C_{\text{hold}}\\&+\alpha_{n\_\tau 4}\text{WLC}_{OX}\left\{V_{DD}-\left[V_i\left(nT-T+\tau_1\right)+\varepsilon_{\text{switch}}\right]-V_T\right\}\\&+\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_{\text{hold}}+C_p}C_{\text{hold}}\end{aligned} \tag{12}$$

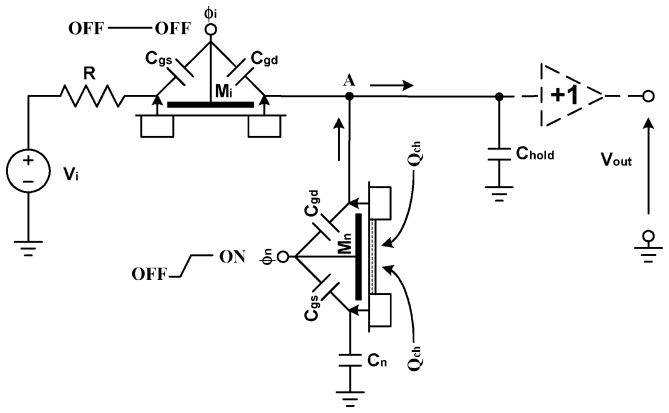

Fig. 6. Operation of INS during time interval τ_4 (nulling phase).

$$
\begin{aligned}
&Q_n\left(nT-T+\tau_1+\tau_2+\tau_3+\tau_4^-\right)\\
&=V_i\left(nT-T+\tau_1\right)C_n-\alpha_{n\_\tau 2}\mathrm{WLC}_{OX}\\
&\quad\cdot\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]-\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_n+C_p}C_n\\
&\quad+\left(1-\alpha_{n\_\tau 4}\right)\mathrm{WLC}_{OX}\\
&\quad\cdot\left\{V_{DD}-\left[V_i\left(nT-T+\tau_1\right)+\varepsilon_{\mathrm{switch}}\right]-V_T\right\}\\
&\quad+\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_n+C_p}C_n \qquad (13)
\end{aligned}
$$

where $\alpha_{n\_\tau 4}$ is the fraction of M_n's channel charges that has been drawn from C_{hold} during τ_4, and $\{V_{DD}-[V_i(nT-T+\tau_1)+\varepsilon_{\mathrm{switch}}]\}$ is the V_{GS} of M_n at the juncture when M_n is switched on.

So, summing the charges in C_{hold} (12) and C_n (13), and dividing the result by $(C_{\mathrm{hold}}+C_n)$, the output voltage of the S/H circuit is obtained as

$$V_{\mathrm{out}}\left(nT^-\right)=V_i\left(nT-T+\tau_1\right)+\varepsilon_{\mathrm{INS}}. \qquad (14)$$

Here, $T=(\tau_1+\tau_2+\tau_3+\tau_4)$, nT^- signifies the point of time just before entering the next sampling period, and $\varepsilon_{\mathrm{INS}}$ is the INS error voltage, which is given by

$$
\begin{aligned}
\varepsilon_{\mathrm{INS}}=&\frac{\mathrm{WLC}_{OX}}{C_{\mathrm{hold}}+C_n}\left[\frac{\left(V_{DD}-V_{SS}\right)C_p}{C_{\mathrm{hold}}+C_p}\right]\\
&+\left[1-\left(\alpha_{n\_\tau 2}+\alpha_{i\_\tau 3}\right)+\alpha_{i\_\tau 3}\frac{\mathrm{WLC}_{OX}}{C_{\mathrm{hold}}}\right]\\
&\cdot\frac{\mathrm{WLC}_{OX}}{C_{\mathrm{hold}}+C_n}\left[V_{DD}-V_i\left(nT-T+\tau_1\right)-V_T\right]. \qquad (15)
\end{aligned}
$$

Note that $(\mathrm{WLC}_{OX}/(C_{\mathrm{hold}}+C_n)) \ll 1$, $(\alpha_{i\_\tau 3}(\mathrm{WLC}_{OX}/C_{\mathrm{hold}})) \ll 1$ and $(\alpha_{n\_\tau 2}+\alpha_{i\_\tau 3}) \approx 1$ for fast clock transition.

Equation (15) reveals that the fundamental uncompensated switch error voltage $\varepsilon_{\mathrm{switch}}$ (11), arising from the injection phase, has been significantly reduced to $\varepsilon_{\mathrm{INS}}$. In this connection, observing the first term, the uncompensated CKFT error voltage $(V_{DD}-V_{SS})\,C_p/(C_{\mathrm{hold}}+C_p)$ is made very much smaller by the factor $(\mathrm{WLC}_{OX}/(C_{\mathrm{hold}}+C_n))$; for the typical values of $WL=1\ \mu\mathrm{m}^2$, $C_{OX}=2\ \mathrm{fF}/\mu\mathrm{m}^2$, $C_{\mathrm{hold}}=2\ \mathrm{pF}$, $C_p=1\ \mathrm{fF}$ and $(V_{DD}-V_{SS})=5\ \mathrm{V}$, the uncompensated error voltage of 2.5 mV has now reduced to 1.25 μV by the factor of 5×10^{-4}. Similarly, shown in the second term, the CI error is greatly minimized since $[1-(\alpha_{n\_\tau 2}+\alpha_{i\_\tau 3})]$ has value that approaches zero and $[\alpha_{i\_\tau 3}(\mathrm{WLC}_{OX}/C_{\mathrm{hold}})(\mathrm{WLC}_{OX}/(C_{\mathrm{hold}}+C_n))]$ is very small. It is worth mentioning that the benefit of having matching transistor characteristics, by utilizing two identically designed transistors, has resulted in this significant reduction of the switch errors. Incidentally, the INS error has a direct relationship with the area (WL) of the transistor. This means that the increase in the area will lead to a larger INS error. Therefore, it is desirable to choose a small switch.

IV. Nonideal Effects on the Injection-Nulling Switch

The previous derivation is further expanded to examine the impact of nonideal effects on the switch. It starts with the addition of junction capacitances followed by the mismatch of geometry and threshold voltages.

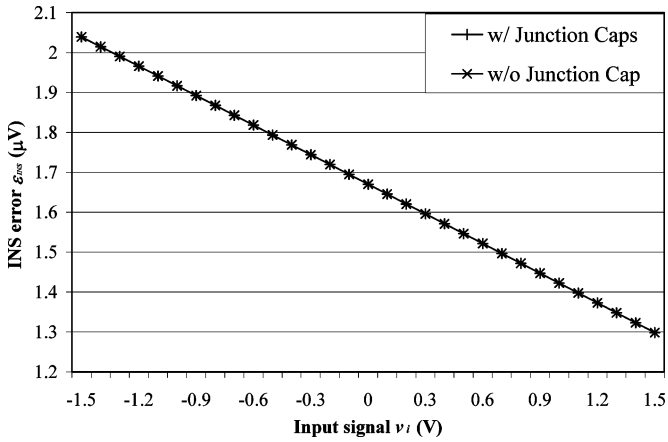

Fig. 7. Plot of INS error $\varepsilon_{\mathrm{INS}}$ against variation of input signal v_i.

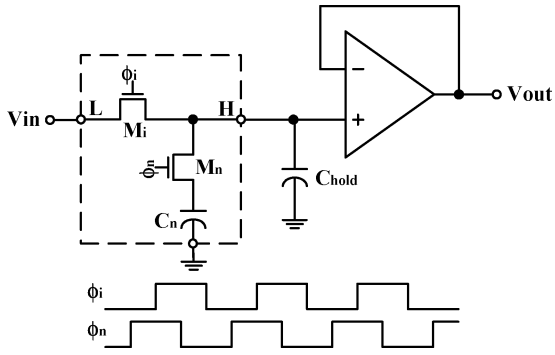

Fig. 8. S/H circuit using INS approach.

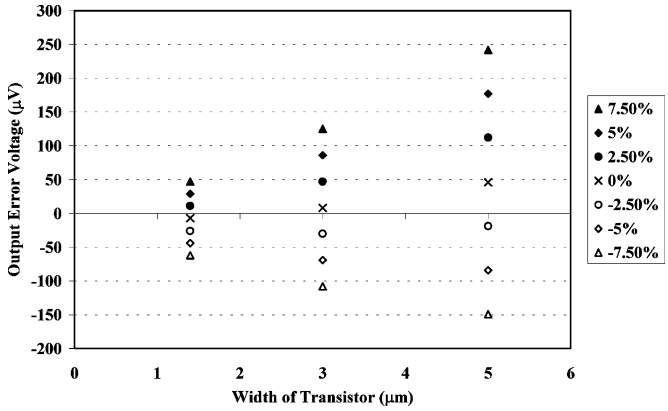

Fig. 9. Output error caused by the mismatch of geometry.

A. Junction Capacitances

Arising from the change in V_{DB} and V_{SB} at different sampling periods, the modulation of the depletion junction capacitances C_{SB} (source-bulk capacitance) and C_{DB} (drain-bulk capacitance) can produce nonlinearity error at the output. The degree of this influence is analyzed as follows. Since V_{DB} approximates to V_{SB} when a NMOS transistor is turned on, C_{DB} and C_{SB} are both represented by C_J

$$
\begin{aligned}
C_{DB}=C_{SB}=C_J&=C_{J0}\left(1+\frac{V_{SB}}{\Phi_0}\right)^{-1/2}\\
&=C_{J0}\left(1+\frac{v_i+V_Q-V_B}{\Phi_0}\right)^{-1/2} \qquad (16)
\end{aligned}
$$

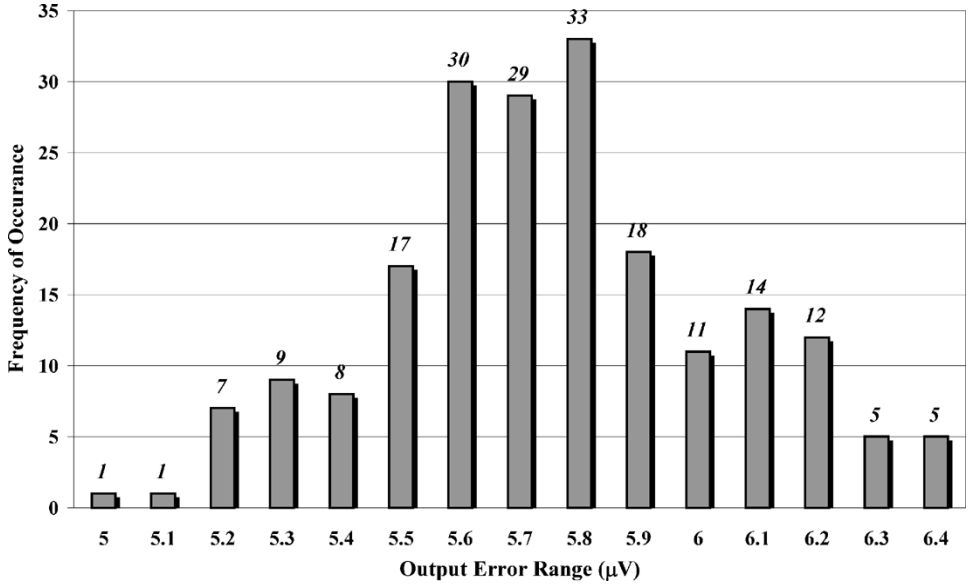

Fig. 10. Histogram of Monte Carlo simulation of output error caused by the variation in V_T (± 10 mV) for transistor with fixed aspect ratio of 2.8/0.6 μm.

where C_{J0} is the junction capacitance of C_J at zero V_{SB}, Φ_0 is the built-in voltage, V_Q and v_i represents the dc and the ac components of the input composite signal V_i, respectively, and V_B is the bulk voltage. By expanding (16) to yield

$$C_J = \sqrt{\frac{\Phi_0}{\Phi_0 + V_Q - V_B}} \cdot C_{J0}\left(1 - \frac{1}{2}x + \frac{3}{8}x^2 - \frac{5}{16}x^3 + \cdots\right), \qquad |x| < 1 \quad (17)$$

where $x = v_i/(\Phi_0 + V_Q - V_B)$, it shows that the root of the nonlinearity problem stems from C_J's signal-dependent terms. Now, to examine the effect of C_J on $\varepsilon_{\rm INS}$, C_J is added to (15). This increases $C_{\rm hold}$ to $(C_{\rm hold} + 2C_J)$ and C_n to $(C_n + C_J)$, causing a change from $\varepsilon_{\rm INS}$ to $\varepsilon_{\rm INS\_JC}$, which is given by

$$\varepsilon_{\rm INS\_JC} = \frac{{\rm WLC}_{OX}}{C_{\rm hold} + C_n + 3C_J}\left[\frac{(V_{DD} - V_{SS})C_p}{C_{\rm hold} + C_p + 2C_J}\right] + \left[1 - (\alpha_{n\_\tau 2} + \alpha_{i\_\tau 3}) + \alpha_{i\_\tau 3}\frac{{\rm WLC}_{OX}}{C_{\rm hold} + 2C_J}\right] \cdot \frac{{\rm WLC}_{OX}}{C_{\rm hold} + C_n + 3C_J}\left[V_{DD} - V_i(nT - T + \tau_1) - V_T\right]. \quad (18)$$

Further expanding (18) with the substitution of (17) and finally adding the result to (14), the output voltage is derived as

$$V_{\rm out} \cong V_i + \varepsilon_{\rm INS}\left(1 + a_0 + a_1 v_i + a_2 v_i^2\right) \quad (19)$$

where $a_0 = -b_1 + b_2$, $a_1 = (b_1 - 2b_2)/2(\Phi_0 + V_Q - V_B)$, $a_2 = (-3b_1 + 8b_2)/8(\Phi_0 + V_Q - V_B)^2$

$$b_1 = \frac{5C_{\rm hold} + 2C_n}{C_{\rm hold}(C_{\rm hold} + C_n)} C_{J0}\sqrt{\frac{\Phi_0}{\Phi_0 + V_Q - V_B}}$$

$$b_2 = \frac{(5C_{\rm hold} + 2C_n)^2 - 6C_{\rm hold}(C_{\rm hold} + C_n)}{\left[C_{\rm hold}(C_{\rm hold} + C_n)\right]^2} C_{J0}^2 \frac{\Phi_0}{\Phi_0 + V_Q - V_B}.$$

Equation (19) states that the junction capacitance has added a dc error (a_o), a linear error term ($a_1 v_i$) and a nonlinear error term ($a_2 v_i^2$) onto $\varepsilon_{\rm INS}$. To examine the intensity of this effect, with the following typical values: ${\rm WLC}_{OX} = 2$ fF, $C_{\rm hold} = C_n = 2$ pF, $C_p = 1$ fF, $V_{DD} = 5$ V, $V_Q = 2.5$ V, $V_B = V_{SS} = 0$ V, $V_T = 0.78$ V, $\Phi_0 = 1$ V, $C_{J0} = 6$ fF, and a range of -1.5 V to 1.5 V for v_i, (15) and (18) are plotted in Fig. 7. Because of the small coefficients ($a_0 = -5.59 \times 10^{-3}$, $a_1 = 7.95 \times 10^{-4}$ V^{-1} and $a_2 = -1.70 \times 10^{-4}$ V^{-2}), the two lines almost overlap each other. This shows C_J has little effect on the $\varepsilon_{\rm INS}$. Thus, it is concluded that the nonlinear effect of junction capacitance on the output signal is negligible.

B. Mismatch of Geometry and V_T

Since a mismatch of geometry will result in a difference in both the transistor area (WL) and the parasitic capacitance (C_p) between M_i and M_n, the area, the parasitic capacitance and the threshold voltage are separately denoted as $W_i L_i$, C_{pi} and V_{Ti} for M_i, and $M_n L_n$, C_{pn} and V_{Tn} for M_n. With that and following the similar steps in Section III, the effective INS error $\hat{\varepsilon}_{\rm INS}$ (inclusion of mismatching factors) is derived as

$$\begin{aligned}\hat{\varepsilon}_{\rm INS} = {} & \frac{-\alpha_{i\_\tau 3} W_i L_i C_{OX}}{C_{\rm hold} + C_n}\left[V_{DD} - V_i(nT - T + \tau_1) - V_{Ti}\right] \\ & - \left(\frac{C_{\rm hold}}{C_{\rm hold} + C_n}\right)\frac{(V_{DD} - V_{SS})C_{pi}}{C_{\rm hold} + C_{pi}} \\ & + \frac{\alpha_{n\_\tau 4} W_n L_n C_{OX}}{C_{\rm hold} + C_n} \\ & \cdot \left\{V_{DD} - \left[V_i(nT - T + \tau_1) + \varepsilon_{\rm switch}\right] - V_{Tn}\right\} \\ & + \left(\frac{C_{\rm hold}}{C_{\rm hold} + C_n}\right)\frac{(V_{DD} - V_{SS})C_{pn}}{C_{\rm hold} + C_{pn}} \\ & + \frac{-\alpha_{n\_\tau 2} W_n L_n C_{OX}}{C_{old} + C_n}\left[V_{DD} - V_i(nT - T + \tau_1) - V_{Tn}\right] \\ & - \left(\frac{C_n}{C_{\rm hold} + C_n}\right)\frac{(V_{DD} - V_{SS})C_{pn}}{C_{\rm hold} + C_{pn}} \\ & + \frac{(1 - \alpha_{n\_\tau 4}) W_n L_n C_{OX}}{C_{\rm hold} + C_n} \\ & \cdot \left\{V_{DD} - \left[V_i(nT - T + \tau_1) + \varepsilon_{\rm switch}\right] - V_{Tn}\right\} \\ & + \left(\frac{C_n}{C_{\rm hold} + C_n}\right)\frac{(V_{DD} - V_{SS})C_{pn}}{C_{\rm hold} + C_{pn}}. \end{aligned} \quad (20)$$

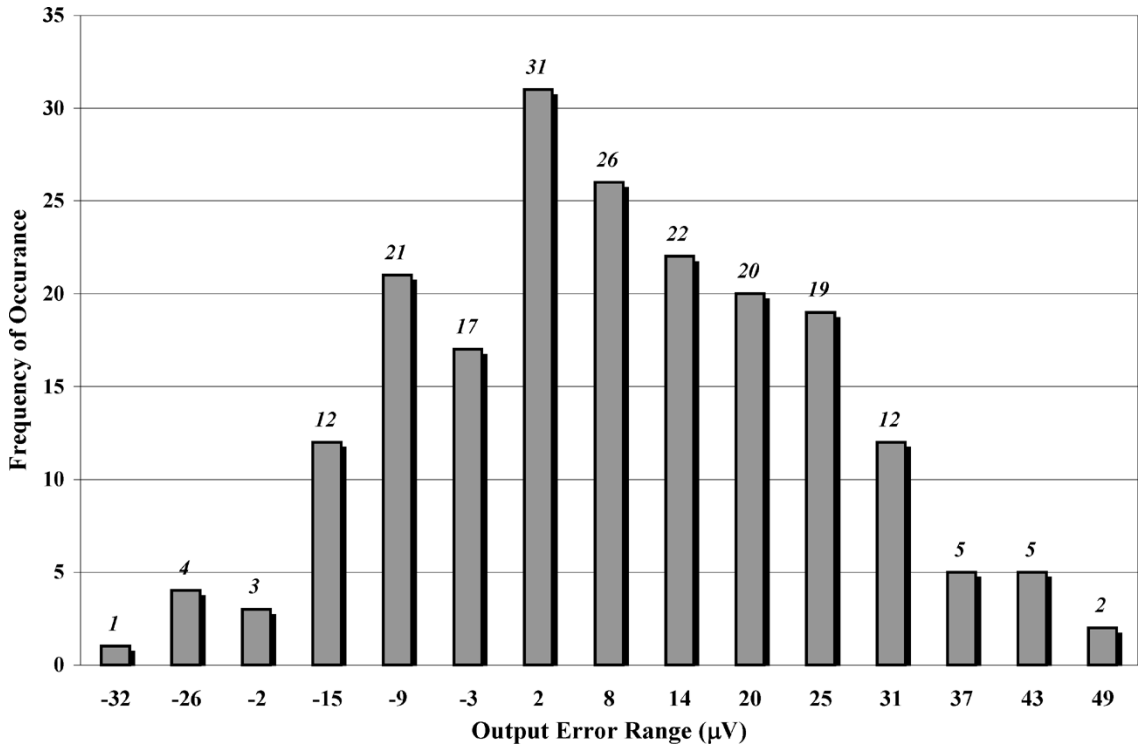

Fig. 11. Histogram of Monte Carlo simulation of output error caused by the variation in WL ($\pm 5\%$), variation in V_T (± 10 mV) and variation in t_{ox} ($\pm 1\%$).

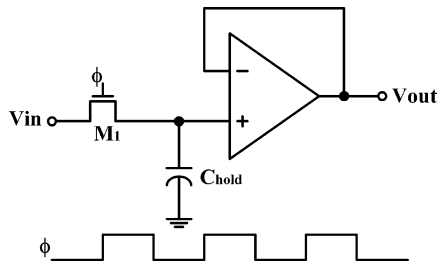

Fig. 12. S/H circuit using SS as switch.

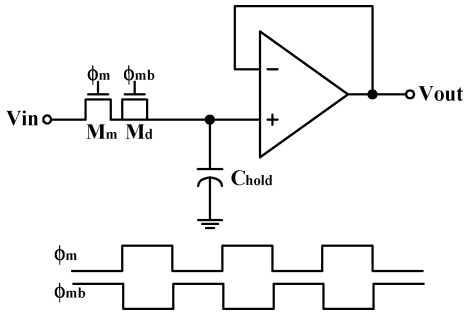

Fig. 13. S/H circuit using DS approach.

To simplify this, all the values of M_n's parameters are expressed in terms of that of M_i's, that is, $W_nL_n = W_iL_i(1+\Delta W_iL_i/W_iL_i)$, $C_{pn} = C_{pi}(1+\Delta C_{pi}/C_{pi})$, and $V_{Tn} = V_{Ti}(1+\Delta V_{Ti}/V_{Ti})$ where the terms $\Delta W_iL_i/W_iL_i$, $\Delta C_{pi}/C_{pi}$ and $\Delta V_{Ti}/V_{Ti}$ represent the fractional change of W_iL_i, C_{pi} and V_{Ti} respectively. Thus, by substituting them into (20), it yields

$$\hat{\varepsilon}_{\mathrm{INS}} \cong \varepsilon_{\mathrm{INS}} + \varepsilon_{\mathrm{INS\_\Delta WL}} + \varepsilon_{\mathrm{INS\_\Delta C_p}} + \varepsilon_{\mathrm{INS\_\Delta V_T}} \quad (21)$$

where $\varepsilon_{\mathrm{INS}}$ has been defined in (15)

$$\varepsilon_{\mathrm{INS\_\Delta WL}} = \left(\frac{\Delta W_iL_i}{W_iL_i}\right)\varepsilon_{\mathrm{INS}} + \alpha_{i\_\tau 3}\left(\frac{\Delta W_iL_i}{W_iL_i}\right) \cdot \frac{W_iL_iC_{ox}}{C_{\mathrm{hold}}+C_n}[V_{DD}-V_i(nT-T+\tau_1)-V_{Ti}] \quad (22)$$

$$\varepsilon_{\mathrm{INS\_\Delta C_p}} = \left\{\frac{C_{\mathrm{hold}}+C_{pi}}{C_{\mathrm{hold}}+C_{pi}\left(1+\frac{\Delta C_{pi}}{C_{pi}}\right)}\left(\frac{C_{\mathrm{hold}}}{C_{\mathrm{hold}}+C_n}\right)\left(\frac{\Delta C_{pi}}{C_{pi}}\right)\right\} \cdot \left[\frac{(V_{DD}-V_{SS})C_{pi}}{C_{\mathrm{hold}}+C_{pi}}\right] \quad (23)$$

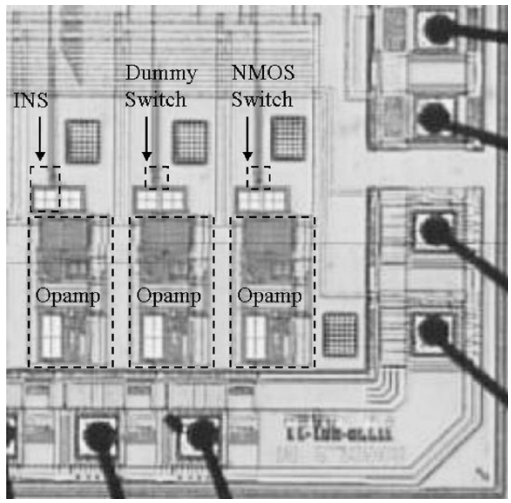

Fig. 14. Microphotograph of the S/H circuits using SS, DS, and INS.

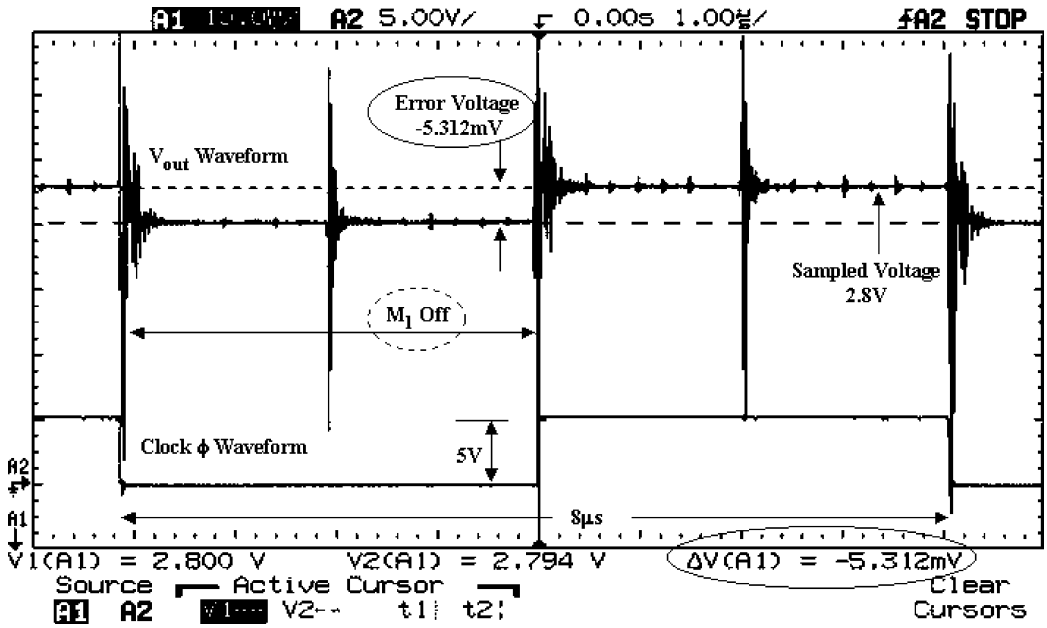

Fig. 15. Measured time domain response of S/H circuit using SS.

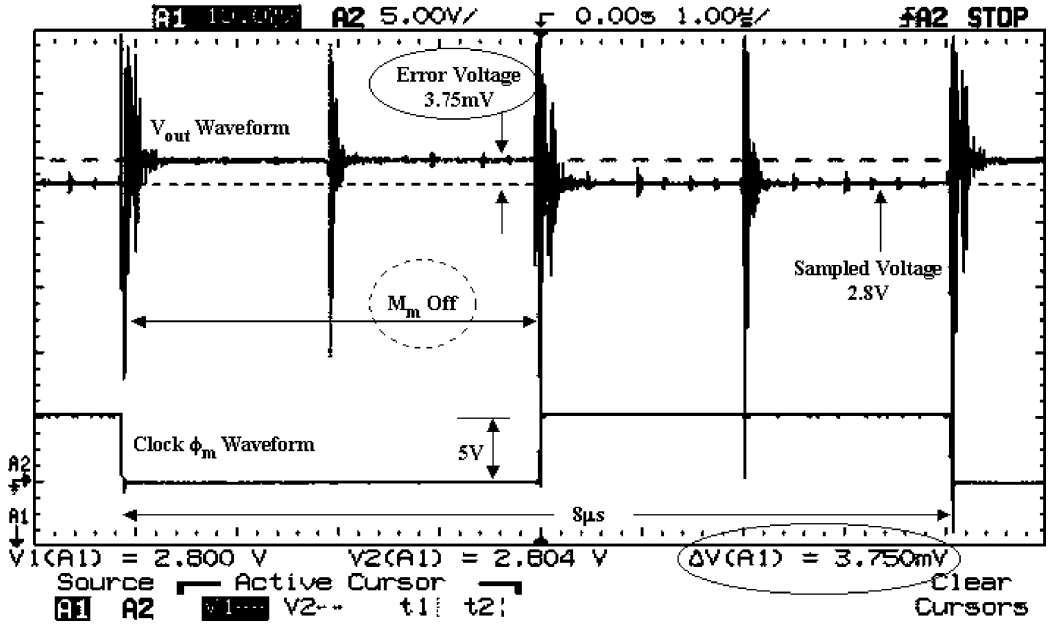

Fig. 16. Measured time domain response of S/H circuit using DS.

$$\varepsilon_{\mathrm{INS\_\Delta V_T}} = -(1-\alpha_{i\_\tau 2})\left(1+\frac{\Delta W_i L_i}{W_i L_i}\right)\frac{W_i L_i C_{ox}}{C_{\mathrm{hold}}+C_n}\Delta V_{Ti}. \tag{24}$$

In (21), the first error $\varepsilon_{\mathrm{INS}}$ (15) is typically less than 1% of the uncompensated switch error $\varepsilon_{\mathrm{switch}}$ (11). Having a factor of $\Delta W_i L_i / W_i L_i$, the second error $\varepsilon_{\mathrm{INS\_\Delta WL}}$ (22) can possess a value of a few percent of the CI error voltage because of its second term. Since the third error $\varepsilon_{\mathrm{INS\_\Delta C_p}}$ (23) relates to the CKFT error, for the case $\Delta C_{pi}/C_{pi}$ of 5%, it can reach a few percentage of the $(V_{DD}-V_{SS})\,C_{pi}/(C_{\mathrm{hold}}+C_{pi})$. To take a closer look at the effects of these errors, by fixing a nominal M_i's width while varying that of M_n's from $-$ 7.5% to 7.5% (in steps of $\pm 2.5\%$) of the nominal, the HSPICE simulation was performed using the circuit in Fig. 8. It was then repeated for several nominal widths of M_i (1.4, 3, and 5 μm) to plot the overall error trend in order to find the optimal size of M_i and M_n that would give the minimum output error. Note that the length of transistors was both 0.6 μm (minimum allowable limit). From Fig. 9, which shows the results of the output error voltages against different nominal widths, a few points can be noted. First, for each nominal width (reading points vertically), the magnitude of the error gets larger with the increase of the mismatching factor. Moreover, comparing each width (across horizontal points), this increment becomes more significant in larger width. Hence, this validates $\varepsilon_{\mathrm{INS\_\Delta WL}}$ and $\varepsilon_{\mathrm{INS\_\Delta C_p}}$. Second, on the basis that small transistors exhibit a higher mismatching factor than the larger ones, the comparison of the error voltage of 7.5% in the small switch ($W_i = 1.4$ μm), 2.5% in the medium switch ($W_i = 3$ μm) and 0% in the large switch

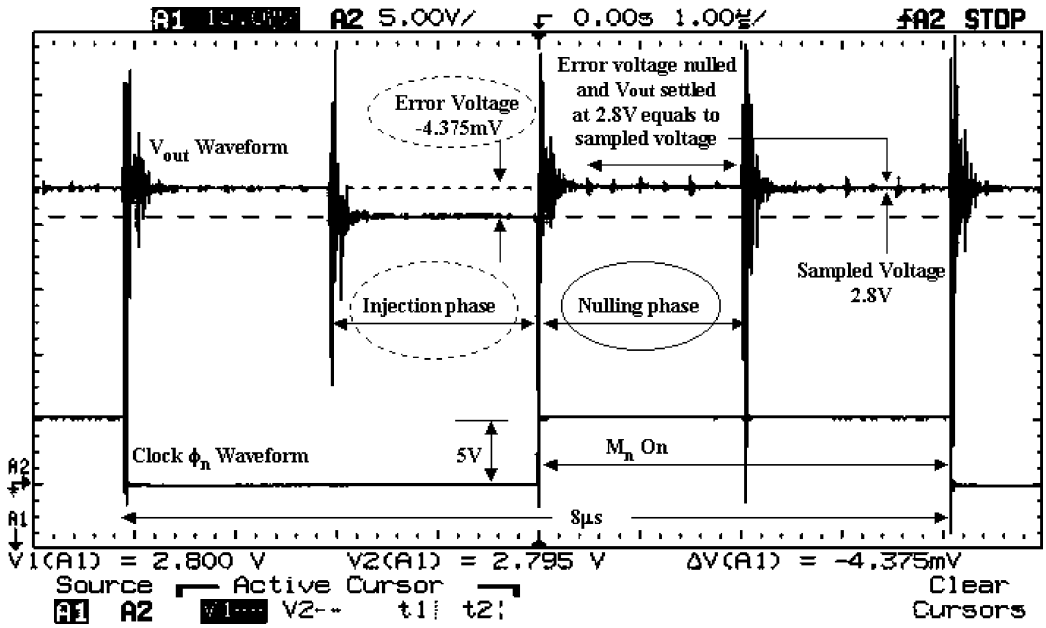

Fig. 17. Measured time domain response of S/H circuit using INS.

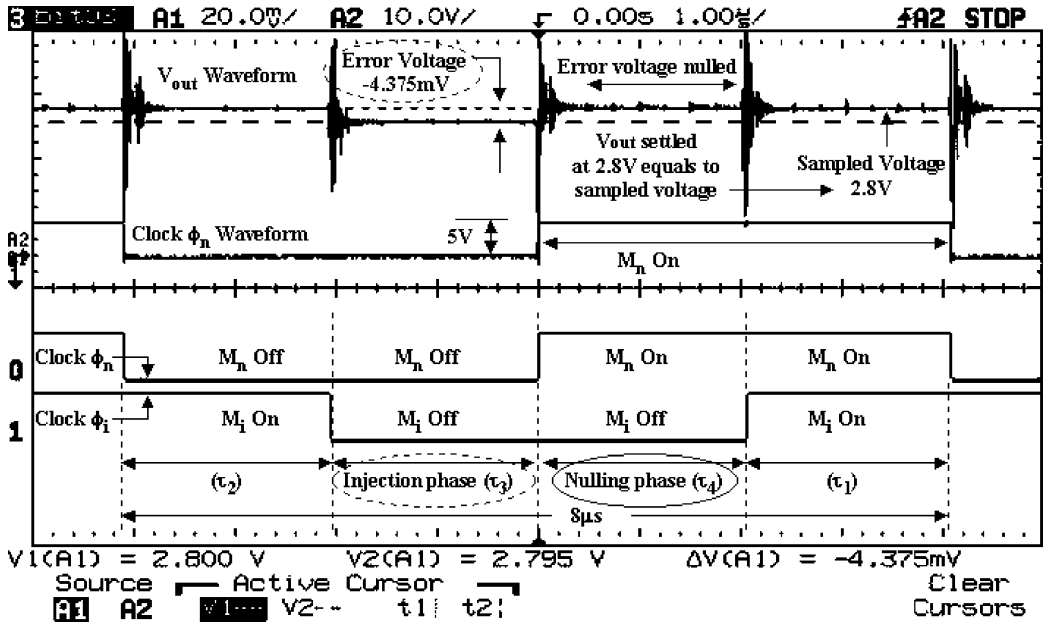

Fig. 18. Measured time domain response of Fig. 17 with detailed clock sequence.

($W_i = 5\,\mu$m) is performed. It is found that they are quite similar. This shows that there is no apparent minimum point for output error voltage, leading to the conclusion that the recommended optimal size for the transistors is the minimum size. Thirdly, the simulation results have also verified that $\varepsilon_{\rm INS}$ (0% mismatch) is small, but it increases with the switch size. This is consistent with the observation in (15).

Regarding V_T mismatch, from the fourth error voltage $\varepsilon_{\rm INS\_\Delta V_T}$ (24), it can be observed that the effect of this error is not as significant as those of $\varepsilon_{\rm INS\_\Delta WL}$ and $\varepsilon_{\rm INS\_\Delta C_p}$ because ΔV_{Ti} is minimized by the factor $\{(1-\alpha_{i\_\tau 2})\,W_iL_iC_{ox}/(C_{\rm hold}+C_n)\}$; even though there is a direct relationship of geometry mismatch shown in the factor $(1+\Delta W_iL_i/W_iL_i)$, the contribution is small. To verify this observation, Monte Carlo simulation of 200 samples was performed on both transistors having a maximum ± 10 mV random variation in their V_T. Note that for comparing DS technique experimentally (in the next section), the aspect ratio of M_i and M_n were both fixed at 2.8/0.6 μm because the dummy transistor has taken the minimum size ($W_i = 1.4\ \mu$m, $L_i = 0.6\ \mu$m). The results from the simulation are presented in the form of a histogram (see Fig. 10). A mean of 5.7188 μV and a standard deviation of 0.2852 μV are obtained. As the standard deviation is very small, it correlates well with $\varepsilon_{\rm INS\_\Delta V_T}$ (24) for having small error contribution.

To evaluate the robustness of the INS scheme in a manufacturing prospective, Monte Carlo simulation of 200 samples was run. The selected parameters were: a $\pm 5\%$ random variation in

TABLE I
ERROR VOLTAGE RESULTS OF THE THREE S/H CIRCUITS

Compensation Method	From Figure	Error Voltage Magnitude
Single NMOS switch	15	5.312 mV
Dummy switch	16	3.75 mV
Injection-nulling switch	17, 18	Less than 25μV (Cursor resolution limit)

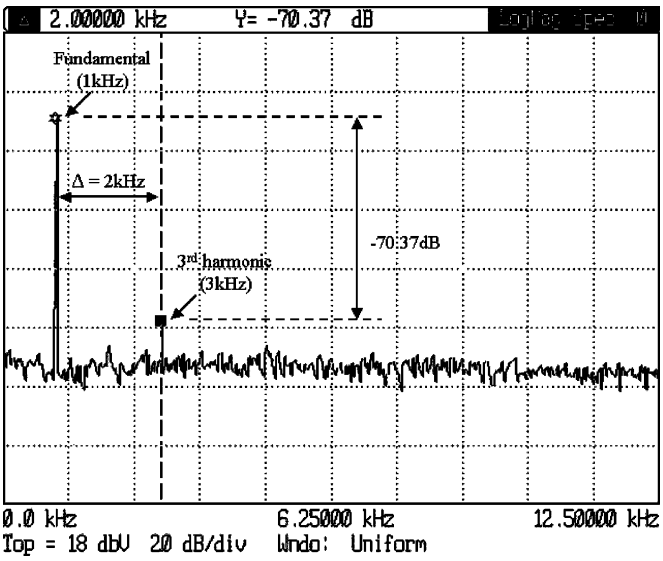

Fig. 19. Measured spectral harmonic distortion of the S/H circuit in Fig. 12 using SS.

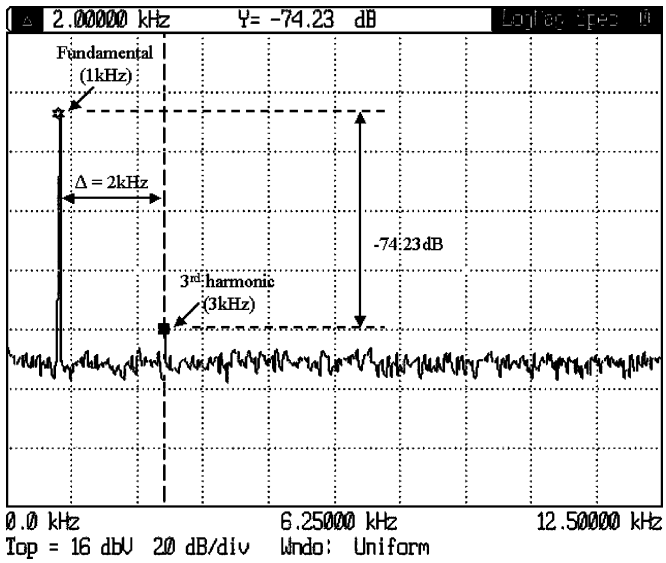

Fig. 20. Measured spectral harmonic distortion of the S/H circuit in Fig. 13 using DS.

transistors' width from 2.8 μm, a ± 10 mV random variation in V_T and a $\pm 1\%$ in t_{ox} (thickness of gate oxide). Fig. 11 displays the histogram of the results. The mean and standard deviation of the distribution are 5.9953 and 16.7036 μV, respectively. Statistically, these results show that the output error voltage of the fabricated S/H circuit (Fig. 7) will range from a few μV to tens of μV, in other words, less than 10% of $\varepsilon_{\text{switch}}$.

Although the mismatch error of M_i and M_n poses some constraints on the INS technique, it is kept small since the two transistors are designed to be identical to each other. Compared to the matching transistors of different sizes, the task of matching two identically designed transistors is easier. Besides, the two transistors will also have much better matching characteristics. Therefore, using this scheme, the switch error due to the mismatch error of transistors can be also kept to the minimum.

V. EXPERIMENTAL RESULTS AND PERFORMANCE COMPARISON

To verify the effectiveness of the proposed technique, a comparison with the conventional switch topologies, the single NMOS switch (SS) and the DS, was performed using the basic S/H circuit implementation. Shown in Fig. 12 (SS), Fig. 13 (DS) and Fig. 8 (INS), each circuit consists of a holding capacitor C_{hold}, a folded-cascode noninverting opamp with high-swing current mirrors, and its own switch element. The driving clock signal for the switches are also displayed. With the following values: $C_n = C_{\text{hold}} = 2$ pF, W/L ratio of $\text{M}_\text{d} = 1.4/0.6$ μm, and that of M_1, M_m, M_i, and $M_n = 2.8/0.6$ μm, all three circuits were fabricated on the same test chip using AMS (Austria Mikro Systeme International AG) 0.6 μm n-well CMOS process. The microphotograph is shown in Fig. 14.

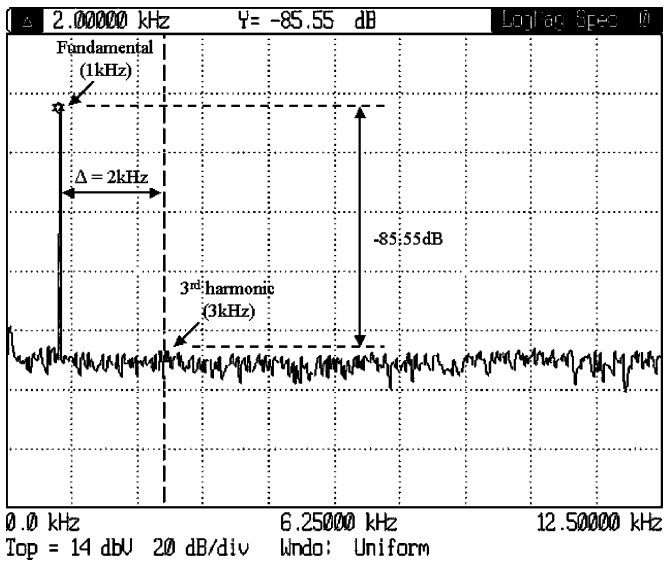

Fig. 21. Measured spectral harmonic distortion of the S/H circuit in Fig. 8 using INS.

Two types of measurement were taken on the chip. These are the time domain for comparing the effectiveness of switch error minimization, and the frequency domain to support the former on the reduction of signal-dependent CI error since high CI error can lead to the existence of some higher-order harmonics. The respective measurement instruments being employed were an oscilloscope (HP 54 645D MegaZoom Mixed-Signal oscilloscope) with a cursor measurement resolution of 25 μV and an

TABLE II
COMPARISON OF THD OF THE COMPENSATION METHODS ON S/H CIRCUITS

Compensation Method	Technology	Sampling Frequency	THD
Single NMOS switch	0.6 μm	125 kHz	- 68 dB
Dummy switch	0.6 μm	125 kHz	- 74 dB
Injection-nulling switch	0.6 μm	125 kHz	- 85 dB

analyzer (Stanford Research Systems Model SR770 FFT Network Analyzer) with a low distortion output source. A DC input voltage calibrated to compensate for the opamp's offset was used for the time domain measurement to produce an output voltage ($V_{\rm out}$) of 2.8 V. This value is chosen to prevent any voltage swing or common-mode issues arising from the noninverting opamp. As for the frequency domain measurement, the input was a 1 kHz, 1 $V_{\rm pk}$ AC signal coming from the analyzer output source. The circuits were operating on a 5 V supply, and the clock signals were running on 125 kHz from an on-chip 1-MHz divided digital ring oscillator. A discussion for each measurement is as follows.

First of all, Figs. 15–17 show the time domain $V_{\rm out}$ waveforms and the clock signals of Figs. 12, 13, and 8, respectively. Note that although some spikes may appear along the $V_{\rm out}$ waveform due to the switching noise originating from the multistage divider circuits, their effects are not of concern because from observation, the output voltage was able to recover from them within a short time. The error voltage of SS (Fig. 15) and DS (Fig. 16) are highlighted in the circle. Basically, SS presents the common switch error voltage, which is -5.312 mV, while 3.75 mV error in DS was caused by the mismatch transistor characteristics between the main and dummy transistors. Unlike the two, the actual INS error in Fig. 17 should be read from the nulling phase instead of the "error voltage" in the injection phase. Displaying the same waveform but with the addition of the clocking signals, Fig. 18 presents a finer illustration of the INS technique. In particular, when M_n is turned on again in the nulling phase, the -4.375 mV switch error (in the injection phase) was substantially reduced, resulting in an output voltage that appeared to be the same as the required 2.8 V in τ_1. Table I summarizes the above-mentioned error magnitude. In brief, it shows that the INS technique does have a definite edge over its counterparts in terms of minimization of switch errors.

Next, Figs. 19–21 show the respective frequency spectrum of $V_{\rm out}$. For the case of SS (Fig. 19), the third harmonic component was -70.37 dB below the fundamental component and the THD was measured at -68 dB. For DS, (Fig. 20), it was -74.23 and -74 dB, respectively. For INS (Fig. 21), however, the respective results of -85.55 and -85 dB were obtained. All these are summarized in Table II. The results have again supported the fact that INS performs better in the reduction of CI error.

VI. CONCLUSION

A new circuit technique using the INS for minimizing both the CI error and the CKFT error has been presented. A series of analyses including the INS operation, the INS switch error and the nonideal effects on the INS have been discussed. From the analyses and the simulation results, the INS error has been verified to be small, and insensitive to the junction capacitance effect. Moreover, the dominant geometrical mismatch effect is minimized through the use of two identically designed transistors. Comparative experimental results have validated the effectiveness of INS over other conventional switch techniques. Not only does the proposed technique support monolithic circuits, it is also applicable to discrete component implementations since discrete IC's with identically designed switches are readily available. Besides, it can also be modified to have two branches of the NMOS switch and a capacitor if compensation is needed on both sides of M_i. Finally, the flexibility and the effectiveness of the INS technique will be useful for signal-conditioning building blocks and interfaces in both analog and mixed-signal signal-processing applications.

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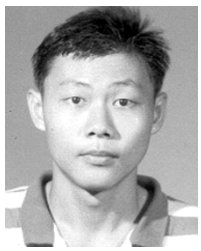

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