Record-low contact resistance for InAlN/AlN/GaN High Electron Mobility Transistors on Si with non-gold metal

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We have demonstrated 0.17-μm gate-length $In_{0.17}Al_{0.83}N$/GaN high-electron-mobility transistors (HEMTs) on Si (111) substrates using a non-gold metal stack (Ta/Si/Ti/Al/Ni/Ta) with a record-low ohmic contact resistance (R_c) of 0.36 Ω-mm. This contact resistance is comparable to the conventional gold-based (Ti/Al/Ni/Au) ohmic contact resistance (R_c = 0.33 Ω-mm). A non-gold ohmic contact exhibited a smooth surface morphology with a root mean square surface roughness of ~2.1 nm (scan area of 5×5 μm^2). The HEMTs exhibited a maximum drain current density of 1110 mA/mm, a maximum extrinsic transconductance of 353 mS/mm, a unity current gain cutoff frequency of 48 GHz, and a maximum oscillation frequency of 66 GHz. These devices exhibited a very small (<8%) drain current collapse for the quiescent biases (V_{gs0} = -5 V, V_{ds0} = 10 V) with a pulse width/period of 200 ns/1 ms. These results demonstrate the feasibility of using a non-gold metal stack as a low R_c ohmic contact for the realization of high-frequency operating InAlN/AlN/GaN HEMTs on Si substrates without using recess etching and regrowth processes.

1. Introduction

InAlN/GaN high-electron-mobility transistors (HEMTs) have great advantages over conventional AlGaN/GaN HEMTs owing to their larger band gap discontinuity ($\Delta E_c \sim 0.68$ eV)[1], which results in a 2 – 3-times higher two-dimensional electron gas (2DEG) density in the order of ~ 2.73×10^{13} cm^{-2} and in current densities of more than 2 A/mm at room temperature and 3 A/mm at 77 K[2] . Such devices emerged as a high-power HEMT technology[3]. Moreover, AlGaN/GaN HEMTs also exhibit strain induced reliability issues owing to the large (~ 18%) lattice mismatch between the AlGaN barrier and the GaN buffer layer[1]. A lattice-matched $In_xAl_{1-x}N$/GaN HEMT (x~0.17) mitigates strain-induced reliability owing to the absence of piezoelectric polarization which helps to improve overall device characteristics. By inserting a thin layer of AlN between the InAlN barrier layer and the GaN active buffer layer, alloy disorder scattering is significantly reduced, which in turn enhances the transport properties of the channel[4]. The optimized heterostructure with gate-length scaling and an efficient process technique can provide improved DC and RF performance characteristics. There are few reports on high f_T in InAlN/AlN/GaN HEMTs on SiC[5,6] and sapphire[7,8] substrates. Recently, Yue et al. [9] have achieved a very high f_T/f_{max} of 400/33 GHz with a 30-nm-gate-length InAlN/AlN/GaN HEMT on a SiC substrate using conventional Au-based ohmic contacts with regrown n^+-GaN. However, very few reports[10-13] on InAlN/AlN/GaN HEMTs fabricated on Si substrates are available. Furthermore, most frequently reported InAlN/AlN/GaN HEMTs were fabricated using conventional III–V Au-based ohmic metal stacks that were not compatible with the existing Si process line. Hence, non-gold ohmic contacts with low contact resistance (R_c) are essential for InAlN/AlN/GaN HEMTs to be manufacturable in the matured Si process line. Table I shows some of the best reported R_c values for non-gold ohmic contacts for InAlN/AlN/GaN HEMTs[14-17]. Few researchers have utilized non-gold ohmic metal stacks {Ti/Al/Ni/W[14], Hf/Al/Ta[15], Ta/Al/Ta[16]} to demonstrate a low R_c for InAlN/AlN/GaN HEMTs.

Alomari et al. realized first a very high R_c of 1.6 Ω-mm on InAlN/AlN/GaN HEMTs on sapphire substrates by using a non-gold {Ti/Al/Ni plus Ta/Cu/Ta} ohmic metal[17]. Malmros et al. have reported R_c = 0.64 Ω-mm obtained using a Ta/Al/Ta metal stack on InAlN/AlN/GaN HEMTs on SiC substrate by annealing at 550 ºC[16]. Recently, Tripathy et al. have reported an R_c of 0.56 Ω-mm in an InAlN/AlN/GaN HEMT structure on a 200-mm–diameter Si substrate obtained by annealing at 900 ºC for 60 s[14]. More recently, we have proposed and demonstrated a non-gold ohmic metal scheme using Ta with a thin layer of Si for AlGaN/GaN HEMTs on Si substrates[18]. In this work, we have achieved a record-low R_c of 0.36 ±0.03 Ω-mm in InAlN/AlN/GaN HEMTs on Si substrates using a work-function-engineered "Ta/Si"–based non-gold metal stack. In addition, we report DC and microwave characteristics of 0.17-µm-gate InAlN/AlN/GaN HEMTs on Si substrates with low (~8%) drain current collapse.

2. Experimental methods

The GaN HEMT structure was grown by metal–organic chemical vapor deposition (MOCVD) with a 9-nm-thick $In_{0.17}Al_{0.83}N$ barrier, an ~1-nm-thick AlN spacer layer, an ~1000-nm-thick i-GaN buffer layer and an ~100-nm-thick nucleation layer on a high-resistivity Si (111) substrate [see Fig. 1(a)]. The grown structure exhibited a room-temperature 2-DEG mobility of ~796 cm^2/V.s, an average sheet resistance of ~381 Ω/□, and a sheet carrier density of 2.06 × 10^{13} cm^{-2}. After mesa isolation by dry etching using BCl_3/Cl_2 plasma, a Ta/Si/Ti/Al/Ni/Ta (5/5/20/120/40/30 nm) ohmic metal was deposited and annealed at 825 ºC for 30 s in a N_2 environment with a rapid thermal annealing (RTA) system. Figure 1 shows the optical microscope images of (b) non-gold ohmic and (c) conventional gold ohmic contacts on InAlN/AlN/GaN HEMTs. The non-gold ohmic metal stack exhibits a smooth surface morphology with good edge definition, which is similar to our previous work on AlGaN/GaN HEMTs on Si substrates[18]. The non-gold ohmic contact exhibits a smooth

surface morphology with an RMS surface roughness of ~2.1 nm (AFM scan area = 5×5 μm^2) which is better than that (20-160 nm) of conventional ohmic contacts (Ti/Al/Ni/Au) (20/120/40/50 nm) on AlGaN/GaN HEMTs. Other research groups have also observed similar RMS roughness ranges[19-23]. A 0.17 μm Schottky T-gate foot print with a 0.5 μm gate-head was formed with a metal stack of Ni/Au (150/400 nm) using electron beam evaporation. Figure 1(d) shows the cross-sectional high resolution transmission electron microscopy (HR-TEM) image of the T-gate formed on InAlN/AlN/GaN HEMTs. Subsequently, a non-gold Ti/Al/Ta (50/800/30 nm) metal stack was also formed as an interconnect metal. Finally, the devices were passivated with 120-nm-thick PECVD-grown SiN at 300 ºC. The device dimensions used for this study are $L_{sg}/L_g/L_{gd}/W_g$ = 0.8/0.17/1.7/(2×75) μm. On-wafer DC and pulsed *I–V* characteristics of the HEMTs were measured using an Agilent B1500 semiconductor parameter analyzer and an Accent Diva D265, respectively. Microwave small-signal measurements were also carried out using an HP 8510c vector network analyzer (VNA). To study the interface properties of metal-semiconductor contacts, HR-TEM and energy-dispersive X-ray (EDX) were also carried out and analyzed.

3. Results and discussion

Figure 2(a) shows the current-voltage characteristics of non-gold (Ta/Si/Ti/Al/Ni/Ta) and gold ohmic contacts for InAlN/AlN/GaN HEMTs on Si substrates. Figures 2(b) and 2(c) show the total resistance versus transfer length model (TLM) gap (5 to 80 μm) characteristics of non-gold and gold ohmic contacts, measured across five locations {Centre (C), Top (T), Bottom (B), Left (L), Right (R)} of the 2-inch wafer [see inset of Fig. 2(a)]. The conventional gold ohmic contact the (Ti/Al/Ni/Au) on the InAlN/AlN/GaN HEMT structure exhibited an average R_c as low as 0.33 ±0.02 Ω-mm and an average specific contact resistivity (ρ_c) of 3.27x10^{-6} Ω-cm^2. The non-gold ohmic contacts exhibited an average R_c as low as 0.36 ± 0.03 Ω-mm with a ρ_c of 4.47x10^{-6} Ω-cm^2, which is

comparable to that of the gold-based ohmic contacts. Table II shows the best reported R_c values of conventional gold ohmic contacts for InAlN/AlN/GaN HEMTs on Si and SiC substrates[9-12, 24-27]. Thus far, the lowest R_c values of 0.15[25,26] and 0.16 Ω-mm[9] were obtained using $SiCl_4$ recess etching and regrown n^+-GaN on InAlN/AlN/GaN HEMT structures, respectively, on SiC substrates. We have also achieved low R_c values in AlGaN/AlN/GaN HEMTs by an optimized ohmic-recess etching process[28]. However, these techniques are more complex than our ohmic process reported in this work, which will facilitate the high-volume manufacturing process. Figure 3 shows the cross-sectional (a) HR-TEM image, (b) zoomed EDX area mapping, (c) EDX line scan and (d) zoomed EDX line scan of the annealed non-gold ohmic contact on the InAlN/AlN/GaN HEMT structure. From the results of qualitative EDX analysis, the observed of low R_c is possibly due to the formation of a mixture of Ta_xSi_y and Ti_xSi_y at the interface of metal-semiconductor contacts. Further investigation is required to determine the exact metal alloy at the interface. Recently, we have also realized a low R_c by the intermixing of the Ti_xSi_y alloy in the Ta layer on the AlGaN/GaN HEMT structure with a similar non-gold metal stack[29]. The achieved R_c is believed to be the lowest ever reported for non-gold ohmic contacts on InAlN/AlN/GaN HEMTs on Si substrates and is about 56% lower than that of Ta-based non-gold ohmic contacts (R_c=0.64 Ω-mm) on InAlN/AlN/GaN HEMTs on SiC substrates[16]. Figure 4(a) shows the two-terminal Schottky gate current-voltage characteristics of InAlN/AlN/GaN HEMTs. The reverse gate leakage current of the device measured at V_G = -15 V was 1.47×10^{-2} mA/mm, which is typical for the Ni/Au Schottky gate for InAlN/AlN/GaN HEMTs[12,13,25]. The device exhibited a Schottky barrier height (ϕ_B) of 0.81 eV with an ideality factor (n) of 1.38. Figure 4(b) shows the *C-V* characteristics of the Ni/Au Schottky diodes, measured at 1 MHz. The threshold voltage (V_{th}) of the Schottky diodes from the *C-V* curve is the -2.6 V, which is in agreement with the V_{th} value obtained from the device transfer characteristics. The observed very small hysteresis in the C-V characteristics is believed to be due to the existence of a negligible number of interface traps between Ni and InAlN layers.

Figure 5 shows the typical (a) I_{DS}–V_{DS} and (b) transfer characteristics of 0.17-μm-gate InAlN/AlN/GaN HEMTs on Si substrates. The fabricated HEMTs exhibited a maximum drain current density (I_{Dmax}) of 1110 mA/mm and a maximum extrinsic transconductance (g_{mmax}) of 353 mS/mm with good channel pinch-off. The achieved I_{Dmax} is close to the reported 1170 mA/mm, however it is obtained with a small gate length of 50 nm with a small source-drain distance of 1.0 μm[16]. Moreover, the devices suffer from the short channel effect with high output conductance beyond V_D = 4V. Figure 6(a) shows the small-signal microwave performance of InAlN/AlN/GaN HEMTs measured at V_g= -2.2V and V_D= 6V. The HEMT exhibited an f_T of 48 GHz and an f_{max} of 66 GHz without de-embedding. Figure 6(b) shows the pulsed I_{DS}-V_{DS} characteristics (width/period=200ns/1ms) of InAlN/AlN/GaN HEMTs on Si substrates under gate-lag (V_{gs0} = -5 V, V_{ds0} = 0 V) and drain-lag (V_{gs0} = -5 V, V_{ds0} = 10 V) conditions. A very small (~8%) drain current (I_D) collapse was observed from the gate-lag and drain-lag measurements. The observed of small I_D collapse in the gate-lag measurement is due to the lattice-matched InAlN/AlN/GaN HEMT structure, thus the absence of piezoelectric polarization. The strain-free InAlN barrier layer has also been verified by Leach et al.[30]. In addition, the surface-related current collapse is also suppressed by the optimized SiN passivation with $(NH_4)_2S_x$ pretreatment[31,32].

4. Conclusions

We have demonstrated for the first time 0.17-μm-gate-length InAlN/AlN/GaN HEMTs on Si substrates with promising device performance characteristics using a non-gold metal stack. A Ta/Si-based ohmic contact exhibited the lowest R_c of 0.36 ± 0.03 Ω-mm with a smooth surface morphology (RMS roughness~2.1 nm). The measured R_c values of non-gold ohmic contacts are comparable to those of the gold-based ohmic contact on the same device structure. The HEMTs exhibited I_{Dmax} = 1110 mA/mm, g_{mmax} = 353 mS/mm, f_T = 48 GHz, and f_{max}= 66 GHz, and I_D collapse < 8%. These results demonstrate the feasibility of using a non-gold metal stack as a low R_c ohmic

contact to achieve good performance submicron-gate InAlN/AlN/GaN HEMTs on Si substrates for high-frequency applications.

Acknowledgments

This work was partially supported by the A*STAR SERC GaN-on-Si Thematic Strategic Research Program (Grant No. 102 169 030). Authors are grateful to T. K. Leng, B. Maung, L. Nicholas, D. Ho and T. Lihuang for their help.

References

1) J. Kuzmik, IEEE Electron Device Lett. **22**, 510 (2001).
2) F. Medjdoub, J.-F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, D. Ducatteau, C. Gaquiere, N. Grandjean, and E. Kohn, IEDM Tech. Dig., 2006, p.1.
3) F. Medjdoub, J.F. Carlin, C. Gaquiere, N. Grandjean, and E. Kohn, Open Electr. Electron. Eng. J., **2**, 1 (2008).
4) J. Liberis, I. Matulioniene, A. Matulionis, E. Sermuksnis, J. Xie, J. H. Leach, and H. Morkoc, Phys. Status Solidi A **206**, 1385 (2009).
5) H. Sun, A. R. Alt, H. Benedickter, E. Feltin, J. -F. Carlin, M. Gonschorek, N. Grandjean, and C. R. Bolognesi, IEEE Electron Device Lett. **31**, 293 (2010).
6) D. S. Lee, J. W. W. Chung, H. Wang, X. Gao, S. Guo, P. Fay, and T. Palacios, IEEE Electron Device Lett. **32**, 755 (2011).
7) F. Medjdoub, D. Ducatteau, C. Gaquie`re, J.-F. Carlin, M. Gonschorek, E. Feltin, M. A. Py, N. Grandjean, and E. Kohn, Electron. Lett. **43**, 71 (2007).
8) Z. X.- Feng, W. Li, L. Jie, W. Lai, and X. Jian, Chin. Phys. B, **22**, 017202 (2013).
9) Y. Yue, Z. Hu, J. Guo, B. S. Rodriguez, G. Li, R. Wang, F. Faria, B. Song, X. Gao, S. Guo, T. Kosel, G. Snider, P. Fay, D. Jena, and H. Xing, Jpn. J. Appl. Phys., **52**, 08JN14 (2013).
10) S. Arulkumaran, K. Ranjan, G. I. Ng, C. M. Manoj Kumar, S. Vicknesh, S. B. Dolmanan, and S. Tripathy, IEEE Electron Device Lett. **35**, 992 (2014).

11) H. Sun, A. R. Alt, H. Benedickter, C. R. Bolognesi, E. Feltin, J. -F. Carlin, M. Gonschorek, and N. Grandjean, App. Phys. Express **3**, 094101 (2010).
12) A. Watanabe, J. J. Freedsman, R. Oda, T. Ito, and T. Egawa, App. Phys. Express **7**, 041002 (2014).
13) S. Arulkumaran, G. I. Ng, C. M. Manojkumar, K. Ranjan, K. L. Teo, O. F. Shoron, S. Rajan, S. B. Dolmanan and S. Tripathy, IEDM Tech. Dig., 2014, p. 594.
14) S. Tripathy, L. M. Kyaw, S. B. Dolmanan, Y. J. Ngoo, Y. Liu, M. K. Bera, S. P. Singh, H. R. Tan, T. N. Bhat, and E. F. Chor, ECS J. Solid State Sci. Technol., **3**, Q84 (2014).
15) Y. Liu, S. P. Singh, Y. J. Ngoo, L. M. Kyaw, M. K. Bera, G. Q. Lo, and E. F. Chor, J. Vac. Sci. Technol. B **32**, 032201 (2014).
16) A. Malmros, P. Gamarra, M. Thorsell, M.-A. Di. F-Poisson, C. Lacam, M. Tordjman, R. Aubry, H. Zirath, and N. Rorsman, Phys. Status Solidi C **11**, 924 (2014).
17) M. Alomari, D. Maier, J.-F. Carlin, N. Grandjean, M. A. D.-Poisson, S. Delage, and E. Kohn, presented at 216th ECS Meet. 2009.
18) S. Arulkumaran, G. I. Ng, S. Vicknesh, H. Wang, K. S. Ang, C. M. Manoj Kumar, K. L. Teo, and K. Ranjan, App. Phys. Express **6**, 016501 (2013).
19) R. Gong, J. Wang, S. Liu, Z. Dong, M. Yu, C. P. Wen, Y. Cai, and B.Zhang, Appl. Phys. Lett. **97**, 062115 (2010).
20) N. A. Papanicolaou, M. V. Rao, J. Mittereder, and W. T. Anderson, J. Vac. Sci. Technol. B **19**, 261 (2001).
21) X. Kong, K. Wei, G. Liu, and X. Liu, J. Phys. D **45**, 265101 (2012).
22) Y-L. Lan, H.-C. Lin, H.-H. Liu, G-Y. Lee, F. Ren, S. J. Pearton, M.-N. Chang, and J.-I. Chyi, Proc. SPIE, 7216, 72162 (2009).
23) H.P. Xin, S. Poust, W. Sutton, D. Li, D. Lam, I. Smorchkova, R. Sandhu, B. Heying, J. Uyeda, M. Barsky, M. Wojtowicz, and R. Lai, CS MANTECH Conf. 2010, p. 149.
24) G. Pozzovivo, J. Kuzmik, C. Giesen, M. Heuken, J. Liday, G. Strasser, and D. Pogany, Phys. Status

Solidi C **6**, 999 (2009).

25) O. Jardel, G. Callet, J. Dufraisse, M. Piazza, N. Sarazin, E. Chartier, M. Oualli, R. Aubry, T. Reveyrand, J.-C. Jacquet, M. A. Di Forte Poisson, E. Morvan, S. Piotrowicz, and S. L. Delage, Int. J Microwave Wireless Technologies, **3**, 301 (2011).
26) J. Lee, M. Yan, B. Ofuonye, J. Jang, X. Gao, S. Guo, and I. Adesida, Phys. Status Solidi A **208**, 1538 (2011).
27) D. S. Lee, S. Guo, D. Kopp, P. Fay and T. Palacios, IEEE Electron Device Lett. **32**, 1525 (2011).
28) S.Arulkumaran, G. I. Ng, S. Vicknesh, L. Zhihong, and B. Maung, Phys. Status Solidi C 7, 2412 (2010).
29) Y. Li, G. I. Ng, S. Arulkumaran, C. M. Manoj Kumar, K. S. Ang, M. J. Anand, H. Wang, R. Hofstetter, and G. Ye, App. Phys. Express **6,** 116501 (2013).
30) J. H. Leach, M.Wu, X. Ni, X. Li, U. Ozgur, and H. Morkoc, Phys. Status Solidi A **207**, 211 (2010).
31) S. Vicknesh, S. Arulkumaran, and G. I. Ng, IEEE MTT-S Microwave Symposium Digest, 2012. p. 1.
32) S. Arulkumaran, G. I. Ng, and S. Vicknesh, IEEE Electron. Device Lett. **34**, 1364 (2013).

Table Captions

Table I. State-of-the-art contact resistances value of non-gold ohmic contacts for InAlN/AlN/GaN HEMTs on silicon, sapphire, and SiC substrates.

Table II. State-of-the-art contact resistances of gold-based ohmic contacts for InAlN/AlN/GaN HEMTs on SiC and silicon substrates.

Figure Captions

Fig. 1. (a) Schematic cross section of InAlN/AlN/GaN HEMT structure, optical microscope images (500X) of (b) non-gold ohmic contact and (c) conventional III–V gold ohmic contact on InAlN/AlN/GaN HEMT structure, and (d) cross-sectional HR-TEM image of T-gate on InAlN/AlN/GaN HEMTs.

Fig. 2. (a) Current-voltage characteristics of non-gold and gold ohmic contacts on InAlN/AlN/GaN HEMTs on Si. The inset is a schematic diagram of the 2-in. diameter wafer with different locations of the TLM patterns. Total resistance versus TLM gaps for (b) non-gold and (c) gold ohmic contacts on InAlN/AlN/GaN HEMTs.

Fig. 3. (a) Cross-sectional HR-TEM image, (b) zoomed EDX area mapping (c) EDX line scan and (d) zoomed line scan (25 to 60 nm) of alloyed Ta/Si/Ti/Al/Ni/Ta ohmic contacts with InAlN/AlN/GaN HEMTs.

Fig. 4. (a) Two-terminal gate-leakage current-voltage (b) C-V characteristics of InAlN/AlN/GaN HEMTs on Si.

Fig. 5. (a) I_{DS}-V_{DS} and (b) transfer characteristics of InAlN/AlN/GaN HEMTs ($W_g/L_g/L_{gd}$) = (2×75)/0.17/1.7 μm) on Si substrates with non-gold ohmic contacts.

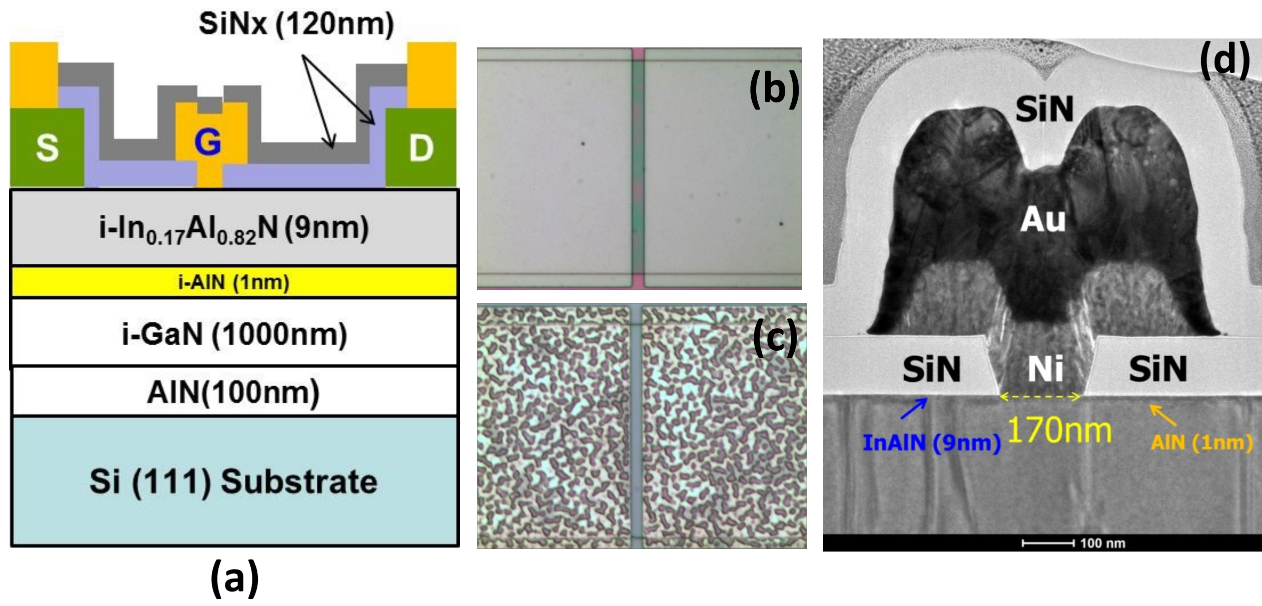
Fig. 6. (a) Small-signal characteristics and (b) pulsed I_{DS}-V_{DS} characteristics (pulse width/period=200ns/1ms) of InAlN/AlN/GaN HEMTs.

Table I

Affiliation	Substrate	Ohmic metal	Annealing temp. / time (ºC /s)	R_c (Ω-mm)
IMRE [14]	Si	Ti/Al/Ni/W	900/60	0.56
NUS [15]	Si	Hf/Al/Ta	600/60	0.58
Chalmers [16]	SiC	Ta/Al/Ta	550/-	0.64
ULM [17]	Sapphire	Ti/Al/Ni & Ta/Cu/Ta	900/-	1.60
This work	**Si**	**Ta/Si/Ti/Al/Ni/Ta**	**825/30**	**0.36**

Table II

Affiliation	Substrate	Ohmic metal	Treatments prior to metallization	Annealing Temp. / time (ºC/ s)	R_c (Ω-mm)
UND[9]	SiC	Ti/Au	Regrown n^+-GaN by MBE	Non alloyed	0.16
NTU [10,13]	Si	Ti/Al/Ni/Au	-	825/30	0.33
ETH [11]	Si	Ti/Al/Au	-	800/30 and 850/30 l(Two fold annealed)	0.36
NIT [12]	Si	Ti/Al/Ni/Au	-	800/30	0.60
ISSE [24]	SiC	Ti/Al/Ni/Au	$SiCl_4$ plasma etching (Ohmic recess)	600/-	0.70
ALCATEL [25]	SiC	Ti/Al/Ni/Au	-	900/30	0.15
UIUC [26]	SiC	Mo/Al/Mo/Au	$SiCl_4$ plasma etching (Ohmic-recess)	650/30	0.15
MIT [27]	SiC	Si/Ge/Ti/Al/Ni/Au	-	820/30	0.35



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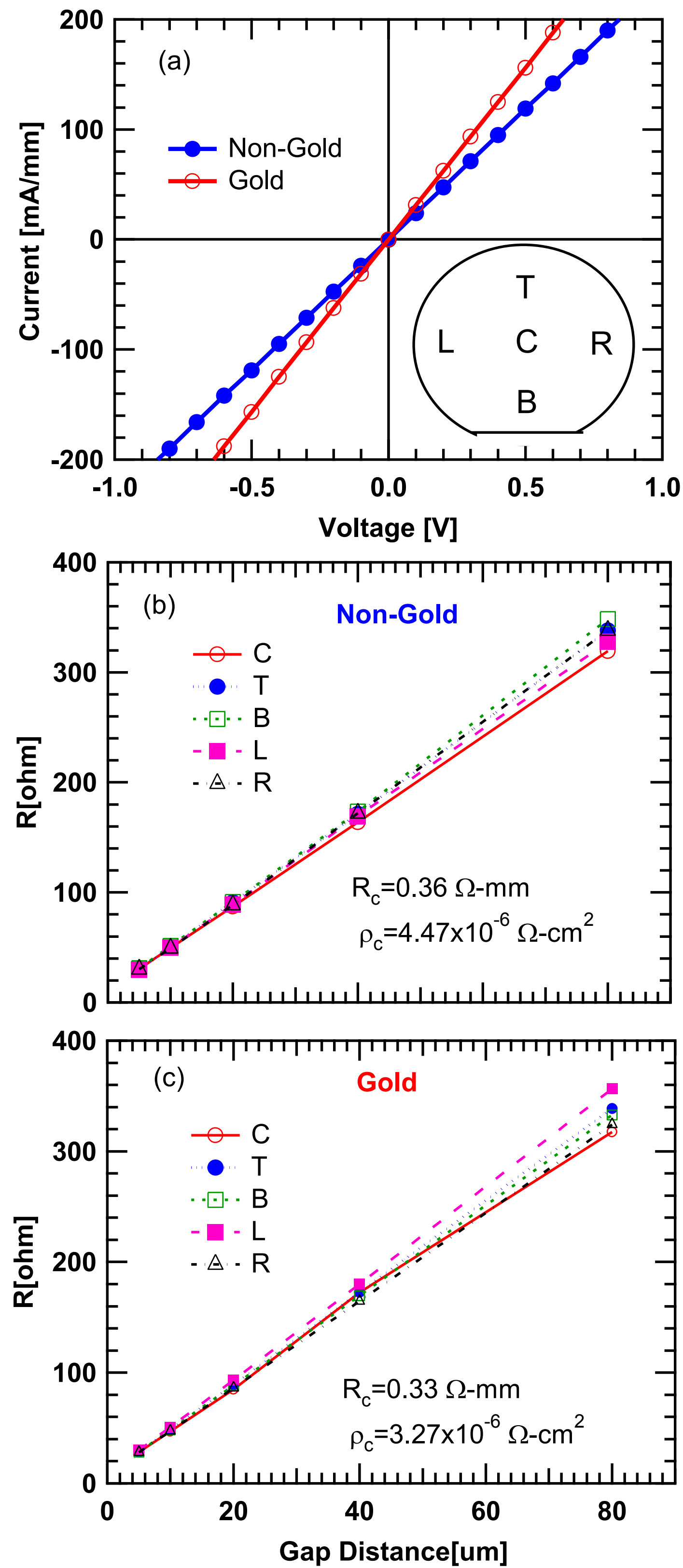

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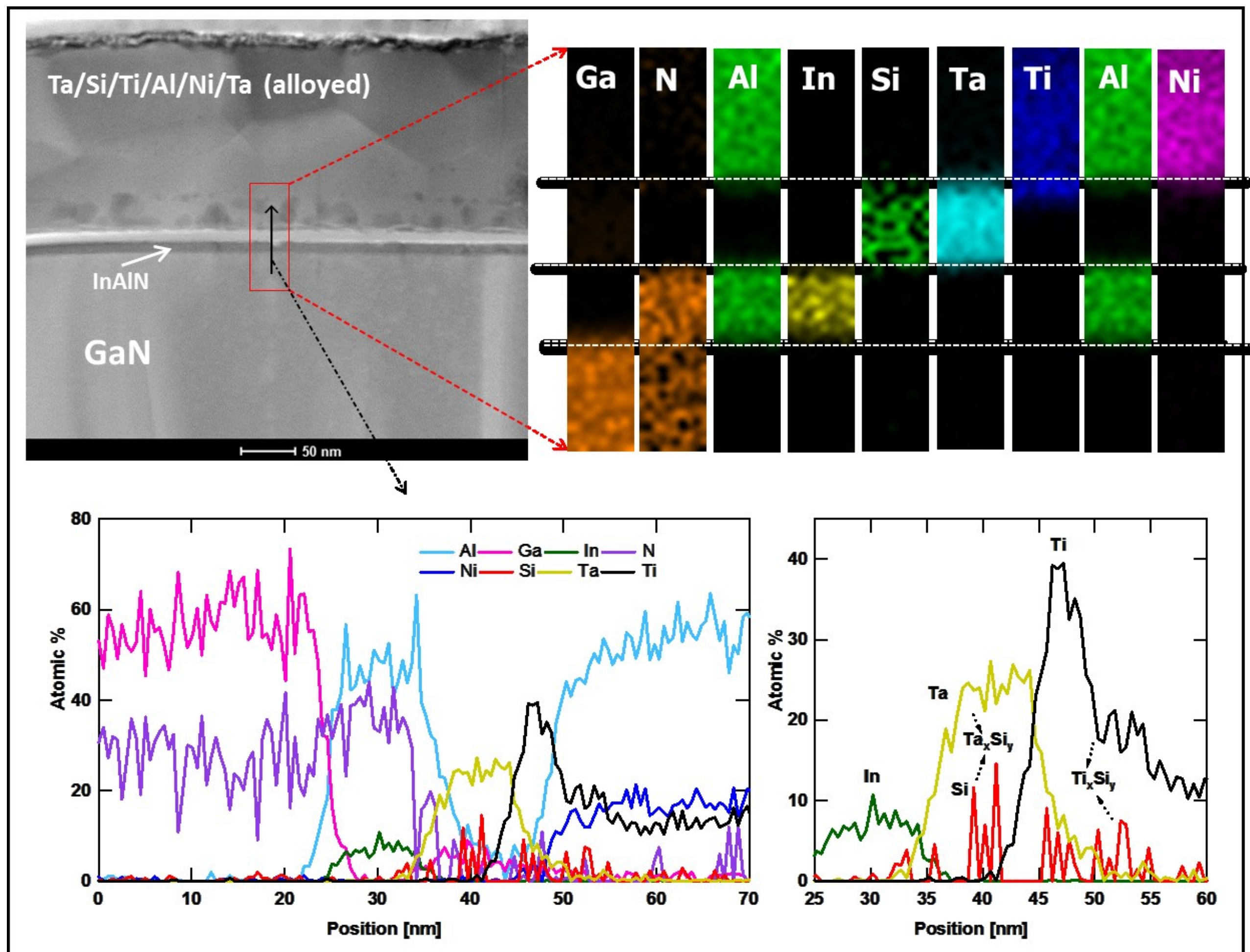

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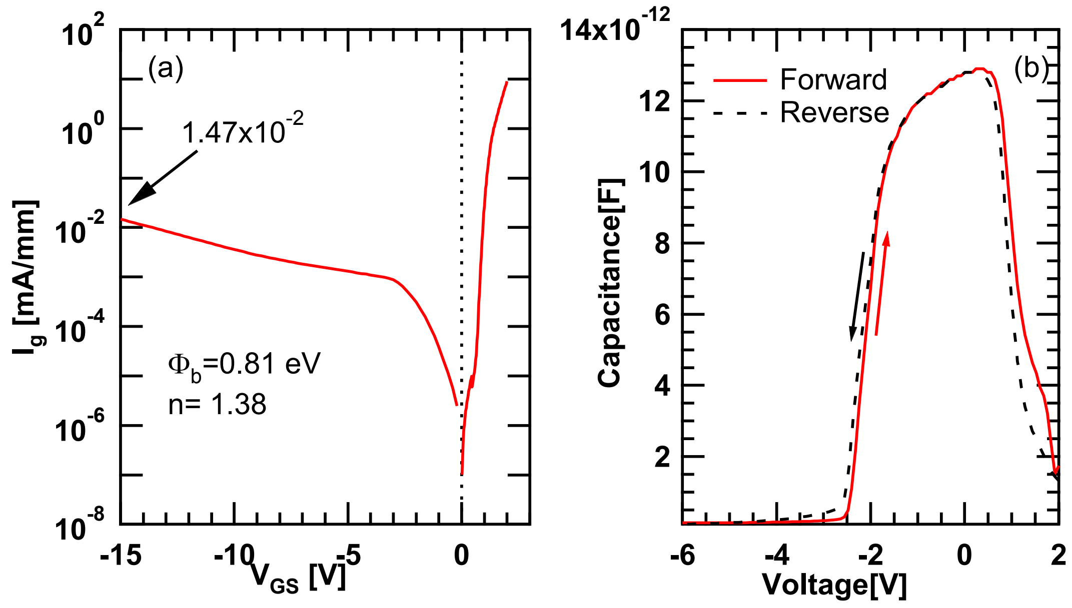

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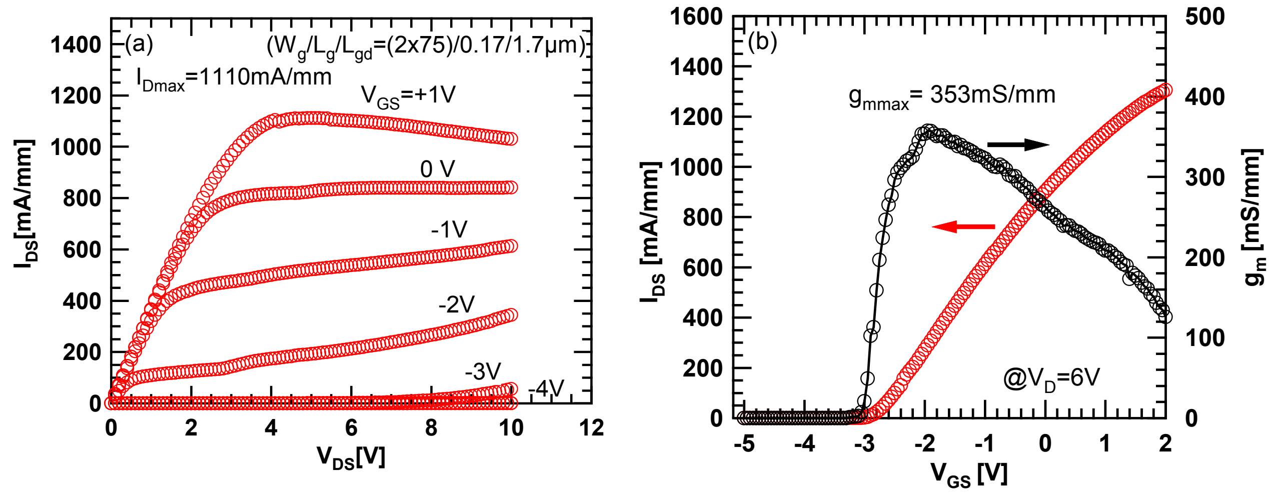

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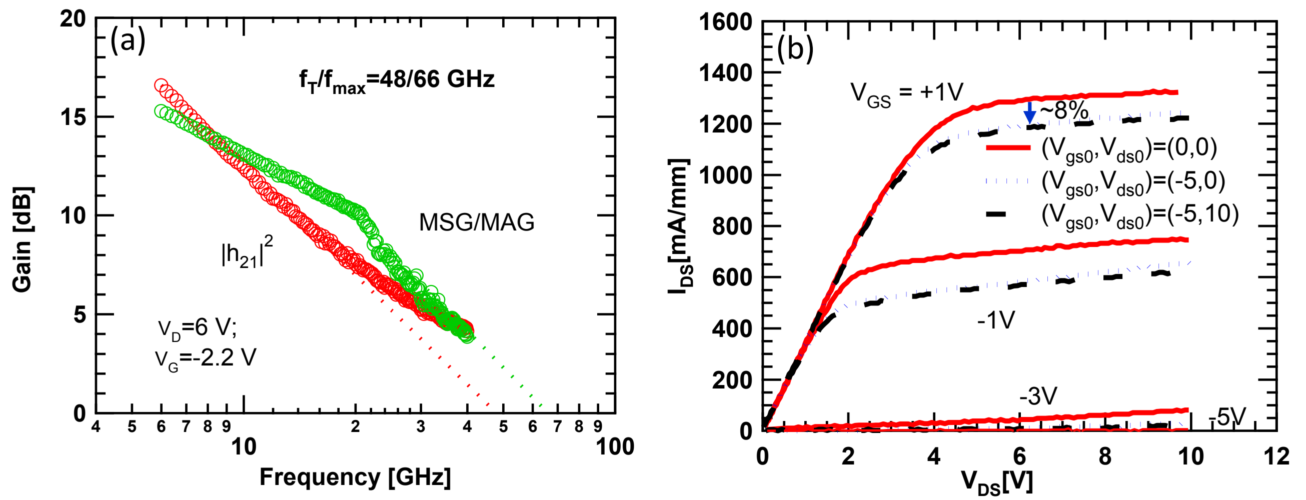

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