Design of SPST/SPDT Switches in 65nm CMOS for 60GHz Applications

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Abstract

This paper presents novel single-pole-single-throw (SPST) and single-pole-double-throw (SPDT) switches for 57-66GHz band applications. At 60GHz band, the SPST switch exhibits an insertion loss of 1.6dB, a return loss of 16dB, an isolation of 27dB and an input 1-dB compression point (IP_{1dB}) of 11dBm; Correspondingly, the SPDT switch achieves an insertion loss of 3dB/2.5dB, a return loss of 12.5dB/12dB, an isolation of 22dB/22dB and an input P_{1dB} of 12dBm/13dBm in the Tx/Rx mode, respectively. The switches are designed and implemented with STMicroelectronics 1.2V 65nm CMOS RF process.

Introduction

Recently, wireless systems for short-range and high-speed communications are pushed up to 60GHz band because of released license-free bands 57-64GHz of U.S. and 59-66GHz of Japan. As an essential component for wireless transceivers, the T/R switch is required with low insertion loss, high isolation and high linearity. Some CMOS T/R switches operating at 60GHz band have been reported recently [1], [2]. However, the performance presented in [2] are not so good for the typical limitations in shunt-series topology [3], whereas Traveling-wave concept as a new design idea introduced in [1] achieves a high performance SPDT switch. Antennas for 60GHz radios [4] make it possible to integrate with T/R switches on the same die for system-on-chip (SoC). In this paper, novel CMOS SPST/SPDT switches are investigated for 60GHz applications with good performance.

Switches Design

Fig. 1 (a) shows a high frequency parasitic capacitances model for an nMOS switch at off state [5], [6]; For reducing analysis of switch circuits, the whole parasitic capacitances are simplified as a capacitance model shown in Fig. 1 (b).

Presented in Fig. 2 (a) is the schematic of the CMOS SPST switch. The SPST switch is a symmetric topology including only one transmit (Tx) path. When the control voltage Vc is set to 0V and applied to the gates of M_1 and M_2 through large bias resistors R_1 and R_2, which separate the dc bias voltage from RF signal, M_1 and M_2 are tuned off and can be simplified as two capacitors C_{M1} and C_{M2}; Combining inductor L_1, C_{M1}-L_1-C_{M2} forms a π impedance matching network to match 50Ω between source and load at 60GHz, the SPST switch is in the Tx mode at this case and power is furthest delivered from the Tx port to the antenna because of the excellent π circuit causing lower insertion loss. The equivalent circuit is shown in Fig. 2 (b). When Vc is configured to 1.2V turning on M_1 and M_2 to work in the linear region with low on-resistance, source and load are shortened to ground simultaneously. The SPST is switched off at this case and no power is delivered, its reduced equivalent circuit is represented in Fig. 2 (c).

The schematic of the CMOS SPDT switch is shown in Fig. 3, which comprise one Tx path and one Rx path. Capacitor C is constructed by two parallel capacitors C_3 and C_4 so that the

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capacitance of C is the sum of capacitances of C_3 and C_4. In the Tx mode, Vc- is pulled up to 1.2V, whereas Vc+ is pulled down to 0V synchronously. Correspondingly, M_4 is shortened to ground to separate the low-noise amplifier (LNA) from the antenna for being turned on by Vc-, C_4 and L_4 form a parallel resonator that resonates at the operating frequency [3]. M_3 is turned off to be simply regarded as one capacitor C_{M3}, C_{M3}-L_3-C_3 composes a π network as 50Ω transformation matching the power amplifier (PA) to the antenna at 60GHz. Considering the signal on the Tx port is much more stronger than that on the Rx port and the required isolation (target value of 20dBm) between the Tx port and the Rx port, the size of M_3 is increased to two times of that of M_4 and the total parasitic capacitance of M_3 is accordingly increased. As a result, the π network of C_{M3}-L_3-C_3 can not match 50Ω environment precisely so as to cause high insertion loss, hence, to ensure the π network to work well at 60GHz, another inductor L_5 is added as a solution to cancel the unwanted capacitance of C_{M3}. This is the reason why the SPDT switch is designed to be asymmetrical. The whole simplified equivalent circuit consisting of one π network of C_{M3}- L_3-C_3 and one resonator of C_4-L_4 is presented in Fig. 3 (b). In the Rx mode, Vc- is set to 0V and Vc+ is set to 1.2V simultaneously, therefore, M_4 is turned off to be a capacitor C_{M4}, which acts as one component of the π network of C_{M4}-L_4-C_4 matching the antenna to the LNA; M_3 shorten the Tx port to ground isolating the PA from the antenna and C_3-L_3 constructs a parallel resonator. Fig. 3 (c) shows the simplified equivalent circuit in the Rx mode.

Simulation Results

The SPST/SPDT switches are simulated and implemented using STMicroelectronics 1.2V 65nm CMOS RF process. The nMOS devices have a f_T of 160GHz and f_{MAX} over 200GHz. The layouts are shown in Fig. 1; (c) is the layout of the SPST switch while (d) represents the layout of the SPDT switch. Chip sizes of the SPST/SPDT switches are $0.34 \times 0.34\text{mm}^2$ and $0.5 \times 0.48\text{mm}^2$, respectively. The chips are under fabrication. Presented in Fig. 4 are post-layout simulation results of the SPST switch. In the 57-66GHz band of Fig. 4 (a), return loss (S_{11}) is better than 10dB, insertion loss (S_{21}) is from 1.6dB to 2.2dB, isolation is around 28dB and input P_{1dB} is 11dBm at 60GHz in Fig. 4 (b). Post-layout simulation results of the SPDT switch are shown in Fig. 5. Similarly, in the 57-66GHz band of Fig. 5 (a), in the Tx/Rx mode, return loss is higher than 10dB, isolation is more than 21dB and insertion loss is less than 3.6dB/2.6dB, respectively. Fig. 5 (b) shows input P_{1dB} of the SPDT switch in the Tx/Rx mode at 60GHz are 12dBm and 13dBm, respectively. The performance summary of the SPST/SPDT switches and comparison with recently reported switches are given in Table Ⅰ.

Conclusion

The SPST/SPDT switches are designed for 60GHz application using STMicroelectronics 1.2V 65nm CMOS RF process. Novel topologies are adopted to minimize the insertion loss and improve the isolation and power handling capability. Sizes of the SPST/SPDT switches are 0.12mm^2 and $0.24\ \text{mm}^2$, respectively.

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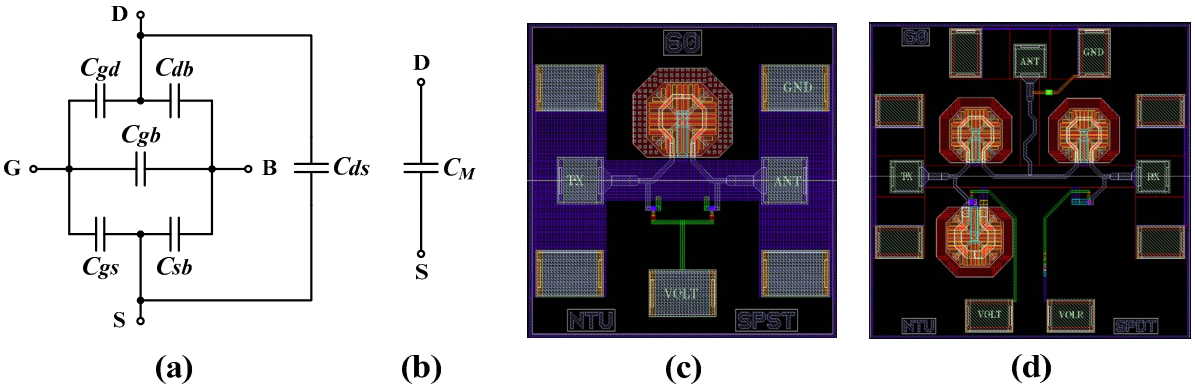

Figure 1. (a) Parasitic capacitances of nMOS switch at off state and (b) its simplified capacitance model; (c) layout of the SPST switch and (d) layout of the SPDT switch.

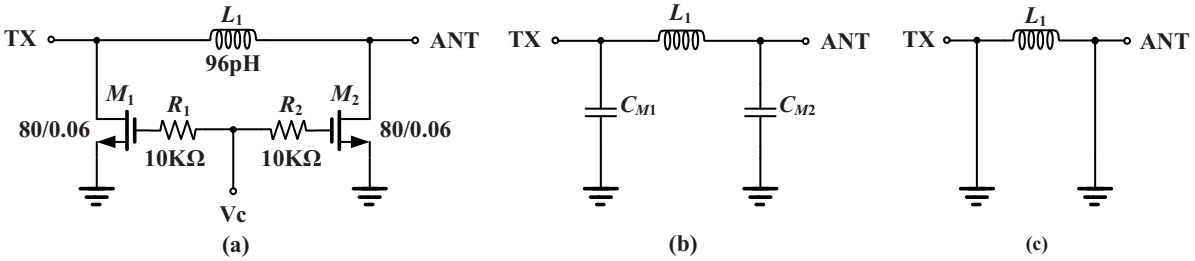

Figure 2. (a) Schematic of the CMOS SPST, (b) and (c) are simplified equivalent circuits when M_1 and M_2 are off/on state, respectively.

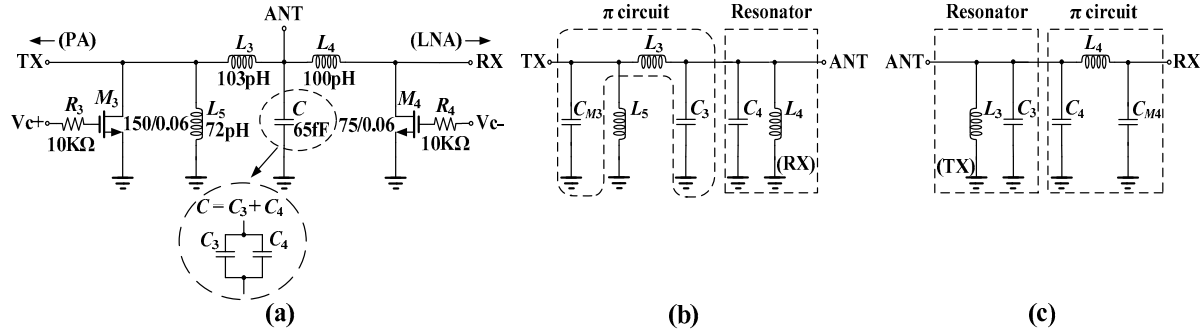

Figure 3. (a) Schematic of the CMOS SPDT, (b) and (c) are simplified equivalent circuits when the SPDT are in Tx/Rx mode, respectively.

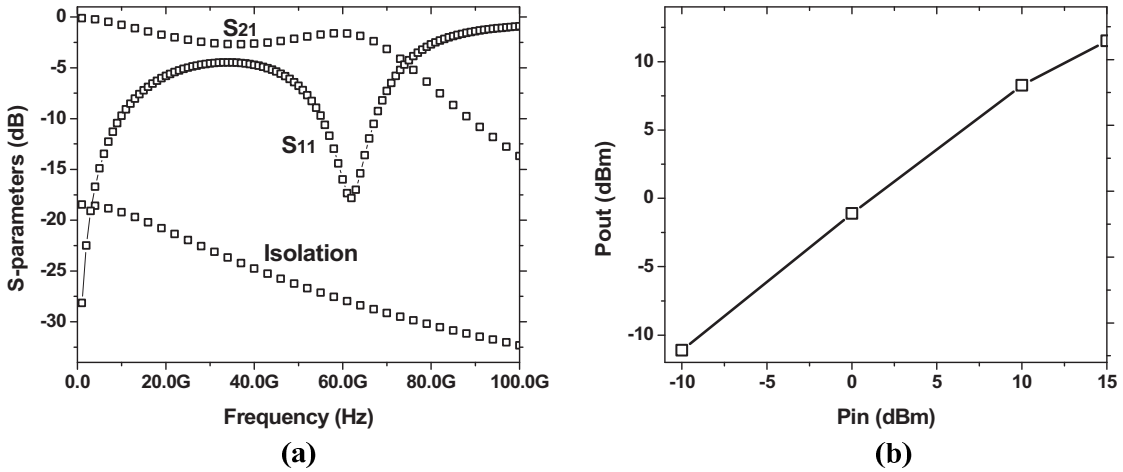

Figure 4. Post-layout simulations of the SPST switch. (a) Insertion loss (S_{21}), input return loss (S_{11}) and isolation; (b) input $P_{1dB.}$

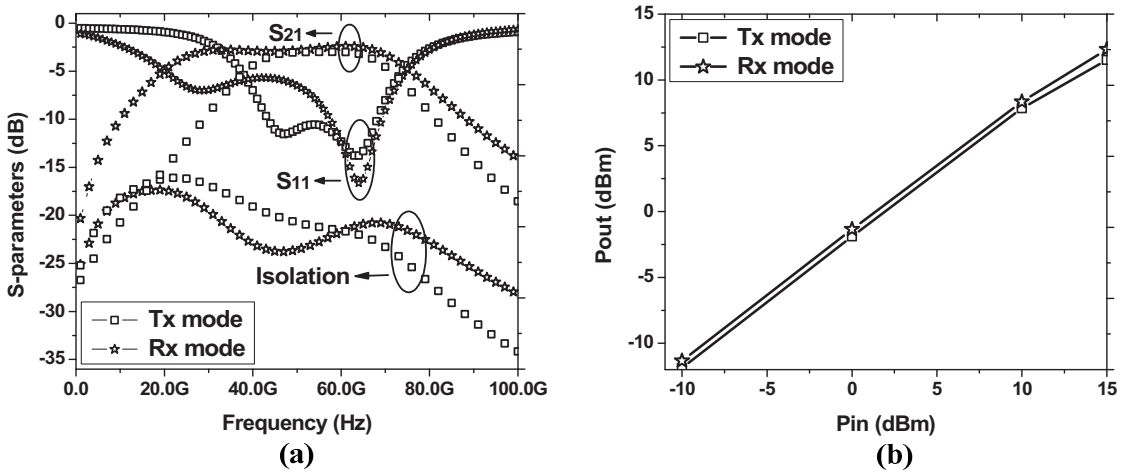

Figure 5. Post-layout simulations of the SPDT switch. (a) Insertion loss (S_{21}), input return loss (S_{11}) and isolation in the Tx/Rx mode; (b) Input P_{1dB} in the Tx/Rx mode.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON

		Frequency (GHz)	Insertion Loss (dB)	Return loss (dB)	Isolation (dB)	P_{1dB}@60GHz (dBm)	CMOS Technology
SPST		57-66	1.6 - 2.2	> 10	> 27	11	65nm
SPDT	Tx	57-66	3 - 3.6	> 10	> 21	12	65nm
	Rx	57-66	2.4 - 2.6	> 10	> 21	13	
[1]		50-94	< 3.3	> 20	> 27	15 @77GHz	90nm
[2]		57-66	4.5 - 5.8	-15 - 27	24.1 - 26	4.1	0.13μm