

**Analysis and Design of Switching Amplifiers
for Smartphones**

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Summary

This thesis pertains to the analysis and design of switching amplifiers with improved specifications over the state-of-the-art for smartphones, including higher power-efficiency to address the short battery lifespan, lower noise, and wider bandwidth. The specific switching amplifiers are the Class D amplifier (CDA) for audio applications and the hybrid CDA for supply modulators for envelope tracking (ET) radio frequency (RF) power amplifiers (PAs).

For the audio CDA, we investigate and analytically derive the effects of the non-ideal AC ground and mechanisms leading to their ensuing effects. Unlike the simplified single-ended integrator model used in literature, our analysis is based on a realistic fully-differential integrator model, and the open-loop and single-feedback topology in literature is extended to the ubiquitous double-feedback topology. We show that a reduction of the noise on the AC ground, as expected, would drastically improve the PSRR. However, the CDA with 1st-order integrators unexpectedly provides similar or higher PSRR than the CDA with 2nd-order integrators if both CDAs are designed with the same carrier attenuation. The derived analytical expressions are verified by means of HSPICE simulations and on the basis of practical measurements on discretely-realized CDAs.

For the hybrid CDA serving as the supply modulator for ET PAs, we investigate the power mechanisms thereto and propose two architectures – the first with the objective of reducing the power dissipation and extending the bandwidth of the supply modulator for a wideband ET PA for 40MHz LTE-A protocol, and the second with the objective of optimizing the power-efficiency of the supply modulator for multi-standard RF

communication protocols, e.g., WCDMA, LTE, LTE-A, etc. To the best of our knowledge, this is the first supply modulator that is optimized for multi-standard RF protocols. The proposed two architectures were designed, monolithically realized and the functionality of the proposed architectures is verified experimentally.

Specifically, for the former, our investigations include the analysis of the effect of the propagation delay to the hysteresis current of the hybrid CDA. On the basis of the said investigations, we propose a hybrid CDA with a delay-based hysteresis controller and Class AB amplifier. The proposed supply modulator (from measurements on the prototype IC) features the widest bandwidth (40MHz) amongst reported supply modulators to date, yet with highly competitive (other) parameters. Specifically, on the basis of a composite figure-of-merit (bandwidth \times output power \times power-efficiency \times output swing \times 1/ripple noise), our proposed supply modulator features a very significant 20x improvement over reported supply modulators.

For the latter, we explore the design challenges of the hybrid CDA for multi-standard RF protocols and analyze the optimum switching frequency for maximum power-efficiency. We propose a hybrid CDA with a novel dual-mode Sigma-Delta control and adaptive biasing Class AB amplifier to self-adjust the operation according to the input envelope signals – the first-ever reported in literature for a hybrid CDA that is optimized for multi-standard communications protocols. On the basis of measurements on IC prototypes, our proposed supply modulator significantly improves its static power-efficiency by up to $\sim 6\%$. When tracking 40MHz LTE-A envelope signals, the proposed supply modulator features the highest power-efficiency (85% at 1.8W) over the state-of-the-art and remains highly power-efficient ($>80\%$) over a wide range of output power.

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Nomenclature

BTL	Bridge-Tied-Load
CDA	Class D Amplifier
CMOS	Complementary Metal Oxide Semiconductor
DFF	D Flip Flop
EMI	Electromagnetic Interference
ET	Envelope Tracking
IC	Integrated Circuit
IMD	Intermodulation Distortion
PA	Power Amplifier
PAE	Power Added Efficiency
PAPR	Peak-to-Average Power Ratio
PCB	Printed Circuit Board
PDM	Pulse Density Modulation
PWM	Pulse Width Modulation
PS-IMD	Power Supply Induced Intermodulation Distortion
PSRR	Power Supply Rejection Ratio
RF	Radio Frequency
SNR	Signal-to-Noise Ratio
THD+N	Total Harmonic Distortion plus Noise

Chapter 1 Introduction

1.1 Background and Motivations

Nowadays, switching amplifier, otherwise also known as the Class D amplifier (CDA), is increasingly prevalent as the power amplifier in many applications due to its significantly high power-efficiency. This high efficiency is contributed by the switching transistors in the output stage of the CDA, which are either fully “on” or fully “off”, with desirable low quiescent power. In this Ph.D. program, we have focused on the analysis and practical design of CDAs for the applications in smartphones.

Smartphones (and phablets), embodying wireless data and voice communication means, are presently the wireless communications transceiver of choice. Nevertheless, the primary and perennial complaint of smartphone users is the short battery lifespan of smartphones between charges. Not unexpectedly, there is continuing intensive research into the power management and the design of key functional blocks to obtain higher power-efficiency smartphones to extend the said battery lifespan.

The battery lifespan of smartphones, to a large degree, depends on the application/functionality. In applications where the smartphone is used as a portable music player (without display and without wireless communications), the audio power

amplifier (PA) (serving as the speakerphone driver) is the most power dissipative block. To obtain high power-efficiency, the audio PA is largely based on the audio CDA [1-4]. At this juncture, the design-art for audio CDAs is mature [1-50] – to the point where CDAs featuring high power-efficiency and high fidelity attributes are somewhat routine [5-14]; the ‘high-fidelity’ are often defined in terms of high power supply rejection ratio (PSRR) [15-21], low power supply induced intermodulation distortion (PS-IMD) [20-21], low total harmonic distortion plus noise (THD+N) [22-24], low intermodulation distortion (IMD) [25-27] and low electromagnetic interference (EMI) [28-31]; see Chapter 2 later. Nevertheless, in a smartphone, the operating condition for the CDA in the context of noise is challenging. Specifically, the audio PA is subjected to high power supply noise due to wireless communications in close proximity. For example, in 2G (GSM) and 4G (LTE), the CDA is subjected to significant power supply noise at 217Hz and 1kHz, respectively [5, 32]. As these noise are within the audio range, PSRR need to be very high (e.g., PSRR>90dB), and PS-IMD be low (e.g., PS-IMD<-90dB). To alleviate this noise problem, the audio circuits (typically the audio codec embodying the CDA and other audio circuits) are usually placed as far as possible from the wireless communication circuits on the printed circuit board (PCB) of the smartphone.

In view of the challenges relating to battery lifespan, the most obvious means to improve the battery lifespan is to increase the size (energy capacity) of the battery. This entails reducing the form factor of the electronics so that the enclosure of the smartphone can accommodate a larger battery. This form factor reduction would involve placing the integrated circuits (ICs) on the PCB of the smartphone in closer proximity (or increasing the functionality of ICs and SOCs (e.g. System-in-Package)). This, in some sense,

contravenes the present practice, as described earlier, of separating the audio circuits and the wireless communication components as far as possible. Put simply, the form factor reduction would further exacerbate the noise subjected to the CDA.

In applications involving wireless communications, the short battery lifespan is largely due to radio frequency (RF) PAs [53, 54], which are often the most power dissipative blocks in the smartphones. Typically, they dissipate >50% of the overall power in many instances. To improve the power-efficiency of RF PAs, the reported design methodologies include envelope tracking (ET) PAs [55-80], envelope elimination and restoration PAs [81-84] and Doherty PAs [85]. At this juncture, the ET PA, comprising a supply modulator and RF PA(s), is ubiquitous and is arguably the most power-efficient. Compared to envelope elimination and restoration PAs, ET PAs feature wider signal bandwidth, better linearity and simpler hardware (hence lower cost) [83]. On the other hand, compared to Doherty PAs, ET PAs feature higher power-efficiency. Despite these advantages of the ET PAs, the performance of the state-of-the-art supply modulators for ET PAs remains unsatisfactory, including limited bandwidth, relatively high noise and low power-efficiency.

Interestingly, a commonality between the audio CDA and the ET PA is the CDA but clocked at different rates. Specifically, the audio CDA whose bandwidth is in the audio range (<20kHz), is typically switched at <1MHz, e.g., several hundreds of kHz. The supply modulator of the ET PA, on the other hand, is usually either a CDA or a hybrid CDA switching beyond the audio frequency range, typically several tens of MHz. Consider now the specifics of the audio CDA and the supply modulator of the ET PA, and some challenges pertaining to their performance.

The speakerphone audio PAs typically comprises a linear amplifier and the CDA. The function of the audio PA is to amplify the low-power electronic signals within the audio frequency range, 20Hz-20kHz, to electronic signals capable of driving speakerphones. The CDA therein is often a unity gain buffer whose output is a low impedance voltage driver (typically pulse width modulation (PWM) scheme [5, 8, 9, 12, 18, 20, 23, 33]; see Chapter 2 later). For the audio PA in smartphones, high power-efficiency is of particular importance. This is, as described earlier, because a power-inefficient amplifier not only reduces the battery lifetime of smartphones, but also requires a heat-sink to avoid thermal runaway which would otherwise result in permanent damage. Heat-sinks are particularly cumbersome because they are typically bulky, thereby incompatible in small-form-factor consideration described earlier, consequent to the need for high power-efficiency CDAs. CDAs are now ubiquitous as the audio PA of choice in smartphones. Specifically, compared to their linear counterparts (i.e., Class A and Class AB amplifiers) and hybrid counterparts (i.e., hybrid CDAs), they feature significantly higher power-efficiency [34-38].

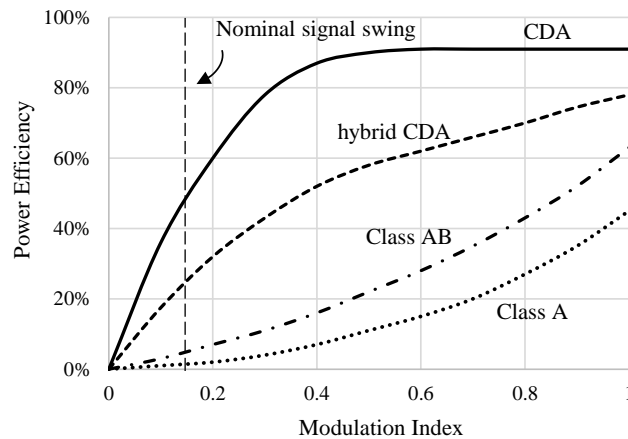


Fig. 1-1: Power-efficiency of various classifications of audio PAs

Fig. 1-1 depicts the typical power-efficiency of the various classifications of audio PAs [37]. There are essentially three classes of amplifiers: linear amplifier (Class A and Class AB), CDA (switching amplifier) and hybrid CDA (switching-cum-linear); the linear Class B amplifier is not considered due to its gross crossover distortion [38]. In this plot, the abscissa is quantified as modulation index (M) which is equivalent to signal swing but normalized to the supply rail, V_{DD} . In the context of audio signals, the nominal modulation index at $M=0.15$ is of particular interest because this is the ‘average’ signal in the CDA. This low M is nominal because of the crest factor of speech and music [34], and to allow sufficient signal headroom for avoiding signal clipping.

From Fig. 1-1, it can be seen that the CDA features the highest power-efficiency over the entire modulation index range. This advantage is most apparent in the low modulation index range, including at the nominal $M=0.15$. The high power-efficiency attribute of the CDAs is largely due to the switching transistors in the output stage [35, 36] which dissipate low quiescent current (zero bias current). By comparison, linear amplifiers are power-inefficient due to the relatively large DC bias required. The maximum efficiency of practical CDAs is typically $>90\%$ and the power-efficiency remains high over a large range of modulation indexes. As expected, the power-efficiency of the hybrid CDAs lies between the CDA and the linear amplifiers.

Despite the power-efficiency advantage offered by CDAs for audio applications that renders them attractive for smartphones, their immunity to noise, particularly PSRR and PS-IMD as described earlier, is poor [17-21]. This conversely limits their proximity to the wireless communication circuits. This is largely because the noise induced into their power supply rail from the close proximity wireless communication circuits can be

excessive. This PSRR and PS-IMD limitations are interesting in the context of the maturity of the design-art of CDAs where, as described earlier, ‘high-fidelity’ CDAs are somewhat routine. Put simply, in the context of smartphone applications and the like where the complex electronics is highly integrated leading to noisy power lines, the ‘fidelity’ measure of the CDA should include high tolerance to noise in the supply rail. For example, high PSRR>90dB, and low PS-IMD<-90dB.

The CDA design community is cognizant of the need for high PSRR and PS-IMD. Nevertheless, it is interesting to note that the analytical investigations thereto reported in literature are incomplete and/or somewhat over-simplified. Particularly the assumption that the AC ground is noise-less and that the fully-differential integrator model is a simple model. For the former, there is, conversely, substantial noise on the AC ground because the AC ground is typically generated by a voltage divider from the supply rail. This simple means is almost universally employed in CDA designs because of hardware simplicity, low power dissipation and because the $\frac{1}{2} V_{DD}$ is automatically scaled to V_{DD} . Put simply, the effect of noise on the AC ground to PSRR and PS-IMD remains unreported – despite the imperativeness thereto.

In the case of the latter, the over-simplification assumes that the resistors and capacitors are perfectly matched, which is untrue in real-life. It is also interesting to note that despite the imperativeness of PSRR, reported PSRR analysis of 3-state Bridge-tied-load (BTL) closed-loop CDAs has to date been limited to the single-feedback topology. Instead, the double-feedback topology is a more ubiquitous topology but an analysis thereto remains lacking. In general, it can be easily appreciated that an analytical analysis of PSRR and PS-IMD is useful because they provide valuable insights to CDA designers

into the PSRR and PS-IMD mechanisms including the effect of various circuit parameters, and ensuing trade-offs.

Consider now the supply modulator for ET PAs [55-80] for improving the power-efficiency of the conventional RF PAs [53, 54]. Fig. 1-2 depicts the block diagram of an ET PA. The supply modulator therein constantly provides dynamically changing supply to the RF PA based on the output power. The output of the supply modulator is high when the output power is high and vice versa. In this fashion, the RF PA is kept nearly always in compression where its power-efficiency is high, hence avoiding operation in the power-inefficient back-off condition. In ET PAs, the supply modulator is essentially a power management circuit for the RF PA. Hence, the overall performance of the ET PA, including bandwidth, linearity, and power-efficiency, is strongly dependent on the supply modulator [55-57].

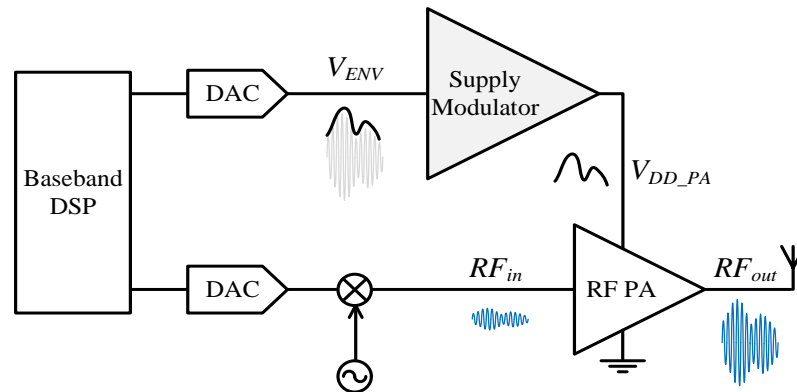


Fig. 1-2: Block diagram of an ET PA

Fig. 1-3 compares the power dissipation of a conventional 3-mode RF PA and an ET PA [57]. From Fig. 1-3, we can see that the power-efficiency of the ET PA has significantly improved compared to the conventional counterpart, especially for low output power.

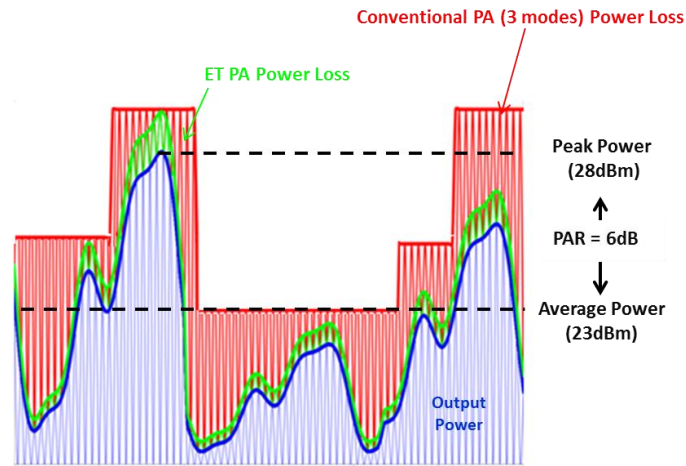


Fig. 1-3: Comparison of power dissipation in an ET PA and a conventional RF PA

It can be easily appreciated that the supply modulator is a critical block in the ET PAs. The supply modulator therein is required to track wideband envelope signals (>1MHz, and goes up to tens of MHz) for modern wireless communication standards [55-57], such as CDMA, WCDMA, LTE/LTE-A. In other words, the bandwidth of the supply modulator in ET PAs is significantly wider than the audio applications (20Hz-20kHz). Although the CDAs feature high power-efficiency, they may not be suitable for tracking wideband signals for ET PAs. This is because the switching frequency of the CDA is required to be at least 5x wider than the bandwidth of the input signals to suppress the

switching noise [11], and the ensuing high switching frequency results in significant large power loss [35]. Although some design techniques such as dual-switch [60], multi-phase [61], multi-level [62], have been proposed to reduce the required switching frequency of the CDA, the bandwidth of the state-of-the-art CDAs [58-64] is still relatively narrow (insufficient), which is limited to $\sim 10\text{MHz}$.

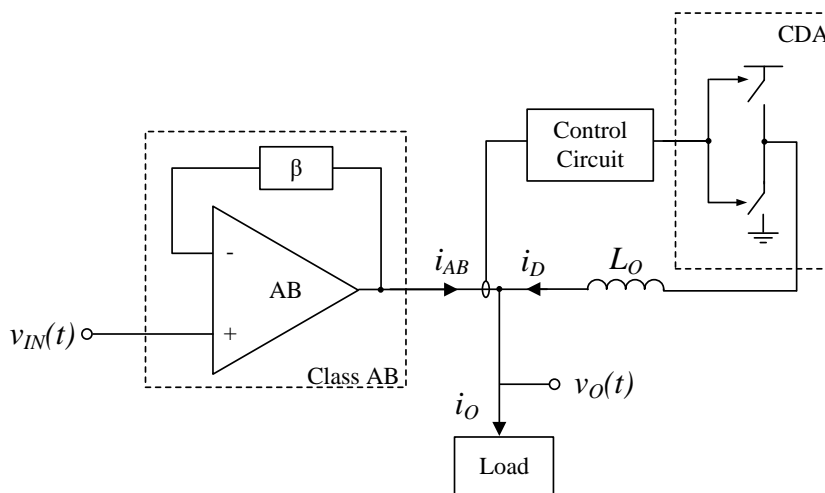


Fig. 1-4: Block diagram of a hybrid CDA

In the contrast, the hybrid CDA comprising a wideband Class AB amplifier and a power-efficient CDA, depicted in Fig. 1-4, generally features wider bandwidth (e.g. 20MHz [66, 74, 75]). This is because the Class AB amplifier therein generally features wider bandwidth and better linearity compared to the CDA. By embodying a Class AB amplifier in parallel with the CDA, the hybrid CDA [65-78] is able to achieve better overall performance for ET PAs (in terms of bandwidth, power-efficiency and noise), compared to other approaches such as the CDA-only [58-64] and the Class AB amplifier-only [81] architectures. In view of this, the hybrid CDA is ubiquitous as the choice of

supply modulator for ET PAs and it is the architecture of interest in our designs. The hybrid CDA for ET PAs will be reviewed in detail in Chapter 2.

Although there are considerable research and development efforts from both academia and industrial [55-80], the design-art of hybrid CDA for ET PAs is immature. At this juncture, the major limitation of state-of-the-art hybrid CDAs [58-74, 76-78, 81] is their limited (and insufficient) bandwidth of $\leq 20\text{MHz}$. The hybrid CDA with bandwidth $\leq 20\text{MHz}$ is largely incompatible with LTE-A whose bandwidth is 40MHz-100MHz. Put simply, a hybrid CDA with very-wide bandwidth is highly desirable for wideband applications, such as LTE-A.

Furthermore, another limitation of state-of-the-art ET PAs is that the supply modulator therein is usually designed and optimized for single communication standard [58-78, 81], e.g. LTE, but when applied to a different standard, they are either incompatible or poorly optimized in terms of power-efficiency. However, modern communication devices, including smartphones and tablets, usually embody multiple communication standards, and each standard requires different bandwidth, peak-to-average power ratio (PAPR) [87, 88], output power, etc. Although multiple RF PAs are embodied to support multiple communication standards, only one supply modulator is used due to limited IC area and cost. According to the operation mode of the communications devices, the supply modulator needs to provide the power supply to the RF PA which is in operation. In view of this, there is a real need to design novel hybrid CDA architectures and pertinent circuits that can be optimized differently for multiple communication standards.

In summary, there are strong motivations to improve the performance of the audio CDA for driving speakerphones and the hybrid CDA for ET PAs in smartphones. For audio CDAs, there is a need to complete analytical investigations, for instance, an analytical investigation to ascertain the mechanisms of noise in the AC ground and their ensuing effect to the PSRR and PS-IMD. For hybrid CDAs, there is a need to design novel hybrid CDA architectures/circuits to achieve improved performance over the state-of-the-art, in terms of bandwidth, power-efficiency and output noise.

1.2 Objectives and Scope

In view of aforementioned motivations, the broad objective of this Ph.D. program pertains to the analysis and practical design of switching amplifiers (in smartphones) with substantially improved specifications over the state-of-the-art. The specific objectives are:

- (i) To analytically investigate the nonlinearities relating to power supply (PSRR and PS-IMD) of the audio PWM CDAs, and to derive the analytical expressions for the said PSRR and PS-IMD. Finally, to verify the said derivations on the basis of HSPICE simulations and on practical measurements on discretely-realized CDAs.
- (ii) To investigate the power dissipation mechanisms of the hybrid CDA (serving as the supply modulator) for a wideband ET PA, with the objective of reducing the power dissipation and extending the bandwidth of the supply modulator. This investigation includes analytical analysis of the effect of the propagation delay to the hysteresis current of the hybrid CDA. Based on the said investigations, to

propose a novel architecture to improve the power-efficiency and extend the bandwidth of the hybrid CDA. Furthermore, to monolithically realize the said proposed architecture using a standard complementary metal oxide semiconductor (CMOS) process. Finally, to verify the efficacy of the proposed architecture on the basis of physical measurements on monolithic prototypes, thereby demonstrating the substantially improved performance of the proposed hybrid CDA in terms of lower power dissipation, and extended bandwidth.

- (iii) To investigate the design challenges of the hybrid CDA (serving as the supply modulator) for multi-standard RF communication protocols, e.g., LTE, LTE-A, WCDMA, etc., and to analytically analyze the optimum switching frequency to achieve maximum power-efficiency in all said protocols. Based on the investigations, to propose a multi-mode hybrid CDA with a novel architecture to optimize the power-efficiency, whose modus operandi self-adjusts according to the characteristics of the input envelope signals. Furthermore, to monolithically realize the said proposed design using a standard CMOS process. Finally, to verify the efficacy of the proposed architecture on the basis of physical measurements on monolithic prototypes, thereby demonstrating the substantially improved power efficiency of the proposed hybrid CDA for multi-standard communications protocols.

1.3 Contributions

The major contributions for this Ph.D. program are largely reported in journal

papers [39, 89, 90 (in preparation)] and conference publications [40, 41, 57]. To the best of the author's knowledge, all contributions delineated herein are novel and unreported in literature. These contributions are congruous to the aforementioned objectives for this Ph.D. program.

The contributions pertaining to objective (i) include:

- (a) An investigation to discover the mechanisms of noise in the AC ground and their ensuing effect to the PSRR and PS-IMD of open-loop and closed-loop audio PWM CDAs,
- (b) An investigation to discover the effect of the resistor and capacitor mismatch based on a realistic fully-differential integrator model (vis-à-vis the oversimplified single-ended integrator model),
- (c) An investigation to ascertain the PSRR of the 3-state BTL PWM CDA from single-feedback topology to double-feedback topology.

The contributions pertaining to objective (ii) includes:

- (d) An investigation into the power dissipation mechanisms of the hybrid CDAs (serving as the supply modulator) for a wideband ET PA, including analytical analysis of the effect of the propagation delay to the hysteresis current of the hybrid CDA,
- (e) The proposal of a delay-based hysteresis controller embodying a novel high-speed current comparator whose reference current (threshold current) is zero, thereby achieving higher power-efficiency and simpler hardware,

- (f) The proposal of a novel Class AB amplifier which features a high bandwidth and accurately controlled quiescent current,
- (g) The realization of monolithic hybrid CDA prototypes embodying the proposed design in (e) and (f) using a commercial 180nm CMOS process. On the basis of physical measurements on the monolithic prototypes, the proposed hybrid CDA features simultaneously the widest bandwidth (40MHz), yet with high output power, high peak efficiency, high output voltage swing and low output ripple noise.

The contributions pertaining to objective (iii) includes:

- (h) An investigation into the design challenges of the hybrid CDA (serving as the supply modulator) for multi-standard applications and analytically analysis of the optimum switching frequency to achieved maximum power-efficiency,
- (i) The proposal of a dual-mode Sigma-Delta control which self-adjusts the operation mode of the hybrid CDA according to according to the characteristics of the input envelope signals, thereby achieving high power-efficiency for multiple communication standards,
- (j) The proposal of an adaptive biasing Class AB amplifier which self-adjusts the bias current to reduce the quiescent power dissipation according to the characteristics of the input envelope signals,
- (k) The realization of monolithic hybrid CDA prototypes embodying the proposed design in (i) and (j) using a commercial 180nm CMOS process. On the basis of physical measurements, the proposed design supports a wide range of

communication standards yet with optimized power-efficiency, and without compromising bandwidth and switching noise. The prototype hybrid CDA features 6% power-efficiency improvement, and peak efficiency of ~91%. For tracking 40MHz LTE-A envelope signals, the prototype hybrid CDA achieves 85% efficiency at 1.8W output power and remains >80% over a wide range of output power.

1.4 Organization of the Thesis

This thesis is organized in the following manner.

In Chapter 1, the introduction and the overview of this thesis are presented, including the background and motivations, objectives and scope, and contributions.

In Chapter 2, a comprehensive literature review on the audio CDA and the hybrid CDA for ET PAs is provided. The commonly used modulation schemes, output stage and practical design considerations for the audio CDA are reviewed. An in-depth review of the hybrid CDA for ET PAs will be subsequently provided, including the control schemes, operating principle and design considerations.

In Chapter 3, the PSRR and PS-IMD of audio PWM CDAs are investigated. This chapter commences with an investigation of the PSRR and PS-IMD of three prevalent open-loop CDA structures with various carrier generators, taking into consideration the effect of the supply noise in the AC ground; this serves as a preamble to the following investigation into the PSRR of the ubiquitous 3-state BTL closed-loop PWM CDAs. Said

closed-loop PWM CDAs include non-ideal AC ground and mismatches of resistor pairs and capacitor pairs. The important practical circuit parameters affecting the PSRR are thereafter discussed. The analytical derivations are verified on the basis of HSPICE simulations and practical measurements on discretely-realized CDAs.

In Chapter 4, we describe a wideband hybrid CDA comprising a proposed delay-based hysteresis controller, proposed wideband Class AB amplifier, and CDA for ET PAs. This chapter commences with an investigation into the power dissipation mechanisms of the hybrid CDA for a wideband ET PA, including the analytical analysis of the effect of the propagation delay (a previously unexploited but imperative parameter) to the hysteresis current of the hybrid CDA. Based on the said investigations, a delay-based hysteresis controller and a wideband Class AB amplifier with an accurate quiescent current control are proposed. The design of the prototype ICs embodying said innovations is presented. The measurements thereto are thereafter benchmarked against reported state-of-the-art designs. When compared to the benchmarked designs, the prototype hybrid CDA demonstrates significant improvements, particularly the bandwidth, output power and peak efficiency.

In Chapter 5, we investigate the design challenges of the hybrid CDA (serving as the supply modulator) for multi-standard RF communication protocols, and analytically analyze the optimum switching frequency for maximum power-efficiency. Based on the investigations, a dual-mode Sigma-Delta control and an adaptive biasing Class AB amplifier are proposed to achieve optimized power-efficiency by self-adjusting the operation according to the characteristics of the input envelope signals. The monolithic prototype hybrid CDA fabricated in a commercial 180nm CMOS process is measured.

With the proposed designs, the static/dynamic power-efficiency has been improved significantly and remains high for a wide output power range.

In Chapter 6, conclusions of this Ph.D. program are drawn and recommendations for further work are presented.

Chapter 2 Literature Review of Audio Class D Amplifiers

This chapter provides a comprehensive and critical review of the audio CDA and the hybrid CDA for ET PAs. The purpose of this serves as a preamble to the contributions in this Ph.D. program delineated in the following chapters.

2.1 A Review of Audio Class D Amplifiers

The concept of the CDA can probably be attributed to Reeves in the 1950s [34]. Interestingly, CDAs were not widely accepted in the early years largely due to the poor performance of power transistors, particularly their low switching speed and high switching loss. As expected, over time with improvements in process technology and innovative circuit designs, the design-art of CDAs is relatively mature where CDAs are ubiquitous in audio-related devices, including the smartphones (as the speakerphone driver), tablets, TVs [12, 32], etc. The performance of present-day CDAs is generally satisfactory – meeting high fidelity standards, particularly with $\text{THD+N} < 0.01\%$ and $\text{PSRR} > 80\text{dB}$ [5, 8, 11, 13, 14].

CDAs typically comprise a modulator, an output stage and a load (typically a loudspeaker and possibly a preceding lowpass filter). For ease of interpretation, a simplified block diagram of an audio CDA is shown in Fig. 2-1.

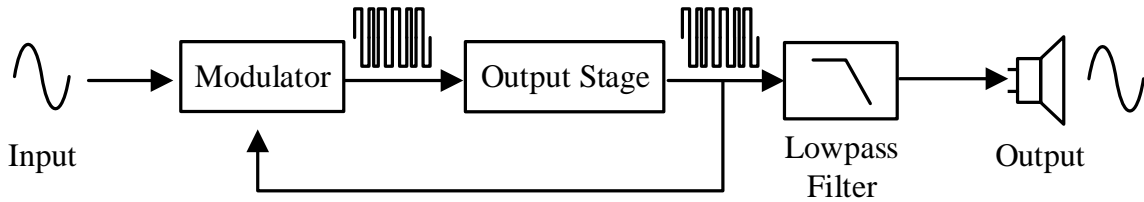


Fig. 2-1: Block diagram of a CDA

The functionality of the various sub-blocks is as follows. The modulator modulates the analog input signal into digital-like switching signal, which controls the switching of the output stage. CDAs are often categorized according to their modulation schemes. The commonly used modulation schemes for CDAs include PWM [5, 8, 9, 12, 18, 20, 23, 33], Sigma-Delta [2, 6, 42], and Bang-bang Control [19, 27]. The judicious selection of an appropriate modulation scheme is particularly imperative because it largely determines the non-linearities, power dissipation, hardware simplicity, and hence performance, IC area, cost, etc. The details of the different modulation schemes, including their advantages and drawbacks, will be provided in Section 2.1.1.

The output stage of the CDAs [35, 36] serves to provide sufficient power to drive the loudspeaker load. Typical loudspeakers have low impedance ratings of 4Ω - 32Ω . The output stage typically occupies $>50\%$ of the total active IC area and dissipates $\sim 90\%$ of

the total power. The critical blocks of the output stage and the output stage topologies will be reviewed in Section 2.1.2 later.

The practical audio CDA designs involve a complete/unambiguous set of design considerations [15, 16]. Parameters that are generally quoted describe the fidelity and power-efficiency of the CDAs. In view of the interest of this Ph.D. research program, a more in-depth review of the design considerations of PWM CDAs will be provided in Section 2.1.3. It would lend some insights into the challenges for the analysis and design of state-of-the-art CDAs.

2.1.1 Modulation Schemes

PWM CDAs

Amongst the commonly used modulation schemes, PWM [5, 8, 9, 12, 18, 20, 23, 33] is arguably the most prevalent due to its relatively simple hardware, moderate signal distortion, and relatively low power dissipation. At this juncture, most commercial CDAs are based on this modulation scheme.

The schematic of an open-loop PWM CDA is depicted in Fig. 2-2. The waveforms at the pertinent nodes of the open-loop PWM CDA are presented in Fig. 2-3. The carrier generator therein generates the carrier signal V_C , which is typically a triangle or saw-tooth wave. The PWM modulator compares the input audio signal V_{in} to V_C . V_M is the resulting high frequency PWM signal and V_{out} is the replica of V_M which is capable of driving the load. As shown in Fig. 2-3, the carrier frequency is designed to be much

higher than the input signal frequency to generate the PWM signal. The carrier frequency is the switching frequency of the CDA, which is typically a few hundred kHz.

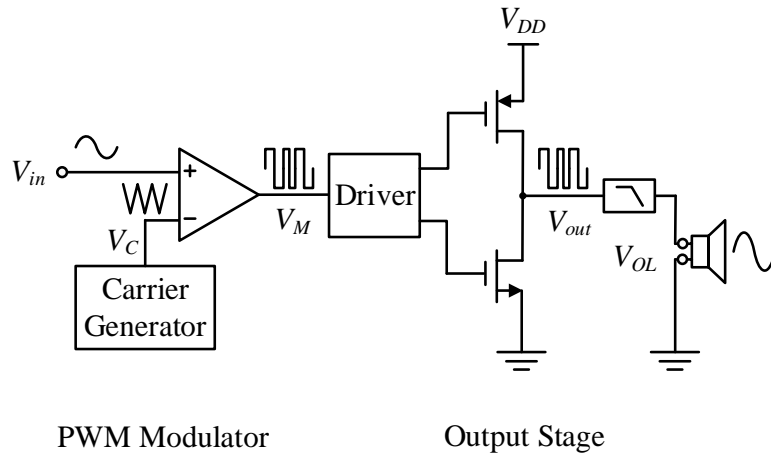


Fig. 2-2: Schematic of an open-loop PWM CDA

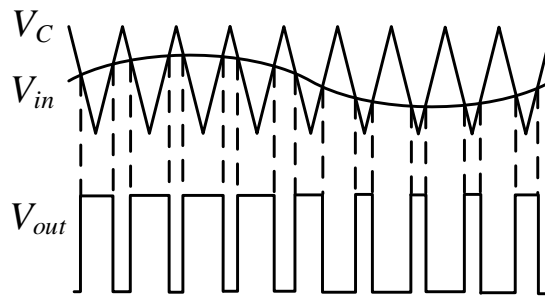


Fig. 2-3: Waveforms of a PWM CDA

The analysis of PWM signals is well-established. Specifically, the double-Fourier expression for a PWM signal generated from an ideal PWM amplifier (i.e., the carrier generator, comparator, output stage and the output lowpass filter are ideal) is expressed in eqn. (2.1) [51].

$$\frac{V_{out}}{V_{DD}} = M \cos(2\pi f_{in} t) + 4 \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{J_n\left(\frac{m\pi M}{2}\right)}{m\pi} \cos(4m\pi f_{sw} t + 4n\pi f_{in} t) \sin\left(\frac{m+n}{2} \pi\right) \quad (2.1)$$

where V_{DD} is the supply voltage, M is the modulation index, f_{in} is the input frequency, f_{sw} is the switching frequency, and $J_n()$ is the Bessel function of the first kind with order n .

The first term in eqn. (2.1) is the replica of the input signal, which is the desired output. The second term comprises the unwanted distortion components due to the intermodulation between the carrier and the input signal. As we mentioned earlier, the carrier frequency is typically much higher ($\sim 10x$) than the input signal. This is to push the unwanted distortion components to high frequencies. The lowpass filter at the output stage can largely attenuate the high frequency distortion components. In this manner, the output audio signal, V_{OL} , is a replica of the input signal, V_{in} , with very-low distortion.

As shown in eqn. (2.1), an ideal PWM CDA does not introduce any (audible) distortion or noise to the output signal [51]. Nevertheless, practical open-loop PWM CDAs suffer from severe distortions and noise, largely arising from non-ideal circuit blocks, such as the non-ideal carrier generator or the non-ideal output stages [35, 36]. Moreover, the open-loop PWM CDAs are very sensitive to supply noise, i.e., their PSRR is undesirably low (e.g., unacceptable 6dB [37]). A noisy supply could consequently exacerbate the noise of an open-loop PWM CDAs. In short, the open-loop PWM CDAs feature simple hardware but with compromised fidelity. Not unexpectedly, the open-loop PWM CDAs are used only in ultra-low power applications such as wearable devices and hearing instruments, where the hardware simplicity is imperative.

In view of the disadvantages of the open-loop PWM CDAs, the closed-loop PWM CDAs are prevalent in practice. Fig. 2-4 depicts the schematic of a single-feedback PWM CDAs comprising an integrator, PWM modulator, output stage, feedback network of R_1 and R_{fb1} , and load with a lowpass filter. Based on negative feedback theory, it is intuitive to appreciate that the feedback loop would suppress the noise induced within the loop. In other words, the closed-loop PWM CDAs would feature higher fidelity and better noise-immunity compared to the open-loop counterparts, but at the cost of increased hardware complexity. Not unexpectedly, the closed-loop PWM CDAs is the most commonly used topology for audio applications ranging from low power (<1W) to high power (>20W). Therefore, the CDAs of interest in this Ph.D. program are the closed-loop PWM CDAs. A more in-depth review of PWM CDAs will be provided in Section 2.1.3.

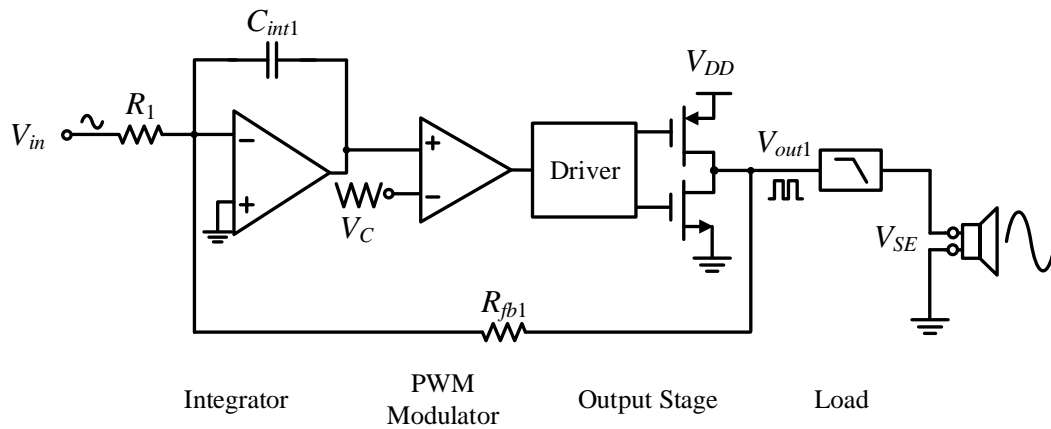
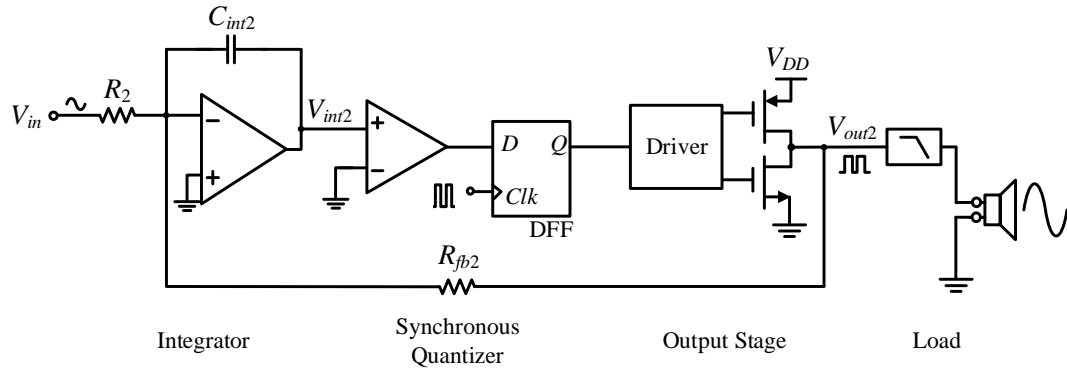


Fig. 2-4: Schematic of a single-feedback PWM CDA

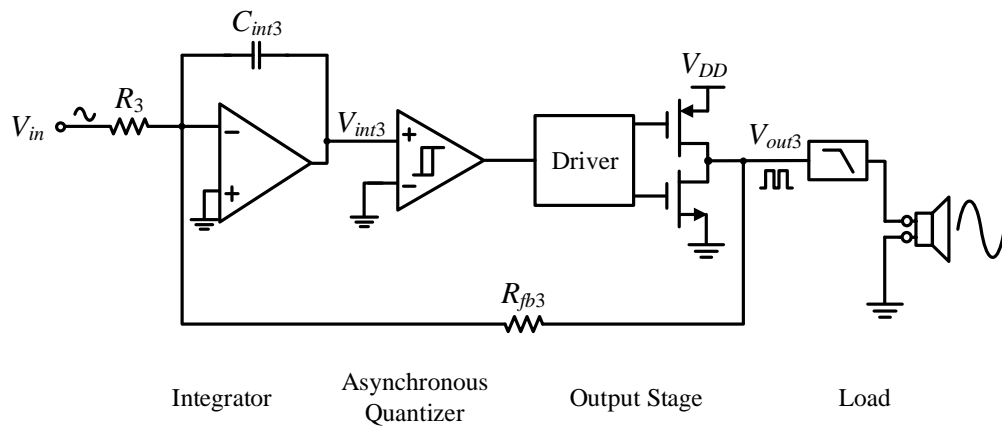
Sigma-Delta CDAs

The Sigma-Delta modulation [2, 6, 42] is an alternative modulation scheme. Compared to the closed-loop PWM CDAs, Sigma-Delta CDAs generally embody a higher-order modulator with higher switching frequency (clock frequency) [42]. Although they generally feature higher fidelity and lower noise level, the penalty includes the cost of increased switching frequency (hence increased power dissipation) and hardware complexity. Put simply, although it is desirable that Sigma-Delta CDAs be implemented in high orders to target applications with high fidelity, the cost in terms of compromised power-efficiency and hardware can be high.

A conventional Sigma-Delta CDA includes an integrator, a quantizer, an output stage, a RC feedback network and a load. In view of the design of the quantizer, Sigma-Delta CDAs can be categorized as synchronous and asynchronous Sigma-Delta, shown in Figs. 2-5 (a) and (b), respectively. The integrator performs a time integration of the difference between the input signal, V_{in} , and the output signal, V_{out2} or V_{out3} . The output of the integrator, V_{int2} or V_{int3} , is fed to the quantizer. The quantizer functions as a single-bit A/D converter generating digital-like waveforms, and the output stage delivers sufficient power to the load.



(a)



(b)

Fig. 2-5: Schematic of single-feedback CDAs with (a) synchronous Sigma-Delta, and (b) asynchronous Sigma-Delta modulation scheme

The quantizer in the synchronous Sigma-Delta CDA (Fig. 2-5 (a)) is realized by a comparator followed by a D flip flop (DFF). The DFF samples the output of the comparator at a high clock frequency. Consequently, instead of varying the pulse widths in the PWM CDA, the synchronous Sigma-Delta CDA varies the number of pulses in a given time window. The synchronous Sigma-Delta modulation scheme is hence also

known as a form of pulse density modulation (PDM). The quantization noise arises from the finite sampling rate, i.e., the clock frequency determines the quantization noise. It is interesting to note that the switching frequency of the synchronous Sigma-Delta CDAs varies with the magnitude and frequency of the input signals – this is unlike the case for PWM CDAs whose switching frequency is fixed and determined by the frequency of carrier signal (V_C in Fig. 2-2 and Fig. 2-4).

On the other hand, the asynchronous quantizer (see Fig. 2-5 (b)) is typically implemented using a hysteresis comparator. The asynchronous Sigma-Delta CDA theoretically has zero quantization noise [43] with a PDM output signal. However, the time of switching is not synchronized and is largely dependent on the input signal. This is because the pulse widths of the asynchronous Sigma-Delta CDA are controlled by a continuous-time comparator instead of a clocked comparator in the synchronous Sigma-Delta CDA. The signal-dependent switching components might undesirably intermodulate with other signals if more than one channel is embodied in a signal IC (for instance, stereo comprising two audio channels resulting in a ‘beating’ noise). This could potentially seriously degrade the fidelity.

Bang-Bang CDAs

Fig. 2-6 depicts the schematic of a Bang-Bang control CDA [19, 27], which comprises a Bang-Bang controller (realized using a hysteresis comparator), an output stage, a RC feedback network and a load. The RC feedback network feeds back the output signal. The error signal, V_e , is the difference between the input signal, V_{in} , and the output

signal, V_{out4} . The output signal is ideally a replica of the input signal for Gain=1. By comparing V_e with the hysteresis band, the Bang-Bang controller generates digital-like switching signals. Finally, the analog signal is obtained at the filter output.

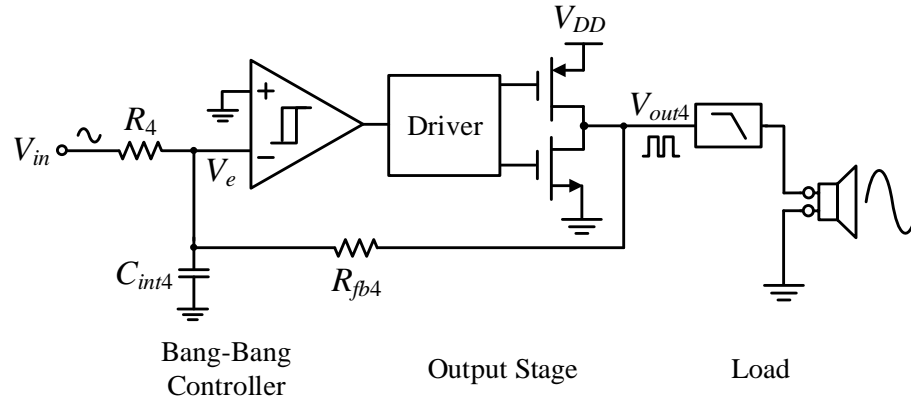


Fig. 2-6: Schematic of a Bang-Bang control CDA

Of the reported switching modulation schemes, CDAs based on Bang-Bang control modulation are arguably the most advantageous in terms of power-efficiency and hardware simplicity. When compared to the PWM and Sigma-Delta CDAs, the Bang-Bang CDA does not require an integrator that consumes relatively large quiescent power is required for Bang-Bang control CDAs. Further, there is no need for the carrier generator or clock signal. Instead, the Bang-Bang controller can be realized using an ultra-low power hysteresis comparator, and the switching frequency of a conventional Bang-Bang CDA is relatively low. Due to aforesaid reasons, the Bang-Bang CDA features relatively low power dissipation and relatively simple hardware. However, Bang-Bang CDAs are deficient in fidelity and noise immunity. Hence, the application space of

Bang-Bang CDAs is limited, particularly to low-voltage power-critical applications, such as hearing instruments (hearing aids).

2.1.2 Output Stage

As discussed earlier, the output stage of the CDA [35, 36] is a critical block due to its large size (in IC area, hence costly) and high power dissipation. The block diagram of a typical output stage is shown in Fig. 2-7. It comprises two power transistors with high-side and low-side drivers, dead-time circuit, control logic and protection circuit.

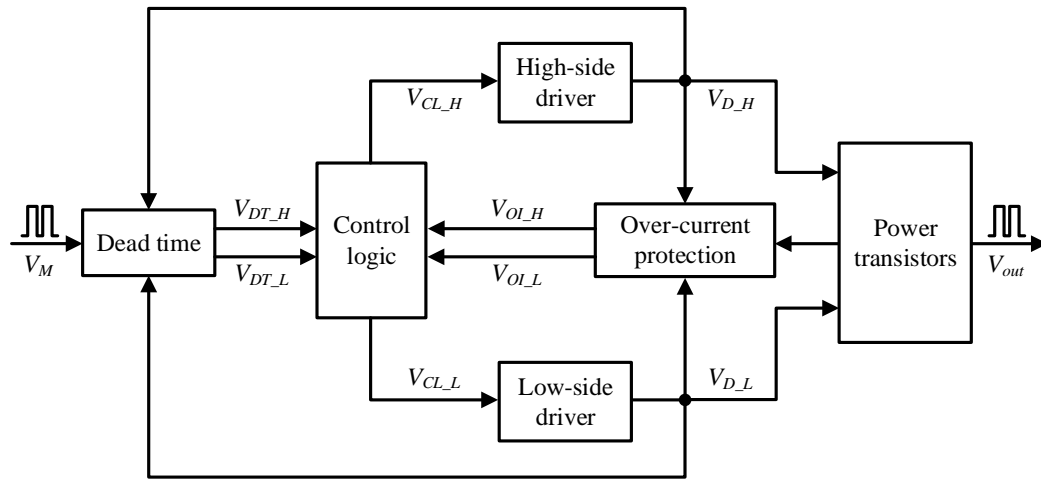


Fig. 2-7: Block diagram of a typical output stage in CDAs

The size of the power transistors is generally large to feature low output impedance and provide sufficient driving capability to the load. These large power transistors have relatively large parasitic capacitance, and these large capacitances are

accommodated by the high-side and low-side drivers serving to provide large driving signals, V_{D_H} and V_{D_L} .

It is important to prevent the power transistors from turning on simultaneously, because a large short-circuit current will flow between the supply and the ground. This short circuit current is high because the resistance of the power transistors is small (e.g. typically in the order of $\sim 0.1 \Omega$ for an 8Ω load) leading to a low resistance path between the supply and ground. To prevent this undesired short circuit current, a dead time circuit is generally embodied in the output stage to contribute to a short dead time interval (typically 10ns~50ns) [11, 22, 44, 45].

The over-current protection block protects the CDAs from damage [46] such as the output unintentionally connected to ground. The outputs of the protection block, V_{OI_H} and V_{OI_L} , and the outputs of the dead time, V_{DT_H} and V_{DT_L} , are sent to the control logic of the output stage, and the control logic controls the output of the power transistors by V_{CL_H} and V_{CL_L} . When the current of the output stage is within normal operation range, V_{CL_H} and V_{CL_L} follow V_{DT_H} and V_{DT_L} , respectively. When the output current exceeds the reference value, the control logic automatically turns off both power transistors for protection. We will now review design techniques and considerations pertaining to each function block in turn.

Design of Power transistors and Drivers

The output power transistors and their drivers can be realized either as PMOS-cum-NMOS configuration (i.e., standard CMOS inverter topology) or as NMOS-cum-NMOS configuration, depicted in Figs. 2-8 (a) and (b), respectively. Both configurations are prevalent for CDAs.

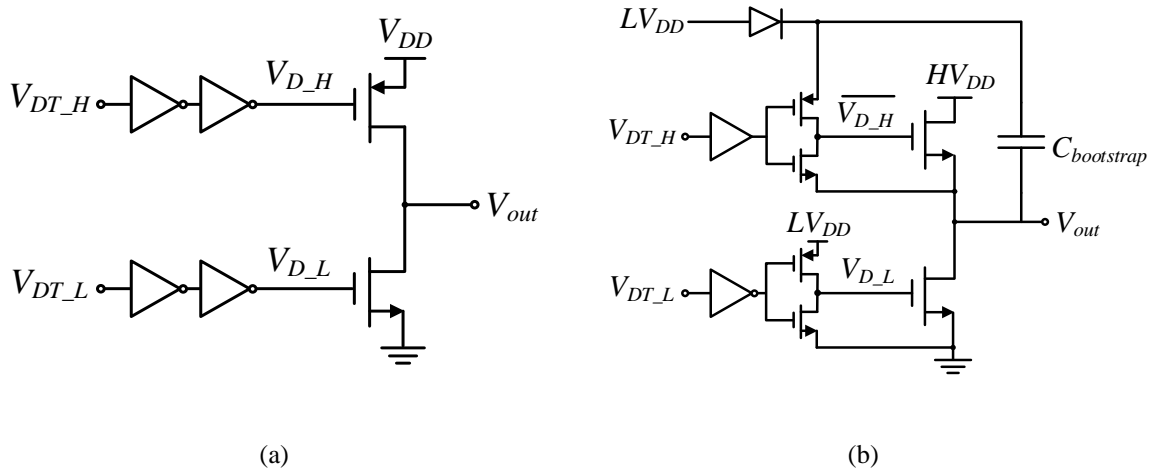


Fig. 2-8: Schematic of power transistors and their drivers in (a) PMOS-cum-NMOS configuration
(b) NMOS-cum-NMOS configuration

The PMOS-cum-NMOS configuration features simpler hardware implementation and with fewer external components. Nevertheless, the major drawback of PMOS-cum-NMOS configuration is its higher switching power dissipation compared to the NMOS-cum-NMOS configuration. This is because the on-impedance of the NMOS transistors is typically 2~3x lower than the PMOS transistors of the same size [38]. In other words, to maintain the same on-impedance on both sides, the size of the PMOS transistors is generally 2~3x of the NMOS transistors, resulting in a larger area size and larger parasitic capacitance (hence larger switching losses). Moreover, in PMOS-cum-NMOS

configuration, the driving signals are in full swing (from ground to V_{DD}) [5, 8] to turn on and off the PMOS and NMOS transistors. In contrast, the voltage swing of the driver signals in NMOS-cum-NMOS configuration is smaller to turn on and off the NMOS transistors.

In practical designs, the PMOS-cum-NMOS configuration is generally employed in the low-to-medium voltage (<5V) applications, such as smartphones where the supply voltage is relatively low (e.g., 3.6V) and the form-factor is desired to be small. On the other hand, the NMOS-cum-NMOS configuration is commonly used in high voltage (>10V) applications [36]. In view of the merits and drawbacks of the output stage configurations and congruous with the aforesaid objectives in this Ph.D. program, the PMOS-cum-NMOS configuration is adopted in our design.

Design of Dead-time Circuit

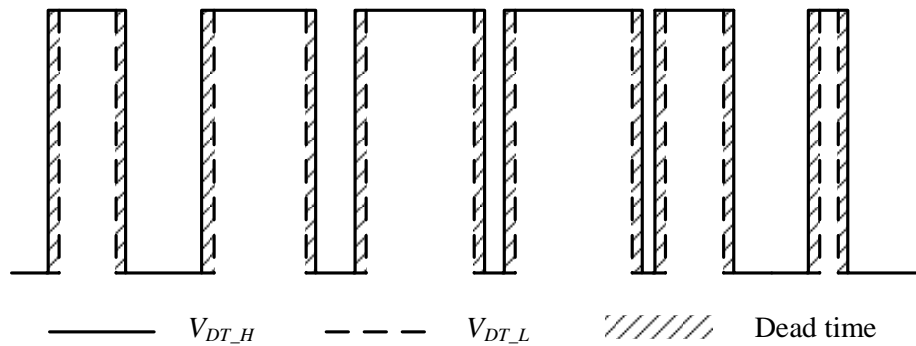


Fig. 2-9: Typical waveforms of the dead time circuit

Fig. 2-9 depicts the typical waveforms of the dead time circuit, where the dead time is indicated by the shaded area in the figure.

As explained earlier, the dead-time circuit serves to add a small time-interval (typically tens of ns) to the output stage to ensure that the two output power transistors (one is connected to the power supply and the other connected to the ground) will not be simultaneously turned on [22]. This is critical because the on-resistance of the power transistors in the output stage is very small (in the order of $\sim 0.1\Omega$) and a low resistance path from supply to the ground will be formed if the said power transistors are turned on simultaneously. The ensuing large current could degrade the power-efficiency, and potentially damage the output transistors. By embodying the dead-time circuit, the power efficiency and reliability of the CDAs can be improved. However, a long dead-time in turn deteriorates the linearity of the CDA. This will be further explained in Section 2.1.3.

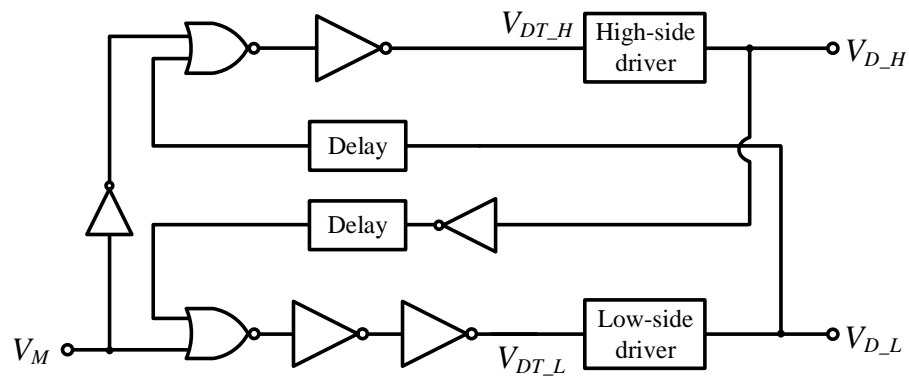


Fig. 2-10: Schematic of a dead time circuit embodying non-overlapping logic method

The non-overlapping logic method [44], depicted in Fig. 2-10, is a commonly used method to realize the dead time circuit due to its high robustness compared to other methods such as controlling the skewing of the power transistors and inducing an offset voltage [45]. The robustness of this design is affected by the feedback mechanism therein.

Design of Over-Current Protection Circuit

The over-current protection circuit is imperative for CDAs to avoid outright device failure. The simplest way to implement the protection circuit is using resistor based current sensing [46], depicted in Fig. 2-11(a). The operation principle is straightforward – when the output current of the power transistors exceeds the reference current over the resistors R_L and R_H (i.e., $V_{ref}/R_{L(H)}$ in Fig. 2-11(a)), the output of the over-current protection circuit, V_{OI_H} and V_{OI_L} , will ‘on’ ($V_{OI_H(L)}=V_{DD}$). The control logic would then turn ‘off’ the corresponding over-current power transistors. Although the resistor based current sensing is a simple method to realize, the embodiment of the integrated resistors in series results in many drawbacks, including the relatively low power-efficiency and high sensitivity to process variations.

The current-mirror based protection circuit is another reported method to implement over-current protection circuit [46], which is depicted in Fig. 2-11(b). Compared to the resistor based current sensing, this current-mirror based protection circuit does not introduce additional resistance into the output stage; thereby improving the power-efficiency. Furthermore, instead of using the absolute value of resistors with relatively high process variations, the current-mirror based protection circuit utilizes the

matching ratio of the current mirrors, which is able to improve the accuracy of the protection circuit significantly.

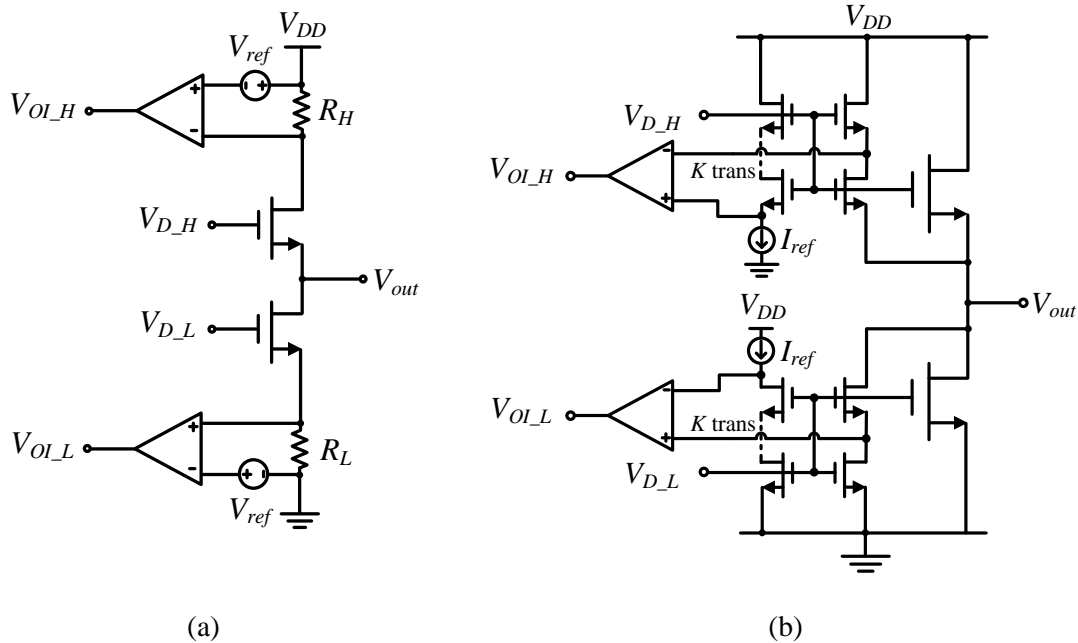


Fig. 2-11: Schematic of over-current protection circuits using (a) resistor based current sensing, and (b) current-mirror based current sensing

Output Stage Topologies

The output stage of CDAs can generally be categorized into two topologies: single-ended (also known as half-bridge, shown in Fig. 2-12(a)) and BTL (also known as full bridge, shown in Fig. 2-12(b)). In the single-ended CDA, the load is connected between the output, V_{SE} , and the ground. The BTL output stage, on the other hand, comprises two single-ended output stages and generates a differential output signal, V_{BTL} , at the load.

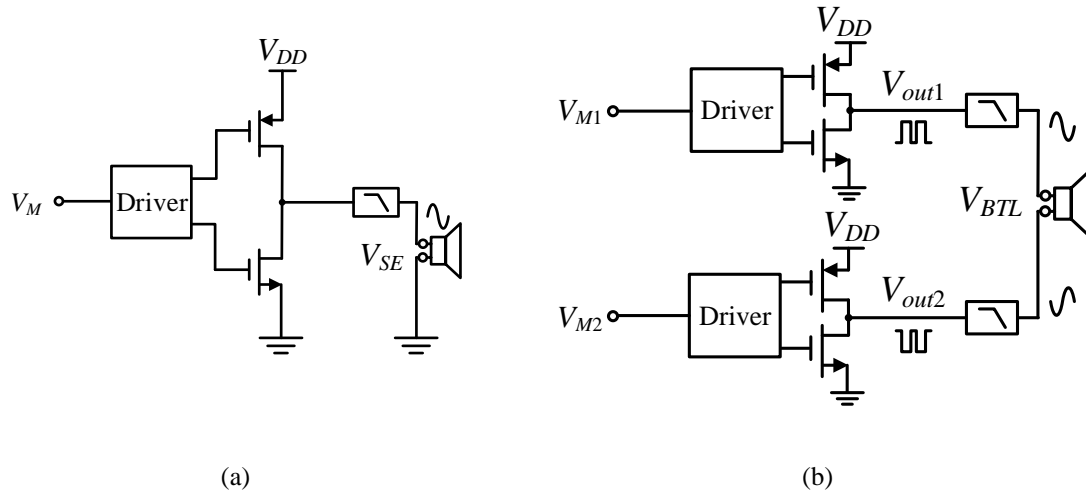


Fig. 2-12: Schematic of CDAs embodying (a) single-ended, and (b) BTL output stage

Compared to the single-end structure, the BTL output stage features $\sim 4x$ higher output power. This is because the available voltage swing across the load of BTL structure is doubled with the same supply voltage and the same load. The BTL CDAs further feature higher audio performance due to the differential output structure which to a first-order, cancels the harmonics and DC offsets. For instance, the PSRR of a BTL output stage is $\sim 6\text{dB}$ higher than its single-ended counterpart. Nevertheless, single-ended CDAs are potentially simpler (occupying smaller IC area) and have higher power-efficiency (due to lower effective output impedance). Put simply, the single-ended CDAs are more suitable for the applications requiring smaller IC area and higher power-efficiency, whilst the BTL CDAs are more appropriate to the applications with higher output power, lower supply voltage, and better audio performance.

In CDAs, the low frequency components of the resulting switching signals are essentially the desired output signal. The high frequency components, on the other hand,

are the carrier signals modulated (with the input signal) to binary signals that are amplified by switching power devices (a cascade of inverters with increasing aspect ratios) at the output stage. The lowpass filter in the output stage filters the high frequency switching components and recovers the desired audio output signals at the loudspeaker load. In general, the lowpass filter in this non-filterless topology is undesirable because it is bulky, typically increasing the PCB area by ~70% and cost by 30%.

In view of this somewhat serious shortcoming associated with the lowpass filter, there are CDAs without the need for the lowpass filter – filterless CDAs [1, 2, 8, 11, 13, 25, 30, 47, 48] based on the three-state PWM modulation modality; this three-state modulation will be discussed in Chapter 3. The output stage with BTL structure is typically employed for filterless CDA designs. It is well established that as the carrier components are small in these filterless CDAs with BTL output stage, the output lowpass LC filter is not necessary to filter these components.

2.1.3 Design Considerations of PWM Class D Amplifiers

As discussed earlier, it is desirable that an audio CDA deliver high fidelity sound and with high power-efficiency. In this section, we will review the specific requirements (of interest pertaining to the research in this PhD program) of the audio PWM CDA, including: (i) PSRR and PS-IMD, (ii) THD+N, (iii) EMI, and (iv) power-efficiency; and the associated tradeoffs amongst these parameters.

(i) High PSRR and low PS-IMD

The definition of PSRR and PS-IMD [15-21] are expressed in eqns. (2.2) and (2.3), respectively.

$$\text{PSRR} = 20 \log \left(\frac{V_{DD@f_n}}{V_{out@f_n}} \right) \text{dB} \quad (2.2)$$

$$\text{PS-IMD} = 20 \log \left(\frac{\sqrt{V_{out@(f_{in}+f_n)}^2 + V_{out@(f_{in}-f_n)}^2}}{V_{DD@f_n}} \right) \text{dB} \quad (2.3)$$

where f_n is the supply noise frequency, f_{in} is the input signal frequency,

$V_{DD@f_n}$ is the supply noise,

$V_{out@f_n}$ is the output noise component at supply noise frequency f_n , and

$V_{out@(f_{in}+f_n)}$ and $V_{out@(f_{in}-f_n)}$ are the output noise components at frequency $f_{in} \pm f_n$, due to the intermodulation between the input signal and the supply noise.

The PSRR and PS-IMD are parameters that describe the supply-noise susceptibility of a CDA, and constitute some of the parameters that collectively qualifies the linearity of the CDAs. As mentioned in Chapter 1, a high PSRR and low PS-IMD (e.g. PSRR>90dB, PS-IMD<-90dB) are particularly critical in smartphones due to the high integration density in SoCs and their proximity to RF transceivers. Particularly, the CDA with high PSRR and low PS-IMD is able to reduce the audible output noise caused by the GSM and/or 4G signals [49, 50], hence enabling direct battery hookup, thereby obtaining high power-efficiency – the power terminal of the CDA is connected directly to the battery terminals without the power-dissipative low dropout regulator. The elimination of the low dropout regulator further reduces the cost.

At this juncture, the mechanisms of PSRR and PS-IMD for PWM CDAs have been somewhat established [18-20, 51]. The PSRR and PS-IMD of an open-loop PWM CDA can be expressed as:

$$\text{PSRR}_{\text{OL}} = 6\text{dB} \quad (2.4)$$

$$\text{PS-IMD}_{\text{OL}} = 20\log\sqrt{\left(\frac{M}{4}\right)^2 + \left(\frac{M}{4}\right)^2} = (-9 + 20\log M)\text{dB} \quad (2.5)$$

where M is the modulation index.

Based on eqns. (2.4) and (2.5), we can observe that the PSRR of an open-loop PWM amplifier is undesirably low, typically 6dB, and it is independent of the input signal. On the other hand, the PSRR-IMD depends on the input signal (indicated by M). In the worst case ($M=1$), the PSRR-IMD is undesirably high, PS-IMD=-9dB. Therefore, the open-loop PWM amplifier is typically not employed for high fidelity applications.

On the other hand, the PSRR and PS-IMD can be improved by embodying a feedback loop. The PSRR and PS-IMD of a single-feedback closed-loop PWM CDA can be expressed as:

$$\text{PSRR}_{\text{CL}} = 6 + 20\log(1 + LG_{@f_n})\text{dB} \quad (2.6)$$

$$\text{PS-IMD}_{\text{CL}} = 20\log\sqrt{\left(\frac{M/4}{1 + LG_{@(f_n+f_n)}}\right)^2 + \left(\frac{M/4}{1 + LG_{@(f_n-f_n)}}\right)^2}\text{dB} \quad (2.7)$$

where $LG_{@f_n}$ is the loop gain at supply noise frequency f_n , and $LG_{@(f_n+f_n)}$ and $LG_{@(f_n-f_n)}$ are the loop gain at frequency $f_n \pm f_n$.

Based on eqns. (2.6) and (2.7), we can make the following observations. First, similar to the PSRR and PS-IMD of the open-loop PWM CDA, the PSRR of the single-feedback PWM CDA is independent of the input signal and the PS-IMD becomes worse with the increase of the input signal. Second, both the PSRR and PS-IMD are determined by the loop gain, LG . Specifically, the higher the LG , the higher (better) is the PSRR and the lower (better) is the PS-IMD. However, a high LG in the audio frequency range may reduce the carrier attenuation, which undesirably increases the THD+N; see (ii) below. Third, by comparing eqns. (2.4) and (2.6), eqns. (2.5) and (2.7), it is apparent that the closed-loop PWM CDA achieves better PSRR and PS-IMD by embodying a feedback loop. As a result of said improvements, closed-loop PWM CDAs are well accepted and widely adopted for audio applications.

(ii) Low THD+N

The definition of THD [15] is expressed in eqn. (2.8). THD+N comprises both the input signal-related non-linearity of the CDA (i.e., THD) and the output noise (i.e., N) due to the thermal noise, flicker noise, etc. A low THD+N is desirable for high fidelity and high fidelity is easily achieved in state-of-the-art CDAs. For example, the typical reported THD+N is <0.01% [5, 8, 11, 13, 14].

$$\text{THD} = \frac{\sqrt{V_{out @ 2f_{in}}^2 + V_{out @ 3f_{in}}^2 + V_{out @ 4f_{in}}^2 \dots}}{V_{out @ f_{in}}} \quad (2.8)$$

where $V_{out @ f_{in}}$ is the output fundamental component at input signal frequency f_{in} , and

$V_{out@2f_{in}}$, $V_{out@3f_{in}}$ and $V_{out@4f_{in}}$ are the output harmonic components at $2f_{in}$, $3f_{in}$ and $4f_{in}$, respectively.

The mechanisms of THD are well established in literature. In the practical open-loop CDA, the main mechanisms of THD are due to the non-ideal carrier generator [93] and non-ideal output stage [22]. For a practical open-loop PWM CDA, it is difficult, if not impossible, to achieve low THD. This is because the distortions introduced by the non-ideal blocks therein will appear on the output signal directly (without any suppression). Moreover, some non-ideality is intentionally introduced in practical designs to ensure the reliability of the CDAs. For instance, both the limited slew rate and non-zero dead time in the output stage [22] deteriorates the THD in the open-loop PWM CDA. A lower slew rate and a longer dead time will introduce longer and unequal delay at the rising and falling edges of the PWM signal. Consequently, the harmonics of the signal frequency are generated, which do not exist in an ideal PWM signal (refer to eqn. (2.1)). However, the increased slew rate usually results in the increased EMI (see (iii) later), and the dead time, as discussed earlier (refer to Section 2.1.2), is necessary to avoid the short circuit current. Consequently, the THD of a practical open-loop PWM CDA is usually unacceptably high, 2%-5% [22, 93].

The mechanisms of THD in the closed-loop CDA have been reported in literature [22-24]. The main parameters include: (a) distortions introduced by the open-loop PWM CDAs, (b) duty-cycle error, and (c) phase error. As discussed, the THD due to (a) is mainly contributed by the non-ideal carrier generator and non-ideal output stage. Due to the feedback loop, THD in the closed-loop PWM CDA can be considerably reduced by a factor of (loop gain+1). Hence, the THD of closed-loop PWM CDAs is significantly

improved over their open-loop counterparts, typically $<0.01\%$ [5, 8, 11, 13, 14]. On the other hand, the THD due to (b) and (c) arises from the feedback of the PWM signal and the intermodulation distortions between the residual (not fully attenuated) switching component and the carrier signal. These distortions exist even for ideal building blocks, and they are largely affected by design parameters, e.g. loop gain and switching frequency. Although a high loop gain in the audio range suppresses THD due to (a), the increased loop gain undesirably introduces more THD due to (b) [23]. This is because the higher loop-gain inevitably reduces the attenuation of the switching components, resulting in the increased residual switching components in the feedback network.

(iii) Low EMI

The EMI arises from the switching operation of the output stage in the CDAs, generating high frequency noises [28-31]. The sensitive circuits in the proximity, such as RF low noise amplifier, may be affected by the said high frequency components. The EMI of CDA is largely determined by the slew rate of the output stage. This is because the slew rate is mainly limited by charging and discharging the relatively large parasitic capacitance of the power transistors and drivers, and a low slew rate slows down the switching operation of the output power transistors. Consequently, the smooth transition at the output stage generates less high frequency component – and EMI is therefore reduced. It is worthwhile to notice that, as aforesaid, the CDAs with a low slew rate can reduce the EMI but at the cost of increased THD+N.

(iv) High power-efficiency

Power-efficiency is a well-recognized parameter for PAs, which is particularly critical for smartphones. This is because a high power-efficiency translates to the prolonged battery life and reduces wasteful heat dissipation. The mechanisms of the power dissipation in the CDAs are well established [35]. The power transistors and drivers in the output stage (refer to Section 2.1.2) are the main sources of power dissipation where larger size of output stage increases power-efficiency (up to a point of diminishing return [35] where the capacitive load may become dominant and power-efficiency suffers thereafter) but at the cost of large IC area. Specifically, the primarily power dissipation mechanisms are (i) the switching power dissipation due to the parasitic capacitance of the power transistors, (ii) the short circuit current during transitions, and (iii) the on-resistance of the power transistors. The design art thereto is also well-established [35] with reported analytical expressions to ascertain the power dissipation and a systematic design/optimization methodology.

2.2 A Review of Hybrid Class D amplifiers for ET PAs

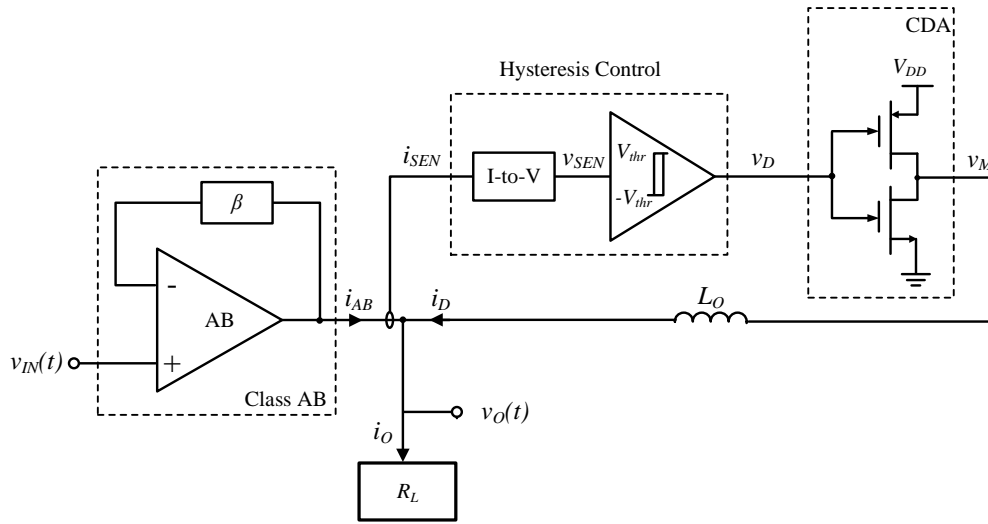
The concept of the hybrid CDA was originally proposed for audio applications (20Hz-20kHz), i.e., as a driver for speakerphones, in 1986 [91]. With the embodiment of a linear Class AB amplifier in parallel, hybrid CDAs [91, 92] feature higher fidelity compared to (non-hybrid) CDAs, but at the cost of decreased power-efficiency due to the embodiment of the power-inefficient linear amplifier. As mentioned earlier, CDAs are now ubiquitous for audio applications for its somewhat satisfactory performance (in terms of PSRR, PS-IMD, THD+N, EMI, and power-efficiency).

As described in Chapter 1, at this juncture, hybrid CDAs [65-78] are increasingly prevalent for ET PAs to track wideband envelope signals (bandwidth >1MHz) due to their higher bandwidth compared to CDAs. In this section, we will review hybrid CDAs for ET PAs in some detail including the control scheme and modus operandi. An in-depth review of design considerations will be subsequently provided. It would lend some insights into the challenges for the analysis and design of state-of-the-art (and beyond) hybrid CDA for ET PAs, thereby providing a preamble to the contributions delineated in the following chapters.

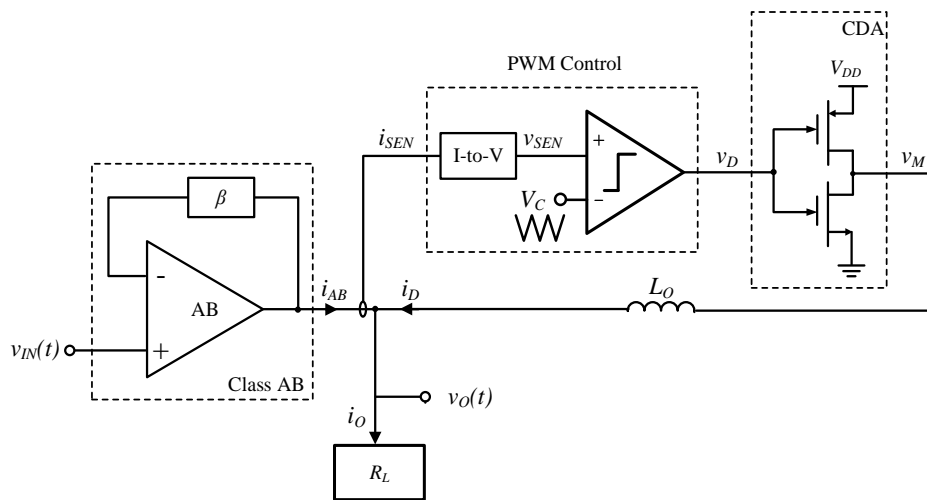
2.2.1 Control Schemes

The hybrid CDA comprises a wideband linear Class AB amplifier, a controller, and a high-efficiency CDA with an external inductor L_O . The resistive load, R_L , of the supply modulator represents/models the RF PA.

Hybrid CDAs can be generally categorized according to their control scheme. There are two commonly used control schemes for hybrid CDAs: hysteresis control, and PWM control, depicted in Figs. 2-13 (a) and (b) respectively. We will now review the hybrid CDA with these two control schemes in turn.



(a)



(b)

Fig. 2-13: Block diagram of hybrid CDAs with (a) hysteresis control, and (b) PWM control

Fig. 2-13(a) depicts the block diagram of hybrid CDAs with hysteresis control. The hybrid CDA has a parallel connection between a wideband Class AB linear amplifier and a high-efficiency CDA. This is because the Class AB amplifier has a wider bandwidth (typically $\sim 100\text{MHz}$) compared to the CDA (hundreds of kHz to several MHz), the CDA features a higher power-efficiency as explained in Section 2.1. By combining the Class AB amplifier and CDA, the hybrid CDA is able to achieve high bandwidth and high efficiency.

In this topology, a large-signal negative feedback network is established to ensure the stability. Specifically, a control block is employed to control the output current, i_D , of the CDA by sensing the output current, i_{AB} , of the Class AB amplifier and comparing it with a reference level. When i_{AB} is high (just above the reference level) the output of the CDA ideally changes from ground to V_{DD} to supply more current, i.e., i_D increases. Similarly, when i_{AB} is low (just below the reference value), the output of the CDA, v_D , ideally changes from V_{DD} to ground to supply less current, i.e., i_D decreases. In this manner, the output current of the low-efficiency Class AB amplifier is minimized – the CDA provides the majority of the current to the RF load, and the Class AB amplifier provides only the ripple current (determined by the reference value) and high-frequency current (to extend the bandwidth).

For the hysteresis control [66, 68, 71, 73-76, 78], the reference level is realized by a hysteresis comparator. Specifically, the hysteresis control embodies a hysteresis comparator with an internal hysteresis $\pm V_{thr}$. The reference level is fixed to $\pm V_{thr}$, and the switching frequency of the hysteresis control depends on the input signal and the design parameters of the hybrid CDA (see Section 2.2.2 later).

Fig. 2-13(b) depicts the block diagram of hybrid CDAs with PWM control. In PWM control [65, 67, 69, 70, 72], i_{AB} is compared with a carrier signal which typically a triangular or a ramp waveform-signal. Similar to PWM CDAs (refer to Section 2.1), the PWM control generate PWM signal, and the reference level is, in fact, changing with the carrier signal. In this case, the switching frequency of the PWM control is independent of the input signal and determined by the carrier frequency.

The loop response of the hysteresis control is faster than the PWM control. In other words, the hysteresis control features wider bandwidth compared to the PWM control. However, the output of the hysteresis control is a PDM signal and the switching frequency of PDM signal varies with the magnitude of the input signal – this is unlike the case of the PWM control. Dynamically changing the switching frequency may introduce wideband spurious emissions at the output of the CDA.

At this juncture, hybrid CDAs based on the hysteresis control and the PWM control are both prevalent. It is prudent to note that depending on the requirements of the specific applications, the aforesaid trade-offs should be carefully considered.

2.2.2 Modus Operandi

Fig. 2-14 [70] depicts the typical current-mode frequency response of the Class AB amplifier, the CDA and the combined hybrid CDA, whose currents are i_{AB} , i_D and i_O , respectively. In the hybrid CDA, the Class AB amplifier not only provides ripple current to suppress the switching noise arising from the switching operation of the CDA, but also

provides current for the high frequency components. The CDA, on the other hand, mainly provides current to the low frequency components. As the low frequency and high frequency components are powered by different amplifiers in the hybrid CDA, the operation of the hybrid CDA for tracking low frequency and high frequency input signals are different.

In the following section, the transition frequency, f_T , in Fig. 2-14 i.e., the frequency between low frequency and high frequency range will first be discussed, followed by the operation of the hybrid CDA in each condition.

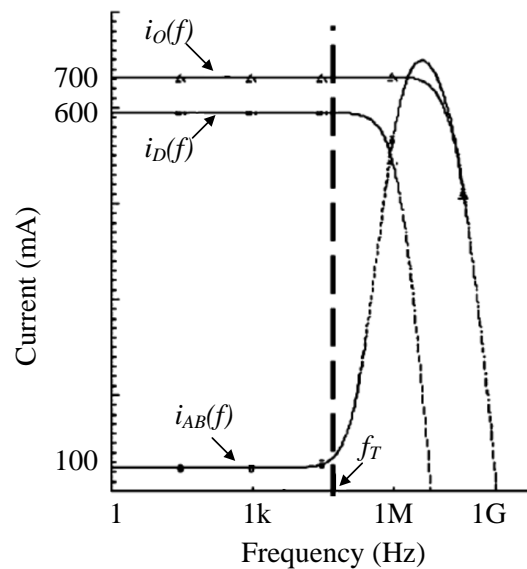


Fig. 2-14: Current-mode frequency response of the Class AB amplifier, the CDA and the combined hybrid CDA

Transition Frequency, f_T

In practical hybrid CDAs for ET PAs, as the voltage swing is generally considered as a large signal, the large-signal analysis method is typically adopted for analysis [66, 68, 84, 92].

Assume that v_{IN} expressed in eqn. (2.9) below is the envelope signal to the hybrid CDA. The desired output voltage, v_O , hence equals to v_{IN} (i.e., $v_O = v_{IN}$) for the hybrid CDA with gain=1.

$$v_{IN} = \frac{1}{2}V_{DD} + \frac{1}{2}V_{DD} \times [A + \alpha \sin(2\pi f_{in}t)] \quad (2.9)$$

where f_{in} is the input signal frequency, A is the DC level,

and α is the AC magnitude of the input signal.

The slew rate, SRi_O , of the desired output current and the slew rate, SRi_D , of current from the CDA are given by [84, 92]:

$$SRi_O = \frac{1}{R_L} \frac{\delta v_O}{\delta t} = \frac{\alpha \pi V_{DD} f_{in} \cos(2\pi f_{in}t)}{R_L} \quad (2.10)$$

$$SRi_D = \frac{v_M - v_O}{L_O} \quad (2.11)$$

where v_M is the output of the CDA in Figs. 2-13(a) and (b).

The transition frequency, f_T , [84] is defined as the frequency where the slew rate of the desired output voltage is equal to the slew rate of the CDA. This means that the CDA can follow the input signals and provide the majority of the output current. Based on eqns.

(2.10) and (2.11), the maximum transition frequency, $f_{T, max}$, is expressed as eqn. (2.12) [92]:

$$f_{T, max} = \frac{R_L}{2\pi L_O} \sqrt{\frac{1}{\alpha^2} - 1} \quad (2.12)$$

$f_{T, max}$ is obtained at $1/2V_{DD}$. This is because the slew rate, SR_{i_D} , of the CDA is at its maximum when the output is $1/2V_{DD}$, and reduces when the output near to ground and V_{DD} . It can be seen from eqn. (2.12) that a smaller L_O translates to a higher f_T . This is intuitive that L_O determines the dynamic response of the CDA, and a small L_O means a higher SR_{i_D} which extends the bandwidth of the CDA. In the hybrid CDA, as f_T determines the current burden of the power-inefficient Class AB amplifier for high frequency components, it is hence desirable for f_T to be higher to reduce the current burden of the Class AB amplifier and the high-efficiency CDA deliver more output current.

Operation in low frequency range

The operation of the hybrid CDA in the low frequency range will now be delineated. Fig. 2-15 shows the details of a typical current for tracking low frequency input signals. In this case, the CDA (i_D) is able to track the input signal closely. The CDA provides the primary current to the RF PA, and the Class AB amplifier (i_{AB}) provides only the ripple current.

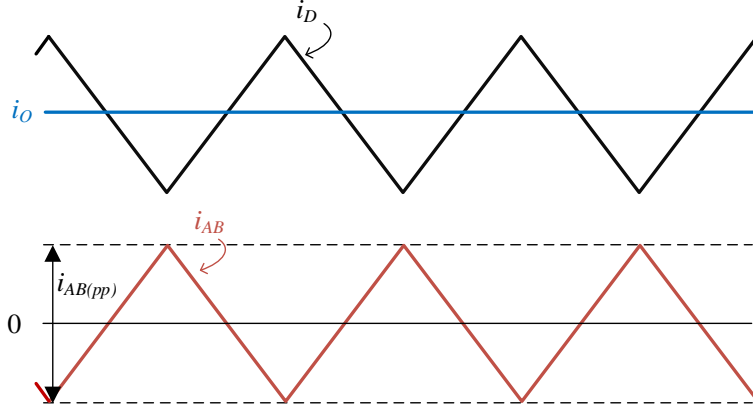


Fig. 2-15: Typical current waveforms of the hybrid CDA for tracking low frequency input signals

It now becomes apparent that for tracking low frequency input signals, there is a tradeoff between the switching frequency of the CDA and the ripple current of the Class AB amplifier – this can be observed from Fig. 2-15. This relationship between the switching frequency, f_{sw} , and the peak-to-peak ripple current, $i_{AB(pp)}$, can be expressed by [66, 84, 92]

$$f_{sw} \times i_{AB(pp)} = \frac{V_{DD}v_O - v_O^2}{L_O V_{DD}} \quad (2.13)$$

In hysteresis control, the peak-to-peak ripple current, $i_{AB(pp)_hys}$, is fixed, which is bounded by the threshold voltage of the hysteresis comparator, $\pm V_{thr}$ in Fig. 2-13(a). Hence, $i_{AB(pp)_hys} = 2V_{thr} \times \frac{i_{SEN}}{v_{SEN}}$ for hysteresis control, and the switching frequency of the hysteresis control, f_{sw_hys} can be expressed by eqn. (2.14a). f_{sw_hys} varies with the output signal v_O , and depends on the design parameters, including the supply voltage V_{DD} and the external inductor L_O . It now becomes apparent that the choice of $\pm V_{thr}$ and L_O should be optimized according to the requirements of bandwidth, output ripple and power-

efficiency [66]; see Section 2.2.3 later. The maximum switching frequency, $f_{sw_hys(max)}$, is obtained at $1/2V_{DD}$, which can be expressed by eqn. (2.14b).

$$f_{sw_hys} = \frac{(V_{DD}V_O - V_O^2)V_{SEN}}{2V_{thr}i_{SEN}L_OV_{DD}} \quad (2.14a)$$

$$f_{sw_hys(max)} = \frac{V_{DD}V_{SEN}}{8V_{thr}i_{SEN}L_O} \quad (2.14b)$$

In PWM control, the operating mechanism is different – the switching frequency, f_{sw_pwm} , is fixed, which equals to the frequency, f_C , of the carrier signal in Fig. 2-13(b), i.e., $f_{sw_pwm}=f_C$. When compared to the hysteresis control, $i_{AB(pp)_pwm}$ in PWM control varies with the input signal, which can be estimated from eqn. (2.15). Similar to f_{sw_hys} in hysteresis control, the ripple current of the Class AB amplifier in PWM control depends on the design parameters, including supply voltage V_{DD} and external inductor L_O ; the maximum ripple current in PWM control is obtained at $1/2V_{DD}$.

$$i_{ab(pp)_pwm} = \frac{V_{DD}V_O - V_O^2}{f_C L_O V_{DD}} \quad (2.15)$$

Operation in high frequency range

For tracking high frequency input signals, the CDA cannot follow the fast-changing input signal. Although the DC component of the input signal is still provided for by the CDA, the AC component is primarily provided for by the Class AB amplifier. For both hysteresis control and PWM control, the switching frequency is independent of the parameters of hybrid CDA and is the same as the input frequency [84], i.e., $f_{sw}=f_{in}$, as

shown in Fig. 2-16. The CDA provides partial current at a slope of $\frac{V_{DD}-v_O}{L_O}$ or $\frac{-v_O}{L_O}$ until the reference level is reached, and the Class AB amplifier provides the remaining current to the load with relatively low power-efficiency.

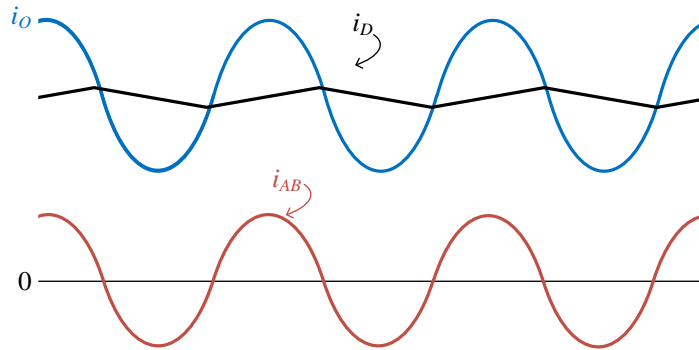


Fig. 2-16: Typical current waveforms of the hybrid CDA for tracking high frequency input signals

2.2.3 Design Considerations

The critical parameters for hybrid CDAs include the output voltage ripple, bandwidth and the power-efficiency. These three parameters are in fact interrelated and the hybrid CDA designs involve tradeoffs between the different parameters. The three parameters and their relationships will now be delineated.

Output Voltage Ripple

As the output of the hybrid CDA serves as the power supply to the RF PA, the noise of the hybrid CDA may introduce noise to the output of RF PA (depending on the

value of the PSRR of the RF PA). This may render the RF PA failing to satisfy the spectrum mask requirements. The output noise of the hybrid CDA is dominated by the output ripple noise (i.e., switching noise) [66, 68, 70, 71], which is due to the switching operation of the CDA. Consequently, the output ripple of the hybrid CDAs would need to be kept low (e.g. 16mV_{pp}) [66].

The output voltage ripple is suppressed by the Class AB amplifier. The Class AB amplifier can be modeled as a voltage source with low output impedance Z_{AB} , expressed in eqn. (2.16a).

$$Z_{AB} = R_{AB} + sL_{AB} \quad (2.16a)$$

where

$$R_{AB} = \frac{R_o}{A_o} \quad (2.16b)$$

$$L_{AB} = \frac{R_o}{2\pi \times GBW} \quad (2.16c)$$

where R_o is the open-loop output resistance,

A_o is the open-loop DC gain, and

GBW is the gain-bandwidth product of the Class AB amplifier.

V_R , peak-to-peak value of the output ripple voltage, can be approximated based on the output impedance of the Class AB amplifier and its output current. V_R is expressed in eqn. (2.17) [68].

$$V_R \approx i_{ab(pp)} \times |Z_{AB}| = \frac{V_{DD}}{4L_O} \times \frac{R_O}{GBW} \quad (2.17)$$

From eqn. (2.17), the following observations are noted for voltage ripple:

(i) Effect of the Class AB amplifier

The Class AB amplifier is required to provide a path of very low impedance over a wide range of frequencies in order to absorb the ripple current in the external inductor L_O , due to the switching operation. It is apparent from eqn. (2.17) that the performance of Class AB amplifier is critical – a larger bandwidth and smaller output impedance is required for a lower V_R .

(ii) Effect of the external inductor L_O

A large L_O facilitates to reduce the output ripple noise. This is intuitive as the external inductor works as a lowpass filter to attenuate the high frequency ripple noise. However, as mentioned earlier, the increased L_O results in a reduced f_T (hence, the increased current burden of the Class AB amplifier) and an increased parasitic resistance of L_O (hence, increased inductor power loss). Considering these tradeoffs, the value of inductor should be judiciously selected on the basis of the specific application. In published literature, the value of inductor ranges from 80nH [66] to 20 μ H [70].

(iii) Effect of the switching frequency f_{sw} and the ripple current $i_{AB(pp)}$

Surprisingly, the output ripple is largely independent of f_{sw} . This counter-intuitive observation is noted because the output impedance of Class AB amplifier is inductive at frequencies above the dominant pole, and the lowpass filter

comprising the Class AB amplifier and the external inductor, in fact, collectively works as a voltage divider at the switching frequency.

Fig. 2-17 shows a typical frequency response of $|Z_{AB}|/|sL_O|$ in hybrid CDAs, which illustrates this phenomenon. The dominant pole of the reported wideband Class AB amplifier normally lies below 100kHz [67]. However, as f_{sw} (typically >10MHz) is apparently higher than the pole frequency, f_{sw} has negligible effect on the ripple noise. This is already apparent in eqn. (2.17) where as $i_{AB(pp)}$ has an inverse proportional relationship with f_{sw} (for a given external inductor), the output ripple is not affected by the ripple current $i_{AB(pp)}$.

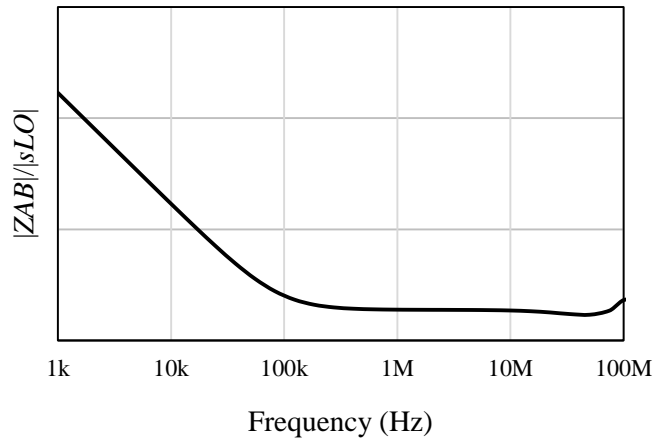


Fig. 2-17: Typical frequency response of $|Z_{AB}|/|sL_O|$

Bandwidth

Bandwidth is another critical parameter for hybrid CDA for ET PAs. This is because to maintain sufficient linearity, the hybrid CDA is required to have a wide

bandwidth to track the envelope signals. As the evolution of wireless standards, modern wireless standards, such as WCDMA, LTE, WLAN, feature higher PAPR and wider bandwidth [87, 88] to pack more bits of information. This consequently imposes more stringent requirements on the bandwidth of the hybrid CDA.

Furthermore, the hybrid CDA suffers from spectral expansion phenomenon, i.e., the spectrum of the input envelope signal is much wider than the bandwidth of the RF signal. This is illustrated in Fig. 2-18, where the spectra of a 20MHz LTE RF signal and its extracted envelope signal are depicted. The bandwidth of the envelope signal is expanded to about 3x of the 20MHz RF signal bandwidth [66, 68, 70], i.e., to 60MHz. This is due to the nonlinear transformation from the modulated RF signal to the envelope signal.

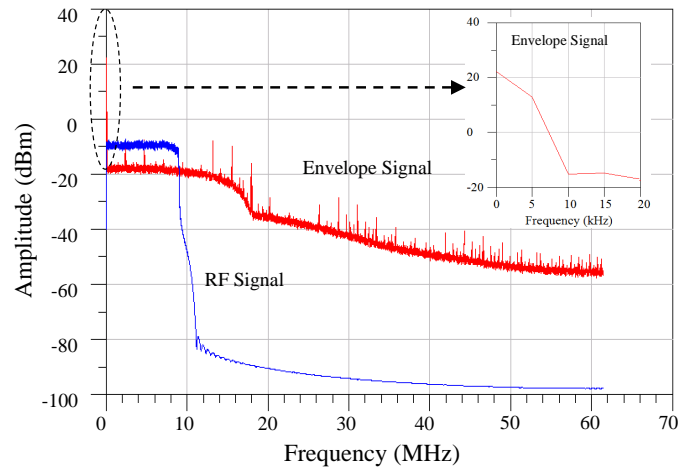


Fig. 2-18: Spectra of a 20MHz LTE RF signal and its extracted envelope signal

Both the small-signal bandwidth and the large-signal bandwidth (i.e., slew rate) of hybrid CDAs should be sufficiently large to avoid nonlinear distortion. The small-signal bandwidth of hybrid CDAs is determined solely by the bandwidth of the Class AB amplifier. This is because the AC component of the input signals can be provided by the Class AB amplifier. In hybrid CDAs, the bandwidth of the Class AB amplifier is a critical parameter to the linearity of the hybrid CDAs, which has significant effect on both of the small-signal bandwidth and output ripple voltage in hybrid CDAs.

On the other hand, the large-signal bandwidth of the hybrid CDA is limited by the Class AB amplifier and the CDA. To provide sufficient output current, the Class AB amplifier is normally designed with large transistors. In order to guarantee large output current while maintaining wide bandwidth, the quiescent current of the Class AB amplifier is relatively high, about several tens of milliamps (e.g. 24mA in [70]). This high quiescent current consumption significantly degrades the power-efficiency of the hybrid CDA with low- and mid-power levels. By increasing the slew rate, SR_{iD} , of the CDA, the transition frequency f_T is increased; therefore the CDA is able to provide more power for the AC component of the input signals to reduce the current burden of the Class AB amplifier. However, the optimization of f_T is limited by the tradeoffs between power-efficiency and output ripple, as discussed earlier.

In short, the bandwidth of the hybrid CDA significantly affects the linearity of the ET PA, which needs to be sufficient for tracking wideband envelope signals. However, there are tradeoffs between bandwidth, power-efficiency, output ripple.

Power-Efficiency and Power Loss

The power optimization of the hybrid CDA is complex problem, involving many tradeoffs between different parameters [66, 70, 71]. We will now review the power dissipation of each critical block and discuss the associated tradeoffs.

The power dissipation of the hybrid CDA, expressed in eqn. (2.18), can be separated into three parts – power loss from the external inductor (P_{loss_L}), from the CDA (P_{loss_D}), and from the Class AB amplifier (P_{loss_AB}).

$$P_{loss} = P_{loss_L} + P_{loss_D} + P_{loss_AB} \quad (2.18)$$

P_{loss_L} , expressed in eqn. (2.19), is due to the parasitic resistance, R_{ind} , of the external inductor, L_O , which largely depends on the parameters of the inductor. In practice, the rule-of-thumb is that inductors with higher values usually have larger (worse) parasitic resistances.

$$P_{loss_L} = i_O^2 R_{ind} \quad (2.19)$$

The expression for P_{loss_D} is given in eqn. (2.20a). The power loss, P_{loss_D} , from the CDA consists of $P_{D(SW)}$ and $P_{D(ON)}$, which is the switching loss and conduction loss, expressed in eqns. (2.20b) and (2.20c), respectively. The switching loss, $P_{D(SW)}$, is due to the parasitic capacitance, C_{eq} , of the drivers and power transistors in the output stage and the conduction loss, $P_{D(ON)}$, is due to the on-resistance, R_{eq} , of the output stage. C_{eq} and R_{eq} are both related to the size of drivers and power transistors. For a given switching frequency, the size of the output stage can be optimized such that resistive and capacitive

dissipations become equal. The optimized power loss, $P_{loss_D(op)}$, from the CDA is expressed in eqn. (2.20d) [66].

$$P_{loss_D} = P_{D(SW)} + P_{D(ON)} \quad (2.20a)$$

where

$$P_{D(SW)} = f_{sw} C_{eq} V_{DD}^2 \quad (2.20b)$$

$$P_{D(ON)} = i_O^2 R_{eq} \quad (2.20c)$$

$$P_{loss_D(op)} = 2V_{DD} i_O \sqrt{f_{sw} R_{eq} C_{eq}} \quad (2.20d)$$

It can be seen that $P_{loss_D(op)}$ is strongly affected by f_{sw} , where a high f_{sw} results in undesirable higher power dissipation. However, it is worthwhile to notice that a low f_{sw} means that the transition frequency, f_T , is low. In other words, more AC current will be sourced from the Class AB amplifier when f_{sw} is low, which undesirably increases the current burden of the power-inefficient Class AB amplifier and the ensuing power loss, P_{loss_AB} , of the Class AB amplifier (see below). This ultimately results in the tradeoffs between the power loss of the Class D amplifier and the power loss of the Class AB amplifier, and the power optimization should be on the basis of the specific input signals.

The power loss from the Class AB amplifier, expressed in eqn. (2.21a), consists of $P_{AB(Q)}$, $P_{AB(LF)}$ and $P_{AB(HF)}$.

$$P_{loss_AB} = P_{AB(Q)} + P_{AB(LF)} + P_{AB(HF)} \quad (2.21a)$$

$$P_{loss_AB} = I_Q V_{DD} \quad (2.21b)$$

$$P_{loss(LF)} = \frac{1}{4} i_{AB(pp)} V_{DD} \quad (2.21c)$$

$P_{AB(Q)}$ is the quiescent current of the Class AB amplifier. $P_{AB(LF)}$ arises from the absorption of the ripple current from the CDA for tracking low frequency signals, and $P_{AB(HF)}$ is due to large output current from the Class AB amplifier for tracking high frequency signals. As mentioned earlier, $P_{AB(Q)}$ is relatively high to maintain the wide bandwidth and sufficient output current. This can undesirably degrade the power-efficiency of the hybrid CDA for low- to mid-power applications. $P_{AB(LF)}$ is mainly due to the ripple current (refer to Fig. 2-15). A low ripple current, i.e., a low $i_{AB(pp)}$, is beneficial to reduce $P_{AB(LF)}$, hence improving the power-efficiency of the hybrid CDA. However, as discussed in eqn. (2.13), there is an inevitable tradeoff between $i_{AB(pp)}$ and f_{sw} . For example, a high f_{sw} increases the switching loss of the CDA (hence increasing P_{loss_D}). For tracking high frequency input signals, as the frequency increases, the AC power from the CDA decreases, and the Class AB amplifier will provide more AC current at a higher frequency (refer to Fig. 2-16), resulting in a larger power loss, hence increased $P_{AB(HF)}$.

In summary, the optimization of power to obtain high power-efficiency is a complex problem, involving a number of trade-offs.

2.3 Conclusions

In this chapter, we have provided a comprehensive and critical review of the audio CDA and the hybrid CDA for ET PAs. A number of design issues have been described and of particular note the design process for an optimized audio CDA and hybrid CDA involves complex tradeoffs. In light of these complex tradeoffs, this chapter has served as a preamble to the contributions in this Ph.D. program delineated in the following chapters.

Chapter 3 PWM Audio Class D Amplifiers:

PSRR and PS-IMD

3.1 Introduction

A large portion of this chapter has been published in Analog Integrated Circuits and Signal Processing [39] and in IEEE International Midwest Symposium on Circuits and Systems [40].

As delineated in Chapters 1 and 2 herein, CDAs are increasingly prevalent as the audio PA of choice for mobile devices, including smartphones, tablets, wearable electronics, etc. This is largely because of their substantially higher power-efficiency over their Class AB amplifier counterparts, such as Class A and Class AB amplifiers. Poor PSRR and PS-IMD may result in audible noise at the output and this is particularly the case when the CDA is highly integrated in ICs and SoCs where the power supply is shared among many circuits and the circuits induce noise to the power supply making the power supply inevitably noisy. As CDAs is typically tied its supply tail to the battery directly, it is imperative that PSRR are high and PS-IMD are low, including high PSRR (>90 dB) at 217Hz, the principle interfering GSM signal frequency, to achieve high audio quality. For completeness, amongst the different CDA architectures, the PWM CDA is the most

popular CDA architecture adopted in mobile devices due to their simple hardware and relatively high fidelity. In this Chapter, this is the specific CDA architecture of interest.

Interestingly, in view of the imperativeness of PSRR and PS-IMD for CDAs, reported analytical investigations in literature are incomplete and/or somewhat oversimplified. For example, investigations [18, 48] into the PSRR and PS-IMD of PWM CDAs revealed that the important parameters affecting PSRR include the loop gain, and for single-ended and BTL CDAs respectively, the design of the carrier generator and the matching between the two branches. Despite the valuable insights provided in these reported investigations, an imperative limitation is a somewhat simplified assumption, particularly that the AC ground is noise-free – an unrealistic assumption in present-day highly-integrated ICs and SoCs. Although the AC ground is recognized to be important [21, 50] to the PSRR of CDAs, their mechanisms to PSRR and PS-IMD remain uninvestigated and unreported. Put simply, as the AC ground serves as the bias point to the carrier generator and to the fully-differential op amps for high dynamic range, the noise in the AC ground would, as expected, affect the PSRR.

Furthermore, the reported analysis [18, 21] of the PSRR of single-feedback BTL CDAs is also somewhat incomplete because it is based on an oversimplified fully-differential integrator model – modeled simply as two independent single-ended integrators. This simplified model is inadequate because the output of a fully-differential integrator depends not only on the common-mode voltage reference (i.e., AC ground) but also on the resistors and capacitors in the two branches of the integrator – specifically that there may be mismatches between the resistors and capacitors in the two branches. An investigation based on a realistic model will depict a comprehensive overview of the

effect of the mismatch of each resistor pair and capacitor pair. This is pertinent because the layout of resistors and capacitors to obtain high matching can be area intensive, hence costly and if possible, avoided.

Yet further, the analyses [18] of the PSRR of BTL CDAs remain largely incomplete. Specifically, to date, only the PSRR of BTL CDAs based on the single-feedback topology has been reported while BTL CDAs based on double-feedback remain unreported. BTL CDAs based on the single-feedback and double-feedback are prevalent, and the latter is generally preferred in applications where higher fidelity is desired. Hence, PSRR is more important for the latter.

In this Chapter, we provide an analysis of the effect of the supply noise in the AC ground to the PSRR and PS-IMD of open-loop PWM CDAs, and show that the PSRR and PS-IMD, as expected, are strongly affected thereto. Analytical expressions are derived, depicting the related mechanisms. We further provide an analysis of the effect of the non-ideal AC ground and of the mismatch of the resistor pair and capacitor pair (of the two branches of the integrator) on the basis of a realistic fully-differential integrator model (vis-à-vis the simple fully-differential integrator model comprising two independent integrators). This analysis pertains to the PSRR of a 3-state BTL closed-loop CDA, and includes the derivation of analytical expressions. On the basis of said investigation, we derive the analytical equations for the PSRR of BTL CDAs based on the double-feedback topology. In general, these analyses and derived expressions are interesting as they offer valuable insights into the mechanisms of the practical circuit parameters affecting the PSRR and PS-IMD, and possible trade-offs in the design of CDAs.

This Chapter is organized in the following manner. In Section 3.2, as a preamble to our ensuing analysis, the PSRR of three prevalent open-loop CDA structures, with various carrier generators, are reviewed and compared, and the effect of the supply noise in the AC ground analyzed. In Section 3.3, the analysis in Section 3.2 is applied to the ubiquitous 3-state BTL closed-loop PWM CDAs, taking into consideration the effect of non-ideal AC ground and mismatches of resistor pairs and capacitor pairs based on realistic fully-differential integrator model. The specific BTL CDAs of interest are that based on the double-feedback topology where their PSRR is investigated and the associated analytical expressions derived. The important practical circuit parameters affecting the PSRR are thereafter discussed. In Section 3.4, the analytical derivations in Section 3.3 are verified on the basis of HSPICE simulations and practical measurements on discretely-realized CDAs. Finally, conclusions are drawn in Section 3.5.

3.2 PSRR and PS-IMD of Open-loop Class D Amplifiers

In CDAs, in part for sake of hardware simplicity and power dissipation, the AC ground is usually realized by a voltage divider (instead of that derived from a bandgap reference) followed by a lowpass filter (whose cut-off frequency is $<50\text{Hz}$) [21, 50]. This simple means provides for the AC ground at $\sim 0.5V_{DD}$ regardless of the supply voltage - this is imperative for high dynamic range. In the following analysis, we denote the AC ground as V_{CM} :

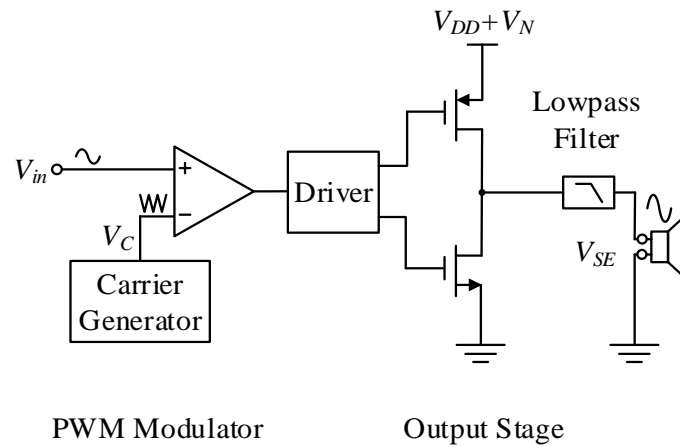
$$V_{CM} = \frac{V_{DD}}{2} + \frac{V_N}{A} \quad (3.1)$$

where V_{DD} is the supply voltage, V_N is the supply noise component on the supply rail, and A is the attenuation of the supply noise in the AC ground, e.g., if $A = 20$, the noise in the AC ground is 1/20 that in the supply rail.

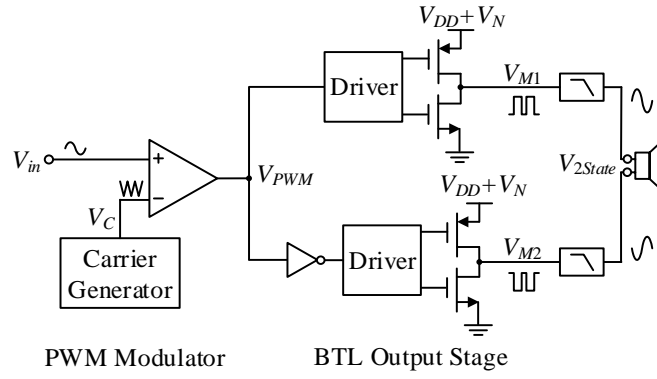
A is typically 20 and 100 at 217Hz and 1kHz respectively. These frequencies are of particular interest as they are the primary noise frequency for GSM and 4G LTE respectively. A large A at low frequency is difficult and expensive to achieve due to IC area and power dissipation constraints; in some cases, A is the limiting factor for the design of a CDA with very high PSRR (e.g. >100dB in closed loop PWM CDAs) and low PS-IMD (e.g. <-100dB).

We will show later that depending on the architecture of the CDA and the design of the carrier generator, the supply noise in the AC ground may or may not degrade the PSRR and PS-IMD of the open-loop CDAs. In some cases, its effect on PSRR and PS-IMD is negligible, which translates to the relaxed design requirements for the AC ground, hence potentially smaller IC area (lower cost) and/or lower power dissipation. In other designs, on the other hand, the supply noise in the AC ground may significantly deteriorate the PSRR and PS-IMD, and a ‘clean’ AC ground is required for high PSRR and low PS-IMD. Put simply, the AC ground should be designed with all due considerations. In view of this, we will now succinctly review the various carrier generators and in the perspective of open-loop CDAs.

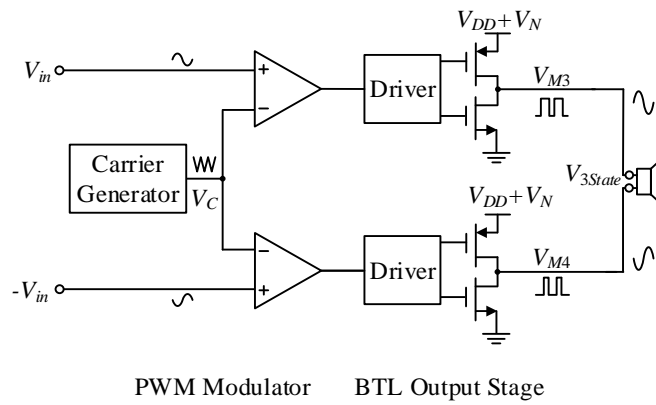
Fig. 3-1 depicts the block diagram of three topologies of open-loop CDAs: (a) Single-ended, (b) 2-state BTL, and (c) 3-state ('filterless') BTL. All CDAs embody a carrier generator, PWM modulator, output stage, and a load (including a lowpass filter for (a) and (b), and a loudspeaker). The three commonly used carrier generators are depicted in Fig. 3-2, where V_{C_I} , V_{C_II} and V_{C_III} are the carrier signals generated by Carrier Generators I, II and III, respectively. The operating mechanism of these carrier generators are similar where by means of charging and discharging a capacitor, a triangular carrier waveform is generated as depicted in Fig. 3-3. By straight-forward analysis, the ideal maximum and minimum voltages of the carrier signal, V_{CH} and V_{CL} , can be ascertained and these are expressed in Fig. 3-2 at the bottom of the schematic of each carrier generator. Practically, due to the delay of the comparator, t_D , the practical maximum voltage of the carrier signal V_{CH_Max} is higher than the ideal V_{CH} , and the practical minimum voltage V_{CL_Min} is lower than the ideal V_{CL} . These are also depicted in Fig. 3-3.



(a)

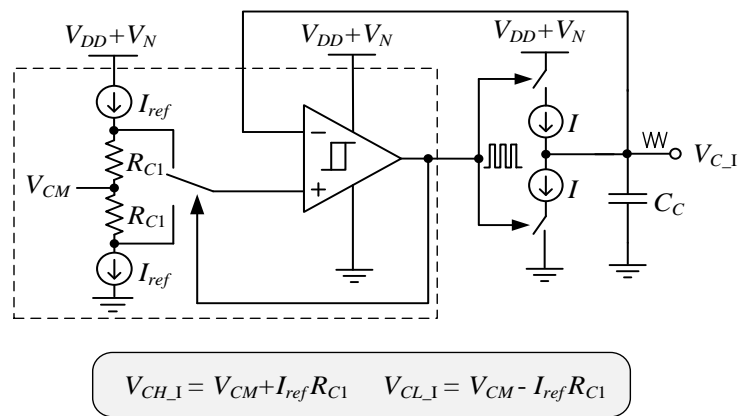


(b)

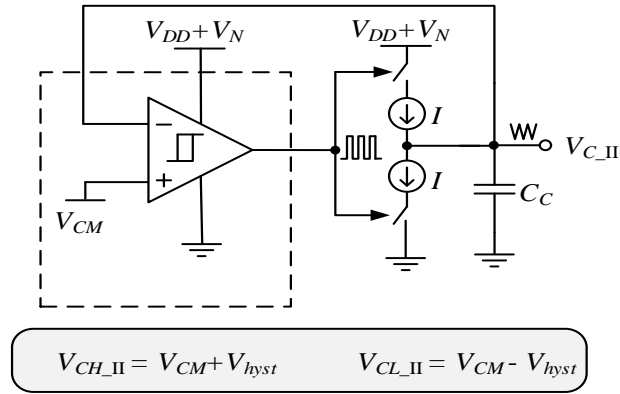


(c)

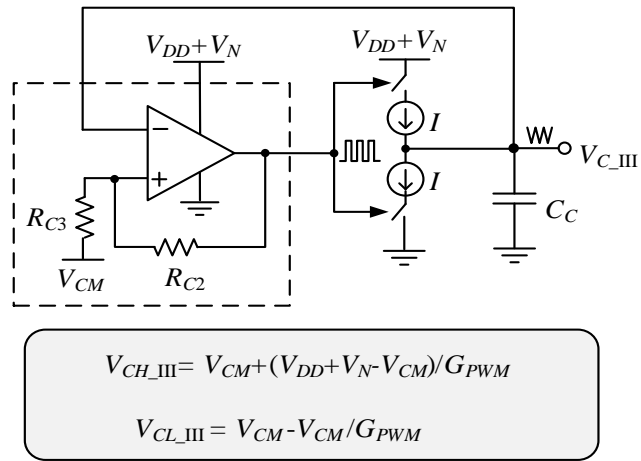
Fig. 3-1: Schematic of CDAs: (a) Single-Ended CDA, (b) 2-state BTL CDA, and (c) 3-state ('filterless') BTL CDA



(a)



(b)



(c)

Fig. 3-2: Schematic of carrier generators: (a) I, (b) II, and (c) III

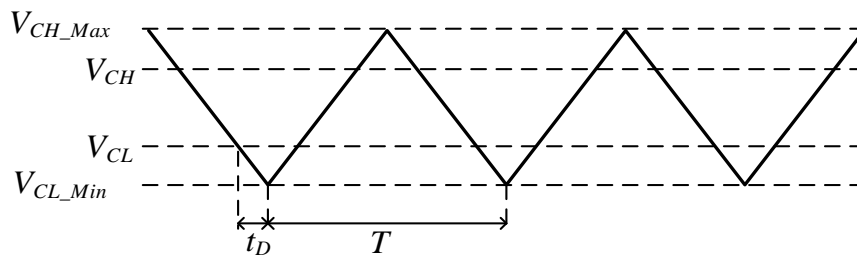


Fig. 3-3: Waveform of the carrier signal

From Fig. 3-2, V_{CH_Max} , V_{CL_Min} and the practical switching period, T , of the carrier signals generated from each carrier generator can be easily derived as follows.

Carrier Generator I

$$V_{CH_MaxI} = V_{CM} + I_{ref} R_{C1} + \frac{t_D}{T_0} (4I_{ref} R_{C1}) \quad (3.2)$$

$$V_{CL_MinI} = V_{CM} - I_{ref} R_{C1} - \frac{t_D}{T_0} (4I_{ref} R_{C1}) \quad (3.3)$$

$$T = T_0 + 4t_D \quad T_0 = \frac{C_C}{I} 4I_{ref} R_{C1}$$

where T_0 is the ideal switching period.

Carrier Generator II

$$V_{CH_MaxII} = V_{CM} + V_{hyst} + \frac{4t_D}{T_0} V_{hyst} \quad (3.4)$$

$$V_{CL_MinII} = V_{CM} - V_{hyst} - \frac{4t_D}{T_0} V_{hyst} \quad (3.5)$$

$$T = T_0 + 4t_D \quad T_0 = 4 \frac{C_C}{I} V_{hyst}$$

where V_{hyst} is the hysteresis of the comparator.

Carrier Generator III

$$V_{CH_MaxIII} = \frac{V_{DD} + V_N}{G_{PWM}} + V_{CM} \frac{R_{C2}}{R_{C2} + R_{C3}} + \frac{t_D}{T_0} \frac{2V_{DD}}{G_{PWM}} \quad (3.6)$$

$$V_{CL_MinIII} = V_{CM} \frac{R_{C2}}{R_{C2} + R_{C3}} - \frac{t_D}{T_0} \frac{2V_{DD}}{G_{PWM}} \quad (3.7)$$

$$T = T_0 + \frac{V_N}{V_{DD}} T_0 + 4t_D \qquad T_0 = \frac{C_C}{I} \frac{2V_{DD}}{G_{PWM}}$$

where $G_{PWM} = (R_{C2} + R_{C3})/R_{C3}$ is the gain of PWM modulator, i.e. G_{PWM} is the ratio of the supply voltage to the carrier signal.

Based on the derived expressions alone and applying the method delineated in [18, 48], the PSRR and PS-IMD of single-ended, 2-state BTL and 3-state BTL open-loop CDAs can be derived and these are tabulated in Table 3-1; refer to Appendix for the detailed derivations.

Table 3-1: PSRR and PS-IMD of the Single-Ended, 2-State BTL and 3-State BTL CDAs based on various Carrier Generators

		Single-Ended	2-State BTL	3-State BTL
Carrier Generator I & II	PSRR	6	$-20 \log K$	$-20 \log K$
	PS-IMD	$-9 + 20 \log M$	$-3 + 20 \log M$	$-3 + 20 \log M$
Carrier Generator III	PSRR	$-20 \log \left(\frac{1}{A} + 2 \frac{t_D}{T_0} \right)$	$-20 \log \left[\left(1 - \frac{2}{A} \right) \left(1 - 4 \frac{t_D}{T_0} \right) \right]$	$-20 \log \left(4 \frac{t_D}{T_0} K \right)$
	PS-IMD	$20 \log \left(2 \frac{t_D}{T_0} \right) - 3 + 20 \log M$	$20 \log \left(2 \frac{t_D}{T_0} \right) + 3 + 20 \log M$	$20 \log \left(2 \frac{t_D}{T_0} \right) + 3 + 20 \log M$

where M is the modulation index, $M = V_{out, peak-to-peak}/V_{DD}$; $K = V_{offset}/V_{DD}$, and V_{offset} is the output offset voltage.

Using the derived expressions in Table 3-1 and on the basis of the following parameters: comparator delay $t_D = 50\text{ns}$, switching period $T_0 = 4\mu\text{s}$ (hence the switching frequency, $1/T_0 = 250\text{kHz}$), normalized DC offset $K = 0.01$ and $K = 0.005$ for the 2-state BTL and 3-state BTL respectively, $M = 0.1$ (nominal operation condition), and $A = 20$ (typical

value at 217Hz), the PSRR and PS-IMD of the different open-loop CDAs (Fig. 3-1) are obtained and tabulated in Table 3-2. The bolded values indicate the best cases for each open-loop CDA topology. These analytically obtained PSRR and PS-IMD values in Table 3-2 are verified against HSPICE simulations. For completeness, note that the aforesaid parameters are typical values in a practical design.

Table 3-2: Comparison of PSRR and PS-IMD for open-loop CDAs (@ 217Hz)

		Single-Ended	2-State BTL	3-State BTL
Carrier Generator I	PSRR	6dB	40dB	46dB
Carrier Generator II	PS-IMD	-29dB	-23dB	-23dB
Carrier Generator III	PSRR	22.5dB	1.4dB	72dB
	PS-IMD	-55dB	-49dB	-49dB

From Tables 3-1 and 3-2, we make the following observations:

- (i) As expected, because open-loop CDAs do not embody negative feedback, in general, they suffer from relatively poor PSRR and PS-IMD.
- (ii) Of the different open-loop CDAs, the 3-state BTL structure typically features the highest PSRR. This is as expected and is similarly observed in linear BTL amplifiers. However, somewhat surprising, the PS-IMD of the BTL CDAs is 6dB worse than that of the single-ended. This is because the PS-IMD components at the two branches of the BTL output are out of phase, i.e., the PS-IMD components in the differential output signal is 2x that of the single-ended output signal.

- (iii) As expected, in part because of the design of the carrier generator, the noise in the AC ground has a different effect on PSRR. From eqns. (3.2) and (3.3) and from eqns. (3.4) and (3.5), it can be seen that for Carrier Generator I and II, the magnitude of that for the Carrier I and II (i.e., $V_{CH_Max}-V_{CL_Min}$) is independent of the supply noise; and V_{CH_Max} , V_{CL_Min} and V_{in} , are AC coupled. The ‘on’ and ‘off’ periods of the output signals (V_{SE} , V_{M1} , V_{M2} , V_{M3} , V_{M4} in Fig. 3-1) are hence independent of the noise in the AC ground and are ascertained from the intrinsic parameters, i.e., I_{ref} and R_{C1} for Carrier Generator I and V_{hyst} for Carrier Generator II. This independence is because the noise in the AC ground does not have a feedforward path to the output of the open-loop CDAs. From eqns. (3.6) and (3.7), it can be seen that V_{CH_Max} and V_{CL_Min} of Carrier Generator III is dependent on a ratio (i.e., $R_{C2}/(R_{C2}+R_{C3})$) of V_{CM} , and that the carrier frequency, $1/T$, varies due to the supply noise of the comparator. The output signal of CDAs is hence affected by the noise on the AC ground and the supply rail of the comparator in the Carrier Generator III.
- (iv) Of the various Carrier Generators, Carrier Generator III yields the best PSRR and PS-IMD for the single-ended and 3-state BTL CDAs, whilst Carrier Generators I and II yields the best PSRR and PS-IMD for 2-state BTL CDAs. This is because for single-ended and 3-state BTL CDAs with Carrier Generator III, the distortion components induced by the supply noise are in part cancelled by the distortion components in the carrier. It is worthwhile to note that although Carrier Generator III can improve the PSRR of the 3-state BTL CDA to a relatively high 72dB, it degrades the PSRR to an unacceptable 1.4dB when it is embodied in the 2-state

BTL CDA. Carrier Generator III is hence recommended for the single-ended and 3-state BTL CDAs but is inapplicable to the 2-state BTL CDA. Instead, Carrier Generators I and II are recommended for the 2-state BTL CDAs.

- (v) For Carrier Generator III, it can be seen from Table 3-1 that a higher supply noise attenuation (A) at the AC ground results in higher PSRR - the PSRR is improved by 6.5dB (from 22.5dB to 29dB) when A is increased from 20 to 100 for single-ended CDAs. From a practical perspective, because the lowpass filter is adopted for generating the AC ground, a larger attenuation effect appears at high frequencies, i.e., the PSRR at 1kHz may be higher than that at 217Hz due to larger A .

3.3 PSRR of 3-state BTL Closed-loop Class D Amplifiers

It was shown in Section 3.2 that 3-state BTL open-loop CDAs with Carrier Generator III generally features a higher PSRR. For this reason, the 3-state BTL CDA is of specific interest herein. Further, because CDAs with higher fidelity is generally preferred (see Section 3.1 earlier), our analyses henceforth will be focused on the double-feedback topology where the integrators therein can be realized as either 1st- or 2nd-order. For completeness, note that configurations other than the 3-state BTL CDA can be similarly analyzed. Consider now the 3-state double-feedback BTL with 1st- or 2nd-order integrators in turn.

3.3.1 Class D Amplifiers with 1st-order Integrators

Fig. 3-4 depicts the schematic diagram of 3-state double-feedback BTL closed-loop PWM CDAs embodying 1st-order integrators. It comprises two 1st-order integrators, a 3-state BTL open-loop PWM CDA, two feedback paths and a load (loudspeaker). For reasons delineated earlier, Carrier Generator III is employed hereto.

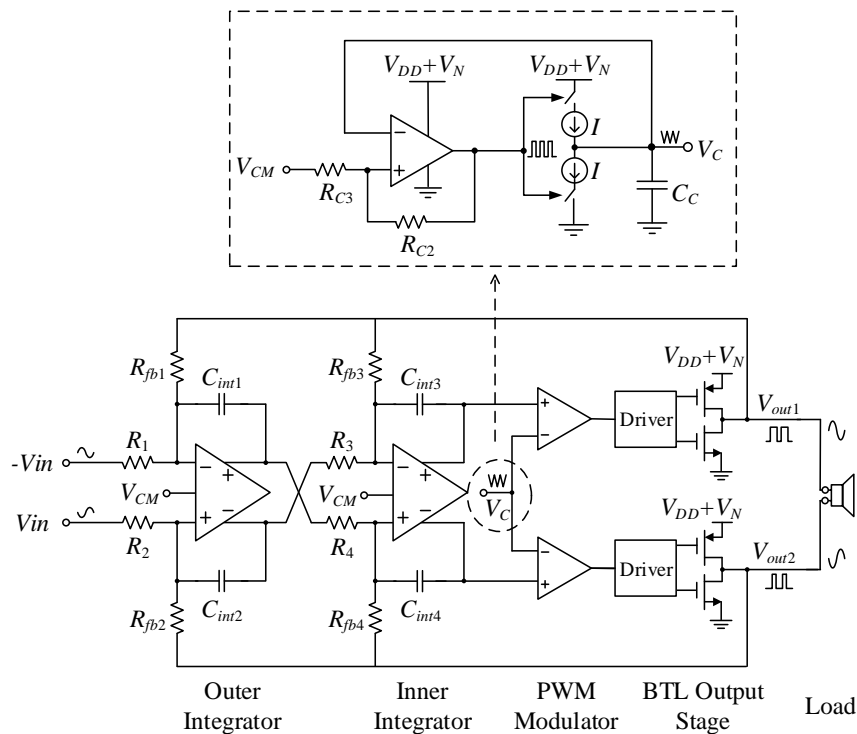


Fig. 3-4: Schematic of a 3-state double-feedback BTL PWM CDA with 1st-order integrators

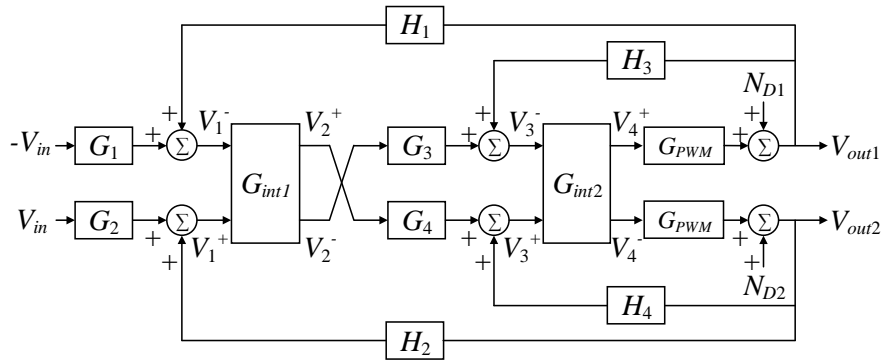


Fig. 3-5: Model of double-feedback BTL PWM CDAs

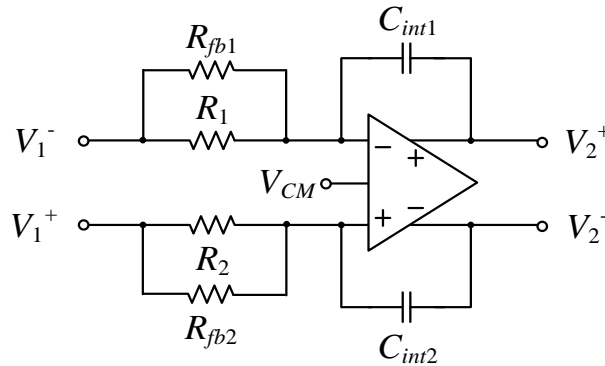


Fig. 3-6: The corresponding circuit of G_{int1} (from V_1^+ and V_1^- to V_2^+ and V_2^-)

To derive the PSRR, we present in Fig. 3-5 the simplified analytical block model of Fig. 3-4. We will now investigate the operation of the integrators. For brevity, we only delineate the operation of the outer integrator (refer to Fig. 3-4). The inner integrator has the same parameters with the outer integrator. G_{int1} in Fig. 3-5 is the transfer functions of the integrators and is a function of the resistors, capacitors and the AC ground, V_{CM} . This can be observed from Fig. 3-6, which depicts a practical model of G_{int1} . In view of a practical realization, we assume that there is a mismatch between R_1 and R_2 , R_{fb1} and R_{fb2} ,

and C_{int1} and C_{int2} . Consequent to these mismatches, the gains of the two branches, i.e., from V_1^+ and V_1^- to V_2^+ and V_2^- , are different.

Assuming that $a(f)$ of the fully-differential op amp is large (e.g., 100dB), and that the DC offset voltages $V_{offset1}$, $V_{offset2}$ and comparator delay t_D have the same values as that assumed earlier in Section 3.2 (i.e., $t_D=50\text{ns}$, switching period $T_0=4\mu\text{s}$, normalized DC offset $K=0.005$), these parameters generally have an insignificant effect to the PSRR of practical BTL closed-loop CDAs. In these practical designs, the transfer function G_{int1} from V_1^+ and V_1^- to V_2^+ and V_2^- (Fig. 3-6) can be expressed as eqns. (3.8) and (3.9) [52].

$$V_2^+ = \frac{(V_1^+ \beta_{2a} - V_1^- \beta_{1a}) + 2V_{CM} \beta_{2b}}{(\beta_{1b} + \beta_{2b})} \quad (3.8)$$

$$V_2^- = \frac{-(V_1^+ \beta_{2a} - V_1^- \beta_{1a}) + 2V_{CM} \beta_{1b}}{(\beta_{1b} + \beta_{2b})} \quad (3.9)$$

where β_{1a} , β_{1b} , β_{2a} , β_{2b} are the parameters for the outer integrator, which can be expressed as eqns. (3.10) and (3.11).

$$\beta_{1a} = \frac{1}{1 + s(R_1 // R_{fb1})C_{int1}} \quad (3.10)$$

$$\beta_{1b} = \frac{s(R_1 // R_{fb1})C_{int1}}{1 + s(R_1 // R_{fb1})C_{int1}} \quad (3.11)$$

In Fig. 3-5, G_1 and G_2 are the gain factors from the input of the CDA to the input of the outer integrator (G_{int1}), and H_1 and H_2 are the feedback factors. G_{PWM} at the output of the inner integrator represents the gain of PWM modulator. N_{D1} and N_{D2} are the augmented noise induced by the noise on the supply rail [18, 48]. As explained in Section

3.2, V_N is the supply noise component on the supply rail and A is the attenuation of the supply noise in the AC ground. The expression of parameters G_1 , H_1 , N_{D1} and N_{D2} can be expressed as:

$$G_1 = \frac{R_{fb1}}{R_1 + R_{fb1}} \quad (3.12)$$

$$H_1 = \frac{R_1}{R_1 + R_{fb1}} \quad (3.13)$$

$$N_{D1} = N_{D2} = \frac{V_N}{A} \quad (3.14)$$

Based on Figs. 3-5 and Fig. 3-6 and the parameters thereof, expressed in eqns. (3.8) - (3.14), we finally derive the PSRR expressed as eqn. (3.15) that includes the integrator parameters (G_{int1} , G_{int2}), transfer functions (G_1 , G_2 , G_3 , G_4), feedback factors (H_1 , H_2 , H_3 , H_4), supply noise attenuation (A), the gain of PWM stage (G_{PWM}), and the time period (T). the PSRR can be derived below:

$$\text{PSRR} \approx -20 \log \left(\frac{2}{A} \times \frac{G_{PWM} G_{int2} G_3}{1 + LG} \times \frac{G_1 \beta_{1a} - G_2 \beta_{2a}}{\beta_{1b} + \beta_{2b}} \right) \text{dB} \quad (3.15)$$

where $LG = G_{PWM}(G_{int1}G_{int2}G_3H_1 + H_3G_{int2})$ is the loop gain of the double-feedback CDA.

We make the following comments from the eqn. (3.15) :

(i) Loop Gain, LG

LG has a suppressing effect on the supply noise, i.e., the higher the loop gain, the larger is the PSRR. This is largely congruous with the general negative feedback

theory.

(ii) The Attenuation of the Supply Noise in the AC ground, A

A has a significant effect on PSRR, largely because the AC ground is the bias point in the differential op amps and because of the embodiment of the carrier generator (Carrier Generator III). Consequently, an adequately designed AC ground with a high supply noise attenuation (large A) can significantly increase the PSRR. In the context of practical designs in highly integrated ICs and SoCs, a voltage reference with a high PSRR would directly translate to the CDA having a high PSRR. As a case in point, by increasing A from 20 to 100, the PSRR of the CDA increases by a significant ~ 14 dB.

(iii) Resistor and Capacitor Matching

The matching in the outer integrator (indicated by $\beta_{1a}, \beta_{1b}, \beta_{2a}, \beta_{2b}$) is another limiting factor as observed by the third term in the parenthesis in eqn. (3.15). Conversely, the matching in the inner integrator (indicated by $\beta_{3a}, \beta_{3b}, \beta_{4a}, \beta_{4b}$), only has a minor effect on the PSRR. These observations are intuitive as the cancellation effect between two branches decreases as the mismatch increases, and the outer loop-gain can suppress the noise induced within the inner loop (where the inner integrator resides). In other words, the matching of the passives in the outer loop (C_{int1} and C_{int2} , R_1 and R_2 , R_{fb1} and R_{fb2}) are important, and conversely, the matching of the passives in the inner loop (C_{int3} , C_{int4} , R_3 , R_4 , R_{fb3} , R_{fb4}) are less important. In the perspective of practical layout, the layout of the latter passives can be laid out with lesser IC area.

For completeness, by defining the matching of the passives as: $R_1 = (1 - a\%)R_D$, $R_2 = (1 + a\%)R_D$, $R_{fb1} = (1 - b\%)R_{fb}$, $R_{fb2} = (1 + b\%)R_{fb}$, $C_{int1} = (1 - c\%)C_D$, $C_{int2} = (1 + c\%)C_D$, where R_D , R_{fb} and C_D are the design values, we derive the PSRR as eqns. (3.16a) – (3.16d).

$$\text{PSRR} \approx 20 \log \left[\frac{A}{(1 - b\%^2)(a\% + c\%)} \times \frac{(R_D + R_{fb})^2 R_{e1}^2 C_{int1}^2 R_{e3} C_{int3}}{2G_{PWM} G_3 R_{fb}^2 R_D C_D} \times \frac{(s + \omega_{z1})(s + \omega_{z2})(s + \omega_{z3})}{s + \omega_p} \right] \text{dB} \quad (3.16a)$$

$$\text{where } \omega_p = \frac{a\% - b\%}{R_{fb} C_D (1 - b\%^2)(a\% + c\%)} \quad (3.16b)$$

$$\omega_{z1} = \frac{1}{R_{e1} C_{int1}} \quad (3.16c)$$

$$\omega_{z2,3} = \frac{-R_{e1} C_{int1} G_{PWM} H_3 \pm \sqrt{(R_{e1} C_{int1} G_{PWM} H_3)^2 - 4R_{e1} C_{int1} R_{e3} C_{int3} G_{PWM} G_3 H_1}}{2R_{e1} C_{int1} R_{e3} C_{int3}}$$

$$\text{Type equation here.} \quad (3.16d)$$

On the basis of our derived eqns. (3.16a) – (3.16d), we make the following observations:

- (i) The PSRR at low frequencies is largely determined by the dominant pole, ω_p , expressed in eqn. (3.16b). Hence, to achieve high PSRR, particularly at low frequencies, reducing the resistor mismatch of the outer integrator is necessary. This is evident from eqn. (3.16a), as the matching in the outer integrator matching is substantially more important than the matching in the inner integrator.
- (ii) Further to aforesaid (i), it can be seen from eqn. (3.16b) that minimizing the

difference between a% and b% (i.e. a%-b%) would desirably reduce ω_p . This is interesting because the mismatch of the resistor pairs, a% due to mismatch between R_1 and R_2 , and b% due to mismatch between R_{fb1} and R_{fb2} , can be tolerated if the mismatch of these two pairs can be matched, i.e., (a%-b%) is small. In the practical context, we recommend adequate layout techniques be employed to match a% and b%. As a case in point, if (a%-b%) decreases from 0.1% to 0.01%, the corner frequency will decrease about one decade, and the ensuing PSRR at low frequency (below the corner frequency, ω_p , given in eqn. (3.16b)) will increase significantly by ~ 20 dB.

- (iii) Above the corner frequency, ω_p , the PSRR decreases at ~ 20 dB/dec within audio frequency range (20Hz to 20kHz); note that the zeros, ω_{z1} , ω_{z2} , ω_{z3} are normally >20 kHz as given in eqns. (3.16c) and (3.16d).
- (iv) From eqn. (3.16a), we note, as expected, that the smaller the mismatches (i.e., smaller a%, b%, c%), the better is the PSRR. Further, it is interesting to note that the mismatch between R_1 and R_2 (a%) and the mismatch between C_{int1} and C_{int2} (c%) are almost equally important to the PSRR above the corner frequency, ω_p .

3.3.2 Class D Amplifiers with 2nd-order Integrators

Fig. 3-7 depicts the schematic of the 3-state double-feedback BTL closed-loop CDA comprising two 2nd-order integrators. The analytical block model depicted in Fig. 3-5 for Fig. 3-4, can be applied to Fig. 3-7. The major difference between Fig. 3-4 and Fig. 3-7 is the integrator parameters. The 2nd-order integrator parameters, β_{1a} , β_{1b} , are

presented in eqns. (3.17) and (3.18). With the similar analysis method delineated in Section 3.3.1, we can derive the analytical expression for PSRR as eqn. (3.19).

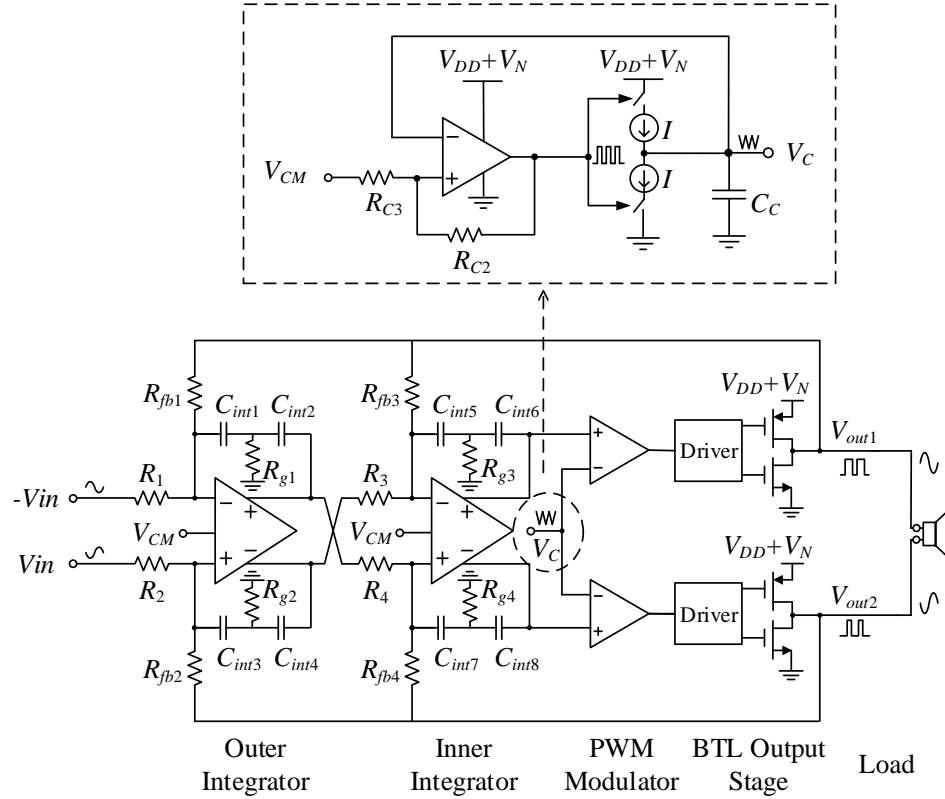


Fig. 3-7: Schematic of a double-feedback BTL CDA with 2nd-order integrators

It can be seen from eqn. (3.19) that the PSRR of BTL PWM CDAs with 2nd-order integrators is also affected by loop gain LG , noise attenuation A , and the outer integrator matching (by the third term in the parenthesis in eqn. (3.19)). This is similar to the CDAs with 1st-order integrators in Fig. 3-4 earlier.

$$\beta_{1a} = \frac{1 + s(R_{g1}C_{int1} + R_{g1}C_{int2})}{1 + s(R_{e1}C_{int1} + R_{g1}C_{int1} + R_{g1}C_{int2}) + s^2R_{e1}R_{g1}C_{int1}C_{int2}} \quad (3.17)$$

$$\beta_{1b} = \frac{s^2 R_{e1} R_{g1} C_{int1} C_{int2}}{1 + s(R_{e1} C_{int1} + R_{g1} C_{int1} + R_{g1} C_{int2}) + s^2 R_{e1} R_{g1} C_{int1} C_{int2}} \quad (3.18)$$

$$\text{PSRR} \approx -20 \log \left(\frac{2}{A} \times \frac{G_{PWM} G_{int2} G_3}{1 + LG} \times \frac{G_1 \beta_{1a} - G_2 \beta_{2a} + \beta_{2t} - \beta_{1t}}{\beta_{1b} + \beta_{2b}} \right) \text{dB} \quad (3.19)$$

where $LG = G_{PWM}(G_{int1}G_{int2}G_3H_1 + H_3G_{int2})$ is the loop gain.

By defining the matching of the passives as: $R_1 = (1 - a\%)R_D$, $R_2 = (1 + a\%)R_D$, $R_{fb1} = (1 - b\%)R_{fb}$, $R_{fb2} = (1 + b\%)R_{fb}$, $C_{int1} = (1 - c\%)C_{D1}$, $C_{int3} = (1 + c\%)C_{D1}$, $R_{g1} = (1 - d\%)R_g$, $R_{g2} = (1 + d\%)R_g$, $C_{int2} = (1 - e\%)C_{D2}$, $C_{int4} = (1 + e\%)C_{D2}$, where R_D , R_{fb} , R_g , C_{D1} and C_{D2} are the design values, we derive the PSRR as eqns. (3.20a) – (3.20c).

On the basis of eqns. (3.20a) – (3.20c), we make the following observations:

- (i) It is interesting to note that the matching between R_1 and R_2 (a%), R_{fb1} and R_{fb2} (b%), and C_{int1} and C_{int3} (c%) are more critical than that of C_{int2} and C_{int4} (d%), and R_{g1} and R_{g2} (e%). This is because d% and e% only have little effect on PSRR.

$$\text{PSRR} \approx 20 \log \left[\frac{A}{2(a\% - b\%)[(1 + c\%d\%)C_{D1} + (1 + e\%d\%)C_{D2}]R_g - (1 - a\%^2)(b\% + c\%)R_D C_D} \times \frac{(R_D + R_{fb})^2 (R_{e1} R_{g1} C_{int1} C_{int2})^2 R_{e2} C_{int3} C_{int4}}{2G_{PWM} G_3 R_D R_{fb} (C_{int3} + C_{int4})} \times \frac{(s + \omega_{z1})(s + \omega_{z2})(s + \omega_{z3})(s + \omega_{z4})(s + \omega_{z5})(s + \omega_{z6})}{(s + \omega_{p1})(s + \omega_{p2})} \right] \text{dB} \quad (3.20a)$$

$$\omega_{p1} = \frac{a\% - b\%}{2(a\% - b\%)[(1 + c\%d\%)C_{D1} + (1 + e\%d\%)C_{D2}]R_g - (1 - a\%^2)(b\% + c\%)R_D C_D} \quad (3.20b)$$

$$\omega_{p2} = \frac{1}{(1 + d\%)R_g [(1 + c\%)C_{D1} + (1 + e\%)C_{D2}]} \quad (3.20c)$$

ω_{z1} , ω_{z2} , ω_{z3} , ω_{z4} , ω_{z5} , ω_{z6} are at high frequency (above audio frequency)

From a practical perspective, the layout design for C_{int2} , C_{int4} , R_{g1} and R_{g2} can be relaxed.

- (ii) The dominant pole, ω_{p1} , is derived as eqn. (3.20b). This corner frequency is largely determined by the resistor matching between R_1 and R_2 (a%), and R_{fb1} and R_{fb2} (b%). These resistor matchings dominate the PSRR at low frequency (below the corner frequency).
- (iii) Beyond the corner frequency, the PSRR of the CDA with 2nd-order integrators decreases at a rate of $\sim 20\text{dB/decade}$ within audio frequencies; zeros are located far beyond 20kHz. This is similar to the PSRR of the CDA with 1st-order integrators.
- (iv) Further to (iii), and from eqn. (3.20), smaller mismatches (i.e., smaller a%, b%, c%) result in better PSRR for frequencies above the corner frequency.

3.4 Verification and Results

In this section, the derived analytical expressions (i.e., eqns. (3.15) and (3.16a) for CDAs embodying 1st-order integrators; and eqns. (3.19) and (3.20a) for CDAs embodying 2nd-order integrators) are verified by means of HSPICE simulations and on the basis of physical measurements on discretely-realized CDAs. The CDAs are realized using commercial-off-the-shelf discrete components: TLV3502 as the comparator, THS4521ID as the differential op amp and MCP1404-E/SN as the driver. A supply $V_{DD} = 5\text{V}$ and an 8Ω load are used. As per testing standards, for PSRR measurements, the input is grounded. The power supply with noise ($V_{DD} + V_N$) is obtained from the *Rohde & Schwarz* SMU 200A Vector Signal Generator and measurements are obtained by means of the *Rohde &*

Table 3-3: Circuit Parameters of the 1st- and 2nd-order Double-feedback BTL PWM CDAs

	1 st -order	2 nd -order
R_1, R_2, R_3, R_4	6k Ω	6k Ω
$R_{fb1}, R_{fb2}, R_{fb3}, R_{fb4}$	6k Ω	6k Ω
$R_{g1}, R_{g2}, R_{g3}, R_{g4}$	-	3k Ω
$C_{int1}, C_{int2}, C_{int3}, C_{int4}$	0.5nF	1nF
$C_{int5}, C_{int6}, C_{int7}, C_{int8}$	-	1nF
G_{PWM}	2	2

Schwarz UPV Audio Analyzer. The measured bandwidth of the CDAs is from 20Hz to 10kHz.

The designed circuit parameters of the CDAs with the 1st- and 2nd-order integrators are tabulated in Table 3-3, where for fair benchmarking, the parameters for the 1st- and 2nd-order integrators are selected such that they have the same switching frequency attenuation, where the same fully-differential op amps are employed. For both types of CDAs, the switching frequency is ~250 kHz.

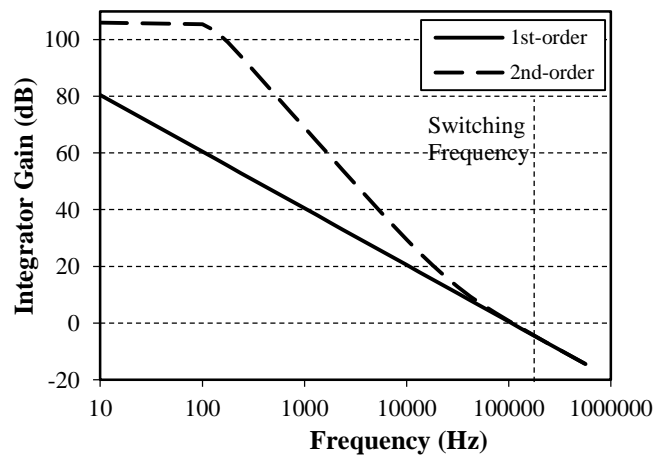


Fig. 3-8: Simulated gains of the 1st- and 2nd-order integrators

The simulated gains of the 1st- and 2nd-order integrators are shown in Fig. 3-8 (where the DC gain of the differential op amp is 100dB and the bandwidth is 100Hz). For completeness, it is worthwhile to note that for mobile devices where the power dissipation is typically critical, the high frequency components (beyond the 20kHz audio range) due to switching should be greatly attenuated by the integrators (i.e., low gain). This reduces the power dissipation due to the high frequency current and the noise at the output of CDAs. Put simply, the attenuation of the switching frequency is an important design parameter for the fully-differential integrators in CDAs (and for single-ended integrators in single-ended CDAs). At low frequencies, the gains of 1st- and 2nd-order integrators are limited by the finite open-loop gain of the fully-differential op amps. The 2nd-order integrators have higher gain in the lower range (about 10Hz to 100kHz), and the gains of 1st- and 2nd-order integrators converge around the switching frequency due to the dominant effect of the capacitances.

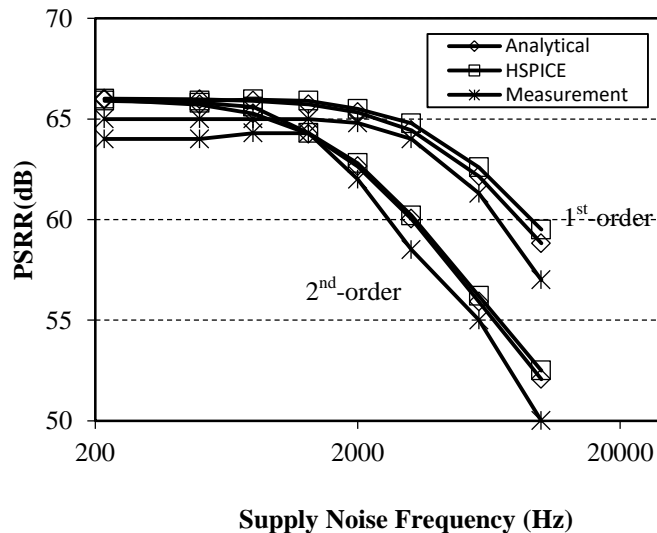


Fig. 3-9: PSRR of the 1st- and 2nd-order CDA obtained analytically (eqns. (3.15) (3.16a) (3.19) and (3.20a)), and from HSPICE simulations and measurement

Fig. 3-9 depicts the PSRR of the 1st- and 2nd-order CDAs against the supply noise frequency. In both designs, a%=0.1%, b%=0.2%, c%=1%, d%= 0.15%, e=1%, the same resistor and capacitor mismatches apply to the inner integrators, and A is equal to 2. On the basis of Fig. 3-9, we make the following observations:

- (i) The analytical results largely agree with both the results obtained from simulations and from physical measurements, thereby verifying the analytical expressions derived herein.
- (ii) From Fig. 3-8, the gain of the 2nd-order integrator is significantly higher than that of the 1st-order integrator. Nevertheless, from Fig. 3-9, somewhat surprisingly, the 1st-order integrator CDA provides similar or better PSRR than the 2nd-order integrator CDA if both integrators are designed to the same switching frequency attenuation. This is because the effective mismatches (the third terms within the parentheses of eqns. (3.15) and (3.19)) depend not only on the mismatches of the outer integrator (i.e., a%, b% and c%), but also on the gain of the outer integrator (G_{int1}); G_{int1} contributes to the loop gain (LG) of the CDA. Put differently, as the gain of the integrator increases, the mismatches of the integrator result in a larger difference to the gains of the two branches, i.e., effectively, an increased mismatch. Hence, the effect of the LG can be in part cancelled by the effective mismatch.
- (iii) Below the corner frequency, ω_p , the PSRR for the 1st- and 2nd- order CDAs are largely similar. From our analytical expressions in eqns. (3.16a) and (3.20a), it can be seen that this is because at low frequencies, the PSRR is largely determined by the difference between a% and b% (i.e., a%-b%). This therefore indicates that the

LG has little effect on the PSRR below the corner frequency.

- (iv) Further to aforesaid (iii), for frequencies above the corner frequency, the 2nd-order integrator CDAs are more sensitive to mismatch than the 1st-order integrator CDAs, thereby leading to worse PSRR ($\sim 6\text{dB}$ lower). Further, as the frequency increases, the LG of both the 1st- and 2nd-order CDAs decreases and their ensuing PSRR decreases at a rate of $\sim 20\text{dB/decade}$ beyond their respective corner frequencies. This can be seen from the eqns. (3.16a) and (3.20a), where only one dominant pole exists within the audio frequency. This also implies that above the corner frequencies, the higher loop gain LG results in higher PSRR – this unlike the case before the corner frequency (see comment (iii)). This ‘not apparent’ insight can be obtained from our derived eqns. (3.15) and (3.19).

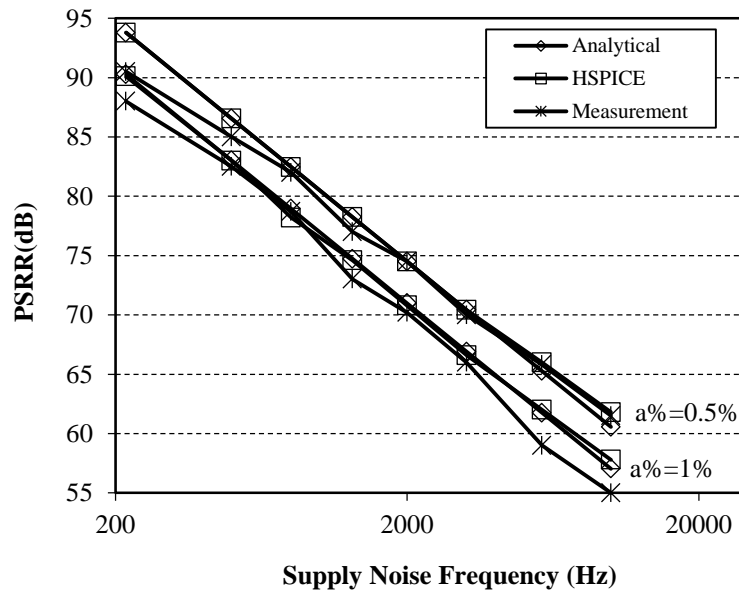


Fig. 3-10: PSRR of the 1st-order CDA obtained analytically (eqns. (3.15) and (3.16a)), and from HSPICE simulations and measurements

Fig. 3-10 depicts the PSRR of the 1st-order CDA for two different cases – Case 1: $a\%=b\%=0.5\%$, and Case 2: $a\%=b\%=1\%$. For both cases, $c\%=0.5\%$, $A=2$, and the same resistor and capacitor mismatches apply to the inner integrators. We note the following:

- (i) The analytical results largely agree with simulations and experimental results, thereby verifying the analytical expressions derived herein.
- (ii) For $a\%=b\%$, there is no corner frequency ($\omega_p=0$). This is analytically predicted by eqn. (3.16b).
- (iii) A comparison of the PSRR for Cases 1 and 2 depicts that reducing the mismatch ($a\%$ and $b\%$) by half would improve the PSRR by $\sim 3\text{dB}$. This insight can be obtained from eqn. (3.16) and provides the CDA designer a means to trade-off some design parameters.

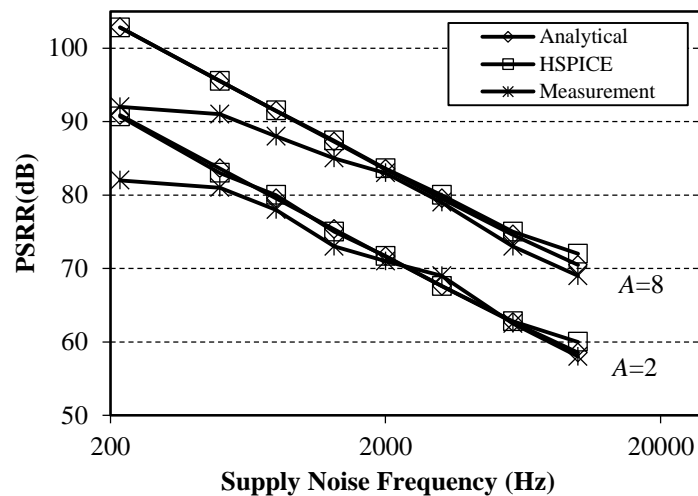


Fig. 3-11: PSRR of the 2nd-order CDA obtained analytically (eqns. (3.19) and (3.20a)), and from HSPICE simulations and measurements

Fig. 3-11 depicts the PSRR of the 2nd-order integrator CDA with the AC ground at different noise levels, i.e., $A=2$ and $A=8$ (under the condition $a\%=b\%=d\%=0.2\%$, $c\%=e\%=0.5\%$, and the same resistor and capacitor mismatches apply to the inner integrators). We note the following:

- (i) The analytical results largely agree with that from simulations and measurements, thereby verifying the analytical expressions herein.
- (ii) As expected, the noise level on the reference, quantified by the noise attenuation term A , has a significant effect on the overall PSRR where as expected, the higher the noise, the lower is the PSRR.
- (iii) The comparison between the CDAs with $A=2$ and $A=8$ shows that a reduction of A by 4x (from $A=8$ to 2) would drastically reduce the PSRR by $\sim 12\text{dB}$. Put simply, it is definitely worthwhile in CDA designs to embody a low-noise half- V_{DD} voltage reference to achieve high PSRR.

3.5 Conclusions

We have discussed the effect of the supply noise in the AC ground to the PSRR and PS-IMD of the open-loop PWM CDAs and have ascertained the effect of the architecture of the CDA and of the carrier generator. We have also analytically investigated the PSRR of 3-state PWM BTL closed-loop PWM CDAs based on the double-feedback topology, taking into account the non-ideal AC ground and the mismatches between resistors and capacitors. Analytical expressions to model/predict the PSRR for said CDAs have been derived and subsequently verified by both simulations

and hardware measurements. These derived analytical expressions have been shown to provide valuable insights to the design of CDAs.

Appendix

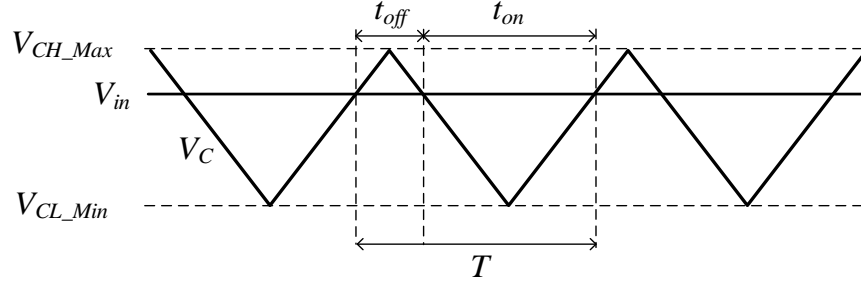


Fig. 3-A1: Waveforms of the input signal and the carrier signal

In this Appendix, the procedures to derive the results in Table 3-1 will be delineated in details. For ease of elaboration, the waveform of the input signal V_{in} and the carrier signal V_C are depicted in Fig. 3-A1. When $V_{in} > V_C$, the output stage is turned “on” (output voltage is $V_{DD} + V_N$). Conversely, when $V_{in} < V_C$, the output stage is turned “off” (output voltage is 0). The “on” and “off” periods, t_{on} and t_{off} , of the output stage can be expressed as eqn. (3.A1) and (3.A2).

$$t_{on} = 2(V_{in} - V_{CL_Min}) \times \frac{C_C}{I} \quad (3.A1)$$

$$t_{off} = 2(V_{CH_Max} - V_{in}) \times \frac{C_C}{I} \quad (3.A2)$$

Based on Fig. 3-1(a), the output signal of a single-ended CDA, V_{SE} , can be derived by taking the average value of the output voltage over one carrier period.

$$V_{SE} = \frac{t_{on} \times (V_{DD} + V_N)}{T} \quad (3.A3)$$

For a 2-state or 3-state BTL CDA, the output signal are the difference between the output of the upper branch and the lower branch. The output of each branch can be derived by using the same method for the single-ended CDA. Put simply, let t_{on1} and t_{on2} be the “on” periods of the upper branch and lower branch, respectively. The output of a 2-state and 3-state BTL CDA can be derived by eqn. (3.A4) [18, 48].

$$V_{2State} = V_{3State} = \frac{(t_{on1} - t_{on2}) \times (V_{DD} + V_N)}{T} \quad (3.A4)$$

As discussed in eqns. (2.2) and (2.3) in Section 2.3, PSRR and PS-IMD are due to the noise component at the output of a CDA. Based on the derived output voltage in eqns. (3.A3) and (3.A4), PSRR and PS-IMD can be calculated. Here, we take PSRR and PS-IMD of a single-ended open-loop CDA with Carrier Generator III as an example. For Carrier Generator III, t_{on_III} can be derived based on eqns. (3.6) and (3.7). The output of the open-loop CDA, V_{SE_III} , can be subsequently derived.

$$t_{on_III} = \frac{V_{in} G_{PWM}}{V_{DD}} T_0 - \frac{R_{C2}}{2R_{C3}} T_0 - \frac{V_N}{AV_{DD}} \frac{R_{C2}}{R_{C3}} T_0 + 2t_D \quad (3.A5)$$

$$V_{SE_III} \approx (V_{in} - V_{CM}) G_{PWM} + \frac{4t_D}{T_0} \frac{V_N}{V_{DD}} (V_{in} - V_{CM}) G_{PWM} + \frac{1}{2} V_{DD} + \frac{V_N}{A} + \frac{2t_D}{T_0} V_N \quad (3.A6)$$

The input of the CDA, V_{in} , and the supply noise component on the supply rail, V_N , can be expressed as:

$$V_{in} = \frac{MV_{DD}}{2G_{PWM}} \cos(\omega_{in} t) + V_{CM} \quad (3.A7)$$

$$V_N = NV_{DD} \cos(\omega_n t) \quad (3.A8)$$

where ω_{in} and ω_n are the input and noise frequency in rad/s respectively, M is the modulation index, N is the normalized magnitude of the supply noise.

Based on eqns. (3.A7) and (3.A8), eqn. (3.A6) can be rewritten as eqn. (3.A9). It comprises the desired output (first and second terms), the output noise components at noise frequency ω_n (third term), and the output noise components at frequency $\omega_{in} \pm \omega_n$ (fourth term). The PSRR and PS-IMD can be subsequently derived as eqns. (3.A10) and (3.11A).

$$V_{SE_III} = \frac{1}{2}MV_{DD} \cos(\omega_{in}t) + \frac{1}{2}V_{DD} + \left(\frac{1}{A} + \frac{2t_D}{T_0}\right)NV_{DD} \cos(\omega_n t) + \frac{t_D}{T_0}MNV_{DD} \cos[(\omega_{in} \pm \omega_n)t] \quad (3.A9)$$

$$PSRR = -20 \log \left[\frac{\left(\frac{1}{A} + \frac{2t_D}{T_0}\right)NV_{DD}}{NV_{DD}} \right] = -20 \log \left(\frac{1}{A} + \frac{2t_D}{T_0} \right) \text{dB} \quad (3.A10)$$

$$\begin{aligned} PS\text{-}IMD &= -20 \log \left[\frac{1}{NV_{DD}} \sqrt{\left(\frac{t_D}{T_0}MNV_{DD}\right)^2 + \left(\frac{t_D}{T_0}MNV_{DD}\right)^2} \right] \\ &= -3 + 20 \log M + 20 \log \left(2 \frac{t_D}{T_0} \right) \text{dB} \end{aligned} \quad (3.A11)$$

Chapter 4 A Wide Bandwidth High Power-efficiency Supply Modulator for Wideband Applications

4.1 Introduction

A large portion of this chapter has been submitted to IEEE Transactions on Power Electronics [89] and is under revision.

As delineated in Chapters 1 and 2, short battery lifespan is one of the challenges of mobile communication devices and is exacerbated with the demand for ever-increasing speed and data. This is in part due to the adopted communication standards, e.g. LTE and LTE-A, that employ spectrally efficient modulation schemes and wide bandwidth. These advanced communication standards impose stringent requirements on the linearity of the RF PA, yet requiring high PAPR [88] – translating to low power-efficiency in conventional RF PAs [53], hence reduced battery-life.

Of the various reported methods to improve the power-efficiency of RF PAs (see Chapter 1), the ET PA has been reported to be one of the most effective means [58-81]. The mechanism thereto is the supply modulator in the ET PA constantly providing a dynamically changing supply to the RF PA based on the time-varying envelope of the RF signals. In this fashion, the RF PA is kept nearly always in compression, where its power-

efficiency is high, hence avoiding operation in the back-off condition.

Many supply modulators in ET PAs employ a hybrid topology (switching-cum-linear) [65-78]. This is because the hybrid CDA features higher power-efficiency compared to the Class AB amplifier-only topology [81], higher bandwidth and lower output ripple compared to the CDA-only topology [58-64]. Nevertheless, at this juncture, the major shortcoming of state-of-the-art supply modulators [65-74, 76-78] is their limited (and insufficient) bandwidth of $\leq 20\text{MHz}$, which is insufficient for LTE-A applications whose bandwidth is 40MHz-100MHz. Another shortcoming is the low output power. For instance, the reported designs in [66, 68, 69] operate at a low supply voltage of 1.2V supply, hence resulting a low output voltage of $< 1\text{V}$ and low maximum output power of $< 0.2\text{W}$. This low output power is, however, generally unacceptable for the recent communication standards including LTE and LTE-A. The typical output power of a LTE/LTE-A RF PA is $\sim 27\text{dBm}$ (0.5W) taking into account the duplexer and antenna losses. Hence, the output power of the supply modulator would need to be $> 1\text{W}$ for the III/V-based RF PA (with $\sim 45\%$ power-efficiency) and $> 2\text{W}$ for CMOS-based RF PA (with $\sim 25\%$ power-efficiency). The limited bandwidth and/or output power is in part due to the inevitable trade-off between bandwidth, output power, output noise and power-efficiency.

In this chapter, we propose a hybrid CDA as the supply modulator for ET PAs to provide wide bandwidth and sufficient output power for LTE and 40MHz LTE-A signals, with high power-efficiency, high output voltage swing and low ripple noise. We achieve this by the following. First, we investigate the power dissipation and optimization method of the supply modulator for wideband applications taking into consideration the effect of

the propagation delay (a previously unexploited but imperative parameter). We show that the threshold current is unnecessary – in fact a controller with zero threshold current results not only high bandwidth but also high power-efficiency for wideband supply modulators. Second, based on the first, we propose a delay-based hysteresis controller for the supply modulators. The proposed controller embodies a novel high-speed current comparator to compare the ripple current with zero current, instead of the conventional approach [66, 71, 73, 84] embodying a hysteresis comparator with a threshold current. By this means, higher power-efficiency and simpler hardware are achieved. Third, a wideband Class AB amplifier with an accurate quiescent current control and sufficient driving capability are proposed. Collectively, the proposed supply modulator features the highest bandwidth (40MHz), yet with high output power (2.5W), high peak efficiency (91%), high output voltage swing (3V) and low output noise (4mVrms) at 3.6V supply, compared to reported designs [58-81]. When the prototype supply modulator is embodied in an ET PA for tracking 20MHz LTE envelope signals, the ET PA achieves a high power-efficiency of 41.4% at peak output power of 28.5dBm and 34.4% at 3dB backoff – a significant >1.6x improvement over the RF PA without the supply modulator. The prototype supply modulator is fabricated in a commercial 180nm CMOS process.

4.2 Design Optimization for Wideband Applications

Fig. 4-1 depicts the block diagram of a supply modulator, comprising a wideband Class AB amplifier, a high-efficiency CDA and a hysteresis controller. The supply modulator provides a variable power supply to the RF PA; for convenient and fair

evaluation of supply modulator, the RF PA is presented by a 6.7Ω resistive load in our analysis. The output current, i_O , of the supply modulator is the sum of the output current, i_{AB} , of the Class AB amplifier and the output current, i_D , of the CDA, i.e., $i_O = i_{AB} + i_D$.

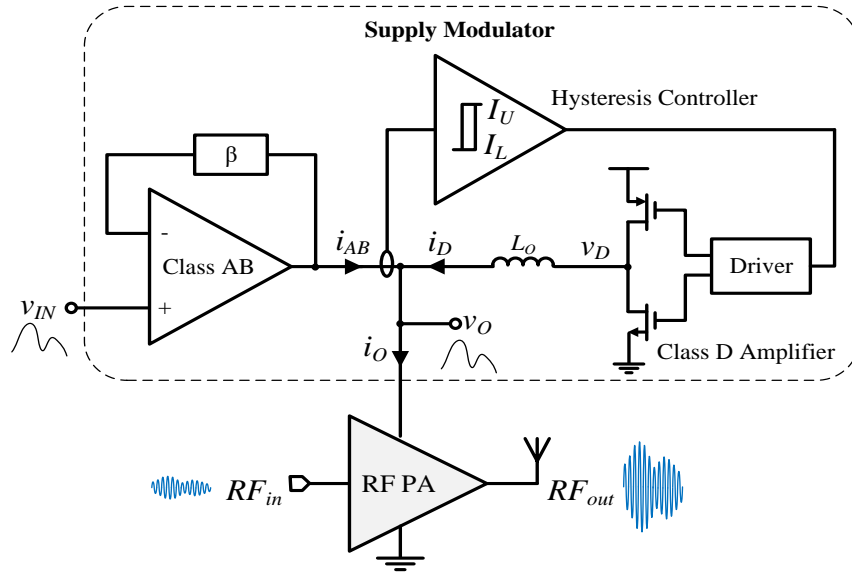


Fig. 4-1: Block diagram of an ET PA with a supply modulator

Fig. 4-2 depicts the simulated frequency response of i_{AB} and i_D , where the DC voltage of the input signal is 1.8V and the AC amplitude is $1.4V_{pp}$. In the low frequency range ($<5\text{MHz}$), i_D is much higher than i_{AB} , and both i_D and i_{AB} remain largely unchanged. In this frequency range, i_D provides most of the output current whilst i_{AB} provides the ripple current due to switching of the CDA; see Fig. 4-3(a) later. In the high frequency range ($>5\text{MHz}$), i_{AB} increases with the frequency whilst i_D reduces with the frequency. This is because in the high frequency range, the CDA is unable to provide sufficient high frequency current and the Class AB amplifier needs to provide not only the ripple current

(due to the switching of the CDA) but also the high frequency components of the output signal; see Fig. 4-3(b) later.

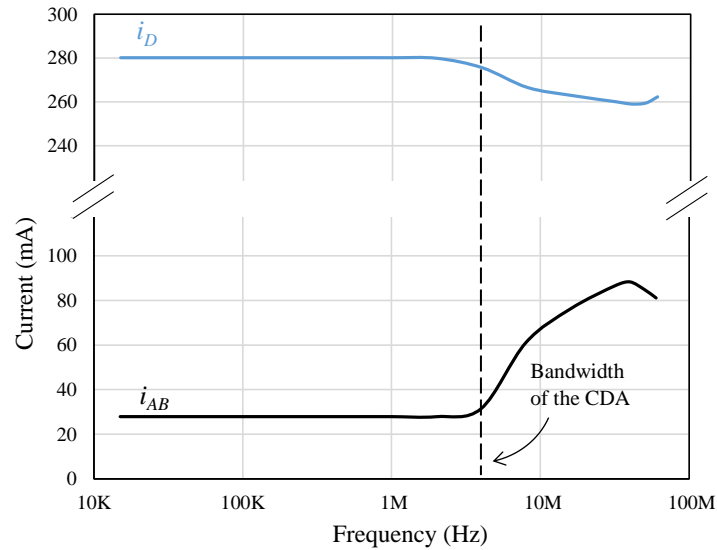


Fig. 4-2: Simulated frequency response of i_{AB} and i_D

Conventionally [66, 71], it is assumed that the threshold currents, $\pm I_T$, of the hysteresis comparator are the actual upper limit, I_U , and lower limit, I_L , of the hysteresis current, and the effect of the propagation delay, t_D , is ignored. However, this is only true for narrowband applications (i.e., low frequency signals, such as EDGE, CDMA envelope signals) whose switching frequency is low (hence the switching period is much longer than t_D). We will now show that due to t_D , this is not the case of the supply modulator for wideband applications (i.e., high frequency signals, such as LTE, LTE-A envelope signals). The optimization of the supply modulator for wideband applications, taking into consideration t_D , will be delineated thereafter.

4.2.1 Effect of Threshold Current and Propagation Delay on Hysteresis

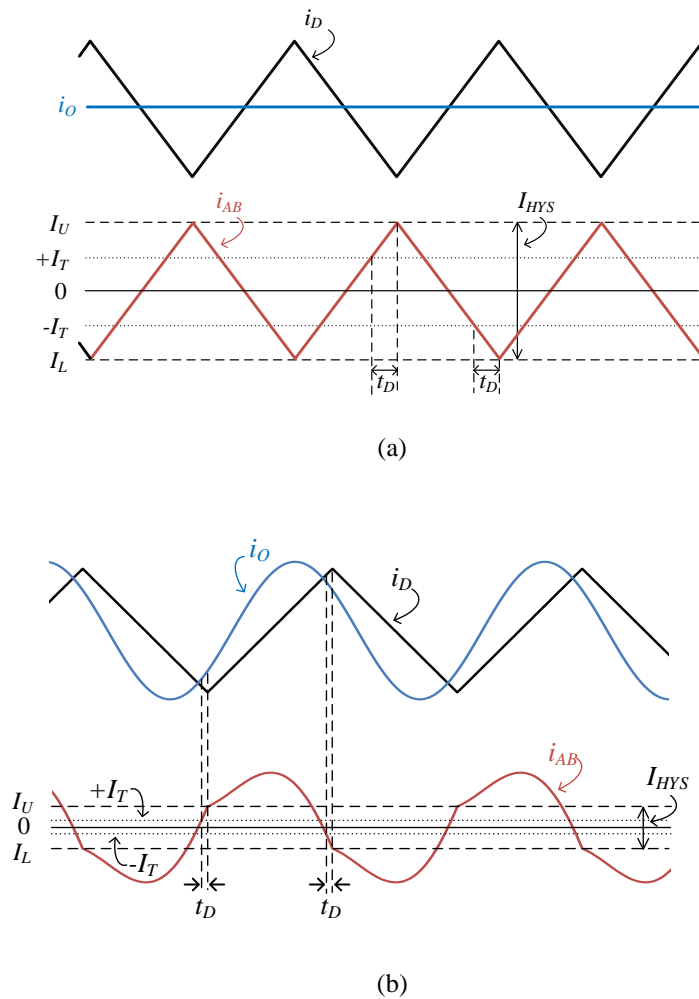


Fig. 4-3: Typical current waveforms of the supply modulator tracking (a) low frequency input signals (b) high frequency input signals

The threshold currents of the hysteresis comparator, $\pm I_T$, are ideally the upper and lower limits of the hysteresis current of the supply modulator. However, due to t_D , the actual upper and lower limits of hysteresis current are conversely I_U and I_L , shown in Figs. 4-3(a) and 4-3(b). Based on Figs. 4-1, 4-3(a) and 4-3(b), I_U and I_L are derived as eqns.

(4.1a) and (4.1b) respectively, which are a reasonable approximation of I_U and I_L for both narrowband applications and wideband applications.

$$I_U = I_T + \frac{V_{DD} - v_O}{L_O} \times t_D \quad (4.1a)$$

$$I_L = -I_T - \frac{v_O}{L_O} \times t_D \quad (4.1b)$$

where v_O is output voltage, V_{DD} is the supply, and L_O is the external inductor in Fig. 4-1.

We define the hysteresis current I_{HYS} as the difference between the upper and lower limits, i.e., $I_{HYS} = I_U - I_L$. It is straightforward to derive I_{HYS} as expressed in eqn. (4.2a). I_{HYS} comprises 2x of the threshold current, $2I_T$, of the hysteresis comparator, and the intrinsic hysteresis, I_{HYS_int} , expressed in eqn. (4.2b). I_{HYS_int} arises from the propagation delay, t_D , and also is affected by the external inductor, L_O , and supply voltage, V_{DD} .

$$I_{HYS} = I_U - I_L = 2I_T + I_{HYS_int} \quad (4.2a)$$

$$\text{where } I_{HYS_int} = V_{DD} \times \frac{t_D}{L_O} \quad (4.2b)$$

In the reported supply modulator designs [66, 71], I_{HYS_int} is typically assumed to be negligible, i.e., $I_{HYS} = 2I_T$. This is true for supply modulators with narrow bandwidth whose switching frequency is low, but it is not the case for wideband supply modulators.

Compared to the supply modulator optimized for narrowband applications, smaller L_O is normally used for wideband applications. This is because in wideband supply modulators, the switching frequency of the CDA is normally designed to be high

(>10MHz) [66-71] to extend the bandwidth of the CDA and to reduce the current burden of the power-inefficient Class AB amplifier, hence featuring high power-efficiency. This high switching frequency is facilitated by employing a relatively small external inductor L_O [71], e.g. 1 μ H in our design (see Section 4.2.2 for the optimization of the external inductor).

On the other hand, t_D in eqn. (4.2b) is relatively long in supply modulators with high output power (>1W) because t_D from the output stage of the CDA is relatively long for the following reasons. First, to provide high output power, $V_{DD} > 3V$ is typically adopted in the supply modulators [58-63, 65, 67, 70-76, 79, 81, 84]. Consequently, to prevent simultaneously turning on both the high-side and low-side power transistors in the Class D output stage (i.e., to reduce the short-circuit current), an anti-shoot-driver with a relatively long dead time (several ns) [71, 73, 84] is generally employed. Second, the size of the power transistors in the output stage of the CDA is large to realize a small output impedance, hence low conduction loss. These large power transistors have relatively large parasitic capacitance, which undesirably results in a long propagation delay [27, 35].

Put simply, as evident in eqn. (4.2b), L_O is relatively small and t_D is relatively long for wideband supply modulators with high output power, resulting in an undesirably high I_{HYS_int} , vis-à-vis I_{HYS_int} assumed to be negligible. I_T is generally several to several tens of mA [66, 68, 71]. As a case in point, in our proposed supply modulator (see Fig. 4-5 later), with $t_D = 7ns$, $L_O = 1\mu H$, and $V_{DD} = 3.6V$, the intrinsic hysteresis I_{HYS_int} is 25mA. Hence, the delay in wideband supply modulators has a significant (not-negligible) effect on the hysteresis current.

4.2.2 Optimization of Hysteresis and External Inductor

We will now describe our proposed optimization means that takes into account the propagation delay t_D .

As delineated in Chapter 2, the power dissipation of the supply modulator comprises three parts – P_{loss_Ind} due to the external inductor, P_{loss_D} due to the CDA, and P_{loss_AB} due to the Class AB amplifier. For wideband applications, the optimization method is different from the case for narrowband envelope signals. In this case, the switching frequency reduces and depends on the input frequency only as observed in Fig. 4-3(b). In other words, f_{sw} is independent of I_{HYS} and fixed for a specific envelope signal; and P_{loss_D} is relatively small. P_{loss_AB} in this case is determined by (i) the bandwidth of the CDA, (ii) the delay between CDA and Class AB amplifier, and (iii) quiescent power loss of the Class AB amplifier. For (i), the current swing (peak-to-peak value) of the i_D in Fig. 4-3(b) is determined by the L_O . A small L_O is preferred to achieve a large bandwidth of CDA; hence more AC current will be delivered by the power-efficient CDA and less current is needed from the Class AB amplifier. For (ii), the delay between the CDA and the Class AB amplifier increases the distortion at the output of the CDA, hence resulting in increased current flow in the Class AB amplifier to compensate for the distortion. Therefore, to reduce the power dissipation, the delay should be as low as possible. The delay of the CDA is contributed by I_{HYS} , and it includes the delay due to the Class D output stage, t_D , and the threshold currents of hysteresis comparator, $\pm I_T$. In view of this, $I_T=0$ is recommended, consequently reducing I_{HYS} to I_{HYS_int} . For (iii), by reducing the current burden of the Class AB amplifier, the Class AB amplifier can be designed with a

small quiescent current I_Q and wider bandwidth, hence further improving the power-efficiency and extending the bandwidth of the supply modulator.

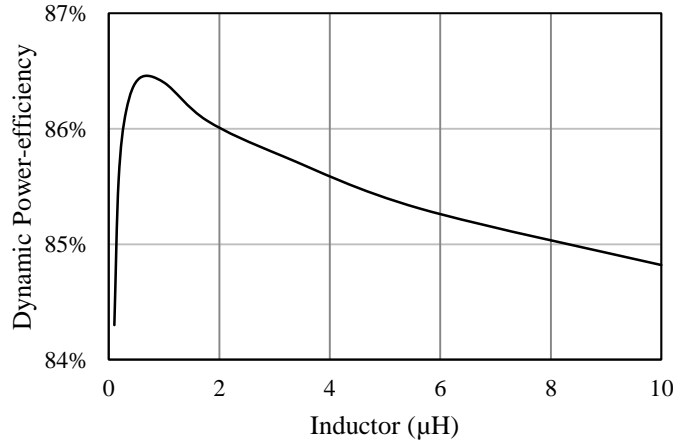


Fig. 4-4: Simulated power-efficiency with various external inductors

In this work, our design (see Fig. 4-5 later) is optimized for tracking wideband envelope signals, particularly for tracking 40MHz LTE-A envelope signals. The optimization procedure is delineated now. First, we begin the design with the estimation of the overall performance based on our experience and the optimization presented above. Specifically, for 40MHz LTE-A envelope signals, we recommend that the average switching frequency of the supply modulator is ~20MHz, and the bandwidth of the Class AB amplifier is >200MHz with >200mA driving capability. Second, the design is simulated for tracking dynamic envelope signals extracted from 40MHz LTE-A RF signals (1.2W output power) with various inductors. The parasitic resistance of the external inductor is approximated by $R_L \approx 0.05\Omega + 0.01\Omega/\mu\text{H} * L_O$ – this is typical for commercial surface mount inductors with sufficient current rating. Third, based on the simulation results, the power losses P_{loss_D} , P_{loss_AB} , and P_{loss_Ind} can be ascertained and the

inductor can be selected to achieve the minimum total power loss. As explained earlier, the supply modulator involves many tradeoffs between P_{loss_D} , P_{loss_AB} , and P_{loss_Ind} , several iterations may be conducted to optimize the design of the supply modulator. Following the optimization procedure, Fig. 4-4 shows the simulated power-efficiency for tracking 40MHz LTE-A envelope signals (1.2W output power) with various inductors. As shown in Fig. 4-4, the maximum power-efficiency of ~86.5% is achieved with 1 μ H inductor. Considering all the abovementioned trade-offs, L_O is chosen to be 1 μ H.

In short, for wideband supply modulators, I_{HYS} is primarily bounded by the intrinsic hysteresis, I_{HYS_int} , due to the propagation delay t_D – not the threshold current, I_T , of the hysteresis comparator as generally perceived. For wideband supply modulators, I_T is, in fact, unnecessary due to the propagation delay of the CDA. By reducing I_T , the output power of the Class AB amplifier is reduced, which in turn extends the bandwidth and improves the power-efficiency of the supply modulator. The external inductor, L_O , can be selected considering the trade-offs between the bandwidth of the CDA, the intrinsic hysteresis, I_{HYS_int} , and the parasitic resistance of the inductor, R_L , to optimize the power-efficiency of the wideband supply modulator.

4.3 Proposed Supply Modulator for Wideband Applications

4.3.1 System Architecture

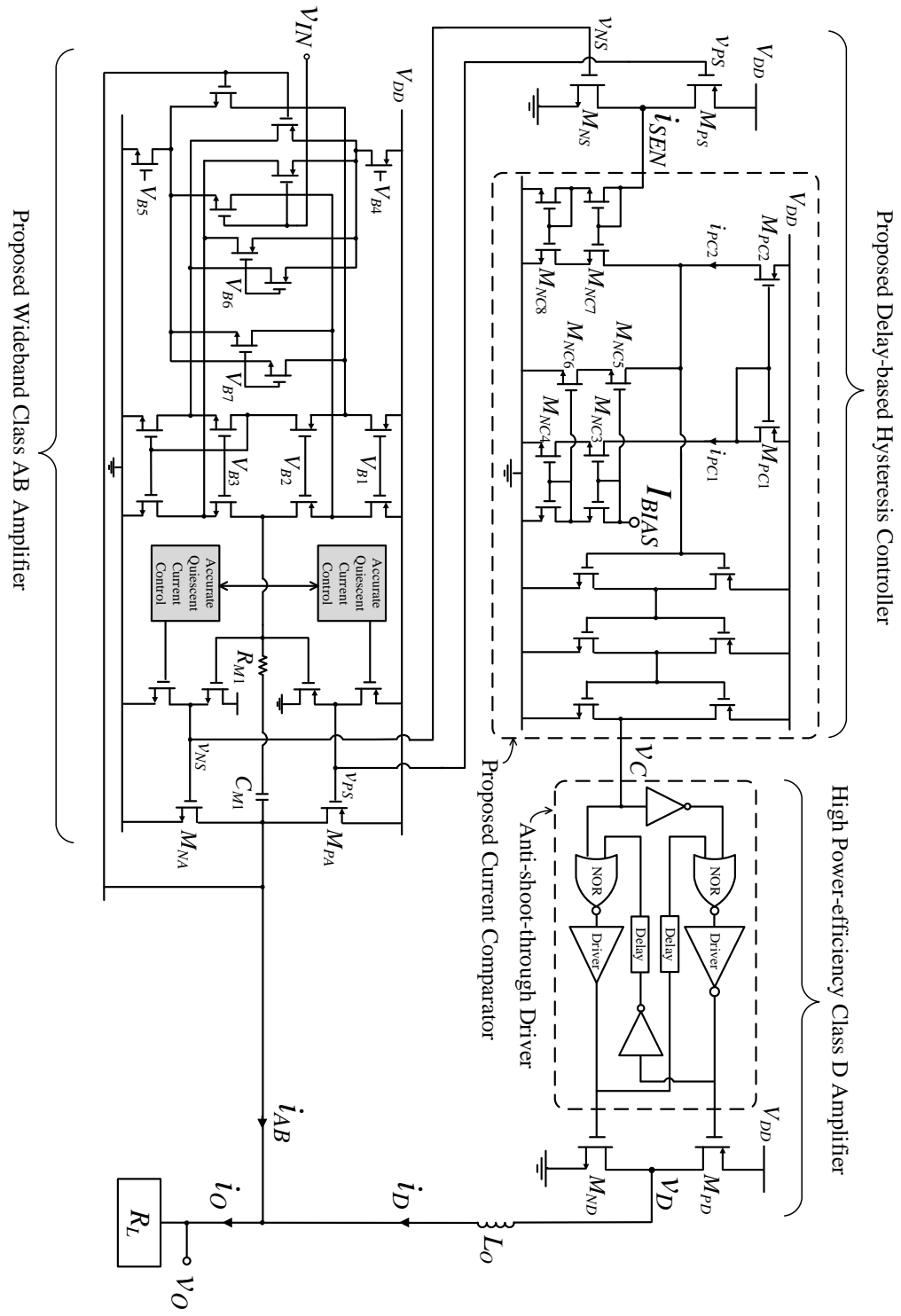


Fig. 4-5: Schematic of the supply modulator embodying a proposed delay-based hysteresis controller, a proposed wideband Class AB amplifier and a high power-efficiency CDA

We have shown in Section 4.2 that to obtain maximum power-efficiency, I_T should be 0. In other words, the hysteresis comparator should be delay-based. We will now discuss the design of our supply modulator embodying a delay-based hysteresis controller.

The schematic diagram of the proposed supply modulator is depicted in Fig. 4-5. With $I_T = 0$ in the proposed controller, the intrinsic hysteresis, I_{HYS_int} , arising from the propagation delay, t_D , determines I_U and I_L as given in eqns. (4.1a) and (4.1b). The ensuing output of the CDA, v_D , will ‘on’ (i.e., $v_D = V_{DD}$) when $i_{SEN} > I_U$, and v_D will ‘off’ (i.e., $v_D = 0$) when $i_{SEN} < I_L$. By this means, the proposed supply modulator embodies a large-signal negative feedback loop. According to the large-signal stability criterion [68], the stability of the supply modulator is assured by controlling the ripple current from the CDA to be within the driving capability of the Class AB amplifier. This is different from the small-signal feedback loop (e.g. the feedback loop in the Class AB amplifier) whose location of its poles and zeros is critical to the stability. In other words, despite the hysteresis, I_{HYS} , depending on the propagation delay, t_D , which may vary with the process variations, the supply modulator with delay-based hysteresis controller is stable if the Class AB amplifier has sufficient output current.

By circumventing the need for the conventional hysteresis comparator, the propagation delay of the comparator is significantly reduced, thereby further improving the power-efficiency and the ensuing hardware is simplified. Furthermore, by adopting a current comparator instead of the more prevalent voltage comparator, wider bandwidth is facilitated.

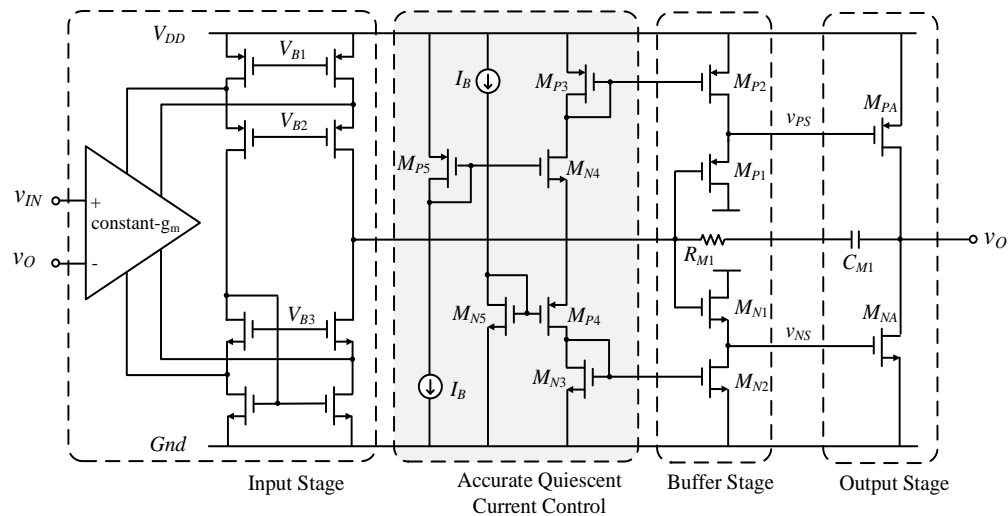
4.3.2 Proposed High-speed Current Comparator in the Hysteresis Controller

The major issue of the conventional current-mode comparator embodied in the supply modulators, e.g. [66], is that the upper and low limits of i_{AB} , I_U and I_L , are both positive (i.e., $I_U > 0$ and $I_L > 0$ vis-à-vis $I_U > 0$ and $I_L < 0$ in our proposed design). In the supply modulators with a conventional current-mode comparator, the Class AB amplifier therein is designed to always provide positive current. This results in an undesirably larger portion of i_o sourced from the Class AB amplifier, which in turn reduces the power-efficiency [68].

To circumvent this, a proposed high-speed current comparator (top left of Fig. 4-5) is embodied in the proposed delay-based hysteresis controller. The current mirror, M_{PC1} and M_{PC2} , serves to compare the currents, i_{PC1} and i_{PC2} , flowing through these transistors. The output of the comparator, v_C , is ‘on’ (i.e., $v_C = V_{DD}$) when $i_{PC2} > i_{PC1}$, and vice versa. By appropriate matching, transistors $M_{NC3} \sim M_{NC6}$ are biased at I_{BIAS} , and the current flowing through M_{NC7} and M_{NC8} is i_{SEN} . Consequently, $i_{PC1} = I_{BIAS}$ and $i_{PC2} = i_{SEN} + I_{BIAS}$. Instead of comparing i_{SEN} and I_{BIAS} in the conventional designs [66], $(i_{SEN} + I_{BIAS})$ is conversely compared with I_{BIAS} in the proposed current comparator. Consequently, the reference current (i.e., I_T) in our proposed current comparator is zero. By eliminating the need for a positive reference current, the supply modulator would feature higher power-efficiency.

4.3.3 Proposed Class AB Amplifier

In the proposed supply modulator in Fig. 4-5, a three-stage Class AB amplifier featuring wide bandwidth and high output power embodies a proposed accurate quiescent current control is designed. For sake of illustration, the three stages of the Class AB amplifier, input, buffer, and output stages, are identified in Fig. 4-6(a), and the model of the three-stage Class AB amplifier is depicted in Fig. 4-6(b). The input stage features rail-to-rail input embodying the well-known constant- g_m technique, and embodies a folded-cascode amplifier to achieve stable and relatively high open-loop gain. The buffer stage embodies two source followers. The output stage is designed as a common-source amplifier to provide high current driving capability with rail-to-rail output swing.



(a)

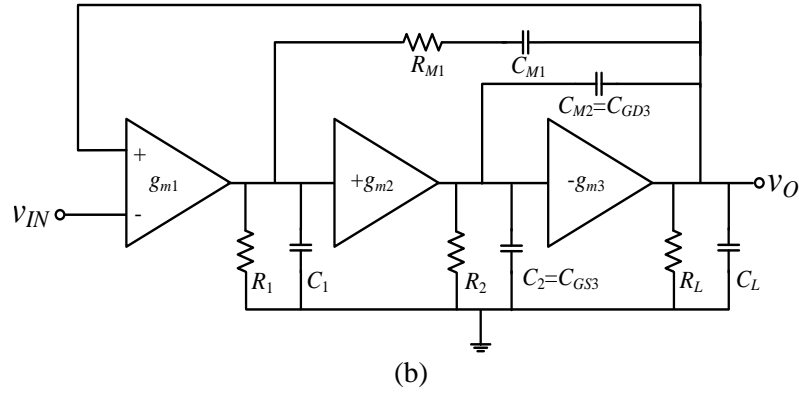


Fig. 4-6: The proposed wideband Class AB amplifier (a) simplified schematic, and (b) model

In the Class AB amplifier, the largest parasitic capacitances therein are the gate-source and gate-drain capacitances, C_{GS3} and C_{GD3} , of the power transistors, M_{PA} and M_{NA} , in the output stage. These large power transistors, occupying $\sim 50\%$ of the chip area of the Class AB amplifier, are designed for low open-loop output impedance and to provide high output current to track the high-frequency input signals. The poles and zeros due to these large parasitic capacitances are critical and are sensitive to process variations. We accommodate them as follows.

In Fig. 4-6(b), we model C_{GD3} (i.e., C_{M2}) as a Miller capacitor across the output stage, and C_{GS3} (i.e., C_2) as the input capacitance of the output stage. The source followers in the buffer stage extend the bandwidth of the supply modulator by means of its small C_1 (input capacitance of the source follower) at the output of the input stage and a small R_2 (output impedance of the source follower) at the input of the output stage. This subsequently pushes the non-dominant poles due to parasitic capacitances, i.e., $1/R_1C_1$ and $1/R_2C_2$, to high frequencies. A small Miller capacitor, C_{M1} (3.2pF in our design), is added

across the buffer stage and the output stage to create a dominant pole, thereby mitigating the sensitivity and enhancing the stability.

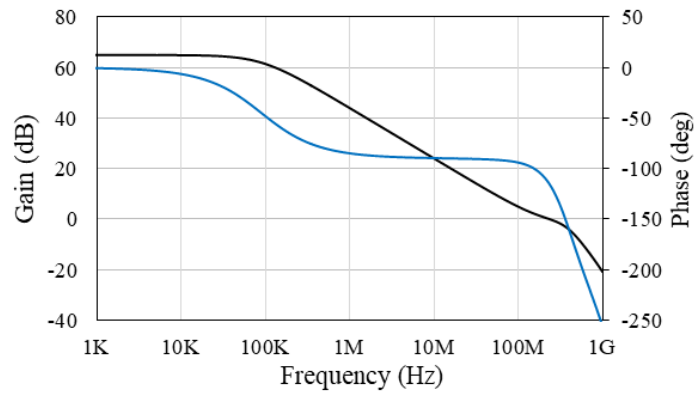
Although the three-stage amplifier with a buffer stage has many advantages, this structure is not commonly used in the designs of Class AB amplifier. This is because the quiescent current of power transistors, M_{PA} and M_{NA} , in this structure are sensitive to process variations and supply. To address this issue, an accurate quiescent current control, M_{P3} - M_{P5} and M_{N3} - M_{N5} shown in the shaded area in Fig. 4-6(a), is proposed. Two translinear circuit loops are formed: (1) M_{P4} , M_{N4} , M_{P5} and M_{N5} (2) M_{PA} , M_{NA} , M_{P1} and M_{N1} . Through the current mirrors (M_{P2} and M_{P3} , M_{N2} and M_{N3}), the biasing current of transistors M_{P1} and M_{N1} in loop (2) is controlled by the current of transistors M_{N4} and M_{P4} in loop (1). Due to the abovementioned circuit loops, the quiescent current of M_{PA} and M_{NA} is determined by I_B in M_{P5} and M_{N5} . By appropriately matching the transistors, the quiescent current of M_{PA} and M_{NA} is set to be $r \times I_B$ (r is 250 in the design).

Table 4-1: Results of corner simulations for quiescent current

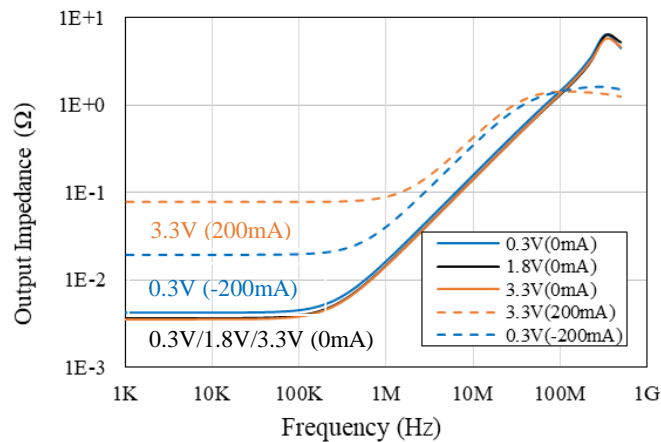
	Quiescent current (mA)			Quiescent current (mA)		
	without quiescent current control			with proposed quiescent current control		
Supply	3.5V	3.6V	3.7V	3.5V	3.6V	3.7V
typical	21.62	30.03	39.71	29.95	30.06	30.11
ss*	0.73	1.62	3.24	27.20	28.20	29.07
ff*	91.59	107.64	124.55	33.59	34.64	35.91
sf*	18.58	26.38	34.71	30.44	30.78	31.02
fs*	23.84	32.63	42.67	30.30	30.36	30.38

*ss=slow NMOS & slow PMOS; ff=fast NMOS & PMOS; sf=slow NMOS & fast PMOS; fs=fast NMOS & slow PMOS

To check the sensitivity of the quiescent current, corner simulations for our proposed design have been conducted, and the results are presented in Table 4-1. The bolded values in red color and in blue color indicate the worst cases and the nominal values, respectively. We can clearly see that without the accurate quiescent current control, the conventional structure is sensitive – the variations of the quiescent current can be unacceptable 300% bigger. With the proposed accurate quiescent current control, the quiescent current is significantly improved – the variations are controlled within 20%.



(a)



(b)

Fig. 4-7: Simulated results of the proposed Class AB amplifier (a) frequency response, and (b) closed-loop output impedance

The Class AB amplifier features high output swing, from 0.3V to 3.3V, and can drive 600mA at mid-rail, and 200mA at 0.3V and 3.3V. It also features a high slew rate of $\sim 250\text{V}/\mu\text{s}$. The simulated frequency response of the Class AB amplifier and its closed-loop output impedance are depicted in Figs. 5-7(a) and (b), respectively. It features a DC gain of 65dB, and GBW of $\sim 230\text{MHz}$ (with 64° phase margin and 6.5dB gain margin) for $6.7\Omega//100\text{pF}$ load. In the quiescent condition ($i_{AB} = 0$), the output impedance is small ($\sim 4\text{m}\Omega$) at frequencies below the dominant pole ($\sim 250\text{kHz}$), and the output impedance is $< 0.45\Omega$ at the maximum switching frequency of 35MHz. Under the worst-case operating conditions, i.e., the Class AB amplifier sourcing 200mA at 3.3V and sinking 200mA at 0.3V, the performance of the amplifier remains adequate. Specifically, when sourcing 200mA at 3.3V, the output impedance is $78\text{m}\Omega$ at low frequencies, and 1.08Ω at 35MHz; and when sinking 200mA at 0.3V, the output impedance is $19\text{m}\Omega$ and 0.96Ω at low frequencies and at 35MHz, respectively.

4.4 Measurement Results

Fig. 4-8 depicts the die micrograph of the prototype supply modulator fabricated in 180nm CMOS process where the core area is 0.6mm^2 in the 2.25mm^2 die. The prototype supply modulator is packaged in a $4\text{mm}\times 4\text{mm}$ QFN package.

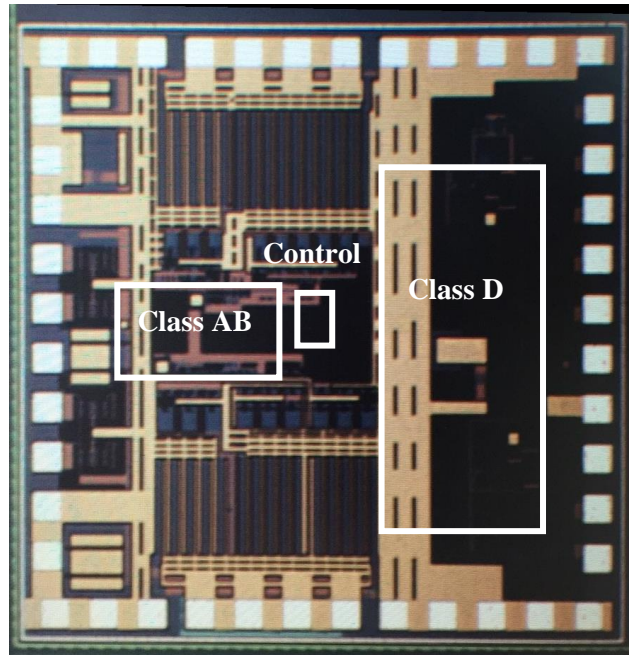


Fig. 4-8: Microphotograph of the prototype supply modulator

Congruous with the aforesaid trade-off, a small $1\mu\text{H}$ off-chip inductor, whose DC resistance and self-resonance frequency are 0.06Ω and 490MHz , respectively, is selected. A 100pF load capacitance is added at the output of the supply modulator to filter the high frequency noise. In Fig.4-9 – Fig. 4-13, a 6.7Ω load is used to ascertain the performance of the supply modulator, as it corresponds to our testing of a commercial RF PA whose $V_{DD} = 3.2\text{V}$ (i.e., $v_o = 3.2\text{V}$ for the supply modulator) and 28.5dBm output power. For completeness, in Fig. 4-14 and Fig. 4-15, the tests include an evaluation of the overall performance of the ET PA embodying our supply modulator as the supply of a commercial RF PA. The RF signals and the envelope signals were generated from the vector signal generator and the measurements of the output power spectrum were obtained using the signal and spectrum analyzer. In all measurements, $V_{DD} = 3.6\text{V}$ was used for our supply modulator.

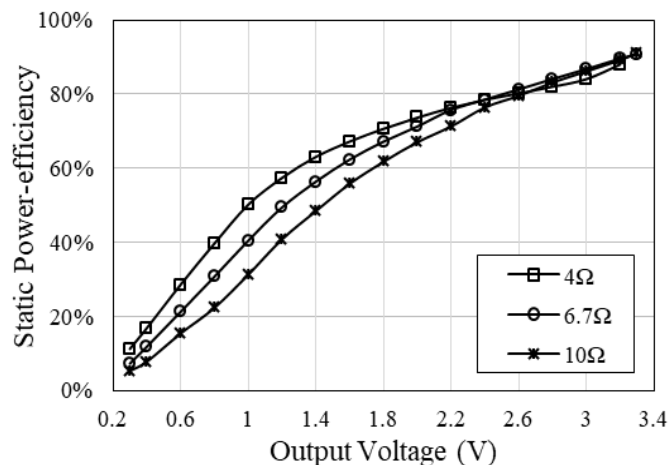
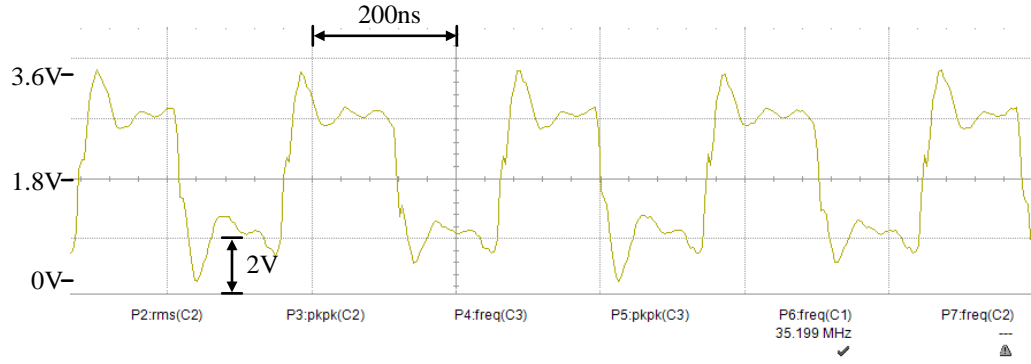
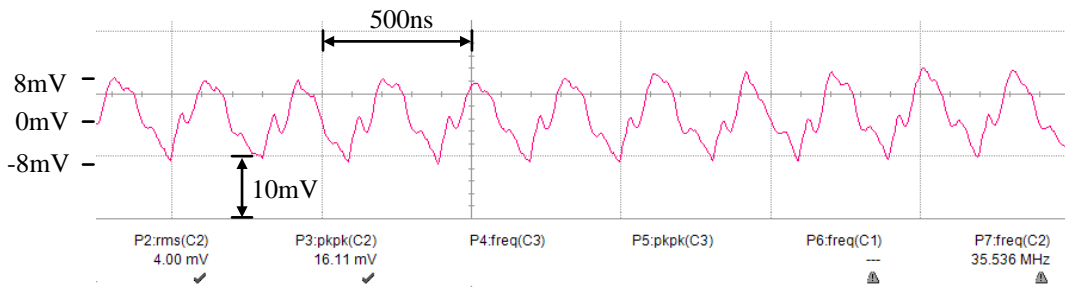


Fig. 4-9: Static power-efficiency

Fig. 4-9 depicts a plot of the measured power-efficiency of the supply modulator when tracking different DC output voltages, i.e., static power-efficiency. Three resistive loads, 4Ω , 6.7Ω and 10Ω , were used. The 4Ω load serves to ascertain the driving capability of the supply modulator, where the supply modulator provides a maximum output power of 2.5W at $v_o = 3.2\text{V}$, with $\sim 88\%$ power-efficiency. With the nominal 6.7Ω load, the output voltage swing ranges from 0.3V to 3.3V , and a peak efficiency of 91% is achieved at $v_o = 3.3\text{V}$, i.e., the output power is 1.63W . These output voltage range and power-efficiency parameters will be benchmarked against the state-of-the-art supply modulators in Table 4-2 later. It can be observed from Fig. 4-9 that the power-efficiency of the supply modulator, as expected, reduces for higher resistive loads at low output voltages. For example, at $v_o = 1.8\text{V}$ ($\sim 5\text{dB}$ backoff), the power-efficiency of the supply modulator for 4Ω , 6.7Ω , 10Ω is 70.6% , 67.2% and 61.7% , respectively. This is because higher power-efficiency is achieved with higher output power due to the largely constant and relatively small quiescent power dissipation.



(a)



(b)

Fig. 4-10: 35MHz measured waveforms (a) switching frequency, and (b) output ripple

Fig. 4-10(a) depicts the output waveform, v_D , of the CDA at the maximum switching frequency of 35MHz, where the propagation delay is ~ 7 ns. As expected, there is ground-bounce noise, i.e., voltage spikes on the otherwise clean supply rails. This is largely due to the switching operation of the CDA and the inductance of the bonding wires. In the prototype supply modulator, the CDA is powered separately from the other analog circuits (including the Class AB amplifier and the hysteresis controller). In the packaging of the prototype supply modulator, multiple power pins and multiple bonding wires were employed to reduce the bonding wire inductance (hence reducing the ground-bounce). Fig. 4-10(b) depicts the output waveform, v_o , of the supply modulator, at

$v_o = \frac{1}{2}V_{DD}$. The ripple noise is $\sim 4\text{mV}_{\text{rms}}$ (i.e., 16mV_{pp}) at 35MHz switching frequency, and this complies with the stipulated spectrum mask of the 20MHz LTE signals; see Fig. 4-14 later. The ripple voltage is relatively small – suppressed by the wideband Class AB amplifier with small output impedance at the switching frequencies (refer to Fig. 4-7(b)) and the $1\mu\text{H}$ external inductor.

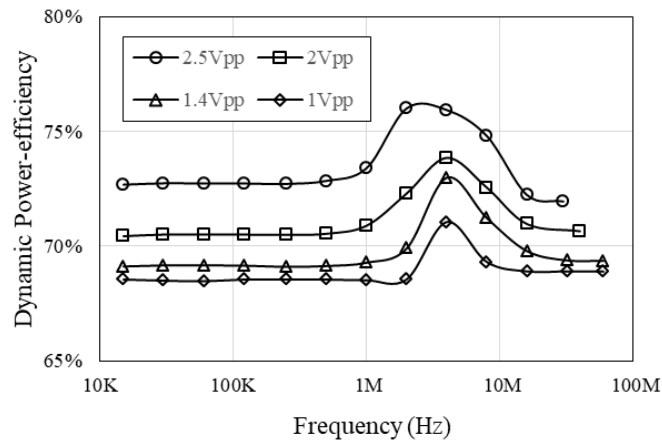


Fig. 4-11: Dynamic power-efficiency

Fig. 4-11 depicts a plot of the measured dynamic power-efficiency of the supply modulator when tracking sinusoidal signals with different frequencies, ranging from 15kHz to 60MHz . Four sinusoidal signals with a DC voltage of 1.8V and with different peak-to-peak values, 1V_{pp} , 1.4V_{pp} , 2V_{pp} , and 2.5V_{pp} , were used. With 1V_{pp} and 1.4V_{pp} , the supply modulator is able to track sinusoidal inputs to $\sim 60\text{MHz}$ (i.e., $\sim 60\text{MHz}$ bandwidth), while at 2V_{pp} and 2.5V_{pp} , the bandwidth of the supply modulator is $\sim 40\text{MHz}$ and $\sim 30\text{MHz}$ respectively. The prototype supply modulator features high dynamic power-efficiency over a wide range of input frequencies, and of particular interest, its power-

efficiency is 68.9% and 71.9% for the 60MHz 1.4V_{pp} and 30MHz 2.5V_{pp} sinusoidal inputs respectively. The power-efficiency is almost constant when tracking low frequency input signals because the switching frequency and the ripple current from the Class AB amplifier are almost constant. When the frequency of the input sinusoidal signal increases from ~1MHz to 2-4MHz, the power-efficiency of the supply modulator increases. This is due to the low switching frequency (equals to the signal frequency), hence low switching losses. Beyond 2-4MHz, the power-efficiency decreases due to the increased output power from the relatively power-inefficient Class AB amplifier.

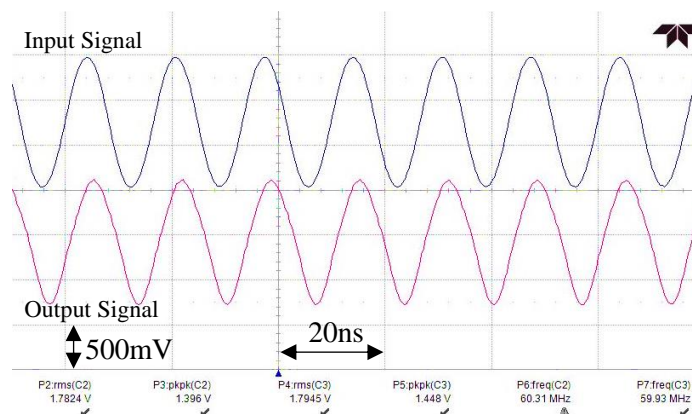


Fig. 4-12: Time domain response of our supply modulator tracking a 60MHz 1.4V_{pp} sinusoidal signal (from 1.1V to 2.5V)

To ascertain the bandwidth of the supply modulator, a 60MHz 1.4V_{pp} sinusoidal signal (from 1.1V to 2.5V) is applied separately to the supply modulator. Fig. 4-12 depicts the ensuing output waveform of the supply modulator where the respective output signal closely tracks the input signal.

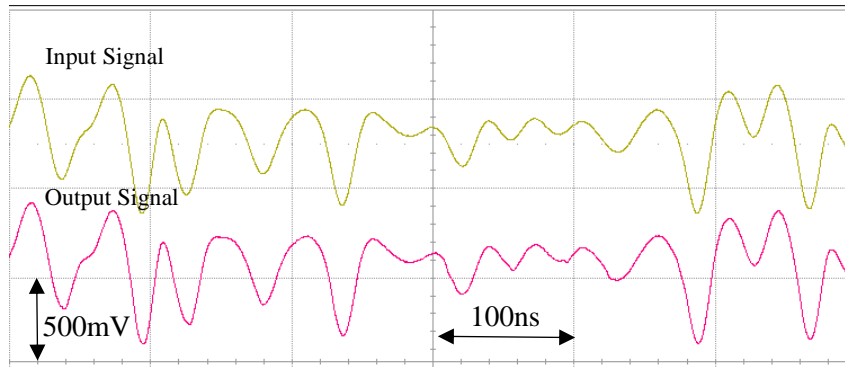


Fig. 4-13: Time domain response of our supply modulator tracking a 40MHz LTE-A envelope signal

The waveforms of the input signal and the time domain response of our supply modulator tracking an envelope signal extracted from a 40MHz LTE-A RF signal is depicted in Fig. 4-13. To the best of our knowledge, there is no commercially available 40MHz LTE-A RF PA for ET PA at this stage. In the measurements, the 6.7Ω resistor is connected as the load to the supply modulator. The 40MHz LTE-A RF signal consists of two component carriers and each component carrier is a 20MHz LTE (100RB, QPSK) RF signal. The supply modulator is able to track the envelope signals closely with relatively high power-efficiency – the measured efficiency of the supply modulator is $\sim 83\%$ for $\sim 1W$ output power.

To ascertain the overall performance of the ET PA embodying the prototype supply modulator and a commercial RF PA, Band VIII 20MHz LTE (100RB, QPSK) RF signals and their extracted envelope signals are applied to the ET PA. Fig. 4-14 depicts the measured output spectrum at 27dBm RF PA output power, which meets the spectrum mask of 20MHz LTE signals.

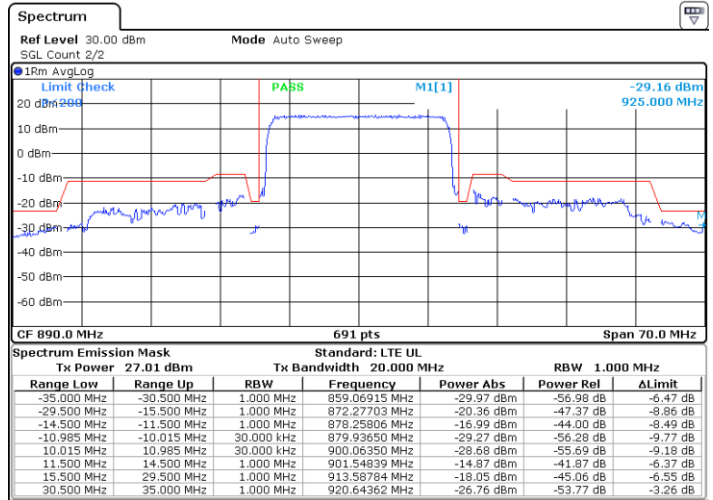


Fig. 4-14: Measured RF PA output spectrum for 20MHz LTE signal at 27dBm RF PA output power

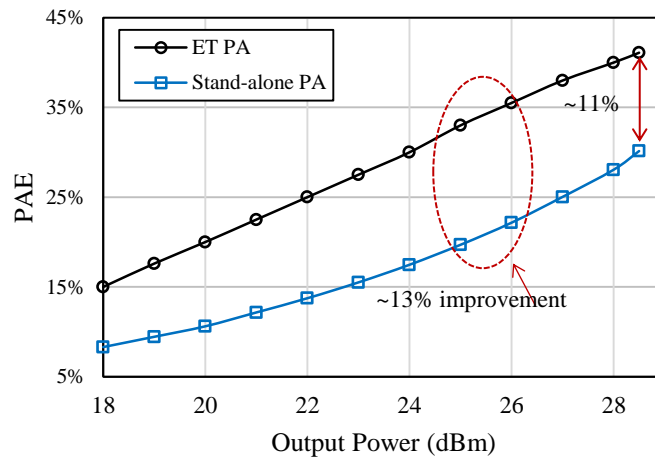


Fig. 4-15: PAE of the ET PA and the stand-alone RF PA

Fig. 4-15 depicts the measured power added efficiency (PAE) of the ET PA and the stand-alone RF PA against the RF PA output power. The measured overall PAE of the ET PA is 41.1% @28.5dBm – a significant 11% power-efficiency improvement compared to the stand-alone PA. Of particular interest, the improved power-efficiency is even more

significant around 3dB backoff where the improvement is ~13% – a significant >1.6x improvement compared to the RF PA without the supply modulator.

The measurements of the prototype supply modulator are consolidated in Table 4-2 and are benchmarked against pertinent state-of-the-art designs [65-69]. For ease of interpretation, an intuitive radar chart is shown in Fig. 4-16, which includes five important parameters: bandwidth, maximum output power, maximum power-efficiency, output voltage swing and 1/ripple noise. The composite figure-of-merit (FOM) encompassing the aforesaid five imperative parameters for the different supply modulators, where each of the said five parameters are equally weighted to a maximum of unity, is given in the parenthesis in the legend. For example for our work, the composite FOM is $\frac{40\text{MHz}}{40\text{MHz}} *$

$$\frac{2.5\text{W}}{2.5\text{W}} * \frac{91\%}{91\%} * \frac{3\text{V}}{3\text{V}} * \frac{1/16\text{mV}}{1/8\text{mV}} = 0.500 .$$

From Table 4-2 and Fig. 4-16, it can be seen that the prototype supply modulator features the highest performance for four imperative parameters – 40MHz bandwidth, 2.5W maximum output power, 91% peak power-efficiency, and 3V output voltage swing. Collectively, on the basis of the aforesaid composite FOM, our proposed supply modulator features an FOM=0.500. This FOM is >20x better than that of the reported supply modulators benchmarked. In short, the proposed supply modulator is highly competitive.

Table 4-2: Benchmark of state-of-the-art supply modulators

Design	This work	[65] JSSC'07	[66] JSSC'09	[67] JSSC'10	[68] JSSC'16	[69] JSSC'17
Bandwidth	40MHz LTE	2MHz EDGE	20MHz WLAN	5MHz WCDMA	-	-
	60MHz 1.4V _{pp} sine wave	160kHz full-wave rectified signal	-	4MHz full-wave rectified signal	10MHz 0.8V _{pp} sine wave	13MHz 0.8V _{pp} sine wave
Maximum output power	2.5W	2.25W	0.186W	2W	0.2W	0.2W
Maximum static power-efficiency	91%	88.3%	87.5%	89%	88.3%	88.2%
Output voltage	3V	2.6V	0.8V	2.4V	0.8V	0.8V
	0.3-3.3V	0.4-3V	0.2-1V	0.4-2.8V	0.2-1V	0.2-1V
Ripple noise	16mV _{pp}	12mV _{pp}	16mV _{pp}	40mV _{pp}	8mV _{pp}	8mV _{pp}
Supply voltage	3.6V	3.5V	1.2V	3.3V	1.2V	1.2V
Process	180nm	350nm	65nm	350nm	130nm	130nm

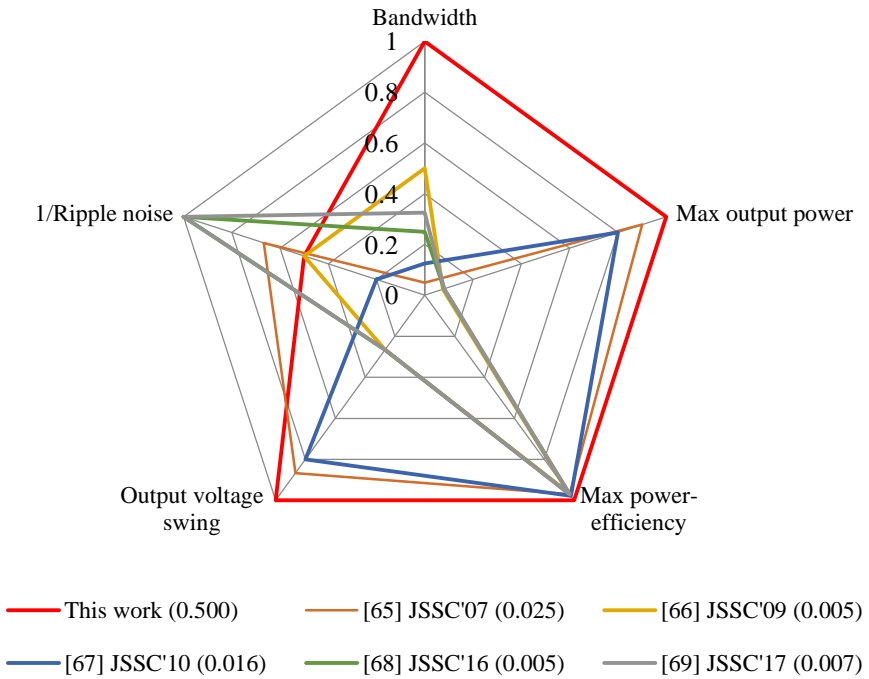


Fig. 4-16: Radar chart benchmarking. The composite FOM encompassing the five benchmarking parameters is shown in the parenthesis, e.g. (0.500) for this work.

4.5 Conclusions

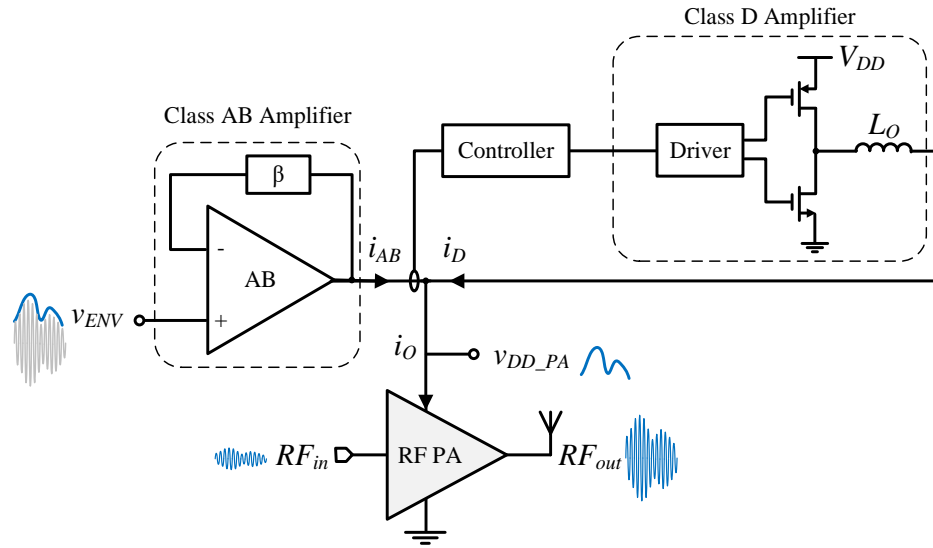
In this chapter, we have described a supply modulator comprising a proposed delay-based hysteresis controller, proposed wideband Class AB amplifier, and CDA for an ET PA. We have shown that to achieve maximum power-efficiency for wideband supply modulators, the hysteresis should be controlled by the propagation delay of the supply modulator – not the threshold current of the hysteresis controller. The prototype supply modulator was shown to be the most competitive design when benchmarked against reported supply modulators – it featured the widest bandwidth, highest output power and highest static power-efficiency, yet with high dynamic power-efficiency, high output swing and low ripple noise at 3.6V supply. The ET PA embodying our supply modulator achieved 41.4% power-efficiency at 28.5dBm peak output power and 34.4% at 3dB backoff – a significant 1.6x improvement over the standard-alone RF PA.

Chapter 5 A 40MHz Dual-mode Sigma-Delta Control Based Supply Modulator for Multi-standard Applications

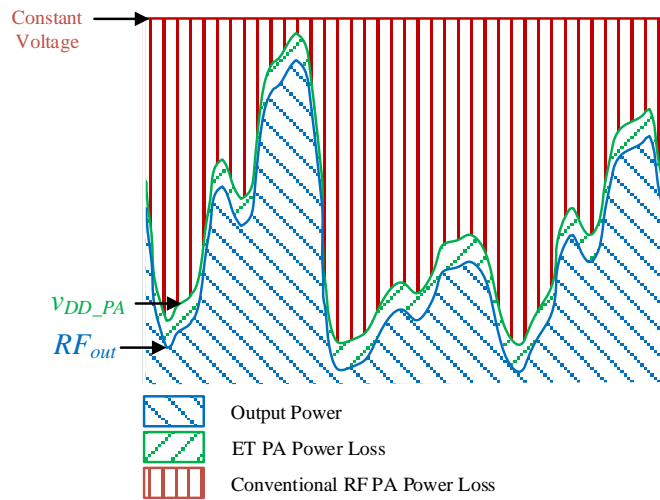
5.1 Introduction

This chapter is largely extracted from our paper [90] in preparation for submission to Journal of Solid-State Circuit.

As delineated in Chapters 1, 2 and 4, the primary complaint of smartphone users is the short battery lifespan of their smartphone. ET PAs, depicted in Fig. 5-1(a), are ubiquitous instead of conventional RF PAs. The supply modulator provides a variable voltage supply, v_{DD_PA} , to the linear RF PA based on the RF output, RF_{out} ; in the case of conventional RF PA, the supply is a constant voltage. Consequently, as desired, the RF PA in the ET PA would nearly always operate in compression, hence featuring higher power-efficiency compared to the conventional RF PA. The operational modality of an ET PA and a conventional RF PA is depicted in Fig. 5-1(b), where the power-efficiency of the ET PA is typically ~20% higher [55, 56].



(a)



(b)

Fig. 5-1: (a) Block diagram of an ET PA comprising a hybrid CDA and a RF PA, and (b) comparison of power dissipation in ET PA and conventional RF PA

Despite the power-efficiency advantage of ET PA as alluded to in Chapter 4, one limitation of state-of-the-art supply modulators is that they are optimized for a single communications standard [58-78, 81], e.g. LTE, or the optimization is compromised when

designed for multiple standards. Put simply, as modern communication devices, including smartphones and tablets, usually embody multiple communication standards where each standard requires different bandwidth, PAPR, output power, etc. (see Table 5-1 later), state-of-the-art supply modulators are often unoptimized or semi-optimized. For instance, Fig. 5-2 depicts the block diagram of a typical RF system embodying a supply modulator. Of specific interest, although multiple RF PAs are embodied in the RF system to support multiple communication standards, only one supply modulator is used. This is largely because of the limited form-factor (IC area) and the high cost.

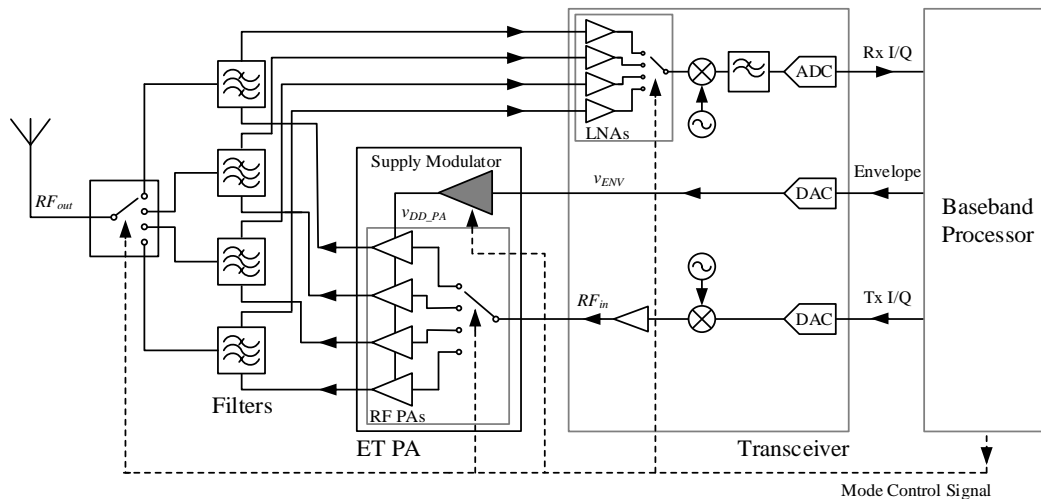


Fig. 5-2: Block diagram of a RF system with an ET PA

Other limitations in state-of-the-art supply modulators include narrow (and insufficient) bandwidth, low power-efficiency, and/or high switching noise (see Table 5-2 later). This is in part due to the tradeoffs between these parameters. For instance, narrow bandwidth and low switching noise usually require high switching frequency which in

turn leads to high switching loss, hence reducing the power-efficiency of the supply modulator.

In this chapter, we will address the aforementioned limitations by our proposal of a supply modulator whose modus operandi is self-adjusted such that it is optimized for multi-standard applications, yet with wide bandwidth, high power-efficiency and low switching noise. The proposed supply modulator employs a hybrid CDA with a novel dual-mode Sigma-Delta control to automatically adjust the operation mode of the supply modulator according to the communication standards. For narrowband applications (see Table 5-1 later), the supply modulator operates in the synchronous Sigma-Delta mode where the switching frequency of the CDA is reduced and controlled by a clock signal – the aim is to reduce the switching frequency when tracking narrowband envelope signals. Conversely, for wideband applications (see Table 5-1 later), the supply modulator operates in the asynchronous Sigma-Delta mode where the hysteresis of the controller is minimized and controlled by a high speed comparator and the inherent delay of the CDA – the purpose here is to reduce the phase lag of the CDA when tracking wideband envelope signals. Collectively, the proposed supply modulator achieves high power-efficiency for both narrowband and wideband applications.

To further improve the power-efficiency without compromising the bandwidth and switching noise, a Class AB amplifier with adaptive bias current is proposed. The bias current and the ensuing quiescent current of the Class AB amplifier are adjusted according to the communication standards and the operation of the supply modulator. During narrowband applications, the required output current of the Class AB amplifier is low and a fixed low quiescent current is used. Conversely, during wideband applications where

the output current of the Class AB amplifier is high, a high and variable quiescent current is used – the quiescent current increases when the output power increases and vice versa.

The prototype supply modulator is designed and monolithically realized in 180nm CMOS process. On the basis of measurements on prototype ICs, the static power-efficiency of our proposed supply modulator features up to a significant 6% improvement and peak efficiency of ~91%. For tracking 40MHz LTE-A envelope signals, the prototype supply modulator achieves 85% efficiency at 1.8W output power and remains >80% over a wide range of output power, from 0.5W to 1.8W.

This chapter is organized as follows. In Section 5.2, the design challenges of supply modulator for multi-standard applications are delineated. Section 5.3 presents the operation principle and the design of the proposed supply modulator. Section 5.4 presents the measurement results followed by conclusions in Section 5.5.

5.2 Design Challenges for Multi-standard Applications

In this section, the operation of a conventional supply modulator is first delineated, followed by the design challenges towards the supply modulator for multi-standard applications. The analysis here serves as a preamble for our subsequent proposed design.

As shown in Fig. 5-1(a) and described in Chapters 2 and 4, a conventional supply modulator comprises a hybrid CDA embodying a linear Class AB amplifier, a high-efficiency CDA and a controller which controls the switching of the CDA. According to input signal and the amount of current provided by the CDA and Class AB amplifiers, the

operation of the supply modulator can be divided into two cases, which will now be delineated in detail.

Case 1: Low input frequency (narrowband application)

In this case, the average slew rate, SRi_O , of the output signal is less than the slew rate, SRi_D , of the CDA (i.e., $SRi_O < SRi_D$), such that the CDA is able to track the output signal closely. The switching frequency of the CDA, $f_{sw(nb)}$, expressed in eqn. (5.1) [66], is much higher than the input frequency, f_{in} .

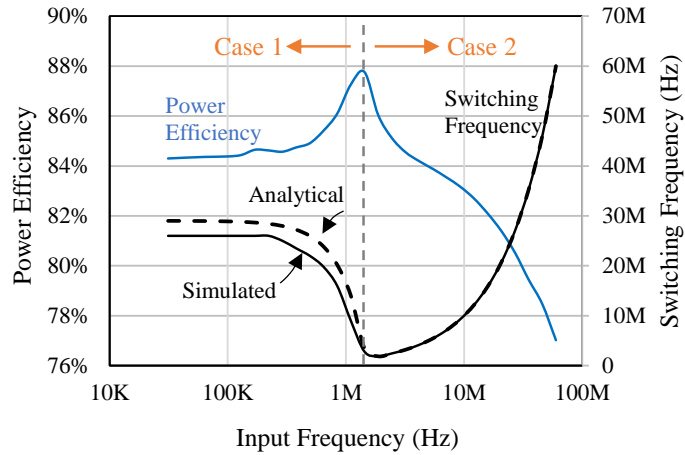
$$f_{sw(nb)} = \frac{V_{DD}}{4I_{HYS}L_O} \left[1 - \left(\frac{L_O \times SRi_O + v_{DD-PA} - \frac{1}{2}V_{DD}}{\frac{1}{2}V_{DD}} \right)^2 \right] \quad (5.1)$$

where V_{DD} is the supply voltage, I_{HYS} is the current hysteresis of the supply modulator, and L_O is the output inductor in Fig. 5-1(a).

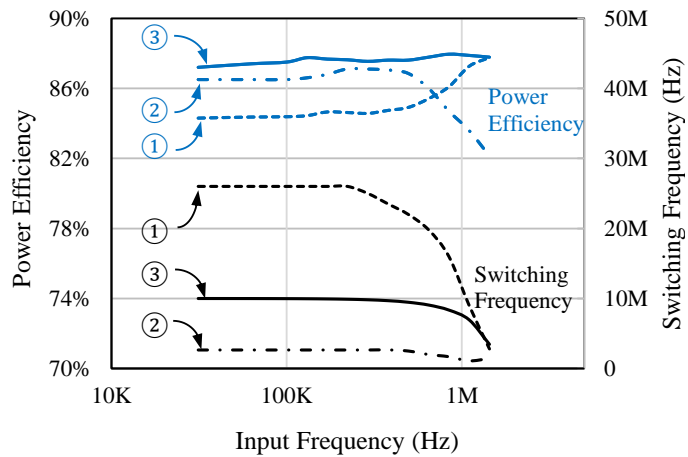
Fig. 5-3(a) depicts the average switching frequency and power-efficiency at various input frequencies f_{in} (with $1.8V_{DC}$ and $0.5V_{pp}$). For sake of completeness, the switching frequency and the power-efficiency for Case 2 are also depicted.

It can be seen that the switching frequency based on eqn. (5.1) is similar to that obtained from simulations. From eqn. (5.1), it can be observed that the switching frequency is affected by both the design parameters of the supply modulator (in this case, $I_{HYS}=6mA$, $V_{DD}=3.6V$, and $L_O=4.7\mu H$), and the slew rate of the signal, SRi_O . When SRi_O is low, the switching frequency is nearly constant, and reduces when SRi_O increases.

When SRi_O increase further, the CDA is unable to track the output signal, and this leads to the Case 2 of the CDA (i.e., $SRi_O > SRi_D$); see later.



(a)



(b)

Fig. 5-3: (a) Switching frequency and power-efficiency with various input frequency, and (b) simulated power-efficiency at three different switching frequencies

The optimum switching frequency, $f_{sw_op(nb)}$, for maximum power-efficiency can be derived as eqn. (5.2); refer to Appendix for the detailed derivations.

$$f_{sw_op(nb)} = \sqrt{\frac{1 - \left(\frac{L_O \times SRi_O + v_{DD_PA} - \frac{1}{2}V_{DD}}{\frac{1}{2}V_{DD}} \right)^2}{16C_{eq}L_O}} \quad (5.2)$$

where C_{eq} is the parasitic capacitance of the drivers and power transistors in the CDA.

To verify eqn. (5.2), Fig. 5-3(b) depicts the simulated power-efficiency at three different switching frequencies. The switching frequencies for line ① and line ② are simulated with fixed I_{HYS} ($I_{HYS}=6mA$ and $50mA$, respectively); and at low frequencies ($f_{in}<500kHz$), the switching frequency is $\sim 25MHz$ for line ① and $\sim 4MHz$ for line ②. The line ③ is the optimum switching frequency derived from eqn. (5.2), which is $\sim 10MHz$ at $f_{in}<500kHz$ and drops to $\sim 4MHz$ at $f_{in}=1.5MHz$.

The power-efficiency is at its maximum when the switching frequency is designed at the optimum switching frequency – the power-efficiency is reduced when the switching frequency is below or above the optimum switching frequency. This is mainly due to the trade-off between the switching loss of the CDA and the power dissipation in the Class AB amplifier. In other words, the power dissipation in Class AB amplifier increases with the decrease of the switching frequency (i.e., the decrease of the switching loss). This is because the output current of the Class AB amplifier, i_{AB} , is bounded by the hysteresis current, I_{HYS} , of the controller (i.e., the peak-to-peak current $i_{AB(pp)}$ equals to I_{HYS}) to cancel the ripple current due to the switching of the CDA, and there is a trade-off between I_{HYS} and $f_{sw(nb)}$ as expressed in eqn. (5.1). Taking both power dissipation mechanisms into

consideration, the maximum power-efficiency is achieved at $f_{sw_op(nb)}$ expressed in eqn. (5.2).

It can be seen from eqn. (5.2) that the optimum switching frequency depends on the slew rate of the signal, SRi_O . In other words, the optimum switching frequencies for different communication standards are different. However, as conventional designs [66, 68, 71, 73-76, 78] embody a fixed I_{HYS} , for instance line ① and line ② in Fig. 5-3(b), optimized power-efficiency can only be achieved for a specific input signal and is hence unoptimized for other input signals.

Case 2: High input frequency (wideband application)

When the input frequency is high (i.e., for wideband applications), the slew rate of the output signal exceeds the slew rate of the CDA (i.e., $SRi_O > SRi_D$). In this case, the DC component of the output signal is provided by the CDA whilst the AC component is collectively provided by the CDA and the Class AB amplifier – this is different from Case 1 earlier. The switching frequency, $f_{sw(wb)}$, of the CDA only depends on the input signals, and it is independent of the hysteresis I_{HYS} . This can be analytically verified from Fig. 5-3(a).

Fig. 5-4 illustrates the peak-to-peak current in the Class AB amplifier, $i_{AB(pp)}$, and the power-efficiency with various hysteresis current I_{HYS} . In this figure, the input frequency is 2.5MHz (with $1.8V_{DC}$ and $0.5V_{pp}$). It can be seen that when the hysteresis current I_{HYS} increases, the current burden of the Class AB amplifier increases and the

power-efficiency of the supply modulator is reduced. This is because, in this case, the hysteresis results in a phase lag (delay) in the CDA. The phase lag in the CDA subsequently results in a current flow between the Class AB amplifier and the CDA - this is to compensate for the distortion in the output signal due to the phase lag in the CDA. Consequently, the output current in the Class AB amplifier increases, thereby decreasing the overall power-efficiency of the supply modulator. Put simply, to improve the power-efficiency, the hysteresis of the supply modulator should be low in Case 2.

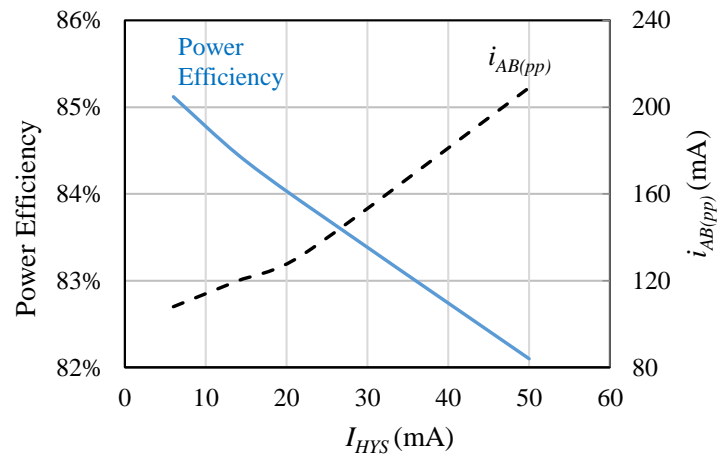


Fig. 5-4: Power-efficiency and $i_{AB(pp)}$ with various I_{HYS}

Design challenges for multi-standard operation

As explained earlier, in conventional designs [66, 68, 71, 73-76, 78] where the hysteresis, I_{HYS} , of the supply modulator is fixed, I_{HYS} and $f_{sw(nb)}$ can only be optimized for single standard application. Undoubtedly, there are challenges to design a supply modulator optimized for multi-standard applications. Consider the following.

For narrowband applications, the switching frequency should be designed at its optimum switching frequency (eqn. (5.2)) and it is application dependent. Conversely, for wideband applications, the inherent delay and the hysteresis should be as small as possible – this somewhat contradicts the requirements for the narrowband applications as small inherent delay and hysteresis translates to high switching frequency in narrowband applications, translating to high switching losses. As a case in point, with $I_{HYS}=6\text{mA}$ (the minimum hysteresis due to the inherent delay in our design; see Fig.5-5 later), the supply modulator achieves the highest power-efficiency for wideband applications (refer to Fig. 5-4). However, its power-efficiency would be compromised in narrowband applications due to its excessively high switching frequency (refer to line ① in Fig. 5-3(b)). Put simply, to achieve a high power-efficiency for multi-standard applications, the controller of the supply modulator should be designed differently for each application. We will now explain how this is addressed in our proposed design.

5.3 Proposed Supply Modulator for Multi-standard Applications

To address the abovementioned design challenges for multi-standard applications, we propose a supply modulator (Fig. 5-5) with a dual-mode Sigma-Delta control and an adaptive biasing Class AB amplifier. The proposed control method enables two operation modes – the synchronous Sigma-Delta mode for narrowband applications and the asynchronous Sigma-Delta mode for wideband applications. The proposed Class AB amplifier adjusts the bias current (hence the ensuing quiescent current) according to the applications to minimize the quiescent power dissipation of the Class AB amplifier. The

operations are controlled by the ‘Mode Control Signal’ from the baseband processor in Fig. 5-2. The design and operation of the proposed supply modulator (see Table 5-1 later) will now be delineated.

5.3.1 System Architecture

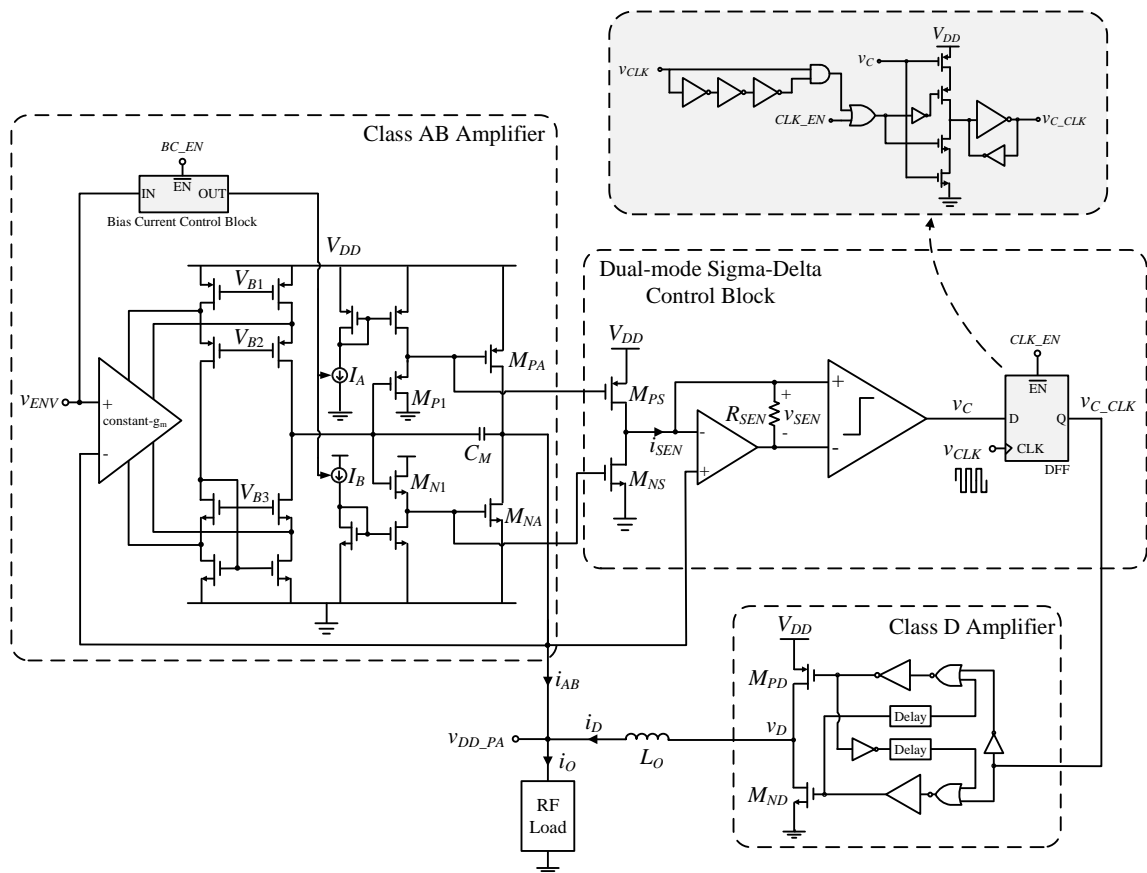


Fig. 5-5: Schematic of the proposed supply modulator with dual-mode Delta-Sigma Control

The schematic diagram of the proposed supply modulator, depicted in Fig. 5-5, embodies a proposed dual-mode Sigma-Delta control, a proposed Class AB amplifier with

adaptive bias current, and a high-efficiency CDA including an anti-shoot-through driver and an output inductor L_O .

5.3.2 Proposed dual-mode Sigma-Delta Control

For narrowband applications, DFF is enabled (i.e., $CLK_EN=0$) and the supply modulator operates as synchronous Sigma-Delta control. In this mode, the DFF samples the comparator output, v_C , at the rising edge of the clock signal v_{CLK} , and the output, v_{C_CLK} , of the DFF is a pulse density modulated signal. The quantization noise of the CDA arising from the finite clock rate is primarily attenuated by the Class AB amplifier in parallel. To obtain high power-efficiency over a wide range of communication standards, the clock rate/sampling frequency f_{CLK} is selected according to the bandwidth of the communications standard. This is to achieve optimized switching frequency (eqn. (5.2)); see Table 5-1 later. For instance, with $f_{CLK}=20\text{MHz}$, the switching frequency for tracking low-frequency signals (such as GSM EDGE) is $\sim 10\text{MHz}$. Compared to the conventional hysteresis control, the synchronous Sigma-Delta control achieves a higher power-efficiency for multi-standard applications without compromising the hardware simplicity.

For wideband applications, the supply modulator operates with the asynchronous Sigma-Delta control by disabling DFF (i.e., $CLK_EN=1$), and v_{C_CLK} follows v_C . Instead of the hysteresis comparator in the conventional hysteresis control [66, 68, 71, 73-76, 78], the proposed control block embodies a simple voltage comparator without hysteresis. This is because, as mentioned earlier, the hysteresis will undesirably generate delay/phase lag in the CDA for wideband applications, thereby decreasing the power-efficiency. In

our design, the hysteresis is minimal, which depends only on the inherent delay of the supply modulator.

Table 5-1: Operation for various wireless mobile telecommunication standards

Standards		BW (Hz)	Uplink Modulation	PAPR (dB)	Max Output Power * (dBm)	Mode Control Signal			Control Mode	I_Q (mA)
						CLK_EN	f_{CLK} (Hz)	BC_EN		
Narrow-band	GSM EDGE	384k	8-PSK	3.2	22	0	20M	1	Syn. Sigma-Delta	8.2
	CDMA 2000-1X	1.25M	BPSK/QPSK / 8-PSK	3.5-7	30	0	20M	1		
	LTE	1.4M	QPSK/16QAM/64QAM	6-9	23	0	20M	1		
	UMTS WCDMA	3.84M	QPSK	3.5	24	0	30M	1		
Wide-band	LTE	5M/10M /15M/20 M	QPSK/16QAM/64QAM	6-9	23	1	-	0	Asyn. Sigma-Delta	8.2-28.2
	LTE-A	40M	QPSK/16QAM/64QAM	6-9	23	1	-	0		

*UE Maximum Output Power for power Class 3

To illustrate the operation of our proposed supply modulator, two envelope signals extracted from 20MHz and 1.4MHz LTE standards are applied. The former is to illustrate the wideband application and the latter is to illustrate the narrowband application. The probability density function (PDF) and power spectral density (PSD) of the envelope signals are respectively depicted in Figs. 5-6(a) and (b). The two envelope signals have a similar PDF, and the power in both cases are primarily within the DC to 10kHz frequency range.

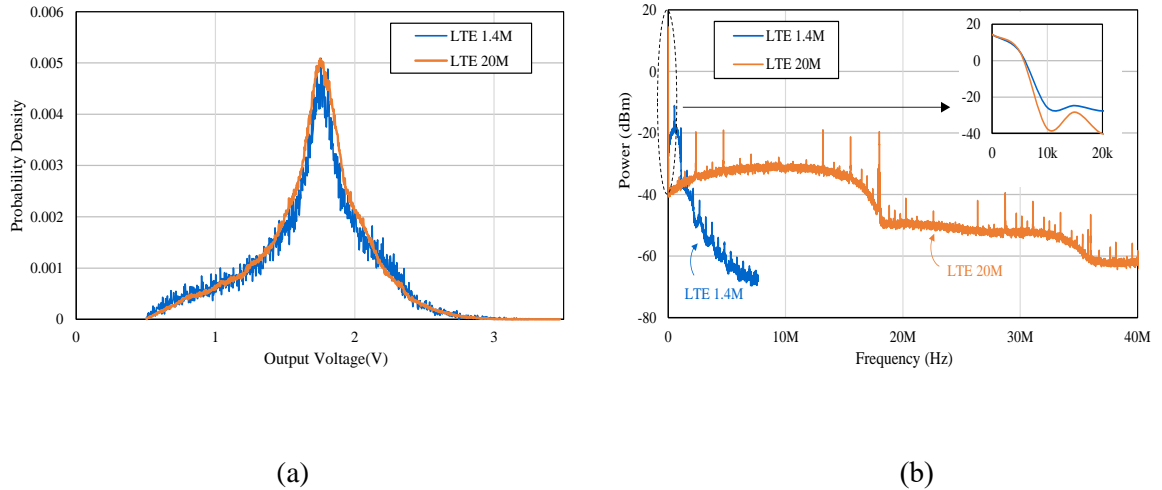
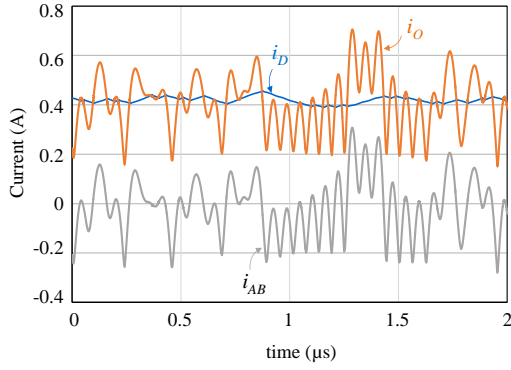
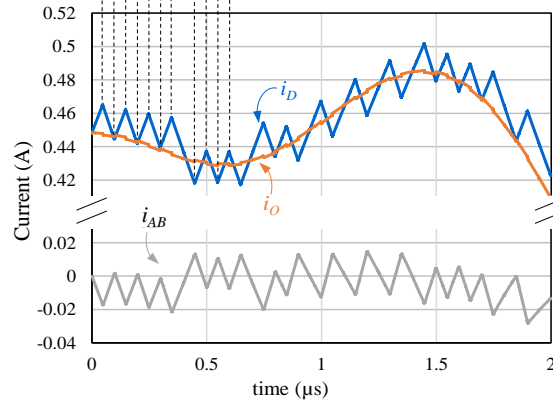
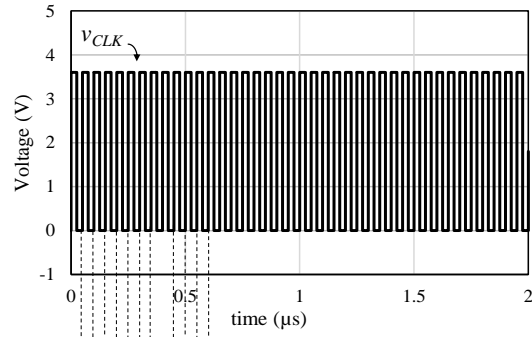


Fig. 5-6: (a) PDF and (b) PSD of the envelop signals extracted from 1.4MHz LTE and 20MHz LTE signals

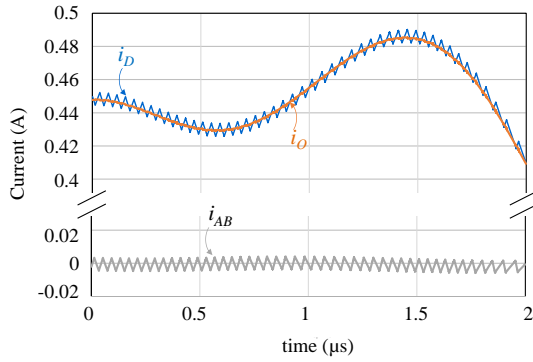
The current waveforms for tracking 20MHz LTE envelope signals are shown in Fig. 5-7(a). In this case, the supply modulator operates in the wideband mode, i.e., DFF is disabled and the asynchronous Sigma-Delta control is employed. It can be seen from Fig. 5-7(a) that the switching frequency is largely the same as the input (output) frequency. Fig. 5-7(b) depicts the waveform of the supply modulator when tracking a narrowband signal of a 1.4MHz LTE envelope signal. To illustrate the efficacy of the synchronous Sigma-Delta control (DFF enabled), Fig. 5-7(c) further depicts the waveforms by using asynchronous Sigma-Delta control (DFF disabled). It can be seen that by using the synchronous Sigma-Delta control, the switching frequency of the supply modulator is significantly reduced, from a high ~ 25 MHz (Fig. 5-7(c)) to a low ~ 8 MHz (Fig. 5-7(b)), translating to an improved power-efficiency from 79% to 82%.



(a)



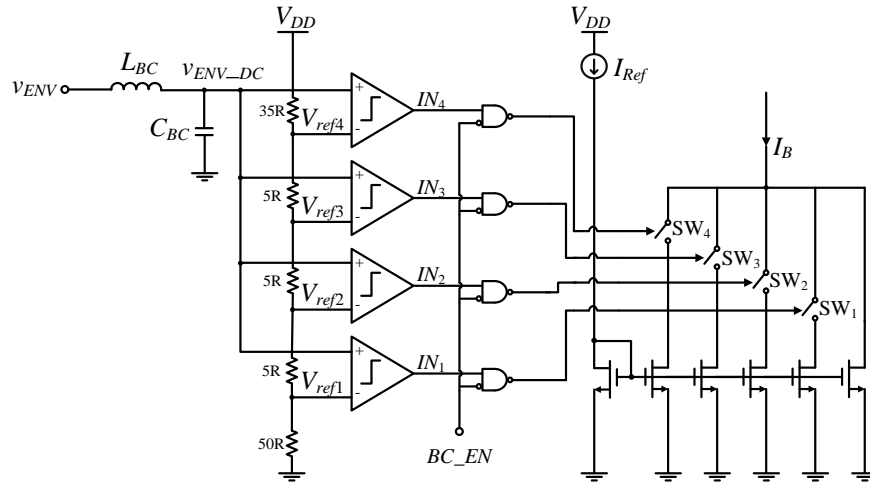
(b)



(c)

Fig. 5-7: Current waveforms of the supply modulator tracking: (a) 20MHz LTE envelope signal with asynchronous Sigma-Delta control, (b) 1.4MHz LTE envelope signals with synchronous Sigma-Delta control ($f_{CLK}=20\text{MHz}$), and (c) 1.4MHz LTE envelope signals with asynchronous Sigma-Delta control

5.3.3 Proposed Class AB Amplifier



V_{ENV_DC}	BC_EN	SW1	SW2	SW3	SW4	I_B	I_Q
X	1	ON	ON	ON	ON	500 μ A	8.2mA
$<V_{ref1}$	0	ON	ON	ON	ON	500 μ A	8.2mA
$>V_{ref1}$ and $<V_{ref2}$	0	OFF	ON	ON	ON	400 μ A	10.5mA
$>V_{ref2}$ and $<V_{ref3}$	0	OFF	OFF	ON	ON	300 μ A	14.0mA
$>V_{ref3}$ and $<V_{ref4}$	0	OFF	OFF	OFF	ON	200 μ A	19.3mA
$>V_{ref4}$	0	OFF	OFF	OFF	OFF	100 μ A	28.2mA

Fig. 5-8: Schematic of the bias current control block of the proposed Class AB amplifier

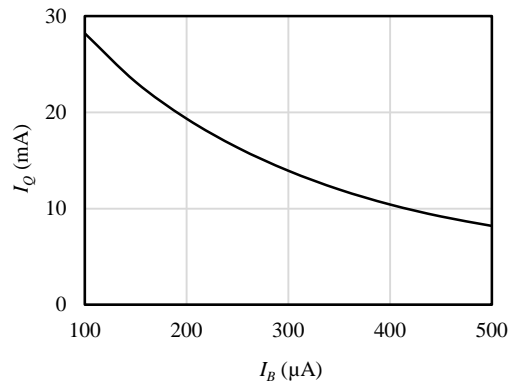
To further improve the power-efficiency of the supply modulator over a wide range of communication standards with various output-power levels, a Class AB amplifier with adaptive bias current is proposed. The block diagram of the bias current control block is depicted in Fig. 5-8. The modus operandi of the control block is the adjustment of the bias current according to the bandwidth and the output power of the output signal. In this manner, the quiescent current of Class AB amplifier, I_Q , is varied according to the

input signals, thereby providing sufficient driving capability yet with minimal quiescent power loss.

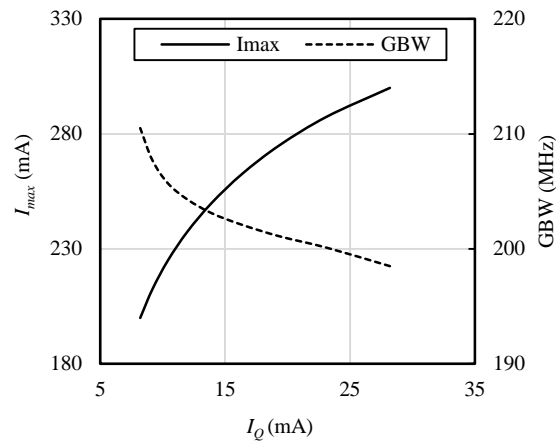
In narrowband applications (see Table 5-1), the bias current control block is disabled (i.e., $BC_EN=1$) and I_Q is fixed to be 8.2mA. This is because in narrowband applications, the Class AB amplifier serves to only provide ripple current and the amount of ripple current needed is usually small. Conversely, in wideband applications, the current required from the Class AB amplifier is higher and largely proportional to the output power of the supply modulator. This is because the Class AB amplifier needs to provide both the ripple current and the AC component of the output signal. In this case, the bias current control block is enabled (i.e., $BC_EN=0$) and the quiescent current of the Class AB amplifier should be high and adjustable based on the output power of the output signal. In our design, I_Q is determined by the comparison between the DC voltage of the output signal, v_{ENV_DC} , and the reference voltages, V_{ref1} , V_{ref2} , V_{ref3} , and V_{ref4} , as shown in Fig. 5-8. I_Q ranges from 8.2mA to 28.2mA to meet the various communication standards.

The block diagram of the proposed three-stage Class AB amplifier is depicted in Fig. 5-5 (top left). In our design, the bias current for the first stage is separated from the middle stage. By controlling the bias current in the middle stage, i.e., I_A , I_B , V_{GS} of the floating voltage source, M_{P1} , M_{N1} , can be adjusted. If I_A and I_B increase, V_{GS} of M_{P1} , M_{N1} are increased, hence the ensuing quiescent current for M_{PA} and M_{NA} is reduced. In this manner, the quiescent current for the power transistors can be adaptively controlled. Since the size of the PMOS transistors is designed to be ~2x the size of the NMOS transistors to maintain the same rising time and falling time, the bias current I_A for PMOS is designed to be 2x the bias current of I_B for NMOS transistors. Fig. 5-9(a) depicts I_Q

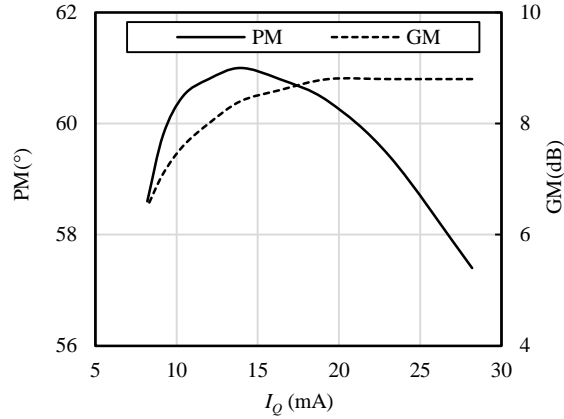
with various biasing condition I_B . By increasing the bias current I_B from 100μ to 500μ , the quiescent current is reduced by $\sim 3.5x$ – from 28.2mA to 8.2mA . The maximum output current, I_{max} , and gain-bandwidth product (GBW) of the Class AB amplifier with various quiescent current, I_Q , are summarized in Fig. 5-9(b). The phase margin (PM) and gain margin (GM) are depicts in Fig. 5-9(c) to illustrate the stability. It can be seen that the Class AB amplifier maintains wide bandwidth ($\sim 200\text{MHz}$) and good stability over the whole quiescent current range. With $I_Q=28.2\text{mA}$, the Class AB amplifier can drive up to $\sim 300\text{mA}$.



(a)



(b)



(c)

Fig. 5-9: Simulated results of (a) I_Q with biasing condition I_B , (b) I_{max} and GBW with various I_Q , and (c) PM and GM with various I_Q

5.3.4 Class D Amplifier

The schematic of the CDA is shown in Fig. 5-5 (right bottom). The output power transistors, M_{PD} and M_{ND} , therein adopt a standard CMOS inverter topology. M_{PD} and M_{ND} are designed to feature a low switching loss and conduction loss [35] to achieve high power-efficiency. To prevent large shoot-through current, an anti-shoot-through driver is included in the CDA [71, 73, 84], which contributes ~ 4 ns dead time. The output inductor, L_O , affects the slew rate, SR_{iD} , of the CDA, and determines the transition frequency between the two cases (refer to Fig. 5-3(a)). A small L_O increases SR_{iD} , but at the cost of the increased switching noise. Moreover, the parasitic resistance of L_O contributes the power loss from the inductor where the inductor with higher inductance usually has larger (worse) parasitic resistance. Considering the abovementioned tradeoffs, an inductor value of $4.7\mu\text{H}$ is judiciously selected to optimize the performance of the supply modulator.

5.4 Measurement Results

Fig. 5-10 depicts the die micrograph of the prototype supply modulator fabricated using 180nm CMOS process. The total area of the prototype IC is 2.25mm^2 and it is packaged in a $4\text{mm}\times 4\text{mm}$ QFN package. The output inductor L_O is $4.7\mu\text{H}$ and decoupling capacitance at the output of the supply modulator is 100pF . The supply voltage is $V_{DD}=3.6\text{V}$. A resistive load of 4Ω is used for measurements – this is a typical load used to qualify and quantify the performance of a supply modulator. The clock frequency for the synchronous Sigma-Delta mode is 20MHz unless otherwise stated.

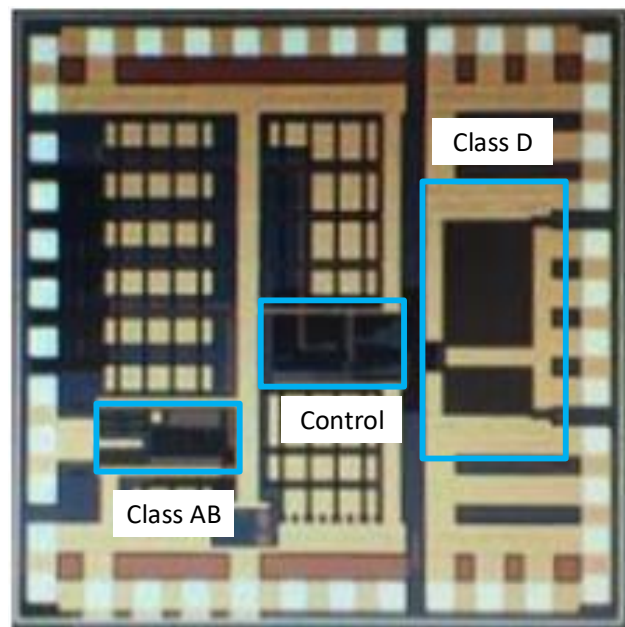


Fig. 5-10: Die Photo

Figs. 5-11(a) and 11(b) respectively depict the output waveforms, v_D , of the CDA for wideband application (asynchronous Sigma-Delta mode) and for narrowband application (synchronous Sigma-Delta mode). The input for both cases is a DC input and

$v_{ENV}=1.8V$ (0.8W output power). For wideband applications (Fig. 5-11(a)), the DFF is disabled and the switching frequency is a high 25MHz – this is the maximum switching frequency of our supply modulator. For narrowband applications, (Fig. 5-11(b)), the DFF is enabled and the switching frequency depends on the clock frequency. In this case the switching frequency is 10MHz ($f_{CLK}=20MHz$).

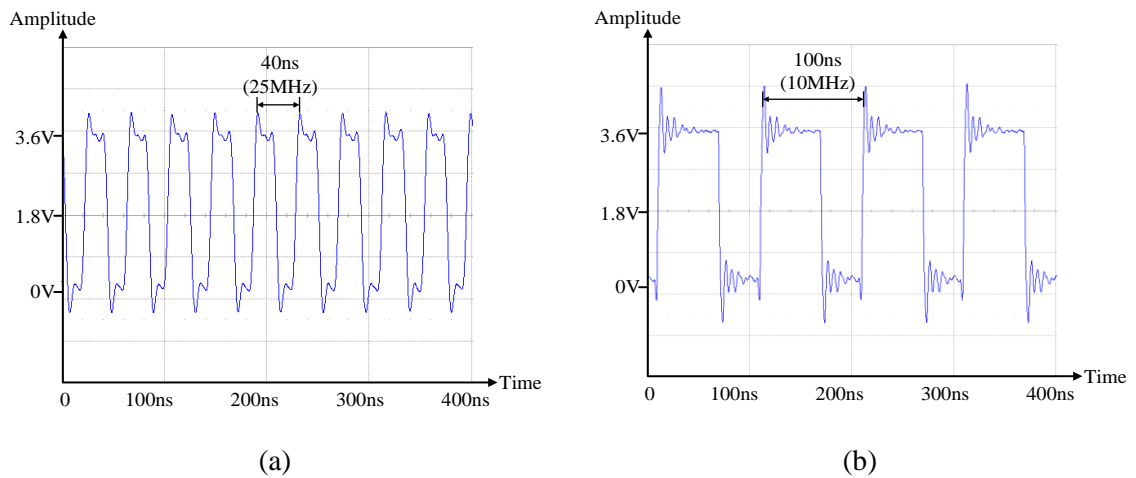


Fig. 5-11: Output waveform of the CDA at $v_{DD_PA}=1.8V$ with (a) asynchronous mode, and (b) synchronous mode

Figs. 5-12(a) and (b) depict the average switching frequency and the static power-efficiency of the supply modulator for narrowband and wideband applications. It can be seen that the switching frequency for narrowband applications is 4x lower – translating to a worthy ~6% improvement in power-efficiency (Fig. 5-12(b)). Further, for both narrowband and wideband applications, the switching frequency is maximum at output power of 0.8W (i.e., $v_{DD_PA}=1.8V$), and reduces when output power increases or reduces. This is similar to the case of Sigma-Delta converters and Sigma-Delta CDAs whose

switching frequency is maximal when the output is at half V_{DD} (or AC ground). Fig. 5-13 shows the measured switching noise for $v_{DD_PA}=1.8V$. The switching noise is $\sim 18mV_{pp}$, which equals to $\sim 5mV_{rms}$. The power-efficiency and switching noise will be benchmarked against the state-of-the-art supply modulators in Table 5-2 later.

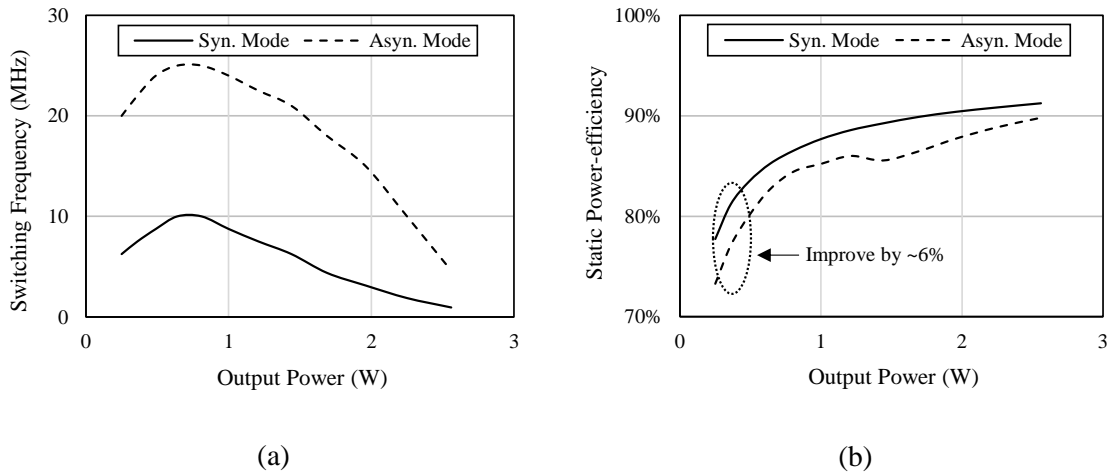


Fig. 5-12: The measurement of (a) the switching frequency, and (b) the static power-efficiency of the supply modulator with asynchronous and synchronous mode

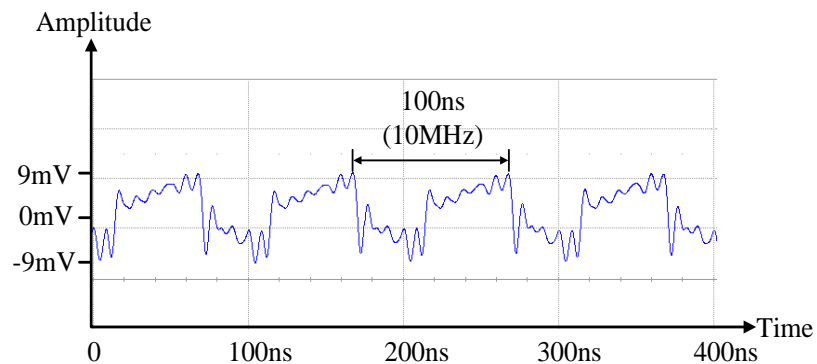
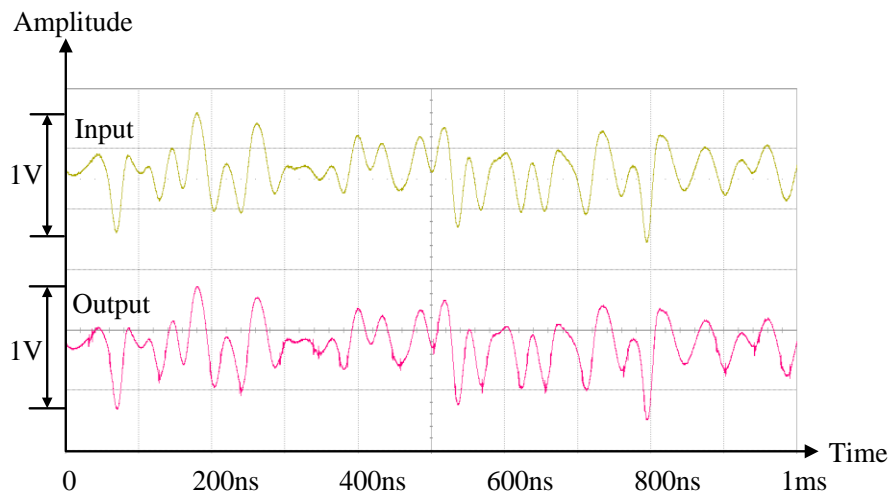
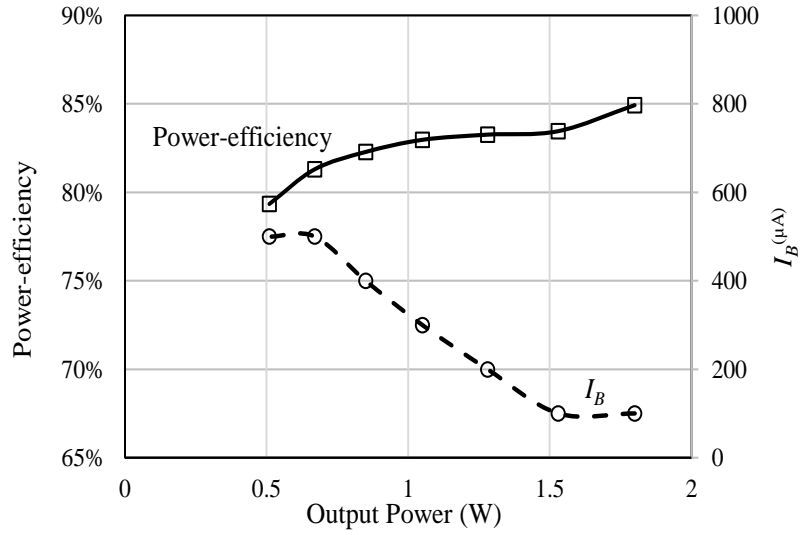


Fig. 5-13: Measured waveform of the ripple noise of the supply modulator at $v_{DD_PA}=1.8V$ with synchronous mode ($f_{CLK}=20MHz$)

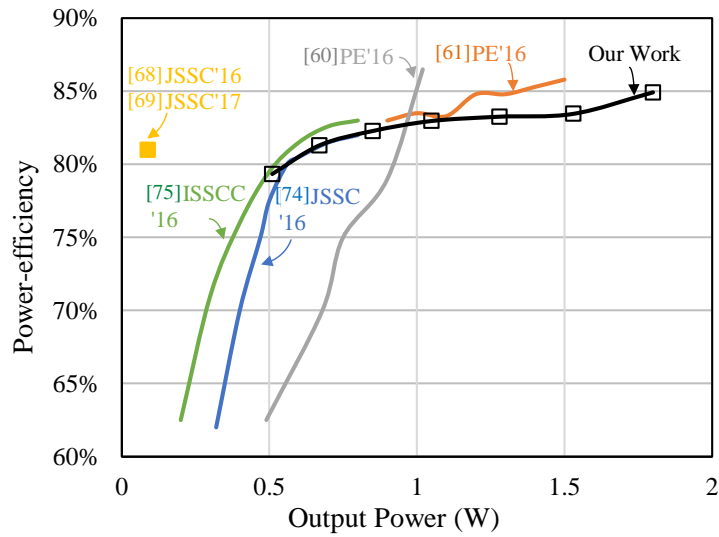
Figs. 5-14(a) and (b) illustrate the performance of the supply modulator for 40MHz LTE envelope signals. Fig. 5-14(a) depicts the waveforms of the input signals, and the time domain response of our supply modulator tracking the extracted envelope signals from 40MHz LTE RF signals ($\sim 2.6V_{\text{rms}}$ and $\sim 1V_{\text{pp}}$). The supply modulator is able to follow the envelope signals very closely. Fig. 5-14(b) depicts the power-efficiency of the supply modulator tracking the 40MHz LTE with various output-power levels. The proposed supply modulator can provide a maximum power of 1.8W with a maximum efficiency of 85% (I_B is 100 μA for maximal quiescent current). By automatically adjusting the quiescent current of the Class AB amplifier according to the output power of the envelope signals (see Fig. 5-8), the power-efficiency remains $>80\%$ for a wide range of output power, from 0.5W to 1.8W. Fig. 5-14(c) compares the dynamic efficiency of the proposed supply modulator against the state-of-the-art designs [60, 61, 68, 69, 74, 75]. The proposed supply modulator improves the dynamic power-efficiency broadly and is capable of supplying the maximum output power of 1.8W.



(a)



(b)



(c)

Fig. 5-14: Measured results of the (a) transient response of the supply modulator of tracking a 40MHz LTE envelope signal (b) power-efficiency of the supply modulator tracking the 40MHz LTE with various output power (c) its comparison with state-of-the-art designs

The measurements of the prototype supply modulator are consolidated in Table 5-2 and are benchmarked against pertinent state-of-the-art designs. From Table 5-2, it can be seen that the prototype supply modulator features the highest output power (2.5W), highest static power-efficiency (91%) and highest bandwidth (40MHz) of all benchmarked supply modulators. Its features high dynamic power-efficiency (85%) and low switching noise (18mV_{pp}). Of specific interest, the prototype supply modulator also features high back-off power-efficiency as observed in Fig. 5-14(c). In short, the performance of the proposed supply modulator is highly competitive.

Table 5-2: Benchmark of state-of-the-art SMs

Design	This work	[61] PE'16	[60] PE'16	[68] JSSC'16	[74] JSSC'16	[69] JSSC'17	[75] ISSCC'16
Control	Dual-mode Sigma-Delta	SAVT	SIDO	SCCI	Hysteresis with AC- coupling	Ripple- current-based PWM	Hysteresis with AC- coupling
Topology	Hybrid	CDA	CDA	Hybrid	Hybrid	Hybrid	Hybrid
Signal tracked	40MHz LTE-A	10MHz LTE	10MHz LTE	10MHz 0.8V _{pp} sine wave	10MHz LTE	13MHz 0.8V _{pp} sine wave	40MHz LTE-A
Max output power	2.5W	2W	-	0.2W	-	0.2W	-
Max static power- efficiency	91%	87%	-	88%	-	88%	-
Max dynamic power- efficiency	85%	86%	87%	81%	82%	81%	83%
Switching noise	18mV _{pp}	-	-	8mV _{pp}	-137dBm/Hz	8mV _{pp}	-136dBm/Hz
Supply voltage	3.6V	3.3V	3.3V	1.2V	4V	1.2V	4V
Process	180nm	180nm	180nm	130nm	130nm	130nm	130nm

5.5 Conclusions

We have described a supply modulator with proposed dual-mode Sigma-Delta control for multi-standard applications. By embodying a simple comparator without adding hysteresis for wideband applications, regulating the switching frequency of the CDA for narrowband applications, and self-adjusting the quiescent current of the Class AB amplifier according to the characteristics of the envelope signals. We have shown that the power-efficiency of the supply modulator was improved for a wide range of applications with different output-power levels. The prototype supply modulator was shown to be a competitive design when benchmarked against reported supply modulators.

Appendix

The power dissipation, P_{loss} , of the supply modulator in Case 1 can be separated as two parts – power loss, P_{loss_D} , from the CDA and power loss, P_{loss_AB} , from the Class AB amplifier. P_{loss_D} , expressed in eqn. (5.A1), consists of the switching loss and conduction loss, due to the parasitic capacitance (C_{eq}) and the parasitic resistance (R_{eq}) of the drivers and power transistors. P_{loss_AB} , expressed in eqn. (5.A2), consists of the quiescent power due to the quiescent current I_Q , and the power loss due to the absorption of the ripple current in the CDA ($i_{AB(pp)}=I_{HYS}$).

$$P_{loss_D} = f_{sw(nb)} C_{eq} V_{DD}^2 + \frac{R_{eq}}{R_L} i_o v_{DD_PA} \quad (5.A1)$$

$$P_{loss_AB} = I_Q V_{DD} + \frac{1}{4} I_{HYS} V_{DD} \quad (5.A2)$$

where R_L represents the RF load.

By substituting eqn. (5.1) into eqn. (5.A1), P_{loss} is derived as:

$$P_{loss} = f_{sw(nb)} C_{eq} V_{DD}^2 + \frac{R_{eq}}{R_L} i_o v_{DD_PA} + I_Q V_{DD} + \frac{V_{DD}^2}{16L_O f_{sw(nb)}} \left[1 - \left(\frac{L_O \times SR i_o + v_{DD_PA} - \frac{1}{2} V_{DD}}{\frac{1}{2} V_{DD}} \right)^2 \right] \quad (5.A3)$$

The optimum switching frequency $f_{sw_op(nb)}$ can be derived by taking the derivative of P_{loss} (eqn. (5.A3)) and equating it zero (i.e., $\partial P_{loss} / \partial f_{sw(nb)} = 0$). $f_{sw_op(nb)}$ is derived as eqn. (5.2).

Chapter 6 Conclusions and Recommendations

In this chapter, conclusions will be drawn for the work reported in this Ph.D. program, and recommendations for future work will be delineated thereafter.

6.1 Conclusions

This Ph.D. program pertained to the theoretical analysis, and practical design and realization of switching amplifiers with the objective of attaining improved specifications over the state-of-the-art for smartphones, including higher power-efficiency to address the short battery lifespan, lower noise, and wider bandwidth. The specific switching amplifiers were the CDA for audio applications and the hybrid CDA for supply modulators for ET RF PAs. Our theoretical work and derived expressions of the audio CDA have been verified by SPICE simulations and on the basis of measurements on a discretely-realized CDA. For the hybrid CDA, our theoretical work and derived expressions have been verified by SPICE simulations and on the basis of measurements on two monolithically realized hybrid CDAs based on a standard 180nm bulk CMOS process.

In Chapters 2, we have provided a comprehensive and critical literature review of the audio CDA and the hybrid CDA for ET PAs. The literature review served as a preamble to the contributions in this Ph.D. program delineated in Chapters 3-5.

In Chapter 3, the effect of supply noise in the AC ground to PSRR has been analytically investigated, and the associated analytical expressions have been derived. Of specific interest, the analysis has been applied to the ubiquitous 3-state BTL closed-loop PWM CDA, taking into consideration not only the effect of the non-ideal AC ground, but also the effect of the resistor and capacitor mismatch based on a realistic fully-differential integrator model; reported literature assumed a simplistic model, leading to incomplete inferences. Further, the PSRR analysis of 3-state BTL closed-loop CDAs has been extended to the double-feedback topology.

We have shown that a reduction of the noise on the AC ground, as expected, would drastically improve the PSRR. However, the CDA with 1st-order integrators unexpectedly provided similar or higher PSRR than the CDA with 2nd-order integrators if both CDAs were designed with the same carrier attenuation – this inference is counter intuitive to that reported in literature. In short, the theoretical analyses and derived equations provide valuable insights to CDA designers into the mechanisms of PSRR in audio CDAs.

In Chapter 4, we have investigated the mechanisms of power dissipation and have proposed an optimization method of the supply modulator for wideband applications. Particularly, we have shown that a controller with zero threshold current not only improved the bandwidth of the supply modulator but also reduced its power dissipation.

Based on our aforesaid investigations, we have proposed a wideband high power-efficiency hybrid CDA embodying a novel delay-based hysteresis controller and a novel wideband Class AB amplifier. The proposed supply modulator (from measurements on the prototype IC) featured the widest bandwidth (40MHz) amongst reported supply modulators to date, yet whose other parameters are highly competitive. Specifically, on the basis of a composite figure-of-merit (bandwidth \times output power \times power-efficiency \times output swing \times 1/ripple noise), our proposed supply modulator featured the most competitive figure-of-merit to date – a very significant 20x improvement over reported supply modulators.

In Chapter 5, we have explored the design challenges of the hybrid CDA for multi-standard RF communication protocols and have analyze the optimum switching frequency for maximum power-efficiency. On the basis of the aforesaid, we have proposed a hybrid CDA with a novel dual-mode Sigma-Delta control and adaptive biasing Class AB amplifier to self-adjust the operation according to the input envelope signals. On the basis of measurements on IC prototypes embodying the proposed architecture, our proposed supply modulator significantly improved its static power-efficiency by up to ~6%. When tracking 40MHz LTE-A envelope signals, the proposed supply modulator featured the highest power-efficiency (85% at 1.8W) over the state-of-the-art and remained highly power-efficient (>80%) over a wide range of output power. To the best of our knowledge, this is the first reported hybrid CDA that is optimized for multi-standard RF communications protocols.

6.2 Recommendations for Future Work

On the basis of the work in this research program, the following further work is recommended:

- (i) Investigation into the parameters pertaining to the noise of PWM CDAs, specifically the (integrated output) noise and signal-to-noise ratio (SNR). These parameters are pertinent because noise and SNR are commonly quoted and physically meaningful parameters, affecting the noise level of the audio CDA, and ultimately its fidelity. Interestingly, the mechanisms of noise and SNR remain uninvestigated for PWM switching amplifiers. In view of this, it would be interesting to analytically investigate the circuit parameters affecting the noise and SNR, and the mechanisms thereto.
- (ii) Investigation into the mechanisms of non-linearities (including THD, IMD, noise, PSRR and PS-IMD) of practical hybrid CDAs for ET PAs. These non-linearities are pertinent because they could introduce significant noise to the RF PA, thereby affecting the linearity of the RF PA. At this juncture, it appears that these non-linearities are largely overlooked by supply modulator designers and the mechanisms thereof remain largely unknown. In view of this, we recommend that these non-linearities of hybrid CDAs be investigated and thereafter modeled.
- (iii) Investigation into the interaction between the hybrid CDA and the RF PA in ET PAs. This includes the theoretical analysis of the optimal shaping function of the envelope signals, and the effect of non-idealities of hybrid CDA to the RF PAs. At this juncture, the interaction analysis between the hybrid CDA and the RF PA

remains uncompleted or inadequately understood, including that reported analyses are largely based on ideal models when real circuits may behave very differently. We recommend this interaction analysis based on realistic models of hybrid CDA and RF PA would provide valuable insights into the optimization of the hybrid CDA in terms of bandwidth, power-efficiency, and noise.

- (iv) Finally, an investigation into the thermal effects of the hybrid CDAs. The thermal effects such as dynamic surface heating effects are important parameters in the design of hybrid CDAs, particularly high output power hybrid CDAs. Further this investigation may potentially lead to better optimizations of the sub-circuits therein and the ensuing complete hybrid CDA.

Author's Publication

Patent Publications

1. Joseph S. Chang, Tong Ge, **Huiqiao He**, and Linfei Guo, "Ultra-Wide-Bandwidth-cum-Ultra-High-Output-Power Supply Modulators for Multi-Standard Applications," Singapore Provisional Patent 10201804846Y, 2018.

Journal Publications

2. **Huiqiao He**, Yang Kang, Tong Ge, Linfei Guo, and Joseph S. Chang, "A 2.5W 40MHz-Bandwidth Hybrid Supply Modulator with 91% Peak Efficiency, 3V Output Swing and 4mV Output Ripple at 3.6V Supply," *IEEE Trans. on Power Electronics*, DOI: 10.1109/TPEL.2018.2827396, Early Access.
3. **Huiqiao He**, Tong Ge, Linfei Guo, and Joseph S. Chang, "3-state BTL Closed-loop PWM Class D Amplifiers," *Analog Integrated Circuits and Signal Processing*, vol. 88, pp. 255-266, 2016.
4. Tong Ge, **Huiqiao He**, Linfei Guo, and Joseph S. Chang, "A Direct Battery Hookup Filterless PWM Class D Amplifier with >100dB PSRR for 100Hz to 1kHz, 0.005% THD+N and 16 μ V noise," *IEEE Trans. on Power Electronics*, submitted.

Conference Publications

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