Low-thermal-mass LEDs: size effect and limits

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Abstract: Low-thermal-mass LEDs (LTM-LEDs) are developed and demonstrated in flip-chip configuration, studying both experimentally and theoretically the enhanced electrical and optical characteristics and the limits. LTM-LED chips in 25×25 μm^2, 50×50 μm^2, 100×100 μm^2 and 200×200 μm^2 mesa sizes are fabricated and comparatively investigated. It is revealed that the electrical and optical properties are improved by the chip size due to reduced thermal mass. With a smaller chip size (from 200 μm to 50 μm), the device generally presents higher current density against voltage and higher power density against current density. However, the 25×25 μm^2 device behaves differently, limited by the fabrication margin limit of 10 μm. The underneath mechanisms of these observations are uncovered, and furthermore, based on the device models, it is proven that for a specific flip chip fabrication process, the ideal size for LTM-LEDs with optimal power density performance can be identified.

Key words: Light-emitting diodes; Thermal effects; Semiconductor materials; Microstructure fabrication.

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1. Introduction

InGaN/GaN light-emitting diodes (LEDs) are playing an important role in many fields including artificial lighting,[1-6] displays,[5,7,8] communications[9],[10] and neurosciences[11]. To fulfill the requirements of these different applications, LEDs always have been designed into various sizes and geometries. As widely accepted, one of the important applications for GaN based LEDs is general lighting. In this respect, broad-area LEDs have usually been commonly adopted to meet the requirements of high output power, high efficiency and reliability.[12-14] The current density of the broad-area LEDs is typically in the range of 1A/cm^2 to 100A/cm^2. Yet, such LEDs with much larger chip sizes are not effective in achieving higher light extraction efficiency,[15],[16] higher power densities[17],[18] and faster pulsed operation[16] even when operating at higher current densities, which make

them unsuitable for the applications that require high current densities, high power densities and high speed operation. Therefore, smaller sized LEDs have been proposed, which are deemed more appropriate for such applications including micro-displays[19] and visible communications,[10] which typically need the LEDs to operate in the current density range beyond 1,000A/cm^2. To understand why smaller-sized LEDs can sustain higher current densities and deliver higher power densities, LEDs of different sizes were previously reported.[20]

In the fabricating process of both conventional and micro-sized LEDs, it is important to prevent surface recombination on the mesa sidewalls, and the current spreading layer should therefore be made smaller than the P-GaN mesa.[16],[17],[21] Nominally, P-contact area is used as the LED effective area to calculate the current density and power density. However, it is reported that the current will not stop at the edge of the spreading layer, and instead will decrease exponentially away from the edge of the P-contact.[17] As a result, the mesa area around the P-contacts, which is not covered by the metal-contact, will also emit light, even though not as strong as the covered area. Therefore, there exists a deviation from the effective area. This deviation will become even larger when the size of the LEDs decreases to several tens of micrometers. On the other hand, as a conductive path, the distance between the N-contact and the LED mesa has a big influence on the current spreading and output power of the LEDs, especially for the smaller sized LEDs.[17] This will place a constraint limiting the potential improvement achievable with the size effect. However, previous works did not study these issues or report the limits.

In this work, we developed and comparatively studied LTM-LEDs with their mesa area varied from 200×200 μm^2 down to 25×25 μm^2 in flip-chip configuration. To make a fair comparison between the different sizes of the LEDs, we purposely keep the distance between the N-pad and the LED mesa a constant. Also, we take the mesa area (instead of the P-contact area) as the effective area for the calculation of the current density and power density, which is more meaningful and accurate for the assessment of the smaller sized LEDs. The revaluation of the size-dependent electrical and optical properties of the LTM-LEDs is carefully studied here, which is found to help to identify the optimized size of the LTM-LEDs for the high-power density and for high-speed applications.

2. Experiments

The LED epitaxial wafers used in this work were grown on c-plane sapphire substrates by metal-organic chemical vapor deposition (MOCVD) system. Trimethylgallium (TMGa), trimethylindium (TMIn), trimethylaluminum (TMAl), and ammonia (NH_3) were used as Ga, In, Al and N precursors, respectively. First, a 3 μm thick unintentionally doped GaN was grown, and then followed by a 5.5 μm thick N-doped GaN (doping concentration≈5×10^{18}/cm^3), in which silane (SiH_4) was used as the dopant source. Then, eight

pairs of $In_{0.15}Ga_{0.85}N$/GaN (3nm/12nm thick) multiple quantum wells (MQWs) were grown. Next, a 20 nm thick P-doped $Al_{0.15}Ga_{0.85}N$ electron blocking layer (EBL) was utilized to suppress the excess electron overflow into the P-GaN region. Finally, a 200 nm thick P-doped GaN (doping concentration$\approx 3\times10^{17}/cm^3$) was grown as the hole source layer. The p-type conductivity of the EBL and the hole source layer was realized by Mg doping where Bis(cyclopentadienyl)magnesium (Cp2Mg) was used as the Mg precursor.

Following the MOCVD growth, the LED wafers were fabricated into flip-chip LED devices using standard micro fabrication techniques. Mesa areas in four different sizes of 25×25 μm^2, 50×50 μm^2, 100×100 μm^2 and 200×200 μm^2 were prepared using reactive ion etching (RIE) on the same wafer. Ni/Ag based metal layers were deposited and annealed in oxygen ambient as the current spreading layer. The areas of the current spreading layers are 15×15 μm^2, 40×40 μm^2, 90×90 μm^2 and 190×190 μm^2, correspondingly. Ti/Au (30 nm/1000 nm thick) metal layers were deposited by an e-beam evaporation as the P- and N-contact pads. The current-voltage characteristics of the LED chips were measured using a LED tester (M2442S-9A Quatek Group) and the optical output power was measured by an integrating sphere attached to an Ocean Optics spectrometer (QE65000).

To understand the underlying physics, numerical modeling was performed to reveal the effect of the mesa size on the electrical and optical characteristics. In our simulations, we used the APSYS software to self-consistently solve the Poisson equation, the continuity equation, and Schrödinger equation with proper boundary conditions. The carrier screening effect in the InGaN quantum wells was taken into account using the self-consistent six-band *k•p* theory.[22] The Auger recombination coefficient was set to be $1\times10^{-30}cm^6s^{-1}$.[23] The Shockley-Read-Hall (SRH) lifetime was set to be 43 ns.[23] Simultaneously, due to the crystal relaxation through dislocation generation during the growth, a 40% of the theoretical polarization induced sheet charge density was assumed in the heterojunction.[24] In the $In_{0.15}Ga_{0.85}N$ quantum well regions, the energy band offset ratio $\Delta E_C/\Delta E_V = 70/30$[25] was taken. The other parameters used in the simulation can be found elsewhere.[26],[27]

3. Results and discussion

Figs. 1(a) and 1(b) are the experimental measurement and numerical simulation of the current density-voltage (*J-V*) characteristics for the LTM-LEDs with different sizes. The computed results show the same trend with the experimental data for different sized LEDs. From Figs. 1(a) and 1(b), it is clear that the *J-V* property is improved as the device size decreases from 200×200 μm^2 to 50×50 μm^2. Higher current density can be obtained in smaller devices at a given voltage. Although the simulation results are consistent with the experimental results, the physical reason of this phenomenon is not straightforward to understand. Therefore, we further developed a physical model as follows to elucidate the physical mechanisms.

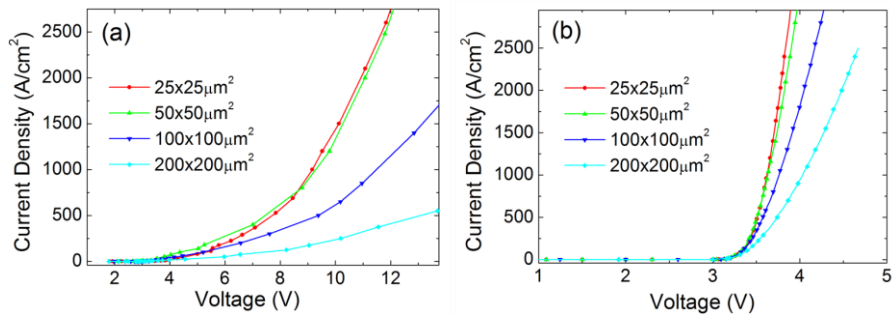

Fig. 1. *J-V* diagrams of LTM-LEDs of different sizes for (a) experimental data; and (b) simulated data.

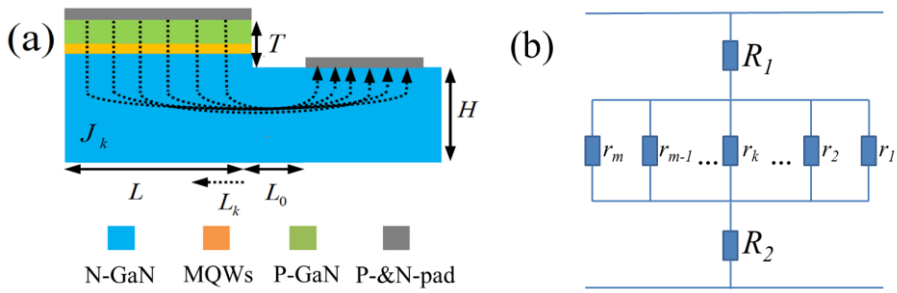

Fig. 2. (a) Schematic current paths of the LTM-LED and (b) the simplified circuit model for the LTM-LED.

Fig. 2(a) shows the schematic drawing of the current paths of the LTM-LED. The width and length of the mesa are both L. L_0 is the distance between the mesa edge and the N-contact edge. (L_k + L_0) is the N-GaN distance across which J_k is flowing before reaching the N-contact. H is the thickness of N-GaN after mesa etching. T is the mesa depth which includes the P-GaN, the MQWs and part of the N-GaN. In our devices, L_0, H and T are fixed for all these four LEDs with different sizes. To facilitate the analysis, we further simplified the equivalent circuit as shown in Fig. 2(b), in which R_1 denotes the resistance along the vertical direction from the p-current spreading layer to the N-GaN and R_2 denotes the resistance corresponding to L_0. The current horizontally flowing along the N-GaN can be divided into m sub-paths, and r_k is the resistance corresponding to L_k where k = 1, 2, …, m-1 and m, in which m is infinity. As we know, for a fixed bias voltage, the higher the resistance is, the lower the current is. Based on the above analysis, the current density is heavily influenced by L. Therefore we use the above model to deduce the relationship between the current density J and L.

First, we deduce the resistance R_1, r_k and R_2 between the P-Pad and the N-pad.

$$R_1 = \sum \rho_i \frac{T_i}{S_1} \tag{1}$$

$$r_k = \rho_{N-GaN} \frac{L_k}{S_2} \tag{2}$$

$$R_2 = \rho_{N-GaN} \frac{L_0}{S_2} \tag{3}$$

where $S_1=L^2$ is the mesa area, $S_2=L\times H$, $T=\sum T_i$ and i refers to individual epitaxial layers, including P-GaN, MQW, and part of N-GaN.

Based on Eq. (1), (2), and (3) we can obtain the current density component J_k :

$$J_k = \frac{V}{\sum \rho_i T_i + \rho_{N-GaN} \frac{L}{H} \times (L_k + L_0)} = \frac{V}{R_0 + aL(L_k + L_0)} \tag{4}$$

where $R_0 = \sum \rho_i T_i$ and $a = \frac{\rho_{N-GaN}}{H}$. Based on Eq. (4), we arrive at the average current density J_{ave}:

$$J_{ave} = \frac{1}{L}\int_0^L J_k dL_k = \frac{V}{aL^2}(\ln^{aL^2+aL_0L+R_0} - \ln^{aL_0L+R_0}) \tag{5}$$

Here, J_{ave} is the current density in our experiments and simulations. Eq. (5) reveals the relationship between the current density J_{ave} and the edge length of the mesa L. To plot the J_{ave} as a function of L, the parameters a and R_0 appearing in Eq. (5) have to be estimated. Based on our experimental result ρ_{N-GaN}=4.745×10^{-3} Ω•cm, and H=5.5 μm, and therefore a=8.627 Ω. R_0 is related to the material properties and device geometry and can be obtained from a specific experimental result. Taking the device of 50×50 μm^2 as an example, when V=11.073 V, J=2,000 A/cm^2, from Eq. (5) we find R_0=5.343×10^{-3} Ω•cm^2. Using the parameters above, the relationship between the current density and the mesa length (J-L) is presented in Fig. 3(a). Although R_0 has an influence on the absolute value of J, it will not change the trend of this relationship. From Fig. 3(a), it can be seen that J decreases with increasing L. That is to say, the smaller the size is, the higher the current density is. This well matches the previously reported results[20] and our observations in Fig. 1. As it is well known that the N-pad and the mesa have to be separated to prevent the side-wall current leakage. The distance L_0 between the N-pad and the mesa is an important parameter to be optimized as it also affects the characteristics of the current density as shown in Fig. 3(b). It can be seen from Fig. 3(b) that with the increasing L_0, the current density J will decrease. This is because the resistance from N-pad to P-pad is increasing with L_0. Therefore, L_0 has to be optimized to fulfill the requirement of both preventing current leakage and increasing the current density.

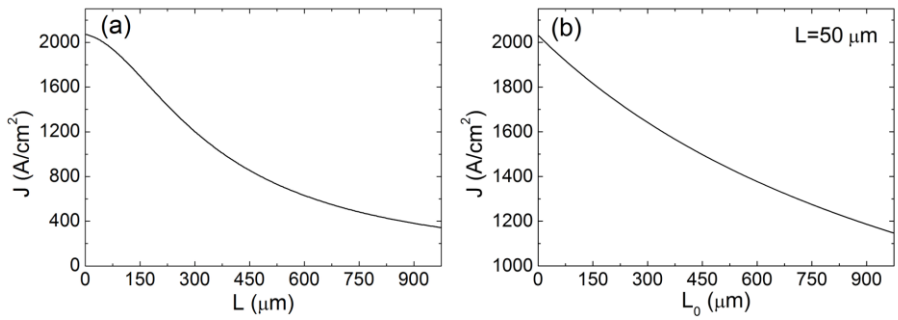

Fig. 3. (a) *J-L* and (b) *J-L$_0$* behaviour at a fixed voltage bias (11.073V).

It is worth noting that the *J-V* improvement in Fig. 1 is less significant when the chip size is further scaled down from 50×50 μm^2 to 25×25 μm^2. This is different from the previously reported results,[20] where the *J-V* is improved consistently even when the chip size is smaller than 50×50 μm^2. The reason for this difference is that the P-contact area was used as the LED effective area to calculate the current density in the previous reports while in our results the mesa area was used. Therefore, due to the fact that the P-contact area is always smaller than the mesa area (the edge of the mesa is not covered by the metal layer), there is a limit on the current density improvement with the decreasing device size and an optimal mesa size should exist and can be found out through numerical simulations. A further detailed discussion in this report will be conducted later.

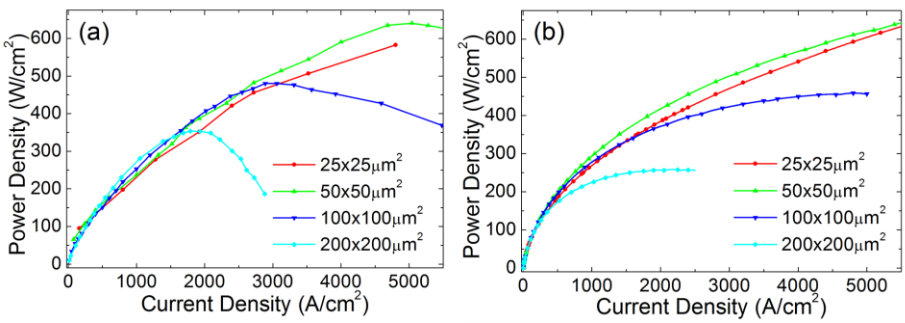

Fig. 4. *PD-J* diagrams of LTM-LEDs in different sizes: (a) experimental results and (b) simulation results.

Figs. 4(a) and 4(b) show the experimentally measured and numerically simulated power density-current density (*PD-J*) diagrams of the LTM-LEDs of different sizes, respectively. The simulated *PD-J* characteristics of the studied chips exhibit the same trend with the experimental ones. It can be seen that the power density is increasing initially with the increasing current density and then starts saturating and decreasing after reaching a peak point as the current density further increases for the devices of 200×200 μm^2, 100×100 μm^2 and 50×50 μm^2. More importantly, the power density of the smaller chips is always larger than that of the larger chips in the whole current density range and the peak power density of the smaller chips is much larger than that of the larger chips at much larger current density.

These characteristics of *PD-J* of the different sized chips show that the smaller chips are much superior when operating at high current density and delivering high power density. The reason behind this is the low thermal mass of the smaller chips, storing less heat. As the LTM-LED size decreases, r_k will become smaller. Accordingly, the heat generated by the additional r_k is $I^2 r_k t$. This decreased resistance will generate less Joule heat, which is the main reason for low thermal effect of the smaller chips. The external quantum efficiency (EQE) of the LEDs is adversely affected by the heat generated in the devices[28]. Since much less heat is generated in the LTM-LED chips, the EQE is preserved well even at high current density, and therefore a much improved power density is realized in the LTM-LEDs. It should be noted in Figs. 4(a) and (b) that as the chip size further scales down from 50×50 μm^2 to 25×25 μm^2, the power density performance starts to degrade. This phenomenon can be explained by the difference of the areas of the current spreading layer and the mesa. As we have mentioned above that the side length of the current spreading layer is 10 μm shorter than that of the mesa, this means high resistance region exists in the margin area, which becomes critical in the very small device size. To find how the margin area affects the 25×25 μm^2 device, we put forward a model to analyze the structure.

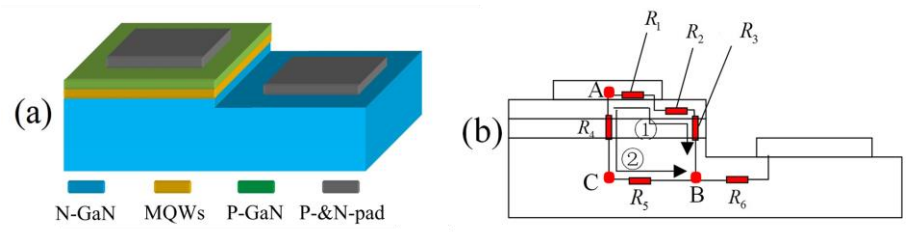

Fig. 5.

Schematic view of (a) LTM-LED current spreading layer and mesa margin and (b) the equivalent circuit model for the margin effect.

Fig. 5(a) shows the general view of the LTM-LED, especially the perceptual intuition of the current spreading layer and the mesa. Fig. 5(b) shows the schematic diagram of the circuit of the different current path ways between the current spreading layer and the mesa. R_1 is the resistance of the P-pad, which is made of metal, so the resistance is very small. R_2 is the resistance of P-GaN in the margin area. R_3 and R_4 are the resistance of PN junction, which is from P-GaN, through MQWs to N-GaN. R_5 and R_6 are the N-GaN resistance from point *C* to point *B* and point *B* to N-pad, for which the resistivity is much smaller than that of P-GaN. To compare the effect of the margin area, we select two current path ways from point *A* to point *B*. One includes the resistance of P-GaN in the margin area, and the other one is randomly selected just under the P contact area: ① is the path through R_1, R_2 and R_3, including P-pad, the margin area and PN junction, which has the current value of I_1; ② is the path through R_4

and R_5, including PN junction and part of N-GaN, which has the current value of I_2. If we consider the current ratio of ① and ②:

$$\frac{I_1}{I_2} = \frac{R_4 + R_5}{R_1 + R_2 + R_3} \tag{6}$$

From Eq. (6), we can see that when R_2 is much larger than R_1, R_3, R_4 and R_5. Therefore, I_1 will be much smaller than I_2. This is the main reason for the similar current density vs. voltage behavior for the devices with the size of 25×25 μm^2 and 50×50 μm^2. Due to the fabrication limitation that a margin area without the cover of current spreading layer is inevitable for a reliable device, with the decrease in the chip size, the current density improvement as a function of the voltage will be diminished. On the other hand, the ratio of the current spreading layer area to the mesa area for the 25×25 μm^2 device is 0.36, much smaller than that of 50×50 μm^2 device which is 0.64. The mesa area without the current spreading layer cover has much lower optical output power density due to the lower current density. Therefore, the ratio of the effective radiation area is smaller for the 25×25 μm^2 device. This leads to the degradation of the power density of the 25×25 μm^2 device compared to that of the 50×50 μm^2 size one.

4. Conclusions

In conclusion, the size effect and the fabrication limitation of LTM-LEDs have been experimentally and theoretically studied and understood. Both experimental and numerical results show that there exists an optimal mesa size for the current density and power density performance of the LTM-LEDs with the mesa area different from the current spreading layer area. Based on this work, as a design rule of thumb for high current density and high power density LTM-LEDs, three key points can be listed: first, the current spreading layer size should be made as close as possible to the mesa size; second, an optimum mesa size should be determined according to the specific layer structures and the design layout; third, the N-pad should be made as close to the P-pad as possible before any severe current leakage happens.

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