Broad-Band Design Techniques for Transimpedance Amplifiers

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***Abstract*—In this paper, a novel bandwidth enhancement technique based on the combination of capacitive degeneration, broad-band matching network, and the regulated cascode (RGC) input stage is proposed and analyzed, which turns the transimpedance amplifier (TIA) design into a fifth-order low-pass filter with Butterworth response. This broad-band design methodology for TIAs is presented with an example implemented in CHRT 0.18-μm 1.8-V RF CMOS technology. Measurement data shows a −3-dB bandwidth of about 8 GHz with 0.25-pF photodiode capacitance. Comparing with the core RGC TIA without capacitive degeneration and broad-band matching network, this design achieves an overall bandwidth enhancement ratio of 3.6 with very small gain ripple. The transimpedance gain is 53 dBΩ with a group delay of 80 ± 20 ps. The chip consumes only 13.5-mW dc power and the measured average input-referred noise current spectral density is 18 pA/$\sqrt{\text{Hz}}$ up to 10 GHz.**

***Index Terms*—Bandwidth enhancement, broad-band, matching network, regulated cascode (RGC), transimpedance amplifier (TIA).**

I. Introduction

THE dramatic growth of data transportation volume and speed over the Internet in recent years entails the development of low cost integrated optical communication systems with ever-increasing transmission bandwidth [1]. Currently, the most successful high-speed digital communication protocol is SONET OC-192 while the 10-Gb/s Ethernet (IEEE 802.3ae) is also emerging as an alternative for point-to-point applications [2]. Therefore, optical communication systems operating at 10 Gb/s are of great interest. Transimpedance amplifiers (TIAs) are extensively exploited as the front-end of optical communication receivers. Traditionally, such front-end circuits and devices are heavily dependent on III/V technologies due to their speed and noise advantages. However, the demand for high volume and wide deployment of optical components in recent years makes silicon based integrated circuits the most economical solution. CMOS appears to be the best candidate for fully integrated TIA design due to its cost, integration and manufacturability advantages and providing reasonable speed, noise performances at the same time.

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Among all the challenges in the design of fully integrated CMOS broad-band TIAs, sufficient bandwidth with small gain ripple is of first priority and low-noise is second because the noise of the preamplifier dominates that of the whole receiver. Due to the inferior parasitic and noise characteristics of CMOS technology, many circuit techniques have been studied in CMOS TIA design to achieve comparable performances to those III/V or SiGe counterparts.

The main bandwidth restriction of a conventional TIA is usually at the input node due to the large parasitic photodiode capacitance. By modifying conventional common-gate (CG) input stage to regulated cascode (RGC) [3] or common gate feedforward [4] topology containing negative feedback, very small input impedance can be obtained to relax the gain-bandwidth tradeoff at the input node. Capacitive degeneration [5] or peaking [6] utilizes capacitive elements to add an extra zero that compensates the dominant pole or an extra pole to implement a well-controlled Butterworth response, respectively. Inductive peaking is found effective both in noise reduction and bandwidth enhancement [7]. Shunt inductive peaking [8], [9] simply uses inductor in series with the load resistor to maintain a constant effective load over a wider frequency range. Series inductive peaking [10], [11] normally employs inductors between active devices of gain stages or between active device and capacitive load at input/output node so that the combined parasitic capacitances at each node are split into *LC* networks. The whole TIA is turned into a low-pass filter with controllable passband characteristics. This paper describes a novel bandwidth enhancement method that based on the interaction of matching *LC* network, RGC input stage and capacitive degeneration stage, which turns the TIA into a fifth-order Butterworth low-pass filter. The merit of this topology is, as we will discuss in Section III, while enhancing the bandwidth, providing efficient noise reduction.

II. Broad-band Design Techniques

A. RGC Stage

The RGC input stage in Fig. 1(a) is well suited for broad-band TIA design by its very low input impedance [3], which could be derived from the small-signal circuit model in Fig. 1(b) as shown in (1) at the bottom of the next page, where $C_i \approx C_{sb1} + C_{gs2}$ and $C_j \approx C_{gs1} + C_{gd2}$. The small-signal input resistance is therefore given by

$$r_i = Z_{\text{in}}(0) \approx \frac{1}{g_{m1}(1 + g_{m2}R_2)}. \tag{2}$$

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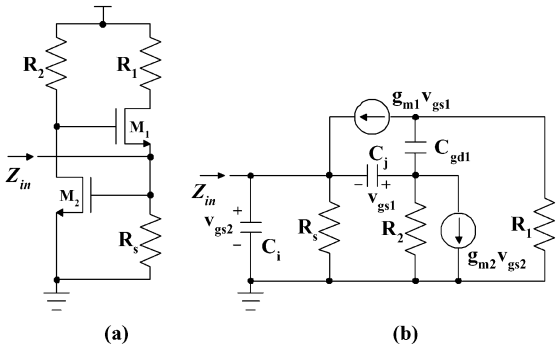

Fig. 1. RGC stage. (a) Its circuit schematic. (b) Its small-signal model.

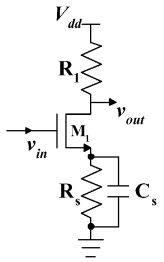

Fig. 2. Gain stage with capacitive degeneration.

This very small input impedance in large part isolates the photodiode capacitance from bandwidth determination and therefore, unlike common gate or common source TIAs, the dominant pole of an RGC TIA is usually located within the amplifier rather than at the input node [3].

B. Capacitive Degeneration

Besides pushing the dominant pole to higher frequencies to increase the bandwidth, it is also possible to compensate the dominant pole with a zero, which could be accomplished by capacitive degeneration. As shown in Fig. 2, the voltage gain of a gain stage with capacitive degeneration is expressed by [5]

$$A_v = \frac{v_{\text{out}}}{v_{\text{in}}} = \frac{g_{m1}R_1}{1+g_{m1}R_s}\frac{1+sR_sC_s}{1+s\frac{R_sC_s}{1+g_{m1}R_s}} \tag{3}$$

which contributes a zero at $(R_sC_s)^{-1}$ and a pole at $(1+g_{m1}R_s)/R_sC_s$. The zero could be used to compensate the dominant pole of the circuit. The -3-dB cutoff frequency is therefore determined by the second lowest pole of the circuit.

C. Passive Broad-Band Matching Networks

The simplest way that we increase the bandwidth of an existing amplifier topology is to increase the -3-dB cutoff frequency of each gain stage, which is usually accomplished by decreasing the respective resistive load. Smaller resistive load means lower gain and higher input-referred noise current. Since the gain and sensitivity of a front-end amplifier counts to the communication distance directly, it is desirable to maintain a constant gain while pushing the cutoff frequency higher. Passive matching networks could be used to explore the gain-bandwidth limitation without degrading other parameters of an existing amplifier [12]. The principle of increasing the gain-bandwidth product is to maintain a constant load over a wider frequency range. This can be realized by a constant-k filter, which means the passband gain of the filter is constant. The *LC* ladder filter in Fig. 3 is such a realization. Based on Bode–Fano Limit, it is proven [10] that the maximum obtainable gain-bandwidth product enhancement is four times by a two port passive matching network, i.e., the bandwidth at most could be extended to four times of the original amplifier with the gain unchanged. It is notable that four times is the maximum obtainable enhancement. With finite sections of *LC* ladders, we can only achieve maximum bandwidth enhancement with significant gain ripple at the same time. It is hence desirable to design the filter with sufficient bandwidth enhancement and maximum gain flatness (Butterworth-type response). In the case of the two port matching network in Fig. 3, which is designed to exhibit nth-order Butterworth characteristic, the power gain of this filter must satisfy [12]

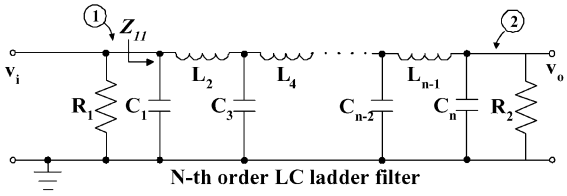

Fig. 3. Small-signal model of an nth-order *LC* ladder filter.

$$|S_{21}(j\omega)|^2 = \frac{K_n}{1+\left(\frac{\omega}{\omega_c}\right)^{2n}} \tag{4}$$

where K_n is the dc gain and ω_c is the cutoff frequency. It is derived that, to satisfy (4), the impedance matching condition is given by [12]

$$Z_{11}(s) = R_1\frac{q(y)-\delta^n q(y/\delta)}{q(y)+\delta^n q(y/\delta)} \tag{5}$$

where $y = s/\omega_c$, $\delta = \sqrt[n]{(R_1-R_2)/(R_1+R_2)}$ and $q(y)$ is the Butterworth polynomial defined as

$$q(y) = \sum_{m=0}^{n} a_m y^m \tag{6}$$

$$Z_{\text{in}}(s) \approx \frac{\left(\frac{1}{R_2}+sC_j\right)}{\left(g_{m2}+\frac{1}{R_2}\right)(g_{m1}+sC_j)+\left(\frac{1}{R_2}+sC_j\right)\left(\frac{1}{R_s}+sC_i\right)} \tag{1}$$

and the coefficients a_m follow a recursion formula given by

$$\frac{a_{k+1}}{a_k} = \frac{\cos(k\pi/2n)}{\sin[(k+1)\pi/2n]}, \qquad k = 0, 1, 2 \ldots, n-1. \quad (7)$$

Looking into node 1 of Fig. 3 the input admittance of the passive matching network can also be written as

$$\frac{1}{Z_{11}} = sC_1 + \frac{1}{sL_2 + \frac{1}{\cdots sL_{n-1} + \frac{1}{sC_n + \frac{1}{R_2}}}}. \quad (8)$$

Comparing (5) with (8) and following the recursion formula given by (7), the values of *LC* elements can be computed. The detailed derivation can be found in [12].

III. Circuit Design and Analysis

The three broad-band design techniques introduced in Section II are combined together to design a high-performance 10-Gb/s TIA in this section. The *LC* ladder filter employed in this design is used to enhance the bandwidth and reduce the equivalent input noise current as well, which will be analyzed in detail in this section.

A. Bandwidth Enhancement

The proposed design schematic is shown in Fig. 4(a). The circuit is composed of four parts, namely the matching network, the RGC input stage, the gain stage with capacitive degeneration and the source follower output stage. The dc transimpedance gain is given by

$$Z_T(0) \approx R_1 \frac{g_{m3}R_3}{1+g_{m3}R_b} \frac{g_{m4}R_4}{1+g_{m4}R_4} \quad (9)$$

where we can infer that the transimpedance gain is mainly determined by R_1. The RGC stage [3] presents a very small input resistance and therefore the lowest pole of the circuit is located within the TIA at node A, which is given by

$$f_{-3\text{ dB},0} = \frac{\omega_0}{2\pi} \approx \{2\pi R_1[C_{gd1} + C_{db1} + C_{g3}]\}^{-1} \quad (10)$$

where C_{g3} is approximately the sum of the Miller capacitances of C_{gd3} and C_{gs3}. In this design, we choose a small R_2 to avoid possible peaking due to the zero generated by the local feedback of the RGC stage [3] and a relatively large R_s to minimize its noise current contribution and signal loss.

The capacitive degeneration [5] gain stage consists of M_3, R_3, R_b, C_b contributes a zero $(R_bC_b)^{-1}$ that is used to compensate the lowest pole determined at node A, which means

$$f_{-3\text{ dB},0} \approx \{2\pi R_1[C_{gd1} + C_{db1} + C_{g3}]\}^{-1} = (2\pi R_bC_b)^{-1}. \quad (11)$$

Besides this zero, the capacitive degeneration also generates an additional pole $(1+g_{m3}R_b)/R_bC_b$ at a higher frequency,

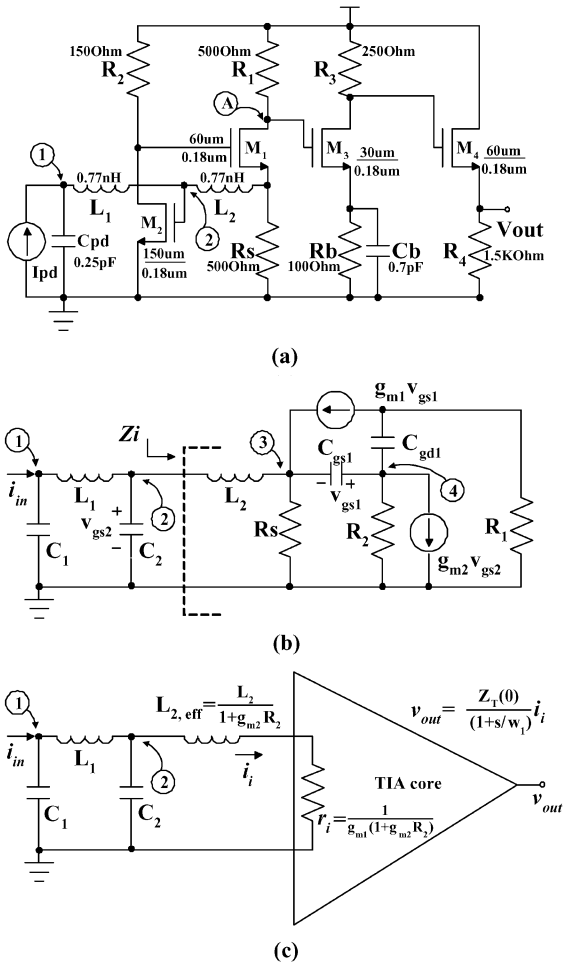

Fig. 4. (a) Schematic of the proposed TIA. (b) Small-signal model of the matching network and the RGC stage. (c) Equivalent low-pass filter representation of the proposed TIA.

which, in this design, is the second lowest pole of the circuit and therefore the new -3-dB bandwidth can be estimated by

$$f_{-3\text{ dB},1} = \frac{\omega_1}{2\pi} \approx \frac{1+g_{m3}R_b}{2\pi R_bC_b}. \quad (12)$$

M_4, R_4 is the source follower output stage to drive the capacitance of the output pad. In this design, the lowest pole at node A is targeting at about 2.5 GHz and the bandwidth after capacitive degeneration is chosen to be around 4.5 GHz, which means $g_{m3}R_b \approx 0.8$. For a typical 10-Gb/s TIA, the bandwidth is usually between 0.6 and 1.2 B (where B stands for the bit rate) [13]. Therefore, the bandwidth of the core TIA is not enough and additional bandwidth extension is to be achieved by a broad-band matching network between the photodiode and the core TIA. Fig. 4(b) illustrates the small-signal model of the matching network and the RGC input stage, where C_1 is the combined parasitic capacitance at node 1 including photodiode capacitance C_{pd}, and C_2 is the combined parasitic capacitance at node 2. In essence, this matching network is not purely passive because it interacts with the RGC input stage and we need to convert it to an equivalent passive matching network so that the analysis method introduced in Section II-C could be applied. Looking

from left to right at node 2 in Fig. 4(b) and based on small-signal circuit analysis in the Appendix, we can get

$$Z_i \approx \frac{sL_2}{1+g_{m2}R_2} + \frac{1}{g_{m1}(1+g_{m2}R_2)} = sL_{2,\text{eff}} + r_i \quad (13)$$

where we define $L_{2,\text{eff}} = (L_2)/(1+g_{m2}R_2)$ and $r_i = (1/g_{m1}(1+g_{m2}R_2))$. Based on this definition, we can simplify the matching network in Fig. 4(b), which is not purely passive due to its interaction with active devices of the RGC input stage, to a purely passive one. As shown in Fig. 4(c), the whole amplifier is simplified to a passive matching network with L_2 replaced by $L_{2,\text{eff}}$ followed by a core TIA with a dominant pole ω_1 expressed by (12) and an input resistance defined in (13). To simplify the analysis, we have neglected the effects of all other poles and zeros of the core TIA circuit. The reason is, firstly there are two prominent zeros in the proposed design, one is used to compensate the lowest pole of the circuit and the other is due to the local feedback of the RGC stage and can be optimized to be beyond the bandwidth of interest, secondly the poles at the drains of M_2 and M_3 are designed to be at much higher frequencies, finally the pole at the output node is also neglected due to the small output resistance of the source follower stage. Though these poles are neglected for analysis simplicity, their combinational effect will cause the actually -3-dB bandwidth of the core TIA lower than that expressed in (12).

The effective inductance $L_{2,\text{eff}}$ in the equivalent matching network is $(1+g_{m2}R_2)$ times smaller than the actual value of L_2 by the effect of RGC stage. This equivalent matching network consists of C_1, L_1, C_2 and $L_{2,\text{eff}}$ is fourth-order and considering the dominant pole ω_1 of the core TIA, the whole amplifier can be approximated to a fifth-order low-pass filter with a frequency independent gain $Z_T(0)$. From the small-signal circuit model in Fig. 4(c), the transfer function of the whole circuit can be derived as

$$Z_T(s) = \frac{Z_T(0)}{1+\frac{s}{\omega_1}} \times \frac{1}{1+s(C_1+C_2)Z_i + s^2L_1C_1 + s^3L_1C_1C_2Z_i} \quad (14)$$

where ω_1 is the estimated -3-dB bandwidth of the core TIA, which is given by (12), and Z_i is given by (13). To design this transfer function with Butterworth response, the most convenient way is to map the coefficients of the denominator of (14) to the fifth-order Butterworth coefficients. As introduced in Section II-C, the coefficients of a fifth-order Butterworth polynomial $q(y) = a_0 + a_1y + a_2y^2 + a_3y^3 + a_4y^4 + a_5y^5$ can be computed as $a_0 = 1, a_1 = 3.2360, a_2 = 5.2360, a_3 = 5.2360, a_4 = 3.2360, a_5 = 1$ [12]. Therefore, we can write the coefficients of the denominator of (14) as

$$\omega_c\left[\frac{1}{1\omega_1} + r_i(C_1+C_2)\right] = a_1 \quad (15)$$

$$\omega_c^2\left[L_1C_1 + \left(L_{2,\text{eff}} + \frac{r_i}{\omega_1}\right)(C_1+C_2)\right] = a_2 \quad (16)$$

$$\omega_c^3\left[\frac{L_1C_1 + L_{2,\text{eff}}(C_1+C_2)}{\omega_1} + L_1C_1C_2r_i\right] = a_3 \quad (17)$$

$$\omega_c^4\left[\frac{L_1C_1C_2r_i}{\omega_1} + L_1L_{2,\text{eff}}C_1C_2\right] = a_4 \quad (18)$$

$$\omega_c^5\frac{L_1L_{2,\text{eff}}C_1C_2}{\omega_1} = a_5 \quad (19)$$

where r_i and $L_{2,\text{eff}}$ are given in (13), ω_c is the cutoff frequency of the whole amplifier with matching network. Our design goal is to achieve $\omega_c = 2\omega_1$, i.e., $f_c = 2f_1 = 9$ GHz. The design parameters can be computed from these equations to implement a Butterworth-type response TIA. Simulation result in Fig. 10 shows that, without any bandwidth enhancement technique employed, the RGC TIA exhibits only about 2.2 GHz -3-dB bandwidth and after the compensation by capacitive degeneration, the bandwidth is extended to about 4.5 GHz. A bandwidth enhancement ratio of 2 is further achieved by the broad-band matching network and the simulated bandwidth is extended to about 9.1 GHz.

B. Noise Analysis and Reduction

The equivalent input noise current, also called input-referred noise current, is a significant figure of merit of TIAs in that it directly affects the optical link budget. The bit error rate (BER) of an optical front-end can be expressed in terms of the total equivalent input noise current $i_{\text{total},n,\text{eq}}$ by [5], [13]

$$\text{BER} = Q\left(\frac{i_{\text{in,pp}}}{2i_{\text{total},n,\text{eq}}}\right) \quad (20)$$

where $i_{\text{in,pp}}$ is the peak to peak input current signal amplitude and $Q(x) = \int_x^\infty (1/\sqrt{2\pi})\exp(-(x^2/2))\,dx$. The equivalent input noise current is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actually noisy TIA [13]. Although the TIA noise model can be conveniently represented by a noise current source only, the equivalent input noise current is dependent on the source impedance, which is mainly determined by the photodiode capacitance and the matching network [13]. Therefore, standard noise analysis in terms of $E_n - I_n$ model (both noise voltage and noise current sources are present) [14] is necessary to evaluate the influence of the input matching network on noise.

In this section, we will evaluate the noise reduction effect in our proposed circuit by expressing the equivalent input noise current in terms of the $E_n - I_n$ pair. From the schematics in Fig. 4 and (9), (24), we can see that, only a portion of the input current that flows through the channel of M_1 to the following stages will produce the transimpedance gain, other portion of the input current will be lost through parasitic capacitances and the channel of M_1 can be viewed as a resistive element $r_i = (1/(g_{m1}(1+g_{m2}R_2)))$. Based on this concept, we can draw the TIA noise model in Fig. 5(a). Only $i_{n,\text{eq},0}$, which is the portion of the total input-referred noise current flowing through r_i, will produce output noise $v_{n,o}$ and $Z_T = (v_{n,o})/(i_{n,\text{eq},0})$. Fig. 5(a) also represents a simple TIA model with series inductive matching between the photodiode and the amplifier, which is renowned to be very helpful in reducing the frequency dependent noise and improving the front-end sensitivity [7], [15].

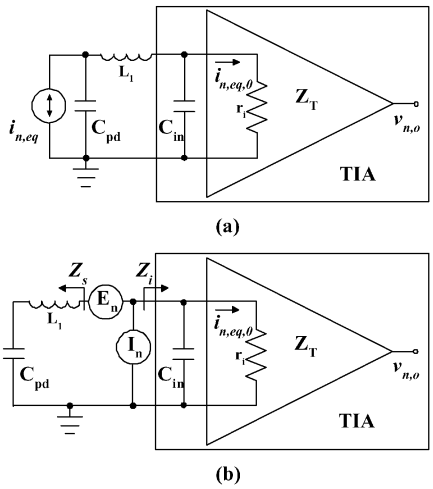

Fig. 5. TIA noise model with series inductive noise reduction: (a) equivalent input noise current model. (b) $E_n - I_n$ model.

Fig. 5(b) shows the $E_n - I_n$ noise model for the same TIA. By small-signal analysis based on Fig. 5(a) and (b), we can express the matching-network-dependent equivalent input noise current spectral density $i_{n,\mathrm{eq}}$ in terms of the $E_n - I_n$ pair as

$$|i_{n,\mathrm{eq}}|^2 = (1-\omega^2 L_1 C_{\mathrm{pd}})^2 I_n^2 + \omega^2 C_{\mathrm{pd}}^2 E_n^2 \tag{21}$$

where C_{pd} stands for the photodiode parasitic capacitance. For a given $E_n - I_n$ noise model, E_n and I_n are independent on the input matching network. However, they are typically frequency dependent [14].

It is also noteworthy that in microwave circuit design, noise representations are usually based on four noise parameters, i.e., minimum noise figure $F_{\min}$, real and imaginary parts of optimum source admittance Y_{opt} and noise resistance R_n. It is proven in [16] that a general expression for equivalent input noise current spectral density for TIAs with arbitrary matching networks can also be derived based on the above-mentioned noise parameters

$$\overline{|i_{n,\mathrm{eq}}|^2} = 4KT_0 \frac{R_n}{Z_0^2} \left| \frac{1-\Gamma_{\mathrm{opt}}}{1+\Gamma_{\mathrm{opt}}} \right|^2 \tag{22}$$

where T_0 is the reference temperature, Z_0 is the characteristic impedance, Γ_{opt} is the optimum source reflection coefficient.

As we can observe from (21), besides bandwidth enhancement, the broad-band matching network can also help to reduce the equivalent input noise current of the proposed TIA design. The dominant noise sources that referred to the input of a CMOS high frequency TIA are thermal noise and induced gate noise [17]. Although the induced gate noise itself adds to the total input noise, it is correlated with the channel thermal noise. The correlated noise, when referring to the input, cancels with other noise sources and helps to reduce the total input-referred noise [18]. In this paper, we will only examine the input-referred noise due to the thermal noise sources by neglecting the induced gate noise. Without the matching network, the equivalent input noise current spectral density of the proposed TIA can be estimated using the analysis method in [3] as

$$\begin{aligned}
\overline{|i_{n,\mathrm{eq}}|^2} \approx{}& \frac{4KT}{R_s} + \frac{4KT}{R_1} && \text{(I)}\\
&+ \frac{4KT\omega^2 C_y^2}{1+\omega^2 C_b^2 R_b^2} \\
&\times \left[\left(\Gamma g_{d0,3} + \frac{1}{R_3} \right) \left(\frac{1+g_{m3}R_b}{g_{m3}} \right)^2 \right. \\
&\left. + R_b \right] && \text{(II)}\\
&+ \frac{4KT\left(\Gamma g_{d0,1} + \frac{1}{R_1}\right)}{g_{m1}^2} \omega^2 \\
&\times \left(C_j + \frac{C_{\mathrm{pd}}}{1+g_{m2}R_2} \right)^2 && \text{(III)}\\
&+ \frac{4KT\left(\Gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2} \\
&\times \left[\frac{1}{R_s^2} + \omega^2 \left(C_{\mathrm{pd}} + C_i \right)^2 \right] && \text{(IV)}
\end{aligned} \tag{23}$$

where K is Boltzmann constant, T is the absolute temperature, Γ is the noise factor of the MOSFET, g_{d0} is the zero-bias drain conductance, $C_i \approx C_{sb1} + C_{gs2}, C_j \approx C_{gs1} + C_{gd2}$, C_y is the total parasitic capacitance at node A in Fig. 4(a) including C_{gd1}, C_{db1} and the Miller capacitances of C_{gd3} and C_{gs3}. Items (I), (III), and (IV) of (23) are due to the thermal noises of the RGC input stage including M_1, R_1, M_2, R_2, and R_s. Item (II) is contributed by the capacitive degeneration stage. On one hand because $R_b C_b$, $g_{m3}R_b$ are predetermined as mentioned in Section III-A and if we choose a small R_b and a large C_b, this noise component can be reduced and on the other hand the numerator and denominator of item (II) both increases with frequency. Hence, at higher frequencies, this noise component can be approximated as $(4KTC_y^2)/(C_b^2R_b^2)[(\Gamma g_{d0,3} + (1/R_3))((1 + g_{m3}R_b)/(g_{m3}))^2 + R_b]$, which is frequency independent. We can observe that the capacitive degeneration not only boosts the bandwidth but contributes small noise as well. Therefore, the major noise contribution is from the RGC input stage including M_1, R_1, M_2, R_2, and R_s.

We will now recalculate the equivalent input noise current contributed by the RGC input stage based on the $E_n - I_n$ model and discuss the noise reduction effect of the input matching network on the proposed TIA design. According to (1), the input admittance of the core TIA without input matching network is

$$\begin{aligned}
Y_{\mathrm{in}}(s) &= g_{m1}(1+g_{m2}R_2) + \frac{1}{R_s} + sC_i + sC_j(1+g_{m2}R_2) \\
&= \frac{1}{r_i} + \frac{1}{R_s} + sC_{\mathrm{in}}.
\end{aligned} \tag{24}$$

Therefore the $E_n - I_n$ noise model of the proposed TIA without matching network can be represented by Fig. 6(a), where C_i and

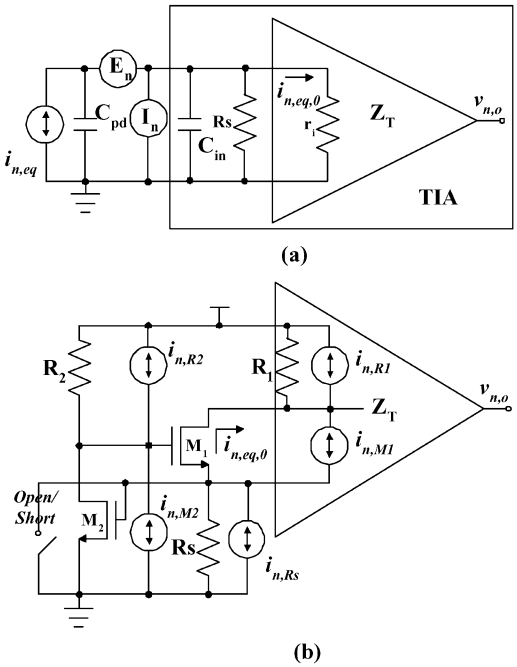

Fig. 6. (a) $E_n - I_n$ noise model of the RGC TIA without input matching network. (b) Its equivalent circuit for noise analysis.

C_j are the same as those in (1) and (23), $C_{\rm in} \approx C_i + (1 + g_{m2}R_2)C_j$, r_i is defined by (2). Usually, one can assume the $E_n - I_n$ correlation to be zero with little error especially when they are only partially correlated [14]. Based on Fig. 6(a) we have

$$|i_{n,\rm eq}|^2 = I_n^2 + \omega^2 C_{\rm pd}^2 E_n^2 \tag{25}$$

where E_n can be evaluated by setting $C_{\rm pd} = \infty$ (short circuit) and I_n can be evaluated by setting $C_{\rm pd} = 0$ (open circuit). As introduced in the beginning of this section, $i_{n,\rm eq,0}$ is the equivalent noise current flowing through the channel of M_1 to the following stages. When assuming the TIA is noiseless, this noise current produces the same output noise as the actual noisy TIA. Based on Fig. 6(a) we can write

$$|i_{n,\rm eq,0}|_{\rm short}|^2 = \left|\frac{E_n}{r_i}\right|^2 \tag{26}$$

$$|i_{n,\rm eq,0}|_{\rm open}|^2 = \left|\frac{R_s}{R_s + r_i + sC_{\rm in}R_s r_i} I_n\right|^2 \tag{27}$$

where $i_{n,\rm eq,0}|_{\rm short}$ stands for the equivalent noise current $i_{n,\rm eq,0}$ when $C_{\rm pd} = \infty$ (short circuit) and $i_{n,\rm eq,0}|_{\rm open}$ denotes the equivalent noise current $i_{n,\rm eq,0}$ when $C_{\rm pd} = 0$ (open circuit). By analyzing the noise sources in Fig. 6(b), we obtain

$$\begin{aligned} &|i_{n,\rm eq,0}|_{\rm short}|^2 \\ &\quad \approx i_{n,R1}^2 + i_{n,M1}^2 + \left(i_{n,R2}^2 + i_{n,M2}^2\right) R_2^2 g_{m1}^2 \end{aligned} \tag{28}$$

$$\begin{aligned} &|i_{n,\rm eq,0}|_{\rm open}|^2 \\ &\quad \approx i_{n,R1}^2 + i_{n,M1}^2 \left(1 - \left|\frac{R_s}{R_s + r_i + sC_{\rm in}R_s r_i}\right|^2\right) \\ &\qquad + i_{n,Rs}^2 \left|\frac{R_s}{R_s + r_i + sC_{\rm in}R_s r_i}\right|^2 \\ &\qquad + \frac{i_{n,R2}^2 + i_{n,M2}^2}{\left(g_{m2} + \frac{1}{R_2}\right)^2} \left|\frac{1 + sC_i R_s}{R_s + r_i + sC_{\rm in}R_s r_i}\right|^2 \end{aligned} \tag{29}$$

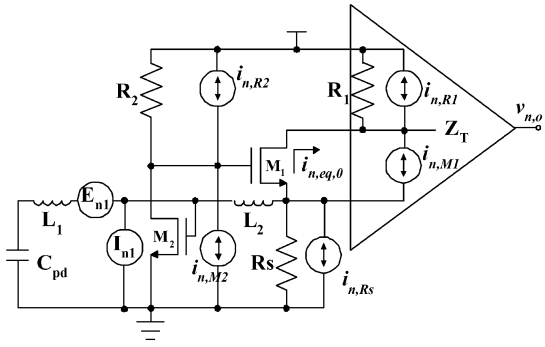

Fig. 7. $E_n - I_n$ noise model of the RGC TIA with input matching network.

where $i_{n,R1}^2 = (4KT/R_1), i_{n,R2}^2 = (4KT/R_2,), i_{n,Rs}^2 = (4KT/R_s), i_{n,M1}^2 = 4KT\Gamma g_{d0,1}, i_{n,M2}^2 = 4KT\Gamma g_{d0,2}$. Substituting (26) into (28) and (27) into (29), we get

$$E_n^2 \approx \frac{4KT\left(\Gamma g_{d0,1} + \frac{1}{R_1}\right)}{g_{m1}^2(1 + g_{m2}R_2)^2} + \frac{4KT\left(\Gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2} \tag{30}$$

$$\begin{aligned} I_n^2 \approx{}& \frac{4KT}{R_1} + \frac{4KT}{R_s} + \frac{4KT\left(\Gamma g_{d0,1} + \frac{1}{R_1}\right)}{g_{m1}^2}\omega^2 C_j^2 \\ &+ \frac{4KT\left(\Gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2}\left(\frac{1}{R_s^2} + \omega^2 C_i^2\right) \end{aligned} \tag{31}$$

where C_i and C_j are the same as those in (1) and (23), $C_{\rm in} \approx C_i + (1 + g_{m2}R_2)C_j$. One can find that by substituting (30), (31) into (25), the derived equivalent input noise current spectral density contributed by the RGC input stage based on the $E_n - I_n$ model is essentially the same as the sum of items (I), (III), and (IV) of (23), disregarding the small difference that is due to the omission of the $E_n - I_n$ correlation in our analysis. Fig. 7 shows the noise model for the proposed TIA with input matching network. Based on preceding discussion, the correlated noise of E_{n1} and I_{n1} is only a small portion of the total noise. Therefore, we still assume E_{n1} and I_{n1} are uncorrelated for simplicity. According to (21) we have

$$|i_{n,\rm eq}|^2 = (1 - \omega^2 L_1 C_{\rm pd})^2 I_{n1}^2 + \omega^2 C_{\rm pd}^2 E_{n1}^2. \tag{32}$$

The noise reduction effect of L_1 is clearly demonstrated by (32). The effect of L_2 is similar to that of L_1. According to the analysis in the Appendix, the effective inductance of L_2 is $L_{2,\rm eff} = (L_2/1 + g_{m2}R_2)$, which is relatively small. The noise reduction effect of L_2 should be less than that of L_1. Based on

Fig. 7 and using the preceeding analysis method based on Fig. 6, we obtain

$$E_{n1}^2 \approx N_1^2 + N_2^2 \tag{33}$$

$$I_{n1}^2 \approx (1-\omega^2 L_{2,\text{eff}} C_\alpha)^2 \times \left(\omega^2 C_\beta^2 N_1^2 + \omega^2 C_{sb1}^2 N_2^2 + N_R^2\right) + \omega^2 C_\alpha^2 N_1^2 + \omega^2 C_{gs2}^2 N_2^2 \tag{34}$$

where

$$N_1^2 = \frac{4KT\left(\Gamma g_{d0,1} + \frac{1}{R_1}\right)}{g_{m1}^2 (1+g_{m2}R_2)^2}$$

$$N_2^2 = \frac{4KT\left(\Gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2}$$

$$N_R^2 = \frac{4KT}{R_1} + \frac{4KT}{R_s} + \frac{4KT\left(\Gamma g_{d0,2} + \frac{1}{R_2}\right)}{\left(g_{m2} + \frac{1}{R_2}\right)^2}\frac{1}{R_s^2}$$

$$C_\alpha \approx C_{gs2} + (1+g_{m2}R_2)C_{gd2}$$

$$C_\beta \approx (1+g_{m2}R_2)C_{gs1}.$$

Substituting (33) and (34) into (32), we can approximate the equivalent input noise current spectral density of our proposed TIA with input matching network as

$$|i_{n.\text{eq}}|^2 \approx \omega^2 C_{\text{pd}}^2 \left(N_1^2 + N_2^2\right) + (1-\omega^2 L_1 C_{\text{pd}})^2 \cdot \left\{ \begin{array}{l} (1-\omega^2 L_{2,\text{eff}} C_\alpha)^2 \left(\omega^2 C_\beta^2 N_1^2 + \omega^2 C_{sb1}^2 N_2^2 + N_R^2\right) \\ +\omega^2 C_\alpha^2 N_1^2 + \omega^2 C_{gs2}^2 N_2^2 \end{array} \right\}. \tag{35}$$

Fig. 8(a) shows the MATLAB calculated equivalent input noise current spectral density of the proposed TIA input stage. The calculation uses the same device parameters as the SpectreRF simulator does. In Fig. 8(a), curve a is based on (25), which is without any noise reduction effect; curve b is based on (35) with $L_1 = 0$, which shows the noise reduction effect with L_2 only; curve c is based on (21) with E_n and I_n expressed by (30) and (31), respectively, which shows the noise reduction effect with L_1 only; curve d is based on (35), which shows the noise reduction effect with L_1 and L_2. Within the bandwidth of interest, the noise could be reduced significantly. Intuitively, such kind of noise reduction effect is two-fold. On one hand, the inductor splits the large capacitive load to two smaller parts. On the other hand, according to (35) and curve d of Fig. 8(a), the noise decreases until it reaches a minimum level, after which it starts to increase. As illustrated by curve a of Fig. 8(a), the noise increases monotonically without the input matching network.

The noise simulation of the whole TIA circuit, carried out under Cadence SpectreRF with CHRT 0.18-μm 1.8-V RFCMOS technology, also confirms our mathematical evaluation. The simulation result is shown in Fig. 8(b). We can observe that, the simulated equivalent input noise current spectral density is dominated by flicker noise at low frequencies and

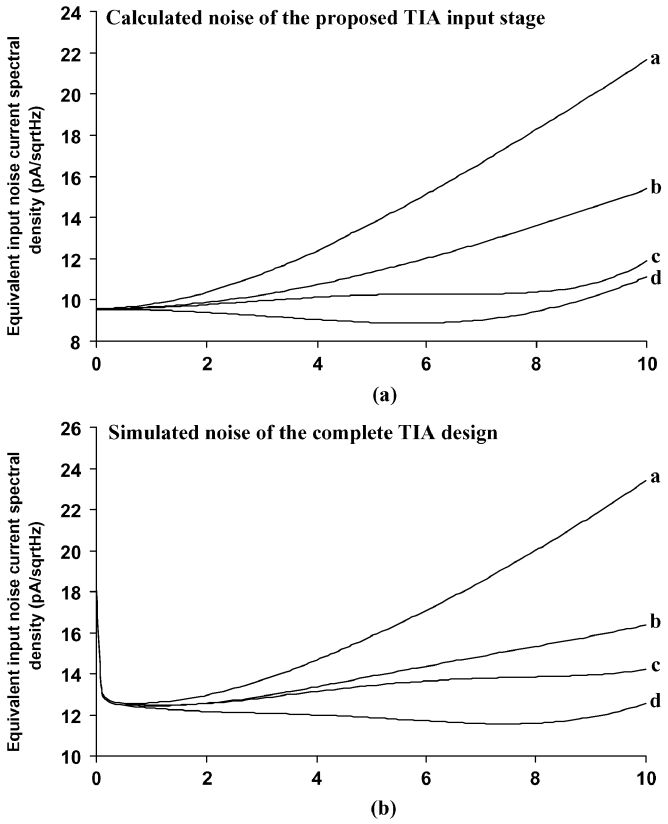

Fig. 8. (a) Calculated equivalent input noise current spectral density of the propose TIA input stage. (b) SpectreRF post-layout simulated equivalent input noise current spectral density of the complete TIA circuit. (Curve a: without noise reduction; curve b: noise reduction with L2 only; curve c: noise reduction with L1 only; curve d: noise reduction with L1 and L2).

as frequency increases it exhibits similar characteristic to that MATLAB-calculated equivalent input noise current spectral density shown in Fig. 8(a). Disregarding the flicker noise, the discrepancy between the calculated and the simulated results is mainly due to three reasons. Firstly, in our calculation we only consider the noise of the input stage while the simulation is based on the whole TIA circuit. Secondly, in our calculation we have neglected the correlated noises that is ususally a very small portion as mentioned previously. Finally, the inductors used in calculation are ideal. The first reason explains why there is roughly 2 pA/$\sqrt{\text{Hz}}$ difference between the calculated and the simulated results. According to curve a and curve d in Fig. 8(b), without noise reduction the simulated average input-referred noise current spectral density is about 18 pA/$\sqrt{\text{Hz}}$ and with noise reduction it is 12 pA/$\sqrt{\text{Hz}}$ in average. According to (20), this kind of noise reduction can improve the input sensitivity by more than 30% at a given BER requirement. Fig. 9 shows the post layout simulated eye diagram with 10-Gb/s $2^{31}-1$ pseudorandom binary sequence (PRBS). The transimpedance response simulation result is shown in Fig. 10. The simulated $-$3-dB bandwidth enhancement is from 2.2 GHz to 4.5 GHz by capacitive degeneration and to 9.1 GHz by broad-band matching network.

IV. Experimental Results

The proposed TIA design is implemented in CHRT 0.18-μm 1.8-V RFCMOS technology. Fig. 11 shows the chip micropho-

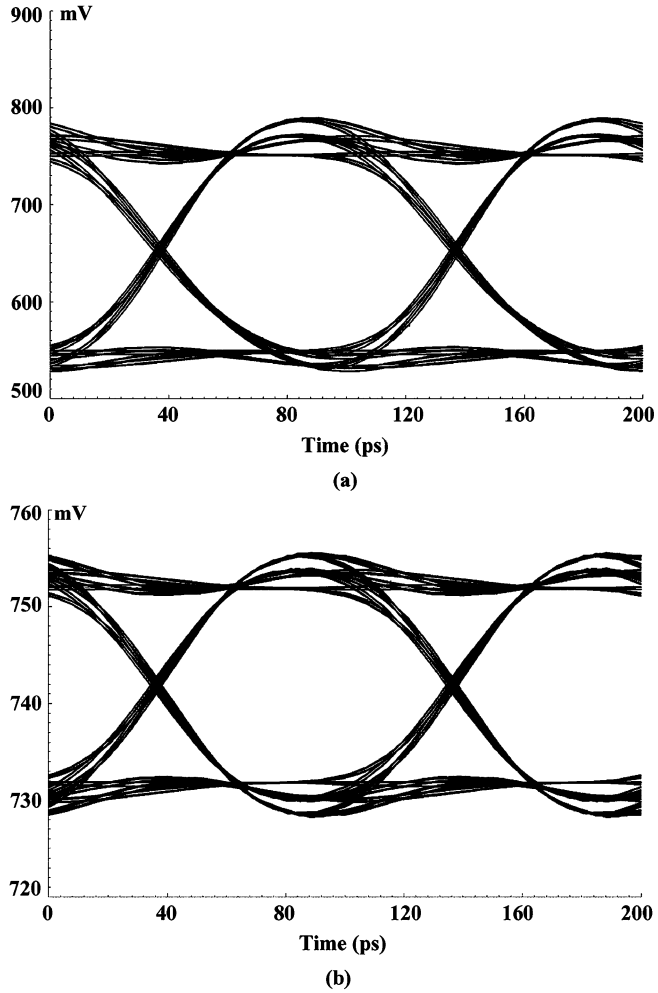

Fig. 9. Post-layout simulated eye diagram with (a) 500-μA peak–peak input current, (b) 50-μA peak–peak input current, both with 10-Gb/s $2^{31}-1$ PRBS.

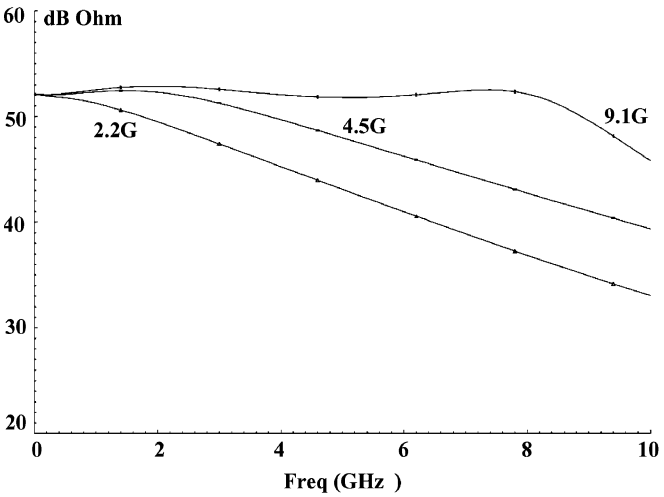

Fig. 10. Post-layout simulated transimpedance response: -3-dB bandwidth of 2.2 GHz for core TIA, 4.5 GHz for TIA with capacitive degeneration, 9.1 GHz for TIA with capacitive degeneration and broad-band matching network.

tograph of the proposed TIA. L_1 and L_2 are implemented using on-chip spiral inductors for the purpose of monolithic implementation and improving area efficiency. Because they are used

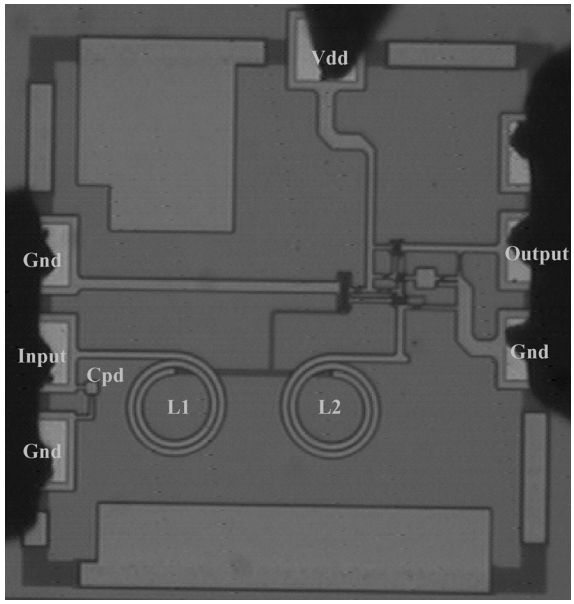

Fig. 11. Chip microphotograph of the proposed TIA design.

for series broad-band matching, their quality factors are not the primary issue [8]. An on-chip MIM capacitor $C_{\rm pd}$ of 0.25 pF is used to mimic the effect of the photodiode parasitic capacitance, and together with the parasitic capacitance of the input pad, the total input parasitic capacitance is about 0.35 pF. The frequency response is measured with a 8510C network analyzer. The transimpedance and group delay response of the proposed design are shown in Figs. 12 and 13, respectively. The transimpedance response exhibits a -3-dB bandwidth of about 8 GHz and 53-dBΩ transimpedance gain with very small gain ripple. Compared to the simulated result in Fig. 10, the low frequency gain matches well while at higher frequencies the measured gain drops faster than simulated, which is possibly due to the non-ideality of the inductors, the EM radiation loss, the silicon substrate loss and process variations. A good phase linearity is another important requirement for TIA design to limit the generation of data-dependent jitter [13]. The group delay is calculated from the measured phase response. From Fig. 13, we can observe that the group delay is about 80 ± 20 ps. The measured noise response is shown in Fig. 14. The average measured input-referred noise current spectral density is about 18 pA/$\sqrt{\rm Hz}$ up to 10 GHz and the total input-referred noise current is 1.6 μA integrated up to 8 GHz. The measured input-referred noise current spectral density is higher than the simulated one, possibly due to inaccurate noise model, additional parasitic elements and substrate noise/losses that are not considered in the simulation. However, the noise reduction effect is still noticeable from the measured data because over the bandwidth of interest the noise level is stable and does not increase with frequency. The whole chip size is 0.6×0.6 mm^2 including pads while the core circuit occupies only 0.45×0.25 mm^2 and dissipates 13.5-mW dc power from a single 1.8-V supply.

V. Conclusion

A novel bandwidth enhancement method for broad-band TIA design is proposed, which is based on a unique combination of capacitive degeneration, RGC input stage and broad-band

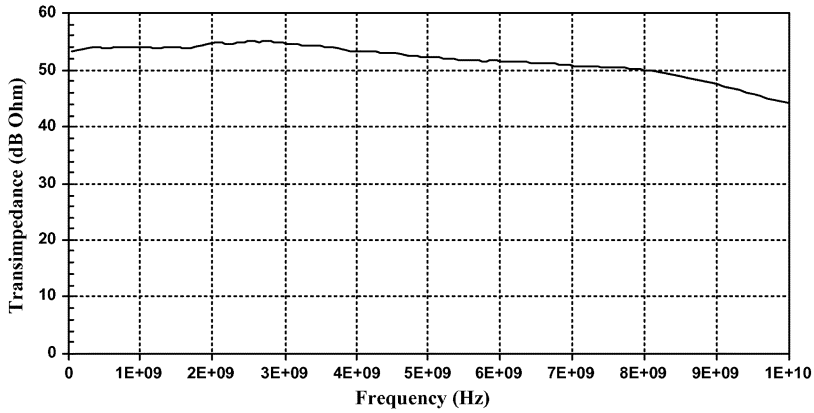

Fig. 12. Measured transimpedance response of the proposed TIA.

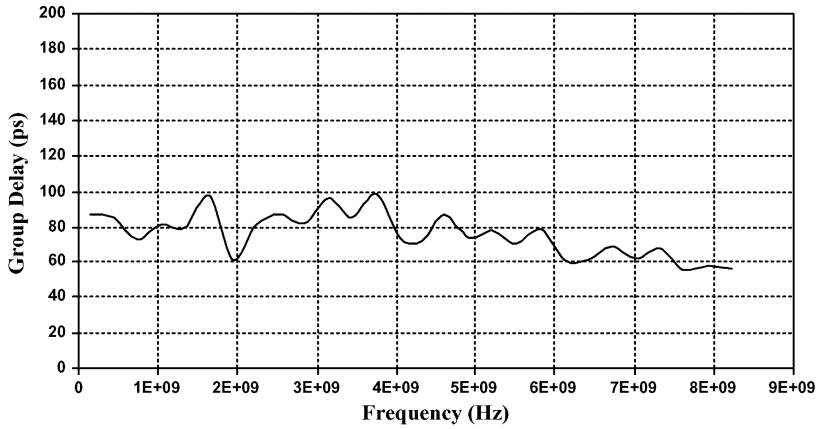

Fig. 13. Measured group delay response of the proposed TIA.

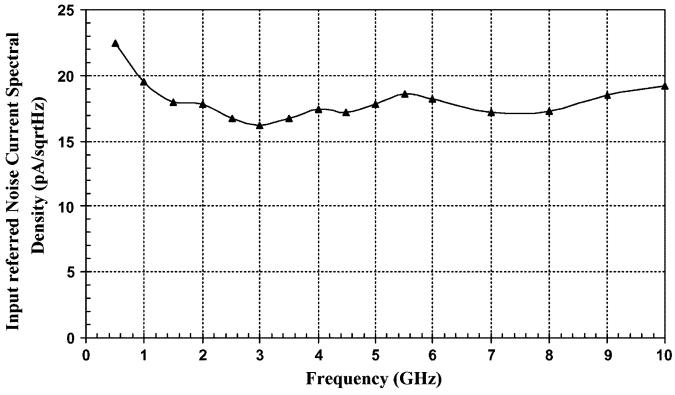

Fig. 14. Measured noise response of the proposed TIA.

TABLE I
PERFORMANCE COMPARISON OF 10-GB/S TIAS

Design	[19]	[11]	[10]	This Design
Technology	0.1μm pHEMT	0.25μm BiCMOS	0.18μm CMOS	0.18μm CMOS
Bandwidth (GHz)	8@0.25pF	9@0.1pF	9.2@0.5pF	8@0.25pF
Gain(dBΩ)	63.3	55	54	53
Power Consumption (mW)	500@5V single-ended	140@5V differential	130@2.5V single-ended	13.5@1.8V single-ended
Input-Referred Noise ($pA/\sqrt{Hz}$)	6.5	14	17	18
Chip Area (mm^2)	1.6×1.3	NA	0.8×0.8	0.45×0.25
Group Delay (ps)	±40	±10	±25	±20

matching network. The noise performance of the proposed TIA is discussed based on the equivalent input noise current expressed in terms of the $E_n - I_n$ pair, which could be used to evaluate the input-referred noise current of a given TIA with arbitrary input matching network. A prototype CMOS TIA is implemented based on the proposed broad-band design technique, which turns the TIA design to a problem of solving a fifth-order Butterworth low-pass filter. The overall bandwidth extension, based on measured data, is from 2.2 GHz to 8 GHz, which translates to an enhancement ratio of 3.6. Table I lists the performance comparison of four 10-Gb/s TIAs. This work achieves comparable performance to those III/V and SiGe counterparts while possessing the merits of the CMOS technology.

APPENDIX

Based on the small-signal equivalent circuit model in Fig. 4(b) and applying Kirchhoff's current law at node 3 and node 4 we obtain

$$Z_i \approx \frac{g_{m1}\left(1+s\frac{C_{gs1}}{g_{m1}}\right)sL_2+(1+sC_{gs1}R_2)\left(1+\frac{sL_2}{R_s}\right)}{g_{m1}(1+g_{m2}R_2)\left(1+s\frac{C_{gs1}}{g_{m1}}\right)+\frac{1}{R_s}(1+sC_{gs1}R_2)}. \tag{36}$$

As mentioned in Section III-A, R_s is a relatively large resistance and R_2 is a small one in this design, within the bandwidth of interest (below 10 GHz), it is reasonable to make following simplifications:

$$\begin{aligned} Z_i &\approx \frac{g_{m1}\left(1+s\frac{C_{gs1}}{g_{m1}}\right)sL_2+(1+sC_{gs1}R_2)\left(1+\frac{sL_2}{R_s}\right)}{g_{m1}(1+g_{m2}R_2)\left(1+s\frac{C_{gs1}}{g_{m1}}\right)} \\ &\approx \frac{sL_2}{1+g_{m2}R_2}+\frac{1+sC_{gs1}R_2}{g_{m1}(1+g_{m2}R_2)}\frac{1+\frac{sL_2}{R_s}}{1+s\frac{C_{gs1}}{g_{m1}}} \\ &\approx \frac{sL_2}{1+g_{m2}R_2}+\frac{1}{g_{m1}(1+g_{m2}R_2)}. \end{aligned} \tag{37}$$

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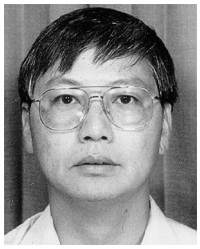

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Xueying Chen, photograph and biography not available at the time of publication.