Design and Analysis of Ultra-Broadband Distributed Power Amplifiers for Multi-platform Communications

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Table of Contents

Summary

The growth in wireless communication, the evolution of applications in smart mobile devices, the elimination of cord clutter from devices and different spectrum allocations around the world are calling for integration of multiple communication platforms in a single device. Implementing multiple narrow-band amplifier chips with corresponding matching networks and biasing circuitry to fulfill the requirements will be a complicated way. This indicates a need for ultra-broadband amplifier, which can operate over a wide range of frequency to eliminate various individual narrowband amplifiers. Moreover, one major trend in future applications is the increasing demand for more power over a very wide bandwidth. Hence, this thesis aims to analyze the necessities and develop a distributed power amplifier, which is often a constriction in the transmitter unit, for multi-platform systems.

First of all, some of the existing bandwidth enhancement techniques in the literature are reviewed and their advantage and disadvantages are examined with detailed studies on the distributed amplification technique. The review is extended to contemporary device technologies, thermal issue, equivalent circuit model, active cell configuration and biasing. State-of-the-art techniques used to improve the distributed power amplifier (DPA) performances are also summarized.

As the aim is to develop a broadband power amplifier, GaAs based hetero-junction bipolar transistor (HBT) is selected for this application. Poor thermal conductivity

and higher power dissipation inside the HBT make thermal characterization unavoidable. Both steady state and dynamic thermal behaviors are analyzed in detail. Modern high speed communication systems use OFDM and QAM signaling for high system capacity resulting in large peak to average signal envelope and thus, dynamic self-heating effect become an important issue for PA. The short-falls of current thermal models are addressed and a new model together with numerical technique capable of predicting highly fluctuating dynamic junction temperature of a power HBT is developed. The new model can cover thermal cutoff frequency range of up to 30MHz, with the modulated carrier frequency having the pulse width as short as 10ns and power levels of up to 10dB higher than the power dissipation under class-A operation of the HBT under consideration. The numerical technique which uses frequency domain dynamic thermal analysis is applicable for a wide range of signal types, power levels, frequencies, substrate position and material properties. A multi-section thermal network model is proposed and verified for incorporation into compact simulation software such as Agilent's Advance Design Systems for transient thermal simulation.

Unilateral model for the transistor is often used as a building block for DA design, particularly when design formulae are to be developed. The validity of using simplified and Miller's approximated unilateral model for the transistor in high frequency and high power amplifier is analyzed. It was found that the two unilateral models are not accurate enough and hence a modified unilateral model is introduced. The detail steps of parameter extractions for the modified transistor unilateral model are presented. The model is validated with measurement results at various biasing conditions; 3mA to 150mA collector currents with V_{cc} = 1V and V_{cc} = 5V. The model is able to accurately predict input reflection coefficient, forward transmission coefficient and output reflection coefficient of the transistor over 250MHz to 30GHz frequency range.

The developed transistor unilateral modeling is then used to derive close form de-

sign formulae for artificial transmission lines incorporating the transistor as gain unit. The formulae take into account all intrinsic and extrinsic elements of the transistor. Using these formulae a highly efficient DPA is designed and fabricated using WIN Semiconductors Corp's H02U-41 InGaP/GaAs HBT technology. For thermal stability every finger in the transistor cells is ballasted at the base. Dual-feed technique is applied for power added efficiency (PAE) improvement. The DPA is biased from 4V supply and achieved average output power of 28.5dBm over 2GHz to 6GHz. Average PAE across the pass band is better than 30% and the highest PAE is 43.5% at 3.5GHz. However, the gain of the amplifier is relatively low and driver stage amplifier would be needed. This would compromise the amplifier PAE performance. Hence, an analysis is carried for high gain DA. Specifically, collector line attenuation is carefully examined and a technique is developed to control the output impedance using external components. The concept is realized through cascode-configuration of the transistors. Using this technique, the relatively low output impedance of the HBT cascode cell is increased 3 times. As a result, the attenuation through the collector line is significantly reduced. The redesigned DPA incorporating this technique has small-signal and large signal gain of more than 20dB over 500MHz to 6GHz bandwidth and 17dB over 500MHz to 10GHz bandwidth with very good reflection coefficients. Without any other optimization techniques, significant PAE improvement can be observed for this 28.5dBm output power amplifier.

List of Figures

List of Tables

List of Notations

List of Abbreviations

DPA	Distributed Power Amplifier	v
GaAs	Gallium Arsenide	vi
dB	Decibel	vi
HBT	Hetero-junction Bipolar Transistor	vi
OFDM	Orthogonal Frequency Division Multiplexing	vi
QAM	Quadrature Amplitude Modulation	vi
PAE	Power Added Efficiency	vii
dBm	Power Ratio in Decibels, Referenced To One Miliwatt	vii
EW	Electronic Warfare	1
SWR	Standing-Wave-Ratio	2
RF	Radio Frequency	3
DA	Distributed Amplifier	4
FET	Field Effect Transistor	4
InGaP	Indium Gallium Phosphide	4
GaN	Gallium Nitride	28
HEMT	High Electron Mobility Transistor	4
pHEMT	Pseudomorphic High Electron Mobility Transistor	4
BiCMOS	Bipolar-Complementary Metal Oxide Semiconductor	4
AVG	Average	4
AlGaN	Aluminium Gallium Nitride	4
MMIC	Monolithic Microwave Integrated Circuit	4
BW	Bandwidth	4
PRF	Pulse Repetition Frequency	12
CW	Continuous Wave	12
MESFET	Metal-Semiconductor Field Effect Transistor	14
PAPR	Peak-to-Average Power Ratio	14
Q	Quality Factor	21
CSSDA	Cascaded Single-Stage Distributed Amplifier	24
TWM	Traveling Wave Matching	24
SiGe	Silicon Germanium	28
InP	Indium Phosphide	28
DCIV	DC Current-Voltage	28
GaN	Gallium Nitride	28

Si	Silicon	30
VBIC	Vertical Bipolar Inter-Company	30
HiCUM	High Current Model	30
MEXTRAM	Most Exquisite Transistor Model	30
CE	Common Emitter	37
CB	Common Base	37
OPEX	Operating Expenses	46
EVM	Error Vector Magnitude	60
WiMAX	Worldwide Inter-Operability for Microwave Access	60
FEM	Finite Element Method	61
SDD	Symbolically Defined Device	67
ADS	Advance Design System	67
CCDF	Cumulative Distribution Function	77
VNA	Vector Network Analyzer	96
DUT	Device Under Test	96
SOLT	Short-Open-Load-Thru	97
ISS	Impedance Standard Substrate	97
SGP	Spice Gummel-Poon	98
KCL	Kirchhoff's Current Law	124
HB	Harmonic Balance	171

Chapter 1

Introduction

1.1 General Back Ground

Broadband amplifiers have been firmly established in the fields of broadband microwave communication, high data rate optical communication, instrumentation, phase array radar, and electronic warfare (EW). As the name suggests these amplifiers have broad bandwidth over which the amplifier can provide constant output power. The bandwidth specification of these amplifiers is ranging from 5% of carrier frequency (e.g., multi-carrier wireless communication system) to multi-decade bandwidth (e.g., high-speed and high-capacity optical communication system). Ultra-broadband system is commonly assumed which has multi-octave to decade bandwidth properties. Increasing demands for transferring huge amount of data in multimedia communication, identifying targets in radar system with high precision as well as integrating different communication platforms in EW or multi-band wireless communication systems suggest the need for a multitude of critical enabling techniques have to be developed.

Various techniques have been developed in the past to achieve constant amplification over broader bandwidth. The bandwidth enhancing techniques common in

the literature are (1) the reactively matched circuit, (2) the feedback circuit, (3) the lossy match circuit and (4) the distributed circuit. Base on their properties, different techniques are well-suited to be implemented in different applications which require certain specifications that need to be addressed: gain, bandwidth, noise, stability and ports standing-wave-ratio (SWR).

In reactively matched circuit technique, the gain of the amplifier is compensated by selectively controlling reflections between the matching network and the active device using reactive components such as inductors (L) and capacitors (C). The bandwidth of a LC matching network is inversely proportional to its Q value and hence low-Q networks are generally cascaded to achieve broader bandwidth. In feedback circuit technique, a component which can be either a resistive, a reactive or an active component is used to feedback the signal from output of the amplifier to the input. This technique offers bandwidth enhancement in exchange of the gain. Stronger feedback is necessary to achieve broad bandwidth. In the case of lossy match technique, resistors are used at the input and output matching networks, with a corresponding loss in gain and noise figure. It has good input and output match over the desired bandwidth.

The distributed circuit technique is well established and immensely popular for the amplifiers which are required for achieving ultra-wide bandwidth properties [1–3]. The principle of this technique is to increase the gain-bandwidth product of an amplifier by spreading the junction capacitances of individual active device used while adding their trans-conductances constructively. The separated junction capacitances of the devices are absorbed into the formation of artificial transmission line. The two artificial lines, namely the base-line and collector-line, are designed to match the source and load impedance. These lines have a much higher cutoff frequency than the cutoff frequency of the amplifier where the same numbers of active devices are simply lumped together. The most desirable attributes of the distributed amplifier (DA) are the almost flat gain

and good terminal match. The gain of a DA can be increased by cascading more active devices [4, 5].

1.2 Motivation

Over the recent years, the growth in wireless communication and the evolution of applications found in today's mobile devices are pushing the need to integrate more communication platforms into a single device. Another factor in high demand for multi-band operation is the different spectrum allocations in different regions of the world. In addition, the electronic device manufactures are trying to integrate wireless technologies to their electronic devices to address unsatisfied customers over cord clutter and limited mobility. Hence, the interest in microwave techniques for communication systems has grown immensely. In the near future, the electronic devices, especially mobile units, will be utilizing wide range of communication platforms, which will be covering multi - octave bandwidth of 700MHz to 6GHz. This requires for the RF engineer to implement different RF front-end circuits in a single device, under the constraint of size, weight, cost, and performances. An RF front-end circuit is indeed a complex creature.

Integrating multiple narrow-band PA chips with corresponding matching networks is presented in [6, 7]. Switches are used to control the matching networks for the frequency band tuning. These implementations need multiple chips and very complicated biasing circuitry. Large amount of components are needed for the matching networks. This indicates a need for multifunction ultra - broadband RF system, which has ability to operate over a wide range of frequency and integrate different individual RF systems into a single one. A single broadband amplifier will be beneficial to reduce the size, weight and cost in conjunction with multi-platform RF front-end system.

DAs are appealing aspirants for broadband systems due to their inherently large bandwidth, flat gain, good noise figure, and good input/output matching over the mulit-octaves or decades bandwidth properties [8]. It also possesses comparative freedom from any tendency of self-oscillation. The failure of an active device in the amplifier merely results in a slight loss in gain [9]. This makes DAs more reliable for a system than other broadband circuit configurations. DAs have been widely and successfully implemented in low power applications [1, 10–12].

One major trend in wireless communication is the increasing demand for more power over a very wide bandwidth. For example, applications such as spread spectrum transmitter and indoor applications need 30dBm output power. The transmit power specifications for most commercial devices are in the range of 20dBm to 33dBm. For decades, realization of ultra-broadband power amplifiers has posed a significant challenge to RF design engineers. The output powers of several small transistors are combined to achieve higher output power in microwave frequency range. The conventional parallel power combining technique suffers from bandwidth limitation and requires the n-way power combiner. The distributed amplification technique offers simultaneous satisfaction of the bandwidth requirement and the power combining capability without the use of power combiners. The distributed amplifier theory does not inherently limit power and efficiency performances obtainable.

Table 1.1 shows the developed ultra-broadband amplifiers over one and a half decade for various applications. However, relatively smaller numbers of designs are intended for multi-octave bandwidth power amplifier applications. As there are various figure of merits that these designs targeted to achieve, the analysis is narrowed down to the designs which have the output power in the range of 15dBm to 40dBm, together with mulit-octave bandwidth over the frequency range of 0.5GHz to 20GHz, as shown in Fig. 1.1, for better comparative understanding in the region of interest.

Table 1.1: Summary of developed broadband amplifiers over 1997 - 2011.

Ref.No.	Device Technology	Gain (dB)	Pout (dBm)	PAE (%)	BW(GHz)	Topology	Cell Config.	Year
[13]	HBT	8	27	20 (AVG) 30 (Peak)	2 to 8	Distributed	CE	1997
[14]	GaAs HBT	9	33	>20	2 to 8	Distributed	Cascode	2000
[15]	GaAs MESFET, GaN HEMT	12	23	25	0.2 to 6	Resistive Feedback	-	2000
[16]	HEMT	7	30	20	4 to 19	Distributed, Uniform, Non-Uniform	CS	2001
[17]	InGaP HBT	7.5	-	-	23	Traveling Wave Matching	Cascode	2005
[18]	InGaP/GaAs HBT	15	-	-	41	Matrix Distributed 2 Stage Buffer	Cascode	2005
[19]	InGaP/GaAs	27	30	40	0.85 to 0.95	Reactive Matching	-	2005

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Table 1.1 – continued from previous page

Ref.No.	Device Technology	Gain (dB)	Pout (dBm)	PAE (%)	BW(GHz)	Topology	Cell Config.	Year
	HBT				1.71 to 1.95			
[20]	GaAs HEMT	12.5	-	-	DC to 50	Distributed	Cascode	2005
[21]	GaAs pHEMT	5-12	20	-	43	Distributed	Cascode	2005
[22]	GaAs pHEMT	15.3	20-23	-	4 to 37	Distributed Two Stages	CS	2005
[23]	GaAs HEMT	19.5	26	-	38	Distributed (W/Pre-Amp)	Cascode	2005
[2]	InGaP/GaAs HBT HBT	-	-	-	DC to 20	Distributed	Cascode	2006
[24]	MOSFET	13	30	23	0.1 to 0.6	Distributed Tapered	CE	2006
[12]	FET	10	18	24	0 to 4.5	Distributed, Tapered Tapered	-	2006
[3]	InP HBT	14	-	-	75	Distributed,	Cascode	2006

Continued on next page

Table 1.1 – continued from previous page

Ref.No.	Device Technology	Gain (dB)	Pout (dBm)	PAE (%)	BW(GHz)	Topology	Cell Config.	Year
						Inductive Peaking		
[25]	GaAs HBT	25	23.2	15	3.3 to 3.6	Reactive Matching	-	2006
[26]	GaAs HBT	18	22	-	DC to 3	Reactive matching	Darlington	2006
[27]	GaAs pHEMT	25	26	-	37 to 40	3 stage matching	-	2006
[28]	GaAs pHEMT	16.5	-	-	26 to 65	single stage DA, 3 Stage Cascaded	-	2006
[29]	HBT	24	27.4	46.5	0.1 to 0.6	Distributed (W/Pre-Amp)	Cascode	2007
[30]	GaAs HEMT	10	25.5	50-82	7 to 14	Class E, Reactive Matching	-	2007
[31]	GaAs HBT	23.5	22	15	5 to 6	Reactive Matching 2 Stage	-	2007
[32]	AlGaN/GaN HEMT	-	28	-	-	Distributed	Cascode	2008

Continued on next page

Table 1.1 – continued from previous page

Ref.No.	Device Technology	Gain (dB)	Pout (dBm)	PAE (%)	BW(GHz)	Topology	Cell Config.	Year
[33]	GaAs HBT	13	25	42(Peak)	2.4 to 6	-	Cascode	2008
[11]	BiCMOS	11	19	22.1	1 to 12	Distributed, Optimum Load, Inductive Peaking	Cascode	2009
[34]	GaAs HBT	18	-	-	23	2 Stage Differential Distributed	-	2009
[35]	GaN	-	41.5	28(Avg)	2 to 18	Distributed, Non-uniform	-	2010
[36]	GaAs HBT	10	19.6	25	2.3 to 2.7	Adaptive Current-draw Envelop-detection	-	2010
[37]	InGaP GaAs HBT	10	21	-	0.5 to 3	Distributed	CE	2010
[1]	GaAs HBT	8.1	13.9	21.9	1 to 12	Distributed, Optimum Load,	CE	2011

Continued on next page

Table 1.1 – continued from previous page

Ref.No.	Device Technology	Gain (dB)	Pout (dBm)	PAE (%)	BW(GHz)	Topology	Cell Config.	Year
						Tapered		
[10]	GaAs HEMT-HBT	8.5	8	-	DC to 43.5	Distributed, Inductive Peaking	Cascode	2011
[38]	GaN HEMT	20	38.5	-	0.2 to 3	Feedback	Cascode	2011

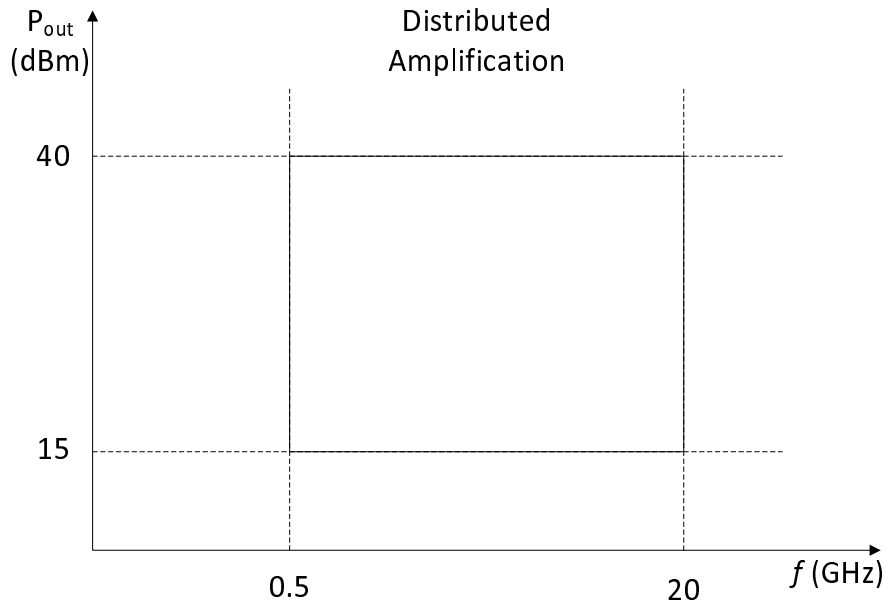


Figure 1.1: The region of interest for performances comparison of various distributed power amplifiers.

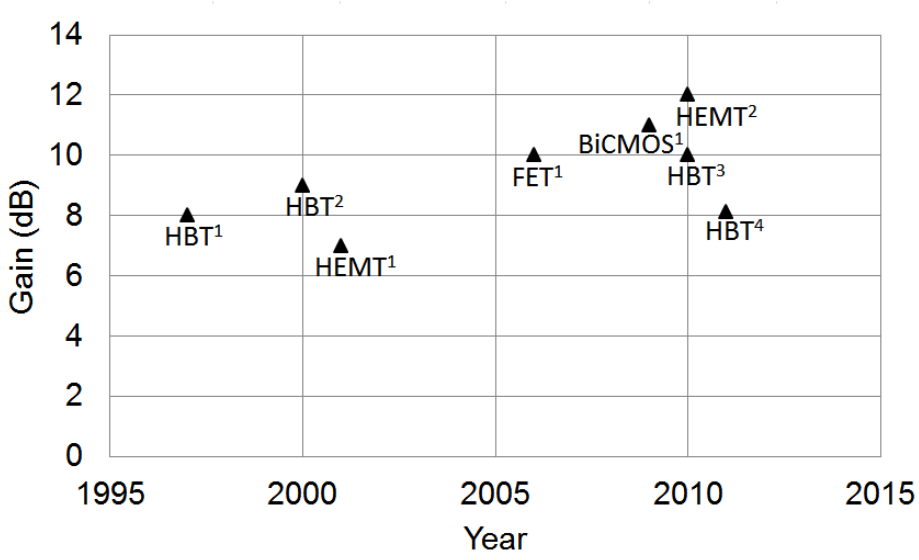


Figure 1.2: Gain improvement of distributed power amplifiers over the years for most commonly use MMIC technologies.

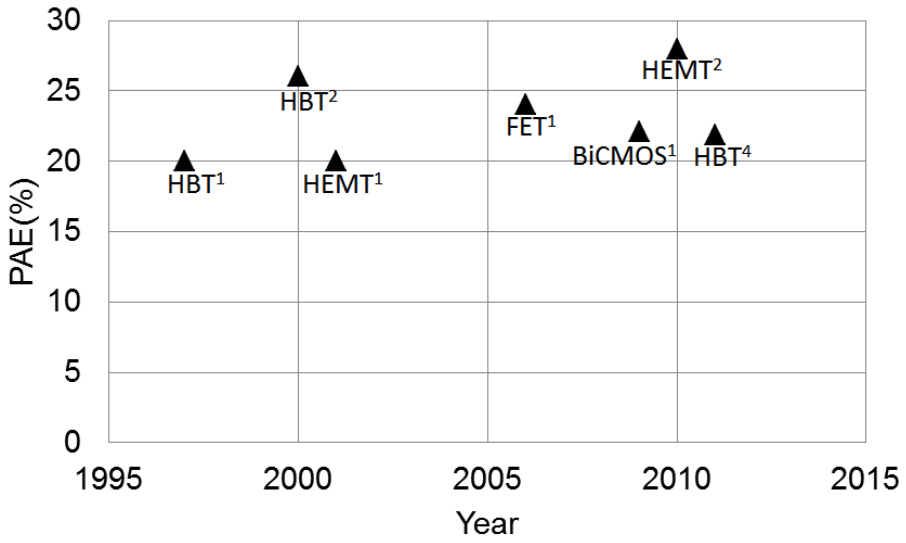


Figure 1.3: Associated PAE improvement of distributed power amplifiers over the years for most commonly use MMIC technologies (PAE information of HBT3 is not available).

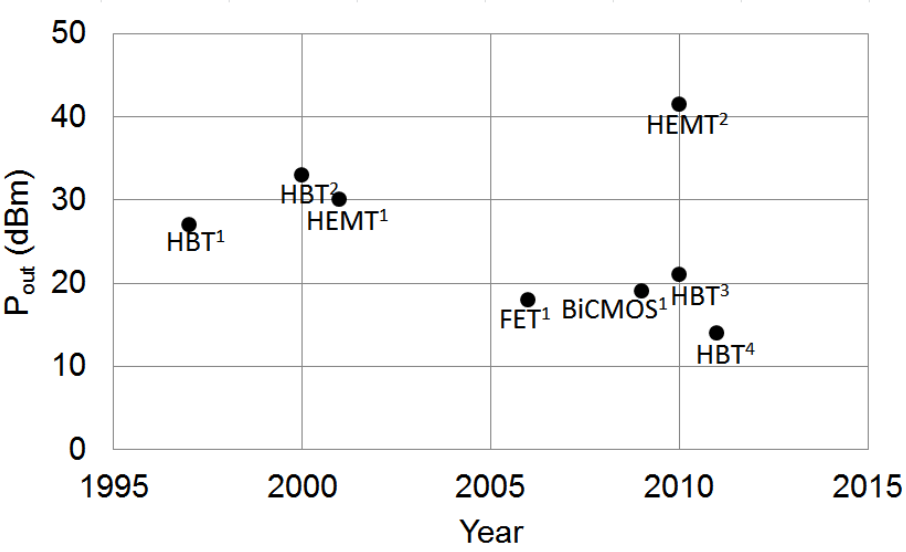


Figure 1.4: Associated output power of distributed power amplifiers over the years for most commonly use MMIC technologies.

References - HBT[1,2,3,4] are from [13], [14], [37] and [1] respectively, HEMT[1,2] are from [16] and [35], FET[1] is from [12], BICMOS[1] is from [11].

Figure 1.2, Fig. 1.3 and Fig. 1.4 show the gains, efficiencies and their respective output powers. Large signal performances of HBT[1] [13] and HBT[2] [14] are determined from pulsed RF measurements using 10us pulsed with pulse-repetition-frequency (PRF) of 10kHz from 8V supply. HEMT[1] [16] and HEMT[2] [35] performances are determined using large-signal continuous wave (CW). HBT[3] [37] power performances are determined using two-tone with varying spacing of 10MHz to 50MHz. [13], [14] and [16] designs are powered from 8V supply, mean while [35] is from 35V, [12] is from 3V, [11]and [37] are from 5V and [1] from 2V supply respectively. The summary shows that the gain, efficiency and output power over the last one and half decade do not have significant performance improvement. Most of the designs which have very high gain features in Table 1 used two stages DA or cascaded with pre-amplifier stage [22, 23] [28, 29] [34]. These imply that there are many challenges in designing high performance distributed power amplifiers (DPA). The major challenges are achieving higher output power and good efficiency while maintaining its linearity characteristic over the entire bandwidth.

Low gain characteristic is another undesirable property of DA technique. Moreover, the electro-thermal properties of major monolithic microwave integrated circuit (MMIC) technologies commonly used for power amplifier application like GaAs, also imposes limitations.

1.3 Objective

The objective of this work is to develop an ultra-broadband power amplifier using distributed amplification technique for multi-platform application. Despite the fact

that distributed technique is mainly employed in low power application, the developed distributed power amplifier (DPA) is expected to be capable of transmitting output power of 27dBm to 30dBm over 700MHz to 6GHz bandwidth. The nominal gain of most DAs [1, 11–14, 16, 35, 37] is about 10dB as shown in Figure 1 1. Higher gain is one of the most desirable features of an amplifier. The need for high gain in PAs will become apparent once we understand the overall efficiency specification of an amplifier. As the power added efficiency (PAE) accounts for the input RF power required for the amplifier, it can be clearly seen that higher power gain will return higher PAE. A technique for the gain improvement of a DA needs to be developed. Both small and large signal gain of 20dB or higher are targeted to achieve. The average PAEs over the entire bandwidth in state-of-the-art DPA designs are less than 25% [1, 11–13, 16]. Hence, the efficiency improvement is one of the primary objectives for this design. The average PAE of 30% or higher is anticipated.

Due to its high current gain and current density features, GaAs based HBT are preferred for DPA application. However, there are many limitations associated with GaAs based HBTs. First of all, input/output impedances of multi-fingers HBTs are very low. These cause higher losses in the input and output artificial transmission lines of a DPA circuit. The losses limit the number of active devices that can be cascaded in a DPA and limit the overall DPA gain. Hence, a circuit analysis has to be conducted, to counter the losses associated with the artificial transmission lines. For PA, the output network attenuation is more severe than the input side. Hence, this analysis will be especially focused on output networks. The large input capacitance characteristic of HBTs also makes the realization of input artificial transmission line difficult and also lowers the bandwidth achievable.

The collector-emitter breakdown voltage of a transistor determines the upper limit of the voltage swing that the device can deliver to a load; normally 50 Ohm. So, the

breakdown voltage imposes the second limitation for the DPA development. The breakdown voltages of GaAs based HBTs are lower than its counterpart MESFETs. Lower breakdown voltage makes the HBTs in ultra-broadband power amplifier hard to generate output power of 30dBm over a decade bandwidth. Hence, an alternative circuit topology like cascode configuration has to be investigated.

Another limitation is electro-thermal interaction. As the transistors are scaled into sub - micron size geometry and are operated with high current densities, electro-thermal effects are expected to be considered in the DPA designs. The device reliability and both DC and RF performances of a PA could significantly be degraded by electro-thermal effects. Poor thermal characteristics of GaAs demands more robust analyzes to protect thermal break down and to achieve thermally stable design. The designer also needs to make sure that the dynamic electro-thermal effects is considered properly as current and future communication systems prefer to use non-constant envelopes signal with very high peak-to-average-power-ratio (PAPR) (e.g., OFDM signal of WiFi). Hence, transient thermal behavior of the transistor used in the design should be accurately described and modeled.

Aside from the above limitations, design analyzes and formulae of DA are assumed to be heavily grounded on simplified unilateral model for simplicity. This assumption is valid for the ideal case and low frequency applications. However, as the frequency of operation and power of the signal being amplified by the amplifier increases, shunt feedback element of active device such as base-collector junction capacitance and series feedback element such as emitter resistance eventually become significant and important. Using Miller approximation is no longer sufficient and these feedback effects are needed to be included in the DPA design. Hence, a unilateral circuit model which is valid for high frequency and high current applications together with effects of terminal load factors need to be developed. Also, different active device technologies require

different configurations of implementation. The lack of real implementation oriented design formulae also present challenges to the development of high performance DPAs. In brief, the objective of this project is to develop techniques for the design of high gain and more efficient ultra-broadband PA.

1.4 Major Contribution of this Thesis

The first major contribution of this thesis is in analyzing dynamic thermal characteristic of GaAs HBT in frequency domain over 1kHz to 30MHz signal bandwidth. Dynamic thermal characteristics of GaAs HBT are analyzed and numerically simulated for single tone waveform, arbitrary periodic waveform, arbitrary aperiodic waveform and square pulse waveform signals. Validation of the analysis is also conducted by comparison of computed results with on-wafer measurement results. The results are used to develop a higher order thermal equivalent circuit for compact circuit simulator. The results of these findings are published in Author's Publications [1].

The second major contribution of this thesis is in the development of small-signal unilateral model which takes all bilateral model elements into account for precise prediction of the reflection coefficients and the transmission coefficient over the frequency range of 250MHz to 30GHz. More accurate equivalent output impedance network is introduced. This model overcomes the shortcoming of simplified unilateral model and Miller's approximated model used in design analyzes. A precise model parameter extraction procedure is developed for extraction of the transistor unilateral model from measured small signal S-parameters. The model is validated by comparison with measured S-parameters at various bias conditions. The results of these finding are published in Author's Publications [2].

The third major contribution of this thesis is in the analysis of artificial trans-

mission lines which incorporates HBT transistor. The analysis include the parasitic elements of the HBT hence allowing the designer to carry out performances analysis of the artificial lines which have far more complicated equivalent circuit compare to standard L and C representation. This also permits the designer to examine influential parasitic and to perform customized design.

The last major contribution of this thesis is in the analysis and development of a high-gain ultra-broadband DPA. Following the developed unilateral model, the elements which determine the output impedance characteristics of the HBT are carefully analyzed. Using the knowledge gained from this analysis, the output impedance of the cascode pair is systematically controlled using external components to obtain a high impedance value. This minimizes the attenuation and losses along the output artificial transmission line and significantly improves the amount of power deliver to the load. Together with careful biasing, both small-signal and large signal gains of the DPA could achieve 20dB or higher over multi-octave or decade bandwidth. For the same number of active device, this technique delivers very high gain and higher output power which in turn improves the PAE.

1.5 Thesis Organization

This thesis includes six chapters. Chapter one is introduction of this thesis; it includes the general background, motivation, objective, major contribution of this thesis and outline the structure of the thesis.

In Chapter 2, the literature study on the most commonly used bandwidth enhancement techniques for ultra-broadband amplifiers together with their advantage and disadvantages is presented. It is supplemented by reviews on related device technologies which are preferred for broadband applications and the strength of HBTs over

its contemporary technologies. The advantages and disadvantages of different HBT technologies and suitability of these technologies for various applications are discussed in detail. Then the short-falls of standard thermal model which is being integrated with most of the large-signal electro-thermal models are examined. The validness of using unilateral equivalent circuit in an analysis is also highlighted in the consecutive section. The circuit configuration, biasing and efficiency issues related to DPA are also studied. The state-of-the-art techniques used to improve the DPA performances are summarized in the final section.

In Chapter 3, the mechanism of heat generation and dissipation in a transistor is first analyzed. Then, the two dimensional heating behaviors in GaAs substrate are numerically analyzed for both steady state and in dynamic conditions. The dynamic thermal analysis are conducted in frequency domain for different types of time varying signals. A numerical technique which is able to predict the fluctuating characteristic of a power HBT's junction temperature, is presented. The technique is easily adaptable for a wide range of signal types, power levels, envelope frequencies, substrate position and material properties. The implementation of higher-order thermal equivalent circuit using Causar [39] canonical form for circuit simulation purpose is discussed in the final section of this chapter.

In Chapter 4, the detail steps of transistor model parameter extraction and small-signal modeling are presented. At first, the parameters for the bilateral hybrid-π model are extracted from S-parameters data which are measured at various bias conditions. This bilateral model development is followed by the validation using measured results. The importance of valid unilateral model for high frequencies and high power application is examined along with short-fall of the current simplified unilateral assumption and Miller's approximation. Then the analysis is extended to develop a modified unilateral circuit model for InGaP/GaAs HBT technology over 250MHz to 30GHz. The

modified model is validated with measurement and bilateral results.

In Chapter 5, the design parameters of artificial transmission lines used in DPA are analyzed and derived from the perspective of physical implementation requirements imposed by the active device technology and applications. Associated close form formulae are provided to determine amplitude and phase attenuation characteristics of the input and output line. Highly efficient dual feed distributed amplifier is designed and fabricated at a cost of terminal match and stability. As output impedance of HBT is low, output impedance analysis from Chapter 4 is extended to control the HBT's output impedance with the use of external components and cascode transistor configuration. The output impedance of the cascode cell is systematically configured to the higher impedance region to minimize the attenuation along collector line. The small-signal performances (e.g., reflection and transmission coefficients) and large-signal power performances (e.g., gain, output power and PAE) of high-gain decade bandwidth DPA designs are discussed.

In Chapter 6, the achievements of this thesis are concluded and the suggestions for achieving further power and efficiency improvement are discussed. Future works in these areas are also proposed.

Chapter 2

Literature Review on Broadband Power Amplifier

2.1 Introduction

Amplifier can be classified into two broad categories, namely broadband and narrow band, depending on the bandwidth over which it can provide constant output power. The distinction between the narrow band and broad band classification has become increasingly unclear with the deployment of highly tuned narrowband amplifier with the bandwidth of less than 1% of the center frequency. This has led to claims of power amplifiers with 10% bandwidth as relatively broadband power amplifiers. Since, this work is looking at the power amplifiers with multi-octave or decade bandwidth, the term broadband amplifiers will be used for the amplifiers which have a bandwidth of two octaves or more.

2.2 Bandwidth Enhancement Techniques

Various techniques have been developed for the broadband amplifiers in the past. The most popular and well established bandwidth enhancement techniques employed in the hybrid and the monolithic technologies are

1. Reactively matched circuit,
2. Feedback circuit,
3. Lossy matched circuit and
4. Distributed circuit.

2.2.1 Reactively Matched

In this technique, the gain compensation is accomplished by selectively controlling reflections between the matching network and the active device. The reactive components such as inductor (L) and capacitor (C) are used for impedance transformation. A single section low-pass LC circuit is one of the simplest matching networks. It can realize a perfect impedance transformation at a single frequency and has good match over a certain bandwidth. However, it doesn't have much control over the bandwidth. The quality factor (Q) of a matching network determines the bandwidth achievable and it is inversely proportional to the bandwidth of the network. Hence, low Q networks are generally cascaded to achieve broader bandwidth. Figure 2.1 shows the multi-section reactive matching networks. Each network of this multi-sections design has lower impedance transformation ratio. By distributing the impedance transformation ratio equally among the N-sections, the intermediate impedances can be decided. As matching networks are constructed exclusively using reactive components, maximum gain, minimum noise figure and maximum power output are possible to achieve. The reactively matched ultra - broadband PAs are presented in [40] and [41]. How-

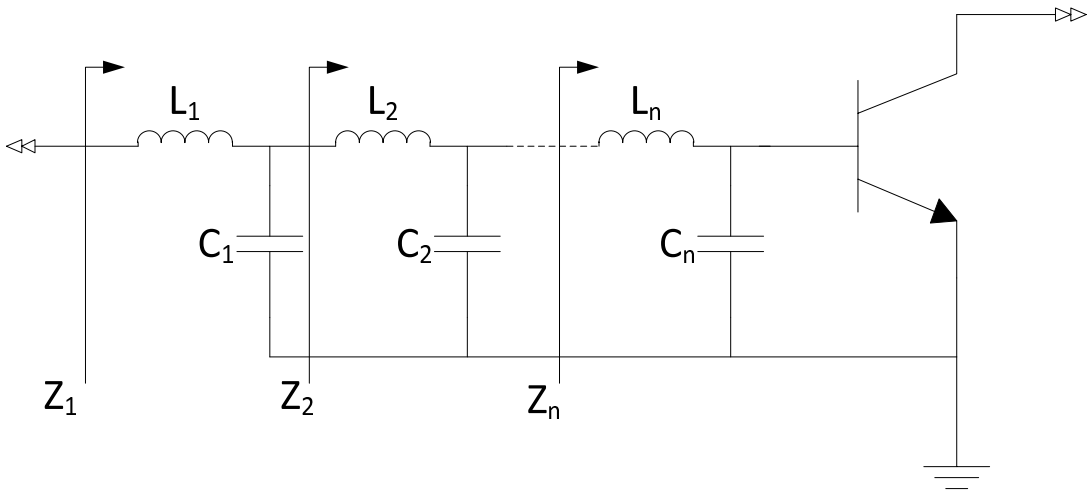


Figure 2.1: Multi-sections matching network using reactive components.

ever, the disadvantages of this technique are poor impedance match over multi-octave or decade bandwidth and the overall size of the amplifier module [4].

2.2.2 Feedback Amplifier

In this technique, the signal from the output of an amplifier is fed back to the input using resistive, reactive or active component. Multi-octave bandwidth is realizable with a single active device [42, 43]. This technique offers the bandwidth enhancement in exchange of the gain. Two basic feedback configurations most commonly see in the literature are shown in Fig. 2.2. Sometimes more than one feedback topology can be applied to take full advantage of the benefits of the feedback. This technique offers less complex circuit, higher PAE then distributed amplifier, flat gain, very good input and output matching. The main disadvantages of this technique are the lossy characteristic of feedback network which erode significant amount of available output power and sensitive to self-oscillation.

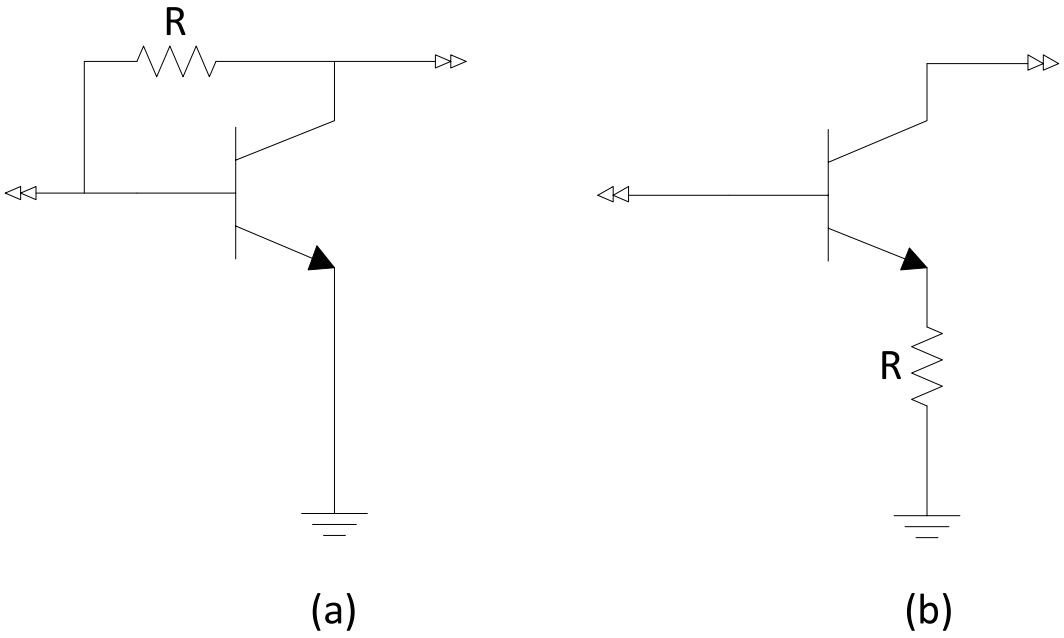


Figure 2.2: Shunt-shunt and series-series resistive feedback configurations.

2.2.3 Lossy Matched Amplifier

In this technique, resistors are used for implementing the matching network which provides the gain equalization. It possesses good input and output match over the desire bandwidth. The lossy matched amplifier provides the broad bandwidth performance at the expense of low gain, low output power and poor PAE [44,45]. The lossy matching technique is normally avoided at the output for achieving best efficiency and output power. Figure 2.3 shows some configurations of lossy matching network.

2.2.4 Distributed Amplifier

Among the broadband amplifier techniques, the distributed amplifier (DA) is a well-established technique [11, 13, 14, 46]. The flat gain and the good terminal match are

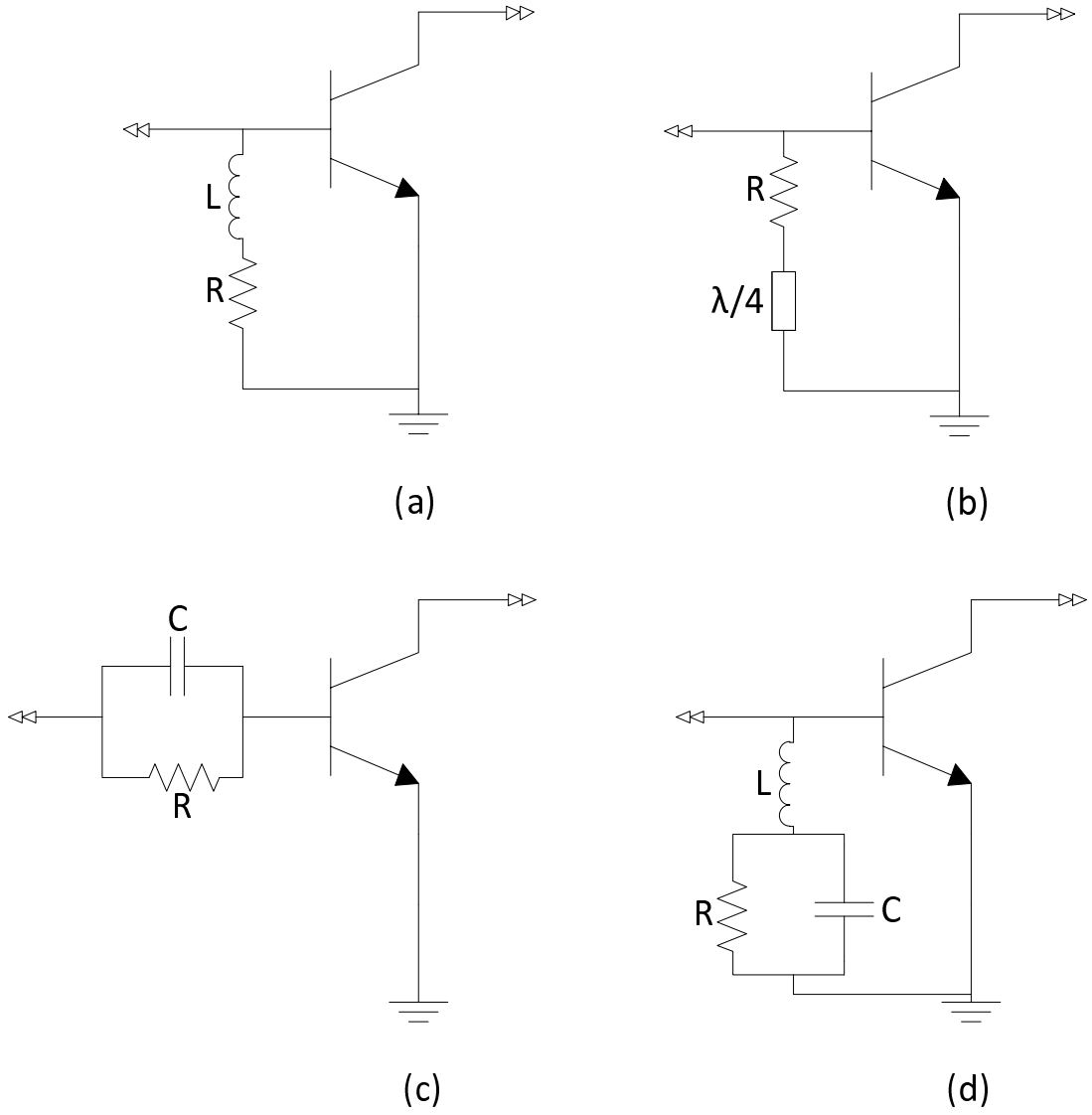


Figure 2.3: AC circuit schematics of some lossy matched configurations.

the most desirable attributes of this technique. It also allows tuning over multi-octave bandwidths. Theoretically, a DA gain can be increased by adding more stages. It also offers more options for the design of input and output matching networks than

a single stage amplifier. It possesses comparative freedom from any tendency of self-oscillation. The failure of an active device in the amplifier merely results in a slight loss in gain [9]. This makes DAs more reliable for a system than other broadband circuit configurations. So, DAs are appealing aspirants for broadband systems due to their inherently good attributes. Figure 2.4 shows the simplified schematic of the DA topology.

Some of other techniques available in the literature are cascaded single-stage distributed amplifier (CSSDA) [4], traveling wave matching (TWM) structure [17] and frequency doubler with resistive feedback [15].

2.3 Distributed Power Amplifier

One major trend in the wireless communication is the increasing demand for more power over a very wide bandwidth. Most of the broadband designs are aimed for low power applications. However, some applications such as the spread spectrum transmitter, the multi-platform communications system and the indoor localization applications need 30dBm of output power. For decades, the realization of ultra-broadband power amplifiers has posed a significant challenge to RF design engineers.

The distributed amplification technique offers simultaneous satisfaction of the bandwidth requirement and the power combining capability without the use of additional power combining networks. Also, DA theory does not inherently limit the power and the efficiency performances obtainable. However, there are many challenges in designing distributed power amplifiers (DPA). The major challenges most commonly referred in the literature are achieving high output power and efficiency while maintaining its linearity characteristic over multi-octave or decade bandwidth. The low gain characteristic is another undesirable property.

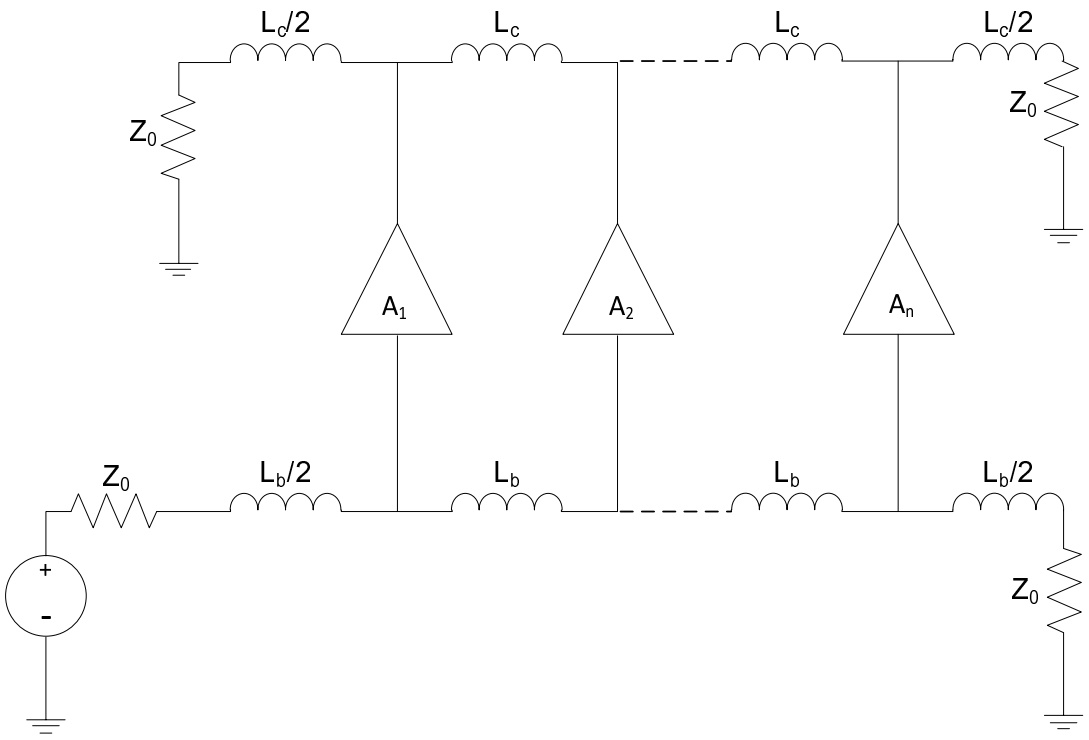


Figure 2.4: Simplified schematic of distributed amplifier topology.

As it is making use of the active device's input/output impedances, the DPA performances are limited by the characteristics of the active components. Several power and efficiency limiting mechanisms can be identified for a DPA design. The requirement of larger periphery for achieving higher output power lowers the terminal impedance of the active device. It presents difficulty for matching networks design, introduces higher attenuation and limits the bandwidth achievable. Low gain, low output power and poor efficiency are the consequences. In addition, the frequency-dependent power behavior of the active devices makes the non-uniform power generation over the band width. Hence, the power and efficiency vary significantly over bandwidth.

Another limitation comes from the configuration of the DA design itself. The dumping load terminated at the end of input and output lines absorb the available

power significantly in conventional DA design. On the other hand, the termination must be provided for at least gain flatness and matching, as well as for stability considerations [4]. These facts pointed out that, complex optimization techniques are needed to achieve high gain and efficient broadband DPA.

2.4 Devices Technologies

The characteristics of the active devices used in the DPA limit the overall performances and active device technologies play an important role. All technologies have their pros and cons and are desirable for different applications. Vacuum tube-valve technology is utilized to implement the first DA formulated by William S. Percival in 1936 [47]. DA technique has evolved together with the junction transistor technology. The advancement in FET technology in particular the MESFET escaladed the development of DAs in hybrid technology initially. Starting from 1980's, DA are developed using advance devices technologies based on monolithic microwave integrated circuits (MMIC) and are currently still widely used in many applications [4]. They offer low loss, improved reliabilities, small size, light weight and circuit design flexibility. MMICs are relatively easy to design and simulate. During the last decade, GaAs based hetero-junction bipolar transistor (HBT) and high electron mobility transistors (HEMT) are widely used for broadband applications.

2.4.1 Hetero-junction Bipolar Transistor (HBT)

HBTs have many advantages over HEMTs [48–50]. First, HBTs have higher transconductance, generally 10 - 100 times depending on the output current. This is result of the exponential relation between the output current and the input voltage of the bipolar transistor (BJT). It is much larger than the quadratic or the linear character-

istic resulting from the indirect modulation of charge carriers through a depletion or intervening layer between the gate and the active channel of a FET.

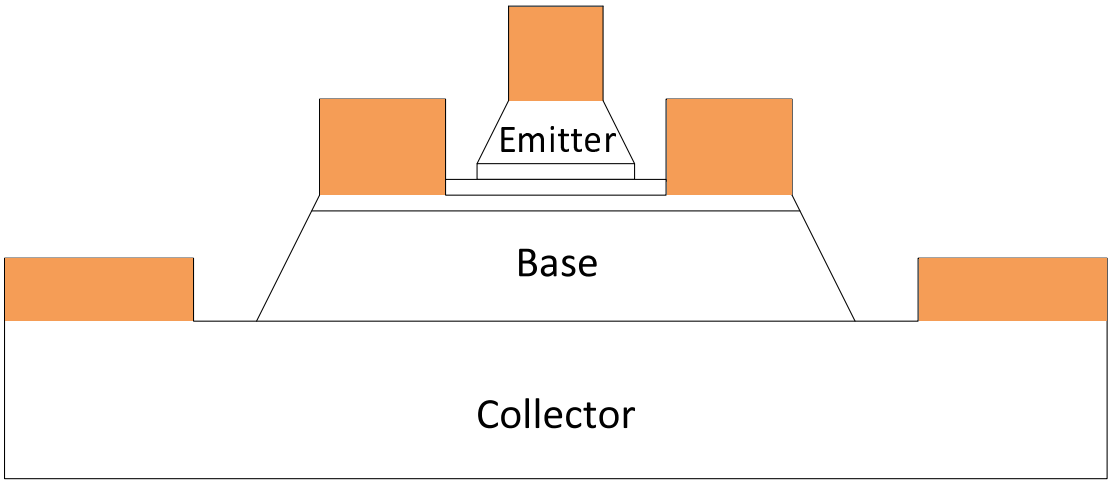


Figure 2.5: Un-scaled cross section schematic of hetero-junction bipolar transistor (HBT).

Second, the HBT has lower output conductance, especially in the case of common emitter configuration, as a result of the highly doped base. This minimizes the base width modulation and the variation of the collector current with collector-emitter voltage. In FETs, the output conductance is governed by the surface and active channel-substrate leakage together with trapping effects leading to frequency-dependent characteristics, which is undesirable for high-accuracy analog applications. The HBT's low also yields high linearity and dc voltage gain, which are important parameters for analog applications.

Third, HBT has less trapping effects and lower $1/f$ noise as a result of carrier flow primarily through active junctions isolated from surfaces and substrate interfaces. In FET, as the carriers travel between the surface and active channel-substrate interfaces, they experience greater trapping effects. Finally, HBT offers higher cur-

rent per effective transistor area than the MESFET or HEMT. This arises from the vertical structure of HBT, shown in Fig. 2.5, compared to the lateral structure of FET. The entire emitter area contributes to the current rather than a thin channel in the FET. The result is a higher current handling capability per effective transistor area which turned out as one of a preferable characteristic for power applications. In addition, HBT permits breakdown voltages to be tailored for optimized power performance [51, 52].

2.4.2 GaAs HBTs

Advantages such as low harmonic distortion, exponential voltage-current transfer function, low $1/f$ noise, and high-efficiency output power capabilities of HBT technologies are receiving increasing attention. The well-developed and popular HBT technologies are based on GaAs, SiGe and InP. The performances of HBTs which are fabricated using these technologies are compared and analyzed in [52], under the same conditions. The DCIV analysis reveals that GaAs HBT has higher collector to emitter breakdown voltage than the other two and the SiGe HBT has the lowest. At the optimum bias condition for class-A, GaAs HBT consumes lowest power among the three and the SiGe HBT consumes the highest. However, SiGe HBT offers higher output power than the others and the InP provide lowest power output. Frequency related merit testing shows that InP HBT can give the highest frequency of oscillation and the SiGe gives the lowest. From noise figure point of view, SiGe HBT has the lowest noise level and the GaAs has the highest. InP technology suffers from higher cost, while GaAs and SiGe technologies offer low cost and high yield.

Another very promising technology is Gallium Nitride (GaN). GaN is a very hard and wide bandgap semiconductor material. GaN possess high heat capacity and ther-

mal conductivity compare to GaAs, and hence can handle higher temperature. Larger band gap means higher breakdown voltages for a transistors [53]. It can be an ideal candidate for high-power, high-temperature and high-frequency microwave applications, such as power amplifiers for high-speed wireless data transmission, high-voltage switching devices for power grids, and high power microwave source for microwave ovens. Nanotubes of GaN are proposed for applications in nanoscale electronics, optoelectronics and biochemical-sensing applications [54].

Although the benefits of these materials are significant, they are not as technologically mature as Si and GaAs. Si and GaAs can easily be grown and their transport characteristics are very well known. GaN families, are relatively much more difficult to grow and process into devices. For this reason, they are not nearly as well studied as Si and GaAs [**?**]. Substrates for GaN are either silicon carbide, sapphire, or silicon. Expensive alchemy is needed to align the GaN crystal onto these mismatched substrates. The main problem with GaN technology is cost. A special process is required to grow a GaN crystal or wafer on which transistor s and integrated circuits (ICs) can be fabricated [55].

After compromising different figure of merits, [52] concludes that GaAs HBT is the stronger technology for power applications. Meanwhile, SiGe HBT is suitable for low noise application and InP HBT will be the best choice for high speed applications. GaAs technology is more mature than other HBT technologies and is ideal for the combined microwave and digital functions since the same epitaxial structure facilitates the microwave and digital performances [51].

2.5 Thermal Properties of GaAs and Thermal Protection in HBT

GaAs HBTs are preferred for power applications and have attained enough maturity as RF power devices due to their intrinsic high power density. However, GaAs has lower thermal conductivity (55 W/m^{o}C) compare to the standard technologies such as Si. As the transistors are scaled into sub-micron size geometry and are operated with high current densities, thermal effect plays an important role. The junction temperature (T_j) of a HBT depends not only on the temperature of its environment but also on the heat generated inside it. This phenomenon is called self-heating effect. The current gain (β_i) fall-off and the collapse in DCIV characteristics are the significant consequences of self-heating effect [50]. The device reliability and both DC and RF performances of a PA are significantly degraded because of self-heating effect. Therefore, thermal behavior of the HBT must be accurately described and modeled as the accurate models will help to save valuable resource such as cost and time. Self-heating effect in HBT has been extensively analyzed and equivalent circuit models have been developed. The first order thermal equivalent circuit which includes a resistor and a capacitor is the most commonly used model. This model has low-pass behavior. The model is being integrated with the standard bipolar compact models such as VBIC, HiCUM, MEXTRAM, and Agilent HBT [50, 56–58].

The mutual heating among fingers of power HBTs is also analyzed and modeled using thermal resistance matrix [59]. Under steady state condition, the first order model predicts the junction temperature accurately. However, the model will have limited accuracy when predicting dynamic junction temperature of a HBT induced by the signal components which lies above thermal cutoff frequency of the first order circuit.

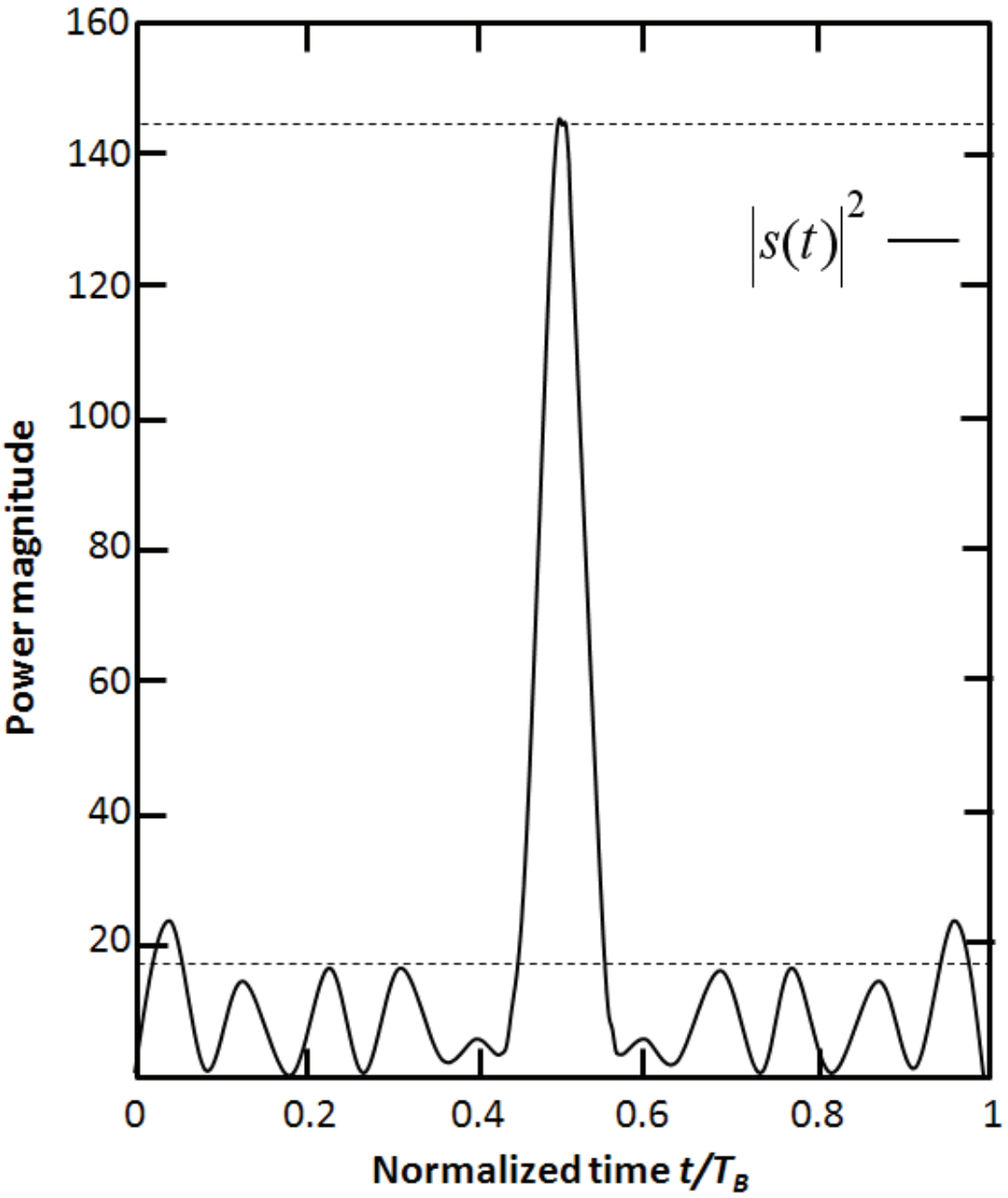


Figure 2.6: The instantaneous signal power of OFDM signal with 16 carriers without amplitude modulation.

Modern high speed communication systems use spectrally efficient multi-carrier technique like orthogonal frequency division multiplexing (OFDM) and quadrature

amplitude modulation (QAM). Figure 2.6 shows the peak to average power ratio (PAPR) of OFDM signal which is using 16 carriers. Very high peaks generated from these systems can cause significant junction temperature excursion from the average power level and hence resulting in nonlinear current gain that is highly depend on the magnitude of the adjacent symbol envelope. The signal envelope is complex and the power waveform contains various baseband components which could lie below the thermal cutoff frequency defined by the standard first order thermal circuit.

Electro-thermal response under this circumstance is un-detectable for first order thermal circuit. There is a need for a compact simulation model which is capable of capturing the fluctuating thermal characteristic due to short duration large-signal dynamics of multi-carrier systems, especially for the simulation and optimization of PA.

2.5.1 Thermal Protection

The collapse of current gain is a very significant phenomenon in vulnerable multi-fingers power HBTs. When the transistor is operating at high power levels, the junction temperature elevates and one of the fingers may become hotter than the others. This results in current crowding towards the hotter finger and causes a sudden decrease in total current gain. Ballasting at the base or emitter of the transistor can protect against current collapse. Emitter ballasting is a popular technique. However, it degrades the collector efficiency and is not preferred for PA [5].

Base ballast resistor resides outside the collector current path. This gives simultaneous thermal stability and better large signal performance for PA. At a given collector current (I_c), temperature (T) and constant base emitter voltage (V_{bej}), the minimum emitter ballast resistance required for thermally stable conditions can be calculated

as [60] and the equivalent resistance for base ballasting can be modified as,

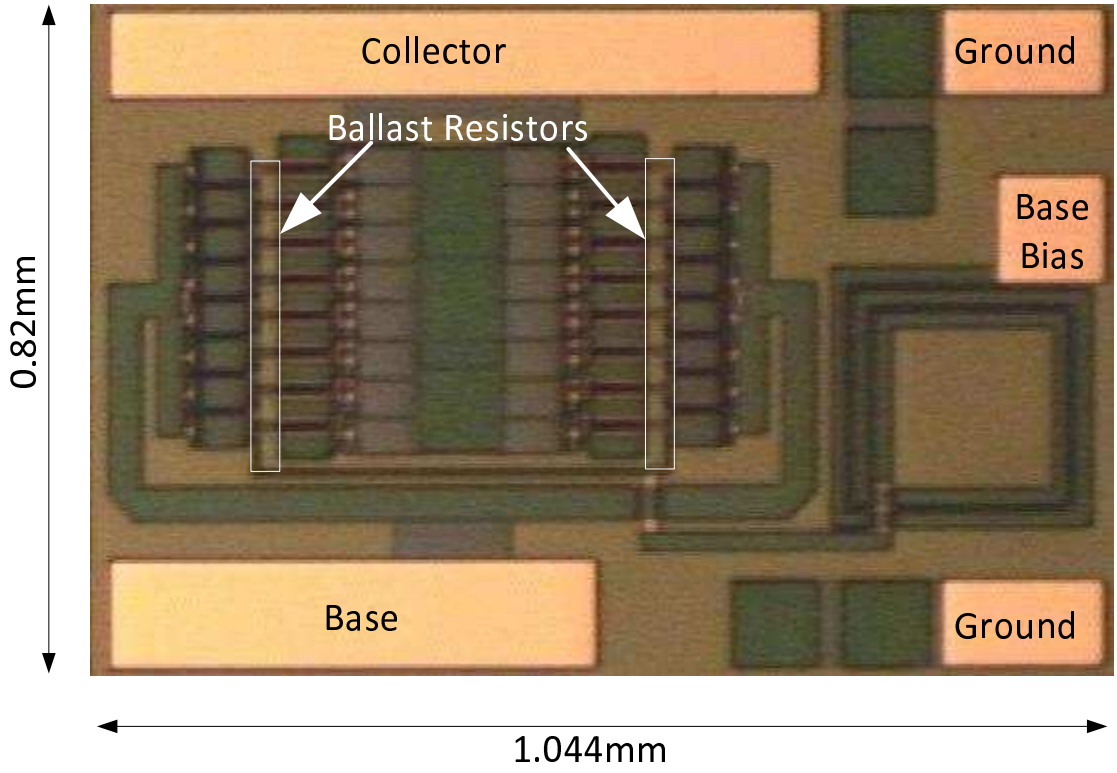


Figure 2.7: Base ballasted multi-fingers power HBTs for thermal protection.

$$R_b \geq \beta_i \mathrm{R}_e = \beta_i \left(R_{th} V_{ce} \frac{V_g - V_{bej}}{T} - \frac{kT}{qI_c} \right). \tag{2.1}$$

Figure 2.7 shows the base ballasted multi-fingers power HBTs and the resistances are computed according to (2.1).

2.6 Small-Signal Equivalent Circuit Models

Amplifier can be classified into two broad categories, namely broadband and narrow band, depending on the bandwidth over which it can provide constant output power.

HBTs have been adopted as active devices in MMICs. Using accurate equivalent-circuit model is essential for analyzing and simulating circuit performances. Bilateral equivalent circuit models are extensively used for circuit simulation in various design processes. Some applications such as distortion analysis [61,62], non-linearity analysis [63–65], distributed amplifier design [29,61] and others [66,67], use simplified unilateral models.

Figure 2.8 shows the small-signal bilateral model and Fig. 2.9 shows the simplified unilateral model schematics. The feedback elements of the transistor are assumed to be very small and are simply neglected in the simplified unilateral model. This assumption may be invalid in the cases of large voltage gain, high operating frequency and high power transistors. The base-collector feedback capacitance of a HBT changes the input impedance when the voltage gain of the transistor is high. A common technique used to compensate the feedback capacitance effect is the Miller approximation. Figure 2.10 shows a small-signal unilateral schematic modified by applying Miller approximation. However, Miller approximation is only useful for calculating forward transmission parameters and input impedance of HBT. It is useless for calculating output impedance [68, 69] which is necessary for valid performance analyzes of the PA.

High operating frequency is also an issue related to capacitive feedback elements to be taken care of. At low operating frequency, the reactance of the feedback capacitance is large enough to isolate the input (base) and output (collector) ports and hence, the unilateral assumption is valid. However, the reactance of the feedback capacitance is insufficient to decouple input and output ports at higher operating frequency and the simplified unilateral assumption becomes invalid. Hence, the operating frequency should be taken into account when one needs to apply unilateral assumption.

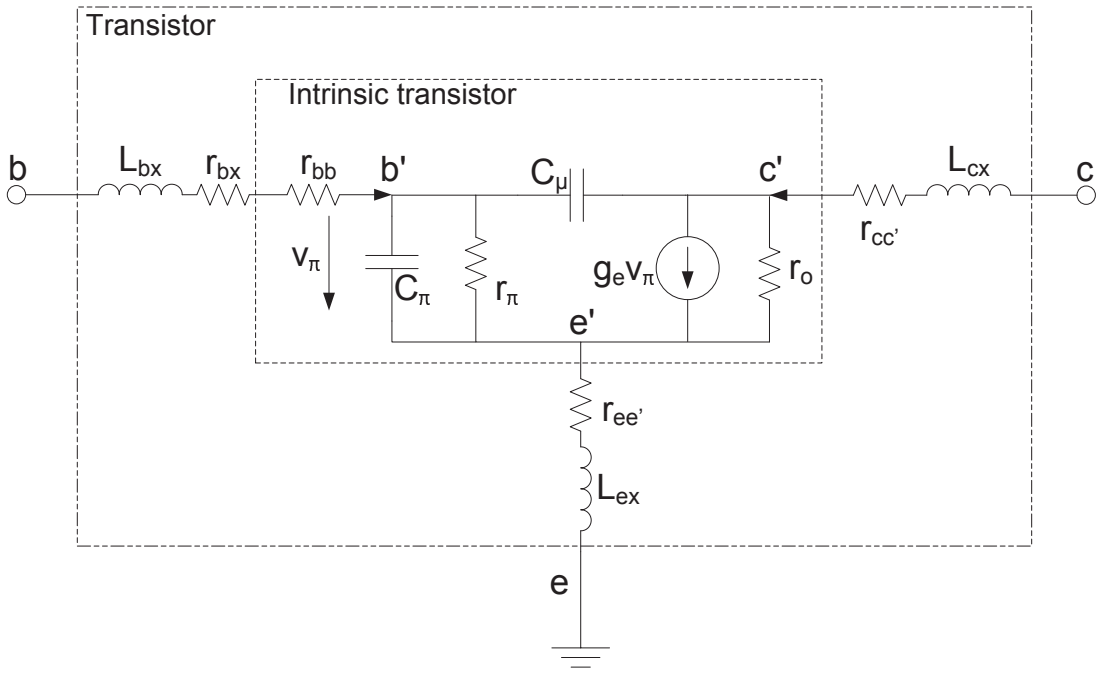


Figure 2.8: Bilateral small-signal equivalent circuit model for HBT.

The same analogy goes for the series feedback element such as emitter resistance. For low power applications, the current flowing through the emitter resistance is small and the voltage drop across the resistor is insignificant compare to the input bias voltage. With the large current flow in high power transistors, this voltage may be significant. Hence, the series feedback effect introduced by emitter resistance is not negligible in power applications.

In reality, all devices will be terminated with specific impedances at the input and output ports. Simplified unilateral model simply neglect the terminated impedance at the ports. In the Miller approximation, the output port is loaded with an impedance [68], 50Ω is commonly used for high frequency analysis, and terminal impedance effect is being considered in terms of voltage gain parameter. However, the terminated impedance at the input port is not considered in the approximation.

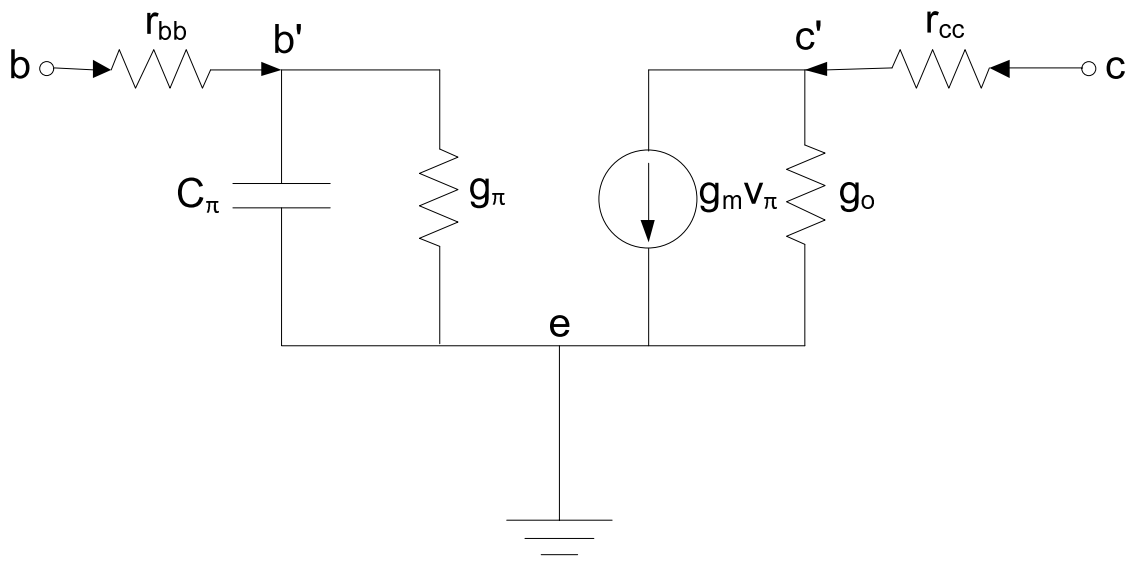


Figure 2.9: Simplified unilateral small-signal equivalent circuit model for HBT.

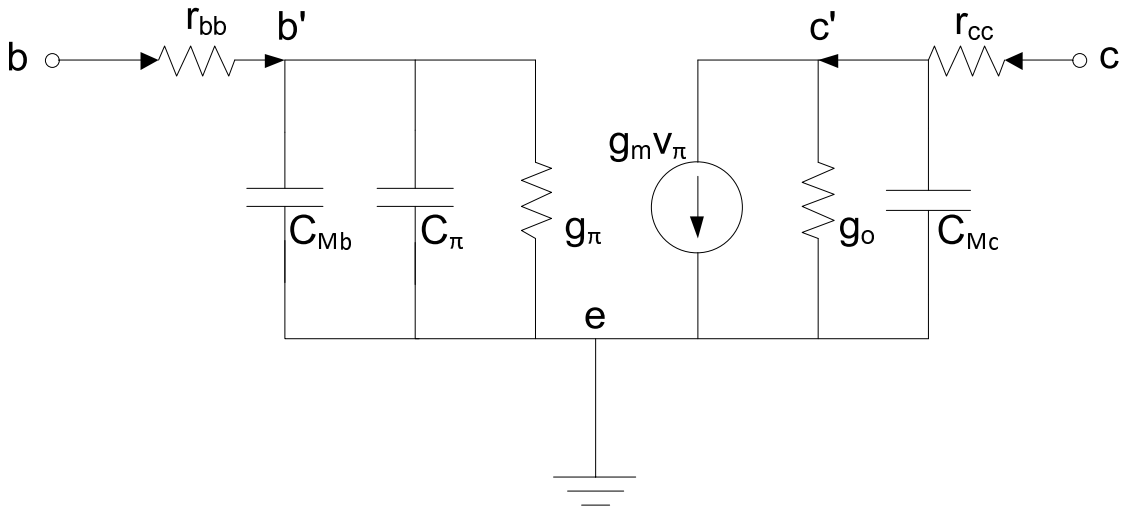


Figure 2.10: Unilateral model of HBT with Miller approximation.

On the other hand, DA's design analysis and formulae are developed based on the transistor unilateral model for simplicity [5]. As the technologies and applications

are so diverse, [70] suggested a refined unilateral model should be applied taking into consideration the analytical formulation.

2.7 Active Cell Configuration

The collector-emitter breakdown voltage of a transistor determines the upper limit of the voltage swing that the device can deliver to a load, normally 50Ω. The breakdown voltage imposes a limitation for DPA development. Also, the popular common-emitter (CE) gain cell usually suffers from the Miller effect [68].

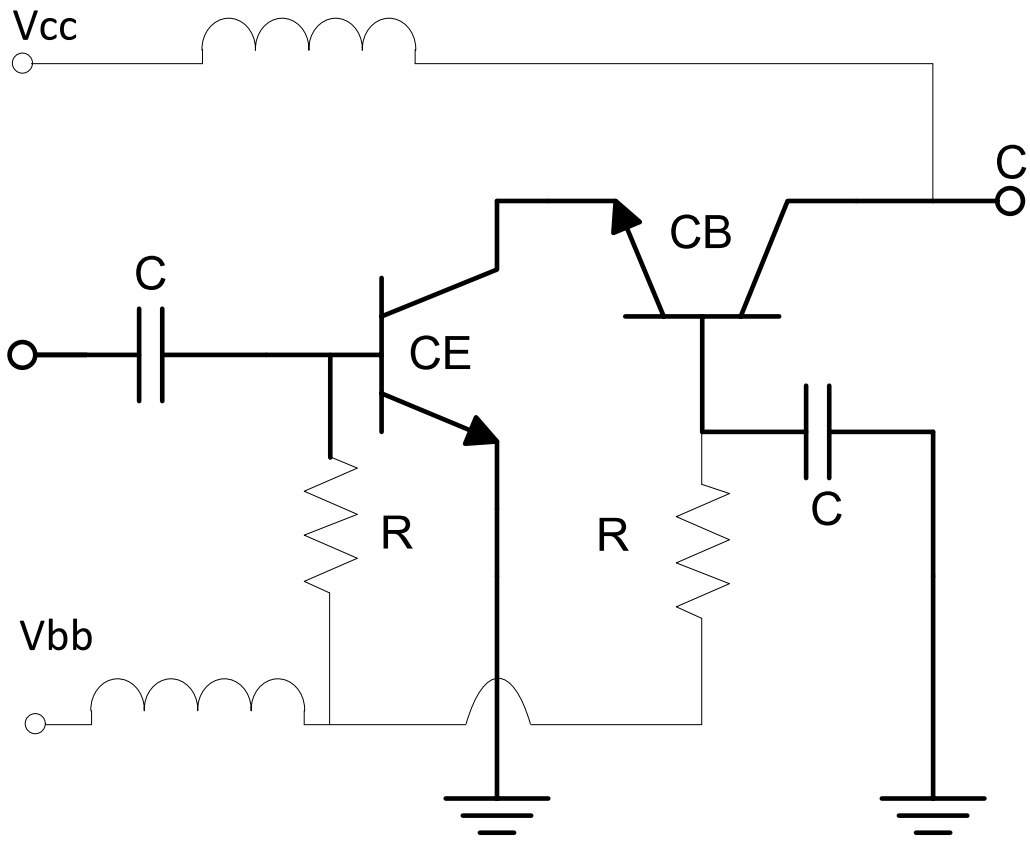


Figure 2.11: Simplified schematic of the cascode configuration.

The cascode pair is an appealing configuration for DPA application. It is a two-stage amplifier with a trans-conductance amplifier implemented using common emitter (CE) configuration and a current buffer implemented using common base (CB) configuration. The CB stage follows the CE. Figure 2.11 shows the circuit schematic of the cascode configuration. This configuration possesses the combine advantages of CE and CB configurations. The input impedance of the CB stage is given by $1/g_m$, mean while the voltage gain of the CE stage is very low [10]. Thus, the influence of the Miller effect is minimized and this contributes to a much higher bandwidth. The input and output impedances of the cascode configuration are relatively higher than the corresponding CE configuration while the overall voltage gain is about the same. As its output is effectively isolated from the input in terms of both electrically and physically, hence stability performance is also better. Consequently, the cascode cell obviously is more attractive for power distributed amplification [14, 18, 32, 68, 71].

2.8 Biasing

An important step that needs to be addressed in any amplifier design is the selection of the dc quiescent point for the active device (class of operation). A bias network is used to provide the appropriate quiescent point for an active device under the specified operation conditions. RF/Microwave PAs are commonly designed as class A, B, C, D, E and F [4]. The selection of class depends primarily on the particular application that is intended for the amplifier. The class of operation differs not only in the method of operation but also in efficiency and output power capability.

2.8.1 Class-A

An amplifier is defined as class-A if the active device used in the amplifier is conducting over the entire 360 degree cycle of the input waveform. Class-A amplifiers are considered to be the most linear, since, the transistor is biased at the center of the maximum voltage and current swing range. Figure 2.12 shows output current and voltage waveform of class-A operation.

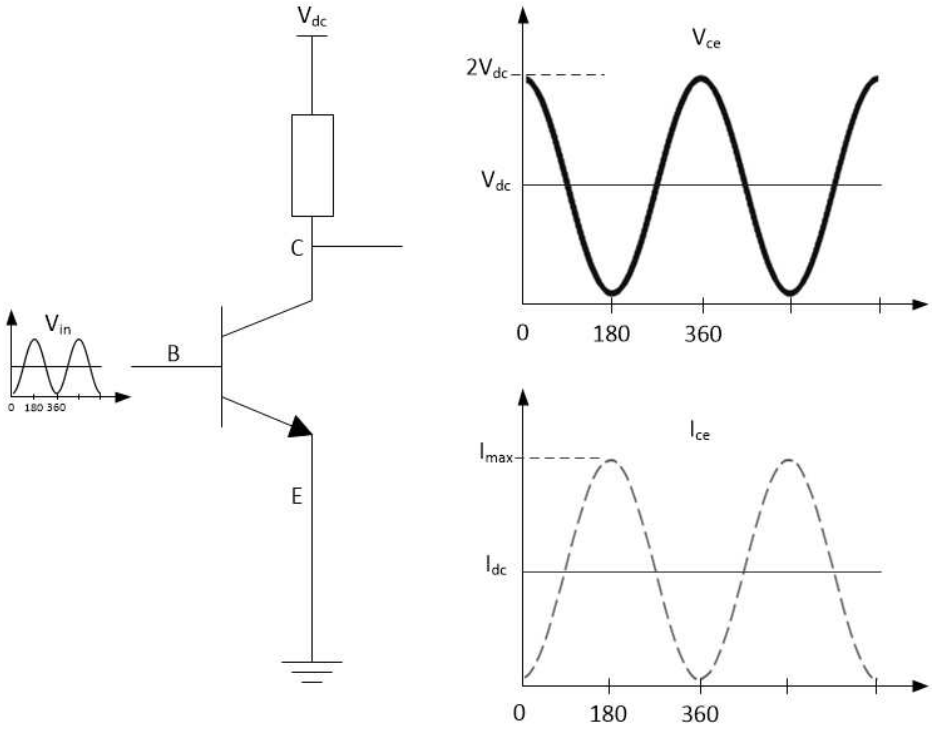


Figure 2.12: Voltage and current waveforms at different terminals of a transistor under class-A operation.

The varying signal amplitude is not visiting into the cutoff or saturation region of the transistor and the output wave from is a perfect replica of the input wave. As it is operating in linear region, the output waveform is pure sinusoidal and no harmonics components present. However the transistor is draining current at all times and faces

higher power loss. The theoretical maximum efficiency achievable from a class-A operation is 50% and practical efficiency is typically much lass.

2.8.2 Class-B

In this mode, a transistor is biased at the cutoff-threshold point. Hence, the current is flowing at the output of the device for the positive half cycle of the input signal. During negative half cycle the device remains turned off. The transistor is conducting only 180 degree of a cycle of the input waveform. Figure 2.13 shows the output current and voltage waveforms of class-B amplifier. The quiescent current is either zero or less than 10% of maximum collector current ($< 0.1 I_{cmax}$). Switching the transistor off during the negative half cycle saves the power consumption significantly. The output current waveform in this mode is a half-wave rectified sinusoid as shown in Fig. 2.13. The theoretical maximum efficiency of class-B operation is 78.5% and 50% to 60% is practically achievable.

Theoretically a class-B amplifier is as linear as a class-A. However, inside the transistor neither turned-on nor turned-off occurs abruptly from one state to another . Instead the transition is gradual and nonlinear. This distorted the wave form and called crossover distortion. It reduces the linearity performance of class-B amplifier. In addition, the rectification of waveform generates significant even harmonic components. These harmonics components are needed to terminate properly to eliminate harmonics distortion. Hence, the class-B amplifier is inherently hard to realize above the single octave bandwidth.

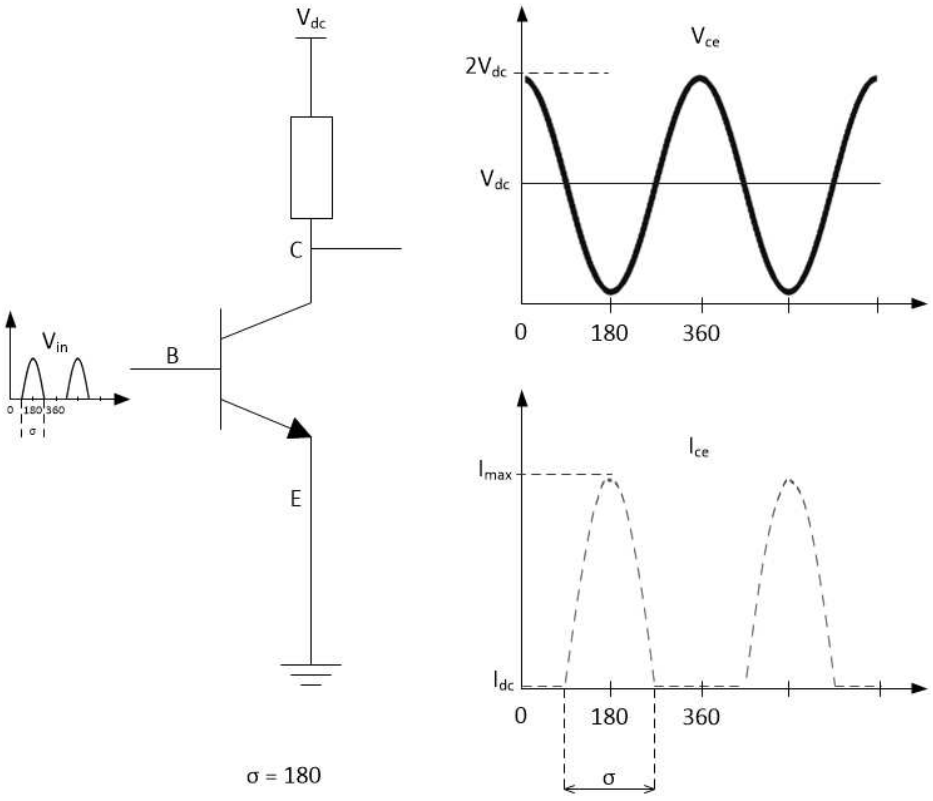


Figure 2.13: Voltage and current waveform at different terminals of a transistor under class-B operation.

2.8.3 Class-AB

An amplifier operated in class - AB mode is defined as having a dc quiescent collector current in the range of 0.1 to $< 0.5I_{cmax}$. The conduction angle can be anywhere between 180 degree and 360 degree. The input and output waveforms are presented in Fig. 2.14. As the name suggests, it can be considered as a class compromised between class-A and class-B. The crossover distortion effect found in class-B is minimized the poor efficiency performance of class-A is compensated. The theoretical maximum efficiency of a class-AB operation is between 50% to 78.5% and 40% to 55% efficiency is practically achievable. However as in the case of class-B, the bandwidth achievable

is still limited to single octave. Class-AB is a reasonable choice to tradeoff linearity and efficiency in a classic way.

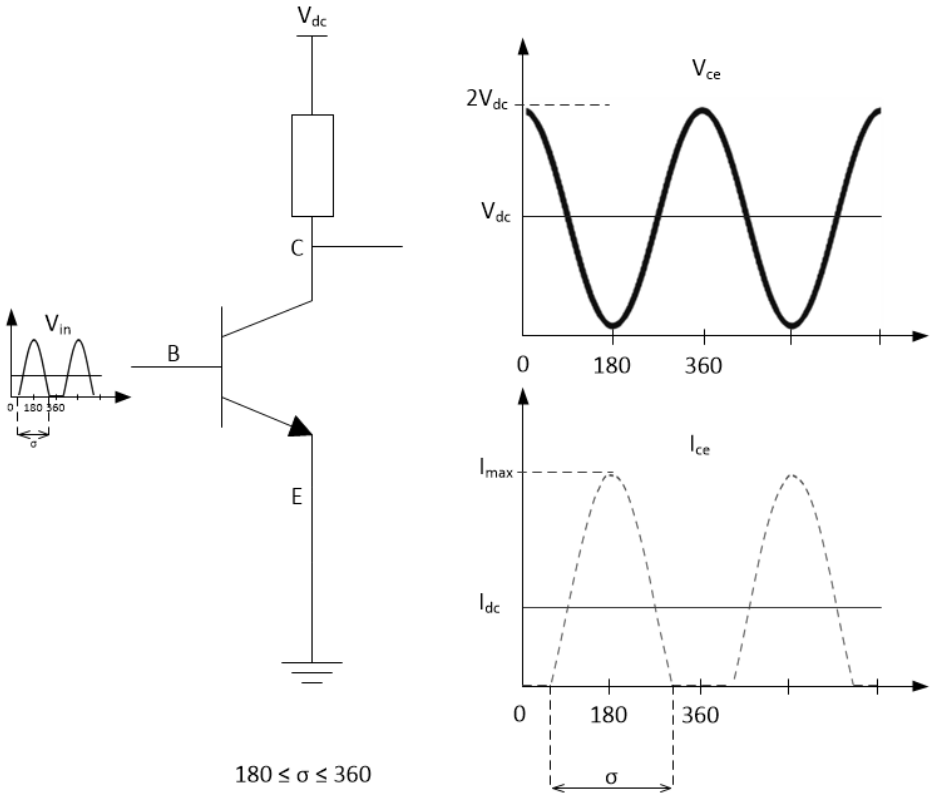


Figure 2.14: Voltage and current waveform at different terminals of a transistor under class-AB operation.

2.8.4 Other Classes

Other classes such as C, D, E, and F need resonators at the output to obtain the fundamental power at the load. Unfortunately, harmonic terminations are not always possible in broadband designs because the harmonics can easily fall within the operating bandwidth of the amplifier.

2.9 Stability

Stability is an important factor for amplifiers. An amplifier is potentially unstable at a frequency (f) if there are passive ports terminations that produce self-sustained oscillations with the frequency (f) [58].The amplifier should be stable and not oscillate at an frequency under normal operating conditions. The stability of an amplifier depends on matching at its terminals or ports. Since, input and output matching networks depend on frequency, stability conditions become frequency dependent.

Analyzing stabilities characteristics of an amplifier requires examination of small signal and associated reflection coefficient Γ behaviors. Figure 2.15 shows simplified single stage RF amplifier together with input and output matching networks and their associated reflection coefficients. The amplifier is unconditionally stable if the absolute magnitude of both input and output reflection coefficients are less than one ($|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$) for all passive source and load impedances [8]. The amplifier can also be conditionally stable if the mentioned condition satisfy only for a range of passive source and load impedances.

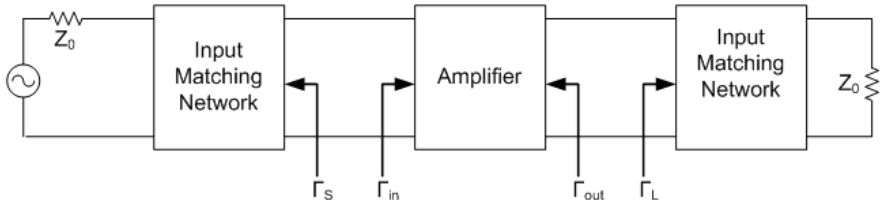


Figure 2.15: The simplified single stage amplifier circuit.

The input and output reflection coefficients can be present using S-parameter as [8]

$$|\Gamma_{in}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| \tag{2.2}$$

$$|\Gamma_{out}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| \tag{2.3}$$

As mention before, unconditionally stable situation can achieve when

$$\left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1 \tag{2.4}$$

$$\left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1 \tag{2.5}$$

If the device is unilateral, $S12 = 0$ and hence $|S11| < 1$ and $|S22| < 1$ are sufficient conditions for unconditional stability. Otherwise, the inequalities in (2.4) and (2.5) define a range of values for Γ_S and Γ_L where the amplifier will be stable. By defining

$$\Delta = S_{11}S_{22} - S_{12}S_{21} \tag{2.6}$$

and simplifying the (2.4) and (2.5) results

$$\left| \Gamma_L - \frac{(S_{22} - \Delta S_{11}^*)^*}{\left(|S_{22}|^2 - |\Delta|^2\right)} \right| = \left| \frac{S_{12}S_{21}}{\left(|S_{22}|^2 - |\Delta|^2\right)} \right| \tag{2.7}$$

$$\left| \Gamma_S - \frac{(S_{11} - \Delta S_{22}^*)^*}{\left(|S_{11}|^2 - |\Delta|^2\right)} \right| = \left| \frac{S_{12}S_{21}}{\left(|S_{11}|^2 - |\Delta|^2\right)} \right| \tag{2.8}$$

Equation (2.7) and (2.8) have the form $|\Gamma - C| = R$ and which represents a circle with center at C and radius R. Where, both Γ and C are complex numbers and R is a real. Then center C and radius R can be present as

$$C_L = \frac{(S_{22} - \Delta S_{11}^*)^*}{\left(|S_{22}|^2 - |\Delta|^2\right)} \tag{2.9}$$

$$R_L = \left| \frac{S_{12}S_{21}}{|S_{22}|^2 - |\Delta|^2} \right| \tag{2.10}$$

on the Γ_L complex plane and

$$C_S = \frac{(S_{11} - \Delta S_{22}^*)^*}{\left(|S_{11}|^2 - |\Delta|^2\right)} \tag{2.11}$$

$$R_S = \left| \frac{S_{12}S_{21}}{|S_{11}|^2 - |\Delta|^2} \right| \tag{2.12}$$

on the Γ_S complex plane.

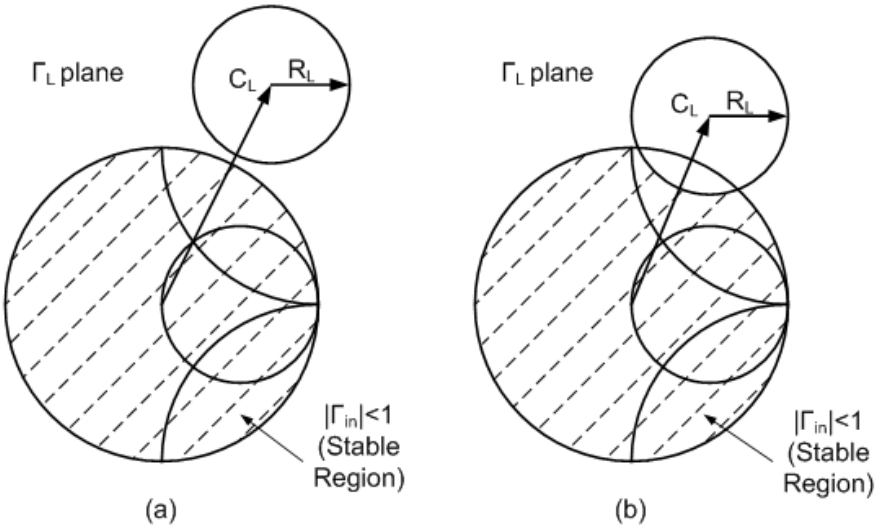


Figure 2.16: Output stability circles for a unconditionally stable and conditionally stable situation with $S11 < 1$.

Using those C and R, source and load stability circles can be plotted on the Smith chart. These stability circles are defined as loci for which $|\Gamma_{in}| = 1$ and $|\Gamma_{out}| = 1$. Then, the circles define the boundaries between stable and potentially unstable regions of Γ_S and Γ_L. Determining which side of the boundary represents the stable region requires checking magnitude of $S11$ for load stability circles and $S22$ for source stability circles. The device is unconditionally stable, then the stability circles must

be completely outside or totally enclose the Smith chart [8] and can express as

$$||C_L| - R_L| > 1, \text{for } |S_{11}| < 1 \tag{2.13}$$

$$||C_S| - R_S| > 1, \text{for } |S_{22}| < 1 \tag{2.14}$$

Figure 2.16 shows the unconditionally stable situation and conditionally stable situation with stable regions identification. If $|S11| > 1$ or $|S22| > 1$, the amplifier cannot be unconditionally stable. If the amplifier is conditionally stable, operating points for Γ_L and Γ_S must be chosen in stable regions. An amplifier can be made to be unconditionally stable by using resistive load, with the compromise of the gain.

2.10 Efficiency

Microwave PA is a circuit converting DC input power to microwave output power. The power consumption of the PA can dominate over all other electronics and digital processing circuits of a mobile unit in most of the communication systems. That demand highly efficient PA for extending the operating time of the terminal unit, which is totally dependent on the limited power source. PA also plays a major role in terms of base station energy consumption and heat dissipation. Operators want to cut their radio network operating expenses (OPEX), of which energy consumption is a significant factor. In addition, increasing mobile usage requires enormous number of base stations around the world and this will have significant impact on the environment. Reducing the energy consumed by the radio base stations will also reduce the environmental impact of the radio access network.

2.10.1 State-of-the-Art Techniques for Power and Efficiency Improvement in DPA

Over the past two decades, numerous efforts have been made to maximize the output power and efficiency of DA for high power wide band applications. The most popular technique for minimizing DC power consumption is to reduce the conduction angle by operating in class-AB or class-B or even class-C, rather than using class-A. This approach faces bandwidth limitation as harmonic terminations are required to reshape the waveforms. Another consideration in minimizing the DC power consumption in a DPA design is in optimizing the number of amplifier stages. A higher number of stages will consume more DC power. This scenario will be more significant when the attenuations of the input and output lines become high. Attenuation characteristics of the input/output lines and the number required amplifier stages need to be carefully analyzed. However, attenuation analysis and optimizing the number of stages have been largely neglected in most previous efficiency improvement works [1,14,29,36,72].

The efficiency of a DPA is also affected by its power gain. The need for high gain in PA designs will become apparent from the overall efficiency specification of the amplifier. As power added efficiency (PAE) of an amplifier accounts for the input drive signal power required for the amplifier, it can be clearly seen that higher power gain will return higher PAE. Generally, the power gain of a single DA are less than 15dB and typically around 10dB [11,14–16,71]. Some work on the power gain improvement is given in [18], however no analytical solutions are provided.

The final factor governing the efficiency is output power of a DPA. Increase in output power level with the same DC power consumption will result in higher efficiency. Output power level also determines the range of the system and hence optimization of output power level and efficiency is actively researched [1, 13, 14, 16, 72]. Various

techniques have been presented to improve the power and efficiency performances. Most popular techniques are summarized in the following.

Optimum Load Analysis and Tapered Design

Ideally, maximum RF output power should be obtained by promoting the maximum peak-to-peak swing of the collector voltage and current. The optimum load impedance for an amplifier is the load at which both voltage and current can achieve maximum swing. The most effective way to achieve an optimal value of load termination is by load - pull measurement. Load-pull measurement is an ultimate tool that effectively considers all characteristics of the device and expresses the results from the actual working conditions. However, optimum load for fundamental single frequency and each of its harmonics (in aspect of optimum power or optimum PAE) are at different impedance values. As DAs cover multi-octave bandwidth, it is unreasonable to use optimum load obtain from load-pull measurement. Instead, it is more meaningful to use general DC load line theory to find out the optimum load.

If the transistor output is terminated with the optimum load, then the current swings over its maximum linear range $0 \sim I_{c\max}$ with amplitude of $I_{c\max}/2 = I_{cc}$ and the voltage swings over its maximum range of 0 to $2V_{cc}$ with amplitude of V_{cc}. Then the load resistor in this optimum power matched conditions has a value of [73]

$$R_{opt} = \frac{V_{cc}}{0.5 I_{c\max}} = \frac{V_{cc}}{I_{cc}} \tag{2.15}$$

Under this optimally power matched condition, RF power $P_{out-opt}$is

$$P_{out-opt} = 0.5\,(V_{cc} \times I_{cc}) \tag{2.16}$$

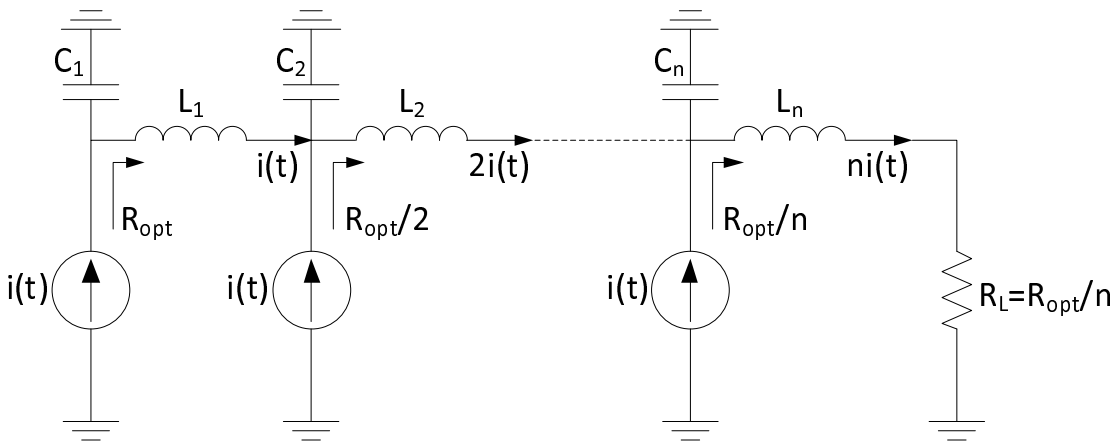


Figure 2.17: Schematic for n-stages tapered collector transmission line to achieve power matched condition.

For conventional DA, the load impedance presented to each active cell is not at its optimum as its input and output ports are purposely design for broadband. Optimum load line technique has been integrated into DPA designs [1, 13, 14, 16, 72] where each sections of the output artificial line is designed to match for optimum power of each active cell as closely as possible over the frequency range. By doing so, each device will deliver maximum power over the bandwidth.

Tapered collector (drain) line technique is the most utilized method to implement the optimum load concept in DA design. Figure 2.17 shows simplified schematic of tapered collector line technique. The impedance of the collector line is changing from one segment to another. By assuming that all active cells are identical and all input receive equal amplitude, the equivalent load resistance seen by n^{th} cell can simply be calculated as

$$R_{nL} = \frac{R_{opt}}{n} \tag{2.17}$$

Since the collector line is terminated by the dumping load Z_c at the other end, the

effective load impedance of the first cell is $(g_{opt} + Y_c)^{-1}$, which results in reduced output power of the first cell. In addition, the dumping termination at the reverse port absorb significant amount of output power.

Every active device also has parasitic and non - zero output conductance which eventually alter the load line contour. As discussed above, actual optimum load impedance is varying with frequency. It is very difficult to get optimum load for wide range of frequencies. Hence, in the case of DA, optimum load technique is a partial solution to improve output power performance.

Dual-Fed Distributed Power Amplifier

In this technique, no dumping base and collector line terminations are used. The short - circuit terminations at the end of both input and output lines emulate the dual feeding behavior of the input and output line. The signal at the input port travels down the base line and is reflected at the reactively terminated end and amplified again [74, 75].

Similar scenario can be applied to the collector line. For moderate bandwidth applications, the amplifier matching may not be so critical and the dumping load may be eliminated [16]. Maximum output power can be achieved when $Z_c = \infty$ [11].

Figure 2.18 shows the schematic of dual feed DA with reactive termination. Other pure reactive terminations can also be used instead of a short [4]. Despite the above advantages, dual feed DA has degraded input and output match. Stability is another issue with this configuration. In addition, it is very difficult to get a constructive wave from incident and reflected waves for multi - octave bandwidth and larger number of stages.

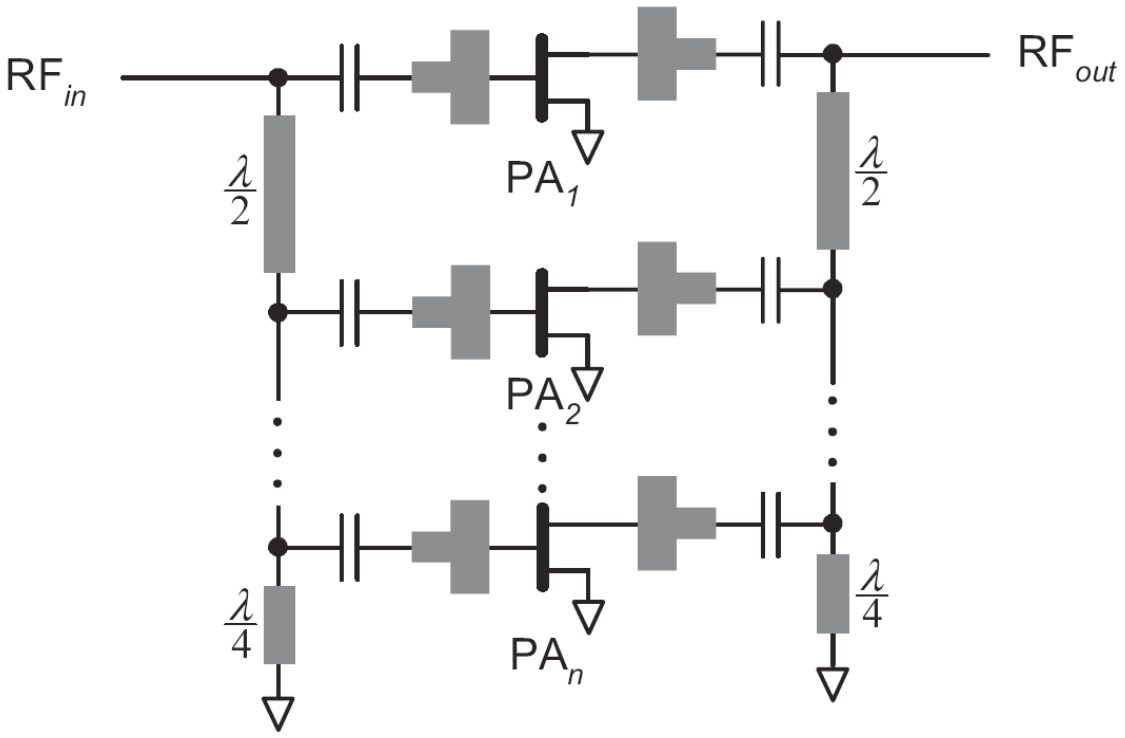


Figure 2.18: Transmission line implementation of dual-feed distributed amplifier.

Non Uniform Distributed Power Amplifier

In the case of uniform distributed amplifiers with identical transistors, the optimum power load is constant for each section of the output line. Since all the active devices are imbedded within the same impedance conditions, (2.17) shows that the optimum impedance for the final device is n times smaller than R_{opt} of the first stage and the power contributions of the stages closer to the load are much smaller than their previous stages. The final stage optimum load impedance can be much smaller than the standard terminating impedance of 50Ω.

Impedance matching may not be a good option, since the ratio for each matching circuit should be less than 1.5 in order to achieve larger than 3:1 bandwidth, in general.

Hence, this technique proposed utilization of different transistor sizes to minimize the impedance variation along the output line, to achieve the final stage optimum load with direct match to 50Ω termination [16]. Choosing different size of the transistor for different stages according to their power contribution behaviors will reducing DC power consumption. Figure 2.19 shows the output line schematic of a non-uniform DA.

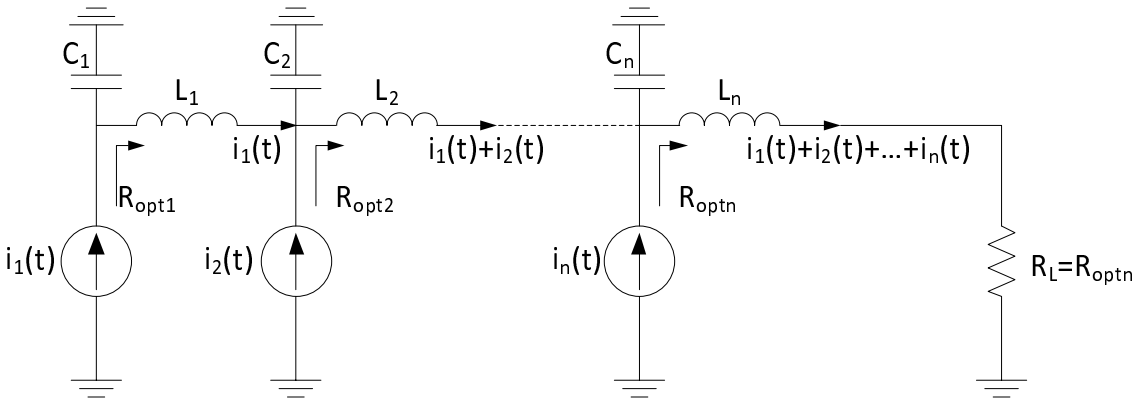


Figure 2.19: Output artificial transmission line schematic of n-stages, non-uniform distributed amplifier.

Inductive Peaking

The gain and bandwidth [10, 11] performance of the cascode cell is optimized using inductive peaking technique. Figure 2.20 shows the schematic of inductive peaking in a cascode cell. A series inductor is placed between collector of the CE stage and emitter of the CB stage. This is used to resonate with the capacitor terminated at the base of the CB stage. This is supposed to provides higher gain and wider bandwidth. However, only bandwidth improvement is observed in the result and no significant DA in overall gain improvement is observed in the results [10, 11].

In addition to above mention techniques efficiency and power are optimized using

the unequal biasing and input signal equalization in [72].

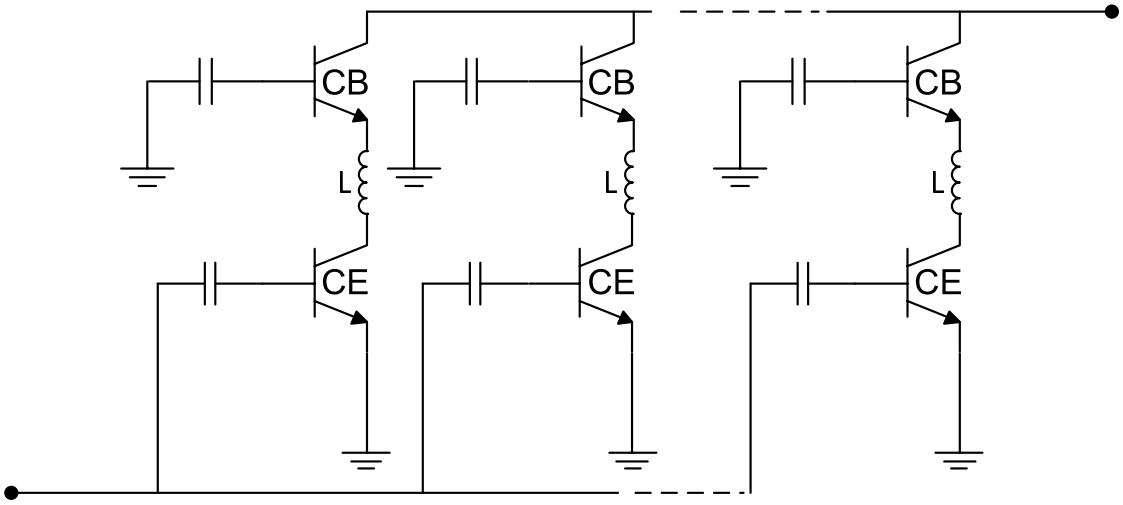


Figure 2.20: Schematic of inductive peaking in cascode cells.

2.11 Conclusion

In this chapter, some of the well-known bandwidth enhancement techniques are reviewed and particularly on the distributed amplification technique. The advantages and disadvantages of DA technique for ultra-broadband PA application are also presented. The available device technologies which are preferred for broadband applications are reviewed. The advantages and disadvantages of different HBT technologies and suitability of these technologies for various applications are discussed in detail. GaAs HBT is selected for its power handling capabilities. Thermal issue related to GaAs is discussed and the short-falls of first order standard thermal models are examined. As DA design analysis and formulae are derived based on unilateral assumption, the validity of various unilateral equivalent circuit models in higher frequency and power applications is discussed. To overcome the low collector-emitter break-

down voltage characteristic of GaAs HBT, the circuit configurations for active cells are also reviewed. The strength of cascode configuration for DA application is presented. The state-of-the-art techniques used to improve the DPA performances are also summarized in the final section.

Chapter 3

Electro-Thermal Analysis

3.1 Introduction

The objective of this chapter is to numerically analyze both steady state and dynamic thermal behavior of an InGaP/GaAs HBT for PA application. A technique capable of predicting fast fluctuating junction temperature of a power HBT is developed. The technique is expected to be applicable for a wide range of signal types, power levels, frequencies, substrate position and material properties.

3.2 Self-heating Effect

Heat is generated in the transistor by dissipated power and flows through the substrate. The power dissipated in the device can be express as a combination of thermal power ($\widehat{p}_{th}(t)$) and the rate of heat energy changes with time ($\frac{dW_{th}}{dt}$) [58] as

$$p_{diss}(t) = \frac{dW_{th}}{dt} + \widehat{p}_{th}(t), \tag{3.1}$$

$$\frac{dW_{th}}{dt} = \frac{dW_{th}}{dT} \times \frac{dT}{dt}, \tag{3.2}$$

$$\widehat{p}_{th}(t) = \frac{\Delta T(t)}{\widehat{R}_{th}}. \tag{3.3}$$

The rate of change of the thermal energy with temperature (dW_{th}/dT) can be presented as thermal capacitance ($\widehat{C}_{th}$). Then (3.1) becomes the differential equation for excess temperature ($\Delta T(t)$) due to power dissipation,

$$\widehat{C}_{th}\frac{d}{dt}\Delta T + \frac{\Delta T}{\widehat{R}_{th}} = p_{diss}(t) \tag{3.4}$$

Equation (3.3) together with Ohm's law analogy allows one to describe the excess temperature relaxation using thermal equivalent circuits. The heat flow, $\widehat{p}_{th}(t)$, due to the temperature difference, ΔT, is determined by the thermal resistance, while the electrical current, i, due to a potential difference, v, is determined by the electrical resistance. The thermal time constant, τ_{th}, corresponds to the RC time constant of the equivalent circuit. Then $\widehat{p}_{th}(t)$, $\widehat{R}_{th}$ and $\widehat{C}_{th}$ are related to the parameters and elements used in thermal equivalent circuit i_{th}, R_{th} and C_{th} according to

$$i_{th} = 1\frac{A}{W}\widehat{p}_{th},\ C_{th} = 1\frac{FK}{J}\widehat{C}_{th},\ R_{th} = 1\frac{\Omega W}{K}\widehat{R}_{th}. \tag{3.5}$$

where,the unit A = Ampere, W = Watt, F = Farad, K = Kelvin, J = Joule, Ω = Ohm. Then, the voltage v across the capacitor (C_{th}) varies in directly proportional to the excess temperature as,

$$\Delta T = 1\frac{K}{V}v \tag{3.6}$$

Figure 3.1 shows first order thermal equivalent circuits, composed of an equivalent thermal resistance (R_{th}) and a thermal capacitance (C_{th}). It is used to approximate complex thermal behavior of a transistor. This model possess low pass behavior and

it is commonly included in standard bipolar compact models such as VBIC, HiCUM, MEXTRAM, and Agilent HBT [50, 57, 76].

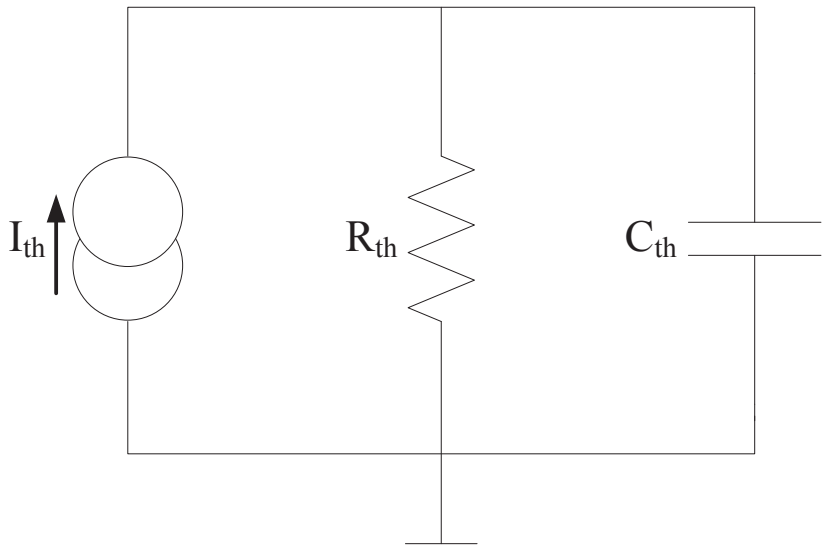


Figure 3.1: First order thermal equivalent circuit.

Various techniques, (i) Numerical Analysis [77–79], (ii) 3D Simulation [80–82], (iii) Measurement [83], and (iv) Behavior Modeling [84–86], have being developed to identify thermal characteristics of a transistor. In many case [87–89] thermal resistance is used to compute the junction temperature. Thermal resistance characterization using DC measurements at different base plate temperature produce relatively accurate results. As various transistor's parameters such as base-emitter junction voltage (V_{be}), current gain (β_i) and collector current (I_c) are sensitive to temperature and are used for thermal characterization. Among them collector current measurement at different base plate temperature give relatively easy and highly reliable results [88]. It overcomes the drawbacks of other methods and can be used to find thermal resistance under high power dissipation.

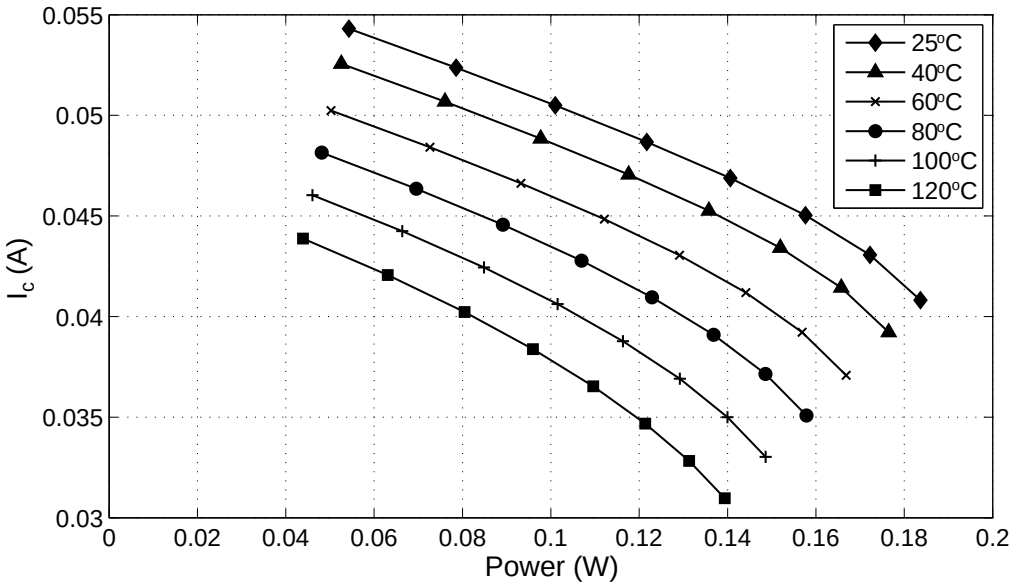


Figure 3.2: Measured collector current variation with different static power levels and base plate temperature.

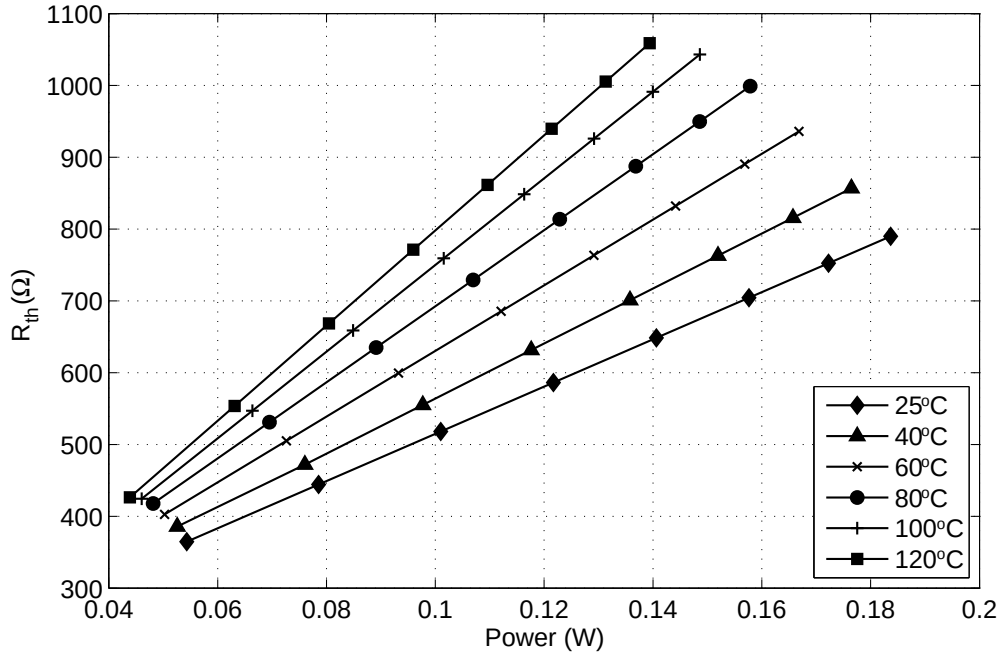


Figure 3.3: Extracted R_{th} verses power dissipation at various base plate temperatures.

Figure 3.2 shows measured collector current variation of $1 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT at different base plate temperature ranging from 25°C to 120°C over various steady state power levels. Indirect measurement technique developed in [88] is used to extract thermal resistance of the transistor. The extracted R_{th} values are presented in Fig. 3.3. The results show thermal resistance is increasing with power dissipation. Analytically computed thermal resistance can also be seen in [50].

Mutual thermal coupling between fingers of a power HBT is modeled as a thermal resistance matrix and multi-fingers effect on T_j is integrated [90]. Those characterizations and models predict reliable junction temperature for steady state condition. However, they have limitation in predicting dynamic T_j.

Frequency-dependent dynamic T_j analysis are conducted using different envelope frequencies of up to 100kHz in [83], 1MHz in [81] and 10MHz in [77, 80]. The work of [81] reports that the thermal transient cutoff frequency is around 1MHz while [80] reported transient cutoff frequency of up to 10MHz. These large variations in cutoff frequencies are due to the amount of heat dissipation and their dynamic variations in each case. For low power applications, small-signal transient thermal analysis [91] is valid.

Modern high speed communication systems use spectral efficient multi-carrier technique like orthogonal frequency division multiplexing (OFDM) and transmission efficiency improvement technique like quadrature amplitude modulation (QAM). Regardless of individual carrier's characteristics, OFDM typically introduces peak to average power ratio (PAPR) of (8 to 13) dB and QAM contribute another (3 to 6) dB [91].

Very high peaks generated from these systems can cause significant T_j excursion from the average. This phenomenon induces nonlinear current gain that is highly depending on the magnitude of the adjacent symbol envelope. This poses thermal memory effect. These nonlinear effects with memory cause distortion of the enve-

lope resulting in data reception error and spill-over of signal into adjacent channels. These distortions are regulated in transmitter performance measures. Less than 3% error vector magnitude (EVM) is demanded in WiMAX [92]. Hence, in the case of multi fingers power HBT and PA applications with large dynamic envelope amplitude variations above the average value, the use of small signal transient thermal analysis will produce erroneous results. These large amplitude signals perturb the DC bias and the collector (drain) supply of the PA is modulated at envelope frequency. Huge power dynamic could occur in a short period of time. Even for very short time duration which are much smaller than the junction thermal time constant [82], those power dynamics may cause T_j fluctuations. So, there is a need for compact simulation model that is able to model the short time dynamic thermal effects especially for the simulation and optimization of a PA operating for high PAPR signals. In most of the cases, the signal envelope is complex and the dissipated power waveform contains various baseband components below the thermal cutoff frequency. The interaction of nonlinearity and dynamic effects make T_j prediction and thermal modeling complex.

This led us to analyze dynamic temperature behavior under CW, periodic arbitrary and aperiodic arbitrary pulse signal with high power. The interest includes very short time period of a few tens of nano-seconds, which need very fine mesh for finite element method (FEM) like 3D simulation and this make it time consuming [90]. Numerical approach offers the advantage that a lot of parameters, including structure dimension and material's thermal properties, can be varied and standard model for different technologies can be achieved.

In the following section, temperature distributions in GaAs HBT are numerically analyzed in frequency domain, as a function of power dissipation, frequency and space. It incorporates frequency-dependent complex thermal impedance behavior in the transistor. Through the use of Fourier signal analysis, this thermal analysis is extended

into arbitrary periodic or aperiodic pulse heating operation. To mimic the heating by multi-carrier signals which have tens of MHz bandwidth with high PAPR, T_j for high power square pulses with power levels of 0dB, 3dB, 6dB and 10dB above the nominal average level of 40mW and with pulse widths ranging from 10ns to 100ns, are analyzed.

3.3 Analyzed Structure and Technology

We investigate a structure that is modeling a transistor on top of a semiconductor substrate. Uniform cylindrical heat sources, which are volumetrically equivalent to a real single finger $1 \times 2\mu$m $\times$ 20μm and $1 \times 3\mu$m $\times$ 40μm HBTs, are analyzed. The considered schematic is shown in Fig. 3.5. GaAs is chosen as substrate material with the following thermal properties: $\kappa = 55W/m^{\circ}C$, $c = 330J/kg^{\circ}C$, and $\rho = 5318kg/m^3$. The thickness of the transistor and substrate are $a = 1\mu$m and $b = 75\mu$m respectively.

3.4 Numerical Analysis

The general heat conduction equation for a medium with its thermal conductivity at any point in the medium is the same in all directions (*isotropic*) and can be express as [93],

$$\nabla^2 T + \frac{\nabla\kappa \cdot \nabla T}{\kappa} + \frac{Q_0}{\kappa} = \frac{1}{\alpha_T}\frac{\partial T}{\partial t} \tag{3.7}$$

where, $\nabla^2 = \nabla \cdot \nabla$ is the Laplacian operator, Q_0 is heat flow rate per unit volume; κ is thermal conductivity of the material and α_T is the thermal diffusivity. The heat flow rate and thermal diffusivity can be expressed as: $Q_0 = P_0(t)/(\pi r^2 L)$; for cylindrical heat source and $\alpha_T = \kappa/\rho c$ respectively. Where: $P_0(t)$ is power dissipation in the

transistor, L is the length of the heat source, ρ is volumetric density and c is specific heat capacity of the substrate.

In general, materials become more conductive with respect to the average temperature increase. As a result, κ of a material is temperature dependent. Thermal conductivities of the materials used in HBTs are highly dependent on the temperature, such as GaAs and Si. However, for GaAs, κ is decreasing with increasing temperature above 20 Kelvin [94]. This is a reason of increasing thermal resistance with power dissipation in Fig. 3.3. If κ is a function of temperature, (3.7) becomes a nonlinear partial differential equation. However,(3.7) can be reduced to a linear differential equation by means of the Kirchhoff transformation [93],

$$\nabla^2 \vartheta + \frac{Q_0}{\kappa} = \frac{1}{\alpha_T} \frac{\partial \vartheta}{\partial t} \tag{3.8}$$

$$\nabla \vartheta = \frac{\kappa(T)}{\kappa_0} \nabla T \tag{3.9}$$

The dependent of α_T on temperature can usually be neglected compared to that of κ for many solid [93]. In our analysis, we mainly focus on frequency and amplitude dependent dynamic thermal behavior of a transistor. Hence, the transistor and substrate material is assumed as homogeneous and isotropic (constant κ) for simplicity.

The heat is generated in a transistor by dissipated power. It is very common that the length of the active heat source in a transistor is longer than all other dimensions and it can be treated as a line source. Figure 3.4 shows image of fabricated single finger $1 \times 2\mu m \times 20\mu m$ InGaP/GaAs HBTs. The rectangular shape heat generating volume is transformed into an equivalent cylindrical volume and analyzed in cylindrical coordinates as heat is conducted in radial direction. Applying cylindrical coordinate simplifies two rectangular space variables, x and y, into a single radial variable r.

Figure 3.5 shows an un-scaled geometry of a single finger HBT on the substrate with cylindrical isothermal surfaces. The initial and boundary conditions are assumed to be independent of θ and z. The heat conduction equation in cylindrical coordinate with the presence of heat source, assumed uniformly distributed, is given by [95],

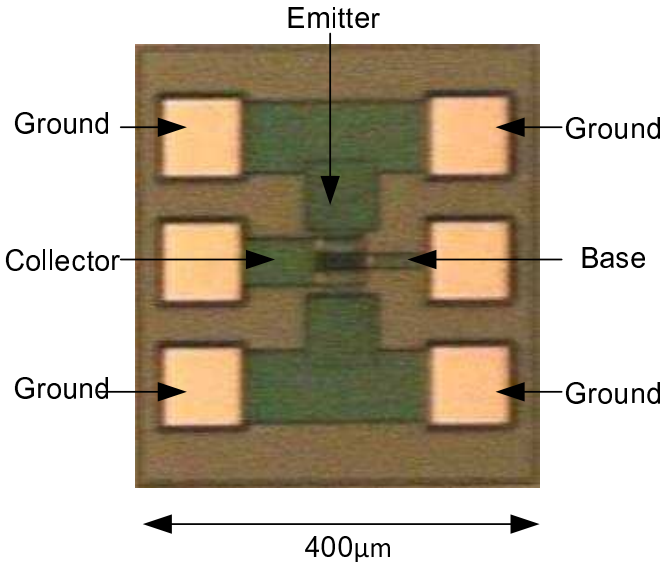


Figure 3.4: Image of fabricated single finger ($1 \times 2\mu m \times 20\mu m$) InGaP/GaAs HBT devices.

$$\frac{\partial^2 T_1}{\partial r^2} + \frac{1}{r}\frac{\partial T_1}{\partial r} + \frac{Q_0}{\kappa} = \frac{1}{\alpha_T}\frac{\partial T_1}{\partial t} \qquad 0 \leq r \leq a \tag{3.10}$$

and, the equation for the substrate without the heat source is

$$\frac{\partial^2 T_2}{\partial r^2} + \frac{1}{r}\frac{\partial T_2}{\partial r} = \frac{1}{\alpha_T}\frac{\partial T_2}{\partial t} \qquad a < r < b. \tag{3.11}$$

Where: T_i with $(i = 1, 2)$ is the temperature increment above the ambient temperature, a is the volume equivalent radius of the heat source and b is the thickness of substrate. Equation(3.10) and (3.11) are needed to satisfy the initial and boundary

conditions simultaneously.

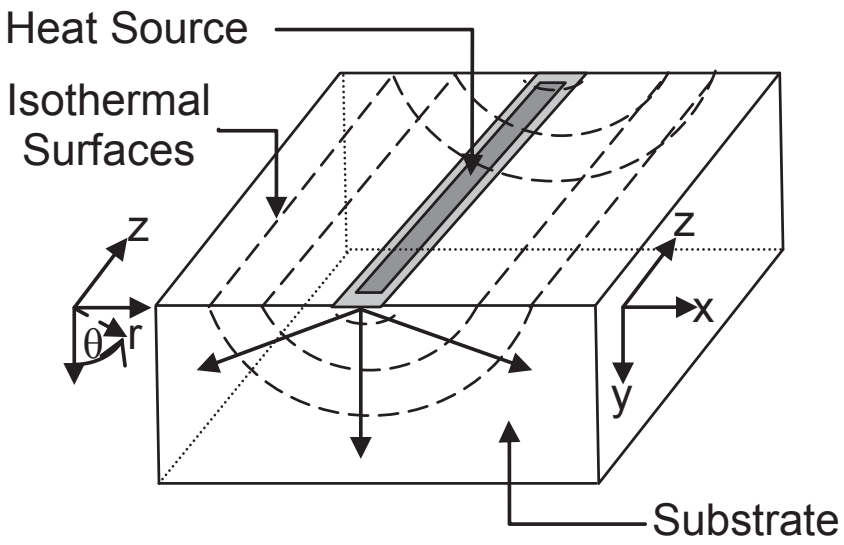


Figure 3.5: Single finger HBT schematic (un-scaled) with cylindrical isothermal surface.

3.4.1 Steady State Analysis

For steady state condition rate of change of temperature with respect to time is zero and Q_0 is constant. Then heat conduction (3.10) and (3.11) become,

$$\frac{\partial^2 T_1}{\partial r^2} + \frac{1}{r}\frac{\partial T_1}{\partial r} + \frac{Q_0}{\kappa} = 0 \qquad 0 \leq r \leq a \tag{3.12}$$

$$\frac{\partial^2 T_2}{\partial r^2} + \frac{1}{r}\frac{\partial T_2}{\partial r} = 0 \qquad a < r < b \tag{3.13}$$

Integrating (3.12) and (3.13) twice yield the general solutions,

$$T_1(r) = -\frac{Q_0 r^2}{4\kappa} + C_1 \ln r + C_2 \tag{3.14}$$

$$T_2(r) = C_3 \ln r + C_4 \tag{3.15}$$

We have to identify four coefficients $C_1,\ C_2,\ C_3,\ C_4$ using boundaries conditions. We assume that perfect thermal contact between the transistor and the substrate at $r = a$, the substrate and the gold-plate with heat sink at $r = b$ which is maintained at room temperature ($T_{amb} = 27^oC$). The rest of the surface is supported to be adiabatic. And the four boundary conditions can be written as

$$\frac{dT_1(r)}{dr} = 0 \qquad \text{at } r = 0, \qquad T_2(r) = 0 \qquad \text{at } r = b, \tag{3.16a}$$

$$T_1(r) = T_2(r) = T_x \qquad \text{at } r = a, \qquad \frac{dT_1(r)}{dr} = \frac{dT_2(r)}{dr} \qquad \text{at } r = a. \tag{3.16b}$$

Where, T_x is the temperature at the contact point of transistor to substrate and is assumed as junction temperature T_j, throughout the following analysis. Applying (3.16) to (3.14) and (3.15), T_x becomes

$$T_x = \frac{Q_0 a^2}{2\kappa} \ln \frac{b}{a} \tag{3.17}$$

and four coefficients can be computed as,

$$C_1 = 0, \qquad C_2 = \frac{Q_0 a^2}{2\kappa} \left(\ln \frac{b}{a} + \frac{1}{2} \right) \tag{3.18a}$$

$$C_3 = -\frac{Q_0 a^2}{2\kappa}, \qquad C_4 = \frac{Q_0 a^2}{2\kappa} \left(\ln \frac{b}{a} + \ln a \right) \tag{3.18b}$$

Then the steady state temperature distribution in the transistor fingers and in the substrate can be calculated numerically. To validate the numerical analysis, without computing thermal resistance, (3.14) and (3.15) are directly implemented in Agilent's Advance Design System (ADS) by using symbolically defined device (SDD).

DCIV simulations are conducted for $1 \times 3\mu m \times 40\mu m$ HBT and $3 \times 3\mu m \times 40\mu m$ HBT devices along with varying base plate temperature settings.

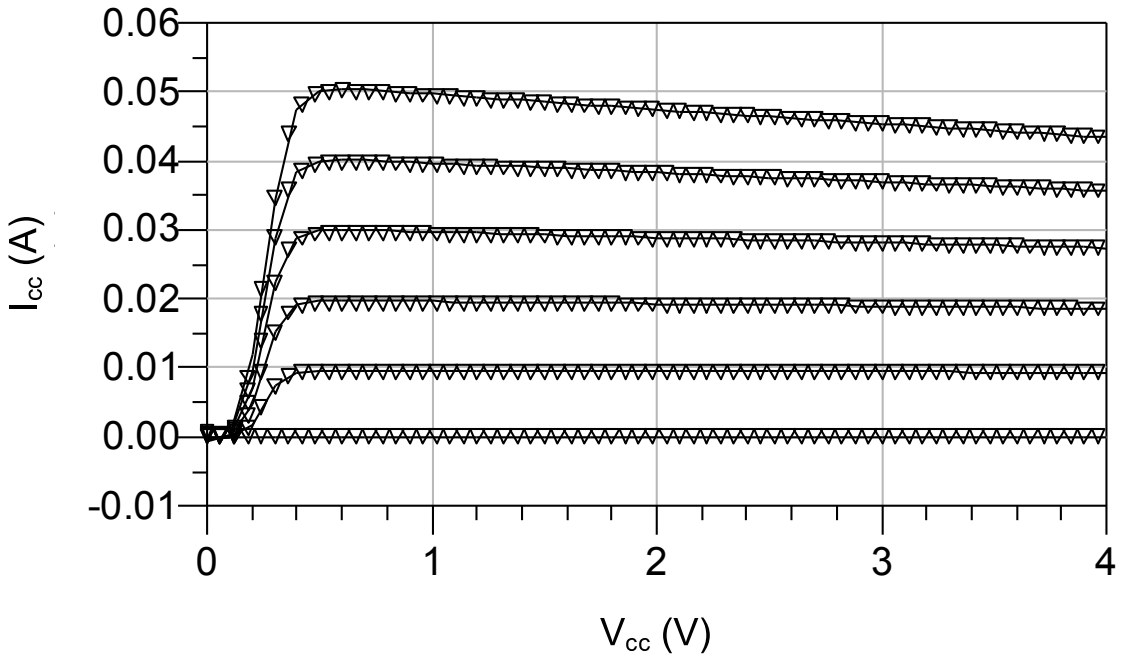


Figure 3.6: Measured (symbol) and simulated (solid line) collector current versus various collector voltages for different base biases for $1 \times 3\mu m \times 40\mu m$ HBT at base plate temperature 25°C.

Figure 3.6 and Fig. 3.7 show overlay plot of measured and simulated collector current versus collector emitter voltage of single fingers device at two different ambient temperatures, 25°C and 125°C. Figure 3.8 shows the corresponding result of a three fingers device. The developed numerical equations precisely provide the thermal characteristics in the simulation for both devices and accurately predict the collector current slope, even at high power dissipation region. Thermal resistance for steady state condition can be computed using $Q_0 = P_0(t)/(\pi a^2 L)$; and applying impedance

concept in (3.3) as,

$$R_{th}(r) = \begin{cases} \frac{1}{2\pi\kappa L}\left\{\ln\frac{b}{a} + \frac{1}{2}\left[1 - \left(\frac{r}{a}\right)^2\right]\right\} & 0 \le r \le a \\ \frac{1}{2\pi\kappa L}\ln\frac{b}{r} & a \le r \le b \end{cases} . \tag{3.19}$$

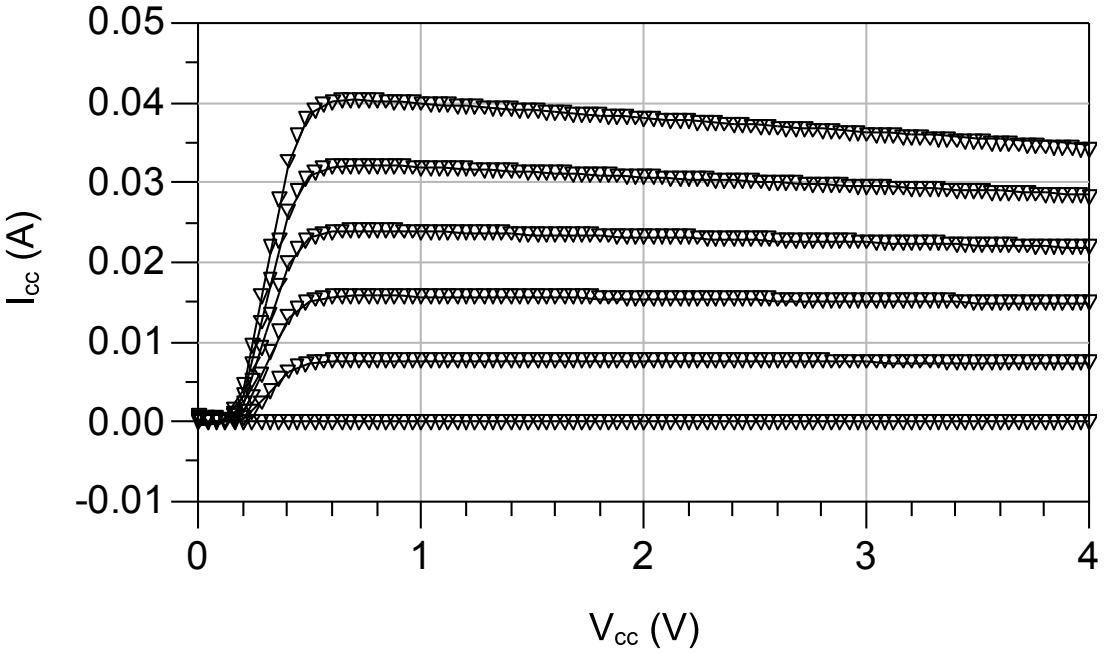


Figure 3.7: Measured (symbol) and simulated (solid line) collector current versus various collector voltages for different base biases for $1 \times 3\mu m \times 40\mu m$ HBT at base plate temperature 125°C.

3.4.2 Sinusoidal Thermal Wave

To analyze dynamic thermal behavior of a transistor, we first consider sinusoidal heat source for equations (3.10) and (3.11). By assuming the solution form as in [95],

$$T(t, r) = T_r(r)T_t(t) = T_r(r)e^{i\omega t} \tag{3.20}$$

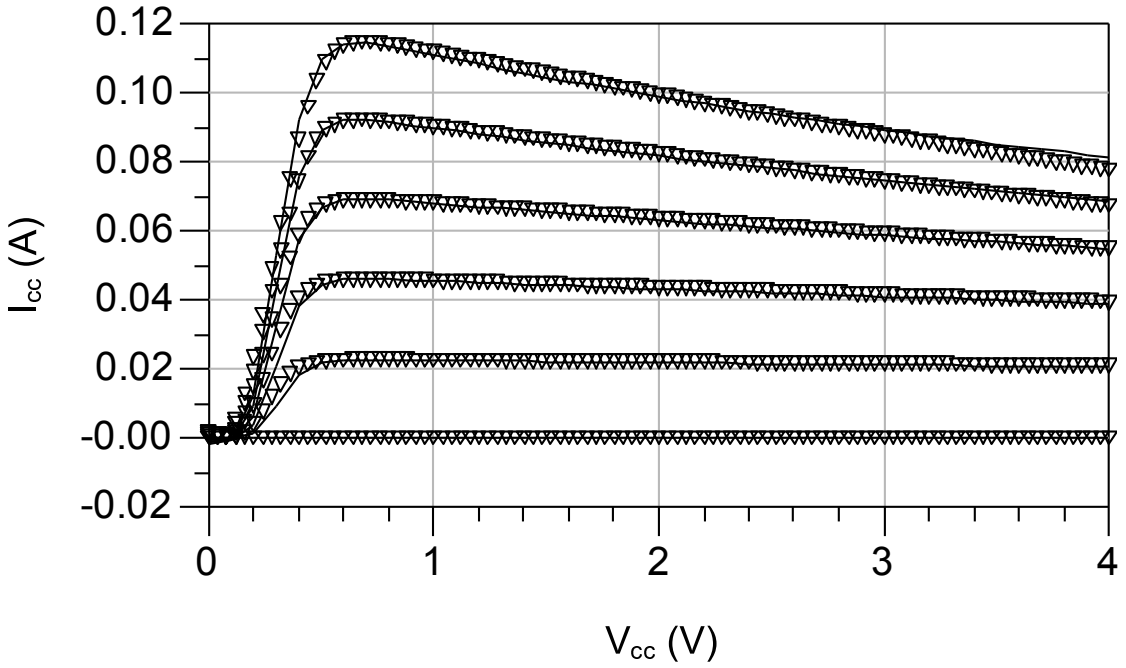


Figure 3.8: Measured (symbol) and simulated (solid line) collector current versus different collector voltages for various base biases for $3 \times 3\mu m \times 40\mu m$ HBT at base plate temperature 125° C.

Pure AC thermal sources (having negative heat dissipation) cannot exist in reality, however, the frequency response can be measured experimentally [79]. By substituting (3.20) into (3.10) and (3.11), frequency domain heat conduction equations for cylindrical coordinates [95] are defined as,

$$\frac{\partial^2 T_{r1}(\omega, r)}{\partial r^2} + \frac{1}{r}\frac{\partial T_{r1}(\omega, r)}{\partial r} - q^2 T_{r1}(\omega, r) = -\frac{Q_0}{\kappa} \tag{3.21}$$

$$\frac{\partial^2 T_{r2}(\omega, r)}{\partial r^2} + \frac{1}{r}\frac{\partial T_{r2}(\omega, r)}{\partial r} - q^2 T_{r2}(\omega, r) = 0 \tag{3.22}$$

with, $q^2 = i\omega/\alpha_T$.

Equations (3.21) and (3.22) are non-homogeneous and homogeneous modified Bessel functions respectively. The general solution to non-homogeneous partial

differential equation can be express as a superposition of a particular solution to non-homogeneous version and general solution of homogeneous equation. Hence, the general solutions can be written in the forms,

$$T_{r1}(\omega, r) = T_{r1P} + C_1 I_0(qr) + C_2 K_0(qr) \tag{3.23}$$

$$T_{r2}(\omega, r) = C_3 I_0(qr) + C_4 K_0(qr) \tag{3.24}$$

where, T_{r1P} is the particular solution of $T_{r1}(\omega, r)$, $I_x(qr)$ and $K_x(qr)$ are first and second kind of modified Bessel solutions and are shown in Fig. 3.9 for $x = 0,\ 1,\ 2,\ 3$. The particular solution can be defined by setting left hand side of (3.21) as a constant and can be computed as [95],

$$T_{r1P} = Q_0/kq^2 \tag{3.25}$$

assuming that finite temperature rise in the heat source at $r = 0$ by power dissipation. Then the appropriate boundary conditions for homogeneous equations can be written as,

$$T_{r1} = finite \qquad \text{at } r = 0, \qquad T_{r2} = 0 \qquad \text{at } r = b, \tag{3.26a}$$

$$T_{r1} = T_{r2} \qquad \text{at } r = a, \qquad ,\frac{dT_{r1}}{dr} = \frac{dT_{r2}}{dr} \qquad \text{at } r = a, \tag{3.26b}$$

As $I_0(qr)$ and $K_0(qr)$ are exponentially growing and decaying functions, $T_{r1} = finite$ is only possible when $C_2 = 0$ at $r = 0$ and (3.23) becomes,

$$T_{r1}(\omega, r) = \frac{Q_0}{kq^2} + C_1 I_0(qr) \tag{3.27}$$

Then using second boundary conditions ($T_{r1} = T_{r2}$) and third boundary conditions

($dT_{r1}/dr = dT_{r2}/dr$) at $r = a$, (3.23) and (3.24) are modified and solved as,

$$\frac{Q_0}{kq^2} + C_1 I_0(qa) - C_3 I_0(qa) - C_4 K_0(qa) = 0 \tag{3.28}$$

$$q\left(C_1 I_1(qa) - C_3 I_1(qa) + C_4 K_1(qa)\right) = 0 \tag{3.29}$$

Finally using $T_{r2} = 0$ at $r = b$

$$C_1 I_0\left(qb\right) + qaK_0\left(qb\right)\frac{Q_0 I_1\left(qa\right)}{\kappa q^2} \tag{3.30}$$

From [95], for the case $v = 0$ the following hold,

$$I_0{}'(z) = I_1(z), K_0{}'(z) = -K_1(z) \tag{3.31}$$

$$I_v(z)K_{v+1}(z) + I_{v+1}(z)K_v(z) = \frac{1}{z} \tag{3.32}$$

Where,

$$I_v(z) = \frac{d^v I(z)}{dz^v} \text{ and } K_{v+1}(z) = \frac{d^{v+1}K(z)}{dz^{v+1}} \tag{3.33}$$

Applying (3.31) and (3.32) and solving the three equations (3.28), (3.29) and (3.30) give three remaining coefficients $C_1,\ C_3$ and C_4 as,

$$C_1 = -\frac{Q_0 a}{kq}\left[\frac{I_1(qa)}{I_0(qb)}K_0(qb) + K_1(qa)\right], \qquad C_2 = 0 \tag{3.34a}$$

$$C_3 = -\frac{Q_0 a}{kq}\left[\frac{I_1(qa)}{I_0(qb)}K_0(qb)\right], \qquad C_4 = \frac{Q_0 a}{kq}I_1(qa) \tag{3.34b}$$

Substituting (3.34) into (3.23) and (3.24) gives the dynamic thermal behavior directly in the frequency domain as a function of power dissipation, frequencies and radial distance r. This scheme avoids the risk of unstable solutions associated with

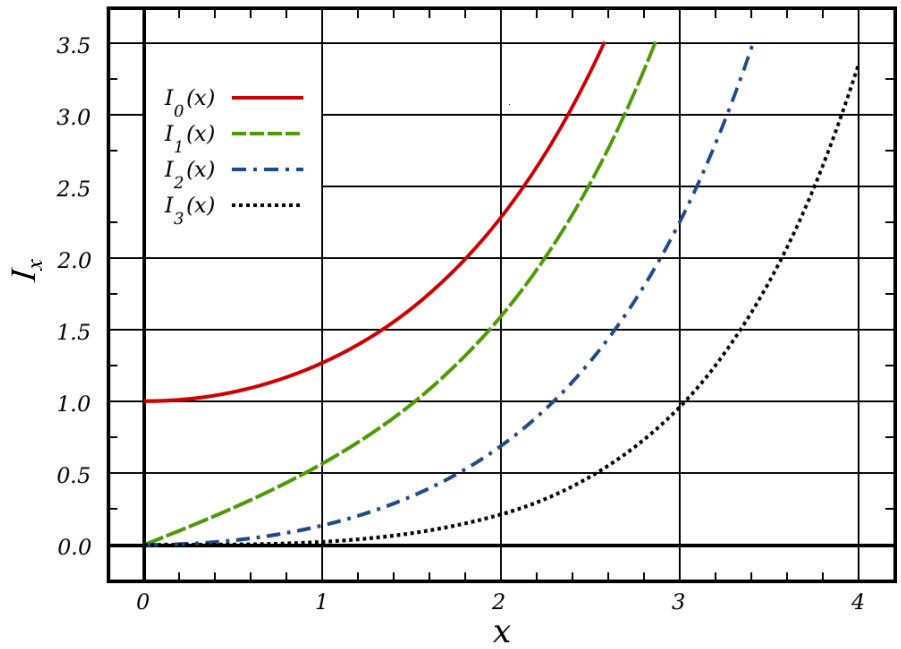
time domain and provides a complete, systematic dynamic characterization of the system [96].

As seen in (3.23) and (3.24), the solution can be express with a combination of modified Bessel solutions. Unlike the ordinary Bessel functions which are oscillating as functions of a real argument, $I_x(qr)$ and $K_x(qr)$ are exponentially growing and decaying functions respectively, shown in Fig. 3.9. Hence, when the generated heat spread out to the wider substrate, the temperature field will be attenuated and decays exponentially. Constant power dissipation can heat up both the transistor and substrate to certain steady state level.

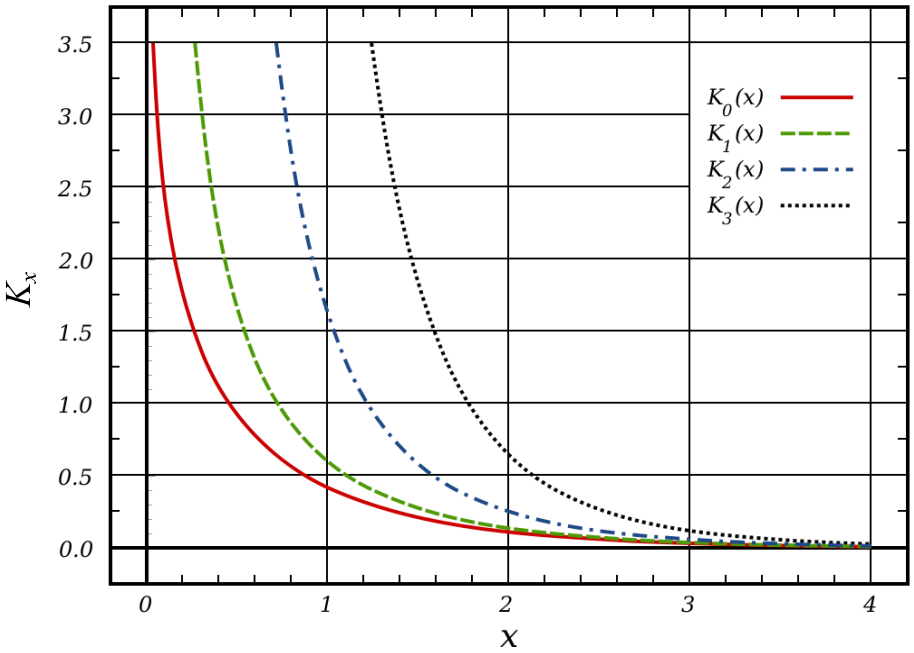
However, the frequency can be seen as an indicator inversely proportional to a temporal scale, $\omega \leftrightarrow 1/t$ and high frequency phenomena mostly relate to fast transients occurring at small time values. Meanwhile, low frequencies are most representative for slow transitions. As a result, instantaneous high frequency sinusoidal power dissipation cannot heat up the whole substrate. Instead, it only heated the substrate up to certain region. The effective radial distance, which defines the region, is often characterized by a parameter known as thermal layer thickness (δ) [93], beyond which the substrate temperature remains unchanged.

Using (3.23) and (3.24), the thermal impedance can be determined. The magnitude of the thermal impedance is nothing but the amplitude of the temperature oscillation induced by sinusoidal power dissipation at specific frequency. It can be seen as the thermal frequency response of the structure, which in fact captures the complete dynamic behavior in an elegant and efficient way. This complex quantity can be defined as,

$$Z_{th}(\omega, r) = \frac{T_r(\omega, r)}{P_0(\omega)} \tag{3.35}$$



(a)



(b)

Figure 3.9: Modified Bessel function of first kind (a) and second kind (b) for $i = 0, 1, 2, 3$.

Then, frequency dependent thermal impedance becomes,

$$Z_{th}(\omega, r) = \begin{cases} \dfrac{1}{\pi\kappa L q^2 a^2}\left\{1 - \dfrac{qaI_0(qr)}{I_0(qb)}\left[K_0(qb)I_1(qa) + I_0(qb)K_1(qa)\right]\right\} & \leq r \leq a, \\ \dfrac{1}{\pi\kappa L qa}\dfrac{I_1(qa)}{I_0(qb)}\left[I_0(qb)K_0(qr) - K_0(qb)I_0(qr)\right] & 0 \leq r \leq b \end{cases} \tag{3.36}$$

where, ω is the angular frequency of the heat source. As $Z_{th}(\omega, r)$ also varies with radial distance r, in other words heated volume, smaller effective region indicates that significant thermal impedance changes. From the thermal impedance, one can also derive equivalent thermal networks.

Moreover, as heat cannot transfer at infinite speed [95], it takes significant time for the temperature at a particular radial distance to follow the instantaneous power dissipation in the transistor. This introduces certain amount of phase lag, which is strongly depend on frequency,

$$T_r(\omega, r) = |T_r|\, e^{j\varphi_1(\omega, r)} \tag{3.37}$$

As the phases lags differ for different frequencies, this phase lag parameter is an important factor for multiple sinusoidal thermal waves such as those encountered in dynamic T_j analysis under pulse heating conditions. Various frequency components of the pulse will have different phases lag with respect to each other and hence may introduce constructive or destructive effects on the resultant thermal fields at a particular radial distance.

3.4.3 Periodic Arbitrary Analog Signals

In the case of periodic non-constant envelope analog signal input, the resultant power wave contains various baseband components below the thermal cutoff frequency. As

we analyzed frequency-dependent thermal behavior in previous section, the decomposition of the signal into its frequency components allows us to analyze thermal field generated by periodic arbitrary signals using (3.23) and (3.24).

Frequency analysis of a signal involves the resolution of the signal into its frequency components. Function $x(t)$ can be represented as a linear combination of harmonically related complex exponentials, called Fourier series [97], if it is periodic and satisfies the Dirichlet conditions. It can be written in a close form,

$$x(t) = \sum_{n=-\infty}^{\infty} c_n e^{j2\pi n F_0} \tag{3.38}$$

where, c_n $(n = 0, \pm 1, \pm 2, ...)$ are arbitrary complex constants. The signal $x(t)$ is periodic with fundamental period $T_P = 1/F_0$. Those complex constants are the Fourier series coefficients and define the frequency contents of $x(t)$. In the case of analysis, the integral for $\{c_n\}$ can be written as,

$$c_n = \frac{1}{T_P} \int_{T_P} x(t) e^{-j2\pi n F_0 t} dt \tag{3.39}$$

As a consequence of the periodicity the signal possess finite number of frequency components with equal frequency spacing of fundamental frequency. This in turn is the inverse of the fundamental period of the signal. As the coefficients, c_n, are complex valued, they can be represented as,

$$c_n = |c_n| \, e^{i\theta_n} \tag{3.40}$$

where, $\theta_n = \angle c_n$. We may also plot the magnitude spectrum $\{|c_n|\}$ and the phase spectrum $\{\theta_n\}$ as a function of frequency. In this way, we can analyze both amplitude and phase information of each frequency component. Applying Fourier analysis, the

frequency components of $P_0(t)$ can be evaluated as,

$$\begin{aligned} P_0(\omega) &= \sum_{n=-\infty}^{n=\infty} \frac{1}{T_P} \int_{-T_P/2}^{T_P/2} P_0(t) e^{-j2\pi n \Delta f t} dt \\ &= \sum_{n=-\infty}^{n=\infty} c_n = \sum_{n=-\infty}^{n=\infty} |c_n| e^{j\varphi_n(\omega)} \end{aligned} \tag{3.41}$$

The calculate amplitude and phase components of each frequency contents are used in (3.23) and (3.24) to evaluate dynamic temperature response to arbitrary shape periodic power waveform heating. The vectorial combination of the temperature responses contributed from each component gives complete dynamic thermal behaviors of the transistor in frequency domain. The total phase shift at a particular frequency shown in (3.37) becomes,

$$T_r(\omega, r) = |T_r| \, e^{j\varphi(\omega,r)} = |T_r| \, e^{j\varphi_1(\omega,r)+\varphi_n(\omega)} \tag{3.42}$$

3.4.4 Aperiodic Pulse Signals

Pulsed current-voltage (IV) is widely used to decouple thermal-electrical interaction in characterization of a transistor. Wide range of pulse widths, from millisecond to sub-nanosecond, is used in characterization for different applications. [98] report that self-heating effect is still significant, even when the pulse width used to characterize the transistor is reduced to hundreds of nano-second. Isothermal behaviors of the transistor are observed when the pulse width is 40ns. However, the quiescent thermal state of the transistor is accurately preserved, when the pulse width is as short as 0.2ns [99]. By doing so, electrical performance of the transistor without coupling with thermal is observed. The impact ionization effect, the safe operation area beyond fly-back and the performance of high power amplifier are characterized without being

complicated by the self-heating effect [99]. Without self-heating, high current and high voltage characteristics are governed by Kirk effect and impact ionization [99].

[98, 99]have reported possibilities of junction temperature excursion when large envelope amplitude signal is applied with short time duration in a transistor. Particularly, this is the case in multi-carrier communication systems and pulse radar systems. In these systems, transistors are heated up by high amplitude square pulses or parabolic pulse spikes generated by multi-carrier multiplexing like OFDM [100]. The pulse widths are in the range of tens of nano-seconds to tens of micro seconds. That duration may be short enough to heat up the transistor and the substrate. Another factor to consider is the amplitude of the signal, which is generally neglected in transient thermal analysis. Pulse power dissipation of 10dB above the average power level, can cause substantial temperature rise.

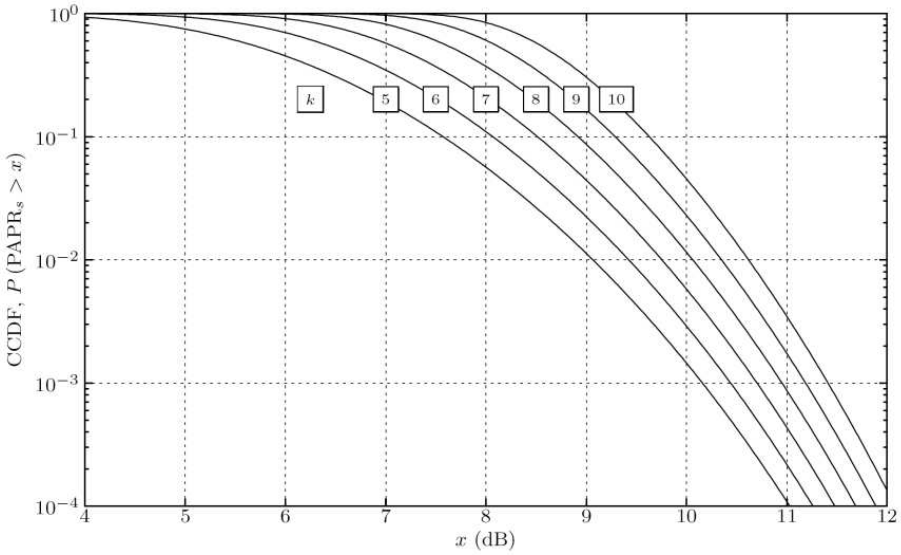


Figure 3.10: Complementary cumulative distribution function (CCDF) for PAPR of OFDM system [101].

Junction temperature variation in a transistor is a sign of nonlinear transfer behavior and will introduce distortions to the signal. Understanding transient ther-

mal behaviors induced by pulse input signal is very important for modern PA. Figure 3.10 shows the complementary cumulative distribution function (CCDF) for PAPR of OFDM system. The figure shows that occurrence of large peaks is very low. So, it is more convenient to treat the signal for our dynamic thermal analysis as an aperiodic pulse.

In previous section, frequency decomposition is carried using Fourier series analysis. Equation(3.41) can be adopted for arbitrary shape aperiodic signal. Considering a periodic pulse signal $x(t)$ with finite duration, we can create an aperiodic pulse signal by setting the limit on the period $T_P \rightarrow \infty$ in (3.41) and apply the Fourier transform to obtain the spectrum of aperiodic pulse signal. By following the procedure used in [97], the Fourier transform for a periodic pulse signal,

$$P_0(f) = \int_{-\infty}^{\infty} P_0(t) e^{j2\pi ft} dt \tag{3.43}$$

The spectrum in this case is continuous.

3.5 Simulation Using MATLAB

A cylindrical heat source, which is volumetrically equivalent to a real single finger HBT is simulated in Math Lab using the structure and material of the device presented in section 3.3. The HBT is biased in class-C and driven by the signal input initially with collector current of 11mA at 3.6V which corresponds to 40mW of power consumption (reference dissipative power level). Subsequently, an input signal is increased such that the dissipated power increases by 2 times, 4 times and 10 times relative to the reference. These power levels will be referred to as 0dB, 3dB, 6dB, and 10dB respectively.

Frequency dependent temperature variation in the transistor and substrate for

four different power levels are computed at 10kHz, 100kHz, 1MHz, 10Mhz, 20MHz and 30MHz frequencies. For each chosen frequency and power level, T_r the temperature at various radial distances from the junction is computed numerically, using the aforementioned analysis. The calculated $T_r(\omega, r)$ at $r = a$ as a function of frequency is plotted in Fig. 3.11.

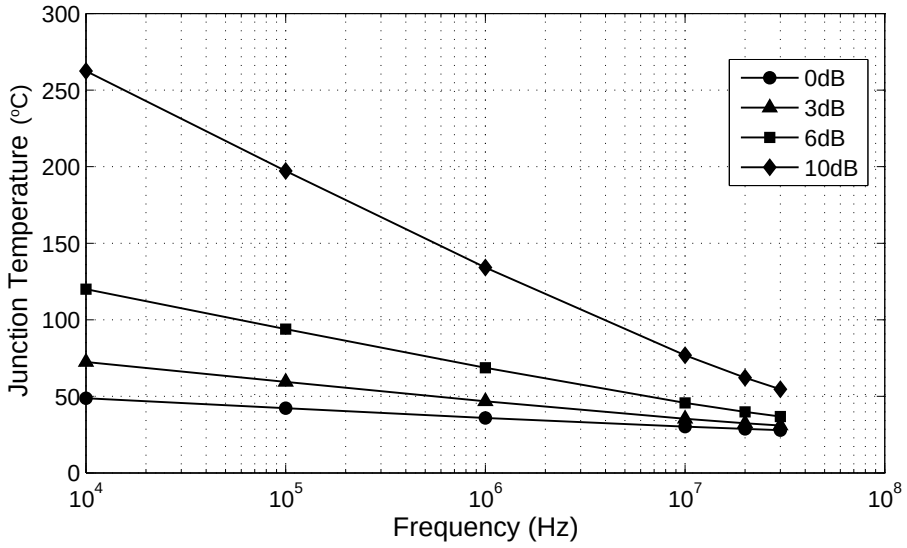


Figure 3.11: Calculated frequency dependent junction temperature at different power dissipation levels.

The results show that as the frequency (f) increase from 10kHz to 30MHz at fixed power dissipation, $T_a(\omega, a)$ drops linearly with log (f). It is also noted that T_a rises from 48^oC to 262^oC for 10kHz input signal at 10dB power overdrive. However, if the input signal frequency increases to 30MHz at the same power overdrive, T_a increases from 27^oC to 54^oC. As predicted in the analysis, these results show that there are significant dynamic temperature changes in the transistor.

Figure 3.12 shows the temperature distribution along the radial direction into the substrate at 10dB power level for different frequencies. The attenuation rate increases with frequency and effective radial distance is reduced. Figure 3.13 shows

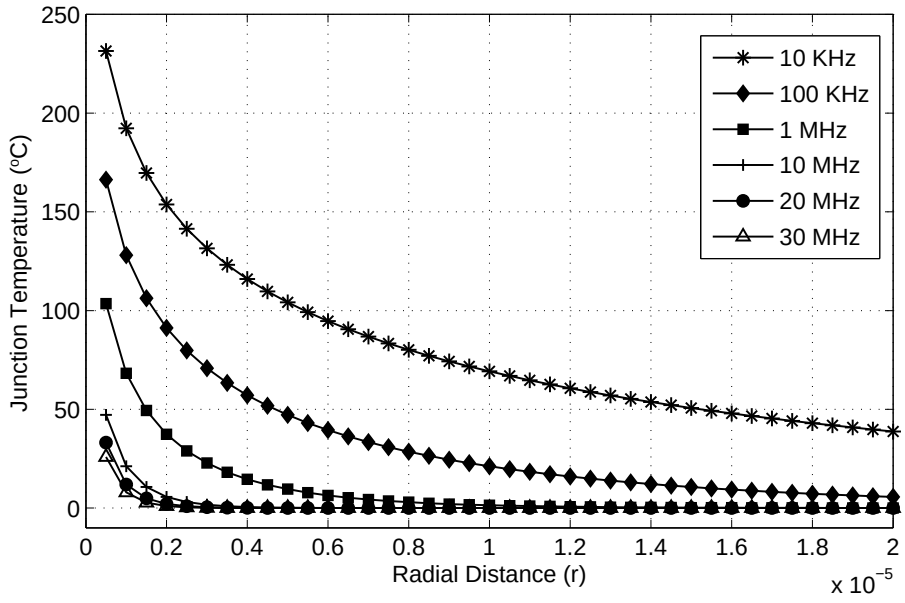


Figure 3.12: Frequency-dependent temperature distribution into GaAs substrate, at 10dB.

the computed phase lag at the junction radial distance, $r = a$, at different frequency. However, the phase doesn't change with power.

Figure 3.14 shows the ac thermal impedance Z_{th} which is a complex frequency dependent parameter at the junction radial distance, $r = a$. Frequency-dependent nonlinear thermal impedance is clearly observed. This correlates well with thermal impedance analyzed by [79, 102]. In reality, Z_{th} is varying with power through temperature-dependent thermal conductance κ. However, isotropic assumption in this analysis makes it power independent.

Dynamic thermal response to square pulse signal input to the transistor is analyzed. Pulsed widths (τ) ranging from 10ns to 100μs with PRF of 1kHz, are selected for the analysis at various power levels. To isolate the steady state heating effect, the analysis is conducted neglecting the average DC power level. The amplitude and phase of each frequency component of the pulse signal are determined based on (3.41) and (3.42

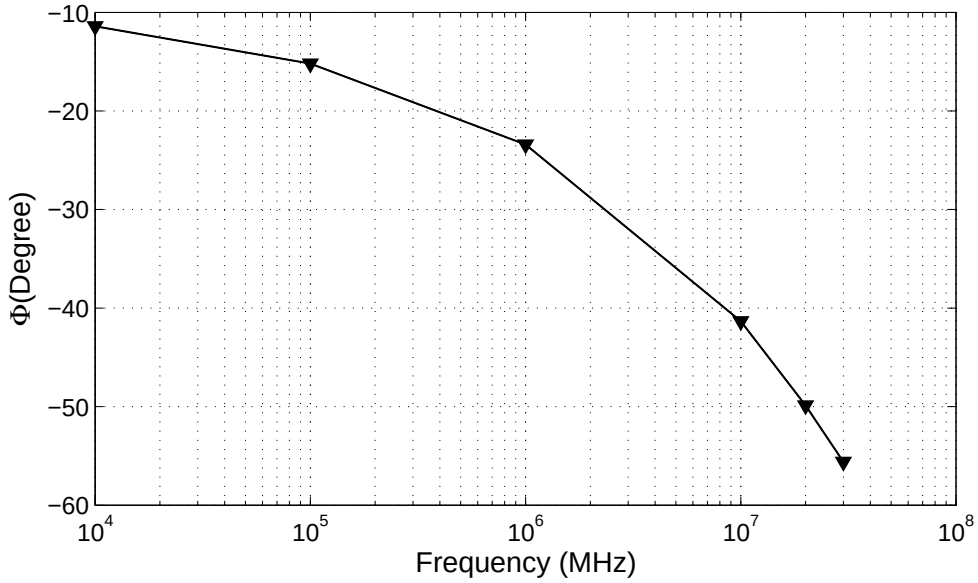


Figure 3.13: Frequency-dependent phase lagging of thermal wave in GaAs, at $r = a$.

), with finite number of frequency components.

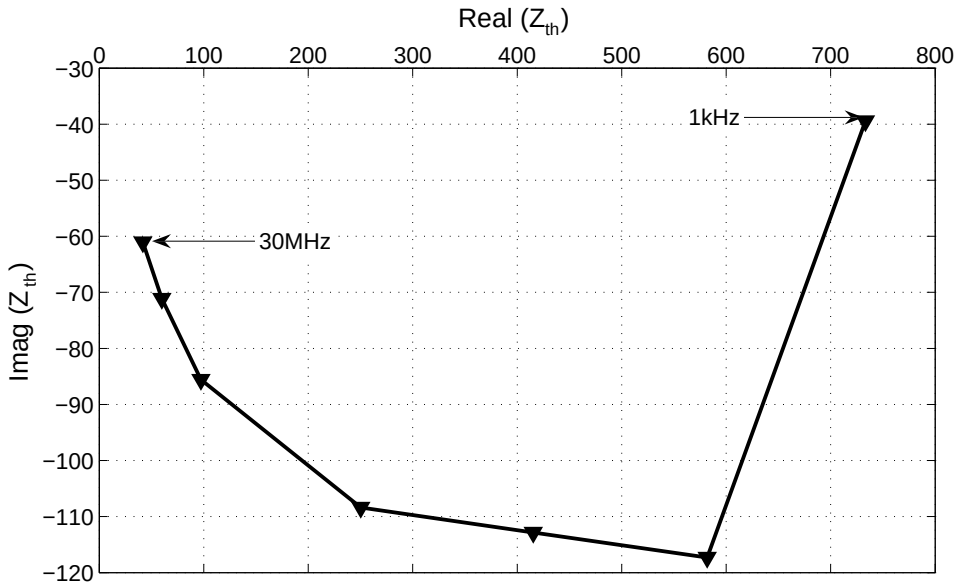


Figure 3.14: Calculated frequency - dependent nonlinear thermal impedance of the single finger $1 \times 2\mu m \times 20\mu m$ transistor.

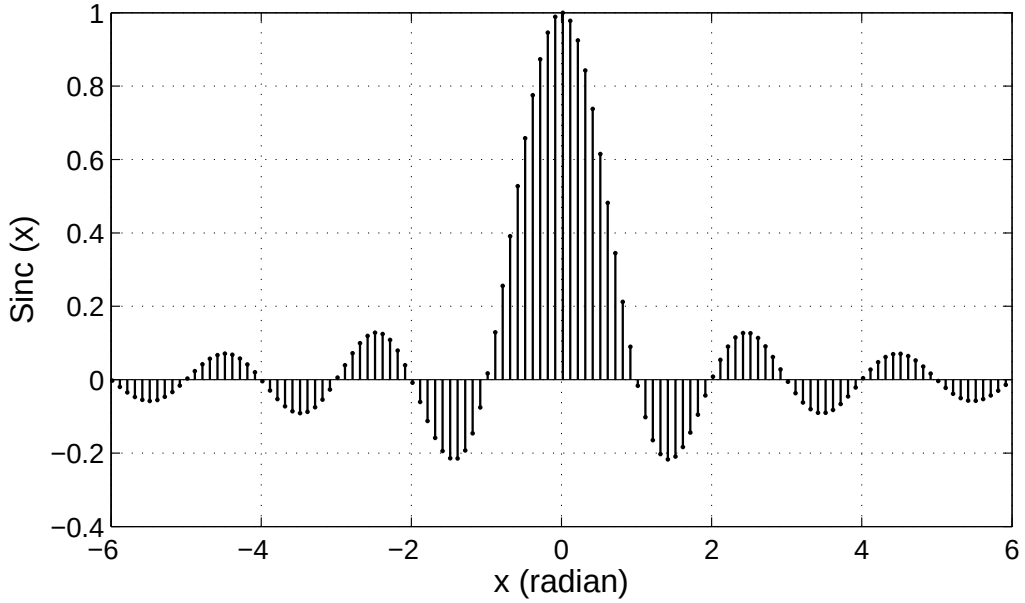


Figure 3.15: Normalized and truncated Fourier coefficient of a square pulse.

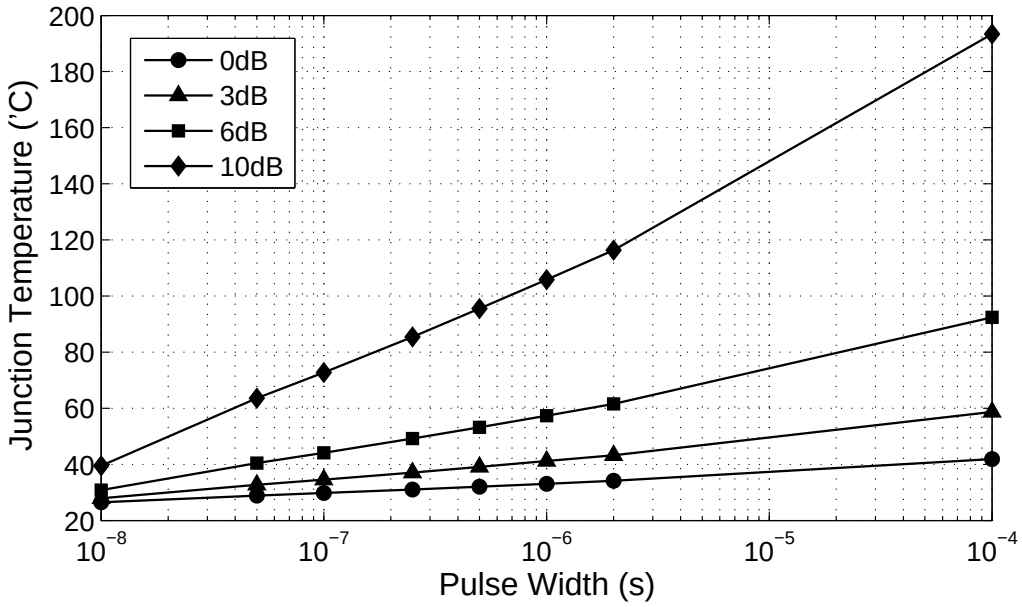


Figure 3.16: Computed junction temperature for various pulse widths at different power levels.

Figure 3.15 shows the normalized amplitude and phase spectrum of c_n in a single graph. Fourier coefficients, c_n, of the square pulse are real and consequently,the phase spectrum is either zero, when c_n is positive, or π when c_n is negative. $T_a(\omega, a)$ is then calculated at every frequency components (except DC) within a truncated range. The temperature contributed from each frequency components are summed up in a vector form.

Figure 3.16 shows the computed $T_a(\omega, a)$ as a function of pulse width and power. The results show that as pulse power increases from 0dB to 10dB, $T_a(\omega, a)$ is raised to 40^oC for 10ns pulse, 72^oC for 100ns pulse, 105^oC for $1\mu s$ and to 193^oC by $100\mu s$. Temperature increases only slightly for 10ns pulse. This is because; the dissipation time is too short, though power is 10dB higher than average power level, to heat the transistor up.

3.6 Validation thru Measurement

3.6.1 Measurement Setup

To validate the analysis, time domain on wafer measurement is carried out using $1 \times 2\mu m \times 20\mu m$ InGaP/GaAs HBT, shown in Fig. 3.4. We introduce a novel measurement setup where both pulsed base and collector can be applied. Matched load conditions with DC signal coupling are provided at both the base and collector monitoring circuits for measurements with a wide range of pulse width from DC to a few ns. The schematic and image of measurement setup are shown in Fig. 3.17 and Fig. 3.18 respectively.

A base current sensing resistor (R_{BS}) is inserted in series between the pulse generator and the base of the transistor. The voltages across R_{BS} are measured through sensing resistors R_{CH1} and R_{CH2}. Precise indication of I_b and V_{be} is mandatory in

these measurements. The values of R_{BS}, R_{CH1} and R_{CH2} are optimized for a given range of I_b and V_{be}. In these measurements, I_b is in the range of 10μA to 10mA, while V_{be} is ranging from 1.3V to 1.6V. The values used are R_{BS}=500Ω, R_{CH1}=1kΩ, and R_{CH2}=1kΩ. Similarly, R_{CS} is used to sense the collector current by measurement of the potential difference across it through sensing resistors R_{CH3} and R_{CH4}.

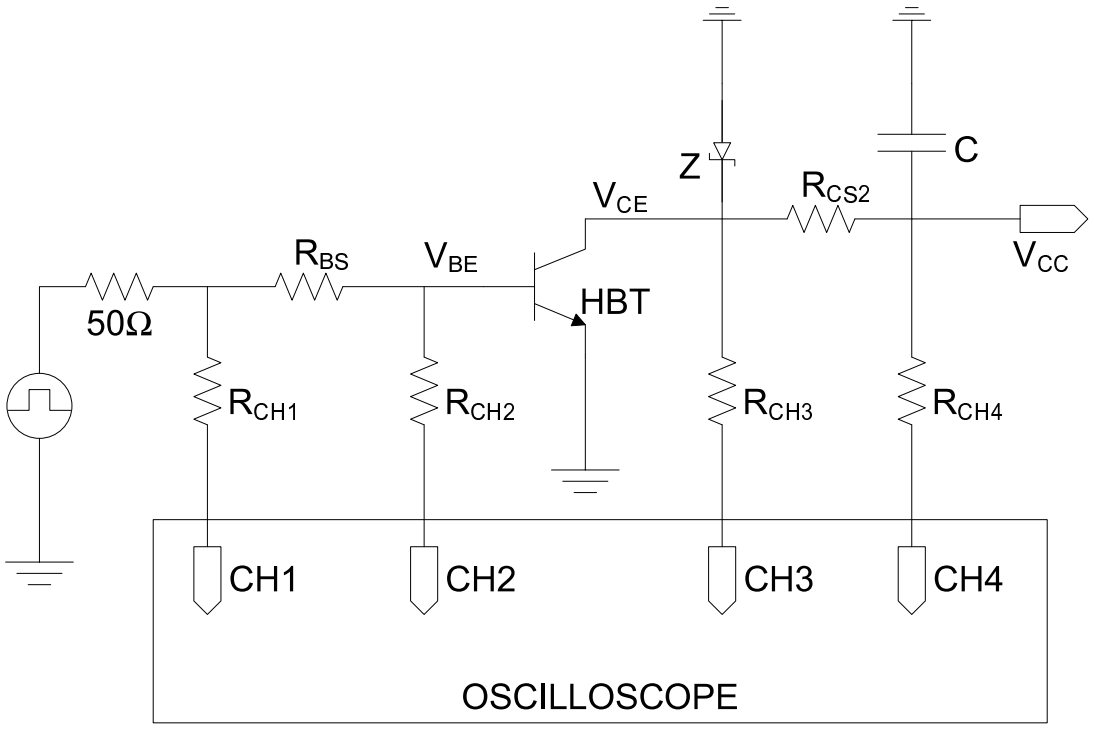


Figure 3.17: Schematic of time domain on wafer pulsed thermal measurement setup.

The value of R_{CS} should be chosen to ensure that the HBT is in a stable condition in addition to consideration of I_c measurement accuracy. In these measurements, I_c is in the range of 1mA to 200mA. The values used are R_{CS}=50Ω, R_{CH3}=1kΩ, and R_{CH4}=1kΩ. DC feed inductor is eliminated to minimize voltage spike [103]. A shunt capacitor (C) is added to provide instantaneous charges at the rising edges. A zener diode is added in shunt to prevent the HBT from damage during off period.

All sampled voltages at the oscilloscope are de-embedded to the base and collector of the HBT. 50Ω cables are used to connect the voltage monitoring points to the oscilloscope and the input impedance of the oscilloscope is set to 50Ω to prevent reflections. The HBT is biased in the common emitter configuration for Class-C operation.

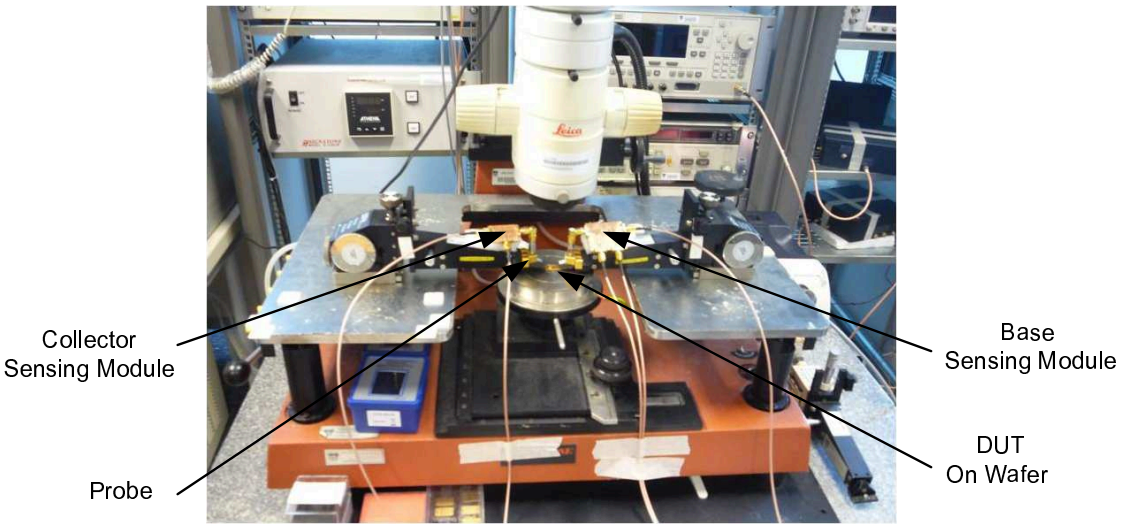


Figure 3.18: Image of time domain on wafer pulsed thermal measurement setup.

It has a cutoff frequency of 35GHz, a maximum frequency of oscillation is more than 100GHz, a common base open-emitter break down voltage (B_{VCBO}) of 30V, a common emitter open-base breakdown voltage (B_{VCEO}) of 16V and a common emitter open-collector breakdown voltage (B_{VBEO}) of 7V.

3.6.2 Thermal-Dependent V_{be} Characterization

Temperature dependency of V_{be} is measured. V_{be} variation with temperature is measured at fixed I_b by using a Semiconductor Parameter Analyzer (SPA). The base plate temperature of the HBT is varied from 25°C to 120°C using a heated platform and V_{ce}

is varied from 1V to 4.5V with 0.5V step. Figure 3.19 shows measured V_{be} at different power dissipation. Results show that V_{be} reduce as base plate temperature and power dissipation increases. It is also noted that V_{be} is a nonlinear function of power and it drops down linearly with temperature at around 1.3mV/^oC as shown in Fig. 3.20.

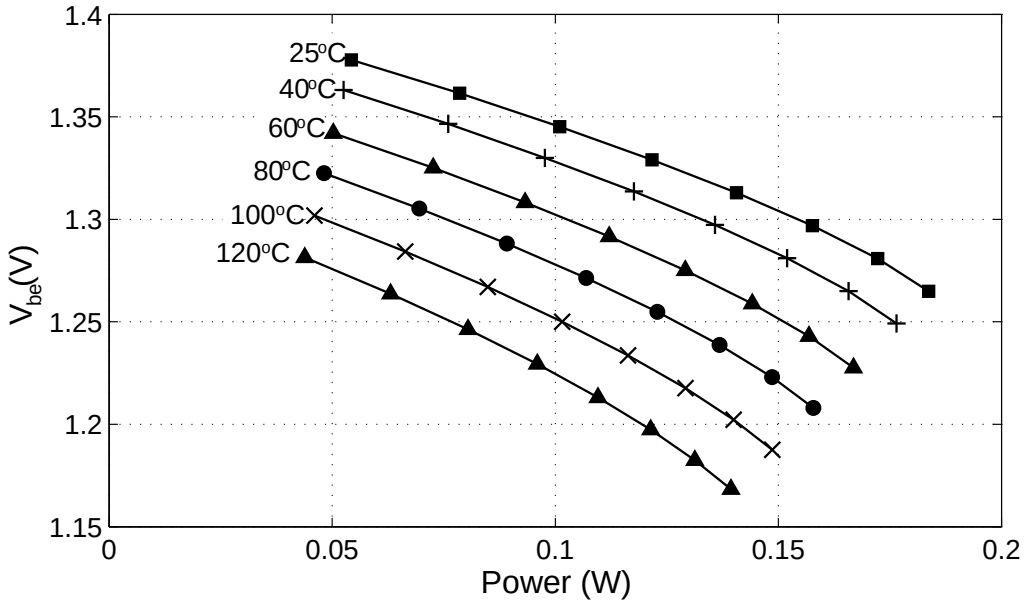


Figure 3.19: Measured V_{be} at various power levels and different base plate temperatures.

3.6.3 Time Domain Pulsed Characterization

In section 3.3.5 we discussed about device characterization using pulses for isothermal condition to analyze electrical behavior of a transistor. Base on the pulse width used for characterization, thermal coupling effect can be identified. As thermal-electrical interaction is much stronger in PA, it is worth to characterize the dependency of current gain (β_i) and V_{be} on temperature, which is induced by pulse power dissipation. Current gain fall-off and V_{be} lowering are significant nonlinear mechanisms for bipo-

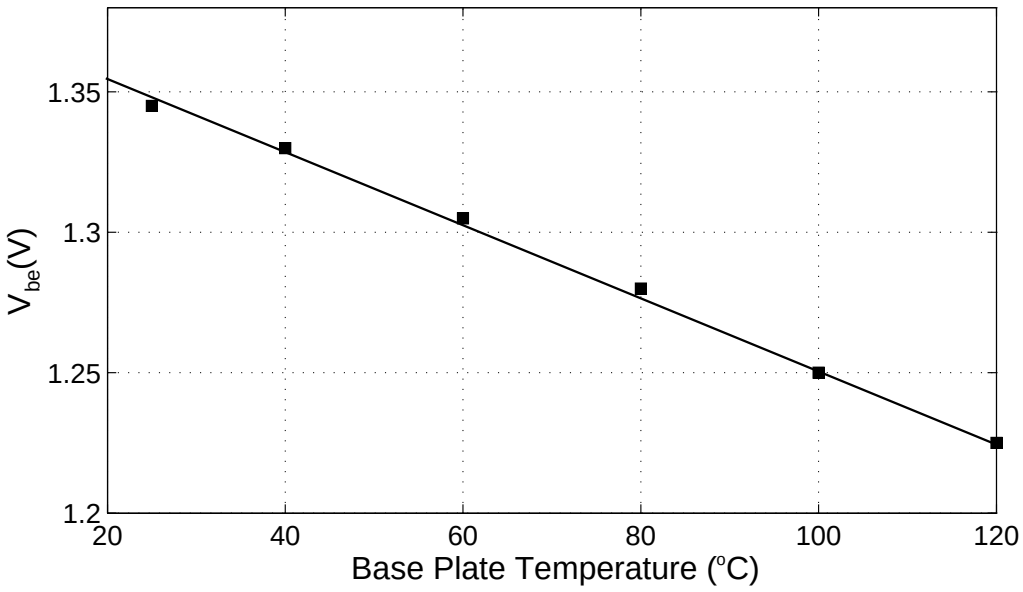


Figure 3.20: Measured V_{be} variation as a function of base plate temperature at power dissipation of 100mW.

lar transistors. Those set an upper bound to the operating current, which is very important in identifying the maximum output power for PA, and determine linearity characteristic of PAs.

Pulse thermal characterization would unveil the bandwidth dependent nonlinear behaviors of the transistor. Five-fold of I_c increment over Kirk is reported in [104], when approaching isothermal operation. In [99], sub-ns pulse is used to isolate heating effects and a much larger safe operating area was observed. However, self-heating dependent characteristics of β_i and V_{be} are unavailable.

The setup shown in Fig. 3.18 is used to investigate self-heating induced nonlinear characteristics through isothermal, semi-isothermal and self-heated situations. Base-collector voltage is preserved at $V_{bc} = 0$ to minimize the contribution of Kirk effects in β_i measurement and to minimize power dissipation across base-collector junction. This ensures that the power is solely dissipated in the base-emitter junction. The

HBT is biased in the common emitter configuration for class-C operation.

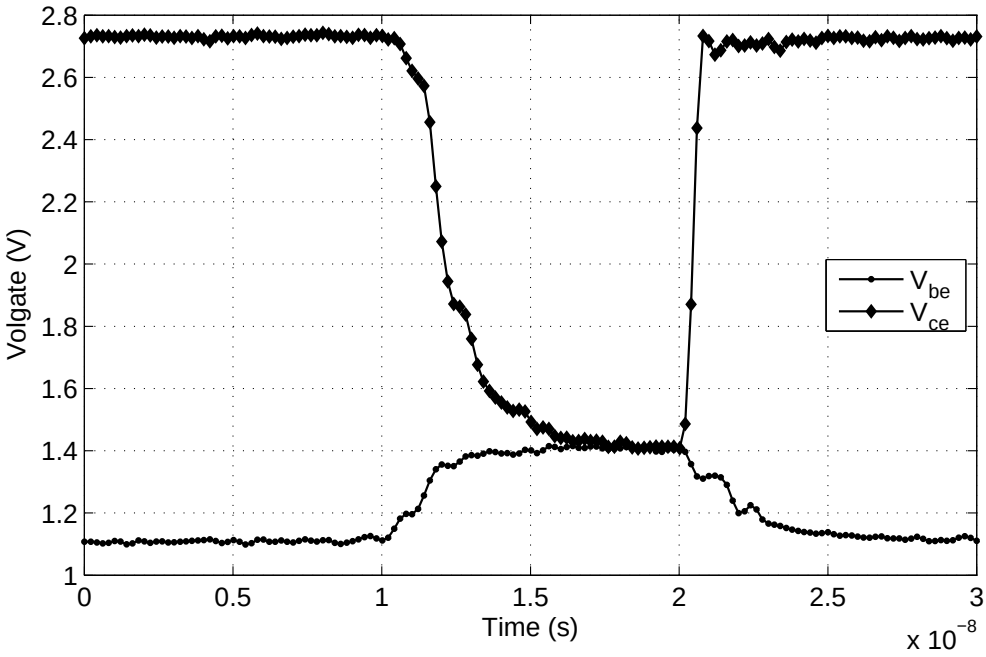


Figure 3.21: Measured time domain pulse response for 10 ns input with constant V_{ce}.

The input pulse widths ranging from 10ns to 100μs are selected for this identification to cater for wide range of signal bandwidth. A sample measured time domain pulse response for 10ns input with constant V_{cc} is shown in Fig. 3.21. To eliminate heat accumulation effect, PRF of 10Hz is set with 100μs pulse width while 1kHz PRF is used for other pulse width. The pulses are superimposed with 1.1V DC generated from a HP8131A pulse generator and applied to the base. A DC power supply is directly connected to V_{cc} and is adjusted so that, $V_{be} = V_{ce}$ ($V_{bc} = 0$) is maintained for all pulse amplitudes.

Measurements are conducted at three different power levels: 0dB, 3dB and 6dB above 40mW. However, due to limitations of equipment's power handling 10dB power level is dropped from the measurement.

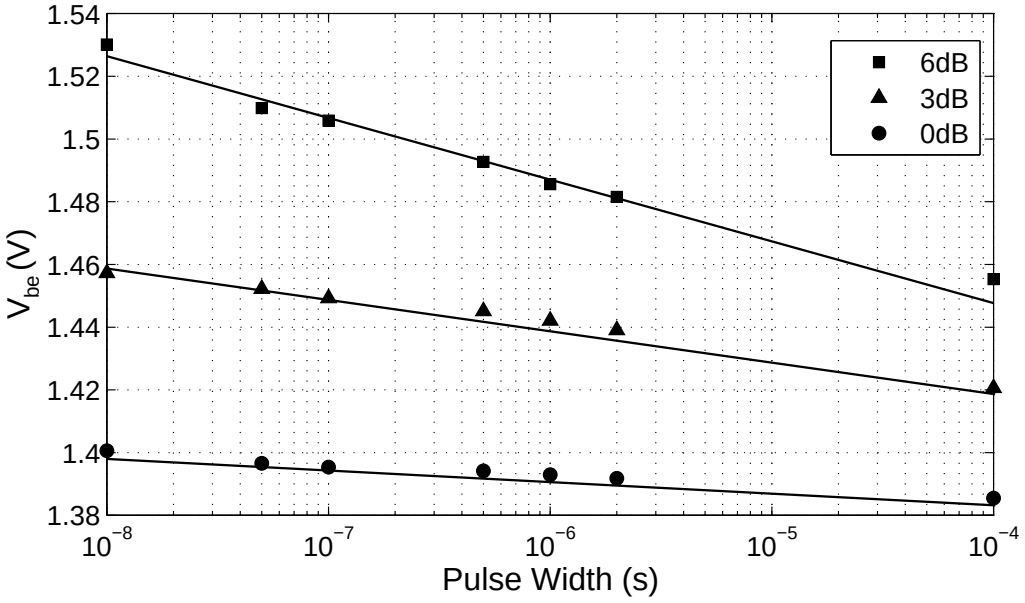


Figure 3.22: V_{be} variation under pulsed measurements at different power levels.

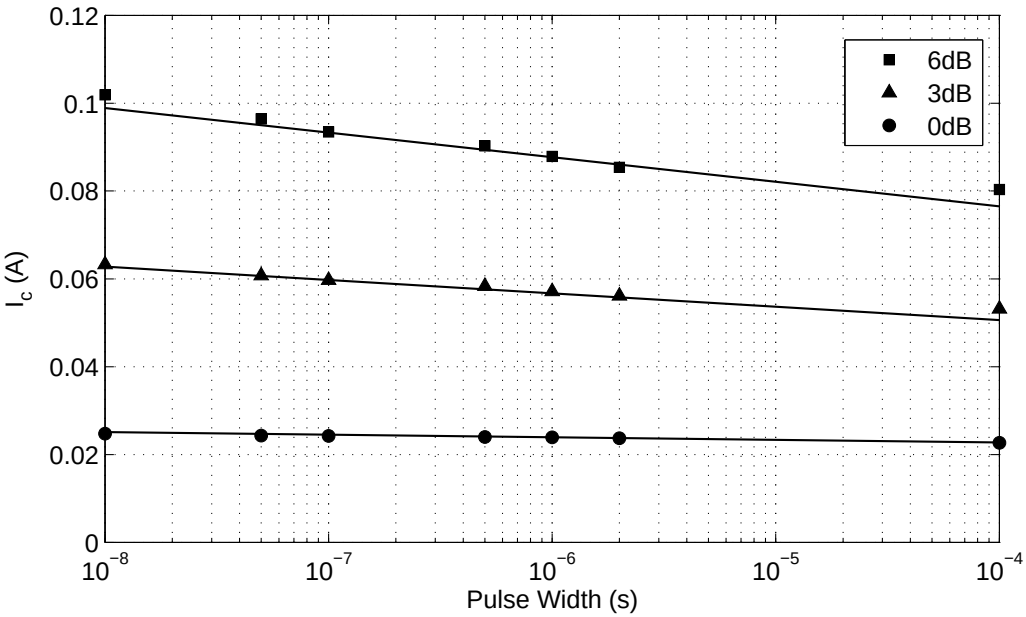


Figure 3.23: Corresponding I_c variation under pulsed measurements at different power levels.

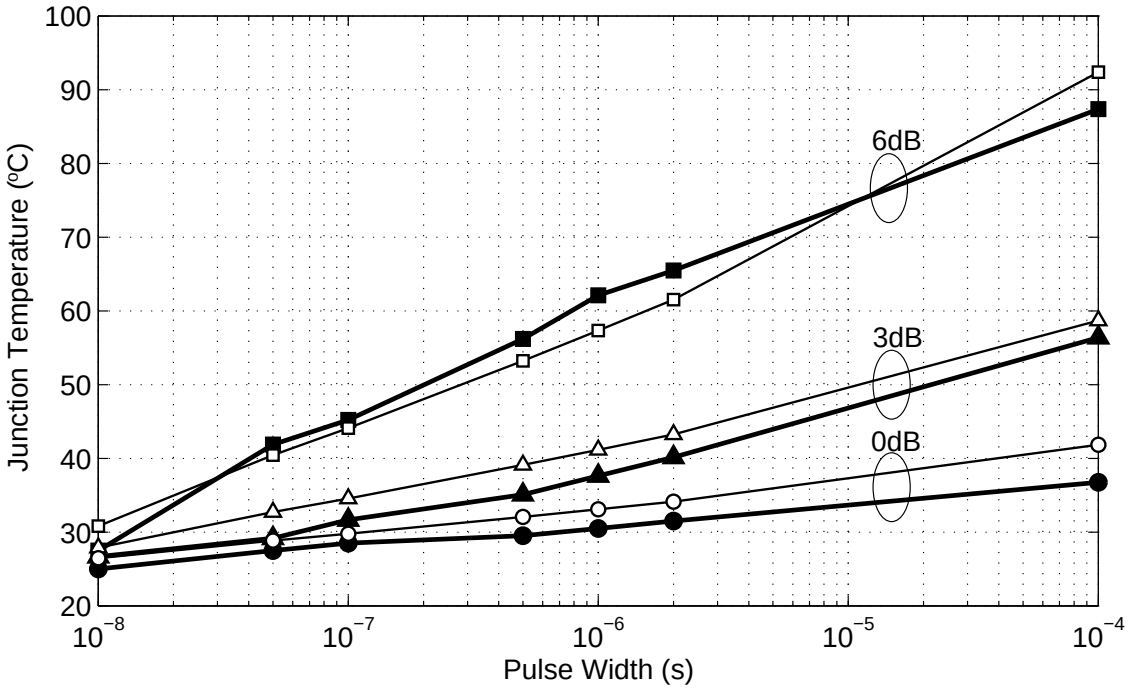


Figure 3.24: Junction temperature (T_j) measured (black symbol) verses analytically predicted (white symbol) at different power levels.

Base-emitter voltage V_{be} , I_b and I_c are monitored for different input pulse widths. Figure 3.22 shows V_{be} variation under pulsed measurements at three different power levels. The corresponding I_c are shown in Fig. 3.23. Results show that, V_{be} drops by 15mV, 37mV and 75mV with increasing pulse width from 10ns to 100μs, for 0dB, 3dB and 6dB power levels, respectively. Meanwhile, the collector currents drop 2mA, 10mA and 21mA accordingly.

As shown in earlier analysis, 10ns pulse with 0dB power level is short enough to ensure that the transistor is not heated up and isothermal condition is set. The response of the transistor in this case can be assumed to be purely electrical. Hence, the base-emitter voltage corresponding to 10ns pulse with 0dB power level is taken as a reference. Assuming a V_{be} temperature dependent coefficient of 1.3mV/^oC, the

junction temperature T_j is extracted from the measured data. Figure 3.24 shows the extracted T_j from measurement and analytically predicted. Close agreements between measured and analytically predicted junction temperatures of within 5^oC is observed.

3.7 Dynamic Thermal Equivalent Circuit Model

Thermal networks are widely used for modeling heat conduction problems in components and packages. Static heat conduction has been modeled using first order thermal network presented in section 3.2. However, for highly miniaturized devices, (3.4) becomes inaccurate and hence also for the thermal impedance (Z_{th}) network which is deduced from it. As discussed before, different power dissipation periods penetrate into the substrate with different depths and will have multiple temperature variation with time profiles. Multi-section thermal network model is proposed for transient thermal simulation. In [39], different forms of one port passive distributed thermal networks are systematically analyzed.

Two different generalized canonical forms of lumped RC networks are reported in literature for modeling thermal impedances. Detail analysis of these canonical forms are presented in [39]. Foster canonical form is a network composed by the series connections of an infinite number of sub-networks, each of which is a circuit connecting a resistor and a capacitor in parallel. Figure 3.25 shows an equivalent distributed electrical network representing thermal diffusion using Foster form. The Foster circuit is only a behavioral description of the subsystems and not a true physical description. The heat propagation through the Foster circuit is instantaneous [105].

Cauer form, on the other hand, is a combination of node-to-node resistors and node to ambient (grounded) capacitors. Figure 3.26 shows the Cauer form. Cauer form is highly preferable from a physical point of view because the network elements are then

directly associated with the thermal conduction and energy storage in the elementary sections of the heat flow path [96]. Both forms of the ladder network are mathematically equivalent, in the sense that they have the same input impedance. However, the mathematical representation of the Cauer form is much more complicated and it is difficult to determine the Cauer network parameters.

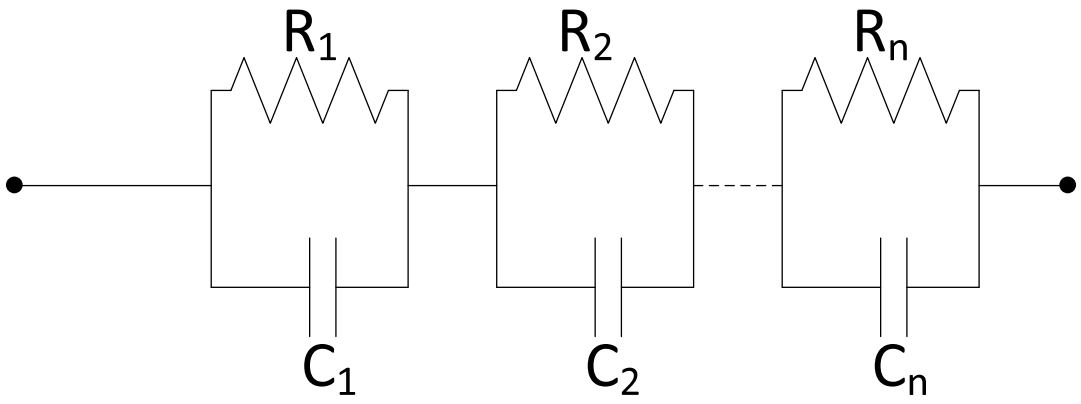


Figure 3.25: Distributed thermal equivalent circuit, Forster canonical form.

In previous sections, we discussed the relation between the dissipated power and the temperature rise in term of thermal impedance over wide range of frequency. These impedances are implemented in ADS as a Cauer form. The first capacitor C_1 and R_1 is defined at the highest frequency of interest $\omega \rightarrow \omega_{high}$. The total resistance of the series connections of the Cauer form is

$$R_0 = \sum_i R_i \tag{3.44}$$

and R_0 is defined at $\omega \rightarrow 0$ [39]. Then, computed thermal impedances are implemented in ADS using six sections Cauer form for circuit simulation. The value of R and C used are presented in Table 3.1. The impedance variation of the distributed thermal

equivalent circuit simulation results are compared with computed thermal impedances at various frequency points.

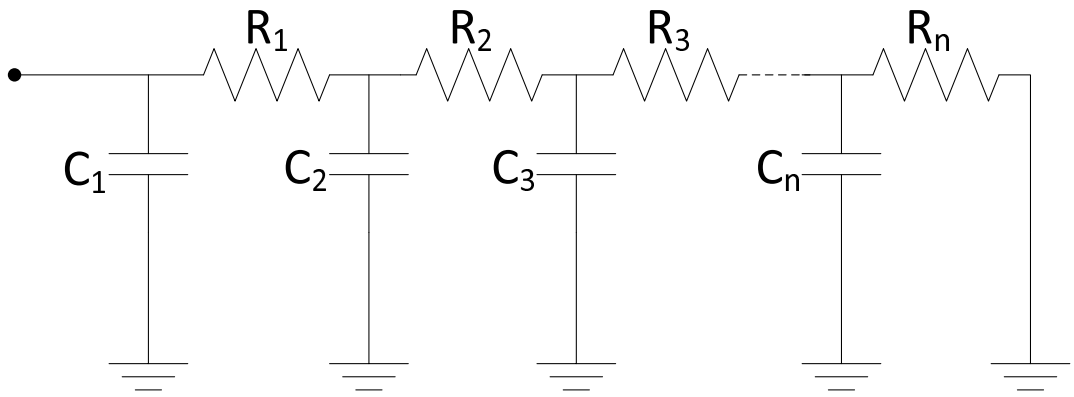


Figure 3.26: Distributed thermal equivalent circuit, Cauer canonical form.

Table 3.1: The values of resistances and capacitances used in distributed thermal equivalent circuit.

Parameter	Value	Parameter	Value
R1	1.5Ω	C1	.5nF
R2	44.5Ω	C2	1.1nF
R3	76.5Ω	C3	3nF
R4	82.5Ω	C4	31.5nF
R5	75Ω	C5	293nF
R6	40Ω	C6	8μF

Figure 3.27 shows the overlay plot of simulated circuit model and numerically computed thermal impedance at different frequency values. The circuit model closely

follows the computed impedance variation. In addition the circuit model is also satisfied for the static case. Hence, the developed model is useable for both static and dynamic cases and can be integrated with large signal model compact circuit simulation.

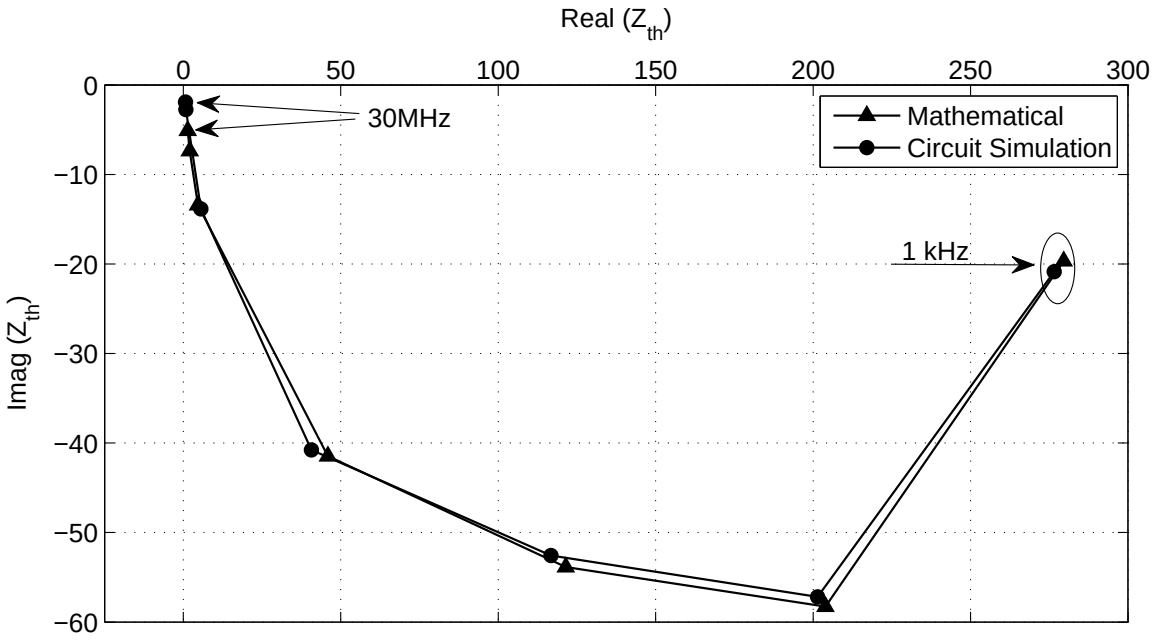


Figure 3.27: Comparison of numerically computed and circuit model simulated thermal impedance as a function of frequencies.

3.8 Conclusion

In this chapter, self-heating effects associated performance degradations are discussed and shortfall of current first order thermal network, especially for dynamic self-heating, is examined. Heat distribution into GaAs substrate is analyzed in cylindrical coordinate. The distribution characteristics under CW signal, periodic arbitrary signal and aperiodic signal power dissipation are numerically derived and formulated. Pulsed heat distribution analysis allows RF engineer to accurately predict the dynamic junc-

tion temperature of HBT under short period excessive heating. The analysis is applicable to a wide range of signal types, power levels, frequencies, substrate position and material properties. Time domain on-wafer pulsed thermal measurement setup is developed to probe short period excessive heating effects and thermal analysis have being validated. Finally, higher-order thermal equivalent circuit is implemented using Cauer canonical form for circuit simulation purpose.

Chapter 4

Small-Signal Unilateral Modeling

4.1 Introduction

As discussed in Chapter 2, developing a unilateral circuit model for InGaP/GaAs HBT over a wide range of frequency is important to accurately utilize developed techniques and formulae. Despite the fact that large-signal model is provided by foundry service, small-signal unilateral circuit model development is not a very straight forward one. It includes intensive parameter extraction to achieve small-signal bilateral circuit model first and the parameter are extracted from bias dependent S-parameter measurements. Hence, solid understanding of parameter extraction procedures is needed. Upon successful parameter extraction for bilateral circuit model, a unilateral circuit model is developed analytically. The developed unilateral circuit model is then validated with bilateral large-signal models response under small-signal conditions.

4.2 Measurement Setup and Circuit Topology

The device models are highly dependent on the accuracy of the measurement techniques employed to characterize the device. Dealing with real-life measurement data is different from solving exact mathematical equations in theory. This characterization is associated with random and systematic errors, occurring in the measurement. Example of random errors are noise, drift and connector repeatability. They cannot be characterized and removed. However, they can be minimized by averaging the measurement data. On the other hand, systematic errors are stable and repeatable. They can be characterized and removed from the measurement system. In the following section, some issues related to characterization are addressed.

Modern transistors feature very low parasitic resistances and hence overlooking a few ohms may introduce large errors. All the resistances of the measurement system show up in the same way and especially at high current measurements. It is necessary to know the electrical characteristics of the measurement system. The observed current or voltage must be corrected for the resistances effects of the measurement system.

4.2.1 System Calibration

Generally, small-signal behavior of an active device is characterized in terms of S-parameters using vector network analyzer (VNA). VNA can evaluate the characteristics of the device under test (DUT) with a high level of precision. It is only as useful as the accuracy with which it makes measurements, and this requires the instrument to be calibrated. A poor calibration performance can introduce errors that otherwise would not have occurred.

Very large numbers of calibration techniques have been developed. Active device characterization generally carries out in wafer level and hence the short-open-load-thru

(SOLT) calibration technique is applied. A precision impedance standard substrate (ISS) developed by Cascade Microtech, is used as the calibration standard. The *short*, and *open* must be measured on both ports of the analyzer. The *thru* measurement between two ports must be measured as well.

The connectors, the interfaces between instruments, cables, DUT, test fixture and in the case of semiconductor, the wafer probes, are critical elements in achieving good measurements results. It also needs to make sure that cables and connectors are handled with care and that no stresses are placed on them that exceed their specifications.

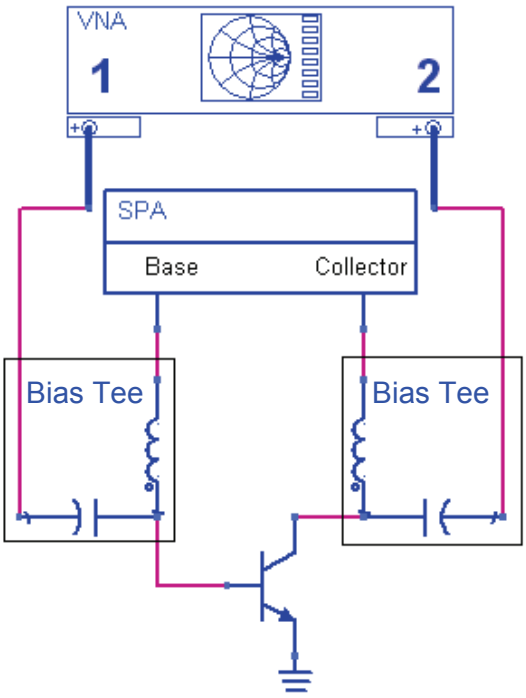


Figure 4.1: Simplified schematic of small-signal parameter measurement setup

Agilent's N5244A VNA is used to measure S-parameter. HP's 4156A Semiconductor Parameter Analyzer is used to source and sense the current and voltage at the base and collector of the DUT. Figure 4.1 shows the schematic of the measurement

system setup. Calibration accuracy is assured through standard impedance substrate measurements.

4.2.2 Equivalent Circuit Topology

The equivalent circuit topology must be suitable for the DUT. Many approaches have been suggested in the literature to develop an accurate and physical oriented small signal model of HBT, especially for III-V HBT. For bipolar transistors, both T and hybrid-π topology equivalent circuits are in use.

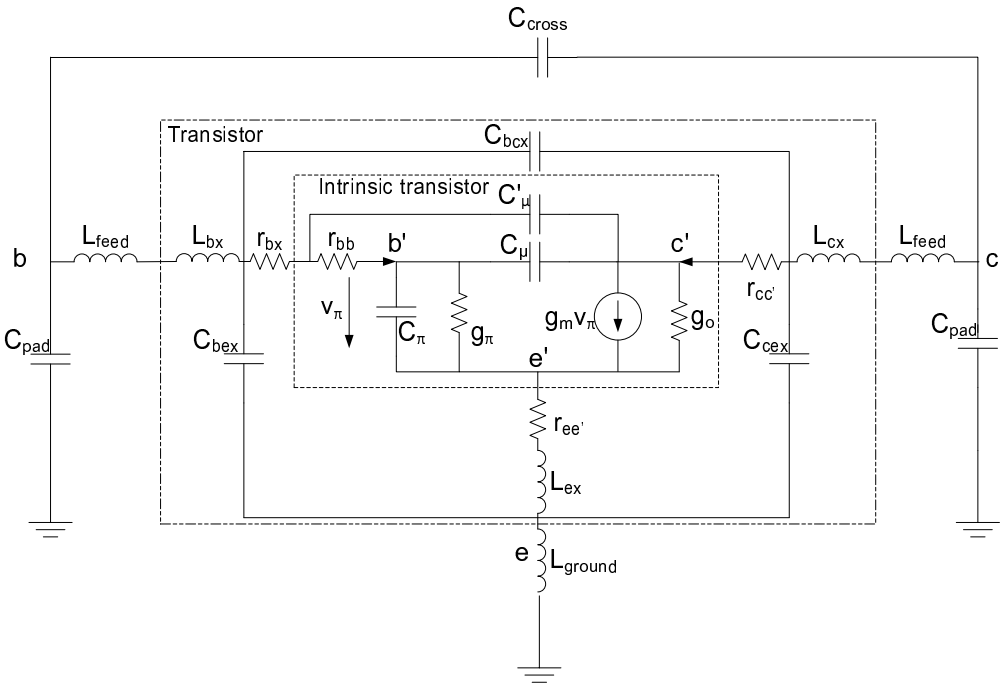


Figure 4.2: Complete small-signal equivalent circuit model for three fingers InGaP/GaAs HBT.

It is possible to transform from one model topologies into another [54]. T-topology model is directly matched to the physics of the device. However, most of the popular compact models such as SGP, VBIC, MEXTRAM and HICUM are based on the

hybrid-π topology and are widely used in commercial circuit simulators. There is no obvious reason to give up one of the circuit configurations. However hybrid-π-topology has the advantages like less complexity and a more intuitive link to DC measurements. All the parameters related to DC, in the ideal case, can directly be determined from Gummel plot measurements [57].

Figure 4.2 shows a complete small-signal equivalent circuit model, including pads and feed lines parasitic of the test structure, for InGaP/GaAs HBT. For most of III-V compound HBT, the substrate has negligible effect on the performance [106–109]. Hence, substrate related parasitic are neglected. The model is based on well known, hybrid-π equivalent circuit which is linearized version of the VBIC compact model. The circuit is split into three layers, test-structure parasitic, extrinsic and intrinsic.

The test-structure parasitic includes pads capacitances and feed-line inductances which form the first outer shell in the equivalent circuits. The extrinsic elements are the inductances, the resistances of contact metal and the metallization capacitances of the transistor. Those elements make second shell around the intrinsic equivalent circuit. Test-structure parasitic and extrinsic elements are considered as bias-independent. The intrinsic elements such as junction capacitances, junction resistances and voltage dependent current source, are considered as bias-dependent.

4.3 Parameter Extraction

Many attempts have been made to extract a small-signal equivalent circuit using analytical and optimization techniques [106,107,110–112]. The conventional numerical optimization method requires the small-signal model to be *fitted* to a large number of measured S-parameter data at various bias settings. One of the main problems of this method is the determination of the starting component values for the optimization

procedure. Depending on these starting values, the final values may be very different. Even with low error functions, component values can be lack of any physical meaning and leading to an inaccurate device model [111].

Recently, much efforts have been devoted to analytical approaches of HBT equivalent circuit parameter extraction [106, 107, 110, 113]. The direct parameter extraction is believed to be the most accurate method for equivalent-circuits modeling of HBTs [114]. In this method, the parasitic elements, followed by the intrinsic elements of the small signal equivalent circuit model are determined and extracted directly from measured S-parameter data, without employing any optimization. The direct parameter extraction technique and method presented in [115] is used in our characterization.

4.3.1 Extraction of Test-Structure Parasitic

The first step in determining the equivalent-circuit elements is the accurate extraction of test-structure parasitic and extrinsic element. The quality of these parasitic and extrinsic elements extraction plays an important role in the accuracy and robustness of the entire extraction algorithm. The values of parasitic elements are relatively small. However, they have significant influence on the extraction of intrinsic elements as their errors are accumulated. Thus, their values have to be determined with great accuracy.

De-Embedding Pads and Test Structure Feed Lines

The transistor fabricated for characterization is structured with probe pads and feedlines. To de-embed pads capacitances and feed lines inductance from measured data, test-structure characterization is conducted using two additional dummy test structures, *open* and *short* and shown in Fig. 4.3 and their respective equivalent circuits in Fig. 4.4. The *open* test-structure equivalent circuit elements can be de-embedded

from the HBT data, simply by subtracting the admittance (Y) matrix of the open test structure Y_{open} from the Y-matrix of the whole structure with DUT, Y_{hbt0}, as show in (4.1).

$$Y_{hbt1} = Y_{hbt0} - Y_{open} \tag{4.1}$$

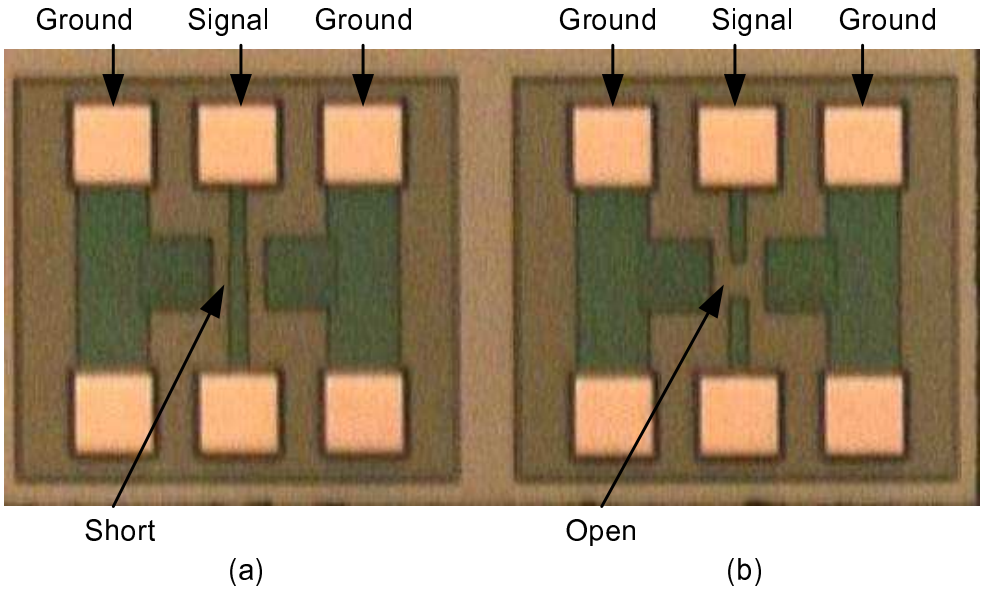


Figure 4.3: The image of fabricated dummy short (a) and open (b) test-structure.

The series impedances of the feed lines can be evaluated by using a *short* test-structure. However, Fig. 4.4(a) shows that *short* test-structure equivalent circuit is also bound with *open* structure elements. The same principle as in (4.1) can be applied to remove the *open* circuit elements. The impedance (Z) matrix of series impedances Z_b, Z_c and Z_e can be extracted by subtracting Y_{open} from the Y-matrix of the *short* test-structure, Y_{short0} [57] as in (4.2).

$$Z_{short1} = \frac{1}{Y_{short1}} = \frac{1}{Y_{short0} - Y_{open}} \tag{4.2}$$

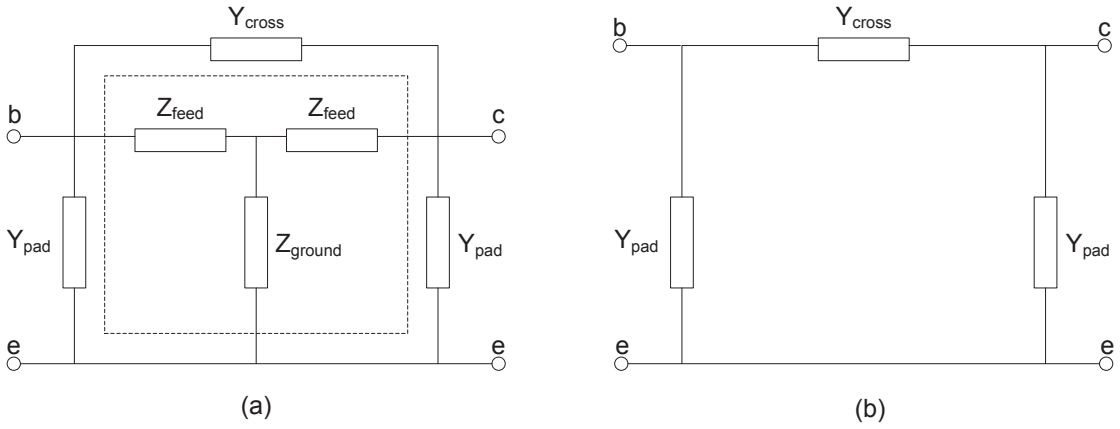


Figure 4.4: Equivalent circuit schematic of dummy short (a) and open (b) test-structure.

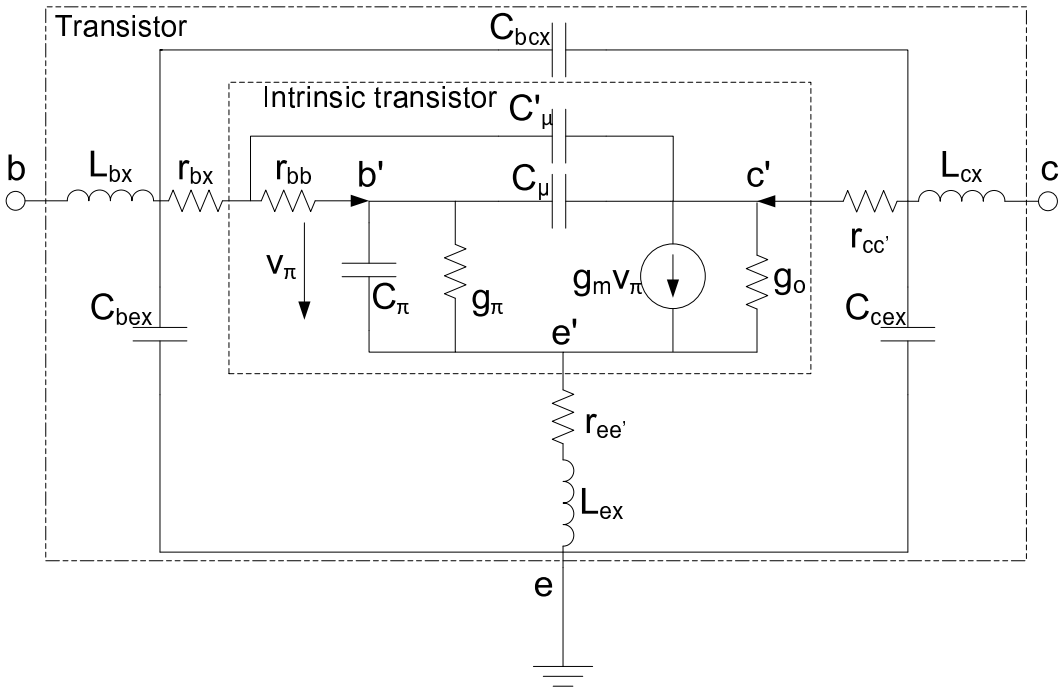


Figure 4.5: Transistor small-signal equivalent circuit model subsequently test structure related parasitic have being de-embedded.

The feed-line impedance network is in series-series connection with the elements of HBT's equivalent circuit. The Z-matrix of the HBT, Z_{hbt}, can be obtained by subtracting

$$Z_{hbt} = Z_{hbt1} - Z_{short1}. \tag{4.3}$$

4.3.2 Extraction of Extrinsic Elements

There are different approaches to determine the extrinsic parameters and some of the main facts of these methods are discussed in the following.

- Electromagnetic Simulation - An elaborate task and rather suited for the design of an optimized HBT layout.

- Measurement at Specific Bias Conditions - It take advantage of the fact that the extrinsic elements are assumed to be bias-independent. By biasing at different points, the numbers of variables is minimized. It allows us to distinguish the constant extrinsic parameters from the bias-dependent intrinsic. Moreover, they provide well-calibrated reference planes, more information and less susceptible to obscure nonlinear effects.

- Global Optimization - The optimization is needed to perform over various bias points and aiming the best fit of the model's calculated S-parameter to the measured ones. However, the resulting parameter values might be nonphysical

Extrinsic Inductances and Access Resistance

The equivalent circuit of the HBT after pads and test-structure feed line inductances have being de-embedded is shown in Fig. 4.5. The next step is determining the extrinsic elements values of HBT's equivalent-circuit. [110] reported that, the series

extrinsic elements such as access resistance ($r_{cc'}$, $r_{ee'}$, r_{bx}) and parasitic inductance (L_c, L_e, L_b) can be extracted from the S-parameter data of the DUT, which is biased at high current forward operation called *over driven* I_b. A 3-fingers InGaP/GaAs HBT with emitter area of $3 \times 3\mu m \times 40\mu m$ is biased with $V_{CE} = 0V$ and $I_{bb} = 10$mA to 200mA.

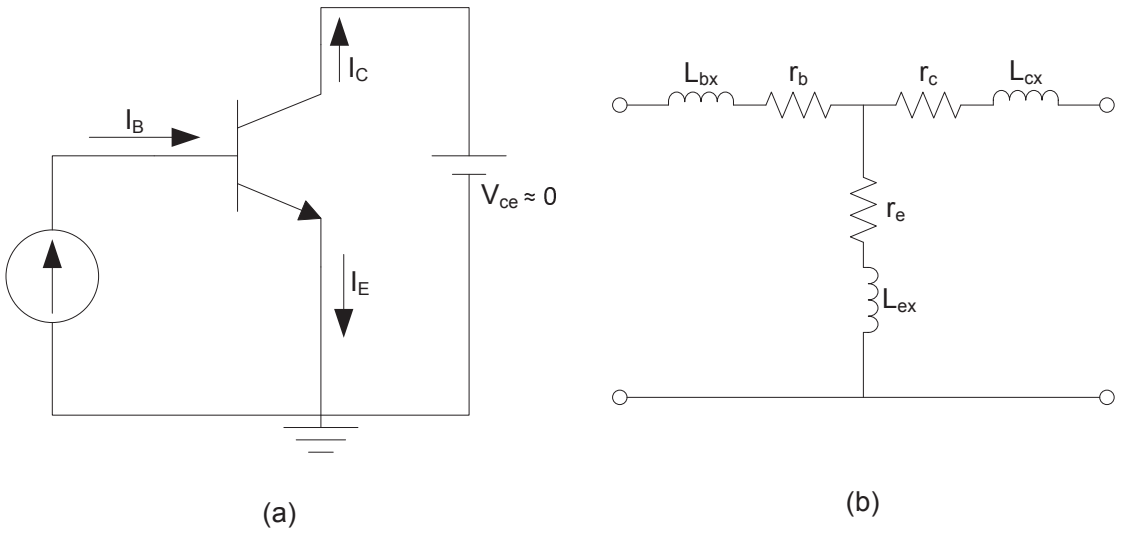


Figure 4.6: Simplified schematic of over - driven I_{bb} measurement setup (a) and equivalent circuit under this bias condition (b).

This bias condition makes both base-collector and base-emitter junctions forward biased. At high current densities, the junction dynamic resistances tend to be nearly zero. This, conceptually, shorts both junctions and minimizes the intrinsic element effects. The injected base current is divided, but not symmetrically, into the collector and emitter [115]. Meanwhile, junction capacitances become quite large and short themselves in the middle frequency range [110]. Hence, the influence of the parasitic capacitances remains negligible in that frequency range. Some residual parasitic remain from the imperfect test-structure de-embedding is also corrected by this

over-driven I_b operation [115].

Measurement setup and the HBT equivalent circuit in such operation mode are shown in Figure 4.6. The access resistances and parasitic inductances of the device can be describe by the Z-parameters of this circuit by the following equations [115],

$$r_b = \mathrm{Re}\{Z_{11} - Z_{12}\} \tag{4.4}$$

$$r_e = \mathrm{Re}\{Z_{12}\} \tag{4.5}$$

$$r_c = \mathrm{Re}\{Z_{22} - Z_{21}\} \tag{4.6}$$

$$L_{bx} = \frac{\mathrm{Im}\{Z_{11} - Z_{12}\}}{\omega} \tag{4.7}$$

$$L_{ex} = \mathrm{Im}\{Z_{12}\} \tag{4.8}$$

$$L_{cx} = \frac{\mathrm{Im}\{Z_{22} - Z_{21}\}}{\omega} \tag{4.9}$$

As discussed before, the resistances and inductances values are determined at the middle frequency range of 5GHz to 15GHz. The extrapolated line of the real parts of $Z_{11} - Z_{12}$, Z_{12} and $Z_{22} - Z_{21}$ as a function of $1/I_{bb}$ intercepts at the ordinate, where $I_{bb} \to \infty$ conceptually, give the values of r_{bx}, $r_{ee'}$ and $r_{cc'}$. Fig. 4.7 shows variation of extracted access r_{bx}, $r_{ee'}$ and $r_{cc'}$ with $1/I_{bb}$.

The frequency dependent behaviors of these resistances over middle frequency range are shown in Fig.4.8 and are nearly constant over 5GHz to 15GHz. The extracted r_{bx}, $r_{ee'}$ and $r_{cc'}$ values for $3 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT are 1.72Ω, 0.3Ω and 1.2Ω respectively.The parasitic inductances, L_{bx}, L_{ex} and L_{cx}, can be extracted using equation (4.7) to (4.9) over middle frequency range and we obtain 20pH, 18pH and 3.5pH respectively. Figure 4.9 shows extracted parasitic inductances across mid-band frequencies.

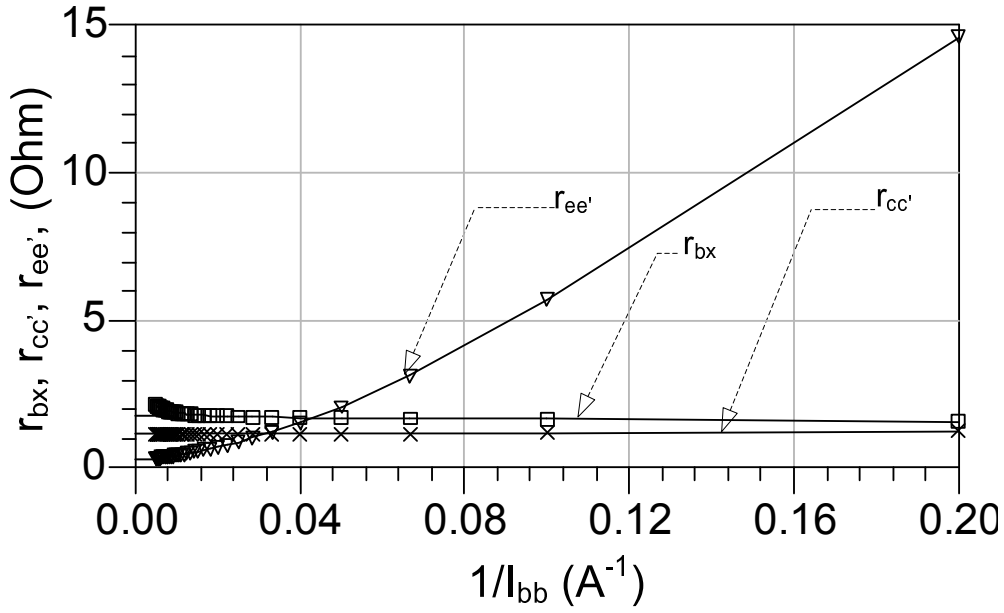


Figure 4.7: Plot of the real part of $\{Z_{11} - Z_{12}\}$,$\{Z_{12}\}$ and $\{Z_{22} - Z_{21}\}$ versus $1/I_{bb}$

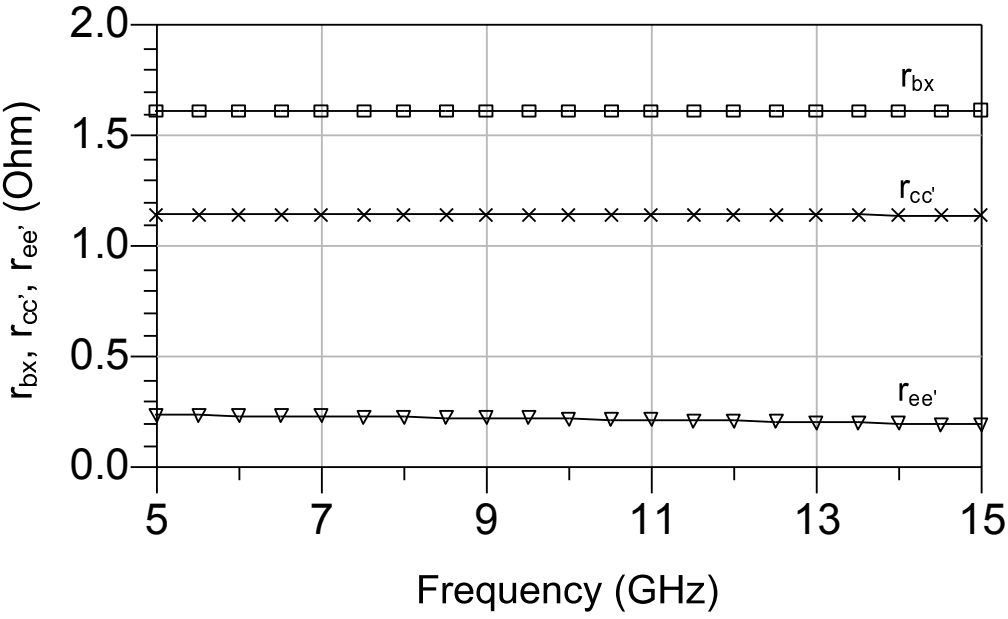


Figure 4.8: Frequency dependent characteristic of the real part of $\{Z_{11} - Z_{12}\}$,$\{Z_{12}\}$ and $\{Z_{22} - Z_{21}\}$ over mid-band frequencies.

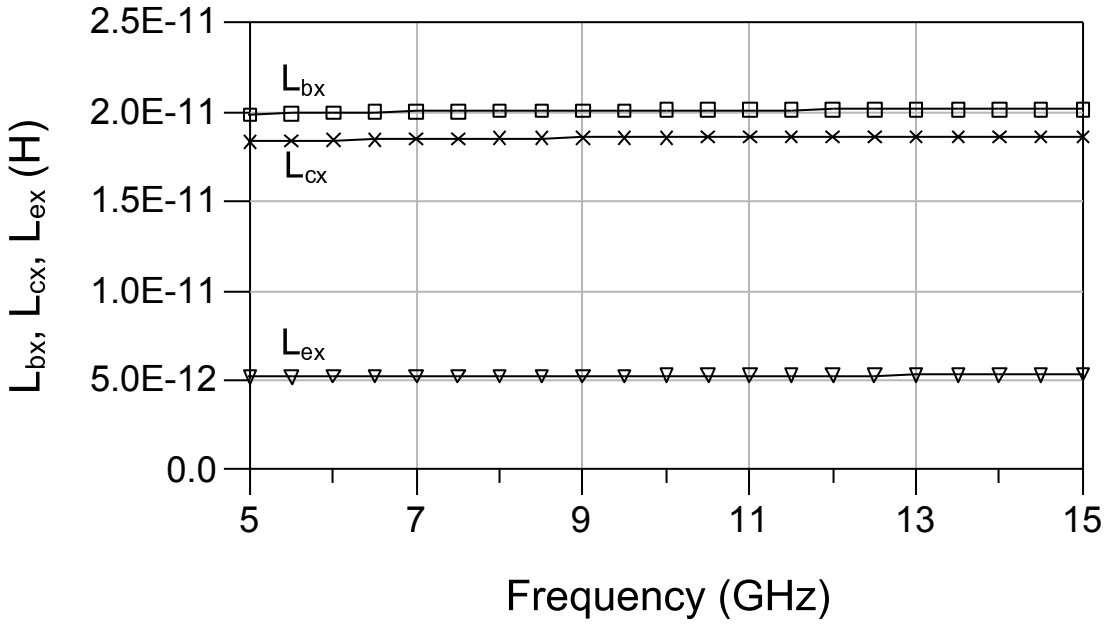


Figure 4.9: Frequency dependent characteristic of the imaginary part of$\{Z_{11} - Z_{12}\}$,$\{Z_{12}\}$ and $\{Z_{22} - Z_{21}\}$ over mid-band frequencies.

Extraction of Parasitic Capacitances

The overlap capacitances can be determined from *cold* or *cutoff* state S-parameter data. The cold state condition is achieved by setting V_{ce} open with reverse and/or low forward V_{be} voltage. Under such conduction, the small signal equivalent circuit model for InGaP/GaAs HBT is reduced effectively to capacitance elements network as shown in Fig. 4.10. The effects of series resistances, dynamic resistance, and transconductance are negligible compare to the capacitive elements at the middle frequency range [115]. Then the elements of equivalent circuit related to Y parameters can be expressed as,

$$C_{bTotal} = C_{\pi} + C_{bex} = \frac{\mathrm{Im}\{Y_{11} + Y_{12}\}}{\omega} \tag{4.10}$$

$$C_{\mu} + C'_{\mu} + C_{bcx} = \frac{\mathrm{Im}\{-Y_{12}\}}{\omega} \tag{4.11}$$

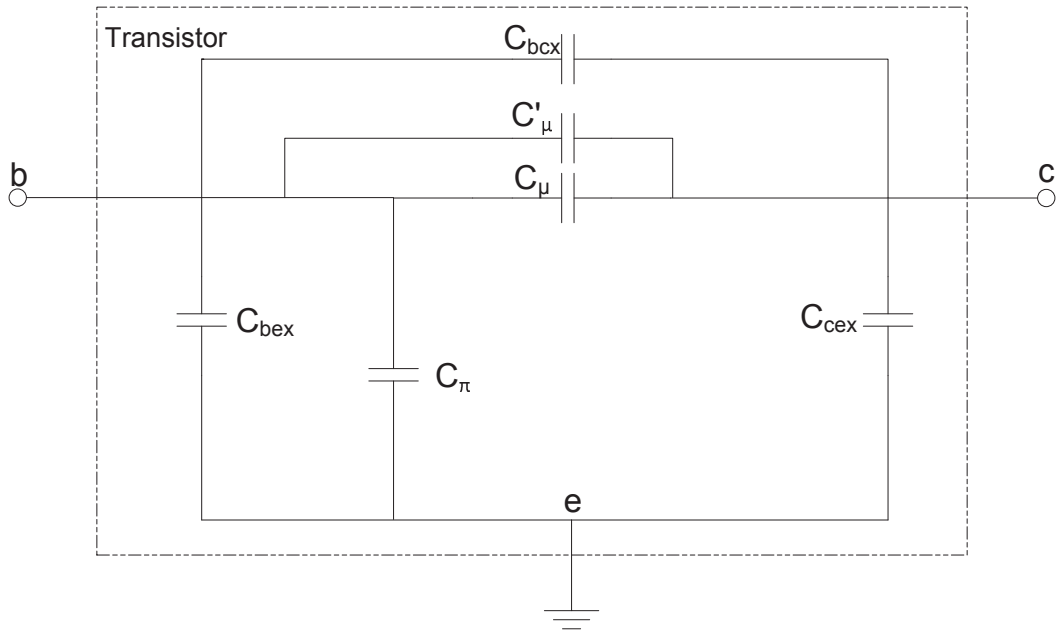


Figure 4.10: Equivalent circuit representation of HBT under cool state operation.

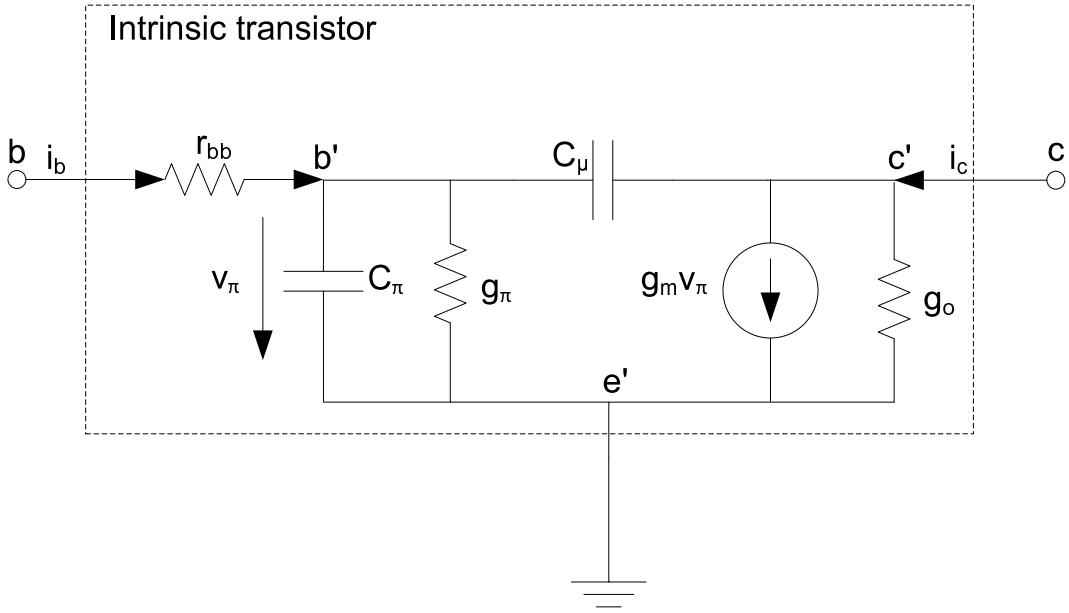


Figure 4.11: De-embedded equivalent circuits of the intrinsic part of HBT.

$$C_{cex} = \frac{\mathrm{Im}\left\{Y_{12} + Y_{22}\right\}}{\omega} \tag{4.12}$$

In reality, it is difficult to distinguish between parasitic capacitances, C_{bex}, C_{bcx} and C_{cex} from their corresponding junction capacitances [110, 116]. Hence, in this extraction procedure, their values are fixed to zero and if their presence exists, they are supposed to be absorbed by the junction capacitances.

4.3.3 Extraction of Intrinsic Elements

The calculated extrinsic parameters are then de-embedded from measured data. Parasitic inductances L_{bx}, L_{ex} and L_{cx} are de-embedded from the impedance matrix determined from (4.3) as,

$$Z_{\mathrm{int}\,1} = Z_{hbt} - \begin{bmatrix} j\omega L_{bx} + j\omega L_{ex} & j\omega L_{ex} \\ j\omega L_{ex} & j\omega L_{cx} + j\omega L_{ex} \end{bmatrix} \tag{4.13}$$

and it is followed by de-embedding access resistances r_{bx}, $r_{ee'}$ and $r_{cc'}$ as,

$$Z_{\mathrm{int}} = Z_{\mathrm{int}\,1} - \begin{bmatrix} r_{ee'} + r_{bx} & r_{ee'} \\ r_{ee'} & r_{ee'} + r_{cc'} \end{bmatrix}. \tag{4.14}$$

After above two ports matrix operations, Z_{int} is reconverted into Y_{int}. Figure 4.11 shows the intrinsic equivalent circuit of the HBT. The equivalent admittances of the intrinsic circuit elements are analytically derived.

The small-signal base and collector currents of the intrinsic transistor located between b', c' and e' are given by [58],

$$i_b = \left(Y_\pi + j\omega C_\mu\right) v_\pi - j\omega C_\mu v_c \tag{4.15}$$

$$i_c = (g_m - j\omega C_\mu)v_\pi + (g_o + j\omega C_\mu)v_c \tag{4.16}$$

$$\begin{pmatrix} i_b \\ i_c \end{pmatrix} = \begin{pmatrix} y_{11}^{'} & y_{12}^{'} \\ y_{21}^{'} & y_{22}^{'} \end{pmatrix} \begin{pmatrix} v_\pi \\ v_c \end{pmatrix} \tag{4.17}$$

where,$Y_\pi = (g_\pi + j\omega C_\pi)$, $y_{11}^{'} = (Y_\pi + j\omega C_\mu)$, $y_{12}^{'} = -j\omega C_\mu$, $y_{21}^{'} = (g_m - j\omega C_\mu)$ and $y_{22}^{'} = (g_o + j\omega C_\mu)$. Then, those current can be related to the terminal voltage v_b as,

$$v_b = v_\pi + r_{bb}i_b = \left(1 + r_{bb}y_{11}^{'}\right)v_\pi + r_{bb}y_{12}^{'}v_c. \tag{4.18}$$

$$v_c = v_c \tag{4.19}$$

The voltages v_π and v_c can be expressed using terminal voltages as,

$$\begin{pmatrix} v_\pi \\ v_c \end{pmatrix} = \frac{1}{\Delta}\begin{pmatrix} 1 & -r_{bb}y_{12}^{'} \\ 0 & 1 + r_{bb}y_{11}^{'} \end{pmatrix} \begin{pmatrix} v_b \\ v_c \end{pmatrix}, \ \Delta = \left(1 + r_{bb}y_{11}^{'}\right) \tag{4.20}$$

Then applying (4.20) in (4.17) gives,

$$\begin{pmatrix} i_b \\ i_c \end{pmatrix} = \frac{1}{\Delta}\begin{pmatrix} y_{11}^{'} & y_{12}^{'} \\ y_{21}^{'} & y_{22}^{'} \end{pmatrix} \begin{pmatrix} 1 & -r_{bb}y_{12}^{'} \\ 0 & 1 + r_{bb}y_{11}^{'} \end{pmatrix} \begin{pmatrix} v_b \\ v_c \end{pmatrix} \tag{4.21}$$

Equation (4.21) can be solved as,

$$\begin{pmatrix} i_b \\ i_c \end{pmatrix} = \begin{pmatrix} \dfrac{Y_\pi + j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} & \dfrac{-j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \\ \dfrac{g_m - j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} & \dfrac{g_o\left(1 + r_{bb}Y_\pi\right) + j\omega\left[C_\mu + r_{bb}C_\mu(g_m + Y_\pi + g_o)\right]}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \end{pmatrix} \begin{pmatrix} v_b \\ v_c \end{pmatrix} \tag{4.22}$$

If, g_o is assumed small and being neglected, then (4.22) will reduce to the analysis

presented in [115]. The admittance parameters of Y_{int} can be represented as,

$$Y_{11-\text{int}} = \frac{Y_\pi + j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \tag{4.23}$$

$$Y_{12-\text{int}} = \frac{-j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \tag{4.24}$$

$$Y_{21-\text{int}} = \frac{g_m - j\omega C_\mu}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \tag{4.25}$$

$$Y_{22-\text{int}} = \frac{g_o\left(1 + r_{bb}Y_\pi\right) + j\omega\left[C_\mu + r_{bb}C_\mu(g_m + Y_\pi + g_o)\right]}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)} \tag{4.26}$$

Generally for HBT, the output conductance is very small and it is also valid for our transistor. Hence, output conductance g_o is neglected and (4.26) can be simplified as

$$Y_{22-\text{int}} = \frac{j\omega\left[C_\mu + r_{bb}C_\mu(g_m + Y_\pi)\right]}{1 + r_{bb}\left(Y_\pi + j\omega C_\mu\right)}. \tag{4.27}$$

Extraction of Intrinsic Base Resistance

The intrinsic base resistance is included in the equations for most of the intrinsic parameter extraction, an accurate extraction of the resistance is crucial to avoid accumulated errors. Following the technique presented in [115, 117], the intrinsic base resistance can be express as,

$$r_{bb} \approx \text{Re}\left\{\frac{1}{Y_{11-\text{int}}}\right\}_{\text{at high frequency}}. \tag{4.28}$$

Figure 4.12 shows the value of intrinsic base resistance r_{bb} variation over test frequency range and it is nearly constant over higher frequency region and r_{bb} can be extracted accurately.

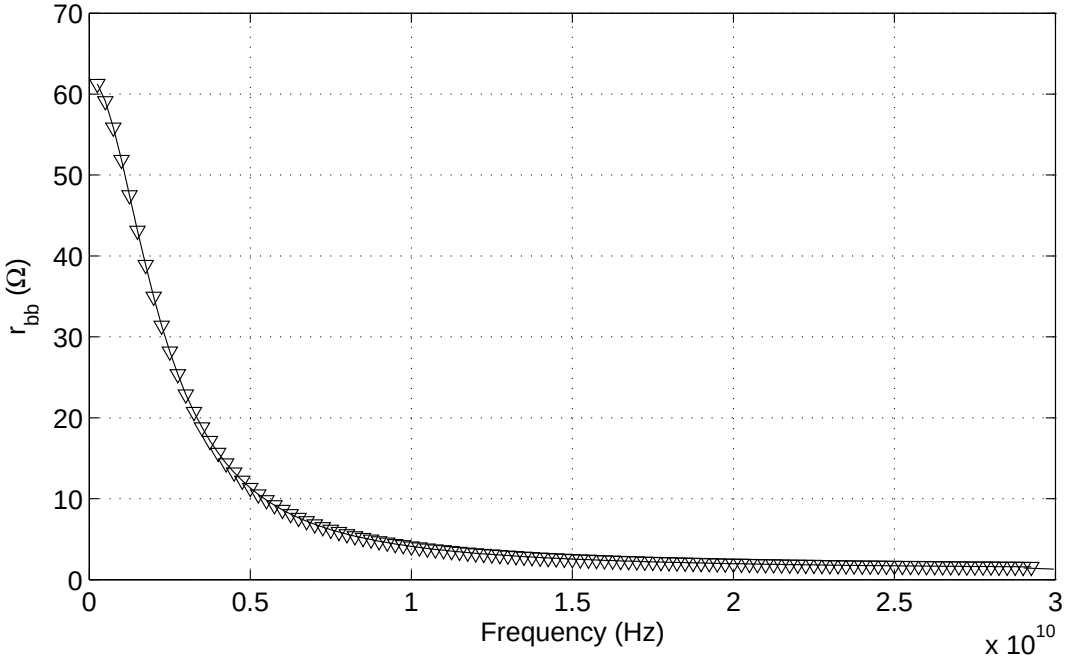


Figure 4.12: Intrinsic base resistance characteristic as a function of operating frequencies.

Extraction of C_μ

The small-signal intrinsic base-collector junction capacitance C_μ is extract from two auxiliary equations [117] shown in (4.29) and (4.30).

$$\mathrm{Im}\left\{\frac{Y_{11-\mathrm{int}}Y_{22-\mathrm{int}}+Y_{12-\mathrm{int}}Y_{21-\mathrm{int}}}{Y_{11-\mathrm{int}}-Y_{21-\mathrm{int}}}\right\}=\omega\left(C_\mu+C_\mu^{'}\right)+\mathrm{Im}\left\{\frac{-2\omega^2C_\mu C_\mu^{'}}{g_m+Y_\pi}\right\} \quad (4.29)$$

$$\mathrm{Re}\left\{\frac{Y_{11-\mathrm{int}}Y_{22-\mathrm{int}}-Y_{12-\mathrm{int}}Y_{21-\mathrm{int}}}{Y_{22-\mathrm{int}}+Y_{12-\mathrm{int}}}\right\}=\frac{1}{r_{bb}}\left(\frac{C_\mu+C_\mu^{'}}{C_\mu}\right)-\mathrm{Re}\left\{\frac{\omega^2C_\mu^{'2}}{r_{bb}\left(g_m+Y_\pi\right)}\right\} \quad (4.30)$$

At the middle frequency range, the second term of both (4.29) and (4.30) is much smaller than the first term in the right hand side of the equations and can be

approximated as,

$$\left(C_\mu + C_\mu^{'}\right) \sim \frac{1}{\omega} \cdot \mathrm{Im}\left[\frac{Y_{11-\mathrm{int}}Y_{22-\mathrm{int}} + Y_{12-\mathrm{int}}Y_{21-\mathrm{int}}}{Y_{11-\mathrm{int}} - Y_{21-\mathrm{int}}}\right]_{\text{mid-frequencies}} \tag{4.31}$$

$$\left(\frac{C_\mu}{C_\mu + C_\mu^{'}}\right) = r_{bb} \cdot \mathrm{Re}\left[\frac{Y_{11-\mathrm{int}}Y_{22-\mathrm{int}} - Y_{12-\mathrm{int}}Y_{21-\mathrm{int}}}{Y_{22-\mathrm{int}} + Y_{12-\mathrm{int}}}\right]^{-1}_{\text{mid - frequencies}} \tag{4.32}$$

Equation(4.31) provides total capacitance and (4.32) gives the ratio of capacitances. For $V_{ce} = 4V$, $I_c = 39mA$, the total capacitance is 150fF and the ratio is 0.97. Figure 4.13 shows the capacitance distribution ratio $C_\mu/\left(C_\mu + C_\mu^{'}\right)$ over middle frequency range and Fig. 4.13 shows the value of C_μ and $C_\mu^{'}$. As $C_\mu^{'}$ is very small, it is neglected in the subsequence analysis.

Extraction of r_π, g_m, C_π

After de-embedding r_{bb} and C_μ, the remaining trans-conductance (g_m), dynamic base-emitter resistance(r_π) and base-emitter capacitance (C_π) can be derived analytically using intrinsic Y-parameters shown in (4.23) to (4.27). The base-emitter junction intrinsic admittance parameter $Y_\pi = g_\pi + j\omega C_\pi$ can be expressed by rearranging (4.23) as,

$$Y_\pi = \frac{-Y_{11-\mathrm{int}}\left(1 + j\omega r_{bb}C_\mu\right) + j\omega C_\mu}{Y_{11-\mathrm{int}}r_{bb} - 1} \tag{4.33}$$

The real part of (4.33) holds r_π information and the imaginary part provide C_π as

$$r_\pi = \mathrm{Re}\left\{Y_\pi\right\},\ C_\pi = \frac{1}{\omega}\,\mathrm{Im}\left\{Y_\pi\right\}. \tag{4.34}$$

Figure 4.15 shows r_π and Fig. 4.16 shows C_π at a middle frequency range extracted from real and imaginary parts of Y_π respectively. Extracting g_m required us to derive two auxiliary equations [115]

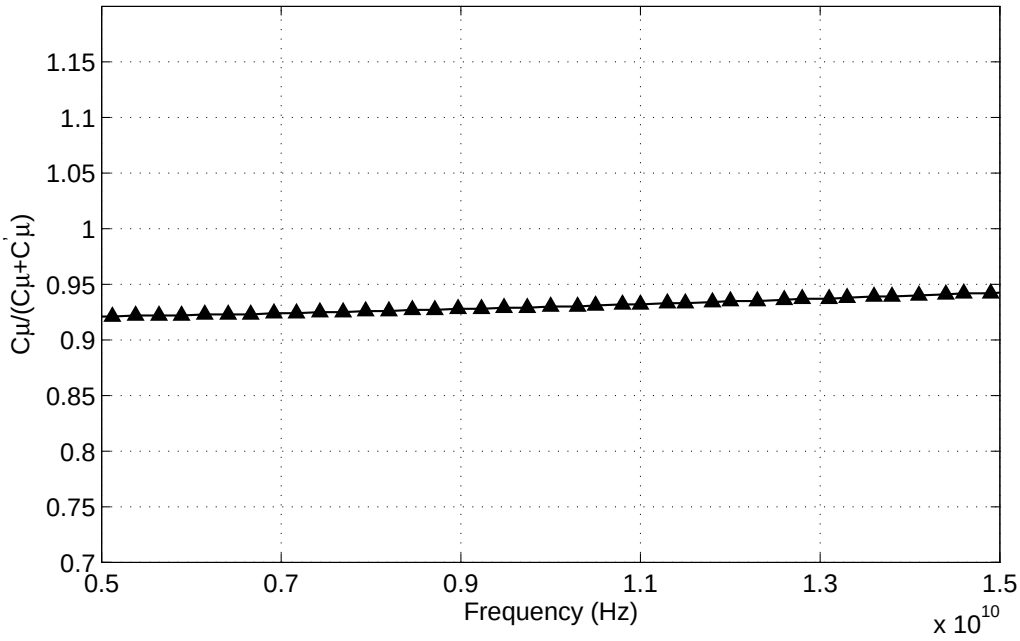


Figure 4.13: Capacitance distribution ratio of C_μ and $C_\mu{}'$ over mid-band frequencies.

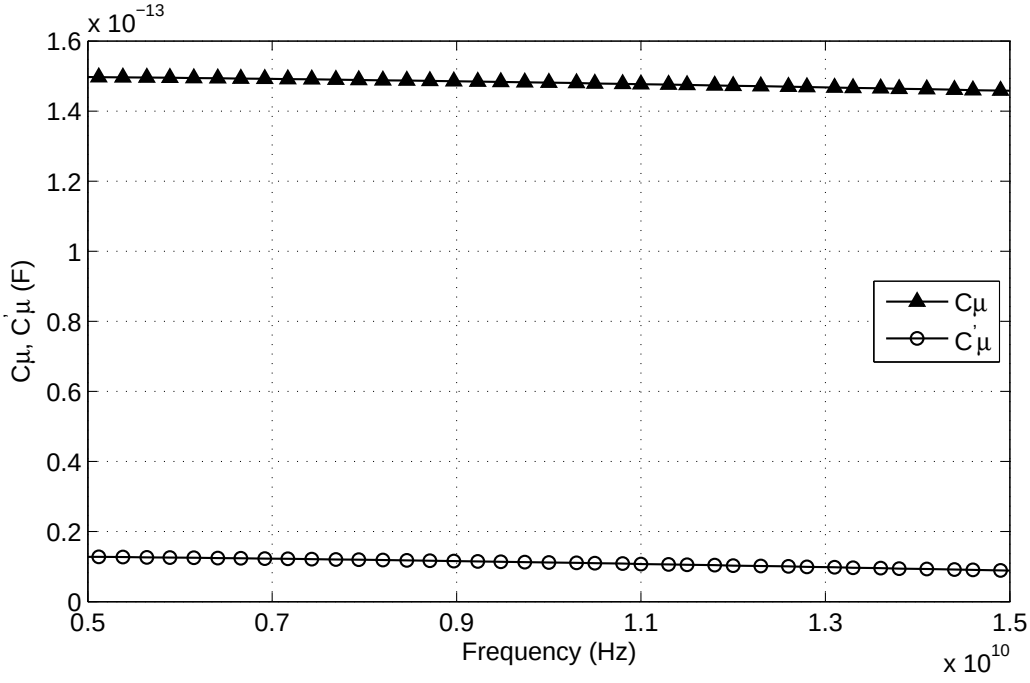


Figure 4.14: Extracted capacitance values of C_μ and $C_\mu{}'$ over mid-band frequencies.

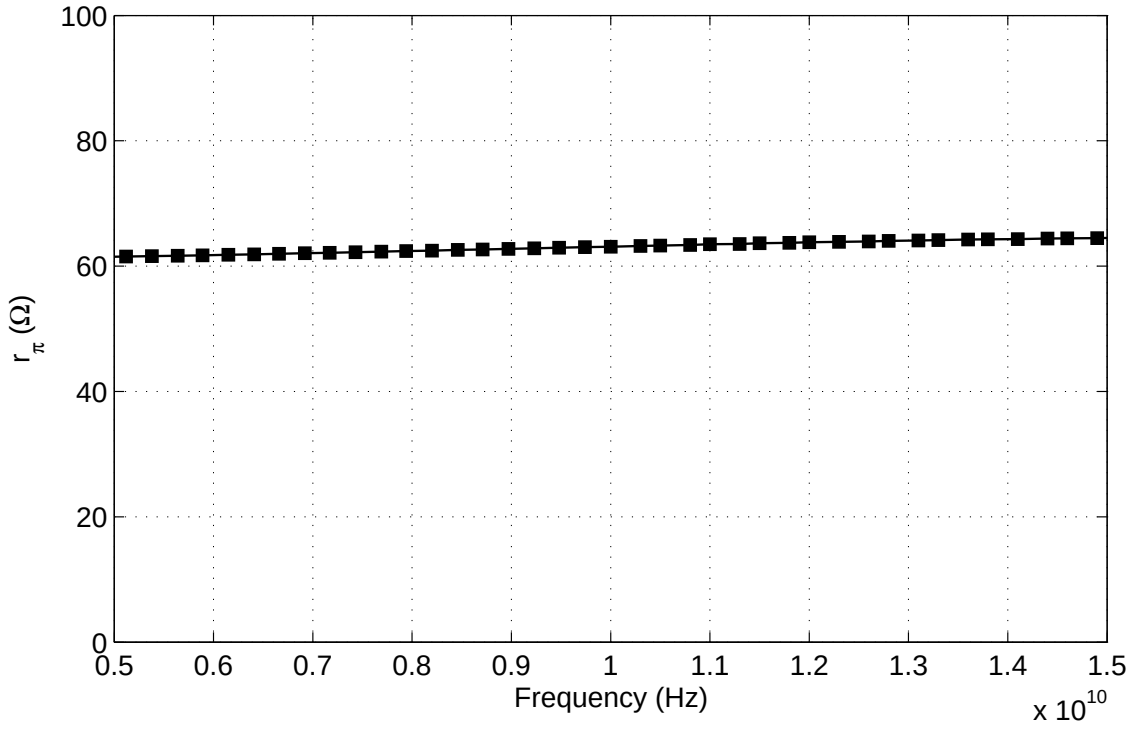


Figure 4.15: Frequency dependent characteristics of extracted base emitter junction dynamic resistance r_π.

$$\frac{Y_{11-\text{int}} + Y_{12-\text{int}}}{Y_{21-\text{int}} - Y_{12-\text{int}}} = \frac{1}{g_m r_\pi} + \frac{j\omega C_\pi}{g_m}, \tag{4.35}$$

$$\frac{1}{Y_{21-\text{int}} - Y_{12-\text{int}}} = \frac{1}{g_m} + \frac{r_{bb}}{g_m r_\pi}. \tag{4.36}$$

Solving (4.35) and (4.36) gives the parameter g_m in term of admittance parameters as shown in (4.37).

$$g_{m0} \cong \left[\text{Re}\left\{ \frac{1}{Y_{21-\text{int}} - Y_{12-\text{int}}} \right\} - r_{bb} \cdot \text{Re}\left\{ \frac{Y_{11-\text{int}} + Y_{12-\text{int}}}{Y_{21-\text{int}} - Y_{12-\text{int}}} \right\} \right]^{-1} \tag{4.37}$$

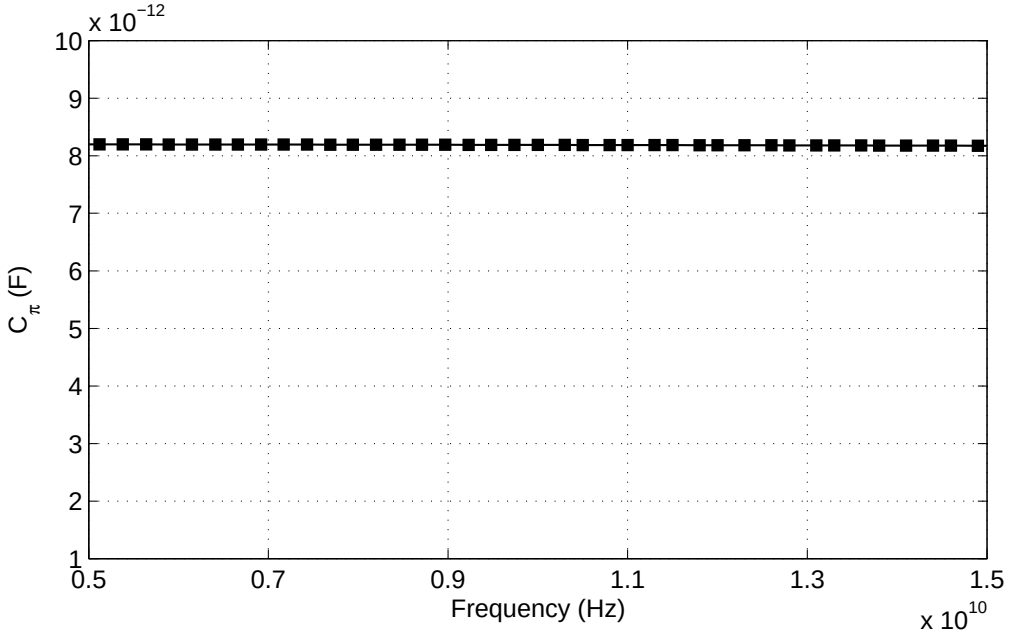


Figure 4.16: Extracted small-signal base-emitter junction capacitance over mid-band frequencies.

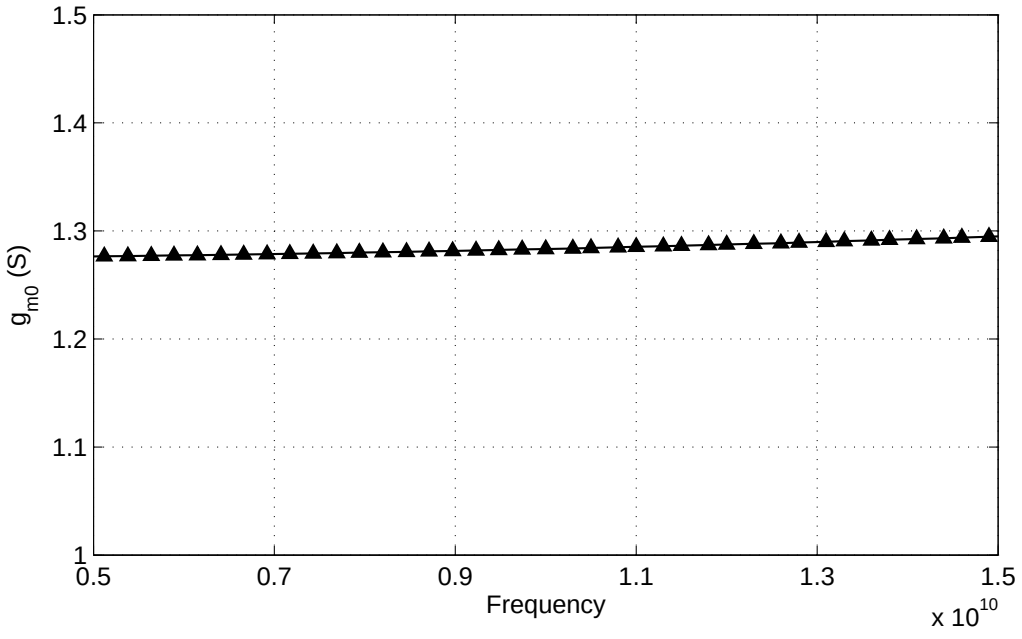


Figure 4.17: Extracted small-signal trans-conductance g_{m0}.

Figure 4.17 shows the extracted g_{m0} at various frequencies. The extracted equivalent circuit parameters are summarized in Table 4.1 and the bilateral small-signal equivalent circuit model for three fingers InGaP/ GaAs HBT is shown in Fig. 4.18.

4.4 Verification through Measurements

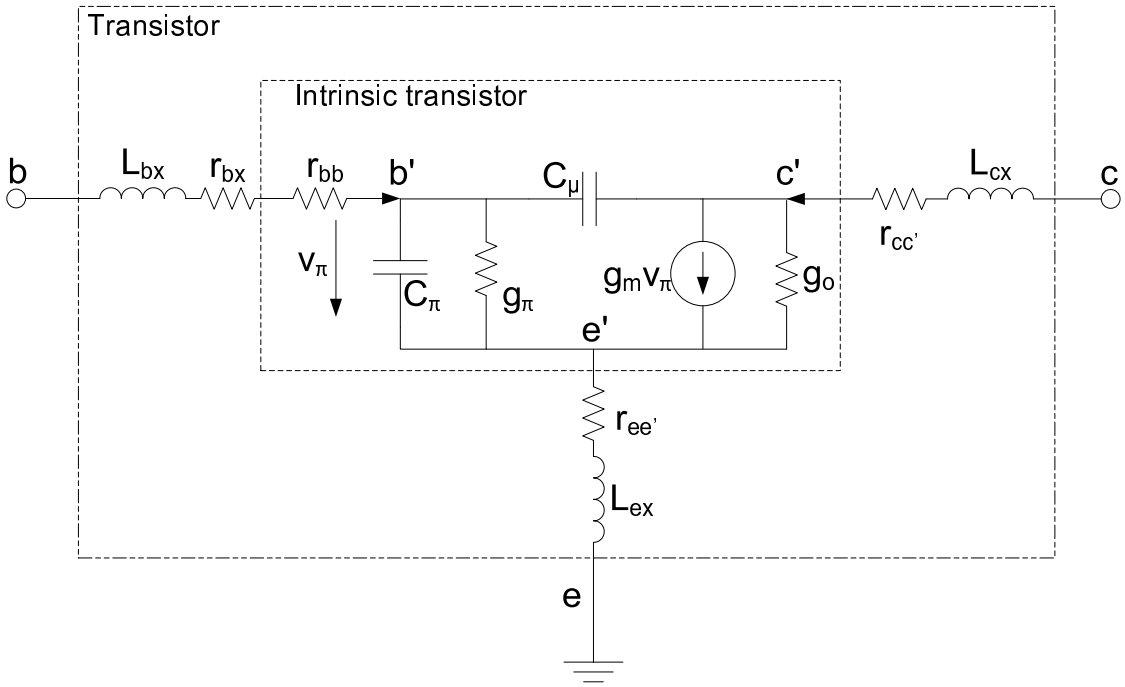


Figure 4.18: Developed bilateral small-signal equivalent circuit model.

To validate the analytical extraction and evaluate the accuracy of the model, on wafer small-signal S-parameter measurements are carried out for three fingers $3 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT over the frequencies range of 250MHz to 30GHz. HBT is biased at V_{ce}=4V and I_c=39 mA. The developed small-signal model is implemented in Agilent's advance design system (ADS) and simulated.

Table 4.1: Extracted parameter values of small-signal equivalent circuit model for $V_{cc} = 4V$, $I_{cc} = 39mA$, $3 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT.

Parameter	Value	Parameter	Value
L_{bx}	20.17pH	r_{bb}	1Ω
L_{ex}	5pH	r_{ee}	0.2Ω
L_{cx}	18pH	r_{cc}	1.2Ω
r_{bx}	1.8 Ω	C_{μ}	147fF
C_{π}	8.2pF	r_{π}	62 Ω
g_m	1.27 S	g_o	0 S

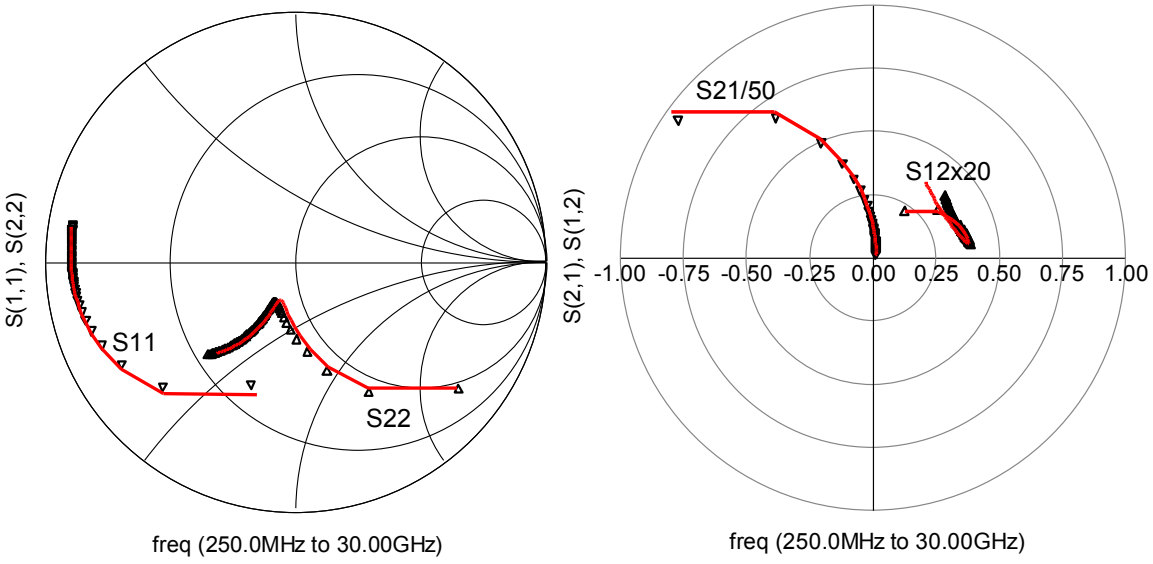


Figure 4.19: Measured and simulated S-parameter responses of developed small-signal model (model implemented in ADS).

Figure 4.19 shows the comparison between the measured and model simulated S-parameter response at extracted bias point. The modeled S-parameters are presented without any optimization. Very good agreement over the whole frequency range is

obtained.

4.5 Unilateral Circuit Model for InGaP/GaAs HBT

Bilateral equivalent circuit models, as developed in the previous sections, for the active device are extensively used for circuit simulation in various design processes. These design processes often uses optimization to achieve the design goals which often do not result in optimal designs. As we discussed in Chapter 2, analytical formulations like distortion analysis, non-linearity analysis, distributed amplifier design and other applications are derived based on simplified unilateral model assumption for the active device. However, there is no unilateral models development for their respective technologies. In the following section simplified unilateral model and unilateral model using Miller approximation are validated with bilateral small signal responses.

4.5.1 Simplified Unilateral and Miller's Approximation Performances

The bilateral small-signal equivalent circuit model presented in Fig. 4.18 incorporates with two feedback networks, emitter resistance ($r_{ee'}$) and base-collector junction capacitance (C_μ). The extracted emitter resistance is 0.2Ω, which is bias independent and is assumed to be negligible at low collector current levels. However, the voltage drop across it is about 20mV when the collector current reaches 100mA, which is 66% of maximum operating current. This amount of feedback voltage is large enough to offset the base bias point.

To develop a more robust circuit model, we assume $r_{ee'}$ is a substantial feedback element. The extracted bias dependent, C_μ is 147fF. The reactance of this feedback path changes from 4.33kΩ at 250MHz to 36Ω at 30GHz. This suggests baseband,

fundamental and harmonics will experience difference impedances. Any assumption applied on this feedback element based on specific frequency for nonlinear analysis is incomplete.

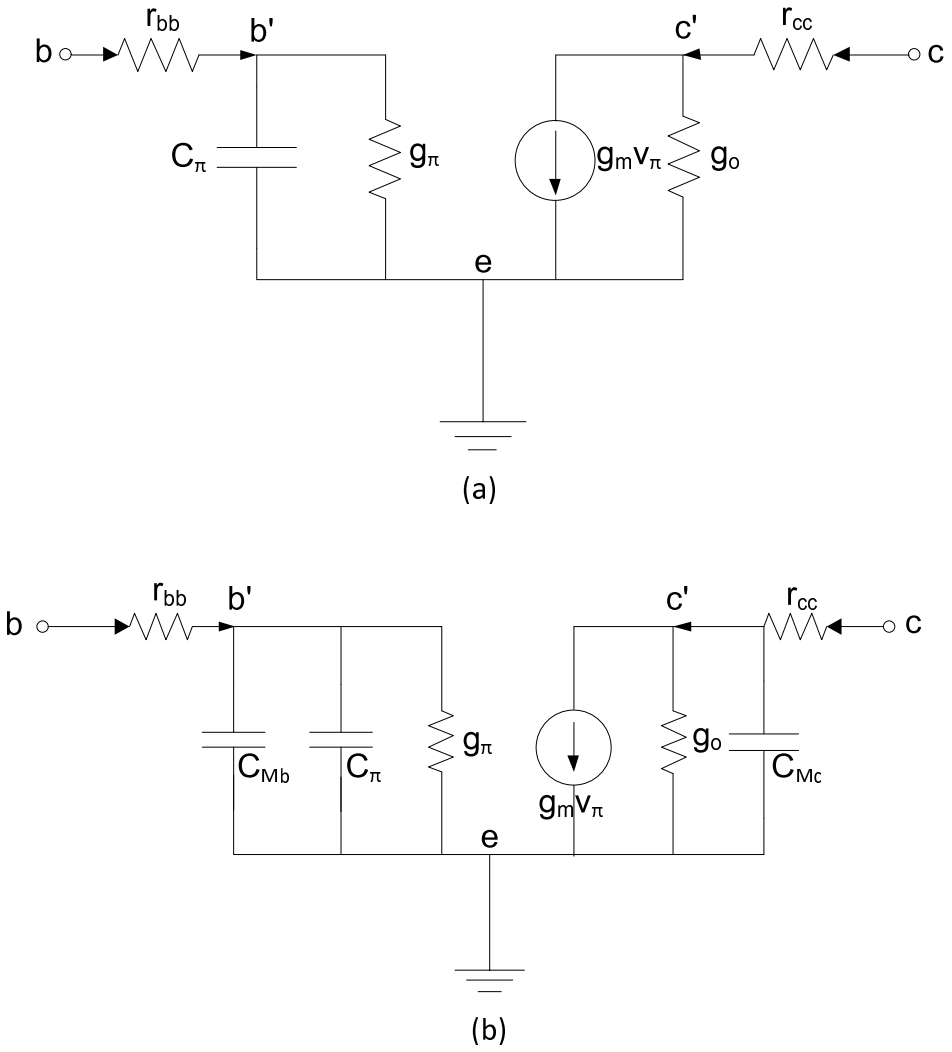


Figure 4.20: Circuit schematic of simplified unilateral model (a) Miller approximation (b).

Simplified unilateral and Miller approximated circuits are simulated and their validity are analyzed. 50Ω load is assumed in Miller capacitance computation. The circuits used for simulation are shown in Fig. 4.20 and S-parameter responses of bilat-

eral, simplified unilateral and Miller approximation, are shown in Fig. 4.21. Simplified unilateral circuit responses are significantly different from bilateral data for $S11$ and $S21$, even at the frequency as low as 250MHz. Meanwhile, as mention before, Miller approximation gives very close responses for $S11$ and $S21$.

However, both circuits completely fail to predict $S22$. In addition, $S22$ is not following a constant conductance circle in the Smith chart and it switches from constant resistance to constant conductance above the resonance frequency.

4.5.2 Analysis for Unilateral Circuits Model

Decoupling $r_{ee'}$

A quantitative analysis is applied on the bilateral circuit shown in Fig. 4.18. Emitter resistance is uncoupled in the first step. As discuss before, g_o is very small for HBT (also in our case) and can be neglected. However, for the sake of model completeness for the transistor with larger g_o and as an intrinsic element, it is included in the formulation. On the other hand, the parasitic small series inductance (L_{bx}, L_{ex} and L_{cx}) are neglected.

The analysis conducted in section 4.3.3 is modified to taking parasitic emitter resistance $r_{ee'}$ effects into account. Instead of terminal voltage v_b in (4.18), the junction voltage to ground $v_{b'}$ and $v_{c'}$ are defined at node b' and c' respectively.

$$v_{b'} = v_\pi + v_{e'e} = v_\pi + r_{ee'}(i_b + i_{c'}) \tag{4.38}$$

$$v_{c'} = v_{c'e'} + v_{e'e} = v_{c'e'} + r_{ee'}(i_b + i_{c'}) \tag{4.39}$$

Applying (4.15) and (4.16) into (4.38) and (4.39) gives the junction voltage v_π in term of nodal voltages $v_{b'}$ and $v_{c'}$ as

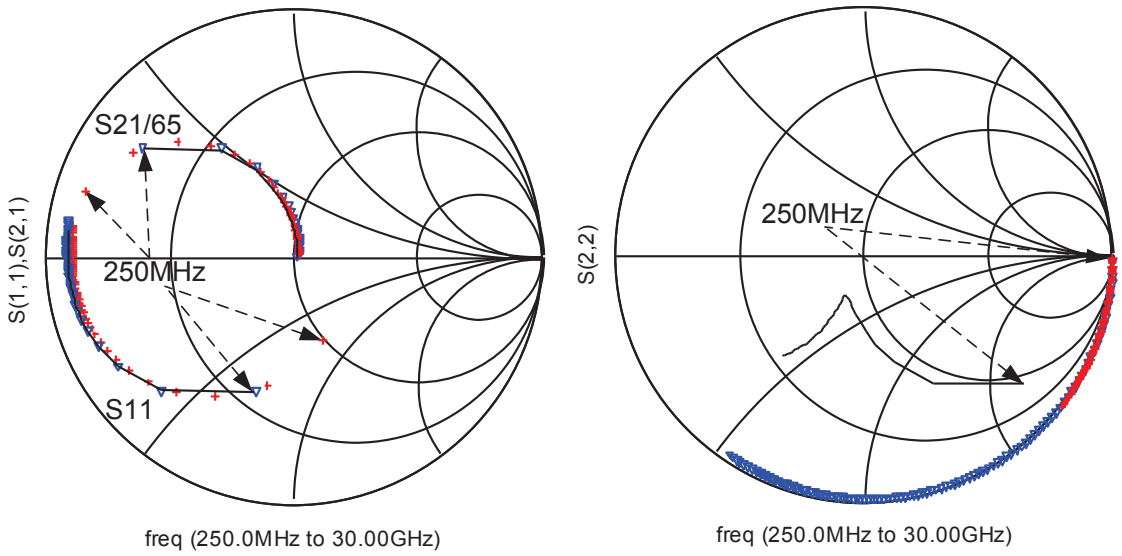


Figure 4.21: Simulated S-parameter responses of bilateral model (solid-line), simplified unilateral (cross) and Miller's approximation (triangle).

$$v_\pi = \frac{v_{b'} - r_{ee'} g_o (v_{c'} - v_{b'})}{1 + r_{ee'}(Y_\pi + g_m + g_o)}. \tag{4.40}$$

Then the small-signal base and collector current including emitter feedback resistance effect, can be derived as

$$i_b = \left(\frac{1}{\Delta} Y_\pi \left(1 + r_{ee'} g_o\right) + j\omega C_\mu\right) v_{b'} - \left(\frac{1}{\Delta} Y_\pi r_{ee'} g_o + j\omega C_\mu\right) v_{c'}, \tag{4.41}$$

$$i_c = \left(\frac{1}{\Delta}\left(g_m - Y_\pi r_{ee'} g_o\right) - j\omega C_\mu\right) v_{b'} + \left(\frac{1}{\Delta}\left(g_o + Y_\pi r_{ee'} g_o\right) + j\omega C_\mu\right) v_{c'}. \tag{4.42}$$

where $\Delta = 1 + r_{ee'}(Y_\pi + g_m + g_o)$. Then (4.41) and (4.42) can alternatively be presented as,

$$i_b = \left(Y_{\pi 1} + j\omega C_\mu\right) v_{b'} - \left(g_\mu + j\omega C_\mu\right) v_{c'}, \tag{4.43}$$

$$i_c = \left(g_{m1} - j\omega C_\mu\right) v_{b'} + \left(g_{o1} + j\omega C_\mu\right) v_{c'} \tag{4.44}$$

With,

$$Y_{\pi 1} = a_1 Y_\pi = Y_\pi \left[\frac{(1 + r_{ee'} g_o)}{1 + r_{ee'}(Y_\pi + g_m + g_o)} \right], \; g_\mu = a_2 g_o = g_o \left[\frac{r_{ee'} Y_\pi}{1 + r_{ee'}(Y_\pi + g_m + g_o)} \right]$$

(4.45a)

$$g_{m1} = a_3 g_m = g_m \left[\frac{1 - r_{ee'} g_o Y_\pi / g_m}{1 + r_{ee'}(Y_\pi + g_m + g_o)} \right], \; g_{o1} = a_4 g_o = g_o \left[\frac{1 + r_{ee'} Y_\pi}{1 + r_{ee'}(Y_\pi + g_m + g_o)} \right].$$

(4.45b)

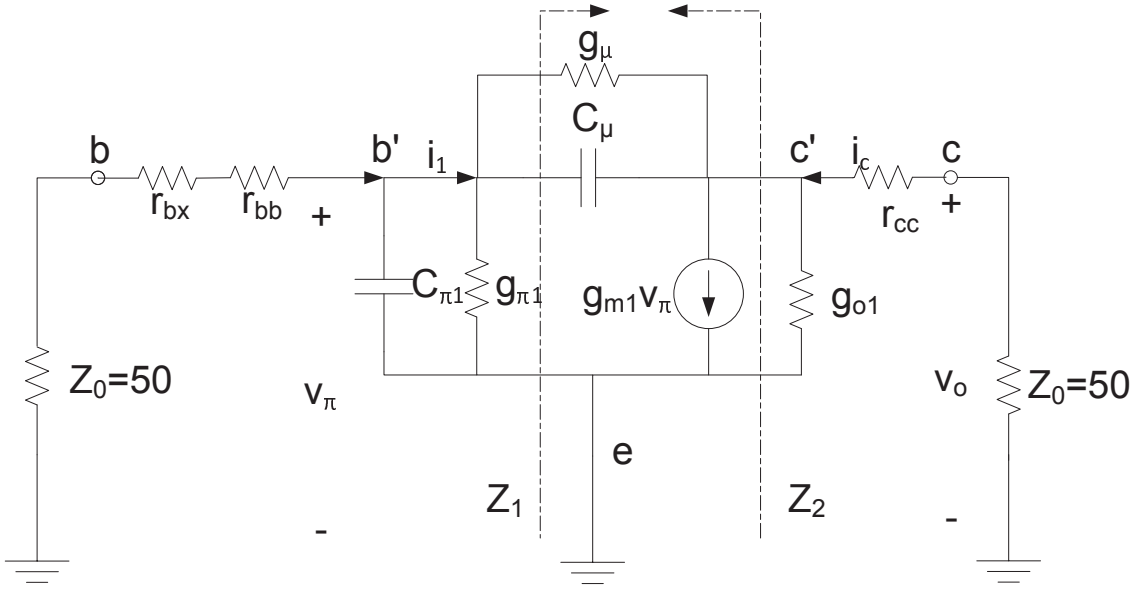


Figure 4.22: The equivalent circuit after $r_{ee'}$ is uncoupled (intermediate state).

In the case where Y_π is much smaller than g_m (with g_o neglected), (4.45) will be reduced to local series-series feedback concept shown in [68, 118, 119]. With some necessary circuit elements modification as in (4.45), emitter resistance is uncoupled. As long as g_o is concerned, an additional conductance is needed to add in parallel with C_μ. The four coefficients a_1, a_2, a_3 and a_4 in (4.45) are smaller than 1, The effective

base-emitter admittance $Y_{\pi 1}$, trans-conductance g_{m1} and output conductance g_{o1} are smaller than original values. Meanwhile C_μ is unaffected. The resultant equivalent circuit after uncoupling $r_{ee'}$ is presented in Fig. 4.22.

Decoupling Z_μ

Decoupling the feedback, $Z_\mu = (g_\mu + j\omega C_\mu)^{-1}$ between base and collector requires quantification of the equivalent impedances Z_1 (looking toward load) and Z_2 (looking toward source) as shown in Fig. 4.22. They are specified under the condition that the input and output port are terminated with 50Ω. Analyzing i_1,shown in Fig. 4.22, flowing into Z_μ and applying KCL at node c' gives,

$$i_1 = (v_\pi - v_c)\, Y_\mu, \tag{4.46}$$

$$g_{m1} v_\pi + \frac{v_o}{Z_0} + \left(1 + \frac{r_{cc}}{Z_0}\right) g_o v_o + \left[v_o \left(1 + \frac{r_{cc}}{Z_0}\right) - v_\pi\right] Y_\mu = 0. \tag{4.47}$$

$$\left[g_{m1} - Y_\mu\right] v_\pi + \frac{1}{Z_0}\left[1 + g_o\left(Z_0 + r_{cc}\right) + j\omega\left(Z_0 + r_{cc}\right) C_\mu\right] v_o = 0 \tag{4.48}$$

Let $Z_l = Z_0 + r_{cc}$ and then Z_1 can be calculated as,

$$Z_1 = \frac{v_\pi}{i_1} = \left[\left(1 - A_v\right) Y_\mu\right]^{-1} \tag{4.49}$$

$$A_v = \frac{v_o}{v_\pi} = -g_{m1} Z_l \left(\frac{1 - \dfrac{Y_\mu}{g_{m1}}}{1 + g_o Z_l + Z_l Y_\mu}\right) \tag{4.50}$$

The impedance Z_1 is frequency dependent. However, neglecting g_μ and low frequency analysis will yield Z_1 to be the impedance of the Miller approximation equivalent. The equivalent output impedance, Z_2, can be express as,

$$Z_2 = \left[Z_{\pi 1}^{'} + Z_{\mu}\right] // \left[\frac{\left(g_{m1} Z_{\pi 1}^{'}\right)}{\left(Z_{\pi 1}^{'} + Z_{\mu}\right)}\right]^{-1} \tag{4.51}$$

$$Z_{\pi 1}^{'} = \left(Z_0 + r_b\right) \| Z_{\pi 1} \tag{4.52}$$

where, $r_b = r_{bb} + r_{bx}$ Then, the real and imaginary parts of Z_2 can be defined as,

$$\mathrm{Re}\, Z_2 = \frac{g_T A + \omega^2 C_T B}{A^2 + \omega^2 B^2}, \;\; \mathrm{Im}\, Z_2 = -j\omega \frac{g_T B - C_T A}{A^2 + \omega^2 B^2} \tag{4.53}$$

$$A = \left[g_{\mu}\left(g_{\pi 1}^{'} + g_{m1}\right) - \omega^2 C_{\pi 1}^{'} C_{\mu}\right], \;\; B = \left[C_{\mu}\left(g_{\pi 1}^{'} + g_{m1}\right) - C_{\pi 1}^{'} g_{\mu}\right] \tag{4.54}$$

where, $g_T = g_{\pi 1}^{'} + g_{\mu}$ and $C_T = C_{\pi 1}^{'} + C_{\mu}$. Equation(4.53) provides an inclusive close form formula for impedance Z_2 without pre-assumption and neglected circuit elements. However, g_o for our transistor is very small and so related terms, including g_{μ}, are negligible. Then (4.53) can be simplified into,

$$\mathrm{Re}\, Z_2 = \frac{-\omega^2 g_{\pi 1}^{'} C_{\pi 1}^{'} C_{\mu} + \omega^2 C_T C_{\mu}\left(g_{\pi 1}^{'} + g_{m1}\right)}{\left(\omega^2 C_{\pi 1}^{'} C_{\mu}\right)^2 + \omega^2 C_{\mu}^2 \left(g_{\pi 1}^{'} + g_{m1}\right)^2} \tag{4.55}$$

$$\mathrm{Im}\, Z_2 = -j\omega \frac{\omega^2 C_T C_{\pi 1}^{'} C_{\mu} + C_{\mu} g_{\pi 1}^{'}\left(g_{\pi 1}^{'} + g_{m1}\right)}{\left(\omega^2 C_{\pi 1}^{'} C_{\mu}\right)^2 + \omega^2 C_{\mu}^2 \left(g_{\pi 1}^{'} + g_{m1}\right)^2} \tag{4.56}$$

Equation(4.55) and (4.56) are the same formulas used in [118, 119] with no g_{μ} consideration. This proofs the robustness of the formulation. As shown in Fig. 4.19, S_{22} is switching from series R-C at low frequencies to shunt R-C behavior at high frequencies. Hence, frequency limit is imposed and under low frequency analysis, (4.56) can be further simplified into,

$$\mathrm{Re}\, Z_2 = R_2 \approx \frac{C_{\pi 1}^{'}}{C_{\mu}} \frac{g_{m1}}{\left(g_{\pi 1}^{'} + g_{m1}\right)^2} + \frac{1}{\left(g_{\pi 1}^{'} + g_{m1}\right)} \tag{4.57}$$

$$\mathrm{Im}\, Z_2 = \frac{1}{j\omega C_2} \approx -j\frac{g_{\pi 1}^{'}}{\omega C_\mu (g_{\pi 1}^{'} + g_{m1})} \tag{4.58}$$

Equations(4.57) and (4.58) show at low frequencies Z_2 can be seen as a series network of a resistance (R_2) and a capacitance (C_2). This agrees with bilateral S_{22} response shown in Fig. 4.19. At high frequencies,

$$\mathrm{Re}\, Y_2 = \frac{1}{R_3} \approx g_{\pi 1}^{'}\left(\frac{C_\mu}{C_T}\right)^2 + \frac{g_{m1}C_\mu}{C_T} \tag{4.59}$$

$$\mathrm{Im}\, Y_2 = j\omega C_3 \approx j\omega\frac{C_\mu C_{\pi 1}^{'}}{C_T} \tag{4.60}$$

where, $Y_2 = 1/Z_2$. In (4.59) and (4.60), R_3 and C_3 are in parallel. Again, this also follows S_{22} response at high frequency. As the output network is being modified, the trans-conductance (g_{m1}) is being compensated as,

$$g_{m2} = g_{m1}\,|Z_m|\, e^{i\theta_m}. \tag{4.61}$$

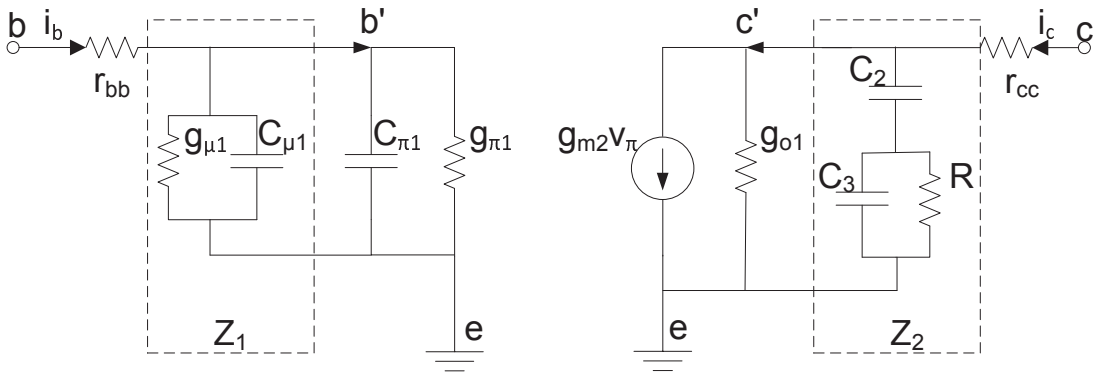


Figure 4.23: Developed equivalent unilateral circuit model.

Where, $Z_m = (Z_0 + Z_2)/Z_2$. The modified g_{m2} is strongly varying in the frequency region of <5GHz.

Two equation pairs (4.57) and (4.58) and (4.59) and (4.60) will yield two different R-C values. However, numerical valuation at different bias points revels that R_2 and R_3 have slightly different values (6% of their absolute values). Hence, we select a resistance (R), which is a mean of R_2 and R_3. Complete unilateral equivalent circuit model is presented in Fig. 4.23. Note that a single resistor is presented in Z_2 network for both low and high frequencies.

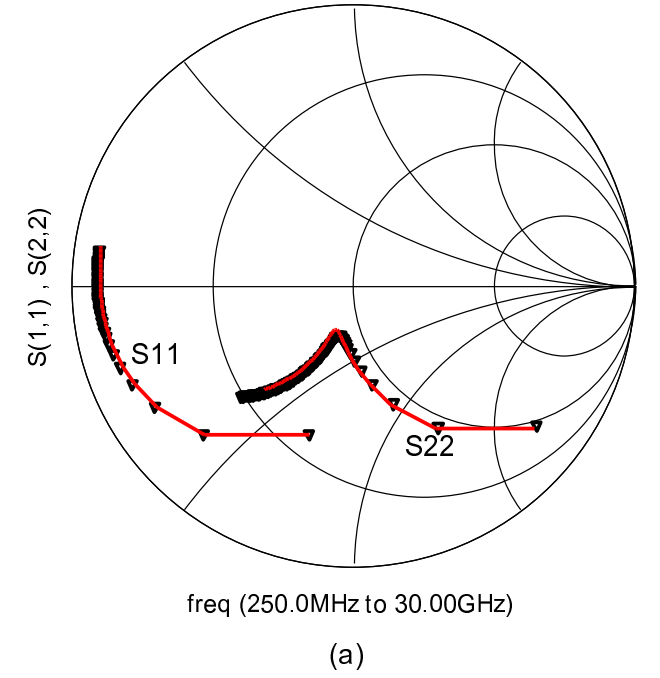
4.5.3 Simulated Results and Discussion

In order to validate and evaluate the accuracy of the proposed technique, we transform the bilateral model shown in Fig. 4.18 into unilateral. Table 4.2 gives the computed unilateral model parameter values using the aforementioned technique.

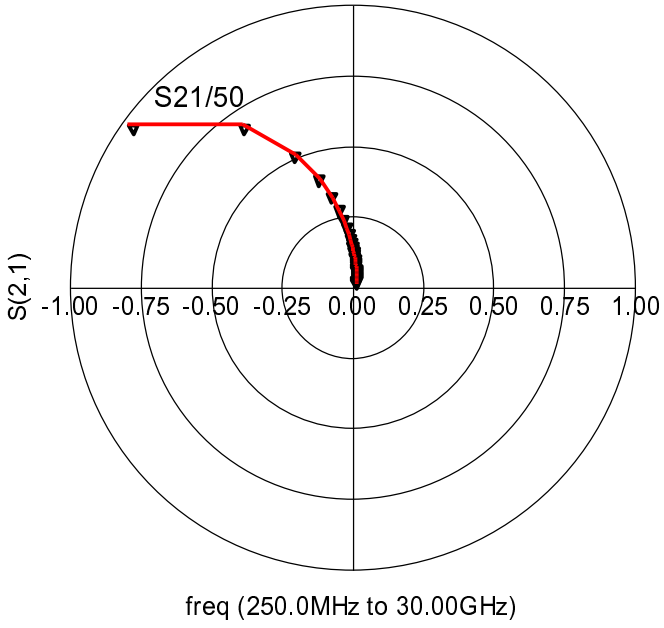
Table 4.2: Computed unilateral parameter values for for$V_{cc} = 4V$, $I_{cc} = 39mA$, $3 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT.

Parameter	Value	Parameter	Value
r_b	2.8Ω	$C_{\mu 1}$	8.0pF
$r_{cc'}$	1.2Ω	g_{m1}	1.02S
$g_{\pi 1}$	13.13mS	R	43.5Ω
$C_{\pi 1}$	6.5pF	C2	4.7pF
C3	135fF	-	-

Both g_o and g_μ are neglected in the simulation. The trans-conductance g_{m2} is defined as frequency dependent parameter. The circuit models are simulated in Agilent's ADS. Parasitic contact inductances of L_b=20.17pH, L_c=18.532pH and L_e=5pH are included in the simulation.

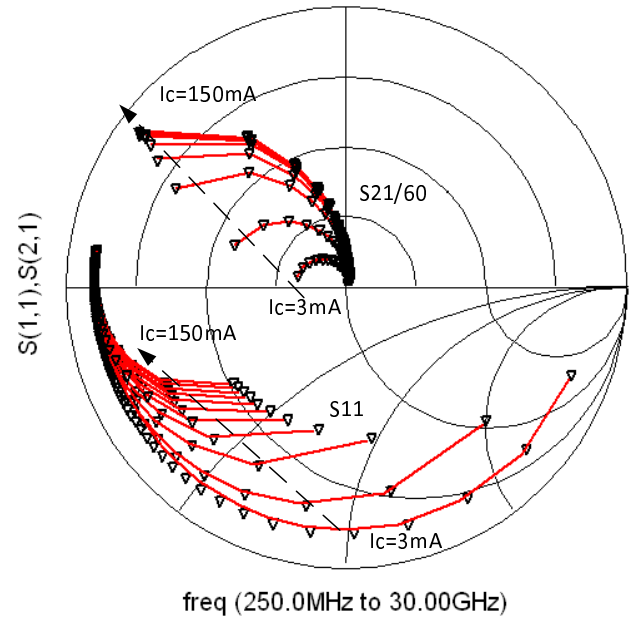


(a)

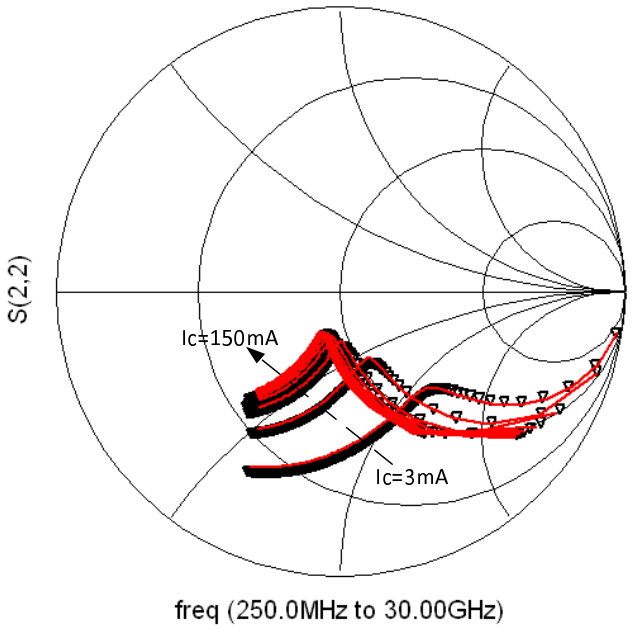


(b)

Figure 4.24: Simulated S-parameters response of bilateral (line) and developed unilateral model response (triangle) for $V_{cc} = 4V$ and $I_c = 39mA$.

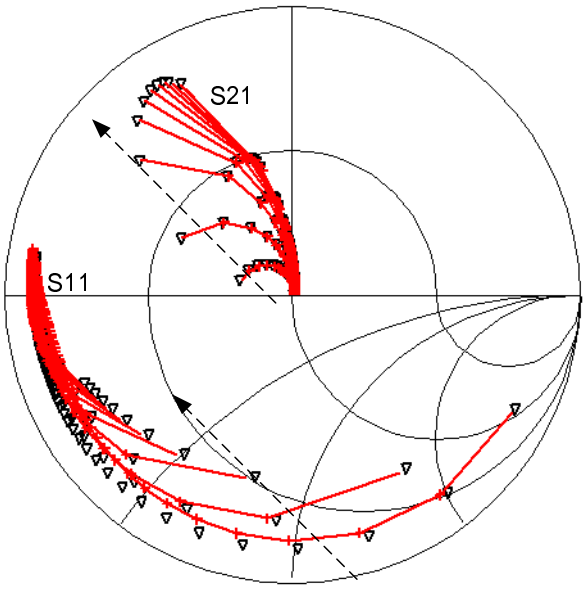


(a)

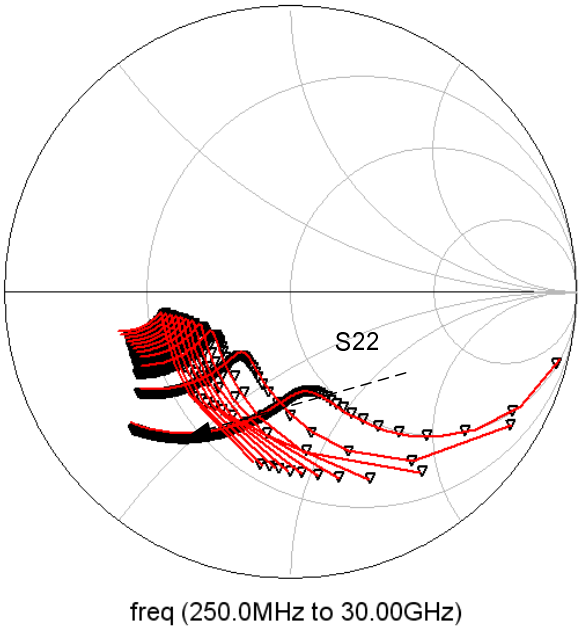


(b)

Figure 4.25: Simulated S-parameter response of bilateral (lines) and developed unilateral (triangle) circuit models for $V_{cc} = 5V$ and from $I_c = 3mA$ to $150mA$.



(a)



(b)

Figure 4.26: Simulated S-parameter response of bilateral (lines) and developed unilateral (triangle) circuit models for $V_{cc} = 1V$ and from $I_c = 3mA$ to $150mA$.

Figure 4.24 shows the comparison of S-parameters generated from the bilateral and unilateral model for the bias point of I_c=39mA and V_{cc}=4V. Very good agreements over the frequency range of 250MHz to 30GHz are obtained.

The robustness of the technique is investigated at various bias points. Bilateral parameters, extracted for various collector currents (3mA to 150mA) at V_{cc}=1V and V_{cc}=5V, are used to develop unilateral equivalent circuit models. Fig. 4.25 and Fig. 4.26 show the overlay plot of simulated unilateral and bilateral S-parameters data at V_{cc}=5V and V_{cc}=1V respectively. Unilateral responses agree very well with bilateral response for all collector currents. This indicates that the technique is robust and applicable for different bias sets.

4.5.4 Conclusion

In this chapter, the detail steps of parameter extraction and small-signal modeling are presented. Bilateral hybrid-π model parameters are extracted from S-parameters data which have been measured at various bias conditions. The developed bilateral model is validated using measured results. The importance of valid unilateral model for high frequencies and high power application is examined and the short-fall of simplified unilateral assumption and Miller's approximation are presented. The analysis is extended to develop a unilateral circuit model for InGaP/GaAs HBT technology over a wide range of frequencies. The model is validated with measurement and bilateral results. The developed unilateral model agrees very well with the bilateral responses over 250MHz to 30GHz at various collector-emitter voltages and currents.

Chapter 5

Ultra-Broadband Power Amplifier Design

5.1 Introduction

Broadband technique has received significant attention as a promising and strongly evolving technique as it spread the signal power over a wide range of the radio spectrum giving frequency diversity, high spatial resolution and high sensitivity. This technique has been using in wide range of systems including high data rate communication, high resolution short range radar sensors, multiband WiFi, WiMAX, high precision localization systems, instrumentation and electronic warfare.

5.2 Distributed Amplifier

The principle of distributed amplification was originally initiated from an attempt to increase the gain-bandwidth product limit of an amplifier by spreading the individual junction capacitances while adding their trans-conductances [5]. Instead of lumping

junction capacitances at the input and output of the active devices, they are spatially distributed. So, DA allows, at least in theory, the combination of as many amplifying devices as desired without compromising the gain - bandwidth product of each device. This is the main reason why this topology is preferred over others for achieving broadband amplification behavior.

By making use of transistor's junction capacitances together with interconnecting metal inductances, the network seemingly form a transmission line, which basically consist of a ladder network of series inductance and shunt capacitance. The DA is associated with two artificial transmission lines one that makes up the input base line and another that forms the collector output line. These two lines basically consist of a ladder network of series inductance and shunt capacitances, hence forming a constant-k artificial transmission line. The shunt capacitor of base line is provided by base emitter capacitance and collector to emitter capacitance is used for collector line. Inductors or high impedance transmission lines are used as inductive components of the artificial transmission lines. Figure 5.1 shows simplified bilateral small-signal equivalent circuit of HBT and Fig. 5.2(a) shows schematic of DA with its input and output artificial transmission line making use of base-emitter junction capacitance (C_π) and collector-emitter capacitance (C_o) of HBTs. Figure 5.2 (b) shows a DA schematic when the transistor are assumed unilateral.

5.3 Fundamental of Distributed Amplifier

The distribution of a prescribed capacitance over an extended network allows one to maintain a required impedance level, through impedance transformation, and hence achieve the desired gain without sacrificing bandwidth. To characterize the transmission properties of distributed networks, each section of the networks is facilitated as a

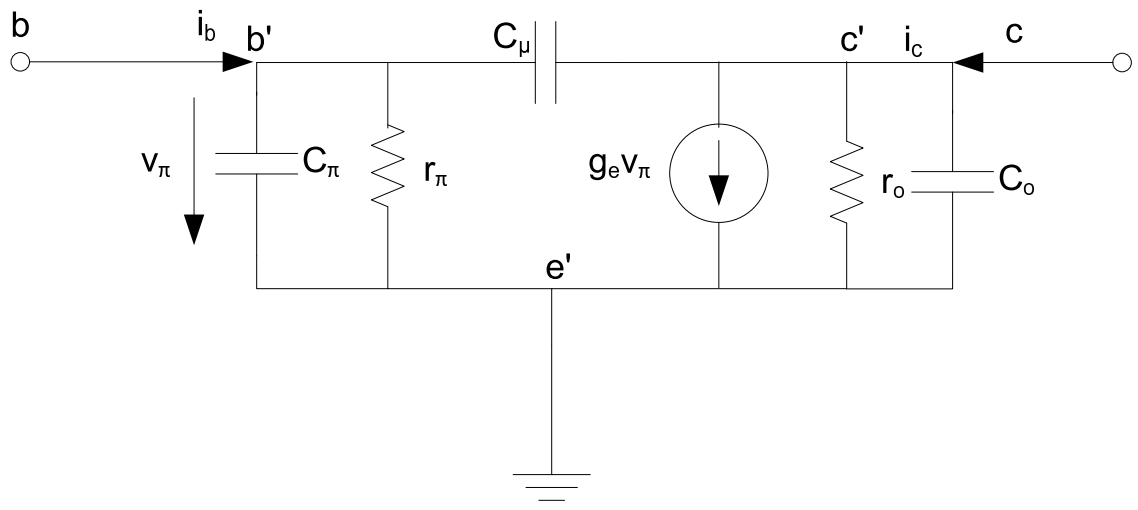


Figure 5.1: Simplified small-signal equivalent circuit model of a HBT.

two port network as shown in Fig. 5.3(a). In many aspects it is no different from a filter and can be analyzed as two elementary L filter section as shown in Fig. 5.3(b). The image impedances are referred as Z_{0T} and $Z_{0\pi}$ and are the characteristic impedance of the T-network and π-network. Their impedance can be express using network element as

$$Z_{0T} = \sqrt{\frac{Z}{Y}\left(1 + \frac{ZY}{4}\right)}, \tag{5.1}$$

$$Z_{0\pi} = \sqrt{\frac{Z}{Y}\left(1 + \frac{ZY}{4}\right)^{-1}}. \tag{5.2}$$

The characteristic impedance of the network can be define using the image impedances as

$$\mathrm{Z}_0 = \sqrt{Z_{0T} Z_{0\pi}} \tag{5.3}$$

The propagation factor of an L section is bilateral as a result of reciprocity, the T and π sections have the same propagation factor, which is twice that of the corresponding L section.

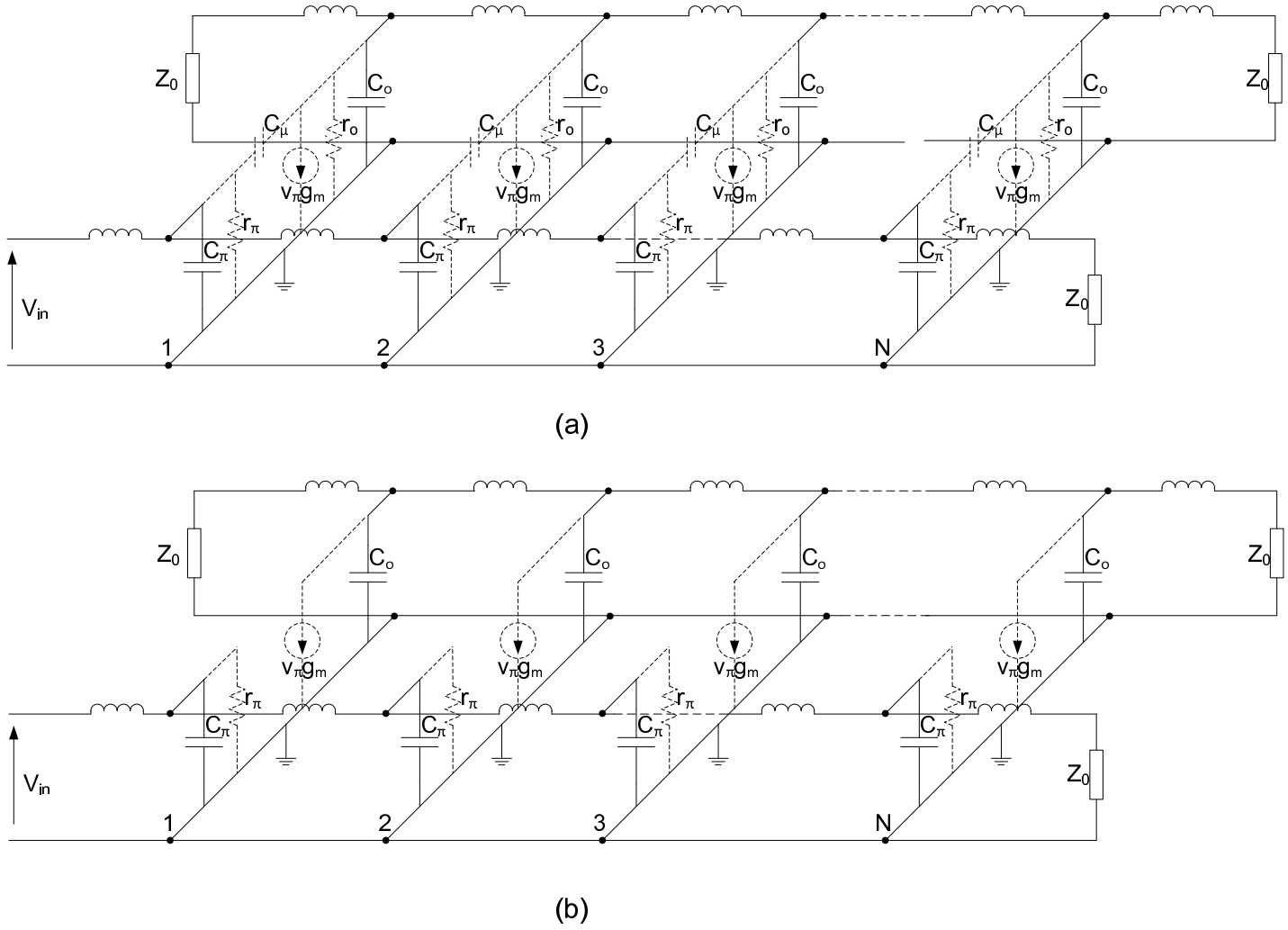


Figure 5.2: Schematic of distributed amplifier with bilateral small-signal circuit model (a) and unilateral circuit model (b).

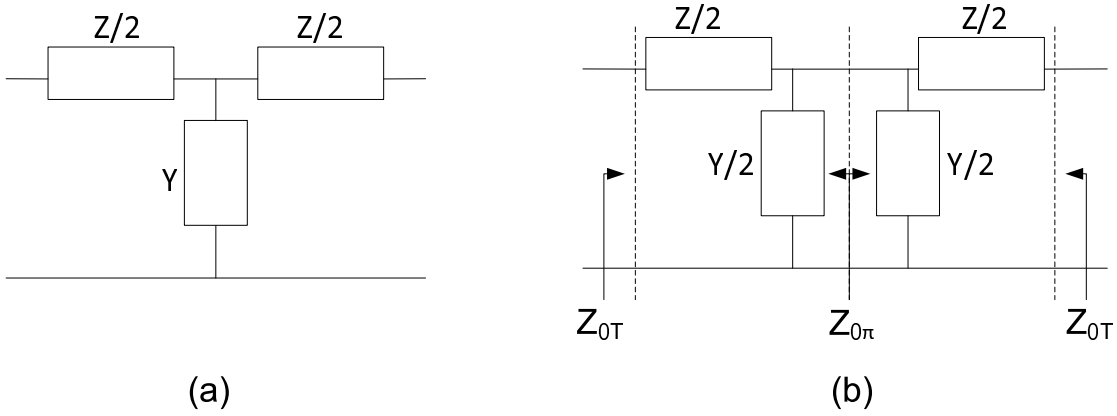


Figure 5.3: Equivalent network section of base and collector artificial transmission line (a) and elementary L section representation (b).

The exact solution for propagation constant of T or π section is

$$\gamma = \alpha + j\beta = \ln\left[1 + \frac{ZY}{2} + \sqrt{ZY\left(1 + \frac{ZY}{4}\right)}\right]. \tag{5.4}$$

A transmission network is formed when the filter sections discussed are cascaded to form a ladder structure and appropriate excitation and termination are placed at the terminal ports. HBTs are used as the active devices and hence, the input artificial transmission line is referred as the *base line* and the output artificial line is referred as the *collector line*, from which the subscripts b and c follow.

5.3.1 Lossless Analysis

The distributed amplifier represents a rather complex active system. To gain insight into the operation of a complex physical system, as a first step, a simplified model that retains only the most essential features is analyzed first. In this sense the analysis of distributed amplifier is facilitated by the assumptions of lossless transmission networks and unilateral active device. Then each network section on the base line and collector

line can be simplified as in Fig. 5.4.

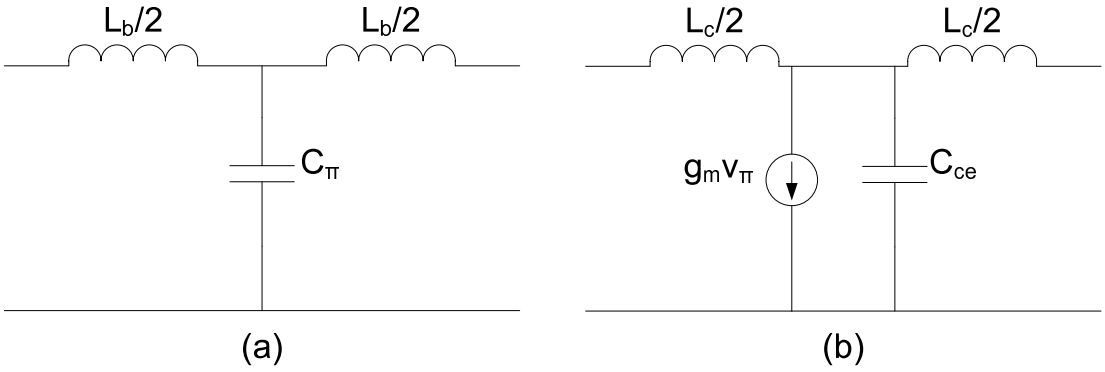


Figure 5.4: A lossless network section of the base line (a) and collector line (b).

Hence, the base-emitter admittance (Y_b), base line series impedance (Z_b), collector-emitter admittance (Y_c) and collector line series impedance (Z_c) are

$$Z_b = j\omega L_b,\ Y_b = j\omega C_\pi, \tag{5.5}$$

$$Z_c = j\omega L_c,\ \text{and}\ Y_c = j\omega C_{ce} \tag{5.6}$$

respectively. Where, ω is angular frequency. To get real transmission line impedances, both image impedance Z_{0T} and $Z_{0\pi}$ must be either real or complex with opposite argument. We can compute the characteristics of the artificial transmission lines along with cutoff frequencies as

$$Z^b_{0T} = \sqrt{\frac{L_b}{C_\pi}\left(1-\frac{\omega^2}{\omega^2_{cb}}\right)},\ Z^b_{0\pi} = \sqrt{\frac{L_b}{C_\pi}\left(1-\frac{\omega^2}{\omega^2_{cb}}\right)^{-1}}, \tag{5.7}$$

$$Z^c_{0T} = \sqrt{\frac{L_c}{C_{ce}}\left(1-\frac{\omega^2}{\omega^2_{cc}}\right)},\ Z^c_{0\pi} = \sqrt{\frac{L_c}{C_{ce}}\left(1-\frac{\omega^2}{\omega^2_{cc}}\right)^{-1}} \tag{5.8}$$

$$\omega_{cb} = \frac{2}{\sqrt{L_b C_\pi}},\ \omega_{cc} = \frac{2}{\sqrt{L_c C_{ce}}} \tag{5.9}$$

$$Z_0^b = \sqrt{\frac{L_b}{C_\pi}},\ Z_0^c = \sqrt{\frac{L_c}{C_{ce}}} \tag{5.10}$$

And the propagation constant of each section of base and collector line can be express as

$$\gamma_x = \alpha_x + \beta_x = \ln\left[1 - \frac{2\omega^2}{\omega_{cx}^2}\left(1 + \sqrt{1 - \frac{\omega_{cx}^2}{\omega^2}}\right)\right]. \tag{5.11}$$

Where, $x = b$ or c. For a network with pure reactance, this is not difficult to compute. It should be noted that the logarithm of a complex quantity of $A\angle a$ is equal to $\ln A + ja$. Simplified solution can be seen at [5],

$$\cosh\gamma = 1 + \frac{ZY}{2}, \tag{5.12}$$

$$\cosh\gamma = \cosh\alpha\cos\beta + j\sinh\alpha\sin\beta. \tag{5.13}$$

However, in (5.13) we have made use of $\sinh\alpha \simeq \alpha$ for small α and hence approximation using the (5.13) is only valid for small value of α. The accuracy of (5.13) decreases as the operating frequency approach cutoff frequency of the line [5]. More precise network performances over the frequencies can be achieved with (5.4). The voltage presented at the base of each active cell can be express as

$$V_{\pi n} = V_{in}\sqrt{\frac{Z_{o\pi}^b}{Z_{oT}^b}}e^{-(n-1/2\,)\gamma_b} = V_{in}\frac{\omega_{cb}^2}{(\omega_{cb}^2 - \omega^2)}e^{-(n-1/2\,)\gamma_b} \tag{5.14}$$

where $n = 1, 2, 3, ..., N$.

Generally, artificial transmission line is excited by a confined source located at the sending end of the line. However the output transmission line networks found in distributed amplifiers are excited by multiple sources as shown in Fig. 5.2.Output

current generated by each active device can be derived as

$$I_{cn} = g_m V_{\pi n} = V_{in} \frac{g_m \omega_{cb}^2}{(\omega_{cb}^2 - \omega^2)} e^{-(n-1/2\,)\gamma_b}. \tag{5.15}$$

Total current at the load, along with characteristic impedance termination at the other end of the line, can be computed using superposition technique as

$$I_o = \frac{1}{2} \sum_{n=1}^{N} I_{cn} e^{-(N-n+1/2\,)\gamma_c}, \tag{5.16}$$

and output voltage match load is

$$V_o = Z_{0c}\ I_o. \tag{5.17}$$

Assuming base and collector lines are identical and phased synchronized, then $\gamma_b = \gamma_c = \gamma$ and the voltage gain is,

$$A_v = \frac{Z_0^c N g_m}{2} \frac{\omega_c^2}{\sqrt{\omega_c^2 - \omega^2}} e^{-N\gamma}, \tag{5.18}$$

and the amplifier power gain can be calculated as,

$$G = \frac{P_{out}}{P_{in}} = \frac{I_o^2 Z_0^c}{\left|\frac{V_{in}}{Z_0^b}\right|^2 Z_0^b} = \frac{N^2 g_m^2 \omega_c^2 Z_0^b Z_0^c}{4\,(\omega_c^2 - \omega^2)} e^{-2N\gamma}. \tag{5.19}$$

5.4 Physical Oriented Lossy Section Analysis for HBTs

In reality, additional elements are often encountered in the equivalent circuit, in addition to the trans-conductance and the shunt capacitances. These additional elements

are usually dissipative, so their presence and specific location will affect the maximum gain-bandwidth product. Losses within the distributed amplifier cause its performance to deviate from that of the ideal one. The power dissipation in each active device or cell has significant influence on the amplifier characteristics.

5.4.1 Base Network Analysis

The input admittance of a HBT includes a small series inductance, a small series resistance, and a shunt resistor along with the useful junction capacitors. In addition, a series capacitance (C_{bs}) is added at the base of the HBTs cells to reduce the effective input capacitance. Without this series capacitance, the cutoff frequency and/or the characteristic impedance of the base line will be too low. A practical input equivalent circuit schematic of the HBT including , is shown in Fig. 5.5. This network represents the shunt arm of each transmission network sections and is more complex than the lossless case.

The values of the circuit elements are as follows: base series capacitance ($C_{bs} = 1pF$), effective junction capacitance ($C_{\pi eff} = C_{\pi 1} + C_{\mu 1}$) is =14.5pF, dynamic resistance ($r_{\pi 1} = 76\Omega$), intrinsic and extrinsic base resistance ($r_b = 2.8\Omega$) and parasitic inductance ($L_{bx} = 20.17pH$). Since, r_b and L_{bx} are relatively small, they are neglected. The inductor losses are assumed to be small so the series arms resistance R_b is set to zero. (*Note* - The analysis inclusive of these parasitic resistances and inductor losses is presented in appendix A). Then the series arm impedance and shunt arm admittance of each section of the base line become

$$Z_b = j\omega L_b \tag{5.20}$$

$$Y_b = \frac{-\omega^2 r_\pi C_{bs} C_\pi + j\omega C_{bs}}{1 + j\omega r_\pi \left(C_{bs} + C_\pi\right)} \tag{5.21}$$

and their image impedances can be express as

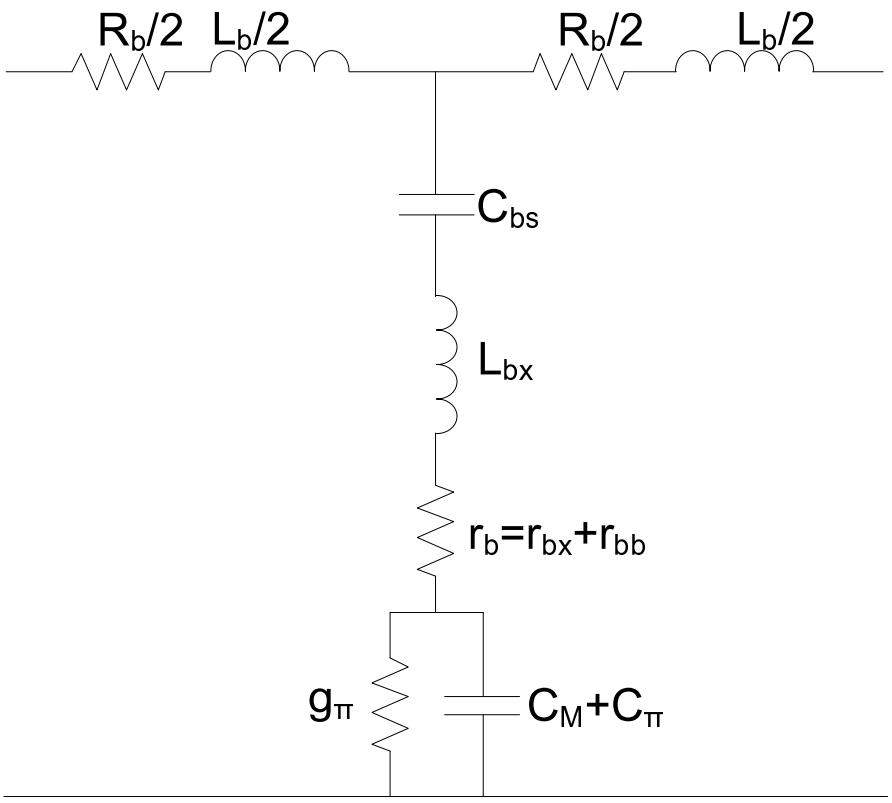


Figure 5.5: A network section of the base transmission line of DA, inclusive of HBT's parasitic and solution for design constrain.

$$Z_T^b = \sqrt{\frac{L_b}{C_{bs}} \frac{\left(1 + \frac{C_{bs}}{C_\pi} - j\frac{\omega_{attb}}{\omega}\right)}{\left(1 - j\frac{\omega_{attb}}{\omega}\right)} \left[1 - \frac{\frac{\omega^2}{\omega_{cb}^2}\left(1 + j\frac{\omega}{\omega_{attb}}\right)}{\frac{\omega}{\omega_{attb}}\left(\frac{\omega_{attb}}{\omega} + j\left(1 + \frac{C_{bs}}{C_\pi}\right)\right)}\right]} \tag{5.22}$$

$$Z_\pi^b = \sqrt{\frac{L_b}{C_{bs}} \frac{\left(1 + \frac{C_{bs}}{C_\pi} - j\frac{\omega_{attb}}{\omega}\right)}{\left(1 - j\frac{\omega_{attb}}{\omega}\right)} \left[1 - \frac{\frac{\omega^2}{\omega_{cb}^2}\left(1 + j\frac{\omega}{\omega_{attb}}\right)}{\frac{\omega}{\omega_{attb}}\left(\frac{\omega_{attb}}{\omega} + j\left(1 + \frac{C_{bs}}{C_\pi}\right)\right)}\right]^{-1}} \tag{5.23}$$

As C_{bs} and C_π are in series and $C_{bs} \ll C_\pi$, the cutoff frequency of the line in terms of

C_{bs} is

$$\omega_{cb} \approx \frac{2}{\sqrt{L_b C_{bs}}},\ \omega_{attb} = \frac{1}{r_\pi C_\pi}. \tag{5.24}$$

The series arm inductance ($L_b = 2.5nH$) is selected to achieve a cutoff frequency of around ≈ 6.4GHz and characteristic impedance $Z_0^b = 50\Omega$. Z_0^b of the base line can be computed using (5.22) and (5.23) as,

$$Z_0^b = \sqrt{\frac{L_b}{C_{bs}} \frac{\left(1 + \frac{C_{bs}}{C_\pi} - j\frac{\omega_{attb}}{\omega}\right)}{\left(1 - j\frac{\omega_{attb}}{\omega}\right)}}. \tag{5.25}$$

Figure 5.6 shows the computed Z_0^b with and without ($r_{\pi 1} = 76\Omega$ and $r_{\pi 1} = \infty$ respectively) the effect of $r_{\pi 1}$, as a function of frequency dependent variable ω/ω_{cb} . The attenuation and phase factors of the base-line can be determine using

$$\alpha_b = \mathrm{Re}\left\{\ln\left[1 + 2A + \sqrt{4A\left(1 + A\right)}\right]\right\}, \tag{5.26}$$

$$\beta_b = \mathrm{Im}\left\{\ln\left[1 + 2A + \sqrt{4A\left(1 + A\right)}\right]\right\}, \tag{5.27}$$

$$A = -\frac{\omega^2}{\omega_{cb}^2} \frac{\omega_{attb}}{\omega} \frac{\left(1 + j\frac{\omega}{\omega_{attb}}\right)}{\left(\frac{\omega_{attb}}{\omega} + j\left(1 + \frac{C_{bs}}{C_\pi}\right)\right)}. \tag{5.28}$$

Figure 5.7 shows the attenuation factor per section of the base artificial transmission line computed with and without the $r_{\pi 1}$ effect at different frequencies. Despite $r_{\pi 1} < 100\Omega$ large $C_{\pi eff}$ provides lower impedance path for the frequencies of interest. Hence, in the pass band attenuation causes by $r_{\pi 1}$ is very low and is comparable with the case without $r_{\pi 1}$. As different device technologies introduce different limitations, this base line attenuation behavior differs from FET based analysis, where the frequency and gain performance are limited by the large gate line attenuation [4]. Figure 5.8 shows the phase factor per section at different frequencies.

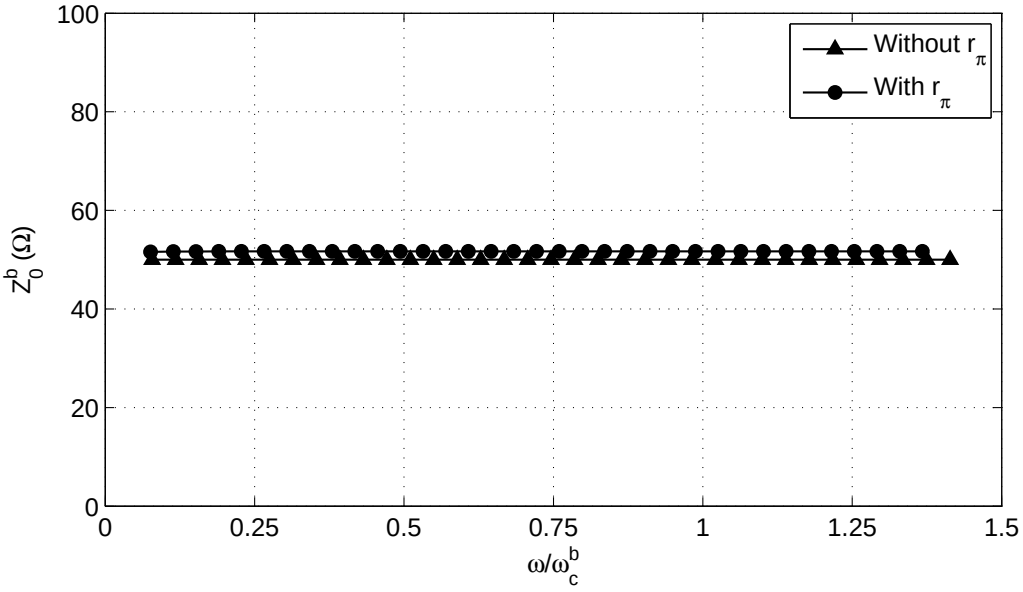


Figure 5.6: Characteristic impedance variation across frequencies at different r_π value. With r_π ($r_\pi = 76\Omega$) and without r_π ($r_\pi = \infty$).

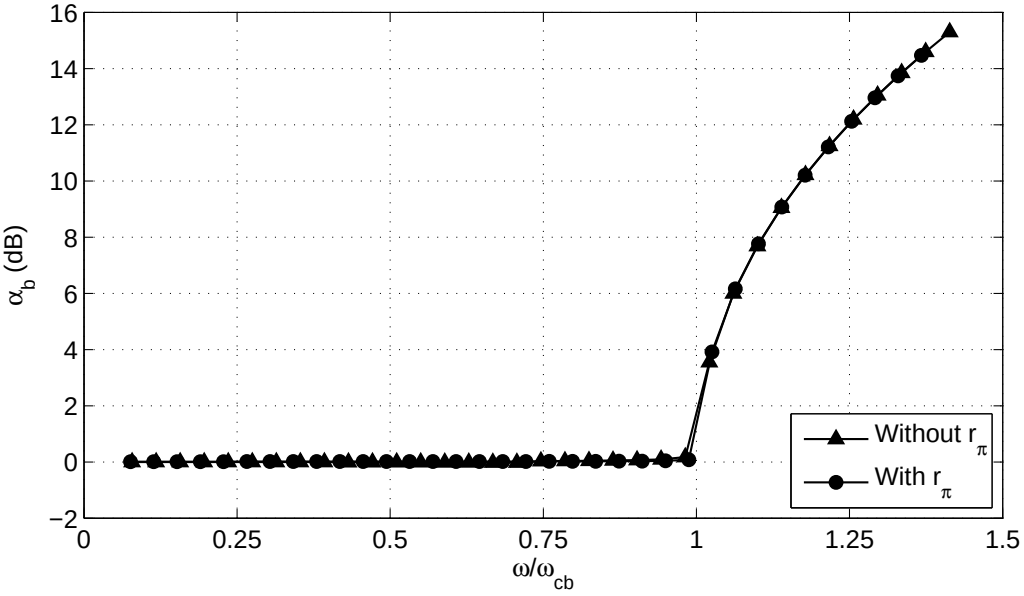


Figure 5.7: Attenuation characteristics over pass band and stop band per network section. With r_π ($r_\pi = 76\Omega$) and Without r_π ($r_\pi = \infty$).

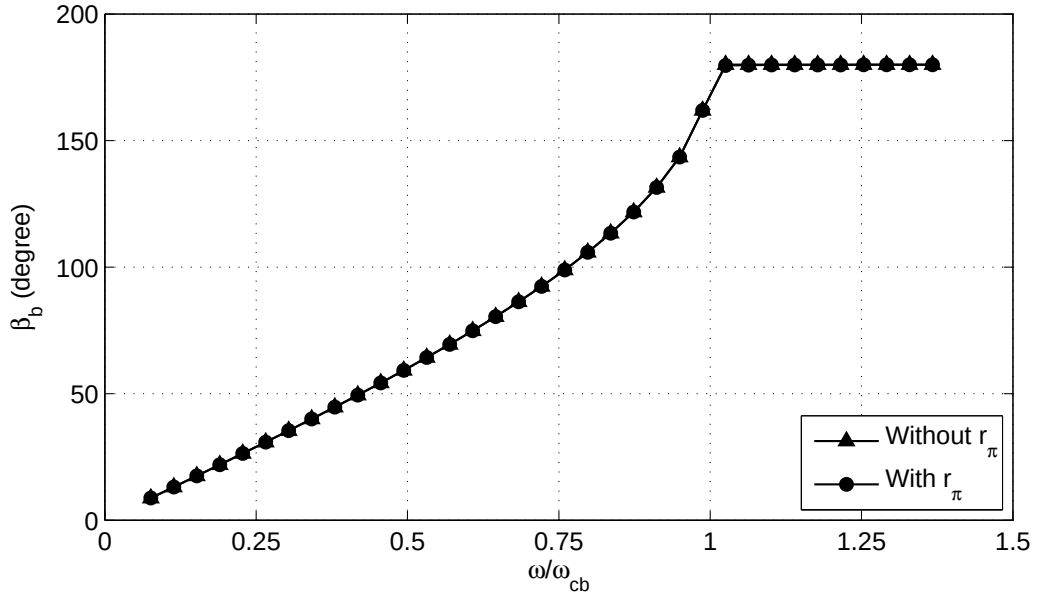


Figure 5.8: Phase characteristic over pass band and stop band per network section. With r_π ($r_\pi = 76\Omega$) and without r_π ($r_\pi = \infty$).

5.4.2 Collector Network Analysis

The equivalent circuit schematic of the output impedance of the HBT is presented in Fig. 5.9 and is periodically loaded along the collector-line. The values of capacitance (C_2) and resistance (R) are $4.7pF$ and 43Ω respectively. Unfortunately, the capacitance ($C_3 = 135fF$) is significant enough for high frequencies and is included in the shunt arm equivalent circuit.

Likewise for the base line, collector series resistance ($r_{cc} = 1.2\Omega$) and inductance ($L_{cx} = 18.532pH$) on the shunt arm are neglected. Series arms resistance R_c is also assumed to be zero. The network configuration of the collector line section is exactly the same as the base line and the same formulation can be applied.

$$Z_c = j\omega L_c \tag{5.29}$$

$$Y_c = \frac{-\omega^2 R C_2 C_3 + j\omega C_2}{1 + j\omega R\left(C_2 + C_3\right)} \tag{5.30}$$

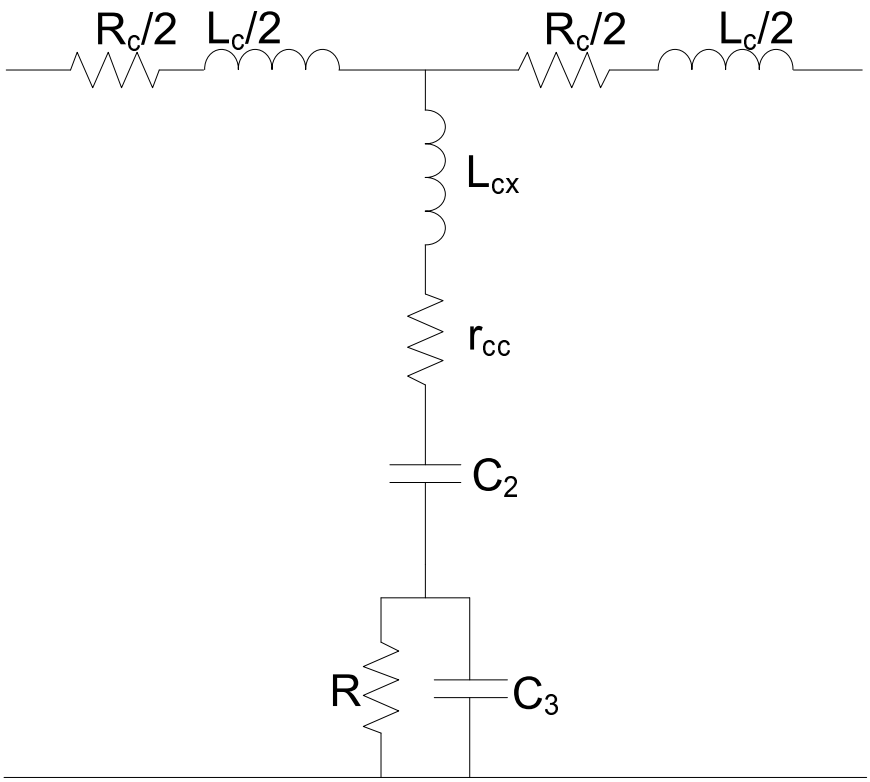


Figure 5.9: A network section of collector transmission line of DA, inclusive of parasitic, feed-back and terminating effects.

$$Z_T^c = \sqrt{\frac{L_c}{C_2}\frac{\left(1 + \frac{C_2}{C_3} - j\frac{\omega_{attc}}{\omega}\right)}{\left(1 - j\frac{\omega_{attc}}{\omega}\right)}\left[1 - \frac{\frac{\omega^2}{\omega_{cc}^2}\left(1 + j\frac{\omega}{\omega_{attc}}\right)}{\frac{\omega}{\omega_{attc}}\left(\frac{\omega_{attc}}{\omega} + j\left(1 + \frac{C_2}{C_3}\right)\right)}\right]} \tag{5.31}$$

$$Z_\pi^c = \sqrt{\frac{L_c}{C_2}\frac{\left(1 + \frac{C_2}{C_3} - j\frac{\omega_{attc}}{\omega}\right)}{\left(1 - j\frac{\omega_{attc}}{\omega}\right)}\left[1 - \frac{\frac{\omega^2}{\omega_{cc}^2}\left(1 + j\frac{\omega}{\omega_{attc}}\right)}{\frac{\omega}{\omega_{attc}}\left(\frac{\omega_{attc}}{\omega} + j\left(1 + \frac{C_2}{C_3}\right)\right)}\right]^{-1}} \tag{5.32}$$

$$\omega_{cc} = \frac{2}{\sqrt{L_c C_2}},\ \omega_{attc} = \frac{1}{RC_3} \tag{5.33}$$

Now, the characteristic impedance of the output line can be express as

$$Z_0^c = \sqrt{\frac{L_c}{C_2}\frac{\left(1+\frac{C_2}{C_3}-j\frac{\omega_{attc}}{\omega}\right)}{\left(1-j\frac{\omega_{attc}}{\omega}\right)}} \tag{5.34}$$

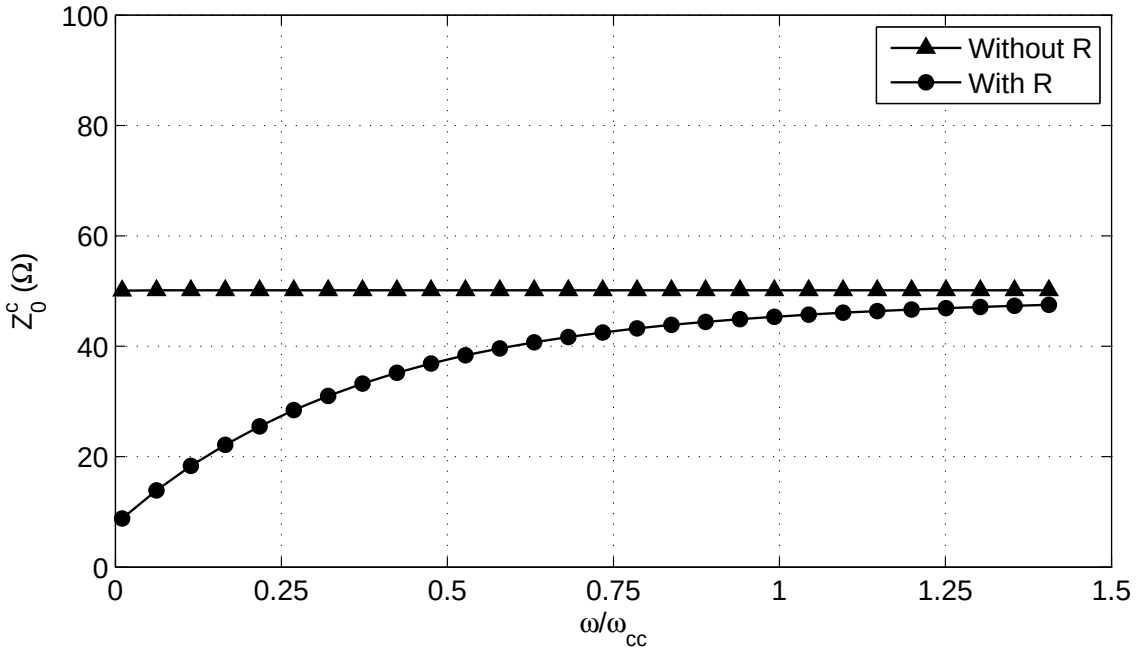


Figure 5.10: Characteristic impedance of the collector line at over pass band and stop band frequencies. With R (R = 43 Ω) and Without R (R = ∞).

Computed characteristic impedance of the collector line is presented in Fig. with the presence of R. The attenuation and phase factor for collector-line can be evaluated using

$$\beta_c = \mathrm{Im}\left\{\ln\left[1+2B+\sqrt{4B\left(1+B\right)}\right]\right\}, \tag{5.35}$$

$$\alpha_c = \mathrm{Re}\left\{\ln\left[1+2B+\sqrt{4B\left(1+B\right)}\right]\right\}, \tag{5.36}$$

$$B = -\frac{\omega^2}{\omega_{cc}^2}\frac{\omega_{attc}}{\omega}\frac{\left(1+j\frac{\omega}{\omega_{attc}}\right)}{\left(\frac{\omega_{attc}}{\omega}+j\left(1+\frac{C_2}{C_3}\right)\right)}. \tag{5.37}$$

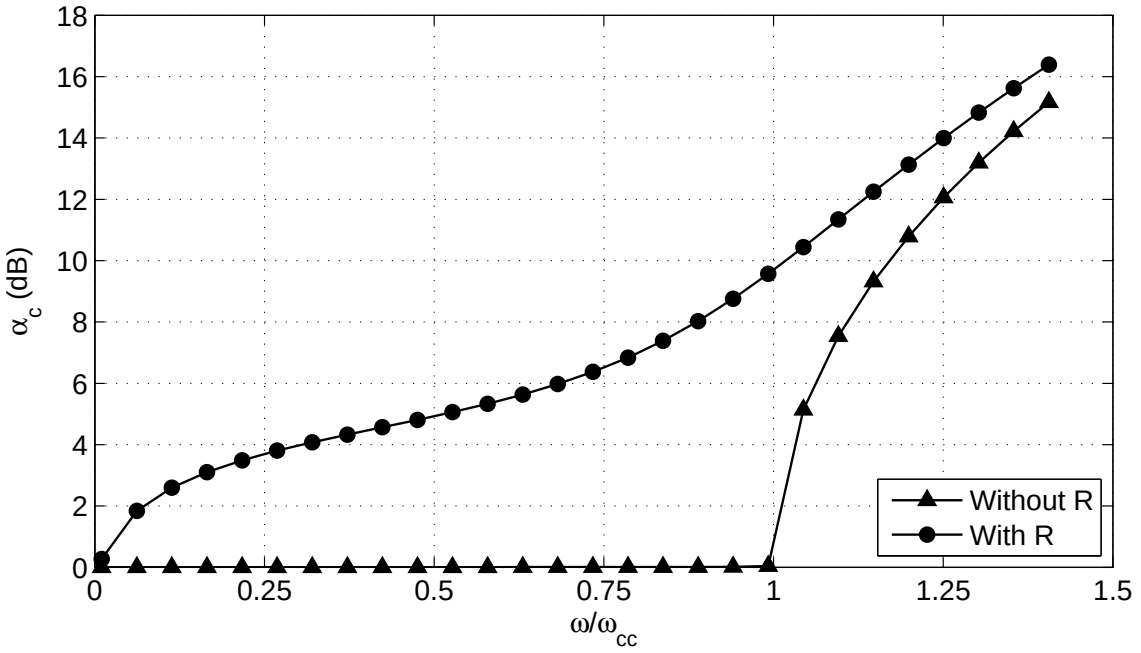


Figure 5.11: Collector line attenuation at different frequencies (per section). With R (R = 43 Ω) and Without R (R = ∞).

Figure 5.11 and Fig. 5.12 show the computed α_c and β_c as a function of frequency at two different R values ($R = 43\Omega$ and $R = \infty$). Small C_3 yield high impedance to the frequencies of interest and the signals in the interested band are highly attenuated by$R$, which is a low impedance alternative path to C_3. The attenuation per section is as high as $5dB$ at center frequency of 3GHz (mid-band) and close to $10dB$ at the cutoff frequency of the collector line. At this high attenuation the power generated from earlier cells will be highly attenuated as it travels along the line before reaching the load as illustrated in Fig. 5.13.

In the case where the attenuation of the line is negligible, (5.19) state that the

output power and power gain of the distributed amplifier will increase with increasing number of stages. However, high attenuation over the collector line make power contribution from early stages useless and result lower output power, higher DC consumption and lower PAE. Moreover, frequency dependent attenuation diminish the DA's bold advantages like gain flatness across the pass band.

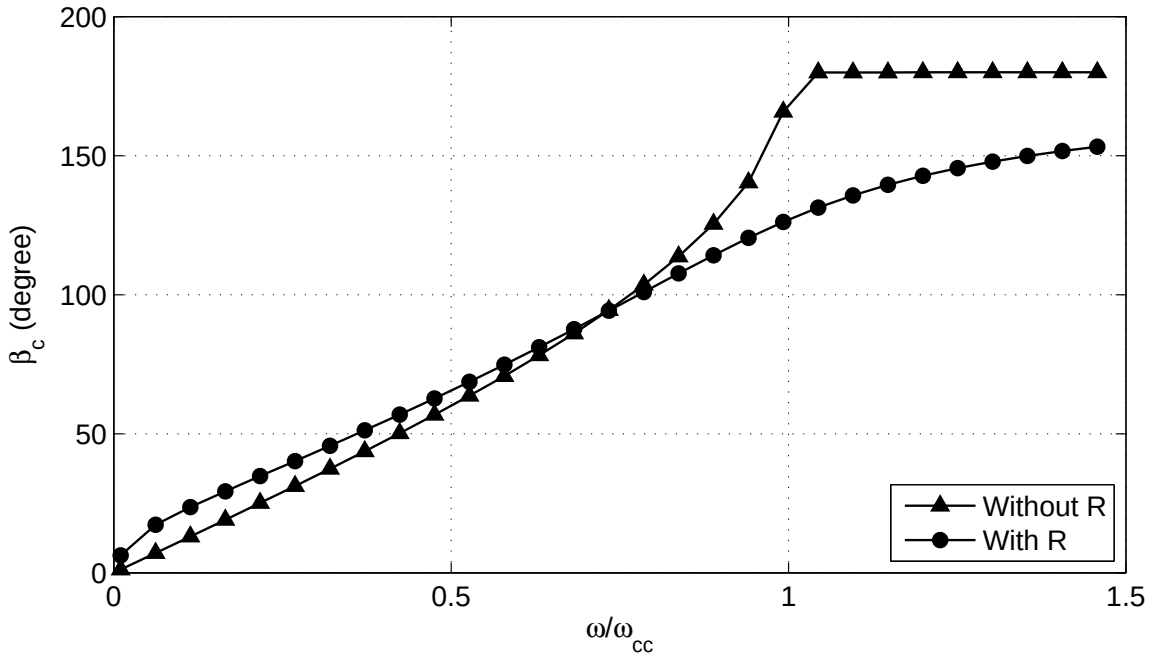


Figure 5.12: Phase characteristics of the collector line at different frequencies (per section). With R (R = 43 Ω) and Without R (R = ∞).

Figure 5.14 shows the simulated S-parameter response of 3-stage and 5-stage DA design, which are utilizing $3 \times 3\mu m \times 40\mu m$ InGaP/GaAs HBT as a unit cell. Simulation results show slight gain increment with number of stages (N) from 3 to 5 at low frequency region. However, no significant gain improvement can be seen at middle and high frequencies. This circuit simulation results agree with the analysis above.

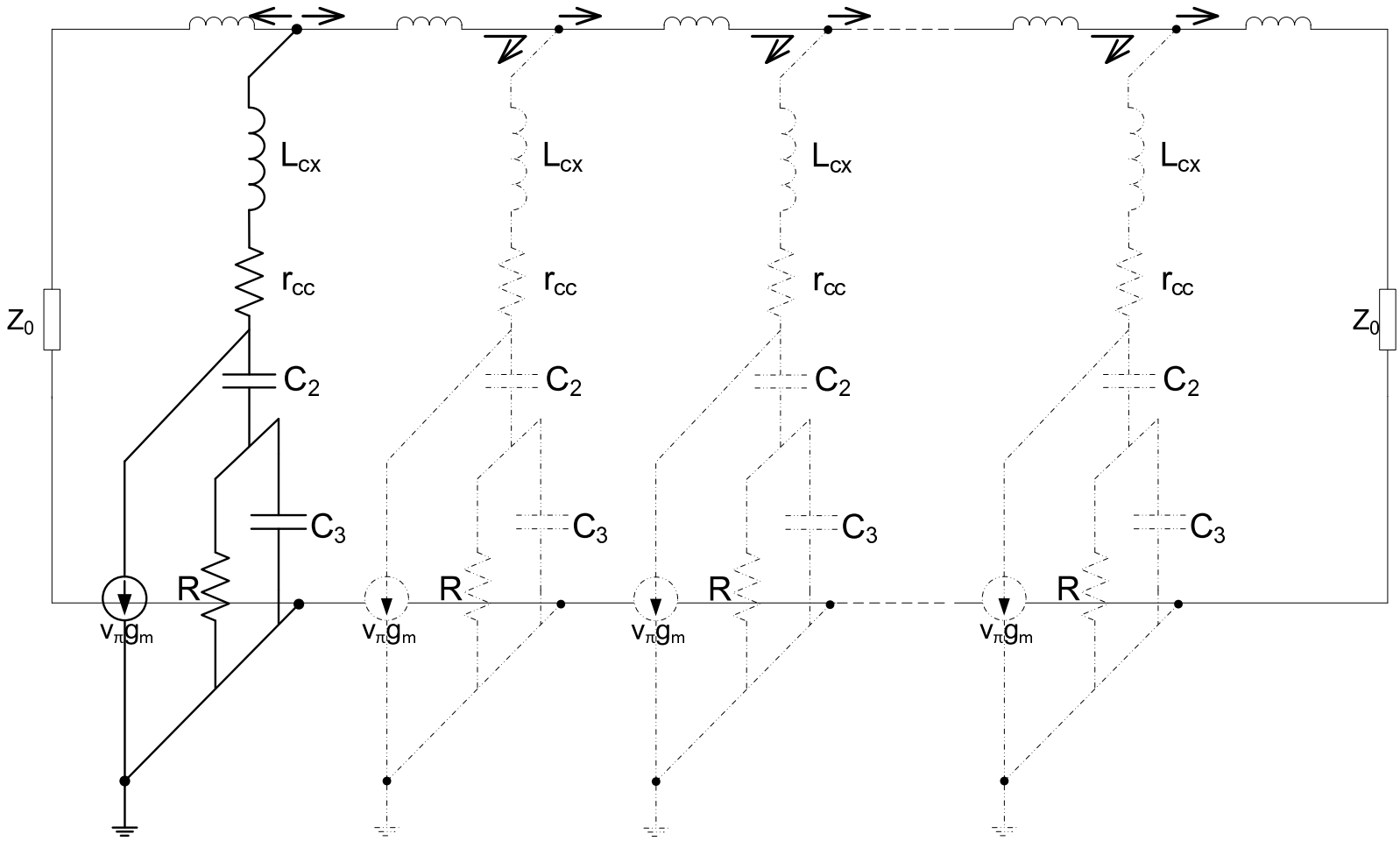


Figure 5.13: The current source at the left most position in the figure is being loaded along the collector transmission line by output impedances of consecutive active devices.

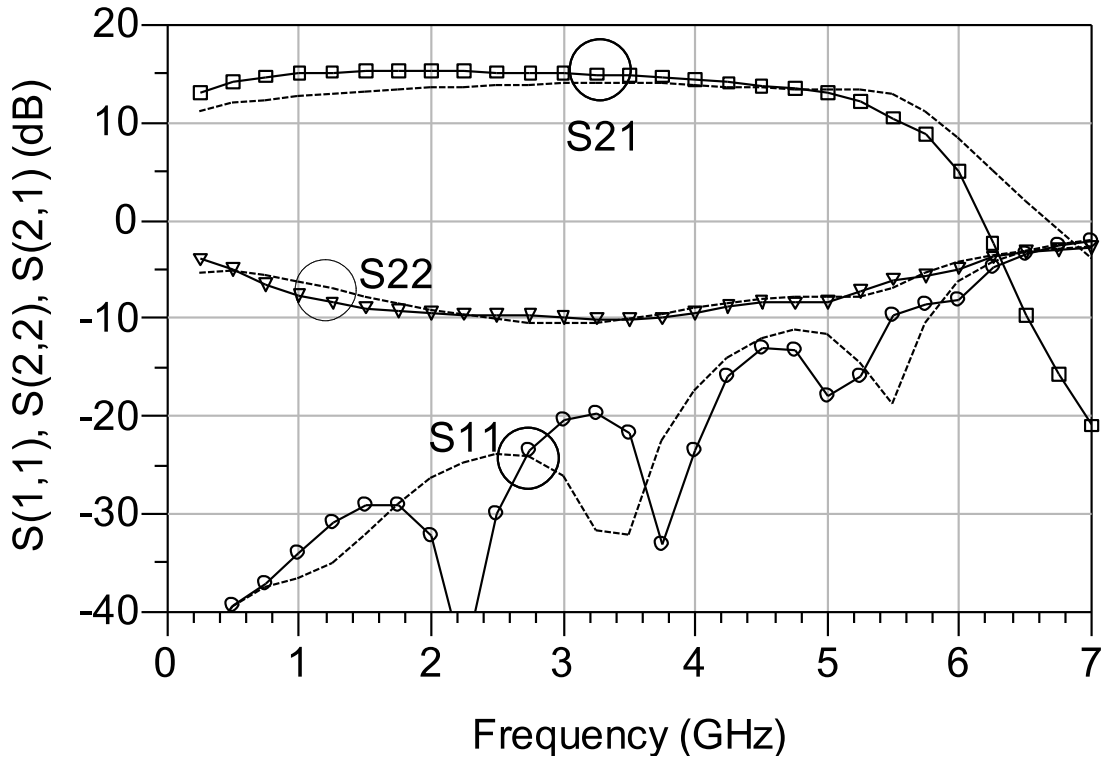


Figure 5.14: Small-signal responses of 3-stages (solid-line) and 5-stages (symbol line) DA design.

Another problem is poor S22 match. Large C_2 allows the signal which is traveling on the collector line to go through resistance R, which has the same order of magnitude as Z_0^c. This makes the load (50Ω) see a transmission line which is periodically loaded with smaller resistance $R = 43\Omega$. As the value of R is smaller than Z_0^c, it determines the S22 response. Meanwhile, S11 is matched well over the pass band.

5.5 Dual Feed DPA Design

Efficiency improvement techniques reported in [120] is adapted in this design.The developed distributed power amplifier (DPA) is expected to be capable of transmitting

output power of 27dBm to 30dBm over 2GHz to 6GHz bandwidth.The average PAEs over the entire bandwidth in state-of-the-art DPA designs are less than 25% [1,11–13, 16]. Hence, the efficiency improvement is one of the primary objectives for this design and The average PAE of 30% or higher is anticipated.

The design is fabricated using WIN Semiconductors Corp's H02U-41 InGaP/GaAs HBT technology. Eight fingers are combined together to form a power active cell of the distributed PA. Each eight-finger cell is designed to generate 300mW of output power. The cells are biased at mid class-AB mode to compromise linearity and efficiency. The amplifier is measured at biasing current of 120mA from 4V supply. The design is fabricated with a die area of 1.8mm^2. Figure 5.15 shows the fabricated compact distributed PA. Each finger has emitter area of $3 \times 40\mu$m^2. $C_{bs} = 0.4$pF is added at every base of the fingers and $C_{cs} = 1$pF is added at every collector of active cell.

The idle port of the base line is terminated with short circuit ($Z_b = 1.5\Omega$) and the collector line is terminated with open circuit ($Z_c = \infty$). To maintain the constructive signal combination, the phase different between incidence and reflected signal at the input of final stage is maintained within 5% of higher cutoff frequency. No power match optimization is performed in the design.

Realization of the inductors is through short sections of high impedance lines. However, for high power device with low supply voltage, high collector current is needed through the collector line. Hence, the inductor at the collector line required wider transmission line width to support high current density. The required line width can be calculated using,

$$W_{cmetal} = \frac{P_{out}}{\eta V_{cc} J_{cmetal}} \tag{5.38}$$

where, η, W_{cmetal}, and J_{cmetal} are collector efficiency, metal width and allowed current

density of the contact metal. For wide metal width the inductance per unit length is small. Large inductance requires significant die area. In our design, we choose to lower the artificial transmission line impedance to optimize the length of the line in the given die size. Because of smaller series inductance, cutoff frequency of the collector artificial line is higher than the base; however, the impedance of the line is lower. For thermal stability every transistor in each cells are ballasted at the base.

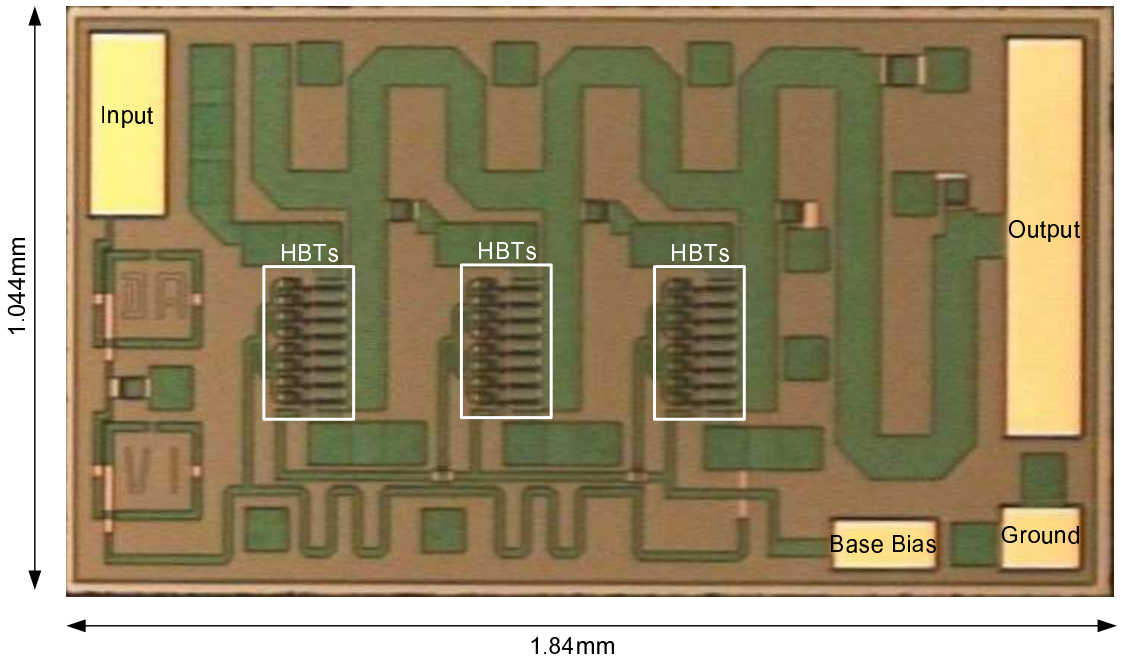


Figure 5.15: Fabricated dual-feed 3-stage InGaP/GaAs HBT DPA.

5.5.1 Performance Measurement

Figure 5.16 shows measured small signal performance of dual-feed 3-stage DPA and Fig. 5.17 shows the overlay plot of measurement versus ADS simulation results . The measured 3dB bandwidth is 12% narrower than the simulated 3dB bandwidth of 4.3GHz. Measured small signal gain is slightly lower than simulations. Except for slight variation, input and output small signal reflection coefficients agree well with

simulation.

Figure 5.16: Measured small signal performance of dual-feed 3-stage DPA.

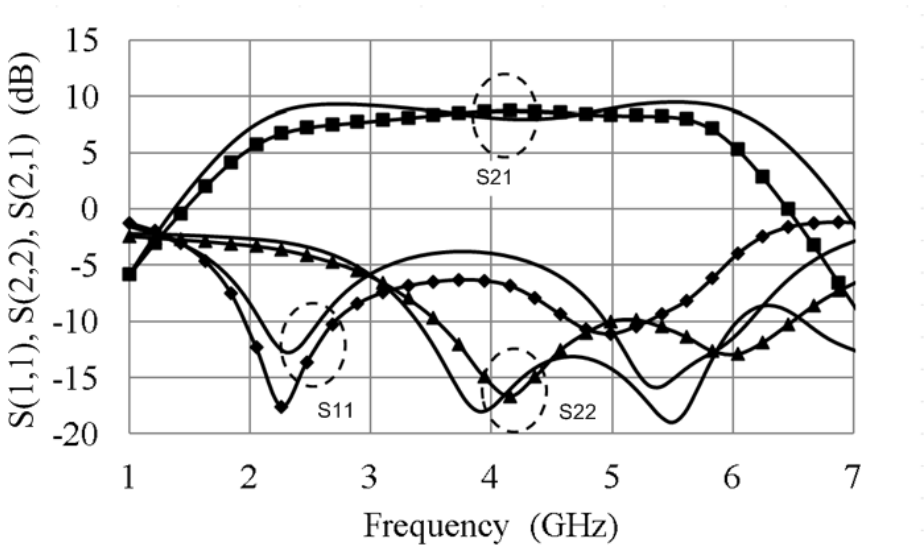


Figure 5.17: Measured (symbol) and simulated (solid) small signal performance.

Large signal performances of the amplifier are characterized using power sweep measurements at different frequencies. Figure 5.18 shows the measured large signal gain performance of dual-feed 3-stage DPA before externally added driver amplifier parameters are de-embedded and Fig. 5.19 the extracted performance of the DPA.

Minimum 1dB compression gain is 5dB at 6GHz and maximum is 9.2dB at 4GHz. Average large signal gain is 7dB across the band width. Figure 5.20 shows the measured output power at different frequencies. The highest output power, at P1dB, is 30.5dBm at 3.5GHz and the lowest P1dB is 26.5dBm at 2.5GHz.

The average output power across the band is 28.5dBm. PAE at P1dB point for mid band frequency is $\geq$35% and best optimum PAE is as high as 43.5% at 3.5GHz. PAE drops at the band edge frequencies. However, average PAE across the band is >30%. Figure 5.21 shows the PAE at different frequencies.

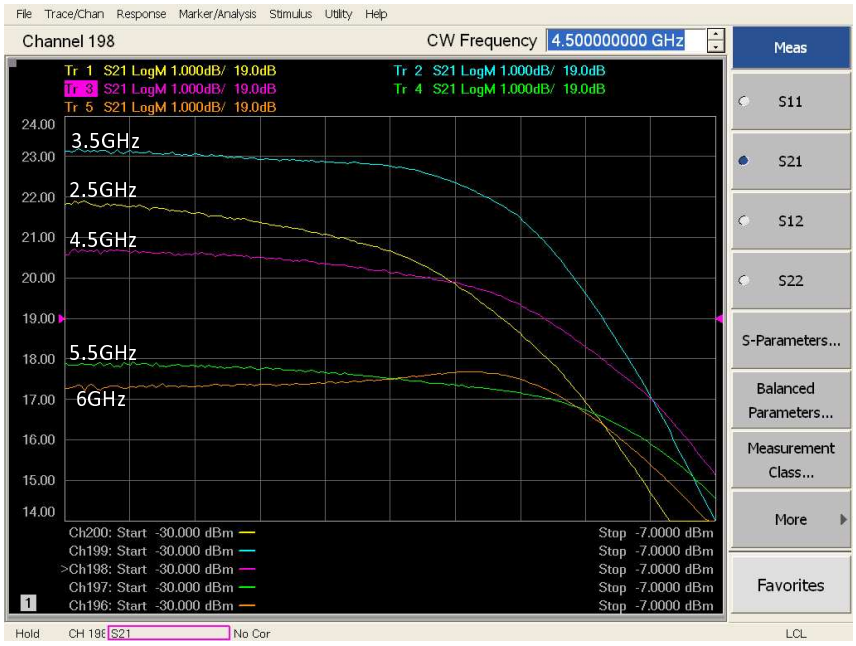


Figure 5.18: Measured large signal performance of dual-feed 3-stage DPA. Note:The response before externally added driver amplifier parameters are de-embedded.

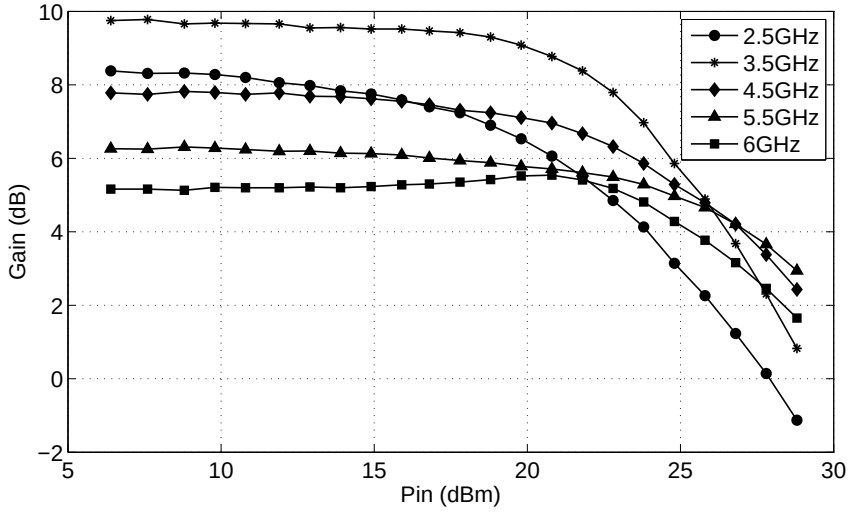


Figure 5.19: Measured large signal gain at 2.5GHz (circle), 3.5GHz (star), 4.5GHz (diamond), 5.5GHz (triangle), and 6GHz (square).

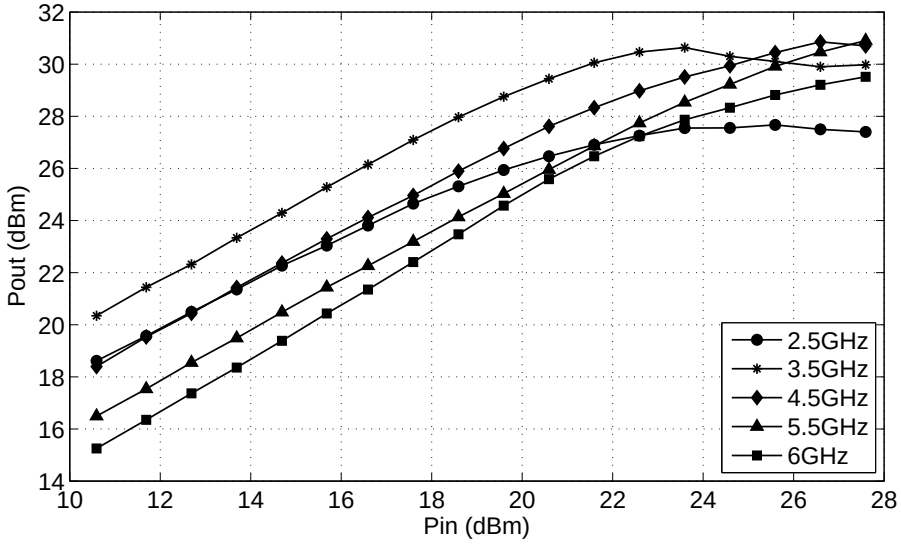


Figure 5.20: Measured output power at 2.5GHz (circle), 3.5GHz (star), 4.5GHz (diamond), 5.5GHz (reverse triangle), and 6GHz (square).

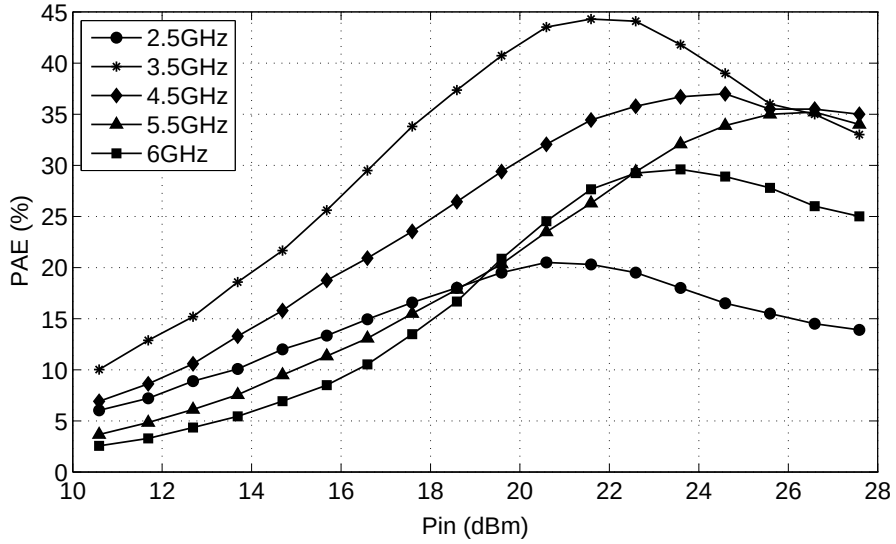


Figure 5.21: Measured PAE at 2.5GHz (circle), 3.5GHz (star), 4.5GHz (diamond), 5.5GHz (triangle), and 6GHz (square).

Table 5.1: Performance Comparison With Previous Wroks

Reference	P1dB (dBm)	PAE (%)	Band (GHz)	Techno-logy	Size (mm^2)	Bias Class	Supply (V)
[121]	33	20	2-8	GaAs	-	-	14
[122]	19.5	22	1-12	SiGe	2	A	5
[123]	15.6	20	3.7-8.8	CMOS	2.8	AB,B	-
[124]	23.6	> 16	1.4-2.7	-	6	A	4.75
[125]	13	19.5	DC-20	CMOS	-	A	1.8
[126]	30	> 20	0.5-6.5	GaN	4	AB	15
This Work	28.5	33	2.5-6	GaAs	1.8	AB	4

As a good terminal match has been traded-off for better PAE and compact size, the disadvantage of this configuration is very poor input and output impedance matching [120] and stability issue. As a result of a very low gain, input power of 25dBm is required to generate 1W output power. This mean, relatively large driver ampli-

fier would be needed in system integration. This huge 25dBm deriver PA's power consumption would compromise the overall PAE performance.

5.6 Analysis and Development of High Gain DA

The need for high gain in PAs is important for higher output and also apparent once we understand the overall efficiency specification of the amplifier. The meaningful efficiency definition for RF and microwave PA applications is PAE. It also accounts the power required to drive at the input, it represents how the gain is going to impact on the efficiency. For a given give bias and an input power level, the power gain is a factor affecting the output power and PAE. Using high gain PA, the input power requirement will be minimized and optimally it is possible to eliminate the driver stage. Smaller input signal demand will help to improve PA's PAE, meanwhile eliminating driver stage will help to improve broader system aspect like total efficiency and cost. In addition, integrating high gain technique with optimum load design will help us to optimize the efficiency of DA. The nominal gain of most DAs [1, 11–14, 16, 35, 37] is about 10dB as shown in Fig. 1.1. A technique has being needed to develop for gain improvement of DPA.

The developed distributed power amplifier (DPA) is expected to be capable of transmitting output power of 27dBm to 30dBm over 700MHz to 6GHz bandwidth. Both small and large signal gain of 20dB or higher are targeted to achieve. The average PAEs over the entire bandwidth in state-of-the-art DPA designs are less than 25% [1, 11–13, 16]. Hence, the efficiency improvement is one of the primary objectives for this design. The average PAE of 30% or higher is anticipated.

III/V compound semiconductor devices such as GaAs HBTs are excellent candidates for power applications and are used in integrated DPAs [11, 13, 14]. HBT with

larger emitter area is required resulting in lower Z_{out}. This in turn results in higher attenuation in the collector line which diminishes the power combining feature of the DA. To lower the Miller's capacitance at the input, improve bandwidth performance and increase output impedance, cascade configuration is preferred and used in some DA designs [10, 14, 18, 32]. Those works emphasize on design of collector line sections with characteristic impedance forming optimum load for each cascade cell. For further improvement, [11] combined inductive peaking techniques to the design. Relatively flat gain of 8.9dB [10] and 11dB [11] are achieved. However, neither work analyzes attenuation encountered at the input and output lines.

Usually, high gain is preferred in most of amplifier applications. In DA technique, the gain achievable is not limited by the gain bandwidth product of a single device. However the attenuation effect of the active cell's components often limits the gain of DA and they are the most dominant one. Generally, lower gain of less than 10dB, is expected for multi-octave bandwidth amplifier.

This motivated us to develop a high gain DA, which will also improve output power and PAE before employing power optimization techniques, for DPA application. As discussed above, attenuations are the main factors which control the gain of DA. Hence, the analysis is mainly focus to lower the attenuation and optimize the power deliver to the load.

5.6.1 Output Impedance Analysis

Small-signal equivalent circuit for output impedance of HBT, including all feedback and termination effects, is presented section 4.5.2. The output impedance of the HBT

at low frequency can be expressed as

$$\mathrm{Re}\, Z_2 = R_2 \approx \frac{C_{\pi 1}^{'}}{C_\mu} \frac{g_{m1}}{\left(g_{\pi 1}^{'} + g_{m1}\right)^2} + \frac{1}{\left(g_{\pi 1}^{'} + g_{m1}\right)} \tag{5.39}$$

$$\mathrm{Im}\, Z_2 = \frac{1}{j\omega C_2} \approx -j \frac{g_{\pi 1}^{'}}{\omega C_\mu (g_{\pi 1}^{'} + g_{m1})} \tag{5.40}$$

and under high frequency analysis it can be expressed as

$$\mathrm{Re}\, Y_2 = \frac{1}{R_3} \approx g_{\pi 1}^{'} \left(\frac{C_\mu}{C_T}\right)^2 + \frac{g_{m1} C_\mu}{C_T} \tag{5.41}$$

$$\mathrm{Im}\, Y_2 = j\omega C_3 \approx j\omega \frac{C_\mu C_{\pi 1}}{C_T} \tag{5.42}$$

Where, $C_{\pi 1}^{'} = 6.5pF$, $C_\mu = 135fF$, $g_{m1} = 1.02S$, $g_{\pi 1}^{'} = 31.25mS$ and $C_T = C_{\pi 1}^{'} + C_\mu$. To reduce the attenuation imposed by this output impedance, it needs to increase the real part which is in parallel with effective output capacitance. Equations 5.39 and (5.41) show the possibilities to modify the real part of the output impedance network without effecting imaginary part by tuning $C_{\pi 1}^{'}$.

Basically, $C_{\pi 1}^{'}$ is not adaptable after fabrication. However, unilateral analysis shows that can be adapted using external component. When we determine the equivalent output impedance Z_2 in unilateral analysis, inclusive of feedback and termination effects, the base of the HBT is terminated with $Z_0 = 50\Omega$ as shown in Fig. 5.22(a). Since, $Z_{\pi 1}^{'}$ is

$$Z_{\pi 1}^{'} = (Z_0 + r_b) \,\|\, Z_{\pi 1} \tag{5.43}$$

and (5.43) can be expanded as

$$Z_{\pi 1}^{'} \simeq \left(\frac{1}{(Z_0 + r_b)} + \frac{1}{r_{\pi 1}} + j\omega C_{\pi 1}\right)^{-1} \tag{5.44}$$

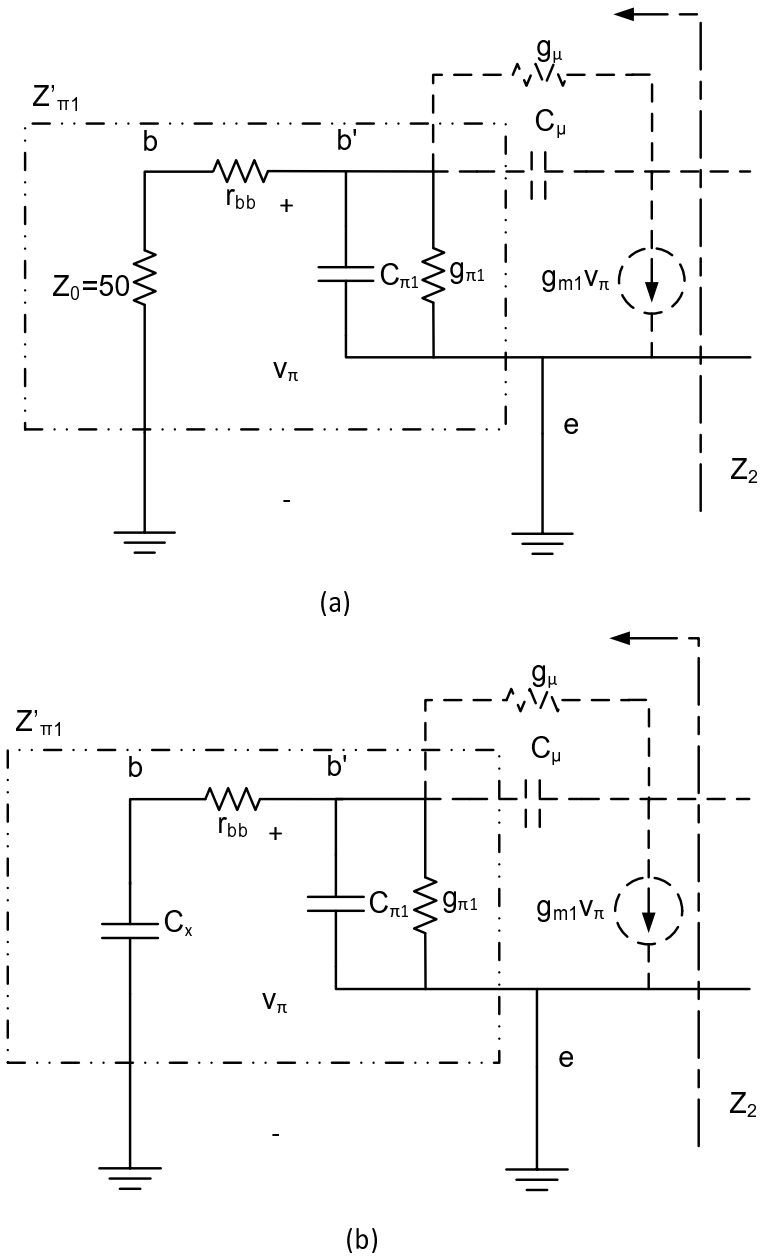


Figure 5.22: Equivalent output impedance network with base is terminated with 50Ω (a) and a capacitor (C_x) (b).

Combination of terminated impedance Z_0 and base series resistance r_b appear in parallel to the input impedance $Z_{\pi 1}$ of the transistor. As Z_0 is purely resistive it

only affects $r_{\pi 1}$ and $C_{\pi 1}$ is unchanged ($C_{\pi 1} = C'_{\pi 1}$). Equation 5.44 shows that instead of terminating with Z_0 at the base, terminating with a capacitor C_x as shown in Fig. 5.22(b) increases $C_{\pi 1}$. Then (5.44) could be modified as

$$Z'_{\pi 1} \simeq \left(\frac{1}{r_{\pi 1}} + j\omega \left(C_{\pi 1} + C_x \right) \right)^{-1} \tag{5.45}$$

This suggests that terminating the base of the transistor with a capacitor helps to increase the real part of the output impedance network. With the capacitance C_x, (5.39) and (5.41) become

$$\mathrm{Re}\, Y_2 = \frac{1}{R_3} \approx g_{\pi 1} \left(\frac{C_\mu}{C_{\pi 1} + C_\mu + C_x} \right)^2 + \frac{g_{m1} C_\mu}{C_{\pi 1} + C_\mu + C_x} \tag{5.46}$$

$$\mathrm{Re}\, Z_2 = R_2 \approx \frac{C_{\pi 1} + C_x}{C_\mu} \frac{g_{m1}}{\left(g_{\pi 1} + g_{m1} \right)^2} + \frac{1}{\left(g_{\pi 1} + g_{m1} \right)} \tag{5.47}$$

This analysis allows adapting the output impedance especially output resistance of a HBT to higher impedance value using external component.

5.6.2 Output Impedance Adaptation using a Cascode Cell

Implementing the concept on a single transistor cell, where the input signal is injected through the base, will be difficult. The most suitable configuration is cascode, where, the input is isolated from output stage and at the same time C_x is employable at the base of the output stage transistor. Figure 5.23 shows a cascode configuration using two HBT cells. In general,the usage of C_x is very common as bypass capacitor, representing a short circuit at the frequencies of interest in common-base configuration. Other than short circuit requirement,no other specific requirement has been imposed on C_x value. However,the analysis shows that instead of terminating the base of CB stage with short circuit, it is better terminated with an impedance value which al-

lows us to optimize output impedance. In other words, selecting C_x have significant influence on the gain and PAE performances. The analysis leads us to deeper understanding of impedance and gain control. These two parameters have not being link to C_x before. Hence,the technique is presented for selecting C_x to optimize the transistor's output impedance to get higher gain in a systematic way.

5.6.3 Stability Analysis

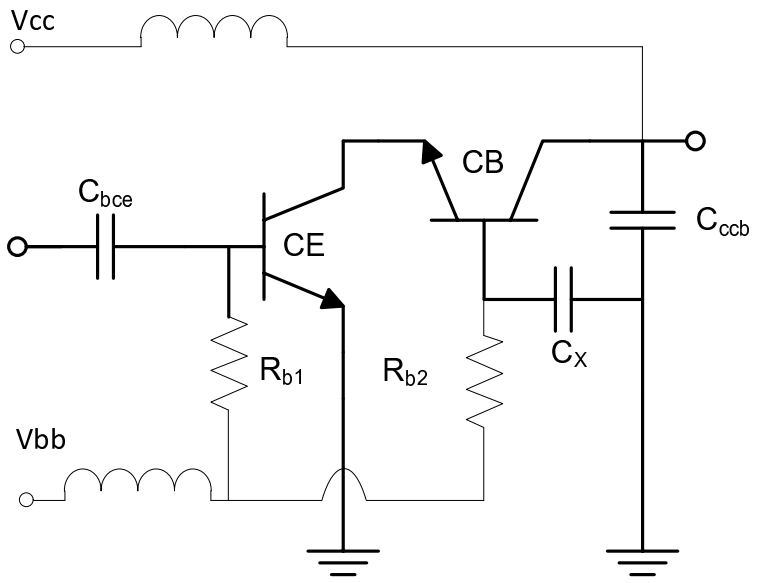


Figure 5.23: Schematic of HBT cascode configuration.

Figure 5.24 shows the S-parameter responses of the cascode cell at different C_x values. S22 which reflect the effective output impedance shifts from low to high impedance region with increasing C_x. The kink resonance frequency where output impedance changes from series capacitance-resistance to shunt capacitance-resistance behavior, is also shifted to lower frequency region and occurs outside the band of interest.The S21 of the cascode cell is also increasing and effective input capacitance is decreasing

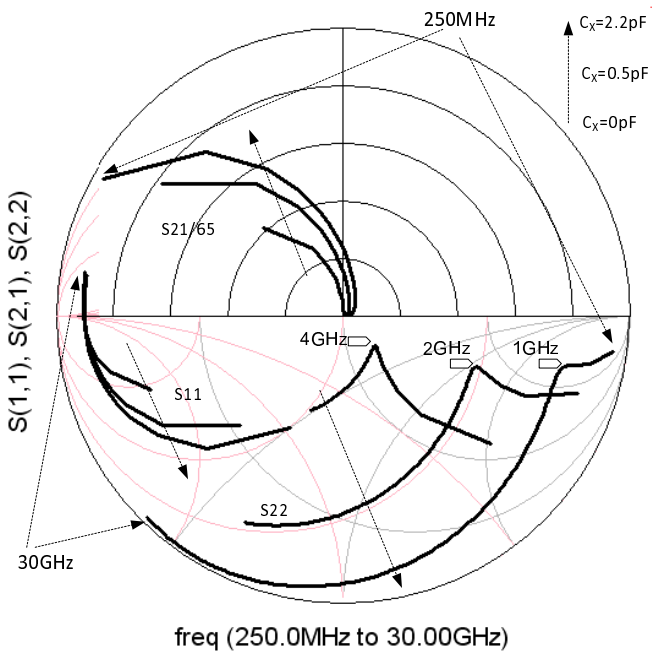


Figure 5.24: Variation of S-parameter responses of the cascode cell at different C_x values 0pF, 0.5pF and 2.2pF, terminated at the base of CB stage.

with increasing C_x. The output impedance is effectively a capacitor and a resistor in shunt. With $C_x = 2.2pF$, the effective output resistance (R) is over 3 times higher than output characteristic impedance of $Z_0^c = 50\Omega$.

The increase in C_x is bounded by the stability properties of the cascode configuration. Stability performance of the cascode structure are simulated for different C_x values in ADS. Figure 5.25 and Fig. 5.26 and show simulated load and source stability circles over 1GHz to 30GHz frequencies at $C_x = 2.0pF$. The circles define the boundaries between stable and potentially unstable regions of Γ_L and Γ_S. Determining which side of the boundary represents the stable region requires checking magnitude of $S11$ for load stability circles and $S22$ for source stability circles.

Since, both $S11 < 1$ and $S22 < 1$,stability define that, the device is unconditionally stable when the stability circles lies completely outside. Hence, the simulation results show that, the cascode structure is unconditionally stable over the frequency range

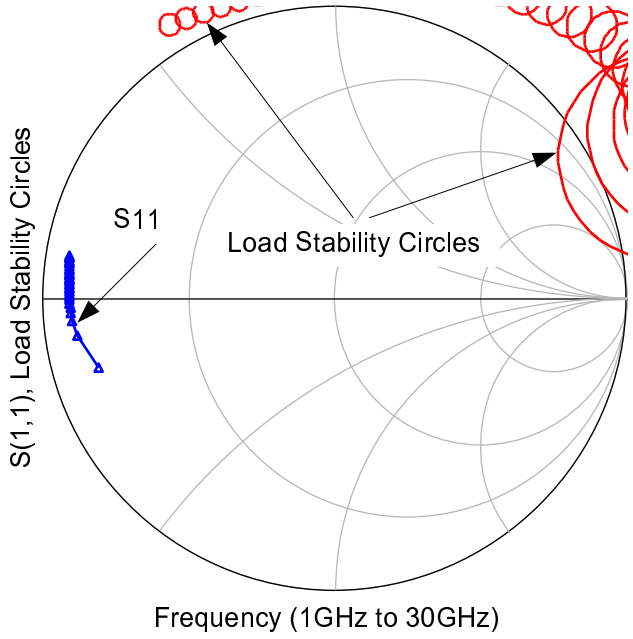


Figure 5.25: Load stability circles from 1GHz to 30GHz with $C_x = 2.0pF$.

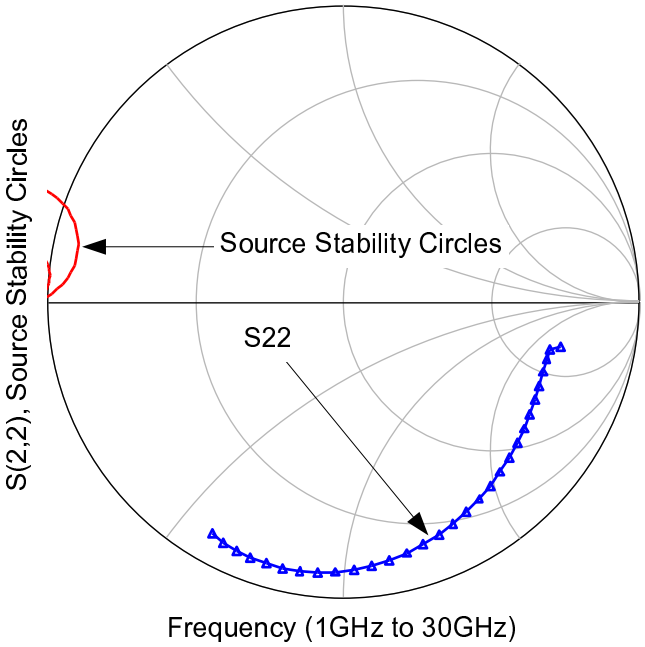


Figure 5.26: Source stability circles from 1GHz to 30GHz with $C_x = 2.0pF$.

except at 1GHz, at which the structure stables conditionally with majority of the Smith chart lies inside stable region.

Figure 5.27 and Fig. 5.28 show the load and sources stability performances of the cascode structure with $C_x = 7.0pF$. Load stability circles shows that the cascode structure is conditionally stable over the frequency range with center and majority area of the Smith chart lies inside the stable region. However, S22 of the cascode structure is greater than 1 over 15GHz to 22GHz band. As source stability circles at those frequencies lie outside the Smith chart totally and hence $S22 > 1$ means that center of the Smith chart become unstable region. Any passive source impedance can make output reflection coefficient $\Gamma \geq 1$ and the structure become un-stable.

Un-stable frequency band lies within the range of second and third harmonic region of the operating frequencies. For power amplifier, harmonic frequencies are as important as fundamental frequencies and the cascode structure must be stable at harmonic frequencies too. Hence, C_x value should be chosen which satisfy output impedance requirement and simultaneously satisfy stability requirement of the systems, in this case including harmonic frequencies.

5.6.4 DA Designs Using Output Impedance Optimized Cascode Cell

The base of CB stage is terminated with a capacitor $C_x = 2.2pF$. Effective component values of the optimized cascode cell are: $C_{\pi eff} = 16.3pF$, $r_{\pi eff} = 55\Omega$, $C_{oeff} = 200fF$ and $R_{oeff} = 265\Omega$ respectively. $C_{\pi eff}$ is still too large and a series capacitance C_{bs} is added at each input of cascode cell to minimize $C_{\pi eff}$.

Meanwhile, output capacitance C_{oeff} is relatively small. As constructive wave combination is preferred on the output transmission line, phase synchronization with

base line must be maintained.

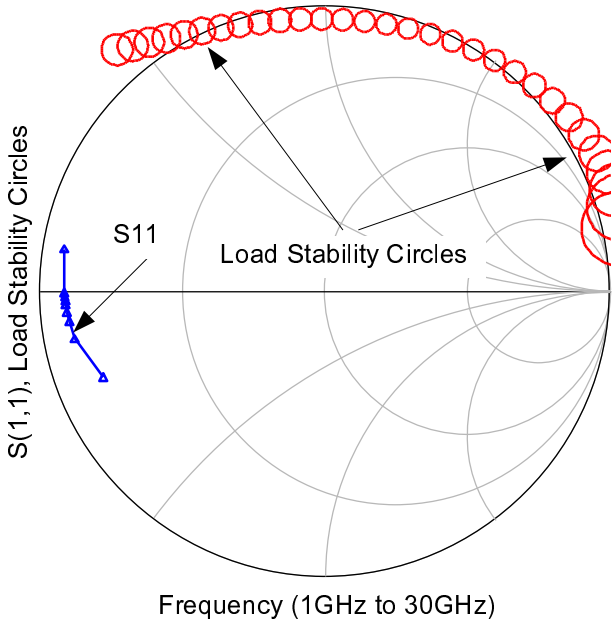


Figure 5.27: Load stability circles from 1GHz to 30GHz with $C_x = 7.0pF$.

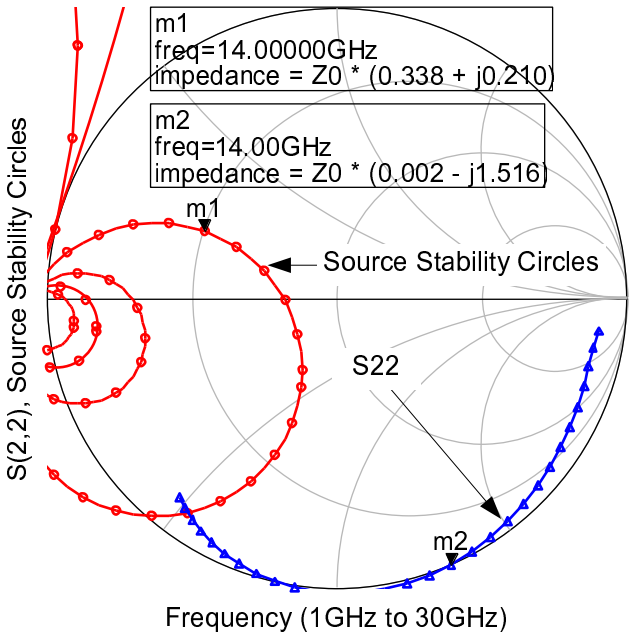


Figure 5.28: Source stability circles from 1GHz to 30GHz with $C_x = 7.0pF$.

A shunt capacitor C_{cs} is added at the output of every cascode cell to match C_{oeff} with $C_{\pi eff}$. Input series capacitance C_{bs} and output shunt capacitance C_{cs} are selected according to the band width requirement. Using (5.10), $C_{bs} = 1pF$ and $C_{cs} = 0.8pF$ are selected along with $L_b = L_c = 2.5nH$ to achieve the input and output line cutoff frequencies (f_{cb} and f_{cc}) of 6.366GHz. Different values of $C_{bs} = 0.72pF$ and $C_{cs} = 0.52pF$ are selected along with $L_b = L_c = 1.9nH$ to extend the cutoff frequencies to 8.7GHz.

Characteristic impedances, attenuations and phases profile introduced by each section of input and output transmission lines are computed. Computed Z_0, α and β of the input and output lines are shown in Fig. 5.29, Fig. 5.30 and Fig. 5.31 respectively.The attenuation factor is reduced significantly compare to single stage and is maintained around 1dB over the pass band. Phase factor of input and output line are synchronized perfectly.

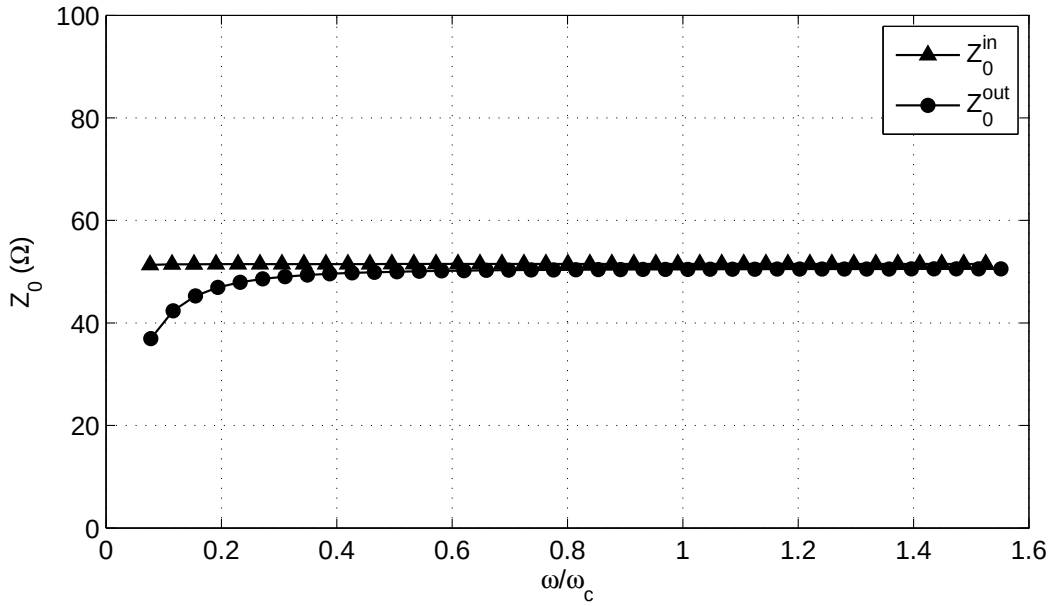


Figure 5.29: Characteristic impedances of the input and output transmission lines which are making use of optimized cascode cell.

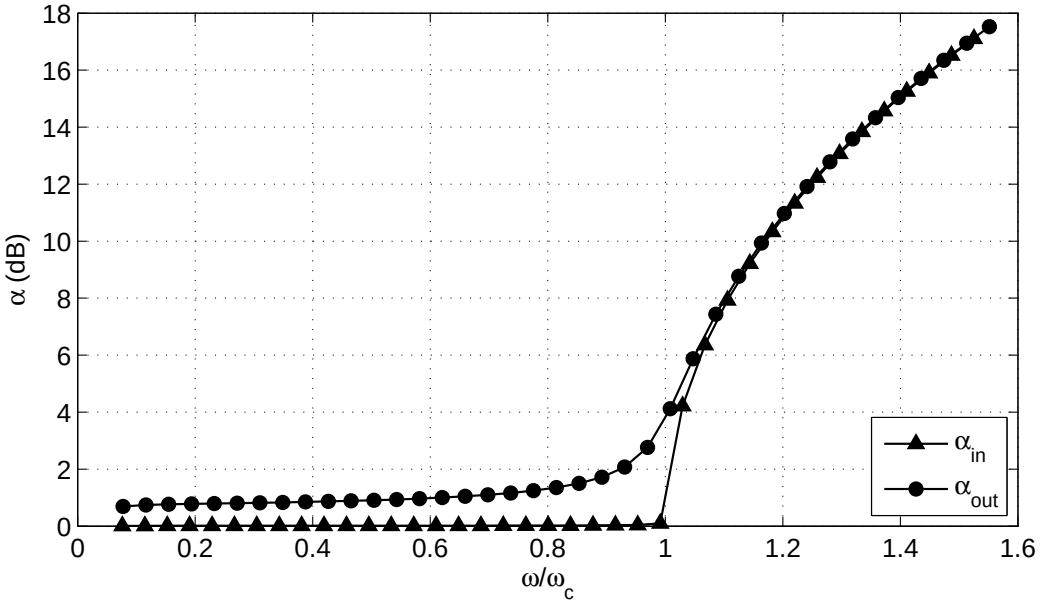


Figure 5.30: Attenuation (per section) of the input and output transmission lines at different frequencies.

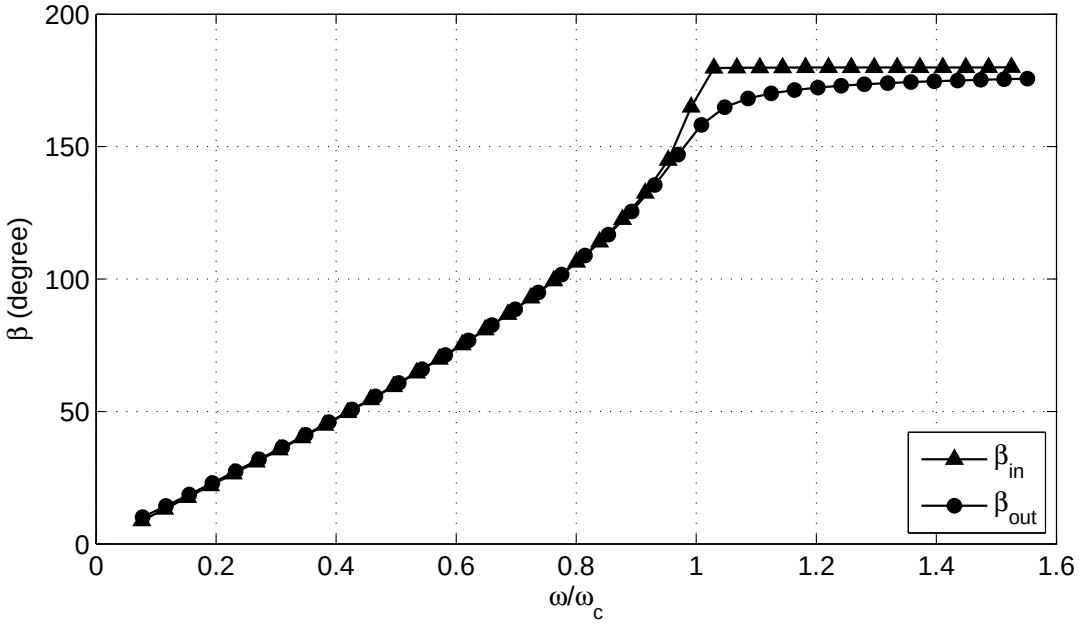


Figure 5.31: Phase variation (per section)of the input and output transmission lines at different frequency.

5.7 Circuit Simulation of High Gain DPA

An uniform distributed amplifier is implemented in Agilent's ADS using the cascode cells.As we discussed in Chapter 1, efficiency improvement techniques such as switching mode amplification and harmonic tuning are not applicable to DA. Hence, the cascode cells are biased in class-A. The bias setting is V_{cc}=6V and I_{cq}=75mA. Maximum output current of each cascode cell is 150mA. All ports are terminated with $Z_0 = 50\Omega$. Figure 5.32 shows the simulated S-parameters responses of uniformly distribute 5-stages DA with -3dB bandwidth of 6GHz (design A). Setting C_{bs}=0.72pF and C_{cs}=0.52pF along with $L_b = L_c$=1.9nH increases the higher -3dB cutoff frequencies to $f_{cb} = f_{cc}$=8.7GHz and the bandwidth is extended to 8.3GHz, (design B). Further lowering C_{bs}=0.62pF, C_{cs}=0.42pF and $L_b = L_c$=1.6nH increases the bandwidth to 10GHz, (design C).

5.7.1 Small Signal Performances

Simulated S-parameters response of 8.3GHz and 10GHz bandwidth designs are presented in Fig. 5.33 and Fig. 5.34 respectively. The small-signal gain of design A is around 23.2dB over the bandwidth. Meanwhile, design B and C still achieves 20dB and 17dB gain respectively. At the same time, the input and output impedance are well matched with better than 10dB return loss over 85% of the bandwidth.

The lower -3dB cutoff frequency of these designs is 400MHz. So, they have ultra-wide bandwidth of 1.5 decades, 2 decades and 2.5 decades respectively.This huge gain improvement comes from minimization of attenuation on the collector line in term of externally controlled output impedance and utilization of cascode configuration.

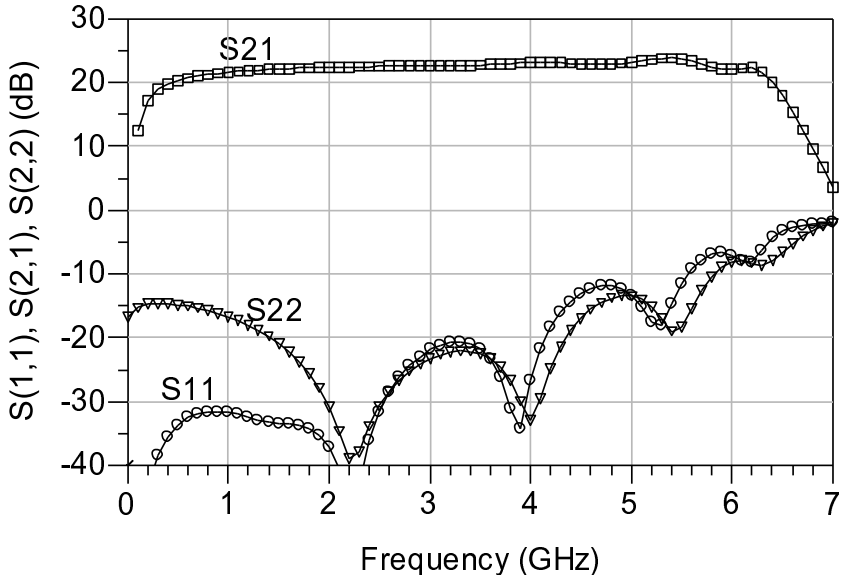


Figure 5.32: Simulated S-parameter response of 6GHz bandwidth 5-stage cascode cell DA.

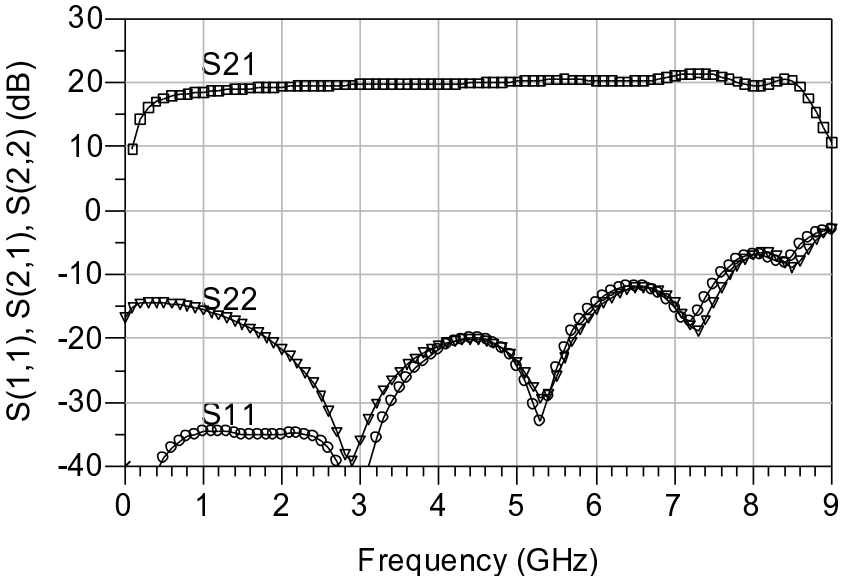


Figure 5.33: Simulated S-parameter response of 8.3GHz bandwidth 5-stage cascode cell DA.

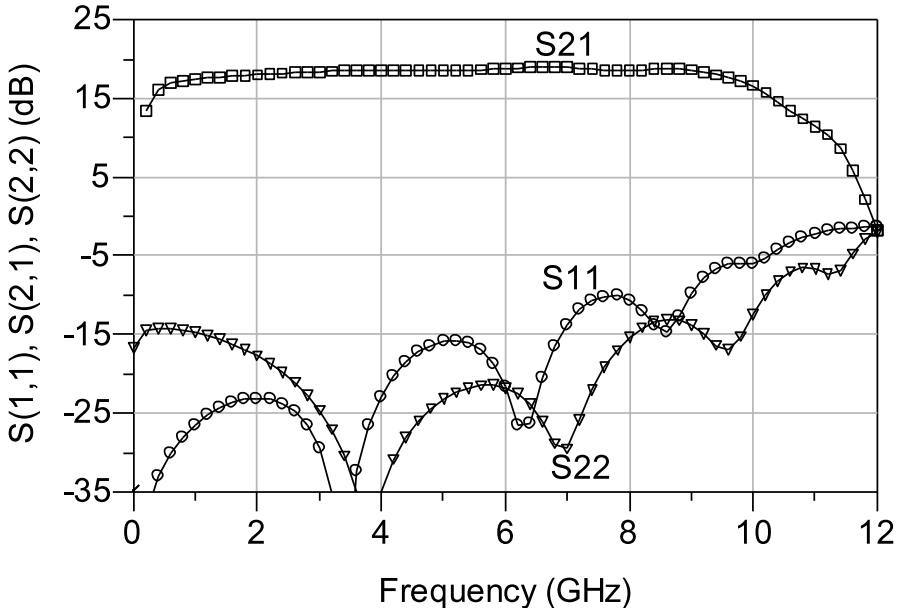


Figure 5.34: Simulated S-parameter response of 10GHz bandwidth 5-stage cascode cell DA.

5.7.2 Large Signal Performances

Power performances such as output power, power gain and PAE of the high gain DPA is evaluated using large signal harmonic balance (HB) simulation in ADS at various frequencies. The thermal model developed in Chapter 3 is integrated with large signal model provided by the foundry services. Single tone is used in the simulation and signal power is swept from -20dBm to +18dBm. The performance of design A, B and C are presented in Fig. 5.35, Fig. 5.36 and Fig. 5.37. Output power at 1dB compression point for design-A is 27.3dBm, B and C are 27.3dBm and 27.6dBm respectively.

The large signal power gain of these design agree with small signal gain over the bandwidth with large signal gain of 22dB, 21dB and 19dB respectively at center frequencies of 3 to 5GHz.Maximum PAE is as high as 33%, 34.2% and 33% for designs - A, B and C respectively under class-A operation.

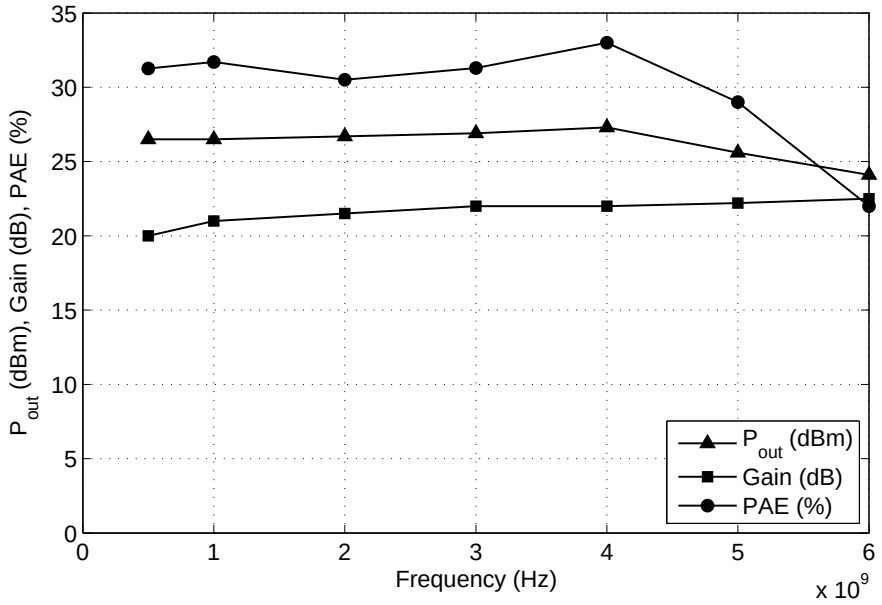


Figure 5.35: Simulated output power , large-signal gain and PAE performances of 5-stages cascode cell DA at P_{1dB}. Design-A.

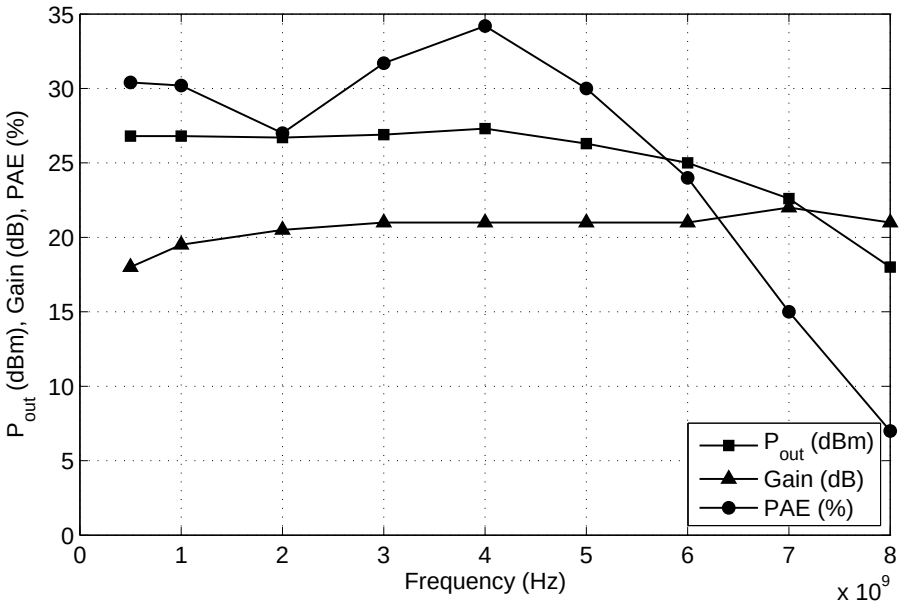


Figure 5.36: Simulated output power , large-signal gain and PAE performances of 5-stages cascode cell DA at P_{1dB}. Design-B.

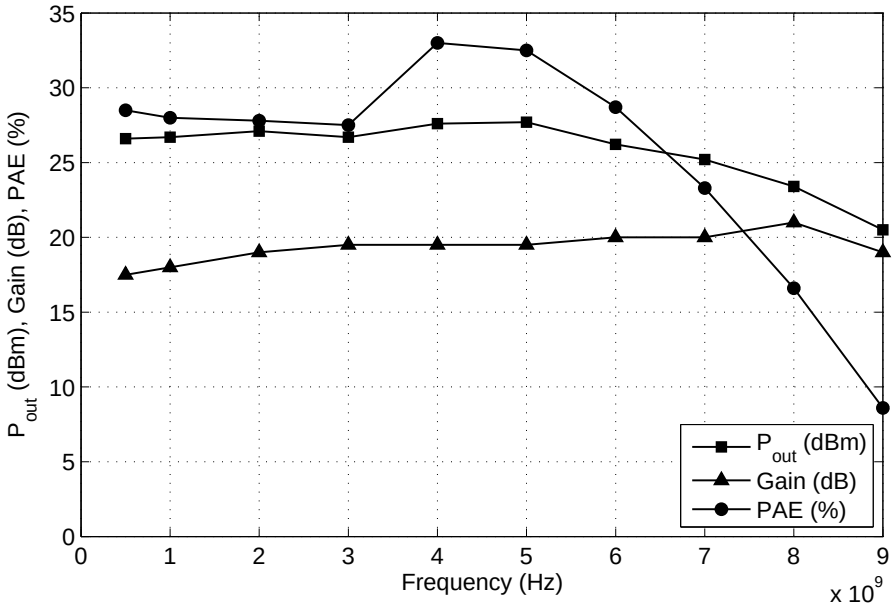


Figure 5.37: Simulated output power , large-signal gain and PAE performances of 5-stages cascode cell DA at P_{1dB}. Design-C.

5.8 Conclusion

In this chapter, the design parameters of artificial transmission lines used in DPA are analyzed and derived from the perspective of physical implementation requirements imposed by the active device technology and applications. Associated close form formulae are derived to determine amplitude and phase attenuation characteristics of input and output line. Highly efficient dual feed distributed amplifier is designed and fabricated. Significant efficiency improvement is achieved at a cost of terminal match and stability. Huge attenuation is observed on the collector line because of low output impedance of HBTs. Output impedance analysis from Chapter 4 is extended to reconfigure the HBT's output impedance using external components and cascode cell configuration. Then output impedance of cascode cell is systematically configured

to higher impedance region to minimize the attenuation along collector line. This low attenuation at the output line together with phase synchronization and proper biasing gives huge improvement to the DPA gain. The small-signal performances (e.g., reflection and transmission coefficients) and large- signal power performances (e.g., gain, output power and PAE) of high-gain decade bandwidth DPA designs are discussed.

Chapter 6

Conclusion and Recommendation for Future Research

6.1 Conclusion

This thesis discusses the analysis and development of ultra-broadband distributed power amplifier. Thermal and small signal model issues associated with GaAs HBT based PA are also discussed and analyzed. New models are developed and design techniques for DPA are proposed.

Firstly, the reviews on the existing bandwidth enhancement techniques are conducted and their advantage and disadvantages are examined. Because of their inherently large bandwidth, flat gain, good noise figure, and good input/output match over muliti-octaves or decades bandwidth properties, distributed amplification technique is investigated in detail. GaAs HBT technology is chosen over its contemporary device technologies and associated thermal issues are addressed. The shortfalls of some small-signal equivalent circuit models for high frequency and high power applications is pointed out in the review. The state-of-the-art DPA techniques are also

summarized.

As the electro-thermal interaction in PA is an important issue steady state and dynamic thermal behaviors of GaAs HBT are analyzed in detail in the second part. Poor thermal conductivity makes GaAs HBT more vulnerable to self-heating effect when dissipated power in the transistor is high. As the modern high speed communication systems use highly fluctuated OFDM and QAM signal for system efficiency, dynamic self-heating effect become an important issue for PA. Standard thermal model which is being integrated with most of the large-signal electro-thermal models have low thermal cutoff frequency and is unable to account for this dynamic self-heating effect. A numerical technique is developed to predict highly fluctuating dynamic junction temperature of a power HBT. Thermal cutoff frequency of up to 30MHz, the pulse width as short as 10ns and with power level up to 10dB higher than reference power level of 40mW are considered. The numerical computation is conducted in frequency domain for better spectral analysis. This numerical analysis is validated using measurement results and it shows that dynamic junction temperature of GaAs HBT can be predicted accurately using the developed technique, especially when the length of HBT finger is relatively longer than its width. Close form formulae are also provided for various signal types. The technique is applicable for a wide range of power levels, frequencies and material properties. For transient thermal simulation, a compact multi-section equivalent thermal network model is also proposed.

Thirdly, this thesis introduces a new compact and complete unilateral model. As the unilateral models are widely used in DA design analysis, it is very important to use a relevant circuit model. Simplified unilateral model has very limited accuracy for high frequency and high power applications. Meanwhile Miller's approximated unilateral model is invalid for output impedance analysis, which is an important parameter to determine PA performance. As these two standard unilateral models are

not accurate enough for the application, a new compact unilateral model is introduced. Hybrid-pi model based small signal bilateral parameters are extracted from measured S-parameters. Upon successful development of the bilateral model, the analysis is extended to develop a unilateral model for InGaP/GaAs HBT. No pre-assumptions are made for this analysis and all intrinsic and extrinsic elements of the HBT are accounted in the formulation. A complete and explicit analysis is provided. The model is validated with measurement results and bilateral results at various biasing conditions. The model can predict input reflection, forward transmission and output reflection coefficient accurately over 250MHz to 30GHz frequency range.

Finally, close form artificial transmission line formulae which take into account all intrinsic and extrinsic elements of HBT and and external components needed for real implementation are derived. These formulae are then used to develop high efficiency DPA and high gain DPA designs. Dual-feed technique is applied for highly efficient DPA design. The design is fabricated using WIN Semiconductors Corp's H02U-41 InGaP/GaAs HBT technology. In this design fingers of transistor are stabilized using base ballasting. Average output power of 28.5dBm is achieved over 2GHz to 6GHz from 4V supply and average PAE is higher than 30%. Optimum PAE is as high as 43.5% at 3.5GHz. However, the low gain feature of the design requires large driver unit and compromises the main PA's good PAE performance. Hence, an analysis is carried out to develop high gain DA. As collector line attenuation causes severe power loss along the line, it is carefully examined. Since, the relatively low output impedance of the HBT is a main reason for high attenuation; output impedance reconfiguration technique using external components is developed. The technique is applied to adjust the output impedances of cascode cells and minimize the attenuation along the collector line. Agilent's ADS is used to simulate the DPA designs. Simulation results show higher than 20dB gain is achievable over 500MHz to 6GHz bandwidth and

17dB gain over 500MHz to 10GHz bandwidth. Input and output ports are also well matched across the band. Significant PAE improvement is observed. The simulation results show that high-gain DPA is a promising option for PAE improvement while preserving its original appealing features such as good input/output matching, flat gain and stability.

6.2 Recommendation for Future Research

Below are the list of works presented in this thesis which could be extended in the future research for the performance and model improvement.

- In Chapter 3, multi-section thermal equivalent circuit model is developed using Cauer canonical technique from numerically determined thermal impedance for InGaP/GaAs HBT. Since, the impedance values are calculated for a specific device structure and material, the thermal equivalent circuit model is valid for a specific device size. It is not scalable, nor valid for other structure or material. Hence, an alternative way is directly implementing numerical equation using nonlinear equation based model. This will allow the designer to have access into all variables such as structure and material properties which govern the dynamic thermal frequency response of a transistor.

- It is also interesting to extend the numerical thermal analysis method to explore mutual heating effect which generally occurs in multi-fingers structure. This will provide thermal matrix between fingers without conducting tedious measurements.

- Extend the unilateral model to include scalable parameters for different HBT size and technologies.

- It is also interesting to integrate the high gain technique with other optimization concept such as optimum power load concept to maximize the output power and PAE while maintaining high gain properties.

Appendix A

This appendix presents analysis of artificial transmission line networks including parasitic and series capacitor for real implementation.

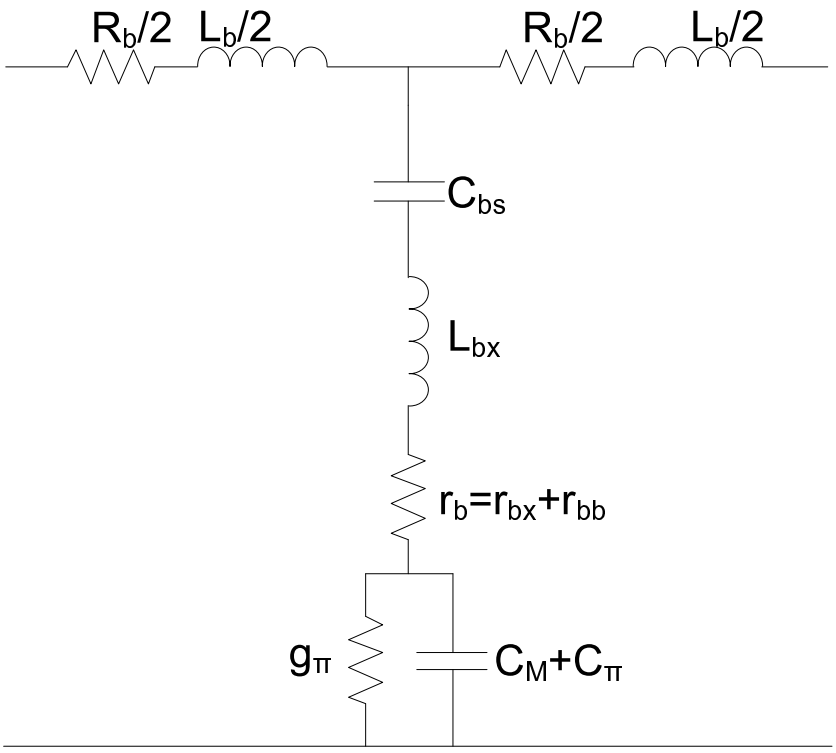


Figure A.1: Equivalent network section of base

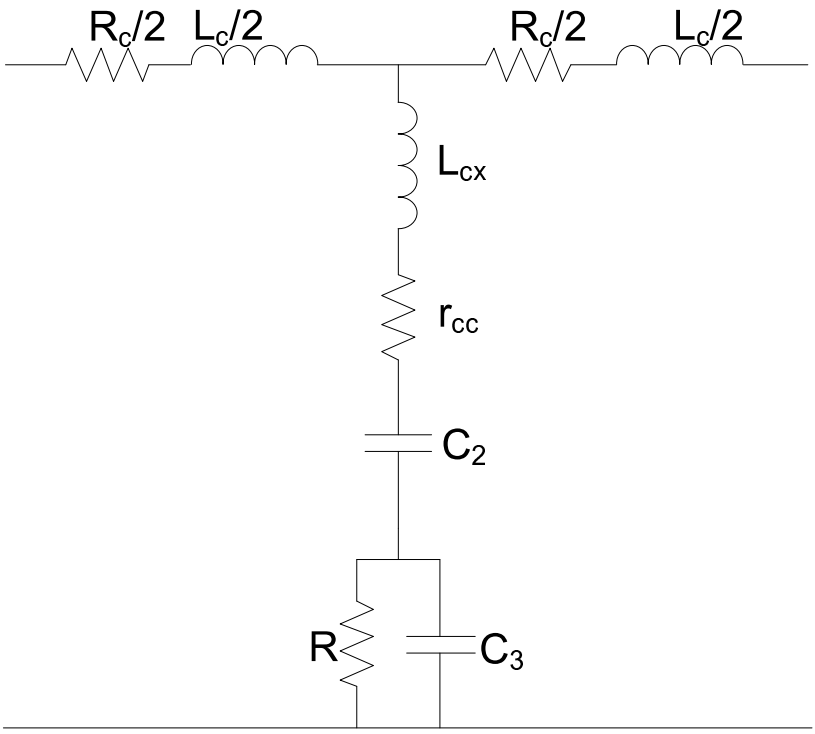


Figure A.2: Equivalent network section of Collector

I. For Base Line

Figure A.1 is the reference figure for this analysis.

$$Z_b = R_b + j\omega L_b \tag{A.1}$$

$$Y_b = \frac{g_\pi + j\omega C_\pi}{1 + r_b g_\pi - \omega^2 L_{bx} C_\pi + j\omega \left(L_{bx} g_\pi + r_b C_\pi\right)}, \tag{A.2}$$

$$Z_T^b = \sqrt{\frac{R_b + j\omega L_b}{g_\pi + j\omega C_\pi}\left[\left(\frac{\mathrm{R}_b g_\pi}{4} - \frac{\omega^2}{\omega_{cb}^2} + \frac{j\omega}{\omega_{cb}^2}\left(\frac{g_\pi}{C_\pi} + \frac{R_b}{L_b}\right)\right) + \left(1 + r_b g_\pi - \frac{\omega^2}{\omega_{sb}^2} + \frac{j\omega}{\omega_{sb}^2}\left(\frac{g_\pi}{C_\pi} + \frac{r_b}{L_{bx}}\right)\right)\right]}. \tag{A.3}$$

$$Z_\pi^b = \sqrt{\frac{\dfrac{R_b + j\omega L_b}{g_\pi + j\omega C_\pi}\left[\left(1 + r_b g_\pi - \dfrac{\omega^2}{\omega_{sb}^2} + \dfrac{j\omega}{\omega_{sb}^2}\left(\dfrac{g_\pi}{C_\pi} + \dfrac{r_b}{L_{bx}}\right)\right)\right]^2}{\left[\left(\dfrac{\mathrm{R}_b g_\pi}{4} - \dfrac{\omega^2}{\omega_{cb}^2} + \dfrac{j\omega}{\omega_{cb}^2}\left(\dfrac{g_\pi}{C_\pi} + \dfrac{R_b}{L_b}\right)\right) + \left(1 + r_b g_\pi - \dfrac{\omega^2}{\omega_{sb}^2} + \dfrac{j\omega}{\omega_{sb}^2}\left(\dfrac{g_\pi}{C_\pi} + \dfrac{r_b}{L_{bx}}\right)\right)\right]}}. \tag{A.4}$$

$$\omega_{cb} = \frac{2}{\sqrt{L_b C_\pi}},\ \omega_{sb} = \frac{1}{\sqrt{L_{bx} C_\pi}}. \tag{A.5}$$

By setting A_b and B_b as follow

$$A_b = \left(\frac{\mathrm{R}_b g_\pi}{4} - \frac{\omega^2}{\omega_{cb}^2} + \frac{j\omega}{\omega_{cb}^2}\left(\frac{g_\pi}{C_\pi} + \frac{R_b}{L_b}\right)\right), \tag{A.6a}$$

$$B_b = \left(1 + r_b g_\pi - \frac{\omega^2}{\omega_{csb}^2} + \frac{j\omega}{\omega_{csb}^2}\left(\frac{g_\pi}{C_\pi} + \frac{r_b}{L_{bx}}\right)\right) \tag{A.6b}$$

The characteristic impedance of the base line can be expressed as,

$$Z_0^b = \sqrt{B_b\left(\frac{R_b + j\omega L_b}{g_\pi + j\omega C_\pi}\right)}. \tag{A.7}$$

and the propagation coefficient of the base line can be expressed as,

$$\gamma_b = \ln\left[1 + 2\left\{\frac{A_b}{B_b} + \sqrt{\frac{A_b}{B_b}\left[1 + \frac{A_b}{B_b}\right]}\right\}\right]. \tag{A.8}$$

II. For Collector Line

$$Z_c = R_c + j\omega L_c \tag{A.9}$$

$$Y_c = \frac{-\omega^2 C_2 C_3 + j\omega C_2}{\frac{1}{\omega_{sc}^2}\left(\omega_{sc}^2 + \omega^2 - \omega^2\frac{r_{cc}C_3}{L_{cx}}\right) + \frac{j\omega}{\omega_{sc}^2}\left(\left(\omega_{sc}^2 - \omega^2\right)C_3 + \frac{(R + r_{cc})}{L_{cx}}\right)} \tag{A.10}$$

$$Z_T^c = \sqrt{\frac{R_c + j\omega L_c}{-\omega^2 C_2 C_3 + j\omega C_2}\left(M_0 + M_1\right)} \tag{A.11}$$

where,

$$M_0 = \frac{1}{\omega_{cc}^2}\left[-\omega^2 - \omega^2\frac{R_c C_3}{L_c} + j\omega\left(-\omega^2 C_3 + \frac{R_c}{L_c}\right)\right] \tag{A.12a}$$

$$M_1 = \frac{1}{\omega_{sc}^2}\left[\omega_{sc}^2 + \omega^2 - \omega^2\frac{r_{cc}C_3}{L_{cx}} + j\omega\left(\left(\omega_{sc}^2 - \omega^2\right)C_3 + \frac{(R + r_{cc})}{L_{cx}}\right)\right] \tag{A.12b}$$

$$Z_{\pi}^{c} = \sqrt{\frac{N_0}{N_1}} \tag{A.13}$$

where,

$$N_0 = \frac{R_c + j\omega L_c}{-\omega^2 C_2 C_3 + j\omega C_2}\left[\frac{1}{\omega_{sc}^2}\left(\omega_{sc}^2 + \omega^2 - \omega^2\frac{r_{cc}C_3}{L_{cx}}\right) + \frac{j\omega}{\omega_{sc}^2}\left(\left(\omega_{sc}^2 - \omega^2\right)C_3 + \frac{(R + r_{cc})}{L_{cx}}\right)\right]^2 \tag{A.14a}$$

$$N_1 = \frac{1}{\omega_{cc}^2}\left[-\omega^2 - \omega^2\frac{R_c C_3}{L_c} + j\omega\left(-\omega^2 C_3 + \frac{R_c}{L_c}\right)\right] + \left[\frac{1}{\omega_{sc}^2}\left(\omega_{sc}^2 + \omega^2 - \omega^2\frac{r_{cc}C_3}{L_{cx}}\right) + \frac{j\omega}{\omega_{sc}^2}\left(\left(\omega_{sc}^2 - \omega^2\right)C_3 + \frac{(R + r_{cc})}{L_{cx}}\right)\right] \tag{A.14b}$$

where,

$$\omega_{cc} = \frac{2}{\sqrt{L_c C_2}},\ \omega_{sc} = \frac{1}{\sqrt{L_{cx} C_2}} \tag{A.15}$$

By setting A_c and B_c as follow

$$A_c = \left[\frac{1}{\omega_{cc}^2}\left(-\omega^2 - \omega^2\frac{R_c C_3}{L_c}\right) + \frac{j\omega}{\omega_{cc}^2}\left(-\omega^2 C_3 + \frac{R_c}{L_c}\right)\right] \tag{A.16a}$$

$$B_c = \left[\frac{1}{\omega_{sc}^2}\left(\omega_{sc}^2 + \omega^2 - \omega^2\frac{r_{cc}C_3}{L_{cx}}\right) + \frac{j\omega}{\omega_{sc}^2}\left(\left(\omega_{sc}^2 - \omega^2\right)C_3 + \frac{(R + r_{cc})}{L_{cx}}\right)\right] \tag{A.16b}$$

The characteristic impedance of the collector line can be expressed as,

$$Z_0^c = \sqrt{B_c\left(\frac{R_c + j\omega L_c}{-\omega^2 C_2 C_3 + j\omega C_2}\right)} \tag{A.17}$$

The propagation coefficient of the collector line can be expressed as,

$$\gamma_c = \ln\left[1 + 2\left\{\frac{A_c}{B_c} + \sqrt{\frac{A_c}{B_c}\left[1 + \frac{A_c}{B_c}\right]}\right\}\right]. \tag{A.18}$$

Author's Publications

[1] Thein, T.T., Law, C.L. and Fu, K., "Frequency Domain Dynamic Thermal Analysis in GaAs HBT for Power Amplifier Applications," in *Progress In Electromagnetics Research* , Vol-118,pp 71-87, 2011.

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