STUDY OF ULTRA-THIN MICA FOR GATE DIELECTRIC PURPOSE

LOW CHONG GUAN

LOW CHONG GUAN

School of Electrical and Electronic Engineering

A thesis submitted to the Nanyang Technological University in partial fulfilment of the requirement for the Degree of Doctor of Philosophy

2017

Acknowledgement

I would like to express my sincere appreciation to the following people who have played important roles in the accomplishment and completion of this report for my PhD Study.

Special thanks to my supervisor, Professor Zhang Qing, for his invaluable advice and information necessary to the completion of this project. I am also thankful for him giving me the opportunity to work under his supervision.

I would also like to thank the group members who had work together with me, Dr Li Hong, Dr Gao Pingqi, Dr Huangkai, Dr Zhou Jianping, Dr Rajkumar, Dr Yuan Shaoning and Ms Luan Xuena for their support and discussion throughout this work. Their invaluable advices were essential in helping me to meet the objective of this project.

Not to forget the lab technicians in Characterization Lab, Nanyang Nanofabircation Centre: Muhd Fauzi bin Abdulah, Mohamad Shamsul Bin Muhammad, etc, their support and contribution are very much appreciated.

Last but not least, I would like to thank Associate Professor Wang Hong (EEE, NTU) for allowing me to borrow their equipment for the characterization of my devices.

Table of Content

Acknowledgement 2
Table of Content 3
List of Figures 5
Abstract 11
CHAPTER 1: Introduction 13
1.1 Bottleneck of Silicon Technology 13
1.2 Novel material systems 15
1.2.1 Graphene and carbon nanotubes - the next promising candidates 16
1.3 Objectives 19
1.4 Major contributions on the dissertation 19
1.5 Thesis organization 20
CHAPTER 2: Literature Review 22
2.1 Carbon-based Materials 22
2.1.1 Graphene 25
2.1.2 Carbon Nanotubes (CNTs) 27
2.1.3 Chiral Vector 29
2.1.4 Translation vector 32
2.1.5 Lattice structure 33
2.1.6 Density of states and energy gap 33
2.1.7 Carbon Nanotube Field-effect Transistor (CNTFET) 34
2.1.8 Conventional-CNTFET (C-CNTFET) 42
2.1.9 Carbon Nanotube Network Field Effect Transistor (CNT-NET-FET) 44
2.1.10 Graphene Field-effect Transistor (GFET) 47
2.2 Overview of Mica 49
CHAPTER 3: Study of Contrast Spectroscopy of Ultra-thin Mica Flakes 52
3.1 Introduction 52
3.2 Theoretical Background and Methodology 55
3.3 Conclusion 68
CHAPTER 4: Ultra-thin and Flat Mica as Gate Dielectric Layer for Carbon Nanotube Field-Effect Transistors 69
4.1 Introduction 70

4.1.1 Why mica is important compared to other dielectric materials? 70
4.2 Experimental Details 71
4.2.1 Mechanical exfoliation (Scotch-tape method) of mica 71
4.3 Fabrication of CNTFETs 74
4.3.1 Top-Contact CNTFETs 74
4.3.2 Bottom-contact CNTFETs 78
4.4 Results and Discussions 80
4.5 Conclusion 89
CHAPTER 5: Graphene Field Effect Transistors with Mica as Gate Dielectric Layers 90
5.1 Introduction 90
5.2 Experimental Details 93
5.2.1 Preparation of graphene and mica specimens 93
5.2.2 Graphene field-effect transistor fabrication 94
5.3 Results and Discussions 96
5.4 Conclusion 110
CHAPTER 6: Conclusive Remarks and Future Works 111
6.1 Conclusive Remarks 111
6.2 Future challenges 113
List of Publications 116
References 117

List of Figures

Figure 2-1: Energy band hybridization process of carbon materials. 23

Figure 2-2: The carbon families – zero-dimension buckyball (left), one-dimension carbon nanotubes (middle) and two-dimension graphene (right) [22] 24

Figure 2-3: The quantized energy levels and density of states of graphene, The Dirac point is the point where the the bandgap is zero. 26

Figure 2-4: (left) The observation of MWCNTs by Iijima *et al.* in 1991 [21] and (right) SWCNTs by Oberlin *et al* [38]. 28

Figure 2-5 The coordinates of the unrolled honeycomb lattice of the carbon nanotube. Rolling of the graphene sheet in different direction gives different type of carbon nanotubes of different electronic properties [40]. 29

Figure 2-6: The graphene sheet can be viewed as the unrolled carbon nanotube. When the site O and A, B and B' are connected, it forms the carbon nanotube [41]. 30

Figure 2-7: Rolling of graphene sheet in different direction gives different types of carbon nanotubes: zigzag, armchair and chiral nanotube [40]. 31

Figure 2-8: Transfer characteristics and I_D-V_{DS} of a CNTFET with channel length of 300 nm [32]. 35

Figure 2-9: Schematic of (a) bottom-contact CNTFETs structure and (b) top-contact CNTFETs structure. 36

Figure 2-10: Band diagram of CNT p-n junction for different doping level. The depletion region of heavily-doped p-n junction (right graph) shows abrupt and short depletion width [48]. 38

Figure 2-11: Calculated conductance versus gate voltage at room temperature, with the work function ranging from -0.2 eV (red dashed), -0.1 eV (orange dashed), 0 eV (mid-

gap work function) (green), +0.1 eV (light blue), to +0.2 eV (blue). (right) The experimentally measured of the role of oxygen adsorption on a annealed (n-type) CNTFET. The CNTFET was exposed to oxygen for 2 min at P = 0 Torr (red), P = 10^{-4} Torr (orange), P = $5x10^{-4}$ Torr (light green), P = $5x10^{-3}$ Torr (dark green), P = 10^{-1} Torr (light blue), and in ambient gas (blue) [46]. 40

Figure 2-12: A CMOS-like inverter was fabricated by Yu *et al*. based on ambipolar CNTs with gain of 4 [57] 41

Figure 2-13: (a) Structure of electrostatically doped C-CNTFET with 4 split gates as reported by Wind *et al.* [28]. (b) Transfer characteristic of the device operating as a SB-CNTFET (black) and C-CNTFET (red) (c) Upper: Band diagram of a p-SB-CNTFET. Lower: Band diagram of a p-i-p p-C-CNTFET [59]. 43

Figure 2-14: (a) Structure of chemically doped C-CNTFET with top gate stack as reported by Ali Javey *et al.* [60]. (b) Transfer characteristic of the device operating as a p-SB-CNTFET before K-doping (blue) and n-C-CNTFET after K-doping (red) (c) Impact of CNT source/drain doping level on the transfer characteristic. It can be shown that the leakage current is higher for high doping C-CNTFET. (d) Band diagram of a n-i-n N-C-CNTFET [60]. 44

Figure 2-15 (a) High density and perfectly aligned CNTs growth by CVD on quartz substrate, with estimation of density of ~5 CNT/µm. (b) Schematic of the layout of top-gated CNT-NET-FET (c) SEM image of the channel of CNT-NET-FET [67]............ 45

Figure 2-16 (a) shows the schematic of the CNT-NET-FETs based inverter, based on a 40 nm Al2O3 and 70 nm Si3N4 for p-type and n-type transistors, respectively. (b) The typical circuit diagram of an inverter. (c) IDS-VGS of the p-type and n-type CNT-NET-FETs. (d) IDS-VDS of the p-type CNT-NET-FETs. (e) The output performance and voltage gain of the inverter. (f) The AC response of the inverter at 1 kHz. 46

Figure 2-17 Mechanical exfoliated few layers graphene flakes as observed under (a) optical microscope and (b) AFM. (c) AFM image of single layer graphene. (d) SEM image of the graphene FETs fabricated on the SiO_2/Si substrate. (e) The schematic view of the GFET [70]..47

Figure 2-18: Schematic of the top-gated and bottom-gated GFETs. Bottom-gated GFETs make use of the doped-Si substrate as the gate, whereas for top-gated GFETs, the top-gate..48

Figure 2-19: The crystal structure of muscovite mica. On {001} planes, vector a and b are used to define the plane, while vector c is the vector normal to the surface. (a) Side view of the crystal structure of muscovite mica. Each aluminosilicate layers were separated by potassium ions. (b) Top view of the muscovite mica {001} surface. The hexagonal atomic structure consists of Si (with Al atoms as the minor elements) and O atoms [82, 83]. 49

Figure 2-20: Atomic force microscopy image of graphene on mica showing the trapped water adlayers (left) and the Raman spectra (right) showing the Raman shift due to the hole-doping effect [94]. 51

Figure 3-1: (a) Optical image of graphene of 1, 2, 3 and 4 layers, as indicated by blue numbers. (b) Raman spectroscopy as a function of the thickness. (c) Raman mapping of the graphene flake by the intensity of G band. (d) AFM measurement of the graphene flake [95]..54

Figure 3-2 : The tri-layer system of mica/SiO_2/Si used in contrast spectroscopy calculation..56

Figure 3-3 : Calculated contrast for 10 nm thick mica/SiO_2/Si system as a function of oxide thickness and wavelength. The red color band indicates the high contrast, while the blue color indicates low contrast. [100] 58

Figure 3-4 : The contrast spectroscope of graphene sheets with different thickness [95]. 59

Figure 3-5 Extracted contrast of few layered mica on 200 nm, 285 nm and 300 nm thick silicon oxide/ silicon substrate [100]. 60

Figure 3-6: Calculated contrast for 10 nm thick mica/SiO_2/Ti system as a function of oxide thickness and wavelength. The red color band indicates the high contrast, while the blue color indicates low contrast. 61

Figure 3-7: Extracted contrast of few layered mica on 2 nm silicon oxide/titanium substrate, in comparison to few layered mica on 200 nm and 285 nm thick silicon oxide/silicon substrate. 62

Figure 3-8: Optical images of mica flake of 25 nm thickness on 200 nm thick SiO_2/Si substrate under different light illumination of (a) white light (b) blue light filter (c) green light filter and (d) red light filter, respectively. Optical images of mica flakes of 17 nm on 285 nm SiO_2/Si substrate under (e) white light (f) blue light filter (g) green light filter and (h) red light filter, respectively. 64

Figure 3-9 : The contrast spectra of 10 nm, 20 nm and 25 nm thick mica on 200 nm SiO_2/Si substrate (blue) and the contrast spectra of 10 nm, 17 nm, and 20 nm thick mica on 285 nm SiO_2/Si substrate (green) [100]. 66

Figure 3-10 : Optical (a) and AFM (b) images of multi-layer mica flakes on 200 nm thick SiO2/Si substrate [100]. 68

Figure 4-1: Comparison of the surface roughness of SiO2 and mica. (a) AFM image of a SiO2 layer and (b) the three-dimensional representation. (c) AFM image of a freshly cleaved mica flake and (d) the three dimensional representation [100]. 74

Figure 4-2: The schematic of the side view of the top-contact mica-based CNTFET. 75

Figure 4-3: AFM (Top) and optical microscope (bottom) image of the ultra-thin mica on an Au/Ti bottom gate between two passivated source/drain electrodes [100]......... 77

Figure 4-4: The schematic of the side view of the bottom-contact mica-based CNTFET. 79

Figure 4-5: (a) Optical microscope and (b) AFM image of the 13 nm bottom-contact ultra-thin mica CNTFET with transferred CNTs network [100]. 81

Figure 4-6: The AFM image of the 28 nm bottom-contact ultra-thin mica FET. Top inset shows the optical image of the CNTFET [100]. 81

Figure 4-7: The transfer characteristics of the 13 nm bottom-contact mica-based CNTFET for $\boldsymbol{VDS}$ =300 mV, 200 mV and 100 mV. Inset is the gate leakage plot of the device [100]. 83

Figure 4-8: The output characteristics for $\boldsymbol{VGS}$ = -4V, -2V, 0V, 2V, 4V ranging from $\boldsymbol{VDS}$ = -1 to 1 V [100]. 83

Figure 4-9: The transfer curve of the bottom-gate-bottom-contact (cross) and bottom-gate-top-contact (triangle) mica-based CNTFET, respectively. For comparison, the transfer characteristics of a bottom-gate-top-contact (square) 50 nm thick Si_3N_4-based CNTFET is also shown [100]. 85

Figure 5-1: Schematic diagram of the ultra-thin mica based GFET as fabricated on 285 nm SiO_2/Si substrate. 96

Figure 5-2 : Top view of the optical microscope image of the ultra-thin mica based GFET as fabricated on 285 nm SiO_2/Si substrate. The source, gate and drain of the GFET were marked as S, G and D respectively. Bottom: Zoom-in view of the GFET [141]. 97

Figure 5-3 : AFM micrograph of the surface of the mechanical exfoliated mica. The mica flake was about 47 nm and remained its high flatness [141]. 98

Figure 5-4 (a) Transport characteristic (I_{DS}-V_{GS}) and (b) output characteristic (I_{DS}-V_{DS}) of the 47 nm mica-based CNTFETs. 99

Figure 5-5 : The top view (left) of the 35 nm thick mica-based GFET, and the Raman spectra (right) of the graphene on mica structure based on the graphene areas marked by red and blue circle, showing the general spectra of single layer graphene [141]. 101

Figure 5-6 : Raman mapping of the graphene at the frequency of (top) 2600-2750 cm^{-1} and (bottom) 800-2700 cm^{-1}. It showed that the underlying mica gate dielectric did not cause any interference to the graphene Raman spectra at the frequency of 800-2700cm^{-1} [141]... 102

Figure 5-7 : Resistance between the source and drain pads as a function of the gate voltage (R-V_{GS}) for the GFETs of different mica thicknesses, namely, T1 (24 nm, red), T2 (29 nm, purple), T3 (35 nm, blue), T4 (40 nm, green) and T5 (47 nm, blue). In comparison, the R-V_{GS} of the SiO_2-based GFET is named as T6 (40 nm, brown) [141]. 104

Figure 5-8 : The maximum small signal transconductance and effective carrier mobility of T1-T5 were plotted, showing that 24 nm mica based GFET has the highest maximum transconductance and effective carrier mobility. 105

Figure 5-9: The Raman spectra of graphene on mica (red) and graphene on SiO_2 substrate (blue), respectively. 109

Figure 5-10: Blue shift of ~16 cm^{-1} is shown in the Raman spectrum of graphene on mica (red) in comparison to graphene on SiO_2 (blue). 110

Abstract

This thesis presents the major findings achieved for my PhD project on the gate dielectric properties of mica which consists of three parts: (1) contrast spectroscopy and observation of ultra-thin mica flakes, (2) electron transport and gate control capability of mica-based carbon nanotubes field-effect transistors (CNTFETs) and (3) electron transport and gate control capability of mica-based graphene field-effect transistors (GFETs).

The observation of ultra-thin mica is as important as the fabrication of it. With the well-known Fresnel's equation, the tri-layer system of mica/silicon dioxide (SiO_2)/silicon substrate (Si) was constructed to study the contrast spectroscopy of mica on SiO_2/Si substrate. The contrast of 1-3 layers of mica is calculated to be less than 10%, suggesting that the observation of single layer mica is extremely challenging under an optical microscope. With proper selection of the underlying substrate material and dielectric thickness, our simulation results show that the optical contrast could be enhanced to ease the observation of ultra-thin mica for the fabrication of mica-based FETs. On top of it, the use of proper light filters tends to enhance the optical contrast of the mica. For example, in our simulated and experimental results, 285 nm SiO_2/Si results in a peak optical contrast at around 520-550 nm whereas 200 nm SiO_2/Si gives a peak optical contrast at around 400-450 nm. The highest optical contrast of single layer mica (~8%) could be achieved by using 200 nm SiO_2/Si substrate at 400-450 nm excitation.

Ultra-thin mica is used as the gate dielectric layer, as well as the substrate of a FET, to study the dielectric property and gate control capability of mica-based FETs. CVD-grown CNTs are used as the channel of mica-based CNTFETs, and the transistors

possess an excellent subthreshold swing (SS) as low as 110 mV/dec with 28 nm mica gate dielectric. The calculated carrier mobility is 554 cm^2/Vs. In comparison, a 50 nm Si_3N_4 based FET was fabricated. The equivalent oxide thickness (EOT) of 28 nm mica is 14 nm whereas the EOT of 50 nm Si_3N_4 is 33 nm. However, the extracted SS of the mica-based CNTFET is 6 times smaller than that of the Si_3N_4-based CNTFETs. The superior gate control capability of mica, in contrast to Si_3N_4, is believed to be due to the high dielectric constant, high dielectric strength and atomically flat surface. The atomically flat surface of freshly cleaved mica is investigated and confirmed by atomic force microscope (AFM). For a 500 x 500 nm scan size, the root mean square (RMS) roughness of the SiO_2 surface was measured to be 275 pm. This is three times smoother than the thermally grown SiO_2. In addition, the 13 nm mica based CNTFET shows negligible gate leakage current in the pico ampere range.

Graphene is a single-atom-thick material. Hence, the choice of the underlying substrate is critical in realising an ultra-flat graphene which is free of corrugations and ripples. Mica, which has an atomically flat surface, is an excellent candidate for graphene to fit the purpose. The transport characteristic of mica-based GFETs are studied, and it is observed that 24 nm mica-based GFET shows an effective carrier mobility of 2748 cm^2/Vs and a transconductance of 3.36 μS. This is 2-fold and 7-fold larger, respectively, than that of the 40 nm SiO_2-based GFET. The transport characteristic of mica-based GFETs shows hole-doped asymmetry characteristics. The observation was further confirmed by Raman spectra, showing the existence of OH- peak and the blue shift of 2D peak for graphene on mica. The observation could be explained by the hold-doping of water layer for graphene on mica structure.

CHAPTER 1: Introduction

During the past 40 years, silicon-(Si) based microelectronics has experienced an inconceivable development. Microelectronic industry has fully compliant with Moore's Law, i.e., doubling the transistor's performance and density in every 18 months [1] [2]. Following Moore's law, higher speed, larger storage, and lower power consumption electronic devices have been fabricated and put into electronic markets on demand. Thanks to the advanced technology, the consumers can now enjoy superior performance electronic devices with low prices.

1.1 Bottleneck of Silicon Technology

Realization of doubling transistor's density comes from the size reduction of the transistors, also known as the scaling down approach [3]. The miniaturization of transistors allows engineers to incorporate millions of transistors on a single silicon die for more functionality [4, 5]. However, the fabrication processes are getting more and more challenging after sub-20 nm node. The widely discussed short channel effect [6], several unwanted quantum phenomena, which possess insignificant effects on large dimensional devices, have significant influences on the performances of the devices after sub-20 nm node. The noticeable short channel effects such as drain-induced barrier lowering (DIBL), velocity saturation, hot carrier injection (HCI), surface scattering and impact ionization are unavoidable. On the other hands, due to the quantum confinement effect, the down scaling approach becomes more and more difficult to follow the roadmap. As the transistor's channel is getting narrower, controlling the dopant

deposition location and concentration becomes challenging as well. Even a single dopant can now change the doping profile severely into heavily doped regime. This will then cause large variation in the device performances.

When the gate dielectric layer thickness is reduced to several nanometers, the barrier created by the insulating dielectric materials is no longer blocking electron effectively. Hot electrons can tunnel through the dielectric materials, resulting in inability to fully turn on/off the transistors through tuning appropriate gate voltage. The miniaturization of the transistors requires better performance of the gate oxide, and the downscaling of SiO_2 as the gate insulator in transistors is one way to overcome the short channel effect [7]. However, it has already come to the fundamental physical limitation when the thickness is merely few silicon atoms thick. The electrical insulation of such thin SiO_2 is questionable when it comes to <0.7 nm (four atomic layers), and this is another noticeable roadblock in the downscaling road map of silicon technology [8]. The use of insulating films with higher dielectric constant will allow the thickness to be much thicker than SiO_2, while at the same time providing similar gate control capability and performance.

Packing more transistors in a single wafer is the ultimate motivation for shrinking the transistors size, however, the ability to “print” transistors of smaller size is seen to be another road block that limits the further miniaturization of silicon devices. Behind this, lithography technology has also come to the bottleneck since the smallest feature size is defined by the limit of the wavelength being used in the conventional optical lithography. The further miniaturization of the transistors will largely depend on the development of the lithography technology with allows the printing of smaller feature size, with extreme ultraviolet lithography being labelled as the next-generation

lithography technology [9, 10]. As the channel width of transistors now is much shorter than the visible wavelength (400-700 nm), the critical requirements in mask alignment and lithography method (e.g., deep-ultraviolet lithography) become inevitable, resulting in higher fabrication costs [11-13].

As long as further miniaturization persists as driven by the market, silicon technology will reach the physical limits. Much efforts have been made to develop advanced technologies, for examples, utilization of novel structures and new material systems (also known as "more Moore"), or adaptation of "more than Moore's" concept, whereas the transistor switching speed is no longer the primary concern to improve the performances of the devices.

1.2 Novel material systems

Limitation of Si-based technology has driven the search of alternative material systems, for examples, silicon germanium (SiGe) based materials and group III-V based (e.g. InP, GaN) materials, etc to replace silicon as primary materials for microelectronic devices. These material systems exhibit a higher switching speed (>100 GHz compared to few GHz of Si-based transistors), high power and lower noise [14-17] than the silicon counterparts. To date, they are widely employed in high-speed communication electronics [18, 19]. However, these materials are not as abundant as silicon and require more stringent processing conditions to produce high quality crystalline substrates. The high material price tag, combining with the strict requirements on growth/deposition environments (temperature, pressure, etc.) have limited them to replace the Si-technology in future.

1.2.1 Graphene and carbon nanotubes - the next promising candidates

The continuing trend towards miniaturization of microelectronic devices in the last few decades approaches the fundamental physical limits of conventional silicon-based devices. Downscaling of the devices for performance enhancement cannot continue forever due to the fundamental and technological limitation. Therefore, the development of alternative device technologies is pursued. The current research has also moved its focus to low-dimensional carbon nanostructures with the search for new device architectures and materials [20]. They portray a variety of different metallic and semiconducting materials with unique optical, electronic, and mechanical properties.

Graphene and carbon nanotubes (CNTs) have graphitic structures composed of a single atomic layer and multiple layers of sp^2-hybridized carbon atoms arranged in a hexagonal lattice, respectively. The Van der Waals coupling between different carbon atomic layers is relatively weak and it can easily break apart, even though the in-plane σ-bonds between carbon atoms are very strong,

In 1985, Richard Smalley, Robert Curl, and James Heath discovered a new carbon structure named fullerene, also known as buckyball. A fullerene or buckyball is a spherical carbon molecule, which has a common form of C_{60} which its mean diameter is 0.68 nm. In fullerene, it is considered as a carbon nanostructure with zero dimension, since the charge carriers are confined spatially in every direction.

In 1991, Iijima discovered the one-dimensional carbon materials, now named as the carbon nanotubes, using the transmission electron microscope [21]. It is a tiny

hollow cylinder that can be represented as the rolling up version of the two-dimensional monolayer graphite (which later named as graphene). Their diameters can be a range from sub-nanometer to sub-micrometer and their lengths could be up to several millimeters. It was quickly getting attention due to the unique electrical structure, where ballistic transport of carriers could be achieved.

Carbon based materials are very promising for future electronic applications. The preliminary results reported by several groups have shown the prospects of carbon material-based transistors. There have been several initiatives done to enhance the performance of CNT-FETs in terms of the on/off ratio, carrier mobility and the operation voltages since the first carbon nanotube (CNT) field effect transistors (FETs) have been successfully demonstrated. However, there are still many technological problems to be solved before CNT-FETs can compete with Si based counterparts. When the channel length of FETs has been reduced to several tens of nanometers, the gate dielectric thickness has to be reduced accordingly. To date the gate thickness is only several nanometers, whereas the quantum-tunnelling effect becomes unavoidable. To relieve the situation, several high-k dielectric materials, such as hafnium oxide, tantalum oxide, have been introduced. Compared to silicon dioxide, relatively thick high-k layers could achieve a similar gate control effect as an ultra-thin silicon dioxide. Using high-k materials and the metal gate electrode, sub-45 node transistors have been realized. However, these high-k dielectric materials are often rare-earth materials that have limited resource. This could impose some supply issue in the future once they are depleted.

In 2004, Andre Geim and Konstantin Novoselov discovered graphene. It was long time being predicted that this magic material was not practical, as two-dimensional

nanomaterials tend to transform into other form due to thermal instability. Graphene can be rolled up to form carbon nanotubes, wrapped into buckyballs, and stack layer by layer to form graphite. Graphene has attracted a lot of research attention due to its unique mechanical, electrical, and optical properties. Firstly, the sp^2 hybridization process has promised graphene to be one of the strongest material structures. The strong σ-bond between carbon and carbon atom remains a strong interaction force. Free electrons from carbon atoms form the π-bond where electrons can move freely without any scattering process, leading to excellent electrical and heat transport properties. Furthermore, the monolayer semimetal could allow large amount of light pass through, making it a potential candidate as transparent conducting electrodes.

Mica is one of aluminosilicate materials and it has a high dielectric constant, high dielectric strength and large bandgap. Similar to graphite, mica can be regarded as a layer-by-layer material in which atomic layers are stacked together in the natural environment. Using the mechanical exfoliation technique, one can cleave it down to monolayer flakes. These mono and few layers flakes still maintain the electrical properties (like high dielectric constant and strength). When it was used as a substrate to support graphene, commonly observed graphene ripple phenomenon was relieved, making it a good supporting substrate for graphene based devices. Although mica has been a common dielectric material that is widely used in capacitors and transformers for many years, the dielectric properties of ultra-thin mica flakes as gate layers in FETs are still unclear. An in-depth study is necessary.

1.3 Objectives

The main objectives of this PhD projects are listed below:

- To study the contrast spectroscopic characterization of mica dielectric on silicon substrate
- To study the gate control capability and dielectric properties of ultra-thin mica flakes as the gate dielectrics
- To study the electronic transport properties of CNTs and graphene supported by thin mica flakes.

1.4 Major contributions on the dissertation

The main contributions of this PhD project are shown below:

Contrast spectroscopic characterization of the two dimensional materials (mica and graphene) have been systematically studied. Randomly distributed mica sheets with different thickness can be prepared using the mechanical exfoliation technique. These mica flakes are then transferred onto another substrates and used as the gate dielectric for CNT and/or graphene FETs. A few nanometer thickness differences in mica gate dielectric could dramatically alter the gate control capability. Thus, identifying mica flake thickness is highly important. The conventional method of using atomic force microscopy can provide a precise measurement on the thickness. However, this technique may not be realistic as it requires plenty of time in the measurement, resulting in a low throughput. The fundamental of optics - refractive index difference between silicon dioxide and thin mica flakes have been used to develop a robust and easy-to-use

way to characterize the mica flake thickness. With this technique, different thickness mica flakes on a silicon oxide substrate can be differentiated under an optical microscope through their contrasts. Detailed analysis and simulation of mica/SiO_2 contrast spectroscopy have been achieved and the results have been further verified using atomic force microscopy.

Mica flakes of different thicknesses have been used as the gate dielectric material to fabricate mica-based CNTFETs. Mica has several advantages such as high dielectric constant and high dielectric strength over SiO_2 and Si_3N_4 dielectric layers. Owing to its advantages, the leakage current can be reduced to a minimum level, while still be able to increase the gate control capability. Besides, it was demonstrated that the fabricated CNTFETs had a subthreshold swing of 110 mV/dec, transconductance of 0.13 μS and carrier mobility of 554 cm^2/Vs. These parameters are much better than those from the CNTFETs with SiO_2 as the gate dielectric layer.

It was shown that mica is compatible not only as an ultra-flat substrate for graphene, but also as the gate dielectric layer of graphene FETs. Using mica gate dielectric can reduce the ripples on the surface of graphene, which are otherwise observed on the commonly used silicon dioxide gate dielectrics.

1.5 Thesis organization

The thesis is composed of six chapters as described below:

Chapter 1 gives the technological background of silicon based FETs and the problems during scale-down approaches, followed by introducing carbon based materials which are promising for future electronic applications.

In Chapter 2, literature review gives the overview of the device physics of transistors, including bipolar junction transistors and metal semiconductor oxide FETs. The fundamentals of carbon nanotubes and graphene based FETs are discussed. Mica, which is a performance enhanced gate dielectric for carbon nanotubes and graphene based FETs, will be introduced.

Chapter 3 introduces a robust technique to identify different thickness mica flakes on a silicon oxide substrate with an optical microscope. The detailed analysis is given.

Chapter 4 provides the overview of the fabrication process of mica-based CNT-FETs. Mica gate dielectric is compared to silicon oxide and silicon nitride gate dielectrics. The results are also comparable to other high-k dielectric materials based CNTFETs.

In Chapter 5, we demonstrate mica as the gate dielectric layer in graphene FETs. The origin of the performance improvement is discussed.

Chapter 6 will summarize the entire project and some future directions are given.

CHAPTER 2: Literature Review

In this chapter, the literature review of the electronic structure and electrical properties of CNTs and graphene and their applications as FETs were provided. In the last part, the literature review of the properties of mica is included.

2.1 Carbon-based Materials

Discoveries of CNTs and graphene in the past two decades have marked as the beginning of highly intensified research in both nanomaterials and nano devices. Carbon is a kind of unique element which exists in a wide variety of stable forms due to its valency, ranging from insulating/semiconducting diamond to metallic/semi-metallic graphite. Among the allotropes of carbon, diamond and graphite are the more commonly-known ones, where carbon atoms are differently bonded. As a result, they have distinct properties. Carbon is a group-IV element which has a ground state electronic configuration of $1s^2 2s^2 2p^2$. When a carbon is under excitation, the four valence electrons on the 2s and 2p orbitals could undergo energy band hybridization process, where the s-orbital and p-orbital electron energy are mixed to from new hybridized energy states. The hybridization of energy states can be of sp^1, sp^2 or sp^3 configuration, depending on the number of p-orbitals being involved in the hybridization. In any cases, it enables carbon to form a maximum four covalent bonds with other elements such as hydrogen atoms or another carbon atom. The details of the hybridization process are as shown in Figure 2-1.

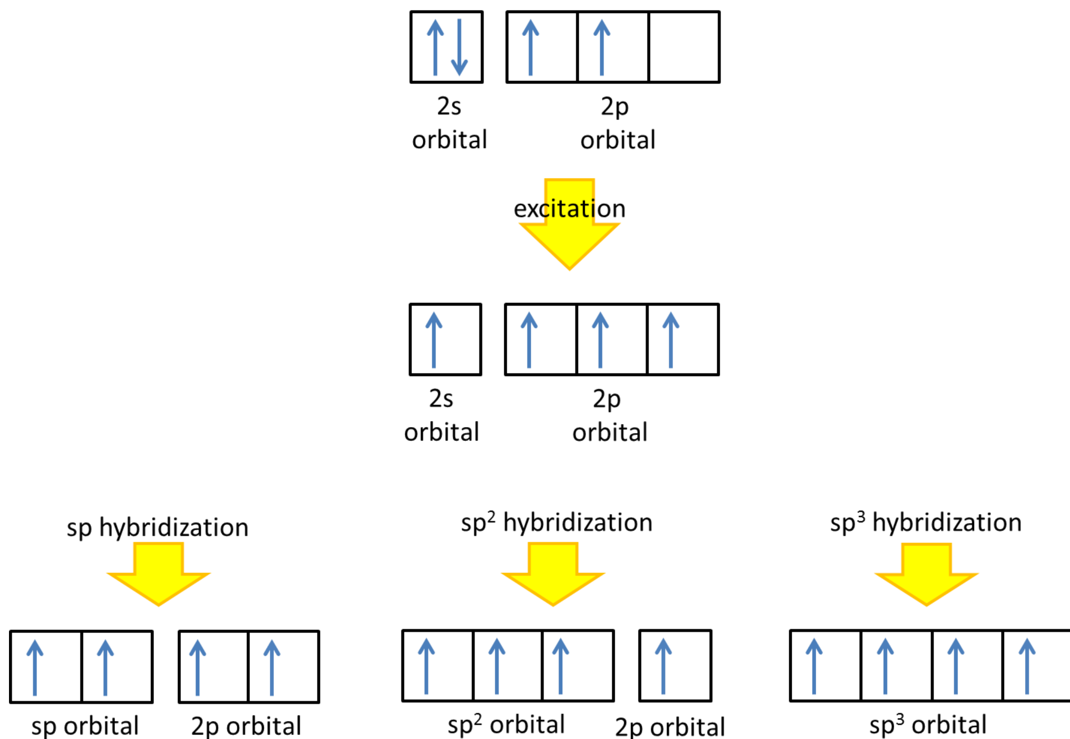


Figure 2-1: Energy band hybridization process of carbon materials.

In the formation of conjugate bonds, the two 2s orbital and two 2p (p_x and p_y) orbital electrons are hybridized for the three sp^2 orbitals. These sp^2 orbitals can form three strong covalent bonds, also known as the σ-bonds on the x-y plane with three other atoms. The remaining one electron on the $2p_z$ orbital that is vertical to the 2-D carbon surface, overlapping with other $2p_z$ orbitals from the adjacent carbon atoms, forms the π-bond. The π-bond can be delocalized easily with an external force (e.g. voltage), and the electrons are able to migrate from one side to another side and therefore, giving sp^2 carbon materials the ability to transport charges.

Carbon allotropes are known to exist in all relevant dimensions - from zero-dimension buckyballs (C60), one-dimension carbon nanotube, two-dimension graphene to three-dimension graphite and diamond. The discovery of buckyballs, carbon nanotubes and graphene has induced an intensive research on low dimension carbon

allotropes due to their extraordinary electronic and mechanical properties. On the other hands, the downscaling challenges and physical limitation such as short channel effect of silicon based technology encourage scientists and researchers to look for alternative materials that may replace silicon. Low dimensional carbon nanostructures do have unique electronic properties and they are regarded as promising materials for nanoelectronics.

In the following part, the report focuses on sp^2 hybridization of carbon materials, i.e. CNTs and graphene, and summarize their unique electronic properties.

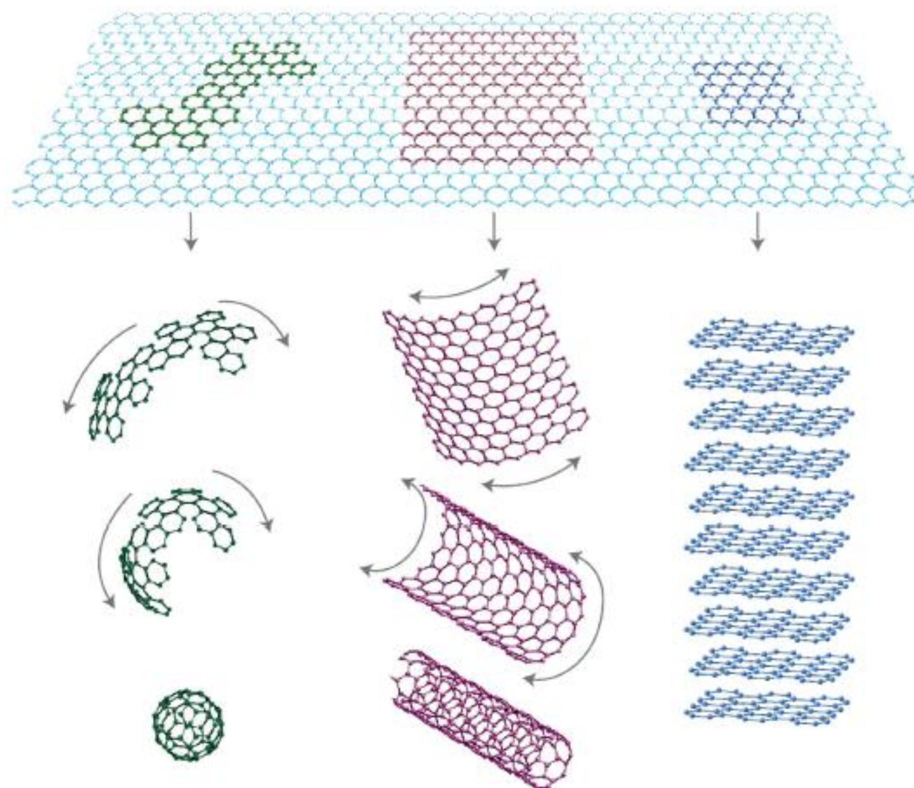


Figure 2-2: The carbon families – zero-dimension buckyball (left), one-dimension carbon nanotubes (middle) and two-dimension graphene (right) [22].

2.1.1 Graphene

Since graphene was first discovered and reported by Andre Geim and Kostantin Novoselov from University of Manchester in 2010 [23-25], it has attracted tremendous interest, not only for fundamental research, but also for potential applications in microelectronics. Graphene is a single-atom sheet of sp^2 bonded carbon atoms in a perfect two-dimensional (2D) honeycomb lattice. It is usually considered as a basic structure to form many other carbon materials. When graphene sheet is rolled up into a cylinder with a nanometer-ranged diameter, it becomes a CNT. Similarly, by stacking over numbers of graphene sheets on top of each other, graphite is formed [22]. As shown in Figure 2-3, graphene has a unique band structure which is different from other carbon nanomaterials. In the Brillouin zone of the band diagram, up to six corners are found to exhibit crossing points at the conduction band and the valence band, and it is called the Dirac points. This is where linear energy dispersion is observed, which contributes to the exceptional optical and electronic properties of graphene. In graphene, electrons move freely with negligible scattering, giving rise to large mean free path. They move like relativistic massless particles over the length scale of hundreds of nanometers. The predicted intrinsic mobility of a suspended graphene is as high as 200,000 cm^2/Vs [26].

The thickness of graphene is around 0.34 nm, which is by far the thinnest material observed. Because of the strong covalent bond between every two carbon atoms in the hexagonal form, it is also one of the strongest materials. The outstanding mechanical strength is due to the strong σ covalent bond. In addition, graphene possesses extraordinary electrical conductivity as well as heat conductivity, and this implies that graphene-based devices retain its electrical property of high carrier mobility at room temperature. These properties and chemical inertness as well as high processability due

to 2D structure promise many potential electronic applications. For example, IBM researcher demonstrated a graphene-based FET by making use of the ballistic transport, achieving 100 Ghz on-off switching speed [27]. This ultra-high speed is otherwise difficult to achieve using conventional silicon-based MOSFETs.

In conjunction to the good mechanical and electronics properties, studies have been done on the optical properties of graphene for its use in transparent electronics and electrodes. The wavelength independency of transmittance of graphene was verified through experiment [28], and it has been demonstrated as high switching speed flexible electronics with transmittance of up to 90% [29].

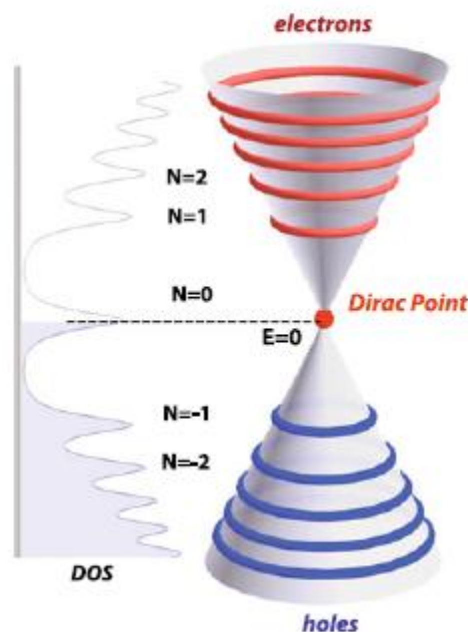


Figure 2-3: The quantized energy levels and density of states of graphene, The Dirac point is the point where the the bandgap is zero.

2.1.2 Carbon Nanotubes (CNTs)

A CNT can be regarded as a piece of graphene rolled up along a certain direction into a nanometer diameter tube with several microns in length. Based on the number of graphene layer in the tube formation, CNTs can be classified as multi-walled carbon nanotubes (MWCNTs), double-walled carbon nanotubes (DWCNTs) and single-walled carbon nanotubes (SWCNTs).

The discovery of thin CNTs was by Iijima *et al.* in 1991 [21] in the soot created in an electric discharge between two carbon electrodes. Under transmission electron microscopy (TEM), as shown in Figure 2-4, the CNT diameters ranged from 4 to 30 nm, and consisted of several graphene shells with the adjacent shell separation of 0.34 nm. In 1993, Iijima *et al.* [30] and another independent team, Bethune *et al*. [31], announced the discovery of SWCNTs. Since then, CNTs captured a great deal of attention.

SWCNTs are very promising for electronic applications due to their outstanding electrical properties that do not exist elsewhere in other material systems [32]. In particular, their energy bandgaps can vary from 0 to 2 eV and they behave as metallic and semiconducting materials accordingly. The electrical and electronic properties of an SWCNT are largely determined by its diameter and chirality. In comparison, MWCNTs show only metallic properties. This cylindrical carbon structure is the strongest and stiffest 1-D material ever discovered due to the covalent sp^2 bonds between the carbon atoms [33, 34]. In addition, from the electronic point of view, the one dimensionality of SWCNTs gives rise to many quantum effects such that the potentials for nanoelectronic applications have been widely reported [35-37]. It has also been identified as a promising semiconductor in International Technology Roadmap of Semiconductors [32].

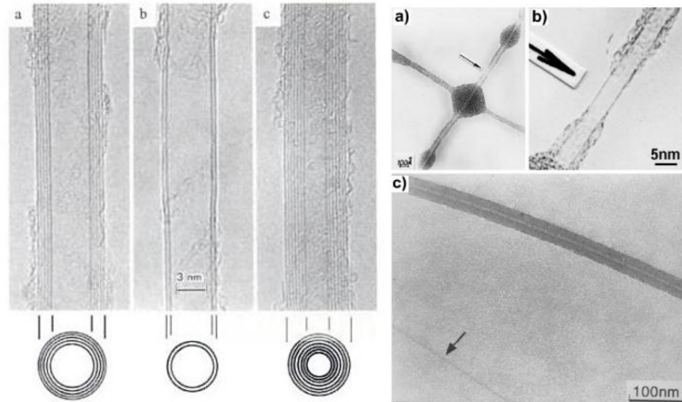


Figure 2-4: (left) The observation of MWCNTs by Iijima *et al.* in 1991 [21] and (right) SWCNTs by Oberlin *et al* [38].

While SWCNTs can be visualized as a rolled-up version of a graphene sheet, it is noted that different rolling directions could generate different CNTs with different electronic properties. The spiral conformation is called chirality and the relationship between the chirality and the electronic properties has been systematically studied and clarified using tight-binding model by several groups [39]. Figure 2-5 shows the graphene sheet, which the direction and orientation of the rolled-up SWCNTs are summarized.

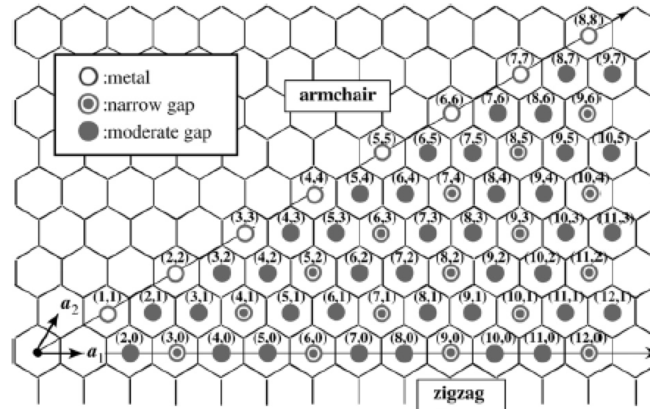


Figure 2-5 The coordinates of the unrolled honeycomb lattice of the carbon nanotube. Rolling of the graphene sheet in different direction gives different type of carbon nanotubes of different electronic properties [40].

2.1.3 Chiral Vector

Figure 2-6 shows an unrolled honeycomb lattice of the nanotube. The basic unit cell of carbon nanotube is formed by the translation vector and chiral vector, which is perpendicular to each other. $\overrightarrow{OB}$ is parallel to the CNT axis, and $\overrightarrow{OA}$ indicates the circumference of the nanotube. By rolling the graphene sheet so that point O and A coincide each other and point B and B’ overlap each other, an SWCNT can be formed. The x and y axis are indicated in Figure 2-6. In Figure 2-6, the vector $\overrightarrow{OA}$ is the chiral vector, $\overrightarrow{C_n}$ whereas $\overrightarrow{OB}$ is the translation vector, $\vec{T}$. The chiral vector, on the other hand, can be expressed by two real space unit vectors of the hexagonal lattice.

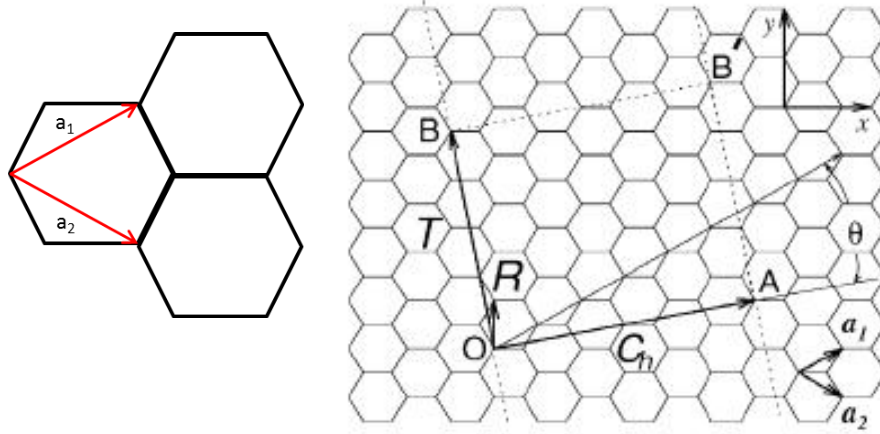


Figure 2-6: The graphene sheet can be viewed as the unrolled carbon nanotube. When the site O and A, B and B' are connected, it forms the carbon nanotube [41].

Based on this, the tube chirality can be defined by chiral vector, which is defined as

$$\overrightarrow{C_n} = m\overrightarrow{a_1} + n\overrightarrow{a_2} \tag{2.1}$$

where n, m denote the distance in primitive vectors, $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ in the hexagonal structure. It can be visualized as the rolling direction of the graphene sheet to form carbon nanotube, and the expression can be described as below [40]:

$$\overrightarrow{a_1} = a_0(\frac{3}{2}x + \frac{\sqrt{3}}{2}y) \tag{2.2}$$

$$\overrightarrow{a_2} = a_0(\frac{1}{2}x - \frac{\sqrt{3}}{2}y) \tag{2.3}$$

where a_0 denotes the graphene lattice constant of 2.461 Å. For simplicity, (n, m) is often used to represent the chiral vector of the SWCNT. For those nanotubes where the circumferential vector is along the exact direction between the two basis vectors, i.e., m = n (chiral vector $\overrightarrow{C_n} = (n, n)$), they are normally called armchair nanotube and they exhibit metallic property. If the circumferential vectors lie along one of the two basis

vectors, i.e., m = 0, ($\overrightarrow{C_n} = (0, n)$), a zig-zag structure is formed. A SWCNT exhibits the semiconducting property if its |n-m| is a factor of 3.

The diameter of the CNT, d, is defined as L/π, in which L is the chiral vector magnitude $\overrightarrow{C_n}$, or the circumferential length of the SWCNT:

$$d = \frac{a\sqrt{m^2+mn+n^2}}{\pi} \tag{2.4}$$

The chiral angle θ is defined as the angle between the vector $\overrightarrow{C_n}$ and $\overrightarrow{a_1}$, with a value range of $0 \leq |\theta| \leq 30°$, which is exactly the angle between the hexagons and the axis of nanotube, as described as the formula below:

$$cos\theta = \frac{\overrightarrow{c_k} \cdot \overrightarrow{a_1}}{|\overrightarrow{c_k}| \cdot |\overrightarrow{a_1}|} \tag{2.5}$$

In particular, zig-zag and armchair nanotubes are of the chiral angle of 0° and 30°, respectively, as shown in Figure 2-7.

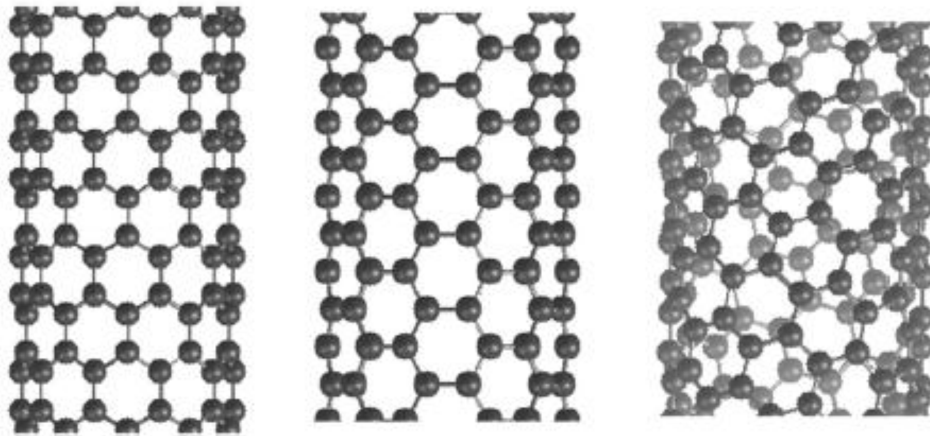


Figure 2-7: Rolling of graphene sheet in different direction gives different types of carbon nanotubes: zigzag, armchair and chiral nanotube [40].

2.1.4 Translation vector

The translation vector $\vec{T}$ is the unit vector of a SWCNT being used to describe the direction parallel to the nanotube axis and as described earlier, it is perpendicular to the chiral vector $\overrightarrow{C_n}$ as shown in Figure 2-6. $\vec{T}$ could be represented by $\overrightarrow{a_1}$ and $\overrightarrow{a_2}$ in the expression below:

$$\vec{T} = t_1\overrightarrow{a_1} + t_2\overrightarrow{a_2} \tag{2.6}$$

For simplicity, $\vec{T}$ is always represented in the form of (t_1, t_2), where t_1, t_2 are integers defined as below

$$t_1 = \frac{2m+n}{d_g} \tag{2.7}$$

$$t_2 = -\frac{2m+n}{d_g} \tag{2.8}$$

and d_g is the greatest common divisor of (2m+n) and (2n+m) and is given by

$$d_g = \begin{cases} q, when\ (n-m)\ is\ not\ the\ multiple\ of\ 3q \\ 3q, when\ (n-m) is\ the\ multiple\ of\ 3q \end{cases} \tag{2.9}$$

where q is the greatest common divisor of (m, n). The magnitude of the translation vector is the unit lattice length along the tube axis direction, and it is given by

$$T = \frac{\sqrt{3}L}{d_g}, \text{ where L is the chiral vector magnitude } \overrightarrow{C_n}, \tag{2.10}$$

2.1.5 Lattice structure

In graphene, every carbon atoms have four valence electrons. Three interacts chemically with the nearest neighbours and form strong in-plane σ bonds, resulting in sp^2 hybridization of the atomic orbitals. A pz orbital pointing outward of the plane is formed, due to the μ bond formed by the residual free electron. The free electron results in the charge current by hopping from one atom to another. With simple tight-binding model, the hopping of the conduction electrons of amplitude of ~3 eV between the nearest neighbours is suitable as the explanation for most of graphene electron properties.

The fundamental unit cell of graphene lattice consists of two atoms. As a result, two sublattice, as well as an associated degree of freedom (DOF) of the electron, exist in the unit cell. The DOF serves as a pheudospin accounted for most of the graphene internal structure of electrons. Apparently, this is a vital aspect in the specificity of electrons in graphene. As a result, several phenomena such as the absence of backscattering for smooth potentials and etc, are all physically seen.

2.1.6 Density of states and energy gap

The density of states $N(E_F)$ per unit length along the CNT axis can be expressed as:

$$N(E_F) = \frac{8}{\sqrt{3}\pi a_0 |\gamma_0|} \qquad (2.21)$$

where a_o is the graphene lattice constant, and $\gamma_0$is the nearest-neighbour C-C tight binding overlap energy. For semiconducting CNTs, the density of states is zero at Fermi

level, whereas for metallic nanotubes, the value is non-zero. The energy gap of semiconducting nanotube can be deduced by the reciprocal of the nanotube diameter.

$$E_g = \frac{2|\gamma_0|a_0}{d} \tag{2.22}$$

It can be seen that the energy gap is independent of the chiral angle. For the case of graphene with infinite diameter, there is no bandgap. The model is confirmed through experiment by using scanning tunnelling microscopy.

2.1.7 Carbon Nanotube Field-effect Transistor (CNTFET)

One of the first proposed applications of carbon-based materials is related to their electrical properties for high speed electronics. While this is true, field-effect transistors consisting of semiconducting CNT channels exhibit very good performance. Due to the quasi one-dimensionality and the high intrinsic carrier mobility and saturation velocity (5.5×10^7 cm s^{-1}), semiconducting CNT based FETs could show a high switching capability and fast operating speed. Carrier saturation velocity is another critical measure for short channel high-speed devices. The carrier saturation velocity becomes a significant criterion for high-speed devices, particularly at short gate lengths. The source-drain electric field is inversely proportional to the channel length. When the channel length is small, the electric field increases, the steady-state carrier velocity begins to saturate. Based on the theoretical calculation, the peak intrinsic average carrier velocity of graphene can be as high as 4.6×10^7 cm s^{-1}, and it is 4 times larger than that

of the conventional Si. For short channel transistors, saturated carrier velocity becomes another critical issue of the transport properties.

Since the first CNTFET was reported in 1998 [42, 43], many groups have made notable effort in studying CNTFETs to investigate the working principle of CNTFETs, as well as to challenge the performance limit of CNTFETs. In 2004, Javey *et al* reported a ballistic CNTFET exhibiting room-temperature conductance near the ballistic transport limit of 4 e^2/h. [32]. The transfer characteristics and the I_D-V_{DS} of the CNTFET were shown in Figure 2-8. It was reported that the CNTFET possessed high current-carrying capability of 25 μA per tube and high on/off ratio of about 5 orders [32].

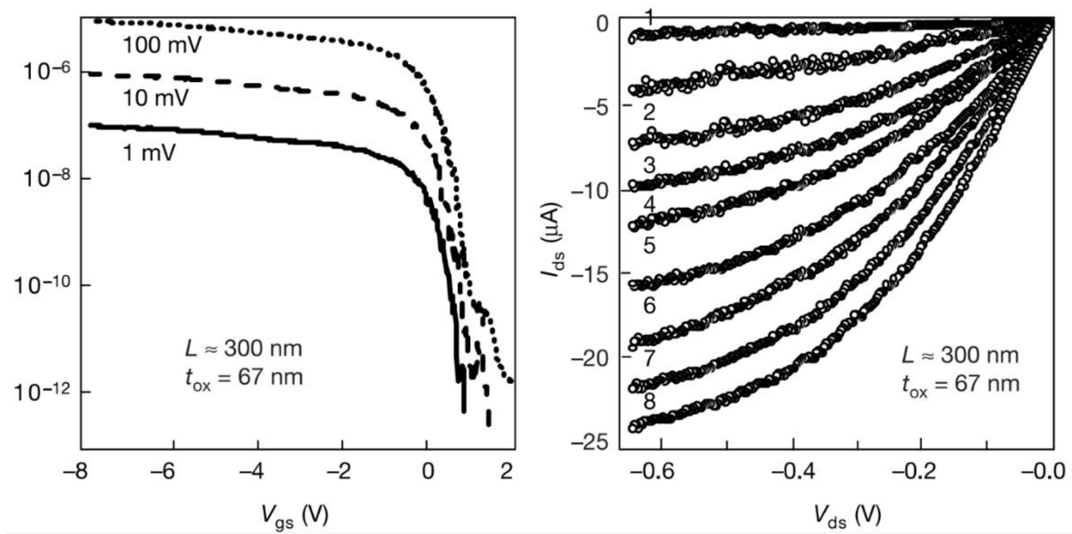


Figure 2-8: Transfer characteristics and I_D-V_{DS} of a CNTFET with channel length of 300 nm [32].

2.1.7.1 Design of CNTFETs

There were several reported CNTFET structures, such as back-gated CNTFETs, top-gated CNTFETs, wrap-around gate CNTFETs, suspended CNTFETs and etc. Among all the reported CNTFETs, back-gated CNTFET is the most commonly reported CNTFET structure, due to their simpler fabrication processes in comparison to, for example, wrap-around gate CNTFETs. In this case, silicon oxide and silicon substrate are usually used as the gate insulating layer and gate of the CNTFET. The device schematic is shown in the Figure 2-9. Metal electrodes are lithographically patterned and then bridged with SWNTs. Figure 2-9 (a) shows the schematic of bottom-contact CNTFET, in which the CNT rests above the electrodes. In this case, the contact relies on the weak Van der Waals force between the CNT and the electrodes, resulting in poorer CNT-electrodes contacts. In comparison, for top-contact CNTFETs, SWNTs are buried underneath the source and drain pads, see Fig 2-9(b). This creates better electrical contacts between the CNT channel and source/drain electrodes, resulting in lower contact resistance. It was widely reported that the contact of metal electrodes and carbon nanotubes plays a significant role in the device performance as CNTFETs function as unconventional "Schottky barrier (SB) transistors" [44-47]. In other words, unlike conventional MOSFET, the switching mechanism of the transistor is mainly modulated by the contact resistance instead of the channel conductance [46].

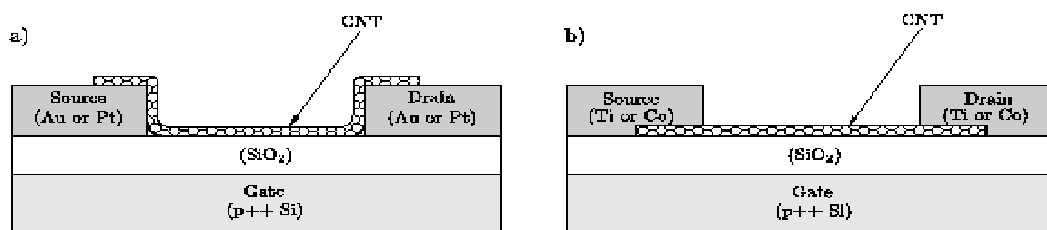


Figure 2-9: Schematic of (a) bottom-contact CNTFETs structure and (b) top-contact CNTFETs structure.

2.1.7.2 Schottky Barrier Carbon Nanotube Field Effect Transistor (SB-CNTFET)

Appenzeller *et al.* showed that one-dimensional Schottky barrier (SB) of metal/electrode interface determines the device performance [47]. Since the performance of SB-CNTFET is highly related to the contact between the electrodes and CNT, the electrical contact properties were studied extensively by many research groups. Heinze *et al.* showed that the geometry and the work function of the metal electrodes determine the characteristics of the CNTFET [46]. The electric field at the contacts is induced by the back gate, indicated by the electric field strength which defines the barrier's width and thus the current injection. Another critical deciding factor affecting the device behaviour (n-type, p-type or ambipolarity) is the work function of the metal electrodes, especially for SB-CNTFET.

The injection of holes (electrons) from the three-dimensional metals to the one-dimensional CNTs is mainly through thermionic emission (which is the dominant mechanism in three-dimensional conventional device) and thermally-assisted tunnelling. Due to the abrupt and short depletion region in one-dimensional CNT, the injection of holes (electrons) from the metal electrodes into the valance band (conduction band) of the CNT is mainly contributed by the tunnelling through the SB. Appenzeller *et al.* studied the competition between tunnelling versus thermionic emission in one-dimensional semiconductor, and suggested that the current injection mechanism is often dominated by thermally assisted tunnelling [47].

Leonard *et al*. reported on the properties of p-n junction, n-i junction and Schottky barriers in nanotube devices, and the simulated and calculated results showed the exponential dependence of depletion width on inverse doping in nanotube devices. This suggested that nanotube devices is not a simple miniature versions of conventional planer devices, instead, the reduced dimensionality of nanotube devices in comparison to conventional planer devices had resulted in drastic difference of the electrostatics, doping and charge transfer [48]. A significant observation was that the depletion length could be a few micro-meter at low doping concentration whereas at a high doping concentration, the depletion length reduced significantly to a nanometer range [48], as shown in the simulation result in Figure 2-10. Hence, tunnelling phenomenon can be observed easily in one dimensional CNT due to the existence of the abrupt and thin energy barrier at the contact junction. Further scaling of SB-CNTFET can be achieved by reducing gate dielectric thickness so that the gate control is sufficiently strong to modify the thin Schottky barrier, resulting in a high tunnelling rate, high on/off ratio and smaller subthreshold swing of approaching 60 mV/dec.

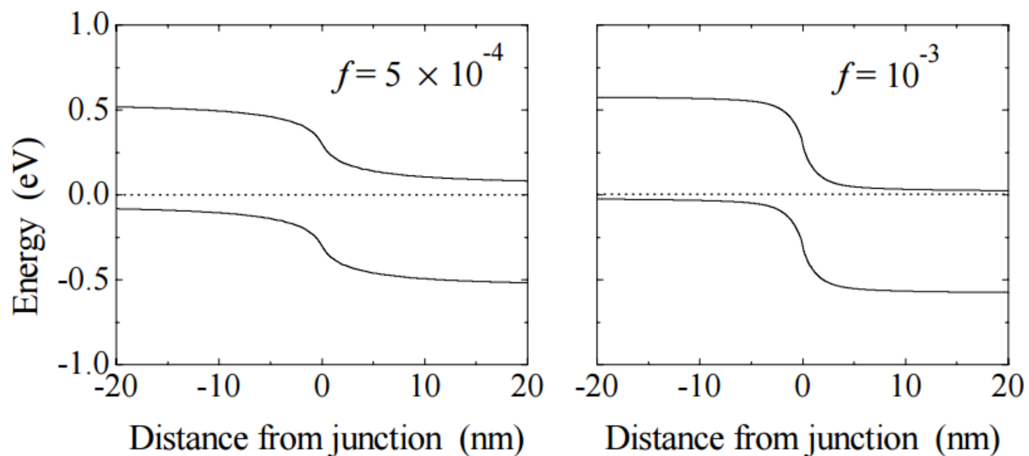


Figure 2-10: Band diagram of CNT p-n junction for different doping level. The depletion region of heavily-doped p-n junction (right graph) shows abrupt and short depletion width [48].

2.1.7.3 Conduction Types of CNTFETs – p-type, n-type and ambipolar

In order to realize ballistic CNTFETs, low contact resistance between the metal electrodes and CNT is preferred. Several attempts were reported to improve the contacts, and one way was thermal annealing at 820 ℃ in an inert ambient gas. High temperature annealing is believed to enhance the coupling between the contacts and CNTs. [49]. Besides, the contact resistance can be reduced intrinsically through proper selection of the contact metal materials of different work functions [50-54].

Choosing an appropriate metal for the electrodes is significant as the metal work function defines the SB profile (height and width) and hence the injection of holes and electrons into the CNT channel. For example, in the design structure as described in previous section, Au/Ti are widely used as the materials for electrodes. The contact resistance is generally higher (>1 MΩ), with low transconductance and high subthreshold swing [50]. In general, most CNTFETs of this type were reported to be p-type. This can be interpreted as oxygen absorption on Au surface [50] [35] could efficiently increase the work function of Au, and hence the Fermi level of Au pad is closer to the valence band of the CNT channel, rather than that of the conduction band. As a result, a small SB for holes and a large SB for electrons are formed, leading to a p-type CNTFET. Well reported high work function metals for p-type CNTFETs are typically Au and Pd [32, 55].

In contrast, when a low work function metal, like Al, is used as the pads, n-type CNTFETs can be fabricated [56]. In Fig 2-11, simulation results of Heinze *et al.* showed the effect of different work function materials on the transfer characteristic of the CNTFETs [46]. For a mid-gap work function metal, a symmetric transfer characteristic of the CNTFET can be observed. Decreasing the work function of metal gives a smaller

SB for electrons. As a result, an n-type CNTFET can be obtained (red dashed in Fig 2-11 (a)). An increase in p-type behavior can be observed if the work function is increased (blue in Fig 2-11 (a)) [46]. The modelling is consistent with the experimental results. In Fig 2-11 (b), Heinze *et al*. showed that the oxygen absorption contributed to the p-type behaviour of CNTFET, as what was discussed in other literature [46].

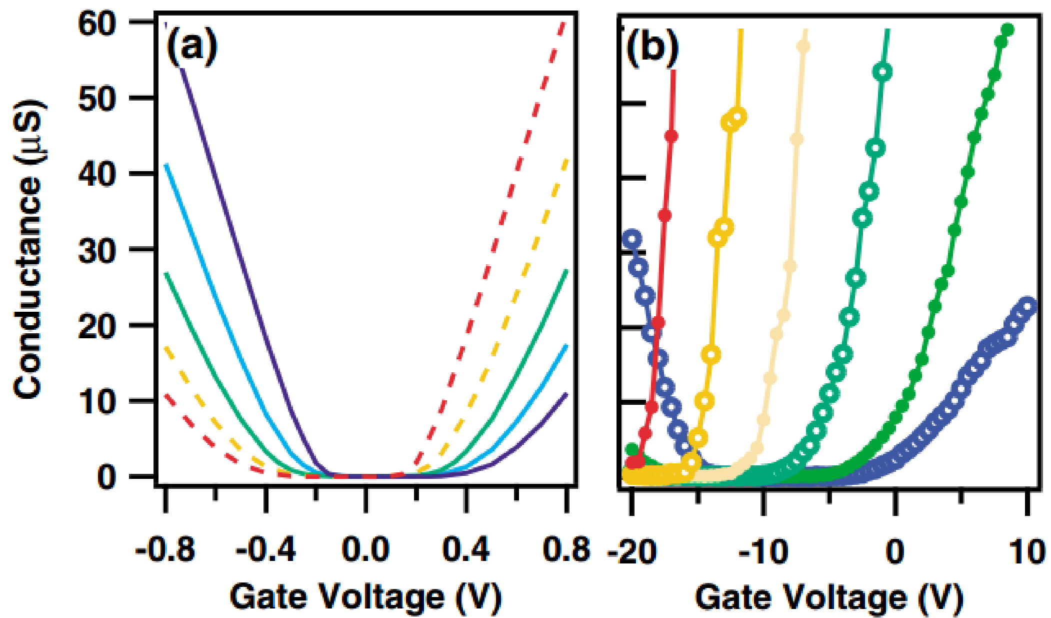


Figure 2-11: Calculated conductance versus gate voltage at room temperature, with the work function ranging from -0.2 eV (red dashed), -0.1 eV (orange dashed), 0 eV (mid-gap work function) (green), +0.1 eV (light blue), to +0.2 eV (blue). (right) The experimentally measured of the role of oxygen adsorption on a annealed (n-type) CNTFET. The CNTFET was exposed to oxygen for 2 min at P = 0 Torr (red), P = 10^{-4} Torr (orange), P = $5x10^{-4}$ Torr (light green), P = $5x10^{-3}$ Torr (dark green), P = 10^{-1} Torr (light blue), and in ambient gas (blue) [46].

The ambipolar CNTFET was also reported by R. Martel *et al.* [49]. The electron conduction is caused by electrons and holes tunnelling at the nanotube/metal contacts under positive and negative gate voltages, respectively. When the gate voltage is positively large enough such that the tunnelling barrier for electrons is thin for tunnelling, electrons can be easily injected in the CNT channel. In contrast, if the gate voltage is

increased negatively, the tunnelling barrier for holes is thin for tunnelling, there is a hole current along the CNT channel.

A unipolar CNTFET with high on current and low off current is preferred in order to achieve a high on-state switching speed and a low off-state leakage current. However, as proven by Yu *et al.*, since the ambipolarity of CNTFET can be suppressed and enhanced by applying a proper gate voltage, the ambipolar CNTFETs based logic circuits can be realised, without doping the CNTs [57]. They made use of the ambipolarity of CNTFET in realising a CMOS-like inverter with gain of 4, which was comparable to Si device level, as shown in Figure 2-12. However, fabrication of ambipolar CNTFETs based CMOS logic circuits is challenging as it requires tight process control of p- and n-type CNTFETs with a high repeatability, as key specifications such as the threshold voltage, the on-off current level, hysteresis and on/off ratio are highly correlated to the process control.

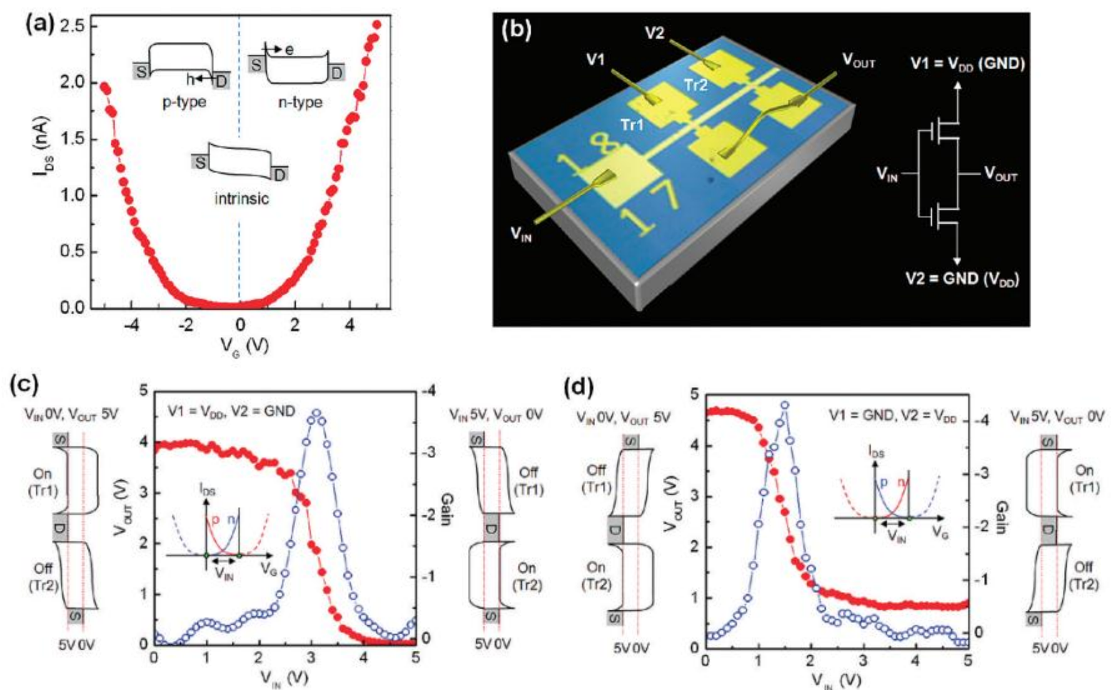


Figure 2-12: A CMOS-like inverter was fabricated by Yu *et al*. based on ambipolar CNTs with gain of 4 [57] .

One way to achieve CNTFETs for better performance is to employ a high-k dielectric insulating layer, such as hafnium oxide (HfO_2) or zirconium oxide (ZrO_2) [55, 58]. As discussed, due to the one dimensionality of CNTs, the Schottky barrier of CNTFETs with high-k dielectric can be very thin, leading to a strong gate control capability so that the CNTFETs can be switched on or off by a small gate voltage change. The transport through the interface between the metal electrodes and CNTs was discussed and reported by Nakanishi *et al.* [58]. For a small gate dielectric thickness, the band bending is mainly located near the metal/CNT end (abrupt and thin Schotty barrier, as discussed above), hence, resulting in a high tunnelling current.

2.1.8 Conventional-CNTFET (C-CNTFET)

In contrast to SB-CNTFETs in which the channel conductance of the CNTFET is controlled by the CNT/metal contact SB, conventional CNTFETs have their channel conductance controlled by the CNT channel itself, instead of the contact SBs. Wind *et al.* have reported on the C- CNTFET in 2004 [59]. They fabricated a CNTFET with 4 split gates of different lengths, and the split gates were separated by around 20 nm in order to ensure that the CNT was completely covered by the 4 gates, see Figure 2-13. Instead of doping the CNT chemically, they doped it electrostatically through the split gates. The p-i-p (p-doped-intrinsic-p-doped) structure, which replicated the band diagram of conventional p-MOSFET, was formed by applying a negative gate voltage at the two outer gates. The I_D-V_G curve obtained by sweeping the two inner gates shows improved subthreshold swing, from 400mV/dec (by sweeping all gates together,

operating as SB-CNTFET) to 180mV/dec. This result shows that the CNTFET with bulk switching can be constructed by using a split gate design to dope the CNT electrostatically, with the working principle and mechanism similar to a conventional semiconductor p-MOSFET.

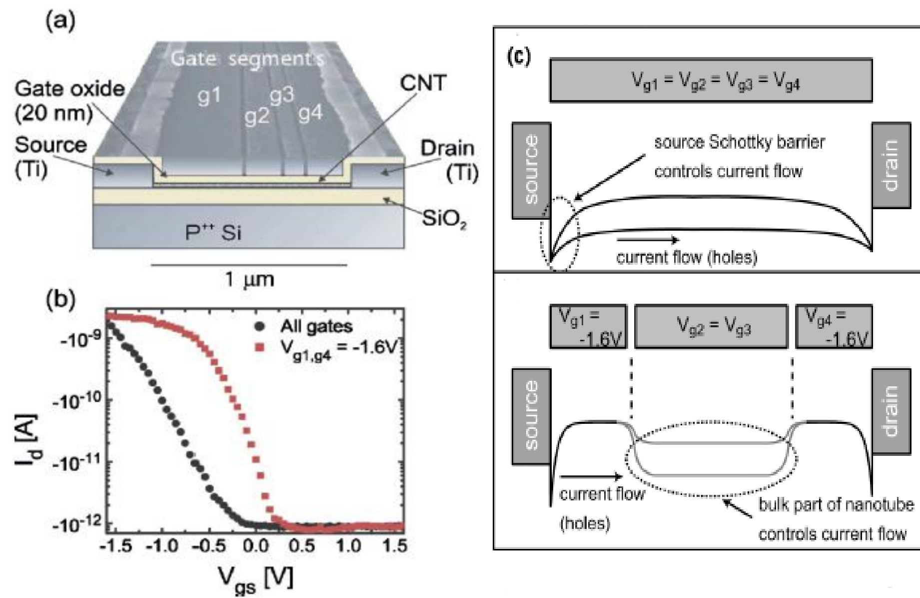


Figure 2-13: (a) Structure of electrostatically doped C-CNTFET with 4 split gates as reported by Wind *et al.* [28]. (b) Transfer characteristic of the device operating as a SB-CNTFET (black) and C-CNTFET (red) (c) Upper: Band diagram of a p-SB-CNTFET. Lower: Band diagram of a p-i-p p-C-CNTFET [59].

Javey *et al.* reported on the device design of C-CNTFET with its working principle and mechanism similar to the n-i-n (n-doped-intrinsic-n-doped) conventional n-MOSFET [60]. Instead of using back gate to turn on or turn off the device, a top gate stack of Ti/Pd/HfO_2 was fabricated on the CNT to control the device. The gate stack did not overlap Pd contact. The section of the CNT (near to the Pd contact) which was not covered by the gate stack was doped chemically by potassium to realize n region. A n-i-n structure was realized. By sweeping the top gate electrode from -1 V to 1 V, the transfer characteristic showed high on-current and small subthreshold swing of 70

mV/dec, implying good switching performance of approaching the limit of 60 mV/dec, see Figure 2-14. Javey *et al.* also reported on the C-CNTFET by using Pd pads for ohmic contact, high-k gate dielectrics and electrostatically induced CNT source and drain region to realize a p-C-CNTFET [53].

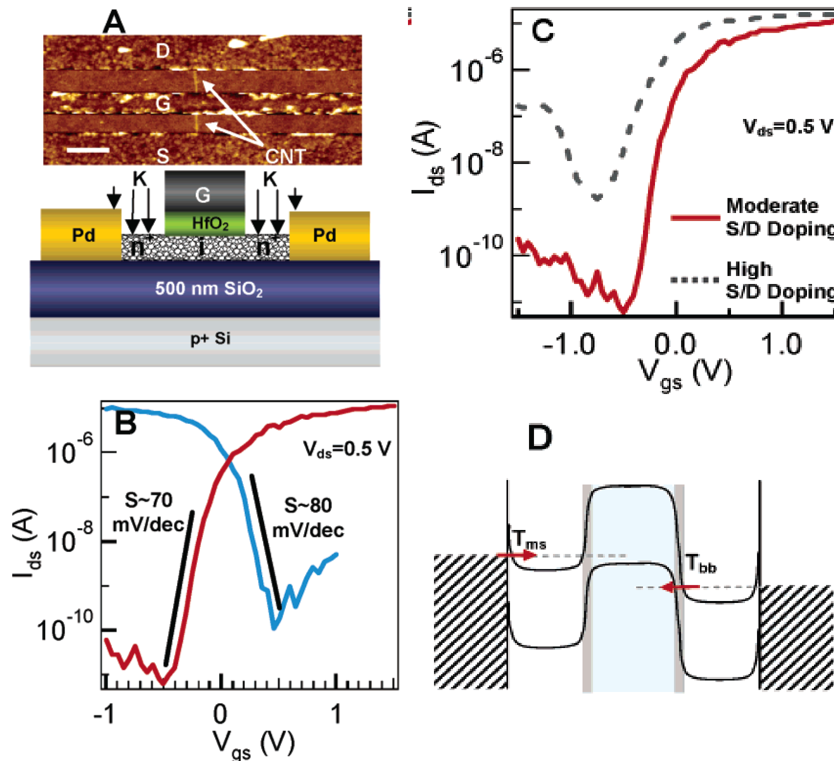


Figure 2-14: (a) Structure of chemically doped C-CNTFET with top gate stack as reported by Ali Javey *et al.* [60]. (b) Transfer characteristic of the device operating as a p-SB-CNTFET before K-doping (blue) and n-C-CNTFET after K-doping (red) (c) Impact of CNT source/drain doping level on the transfer characteristic. It can be shown that the leakage current is higher for high doping C-CNTFET. (d) Band diagram of a n-i-n N-C-CNTFET [60].

2.1.9 Carbon Nanotube Network Field Effect Transistor (CNT-NET-FET)

CNT is well known of its extraordinary electronics properties, however, the reproducibility of CNTFETs due to the difficulty in controlling the chirality, diameter and orientation of the tubes are the major drawbacks and obstacle for scalable integrated

circuit [61]. CNT-NET-FETs are made of CNT networks as the channel of the FETs, which high density and perfectly aligned horizontal arrays of CNTs are preferred to realize the full potential of CNTs. In contrast to CNTFETs based on a single CNT, CNT-NET-FETs minimize device-to-device variations which make it possible for large area fabrication, at the same time retaining the high carrier mobility, high current carrying and excellent mechanical and optical property of CNTs [62]. CNT-NET-FET was reported widely for the application for thin-film transistors (TFTs) [63, 64], flexible electronics [62, 65, 66], complementary devices or logic gates [67, 68].

Kang *et al*. has reported on the high-performance CNT-NET-FETs using dense, perfectly aligned and CVD-growth CNT network, which the device-level mobility is as high as ~1000 $cm^2V^{-1}s^{-1}$ and transconductance of ~3000 Sm^{-1}, as shown in Figure 2-15 [67]. The I_{on}/I_{off} ratio of the device could improve to ~10,000 with electrical breakdown process to remove the metallic tubes in the channel, with I_{on} of up to ~1A was reported.

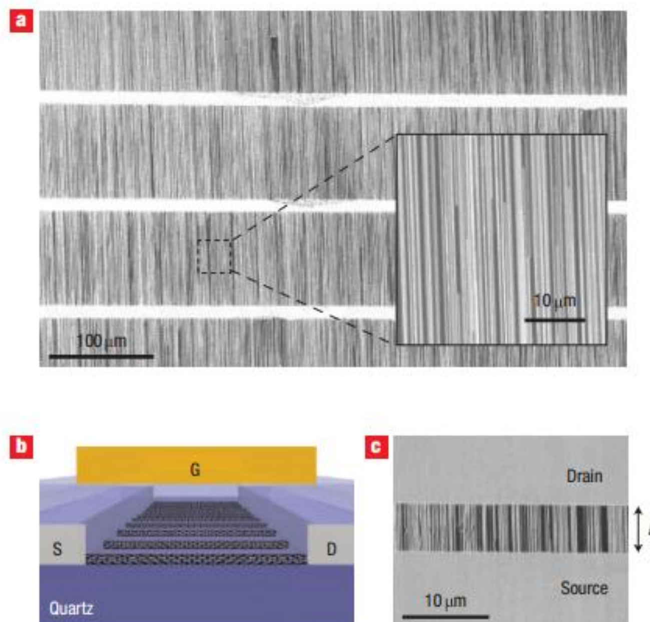


Figure 2-15 (a) High density and perfectly aligned CNTs growth by CVD on quartz substrate, with estimation of density of ~5 CNT/μm. (b) Schematic of the layout of top-gated CNT-NET-FET (c) SEM image of the channel of CNT-NET-FET [67].

As CNTFETs were widely reported to be p-type in the ambient, similar behavior was observed in CNT-NET-FETs too [61, 63, 65, 67]. Gao *et al*. has reported on the conversion of p-type CNT-NET-FETs to n-type behavior by annealing the p-type devices in nitrogen environment for 1 hr at 200 °C, followed by depositing a thin layer of Si_3N_4 layer at 110 °C (~70 nm). This makes it possible to realize complementary logic gate arrays based on CNT-NET-FETs, such as inverter, complementary NOR, OR, NAND, and AND logic gates, as shown in Figure 2-16 [61]. Chimot *et al*. has investigated the performance of gigahertz frequency flexible FETs based on CNT network, and reported that the transistors displayed the transconductance of at least 6 GHz with current gain cutoff frequency as high as 1 GHz at V_{DS}=-700 mV [66].

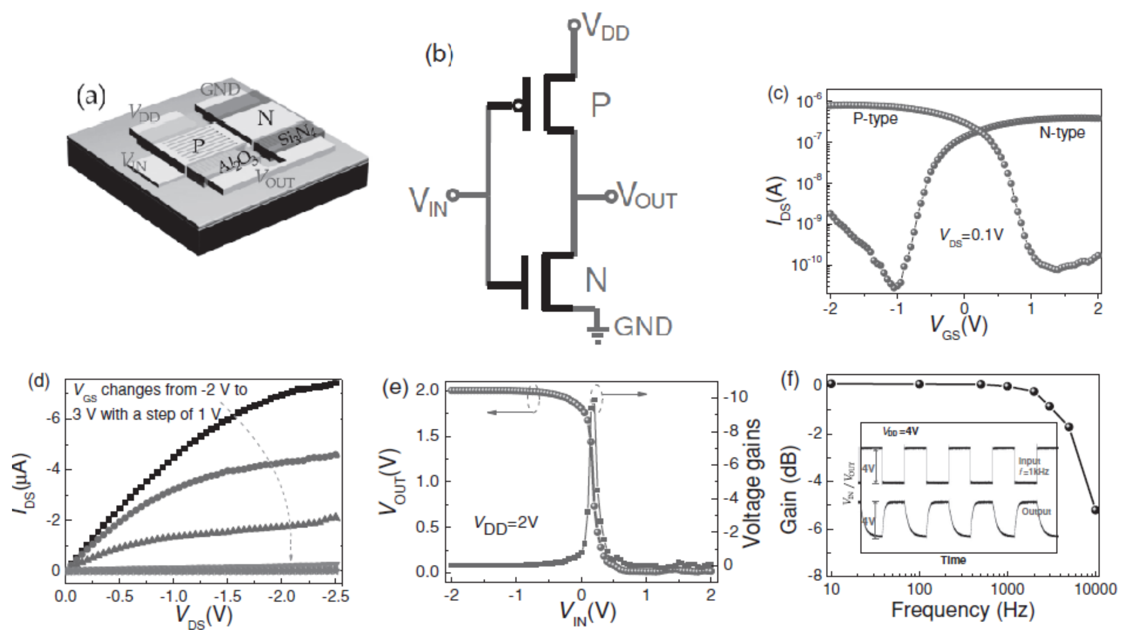


Figure 2-16 (a) shows the schematic of the CNT-NET-FETs based inverter, based on a 40 nm Al2O3 and 70 nm Si3N4 for p-type and n-type transistors, respectively. (b) The typical circuit diagram of an inverter. (c) IDS-VGS of the p-type and n-type CNT-NET-FETs. (d) IDS-VDS of the p-type CNT-NET-FETs. (e) The output performance and voltage gain of the inverter. (f) The AC response of the inverter at 1 kHz.

2.1.10 Graphene Field-effect Transistor (GFET)

Since the discovery of free standing graphene by Novoselov & Geim *et al.*, many other research groups have been reporting on the electronics properties of graphene FETs [22, 69, 70]. The most commonly adopted structure of GFETs is the bottom-gated GFETs, which the graphene was exfoliated mechanically and was placed on the SiO_2/Si substrate, followed by the deposition of the source and drain electrodes to form the FET, as shown in Figure 2-17 [70]. Subsequently, several types of graphene FETs was proposed.

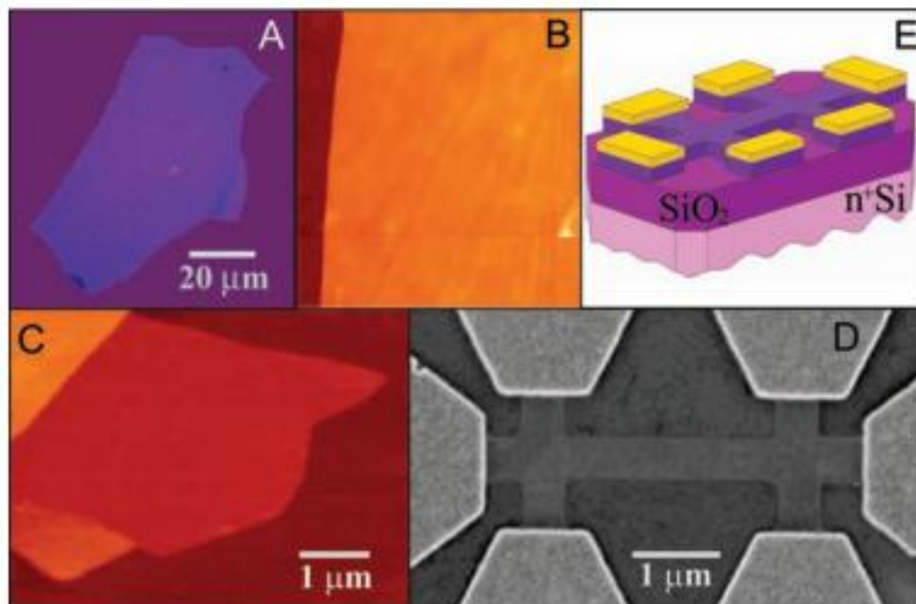


Figure 2-17 Mechanical exfoliated few layers graphene flakes as observed under (a) optical microscope and (b) AFM. (c) AFM image of single layer graphene. (d) SEM image of the graphene FETs fabricated on the SiO_2/Si substrate. (e) The schematic view of the GFET [70].

In 2007, top-gated GFETs has been demonstrated for the first time by M. C. Lemme *et al.* [71] to compare the performance of both types of GFETs. Since bottom-gated GFETs showed unacceptably large parasitic capacitance, the top-gated GFETs structure was then widely adopted, which makes it possible to integrate it with other

components [72]. Figure 2-18 shows the comparison of the top-gated and bottom-gated GFETs. Since then, the electronic properties of top-contact GFETs was widely discussed and reported based on SiO_2, aluminium oxide (Al_2O_3), hafnium oxide (HfO_2) etc [73-78]. Liao *et al*. has reported on the Al_2O_3-based top-gated GFETs with carrier mobility as high as ~23,600 $cm^2V^{-1}s^{-1}$, with more than 10-fold improvement in transconductance in comparison to SiO_2/Si bottom-gated GFETs [74].

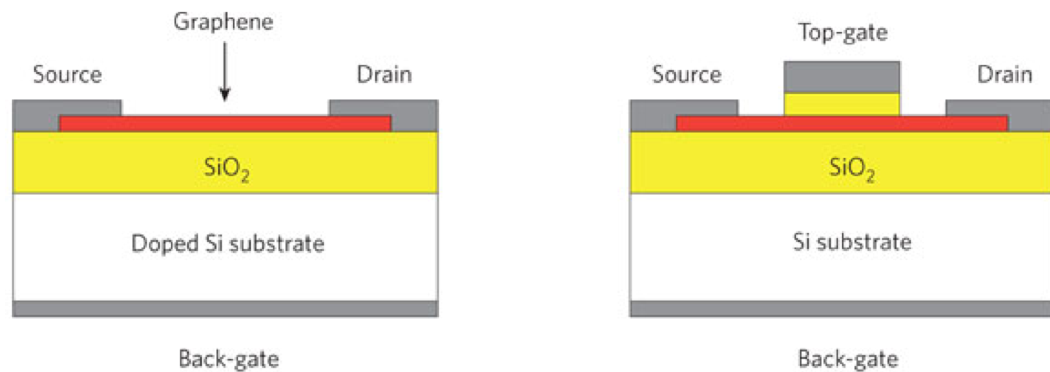


Figure 2-18: Schematic of the top-gated and bottom-gated GFETs. Bottom-gated GFETs make use of the doped-Si substrate as the gate, whereas for top-gated GFETs, the top-gate

One major concern with GFETs is that the I_{on}/I_{off} ratio is much lower than the conventional silicon-based MOSFETs or CNTFETs, make it less realistic for the application of logic devices, with its typical values ranging from 2-20 [72]. This is unavoidable due to the semimetal property of graphene with zero bandgap. By introducing graphene nanoribbons (GNR), it is possible to open up the bandgap of the GFETs to achieve I_{on}/I_{off} ratio of up to 10^4 [79]. Sun *et al*. has reported on the bandgap opening of ~145 meV in GNR through lateral plasma etching, and achieved I_{on}/I_{off} ratio of ~10^5 at room temperature. This corresponds to GNR width of < 10 nm. [80]

2.2 Overview of Mica

Mica is a kind of mineral available in the nature which is being used by the human since the ancient times for different purposes. It is a kind of complex aluminosilicate mineral with chemical formula of $X_2Y_{4\text{-}6}Z_8O_{20}(OH,F)_4$, in which X is K, Na, or Ca or less commonly Ba, Rb, or Cs; Y is Al, Mg, Fe or less commonly Mn, Cr, Ti, Li, etc; Z is Si or Al but may also include Fe^{3+} or Ti [81]. The most widely used mica, muscovite mica, has the chemical formula of $K_2Al_4(Si_6Al_2O_{20})(F,OH)_4$. The crystal structure of muscovite mica can be seen in Figure 2-19.

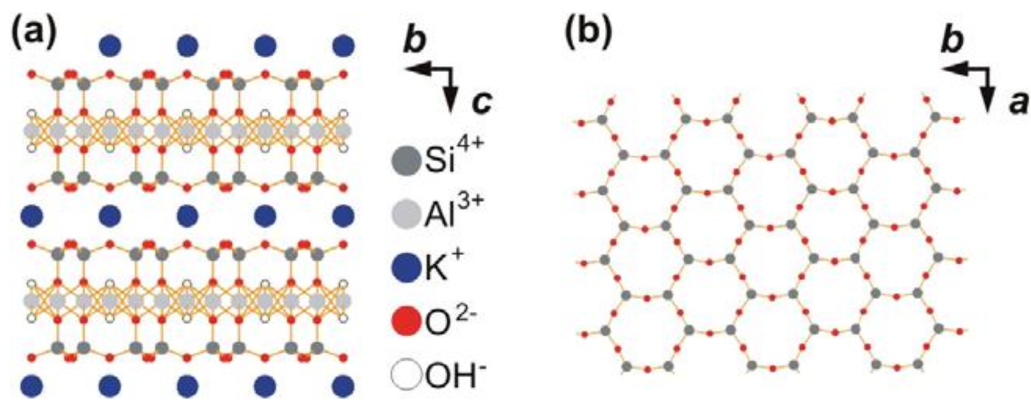


Figure 2-19: The crystal structure of muscovite mica. On {001} planes, vector a and b are used to define the plane, while vector c is the vector normal to the surface. (a) Side view of the crystal structure of muscovite mica. Each aluminosilicate layers were separated by potassium ions. (b) Top view of the muscovite mica {001} surface. The hexagonal atomic structure consists of Si (with Al atoms as the minor elements) and O atoms [82, 83].

Due to the unique atomic structure, mica has perfect cleavages parallel to {001} plane. This property of mica allows it to be cleaved down to a few atomic layers which at the same time still maintain atomically flat and chemically stable surface [82]. It can be seen in Figure 2-19 (a) that there is an interlayer of potassium ions (K+) in between the negatively charged aluminosilicate layers. Since the bonding between these layers is weaker, they can be broken easily, allowing the easy cleavage of mica along the plane.

Upon cleavage of the mica layers, potassium ions are distributed on either of the surfaces randomly.

The lattice top view of mica can be seen in Figure 2-19 (b). It has hexagonal arrangement of Si and O atoms (partly Al), and it is covered partly by potassium ions. The atomically flat surface allows the study of epitaxial growth [82, 83], as well as the study of interaction of water molecules on the mica surface [84, 85]. Because of the charged surface, a layer of airborne contaminants was found to be covering the mica surface [86, 87]. The potassium ions react immediately with the constituents in the air right after cleavage. The water molecules on the mica surface are believed to play an important role as a binding agent to form carbonaceous compounds such as potassium carbonate crystallites [82, 88].

The properties of mica have made it a favoured material for capacitors, transformers, etc. Due to the high dielectric strength, high thermal stability, high electrical resistivity, low power loss/low dielectric loss, perfect cleavage, flexibility and physical and chemical stability at high temperatures and high electric stress, it has been widely used as a very good electrical insulating material for high temperature applications [89]. Physically, it is transparent, optically flat and easily cleaved. Mechanically, it is flexible, elastic, tough and having high tensile strength. Its unique atomic structure allows it to withstand great mechanical pressure perpendicular to the plane. In addition, it is an excellent fire proof that can resist temperature up to 600-900 ^{o}C. Mica has a high chemical stability and is inert to most of the chemicals such as solvents, alkalis, and acids, excluding strong acids such as hydrofluoric acid and sulphuric acids [90]. The dielectric constant of mica is about 8.1 on average, ranging

from 6.4 to 9.3 [91], about a factor of two larger than the dielectric constant of silicon oxide.

Due to its atomically flat surface, mica has been widely used as the standard sample for atomic force microscopy (AFM) calibration [90]. Besides that, the use of mica as the insulator for capacitors has also been extended to field effect transistors. The earlier adoption of mica for the gate dielectric of FETs was by Lu *et al* [90], who has reported on an enhanced carrier mobility of 0.08 cm^2/Vs on mica-based organic FET (OFET) structures with thick mica as the substrate. Following by that, He *et al.* downscaled the gate dielectric thickness down to <100 nm through mechanical exfoliation and fabricated, for the first time, large area organic thin-film FET arrays [92].

Mica, thanks to its atomically flat surface, has been used as a perfect substrate to realise ultra-flat graphene [93]. As such, the interaction of graphene and mica has been widely investigated. Xu *et al.* has reported that graphene helps to visualise the first water adlayers on mica at ambient condition [84]. The interfacial water was reported to dope graphene positively, and the observation was experimentally confirmed through Raman spectroscopy [94], refer to Figure 2-20.

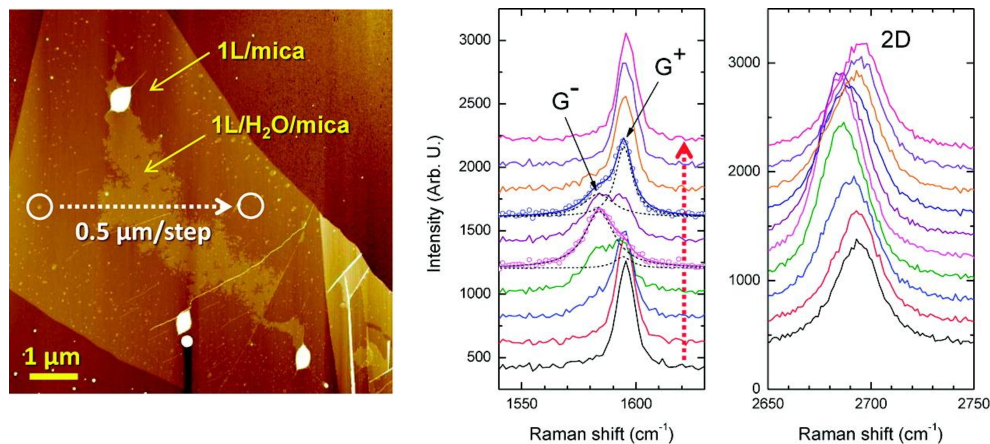


Figure 2-20: Atomic force microscopy image of graphene on mica showing the trapped water adlayers (left) and the Raman spectra (right) showing the Raman shift due to the hole-doping effect [94].

CHAPTER 3: Study of Contrast Spectroscopy of Ultra-thin Mica Flakes

In this chapter, the issue of locating and characterizing mica flakes on SiO_2/silicon substrates is addressed. A contrast spectroscopy based on Fresnel's calculation was implemented on the optical microscope to predict mica flakes thickness that is confirmed using an atomic force microscopy. The first section will give an introduction to mica flakes and the characterization processes. Next, the mathematical background was briefly introduced and discussed for the contrast spectroscopy. Experimental observations are compared with the calculated contrast spectroscopy.

3.1 Introduction

2D materials have been attracting great interest after successful realization of graphene in 2004 [23]. Due to the extraordinary and remarkable electrical properties of graphene monolayer as discussed in Chapter 2, thousands of remarkably studies have been carried out. In the early stage, most graphene was fabricated using the famous micromechanical exfoliation method (also known as the "Scotch tape method"), in which natural graphite was placed on a sticky tape following by folding and peeling the tape repeatedly, resulting in single-layer graphene flakes. This method is well known due to their simplicity, cost effective and yet able to provide extremely high quality graphene flakes. Therefore, this method is widely adapted and employed to study other

2D materials as well, for example, boron nitride (BN), MoS_2, etc. This technique was applied for achieving thin mica flakes in our studies here.

In fact, by using the micromechanical exfoliation method, mica and graphene flakes of different sizes and thicknesses can be obtained. They are randomly distributed over the substrates, and only a small fraction of those flakes are atomically thin, i.e. single or few layers. After transferring them from the tape onto the substrates, it is extremely difficult to locate the monolayer 2-D flakes on the substrates. Although modern characterization techniques such as atomic force microscopy (AFM) and scanning tunnelling microscopy (STM) are capable of identifying single layer graphene, the high equipment cost and low throughput make the searching of single layer graphene less productive. In such, the most robust way to locate a single layer graphene is to observe them directly under an optical microscope. The physics behind originates from the Fabry Perot resonator, in which the graphene layer and the underneath epilayers/substrates (here, SiO_2 was used) are treated as a parallel surface and light interference occurs between layers. Due to different light propagation paths that are caused by different layer thickness, the relative phase difference changed also. These variations on thickness of a fraction of wavelength interfered constructively or destructively which caused light enhancement/suppression on particular wavelengths, resulting in color difference for different flakes, which can be differentiated easily by bare eyes. It was observed and reported that single layer graphene exhibited different color contrasts on silicon oxide substrates of different thickness, leading to the investigation of silicon oxide thickness dependence contrast spectroscopy of graphene.

It was reported that monolayer graphene on 90 nm and 285 nm thick SiO_2/Si substrates exhibited a good optical contrast. Using an optical microscope, Ni *et. al.*

characterized 1 to 4 layered graphene and correlated the results using AFM and Raman spectroscopy, showing the feasibility of using optical microscope to characterize two dimensional nanomaterials. Figure 3-1 presents the contrast of few layer graphene under an optical microscope. The clear color and contrast difference on different graphene thickness can be observed clearly.

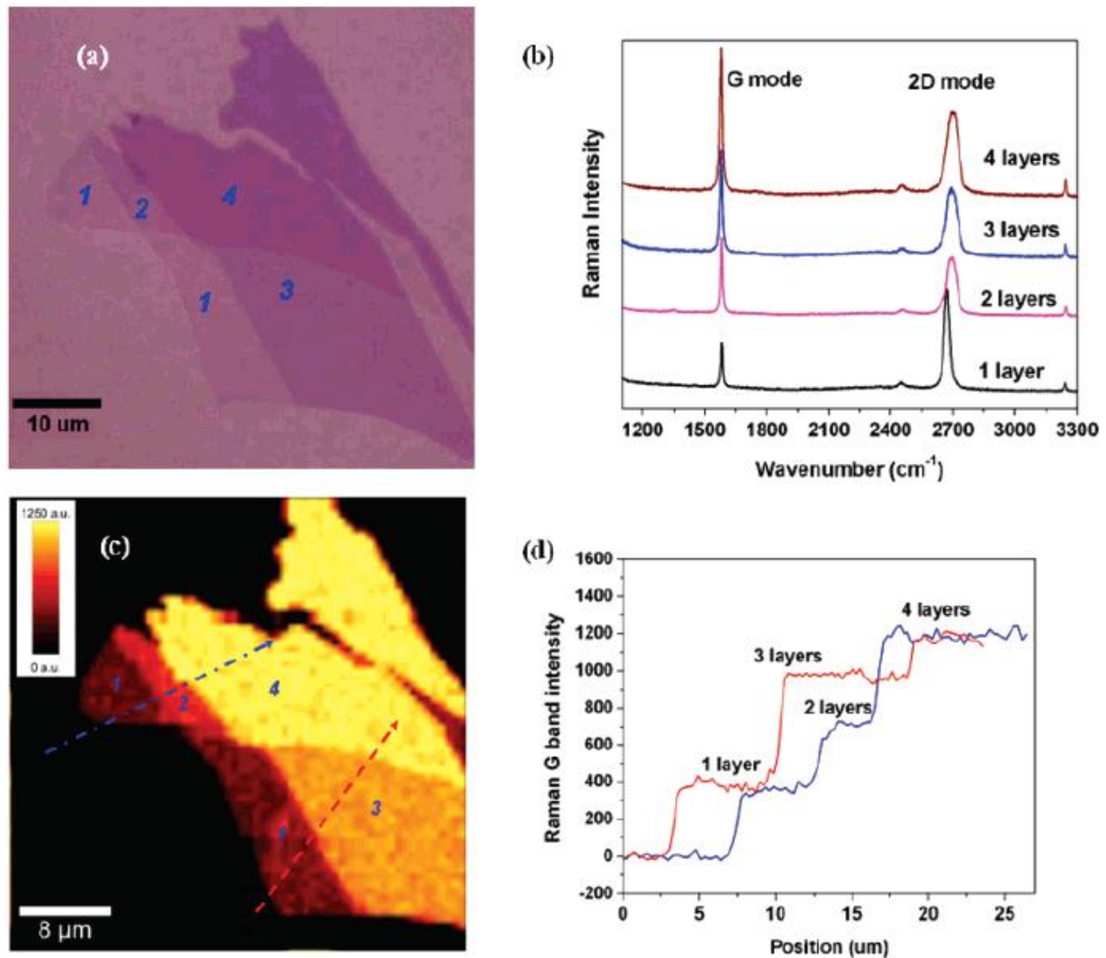


Figure 3-1: (a) Optical image of graphene of 1, 2, 3 and 4 layers, as indicated by blue numbers. (b) Raman spectroscopy as a function of the thickness. (c) Raman mapping of the graphene flake by the intensity of G band. (d) AFM measurement of the graphene flake [95].

Here a similar methodology has been used to study the reflection effect of light from thin mica flakes on SiO_2/Si substrates.

Mica, one of the abundant natural minerals on earth, is getting intensive attention in microelectronics field recently. Lu *et al.* and Matsumoto *et al.* employed mica in OFETs structure and achieved significant improvement on carrier mobility [90, 96]. Recently, mica was reported to be used as a good alternative substrate for graphene. Ripple-free graphene on mica was demonstrated. With their intrinsic high dielectric strength (0.1-1 V/nm), high thermal stability and high electrical resistivity, thin mica can be employed as the gate dielectric materials for CNT and graphene based electronic devices.

In field effect transistors (FETs), the gate dielectric thickness is one of the key parameter to define the gate control capability. Therefore, obtaining thin mica flakes and determining their thickness become critical. As mica is highly transparent, observation of mica under optical microscope is more challenging in comparison to graphene due to the low contrast of mica on SiO_2/Si. The high transparency of mica is due to its large optical bandgap of 10.5 eV. Therefore, it does not absorb light in the visible window. This intrinsic property of mica has made the determination of mica thickness using an optical microscope much more challenging. In the following part, the technical background of the contrast spectroscopy and how to characterize the mica thickness by observing the color bands on the mica flakes will be provided.

3.2 Theoretical Background and Methodology

As the thickness determination of ultra-thin mica flakes on SiO_2/Si substrates using atomic force microscopy (AFM) or Raman spectroscopy is a time consuming and inefficient process, it is critical to investigate the contrast of mica on SiO_2/Si substrates

and identifying the thickness of ultra-thin mica flakes using an optical microscope. The contrast spectroscopy of mica on different thickness of SiO_2/Si substrate under different light wavelength based on Fresnel's equations has been constructed.

The contrast spectroscopy is calculated by assuming normal incidence of the light from air onto the tri-layer system (flat two-dimensional mica/silicon oxide/silicon) as shown in Figure 3-2. However, the analysis can be applicable to other 2-D material, like graphene, boron nitride, MoS_2, etc. As the light passes through the thin mica, it is reflected partially at the air/mica, mica/SiO_2 and SiO_2/Si interfaces. Due to different optical paths caused by mica and silicon dioxide, these three reflected lights interfere each other and the interference will enhance/suppressed certain wavelength, causing a large contrast in different colors which can then be identified by human eyes. Roddaro *et al.* has claimed that the interference of this scenario is due to the amplitude modulation of the reflected lights instead of the phase shift [97].

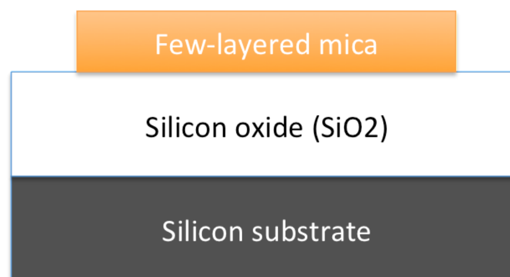


Figure 3-2 : The tri-layer system of mica/SiO_2/Si used in contrast spectroscopy calculation.

In order to optimize the conditions for the best inspection of ultra-thin mica, the contrast spectroscopy for mica/SiO_2/Si system is analysed based on Fresnel's equation, which had been proved to be valid even for an atomic thick graphene on SiO_2/Si substrates. In the simulation, the incident light from the air is assumed to be normal to mica/SiO_2/Si. Given that the air, mica, SiO_2 and thick Si are Medium 0, 1, 2 and 3,

respectively, the reflected light intensity at the particular wavelength can be expressed as:

$$R(\lambda) = |\frac{r_1 e^{i(\phi_1+\phi_2)} + r_2 e^{-i(\phi_1-\phi_2)} + r_3 e^{-i(\phi_1+\phi_2)} + r_1 r_2 r_3 e^{i(\phi_1-\phi_2)}}{e^{i(\phi_1+\phi_2)} + r_1 r_2 e^{-i(\phi_1-\phi_2)} + r_1 r_3 e^{-i(\phi_1+\phi_2)} + r_2 r_3 e^{i(\phi_1-\phi_2)}}|^2 \tag{4.1}$$

where λ is the wavelength of the inspection light. $\phi_1=2\pi n_1 d_1/\lambda$ and $\phi_2=2\pi n_2 d_2/\lambda$ are the phase shift due to the light passing through mica and SiO_2 film, respectively. d_1 and d_2 are the thickness of mica and SiO_2 film. r_1, r_2, r_3 are the relative indices of refraction at the top mica surface, the interface between the mica and SiO_2 and between SiO_2 and Si substrate, respectively, having the following expression:

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \tag{4.2}$$

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{4.3}$$

$$r_3 = \frac{n_2 - n_3}{n_2 + n_3} \tag{4.4}$$

where n_0, n_1, n_2 and n_3 are the reflective index of air, mica, SiO_2 and thick Si, respectively. The contrast of the system can be determined by:

$$C = \frac{R_0(\lambda) - R(\lambda)}{R_0(\lambda)} \tag{4.5}$$

where $R_0(\lambda)$ is the reflected light intensity in absence of mica (or d_1=0). In our simulation, the following are being used: n_0=1, n_1=1.56 [98], n_2=1.47 and n_3=5.6-0.4i [99].

Figure 3-3 shows the contrast spectroscopy of 10 nm thick mica/SiO_2/Si system. The x-axis denotes the illumination wavelength varied from ultraviolet (~400 nm) to

infrared (700 nm), whereas the y-axis denotes the SiO_2 thickness ranging from 0 to 1000 nm. In Figure 3-3, red color bar represents higher contrast value, i.e. the color difference is more significant for the mica on the SiO_2/Si substrate (up to 30-35%). On the other hand, blue color bar shows a lower contrast. It can be seen that the overall contrast is rather small in the studied system for mica, in contrast to the contrast spectroscopy of graphene in Figure 3-4, due to small refractive index difference between mica and SiO_2 [82]. It can be seen that the contrast of 9 layers of graphene on 285 nm SiO_2/Si substrate can be as high as 50%. The highest contrast of 10 nm thick mica (~10-layer thick mica) is only about 35% in the wavelength between 400 nm and 450 nm on 200 nm thick SiO_2.

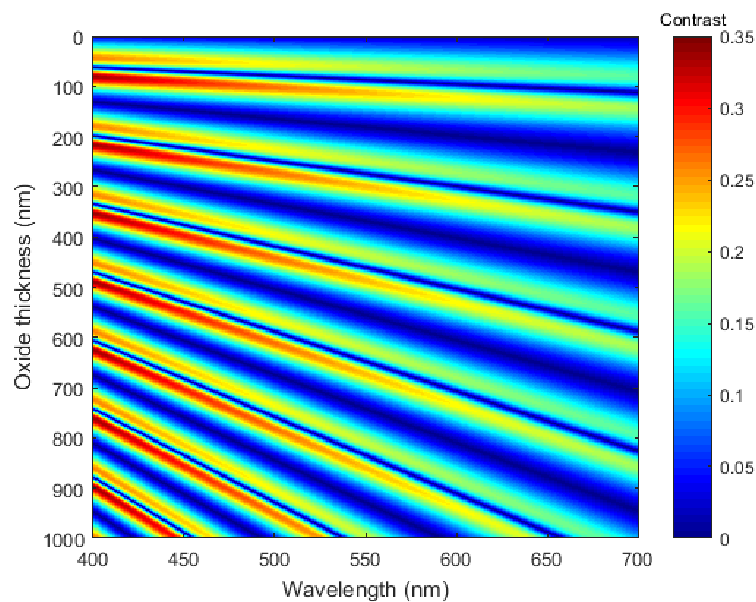


Figure 3-3 : Calculated contrast for 10 nm thick mica/SiO_2/Si system as a function of oxide thickness and wavelength. The red color band indicates the high contrast, while the blue color indicates low contrast. [100]

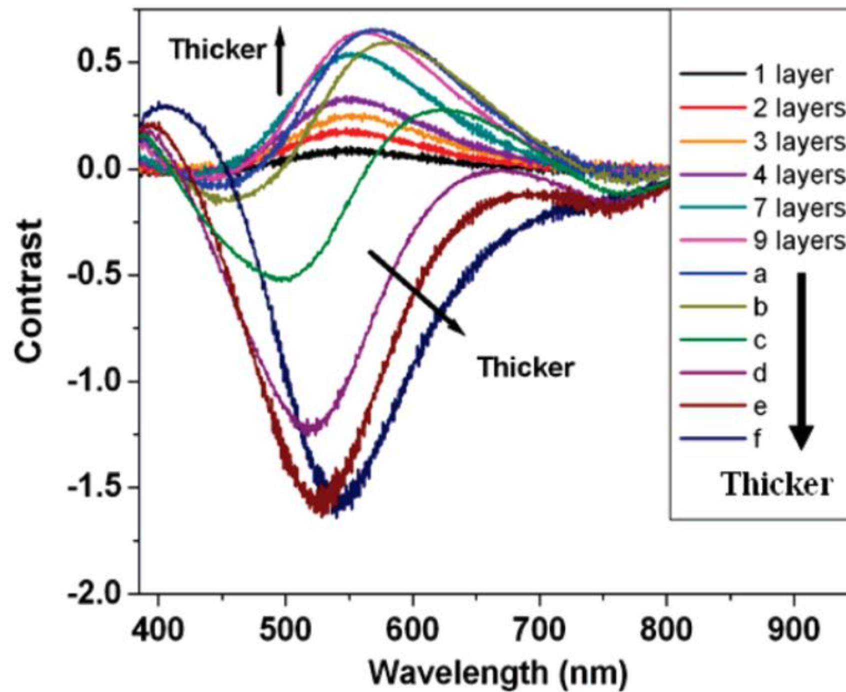


Figure 3-4 : The contrast spectroscope of graphene sheets with different thickness [95].

To further study the mica/SiO_2/Si tri-layer contrast, the contrast of single- and few-layered mica (1 to 3 nm) on 200, 285 and 300 nm thick SiO_2/Si substrate were extracted and replotted in Figure 3-5. The contrast spectra of the single- and few-layer mica on 300 nm thick SiO_2/Si substrate are reasonably consistent with the value reported by Castellanos-Gomez *et al [101]*. It can be observed that the maximum contrast of 1-3 nm mica is in the range of less than 8%, in contrast to the 30-35% of 10 nm mica. This observation suggests that the contrast drops significantly with reducing layer number of the mica flake. Our simulation result shows that the contrast of single-layer mica (1 nm) remains relatively low for all the SiO_2 thickness ranging from 1 to 300 nm. The peak contrast of the monolayer mica is only about 3% under UV-blue light (400 - 430 nm) illumination for 200 nm thick SiO_2/Si substrate, which is challenging to be identified by bare eyes under an optical microscope. In our prediction, mica/SiO_2 (200 nm)/Si tri-layer gives a peak positive contrast under 440 - 450 nm light illumination and shows

weak positive contrast at red (620 - 630 nm) window. In comparison, mica/SiO_2 (285 nm)/Si substrate gives a peak negative contrast under green light (520 - 530 nm) illumination and a peak positive contrast at 620 - 630 nm window. Among these three thicknesses, 200 nm thick SiO_2/Si substrate is favourable for single- and few-layer mica, due to the highest achievable contrast (8%) in the visible light window. It is worth to note that although 285 nm and 300 nm thick SiO_2/Si substrates cause a smaller contrast compared to the 200 nm thick SiO_2, they showed pretty good contrast at around 520 nm and 550 nm, which is most sensitive to human eyes.

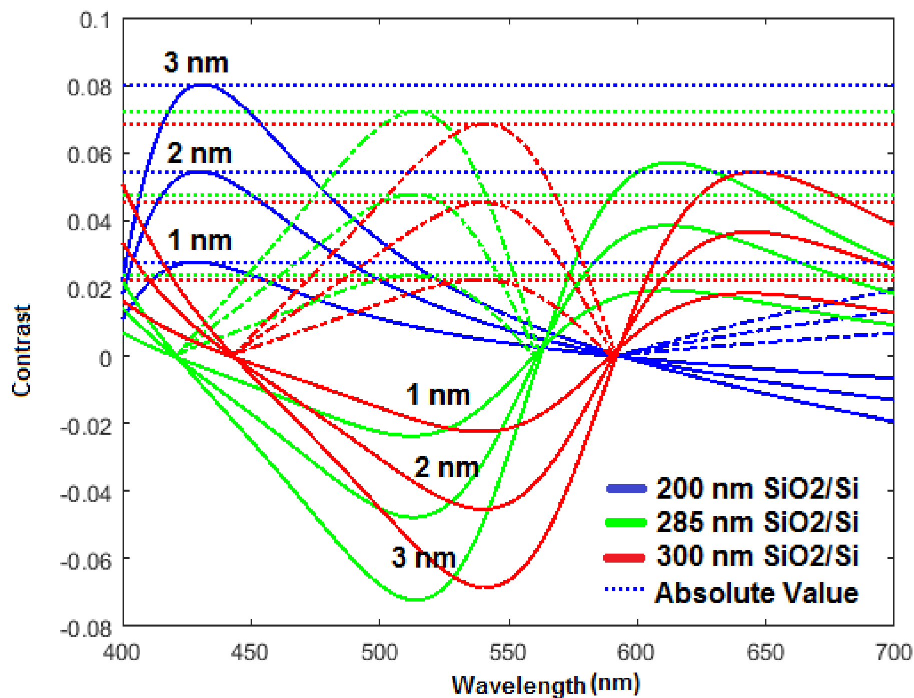


Figure 3-5 Extracted contrast of few layered mica on 200 nm, 285 nm and 300 nm thick silicon oxide/ silicon substrate [100].

On top of that, since most of our mica-based devices consist of mica/titanium (Ti) gate/SiO_2/Si quadruple-layers, the contrast spectroscopy of such system was studied. The system can be simplified as a mica/native oxide (SiO_2)/Ti tri-layers system since the penetration of light through the titanium gate is negligible. Figure 3-6 shows the

calculated contrast for a 10 nm mica/SiO_2/Ti trilayers system. In contrast to 10 nm mica/SiO_2/Si trilayers system, the contrast is relatively lower. In actual case, the native oxide on Ti gate is much thinner and it was assumed to be 2 nm for our simulation. Figure 3-7 shows the calculated contrast of few layered mica on the 2 nm SiO_2/Ti. For 3 nm mica, the contrast is significantly low at ~2.2% (0.022), in contrast to the ~8% of 3 nm mica on 200 nm SiO_2/Si substrate. This shows that it is extremely challenging to identify mica on titanium gate with bare eyes under optical microscope. In our experiments, in most cases, the identification of mica flakes is based on the contrast of mica flakes given by the SiO_2/Si substrate, not by the SiO_2/Ti gate. The details of the fabrication of mica-based FETs will be discussed in Chapter 4 and Chapter 5.

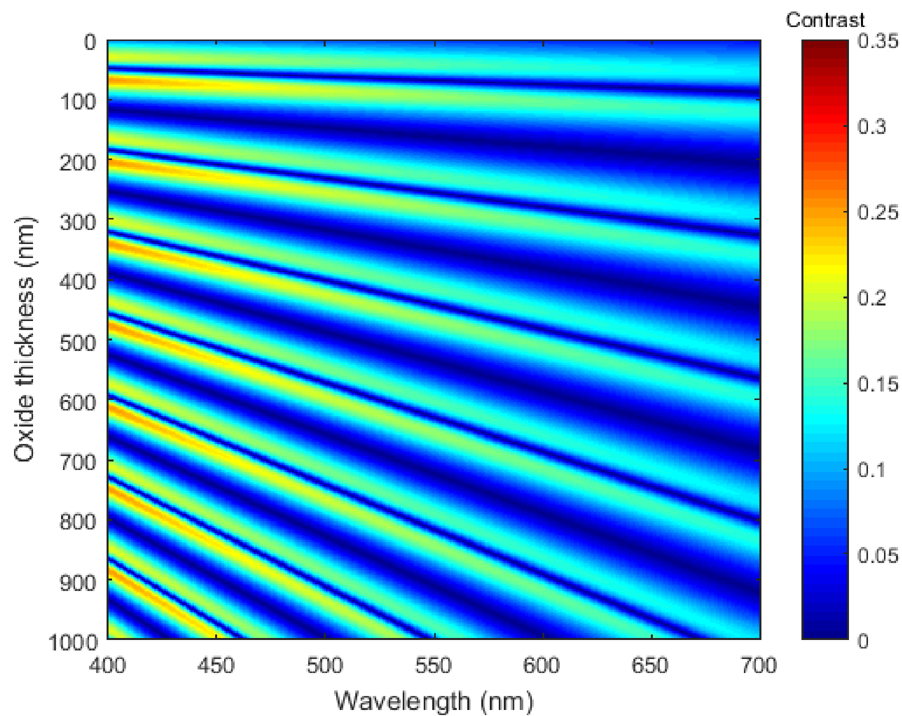


Figure 3-6: Calculated contrast for 10 nm thick mica/SiO_2/Ti system as a function of oxide thickness and wavelength. The red color band indicates the high contrast, while the blue color indicates low contrast.

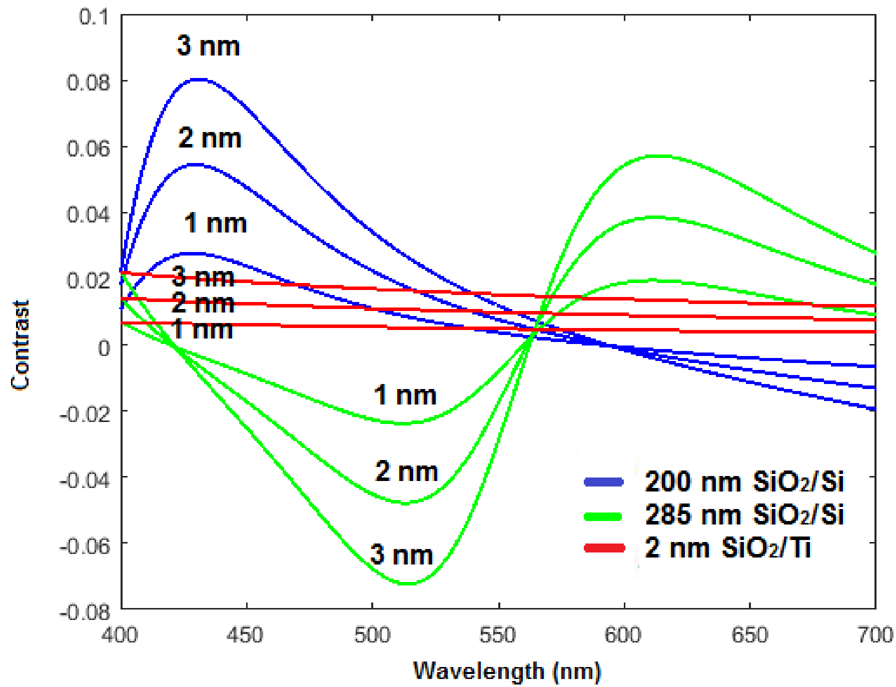


Figure 3-7: Extracted contrast of few layered mica on 2 nm silicon oxide/titanium substrate, in comparison to few layered mica on 200 nm and 285 nm thick silicon oxide/silicon substrate.

In order to verify the calculation, experiments were carried out by placing several mica flakes of different thicknesses on the 200 nm and 285 nm SiO_2/Si substrate for characterization under an optical microscope. In our experiment, mechanical exfoliation i.e. Scotch tape method was employed to produce mica on SiO_2/Si samples. This is a widely used method to fabricate graphene in the lab due to its simplicity and cost effectiveness. First, standard cleaning process of the substrates was carried out to ensure the surface is clean and free of particles. The samples were cleaned by ultrasonication in acetone for 30 minutes, before being treated in piranha solution (mixture of sulfuric acid and hydrogen peroxide) for another 15 minutes. Next, small piece of natural muscovite mica was cleaved repeatedly by Scotch tape. Subsequently, the Scotch tape was put in contact with the surface of the SiO_2/Si substrate for the transfer of mica.

Finally, randomly distributed mica flakes could be found on the substrate surface for further investigation.

Figure 3-8 shows the comparison of the optical images of two ultra-thin mica flakes on 200 nm and 285 nm thick SiO_2/Si substrates under different colour of light illumination - white, blue, green and red, respectively. Both mica flakes exhibit fair contrasts on both 200 nm and 285 nm thick SiO_2/Si substrates under white light illumination. By AFM measurement, it shows the measured thicknesses of the mica flakes to be 25 nm (~ 25 layers) and 17 nm (~17 layers) respectively. Both flakes have 20 - 30 μm lateral dimension, large enough to be found by naked eye under an optical microscope.

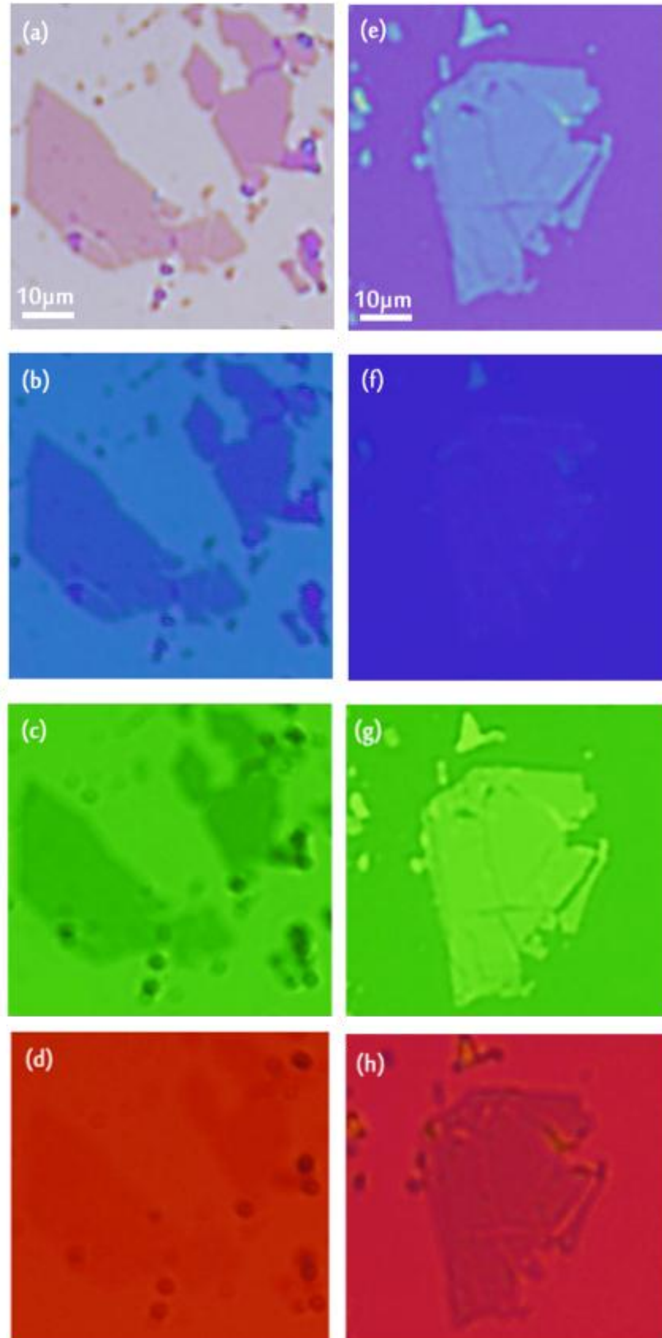


Figure 3-8: Optical images of mica flake of 25 nm thickness on 200 nm thick SiO_2/Si substrate under different light illumination of (a) white light (b) blue light filter (c) green light filter and (d) red light filter, respectively. Optical images of mica flakes of 17 nm on 285 nm SiO_2/Si substrate under (e) white light (f) blue light filter (g) green light filter and (h) red light filter, respectively.

Based on the contrast image of Figure 3-8, it was found that mica flakes with lateral size of 20 - 30 μm can be located easily with optical microscope, and they

exhibited an excellent contrast under white light illumination. This is observed on Si substrates with 200 nm (Figure 3-8 (a)) and 285 nm (Figure 3-8 (e)) thick SiO_2, respectively. The thicknesses of the mica flakes are 25 nm and 17 nm respectively, as measured by AFM, which represents 25 and 17 layers of mica respectively.

From the optical images, one could see that the mica on 200 nm SiO_2/Si substrate showed a higher positive contrast (i.e. mica flake was darker than the SiO_2) under blue light and green light illumination (Figure 3-8 (a)-(b)), in comparison to red light illumination (Figure 3-8 (c)). This is different from the observation on 285 nm thick SiO_2/Si substrate, which it showed a smaller negative contrast under green light illumination (Figure 3-8 (g)) compared to blue light illumination (Figure 3-8 (f)), hence, mica flake was brighter than the $SiO_{2.}$ However, it also differs by showing a positive contrast under red light illumination (Figure 3-8 (h)), in contrast to the negative contrast under blue light and green light illumination. Here, the trend of the positive and negative contrast of mica flakes under blue, green and red light illumination on both 200 nm and 285 nm SiO_2/Si substrate are demonstrated clearly through experiment. Figure 3-9 shows the simulated optical contrast of 25 nm mica on 200 nm SiO_2/Si substrate and 17 nm mica on 285 nm SiO_2/Si substrate for direct comparison with the experimental results. The experimental results show strong consistency to our simulated contrast spectroscopy for SiO_2/Si substrates of 200 nm and 285 nm.

Comparing Figure 3-7: Extracted contrast of few layered mica on 2 nm silicon oxide/titanium substrate, in comparison to few layered mica on 200 nm and 285 nm thick silicon oxide/silicon substrate. with Figure 3-9, the general trend of the optical contrast of 1-3 nm and 10-20 nm mica across 400-700 nm are consistent. However, a slight intensity difference (i.e. change in the contrast) and spectra shift were observed.

Although it is unable to show the numerical accuracy of the simulated contrast in observation, the general trend of the contrast in the major light windows (red, green and blue) is consistent and well aligned for both experimental and simulated results. As the contrast highly relies on the thickness of SiO_2 and the illumination wavelength, this observation is critical as it permits the optimization of the conditions for the direct inspection of single- or few-layer mica under optical microscope. It is clear that the contrast value for single- or few-layer mica has decreased significantly (value of $< 4\%$) as compared to the thick mica flakes. And further reducing the mica thickness from 20 nm to 10 nm would further reduce the contrast significantly, as shown in Figure 3-9.

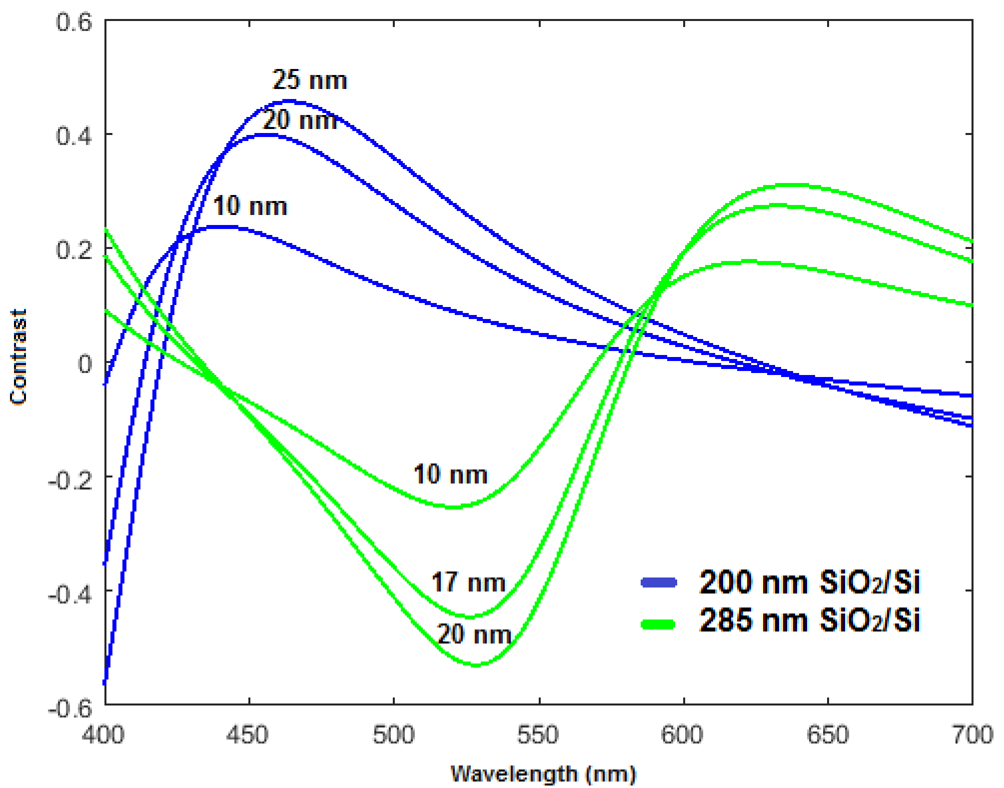


Figure 3-9 : The contrast spectra of 10 nm, 20 nm and 25 nm thick mica on 200 nm SiO_2/Si substrate (blue) and the contrast spectra of 10 nm, 17 nm, and 20 nm thick mica on 285 nm SiO_2/Si substrate (green) [100].

The ultra-thin mica flakes were located experimentally on SiO_2/Si substrates with white light illumination, as shown in Figure 3-10. The optical images of 20 μm lateral size and 4~17 nm thick mica flakes are shown in Figure 3-10 (a). The AFM image of the 4~17 nm thick mica flake were also shown in Figure 3-10 (b). Due to the low contrast difference, the mica flakes of thicknesses less than 20 nm were unable to be differentiated by the optical microscope. However, in this chapter, it was shown, by the mean of simulation and experiments, the factors to improve on the contrast of ultra-thin mica. This includes the optimization of the silicon oxide thickness and the light filter. In this case, the area of interest can be narrowed down and the throughput can be improved subsequently.

The hunt for single or bilayer mica is challenging as shown in previous section, however, it is not impossible, as already been reported by Castellanos-Gomez *et al.* [101]. Nevertheless, the size of single layer mica flakes is usually not larger than 1 x 1 μm^2, in other words, it remains challenging to fabricate a FET on it. It has also been shown that mica gives very weak signal in Raman [101], which means that it is unlikely to search for single or bilayer mica through Raman. Another possible way to identify single or bilayer mica could be by adopting the similar method as proposed by *Li et al.*, which they have developed a universal optical method for fast and reliable identification of 2D materials, such as graphene and MoS_2, by processing the color and grey scale optical images of R, G and B channels to calculate the optical contrast through software ImageJ [102].

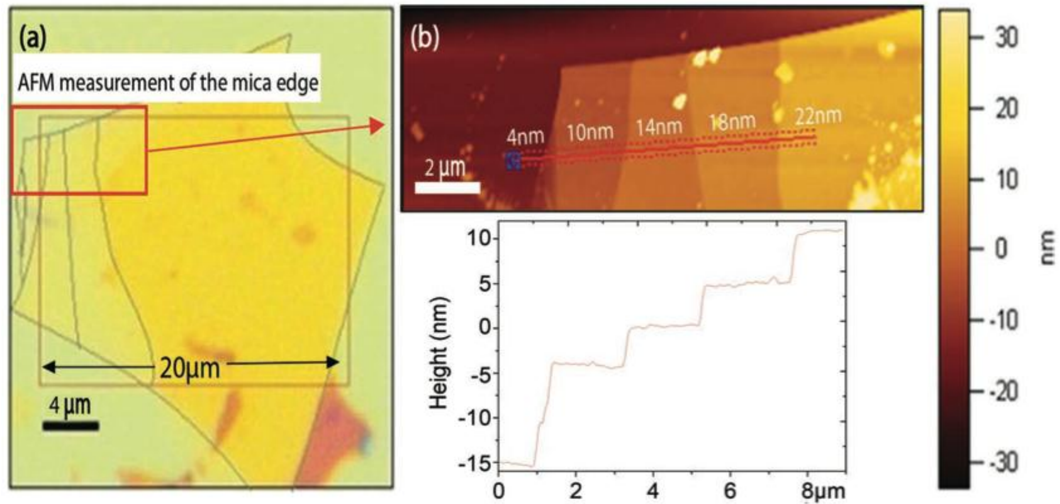


Figure 3-10 : Optical (a) and AFM (b) images of multi-layer mica flakes on 200 nm thick SiO2/Si substrate [100].

3.3 Conclusion

Few-layer mica flakes were characterized based on the correlated contrast spectra calculated using Fresnel's equations. The prediction is well supported by the experimental observation from AFM and optical microscope techniques. The contrast spectroscopy method can differentiate mica flakes down to few nanometers. Further reducing the thickness of mica flakes would result in a greater challenge in the observation based on the optical contrast of the reflected light from mica/SiO_2/silicon systems. This method has opened up a robust way to filtering unwanted area, and therefore improved the AFM throughput significantly.

CHAPTER 4: Ultra-thin and Flat Mica as Gate Dielectric Layer for Carbon Nanotube Field-Effect Transistors

Mica, one of the most abundant natural minerals on earth, has been widely used in electrical and electronic sectors (especially for capacitors, transformers, high frequency and radio frequency) as an insulating material, due to their excellent electrical, mechanical, chemical properties, and their high thermal stability. Mica has been widely known for its atomically flat surface in which it could be used as the substrates of some samples for atomic force microscopy (AFM), which enables the imaging of DNA molecules, protein-DNA complexes and etc. In this chapter, the use of ultra-thin (< 30 nm) and flat mica flakes as the gate dielectric material in carbon nanotube field-effect transistors (CNTFETs) was demonstrated. In this structure, ultra-thin mica remains its atomically flat surface after being transferred onto SiO_2/Si substrate. Ambipolar conduction was observed on the transfer curve of the mica-based CNTFET. In particular, the 28 nm thick mica-based CNTFET has shown sub-threshold slope of ~110 mV/dec, approaching the fundamental limit of 60 mV/dec, whereas the transconductance was 0.13 μS and the carrier mobility was calculated to be 554 cm^2/Vs. In contrast, the performance of mica-based CNTFETs are much greatly improved, as compared to SiO_2 and Si_3N_4-based CNTFETs.

4.1 Introduction

4.1.1 Why mica is important compared to other dielectric materials?

Muscovite mica, one of the commonly found mica, has the general chemical formula of $K_2Al_4Si_6Al_2O_{20}(OH,F)_4$. It has been widely used in the electrical/electronic sector due to their high dielectric strength (0.1-1 V nm^{-1}), high thermal stability, high electrical resistivity, large bandgap (E_g = 10.50 eV), and high chemical resistance under many aqueous, organic, acidic and basic solutions. These advantages have enabled mica to be commonly used in high electric field and high temperature environments, for examples, insulating dielectric layer in the capacitors and other electrical components, high power transformers and radar circuits. Besides that, the dielectric constant of mica could be different depending on the ions attached to it, ranging from 6.4 to 9.3. This is nearly twice/thrice the dielectric constant of SiO_2 [91]. In addition, mica has a perfect basal cleavage parallel to {001} planes, since the potassium ions and aluminosilicate layers are weakly bonded [82]. Because of that, mica can be cleaved down to extremely thin layers through mechanical exfoliation technique, while retaining its atomically flat surface. This method has been commonly used to produce other two-dimensional materials such as graphene, boron nitride (BN), molybdenum dichalcogenide (MoX_2, X = sulphide (S^{2-}), selenide (Se^{2-}), telluride (Te^{2-})), etc. This allow us to produce high quality and thin natural mica without expensive and high tech equipment.

Aside from a high dielectric constant, the atomically flat surface of mica has attracted much attention for the past few years. Fukuma *et al.* [103] and Xu *et al.* [84]

reported the water adlayers's interaction on mica and had studied the dynamic nature of interfacial water on solid surfaces at room temperature. Lu *et al.* [90] and Matsumoto *et al.* [96] fabricated mica-based organic field-effect transistors (OFETs) and successfully achieved improved devices performance with an enhanced carrier mobility. In addition, due to the flat surface of mica, it has been used as the substrate for 2-D materials. It was reported that mica could effectively reduce the commonly found graphene ripples on SiO_2 substrates, and ripple-free ultra-flat graphene on mica has subsequently been reported [93, 104]. Following that, the optical characteristic of mechanical exfoliated mica flakes was carried out by Castellanos-Gomez *et al.* [101]. Mica has outstanding properties with extra emphasis on its high surface flatness and high dielectric constant (6.4~9.3), as well as the high dielectric strength, hence, employing ultra-thin and flat mica as the gate dielectric layer in field effect transistor (FET) could significantly improve the gate control capability compared to commonly-used gate dielectrics. However, prior to this, the electrical characteristics of field-effect transistors using ultra-thin mica (less than 30 nm) as gate dielectrics have remained unclear. This has become the motivation for a more detailed investigation.

4.2 Experimental Details

4.2.1 Mechanical exfoliation (Scotch-tape method) of mica

Similar to graphene and other two-dimensional materials, an ultra-thin mica layer could be isolated from a thick mica flake using the mechanical exfoliation technique [105], due to its perfect basal cleavage along the surface. Prior to the mechanical

exfoliation, the silicon oxide on silicon (SiO_2/Si) substrates were cleaned thoroughly in order to minimize the present of small particles on the surface. Next, the 200 nm thick silicon oxide on silicon (SiO_2/Si) substrates was covered through a photoresist mask. The use of thick photoresist was to protect the substrate surface from possible scratch. Then, the sample substrates were cleaned via ultrasonication in acetone for 30 minutes, followed by drying the substrates using a nitrogen air gun. This process was repeated twice. Then, they were cleaned by piranha solution (a mixture of concentrated sulfuric acid (H_2SO_4) and hydrogen peroxide (H_2O_2)) for 15 minutes to remove the organic residues (photoresist and organic solvent) on the surface. Finally, the substrates were rinsed in de-ionized (DI) water and dried up with nitrogen air gun.

A thick mica sample with a dimension of roughly 5 × 5 mm was cleaved repeatedly by the Scotch tape. The tape was then placed on the clean SiO_2 surface, where freshly cleaved mica flakes were sandwiched between them. By applying a force gently on the tape, the freshly cleaved mica flakes would attach on the SiO_2 surface due to Van der Waal's force. Randomly distributed mica flakes of different thickness on the surface were left upon removal of the Scotch tape. In order to find thin mica flake, the samples were first characterized by contrast spectroscopy under an optical microscope, as described in previous chapter. Atomic force microscopic (AFM) measurement of selected mica flakes was carried out to confirm the thickness.

It was noticed that mica of <20 nm had a low optical contrast. Unlike graphene, it remained challenging to estimate the range of the mica thickness under an optical microscope due to the low contrast. It was also noticed that mica of 4 nm was almost transparent under an optical microscope under white light condition (without using any light filter as discussed in previous chapter).

The surface roughness of SiO_2 substrates and the freshly cleaved mica were evaluated using AFM measurement and the results are shown in Figure 4-1. Figure 4-1(a) shows the topography of a freshly cleaned SiO_2/Si substrate with a 500×500 nm scan size, and root mean square (RMS) roughness of the SiO_2 surface was found to be 275 pm. In comparison, the RMS roughness of the freshly cleaved mica flake on SiO_2/Si substrate (Figure 4-1(c)) was measured to be 78 pm, suggesting that the mica surface was at least three times smoother than the thermally grown SiO_2 [93]. The SiO_2 layer was typically grown by PECVD followed by thermal annealing. During the annealing process the SiO_2 may crystallize and form tiny SiO_2 grains. The imperfection at the grain boundary may cause a rough surface of the SiO_2. Considering low dimensional material such as carbon nanotube in this case, this roughness could reduce the carrier mobility in the CNT channel. In contrast, the surface of the mica is 3 times smoother than that of SiO_2. Taking the superior dielectric constant (2 times larger than the commonly used SiO_2) and dielectric strength of mica into consideration, it is safe to suggest that mica could be a better alternative gate dielectric material for one-dimensional or two-dimensional material based FETs.

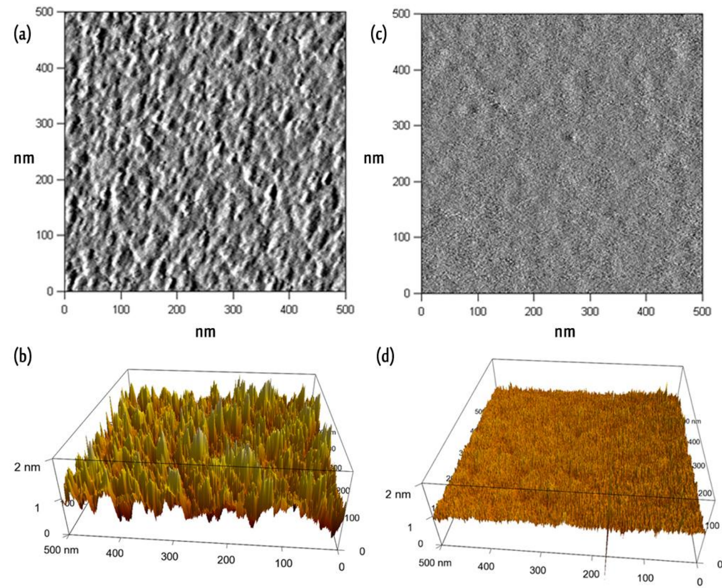


Figure 4-1: Comparison of the surface roughness of SiO2 and mica. (a) AFM image of a SiO2 layer and (b) the three-dimensional representation. (c) AFM image of a freshly cleaved mica flake and (d) the three dimensional representation [100].

4.3 Fabrication of CNTFETs

4.3.1 Top-Contact CNTFETs

Upon confirmation of the thickness, CNTs were placed on top of the mica for CNTFET fabrication. The simplest structure of mica-based CNTFETs was top-contact CNTFETs, in which CNTs were placed on the mica and in between the source and drain as the CNT channel. The CNTs were aligned along the channel region by the alternate current dielectrophoresis (ACDEP) method [106, 107]. The structure of the studied CNTFETs using mica as gate dielectric is shown in Figure 4-2. Thin mica layer, which was placed on top of a Ti/Au bottom gate, was selected. A small photoresist island of size 2 × 8 µm was first defined on the target mica before the deposition of low temperature silicon nitride using plasma-enhanced chemical vapor deposition

(PECVD). After silicon nitride deposition, the photoresist was removed by acetone, leaving a small window open to mica. Hence, the mica/gate lay right at the bottom of the window, as shown in Figure 4-2. This silicon nitride layer is served as additional insulation layer on top of the 200 nm SiO_2 to improve the electrical isolation between the electrodes and the p^{++} silicon. Titanium/gold (Ti/Au) deposited using e-beam evaporator was chosen to be the source and drain electrodes.

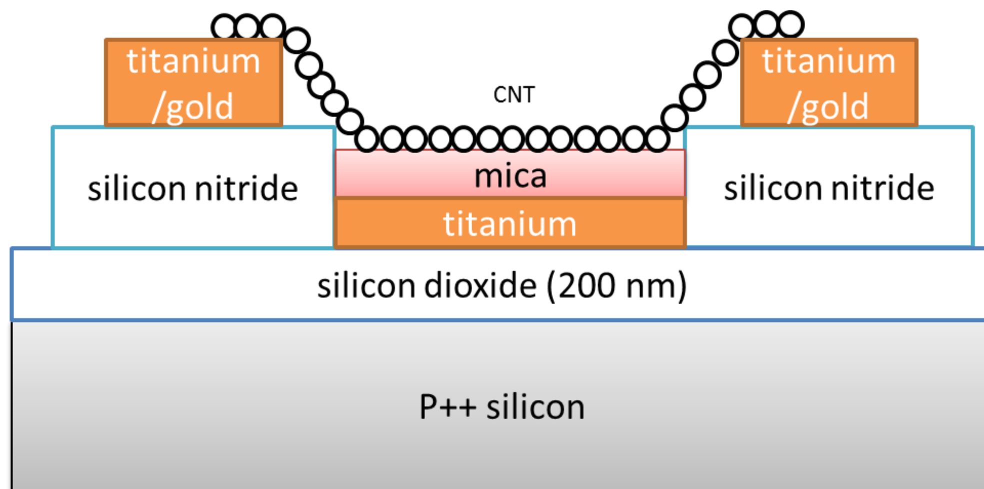


Figure 4-2: The schematic of the side view of the top-contact mica-based CNTFET.

In our experiment, high-purity commercially available SWNTs (95% purity with average diameter of 1.2-1.4 nm) produced by arc-discharge method and purchased from Materials and Electrochemical Research Corporation were employed for the fabrication of top contact mica-based CNTFETs. The SWNTs (~1 mg), which most appeared in the form of CNT bundles, were dissolved in the isopropyl alcohol (IPA) with Triton X-100 as the surfactant to disperse the bundles. ACDEP method was being used to bridge the source and drain electrodes to form the CNTs channel. The frequency and amplitude of the AC current, as well as the time, were optimized depending on the CNT concentration in the suspension – in most case, at the range of frequency ~10 MHz and amplitude of

~5-10 V. A drop of the suspension was placed in the channel area, in between the source and drain electrodes. Due to the dielectrophoresis (DEP) force that was induced by the electrodes, the CNTs in the suspension were aligned along the electric field direction, and subsequently, long CNTs bridged the source and drain electrodes. The formation of CNTs channel was further confirmed by measuring the resistance between the electrodes. In our experiment, the CNTs which bridged the electrodes by ACDEP were hardly a single CNT. In most cases, several CNTs were bundled into a diameter of around 5-10 nm, including metallic and semiconducting CNTs. Existence of metallic CNTs would cause charge leakage and affect the device on-off ratio. In order to realize a good CNTFET with a high on-off ratio, the metallic CNTs between the electrodes were removed by the electrical burnt-off technique [106], in which the gate voltage was applied to switch-off the semiconducting CNTs in the bundle and a large enough source-drain voltage was applied to burnt-off the unwanted metallic SWNTs. A HP4156B semiconductor analyzer was used for this purpose in the ambient. This step was critical to enhance the on/off ratio (I_{ON}/I_{OFF}) of CNTFETs to 10^3-10^4, which the channel was formed by mainly the semiconducting CNTs rather than the undesired metallic CNTs. Finally, the CNTFETs were annealed at 300 ^oC in the ambient environment for 15 min for the removal of the surfactant (Triton X-100). [108]

To that, the simplest form of the top-contact mica-based Schottky barrier-CNTFET, which had a Ti/Au bottom gate and a thin mica gate dielectric layer, was fabricated. Figure 4-3 shows the images under AFM (top) and optical microscope for the top contact mica-based CNTFET. The AFM image shows successful bridging of CNT bundles in between the source-drain electrodes by ACDEP. The transfer

characteristics of this top-contact mica-based CNTFET was included in Figure 4-9 for further discussion.

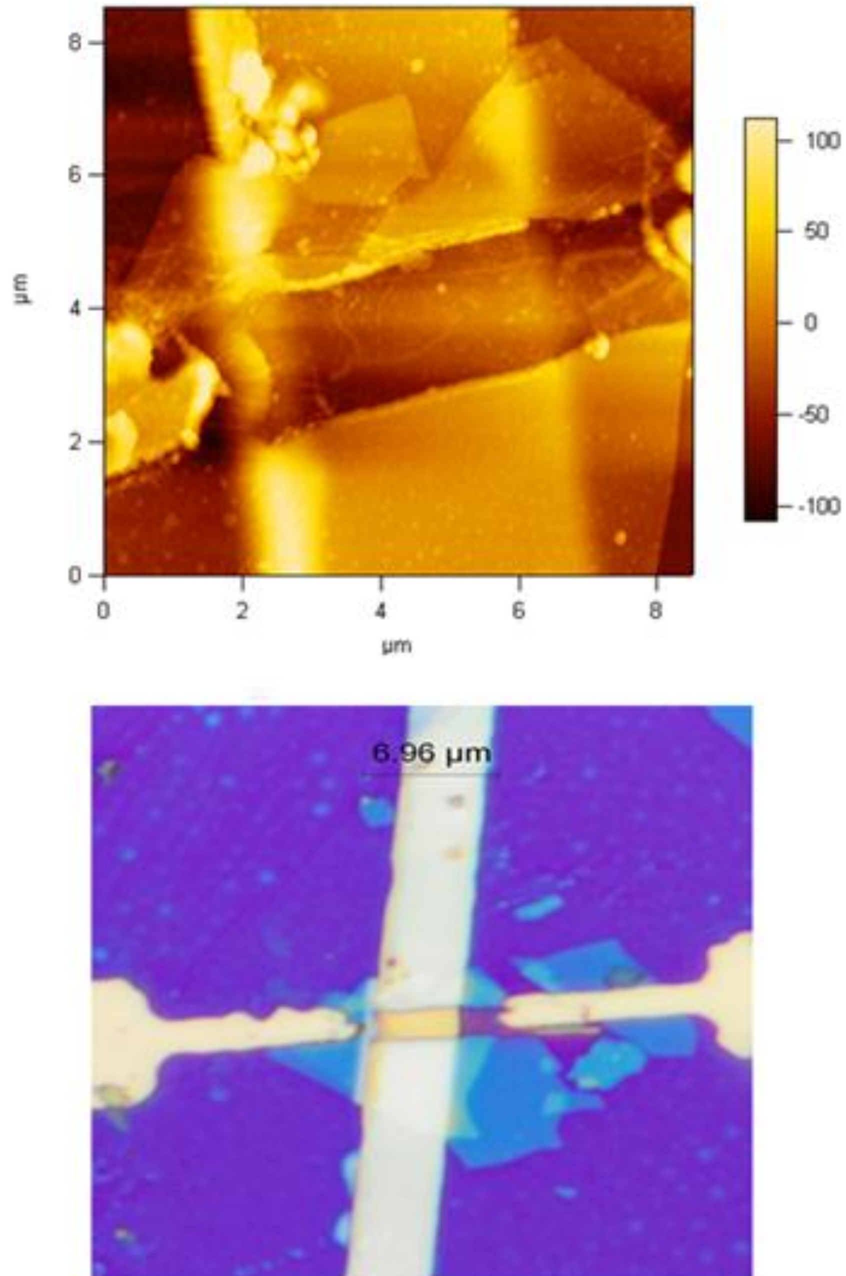


Figure 4-3: AFM (Top) and optical microscope (bottom) image of the ultra-thin mica on an Au/Ti bottom gate between two passivated source/drain electrodes [100].

4.3.2 Bottom-contact CNTFETs

Aside from the top-contact mica-based CNTFETs, bottom-contact mica-based CNTFETs were successfully fabricated. It was found that the electrical contacts between the source/drain and CNTs showed lower contact resistance and had larger contact area than the top-contact mica-based CNTFETs. First of all, the Au/Ti bottom gate was fabricated on the SiO_2/Si substrate, similar to the top-contact CNTFET structure. Secondly, the thin mica flakes were transferred onto the substrate, which only the thin ones on the gate electrodes were used as the gate dielectric layer The thickness of mica flakes was measured by AFM.

For the bottom-contact mica-based CNTFETs, single-walled CNTs (SWCNTs) were grown on a SiO_2/Si substrate by chemical vapor deposition (CVD), with ethanol as carbon source and Ferritin-based Fe as the catalyst [109]. Instead of using ACDEP to bridge CNTs across the source/drain, the CVD-grown CNTs were directly transferred directly from the substrate to the mica flake. Polymethyl-methacrylate (PMMA) polymer was used as the carrier for this purpose. Finally, the source and drain electrodes were deposited. This method ensured that the as-grown CNTs are individual tubes, not the CNT bundles found in the case of solution-based CNTS by ACDEP method. In addition, the density and growth-orientation of the CVD-grown CNTs were optimized by appropriate control of catalyst density, gas flow and CNT growth temperature.

After CNT growth, the samples were spin-coated with polymethyl methacrylate (PMMA) solution and were annealed at 120 ^{o}C for one hour on the hot plate. This was to ensure that the PMMA was in full contact with the CNTs on the substrate for high transfer efficiency. Besides, 120 ^{o}C was reported to be the glass transition temperature

of PMMA at which it reformed and followed the surface morphology of CNTs on SiO_2/Si substrate. Next, the samples were soaked in 1 M potassium hydroxide (KOH) solution for 12 hours so that PMMA-CNT films detached from the SiO_2/Si substrate. The freestanding PMMA-CNT films were rinsed with DI water repeatedly to remove the remaining KOH solution. They were then transferred to the mica/gate/substrate. The samples were annealed at 120 ^{o}C on the hot plate to remove the water trapped between the CNTs and mica for better adhesion. After the PMMA was dissolved and removed with acetone, the CNTs were successfully transferred onto the mica. For better CNTFET performance and high on-off ratio, the active region of a few micrometers is preferred while the CNTs fall outside the active region were removed by RIE etching. Finally, Au/Ti electrodes was deposited. The fabricated bottom contact mica-based CNTFET has the structure as illustrated in Figure 4-4 .

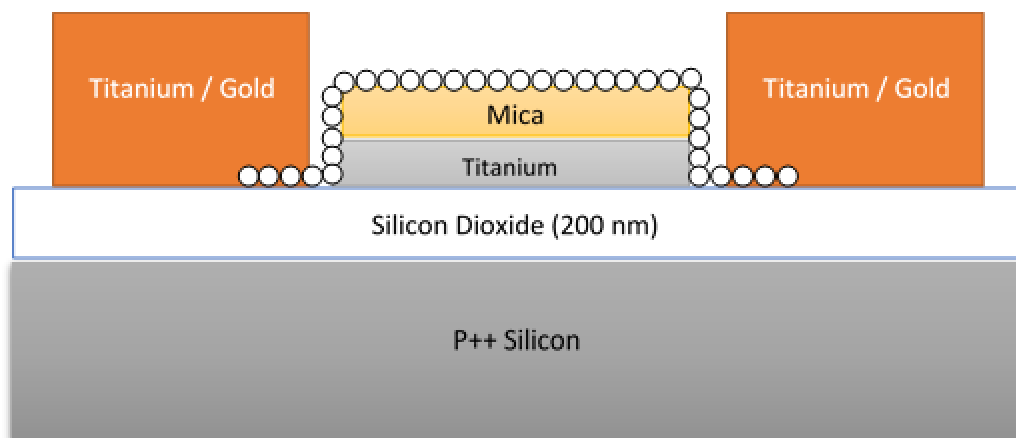


Figure 4-4: The schematic of the side view of the bottom-contact mica-based CNTFET.

4.4 Results and Discussions

In this section, the transport characteristics of the top-contact and bottom-contact mica-based CNTFETs are discussed and compared with silicon nitride and silicon oxide based CNTFETs. The bottom-contact samples were scanned under AFM to inspect the transfer efficiency and the orientation of the CNTs. Figure 4-5 shows the optical microscope and AFM images of the ultra-thin mica and the transferred CNTs network. It can be seen that the orientation of the CNTs was random, forming a CNT network. For discussion purpose, the gate dielectric thicknesses in this dissertation were converted to equivalent silicon oxide thickness (EOT), which indicates the thickness of silicon oxide that would produce the same gate control capability and effect as the high-k material being used as the gate dielectric layer, based on the equation of $EOT = t_{high-k}\left(\frac{k_{SiO_2}}{k_{high-k}}\right)$. For 13 nm mica gate dielectric, the corresponding EOT is 6 nm, which means 6 nm of silicon dioxide with dielectric constant of 3.9 could represent 13 nm of mica with dielectric constant of 8.1. Figure 4-6 shows the optical microscope and AFM images of another mica-based CNTFET, where the mica thickness was 28 nm, corresponding to EOT of 13 nm. An active region of a 3 μm wide strip (the black rectangle) was defined, where unwanted CNTs fall outside the region were removed by RIE etching (see the inset (bottom)).

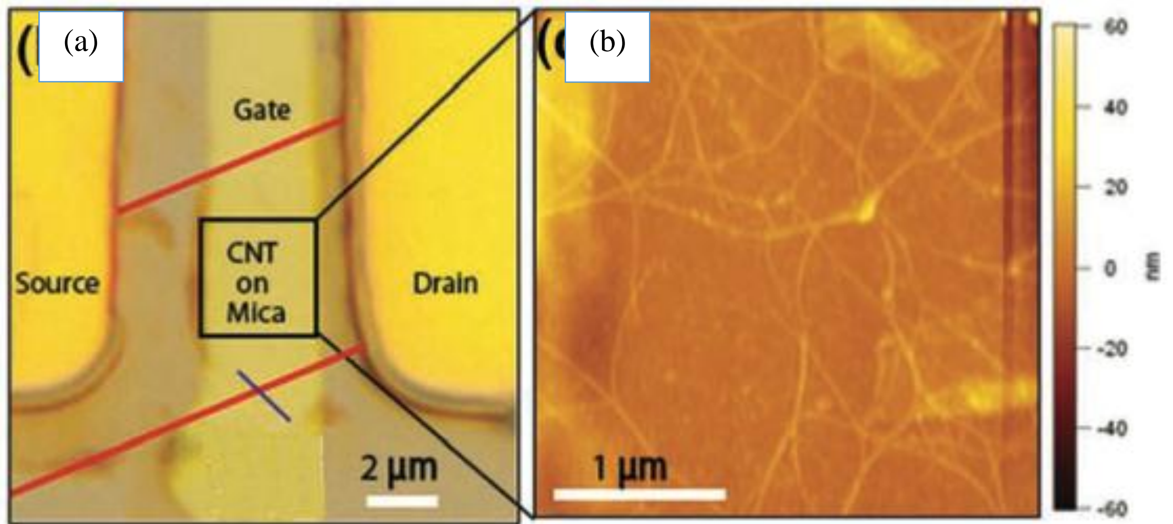


Figure 4-5: (a) Optical microscope and (b) AFM image of the 13 nm bottom-contact ultra-thin mica CNTFET with transferred CNTs network [100].

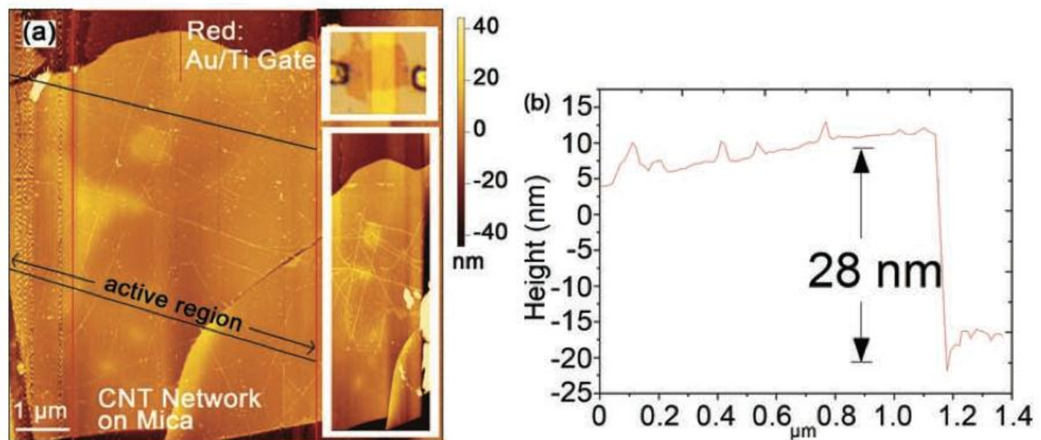


Figure 4-6: The AFM image of the 28 nm bottom-contact ultra-thin mica FET. Top inset shows the optical image of the CNTFET [100].

The transfer characteristics of the 13 nm bottom-contact mica-based CNTFETs are shown in Figure 4-7. The subthreshold slope of the bottom-contact mica-based

CNTFET at V_{DS} = 100 mV is 180 mV/dec, with I_{on} = 0.1 μA and I_{on}/I_{off} of ~10^3. For comparison, the theoretical subthreshold slope of the Si-based MOSFET, which is the lowest possible value for a conventional device to achieve, is 60 mV/dec. As expected, mica exhibits high dielectric strength with a very small gate leakage current. The source drain voltage (V_{DS}) versus output current (I_{DS}) characteristics (from -1.0 to +1.0 V) are shown in Figure 4-8. Comparing I_{DS} of ~500 nA and ~300 nA at V_{GS} = +4V and V_{GS} = -4 V respectively, it can be seen that the CNTFET is in the on-state at both positive and negative V_{GS}, suggesting an ambipolarity behavior. I_{DS} at V_{GS} = +4 V is ~1.67 less times that of I_{DS} at V_{GS} = -4 V, suggesting stronger hole conduction in comparison to electron conduction. It is noted that the I_{DS}-V_{DS} curve does not saturate at the maximum or minimum V_{DS} of ±1.0 V (at V_{GS} = -4 V). This shows that the CNTFET is still operating in its linear mode at V_{DS} = ±1.0 V, but not saturation mode (in saturation mode, the I_{DS} saturates at the saturation current with the increase of the V_{DS}). The maximum I_{DS} in Figure 4-8 is observed to be ~600 nA (0.6 μA), and it is found that the I_{DS} of the fabricated CNTFETs in this dissertation are of the same level, which is much lower than the values as reported elsewhere [32, 50, 110]. One possible explanation could be due to the large parasitic contact resistance of CNTFET (>1 MΩ) [50], which a larger V_{DS} is required to switch the CNTFET to the saturation mode. The contact resistance could be further reduced by thermal annealing at 820 °C for titanium in inert ambient to enhance the coupling between the CNTs and metal contact, as reported by *Martel et al.* [111].

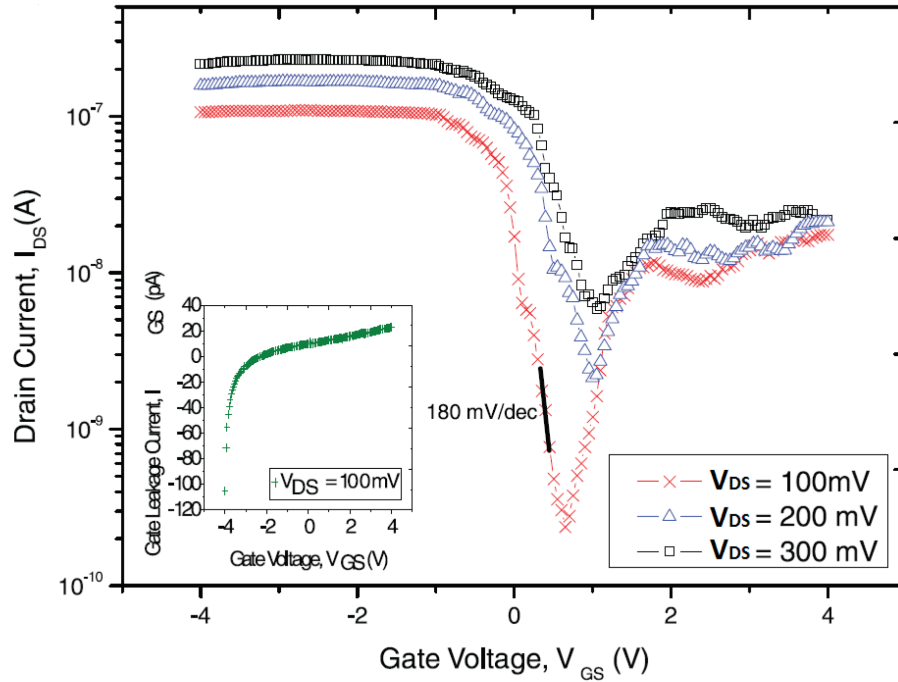


Figure 4-7: The transfer characteristics of the 13 nm bottom-contact mica-based CNTFET for V_{DS} =300 mV, 200 mV and 100 mV. Inset is the gate leakage plot of the device [100].

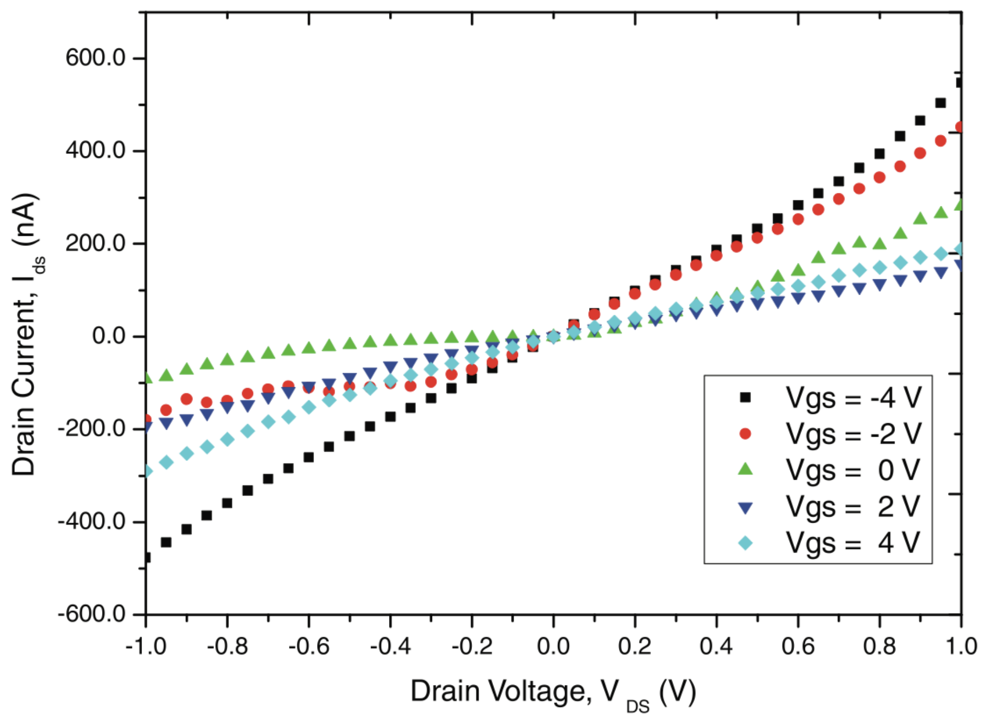


Figure 4-8: The output characteristics for V_{GS} = -4V, -2V, 0V, 2V, 4V ranging from V_{DS} = -1 to 1 V [100].

The inset of the Figure 4-7 shows the gate leakage curve of the device as the function of the gate voltage. It is observed that the gate leakage current is much smaller as compared to V_{DS}. This finding shows that the mica gate layer thickness could be further reduced to enhance the gate control capability and lower subthreshold slope without leading to significant leakage current.

The transfer curve of the 28 nm bottom-contact mica-based CNTFET at V_{DS} = 200 mV is presented in Figure 4-9. For reference, the transfer curve of the top-contact mica-based CNTFET (t_{mica} = 30 nm) and top-contact Si_3N_4-based CNTFET devices ($t_{Si_3N_4}$ = 50 nm) are also included in the figure. The subthreshold slope of the 28 nm mica-based bottom-contact CNTFET (correspond to EOT of 13 nm) was found to be 110 mV/dec while the extracted subthreshold swing (SS) of the top-contact mica-based CNTFET and Si_3N_4-based CNTFET were 610 mV/dec and 3.92 V/dec, respectively. Only taking the top-contact CNTFETs into consideration, the corresponding EOT of 30 nm mica (ε_{mica} = 8.1) and 50 nm Si_3N_4 ($\varepsilon_{Si_3N_4}$ = 6) are 14 nm and 33 nm, respectively. The EOT of Si_3N_4 gate layer in the FET was about two times larger than that of mica based FET. The mica gate dielectric shows superior capability in terms of gate control in comparison to Si_3N_4 gate dielectric layers. This is suggested and seen in the condition where the extracted SS of the mica-based CNTFET is 6-time smaller in comparison to the SS of Si_3N_4-based CNTFET.

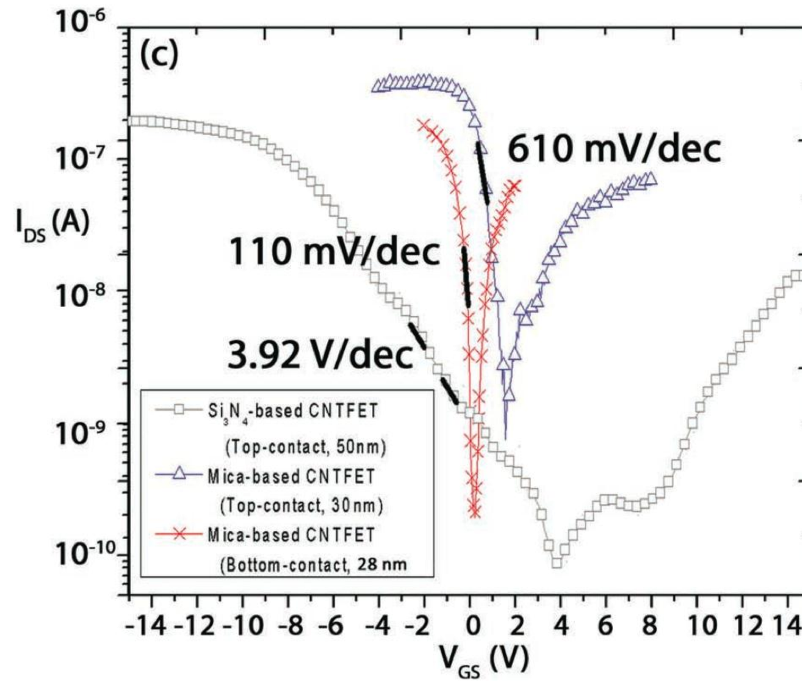


Figure 4-9: The transfer curve of the bottom-gate-bottom-contact (cross) and bottom-gate-top-contact (triangle) mica-based CNTFET, respectively. For comparison, the transfer characteristics of a bottom-gate-top-contact (square) 50 nm thick Si_3N_4-based CNTFET is also shown [100].

The SS of the bottom-contact mica-based CNTFET is observed to be six times smaller, in comparison to top-contact mica-based CNTFET. This observation could be due to several possible reasons. Firstly, the CVD-grown CNTs used in the bottom-contact CNTFET were individual CNTs with an average diameter of approximately 1.4-1.6 nm, as characterized by AFM. Meanwhile, the top-contact CNTFETs fabricated using ACDEP technique consisted of CNT bundles with the bundle diameter as large as ~5-10 nm, connecting the source and drain electrodes. Since the electric field from the gate are being blocked by the outmost CNTs in the bundles, [112] the gate control capability and SS of the top-contact CNTFET is poorer as compared to the bottom-contact CNTFET. Besides that, ultrasonication of CNT solution was required prior to the ACDEP process for the complete dispersion of CNTs in the solution. The

ultrasonication process could damage the CNTs, resulting in deterioration of the carriers transport in the CNTs. Furthermore, adhesion of the CNTs and the metal electrodes for the bottom-contact CNTFET was more intimate for the case of bottom-contact CNTFET since the CNTs are completely covered by the electrodes, a better on-off switching response to the change of gate voltage could be expected.

Previously, Wind *et al.* reported a top-gate CNTFET with subthreshold swing of ~130 mV/dec using 15-20 nm of SiO_2 gate dielectric layer [59]. Franklin *et al.* also demonstrated bottom-gate CNTFET with subthreshold swing of 90-100 mV/dec using 10 nm hafnium oxide (equivalent oxide thickness, EOT ≈ 2 nm) gate dielectric [113]. Our mica-based CNTFET has subthreshold swing of 110 mV/dec for EOT ≈ 13 nm, which is comparable to those reported CNTFETs using high-k dielectric materials. Our devices could be further optimized to achieve a smaller subthreshold swing value if a thinner mica flake (thickness ~ 5-10 nm) were used. In addition to the high dielectric constant, the superior dielectric strength allows mica to be scaled down to a few nanometers thick while maintaining a very small leakage current. Further downscaling of the mica gate layer would further reduce the subthreshold swing of the mica-based CNTFETs.

It is interesting to note that both types of mica-based CNTFETs (top-contact and bottom contact) show ambipolarity, in which, for the top-contact mica-based CNTFET, the CNTs were placed on top of the electrodes (the CNTs were in direct contact with the Au), whereas for the case of bottom-contact mica-based CNTFETS, the CNTs were covered by the Au/Ti electrodes (the CNTs were in direct contact with the Ti). The possibility that the ambipolarity is contributed by different contact mode (top contact or bottom contact) is being ruled out, as ambipolarity are observed in both kind of device

structure. This is different from what was reported by *Cui et al,* which a Au-based CNTFET was reported to be p-type unipolar. *Martel et al* has also reported on the Ti-based unipolar CNTFETs without any passivation layer [114]. However, the conversion from unipolar to ambipolar is achieved with 10 nm SiO_2 passivation layer. It is important to highlight that for our case, the as-fabricated mica-based CNTFETs were not covered by passivation layers. As it can be seen in Figure 4-7 & Figure 4-9, both top-contact and bottom-contact mica-based CNTFETs show strong hole conduction at $-V_{GS}$ and relatively weaker electron conduction at $+V_{GS}$. As such, it is believed that there must be some other factors that contributed consistently to the ambipolarity of the mica-based CNTFETs, without any passivation layer.

This is attributed to the excellent electrostatic field modulation of thin mica gate dielectric, as it has been widely reported that the downscaling or the use of high dielectric constant of the gate dielectric CNTFET leads to the ambipolar conduction, regardless of the Fermi level position of the metal electrodes, due to the thin barriers at the electrodes which are transparent for the injection of the carriers (electrons and holes) into the CNT channels [49, 115-117]. The Fermi level in CNT channel could be efficiently shifted by the gate voltage over the band gap of the CNTs. In addition, it should be pointed out that most of the as-fabricated CNTFETs with SiO_2 gate dielectric prepared by similar processes showed apparent p-type characteristics (without using Triton X-100) [59, 118, 119], probably because of the Schottky barrier height modification at the contacts due to the adsorption of oxygen in air [120] and electron conduction suppression by SiO_2 due to oxygen/water redox couple [119]. The ambipolarity conversion of SiO_2-based CNTFET was reported by Martel *et al.* [49] for the devices passivated with SiO_2 layer and annealed at $800\,^{\circ}C$. In contrast, the

ambipolarity of the mica-based CNTFETs did not need any passivation layer or high temperature annealing. It opens up the possibility of fabricating complementary CNTFETs (i.e. p-type and n-type CNTFETs) for the application in complementary logic [121]. It should be noted that the slightly low electron on-current as compared to the hole on-current may suggest that the Fermi level of the metal electrodes is slightly away from the bandgap center of the semiconducting SWCNTs and near to the valance band, leading to a larger Schottky barrier (SB) for electrons, but smaller for holes [46, 47, 53, 122].

The capacitance of the bottom-contact CNTFET can be estimated based on the cylinder-on-plate model [123]:

$$C_{mica} = \frac{2\pi\varepsilon\varepsilon_0 L}{cosh^{-1}(\frac{r+t_{mica}}{r})} \tag{4.1}$$

where ε is the dielectric constant of mica (here $\varepsilon = 8.1$) [91], L is the CNT channel length (here 9 μm), t_{mica} is the thickness of mica gate dielectric of the bottom-contact CNTFET (t_{mica} = 28 nm), and r is the average radius of CVD-grown CNTs (r = 0.8 nm). The capacitance of the CNTFET C_{mica} was predicted to be 0.95 fF. The transconductance $g_{m,p}$ in the linear region for the p-type branch at V_{ds}=200 mV was calculated to be 0.13 μS using:

$$g_{m,p} = \frac{dI_{DS}}{dV_{GS}} \tag{4.2}$$

and the hole mobility was obtained using the following equation:

$$\mu_h = \frac{dI_{ds}}{dV_{gs}} \times \frac{L^2}{C_{ox}} \times \frac{1}{V_{ds}} \approx 554\ cm^2/Vs \tag{4.3}$$

by assuming that the CNTFET operated in the triode region based on the metal-oxide semiconductor FET model. In addition, the carrier mobility of the mica-based and Si_3N_4-based CNTFETs fabricated using ACDEP method are 137 cm^2/Vs and 15 cm^2/Vs, respectively. The carrier mobility of the mica-based CNTFET is higher than the Si_3N_4-based CNTFET fabricated in the same structure. The higher carrier mobility of the mica-based CNTFET was attributed to the high surface flatness of mica gate dielectric as compared to SiO_2 or/and Si_3N_4 gate dielectric layers. Based on the AFM characterization as discussed before, it was observed that PECVD-grown SiO_2 and Si_3N_4 were in the form of polycrystalline structures and have rough surfaces. There are numbers of scatterers arisen from the trapped charge or physical surface roughness, which could significantly lower down the carrier transport mean free path [44, 124]. In addition, other high-k dielectric material based CNTFETs were also reported to have high concentration of electronic defects which lead to carrier mobility degradation [125-127]. The high surface flatness of mica gate dielectric is favorable for CNTFETs to achieve high carrier mobility.

4.5 Conclusion

Ultra-thin and flat mica flakes were obtained using mechanical exfoliation method. The surface of the mica flakes was found to be atomically flat. The mica flakes were integrated into CNTFET as the gate dielectric layer. The performance of thin mica based CNTFET showed significant improvement in carrier mobility and subthreshold swing compared to SiO_2, Si_3N_4 and HfO_2 based dielectric based CNTFETs. The finding opens up a simple and efficient pathway to the fabrication of high performance thin film field-effect transistors.

CHAPTER 5: Graphene Field Effect Transistors with Mica as Gate Dielectric Layers

In this chapter, mica was presented as an alternative dielectric material for low dimensional electronic devices. In this study, several-nanometer thick mica was incorporated in graphene-based field-effect transistors (GFET) as the gate dielectric materials to study their transport characteristics. It was found that the transfer curve of the GFET using 24 nm thick mica dielectric shows an effective carrier mobility of 2748 cm^2/Vs and a transconductance of 3.36 μS, which are 2-fold and 7-fold larger than the reference device that utilized 40 nm thick SiO_2 as dielectric layer, respectively. This chapter provides an overview of the mica-based GFET.

5.1 Introduction

Graphene has gained a lot of attention since the first discovery due to its high carrier mobility, high thermal conductivity and high mechanical strength, which is claimed to be a promising material for future electronic applications. There are numerous ways to obtain graphene sheets, and the first well-known method is called the Scotch tape method. Subsequently, growing graphene sheet using chemical vapour deposition (CVD) has been widely adapted, due to its capability of producing large area graphene sheet and high yield. In contrast, Scotch tape method only allows the fabrication of graphene of several tens of micrometers, whereas Samsung *et al.* has successfully fabricated large area CVD-growth graphene of several inches [29].

However, a typical CVD-growth graphene sheet exhibits poorer electronic properties as compared to the graphene sheets obtained using the conventional mechanical exfoliation method. Several reasons could account for the poorer electronic properties, such as the electron scattering at the grain boundaries [128, 129], corrugations [130, 131] and the residue caused by the transfer process [132, 133]. While most efforts are focused on the scattering effects on electron transport properties of graphene, one should note that the underlying substrates of the GFET play a significant role to the electrical transport properties, especially for low dimensional materials. Two dimensional materials are highly sensitive to the surrounding environment, such as the underlying substrates and the metal contacts. Hence, choosing a matched substrate for graphene devices become critical as it will strongly affect their performances. However, there are limited studies on the graphene/underlying substrate interaction [134, 135].

285-nm-thick silicon oxide on silicon (SiO_2/Si) substrates has been used as the substrate for graphene-based FET, as this substrate can provide excellent optical contrast under optical microscope investigation when placing graphene sample on top of it [95]. However, it was later on discovered that graphene on SiO_2/Si substrates devices faced inhomogeneous charge distribution and microscopic corrugation issues. The dangling bonds, charged traps, and the roughness of SiO_2 surface are believed to be the primary factors of affecting the carrier mobility of graphene [132]. To address these critical issues, hexagonal boron nitride (h-BN, a two dimensional material) has been investigated recently and reported to be a suitable substrate for graphene-based devices due to its atomically flat surface, free of dangling bonds and small lattice mismatch between h-BN and graphene [136-139]. It is believed that other two dimensional materials could offer similar properties as h-BN, such as muscovite mica.

As discussed in the previous chapters, muscovite mica is an excellent insulating material and widely used in high electric field, high temperature and harsh environments to isolate the electricity. In addition, it has a dielectric constant of 6.4 - 9.3, roughly twice the value of SiO_2 and h-BN [91, 136]. As two-dimensional materials are getting more and more attention, this property of mica is more favorable in comparison to h-BN for downscaling of gate dielectric to achieve excellent gate control capability. Besides that, due to the weak bonding between the potassium ions and aluminosilicate layers, mica can be cleaved along the {001} planes [82], which is similar to other two-dimensional materials such as graphene and h-BN. The atomicially flat surface of mica has often been used as substrate to support materials, including organic semiconductors [90, 96], carbon nanotubes (CNT) [100], graphene [93, 101, 140], etc. It was found that organic semiconductor on mica substrates showed improvement on the carrier mobility [90, 96]. Our previous works successfully demonstrated ultra-thin yet atomically flat mica-based CNT-FETs with improved carrier mobility of 554 cm^2/Vs and subthreshold slope of as small as 110 mV/dec [100]. Chun *et al*. achieved high quality ultra-flat graphene on mica with reduced surface roughness of graphene down to < 25 pm [93], whereas Rudenko *et al.* reported theoretically on the adhesion and electronic properties of graphene on muscovite mica caused by the van der Waals and ionic interaction [104]. The reduced surface roughness and the elimination of intrinsic ripples of graphene that otherwise observed commonly on SiO_2/Si substrates are crucial to achieve high carrier mobility for high switching speed applications.

As high gate control capability and high switching speed performance of transistors can be achieved through thickness reduction of gate dielectric layers, the high dielectric constant and high dielectric strength are the fundamental requirements of a

good dielectric layer. Mica has these excellent properties and meets the requirements so that it could be a good gate dielectric material in addition to h-BN, especially when it is down to a few atomic layers thick. In this chapter, several interesting findings from our ultrathin mica based GEFTs were presented. The electron transport properties of graphene on mica and the performance enhancement of the GFETs in comparison to SiO_2-based GEFTs are presented in details. The electron transport properties of graphene on ultra-thin mica works are reported online [141].

5.2 Experimental Details

5.2.1 Preparation of graphene and mica specimens

Muscovite mica flakes were obtained by mechanical exfoliation of commercially available high quality muscovite mica using the scotch tape method. After that, the mica flakes were transferred onto silicon oxide/silicon substrate where there were pre-defined titanium/gold (Ti/Au) bottom gate electrodes. The 285 nm SiO_2/Si substrate was chosen for better optical contrast of graphene under optical microscope. The thickness of the mica flakes was first identified using optical microscope, before further confirmation through atomic force microscopy (AFM) technique. After confirming the exact location of desired mica thickness, the CVD-grown graphene was placed on top of the mica/Au/Ti/SiO_2/Si sample using polymethyl methacrylate (PMMA) polymer and then patterned into a graphene ribbon.

5.2.2 Graphene field-effect transistor fabrication

Bottom-gated bottom-contact GFET structure was used for this study. To fabricate ultra-thin mica based GFET, Ti/Au (5 nm and 15 nm respectively) bottom gate electrodes were first deposited on the clean 285 nm thick SiO_2/Si substrate using electron beam evaporation technique. Next, the freshly cleaved muscovite mica flakes were transferred onto the substrate. Under optical microscope inspection, the mica flakes were found to be randomly distributed on the substrate and only those mica flakes that cover the bottom gate electrodes entirely were chosen for further GFET fabrication. The mica flakes thickness and surface roughness were analyzed using AFM technique. On the other side, graphene monolayer was grown on a Cu foil using chemical vapour deposition method [142]. With the PMMA-assisted transfer technique [143, 144], the graphene monolayer was transferred onto the mica/Au/Ti/SiO_2/Si sample. The transfer process was critical, including several steps:

(1) Spin-coating of PMMA polymer solution on 1 cm × 1 cm graphene/Cu foil pieces at a speed of 4000 rpm for 60 seconds.

(2) Samples baking at temperature of 180 ^{o}C for 5 minutes to promote the PMMA polymerization.

(3) Dip the samples in ammonium persulfate solution to remove the Cu foil. The PMMA-supported graphene membranes will float on the solution.

(4) Rinse the PMMA-supported graphene membrane with deionized water for several times to ensure the complete removal of ammonium persulfate.

(5) Transfer the PMMA-supported graphene onto the desired sample surface. Here, PMMA-supported graphene was transferred onto the mica flake.

(6) Sample annealing at 180 ^{o}C (the glass transition temperature of PMMA) for 30 minutes in air. PMMA polymer was solidified during the annealing process and the adherence of graphene on the mica was enhanced [145].

(7) Remove the PMMA by immersing the samples in the acetone solution overnight (around 24 hours).

After the graphene flake had been transferred successfully, the active channel region of the GFET was patterned into graphene ribbon using oxygen reactive-ion etching (RIE) method, and the two ends of the graphene ribbon were patterned through photolithography to define the Ti/Au source and drain electrodes. Ti/Au metal alloy was deposited using the e-beam evaporator and GFET fabrication was completed. In this structure, the ultra-thin mica was act as a supporting substrate for graphene to study the electron transport properties of the device. On the other hand, the gate dielectric property of ultrathin mica is also investigated.

Since graphene is extremely sensitive to the surrounding, the use of the chemicals (ammonium persulfate, for example), the transfer polymer (PMMA in this case), the metal electrodes (Ti/Au), the photoresist and etc, could change the property of graphene. Hence, all the mica-based GFETs reported in this chapter were fabricated based on the standard procedure as discussed above to rule out any possible factors that could change the property of graphene unnecessarily.

5.3 Results and Discussions

Figure 5-1 shows the schematic diagram of the ultra-thin mica-based GFET on SiO_2/Si substrate. In this structure, Ti/Au was used as the electrode to provide ohmic contact. Ultra-thin mica was served as gate dielectric material and graphene as the field-effect transistor channel. The structure was built on a 285 nm SiO_2/Si as the substrate.

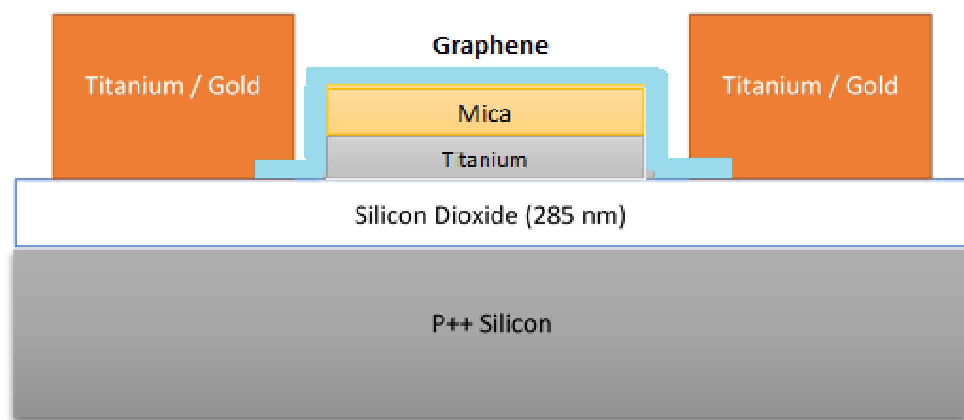


Figure 5-1: Schematic diagram of the ultra-thin mica based GFET as fabricated on 285 nm SiO_2/Si substrate.

The optical image of the mica-based GFET is presented in Figure 5-2. The graphene ribbon with the size of 1.5 µm x 7 µm (marked in red box) was located on the ultra-thin mica (which appeared to be purplish blue) where the ultra-thin mica was sandwiched between the graphene and Ti / Au bottom gate electrode (marked by G). Ti (20 nm) / Au (120 nm) which were deposited by electron beam evaporation and patterned into the source and drain (marked by S and D) at two ends of the graphene ribbons using standard photolithography processes. It was observed that the graphene ribbon generally had low contrast on the mica flake. The graphene ribbon is free from

contamination in the transfer process and the photolithography process. However, ripples (marked by red circle) could still be observed on the graphene ribbon. The graphene ripples were attributed to the wet transfer process involving polymers such as PMMA, as reported widely [131, 146, 147]. In our experiment, PMMA was used in the transfer process, and hence the formation of ripples was unavoidable. Since these unwanted ripples can affect the charge transport of graphene in our study, a gentler and cleaner method which doesn't require polymers (PMMA in our case) can be adopted to transfer the CVD-grown graphene onto the target substrate, such as the direct transfer of graphene method as reported by William Regan *et al* [148].

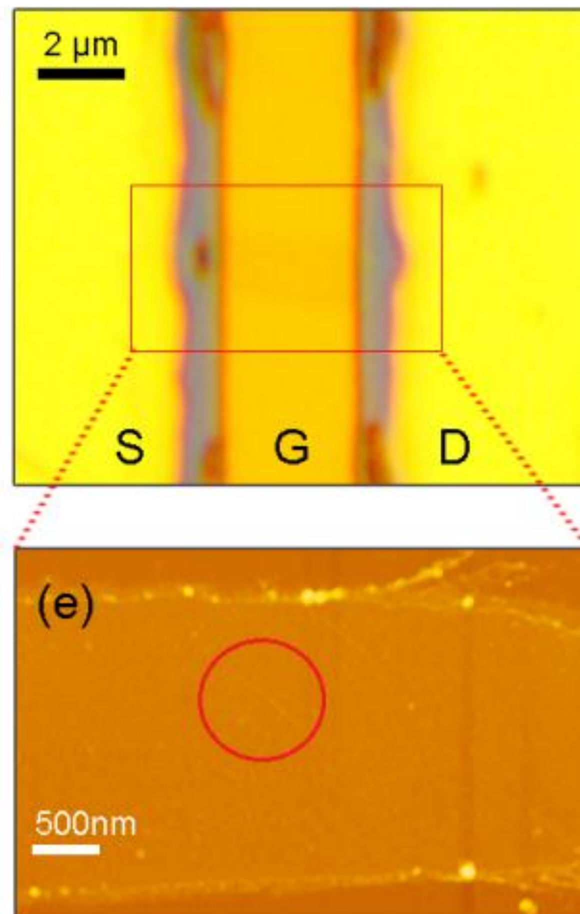


Figure 5-2 : Top view of the optical microscope image of the ultra-thin mica based GFET as fabricated on 285 nm SiO_2/Si substrate. The source, gate and drain of the GFET were marked as S, G and D respectively. Bottom: Zoom-in view of the GFET [141].

The mica flake measured by AFM had an average thickness 47 nm along the measured line (red line), see Figure 5-3. From the AFM image, one could see that ultra-thin mica remained atomically flat surface, consistent with our previous work and the observation by other groups [93, 100].

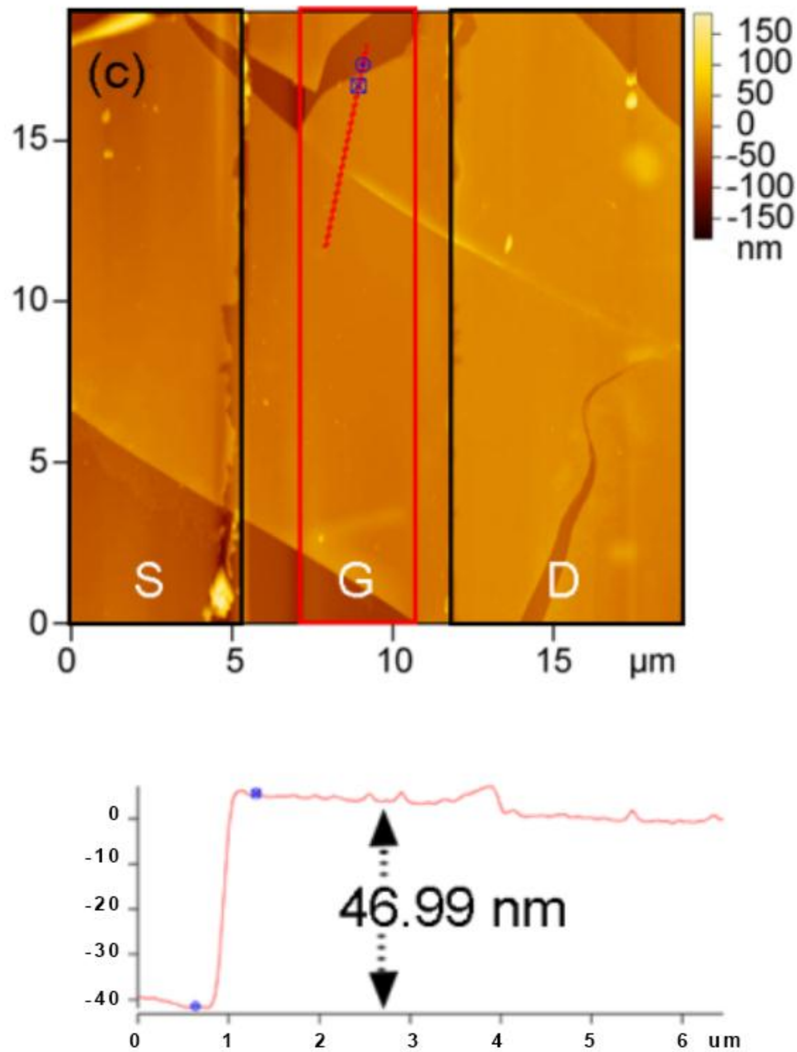
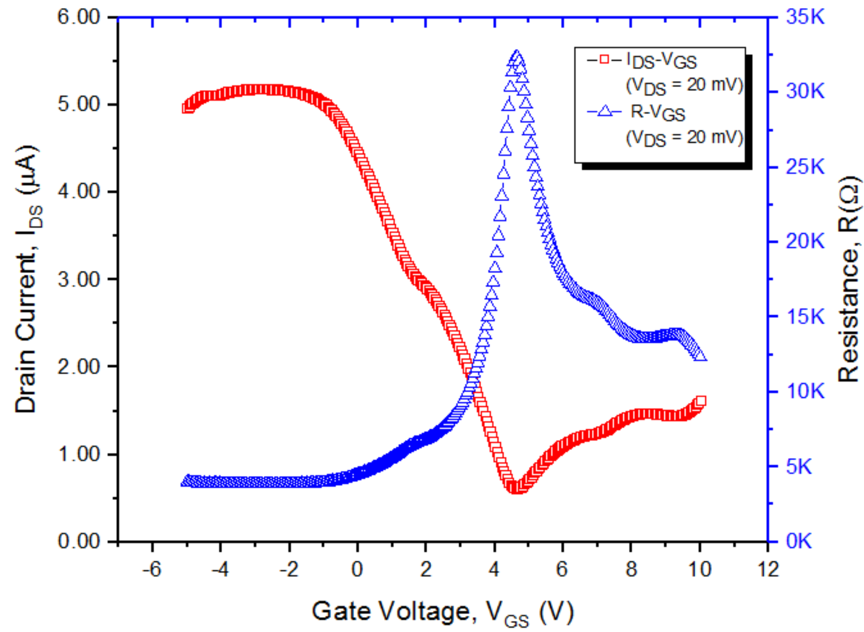


Figure 5-3 : AFM micrograph of the surface of the mechanical exfoliated mica. The mica flake was about 47 nm and remained its high flatness [141].

The transport characteristic (I_{DS}-V_{GS}) and output characteristic (I_{DS}-V_{DS}) of the 47 nm mica-based CNTFETs are shown in Figure 5-4.



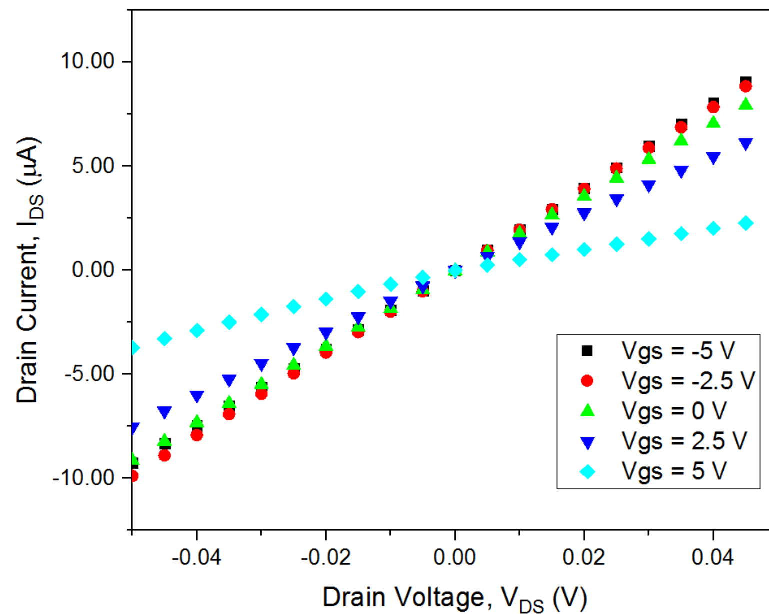


Figure 5-4 (a) Transport characteristic (I_{DS}-V_{GS}) and (b) output characteristic (I_{DS}-V_{DS}) of the 47 nm mica-based CNTFETs.

I_{DS}-V_{GS} curve of the mica-based GFET shows the typical ambipolar conduction ("V" shape), with hole conductance at negative V_{GS} higher than electrons conductance at positive V_{GS}. This is consistent to what have been widely reported about higher hole mobility and lower electron mobility in graphene [72, 149]. The R-V_{GS} curve of the

device was included in Figure 5-4 too. V_{DS} of 20 mV was used for the measurement. Typically, the I_{ON}/I_{OFF} ratio of the GFETs fabricated based on the procedure as described above is around 2-5, due to the semi metal behavior of graphene. The Dirac point is found to be at ~4.5 V, which non-zero Dirac point indicates unintentional doping of the graphene [150, 151]. Figure 5-4 (b) shows the output characteristics (I_{DS}-V_{DS}) of the mica-based GFET, with V_{GS} varying from -5 V to 5 V in the steps of 5. Similar to the observation from other groups, the output characteristics with small V_{DS} shows linear behavior without saturation [27, 73, 152]. The observation in this section will be further discussed and elaborated in the later section, which all the transport characteristics of mica-based GETs are included and compared.

Figure 5-5 shows the optical and AFM images of a 35 nm mica-based GFET, respectively. The quality of the CVD-grown graphene after transfer and etching was evaluated by Raman spectroscopy using 532 nm laser, as shown in Figure 5-5(c). The G and 2D peaks of the graphene on mica flake were observed at ~1583 cm^{-1} and ~2670 cm^{-1} with a full width at half maximum (FWHM) of 21 cm^{-1} and 35 cm^{-1}, respectively, consistent with the G and 2D peaks value reported for the monolayer graphene [153, 154]. The Raman spectra show a sharp and symmetric 2D band with I_{2D}/I_G intensity ratio around 1.15, suggesting that it was single layer graphene. It is interesting to note that the presence of mica did not cause a significant change to Raman spectra of the graphene. Due to the large bandgap of mica (10.50 eV) [90], mica has zero opacity at the visible window, or in the other word, it is transparent under optical microscope and Raman spectra. The invisibility of mica flake indicates that the Raman spectrum of graphene on mica is not interfered so that graphene Raman bands can be directly observed [101].

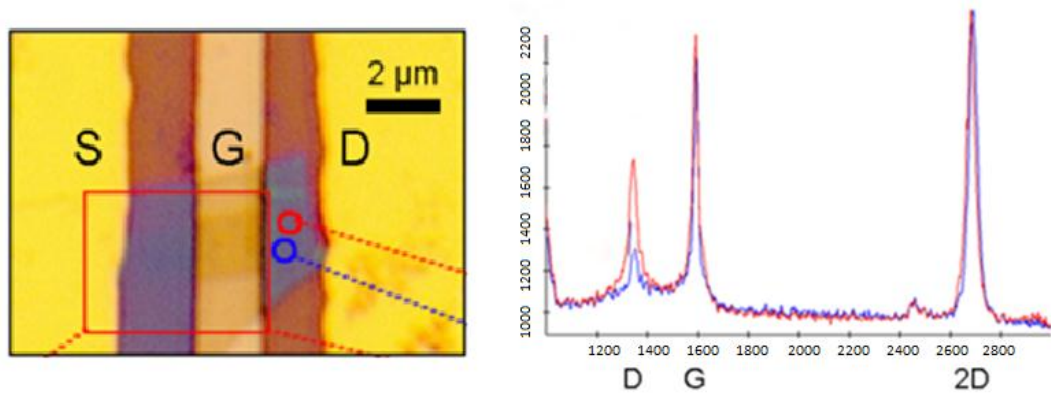


Figure 5-5 : The top view (left) of the 35 nm thick mica-based GFET, and the Raman spectra (right) of the graphene on mica structure based on the graphene areas marked by red and blue circle, showing the general spectra of single layer graphene [141].

Figure 5-6 shows the Raman mapping of the 35 nm mica-based GFET (of area marked by red box in Figure 5-5) at wavelength of ~2600-2700 cm^{-1} and ~800-2700 cm^{-1} respectively. It can be seen that mica remained transparent whereas the positions of the graphene were observed. The S and D pads (Au/Ti) were visible in the range due to the Raman spectra of the metals.

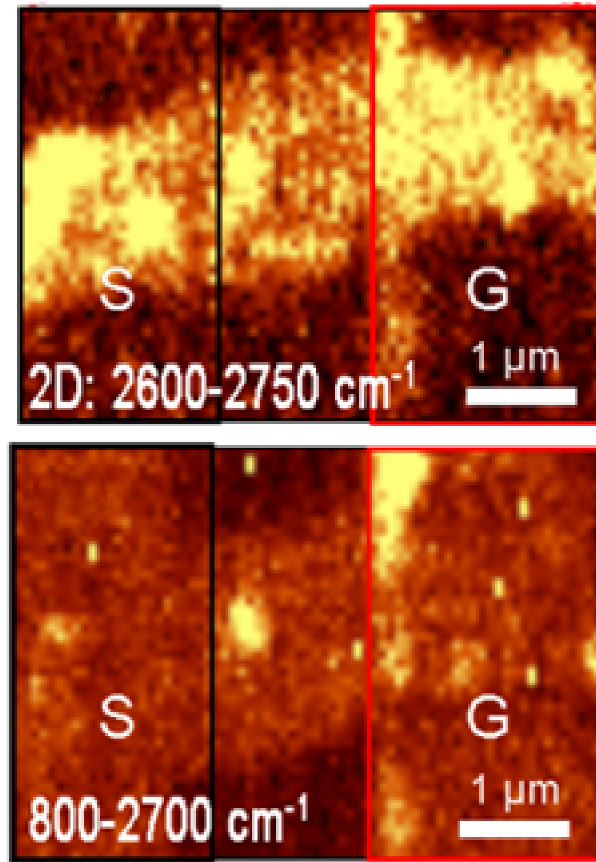


Figure 5-6 : Raman mapping of the graphene at the frequency of (top) 2600-2750 cm^{-1} and (bottom) 800-2700 cm^{-1}. It showed that the underlying mica gate dielectric did not cause any interference to the graphene Raman spectra at the frequency of 800-2700cm^{-1} [141].

To investigate the transport characteristics of graphene on mica, GFETs were fabricated on mica flakes of different thicknesses based on the device structure in Figure 5-7. The thicknesses of the mica of the GFETs (named as T1-T5) were 24 nm, 29 nm, 35 nm, 40 nm and 47 nm, respectively. Figure 5-7 shows the R-V_{GS} characteristics of the T1 – T5 GFETs. The carrier mobility (μ) of the GFETs was calculated using the equation given below [155, 156]:

$$\mu = \frac{L\,V_{DS}}{WC} \times |g_m| = \frac{Lt\,V_{DS}}{W\varepsilon\varepsilon_o} \times \frac{\Delta I_{DS}}{\Delta V_{GS}} \quad (5.1)$$

where L is the length of the graphene channel (L = 6-8 μm based on the experimental measurement of the devices), W is the width of the graphene channel (W = 1.5-2 μm based on the actual device measurement), V_{DS} is the measured source-drain voltage (here, V_{DS} = 0.02 V was chosen), ε is the relative dielectric constant of mica ($\varepsilon_{mica} \approx$ 8.1) [91], ε_0 is the absolute permittivity of vacuum ($\varepsilon_0 = 8.854 \times 10^{-12}$ F/m), t is the thicknesses of the mica gate dielectric (t = 24 nm, 29 nm, 35 nm, 40 nm, and 47 nm for sample T1-T5, respectively), and g_m is the transconductance of the devices.

The transconductance can be obtained by differentiating the I_{DS}-V_{GS} curve, or on the other hand,

$$g_m = \frac{d\,I_D}{d\,V_G} \tag{5.2}$$

The extracted transconductance (g_m) and calculated effective carrier mobility (μ) of the GFETs were plotted in Figure 5-8. The highest g_m and μ were found to be 3.36 μS and 2748 cm^2/Vs, respectively, on device T1 (t_{mica} = 24 nm).

For the performance comparison, a 40 nm SiO_2-based GFET was also fabricated using the same fabrication processes and device structure, except that the mica flake was replaced with SiO_2. The SiO_2-based GFET was plotted on Figure 5-7, showing lower g_m of 0.53 μS and lower μ of 1227 cm^2/Vs as compared to the 40 nm thick mica-based GFET (1.71 μS and 1907 cm^2/Vs, respectively).

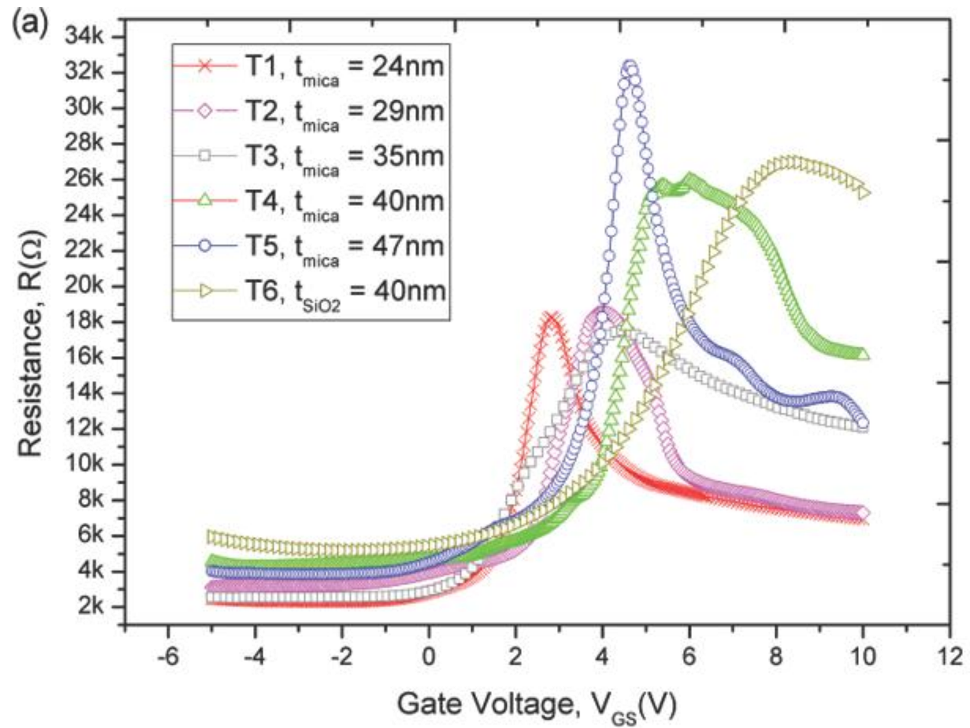


Figure 5-7 : Resistance between the source and drain pads as a function of the gate voltage (R-V_{GS}) for the GFETs of different mica thicknesses, namely, T1 (24 nm, red), T2 (29 nm, purple), T3 (35 nm, blue), T4 (40 nm, green) and T5 (47 nm, blue). In comparison, the R-V_{GS} of the SiO_2-based GFET is named as T6 (40 nm, brown) [141].

The maximum transconductance and the effective carrier mobility of GFETs of different mica gate dielectric thickness were extracted from the Figure 5-7 and re-plotted in Figure 5-8. Figure 5-8 clearly shows that the change of transconductance is proportional to the gate capacitance. When the gate dielectric thickness increased, the gate capacitance decreased accordingly, and resulting in the transconductance reduction. In addition, there was no significant change in the effective carrier mobility when the mica gate dielectric thickness was increased from 24 nm to 47 nm. This is consistent to the observation in other literatures, where the carrier mobility was found to be only strongly dependent on the dielectric thickness when the channel length $L < 10$ nm [157, 158]. Based on Equation 5.1, the calculated carrier mobility of T1-T5 falls in the range

of 2000~2700 cm^2/Vs. This carrier mobility variation could be due to the difference in the channel dimension (width, W and length, L) of the fabricated devices. The range of the channel dimensions of our devices was measured to have length between 6-8 μm and width of 1-1.5 μm. It was also reported the carrier mobility saturated at a constant value on the devices which have channel length of several micrometers [155]. Hence, it is important to highlight here about the limitation of the model being used in the calculation of the carrier mobility for GFET since the dimensions of our devices fall in this range.

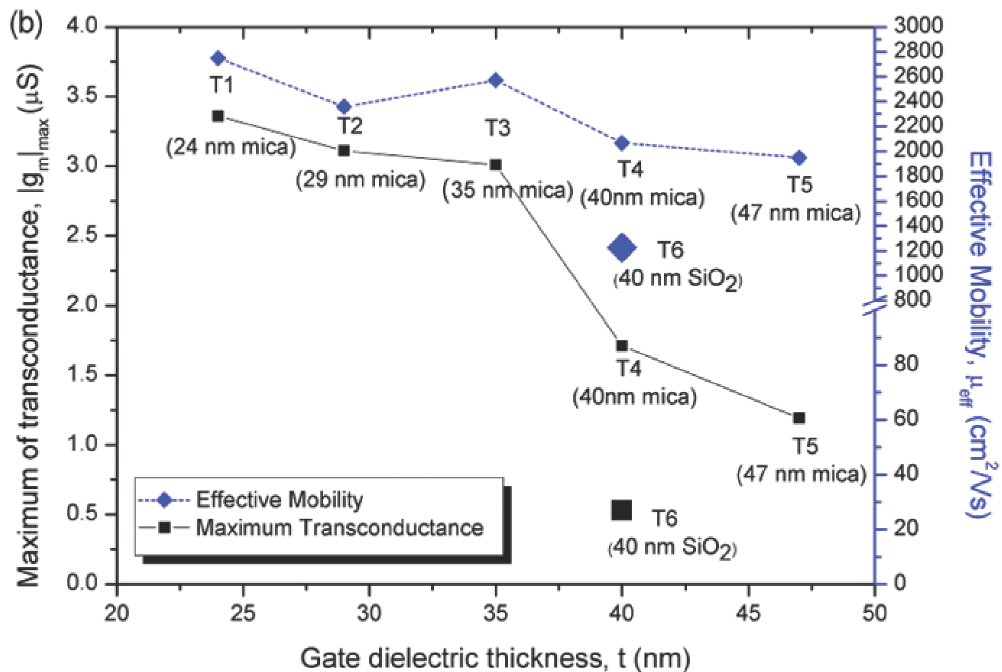


Figure 5-8 : The maximum small signal transconductance and effective carrier mobility of T1-T5 were plotted, showing that 24 nm mica based GFET has the highest maximum transconductance and effective carrier mobility.

The mobility improvement of the mica-based GFET as compared to silicon oxide-based GFET could be attributed to the minimum surface roughness of mica flake. As reported, free-standing graphene commonly consists of microscopic corrugations due to

thermal fluctuation [159], whereas the supported graphene conforms and follows the morphology of the underlying substrates with the presence of ripples of different origins [132]. The substrate effect and the thermally created ripples could result in the long-range scattering potential that may contribute dominantly to the resistivity of the graphene [160]. Therefore, the surface morphology of the substrate plays a significant role in limiting the carrier transport of the graphene. Mica is well-known for its atomically flat surface on which ultra-flat graphene with surface variation of <25 pm could be achieved [93]. Theoretical analysis by Rudenko *et al.* has led to the prediction of ultra-flat graphene on mica as a result of the interaction of the K^+ ions of mica surface on the graphene [104]. The reduction in the surface roughness and the ripples of graphene on mica are believed to be the main factor for the mobility improvement of the mica-based GFET. It has been noted that surface roughness scattering is especially critical for low dimensional materials [161], such as 2D graphene and 1D CNTs. The result of mobility improvement of graphene on mica as reported here is consistent with what has been reported previously for CNT on mica [100].

Charged impurity scattering was widely accepted to be the source of scattering in graphene. However, Ponomarenko *et al.* reported that Coulomb impurities would not limit the mean free path of graphene on a substrate and could only be dominant for devices of low mobility (~100-1000 cm^2/Vs) [140]. For the case of muscovite mica, the distribution of potassium ions on muscovite mica upon cleavage was reported to be randomly distributed [104]. The possibility of the charged impurity scattering for mica-based GFETs cannot be ruled out without any specific mica surface treatment and, hence, the effect of the surface charged impurity scattering of mica based GFET is still unclear at this stage. However, as the calculated mobility of our devices was in the range

of 1000-3000 cm^2/Vs, the charged impurity scattering may not be a dominant mechanism in our case according to the literature [140].

High-k gate dielectric has been widely reported to improve the transport characteristics of FETs in terms of gate control, transconductance and carrier mobility, which are especially important for high frequency applications of graphene electronics [162]. Besides that, the charge transport of the GFETs was reported to be enhanced through dielectric screening by high-k gate dielectric, in which the Coulomb impurity scattering could be strongly damped [163-165]. Hafnium oxide [166], zirconium oxide [167], aluminium oxide [166] and silicon nitride [168] have been widely employed as high-k materials for this purpose. For instance, Liao *et al.* has reported on the aluminium oxide [74], hafnium oxide [166] and zirconium oxide [167] based top-gated high performance graphene transistors, whereas Radisavljevic *et al.* reported on the improvement of carrier mobility in MoS_2 by a factor of 70-400 for hafnium oxide based MoS_2 FET as compared to silicon oxide based device [169]. As the dielectric constant of muscovite mica is 8.1, about twice that of the dielectric constant of SiO_2 (3.9), 40 nm mica-based GFET showed a significant improvement in the transcondutance of more than 3 times in comparison with 40 nm SiO_2-based GETs (Figure 5-8). Hence, the downscaling of mica gate dielectric layer to thickness as thin as 10 nm is predicted to have further improvement in the gate control capability and transconductance of GFETs without significant leakage current.

From the R-V_{GS} curves, it was found that the mica-based GFETs generally showed hole-doped asymmetry characteristics. The Dirac points of the devices were at 2~6 V, whereas the n-branch conductance was lower than the p-branch conductance. Several possible reasons could be responsible for this finding. Firstly, the potassium ions on

mica surface upon cleavage is randomly distributed [82], so that different regions of the surface could have different hole doping effect [104]. In general, all the mica-based GFETs fabricated showed hole-doping characteristics. Secondly, the doping effect could be caused by water adlayers trapped between the graphene and underlying mica. Due to high hydrophilicity of mice surface, mica attracts water molecules [84, 85], and the water adlayers were reported to be strongly bonded on mica surface [170]. Strong and persistent hole doping of graphene induced by water layer and mica substrate was reported [171, 172]. Thirdly, the hole-doping of GFET could also possibly be caused by the residue of PMMA carrier [173, 174]. It was reported that, despite of the high temperature annealing (300 – 400 ºC) in a mixture of argon (Ar) and hydrogen (H_2) gas with a ratio of 95:5 or ultra-high vacuum environment, the thin PMMA layer could not be decomposed and removed completely from graphene surface [133]. Lastly, the observation of electron-hole asymmetry in the R-V_{GS} curves can also be explained by the device geometry, which resulting in the pinning of the charge density at graphene-metal interface and the formation of p-n or p-p junction [175].

Figure 5-9 shows the Raman spectroscopy of graphene on SiO_2/Si substrate and graphene on mica substrate. It was observed that there was a significant OH^- peak at 3600cm^{-1} for the graphene on mica, which was reported to be caused by the OH band of water molecules [176-178]. This shows the existence of water adlayers in between graphene and mica surface, consistent to the observation reported in literature [85, 94]. In contrast, there was no significant OH^- peak for graphene on SiO_2/Si substrate. There was a blue shift of 16 cm^{-1} at the 2D peak of graphene on mica, in comparison to graphene on SiO_2, as shown in Figure 5-10. Similar blue shift of 15 cm^{-1} was observed for graphene on mica as well [94], suggesting that hole-doping of graphene on mica is

a general phenomenon [94]. The observation on the Raman spectra is consistent to the hole-doped asymmetry behaviour as shown in the R-V_{GS} curve in previous section. The hole-doped characteristic of graphene on mica substrate is advantageous for gas sensing, as reported by Aziza *et al* [179], where the graphene/mica based ammonia gas sensor was more sensitive than graphene/SiO_2 based gas sensor.

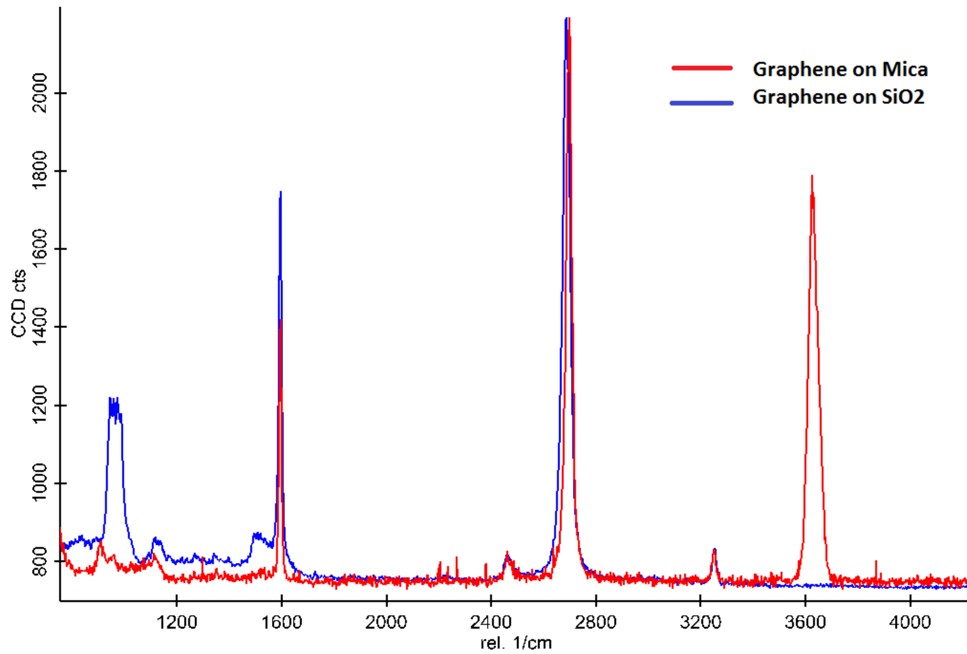


Figure 5-9: The Raman spectra of graphene on mica (red) and graphene on SiO_2 substrate (blue), respectively.

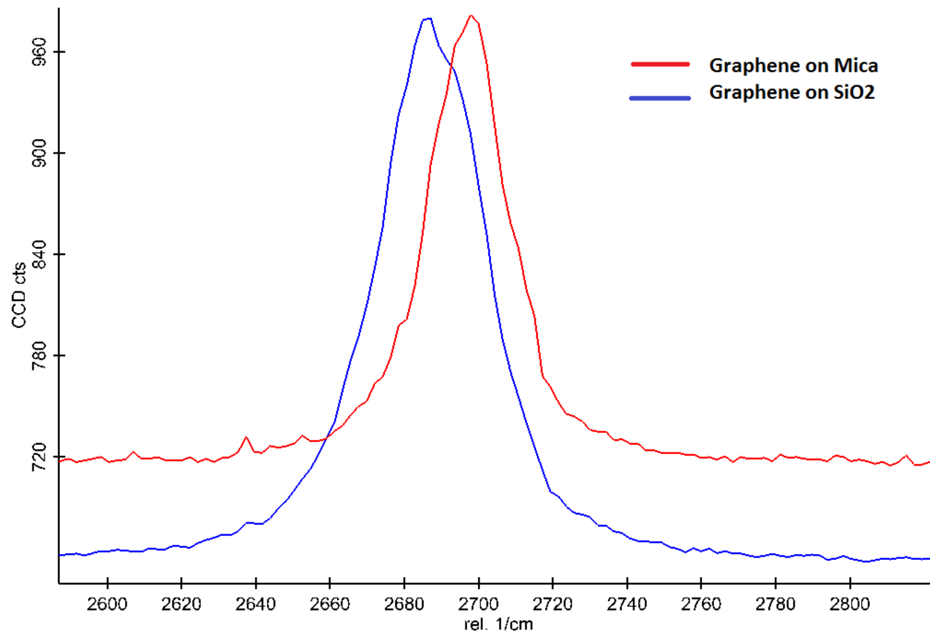


Figure 5-10: Blue shift of ~16 cm^{-1} is shown in the Raman spectrum of graphene on mica (red) in comparison to graphene on SiO_2 (blue).

5.4 Conclusion

Ultra-thin and atomically flat mica-based GFETs were successfully fabricated. Mica-based GFETs show higher effective carrier mobility and transconductance due to the high surface smoothness and high dielectric constant of mica gate dielectric layers. Thin mica gate dielectric layers provide an atomically flat supporting platform for graphene with reduced thermally induced intrinsic ripples.

CHAPTER 6: Conclusive Remarks and Future Works

6.1 Conclusive Remarks

In this thesis, ultra-thin mica was demonstrated to be used as the gate dielectric layers of carbon nanotube (CNTs) field effect transistors and graphene field effect transistors. The key findings and implication of this report can be summarized as below:

1. A cost effective and widely reported method was adopted to realize ultra-thin mica. Similar to other two dimensional materials, mica can be cleaved to few-layer using the simple mechanical exfoliation technique, thanks to the weak interlayer bonding. Unlike graphene where ripples are commonly occurred during the fabrication, mica could maintain the ultra-flat surface after mechanical exfoliation. This enables ultrathin mica flakes to be used as a gate dielectric material for FETs (e.g. sub 20 nm FETs) where the surface roughness plays a key part in the device performance. However, it remains challenging to incorporate ultrathin mica flakes into these FETs, due to the high transparency of mica.

2. A systematic study was carried out to understand the fundamental physics of observing mica flakes under optical microscope, and the condition to locate mica flakes on the substrate were further optimized. Although AFM could give a very accurate thickness up to sub-nanometer range, its small scan size (largest is 1 μm x 1 μm) compared to a large sample size (~a few cm^2) has made the characterization very time consuming. Hence, locating mica flakes by optical microscope is preferred, and the contrast spectroscopy of mica/SiO_2/Si substrate tri-layer system was constructed. It was shown that 10-30 nm thick mica flakes could be identified easily using a contrast

spectroscopy and a bright field optical compound microscope. The physics behind this has been explored and the thickness of observed mica flakes were experimentally confirmed using atomic force microscopy technique. Most importantly, it was discovered that the optical contrast was enhanced by using light filter. Both experimental and simulated results were consistent, suggesting that the spectroscopy was accurately constructed. This method offers an efficient technique to locate mica flakes in a cost effective, reliable and efficient way.

3. In order to verify the hypothesis that freshly cleaved mica flakes retain its atomically flat surface, the surface roughness of the mica flakes was evaluated using AFM measurement. The RMS roughness of freshly cleaved mica surface was measured to be 78 pm, at least three times smoother than the thermally grown SiO_2 surface. This observation is critical as it opens up the possibility to employ exfoliated mica as the gate dielectric of FETs.

4. Atomic flat mica flakes were used as the gate dielectric layer for CNTFETs. Both top-contact and bottom-contact mica-based CNTFETs were fabricated for comparison, and it was concluded that bottom-contact mica-based CNTFETs outperform top-contact mica-based CNTFETs in terms of gate control capability, with subthreshold swing of six time smaller. The subthreshold swing of the 28 nm (EOT $\approx$ 13nm) bottom-contact mica-based CNTFETs achieved is as low as 110 mV/dec, much smaller than that of the CNTFETs with conventional silicon nitride gate dielectric materials. In terms of carrier mobility, mica-based CNTFETs shows higher carrier mobility in comparison to SiN-based CNTFETs. This is attributed to the high surface flatness of mica. Compared to other high-k dielectric gate materials such as hafnium oxide (HfO_2) and tantalum oxide (Ta_2O_5), the mica-based CNTFETs showed comparable performance with a minimum

leakage current. The findings suggest that mica could be a good high-k gate dielectric material for the CNTFETs, with high surface flatness and superior dielectric strength. In other words, it opens up the possibility to downscale the gate dielectric thickness without significant leakage current.

5. Mica-based graphene FETs were also fabricated. Since graphene is a 2D material which is extremely sensitive to the underlying substrate, mica stands out not only as a great support for graphene to realize ultra-flat graphene, but also plays the role of gate dielectric with excellent gate control capability. To our knowledge, ultrathin mica-based graphene FET was demonstrated first time in our report. Mica-based graphene FETs show excellent transconductance and carrier mobility in comparison to SiO_2-based GFETs of the same device structure, attributed to the atomically flat surface of the mica gate layers. In addition, it is noted that mica gate dielectric remains transparent to Raman spectroscopy. Since graphene are often characterized by Raman spectroscopy, the Raman spectrum of graphene on mica will not be interfered.

6.2 Future challenges

Compared to the matured silicon based IC technology, uses of carbon-based materials as building block of FETs is still in the stage of laboratory research. There are a few major challenges to be overcome before going to be commercialized. One of them is to find an appropriate gate dielectric material to achieve a high carrier mobility in low-dimensional carbon materials such as CNTs and graphene, to realise high switching speed and low leakage current. The use of mica as the gate dielectric layer has attracted

much attention recently, however, there are still some aspects that remain unknown and worth further study

1. The fabrication process of mica remains challenging. Although mechanical exfoliation can be used to achieve few-layer mica flakes to build the prototype of CNT FETs and graphene FETs with mica as the gate dielectric, large scale production of these types of FETs is challenging as the thickness and locations of mica flakes are quite randomly distributed if the mechanical exfoliation technique is employed, mainly due to the transparent property of mica thin film.

2. To achieve ultrathin mica flakes with a surface area larger than 10x10 μm^2 using the mechanical exfoliation technique is challenging as mica is very brittle, much more brittle than graphene. To fabricate mica based FETs in a large scale, synthesis of ultrathin mica with atomically flat surface must be developed. Synthesis of mica thin films which are of the dielectric properties and surface flatness of natural mica thin films will open up more study and application of mica.

3. Single or few layer mica remains transparent under optical microscope, which makes it extremely challenging to study its property. In our study, SiO_2/Si based substrates with different SiO_2 thicknesses being optimized to maximize its contrast were used. Further study and investigation could be carried out by optimizing the mica contrast on other materials, for example silicon nitride etc, which under certain combination of material thicknesses and dielectric constants could enhance the contrast of mica under optical microscope.

4. The freshly cleaved mica surface was reported to contain potassium atoms. The influences of potassium atoms on mica surface on the electronic transport properties of

CNT channels or graphene channels remain unclear yet. Since mica is being used as the gate dielectric layer which will be in full contact with the channel area of the FETs, a systematic study on this issue is necessary. The understanding of this will be important for the transport characteristic and gas sensing property of mica-based device.

5. Due to the high dielectric strength and breakdown field of mica, it opens up the possibility to employ mica as the high quality insulator for the application in heterostructure devices and tunnelling devices, such as the barrier layer for electron tunnelling between two graphene layers or in graphene vertical tunnelling transistors. Just like boron nitride, mica has got its pros and cons as the insulator in combination with graphene. However, the study of such kind of mica-graphene 2D layers structure remains unexplored at the moment.

List of Publications

1. **Chong Guan Low**, Qing Zhang, "Graphene Field Effect Transistors with Mica as Gate Dielectric Layers", Small, 10(20), 4213-4218 (2014)

2. **Chong Guan Low**, Qing Zhang, "Ultra-thin and Flat Mica as Gate Dielectric Layers, Small, 8(14), 2178-2183 (2012)

3. **Chong Guan Low**, Qing Zhang, "Carbon Nanotubes and Their Applications, Chapter 7: From Bulk TFETs to CNT-TFETs: Status and Trends", Pan Stanford Publishing, Print ISBN ISBN 9789814241908 (2011)

4. **Chong Guan Low**, Qing Zhang, "Ultra-thin and Flat Mica-based Field Effect Transistor", International Union of Materials Research Society – International Conference on Electronics Materials Yokohama (IUMRS-ICEM) (2012)

5. **Chong Guan Low**, Leck Kheng Swee, Jianping Zou and Qing Zhang, "Ultra-thin and Flat Mica", International Conference on Materials for Advanced Technologies (ICMAT) (2011)

6. **Chong Guan Low**, Qing Zhang, "Contrast Spectroscopy of Ultra-thin Mica and Its Application for Carbon-based Field Effect Transistor", East Asian Postgraduate Workshop on Nanoscience and Technology (PGWS) (2011)

7. **Chong Guan Low**, Qing Zhang, "Ultra-thin and Flat Mica-based Field Effect Transistor", MRS-S Conference on Advanced Material (2012)

References

1. Gundlach, D.J., *et al.*, *Pentacene organic thin-film transistors-molecular ordering and mobility.* IEEE Electron Device Letters, 1997. **18**(3): p. 87-89.
2. Robison, R.A., *Moore's Law: Predictor and Driver of the Silicon Era.* World Neurosurgery, 2012. **78**(5): p. 399-403.
3. Thompson, S.E. and S. Parthasarathy, *Moore's law: the future of Si microelectronics.* Materials Today, 2006. **9**(6): p. 20-25.
4. Sze, S.M. and K.K. Ng, *Introduction*, in *Physics of Semiconductor Devices*. 2006, John Wiley & Sons, Inc. p. 1-3.
5. Sze, S.M. and K.K. Ng, *Physics and Properties of Semiconductors—A Review*, in *Physics of Semiconductor Devices*. 2006, John Wiley & Sons, Inc. p. 5-75.
6. Lee, M.L., *et al.*, *Strained Si, SiGe, and Ge channels for high-mobility metal-oxide-semiconductor field-effect transistors.* Journal of Applied Physics, 2005. **97**(1): p. 011101.
7. Kim, K. *Future silicon technology*. in *2012 Proceedings of the European Solid-State Device Research Conference (ESSDERC)*. 2012. IEEE.
8. Schulz, M., *The end of the road for silicon?* Nature, 1999. **399**(6738): p. 729-730.
9. Wagner, C. and N. Harned, *EUV lithography: Lithography gets extreme.* Nat Photon, 2010. **4**(1): p. 24-26.
10. Bjorkholm, J.E., *EUV lithography—the successor to optical lithography?* Intel Technology Journal, 1998. **3**: p. 98.
11. Xia, Y. and G.M. Whitesides, *SOFT LITHOGRAPHY.* Annual Review of Materials Science, 1998. **28**(1): p. 153-184.
12. Wu, B. and A. Kumar, *Extreme ultraviolet lithography: A review.* Journal of Vacuum Science & Technology B, 2007. **25**(6): p. 1743-1761.
13. Moore, G.E. *Lithography and the future of Moore's law*. 1995.
14. Tsurumi, N., *et al. GaN Transistors for Power Switching and High Frequency Applications*. in *Compound Semiconductor Integrated Circuits Symposium, 2008. CSIC '08. IEEE*. 2008.
15. Scopece, D., *et al.*, *Straining Ge bulk and nanomembranes for optoelectronic applications: a systematic numerical analysis.* Semiconductor Science and Technology, 2014. **29**(9): p. 095012.
16. Sidek, R.M., *et al.*, *SiGe CMOS fabrication using SiGe MBE and anodic/LTO gate oxide.* Semiconductor Science and Technology, 2000. **15**(2): p. 135.
17. Whall, T.E. and E.H.C. Parker, *SiGe heterostructures for FET applications.* Journal of Physics D: Applied Physics, 1998. **31**(12): p. 1397.
18. Del Alamo, J.A., *Nanometre-scale electronics with III-V compound semiconductors.* Nature, 2011. **479**(7373): p. 317-323.
19. Möller, M. *High Speed Electronic Circuits for 100 Gb/s Transport Networks*. in *Optical Fiber Communication Conference*. 2010. Optical Society of America.
20. Malic, E. and A. Knorr, *Introduction – The Carbon Age*, in *Graphene and Carbon Nanotubes*. 2013, Wiley-VCH Verlag GmbH & Co. KGaA. p. 1-8.
21. Iijima, S., *Helical microtubules of graphitic carbon.* Nature, 1991. **354**(6348): p. 56-58.
22. Geim, A.K. and K.S. Novoselov, *The rise of graphene.* Nature Materials, 2007. **6**(3): p. 183-191.

23. Novoselov, K.S., *et al.*, *Electric Field Effect in Atomically Thin Carbon Films.* Science, 2004. **306**(5696): p. 666-669.
24. Dresselhaus, M.S. and P.T. Araujo, *Perspectives on the 2010 Nobel Prize in Physics for Graphene.* ACS Nano, 2010. **4**(11): p. 6297-6302.
25. 2014, N.M.A. *The Nobel Prize in Physics 2010.* 2010 [cited 2015 14 Apr 2015]; Available from: Nobelprize.org.
26. Bolotin, K.I., *Ultrahigh electron mobility in suspended graphene.* Solid State Commun., 2008. **146**: p. 351-355.
27. Lin, Y.-M., *et al.*, *100-GHz Transistors from Wafer-Scale Epitaxial Graphene.* Science, 2010. **327**(5966): p. 662.
28. Nair, R., *et al.*, *Fine structure constant defines visual transparency of graphene.* Science, 2008. **320**(5881): p. 1308-1308.
29. Bae, S., *et al.*, *Roll-to-roll production of 30-inch graphene films for transparent electrodes.* Nat Nano, 2010. **5**(8): p. 574-578.
30. Iijima, S. and T. Ichihashi, *Single-shell carbon nanotubes of 1-nm diameter.* Nature, 1993. **363**(6430): p. 603-605.
31. Bethune, D.S., *et al.*, *Cobalt-catalysed growth of carbon nanotubes with single-atomic-layer walls.* Nature, 1993. **363**(6430): p. 605-607.
32. Javey, A., *et al.*, *Ballistic carbon nanotube field-effect transistors.* Nature, 2003. **424**(6949): p. 654-657.
33. Zhang, X., *et al.*, *Ultrastrong, stiff, and lightweight Carbon‐Nanotube fibers.* Advanced Materials, 2007. **19**(23): p. 4198-4201.
34. Falvo, M.R., *et al.*, *Bending and buckling of carbon nanotubes under large strain.* Nature, 1997. **389**(6651): p. 582-584.
35. Sgobba, V. and D.M. Guldi, *Carbon nanotubes—electronic/electrochemical properties and application for nanoelectronics and photonics.* Chemical society reviews, 2009. **38**(1): p. 165-184.
36. Hartmann, R.R., J. Kono, and M.E. Portnoi, *Terahertz science and technology of carbon nanomaterials.* Nanotechnology, 2014. **25**(32): p. 322001.
37. Bandaru, P.R., *Electrical properties and applications of carbon nanotube structures.* Journal of nanoscience and nanotechnology, 2007. **7**(4-5): p. 1239-1267.
38. Oberlin, A., M. Endo, and T. Koyama, *Filamentous growth of carbon through benzene decomposition.* Journal of Crystal Growth, 1976. **32**(3): p. 335-349.
39. Jiang, J., *et al.*, *Chirality dependence of exciton effects in single-wall carbon nanotubes: Tight-binding model.* Physical Review B, 2007. **75**(3): p. 035407.
40. Saito, S. and A. Zettl, *Carbon Nanotubes: Quantum Cylinders of Graphene: Quantum Cylinders of Graphene*. Vol. 3. 2008: Elsevier.
41. Dresselhaus, M.S., *et al.*, *Raman spectroscopy of carbon nanotubes.* Physics reports, 2005. **409**(2): p. 47-99.
42. Terrones, M., *SCIENCE AND TECHNOLOGY OF THE TWENTY-FIRST CENTURY: Synthesis, Properties, and Applications of Carbon Nanotubes.* Annual Review of Materials Research, 2003. **33**(1): p. 419-501.
43. Hong, S. and S. Myung, *Nanotube Electronics: A flexible approach to mobility.* Nat Nano, 2007. **2**(4): p. 207-208.
44. Martel, R., *et al.*, *Single- and multi-wall carbon nanotube field-effect transistors.* Applied Physics Letters, 1998. **73**(17): p. 2447-2449.

45. Pourfath, M., H. Kosina, and S. Selberherr, *Numerical study of quantum transport in carbon nanotube transistors.* Mathematics and Computers in Simulation, 2008. **79**(4): p. 1051-1059.
46. Heinze, S., *et al.*, *Carbon Nanotubes as Schottky Barrier Transistors.* Physical Review Letters, 2002. **89**(10): p. 106801.
47. Appenzeller, J., *et al.*, *Field-Modulated Carrier Transport in Carbon Nanotube Transistors.* Physical Review Letters, 2002. **89**(12): p. 126801.
48. Leonard, F. and J. Tersoff, *Novel length scales in nanotube devices.* Phys. Rev. Lett., 1999. **83**: p. 5174-5177.
49. Martel, R., *et al.*, *Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes.* Physical Review Letters, 2001. **87**(25): p. 256805.
50. Avouris, P., *Carbon nanotube electronics.* Chemical Physics, 2002. **281**(2–3): p. 429-445.
51. Soh, H.T., *et al.*, *Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes.* Applied Physics Letters, 1999. **75**(5): p. 627-629.
52. Appenzeller, J., *et al.*, *Tunneling Versus Thermionic Emission in One-Dimensional Semiconductors.* Physical Review Letters, 2004. **92**(4): p. 048301.
53. Collins, P.G., *et al.*, *Extreme Oxygen Sensitivity of Electronic Properties of Carbon Nanotubes.* Science, 2000. **287**(5459): p. 1801-1804.
54. Oh, H., *et al.*, *Fabrication of n-type carbon nanotube field-effect transistors by Al doping.* Applied Physics Letters, 2006. **88**(10): p. 103503.
55. Javey, A., *et al.*, *Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-κ Gate Dielectrics.* Nano Letters, 2004. **4**(3): p. 447-450.
56. Léonard, F. and J. Tersoff, *Role of Fermi-Level Pinning in Nanotube Schottky Diodes.* Physical Review Letters, 2000. **84**(20): p. 4693-4696.
57. Yu, W.J., *et al.*, *Adaptive Logic Circuits with Doping-Free Ambipolar Carbon Nanotube Transistors.* Nano Letters, 2009. **9**(4): p. 1401-1405.
58. Nakanishi, T., A. Bachtold, and C. Dekker, *Transport through the interface between a semiconducting carbon nanotube and a metal electrode.* Physical Review B, 2002. **66**(7): p. 073307.
59. Wind, S.J., J. Appenzeller, and P. Avouris, *Lateral Scaling in Carbon-Nanotube Field-Effect Transistors.* Physical Review Letters, 2003. **91**(5): p. 058301.
60. Javey, A., *et al.*, *High Performance n-Type Carbon Nanotube Field-Effect Transistors with Chemically Doped Contacts.* Nano Letters, 2005. **5**(2): p. 345-348.
61. Gao, P., *et al.*, *Complementary Logic Gate Arrays Based on Carbon Nanotube Network Transistors.* Small, 2013. **9**(6): p. 813-819.
62. Cao, Q., *et al.*, *Medium-scale carbon nanotube thin-film integrated circuits on flexible plastic substrates.* Nature, 2008. **454**(7203): p. 495-500.
63. Snow, E., *et al.*, *High-mobility carbon-nanotube thin-film transistors on a polymeric substrate.* Applied Physics Letters, 2005. **86**(3): p. 033105.
64. Zhou, Y., *et al.*, *p-Channel, n-Channel Thin Film Transistors and p−n Diodes Based on Single Wall Carbon Nanotube Networks.* Nano Letters, 2004. **4**(10): p. 2031-2035.
65. Bradley, K., J.-C.P. Gabriel, and G. Grüner, *Flexible Nanotube Electronics.* Nano Letters, 2003. **3**(10): p. 1353-1355.

66. Chimot, N., *et al.*, *Gigahertz frequency flexible carbon nanotube transistors.* Applied Physics Letters, 2007. **91**(15): p. 153111.
67. Kang, S.J., *et al.*, *High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes.* Nat Nano, 2007. **2**(4): p. 230-236.
68. Gao, P. and Q. Zhang, *Encapsulate-and-peel: fabricating carbon nanotube CMOS integrated circuits in a flexible ultra-thin plastic film.* Nanotechnology, 2014. **25**(6): p. 065301.
69. Castro Neto, A.H., *et al.*, *The electronic properties of graphene.* Rev. Mod. Phys., 2007.
70. Novoselov, K.S., *Electric field effect in atomically thin carbon films.* Science, 2004. **306**: p. 666-669.
71. Lemme, M.C., *et al.*, *A Graphene Field-Effect Device.* IEEE Electron Device Letters, 2007. **28**(4): p. 282-284.
72. Schwierz, F., *Graphene transistors.* Nat Nano, 2010. **5**(7): p. 487-496.
73. Lin, Y.-M., *et al.*, *Operation of Graphene Transistors at Gigahertz Frequencies.* Nano Letters, 2009. **9**(1): p. 422-426.
74. Liao, L., *et al.*, *High-κ oxide nanoribbons as gate dielectrics for high mobility top-gated graphene transistors.* Proceedings of the National Academy of Sciences, 2010. **107**(15): p. 6711-6715.
75. Farmer, D.B., *et al.*, *Utilization of a Buffered Dielectric to Achieve High Field-Effect Carrier Mobility in Graphene Transistors.* Nano Letters, 2009. **9**(12): p. 4474-4478.
76. Meric, I., *et al.*, *Current saturation in zero-bandgap, top-gated graphene field-effect transistors.* Nat Nano, 2008. **3**(11): p. 654-659.
77. Ni, Z.H., *et al.*, *Uniaxial Strain on Graphene: Raman Spectroscopy Study and Band-Gap Opening.* ACS Nano, 2008. **2**(11): p. 2301-2305.
78. Kim, S., *et al.*, *Realization of a high mobility dual-gated graphene field-effect transistor with Al2O3 dielectric.* Applied Physics Letters, 2009. **94**(6): p. -.
79. Wang, X., *et al.*, *Room-Temperature All-Semiconducting Sub-10-nm Graphene Nanoribbon Field-Effect Transistors.* Physical Review Letters, 2008. **100**(20): p. 206803.
80. Sun, J., *et al.*, *Lateral plasma etching enhanced on/off ratio in graphene nanoribbon field-effect transistor.* Applied Physics Letters, 2015. **106**(3): p. 033509.
81. Deer, W.A., R. A. Howie and J. Zussman, *An Introduction to the Rock Forming Minerals.* 1966.
82. Poppa, H. and A.G. Elliot, *The surface composition of Mica substrates.* Surface Science, 1971. **24**(1): p. 149-163.
83. Müller, K. and C.C. Chang, *Electric dipoles on clean mica surfaces.* Surface Science, 1969. **14**(1): p. 39-51.
84. Xu, K., P. Cao, and J.R. Heath, *Graphene Visualizes the First Water Adlayers on Mica at Ambient Conditions.* Science, 2010. **329**(5996): p. 1188-1191.
85. Frenken, J.W.M. and T.H. Oosterkamp, *Microscopy: When mica and water meet.* Nature, 2010. **464**(7285): p. 38-39.
86. Christenson, H.K. and J.N. Israelachvili, *Growth of ionic crystallites on exposed surfaces.* Journal of Colloid and Interface Science, 1987. **117**(2): p. 576-577.
87. Israelachvili, J.N., *et al.*, *Preparing Contamination-free Mica Substrates for Surface Characterization, Force Measurements, and Imaging.* Langmuir, 2004. **20**(9): p. 3616-3622.

88. Ostendorf, F. and *et al.*, *How flat is an air-cleaved mica surface?* Nanotechnology, 2008. **19**(30): p. 305705.
89. Hackett, W. and A. Morris Thomas, *The electric strength of mica and its variation with temperature.* Electrical Engineers - Part I: General, Journal of the Institution of, 1941. **88**(8): p. 295-303.
90. Lu, X.F., L.A. Majewski, and A.M. Song, *Electrical characterization of mica as an insulator for organic field-effect transistors.* Organic Electronics, 2008. **9**(4): p. 473-480.
91. Weeks, J.R., *The Dielectric Constant of Mica.* Physical Review, 1922. **19**(4): p. 319-322.
92. He, Y., *et al.*, *Mica, a Potential Two-Dimensional-Crystal Gate Insulator for Organic Field-Effect Transistors.* Advanced Materials, 2011. **23**(46): p. 5502-5507.
93. Lui, C.H., *et al.*, *Ultraflat graphene.* Nature, 2009. **462**(7271): p. 339-341.
94. Shim, J., *et al.*, *Water-Gated Charge Doping of Graphene Induced by Mica Substrates.* Nano Letters, 2012. **12**(2): p. 648-654.
95. Ni, Z.H., *et al.*, *Graphene Thickness Determination Using Reflection and Contrast Spectroscopy.* Nano Letters, 2007. **7**(9): p. 2758-2763.
96. Akira Matsumoto, R.O., Susumu Ikeda, Koichiro Saiki, and Keiji Ueno, *Effect of Organic Buffer Layer on Performance of Pentacene Field-Effect Transistor Fabricated on Natural Mica Gate Dielectric.* Jpn. J. Appl. Phys., 2007. **46**: p. L913-L916.
97. Roddaro, S., *et al.*, *The Optical Visibility of Graphene: Interference Colors of Ultrathin Graphite on SiO2.* Nano Letters, 2007. **7**(9): p. 2707-2710.
98. Palik, E.D., *Handbook of Optical Constants of Solids.* Academic Press: New York, 1991.
99. Anthony, J.W., *et al.*, *Handbook of Mineralogy.* Mineral Data Publishing, 2000.
100. Low, C.G. and Q. Zhang, *Ultra-thin and Flat Mica as Gate Dielectric Layers.* Small, 2012. **8**(14): p. 2178-2183.
101. Castellanos-Gomez, A., *et al.*, *Atomically Thin Mica Flakes and Their Application as Ultrathin Insulating Substrates for Graphene.* Small, 2011. **7**(17): p. 2491-2497.
102. Li, H., *et al.*, *Rapid and Reliable Thickness Identification of Two-Dimensional Nanosheets Using Optical Microscopy.* ACS Nano, 2013. **7**(11): p. 10344-10353.
103. Fukuma, T., *et al.*, *Atomic-Scale Distribution of Water Molecules at the Mica-Water Interface Visualized by Three-Dimensional Scanning Force Microscopy.* Physical Review Letters, 2010. **104**(1): p. 016101.
104. Rudenko, A.N., *et al.*, *Graphene adhesion on mica: Role of surface morphology.* Physical Review B, 2011. **83**(4): p. 045409.
105. Novoselov, K.S., *et al.*, *Two-dimensional atomic crystals.* Proceedings of the National Academy of Sciences of the United States of America, 2005. **102**(30): p. 10451-10453.
106. Li, J., *et al.*, *Fabrication of carbon nanotube field effect transistors by AC dielectrophoresis method.* Carbon, 2004. **42**(11): p. 2263-2267.
107. Li, J., *et al.*, *Manipulation of carbon nanotubes using AC dielectrophoresis.* Applied Physics Letters, 2005. **86**(15): p. 153116.
108. Jingqi, L., *et al.*, *Influence of Triton X-100 on the characteristics of carbon nanotube field-effect transistors.* Nanotechnology, 2006. **17**(3): p. 668.

109. Durrer, L., *et al. SWNT Growth by LPCVD on Ferritin-Based Iron Catalyst Nanoparticles Towards CNT Sensors*. in *Solid-State Sensors, Actuators and Microsystems Conference, 2007. TRANSDUCERS 2007. International*. 2007.
110. Imam, S.-A., N. Kalam, and S. Abdhullah, *Temperature Dependence of Carbon Nanotube Field Effect Transistor under Non-Ballistic Conduction Considering Different Dielectric Materials.* Nanoscience and Nanotechnology, 2014. **4**(3): p. 52-58.
111. Martel, R., *Ambipolar electrical transport in semiconducting single-wall carbon nanotubes.* Phys. Rev. Lett., 2001. **87**: p. 256805-256805.
112. Kim, T., *et al.*, *Electrical transport in small bundles of single-walled carbon nanotubes: Intertube interaction and effects of tube deformation.* Applied Physics Letters, 2010. **96**(17).
113. Franklin, A.D., *et al. Can carbon nanotube transistors be scaled without performance degradation?* in *Electron Devices Meeting (IEDM), 2009 IEEE International*. 2009.
114. Cui, X., *et al.*, *Controlling Energy-Level Alignments at Carbon Nanotube/Au Contacts.* Nano Letters, 2003. **3**(6): p. 783-787.
115. Heinze, S., *et al.*, *Unexpected scaling of the performance of carbon nanotube Schottky-barrier transistors.* Physical Review B, 2003. **68**(23): p. 235418.
116. Jing, G., S. Datta, and M. Lundstrom, *A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors.* Electron Devices, IEEE Transactions on, 2004. **51**(2): p. 172-177.
117. Radosavljevi, M., *Drain voltage scaling in carbon nanotube transistors.* Appl. Phys. Lett., 2003. **83**(12): p. 2435.
118. Yang, D.J., *et al.*, *Memory effects of carbon nanotube-based field effect transistors.* Diamond and Related Materials. **13**(11-12): p. 1967-1970.
119. Aguirre, C.M., *et al.*, *The Role of the Oxygen/Water Redox Couple in Suppressing Electron Conduction in Field-Effect Transistors.* Advanced Materials, 2009. **21**(30): p. 3087-3091.
120. Derycke, V., *Controlling doping and carrier injection in carbon nanotube transistors.* Appl. Phys. Lett., 2002. **80**(15): p. 2773.
121. Avouris, P., *et al.*, *Carbon nanotube transistors and logic circuits.* Physica B: Condensed Matter, 2002. **323**(1-4): p. 6-14.
122. Francois Leonard and J. Tersoff, *Role of Fermi-Level Pinning in Nanotube Schottky Diodes.* Physical Review Letters, 2000. **84**(20): p. 4693.
123. S. Ramo, J.R.W., and T. V. Duzer, *Fields and Waves in Communication Electronics.* 1994.
124. Li, H. and Q. Zhang, *Global and local charge trapping in carbon nanotube field-effect transistors.* Nanotechnology, 2008. **19**: p. 175203.
125. Xiong, K., *et al.*, *Defect energy levels in HfO2 high-dielectric-constant gate oxide.* Applied Physics Letters, 2005. **87**(18): p. 183505.
126. Wilk, G., R. Wallace, and J.W. Anthony, *High-k gate dielectrics: Current status and materials properties considerations.* Journal of Applied Physics, 2001. **89**(10).
127. Robertson, J., *High Dielectric Constant Oxides.* The European Physical Jornal Applied Physics, 2004. **28**(03).
128. Huang, P.Y., *et al.*, *Grains and grain boundaries in single-layer graphene atomic patchwork quilts.* Nature, 2011. **469**(7330): p. 389-392.

129. Yazyev, O.V. and S.G. Louie, *Electronic transport in polycrystalline graphene.* Nat Mater, 2010. **9**(10): p. 806-809.
130. Meyer, J.C., *et al.*, *The structure of suspended graphene sheets.* Nature, 2007. **446**(7131): p. 60-63.
131. Zhu, W., *et al.*, *Structure and Electronic Transport in Graphene Wrinkles.* Nano Letters, 2012. **12**(7): p. 3431-3436.
132. Ishigami, M., *et al.*, *Atomic Structure of Graphene on SiO2.* Nano Letters, 2007. **7**(6): p. 1643-1648.
133. Suk, J.W., *et al.*, *Enhancement of the Electrical Properties of Graphene Grown by Chemical Vapor Deposition via Controlling the Effects of Polymer Residue.* Nano Letters, 2013. **13**(4): p. 1462-1467.
134. Reina, A., *et al.*, *Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition.* Nano Letters, 2008. **9**(1): p. 30-35.
135. Shi, Y., *et al.*, *Effective doping of single-layer graphene from underlying SiO_{2} substrates.* Physical Review B, 2009. **79**(11): p. 115402.
136. Dean, C.R., *et al.*, *Boron nitride substrates for high-quality graphene electronics.* Nat Nano, 2010. **5**(10): p. 722-726.
137. Gorbachev, R.V., *et al.*, *Hunting for Monolayer Boron Nitride: Optical and Raman Signatures.* Small, 2011. **7**(4): p. 465-468.
138. Xue, J., *et al.*, *Scanning tunnelling microscopy and spectroscopy of ultra-flat graphene on hexagonal boron nitride.* Nat Mater, 2011. **10**(4): p. 282-285.
139. Kim, E., *et al.*, *Chemical vapor deposition-assembled graphene field-effect transistor on hexagonal boron nitride.* Applied Physics Letters, 2011. **98**(26): p. 262103-3.
140. Ponomarenko, L.A., *et al.*, *Effect of a High-κ Environment on Charge Carrier Mobility in Graphene.* Physical Review Letters, 2009. **102**(20): p. 206603.
141. Low, C.G., *et al.*, *Graphene Field Effect Transistors with Mica as Gate Dielectric Layers.* Small, 2014. **10**(20): p. 4213-4218.
142. Li, X., *et al.*, *Large-Area Synthesis of High-Quality and Uniform Graphene Films on Copper Foils.* Science, 2009. **324**(5932): p. 1312-1314.
143. Liang, X., *et al.*, *Toward Clean and Crackless Transfer of Graphene.* ACS Nano, 2011. **5**(11): p. 9144-9153.
144. Li, X., *et al.*, *Transfer of Large-Area Graphene Films for High-Performance Transparent Conductive Electrodes.* Nano Letters, 2009. **9**(12): p. 4359-4363.
145. Suk, J.W., *et al.*, *Transfer of CVD-Grown Monolayer Graphene onto Arbitrary Substrates.* ACS Nano, 2011. **5**(9): p. 6916-6924.
146. Ni, G.-X., *et al.*, *Quasi-Periodic Nanoripples in Graphene Grown by Chemical Vapor Deposition and Its Impact on Charge Transport.* ACS Nano, 2012. **6**(2): p. 1158-1164.
147. Calado, V.E., *et al.*, *Formation and control of wrinkles in graphene by the wedging transfer method.* Applied Physics Letters, 2012. **101**(10): p. -.
148. Bae, W.K., *et al.*, *Multicolored Light-Emitting Diodes Based on All-Quantum-Dot Multilayer Films Using Layer-by-Layer Assembly Method.* Nano Letters, 2010. **10**(7): p. 2368-2373.
149. Lemme, M.C., *et al.*, *Mobility in graphene double gate field effect transistors.* Solid-State Electronics, 2008. **52**(4): p. 514-518.
150. Tan, Y.W., *et al.*, *Measurement of Scattering Rate and Minimum Conductivity in Graphene.* Physical Review Letters, 2007. **99**(24): p. 246803.

151. Hwang, E.H., S. Adam, and S. Das Sarma, *Carrier transport in two-dimensional graphene layers.* Phys. Rev. Lett., 2007. **98**: p. 186806.
152. Moon, J.S., *et al.*, *Epitaxial-Graphene RF Field-Effect Transistors on Si-Face 6H-SiC Substrates.* IEEE Electron Device Letters, 2009. **30**(6): p. 650-652.
153. Ni, Z., *et al.*, *Raman spectroscopy and imaging of graphene.* Nano Research, 2008. **1**(4): p. 273-291.
154. Ferrari, A.C., *et al.*, *Raman Spectrum of Graphene and Graphene Layers.* Physical Review Letters, 2006. **97**(18): p. 187401.
155. Venugopal, A., *et al.*, *Effective mobility of single-layer graphene transistors as a function of channel dimensions.* Journal of Applied Physics, 2011. **109**(10): p. 104511-5.
156. Kim, S., *et al.*, *Realization of a high mobility dual-gated graphene field-effect transistor with Al[sub 2]O[sub 3] dielectric.* Applied Physics Letters, 2009. **94**(6): p. 062107-3.
157. Fallahazad, B., *et al.*, *Dielectric thickness dependence of carrier mobility in graphene with HfO2 top dielectric.* Applied Physics Letters, 2010. **97**(12): p. -.
158. Venugopal, A., *et al.*, *Effective mobility of single-layer graphene transistors as a function of channel dimensions.* Journal of Applied Physics, 2011. **109**(10): p. -.
159. Fasolino, A., J.H. Los, and M.I. Katsnelson, *Intrinsic ripples in graphene.* Nat Mater, 2007. **6**(11): p. 858-861.
160. Katsnelson, M.I. and A.K. Geim, *Electron scattering on microscopic corrugations in graphene.* Philosophical Transactions of the Royal Society A: Mathematical, Physical and Engineering Sciences, 2008. **366**(1863): p. 195-204.
161. Guo, J. and M. Lundstrom, *Role of phonon scattering in carbon nanotube field-effect transistors.* Applied Physics Letters, 2005. **86**(19): p. 193103-3.
162. Wu, Y., *et al.*, *State-of-the-Art Graphene High-Frequency Electronics.* Nano Letters, 2012. **12**(6): p. 3062-3067.
163. Jena, D. and A. Konar, *Enhancement of Carrier Mobility in Semiconductor Nanostructures by Dielectric Engineering.* Physical Review Letters, 2007. **98**(13): p. 136805.
164. Konar, A. and D. Jena, *Tailoring the carrier mobility of semiconductor nanowires by remote dielectrics.* Journal of Applied Physics, 2007. **102**(12): p. -.
165. Jang, C., *et al.*, *Tuning the Effective Fine Structure Constant in Graphene: Opposing Effects of Dielectric Screening on Short- and Long-Range Potential Scattering.* Physical Review Letters, 2008. **101**(14): p. 146805.
166. Liao, L., *et al.*, *Top-Gated Graphene Nanoribbon Transistors with Ultrathin High-k Dielectrics.* Nano Letters, 2010. **10**(5): p. 1917-1921.
167. Liao, L., *et al.*, *High-Performance Top-Gated Graphene-Nanoribbon Transistors Using Zirconium Oxide Nanowires as High-Dielectric-Constant Gate Dielectrics.* Advanced Materials, 2010. **22**(17): p. 1941-1945.
168. Zhu, W., *et al.*, *Silicon Nitride Gate Dielectrics and Band Gap Engineering in Graphene Layers.* Nano Letters, 2010. **10**(9): p. 3572-3576.
169. RadisavljevicB, *et al.*, *Single-layer MoS2 transistors.* Nat Nano, 2011. **6**(3): p. 147-150.
170. He, K.T., *et al.*, *Scanning Tunneling Microscopy Study and Nanomanipulation of Graphene-Coated Water on Mica.* Nano Letters, 2012. **12**(6): p. 2665-2672.

171. Shim, J., *et al.*, *Water-Gated Charge Doping of Graphene Induced by Mica Substrates.* Nano Letters, 2012.
172. Sojoudi, H., *et al.*, *Impact of post-growth thermal annealing and environmental exposure on the unintentional doping of CVD graphene films.* Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures, 2012. **30**(4): p. 041213-6.
173. Farmer, D.B., *et al.*, *Chemical Doping and Electron−Hole Conduction Asymmetry in Graphene Devices.* Nano Letters, 2008. **9**(1): p. 388-392.
174. Pirkle, A., *et al.*, *The effect of chemical residues on the physical and electrical properties of chemical vapor deposited graphene transferred to SiO[sub 2].* Applied Physics Letters, 2011. **99**(12): p. 122108-3.
175. Huard, B., *et al.*, *Evidence of the role of contacts on the observed electron-hole asymmetry in graphene.* Physical Review B, 2008. **78**(12): p. 121402.
176. Pershin, S., *Raman spectroscopy of the OH group vibrations in structural complexes of liquid water.* Optics and spectroscopy, 2005. **98**(4): p. 543-554.
177. Kolesov, B., *Raman investigation of H2O molecule and hydroxyl groups in the channels of hemimorphite.* American Mineralogist, 2006. **91**(8-9): p. 1355-1362.
178. Kim, J.-S., *et al.*, *Between scylla and charybdis: Hydrophobic graphene-guided water diffusion on hydrophilic substrates.* Scientific reports, 2013. **3**.
179. Aziza, Z.B., Q. Zhang, and D. Baillargeat, *Graphene/mica based ammonia gas sensors.* Applied Physics Letters, 2014. **105**(25): p. 254102.