High Performance RF CMOS VCO Design for Integrated Frequency Synthesizers

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A thesis submitted to the
Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor Philosophy of Engineering

2006

STATEMENT OF ORIGINALITY

I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

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ABSTRACT

Fully integrated frequency synthesizers have been widely adopted for the wireless communication, data communication and optical communication systems to produce precise local oscillator (LO) signals for the channel selection. A frequency synthesizer is required to have a low phase noise in order to prevent the unwanted signals mixing with the interferences. A major challenge in the design of a fully integrated frequency synthesizer is the design of the voltage controlled oscillator (VCO) that affects the noise performance and power consumption of a synthesizer directly. The phase noise of the VCO is one of the most critical parameters for the quality and reliability of the information transfer. The objective of this project is to design high performance LC VCOs for integrated frequency synthesizers.

In this thesis, two methodologies have been proposed and developed. The first methodology is proposed for optimizing the phase noise of a cross-coupled LC VCO. The fundamental relationship between the phase noise and the channel length of the cross-coupled MOS transistors is theoretically derived, and an optimized channel length of MOS transistors is derived in order to achieve the lowest phase noise. Based on this methodology, two CMOS LC VCOs have been designed and realized using 0.18 μm CMOS technology, one operates around 2 GHz with lower phase noise performance compared with the state of the art designs reported in the literatures, and the other operates around 10 GHz with good performances. A dual band 52/104 GHz millimeter microwave (MMW) LC VCO using IBM 6HP BiCMOS technology which has the cut-off frequency (f_t) of CMOS of 55 GHz has been developed.

The second methodology is proposed to find the relationship between the loop parameters and the noise transfer functions for a charge pump phase locked loop (CPLL) based frequency synthesizer. Three main noise transfer functions of the CPLL based frequency synthesizers are derived in the s-domain and z-domain. By comparing the s-domain model to the z-domain model, it is observed that the noise peak from the inherent sampling behaviors always exists in the loop, and the loop filter with the wide loop bandwidth cannot suppress this peak. On the other hand, such a noise peak causes the instability of the frequency synthesizer. A stability limitation, which depends on the phase margin and the ratio between the reference frequency and the loop bandwidth, is extracted by the simulation in the z-domain analysis.

The design of a fully integrated CPLL for Bluetooth has been completed using the CSM CMOS 0.18 μm technology base on the second methodology. A programmable pulse swallow frequency divider operated at 2.45 GHz is used, in which a 32/33 dual modulus prescaler, a program counter and a swallow counter are utilized. The simulated phase noise of the proposed frequency synthesizer is −112 dBc/Hz at 3 MHz offset frequency. The spurious tone is around −68 dBc at the offset frequency of 1 MHz, and the settling time is around 22 μs. The power consumption is around 31 mW for the supply voltage of 1.8 V.

Acknowledgment

I have been extremely fortunate to have met and dealt with so many people during my Ph.D. work at NTU, I awe so many thanks to so many people and here is the place to express my deepest gratitude to all of them.

I would like to express my deepest gratitude to my supervisor, Professor Yeo Kiat Seng and Professor Ma Jian Guo, for all the guidance and support, they provided throughout my Ph.D. work. Their rigorous attitude to do the research and inspiring thinking to solve problems are invaluable for my professional career.

I am greatly indebted and respectful to Professor Do Manh Anh for their encouragements and supports.

I'd like to express my heartfelt thanks to the help of CICS faculty and staff members, Tsoi Mun Keong, Tan Min Lin, Guee Geok Lian, Gan Siew Kim, Chan Nai Hong, Seow Yang Hing and Sia Liang Poo for their helps of the CAD tools, measurement equipments, etc..

During the course of my Ph.D work, I worked with a long list of extremely talented fellow students. From each of them, I learned something valuable and I believe being in such a talented group of students has added so much to my learning experience. I would like to appreciate my fellow graduate students in CICS. There are too many to mention, Fan Xian Ping, Yu Xiao Peng, Cabuk Alper, Ma Kai Xue, Mou Shou Xian, Boon Chirn Chye, Tan Chee Yuen and Lim Wei Meng. To me, the friendship between CICS members is a big treasure. Their hardworking, perseverance, sharing, and self-motivate always are amazing me.

I would like to thank my parents and parents in law in China for having so much confidence in me and for their continuous love & support.

Last but not least, I would like to express my deepest thanks to my husband, Sun Ju Tao, for his consistent love and patience, support, understanding, and encouragement. Finally, I would like to thank my cute, clever and beautiful daughter, Sunny Sun Jia Qian for her love.

CONTENT TABLE

FIGURE TABLE

TABLE LIST

CHAPTER 1

Introduction

1.1 Motivation

Modern transceivers for wireless communications consist of low noise amplifiers (LNA), power amplifiers (PA), mixers, digital signal processors (DSP) chips, filters, and frequency synthesizers etc.. These building blocks have been realized using hybrid technologies in the past. It has become increasingly attractive to design and monolithically integrate all these building blocks on a single chip [1].

In data communications, such as serial links and disk–drive read channels, frequency synthesizers are used as clock recovery systems [1]. In broadband optical communication networks, frequency synthesizers are adopted as the clock and data recovery (CDR) to generate the clock and retime the data from the received electrical signals [2] [3] [4]. In wireless communications, they are used to synthesize an accurate frequency. In all above mentioned applications, the random temporal variation of the phase or phase noise is one of the most critical performance parameters because it can lead to data transmission errors and functionality failure. However, to design a fully integrated frequency synthesizer for a wireless communication system is, as always, desirable but the most challenging. The first requirement is to achieve a high–frequency operation within reasonable levels of the power consumption. Two more critical requirements concern the phase noise and spurious–level performance. The fourth requirement is to reduce the cost of the monolithic system integration, where a small chip area is essential [5] [6].

The Bluetooth standard defines a short–range wireless connection among mobile computers, mobile phones, portable handheld devices, and the connectivity to the internet [7]. It specifies a 2.4 GHz frequency–hopped spread–spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices without the need for wires or cabling of any kind. The frequency synthesizer in the Bluetooth is required to have the precise channel spacing and low phase noise to meet the stringent noise specification and to prevent unwanted signals mixing with the interferences. Most existing frequency synthesizers are implemented in silicon germanium (SiGe) or bipolar technologies, and use several external devices such as the loop filter. Because of the cost and power consumption requirements, heavily integrated CMOS RF frequency synthesizers for the Bluetooth applications are crucial and worthy to explore.

The LC VCO is one of the most important building blocks in the fully integrated frequency synthesizers. Due to the increasing demand for the bandwidth, the requirements are placed on the spectral purity of the fully integrated LC oscillators. While some designers attempt to improve the phase noise performance by increasing the quality factor of the LC tank through the implementation of bond–wire [8] or special layout technique [9], others seek to improve the phase noise performance through maximizing the oscillation amplitudes [9]. The former increases the cost due to the complicated technology, while the latter increases the power consumption and reduces the frequency tuning range. In spite of these endeavors, the design and optimization of integrated LC VCOs still pose many challenges to circuit designers as far as the simultaneous optimization of multiple variables is required.

Although many phase noise models have been developed for different types of oscillators, each of these models makes some restrictive assumptions applicable only to a limited class of oscillators. Most of these models are based on the assumption of a linear time invariant (LTI) system and they do not have a complete mechanism of the electrical noise sources [10] [11] [12] to describe how the device noise becomes the phase noise. Therefore, those models are incapable of making accurate predictions for the phase noise in oscillators because the oscillator is a periodically time varying system. Even the phase noise model reported in [8] takes into account linearity time variance (LTV), it still can not evaluate accurately the phase noise of an LC VCO directly due to the limitation of the device noise mechanism and the complicated simulation.

In recent years, the 10 Gb/s optical communication system (OC-192) market has been growing rapidly and moving towards high–data–rate applications. High frequency low phase noise oscillators are critical to the building blocks in a frequency synthesizer design for the applications. CMOS processes typically achieve f_T in excess of 50 GHz to make the processes an alternative for low noise circuits operating at these higher frequencies [13] [14] [15] [16] [17]. CMOS oscillators with integrated inductors and P+/Nwell varactors are suitable for such applications. Even though a significant amount of research work has been carried out [13], the CMOS VCO operating at such a high frequency band is still a challenge for the designers. Two papers have been published for the 10 GHz–band VCO adopted CMOS technologies, for example, one is LC delay line VCO with the tuning range of 225 MHz, the phase nose of −75 dBc/Hz at the offset frequency of 100 kHz and the power consumption of 70 mW [13]; The other one is a ring–coupled quadrature (RCQ) VCO with the tuning range of 2.5 GHz, the phase noise

of −80 dBc/Hz at the offset frequency of 100 kHz and the power consumption of 45 mW [14]. The main issue for the recent VCO research is to achieve a monolithic integration while the low phase noise with wide frequency tuning range and low power consumption at given higher operating frequencies are satisfied as well.

The increasing demand for the high speed data rate in communication system, for example, the OC-768 standard proposed in [18], which operates at 40 GHz for a full rate operation, has led to a new challenge to the design of a fully integrated circuit. The next generation of the optical network that will eventually replace the OC−768 will operate at a frequency beyond 100 GHz. Thus a millimeter microwave VCO with a high operation frequency is getting more and more desirable for such applications. To date, most of the required VCOs operating at such a high frequency have been designed using GaAs/InP technologies [18]. However, this technology is very expensive. Using the matured SiGe technology to design MMW VCOs is still a challenge. Another major obstacle in MMW VCO design is the difficult to achieve the high operation frequency with a high output power and low phase noise at the low supply voltage. The difficulty becomes greater when the oscillating frequency approaches the cut−off frequency f_T of the CMOS due to the decrease of gain and the increase of noise. Therefore, the cut−off frequency limits the maximum oscillation frequency of the VCO. Thus, the design of MMW VCOs with good performances through a special circuit architecture and an advance technology will be very meaningful.

1.2 Objectives

The objectives of this thesis focus on as follows:

- To explore a method to optimize the phase noise performance of the LC VCO.
- To realize LC VCOs with a low phase noise and a low power consumption for wireless communication, data communication and optical communication.
- To design LC VCOs that the operation frequency is higher than the cut-off frequency of the active devices for millimeter microwave application.
- To find a method to optimize the loop parameters and the noise performance of the CPLL.
- To develop a fully integrated CPLL based frequency synthesizer with good performance for Bluetooth applications.

1.3 Major Contributions of the Thesis

The major contributions of the thesis are as follows:

(1) A methodology is proposed to optimize the phase noise of a cross–coupled LC VCO. The fundamental relationship between the phase noise and the channel length of the cross–coupled MOS transistors is derived. An optimum channel length of MOS transistors is obtained theoretically for the cross–coupled LC VCO with the lowest phase noise. Based on this methodology, two CMOS LC VCOs have been realized and one BiCMOS MMW LC VCO has been developed:

- A 2 GHz LC VCO is fabricated by using the CSM 0.18 μm CMOS technology. The measured phase noise is −103.3 dBc/Hz at 100 kHz offset and −118.9 dBc/Hz at 600 kHz offset from the carrier frequency of 1.968 GHz with a low-

power consumption of 3.15 mW. The FOM value of 186 is achieved. The frequency tuning range is 280 MHz from 1.9 GHz to 2.18 GHz.

- A 10 GHz LC VCO is fabricated using the CSM 0.18 μm CMOS technology. The measured phase noise is around −89 dBc/Hz at 100 kHz offset from the carrier frequency of 9.83 GHz. The frequency tuning range of the LC VCO is 1.1 GHz from 9.4 GHz to 10.5 GHz. The power consumption of the fabricated LC VCO circuit is 5.8 mW.
- A BiCMOS millimeter microwave LC VCO has been developed. This VCO operates at the dual-band frequency of 52 GHz/ 104 GHz base on the IBM 6HP BiCMOS technology which has the cut-off frequency of CMOS of 55 GHz. From the post-layout simulations, a tuning range of 1.05 GHz, a peak-to-peak buffer output voltage of 1.2 V, and low phase noise of −107.3 dBc/Hz at 600 kHz offset from the carrier frequency of 52 GHz are achieved. The tuning range of 2.1 GHz, the peak-to-peak buffer output voltage of 0.5 V, and low phase noise of −101.4 dBc/Hz at 600 kHz offset from the carrier frequency of 104 GHz are obtained as well. The operating frequencies are near to or higher than f_T.

(2) A methodology is proposed to find the relationship between the loop parameters and the noise transfer functions of a CPLL based frequency synthesizer. Three main noise transfer functions of the CPLL based frequency synthesizers are derived in the s-domain and z-domain. By comparing the s-domain model to the z-domain model, it is observed that the noise peak from the inherent sampling behaviors always exists in the loop, and the loop filter with the wide loop bandwidth cannot suppress this peak. On the other hand, such a noise peak causes the instability of the frequency

synthesizer. A stability limit, which depends on the phase margin and the ratio between the reference frequency and the loop bandwidth for the wide loop bandwidth frequency synthesizer, is extracted by the simulation in the z-domain analysis and verified by Radio Frequency Hardware Description Language (RFHDL). Based on this methodology, a fully integrated CPLL based frequency synthesizer for Bluetooth has been completed using the CMOS 0.18 μm technology as a design demonstration.

1.4 Organization of the Thesis

This thesis is organized into eight chapters. The current chapter provides an introduction to the problem addressed and an outline of the thesis. The fundamentals of the PLL based frequency synthesizer will be discussed in Chapter 2. The main concepts of the frequency synthesizer are studied, and the low frequency building blocks in frequency synthesizers, such as the phase frequency detector (PFD), the frequency divider, the loop filter are investigated. An overview of the LC VCO will be introduced and the existing phase noise models will be discussed.

Chapter 3 proposes a novel methodology to achieve the minimal phase noise of the cross–coupled LC VCO by optimizing the size of active devices. A linear time invariant phase noise analysis is introduced. The simulations and experiments to verify the novel methodology are presented in Chapter 4, in which a 2 GHz and a 10 GHz LC VCOs are designed, implemented and measured.

In Chapter 5, a methodology on the loop parameters' optimization of the CPLL based frequency synthesizer is proposed. The relationship between the loop parameters and

three main noise transfer functions of the CPLL based frequency synthesizer is discussed in the s–domain model and z–domain model. The stability margin is extracted using the z–domain analysis. Chapter 6 presents a fully integrated CPLL based frequency synthesizer for the Bluetooth application as a design example using the 0.18 μm CMOS technology.

In Chapter 7, a dual band 52/104 GHz MMW LC VCO is designed using IBM 6HP BiCMOS technology with f_T of 55 GHz.

Finally, Chapter 8 concludes the thesis with a summary of the results and a list of key research areas for the further investigations.

CHAPTER 2

Fundamental of the Frequency Synthesizer

In this chapter, the fundamental and the main concepts of frequency synthesizers are introduced. The effects of the phase noise and the spurious tones on the performance of a frequency synthesizer are presented. Subsequently, all building blocks of the frequency synthesizer are discussed, which include the phase frequency detector (PFD), loop filter (LF), charge pump (CP), divider and oscillator.

2.1 Phase Locked Loop Based Frequency Synthesizers

2.1.1 Phase Locked Loop

A phase locked loop is a circuit that synchronizes an output signal and an input signal in frequency as well as in phase. In the synchronized or locked state, the phase error between the output signal and the input signal is zero or very small. If a phase error builds up, a control mechanism redirects the output signal in order to minimize the phase error with aspect to the input signal. The phase of the output signal is actually locked to the phase of the input signal hence a phase locked loop.

Fig.2.1 shows the basic components of a PLL, a phase detector (PD), a loop filter, a VCO and optionally a frequency divider. The phase detector compares the phase of the input signal with the divided phase of the VCO's output. The output of the phase detector is a measure of the phase difference between these two inputs. The difference voltage is then filtered by the loop filter and applied to the control input of the VCO. The controlled

voltage on the VCO changes the frequency in the direction that reduces the phase difference between the input signal and local oscillator.

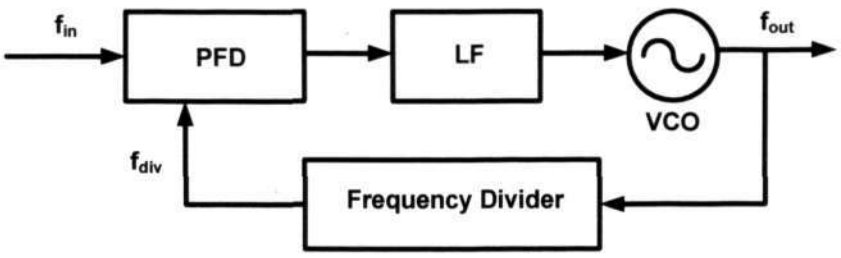


Fig. 2.1 Basic phase locked loop.

2.1.2 Phase Locked Loop Based Frequency Synthesizer Operation

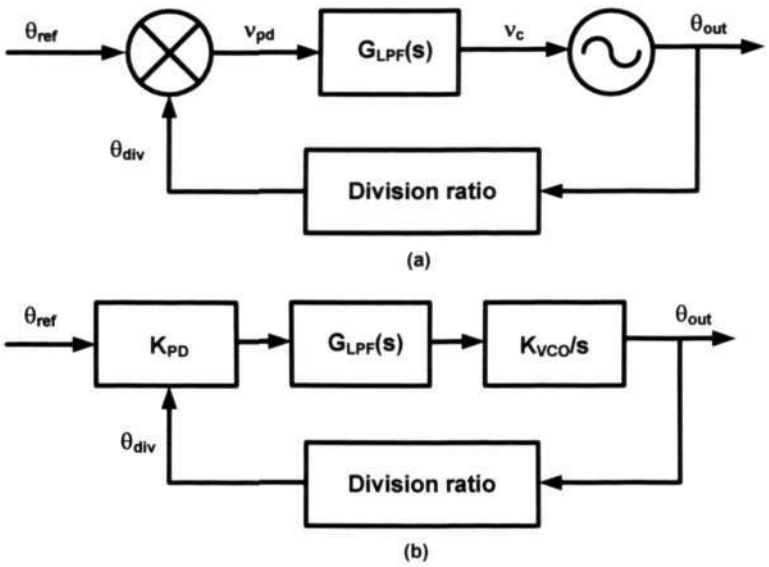


Fig. 2.2 (a) Basic block diagram with state variables, (b) Basic linear time invariant PLL model.

In general, PLL acts as a frequency synthesizer by locking the output frequency to a multiple of the very clean reference frequency, which is depending on the frequency divider as pointed in Fig.2.1, so namely, PLL based frequency synthesizer. The output frequency generated by the VCO is divided by a division ratio of the frequency divider.

For simply derivation, we use an integer N as the division ratio here, while it is also suitable for the analysis of the fractional N divider. The phase of the divided frequency is compared with the phase of the reference frequency $f_{in}=f_{ref}$, generated by a crystal oscillator normally. The voltage output signal of the phase detector is proportional to the phase difference between both inputs, which is consisted of an AC and a DC component. The DC component is accumulated and the unwanted AC component is suppressed by the low pass loop filter. The resulting signal is a DC signal with a small superimposed AC signal, which serves as the control voltage for the VCO. Adjusting the output frequency of the VCO such that the output frequency of the divider is equal to the reference frequency or the difference between both is a constant, thus the frequency synthesizer is called locked. The frequency synthesizer is in lock and the output frequency equals:

$$f_{out} = N \cdot f_{ref} \tag{2.1}$$

The basic block diagram of the PLL based frequency synthesizer with its state variables and the linear model of the PLL based frequency synthesizer are given in Fig.2.2. The reference signal has a phase $\theta_{ref}(t)$ and the VCO output has a phase $\theta_{out}(t)$. The frequency divider divides the VCO frequency by a factor N, and thus the VCO phase has:

$$\theta_{div}(t) = \frac{\theta_{out}(t)}{N} \tag{2.2}$$

When the loop is in lock, the output of the PD is a voltage proportional to the phase difference between the inputs:

$$v_{pd}(t) = K_{PD} \cdot [\theta_{ref}(t) - \theta_{div}(t)] \tag{2.3}$$

where K_{PD} is the phase detector gain in volts per radian. The phase error voltage v_{pd} is filtered by the loop filter, which normally has a low pass transfer characteristic. Noise and high frequency signals, i.e. the unwanted AC components, are suppressed. In addition, the loop filter determines the dynamic performance of the loop. The loop filter transfer function is given by $G_{LPF}(s)$, which will be discussed later.

The VCO frequency is determined by the control voltage v_c. Frequency changes due to the control voltage are given by $\Delta\omega = K_{VCO} \cdot v_c$, where K_{VCO} is the VCO gain in units of rad/Vs. Since the control voltage acts on the frequency, which is the derivative of the phase, the VCO operation is modeled by $d\theta_{out}(t)/dt = K_{VCO} \cdot v_c$. By taking the Laplace Transform we obtain:

$$\theta_{out}(s) = \frac{K_{VCO} \cdot v_c(s)}{s} \tag{2.4}$$

In Fig.2.2 (b), the linear model of the PLL can be viewed as a standard feedback system with a forward transfer function, $G_{Forward}(s) = K_{PD} \cdot G_{LPF} \cdot K_{VCO}/s$ and a feedback gain, $G_{Feed}(s) = 1/N$. The open loop transfer function is expressed as [19]:

$$G(s) = G_{Forward}(s) \cdot G_{Feed}(s) = \frac{K_{PD} \cdot G_{LPF}(s) \cdot K_{VCO}}{N \cdot s} = \frac{K_0}{sN} \tag{2.5}$$

while, $K_0 = K_{PD}K_{LF}K_{VCO}$, is the forward gain of the PLL in s−1 when the loop filter gain is chosen as $G_{LF}(s) = K_{LF}$.

This transfer function determines the static and dynamic performance of the loop. It also reveals the major issue in PLL designs and the loop bandwidth trade–off. For suppression of unwanted AC components, the loop bandwidth needs to be as narrow as possible, while for the dynamic performance the opposite is true.

2.2 Main Concepts of the Frequency Synthesizer

2.2.1 Phase Noise and Spurious Tones

An ideal output spectrum of a frequency synthesizer should be a single tone at the desired frequency in order to provide the prefect reference frequency for the frequency resolution. A single tone in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain. The random amplitude and phase deviations from the desired values produce the energy in the offset frequency rather than the desired frequency. When this energy is mixed with the received RF signal or modulated baseband signal, undesired sidebands are created. Phase noise and spurious tones are the two key parameters to measure the quality of a frequency synthesizer. In this section, we will discuss the mathematical model of phase noise and spurious tones and their effects on a transceiver.

The output of an ideal frequency synthesizer has a pure sinusoidal waveform of the frequency ω_0, i.e. $V_{out}(t) = A\sin(\omega_0 t + \theta)$ with the amplitude A and a fixed phase reference θ. In the frequency domain, this corresponds to a Dirac impulse at ω_0, $\delta(\omega_0)$. In a real oscillator, noise generates fluctuation on the phase and the amplitude of the signal. The output signal becomes:

$$V_{out}(t) = [A + \varepsilon(t)] \cdot \sin[\omega_0 t + \theta(t)] \tag{2.6}$$

where $\varepsilon(t)$ represents the amplitude fluctuations and $\theta(t)$ represents the phase fluctuations. Because the amplitude fluctuations can be removed or greatly reduced by the well–designed, high–quality oscillators, thus $\varepsilon(t)$ can be considered constant over the time. We concentrate on the phase fluctuations in a frequency synthesizer design. In general, the phase fluctuations are caused by the following three main sources:

1) Systematic variations, due to the aging of the resonator material for example, reduce the long term stability.
2) Deterministic periodic variations due to the unwanted frequency or phase modulations.
3) Random variations due to noise sources such as thermal noise, shot noise, flicker noise, and quantization noise in electronic components.

while $\theta(t)$ can be rewritten as:

$$\theta(t) = \eta \cdot t^2 + \sin(\omega_m t) + \varphi(t) \tag{2.7}$$

The first term represents a linear frequency drift since instantaneous frequency is the time rate of the change of phase divided by 2π, and it is usually small enough to be negligible. The second term represents the periodic phase modulation and it produces a spurious tone at an offset frequency of ω_m from the carrier frequency ω_0. Suppose that the phase fluctuation in equation (2.7) is a single sinusoidal tone in the phase $\theta(t) = \theta_m \cdot \sin(\omega_m t)$ with $\theta_m << 1$, then the output voltage becomes [19]:

$$V_{out}(t) \approx A\sin(\omega_0 t) + A \cdot \frac{\theta_m}{2}\{\sin[(\omega_0 + \omega_m)t] + \sin[(\omega_0 - \omega_m)t]\} \tag{2.8}$$

Thus, the output spectrum of the frequency synthesizer consists of a narrow band FM signal with the modulation index θ_m, resulting in a strong component at ω_0 and two spurious tones at $\omega_0 \pm \omega_m$ as given in Fig.2.3. The power ratio of the spurious tone to the carrier is $10\log(\frac{\theta_m}{2})^2$, and the unit for the spurious tone is dBc. That means that the power of the spurious modulation is $10\log(\frac{\theta_m}{2})^2$ dBc.

The third term in equation (2.7) represents the random phase fluctuations. The spectral density of the phase noise is:

$$S_\varphi(\omega) = \int_{-\infty}^{\infty} R_\varphi(\tau) \cdot e^{-j\omega\tau} d\tau \tag{2.9}$$

Where, $R_\varphi(\tau) = E[\varphi(\tau) \cdot \varphi(t-\tau)]$, when amplitude fluctuations are negligible and the root–mean–square (rms) value of $\varphi(t)$ is much smaller than 1 radian, the spectral purity of $V_{out}(t)$ can be approximated as:

$$\begin{aligned} S_\theta(\omega) &= \frac{\theta_m^2}{2} \cdot \delta(\omega - \omega_m) \\ S_{Vout}(\omega) &\approx \frac{A^2}{2}\left[\delta(\omega-\omega_0) + \frac{1}{2}S_\theta(\omega-\omega_0) + \frac{1}{2}S_\theta(\omega_0-\omega)\right] \end{aligned} \tag{2.10}$$

The phase noise is specified in equation (2.11) as the ratio of the noise power P_{noise} in 1 Hz bandwidth at a certain offset frequency $\Delta\omega$ away from the carrier frequency ω_0 to the carrier power $P_{carrier}$, and the unit is dBc/Hz [19].

$$L(\Delta\omega) = 10\log(\frac{P_{noise}}{P_{carrier}}) = 10\log(\frac{S_{Vout}(\omega_0+\Delta\omega)}{A^2/2}) = 10\log(S_\theta(\Delta\omega)/2) \tag{2.11}$$

Since the phase noise spectrum can be seen as a sum of sines, the total noise skirt is directly translated to noise side lobes at both sides of the carrier frequency as given in Fig.2.3.

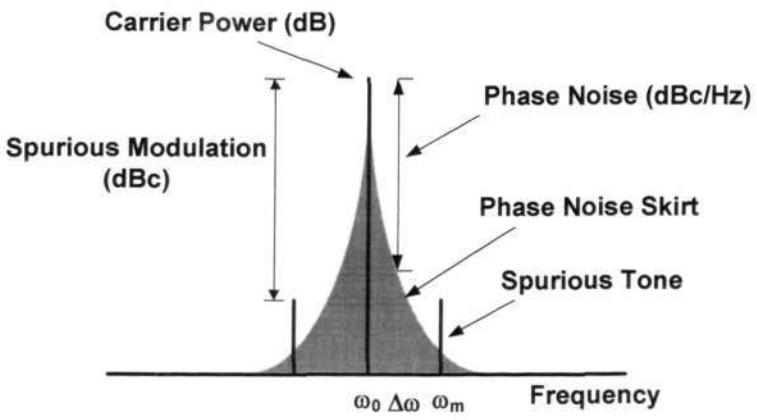


Fig. 2.3 Spectral purity definitions.

2.2.2 Effect of the Phase Noise and Spurious Tone on the Transceiver

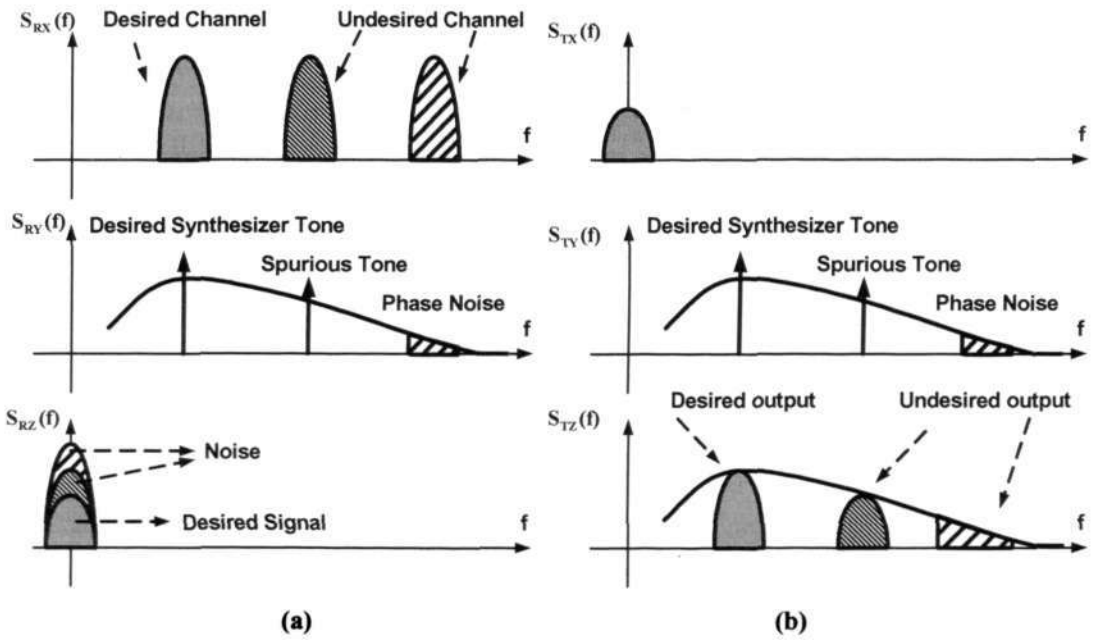


Fig. 2.4 Effect of the phase noise and spurious tones in (a) receiver, (b) transmitter.

Any noise in the circuit will create the phase disturbance as explained in Fig.2.4 for transmitter applications, in which a non–ideal frequency synthesizer spectrum is given. It is no longer a single frequency tone but rather a smeared version. The energy under the skirt is the phase noise, which is concentrated at offset frequencies rather than the desired frequency due to a spurious tone, its appearing looks like a spike above the skirt. The phase noise and spurious tones are the main performance parameters of a frequency synthesizer.

In a receiver, the phase noise and spurious tones of the frequency synthesizer can mix with the desired signal, and produce noise in the desired channel as shown in Fig.2.4 (a), which reduces the sensitivity and selectivity of a receiver. Similarly, in a transmitter, the spurious tones and the phase noise of the frequency synthesizer can mix with the modulated baseband signal and produce undesired spectral emissions as plotted in Fig.2.4 (b), which increase adjacent channel interference and reduce the modulation accuracy. Therefore, the phase noise and the spurious tone are required to be very low for the good performance of the frequency synthesizer.

2.2.3 Loop Dynamics

The derivations of the previous section were based on the steady–state operation of the PLL, i.e., a constant reference frequency is applied and the division modulus is fixed. However, the dynamic behavior of the loop is an equally important design parameter when the reference frequency or the division modulus is changed.

2.2.3.1 Tracking and Settling

First, the phase error $\theta_{err}(t) = \theta_{ref}(t) - \theta_{div}(t)$ for a specified input $\theta_{ref}(t)$ is studied, under the assumption that the loop is in lock, and that the phase error is sufficiently small to justify the linear calculus. Most important is the steady–state phase error $\theta_{err,ss}$, i.e. the value that $\theta_{err}(t)$ assumes after all the transients have died away. It is calculated using the final value theorem of the Laplace transformation $\lim_{t\to\infty}\theta(t) = \lim_{s\to\infty}[s\cdot\theta(s)]$. The resulting steady–state phase error for a first order loop is zero when the reference input is a phase step of $\Delta\theta$. However, when the input frequency changes with a step of size $\Delta\omega$, the resulting steady–state phase error is [20]:

$$\theta_{err,ss} = \lim_{s\to 0}\left[s\cdot\frac{\Delta\omega}{s^2}\frac{1}{1+K_0/(Ns)}\right] = \frac{\Delta\omega\cdot N}{K_0} = \frac{\Delta\omega}{\omega_c} \quad \text{and} \quad \omega_c = \frac{K_0}{N} \tag{2.12}$$

A frequency step happens when suddenly the division modulus in the synthesizer is changed in order to obtain a new output frequency. ω_c is the loop bandwidth of the synthesizer, i.e. the frequency at which the open loop gain is 0 dB. This frequency corresponds to the 3–dB cut–off frequency of the closed loop response of the PLL based frequency synthesizer. To keep the final error small, the forward gain K_0 or the loop bandwidth ω_c must be as high as possible.

The most important situation in a frequency synthesizer is the one where the division modulus N is changed, which is corresponding to a change in the input frequency $\Delta\omega_{in}$. The time for the first order loop to settle to the wanted output frequency is:

$$\theta_{err}(t) = \frac{\Delta\omega_{in}}{\omega_c}(1 - e^{-\omega_c t}) \tag{2.13}$$

Therefore, the final frequency is obtained after an exponential behavior with the time constant $1/\omega_c$. Time T_{settle} to settle the loop to the new output frequency within a specified accuracy ε is given as:

$$T_{settle} = -\frac{\ell n(\varepsilon)}{\omega_c} \tag{2.14}$$

while $\varepsilon = \frac{\Delta\omega_{acc}}{\Delta\omega}$ and $\Delta\omega_{acc}$ is the frequency accuracy. In general, ε is required as 10 ppm.

2.2.3.2 Acquisition

During the startup, the PLL is initially in an unlocked condition, the process of achieving lock state is called acquisition. Since the acquisition is inherently a non–linear process, its qualitative analysis is beyond the scope of this work. In this work, some descriptive analysis will be done, more information can be found in [20].

If the initial VCO frequency is close enough to $N \times f_{ref}$, the PLL will lock up with just a phase transient. The frequency range over, which no cycles will be missed before the lock is obtained, is called the lock range, $\Delta\omega_L$. If a reference frequency outside the lock range is applied, the pull–in process will be slower. The normal operation of the PLL is generally restricted to the lock range.

The pull–in range, $\Delta\omega_{PI}$, describes the PLL in a dynamic state or an acquisition mode. The pull–in range is the range within which a PLL will always become locked through the acquisition process [21]. If the reference frequency is outside the pull–in range, the PLL will not be able to lock onto the reference signal.

The hold range, $\Delta\omega_H$, describes the PLL in a static or locked state. The PLL is initially locked with the reference signal. If the reference signal's frequency changes too much, the PLL will lose lock at the edge of the hold–in range. The PLL is conditionally stable within the hold–in range [19]. The hold–in range is larger than both above defined ranges. As will be discussed in Section 2.3.1, the linear approximation of the phase error due to a frequency offset is shown to be $\theta_{err,ss} = \Delta\omega/K_F$. However, a real phase detector does not have an infinite linear range. For a sinusoidal–characteristic phase detector, the true expression should be $\sin\theta_{err,ss} \approx \Delta\omega / K_F$ [19]. Since the sine function cannot exceed the unit magnitude, there is no solution for $\Delta\omega > K_F$. The hold–in range therefore equals $\Delta\omega = \pm K_F$. Other types of phase detector, for example the charge pump phase–frequency detector, have a larger linear range and can therefore extend the hold–in range. However, these definitions are only valid as long as the limit is set by the phase detector and not by the other nonlinearity, such as the clipping in an operational amplifier (op–amp) or the VCO frequency tuning range.

2.3 Building Blocks of the PLL Based Frequency Synthesizer

2.3.1 Phase Detector/Phase Frequency Detector (PD/PFD)

Three categories of the phase detectors will be described shortly in this part. The analog phase detector of multiplier performs a mixing operation on its input signals and the resulting DC output is a measure of the phase error. Digital phase detectors are implemented using EXOR gates or in sequential way with flip–flops that trigger on the zero–crossings of their inputs. The third category, the phase frequency detector, is

actually also digital and sequential circuit and provides apart from the phase detection also frequency detection to aid the acquisition when the loop is out of lock.

2.3.1.1 Analog Phase Detectors

A multiplier acts as an analog phase detector through the trigonometric identity. Assume that both input signals to the multiplier are $v_1 = A_1 \sin(\omega_1 t + \theta_1)$ and $v_2 = A_2 \cos(\omega_2 t + \theta_2)$, the multiplier output signal will result in:

$$\begin{aligned} v_d &= K_m \cdot v_1 \cdot v_2 \\ &= \frac{1}{2} K_m \cdot A_1 \cdot A_2 \cdot \{\sin[(\omega_1 - \omega_2)t + \theta_1 - \theta_2] + \sin[(\omega_1 + \omega_2)t + \theta_1 + \theta_2]\} \\ &= A_d \cdot \{\sin[(\omega_1 - \omega_2)t + \theta_1 - \theta_2] + \sin[(\omega_1 + \omega_2)t + \theta_1 + \theta_2]\} \end{aligned} \quad (2.15)$$

where $A_d = \frac{1}{2} K_m A_1 A_2$, and K_m is the constant associated with the multiplier.

At the phase lock, both frequencies are the same and the DC component of the phase detector output equals to $A_d \sin(\theta_1 - \theta_2)$. This component indicates the phase difference of $(\theta_1 - \theta_2)$ between two signals. Various undesirable signals are also present the output, such as the sum of the two input frequencies. The loop filter will remove these unwanted signal components. One of the common implementation of the multiplier phase detector is the Gilbert multiplier [21].

The analog phase detector is especially useful in applications where the reference frequency is too high for other circuits and where the loop bandwidth is sufficiently narrow to effectively suppress the unwanted signals.

2.3.1.2 Exclusive OR Gate (EXOR gate)

Fig. 2.5 shows the EXOR gate phase detector. The operation of an EXOR gate phase detector is similar to an over–driven multiplier circuit and it has triangular phase detector

characteristics. However, square wave inputs of 50% duty cycle are recommended for the EXOR phase detector. For other duty cycles, the detection range may be significantly reduced. In addition, it is possible to have the same output voltage for two different phase errors [22]. The output waveforms for inputs A and B are shown in Fig.2.6 (a). The average value $\overline{C}$ of the output waveform is proportional to the phase difference between both input signals. The phase detector transfer characteristic is shown in Fig. 2.6 (b).

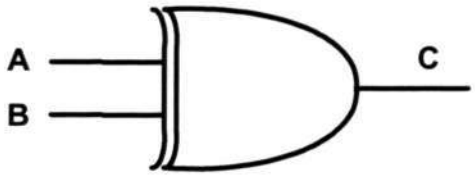


Fig. 2.5 EXOR gate phase detector.

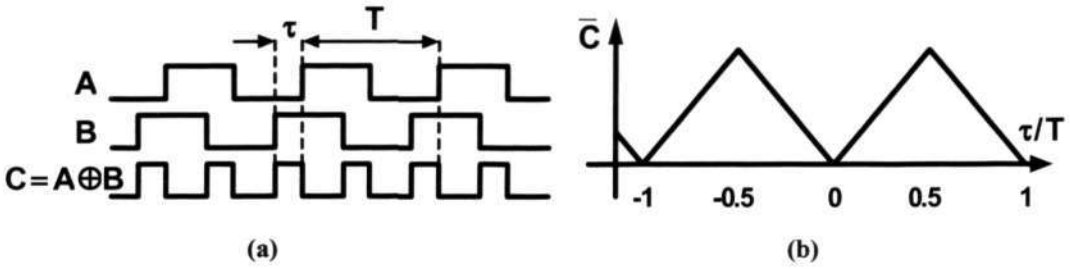


Fig. 2.6 (a) Operation of the EXOR phase detector, (b) Transfer function of the EXOR phase detector.

2.3.1.3 Flip–Flop Phase Detector (FFPD)

An edge–sensitive set–reset (SR) type of flip–flop can be used to detect the phase difference of pulse trains, which do not have 50% duty cycle. The flip–flop phase detector is shown in Fig.2.7 and Fig.2.8. The inputs A and B set and reset the output of this sequential circuit. The operation is again plotted for a negative phase difference. The average value of the output $\overline{C}$ has a sawtooth characteristic. The linear operating range of this phase detector is a full reference period and is centered on around $\pm\pi$ radians.

When the loop is in lock, the output of the phase detector has a component at the reference frequency with a magnitude of $4/\pi$ times the peak to peak range of the PD. Compared to the EXOR PD, the linear operating range is doubled, but the flip–flop is sensitive to the reference spurs. Of course, the same phase characteristic can be realized with the SR flip–flop.

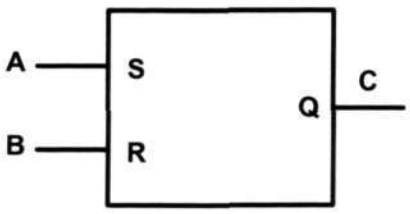


Fig. 2.7 Flip–flop phase detector.

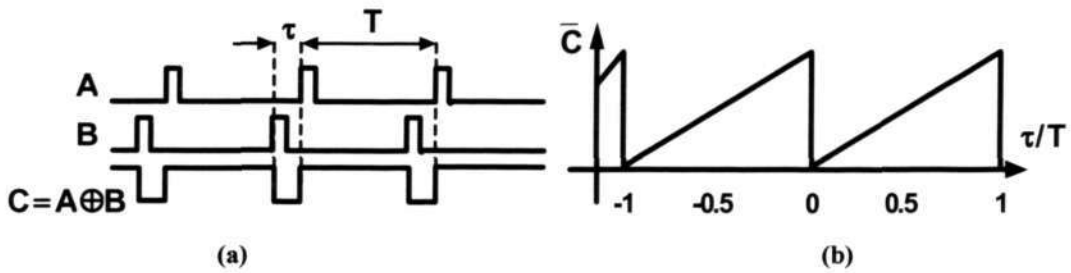


Fig. 2.8 (a) Operation of a flip–flop phase detector, (b) Transfer functions of a flip–flop phase detector.

2.3.1.4 Phase Frequency Detector (PFD)

The phase frequency detector has an unlimited pull–in range [23], which is an advantage over the EXOR, flip–flop and multiplier phase detector. The PFD is usually implemented together with a charge pump, as shown in Fig.2.9. The PFD has two outputs, UP and DN, which open or close the two current sources of the charge pump. The output current is then converted to a voltage across the impedance Z_{lf}.

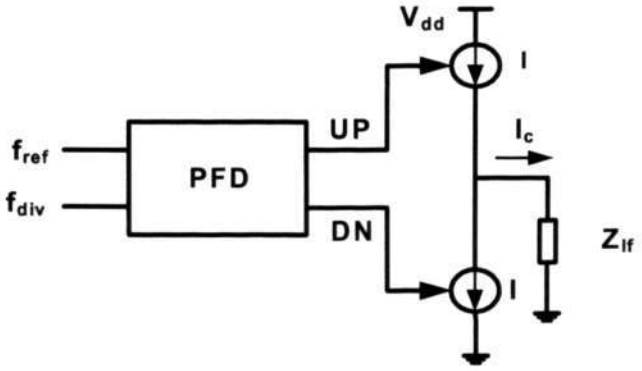


Fig. 2.9 Phase frequency detector.

The operation of the PFD is shown in Fig.2.10 (a). The PFD has two inputs, the reference signal f_{ref} and the feedback signal from the divider f_{div}. The reference pulse causes the output to change to a positive direction, unless the output is already positive, in which the pulse has no effect on the output. Similarly, the loop's divider output causes a negative transition unless the output is already negative. The transfer characteristics of the PFD are plotted in Fig.2.10 (b) and have a linear phase range of 4π.

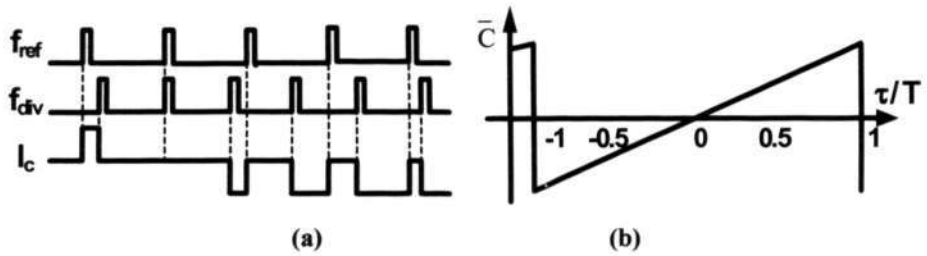


Fig. 2.10 (a) Operation of the phase frequency detector, (b) Transfer characteristics of the phase frequency detector.

The PFD in Fig.2.9 suffers from a "dead zone", which arises from the crossover distortion and changes in gain occurring near the zero phase error [24]. If both the reference pulse and the divider pulse appear at the same time, none of the outputs becomes active and the charge–pump output is in high–impedance state. Even if the

phase difference changes slightly, the phase detector will not respond immediately since it requires some finite time for the UP and DN pulses to propagate through the circuit. Therefore, the charge pump keeps its high impedance state although there is a slight phase difference. Hence, the phase detector characteristic actually has a flat response, which is known as the dead zone, near the zero phase difference.

Giving a fixed minimum width to both the charge pump pulses can solve the problem of the dead zone. Fig.2.11 shows a PFD circuit that is free of the dead zone [25]. The output terminals UP and DN are designed to be active low. The delay block after the 4–input NAND circuit determines the minimum width of the up–pulses and down–pulses. If the divider output lags the reference signal, the up signal will become active for a certain time T_D. Where T_D is equal to the time difference between these two signals, and the delay through the circuit, including the delay caused by the extra delay stage. Similarly, the down–pulse will also become active for a short period due to the extra delay. The net difference between the up–time and down–time determines the total change in the charge pump output voltage, and is proportional to the phase difference between two PFD inputs. For the case when the divider signal leads the reference signal, even without a phase difference between these two inputs, both the up and down signals are active for a short period determined by the delay stage. However, the net charge injected into the impedance Z_{lf} is zero, since these two pulses are of equal magnitude and opposite polarity. In this case, the charge pump is not in a high–impedance state and the loop is always closed.

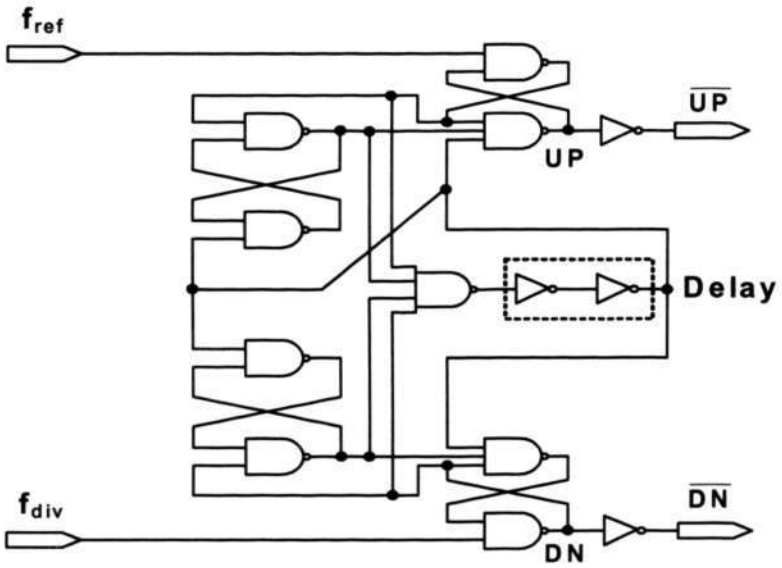


Fig. 2.11 Phase frequency detector without dead zone.

2.3.2 Loop Filters

The design of the loop filter determines most of the specifications of the PLL. Extra poles and zeros in the loop transfer function influence the noise and dynamic performance of the loop. From equation (2.12), it is clear that good tracking and narrow loop bandwidth are incompatible for the first order PLL. Therefore, it is not often used. In what follows the first order loop is extended to higher orders and types in order to improve the PLL performance. There are two types of loop filters, active and passive. An active filter uses op–amps to generate a tuning voltage higher than that generated by a passive filter. However, the op–amp itself provides the DC amplification necessary to develop a high control voltage required by the VCO in wide band applications. A passive filter has the advantages of reduced noise and lower circuit complexity. It is formed by only R (resistor), C (capacitor) elements, and often used as the charge pump loads to generate the control voltage proportional to the phase error. The charge pump passive

loop filter is used widely for wireless applications, and is referred to as the current source loop filter [26]. This is in contrast to the voltage source loop filter for an active loop filter.

2.3.2.1 Third Order, Type–II PLL

Fig.2.12 shows a 3rd order, type–II charge–pump PLL. The phase detector with the charge pump generates the charge current into the loop filter to produce the VCO's control voltage. Compared to a 2nd order charge–pump PLL, the extra capacitor C_2 in the 3rd order PLL is added to smooth out the discrete voltage steps at the control port of the VCO due to the instantaneous changes in the charge pump current output. At each cycle of the PFD, a pump current I_{cp} is driven into the filter impedance with an instantaneous voltage jump of $I_{cp}R_1$. The corresponding frequency jump is:

$$|\Delta\omega| = K_{vco} \times I_{cp} \times R_1 = 2\pi \times \omega_p \tag{2.16}$$

which is generally larger than the average frequency increment per cycle[22].

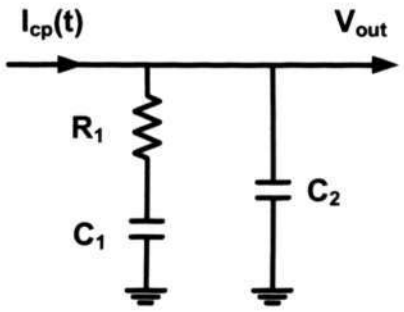


Fig. 2.12 A 2rd order, type–II loop filter.

The filter can be designed based on the open loop gain bandwidth and the phase margin required. Positioning the point of the minimum phase shift at the unity gain

frequency of the open loop response as shown in Fig.2.13 ensures the loop stability. The phase relationship between the pole and zero also allows the determination of the loop filter component values. The phase margin θ_p is defined as the difference between 180° and the phase of the open loop transfer function at the unity–gain frequency $f_c = \frac{\omega_c}{2\pi}$, also namely cross–over frequency. The phase margin is chosen between 30° and 70° for most applications [27]. The larger the phase margin, the more stable the loop. However, the transient response is slower, and resulting in a longer switching time. A loop with a low phase margin may still be stable but could exhibit oscillator problems associated with an un-damped loop, such as longer switching time and increased noise. A phase margin of 45° is a good compromise between the desired stability and the other generally undesired effects.

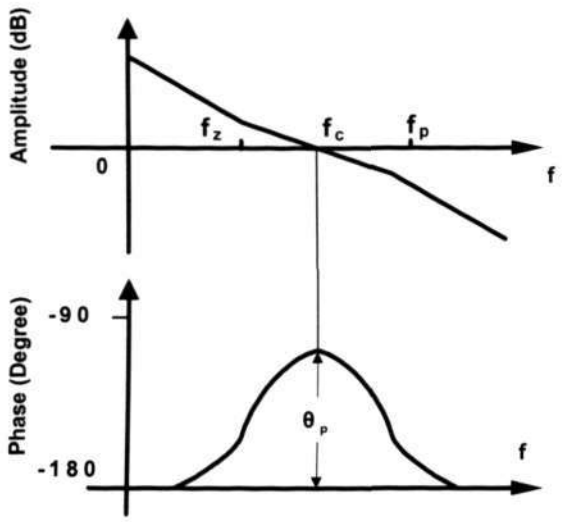


Fig. 2.13 Bode plot of the open loop response for a 3rd order, type II PLL.

The impedance of the loop filter in Fig. 2.12 can be expressed as:

$$Z(s) = \frac{s \cdot C_1 \cdot R_1 + 1}{s^2 \cdot C_1 \cdot C_2 \cdot R_1 + s \cdot C_2 + s \cdot C_1} \tag{2.17}$$

while $s = j\omega$. From equation (2.17), the gain and the phase of the loop filter can be derived. The time constants that determine the pole and zero frequencies of the filter transfer function are defined by the following equations:

$$\tau_z = R_1 \cdot C_1 \tag{2.18}$$

$$\tau_p = R_1 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2} \tag{2.19}$$

Thus, the 3rd order PLL open loop gain defined by equation (2.5) can be rewritten as [19]

$$G(s) = \frac{K_0 \cdot (1 + s \cdot \tau_z)}{s^2 \cdot C_2 \cdot N \cdot (1 + s \cdot \tau_p)} \cdot \frac{\tau_p}{\tau_z} = \frac{I_{cp} K_{VCO}}{2\pi N (C_1 + C_2)} \frac{(1 + s\tau_z)}{s \cdot s \cdot (1 + s \cdot \tau_p)} \tag{2.20}$$

As expected, there are two poles located at the origin, as such the PLL is commonly referred to as type–II third order charge pump PLL (CPLL) [21].

To analysis the stability of the loop, the phase margin θ_p and the loop gain G(s) should be considered. The phase margin is defined as:

$$\theta_p = 180^0 + \angle G(j\omega_c) \tag{2.21}$$

while f_c mentioned before is the cross–over frequency at which the loop gain is equal to 1, thus we got:

$$|G(j\omega_c)| = 1 \tag{2.22}$$

The phase margin of the third–order CPLL is given by:

$$G(j\omega_c) = 180^0 + \angle\left|\frac{I_{cp}K_{vco}(1+j\omega_c\tau_z)}{2\pi N\omega_c^2(C_1+C_2)(1+j\omega_c\tau_p)}\right| \qquad (2.23)$$

Sometimes, the 3rd order structure does not provide the sufficient rejection to the reference spur. The reference spur is caused by the current switching noise in the dividers and the charge pump at the reference frequency f_{ref}. In wireless communications, the phase detector operation frequency is generally a multiple of the RF channel spacing. These spurious sidebands can cause noise in adjacent channels. This is usually the case in the TDMA digital cellular standards, such as GSM. A narrow loop bandwith filter has advantage of a better attenuation of the reference spur, but the requirement of the sub–milliseconds switching between channels makes a relatively wide loop filter mandatory.

2.3.2.2 Fourth Order, Type–II PLL

To further increase the number of design parameters, a third pole can added in the loop filter of the third order, type–II PLL. The extra pole again increases the spurious suppression of the loop. The use of a passive loop filter eliminates the noise contributions from the op–amp in an active filter. This is critical due to the strict phase error and integrated phase noise requirements. For example, the integrated phase noise requirement for the SONET OC–192 specification is 1 ps root–mean–square value (rms). The recommended filter configuration is shown in Fig.2.14.

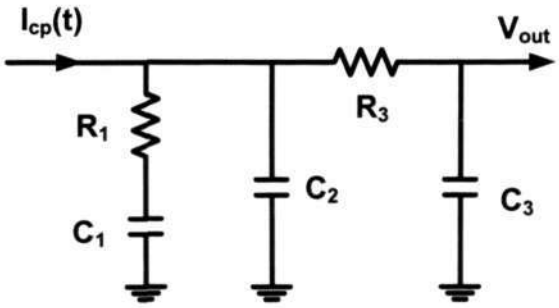


Fig. 2.14 A 3th order, type–II loop filter.

The additional pole frequency must be lower than the reference frequency to significantly attenuate the reference spur, but must be at least 5 times higher than the loop bandwidth to maintain the loop stability [28]. The additional filter time constant can be defined as:

$$\tau_3 = R_3 \cdot C_3 \tag{2.24}$$

The Bode plot of the open loop response for the 4th order charge pump PLL is shown in Fig.2.15.

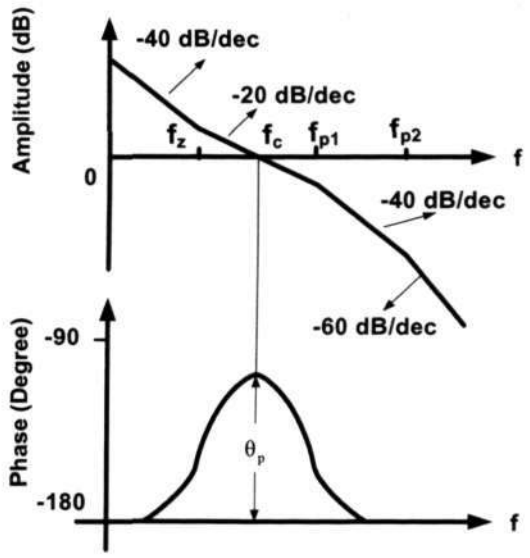


Fig. 2.15 Bode plot of the open loop response for a 4th order, type–II PLL.

2.3.3 Dividers

The most apparent feature that differentiates the PLL frequency synthesizer from other PLLs is the frequency divider. In this section, the three typical frequency dividers, namely, integer N divider, prescaler, dual modulus prescaler with swallow counter, and fractional N divider, are described.

2.3.3.1 Integer N Divider

A popular implementation of an integer N divider is through a pre-settable divider. The pre-settable divider is used to obtain a variable, controllable division ratio [29]. A typical element of the divider is the J–K flip–flop with the asynchronous set (S) and reset (R) capability.

A certain preset number can be loaded into the counter, which starts counting the input pulses till the end number is reached, and an overflow signal is generated. The counter is then reset to the original preset number and starts counting again. The division ratio is equal to $(2^n - P)$, where n is the number of bits of the counter and P is the preset number.

An alternative implementation is to start counting input clock pulses from zero until a certain preset number P is reached and a reset signal is generated. Then the counter is reset to zero and the counting process restarts again. The division ratio then equals P. The limitation of the pre-settable divider is its low operating frequency.

2.3.3.2 Prescaler

When the input frequency of the divider is too high to permit a proper operation of the programmable divider or counter, a prescaler can be used. A prescaler divides the input frequency by fixed ratios, and can therefore operate at higher frequencies because it does not suffer from the delays involved in counting and resetting [29]. Adding a few high–speed prescaler stages will lower the speed requirement for the subsequent counter stages.

The disadvantage of using the prescaler is that it requires a low reference frequency for a given frequency resolution (channel spacing/bandwidth). This is because if the prescaler division ratio is N, the smallest change in the synthesized frequency is $\Delta f = N \times f_{ref}$. So, the reference frequency must be a factor N lower than the channel spacing. This implies a lower loop bandwidth, which is often undesirable [19].

2.3.3.3 Dual Modulus Prescaler with Swallow Counter

In order to resolve the above–mentioned resolution problem, a dual modulus prescaler (DMP) can be used. This circuit extends a fixed–ratio prescaler with some extra logic circuits that enables it to divide by a selectable division by N or by (N + 1) [29]. Due to the extra functionality, the speed of the circuit is slowed down. Notably, there are a few proposals for specialized circuits, for example, NOR/flip–flop combination circuits [30], which have made much improvement in the performance of the DMP. Nevertheless, these types of DMPs still cannot match the speed of the prescaler.

A dual modulus prescaler with swallow counter was developed and used in a full divider that can handle all integer ratios. It is consisted of N+1/N prescaler, Program

counter P and Swallow counter S. Its operation will be presented in Chapter 6. To obtain the complete range of integer numbers, S must be a variable from 0 to (N – 1). For a proper reset of the P–counter, P must always be larger than the largest value of S, or $P \geq N$. So the smallest obtainable division ratio is $M_{min} = N^2$. This sets a limit on the maximum prescaler division ratio for a given minimum synthesized frequency and a given frequency resolution.

2.3.3.4 Fractional N Divider

The required low reference frequency is a general problem in many PLLs. Since a frequency divider of modulus N can only be programmed to integer values, the reference frequency used in the synthesizer must be as low as or lower than the required resolution, e.g. 200 kHz for GSM. The use of a prescaler decreases the reference frequency by a factor N. However, a DMP has a certain minimum division number, so it may not be able to use a higher reference frequency than a simple prescaler [31].

Two problems are created by a too low value of reference frequency, f_{ref}. Firstly, to assure a proper linear operation of the phase detector, the loop bandwidth must be approximately one tenth of f_{ref}. Normally a larger loop bandwidth would be desirable, because this allows a shorter switching time and a better suppression of the VCO noise. Secondly, the output noise contributed by the reference signal noise, the phase detector noise and the loop filter noise will become high due to the large value of N, because these noise sources are all multiplied by a factor N.

A fractional N divider allows PLL synthesizers to have a frequency resolution finer than the reference frequency. Therefore, the tradeoff in the PLL synthesizer with an integer N divider does not apply to fractional N divider. This technique originates from

an early digiphase synthesizer [32], and a later commercial version is referred to as a fractional N synthesizer as shown in Fig.2.16 [33] [34].

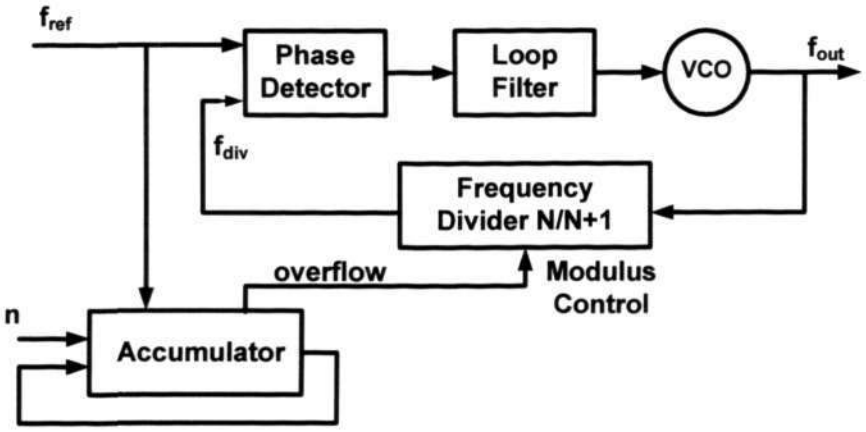


Fig. 2.16 PLL frequency synthesizer with fractional N division.

In the fractional N divider, a dual modulus divider, divide–by–(N / N + 1), is used. The fractional division is obtained by switching between the division value of N and N+1. For instance, in order to achieve a divide–by–(N + 1/2), the division by (N + 1) is done after every one division by N. Thus, the carry of the accumulator follows in the sequence of {010101…}, where the division by (N + 1) corresponds to a "1". Fig.2.17 shows the phase error generated in the process to achieve a divide–by (2 + 1/2), assuming the VCO frequency remains constant.

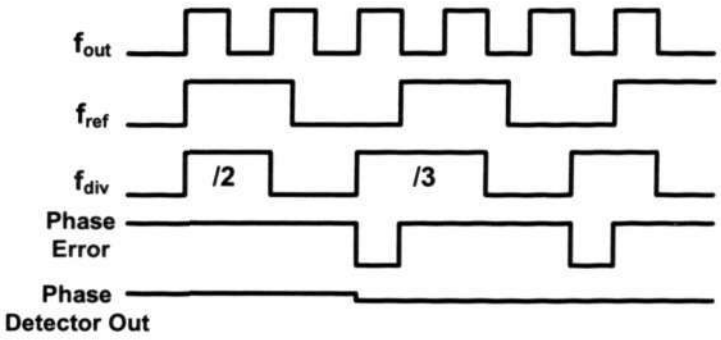


Fig. 2.17 Phase error generated in the process to achieve a divide–by– (2 + 1/2) operation.

Unfortunately, this technique generates unwanted low frequency spur due to the fixed pattern of the dual modulus divider. Since these low frequency spurs can reside inside the loop bandwidth, fractional N frequency synthesizers are not practical unless fixed in band spur is suppressed to a negligible level.

2.4 LC Oscillators

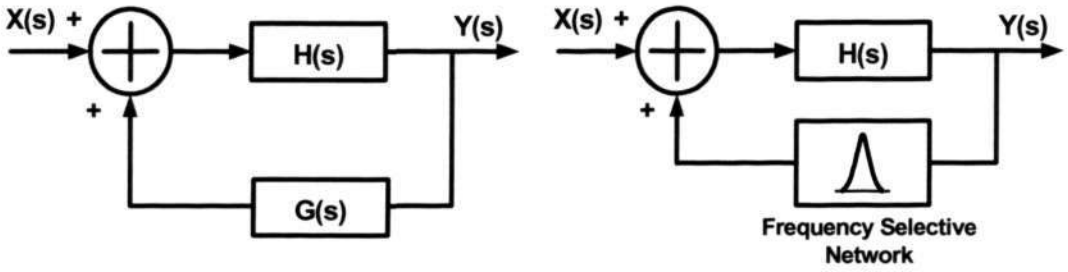
There are two types VCOs that are promising candidates for CMOS frequency synthesizer approaches. One is the resonator–based VCOs which include a resonated tank consisted of on–chip inductors and varactors, they are also called LC VCOs. The other type is resonator–less VCOs such as a ring oscillator and relaxation oscillators, they also offer high frequency operations and a large tuning range. However, the latter type suffers from a bad phase noise performance and is rarely used in RF systems [8]. The best way to achieve monolithic integration of the oscillator is the LC oscillator, and its output frequency is determined by the resonance of an inductor and a capacitor. Since both elements constitute a passive filter, the phase noise is expected to be low. Therefore, this type of oscillator is the subject of this thesis.

2.4.1 General Oscillator Theory

An oscillator generates a periodic output. As such, the circuit must entail a self–sustaining mechanism that allows its own noise to grow and eventually become a periodic signal.

Most RF oscillators can be viewed as feedback circuits. Consider a simple linear feedback system depicted in Fig.2.18 (a), in which the overall transfer function [35] is given as:

$$\frac{Y(s)}{X(s)} = \frac{H(s)}{1 - H(s)G(s)} \tag{2.25}$$



(a) (b)

Fig. 2.18 (a) Feedback oscillatory system, (b) Addition of frequency–selective network.

For steady oscillation, Barkhausen's criteria must be simultaneously met at ω_0 [35]:

(1) The loop gain, $|H(s)G(s)| \geq 1$.

(2) The total phase shift around the loop, $\angle H(s) + \angle G(s) = 0°$ or $360°$.

The above conditions imply that any feedback system can oscillate if its loop gain and phase shift are chosen properly. In most RF oscillators, however, a frequency selective network, e.g., an LC tank, is included in the loop so as to stabilize the frequency. This is illustrated conceptually in Fig.2.18 (b), although such a network can be part of H(s) as well. The frequency selective network is also called a "resonator". Here we should also mention that in some cases Barkausen's criteria are necessary but not sufficient [36]. As a simple example, if the phase shift around the loop is equal to 360° at zero frequency and the loop gain is sufficient, the circuit latches up rather than oscillates.

2.4.2 Basic Concepts of the LC VCO

A resonator–based VCO has a LC resonator tank (LC tank) as a frequency selective element consisting of inductors and capacitors. The energy loss in the tank has to be compensated by active devices. A parallel LC tank is modeled in Fig.2.19. The positive resistor R_p models the resistive loss in the tank, and the negative resistor $-R_a$ models the active device, which provides the energy into the tank. Once the energy loss is equal to the energy provided by the active device, a stable oscillation can be sustained [8]. The effective impedances of the LC tank are expressed as:

$$Z(j\omega) = \frac{1}{\frac{1}{j\omega L} + j\omega C + \frac{1}{R_p}} \tag{2.26}$$

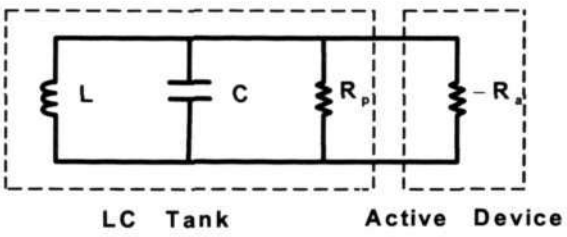


Fig. 2.19 Typical schematic of the LC VCO.

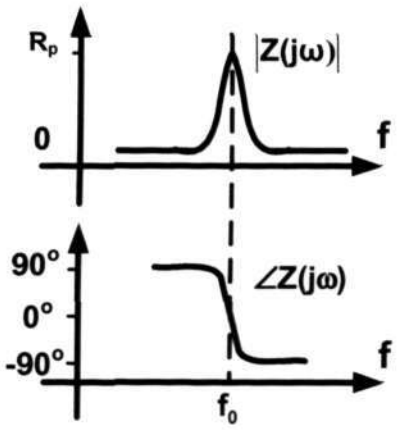


Fig. 2.20 Magnitude and phase of the tank.

The resonant characteristics of $Z(j\omega)$ are illustrated in Fig.2.20. It is observable that the effective impedance $Z(j\omega)$ of the LC tank is purely real at resonance, which is equal to the effective resistance R_p. Simultaneity, the phase of the effective impedance is equal to zero. The frequency f_0 at resonance is given as:

$$f_o = \frac{1}{2\pi\sqrt{L\ C}} \tag{2.27}$$

Therefore, the phase conditions of Barkausen's criteria are satisfied, and the magnitude condition can be achieved by setting $R_p / R_a \geq 1$. In general, R_p is two times of R_a in order to start–up oscillation and be stable for LC oscillators [36].

The important passive components implemented in LC tanks are inductors and varactors, they are affecting the performance of the fully integrated LC VCO directly. The high Q value of the inductors can improve the phase noise of the LC VCO. The large frequency tunable range of the varactors makes the transceiver to cover all frequency channels. In this section, we provide concepts, understanding and modeling of the passive components, such as inductors and varactors, used in the LC VCO latest years.

2.4.3 Inductors

The requirement for a good inductor is its inductance, low series resistance, low substrate losses, small area, and high self–resonance frequency. A smaller series resistance along with lower substrate losses improves the Q value and thus the phase noise of a VCO. A small area is desired to reduce the real estate cost, without counting the fact that substrate losses are proportional to the size of the inductor [37]. A high

self–resonance frequency permits the addition of extra varactors, which enhances the tuning range of the VCO.

2.4.3.1 Definition of Quality Factor (Q)

The efficiency of an inductor is determined by its quality factor Q [37], and the fundamental definition for Q is:

$$Q = 2\pi \frac{\text{Energy stored}}{\text{Energy loss in one oscillation cycle}} \tag{2.28}$$

It is proportional to the ratio of energy stored to energy dissipated per unit time cycle. The energy stored in a LC tank is actually the sum of the average magnetic and electric energies. However, for a silicon spiral inductor, only the energy stored in the magnetic field is off interest. Any energy stored in the form of the electric field by the parasitic capacitance is counterproductive [19]. Hence, Q is proportional to the net magnetic energy stored, which is equal to the difference between the peak magnetic and electric energies:

$$Q = 2\pi \frac{\text{Peak magnetic energy} - \text{Peak electric energy}}{\text{Energy loss per cycle}} \tag{2.29}$$

In a parallel RLC circuit, peak magnetic energy can be calculated as $\frac{V_p^2}{2\omega^2 L}$, while peak electric energy and energy loss per cycle are equal to $0.5CV_p^2$ and $\frac{V_p^2}{\omega R}$ respectively, thus equation (2.23) can be expressed as:

$$Q = \frac{\pi R_p}{\omega L}\left[1 - \left(\frac{\omega}{\omega_{0,self}}\right)^2\right] \tag{2.30}$$

With reference to a spiral inductor built on Silicon, C can be regarded as the parasitic capacitances of the substrate. R_p represents the resistance of the substrate underneath the inductor and $\omega_{0,self}$ represents self–resonate frequency respectively. The self–resonance is mainly from the resonance between the inductor's parasitic capacitance and the inductance. Equation (2.30) shows that when operating frequency equals to the self–resonant frequency, Q vanishes to zero and no net magnetic energy is available from the inductor when operating beyond self–resonant frequency [38].

2.4.3.2 Loss Mechanisms in Si–Based Spiral Inductors

In general, there are four main loss mechanisms, namely, metal resistive loss, skin effect, eddy current and substrate induced loss. These loss mechanisms have inevitably degraded the performance of inductors and increased the difficulty in the prediction of the quality factor for silicon–based spiral inductors [39].

(a) Metal Resistive Loss

The non–zero resistance of a metal contributes to the energy loss in the inductor. In order to achieve an inductance value of a few nH, a spiral inductor with many turns is usually needed. It often has a dimension larger than 100 μm. This results in a very long metal wire. The resistance of a wire is given by $R = \frac{L_m}{\sigma W_m t_m}$, where σ is the conductivity for the metal. L_m, W_m and t_m are the length, width and thickness of the wire, which degrades the quality factor of the inductor [40].

(b) Skin Effect

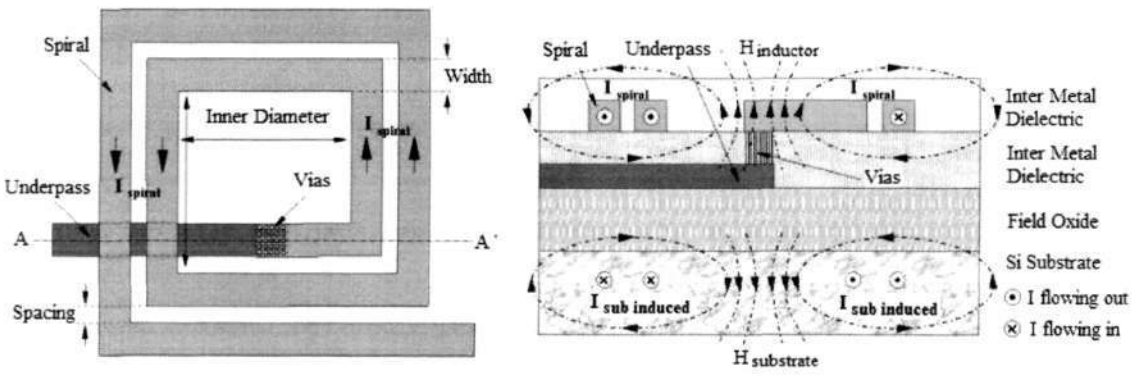
The current density in a wire is uniform at DC. However, as the frequency increases, the current density becomes non–uniform because of the induced electromotive force (EMF). Non–uniform current effectively decreases the cross–sectional area of the conductor, and hence increases in the series resistance. This phenomenon is known as the skin effect and is directly proportional to the frequency [41]. The most critical parameter pertaining to this effect is the skin depth that is defined as:

$$\delta = \sqrt{\frac{\rho}{\pi \mu f}} \tag{2.31}$$

where ρ, μ and f represent the resistivity, permeability, and frequency respectively.

From equation (2.31), note that there is less low resistive path for current to flow at high operating frequency and hence resistance of the metal conductor increases and Q drops due to the higher energy loss.

(c) Eddy Current Induced Loss



(a) **(b)**

Fig. 2.21 (a) Formation of image current, (b) Magnetic flux interaction with that of the inductor.

Magnetic loss occurs when inductors are built flatly on a highly conductive silicon substrate. According to Faraday's law, an image current or eddy current is induced in the substrate underneath the spiral. Since the silicon substrate has low resistivity, this image current can flow easily. In compliance with Lenz's law, the direction of flow for this induced current is opposite to that of the inductor. This generates an parasitic magnetic field in the substrate, which interacts with the magnetic field of the inductor and results in a degradation of the inductor's overall useful inductance. Fig.2.21 shows the top and cross–sectional views of an inductor fabricated on a silicon substrate. It also illustrates the formation of the image current in the substrate and its magnetic flux interaction with that of the inductor.

(D) Substrate Induced Loss

The conventional silicon–based spiral inductor is fabricated using metal layers and it sits on top of the inter–metal dielectric layers (which are made up of the silicon oxide) and the silicon substrate. The layers of the silicon oxide and the substrate contribute to the unwanted capacitive coupling, which degrades the self–resonant frequency of the inductor. Ideally, the substrate and the oxide layer should not be capacitive and should have infinite resistivity so as to minimize unwanted substrate coupling. Inductors built on such ideal substrate will have high quality factor and high self–resonant frequency. The presence of these parasitic components promotes undesirable energy dissipation and loss into the silicon substrate, which will also degrade the quality factor of the inductor.

Therefore, to understand the effects of these parasitics and their impact on the overall device performance, an accurate physical inductor model that takes into considerations

the substrate effects will definitely enable circuit designers to design their required inductors in a much shorter time period.

2.4.3.3 Physical Modelling of Spiral Inductors on Silicon

The accurate physical model of silicon–based inductors fundamentally requires identification of all the relevant parasitic components present in the inductor's structure, together with comprehensive understanding of their effects. The inductor is designed primarily for storing magnetic energy. Therefore, all ohmic and capacitive parasitics present in a silicon–based spiral inductor are counter–productive. The conventional physical model of a spiral inductor on silicon is shown in Fig.2.22 (a), in which the parameters are summarized in Table 2.1. In addition, the inductor's Q can be roughly approximated as $\omega_0 L_s / R_s$ if all parasitic capacitors and substrate resistance are neglected. Fig.2.22 (b) depicts the equivalent circuit of inductors, here, $R_{L,s}$ is the series resistor of the inductor, and L is the inductance.

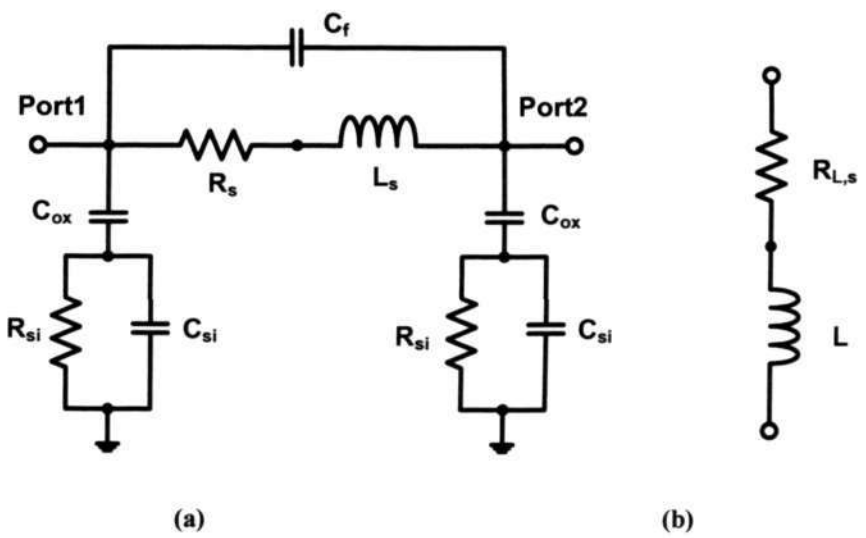


Fig. 2.22 (a) Lump physical model of spiral inductor on silicon, (b) Typical equivalent circuit of the inductor.

Table 2.1 Parameters of the inductor model

Symbols	Description
L_s	Inductance of the spiral
R_s	Resistance of the spiral and underpass
C_f	Series capacitance between the adjacent turns of the metal conductor
C_{ox}	Oxide capacitance between the spiral and the silicon substrate
C_{si}	Capacitance of the silicon substrate
R_{si}	Resistance of the silicon substrate

2.4.4 Varactors

2.4.4.1 Types and Operation Theory

Two type varactors are adopted popularly in the fully integrated VCO. One is the diode varactor, the other is the MOS varactor. The diode varactors become less and less attractive for two reasons. Firstly, p–n juctions suffer from a limited tuning range that is related to nonlinearity in the C–V characteristics. The capacitance varies slowly under the reversed bias and sharply under the forward bias, thereby introducing a significant nonlinearity in the VCO characteristic. Secondly, at low supply voltages, it becomes increasingly more difficult to select the oscillator common–level and signal swings so as to avoid forward biasing the diodes.

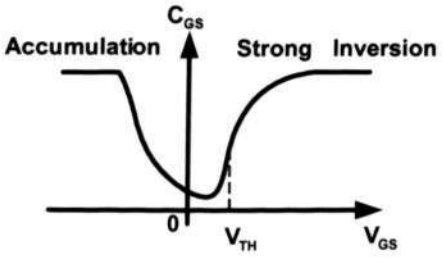


Fig. 2.23 C–V characteristic of a MOSFET.

An alternative varactor that does not exhibit the above mentioned shortcomings is derived from MOSFETs. With their non-monotonic C–V characteristics as shown in Fig.2.23, regular MOSFETs may serve as varactors if the VCO design guarantees the gate–source voltage to be remained in the monotonic region. However, the varactors suffer from a large source–drain resistance in vicinity of the minimum capacitance due to the low carrier concentration in channel. A simple modification resolves these difficulties. Namely, an "Accumulation–mode MOS varactor" or A–MOS varactor and shown in Fig.2.24 (a), this structure resembles an NMOS transistor placed inside an n–well. If V_G is below Vs, the electrons in the n–well are repelled from the silicon/oxide interface and a depletion region is formed shown in Fig.2.24 (b). Under this condition, the equivalent capacitance is given by the series combination of the oxide and depletion capacitances. As V_G exceeds V_S, the interface attracts electrons from the n+ source and drain terminals, creating a channel shown in Fig.2.24 (c). The overall capacitance therefore rises to that of the oxide, exhibiting the characteristics is shown in Fig.2.24 (d). Since the material under the gate oxide is n–type, the concept of strong inversion does not apply here.

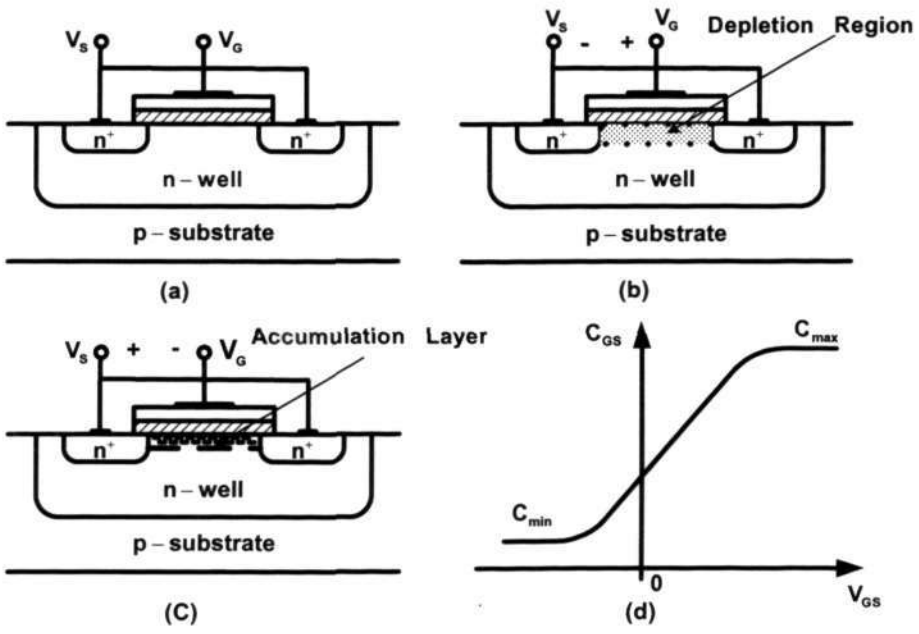


Fig. 2.24 (a) MOS varactor structure, (b) Varactor in depletion mode, (c) Varactor in accumulation mode, (d) C–V characteristic.

MOS varactors have been proved quite useful in VCO designs. While providing a dynamic range, C_{max}/C_{min}, of 2.5 to 3 with $-1.8\ V \le V_G - V_S \le +1.8\ V$ for 0.18μ CMOS technology [2], these devices comfortably tolerate both positive and negative voltages, allowing large VCO swings. In fact, the characteristic of Fig.2.24 (d) indicates that MOS varactors should operate with positive and negative biases so as to provide a maximum dynamic range.

MOS varactors nevertheless suffer from a trade off between the dynamic range and the Q value. The gate–source and gate–drain overlap capacitances of the device constitute of a significant fraction of the overall capacitance because of the minimum channel length, thereby limiting the tuning range. For example, in a typical 0.18 μm CMOS technology with $C_{ov} \approx 0.3\ fF/um^2$, $C_{ox} \approx 10\ fF/um^2$, and $L_{eff} \approx 0.16\ \mu m$, the

ratio of the total overlap capacitance to the oxide capacitance reaches $2 \times 0.3(10 \times 0.16) = 37.5\%$. To alleviate this issue, the channel length may be increased to about three times the minimum value, lowering the above ratio to 10 ~ 15% [2].

It is well known that any varactors can be modeled as a resistor series with a capacitor, and Fig.2.25 (a) shows the equivalent circuit lumped–model. The series resistance, $R_{var,s}$, can be expressed by equation (2.32), in which all parameters are listed in Table 2.2. The capacitance of the varactor, C_{var}, depends on the process. The quality factor, Q value, of the varactor can be expressed by equation (2.33).

$$R_{var,s} = \frac{1}{2}\frac{1}{2}\frac{1}{N_{var}}\left(R_{nwellsheet}\frac{L_{var}}{W_{var}} + R_{polysheet}\frac{W_{var}}{L_{var}}\right) \tag{2.32}$$

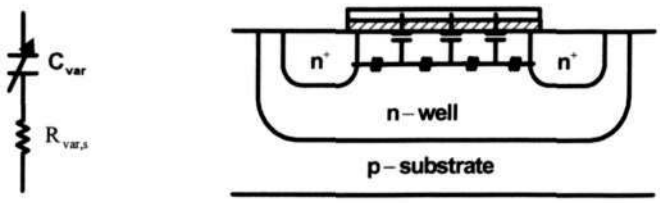
$$Q = \frac{1}{2\pi f C_{var} R_{var,s}} \tag{2.33}$$

Table 2.2 Parameters in the equation (2.32) and (2.33)

Symbol	Description
$R_{var,s}$	Series resistance of the varactors
$R_{nwellsheet}$	Sheet resistance of the n–well
$R_{polysheet}$	Sheet resistance of the poly
L_{var}	Length of the varactors
W_{var}	Width of the varactors
C_{var}	Capacitance of the varactor
N_{var}	Finger number of the varactors

This remedy, however, increases the resistance between the source and the drain terminals as given in Fig.2.25 (b), thus degrading the Q value. Despite those trades–off,

MOS varctors exhibit Q values of several tens in the gigahertz range, it is proved efficient means of the frequency control, especially at low supplies [2].



(a) (b)

Fig. 2.25 (a) Lumped circuit model, (b) Effect of channel resistance in MOS varactor.

2.4.4.2 Modeling of A–MOS Varactors

The layout of an Accumulation–Mode–Varactor (A–Varactor) is shown in Fig.2.26. The structure is similar to that of an n–channel MOSFET with the exception of being fabricated in an n–well instead of the normal p–substrate. This choice was made to eliminate the parasitic p–n–junction capacitances at the source and drain that would otherwise limit the tuning range.

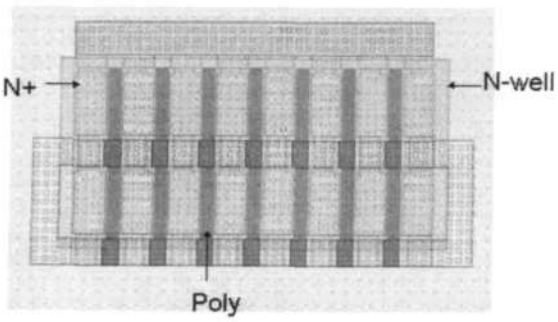


Fig. 2.26 Layout of the MOS varactor.

The source/drain (S/D) and well contacts form one port, and gate forms another port. When the voltage between the gate and S/D is changed from far above the flat–band

voltage to far below the flat–band voltage, the silicon surface is changed from accumulation to the strong depletion, and the overall series capacitance will change from a maximum to a minimum. In both the accumulation and the depletion regions, the overall series capacitance and the overall series resistance are both voltage dependent. Fig.2.27 gives the convention lumped physics model of MOS varactors [42] [43] [44], in which all parameters are summarized in Table.2.3.

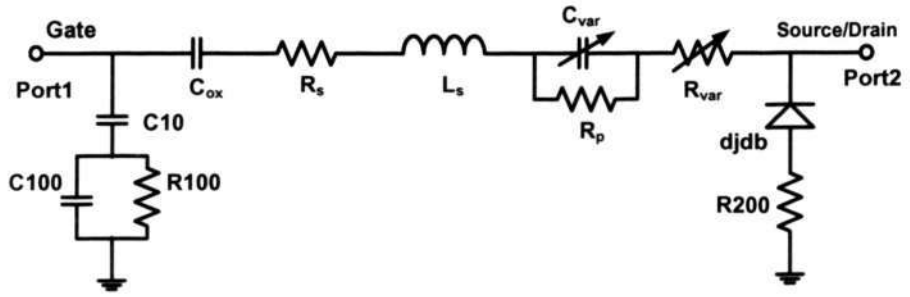


Fig. 2.27 Typical model of the MOS varacator.

Table 2.3 Parameters of A–MOS varactors

Symbols	Description
C_{ox}	Oxide capacitance under the gate
R_s	Parasitic resistance due to the interconnect metal of the gate terminal
L_s	Parasitic inductors due to the interconnect metal of the gate terminal
C_{10}	Coupling capacitance between gate and substrate.
C_{100}	Capacitance of the substrate
R_{100}	Resistance of the substrate
C_{var}	Variation capacitance depend on the voltage between gate and S/D
R_{var}	Variation resistance depend on the voltage between gate and S/D
R_p	Resistance under the channel
d_{jdb}	Drain–body diode
R_{200}	Resistor of substrate under the drain

2.4.5 Alternatives of the LC VCO

2.4.5.1 Colpitts and Hartley LC VCOs

Colpitts and Hartely are two types of LC oscillators, with different methods of the impedance transformation. A colpitts LC VCO utilizes a capacitance divider to supply the loop gain while forming the positive feedback depicted as Fig.2.28 (a). Whereas, an inductance divider is employed in Harltey LC VCO as given in Fig.2.28 (b). Although theoretically both are feasible, in reality the Colpitts structure is more attractive in RFIC fields because it requires fewer inductors. However, the Colpitts structure has its unavoidable drawbacks, in which the positive feedback is formed by connecting the amplifier output to its positive input, the source of the transistor. Without an impedance transformer, the low impedance of the transistor seen from its source will significantly affect the performance of the LC tank by decreasing its Q value. By employing the capacitance divider, the source impedance of the transistor is up–converted by a factor $(1+\frac{C_2}{C_1})^2$. It is obvious to notice that the ratio of C_2 and C_1 must be large enough to ensure the high impedance.

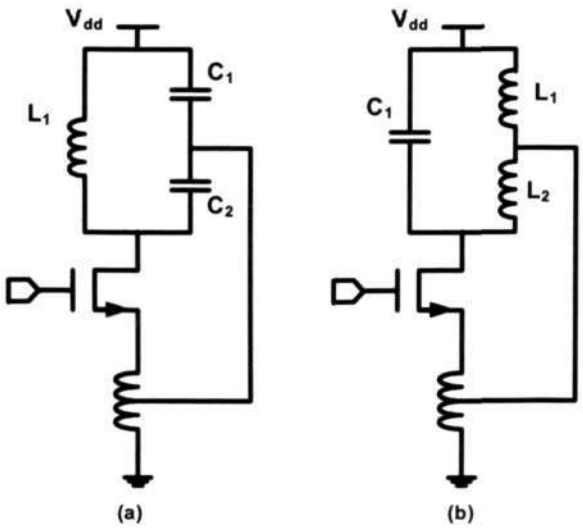


Fig. 2.28 (a) Colpitts LC VCO, (b) Hartley LC VCO.

2.4.5.2 Differential LC VCOs

The local oscillator is usually required to be differential output in RF systems. A differential implementation of the Colpitts LC VCO, also called as the cross coupled structure, is shown in Fig.2.29. It includes the NMOS type, the PMOS type as well as the complementary cross–coupled LC VCO. The inductors and varactors forming the LC tank have to be symmetrical from both sides in order to ensure a true differential circuit. The negative resistors, MOSFETs, supply energy to the loss energy from the positive resistor, LC tank consisted of an inductor (Ind) and a varactor (Var). The system oscillates when the energy from the negative resistors is equal or larger than that from the positive resistors. While, a tail current source, I_{tail}, is implemented in these VCOs' structures, because it has the following effects on the behavior of the VCO:

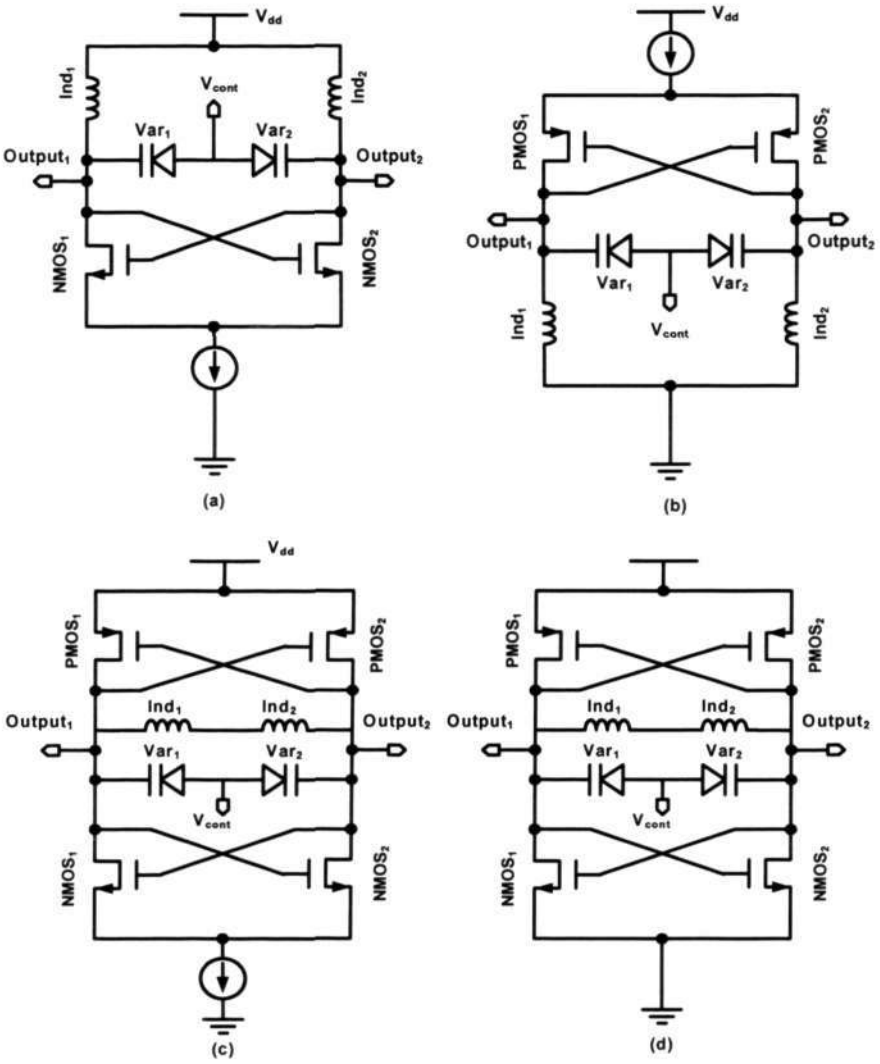


Fig. 2.29 (a) NMOS type VCO, (b) PMOS type VCO, (c) Complementary VCO with tail current source, (d) Complementary VCO without tail current source.

(1). The tail current source determines and keeps the oscillation amplitude not beyond V_{dd}. At the resonance frequency, the admittance of L and C is cancelled, only R_p is left in the tank as pointed in Fig.2.19. The amplitude of the voltage swing across the tank is given in first approximation by: $V_{max} = (2I_{tail}R_p)$ [45]. It refers to this regime of the operation as current limited. In this case, the maximum tank amplitude does not depend on the supply voltage.

(2). The reduction in voltage swing of the tank is more than that compensated by the reduction in the current consumption. Compared with the basic VCO, this allows us to save current, especially in the case of an over–designed g_m (larger transistors are necessary to sustain oscillations). In that case, the basic VCO consumes a lot of "short–circuit current" that is useless to the functioning of the oscillator.

An LC VCO uses a cross–coupled PMOS in addition to the NMOS as shown in Fig.2.29 (c) and (d). The LC tank is not connected to the power supply directly but connected to the output nodes, which are made up of two inductors and two varactors to ensure a perfect symmetry. The complementary LC VCO is used as the design topology in latest years for several reasons:

(1). It increase g_m two times for the same amount of current, hence the oscillation amplitude of this structure is two times of the NMOS type due to the PMOS pair, which results in the better phase noise performance and the faster switching of a cross–coupled differential pair [8].

(2). The cutoff frequency (f_T) of NMOS and PMOS transistors can be improved because the gate capacitor (C_{gs}+C_{gd}) of NMOS and PMOS is reduced to a half by the two series NMOSs and PMOSs respectively [46].

(3). It performs better the rise and fall time symmetry, which results in less upconversion of 1/f noise with the other low frequency noise sources [8].

However, the tail current source reduces the headroom available for oscillations by around 400 mV, which is not negligible as working with low supply voltages [8]. Simultaneity, it raises the source voltage of the cross–coupled pair, thereby reducing their

g_m because of the body effect [46]. That means a smaller inductance to keep the same frequency of the oscillation at the output node (which is now more loaded to keep the same g_m), the Q value of the tank will be reduced. Accordingly, the complementary LC VCO without the tail current source is adopted to realize LC VCO. Whereas, a risk, the oscillation amplitude cannot be controlled under the supply voltage, makes the oscillator unstable and limits its application in RFIC systems.

The tradeoff between the advantages and disadvantages is not obvious and requires different structures to be optimized individually, laid out and compared. In addition to consider the typically methodology for the phase noise optimization of LC VCOs, which includes the NMOS and PMOS, the complementary structure is the best choice for the design and the analysis of the LC VCO presented in the thesis.

2.4.6 Review of Existing VCO Phase Noise Models

In practical designs, the oscillator has to start the oscillation without any help of the external stimuli. It has to amplify its noise existing in the oscillator and keep increasing its amplitude until it reaches a satisfactory level. Therefore, in order to ensure the oscillation of the circuit and to maintain its stability, the Barkhausen's criteria must be satisfied. Furthermore, the oscillation amplitude is required large enough to turn on and off the active devices in the oscillator periodically. As a result, all the oscillators, regardless of their types, are nonlinear time–variant systems, and the linear time invariant (LTI) analysis is not valid for the phase noise studies [47]. Additionally, the device noise contributes to the phase noise, are modulated due to tune on and off the devices periodically. It is no longer stationary. Its self–correlation function is now a periodic

function of time. Hence it becomes cyclostationary instead. Therefore, the phase noise study of oscillators still challenges the designers and researchers of VCOs.

2.4.6.1 Leeson's Model [11]

One of the most well–known models of the phase noise in oscillators is Leeson's model, which was proposed by D. B. Leeson in 1966. The model is heuristically arrived without any formal proof. It relies on noticing the trend of the phase noise as the oscillator parameters change. It can be summed in the following equations as:

$$L(\Delta\omega) = S_{\Delta\theta}(\Delta\omega)\left[1 + (\frac{\omega_0}{2Q\Delta\omega})^2\right] \tag{2.34}$$

$$S_{\Delta\theta}(\Delta\omega) = \frac{\alpha}{\Delta\omega} + \frac{2FkT}{P_s} \tag{2.35}$$

where $S_{\Delta\theta}(\Delta\omega)$ is the spectrum of the input phase noise uncertainly given by equation (2.34), and it has two components. One is the additive white noise at frequencies around the oscillator frequency as well as the noise at other frequencies mixed into the pass band of interest by nonlinearities. Another is the flicker noise, which has a power spectral density inversely proportional to the frequency (a 1/f spectrum) due to the parameter variation at low frequencies around DC, this can be observed from equation (2.35). In equation (2.34) and equation (2.35), ω_0 is the center frequency of the oscillation, Q is the loaded quality factor, $\Delta\omega$ is the offset frequency of interest, α is a constant determined by the flicker noise level, F is an empirical excessive noise factor, k is the Boltzmann's constant, T is the absolute temperature, and P_s is the signal power.

Leeson's phase noise model predicts the phase noise spectrum, which includes $1/(\Delta\omega)^3$, $1/(\Delta\omega)^2$, $1/(\Delta\omega)$ and the noise floor regions as given in Fig.2.30, is also verified by more stringent phase noise analysis developed later as well as numerous measurement results. It is written in a simple mathematical form. This makes it easy to be used and understood. It includes an empirical factor F in its expression, but this factor cannot be explained by this model. Therefore it cannot predict the phase noise from the circuit noise analysis. However, once the phase noise for one oscillator is characterized, other oscillators of the same circuit topology can be calculated by applying the same factor F. Leeson's model assumes no knowledge of the circuit topology for the phase noise analysis. The topology dependence is taken into account by including the factor F. So it is that Leeson's model does not provide a direction for the circuit improvement. This disadvantage has been overcome by the later phase noise theories. Leeson's phase noise model is based on LC tank resonators, and a monolithic CMOS designs is preferred by modern communication systems and has attracted tremendous research work in recent years.

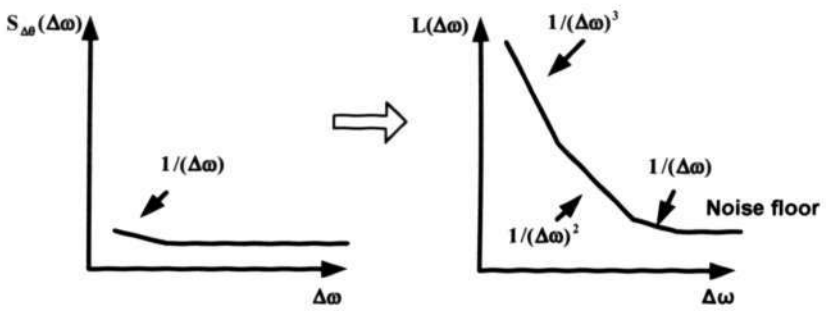


Fig. 2.30 Power spectral density of the input noise and the phase noise .

2.4.6.2 Razavi's Model [12]

B. Razavi proposed a phase noise model in 1996 for inductorless VCOs. In particular, his theory is well suited for CMOS ring oscillators without inductors. The load capacitors are charged and discharged periodically. So there is no energy storage within a clock cycle. Therefore, Leeson's phase noise model is invalid for the ring oscillator. However, Razavi proposed a new definition for Q factor, which makes Leeson's model applicable to inductorless oscillators, i.e., ring oscillators. If an oscillator is modeled as in Fig.2.31, and let $H(j\omega) = A(\omega)e^{j\Phi(\omega)}$, an open–loop Q factor is defined as follows:

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\Phi}{d\omega}\right)^2} \tag{2.36}$$

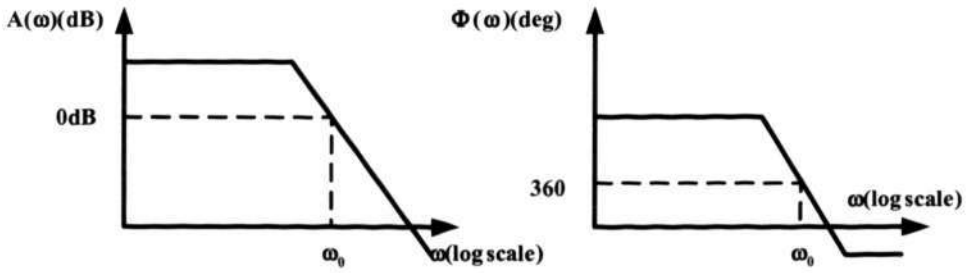


Fig. 2.31 Barkhausen's criteria.

If there exist circuit noise that can modify the transfer the function instantaneously, the open–loop transfer function will be deviated from the Backhausen's criteria. The definition of Q factor in equation (2.36) is a measure of how sensitive the open–loop transfer function is with respect to the circuit parameter variation. For example, an instantaneous increase in a transistor drain current due to noise means a large transconductance g_m at that instance. Hence the open–loop transfer function $H(j\omega)$ is charged in both its magnitude and phase. A large Q factor means more deviation from the

Backhausen's criteria. Therefore, for the same amount of circuit noise, there is a stronger feedback that brings the frequency back to its nominal frequency ω_0 so that both conditions in the Backhausen's criteria are satisfied. It is interesting to note that this definition of Q factor is also consistent with the existing definitions of Q factor for LC resonators.

Once the Q factor has been defined for a ring oscillator, it is implied that Leeson's phase noise model in equation (2.34) can be applied to the ring oscillator. However, in the case of an N–stage ring oscillator, there are N noise sources in total. So the close–in SSB (Single Side Bandwidth) phase noise for an N–stage ring oscillator is given by:

$$L(\Delta\omega) = \frac{2NFkT}{2Q\Delta\omega}\left[\frac{\omega_0}{2Q\Delta\omega}\right]^2 \tag{2.37}$$

Razavi's model considers nonlinearity by briefly discussing the high–frequency multiplicative noise and low–frequency multiplicative noise. However, these effects are only considered as a minor modification to the linear model. In fact, this is only true when quasi–balanced delay stages are used. In the ring oscillators where digital inverters are used, the signals are switched rail–to–rail. Fig.2.32 shows a 3–stage ring oscillator with digital inverter delay stages. The stage voltage is also shown in Fig 2.32. One common misconception about ring oscillators is that it is closed to its balanced state during the transition, which is the most critical moment for the phase noise, and hence a linear model is almost a good approximation to analyze its phase noise. However, it is seen from Fig.2.32 that the input and the output nodes of any of the delay stages never

reach the balanced state together. Therefore, the delay stages rarely act as a linear amplifier even during the transition.

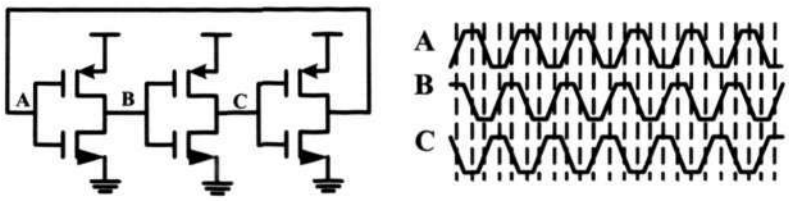


Fig. 2.32 Waveforms in a 3–stage ring oscillator.

2.4.6.3 Hajimiri's Model [47]

A more precise analysis was proposed by A. Hajimiri and T. Lee in 1998. It introduces an Impulse Sensitivity Function (ISF or Γ) to consider the effect of nonlinearity, LTV and cyclostationary noise.

Hajimiri induces a current impulse injected into a circuit node, which changes the voltage waveform instantaneously in both the amplitude and phase. Almost all the oscillators have an automatic amplitude control mechanism naturally built inside. Thus the amplitude will be settled back to its original state after a certain time delay. However, a permanent phase shift will remain after it settles into its steady state. The phase noise stays forever once it is introduced into the circuit. Hence the phase noise is the accumulation or integral of the circuit noise over the time. This can be described as 1/s in the frequency domain.

The magnitude of the phase shift is proportional to the ratio $\Delta q / q_{max}$, while Δq is the injected charge due to the noise, $q_{max,}$ is the maximum charge put on the output node capacitance due to the signal swing.

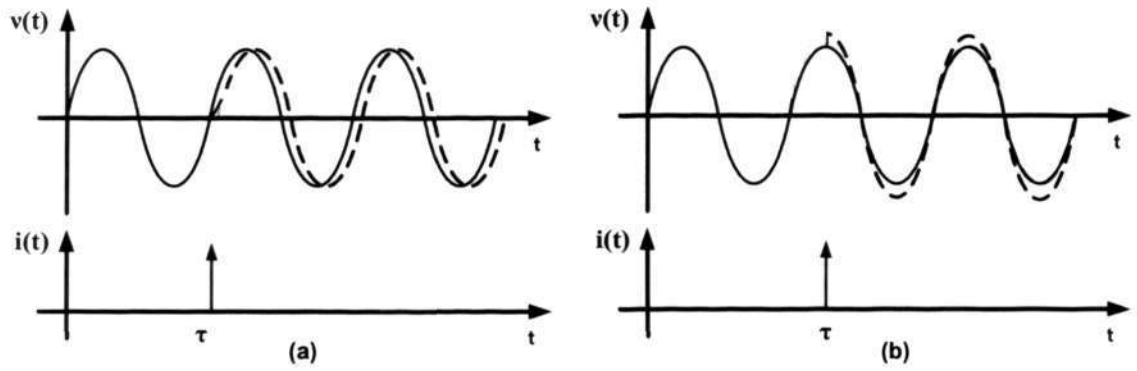


Fig. 2.33 Perturbation of voltage waveform due to a current impulse at (a) Zero crossing, (b) Peak.

On the other hand, the phase noise depends on the time when the current impulse is injected. This is illustrated in Fig.2.33. The circuit is sensitive to the noise during the transitions. An impulse at the zero crossing only causes the phase noise, but it does not cause the amplitude noise as shown in Fig.2.33 (a). An impulse at the peak only causes amplitude noise without any phase derivation observed in Fig.2.33 (b). Hence the impulse response of the phase is a step function whose amplitude depends on the time when the impulse is injected. Moreover, it is a periodic function with the same period as the signal waveform.

The ISF function definition in Hajimiri's Model will be discussed in Chapter 3. If the circuit has white noise with PSD of $\overline{i_n^2}/\Delta f$, its SSB phase noise is given as:

$$L(\Delta\omega) = \frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{2(\Delta\omega)^2} \quad (1/f^2 \text{ region}) \tag{2.38}$$

The SSB phase noise due to the flicker noise is given by:

$$L(\Delta\omega) = \frac{c_0^2}{q_{max}^2} \cdot \frac{\overline{i_n^2}/\Delta f}{8(\Delta\omega)^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \quad (1/f^3 \text{ region}) \tag{2.39}$$

where, $\Delta\omega$ is offset frequency from the carrier, q_{max} is the maximum charge signal swing of the tank, Γ_{rms} is the impulse sensitivity function (ISF), c_0 is the real–valued coefficient and $\omega_{1/f}$ is the corner of the device $1/f$ noise. Γ_{rms} is the root means square (RMS) value of the ISF for each noise source and is $1/\sqrt{2}$ for an ideal sinusoidal waveform. From equation (2.38) and equation (2.39), we can view that Hajimiri's model also indicates $1/(\Delta\omega)^2$ region due to white noise and the $1/(\Delta\omega)^3$ noise region due to the flicker noise, which coincides with the conclusions given in Leeson's model.

According to equation (2.39), we can view that the $1/(\Delta\omega)^3$ corner of the phase noise is the same as the 1/f corner for the flicker noise, because the spectrum close to DC is up–converted to the vicinity of the carrier. However, the $1/(\Delta\omega)^3$ region of the phase noise can be reduced by minimizing c_0. For an ideal case where the waveform is symmetrical, $1/(\Delta\omega)^3$ is completely removed, since $c_0 = 0$.

Hajimiri also considers the cyclostationary noise which can modulate $\Gamma(\omega_0\tau)$ by a factor $\alpha(\omega_0\tau)$, where $\alpha(\omega_0\tau)$ is the modulation factor due to the on and off operation of the devices and it will be discussed in Chapter 3.

In conclusion, Hajimiri's model is a theory that provides a comprehensive phase noise analysis. Meanwhile it has some practical limitations such as the complicated simulation process. However, it is highly simulation–based, and it does not trace the phase noise to its original sources. Hence, it does not provide a direction of how to minimize the phase noise for LC VCOs by optimizing the circuit topological.

2.5 Conclusion

In this chapter, we have given an introductory study of the PLL based frequency synthesizers, in which the basic knowledge of the PLL based frequency synthesizer is introduced, the performance impacts caused by the phase noise and spurious tone is studied, and the dynamic parameters of the system loop are introduced. The different loop building blocks in the frequency synthesizer, such as the phase frequency detector, loop filter, frequency divider, and oscillator are discussed. Some possible implementation alternatives for each component are given, together with the expected advantages and disadvantages.

The voltage controlled LC tank oscillators are reviewed. The operation theory is introduced. The LC tank consisted by the plannar spiral inductors and the varactors are discussed. The alternative structure of the LC VCO are reviewed and compared. The complementary cross coupled LC VCO is uesed in this thesis. The existing phase noise models are summarized. The advantages and disadvantages of the existing models are investigated. The directly optimization methodology of the phase noise during the design of LC VCO is necessary for the designer of VCO.

CHAPTER 3

A Novel Methodology for the Design of LC VCO with Low Phase noise

The voltage controlled oscillator (VCO) is one of the most important blocks in RF communication systems. Due to the ever increasing demand for the bandwidth, very stringent requirements are placed on the spectral purity of oscillators. Efforts to improve the phase noise performance of integrated LC VCOs have resulted in many papers [45] [48] [49]. The reported methods are summarized as: to achieve low phase noise, the oscillation amplitudes must be maximized. This means either increasing the biasing current or increasing the tank inductance (assuming a given tank quality factor). The former increases the power consumption, while the latter reduces the frequency tuning range due to a lower total tank capacitance [47] [48] [49]. In spite of these endeavors, design and optimization of integrated LC VCOs still pose many challenges to circuit designers as simultaneous optimization of multiple variables is required.

Although many phase noise models have been developed for different types of oscillators, each of these models makes restrictive assumptions applicable only to a limited class of oscillators. Most of these models are based on a linear time invariant (LTI) system assumption and suffer from not considering the complete mechanism by which electrical noise sources [11] [12], such as, device noises become phase noise. Therefore, those models are incapable of making accurate predictions about phase noise in oscillators because any oscillator is periodically time varying system. Even the phase

noise model reported in [47] takes into account linearity time invariance (LVT), it still can not evaluate accurately the phase noise of the LC VCO directly due to the incompletely device noise mechanism and the complicated simulation.

To achieve the objectives, a novel methodology to design a LC VCO with lower phase noise is proposed in this Chapter and verified in the next Chapter. A fundamental relationship between the channel lengths of MOSFET in LC VCOs and the phase noise is derived. An optimum channel length is achieved for the LC VCO with the lowest phase noise performance. An accurate phase noise model based on the linear time variant phase noise analysis presented here is capable of proper assessment of the effects on the phase noise of both stationary and cyclostationary noise sources. This model explains the exact mechanism by which the gate induced noise, the drain noise, the tail transistor noise, and random noise, are converted into phase noise and amplitude noise.

3.1 Topology

3.1.1 Operation Theory

The circuit diagram is shown in Fig.3.1 (a). A fully integrated complementary cross–coupled configuration is chosen as a vehicle of the novel methodology because of the advantages mentioned in section 3.2.2.

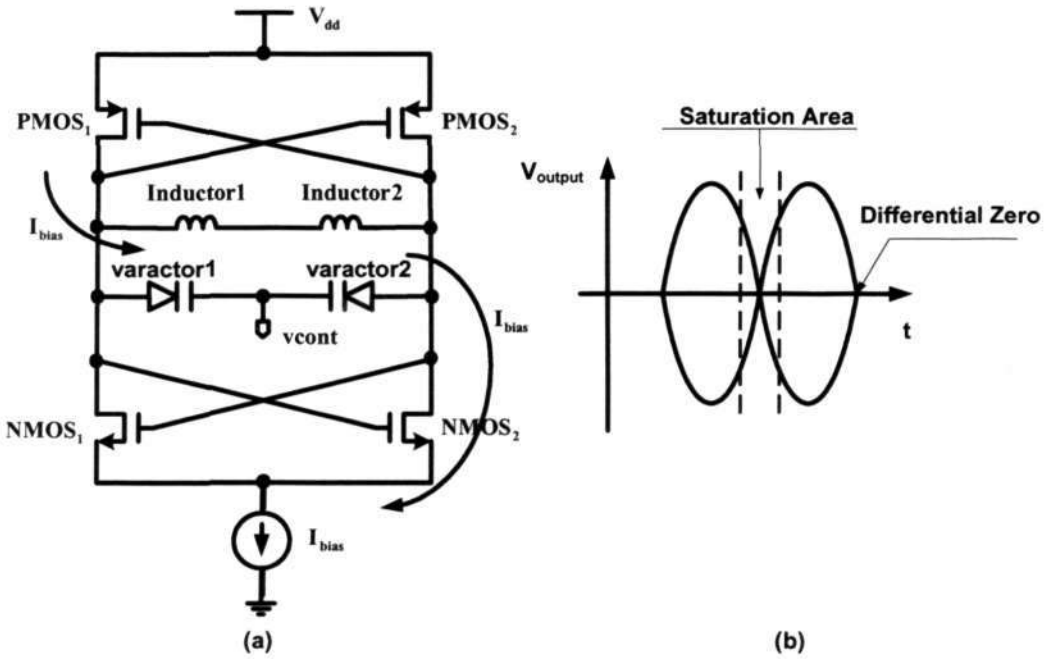


Fig. 3.1 (a) Schematic of the cross–coupled complementary LC VCO with the parasitic elements, (b) Differential zero.

It is well known that the active devices ($NMOS_1$, $NMOS_2$, $PMOS_1$, and $PMOS_2$) serve as the negative resistor to compensate for the energy loss from the tank due to the tank effective resistance. The cross–coupled VCO operates as switches [49]: Firstly, it is noted that the oscillator forces V_{GD} of the NMOS transistors to be equal in magnitudes but with opposite signs to generate a differential voltage across the resonator. At the differential zero voltage, four switching transistors ($NMOS_1$, $NMOS_2$, $PMOS_1$ and $PMOS_2$) are all in saturation region and form a small–signal negative conductance that breed the startup of the oscillation. As the differential oscillation voltage crosses $V_{th,n}$ (the threshold voltage of NMOS), V_{GD} (the voltage difference between Gate–to–Source voltage and Drain–to–Source voltage) of $NMOS_1$ exceeds $+V_{th,n}$, forcing it into the triode region, V_{GD} of $NMOS_2$ falls below $+V_{th,n}$, driving the device into a deeper saturation region, and then $NMOS_2$ turns off.

Simultaneously, as the falling differential oscillation voltage crosses $-V_{th,p}$ (the threshold voltage of PMOS, a negative value in our design) , V_{DG} (the voltage difference between Source–to–Gate voltage and Source–to–Drain voltage of $PMOS_2$) exceeds $-V_{th,p}$, forcing it into the triode region, at the same time, V_{DG} of $PMOS_1$ forces itself into a deeper saturation, and then $PMOS_1$ turns off. Thus, the complementary LC VCO operates when both NMOS and PMOS pairs are all in the saturation region beforehand, then $NMOS_1$ and $PMOS_2$ are at the off states, while $NMOS_2$ and $PMOS_1$ are at the on states. Such switching process is periodical throughout the operation of the VCO depicted in Fig.3.1 (b). The current $I_{bias,}$ as indicated in Fig.3.1 (a), drives the LC VCO into the stable operation.

3.1.2 Equivalent Circuit of the Cross–Coupled LC VCO

The equivalent circuit of the complementary cross–coupled LC VCO is given in Fig.3.2 (a), which is formed by the parasitic components, the LC tank as well as the negative resistors. The broken line in the middle represents either the common mode reference or ground. The symmetric spiral inductors, two identical varactors and two symmetric capacitors C_1 and C_2 kept the oscillation frequency are used. For symmetrical, the inductor is modeled as two components, which is parallel model with the inductance of L/2 ($L_1 = L_2 = L/2$), and conductance of $g_L/2$ ($g_{L1} = g_{L2} = g_L/2$). Similarly, the varactors are modeled as the parallel of the capacitance C_{var} ($C_{var1} = C_{var2} = C_{var}$) and conductance g_{var} ($g_{var1} = g_{var2} = g_{var}$). While $g_{m,n}$ and $g_{m,p}$ are small signal transconductances of the cross–coupled NMOS and PMOS pair to form the negative resistors. The conductances, $g_{o,n}$ and $g_{o,p}$, are the output conductances of the NMOS and

PMOS pair. C_{NMOS} and C_{PMOS} are capacitances associated to the gate of NMOS and PMOS ($C_{NMOS} = C_{gs,n} + C_{db,n} + 2C_{gd,n}$, $C_{PMOS} = C_{gs,p} + C_{db,p} + 2C_{gd,p}$), which will impact the oscillation frequency [8]. R_p and C_p model the parasitic effects due to interconnect of the layout and pad for RF measurement.

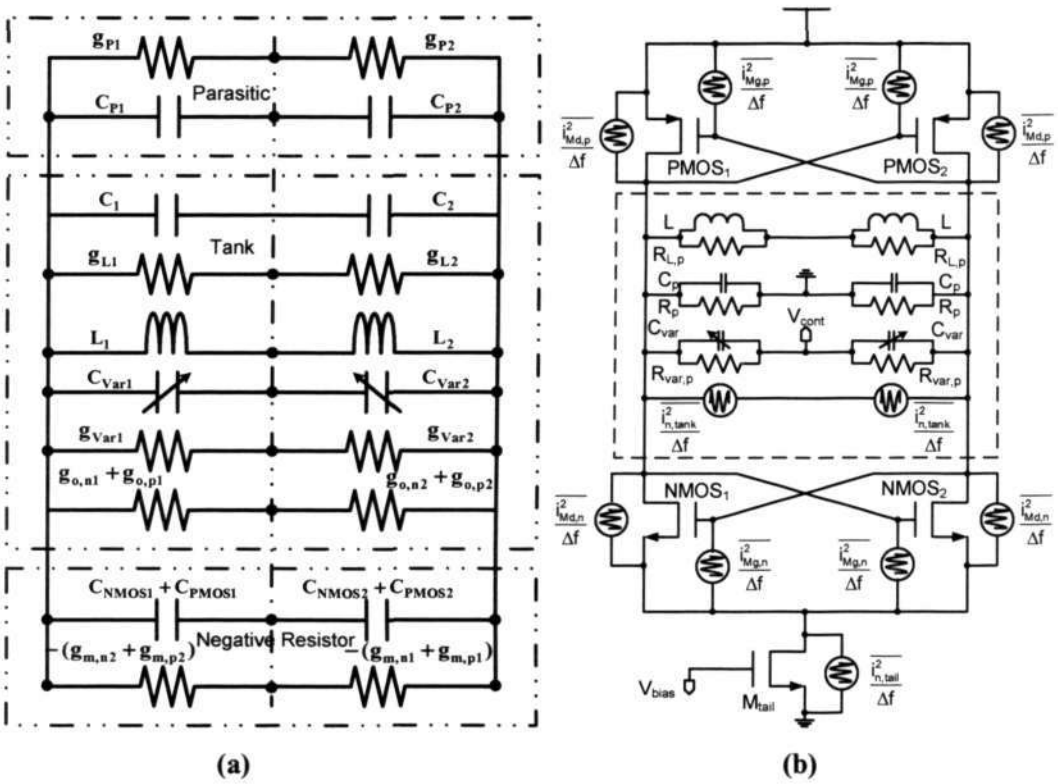


Fig. 3.2 (a) Equivalent circuit of the LC VCO, (b) Complementary LC VCO with noise sources.

3.2 Associate Noise Sources of LC VCO

Fig.3.2 (b) depicts the total noise sources existing in an LC VCO. In general, those noise sources are viewed as the three main contributions: noise from the LC tank resistor, R_{tank}, noise from the active devices as well as the noise contribution of the tail transistor as shown in Fig.3.2 (b).

3.2.1 Noise Sources of the Tank

The noise contribution from the effective resistance of the tank (R_{tank}) is presented by the current noise PSD:

$$\frac{\overline{i_{n,tank}^2}}{\Delta f} = \frac{4kT}{R_{tank}} \tag{3.1}$$

Similar calculation can be used to determine the current noise spectral density of the tank:

$$\frac{\overline{i_{ind}^2}}{\Delta f} = 4kTg_L \tag{3.2}$$

$$\frac{\overline{i_{var}^2}}{\Delta f} = 4kTg_{var}/2 \tag{3.3}$$

here, the conductance of the inductor, g_L , is extracted by equation (3.4) and the conductance of varactors, g_{var} , is given in equation (3.5). The quality factor of the inductors Q_L in equation (3.4) and varactors Q_{var} in equation (3.5) can be extracted by S–parameters' simulation for the inductor and varactors respectively. The noise source of the tank consisted of $\frac{\overline{i_{var}^2}}{\Delta f}$ and $\frac{\overline{i_{ind}^2}}{\Delta f}$ can be controlled to be lower by designers and the process technology. We treat them as a constant during analysis later.

$$g_L = \frac{1}{R_{L,p}} = \frac{1}{Q_L \cdot \omega \cdot L} \tag{3.4}$$

$$g_{var} = \frac{1}{R_{var,p}} = \frac{\omega \cdot C_{var}}{Q_{var}} \tag{3.5}$$

while $R_{L,p}$ and $R_{var,p}$ are parallel resistances of inductor and varactors respectively as shown in Fig.3.2(b).

3.2.2 Upconversion of 1/f Noise in the Tail Transistor

The mechanism of the flick noise upconversion is explained by Rael [50]. When the cross–coupled LC VCO circuit is unbalanced, the common mode node of the current source oscillates at twice the oscillator frequency, $2\omega_0$, because the current source is pulled every time as one of the differential transistors switches on. Through the channel length modulation, the noise of the tail current source (M_{tail} shown in Fig. 3.2(b)) is upconverted to $2\omega_0$. The upconverted noise enters the LC–tank and is mixed with the fundamental frequency, resulting in the phase noise sidebands at the oscillator frequency and 3rd harmonics. Therefore, to minimize the upconversion of the flick and white noises from the tail transistor, balance must be preserved, meaning that all even harmonics must be suppressed. Odd harmonics have little importance for the flick noise upconversion because they do not affect the symmetry. The flick noise from the tail transistor is the main contributor to $1/f^3$ phase noise. The contribution of the differential transistors is smaller due to the high frequency operation. The flick noise is correlated noise and can only exist in the systems with memory. When transistors are ideally switched, all memories and the consequently flick noise are removed [51]. When the switching is not ideal, a small amount of the differential MOSFET flick noise is unconverted. Therefore, the symmetry of the cross–coupled LC VCO is very important and critical for suppression of the 1/f noise upconversion. Lower 1/f noise of the tail transistor can also reduce the upconversion [8], in our designs, we make the area of the tail transistor as large as possible so that it guarantees the current enough to LC tank to suppress

upcoversion. Therefore, the upconversion of the 1/f noise in the tail transistor will not affect the phase noise of the fundamental frequency much in our methodology.

3.2.3 The Noise Sources of the Active Devices

3.2.3.1 High Frequency Noise of the MOS Transistors

It has been known that Non–Quasi–Static (NQS) effect influences the power spectral density of the drain current noise at very high frequencies because the thermal noise in the strong inversion saturation region is the result of random potential fluctuations in the channel. These fluctuations are coupled to the gate terminal through the oxide capacitance, and cause a gate noise current to flow even if all terminal voltages are fixed [52] [53]. This current is called induced gate noise. At high frequencies, the impedance of the gate capacitance becomes smaller, and this effect becomes more pronounced. Thus, only channel noise is not enough to model the noise characteristics of the MOS transistors when it operates at high frequency. Fig.3.3 shows an equivalent small signal circuit model for high frequency noise of a MOS device, in which a common source configuration is used as the example. C_{gs} is the capacitance between the gate and source, R_{gs} is an equivalent assuming resistor which produces the same amount of the thermal noise as the induced gate current, and its value is equal to $1/g_g$ (g_g is caused by distributed nature of channel). $y_m \upsilon_{gs}$ is the small signal current existing in the channel. The reciprocal of R_{ds} is tracking the channel resistance, which is equal to $1/g_{d0}$ (g_{d0} is defined as channel resistance with $V_{ds} = 0$). The current noises of $\frac{\overline{i_{Mg}^2}}{\Delta f} = 4KT\delta g_g$ and

$\frac{\overline{i_{Mg}^2}}{\Delta f} = 4KT\gamma g_{d0}$ are the power spectral densities of the induced gate current noise and drain current noise respectively. δ is gate noise coefficient and γ is called excess noise factor. The cross correlation coefficient of the above current noises is taken to be roughly a constant in the saturation. Therefore, the induced gate noise and drain noise can be considered as two independent noise sources in the following analysis [46] [54].

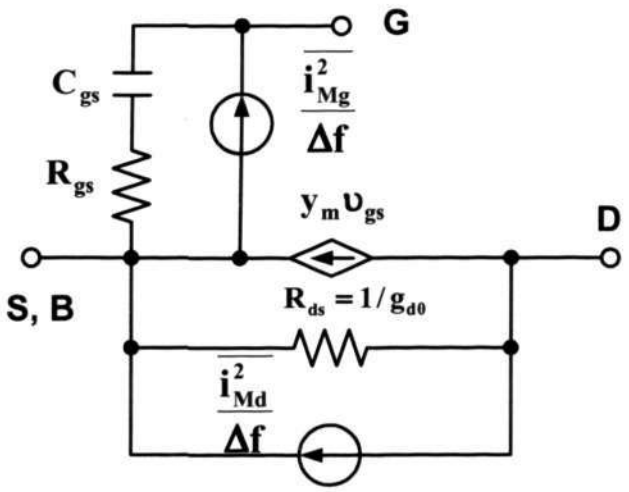


Fig. 3.3 Model of high frequency noise for MOSFET.

3.2.3.2 Active Device's Noise Sources in the Cross–Coupled LC VCO

A complementary cross–coupled differential pair has four current noise sources ($\frac{\overline{i_{Mg,n}^2}}{\Delta f}$, $\frac{\overline{i_{Mg,p}^2}}{\Delta f}$, $\frac{\overline{i_{Md,n}^2}}{\Delta f}$ and $\frac{\overline{i_{Md,p}^2}}{\Delta f}$) as shown in Fig.3.2 (b). However, if the differential pair is switched to one side or the other, there are just two noise sources ($\frac{\overline{i_{Mg,n}^2}}{\Delta f}$ and $\frac{\overline{i_{Mg,p}^2}}{\Delta f}$) due to g_g as given in Fig.3.4 (a), in which the output is further away from the differential zero because the MOSFET is at the deep saturation region. Therefore, the oscillation samples

the MOSFET noise at every differential zero crossing, that is, at the saturation region of the MOSFET when the oscillator is at steady state [55], and the maximum effect on the phase is caused. Thus, Fig.3.4 (b) is adopted in the novel methodology. Although the noise is cyclostationary, its spectrum is white.

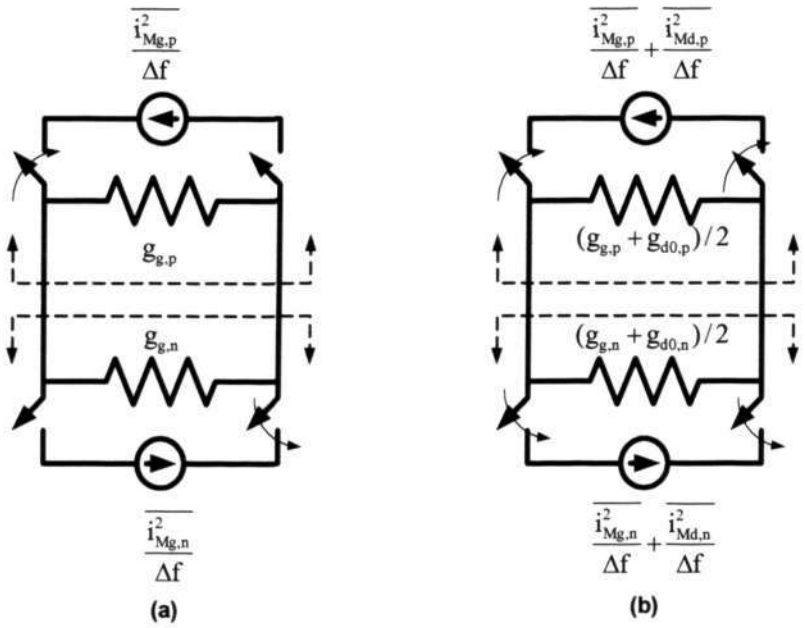


Fig. 3.4 Model of the active device noise contribution in complementary cross–couple LC VCO during switching, (a) Further away zero differential, (b) Nearby zero differential.

We cite a term $\frac{\overline{i^2_{n,active}}}{\Delta f}$ represents the sum of the current noise power spectral density of the active device in the LC VCO, which is the sum of the channel current noise, $\frac{\overline{i^2_{Md}}}{\Delta f}$, the induced gate noise, $\frac{\overline{i^2_{Mg}}}{\Delta f}$, [45] [47]. Therefore, we have:

$$\sum \frac{\overline{i^2_{n,active}}}{\Delta f} = \frac{\overline{i^2_{Md,n}}}{\Delta f} + \frac{\overline{i^2_{Md,p}}}{\Delta f} + \frac{\overline{i^2_{Mg,n}}}{\Delta f} + \frac{\overline{i^2_{Mg,p}}}{\Delta f} = \frac{\overline{i^2_{Md}}}{\Delta f} + \frac{\overline{i^2_{Mg}}}{\Delta f} \tag{3.6}$$

According to the classical Thevenin–to–Norton conversion, the current power spectral densities in the differential cross–coupled VCO are given as:

$$\frac{\overline{i_{Md}^2}}{\Delta f} = \gamma \cdot 4kT(g_{d0,n} + g_{d0,p})/2 \tag{3.7}$$

$$\frac{\overline{i_{Mg}^2}}{\Delta f} = \delta \cdot 4kT(g_{g,n} + g_{g,p})/2 \tag{3.8}$$

Where, γ is varied from 2.5 to 2/3 when the gate length is increased normally. Correlation factor, δ, typically ranges from 0.35 to 0.3 for short channel devices and 0.395 for long channel devices [55]. However, in practice, δ will rise to values from 2 to 5 due to hot electron effects [46]. Therefore, for simplify evaluation, $\delta \approx 2\gamma$ is adopted in our methodology.

3.2.3.3 Optimization Channel Length L_{ch} of the Active Device

The noises from the cross–coupled NMOS and PMOS are the main contribution to the phase noise of a cross–coupled LC VCO. Reducing the channel noise and the induced gate noise is still a stringent challenge for RF IC designs. Hence, a novel methodology to degrade the noise source from the NMOS and PMOS pairs is necessary and important to improve the phase noise performance of VCOs.

The channel conductance g_{d0} and the gate transconductance g_g are given by equation (3.9) and equation (3.10) for a MOSFET respectively [46]:

$$g_{d0} = \frac{I_{dc}}{E_{sat} \cdot L_{ch}} = \frac{\alpha_1}{L_{ch}} \quad \text{, where} \quad \alpha_1 = \frac{I_{dc}}{E_{sat}} \tag{3.9}$$

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_{d0}} = \frac{\omega^2 C_{gs}^2 E_{sat} \cdot L_{ch}}{5I_{dc}} \tag{3.10}$$

Although the values of g_g and g_{d0} vary with the change of the operating points of the transistors in the course of oscillation, the bias conditions for g_g and g_{d0} is $V_{gs}=V_{dd}/2$ when the voltage across the LC tank is zero (i.e., differential cross zero point, that also means that the active devices are in the saturation). From Fig.3.1 (a), it should be observed that the drain current of NMOS and PMOS, I_{dc}, is equal to $0.5I_{bias}$ when the oscillator is working closed to differential zero. E_{sat} is the electric field at which the carrier velocity reaches its saturation velocity. Thus, C_{gs} can be calculated as [46]:

$$C_{gs} = \frac{2}{3} C_{ox} \cdot W_{ch} \cdot L_{ch} = \frac{2}{3} \cdot S \cdot C_{ox} \cdot L_{ch}^2. \tag{3.11}$$

here, an aspect ratio of the MOS transistor, $S = \frac{W_{ch}}{L_{ch}}$, is implemented to simplify the derivation. W_{ch} is the channel width of the MOSFET, and L_{ch} is the channel length of the MOSFET. C_{ox} is the gate oxide capacitance. C_{gs} in equation (3.11) is substituted into equation (3.10), then g_g is rewritten as:

$$g_g = \frac{4\omega^2 \cdot S^2 \cdot C_{ox}^2 \cdot E_{sat} \cdot L_{ch}^5}{45I_{dc}} = \alpha_2 \cdot L_{ch}^5 \quad \text{where,} \quad \alpha_2 = \frac{4\omega^2 \cdot S^2 \cdot C_{ox}^2 \cdot E_{sat}}{45I_{dc}} \tag{3.12}$$

We assume NMOS and PMOS have the same channel length L_{ch} but different aspect ratio for the analysis. The current noise spectral density of the cross–coupled LC VCO, $\frac{\overline{i_{n,active}^2}}{\Delta f}$, in equation (3.6) is rewritten as:

$$\begin{aligned}\frac{\overline{i_{n,active}^2}}{\Delta f} &= \frac{\overline{i_{Md}^2}}{\Delta f} + \frac{\overline{i_{Mg}^2}}{\Delta f} \\ &= 4kT\gamma\left[2(g_{g,n} + g_{g,p}) + (g_{d0,n} + g_{d0,p})\right] \\ &= 4kT\gamma\left[2(\alpha_{2,n} + \alpha_{2,p})L_{ch}^5 + (\alpha_{1,n} + \alpha_{1,p})/L_{ch}\right]\end{aligned} \tag{3.13}$$

While $\alpha_{2,n}, \alpha_{2,p}$, $\alpha_{1,n}$, and $\alpha_{1,p}$ are the factors of transconductances in equation (3.12) and conductance in equation (3.9) for the NMOS and PMOS respectively, and they are all constants because NMOS and PMOS pairs are operating in the saturation region. The channel length, which is used to minimize the phase noise, is obtained by differential equation (3.13) with respect to the channel length as follow:

$$L_{opt} = \sqrt[6]{\frac{\alpha_{1,n} + \alpha_{1,p}}{10(\alpha_{2,n} + \alpha_{2,p})}} \tag{3.14}$$

It means that an optimization gate length exists for any cross–coupled differential VCOs as the noise contributions from active devices are reduced to the minimum level. Therefore, it breaks the conventional rule for RFIC designs to adopt the minimum technology size as the gate length of the active device to improve the phase noise performance.

The minimization phase noise of the cross–coupled LC VCO is achieved when the gate length of the active device is equal to the optimum gate length L_{opt}. It is very useful to improve the phase noise performance of VCOs for the design engineer. The total thermal noise of the LC VCO can be expressed by equation (3.15):

$$\begin{aligned}\sum \frac{\overline{i_n^2}}{\Delta f} &= \frac{\overline{i_{n,active}^2}}{\Delta f} + \frac{\overline{i_{n,tank}^2}}{\Delta f} + \frac{\overline{i_{n,tank}^2}}{\Delta f} \\ &= (4kT\gamma g_{d0,n} + 4kT\delta g_{g,n} + 4kT\gamma g_{d0,p} + 4kT\delta g_{g,p}) + (4kTg_L + 2kTg_{var})\end{aligned} \tag{3.15}$$

3.3 Linear Time Variant (LTV) Phase Noise Analysis

Linear time variant analysis method introduces an impulse sensitivity function (ISF) for the excess phase of the LC VCO and it is a general method to calculate the total phase noise of an oscillator with multiple nodes and multiple noise sources [47].

3.3.1 Define Impulse Sensitivity Function (ISF) $-\Gamma(\omega_0 t)$

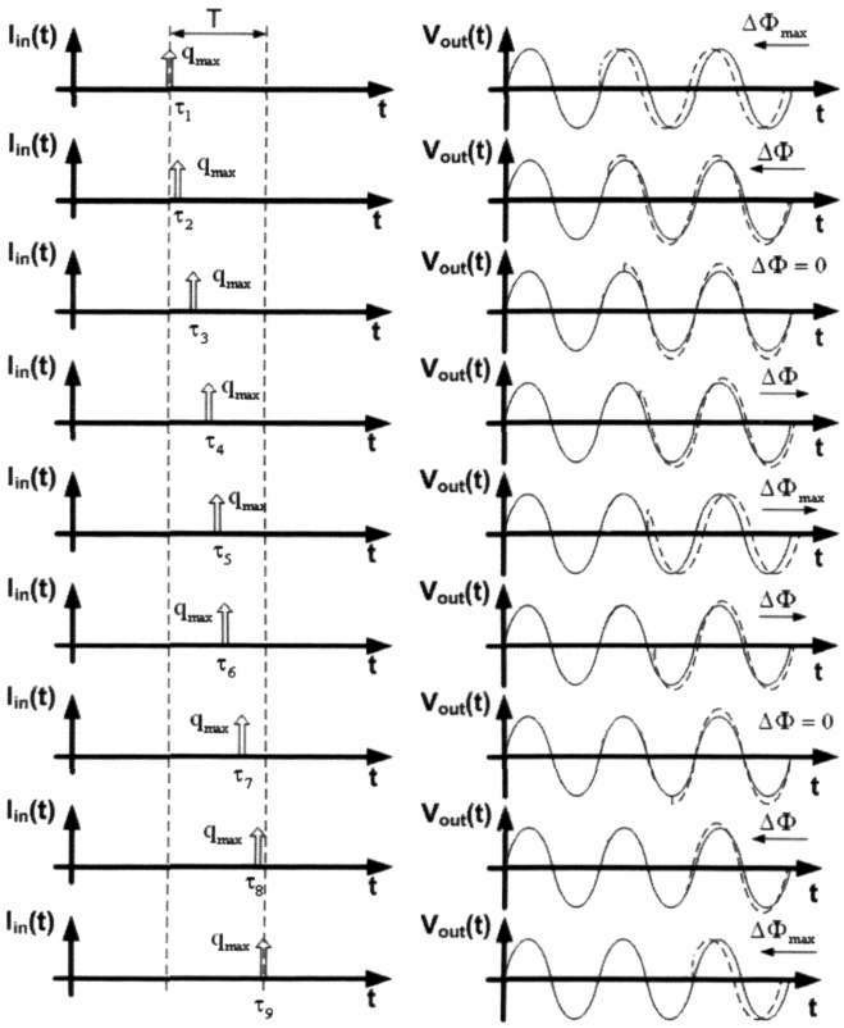


Fig. 3.5 Impulse response of an ideal LC oscillator when the current noise is injected at the varying time.

Impulse Sensitivity Function (ISF) is utilized to the impact of the current noise on the amplitude and phase through their associated impulse responses, i.e., its impact on the phase and amplitude changes if we vary the time at which the current impulse is injected. Therefore, the impact of the current noise is time–varying as shown in Fig.3.5. We can observe that the phase is impacted high when the impulse occurs close to the differential zero of the VCO output and impacted low when the impulse occurs at peak of output, and vice versa for the amplitude deviations. However, the amplitude deviations are suppressed to zero by an explicit automatic gain control (AGC) or the intrinsic nonlinearity of the device. The phase deviations are accumulated in the whole system, and its persist indefinitely. Thus, we will focus on the effect of the phase.

The ISF is constructed by calculating the phase deviations as the impulse position is varied because it is periodic with the same period as the VCO output as given in Fig.3.6. For the differential output, the ISF is approximately proportional to the derivative of the VCO output waveform, and the unit phase impulse responses, $h_{\Phi}(t,\tau)$.

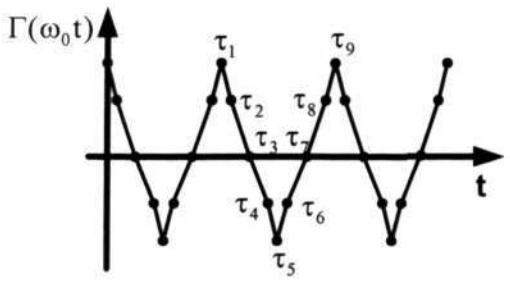


Fig. 3.6 ISF function.

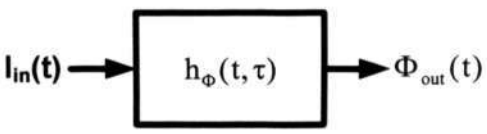


Fig. 3.7 Equivalent diagram of h_{Φ}.

3.3.2 Parameterize Phase Impulse Response ($h_\Phi(t,\tau)$) in Terms of the ISF

$h_\Phi(t,\tau)$ is used to characterize the phase deviations, which is defined as equation (3.16). Here $u(t)$ is the unit step and τ is the time when the impulse is injected. The equivalent system of the phase noise is modeled in Fig.3.7.

$$h_\Phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{3.16}$$

Since the ISF is a periodic function at frequency ω_0, only noise around DC, ω_0 and its harmonics will result in the non–zero excess phase. Noise at all other frequencies will average out over the time. In order to analysis simplified, the ISF can be expanded in Fourier series as:

$$\Gamma(\omega_0\tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau + \theta_n) \tag{3.17}$$

The coefficients c_n represent how much noise is contributed from the vicinity around frequency $n\omega_0$ where n=0,1,2….

The phase deviation $\Phi(t)$ for an arbitrary noise current input can be calculated using the superposition integral as equation (3.18). It results that noise from the current source is mixed down from different frequency bands and scaled according to the ISF coefficients [47].

$$\Phi(t) = \int_{-\infty}^{\infty} h_\Phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau \tag{3.18}$$

where $i(\tau)$ is the current impulse injected at the node of the circuit, and $\Gamma(\omega_0\tau)$ is the impulse sensitivity function (ISF) as expressed by equation (3.17). The ISF is essentially

a transfer function between an arbitrary noise source and an excess phase at the output of the oscillator from Fig.3.2 (b). q_{max} is the maximum charge swing, and $q_{max} = C_{node} V_{max}$, where V_{max} is the voltage swing across the capacitor at the node of the circuit.

3.3.3 Phase Noise Calculation

Submitted equation (3.15) into equation (2.38), the phase noise of an oscillator due to the thermal noise can be rewritten as:

$$L(\Delta\omega) = 10\log\left(\frac{\Gamma_{rms}^2}{q_{max}^2} \cdot \frac{\sum \frac{\overline{i_n^2}}{\Delta f}}{2 \cdot (\Delta\omega)^2}\right) \tag{3.19}$$

and the single–side bandwidth (SSB) phase noise of an oscillator in equation (2.39) due to the flicker noise is rewritten as:

$$L(\Delta\omega) = 10\log\left(\frac{c_0^2}{q_{max}^2} \cdot \frac{\sum \frac{\overline{i_n^2}}{\Delta f}}{8 \cdot (\Delta\omega)^2} \cdot \frac{\omega_{1/f}}{\Delta\omega}\right) \tag{3.20}$$

The quantity Γ_{rms} is the rms value of the ISF. In this work, all ISFs were obtained using Spectre Time Simulations (Periodic Steady–State) by injecting a small current pulse into an oscillator node over one oscillation cycle, and observing the output phase shifts several cycles later. $\omega_{1/f}$ is the corner frequency of the device 1/f noise, and c_0 is the DC value of the ISF, which can be calculated by $c_0 = \frac{1}{2\pi}\int_0^{2\pi} \Gamma(x)dx$.

In general, these noise sources are cyclostationary because of the periodic changes in the currents and voltages of the active devices. Consequently, the cyclostationary nature of the noise sources must be considered in a completive analysis. The ISF contains only the sensitivity to noise as a function of the time, but it does not reveal the information on the time duration, for which a noise source is present. Hence, the effective ISF is given by [47]:

$$\Gamma_{rms,eff}(x) = \Gamma_{rms}(x) \times \alpha(x) \tag{3.21}$$

where $\alpha(x)$ represents the Noise Modulation Function (NMF).

3.3.4 Steps to Achieve the Minimal Phase Noise

The steps of the novel methodology to achieve the minimal phase noise are summarized as:

Step 1: Evaluate the optimization gate length of the active device by equation (3.14).

Step 2: Calculate minimize spectral density of each oscillator noise source by using the optimization gate length of the active device.

Step3: Derive the impulse sensitivity function of each oscillator source after the transient simulation is done when a current noise is injected at the node of the oscillator circuit (Cadence RF Spectre).

Step 4: Combine above results to obtain $\Gamma_{rms,eff}(\omega_0 t)$ for each oscillator noise source.

Step 5: Calculate Fourier Series Coefficient for each $\Gamma_{rms,eff}(\omega_0 t)$.

Step 6: Calculate the overall output phase noise using the results from step 4, 5 and the phase noise expressions in equation (3.19) and equation (3.20).

3.4 Conclusion

The effects of various noise sources in the circuit are analyzed, and it was shown that the noises caused by differential pair can be reduced by exploiting cyclostationary properties of the sources. A novel methodology that achieves the minimal phase noise of the cross–coupled LC VCO is proposed. The fundamental relationships between the gate length and the thermal noise of the active devices used in the cross–coupled LC VCO are derived. An optimization gate length is achieved for the minimal phase noise of the LC VCO. Linear time variant phase noise analysis is discussed based on the novel methodology. This is resulting that the minimal phase noise is obtained by using the optimization gate length of the active device. The steps to optimize the phase noise performance of the LC VCO are summarized. It is very useful for the RF IC designer and also suitable for the other differential LC VCOs.

This methodology will be verified with two designs in the next Chapter.

CHAPTER 4

Experiments to Verify the Novel Methodology

To verify the novel methodology, two LC VCOs as the design examples are presented in this Chapter.

First, a 2 GHz VCO utilized the optimization gate length of the active device is designed and implemented. The measured phase noise performances are –103.3 dBc/Hz at the offset frequency of 100 kHz away from the carrier of 1.97 GHz, –118.9 dBc/Hz at the offset frequency of 600 kHz, and –128 dBc/Hz at the offset frequency of 3 MHz. The frequency tuning range is 14% and the value of figure of merit (FOM) is 186. The power consumption is 3.15 mW. So far, to our knowledge, the performance of this VCO is the best one operating at 2 GHz at the time.

Second, a fully integrated 10 GHz CMOS LC VCO is designed and fabricated by a 0.18 μm CMOS technology. The design is based on the cross–coupled complementary oscillator configuration with around the tuning range of 1.1 GHz, from 9.3 GHz to 10.4 GHz. The low phase noise of –89 dBc/Hz at the offset frequency of 100 kHz away from the carrier of 9.83 GHz is measured. The power consumption of the core circuit is 5.8 mW. To our knowledge, the performances of this design are better than that of the reported 10 GHz–band CMOS oscillators in the literature at the time.

4.1 2 GHz Cross–Coupled LC VCO

Fig.3.2 (b) shows the schematic of the proposed 2 GHz LC VCO. The novel methodology is applied to design a 2 GHz LC VCO, in which the different sizes of the

cross–coupled NMOS and PMOS are given in Table.4.1. The resonant tank is consists of a spiral inductor of 4 nH with the quality factor of 8 and two PN varactors tuning range from 2 pF to 2.8 pF with the quality factor of 40. For making sure six VCOs to operate at the same frequency of 2 GHz, two capacitors C_1 and C_2 given in Fig.3.2 (Metal Insulator Metal, i.e., MIM cap) are utilized to compensate for the capacitance modification of the tank due to the different sizes of the NMOSs and PMOSs and the aspect ratio S for NMOSFETs and PMOSFETs in six cases is fixed respectively.

Table 4.1 Summary of the size of the NMOS and PMOS for 2 GHz VCOs.

Case	NMOS				PMOS				C_1&C_2
	L_{ch}(μm)	W_{ch}(μm)	N	S	L_{ch}(μm)	W_{ch}(μm)	N	S	(fF)
1	0.18	2.5	8	111	0.18	2.5	20	278	933
2	0.27	3.75	8	111	0.27	3.75	20	278	863
3	0.36	5	8	111	0.36	5	20	278	733
4	0.45	6.25	8	111	0.45	6.25	20	278	582
5	0.54	7.5	8	111	0.54	7.5	20	278	399
6	0.63	8.75	8	111	0.63	8.75	20	278	182

4.1.1 Verification and Results Discussion

Based on the above component sizes and parameters, an optimum channel length of 0.26 μm is calculated by using equation (3.14) for the designed 2 GHz VCO.

Six cases for six cross–coupled LC VCOs are simulated by the Spectre–RF of Cadence, in which the process design kit (PDK) is embedded to analysis the performances of the circuit design. The simulated phase noise performances at the offset frequency of 600 kHz are shown in Fig.4.1. Note that the VCO with a channel length of 0.27 μm in case 2 has the lowest phase noise of −123 dBc/Hz. Therefore, we observe that

the lowest phase noise point exists when the gate length of the active devices is varied from 0.18 μm to 0.63 μm.

As we know, γ is defaulted as 2/3 in BSIM3 model because of its limitation. However, in our design, γ around 2.0 is extracted when MOSFETs with 0.18 μm gate length are working in the saturation region (V_{ds}=V_{gs}≈0.9 V). While γ can be approximated as $\gamma = \frac{2}{3}\frac{g_m}{g_o}$ when the transistors operate in the saturation region [56]. Thus, γ is depending on the aspect ratio of the MOSFETs and bias conditions. Therefore, it has the same effect for the phase noise of six cases designed.

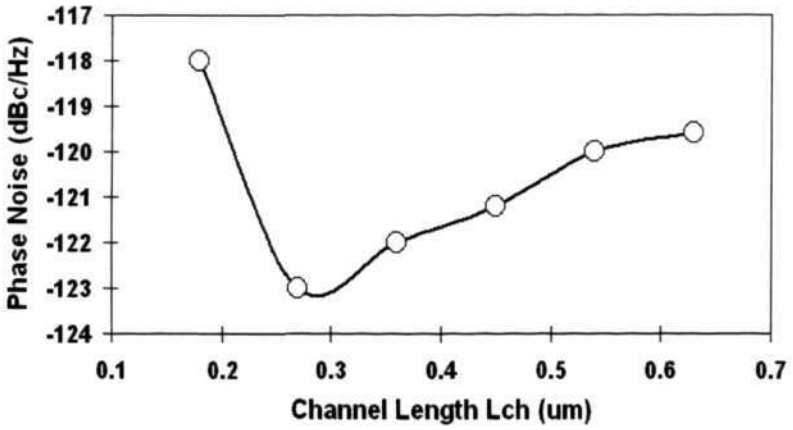


Fig. 4.1 Simulated phase noise performance of six VCOs.

4.1.2 Experimental Results

Case 2 is implemented by the CSM 0.18μm RF CMOS technology. Fig. 4.2 shows the VCO chip photograph. The area is approximately 0.5×0.6 mm^2. The phase noise performance showed in Fig.4.3 is measured by HP8563E Spectrum Analyzer. To measure the phase noise accurately, a GPG (Ground Power Ground) DC probe and a

HP11612B K21 Bias Network are utilized at the power supply, V_{dd}, around 1.8 V. DC bias of the tail transistor, V_{bais} is 0.8 V and the voltage V_{cont}, N+ terminal of the PN varactor, is 1.5 V (controlled voltage between two terminals of the PN varactor is around 0.6 V because P+ is connected to the output around 0.9 V DC level). The low phase noise of −103 dBc/Hz at the offset frequency of 100 kHz, −118 dBc/Hz at the offset frequency of 600 kHz and −128 dBc/Hz at the offset frequency of 3 MHz away from the carrier frequency of 1.968 GHz are achieved. The measured phase noise is around 5 dB higher than the simulated phase noise. This 5 dB discrepancy can be attributed to the uncertain channel noise factor, γ, which is around 2 in the implementation rather than 2/3, degradation of the tank amplitude caused the parasitic resistors in metal layers. Although the frequency is slightly shifted down to 1.968 GHz, it is in the acceptable range [57] [58] [59].

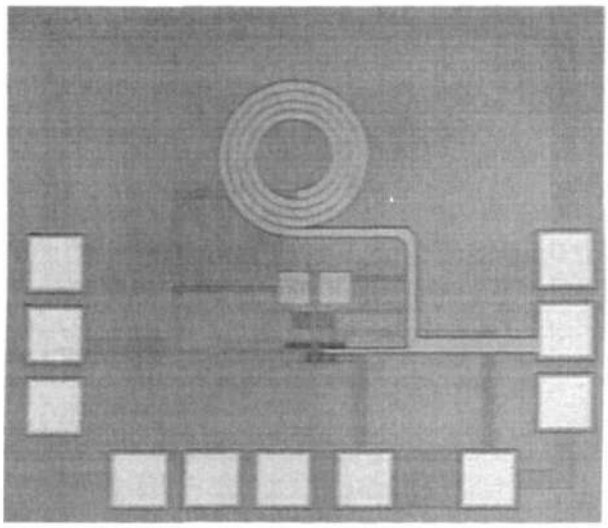


Fig. 4.2 Microphotograph of the test chip.

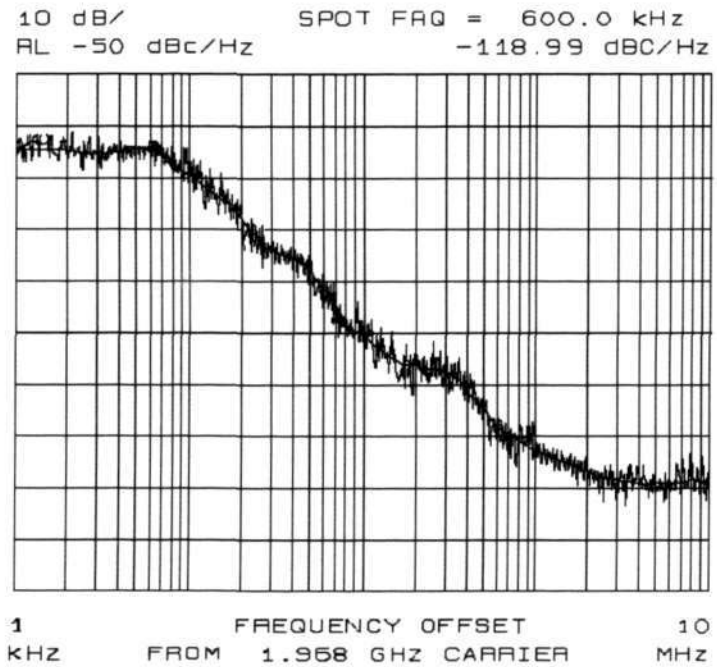


Fig. 4.3 Measured phase noise of 2 GHz VCO.

An optimized gate length of 0.27 μm for the lowest phase noise performance of the 1.968 GHz cross–coupled LC VCO implemented by the CSM 0.18 μm CMOS technology is obtained by the novel methodology, which is found useful to make a significant improvement for the phase noise performance of the cross–coupled LC VCO. A tuning range from 1.9 GHz to 2.18 GHz is depicted in Fig. 4.4.

The big value of Figure of Merit (FoM) for case2 is calculated by [60]:

$$\mathrm{FoM} = 10 \cdot \log\left(\left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{L(\Delta\omega) \cdot p}\right) \tag{4.1}$$

where ω_0 is the oscillation frequency, $\Delta\omega$ is the offset frequency, $L(\Delta\omega)$ is the phase noise at $\Delta\omega$, and P is the power consumption of 3.15 mW. The FoM of this VCO is 186, which is the highest FoM value compared with the reported literatures at the time as

pointed in Table.4.2. The excellent low phase noise and low power consumption for the LC VCO have been achieved.

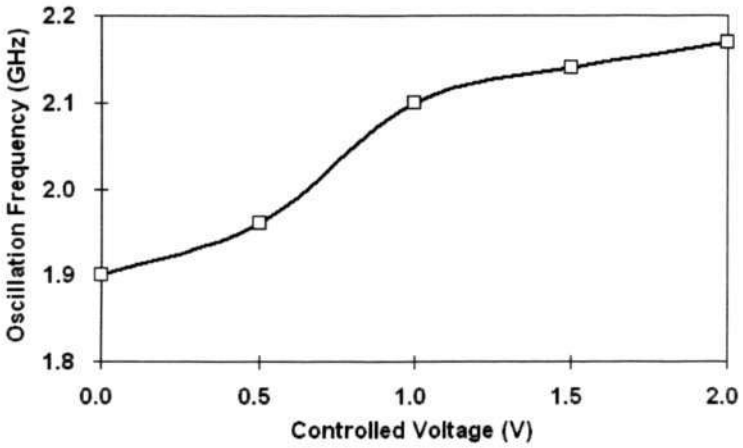


Fig. 4.4 Measured tuning range of the LC–VCO.

Table 4.2 Measured result compared with CMOS VCOs.

Ref.	Tech.	Frequency (GHz)	Phase noise (dBc/Hz)	Power Consumption (mW)	FoM
This work	0.18μm*	2.0	−118.9	3.15	186
[59]	0.25μm*	1.8	−121	6	182.8
[57]	0.65μm**	2.0	−116	6	177.1
[58]	0.35μm*	2.03	−117	10	177.5
[61]	0.65μm**	2.0	−126	34.2	181.1

Note: * -- CMOS; **-- BiCMOS; Phase noise is got at 600 kHz offset

4.2 9.3 ~10.4 GHz–Band Cross–Coupled Complementary Oscillator with Low Phase noise Performance

Based on the phase noise optimization methodology, the optimized gate length of the active device for a 10 GHz LC VCO calculated by equation (3.14) and the thermal noises of active devices (NMOSFETs and PMOSFETs) and LC tank are obtained. The LTV

phase noise analysis is verified then, the schematic used in the design is given in Fig.4.5, in which an impulse injection current source is connected to the output of the LC VCO.

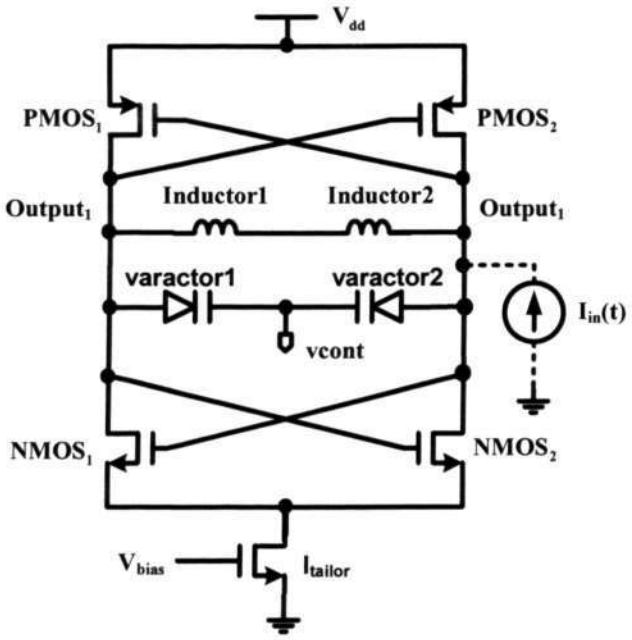


Fig. 4.5 Shematic of the 10 GHz LC VCO with an impulse injection current

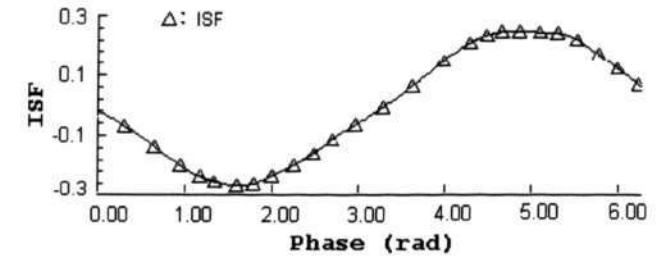
4.2.1 Phase Noise Estimation for 10 GHz LC VCO Used LTV Analysis

The simulated ISFs with an injected charge of 0.1 pC is shown in Fig.4.6 (a). The NMOS and PMOS noise modulation functions (NMF) are presented in Fig.4.6 (b), and the effective ISFs in Fig.4.6 (c). According to equation (3.21), the effective Γ_{rms} of all active devices' noise sources, $\Gamma_{rms,n,eff} = 0.19$ and $\Gamma_{rms,p,eff} = 0.15$ are obtained respectively when the LC VCO operates at 9.83 GHz. The effective ISFs of the active device and LC tank are summarized in Table.4.3. Therefore, the phase noise of –93 dBc/Hz at the offset frequency of 100 kHz away from the carrier of 9.83 GHz is calculated by equation (3.19). As such, the phase noise s of –95 dBc/Hz at the offset of 100 kHz and –89 dBc/Hz at the offset of 100 kHz are calculated when VCO operates at 9.3 GHz and 10.4 GHz respectively. From Table 4.3, the PSD of the active devices

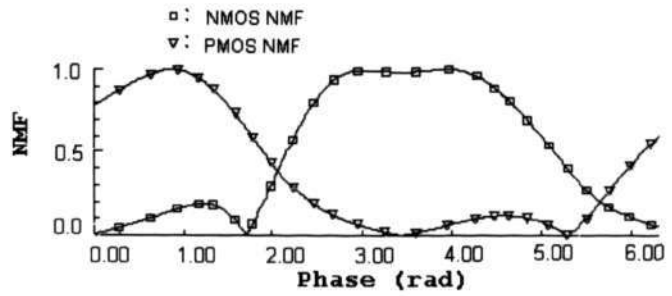
(NMOS and PMOS) is much bigger than that of the tank. Hence, the noises from the active devices are the main contributors to the phase noise of the VCO.

Table 4.3 PSD of all noise sources and effective ISF.

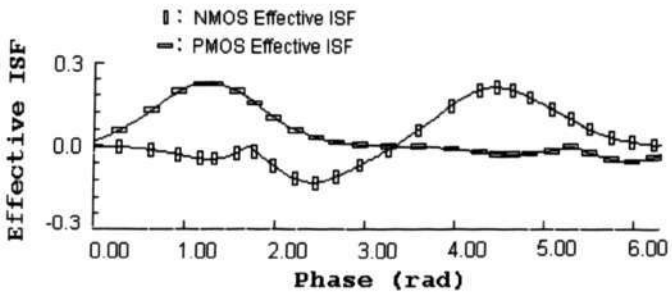
Noise Source	PSD (A^2/Hz)	Γ_{rms}
NMOS	2.86e-22	$\Gamma_{rms,n,eff} = 0.19$
PMOS	1.41e-22	$\Gamma_{rms,p,eff} = 0.15$
Tank	8.10e-23	$\Gamma_{rms,tank} = 0.28$



(a)



(b)



(c)

Fig. 4.6 (a) ISF (Γ_{rms} (x)) of NMOS and PMOS, (b) NMF (α(x)) of NMOS and PMOS, (c) Effective ISF ($\Gamma_{rms,eff}$ (x)) of NMOS and PMOS.

4.2.2 Experimental Results

A commercial 0.18 μm CMOS process (CSM 0.18 μm technology) is used to design and implement the VCO. Six metal layers are used in this process. The technology has a cutoff frequency, f_T, of 58 GHz, a maximum frequency, f_{max}, of 67 GHz [62], and the supply voltage of 1.8 V. Inductors are implemented by stacking the fifth metal layer and the top metal layer (the sixth metal layer) to prevent the loss of the metal and substrate. The simulation of the inductors predicts an inductance of 0.5 nH and an effective Q value of 10 at the operation frequency of 9.83 GHz, which is shown in Fig.4.7. The P+/Nwell varactor of the design incorporates a capacitance of C_{var} = 0.5 pF with the Q value of around 38 at 9.83 GHz, and the dynamic range, C_{max}/C_{min} is about 2.5 with 0 V < V_{var} < 4 V [62].

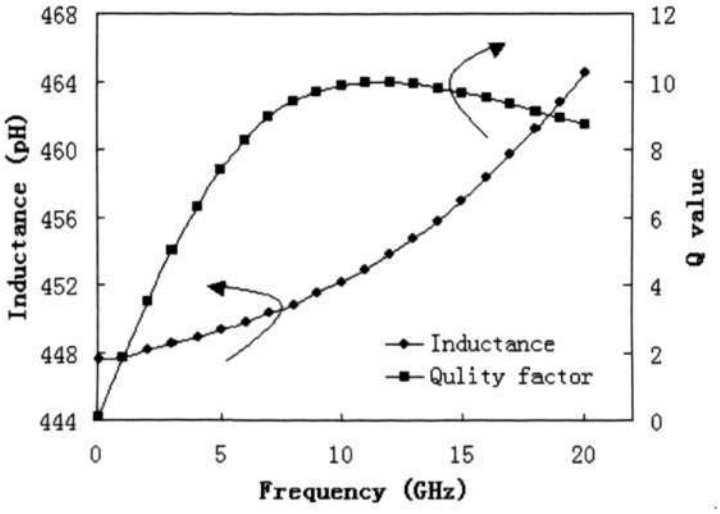


Fig. 4.7 Simulated inductance and Q value of the inductor.

The area of the die is approximately 0.5×0.6 mm^2 as shown in Fig.4.8. The VCO is measured on the wafer level. A GSG RF probe is used at the output of the oscillator ($Output_1$ or $Output_2$ as shown in Fig.4.5). The GPG DC probe connected to the Bias

Network is adopted for power supply V_{dd} to filter the original noise from the DC supply equipment HP4142.

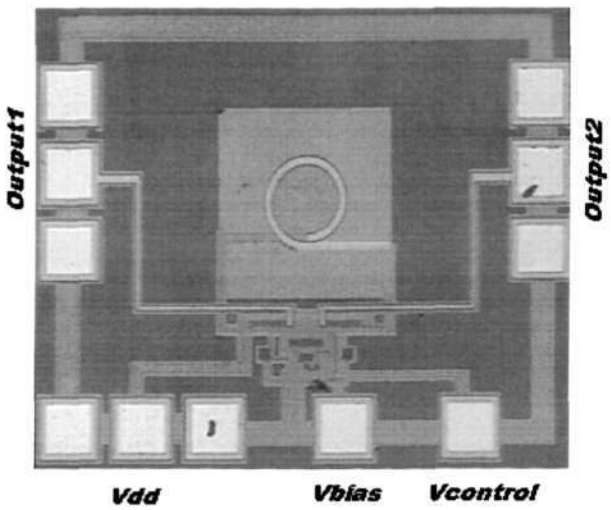


Fig. 4.8 Die photo of the LC tank oscillator.

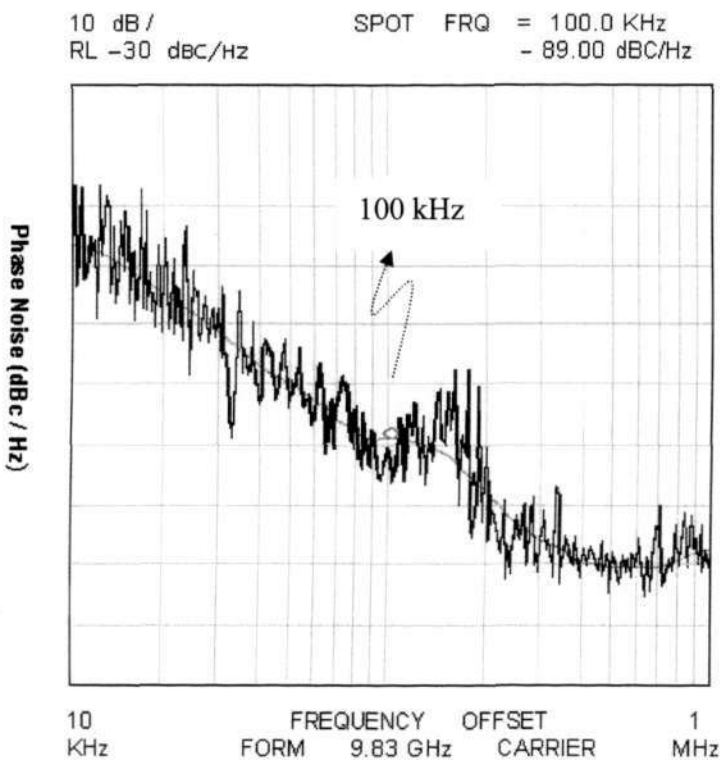


Fig. 4.9 Measured phase noise at 9.83 GHz.

The phase noise and the power spectral density have been measured using HP8564E spectrum analyzer, whose phase noise characteristic for the 9.83 GHz oscillator is shown in Fig.4.9. The phase noise is –91 dBc/Hz at the 100 kHz offset frequency away from the oscillator center frequency of 9.3 GHz, and –89 dBc/Hz at the 100 kHz offset frequency away from the oscillation frequency of 9.83 GHz, and –84 dBc/Hz at the 100 kHz offset frequency away from the scillation frequency of 10.4 GHz.

The FoM characteristic can be calculated by equation (4.1). Fig.4.10 depicts the curves of the oscillation frequency and FoM versus the controlled voltage (which is the voltage difference between the cathode and anode of the PN varactors) from the measurement, the tuning range around 1.1 GHz and FoM value of 165 at 9.83 GHz operation frequency are achieved.

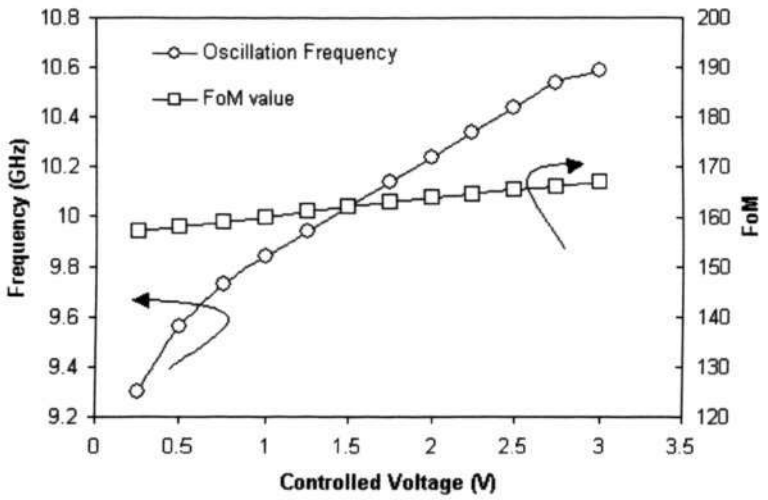


Fig. 4.10 Tuning characteristics and FoM of the VCO.

The phase noise performances from the measurement and LTV method for 9.83 GHz VCO are summarized in Table.4.4. The phase noise using LTV analysis has a good

agreement compared to the measured phase noise at the 100 kHz offset frequency, and the maximum difference between both is about 5 dBc/Hz due to the degradation of tank amplitude caused the parasitic resistors in metal layers. The performance of the 10 GHz VCO is the excellent one for 0.18 μm CMOS technology compared with the reported results in the literatures at the time.

Table 4.4 Summarization of the 10 GHz VCO performance.

Items	Measured	LTV method
Supply voltage	1.8V	1.8V
Core circuit power supply	5.8mW	5.6mW
Center frequency	9.83 GHz	10.2GHz
Tuning Range	11.2%	15.6%
Phase noise (f_0=9.3GHz, @100kHz)	−91dBc/Hz	−95 dBc/Hz
Phase noise (f_0=9.83GHz, @100kHz)	−89dBc/Hz	−93 dBc/Hz
Phase noise (f_0=10.4 GHz, @100kHz)	−84dBc/Hz	−89 dBc/Hz

4.3 Conclusion

The novel methodology is verified by two designs. One is a 2 GHz cross−coupled LC VCO, which has been designed and fabricated. It makes a significant improvement for the phase noise performance. The measured phase noise performance is −103.3 dBc/Hz at 100 kHz offset frequency, −118.9 dBc/Hz at 600 kHz offset and −128 dBc/Hz at 3 MHz offset, the power consumption is 3.15 mW. The FoM is 186. To authors' knowledge, this VCO is the best one among all the operation frequency of 2 GHz VCOs fabricated by 0.18 μm CMOS technology reported in the literature at the time

The other one is a 1.1 GHz tuning range from 9.3 GHz to 10.4 GHz VCO with the low phase noise of −89 dBc/Hz at the offset frequency of 100 kHz away from the center

frequency of 9.83 GHz, which is designed and fabricated by using CSM 0.18 μm technology. The power consumption of the core circuit of VCO is 5.8 mW, and the output peak–to–peak voltage is around 1.1 V. So far, this design is the first one to adopt the complementary cross–coupled differential architecture for 10 GHz–band CMOS VCO, and the performance of the designed VCO is the best one at the time. Further more, this design is very useful to the 10–Gb/s Clock and Data Recovery IC and the SONET communication application.

In conclusion, a novel methodology has a capability to minimize the phase noise performance of the LC VCO by optimization the gate length, and the phase noise predictions made are in good agreement with the measurements by the LTV phase noise analysis. This methodology breaks the traditionally methods that the minimal technology size is utilized as the channel length of the active devices to improve the phase noise during the design of the LC VCO.

CHAPTER 5

Noise Transfer Characteristics of a Charge–Pump PLL Based Frequency Synthesizer

Charge–pump phase locked loop (CPLL) based synthesizers are widely used in microprocessors, wireless receivers, serial link transceivers and disk drive electronics [63] [64] [65] [66] [67]. The most challenging task for the design of a high–frequency synthesizer is the tight tradeoff among the settling time, the loop bandwidth and the amplitude of the ripple on the oscillator control line. In an integer–N PLL based frequency synthesizer, fast frequency settling and narrow channel spacing are reciprocally exclusive. Fast settling demands a wide closed loop bandwidth, which is typically limited to $1/10^{th}$ of the reference frequency because of stability considerations [68] [69] [70] [71]. This limits the performance of such synthesizers, in terms of channel switching speed and the magnitude of the reference sidebands that appear in the synthesizer's output.

Although there are many publications in the literature to provide the useful insights into optimizing the loop dynamics [68] [72], precise analysis and mathematical clarity of the phenomenon are still absent. In addition, most of studies use a continuous time analysis (the s–domain model), even though the continuous time approximation is invalid for wide loop bandwidth frequency synthesizers because of the update rates of the phase frequency detector (PFD). In 1998, P. Hein and W. Scott [73] first introduced a discrete time analysis (z–domain model) to overcome the issues pertaining to the wide loop

bandwidth system. However, the analysis in [73] only focused on the input jitter transfer function and the second order PLLs.

In this chapter, an optimization methodology and a precise calculation for all loop parameters of the third order, Type–II CPLL is proposed. An exact analysis and accurate mathematical model for three main noise transfer functions of the synthesizer system are presented. Those noise transfer functions in the z–domain model are derived and compared with the results from s–domain model. It is found that the noise peak from the inherent sampling behaviors always exists in the loop constantly, and is not suppressed by a loop filter with the wide loop bandwidth.

On the other hand, this kind of noise peak makes the system unstable. The stability limit of the wide loop bandwidth frequency synthesizer is extracted by the behavioral simulation using the z–domain model. This simulation depends on the phase margin and the ratio between the reference frequency and the loop bandwidth and a limitation of the ratio between the reference frequency and loop bandwidth for different phase margins is given and verified using RFHDL. This limitation is very useful when designing synthesizers with a wide loop bandwidth.

5.1 Charge–Pump PLL Based Frequency Synthesizer Architecture

Almost all synthesizers used in wireless communication systems are based on charge–pump PLLs (CPLLs). As shown in Fig.5.1, a frequency synthesizer consists of a phase frequency detector (PFD), a charge pump (CP), a loop filter (LF), a voltage controlled oscillator (VCO), and a divider. The PFD compares the phase and frequency between the reference signal and the output signal of the divider. Depending on the phase

and frequency differences, the CP injects the appropriate currents to adjust the control voltage of the VCO. The loop filter filters out the high frequency components and extracts the average of the control voltage to improve the phase noise of the VCO. In order to obtain the frequency at the desired channels with a fixed input reference frequency, a frequency divider is used in the feedback path. The VCO is adjusted by the loop until the phase of the reference θ_{in} is equal to the phase of the divider output θ_{div}. Finally, the desired output frequency of the synthesizer is locked.

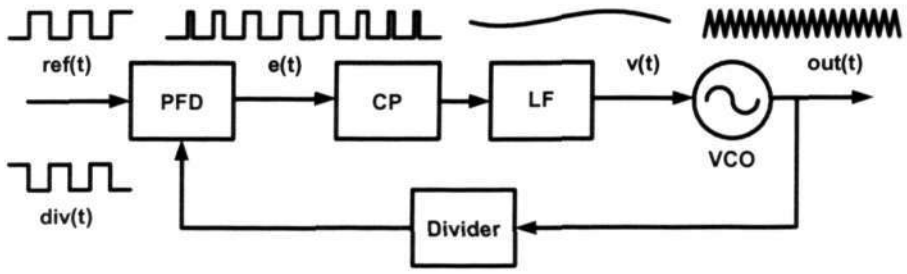


Fig. 5.1 Block diagram of the CPLL based frequency synthesizer.

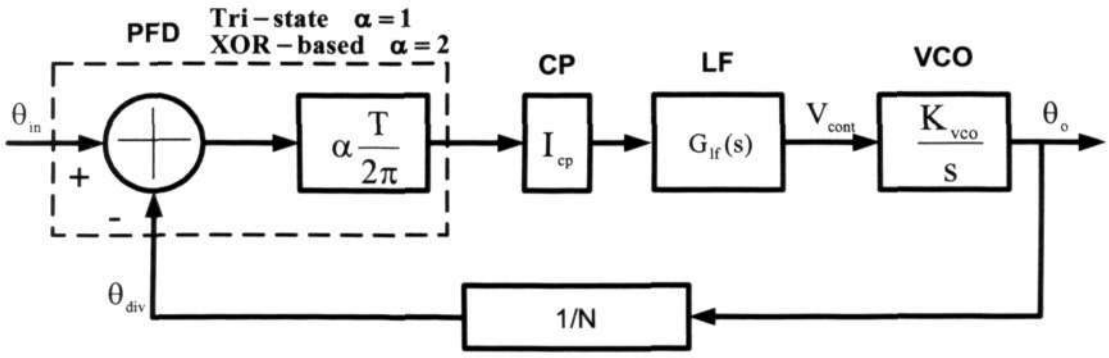


Fig. 5.2 Linear behavior model of the CPLL based frequency synthesizer.

5.1.1 Linear Behavior Model

A linear behavior model for the proposed frequency synthesizer is shown in Fig.5.2,

where the phases of the signals are used to represent the state variables. The phase frequency detector is a block with gain of $1/2\pi$. The value of α depends on the PFD operation methods: it is equal to 1 for a PFD with tri–state operation and 2 for a PFD with XOR–based operation. The resulting phase error controls the current I_{cp} of the charge pump. A loop filter with a low–pass transfer function $G_{lf}(s)$ sends out a DC value to the voltage controlled oscillator. The VCO is represented by a gain of K_{VCO}/s with a pole at zero frequency. The output of the VCO is then divided by N and fed back to the phase frequency detector. If the loop breaks at the point after the divider, then the open–loop transfer function G(s) is expressed as follows [35]:

$$G(s) = \frac{1}{2\pi} I_{cp} G_{lf}(s) \frac{K_{VCO}}{s} \frac{1}{N} = \frac{I_{cp}}{2\pi} \frac{K_{VCO}}{N \times s} G_{lf}(s) \tag{5.1}$$

5.1.2 Loop Filter

The choice of the transfer function $G_{lf}(s)$ in equation (5.1) is very important. It determines the loop bandwidth of the frequency synthesizer, which is related to the performance of the whole frequency synthesizer, in terms of, for example, the phase noise, spurious tone performance and settling time. The order proposed here should be large enough to reduce the output phase noise of the charge pump and the loop filter.

In order to minimize the phase noise and power consumption of the synthesizer, a standard second order, type–II passive loop filter is shown in Fig.2.11. The filter consists of an R–C series network (C_1, R_1) arrange in parallel with a capacitor (C_2). From the impedance of the loop filter given in equation (2.20), the transfer function of the loop filter is rewritten as:

$$G_{lf}(s) = \frac{V_{out}}{I_{cp}} = \frac{1+s\tau_z}{sC_i(1+s\tau_p)} = \frac{1}{(C_1+C_2)} \frac{(\frac{s}{\omega_z}+1)}{s(\frac{s}{\omega_p}+1)} \tag{5.2}$$

where, τ_z and τ_p are defined in equation (2.18) and (2.19) respectively, $C_i = C_1 + C_2$.

The filter has one zero at $\omega_z = \frac{1}{\tau_z}$, which is used to increase the phase margin at the unity–gain frequency ω_c (i.e., crossover frequency or loop bandwidth) of the open loop. It also has two poles, with one of them is at $\omega_p = \frac{1}{\tau_p}$. This pole can be used to improve the level of noise suppression, although it limits the phase margin. A compromise between open loop gain and phase margin is presented later.

5.1.3 Methodology to Optimize Loop Parameters

Combining equation (5.1) and equation (5.2), an open loop transfer function for the CPLL based frequency synthesizer is rewritten as:

$$G(s) = \frac{I_{cp} \cdot K_{VCO}}{2\pi \cdot N \cdot (C_1+C_2)} \times \frac{(\frac{s}{\omega_z}+1)}{s^2(\frac{s}{\omega_p}+1)} = k_s \times \frac{(s+\omega_z)}{s^2(s+\omega_p)} = \frac{k_s s + k_s \omega_z}{s^3 + \omega_p s^2} \tag{5.3}$$

$$k_s = \frac{I_{cp} \cdot K_{VCO} \cdot \omega_p}{2\pi \cdot N \cdot (C_1+C_2) \cdot \omega_z} = \frac{I_{cp} K_{vco}}{2\pi N C_2} \tag{5.4}$$

The Bode plot of the open loop gain is shown in Fig.5.3. The phase margin is expressed by equation (5.5) when the loop gain frequency is equal to the cross–over

frequency (ω_c), and while the loop gain is unity. It can be seen that the third pole degrades the phase margin.

$$\Phi_M = \arctan\frac{\omega_c}{\omega_z} - \arctan\frac{\omega_c}{\omega_p} = \arctan a - \arctan(1/b) \quad \begin{vmatrix} a = \dfrac{\omega_c}{\omega_z} \\ b = \dfrac{\omega_p}{\omega_c} \end{vmatrix} \tag{5.5}$$

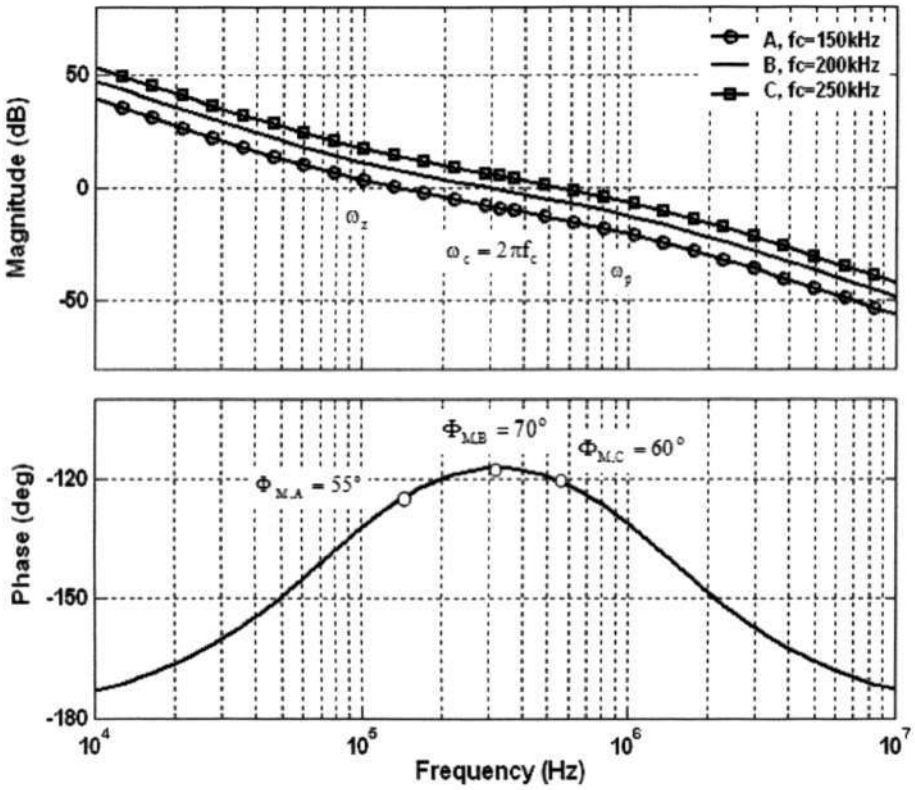


Fig. 5.3 Bode plot of open loop transfer function.

Here, a is the ratio of the cross–over frequency ω_c and the zero frequency ω_z, while b is the ratio of the pole frequency ω_p and the crossover frequency ω_c. The maximum phase margin can be calculated by equating the first derivative of Φ_M to be zero. It can be seen that the maximum phase margin $\Phi_{M\,max}$ occurs when:

$$a = b = \sqrt{\frac{C_1}{C_2} + 1} \Rightarrow C_1 = (a^2 - 1)C_2 \tag{5.6}$$

$$\Phi_{M\max} = \arctan a - \arctan \frac{1}{a} \tag{5.7}$$

Then the crossover frequency can be given when $|G(s)| = 1$ at the maximum phase margin.

$$\omega_c = (k_s/b)^{\frac{1}{2}} \left(\frac{1+a^2}{1+b^2}\right)^{\frac{1}{4}} = \left(\frac{I_{cp} K_{vco}}{2\pi N C_2 b}\right)^{\frac{1}{2}} \tag{5.8}$$

Equation (5.5) describes the relationship between the two capacitors that place the zero and the third pole such that a robust phase margin is created.

The relationship of the open loop gain and phase margin is plotted in Fig.5.3 when the zero frequency, ω_z and the pole frequency, ω_p are kept at different crossover frequency ω_c. Case A in Fig.5.3 shows a phase margin of 55° with a crossover frequency of 150 kHz as a < b, case B presents a phase margin of 70° with a crossover frequency of 250 kHz as a = b, and case C illustrates a phase margin of 60° with a crossover frequency of 350 kHz as a > b. In all the three cases, we can see that the open loop gain increases with A, B and C, but the phase margin does not. Case B has the maximum phase margin of 70° when a = b. In conclusion, the open loop gain cannot be too low or too high if a reasonable phase margin is desired.

In general, loop bandwidth ω_c, phase margin Φ_M and the VCO's gain K_{VCO} are the required parameters for designing a synthesizer. We can get the value of a using equation

(5.8). The typical values for a and b are 5.5, which gives a maximum phase margin of 70° as shown in case B of Fig.5.3 (180°−110°=70°). To guarantee a sufficient phase margin for the loop stability, the crossover frequency is 250 kHz. Based on the above derivation, the other loop dynamic parameters are obtained by the following equations.

k_s in equation (5.4) can be rewritten as:

$$k_s = \omega_c \omega_p \tag{5.9}$$

Substituting k_s into equation (5.4), capacitance C_2 can be obtained:

$$C_2 = \frac{I_{cp} K_{VCO}}{2\pi N b} \tag{5.10}$$

We can get capacitance C_1 and R_1 by substituting C_2 into ω_z, ω_p.

$$C_1 = (a^2 - 1)\frac{I_{cp} K_{VCO}}{2\pi N b} \tag{5.11}$$

$$R_1 = \frac{1}{a^2 - 1} \times \frac{2\pi N b}{I_{cp} K_{VCO} \omega_z} \tag{5.12}$$

Finally, the natural frequency and damping ratio can be evaluated by [70]:

$$\omega_n = (k_s)^{1/2} = \left(\frac{I_{cp} K_{VCO}}{2\pi N C_2}\right)^{1/2} \tag{5.13}$$

$$\xi = \frac{1}{2}\omega_c \left(\frac{1}{k_s}\right)^{1/2} = \frac{1}{2}\left(\frac{2\pi N C_2}{I_{cp} K_{VCO}}\right)^{1/2} \tag{5.14}$$

5.2 Phase-Noise in CPLL Based Frequency Synthesizers

5.2.1 s–Domain Analysis

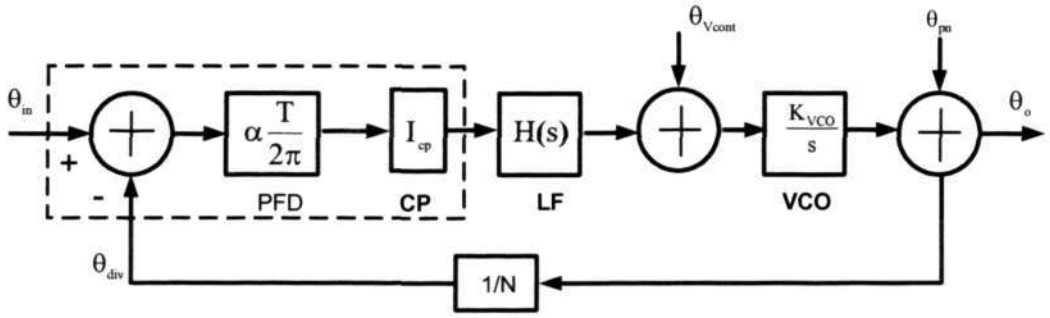


Fig. 5.4 Main noise distribution in CPLL based frequency synthesizer.

Using the linear frequency synthesizer model defined in Fig.5.2, the transfer function for different noise sources within the CPLL respect to the output can be derived. The main noise contributions in the CPLL based frequency synthesizer are indicated in Fig.5.4. θ_{in} is the input noise which includes the noise contributed by the crystal oscillator, divider θ_{div} and the noise from PFD&CP. θ_{Vcont} (the controlled voltage noise) is the noise from LF while θ_{pn} is the noise from VCO phase noise , and θ_o is the output noise of the synthesizer. When the VCO phase noise is modeled as an additive noise source after the VCO block, the closed–loop response to the VCO noise becomes [19]:

$$H_{pn}(s) = \frac{\theta_o(s)}{\theta_{pn}(s)} = \frac{1}{1+G(s)} = \frac{s^3 + \omega_p s^2}{s^3 + \omega_p s^2 + k_s s + k_s \omega_z} \tag{5.15}$$

Similarly, the closed–loop response to the reference noise is:

$$H_{in}(s) = \frac{\theta_o(s)}{\theta_{in}(s)} = \frac{NG(s)}{1+G(s)} = \frac{Nk_s(s+\omega_z)}{s^3 + \omega_p s^2 + k_s s + k_s \omega_z} \tag{5.16}$$

And the closed–loop response to the loop filter noise is:

$$H_{Vcont}(s) = \frac{\theta_o(s)}{\theta_{Vcont}(s)} = \frac{1}{1+G(s)} \times \frac{K_{vco}}{s} = \frac{K_{vco}s^2 + \omega_p K_{vco} s}{s^3 + \omega_p s^2 + k_s s + k_s \omega_z} \qquad (5.17)$$

From equation (5.15), the phase noise of the VCO is high–passed to the output of the CPLL based synthesizer. High frequency noise passes unaltered, because the feedback gain of the loop is too low to suppress the noise at these frequencies. For low frequencies, the feedback action of the loop kicks in and the noise is successfully suppressed. ω_c is the 3_dB point of this action. The VCO phase noise transfer is shown in Fig.5.5 (a). The dashed line represents a typical VCO phase noise spectrum. From Fig.5.5 (a), it is known that there are three typical noise regions. At high offset frequencies, a white phase noise floor can be distinguished. From there, the phase noise raises quadratically with the offset frequency decreases (ω^{-2}). This noise is, in fact, the white device noise that is frequency modulated around the carrier in the VCO circuit. The –20dB/dec slope originates from the fact that the frequency is the derivative of the phase [19]. Close to the carrier, frequency modulated 1/f noise determines the ω^{-3} region. The typical 1/f noise corner is not equal to the $1/f^3$ noise corner, but depends on non–linearity in the VCO. The phase noise at the PLL output is shown in Fig.5.5 (a) as the solid line.

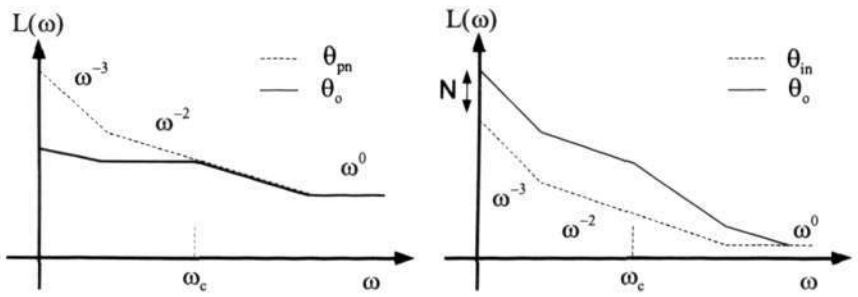


Fig. 5.5 Phase noise transfer functions in PLL based frequency synthesizer for (a) VCO's phase noise , (b) Reference (or input) noise.

The noise from the input is low–passed to the CPLL output with the same cross–over frequency, but within the CPLL and the noise is amplified by the division factor, N. The reference phase noise spectra are depicted in Fig.5.5 (b). The input noise exhibits the same three regions as the VCO's, but with a much smaller magnitude. This noise can corrupt the CPLL output phase noise, since it is amplified by N for frequencies below ω_c. Noise from the loop filter is also low–passed towards the output with a different gain from the reference noise. Therefore, the VCO phase noise dominates the phase noise performance of the CPLL. Fig.5.6 gives the phase noise contributions from three main noise sources in the whole CPLL normally.

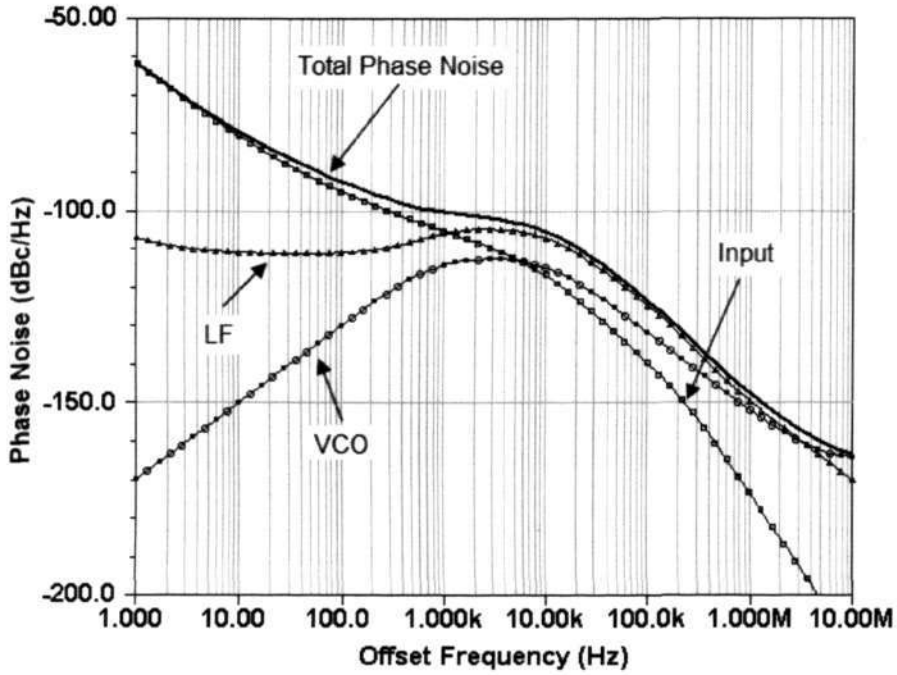


Fig. 5.6 Phase noise contributions from three main noise sources in CPLL

The majority of the above analysis for CPLLs treats the loop as a continuous–time system and using a basic s–domain model. However, due to the sampling nature of the

PFD, the error pulses generated by the PFD are too narrow to be effectively approximated for the PFD output as an impulse train. Thus, the continuous–time approximation introduces a considerable amount of error. For example, the effective phase margin of the CPLL is degraded due to the inherent sampling operation which can lead to the excessive peaking in the noise transfer function, and if one is not careful, to instability. Therefore, it is important to incorporate an impulse–invariant transformation into the CPLL model. For this reason, IC designers have been faithful in keeping the loop bandwidth of the synthesizer to the lower $1/10^{th}$ of the PFD update frequency.

5.2.2 Impulse Invariant Transformation (IIT)

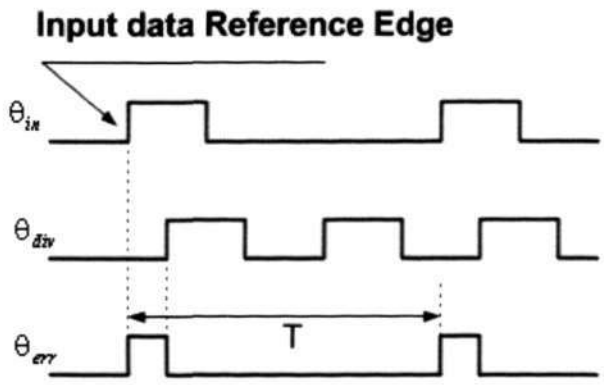


Fig. 5.7 Frequency phase detector operation in z–domain model.

It is well known that continuous time analysis (s–domain model) is a fundamental tool for analyzing the CPLL based synthesizers. However, for these CPLLs with digital inputs and outputs, classic s–domain analysis introduces a considerable amount of errors due to the sampling nature of the PFD (as mentioned in the previous paragraph).

In contrast, the discrete time analysis (the z–domain model) takes into account the sampling data nature of the data in the digital phase detector and accurately predicts the overall loop performance. Here, a transformation, termed the impulse invariant transformation exists to guarantee the exact relationship between two models, and it can be evaluated by $s = j\omega$ and $z = e^{j\omega T}$ [68], where ω is the input frequency in radian, and T is the interval time between both neighbor input data reference edges as depicted in Fig.5.7.

5.2.3 Considerations for Dead Zone of PFD & CP

A common problem associated with CPLLs is the "dead zone" in the CP. The dead zone is the amount of phase error that does not result in a charging/discharging pump current. For a three–state phase detector and CP given in Fig.5.8, the dead zone is overcome by generating small equal width UP/DN pulses when the CPLL is in phase lock. Using this sample technique, a well–designed PFD and CP combination, similar to the one presented in Fig.2.11, has a very small dead zone and hence has a negligible effect on the CPLL behavior. Therefore, we can assume a zero dead zone in this analysis. In addition to the dead zone problem, in a practical CPLL, the current sources implementing the CP suffer from various non-idealities. For example, in a MOS based implementation, the current sources suffer from the channel length modulation, which lead to a CP current that depends on the control voltage. This nonlinearity can be incorporated into the analysis by defining the CP current as a function of the control voltage for a giving channel length modulation factor. However, several circuit design techniques exist to mitigate this effect. One example of such designs uses an active loop

filter [74]. In addition, there is an inherent mismatch between the PMOS and NMOS current sources in the CP which causes the pattern phase noise. This mismatch can be reduced by using a replica biased current source [75]. To simplify the analysis, it is assumed that the effect of the nonlinearity and the current mismatch is negligible.

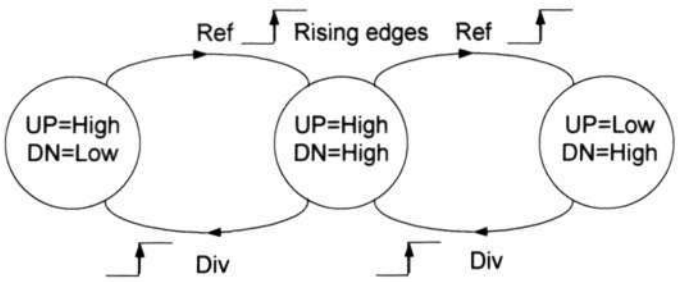


Fig. 5.8 Tri–states transition diagram of the PFD.

5.2.4 z–Domain Analysis

The impulse–invariant transformation was used to map a continuous–time analysis (s–domain model) of the PFD into its z–domain counterpart. First, the impulse response G(t), corresponding to the open loop transfer function G(s) shown in equation (5.15) is calculated by the Inverse Laplace Transform (ILT), which yields:

$$G(t) = \frac{k_s}{\omega_p^2}\left[\omega_p\omega_z t - (\omega_p - \omega_z)e^{-\omega_p t} + (\omega_p - \omega_z)\right] \tag{5.18}$$

Secondly, according to the impulse invariant transform requirement, the sampled impulse response G(nT) in equation (5.19) is obtained by sampling the open loop impulse response G(t) using a periodic impulse train from the output of the PFD. Here, n is the number of the samples and T is the effective sampling or impulse arrival rate at the PFD output shown in Fig.5.6.

$$G_d(n) = G(nT) = \frac{k_s}{\omega_p^2}\left[\omega_p\omega_z(nT) - (\omega_p - \omega_z)e^{-\omega_p(nT)} + (\omega_p - \omega_z)\right] \tag{5.19}$$

Finally, the z–domain transfer function for the open loop gain is derived by taking the z–transform of $G_d(n)$, which results in equation (5.20):

$$\begin{aligned} G(z) &= \frac{k_s T}{\omega_p^2}\left[\frac{T\omega_p\omega_z z}{(z-1)^2} + \frac{(\omega_p - \omega_z)z}{z-1} + \frac{(\omega_z - \omega_p)e^{T\omega_p}z}{e^{T\omega_p}z - 1}\right] \\ &= \frac{k_s T}{\omega_p^2}\frac{\left[T\omega_p\omega_z + (1-\alpha)(\omega_p - \omega_z)\right]z^2 - \left[T\omega_p\omega_z\alpha + (1-\alpha)(\omega_p - \omega_z)\right]z}{(z-1)^2(z-\alpha)} \\ &= k_z\frac{\left[\frac{2\pi\omega_z}{\omega_i} + (1-\alpha)(\frac{C_1}{C_1+C_2})\right]z^2 - \left[\frac{2\pi\omega_z}{\omega_i}\alpha + (1-\alpha)(\frac{C_1}{C_1+C_2})\right]z}{(z-1)^2(z-\alpha)} \end{aligned} \tag{5.20}$$

Here, $T = \frac{1}{f_{ref}} = \frac{2\pi}{\omega_i}$, $\alpha = e^{-T\omega_p}$ and $k_z = \frac{k_s T}{\omega_p} = \frac{I_{cp}\cdot K_{VCO}\cdot R_1\cdot C_1}{N\cdot(C_1+C_2)\cdot\omega_i}$

According to equation (5.15), the VCO's phase noise transfer function in the z–domain is expressed as:

$$\begin{aligned} H_{pn}(z) &= \frac{\theta_o(z)}{\theta_{pn}(z)} = \frac{1}{1+G(z)} \\ &= \frac{\left[z^3 - (\alpha+2)z^2 + (2\alpha+1)z - \alpha\right]}{z^3 + z^2\left[-\alpha - 2 + k_z(\frac{C_1(1-\alpha)}{C_1+C_2} + \frac{2\pi\omega_z}{\omega_i})\right] + z\left[2\alpha + 1 + k_z(\frac{C_1(1-\alpha)}{C_1+C_2} + \frac{2\pi\omega_z}{\omega_i})\right] - \alpha} \end{aligned} \tag{5.21}$$

Similarly, we have the reference transfer function and the loop filter transfer function in the z–domain as:

$$H_{in}(z)=\frac{\theta_o(z)}{\theta_{in}(z)}=\frac{NG(z)}{1+G(z)}$$

$$=\frac{Nk_z\left[z^2\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z}{\omega_i}\right)-z\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z\alpha}{\omega_i}\right)\right]}{z^3+z^2\left[-\alpha-2+k_z\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z}{\omega_i}\right)\right]+z\left[2\alpha+1-k_z\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z\alpha}{\omega_i}\right)\right]-\alpha} \quad (5.22)$$

$$H_{Vcont}(z)=\frac{\theta_o(z)}{\theta_{Vcont}(z)}=\frac{1}{1+G(z)}\times\frac{K_{VCO}}{s}$$

$$=\frac{\left[z^3-(\alpha+2)z^2+(2\alpha+1)z-\alpha\right]\frac{K_{VCO}}{s}}{z^3+z^2\left[-\alpha-2+k_z\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z}{\omega_i}\right)\right]+z\left[2\alpha+1+k_z\left(\frac{C_1(1-\alpha)}{C_1+C_2}+\frac{2\pi\omega_z}{\omega_i}\right)\right]-\alpha} \quad (5.23)$$

5.2.5 Noise Behavioral Simulation by s–Domian Model and z–Domain Model

Synthesizer behavioral simulations are carried out to analyze and verify the results derived above. The synthesizer is designed with an input frequency of 5 MHz (update rate of the PFD), a loop phase margin of 60°, a VCO gain of 60 MHz/V, a charge pump current of 100 μA and a division ratio N of 424. Four different loop bandwidths (1 MHz, 500 kHz, 333 kHz and 250 kHz) are used to analyze the noise of the system. For simplicity, we use the ratio $\eta=\frac{\omega_{in}}{\omega_c}$ based on the input frequency ω_{in} and the crossover frequency ω_c. The corresponding loop dynamic parameters are obtained by the design methodology presented in section 5.1.3. The Bode plot of the open loop gain with the loop bandwidth of 250 kHz is given as case B in Fig.5.3. The simulations for the noise transfer functions in both the s–domain analysis and z–domain analysis are carried out and compared with the results from MatLab. The input noise transfer functions modeled by the s–domain and z–domain for different η are plotted in Fig.5.9.

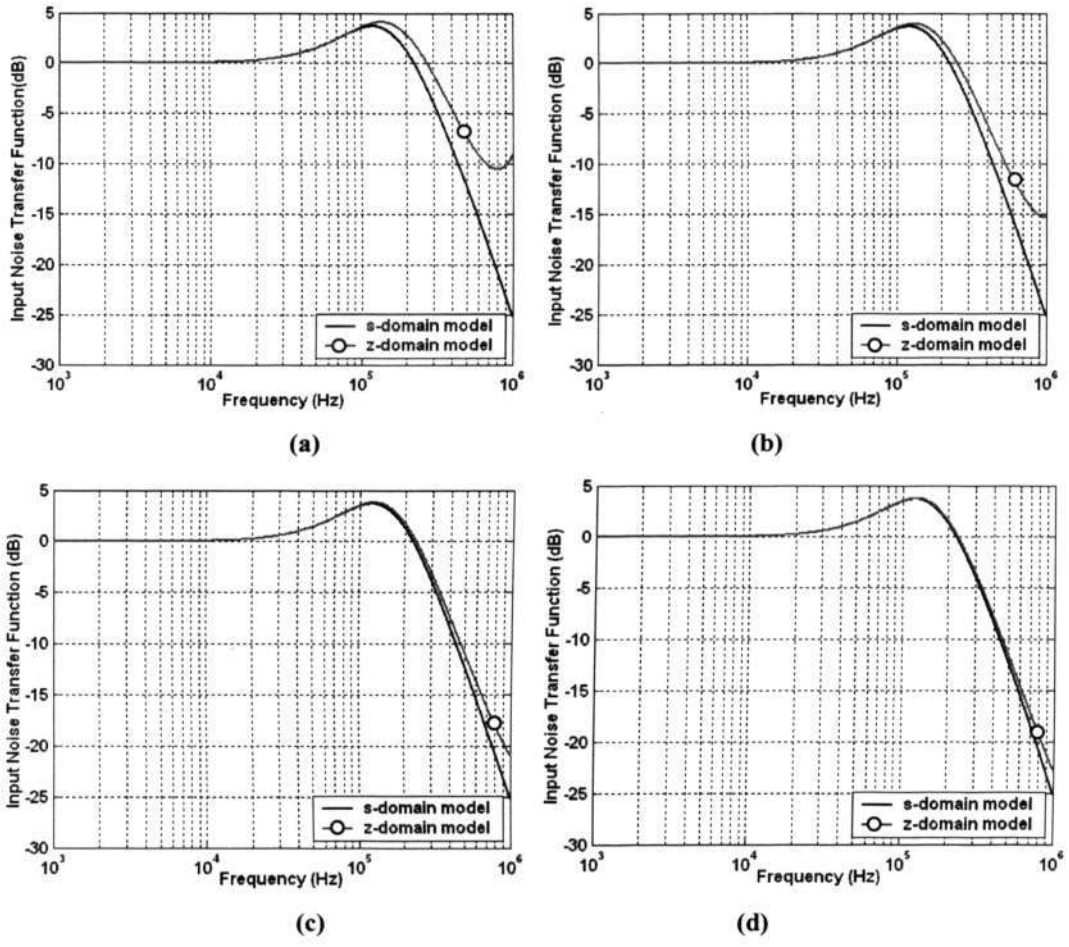


Fig. 5.9 Noise transfers function $\frac{\theta_o}{\theta_{in}}$ of the input (reference frequency) in s–domain and z–domain.
(a) $\eta = 5$, **(b)** $\eta = 10$, **(c)** $\eta = 15$ **and (d)** $\eta = 20$.

We note that a peak exists in the z–domain transfer function compared with the s–domain model when the ratio η is smaller, depicted in Fig.5.9 (a), in which the loop bandwidth of the system is so wide that it is comparable with the reference frequency. The results from the z–domain model are much closer to those from the s–domain model when the ratio η increases. Specifically, the s–domain model matches the z–domain model very well when η increases to 20, as depicted in Fig.5.9 (d). However, this means that the system loop has a narrow loop bandwidth. Based on the above analysis, it is

obvious that a noise peak from the inherent sampling behavior exists in the system when η is smaller. This conclusion means that this noise peak cannot be rejected by a relatively wide loop filter for a system with wide loop bandwidth. However, the s–domain analysis cannot explain the noise peak because it includes an assumption concerning the ability of the loop filters to reject high frequency noise from the PFD [68]. Hence, the z–domain model is more accurate than the s–domain model for the systems with the wide loop bandwidths, although both models can accurately analyze the systems with the narrow loop bandwidth systems.

Fig.5.10 shows the simulation result from the transfer function of the VCO's phase noise $\frac{\theta_0}{\theta_{pn}}$ in the s–domain and the z–domain with the ratios being $\eta = 5$ in Fig.5.10 (a) and $\eta = 20$ in Fig.5.10 (d). We also can see that the z–domain model predicts the noise performance accurately when the loop bandwidth of the system is wider due to the same reason. Similarly, the results from the noise transfer function $\frac{\theta_0}{\theta_{Vcont}}$ of the loop filter (also the control voltage of the VCO) are shown in Fig.5.11 for the two different ratios: $\eta = 5$ in Fig.5.11 (a) and $\eta = 20$ in Fig.5.11 (b). Note that the peaking of the noise due to the inherent sampling behavior (ratio η) is not predicted by s–domain model whereas it is accurately predicted by the z–domain model for the wide bandwidth loop system. This noise peak is proportional to the loop delay around the feedback. Hence, it becomes worse at lower sampling rates or low values of η. Due to the same reason, both s–domain and z–domain analyses accurately model the real system under the high sampling conditions (i.e., high η value).

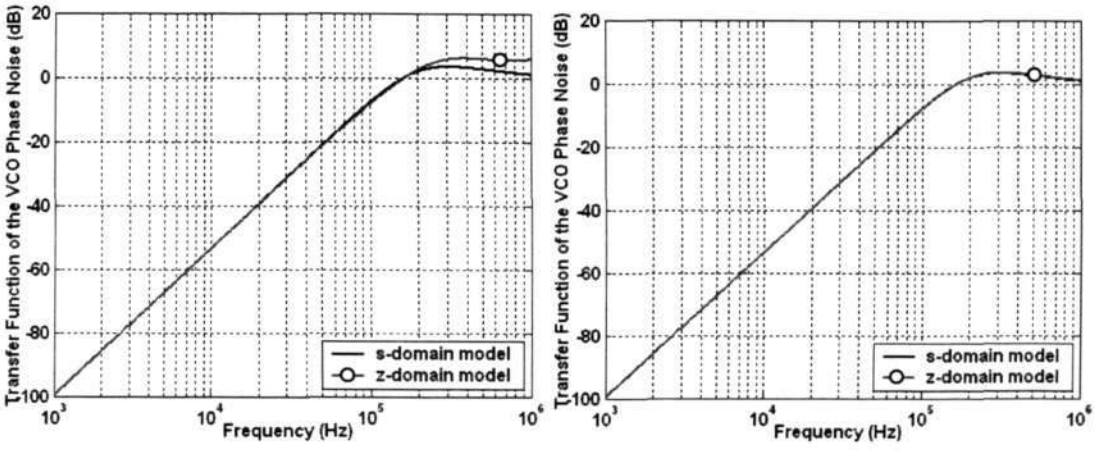


Fig. 5.10 Transfer function $\frac{\theta_o}{\theta_{pn}}$ of the phase noise from VCO (a) $\eta = 5$, (b) $\eta = 20$.

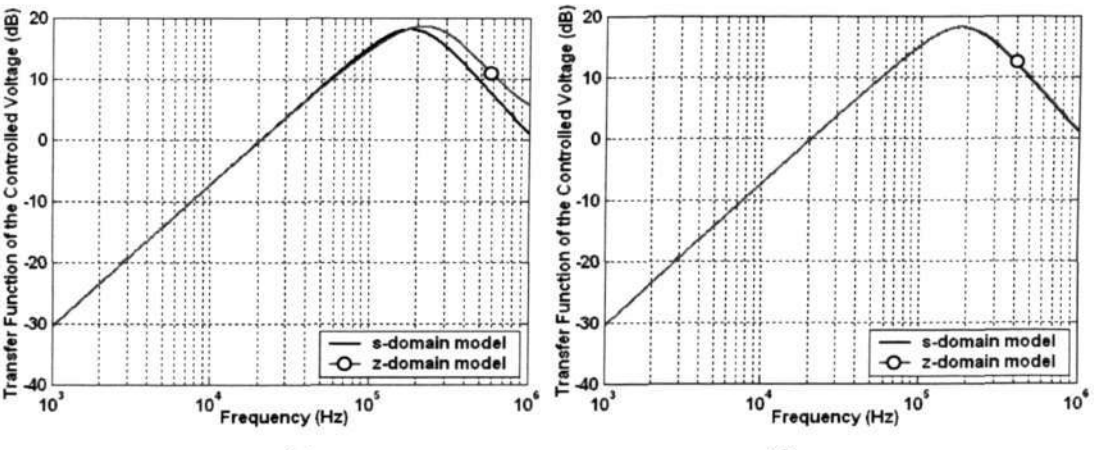


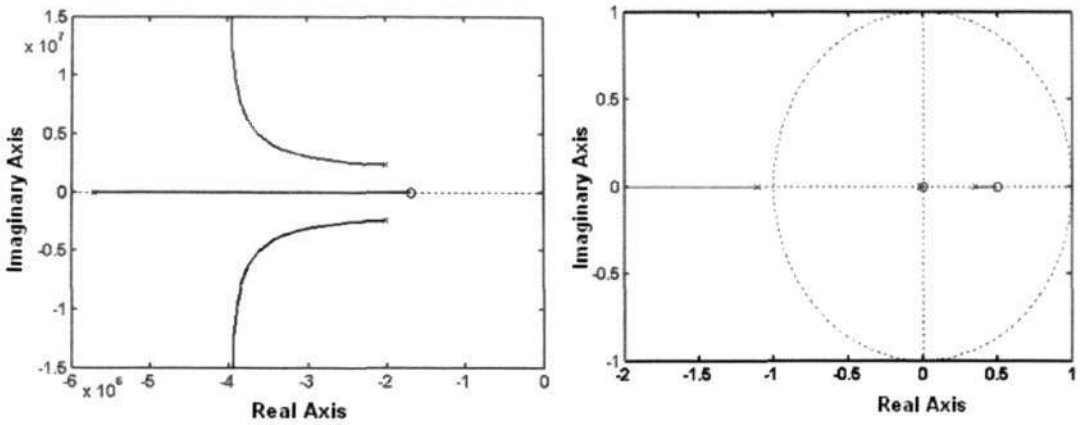
Fig. 5.11 Noise transfer function $\frac{\theta_o}{\theta_{Vcont}}$ from loop filter (a) $\eta = 5$, (b) $\eta = 20$.

5.3 Stability of the Frequency Synthesizer

The stability of the synthesizer depends on the loop gain, the phase margin and the reference frequency. Because the analysis of the s–domain model is accurate for a narrow bandwidth system, the system instability caused by an inadequate phase margin is accurately predicted by the s–domain model. However, when the loop bandwidth is increased to be comparable with the reference frequency, the continuous–time analysis

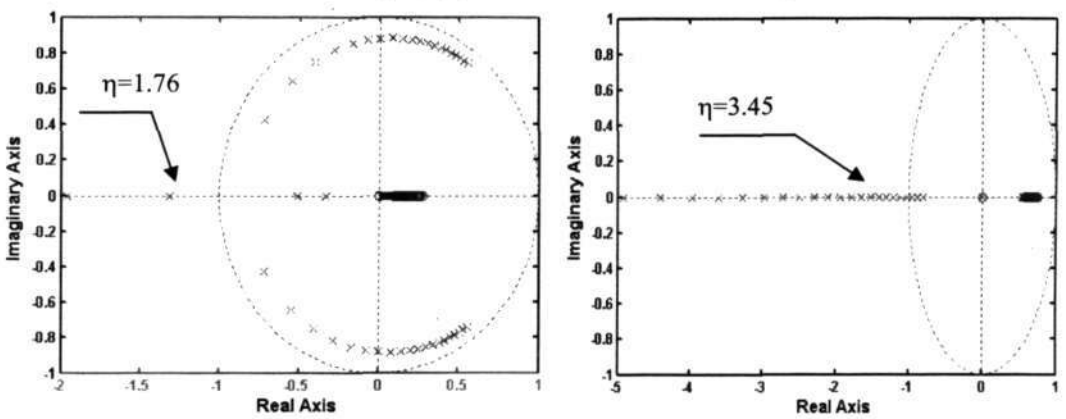
(the s–domain model) is unable to predict the instability accurately any more. Instead, discrete–time analysis (the z–domain model) is required to explain such instability, which is caused by the excessive phase shift introduced by delay around the feedback loop.

This phenomenon can also be explained mathematically using root locus analysis. Here, the stability of the loop in the z–domain is manifested as the synthesizer being stable if the poles of the closed loop's transfer function are all inside the unit circle in the z–plane. Conversely, the system is unstable if any one of the poles is outside the unit circle [76]. The root locus in s–domain analysis (s–plane) and z–domain analysis (z–plane) are presented in Fig.5.12. In Fig.5.12 (a), the root locus is in the s–plane for the closed loop system. When the ratio η is equal to 3.1, three poles and one zero are all in the left part of the root locus, and according to the stability thumb of s–domain analysis, the system is stable. However, the system is predicted to be unstable by the stability thumb of z–domain analysis, as depicted in Fig.5.12 (b), when one of the poles of the closed loop is at outside the unit circle in z root locus plane. To conclude, a stability limit of the system with different phase margin is necessary and can be predicted accurately in the z–domain model.



(a) (b)

Fig. 5.12 Root Locus of the closed loop gain as η=3.1 and phase margin 45° (a) Root locus in s domain analysis, (b) Root locus in z domain analysis.



(a) (b)

Fig. 5.13 Poles and zeros of the close loop synthesizer with the increase of η from 1.6 to 3.7 (a) $\eta = 1.74$ as the phase margin is 10°, (b) $\eta = 3.45$ as the phase margin is 70°.

The stability limit of the synthesizer is extracted by plotting the root locus in the z–plane for the closed loop transfer function. The ratio η is increased from 1.6 to 3.7 in the steps of 0.1 where the phase margin ranges from 10° to 70°, augmented in steps of 10°. Fig.5.13 shows the limit $\eta = 1.74$ when the phase margin is equal to 10° and $\eta = 3.45$ when the phase margin is 70° in the z root locus plane.

Note that the system becomes unstable depending on the ratio η and phase margin mainly, with the stability limit for η being different for the different phase margins.

Fig.5.14 describes the relationship of the stability limit η with the phase margin $\Phi_{M\max}$. This observation is also further verified by using the transient simulations of RFHDL. A synthesizer with a phase margin of 45° is used to verify the limit of $\eta \approx 3.25$ obtained by Fig.5.14, meaning that the system is unstable when $\eta \leq 3.25$. Synthesizers with different ratios ($\eta = 3.1$ and $\eta = 3.3$) of the reference frequency and loop bandwidth are simulated in the transient analysis by RFHDL with the phase margin of 45° kept constant. The results are shown in Fig.5.15 (a) and Fig.5.15 (b) respectively. It can be seen that the loop is stable when the ratio of the reference frequency (update rate of PFD) to the loop bandwidth is 3.3, and the settling time is less than 6 μs while it is unstable when the ratio is equal to 3.1. Fig.5.16 gives the transition response for different η when the phase margin is 70°. Therefore, the system's instability is due to the low sampling rate itself. The stability limitation of a synthesizer is mainly dependent on the ratio η and the phase margin $\Phi_{M,\max}$ but independent of the loop parameters for a given ratio η.

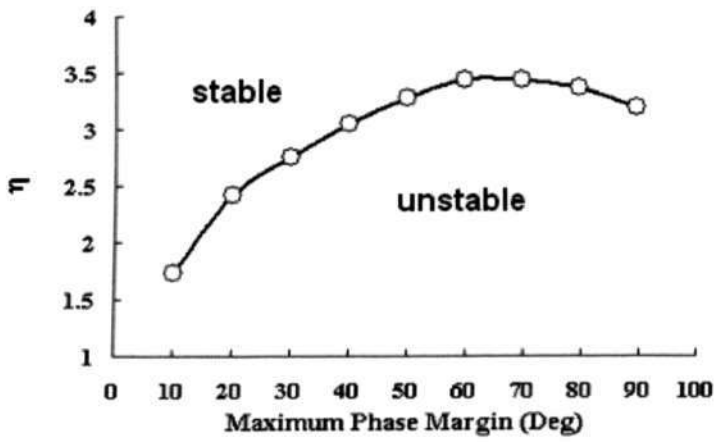


Fig. 5.14 Stability limitations versus phase margin.

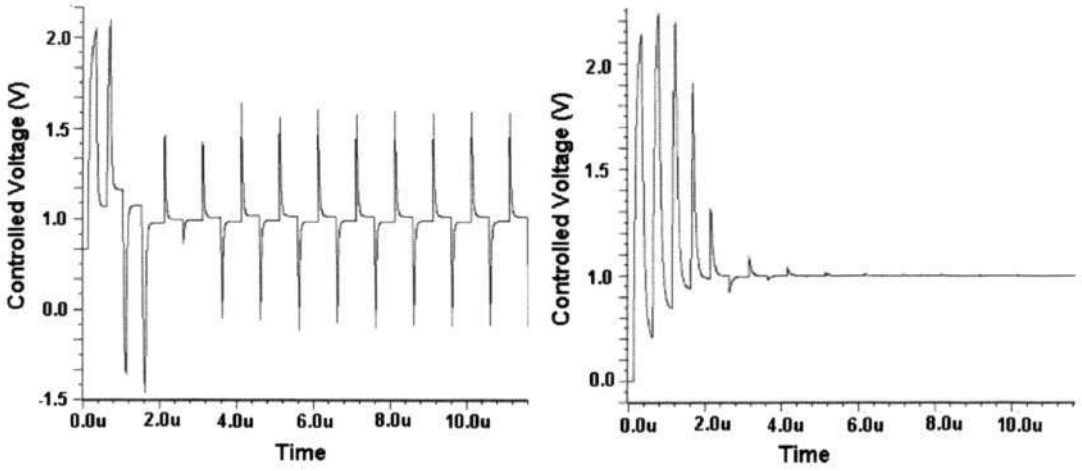


Fig. 5.15 Transient simulation for the synthesizer with the phase margin of 45° and different η, (a) System is unstable when $\eta = 3.1$, (b) System is stable when $\eta = 3.3$.

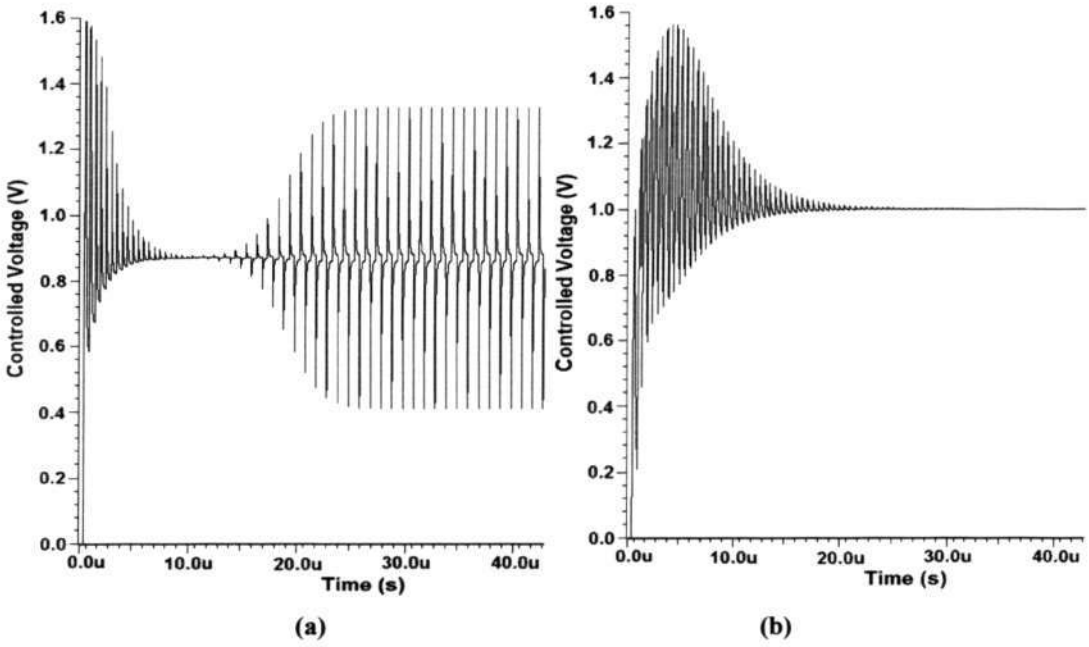


Fig. 5.16 Transient simulation for the synthesizer with the phase margin of 70° and different η, (a) System is unstable when $\eta = 3.3$, (b) System is stable when $\eta = 3.5$.

5.4 Conclusion

A method to optimize the loop parameters for the third order loop filter and extended the z–domain model of the second order loop filter to the third order has been proposed.

Based on the noise distribution model in the synthesizer, three noise transfer functions in z–domain, namely, the input noise transfer functions, the noise transfer function from the loop filter and the noise transfer function from the VCO phase noise, are derived and simulated in the behavioral model. A noise peak exists in the loop and the loop filter has no ability to suppress it when the loop bandwidth is comparable with the reference frequency. The noise peak also causes the system to be unstable, and this can be detected by the z–domain analysis only. The stability margin, which is dependent on the phase margin and the ratio of the reference frequency to the loop bandwidth, has been analyzed and verified by the behavioral model of RFHDL in Cadence. The proposed approach provides a useful insight into the investigations to derive the phase noise transfer functions.

CHAPTER 6

Design and Implementation of the Frequency Synthesizer for Bluetooth Application

The Bluetooth standard specifies 2.4 GHz frequency–hopped spread–spectrum system that enables the users to easily connect to a wide range of computing and telecommunication devices without the need for wires or cabling of any kind. The devices include mobile computers, mobile phones, portable handheld devices, and connectivity to the internet [7]. The transceiver for Bluetooth consists of low–noise amplifiers, power amplifiers, mixers, DSP chips, filters, and frequency synthesizers. These building blocks have been realized using hybrid technologies and require interfacing circuits. However, these circuits increase the power consumption and limit the maximum operating speed of the transceivers. For this reason, it has become increasingly attractive to integrate all these building blocks on a single chip.

Designing fully integrated frequency synthesizers for this integration is as always, desirable but most challenging. The first requirement is to achieve the high frequency operation within the reasonable levels of the power consumption. Two more critical requirements concern the phase noise and spurious–level performance. Fourth, for monolithic system integration, a small chip area is essential.

In this chapter, we design and implement one such monolithic frequency synthesizer in a 0.18 μm CMOS process for the Bluetooth application. The good performances with a high operation frequency from 2.400 GHz to 2.4835 GHz, low power consumption of 31

mW, low phase noise of −112 dBc at 3 MHz offset frequency, a low spurious level of −68.0 dBc at 1 MHz, and fast switching time 22 μs are achieved. The building blocks of the proposed frequency synthesizer are discussed and the optimization methods for each block are presented.

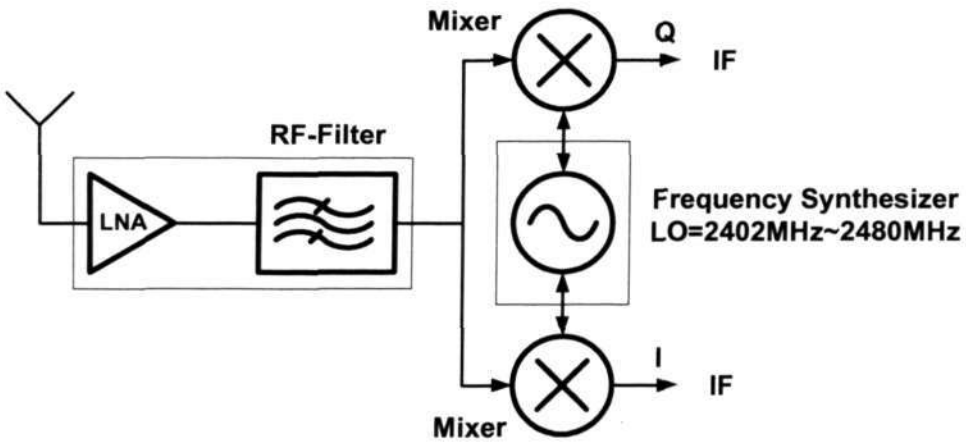


Fig. 6.1 Block diagram of the front–end of the Bluetooth receiver.

6.1 Design Specification

6.1.1 Output Frequency

The Bluetooth system operates in the unlicensed 2.4 GHz ISM (Industrial Scientific Medicine) band [7]. To receive signals in different channels, a front–end of the Bluetooth receiver, shown in Fig.6.1, is adopted. The receiver front–end consists of a low noise amplifier (LNA), an RF filter for filtering out–of–band noise and blocking signals, two mixers for mixing down the received signal to an IF frequency (f_{IF}) for base–band signal processing and a frequency synthesizer for generating a stable LO frequency. To extract

information from the desired channel, the local oscillator (LO) output frequency ($f_{channel}$) of the frequency synthesizer is changed accordingly, as follows:

$$f_{channel} = [2402 + (k-1)\cdot 1] \quad \text{MHz} \tag{6.1}$$

where k=1,2,3,…,79 are the channel numbers and the output frequency range of the frequency synthesizer to be achieved is 2402–2480 MHz, while the frequencies for lower and upper guard band are 2 MHz and 3.5 MHz respectively shown as in Fig.6.2. The modulation scheme in place is the Guassian Frequency Shift Keying (GFSK), with frequency deviations of ± 160 kHz around the carrier.

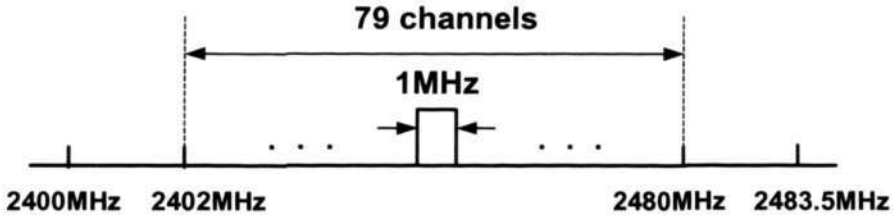


Fig. 6.2 Frequency allocation in the Bluetooth system.

6.1.2 Phase Noise

The desired signal power can be as low as –67 dBm. At 3 MHz offset frequency, the power of the blocking signal can be as high as –27 dBm [7]. Depending on the correct LO frequency, the desired channel signal is downconverted to IF frequency. However, blocking signals are also downconverted with the LO signal and its phase noise. Since the power of the blocking signal is much larger than that of the desired signal, the phase noise power falls into the IF frequency and degrades the signal to noise ratio (SNR). The phase noise specification $L_{spec}(\Delta\omega)$ can be expressed as [35]:

$$L_{spec}(\Delta\omega) < S_{desired} - S_{blocking} - SNR_{spec} - 10\log(BW_{channel}) = -111\,\text{dBc/Hz} \quad (6.2)$$

where SNR_{spec} of 11 dB is SNR specification for the whole receiver [7], $S_{desired} = -67$ dBm is the power level of the minimum desired signal, and $S_{blocking} = -27$ dBm is the power level of the maximum blocking signal. Assuming the phase noise follows $\frac{1}{f^2}$ behavior, the phase noise specifications at the offset frequency of 1 MHz and 2 MHz are −71 dBc/Hz and −101 dBc/Hz respectively. In our design, we adopt the phase noise specifications at the offset frequency of 3 MHz because of the toughest one to meet.

6.1.3 Spurious Tones

Because of the feed-through and modulation of the reference signal, two spurious tones appear at the $\pm f_m$ ($f_m = \omega_m / 2\pi$) away from the desired output frequency, as shown in Fig.2.3. The derivation of the spurious tone specification is similar to that of the phase noise except that the channel bandwidth is not considered in this case. The spurious tone specification S_{spec} can be expressed as equation (6.3) for the offset frequency of 1 MHz [7]:

$$S_{spec} < S_{desired} - S_{blocking} - SNR_{spec} = -51 \quad \text{dBc} \quad (6.3)$$

6.1.4 Switching Time

Bluetooth adopts a frequency hopping scheme. A frequency hop transceiver is applied to combat interference and fading. A shaped, binary FM modulation is applied to

minimize transceiver complexity. The symbol rate is 1 Ms/s and the nominal hop rate is 1600 hops/s.

A slotted channel as shown in Fig.6.3 is applied with a nominal slot length of 625 μs. The slot numberings range from 0 to 2^{27-1} and is cyclic with a cycle length of 2^{27}. For full Duplex transmission, a time–division duplex (TDD) scheme is used. The information is exchanged through packets on the channel, and each packet is transmitted on a different hop frequency. The packet nominally covers a single slot, but can be extended to cover up to five slots.

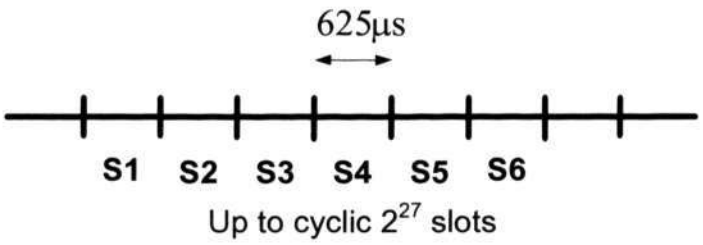


Fig. 6.3 Bluetooth receiver time.

The minimum setting time or switching time is limited by the time taken to switch from the first channel to another channel in the frequency domain. In this case, the settling time requirement of the frequency synthesizer is one–tenth of the frequency hop time. The nominal hop rate is 1600 hops/s, implying that the settling time has to be smaller than 62.5 μs ($1600^{-1} \times 10^{-1}$).

6.2 Architecture and Implementation of Frequency Synthesizer

A 2.45 GHz CMOS frequency synthesizer targeting Bluetooth applications is presented for the demonstration of the RF frequency synthesizer design in this section. The architecture and building blocks of the frequency synthesizer are shown in Fig.5.1.

The forward loop consists with phase/frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO). The feedback loop consists of an integer – pulse swallow frequency divider (PSFD) N whose modulus division ration is $N = M \times P + S$. The reference frequency of 1 MHz is the same as the channel space. Therefore the output frequency of the synthesizer is $f_{out} = N \times 1$ MHz . The loop bandwidth is optimized as 100 kHz ($1/10^{th}$ of the reference frequency).

6.2.1 Voltage Controlled Oscillator

The voltage controlled oscillator, which generates a high frequency sine wave at the output of the frequency synthesizer. The design requirements of the VCO are as follows:

- It should cover the output frequency range from 2.400 GHz to 2.4835 GHz.
- It should satisfy the phase noise performance of −111 dBc/Hz at the offset frequency of 3 MHz with minimum power consumption.
- It should generate output signals with a single–end amplitude larger than 0.5 V to drive the frequency divider N.

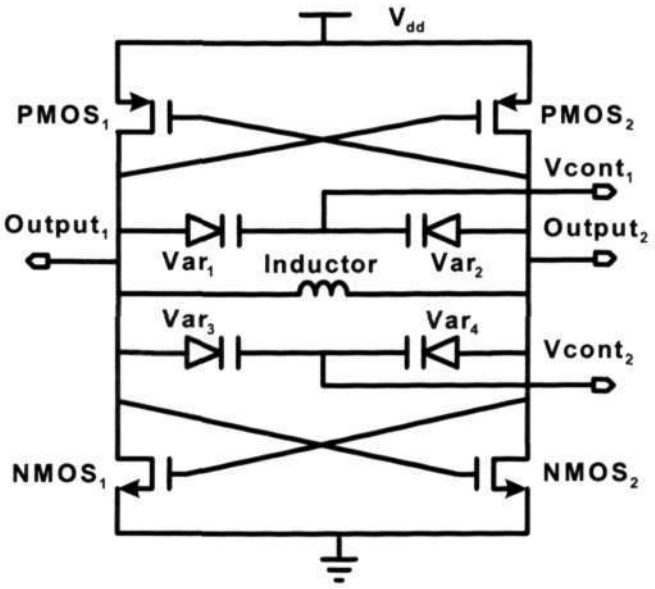


Fig. 6.4 Complementary cross–coupled LC VCO.

To achieve the above requirements, a complementary cross-coupled LC VCO as shown in Fig.6.4 is implemented as being discussed in Chapter 4. The planar inductors are made up of top two layers of metal in order to decrease the series resistance, enhance the inductance, and reduce the chip area. Although the overall quality factor Q of the LC tank is dominated by the Q of the inductor, the varactors still need to have a high Q value to avoid further degradation of the LC tank quality factor [77]. The accumulation–mode varactors are used to offer a better than average Q factor over different biasing conditions with a larger tunable capacitance as compared to conventional p–n junction variactors [78]. Therefore the LC tank consists of on–chip 1.92 nH spiral inductors with a quality factor of 8 as illustrated in Fig.6.5 and two pairs Accumulation-Mode MOS (A-MOS) varactors, in which one pair 1 pF varactors with quality factor of 40 at 2.45 GHz is used to tune slightly, and another pair varactors of 2 pF and quality factor of 30 at 2.45 GHz is used to tune coarsely as illustrated in Fig.6.6. The complementary cross–coupled NMOS

and PMOS pairs serve as the negative resistor for oscillation start–up. These are optimized by the solution proposal in Chapter 3 and traded off with the minimal power consumption. For information on the operation theory of the complementary cross–coupled LC VCO, see Chapter 3.

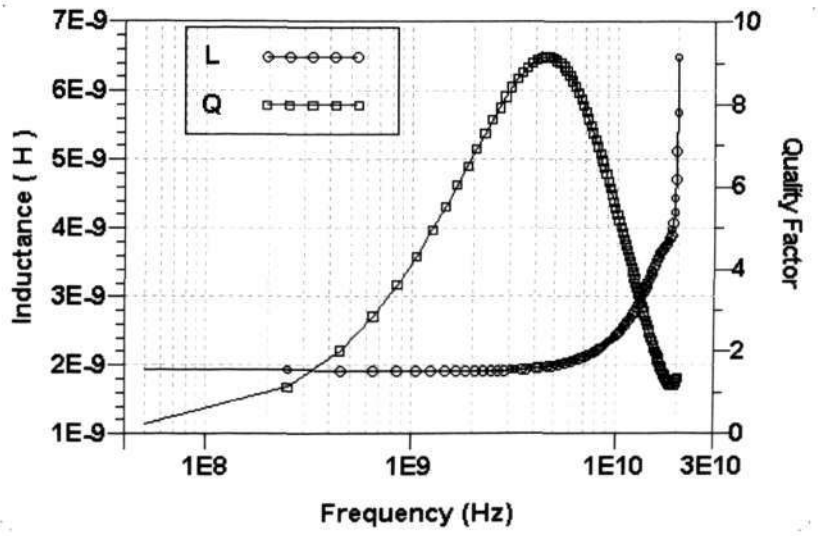


Fig. 6.5 Inductance and Q factor of the inductor adopted in the design.

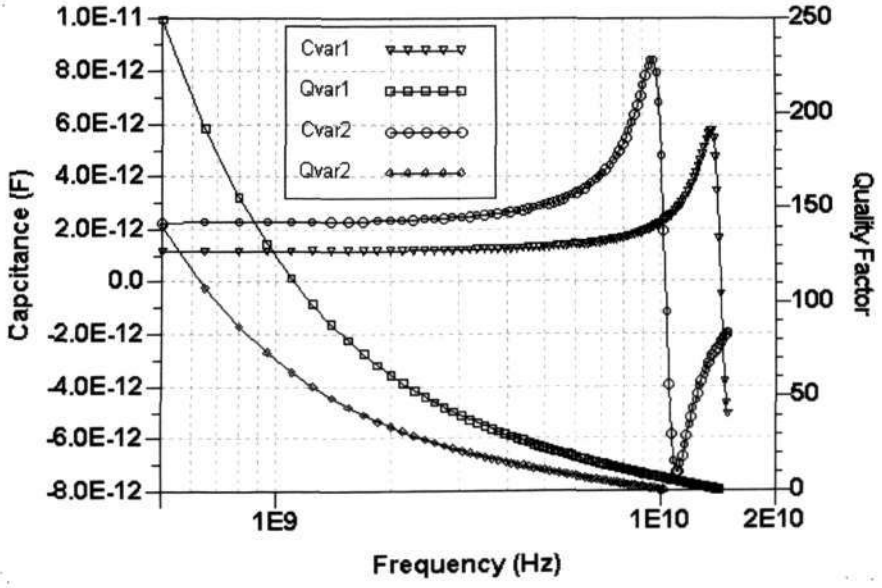


Fig. 6.6 Capacitance and Q factor of the varactors adopted in the design.

The LC VCO is simulated by SprectreRF [79] and the simulation results for the VCO performance are shown in Fig.6.7 and Fig.6.8. The oscillating frequency f_0 is tuning from 2.38 GHz to 2.52 GHz given in Fig.6.7 (a). For Bluetooth application, this covers all channel frequencies from 2.40 GHz to 2.835 GHz. The VCO gain K_{VCO} of 60 MHz/V shown in Fig.6.7 (b) is utilized in the design to make the ripple of controlled voltage as low as possible. The peak–to–peak output amplitude V_{pp} is around 1.35 V as plotted in Fig.6.8 (b), and this is satisfied with the amplitude requirement for the divider set above as 1 V. Spectre-RF [79] is used to perform the periodic–steady–state (PSS) function for the analysis of the phase noise performance as shown in Fig.6.9. The optimization phase noise simulation results of the LC oscillator versus the controlled voltage are shown in Fig.6.8 (a). We note that the low phase noise performance is around −117 dBc/Hz at offset frequency 600 kHz away from the center frequency of 2.45 GHz, −122 dBc/Hz at an offset frequency of 1 MHz and −135 dBc/Hz at offset frequency of 3 MHz. Those performances meet the mark and indeed produce the expected results. The minimal power consumption is smaller than 12 mW as depicted in Fig.6.8 (b).

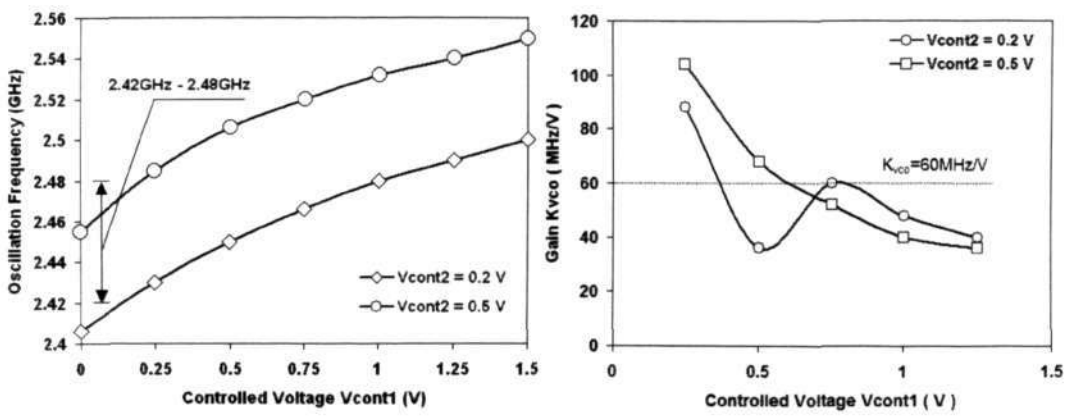
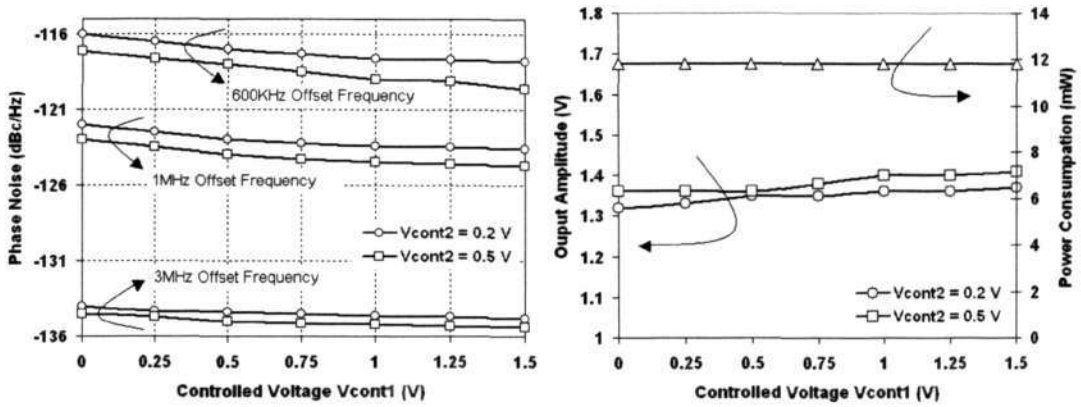


Fig. 6.7 Simulated tuning range of the proposal LC VCO, (b) Gain of the LC VCO.



(a) (b)

Fig. 6.8 (a) Simulated phase noise of the proposal LC VCO, (b) Power consumption and peak–to–peak amplitude of the LC VCO.

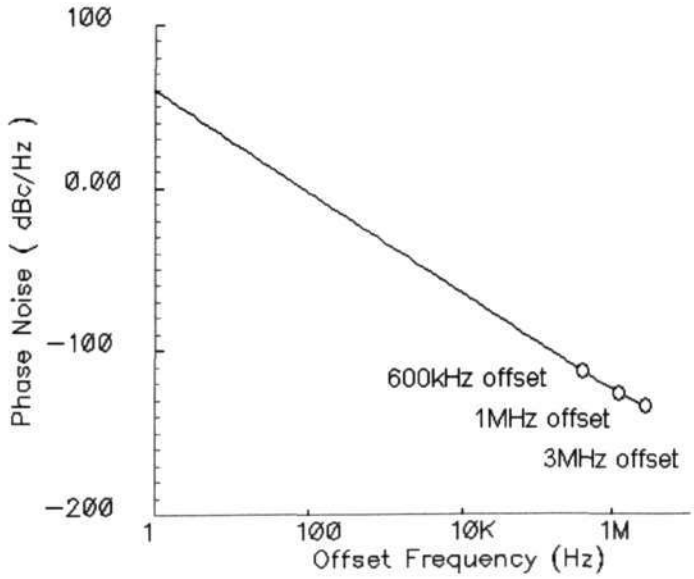


Fig. 6.9 Phase noise simulation results of the LC VCO with 2.45 GHz.

6.2.2 Pulse Swallow Frequency Divider N

In the feedback path of the frequency synthesizer loop, a programmable pulse swallow frequency divider N is utilized for channel selection as shown in Fig.5.4. The design requirements of the divider N are summary as follows:

- Operate at the frequencies up to 2.48 GHz.
- Frequency division ratio N is various between 2402 and 2480.
- Full swing output with rise and fall times of less than 10 percent of the output period.

6.2.2.1 Circuit Implementation

The programmable frequency divider shown in Fig.6.10 consists of a dual–modulus M/M+1 prescaler, a program counter (P counter) and a swallow counter (S counter) [30] [80]. The M/M+1 prescaler divide the input signal by either M or M+1. The P counter, which is itself a programmable frequency divider, divides the precaler output by P. The S counter counts the prescaler output by S.

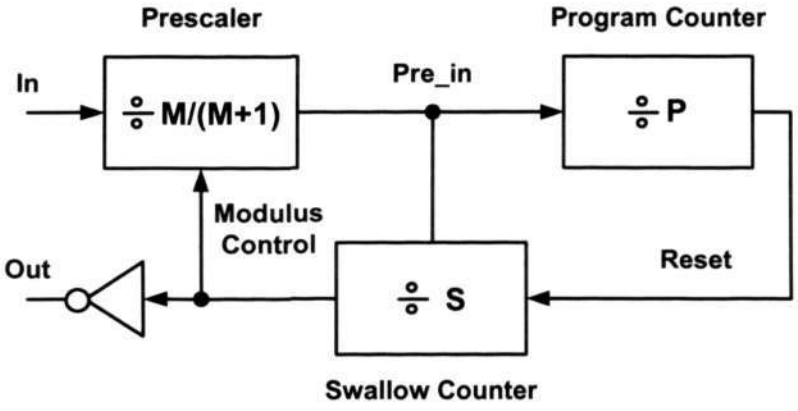


Fig. 6.10 Implementation of the pulses swallow programmable divider M.

When the programmable divider begins from the reset state, the prescaler divides the input signal by M+1. The prescaler output is counted by both the P and S counters. When the S counter has counted S pulses (equivalent to (M+1)S input cycles), the S counter changes the state of the modulus control line mode and the prescaler divides the input by

M. Since the P counter has already sensed S pulses, it counts the remaining (P–S) cycles, corresponding to (P–S)M pulses at the main input, to reach the overflow. Finally, the programmable divider generates one complete cycle for every $(M+1)S+(P-S)M = PM+S$ input cycles. The operation repeats after the S counter is reset.

6.2.2.2 Design Optimization

As the frequency division ration (between 2402 and 2480) can be achieved with the different combinations of M, S, and P, different combinations have their own effect on the frequency divider performance. Therefore, the system design optimization should be done before the design optimization in the transistor level. In this programmable divider design, the minimum power consumption is the top priority. The system design guidelines are given as:

- The division ratio P counter must be larger than that of the S counter.
- The operating frequency and number of bits for both the P and S counters should be minimized.

The prescaler divides by M+1 in the first S cycles and M in the remaining P–S cycles. If S is larger than P, the S counter will be reset before it completes its counting and the divider will not be able to function properly. Therefore, the P counter must be larger than S counter. In general, a programmable counter consumes more power than a non–programmable one. Hence, the operating frequency and complexity of both P and S counters should be minimized. Based on the above analysis, an optimization combination of P, S, and M shown in Table 6.1 is used in the design, to covers all desired Bluetooth channel frequencies.

Table 6.1 Summary of the integrator–N frequency synthesizers.

Frequency f_{out} (MHz)	Division ratio N	M	P	S
2402 ~ 2431	2402 ~ 2431	32	75	2 ~ 31
2432 ~ 2463	2432 ~ 2463	32	76	0 ~ 31
2464 ~ 2482	2464 ~ 2482	32	77	0 ~ 17

6.2.2.3 Dual–Modulus Prescaler

1) Operation

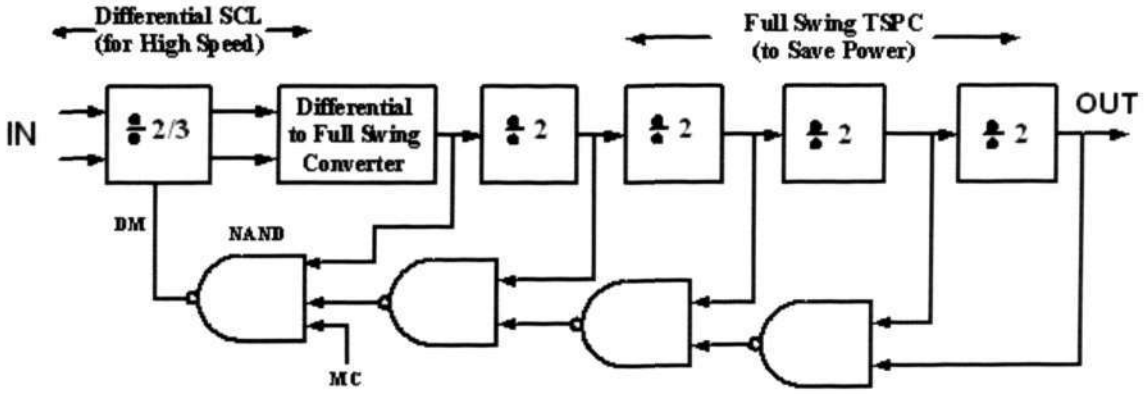


Fig. 6.11 Diagram of the prescaler.

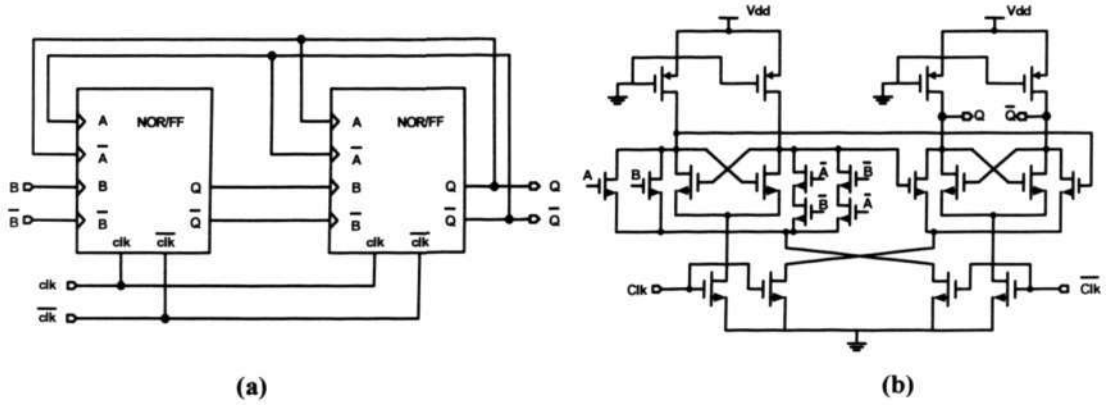
A conventional prescaler is designed by cascading dual–modulus frequency dividers and fixed frequency dividers in order to get the desired division ration. Each dual–modulus frequency divider such as divide–by–2/3 divider generally burns more than twice the power of a fixed divider such as divide–by–2 divider. Therefore, to minimize the power consumption of the prescaler in our design, a dual modulus divider that divide–by–2/3 is combined with differential to full swing converter and four fixed full swing true single phase clock (TSPC) divide–by–2 dividers is shown in Fig.6.11. M then becomes an integer power of two (e.g. $M = 2^5 = 32$). A dual modulus prescaler of that divide–by–32/33 is thus achieved and the modulus control (MC) input selects

between divide–by–32 and divide–by–33. To divide by 32, MC is set to zero and the dual modulus divider divides by 2. When MC=1, the dual–modulus divider divides by 3 only once per output cycle, and therefore, the overall division ratio is 33.

2) High Speed Dual Modulus Divider (divide–by–2/3)

The block diagram of the dual–modulus used in this work (divide–by–2/3) is given in Fig.6.12 (a). Two NOR/flip–flops as shown in Fig.6.12 (b) are cascaded to make up the dual–modulus divide–by–2/3 circuit. When B is set to zero, the dual–modulus divider divides by 2, or by 3. The differential NOR gate is combined at the input of the flip–flop to degrade the power consumption of the divider.

The NOR/flip–flop of the dual–modulus divider is implemented for the following reasons: 1) It operates at high speeds, 2) It is the fully differential and symmetric with respect to both NOR inputs, 3) The power consumption is reduced because the current at each NOR gate is shared with the following flip–flop.



(a) (b)

Fig. 6.12 (a) Block diagram of the prescaler, (b) Schematic of the NOR/flipflop(NOR/FF) of the dual modulus divider

3) Fixed Divide-by-2 Dividers

There are two standard models for divider-by-2 divider. One is that two differential master–slaves current model logical (CML) D flip–flops (DFF) are cascaded to realize the function of the fixed CML divide–by–2 divider as shown in Fig.6.13 (a). The operation of a CML D latch, i.e. the master latch as shown in Fig.6.13 (b), is as follows: If the clock is logically high, the input signal D and $\overline{D}$ are passed to the output with a time constant of RC similar to the case of the MOS Current Mode Logic inverter. When the clock (clk) changes from a logic high to a logic low, the cross–coupled M5 and M6 transistors generate a negative conductance and latch the output.

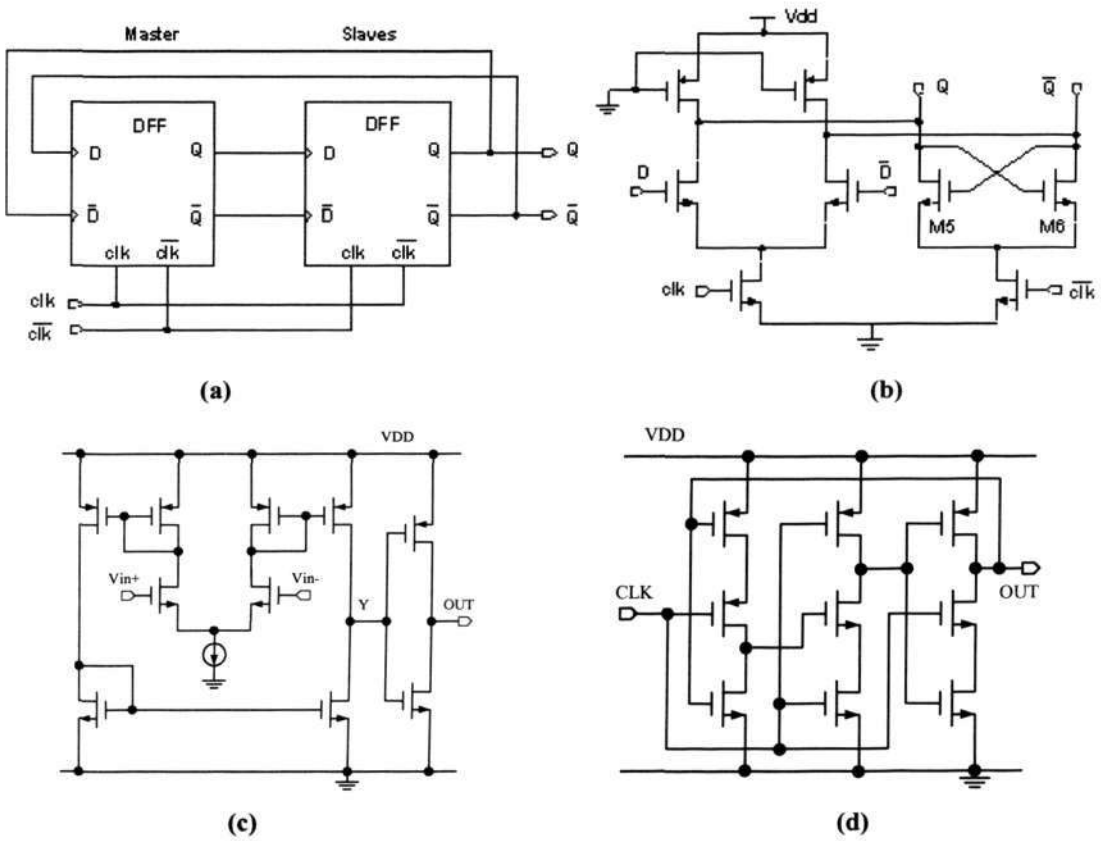


Fig. 6.13 (a) Block diagram of the fixed CML divide–by–2 divider, (d) Schematic of the DFF, (c) Differential to full swing converter, (d) TSPC Divide-by-2 Divider.

The other one is true signal phase clock (TSPC) single end divider. The inversion output is connected to the input of the circuit, a divide-by-2 circuit is formed as shown in Fig.6.13 (d). The TSPC strategy has the advantage of simple and compact clock distribution, a logic design flexibility as well as low power consumption [65].

In our design, a standard differential to full swing converter shown in Fig.6.13 (c) is utilized to convert the differential signal from differential divider to full swing signal for input of a fixed TSPC divide-by-2 divider.

The topologies of the differential CML divide-by2/3 dual modulus divider and TSPC single end dividers are utilized in our design because they can achieve a higher operating frequency, a better immunity to noise along the signal path because of its differential structure as well as they can save power consumption.

4) Simulation Results

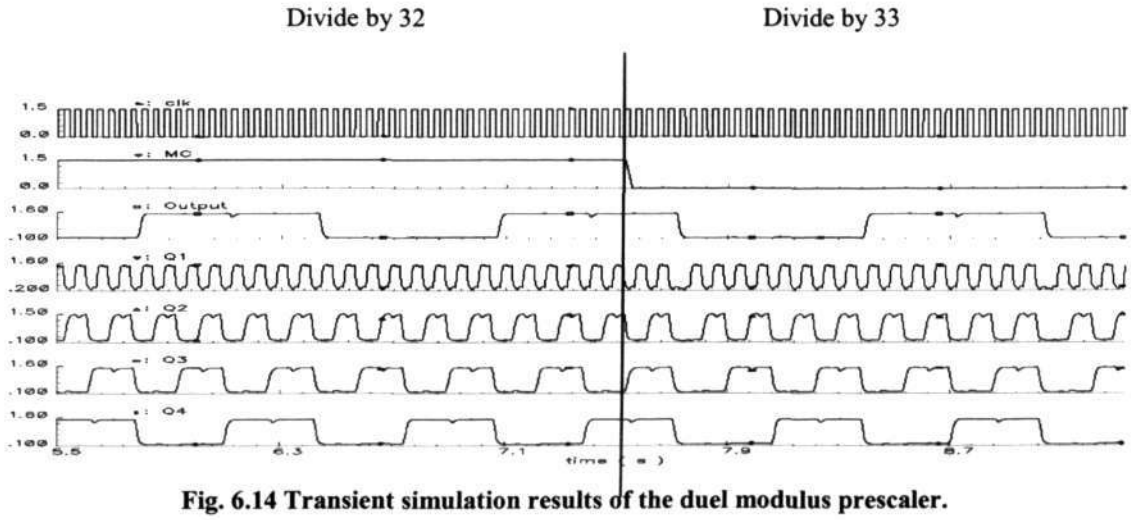


Fig. 6.14 Transient simulation results of the duel modulus prescaler.

For the dual–modulus prescaler design optimization, the timing requirements of each node is identified by the circuit operation. The dual–modulus prescaler is designed by the

iterative simulation of SpectreRF at 2.45 GHz. The modulus–control signal MODE is switched from 1 to 0 to change the frequency division ratio. Simulation results given in Fig.6.14 show that the divide–by–32/33 prescaler functions properly at 2.45 GHz.

6.2.2.4. P and S counter

1) Operation

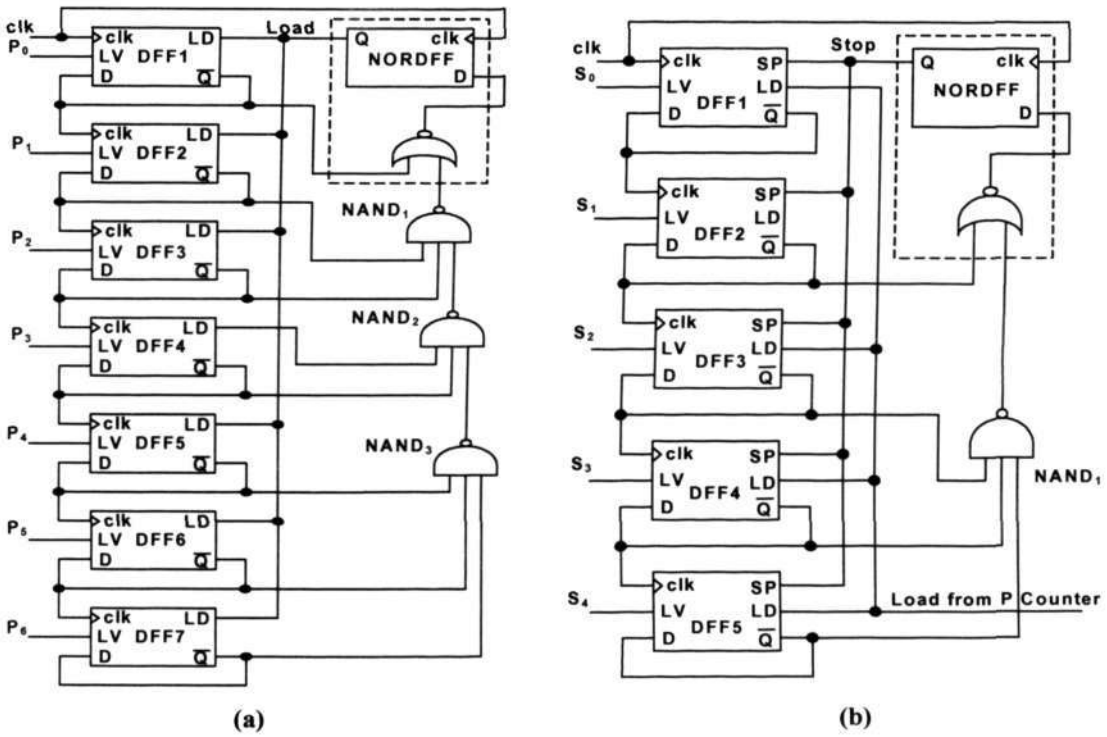


Fig. 6.15 (a) P counter, (b) S counter.

The 7–bit P and 5–bit S counters are implemented in the pulse swallow frequency Divider (PSFD). The P counter shown in Fig.6.15 (a) consists of seven loadable TSPC D–flip–flops (DFF_1—DFF_7) like a loadable ripple counter. Three static logic gates $NAND_1$, $NAND_2$, and $NAND_3$ for the final state detection, and a NOR gate embedded D–flip–flop (NORDFF). At the beginning, inputs P_0 to P_6 are loaded into the signal LV (Load Value) of all the true single phase clock (TSPC) D–flip–flops. The counter then

begins to count down to the final state. At the final state, NORDFF generates the reload signal (Load) so that signal LD (Load) of all the flip–flops is reloaded and the operation repeats itself.

The implementation of the S counter shown in Fig.6.15 (b) is similar to that of the P counter. The difference is that a stop signal (Stop) is generated to stop the counter operation at the final state. The S counter reloads when the P counter completes counting, and the operation repeats itself.

2). True Single Phase Clock

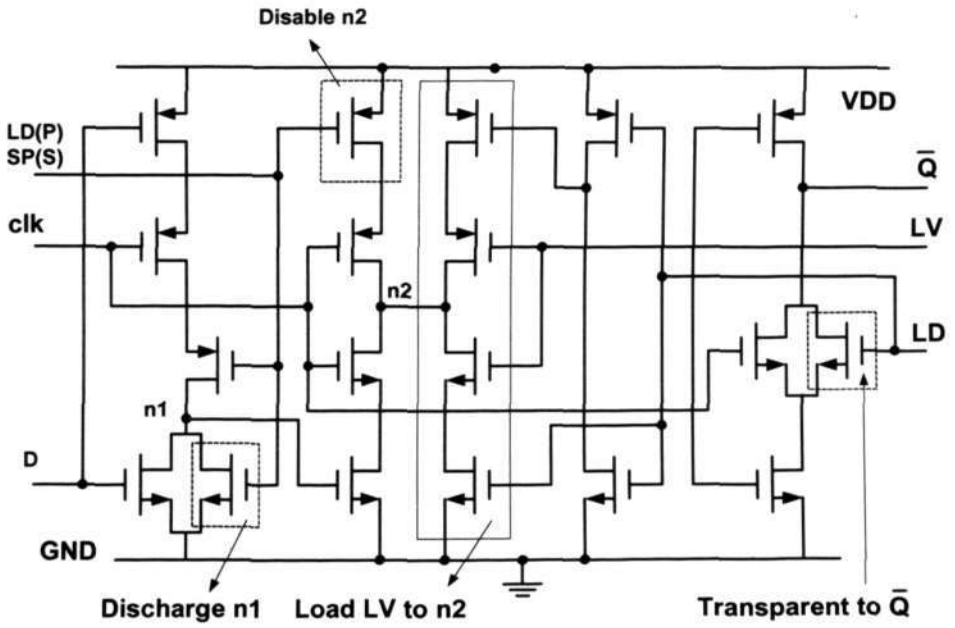


Fig. 6.16 True single phase clock D–flip–flop (DFF).

The implementation of the loadable TSPC D flip–flops for the P counter is shown in Fig.6.16 [81]. When the signal "LOAD" or LD is at logic '1', node n1 is discharged to logic '0' to isolate the input signal D and the output signal $\overline{Q}$. At the same time, nodes n2 and Q are made transparent to the load value LV. Thus $\overline{Q}$ is dependent on LV when LD

is at logic '1' (HIGH) i.e. when LV = '1', $\overline{Q}$ = '1'. On the other hand, when LD is at logic '0', $\overline{Q}$ is dependent of D and positively triggered. At the rising clock, when D is at logic '0', $\overline{Q}$ will rise from '0' to '1'.

2) NOR Gate–Embedded D Flip–Flop (NORDFF)

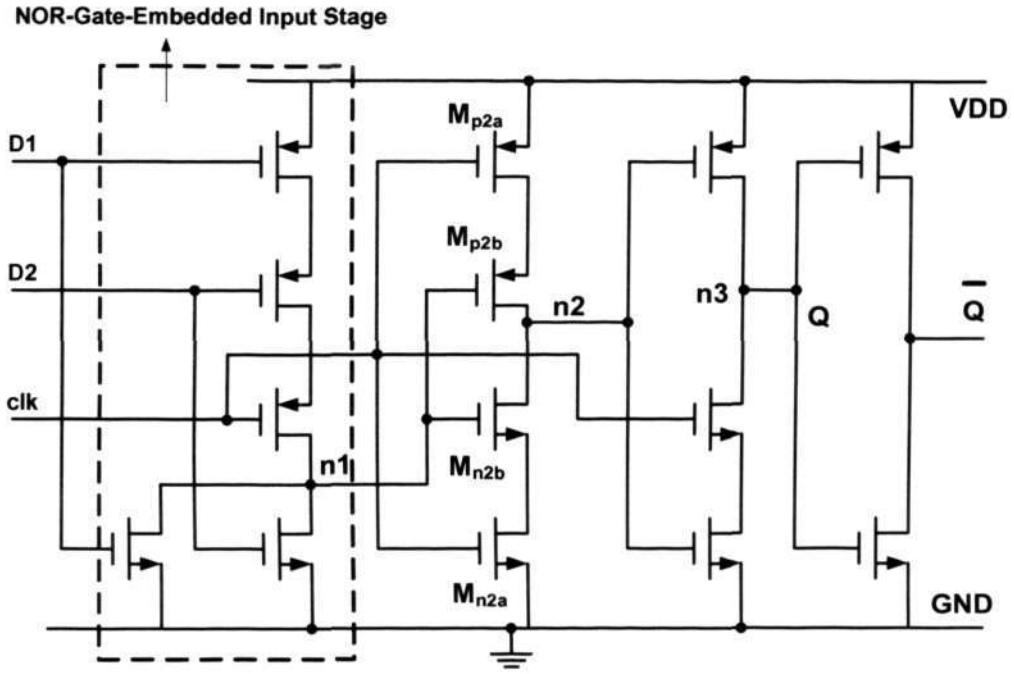


Fig. 6.17 NOR–gate–embedded D–flip–flop (NORDFF).

The NOR–gate–embedded D–flip–flop NORDFF shown in Fig.6.17 is realized by embedding a NOR gate in the input stage of the TSPC D–flip–flop (TDFF). Although there are three PMOS transistors being used in cascade that may degrade the speed, the speed requirement of the first stage is only 50 percent of input period. In TSPC DFF, a transistor M_{p2b} is included so that the node n_2 is not precharged in every clock cycle and output glitches can be eliminated [82].

When D_1 and D_2 are both at logic '0', n1 is high, and it turns on M_{n2b}. With the edge of a rising clock, M_{n2a} becomes on. As a result, n_2 is pulled down to logic '0', and because of the inverter, n_3 becomes high thus resulting a low "Out". Likewise, when both D_1 and D_2 are at logic '1', "Out" is high ("Out" here refers to the $\overline{Q}$ of the NORDFF).

6.2.2.5 Simulation Results

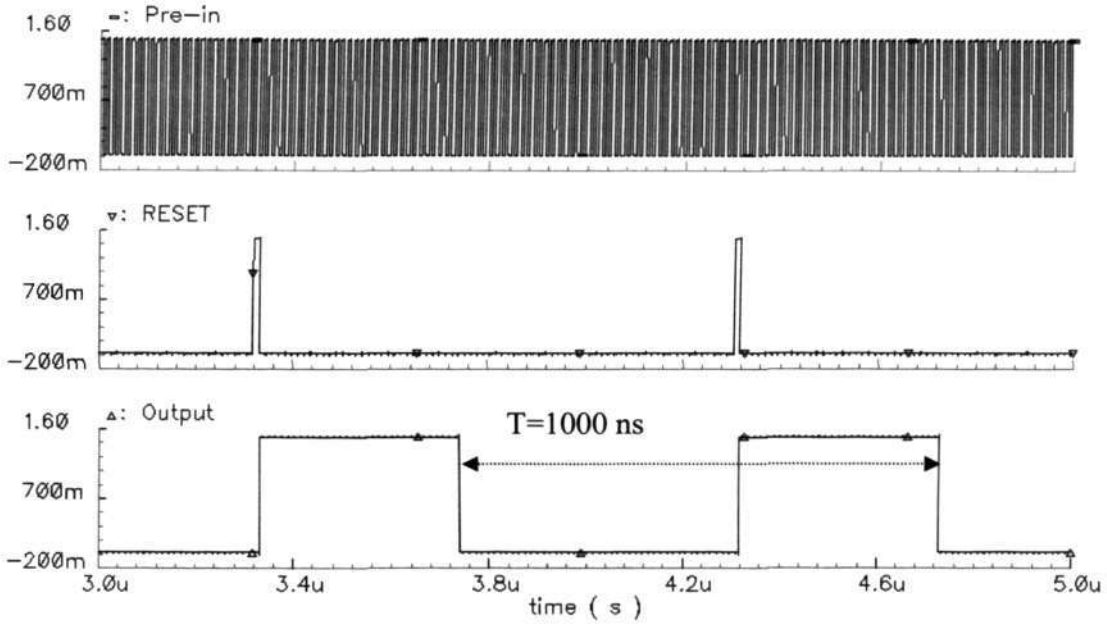


Fig. 6.18 Transient simulation results of the divider with the division ratio 2450.

The programmable–frequency divider is simulated by SpectreRF with a frequency division ratio N=2450 at 2.45 GHz. The results of this simulation are shown in Fig.6.18. The power consumption of the frequency divider is around 18 mW. The functionality of the programmable frequency divider at different frequency division ratios are also verified by the transient simulation.

When the frequency division ratio is changed, the divider N may not change its division ration instantaneously. The worst possible delay is one output cycle (such as 625 ns). However, such a delay is negligible in comparison to the switching requirement of

the system, leading us to conclude that the switching delay of divider N is not critical in such an application.

6.2.3 Phase Frequency Detector

The PFD is used to compare the phase and frequency of the reference input and the frequency–divider output. It generates the corresponding output signal to control the frequency of the VCO. The design requirements of the PFD are as follows as:

- Operate at frequency of up to 1 MHz.
- Detect both the phase and frequency differences between the reference frequency and the output frequency of the divider.
- Eliminate the dead–zone problem which limits the close–in phase noise suppression.

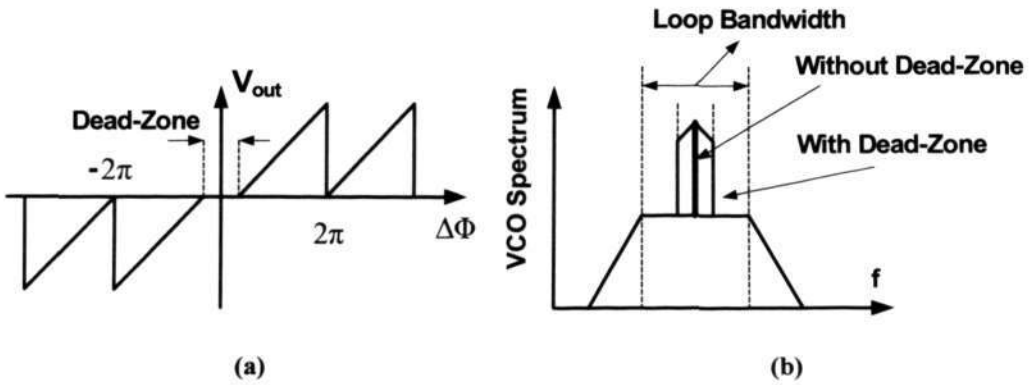


Fig. 6.19 Effect of (a) PFD transfer function, (b) PFD close–in phase noise with and without a dead–zone.

The dead–zone in the PFD can be traced to the inability of the digital logic gate to generate infinitely short pulses. When the phase error $\Delta\Phi$ is very small, the PFD cannot compare the phase error of the reference frequency and the output frequency of the

divider, and the PFD gain K_{PFD} becomes zero as shown in Fig.6.19 (a). As the loop is broken, both reference and VCO phase noise s cannot be suppressed by the loop and the close–in phase noise is significantly degraded as shown in Fig.6.19 (b) [83].

6.2.3.1 Operation

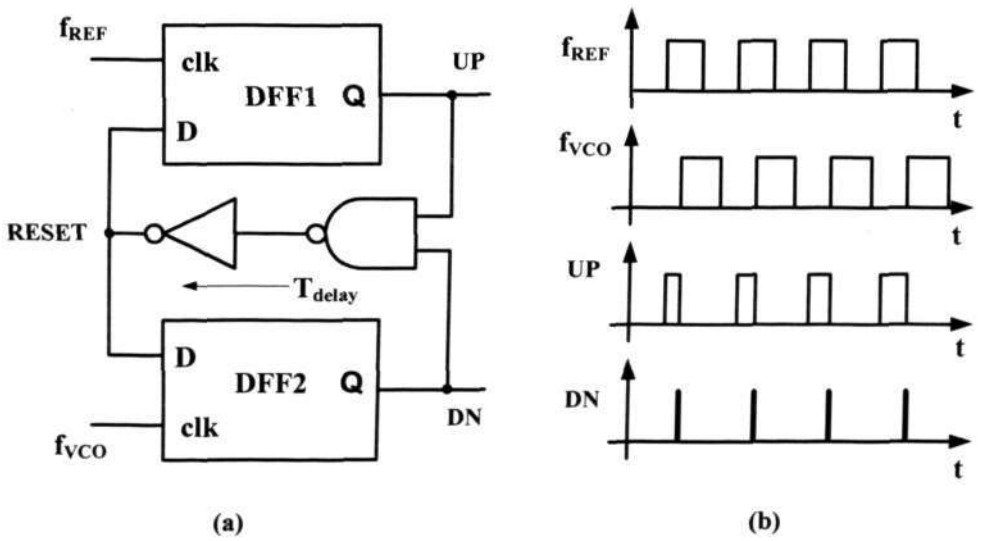


Fig. 6.20 PFD implementation: (a) Block diagram, (b) Operation function.

The implementation of the PFD is shown in Fig.6.20 (a). The PFD consists of two TSPC DFF registers, a NAND gate and an inverter. As shown in Fig.6.20 (b), when the PFD input f_{REF} has a rising edge first, a UP signal is generated to raise the oscillator frequency. After a certain time, the PFD input f_{VCO} has the rising edge, and a DN signal is generated to stop the oscillator frequency increment. Due to the delay of the NAND gate and inverter (T_{delay}), both UP and DN signals are turned on simultaneously for a period of T_{delay}. The pulse width of both UP and DN signals are kept finite so as to eliminate the problem caused by the dead–zone. After T_{delay}, a RESET signal is generated to reset both TSPC half transparent registers. If the frequency of f_{REF} is larger than that of

the f_{VCO}, the pulse width of the UP signal increases gradually so a frequency difference can also be detected.

6.2.3.2 Circuit Implementation

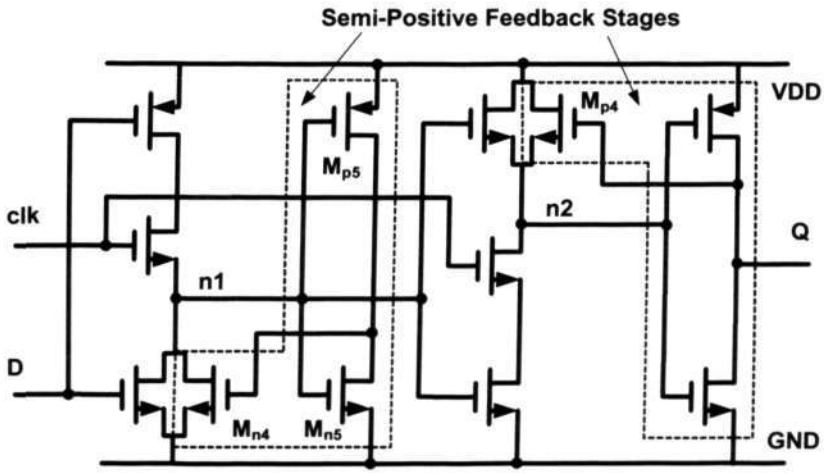


Fig. 6.21 Implementation of the TSPC half–transparent D–flip–flop of the PFD.

The TSPC half–transparent D–flip–flop is implemented as shown in Fig.6.21 which is similar to the one in Fig.6.20 (a) [84]. The half–transparent D–flip–flop HTDFF is transparent to D = "1" and has a one–clock delay to D = "0". As the PFD operates at frequencies as low as 1 MHz in the frequency loop, leakage of the junction of transistors may cause the charges of the pre–charge nodes n_1 and n_2 to leak significantly. Therefore, semi–positive feedback stages (M_{n4}, M_{p4}, M_{n5} and M_{p5}) are added to nodes n_1 and n_2 in order to maintain the pre–charged node voltage [85].

The main advantage of this PFD is : 1) High–speed and low power PFD were brought about by the use of a modified true single phase clock (MTSPC) positive edge triggered D flip–flop. 2) Less than 0.01 ns dead–zone in the phase characteristics. 3) Low phase

sensitivity errors because of a lack of limitation in the phase and frequency error detection range.

6.2.3.3 Simulation Results

To Simulate the PFD by SpectreRF, two input signals at 1 MHz and 1.2 MHz frequencies are applied to the PFD. As shown in Fig.6.20 (b), the increasing pulse that coincides with the UP signal indicates that the PFD is functioning properly as shown in Fig.6.22.

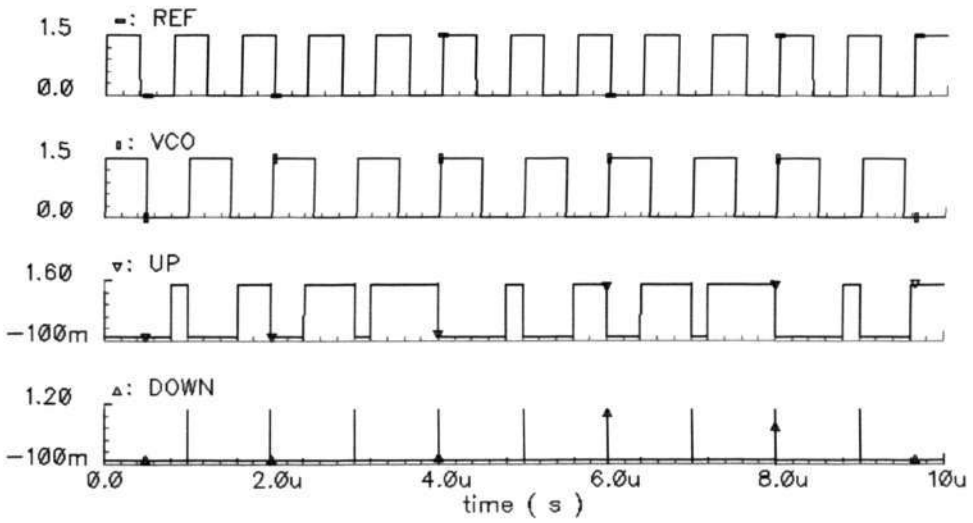


Fig. 6.22 Simulation results of the PFD.

6.2.4 Charge Pump & Low Filter

According to the UP and DN signals of the PFD, charge pump injects or sinks the current to or from the loop filter. The loop filter filters out the high frequency components, so to maintain the spectral purity of the VCO. The design requirements of the charge–pump and loop filters are as follows:

- Operate at frequencices up to 1.2 MHz.

- Minimize the loop filter chip area
- Satisfy the spurious–tone specification (<–51 dBc/Hz@1 MHz) and the phase noise specification (<–111 dBc/Hz@3 MHz) of the frequency synthesizer.

To satisfy both the phase noise and spurious–tone specification, the loop bandwidth of the loop is reduced to several tens of kHz. Therefore, the large capacitors (~ nF) and resistors (~ kΩ) that are used for the loop filter implementation are the very critical to the synthesizer integration.

6.2.4.1 Charge Pump

In order to convert the logic states of the PFD into analog signals suitable for controlling the VCO, a charge pump circuit is used as given in Fig.6.23. Based on the signal from the PFD, the charge pump will generate a charge current and a discharge current that enter the loop filter so that the control voltage of VCO is varied.

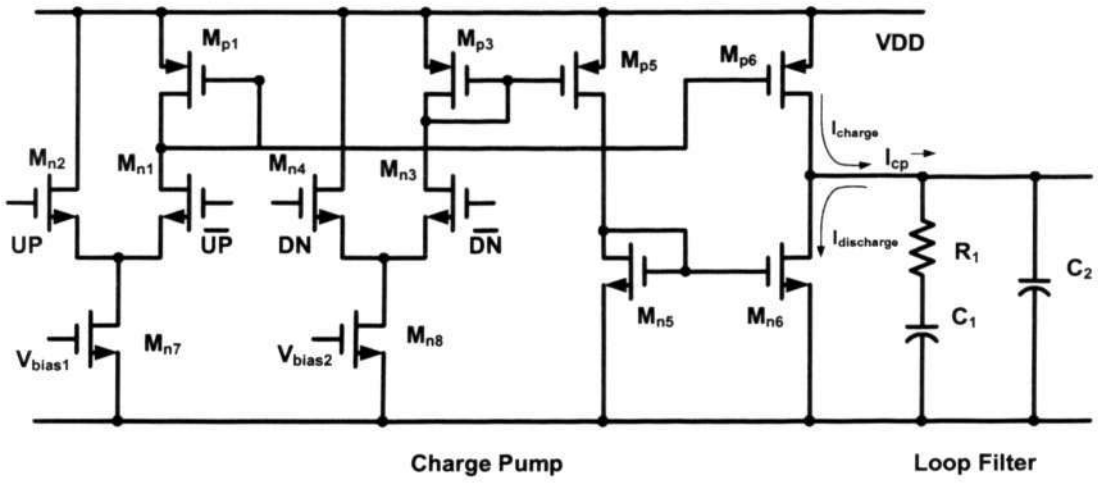


Fig. 6.23 Charge pump circuit.

The charge pump circuit consists of two input differential pairs (M_{n2}–M_{n1} & M_{n3}–M_{n4}) that act as the switches. Two current sources (M_{n7} and M_{n8}) supply stable

currents to the differential pairs, while a pump–up sub–circuit (M_{p1} and M_{p6}) outputs the charge current I_{charge} and a pump–down sub–circuit (M_{p4}, M_{p5}, M_{n5} andM_{n6}) releases the discharge current $I_{discharge}$. The charge pump circuit has two pairs of differential input signals, namely, UP & $\overline{UP}$ and DN & $\overline{DN}$ as shown in Fig.6.23. Four conditions exist when the charge pump is operating. The first one occurs when the UP signal is driven high (UP = 1.5 V, $\overline{UP}$ = 0 V) and the DN signal is low (DN = 0V, $\overline{DN}$ = 1.5 V). The UP signal will turn on M_{n1}, which in turn, switches on the pump–up sub–circuit. Hence, I_{charge} will then flow from M_{p6} and the loop filter will be charged up. At the same time, M_{n3} turns off because the DN signal is low. This causes the pump–down sub–circuit to turn off and no $I_{discharge}$ flows in M_{n6}.

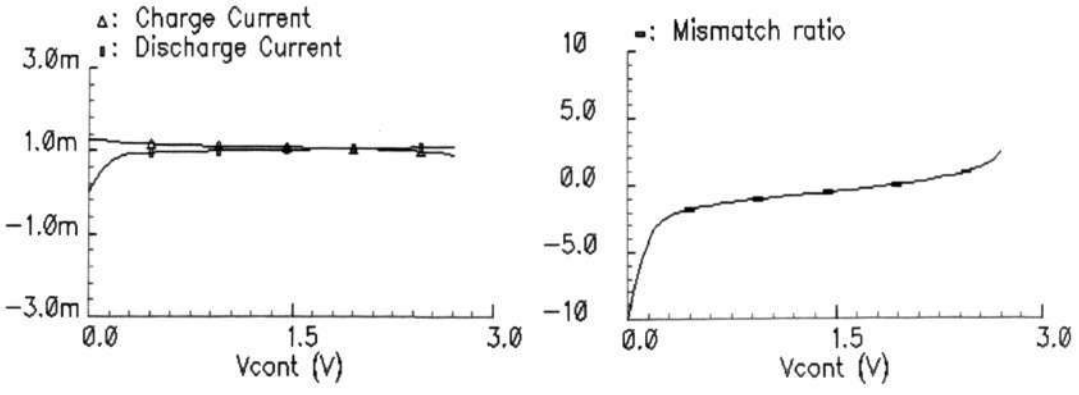
The second condition is the opposite of the first and occurs when the DN signal is driven high (DN = 1.5 V, $\overline{DN}$ = 0 V) and the UP signal is low (UP = 0 V, $\overline{UP}$ = 1.5 V). The DN signal will turn on the pump–down sub–circuit, allowing $I_{discharge}$ to flow to GND, and no current flows from M_{p6}. The third condition is when UP and DN signals are both driven high simultaneously. During such a period, Transistors M_{n2} and M_{n4} will be turned off, allowing the current to flow in M_{n1} and M_{n3}. These currents will be steered to M_{p1} and M_{p3}. If I_{charge} and $I_{discharge}$ are equal, V_{cont} will remain as it is. However, because of the mismatches in I_{charge} and $I_{discharge}$, a net current of $\left|I_{charge} - I_{discharge}\right|$ will flow in the loop filter, and cause a shift in the threshold voltage. This net current will introduce a leakage in the charge pump that will impact the V–CTRL value. Reducing the mismatching current is thus still a challenge for the designers. The last condition is when both UP and DN signals are at zero. Transistors M_{n1} and M_{n3} will be off and therefore, all

the currents from the current sources (M_{n7} and M_{n8}) will be steered to M_{n2} and M_{n4}. I_{charge} and $I_{discharge}$ will then be equal to zero.

To compensate for the finite output difference of the charge and discharge current and match their currents more precisely over all the output voltages, the charge and discharge currents are monitored in the circuit, in which a network is used to measure the charge current and discharge current when the control voltage of the VCO (V_{cont}) is varied from –1.8 V to 1.8 V. Fig.6.24 (a) shows the charge current and discharge current versus V_{cont}, and Fig.6.24 (b) shows a function of the percentage mismatch between the charge/ discharge current and V_{cont}. The percentage error is less than 2% as $0.5\ V \le V_{cont} \le 2.5\ V$.

The function of the percentage mismatch is defined as: $\text{ratio} = \dfrac{(I_{charge} - I_{discharge})}{I_{charge}} \times 100\%$.

The simulation results of PFD&CP are shown in Fig.6.25, and the controlled voltage is increased linearly.



(a) **(b)**

Fig. 6.24 Functions of (a) Charge currents and discharge currents, (b) Mismatch ratio versus the controlled voltage (V_{cont}).

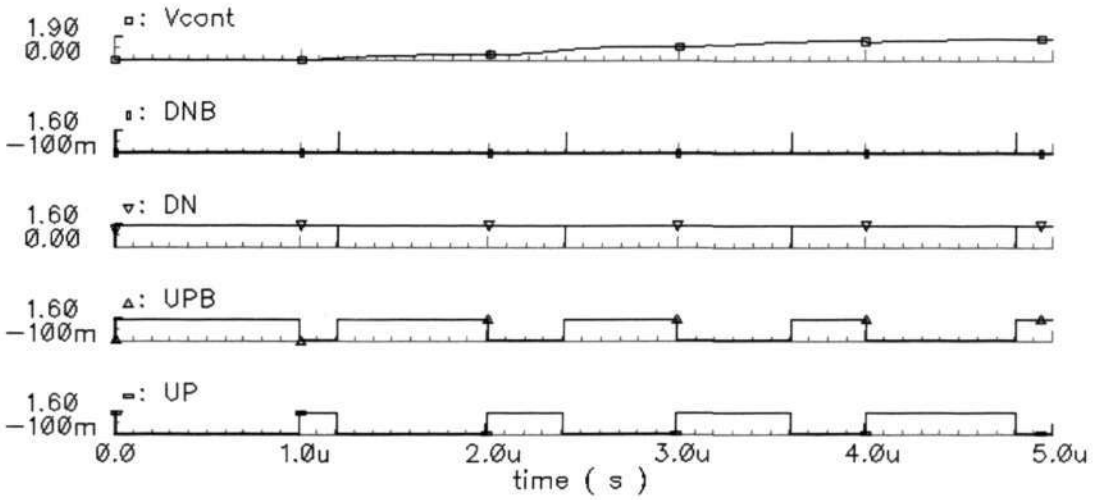


Fig. 6.25 Simulation results for the charge and discharge functions of the charge pump.

6.2.4.2 Second Order Loop Filter

The choice of the transfer function H(s) in equation (5.1) is very important. It determines the loop bandwidth of the frequency synthesizer and this is related directly to the performance of the whole synthesizer, including the phase noise , spurious tone and settling time. In the proposed synthesizer architecture, a second order type II loop filter given as Fig.2.11 is implemented because it is large enough to reduce the output phase noise of the charge pump and loop filter.

Our goal is to achieve a low phase noise within two constraints: The first constraint is the low power consumption, and the second and more important constraint concerns the limited chip area. We must limit the size of the capacitor sizes of C_1 and C_2 in the integrated circuit to a value reasonable. The final optimized loop parameters calculated by equation (5.8) are listed in Table.6.2. Within these parameters, the settling time is around 22 μs by equation (2.14) and the total capacitance value is as large as 55 pF.

Table 6.2 All parameters.

Loop band width	ω_c	100 kHz×2π
Charge pump current	I_{cp}	100 μA
Zero ratio	$a = \omega_c / \omega_z$	4
Pole ratio	$b = \omega_p / \omega_c$	4
Loop filter	R_1	27.3 kΩ
	C_1	50 pF
	C_2	4.5 pF

6.3 Spurious Tone Analysis

In this section, the spurious tone, which is mainly caused by the charge pumps, is discussed. Different causes of the spurious tone such as a mismatch of current, clock feed-through, charge injection and charge sharing are discussed and analyzed. Based on the analysis results, the charge pump is designed to optimize the spurious–tone performance.

6.3.1 Current Mismatch

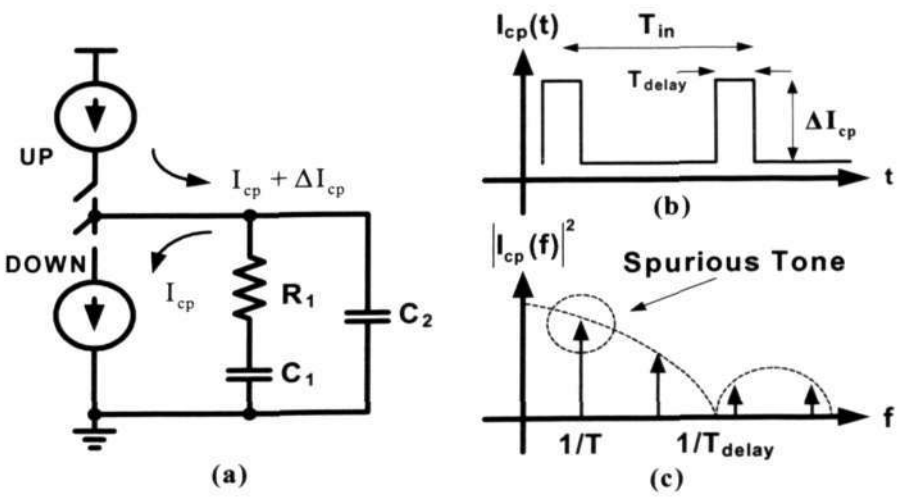


Fig. 6.26 Charge–pump current–injection mismatches (a) Cause, (b) Transient response, (c) Frequency response.

As discussed in section 6.2.3, a feedback delay time T_{delay} is added in the PFD in order to eliminate the dead–zone problem. During the delay time, both pull–up and pull–down charge–pump currents are turned on. In the ideal situation, these pull–up and pull–down currents are exactly the same so that no net current is injected into the loop filter. However, the mismatch between pull–up and pull–down charge–pump currents introduces a current injection ΔI_{cp} as shown in Fig.6.26. Such a current disturbs the controlled voltage of the VCO and causes the spurious tones.

The current mismatch is due mainly to the mismatch of the channel length, channel width and threshold voltage of the current sources, and the mismatches between NMOS and PMOS as given in Fig.6.23. Therefore, long–channel devices for the current sources are used to reduce the current mismatch in our design.

To improve the spurious–tone performance, the charge–pump related current mismatch should be reduced. Since the spurious power is proportional to the current injection time, the feed delay T_{delay} of the PFD is designed to be 1/20 of the input period $T_{in.}$

6.3.2 Switch Clock Feed-Through and Charge Injection

In charge–pumps, every time when the switches are turned off, the clock feed-through and charge injection of the switches disturb the controlled voltage of the VCO though dumping the charge to the loop filter by UP and DN switch operation. To eliminate the clock feed-through, complementary switches with the same transistor size are adopted. However, overlaping–capacitance and channel–width mismatches exist

between NMOS and PMOS transistors. Therefore, the minimum size transistor is adopted in our design to degrade the clock feed-through of the switches, while at the same time, minimizing the charge injection.

6.3.3 Spurious Tone Optimization

To improve the spurious tone performance, the following design guidelines are adopted:

- Use long–channel devices for the current sources to reduce the current mismatch.
- Use minimum size transistors for the switches to reduce clock feed-through and charge injections.
- Reduce loop bandwidth to improve spurious–tone suppression, but the loop filter area is increased. Therefore, the compromise is inevitable.

6.4 Phase Noise Evaluation

In this section, the phase noise of the frequency synthesizer is discussed. The phase noise generated by the reference signal and frequency divider is very low. Therefore, the phase noise discussion is focused on the charge pump, loop filter and the VCO. Fig.6.27 illustrates the linear noise model of the frequency synthesizer.

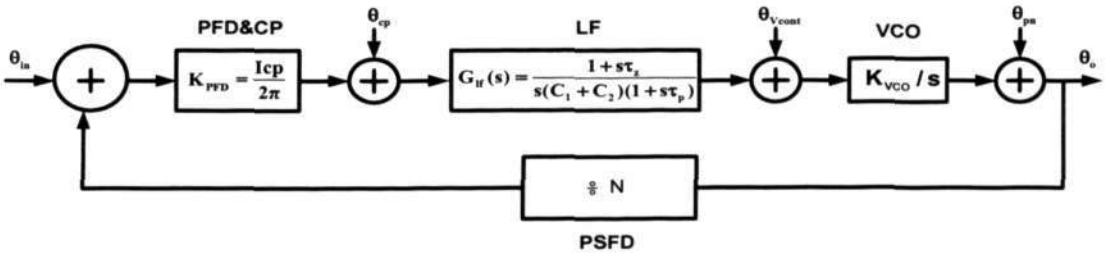


Fig. 6.27 Linear noise model of the proposed frequency synthesizer.

6.4.1 Phase Noise Contributions of the Charge–Pump and Loop Filter

6.4.1.1 The Charge Pump's Noise Contribution

The charge pump output current also makes a contribution to the noise. The current sources of magnitude I_{cp} have a noise current $di^2_{n,cp}$. In the locked condition, all current noises add up quadratically to a value of:

$$di^2_{n,cp} = 4kTg_{m,cp}df \tag{6.4}$$

Here $g_{m,cp}$ is the transconductance of the charge pump when it charge or discharge current to the loop filter.

From the linear noise model of the frequency synthesizer, the noise from the charge pump to the output can be calculated as equation (6.5). For the offset frequencies far outside the loop band width, i.e. larger than ω_c, the loop filter impedance can be approximated by $\frac{1}{sC_2}$.

$$\frac{\theta_o}{\theta_{cp}}(s) = \frac{G_{lf}(s)K_{VCO}}{s + K_{PFD}G_{lf}(s)K_{VCO}\frac{1}{N}}\frac{2\pi N}{I_{cp}}\frac{b\omega_c^2}{s^2} \tag{6.5}$$

Then the single sided spectral phase noise density from the charge pump becomes [19]:

$$\begin{aligned} L_{CP}(\Delta\omega) &= \frac{1}{2}\left(\frac{\theta_o}{\theta_{cp}}\right)^2 4kTg_{m.cp} = \frac{1}{2}\left(\frac{2\pi N}{I_{cp}}\frac{b\omega_c^2}{(\Delta\omega)^2}\right)^2 4kT\frac{2I_{cp}}{V_{gs}-V_{th}} \\ &= kT(4\pi Nb)^2\frac{2}{I_{cp}(V_{gs}-V_{th})}\left(\frac{\omega_c}{\Delta\omega}\right)^4 \end{aligned} \tag{6.6}$$

where, $(V_{gs} - V_{th})$ is the net voltage between the gate and source of the charge transistor M_{n1} and the discharge transistor M_{n3} as shown in Fig.6.23.

The charge pump output phase noise L_{CP} can be lowered a bit by increasing $(V_{gs} - V_{th})$ value of the charge transistor. Also the choice of I_{cp} and the loop bandwidth ω_c is very important, not only for the transient characteristics of the synthesizer, but certainly also for the noise characteristics as demonstrated by the above calculations.

6.4.1.2 Loop Filter's Noise Contribution

The resistor R_1 in the loop filter also generates white noise $di^2_{n,R1} = \frac{4kT}{R_1}df$ that will contribute to the output phase–noise. Like the phase noise contribution of the charge pump, the feedback model given in Fig.6.27 is used for the calculations. For the offset frequency larger than ω_c, and when R_1 is expressed as a function of the loop parameters, the phase noise can be approximated by [19]:

$$L_{LF}(\Delta\omega) = kT(4\pi Nb^2)\frac{K_{VCO}}{I_{cp}\omega_c}\left(\frac{\omega_c}{\Delta\omega}\right)^4 \qquad (6.7)$$

Therefore, the most obvious strategy to reduce the phase noise contribution from the loop filter is to lower the loop bandwidth. This takes into account the fact that there is a dependency on ω_c^3 in the phase noise expression. Obviously, the reduction comes at a price – the size of the capacitors C_1 and C_2 are both inversely proportional to the square of ω_c, and so while increasing I_{CP} helps to degrade the noise contribution, but again the capacitor values inevitable become larger.

6.4.2 VCO's Phase Noise Contribution

In the section of 6.1.2, a 2.45 GHz VCO was designed and analysed by SpectreRF. The performance of the phase noise is around −117 dBc/Hz at an offset frequency 600 kHz away from the center frequency of 2.45 GHz; −122 dBc/Hz at an offset frequency of 1 MHz; and −135 dBc/Hz at an offset frequency of 3 MHz. In general, the phase noise is inversely proportional to the square of the offset frequency and the phase noise of the oscillator can be expressed as follows:

$$L_{VCO}(\Delta\omega) = \frac{10^{-117/10}(2\pi \times 600 \times 10^3)}{(\Delta\omega)^2} \tag{6.8}$$

Here, $L_{VCO}\{\Delta\omega\}$ is the phase noise of the VCO, and $\Delta\omega$ is the offset frequency. Following from the earlier discussion, the phase noise contribution from the VCO to the frequency synthesizer can be calculated as follows:

$$L_{Total-VCO}(\Delta\omega) = \left|\frac{\theta_o}{\theta_{pn}}\right|^2 L(\Delta\omega) \tag{6.9}$$

6.4.3 Total Phase Noise of the Frequency Synthesizer

After taking into account the phase noise due to the VCO, the charge pump and the loop filter, the total phase noise of the frequency synthesizer can be expressed as:

$$L_{SNT}(\Delta\omega) = L_{CP}(\Delta\omega) + L_{LF}(\Delta\omega) + L_{Total-VCO}(\Delta\omega) \tag{6.10}$$

This expression is useful for the design optimization of the charge pump and the loop filter. The design guidelines to optimize the phase noise performance are summarized as follows:

- Increase $V_{gs}-V_{th}$ of the UP and DN transistors in the charge pump to reduce the noise power with the same current bias.
- Reduce resistance R_1 and increase both capacitance C1 and C2 in order to reduce the noise produced by the loop filter.
- Reduce loop bandwidth to further suppress the phase noise brought about by the charge pump and loop filter.

According equations (6.6), (6.7), (6.9) and the parameters of the loop shown in Table 6.2, the phase noise contributions are evaluated and tabulated in Table 6.3. The phase noise related performance of the proposed frequency synthesizer surpasses the Bluetooth's required phase noise performance. A 1 dB phase noise margins at 3 MHz offset frequency is reasonable value for the effect from the reference, divider and layout.

Table 6.3 Phase noise contributions from the building blocks in the frequency synthesizer.

Blocks	Sign	600 kHz offset	3 MHz offset
Charge pump	L_{cp}	−115.7 dBc/Hz	−131.6 dBc/Hz
Loop filter	L_R	−108 dBc/Hz	−124 dBc/Hz
VCO	L_{vco}	−117 dBc/Hz	−122 dBc/Hz
Total phase noise	L_{SNT}	−106 dBc/Hz	−112 dBc/Hz

6.5 Stability

To lock the PLL at the desired output frequency, the loop must have enough phase margin to meet the loop stability consideration. The phase margin is defined in section 5.1, and it depends completely on two ratios $a=\frac{\omega_c}{\omega_z}$ and $b=\frac{\omega_p}{\omega_c}$. Therefore, in our

design, a=b=4 is stipulated for a maximum phase margin of 60°, A detailed explanation is provided in section 5.1. The ratio of the input frequency to the loop bandwidth is 20 in this design, rendering the system is stable in view of the theory presented in section 5.3.

6.6 Simulation and Experiment

The whole system is simulated by ADS and the transient response is shown in Fig.6.28. The settling time is approximately 22 μs. Simulations are also carried out using Spectral-RF when the division ratio is various. Fig.6.29 gives the simulation results when the division ratio N is 2462 and 2463 (N=32, P=76, and S=30, 31). We note that the switching time is as short as 5 μs when two channels are switched.

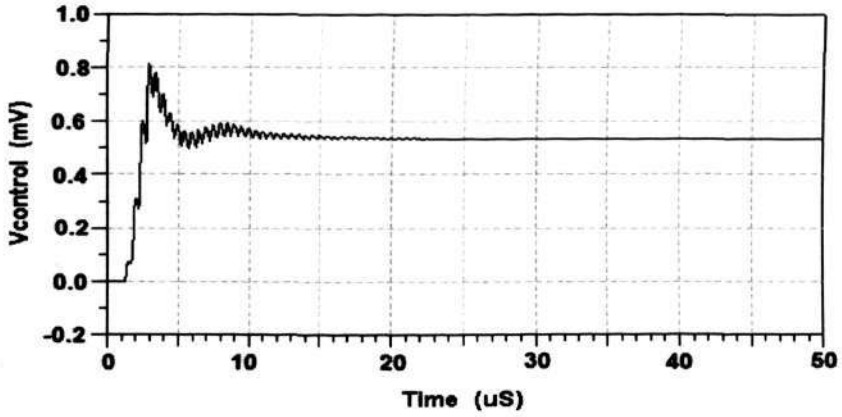


Fig. 6.28 Transient response of the frequency synthesizer by ADS.

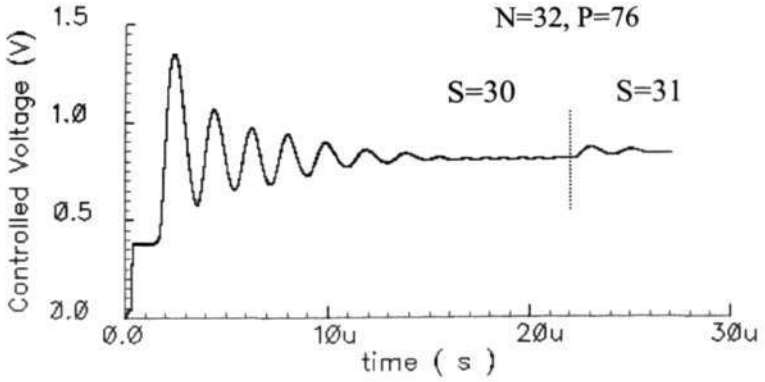


Fig. 6.29 Transient response of the frequency synthesizer with division ratio of 2463 and 2464.

The power consumption of the whole system is around 31 mW, of which the VCO's power is 12 mW, the PFD's power is 0.0075 mW, the charge pump and loop filter's power are 1.2 mW, and the divider's power is 18 mW. The peak–to–peak voltage of the output is around 1.4 V as given in Fig.6.30. The simulated output spectrum of the frequency synthesizer in a locked state is given in Fig.6.31, which depicts the spurious tone of –68 dBc. All parameters meet the requirement of the Bluetooth specification.

Having discussed aspects of the design issue of all the building blocks, we presented the performance of our proposed frequency synthesizer in terms of the phase noise, chip area, spurs tone and power consumption in Table.6.4. The simulated performance is then compared with recently reported other monolithic CMOS frequency synthesizers as shown in Table 6.5. The design proposed in this thesis has the smallest chip area, low supply voltage and provides a truly monolithic on chip for the whole system. We note, at the same time, that it fully satisfies all the Bluetooth application requirements.

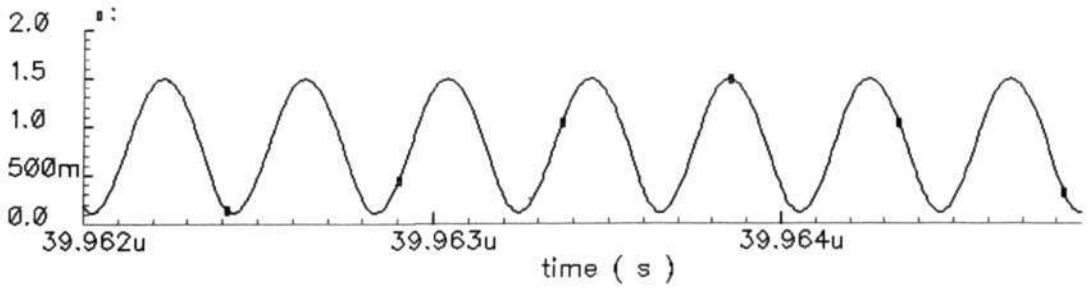


Fig. 6.30 One of the differential outputs.

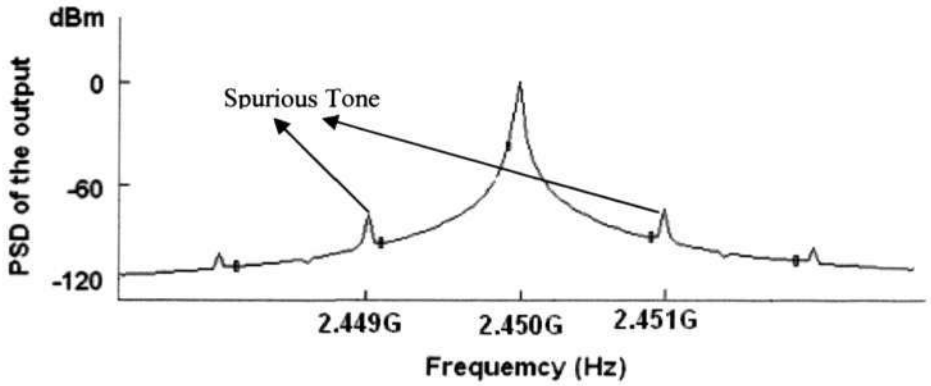


Fig. 6.31 Spurious level of the whole system.

Table 6.4 Summary of the whole system performances.

PAREMETERS	SPECIFICATION	SIMULATION
Supply voltage	1.8 V	1.8 V
Frequency range	2.4 GHz–2.4835 GHz	2.38 GHz–2.56 GHz
Frequency resolution	1 MHz	1 MHz
Tuning range	3%	7.3%
Phase noise at 3 MHz	−111 dBc/Hz	−112 dBc/Hz
Spurious tone	<−51 dBc@1 MHz	−68 dBc@1 MHz
Switching time	<62.5 μs	22 μs
Power	<70 mW	31 mW
Technology	CSM 0.18 μm RF/Analog CMOS	CSM 0.18 μm RF/Analog CMOS
Chip Area	2 mm^2	1.8 mm^2

Table 6.5 Comparison of recent reported designs.

Parameters	Ref [86]	Ref [87]	Ref [30]	This work (simulated)
Voltage supply	2.6 V	3.3 V	2.6 V	1.8 V
Architecture	Fractional–N	Fractional–N	Integer–N	Integer–N
Frequency	2.4 GHz	2.5 GHz	2.6 GHz	2.45 GHz
Reference Frequency	5 MHz	24 MHz	11.75 MHz	1 MHz
Loop bandwidth	35 kHz	700 kHz	N/A	100 kHz
Turning range	N/A	N/A	N/A	180 MHz
Phase noise @600kHz	−88 dBc/Hz	−100 dBc/Hz	−84 dBc/Hz	−106 dBc/Hz
Spurious tone	−85 dBc	−77 dBc	−55 dBc	−68 dBc
Switching time	N/A	5 μs	40 μs	22 μs
Power	16 mW	135 mW	47 mW	31 mW
Technology	0.35μm BiCMOS	0.5μm CMOS	0.45μm CMOS	0.18μm CMOS
On–chip filter	N/A	No	Yes	Yes
On–chip inductor	N/A	No	Yes	Yes
Chip area	6.2mm^2	3.5 mm^2	2 mm^2	1.8 mm^2

6.7 Conclusion

We have described a design of a fully integrated monolithic CMOS 2.45 GHz frequency synthesizer, which is designed for the Bluetooth applications. The integrated VCO uses a spiral inductor with a quality factor of 8.5 to achieve the required phase noise level with the minimal power consumption. The integer–N pulse swallow programmable divider allows for the implementation of a dual–modulus prescaler (divide–by–32/33), in which a dual–modulus high speed divide–by–2/3 divider and one fixed differential CML divide–by–2 divider and three fixed full swing TSPC divide-by-2 dividers are utilized. The programmable P counter and S counters are also used, in which

TSPC–DFFs are used for the full swing output and the division ratio ranges between 2402 and 2480. A behavioral model of the PLL was implemented in ADS to optimize the loop parameters to ensure the low noise levels.

A simulated phase noise performance of −112 dBc/Hz at the offset frequency of 3 MHz was achieved. The spurious tone was degraded to −68 dBc at the offset frequency of 1 MHz. The power consumption was brought down to 31 mW and the output peak to peak voltage is 1.4 V. The tuning range is from 2.4 GHz to 2.4835 GHz. The proposed frequency synthesizer is implemented using CSM 0.18 μm Analog/RF CMOS technology, and the die area is 1.2×1.5 mm^2.

CHAPTER 7

A Dual Band 52/104 GHz VCO Implemented in SiGe BiCMOS Technology

High frequency and low phase noise oscillators are key components in achieving high performance and low cost millimeter wave applications such as wireless communication systems and automotive radar systems. Several monolithic MMW voltage controlled oscillators have been reported using HEMT [88], InP–based HBT [89] and CMOS technologies [90]. However, the phase noise is limited by the high intrinsic 1/f noise presented in HEMTs, the small tuning range as well as the high power consumption in InP based HBTs, and the high substrate loss in CMOS technology [91] [92] [93]. The SiGe BiCMOS is chosen in this thesis because of its impressive high frequency performance at both device and circuit levels. Furthermore, the substrates used in SiGe BiCMOS processes typically have a medium resistivity of 10 ~ 20 Ω–cm resulting in the high quality inductors compared to those made on the standard CMOS processes. The thick metal layer that comes with the state of the art SiGe technologies also improves the inductor performance. This makes the SiGe BiCMOS an attractive alternative for the high frequency VCO design, where both high speed active and high–Q passive devices are needed.

In this chapter, the feasibility of the LC VCO operated at V–band is studied. A dual band 52 GHz/104 GHz MMW LC VCO using IBM BiCMOS–6HP technology is designed. The oscillation frequency is as high as 52 GHz/104 GHz with the best

performance, a tuning range of 1.05 GHz, a peak–to–peak buffer output voltage of 1.5 V, and the low phase noise of –117 dBc/Hz at 600 kHz offset frequency for 52 GHz band, a tuning range of 2.1 GHz, a peak–to–peak buffer output voltage of 0.5 V, and the low phase noise of –101 dBc/Hz at 600 kHz offset frequency for 104 GHz band.

7.1 MMW Complementary LC VCO

A fully integrated MMW LC VCO is shown in Fig.7.1. The complementary cross–coupled LC VCO is chosen because of its advantages mentioned in Chapter 2. The bipolar transistor is employed as the tail transistor in this topology to improve the phase noise performance of the VCO, because the flick noise of the bipolar is 10 dB lower than that of the MOS transistor [46]. The differential buffer is utilized to amplify the amplitude of the differential output and suppress the noise from the oscillator to the next stage circuit in the RF application.

The complementary cross–coupled LC VCO operates as a switch as presented in Chapter 3. Such switching process is periodical throughout the operation of the VCO. According to the equivalent circuit of the LC oscillator as shown in Fig.3.2, the oscillation frequency f_0 is decided by equation (2.33). In order to sustain the oscillation, the in–equality $R_{tank} \geq |R_{active}|$ must be satisfied. Thus, based on the optimization methodology for phase-noise in Chapter 3, the active devices sizes are decided. R_{tank} is the effective resistance which includes the tank parallel resistors, R_p, of the parasitic resistor, $R_{L,s}$, of the inductor series resistor, $R_{var,s}$, of the varactor series resistor at the oscillation frequency, f_0.

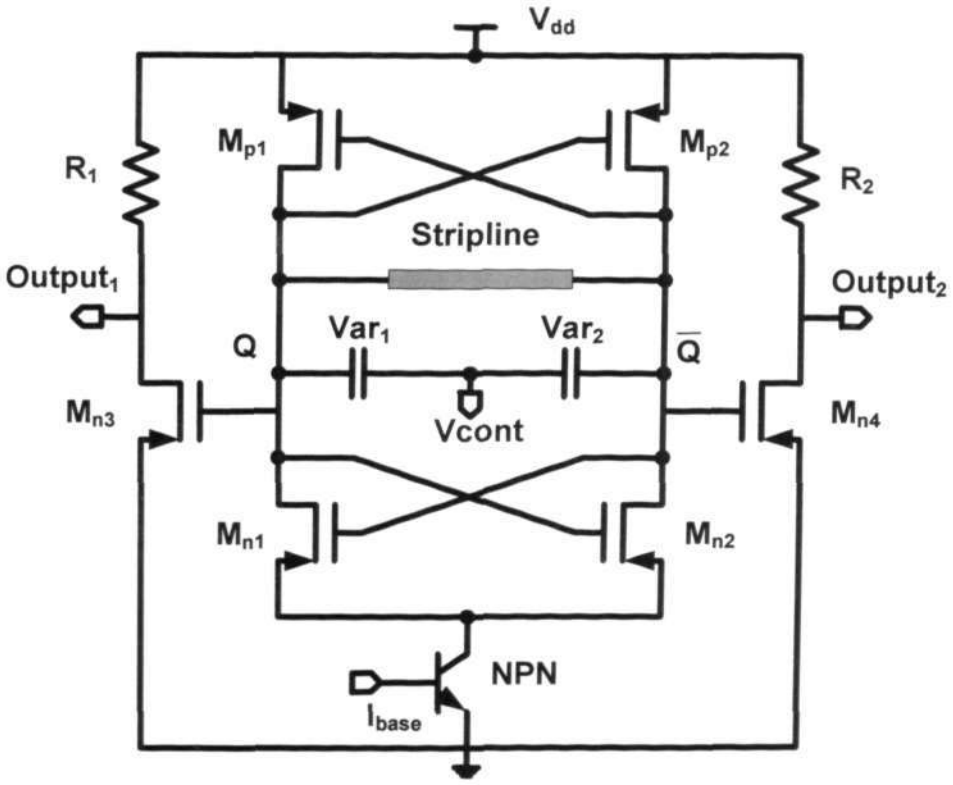


Fig. 7.1 Topology of the MMW complementary LC VCO.

The high–Q inductor and the varactor are the most critical elements in a VCO design when a low phase noise is desired. However, due to the skin effect at microwave frequencies, the inductor Q value and the self–resonation frequency are reduced, thus, the targeted oscillation frequencies are shifted. In order to address these issues, the IBM BiCMOS–6HP process is chosen in our design for the following advantages [94]:

(1). Its high resistive substrate reduces the Eddy currents and the thick metallization minimizes the skin effect. These features make it possible to obtain Q values of around 20 for the inductors at the operation frequency.

(2). It offers the transmission line inductors with the deep trench isolation further improving the inductor Q values, and hence the oscillation frequency above 51 GHz with low phase noise is feasible.

(3). The bipolar tail transistor schematized in Fig.7.1 can be realized together with the CMOS circuit in the SiGe BiCMOS process.

7.2 SiGe Integrated Inductor Line and MOS Varactor

7.2.1 Inductor Line (Microstrip Line)

One of the key components for designing a low phase noise oscillator is the high–Q inductor. Unlike capacitors, inductors are not readily available in a standard CMOS technology. As a result, some design techniques have to be using, those usually limit the performance of an inductor. The active inductors could be very advantageous in the high frequency operation for the VCOs. However, the noise generated by the active elements requires the use of an excessive amount of power [95] [96]. Recently, an inductor of a folded bondwire has been proven to have low series resistance and it is readily available in any IC technology. The semiconductor industry is still hesitant to use this technique because the manufacturers cannot guarantee the repeatability of the bonding process. Currently, various spiral–shaped inductors have been designed and fabricated on the silicon substrate using one or more metal interconnection levels. However, the inductor Q value is limited by the series resistance of the metal traces and the substrate loss.

For frequency around 50 GHz, microstrip line inductors are used as they can provide the required low inductances at high–Q value, The IBM BICMOS–6HP technology

offers a set of microstrip line inductors with an additional deep trench layer underneath the inductor lines to enhance the Q values further.

Fig.7.2 shows L and Q values of the microstrip line inductor and the spiral inductor versus frequency, both aiming for a 50 pH inductance at an operation frequency of 54 GHz. A simple microstrip line inductor exhibits a 50.6 pH inductance and a Q value of 28. Unfortunately, the smallest spiral inductor available in the IBM library is 160 pH. The 50 pH inductance can be obtained by paralleling three spiral inductors of 160 pH, but the space is 5 times bigger than that of the microstrip line inductor and the Q value is only 7. The feasibility of the high frequency and low phase noise LC VCO will be based on the superiority of the microstrip line inductors.

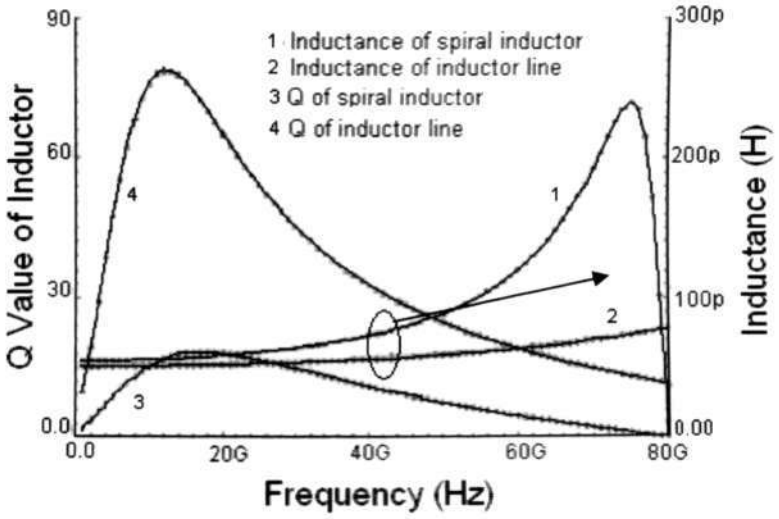


Fig. 7.2 Comparison of inductance and Q between transmission line and spiral inductor at 50 GHz.

7.2.2 MOS Varactor

A varactor diode, which is formed by an intrinsic pedestal NPN collector–base diode, is offered by IBM BiCMOS–6HP technology. The C_{max}/C_{min} ratio is about 12 for this

structure, but Q of the varactor is less than 8 at 53 GHz. The simulated capacitance and Q value versus the controlled voltage are presented in Fig.7.3.

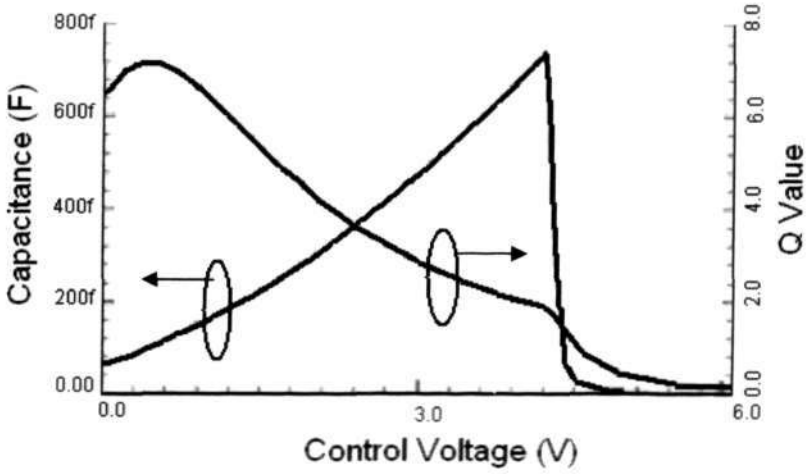


Fig. 7.3 Capacitance and Q value of diode varactor versus control voltage.

The IBM BiCMOS–6HP process also offers an nMOS varactor with a higher Q value, which is suitable for realizing small capacitances for the high frequency VCO. The capacitance and Q are shown in Fig.7.4 at the operation frequency of 54 GHz. A nMOS varactor (MOS Varactor) uses a thin oxide nFET in an N–well with the N+ source and drain shorted together. The variable capacitance is achieved by controlling the gate to the diffusion/N–well potential within the range from –0.7 V to 1.0 V, which drives the device from the depletion to the accumulation. The capacitance per unit area can be varied from C_{max} (5.8 fF/μm^2) to the value of 40% of C_{max} over this range. There is also a slight dependence on the channel width and length. At the gate to the source–drain voltage (Vg–sd) below –0.7 V and above 1.0 V, a depletion region in the gate polysilicon layer starts to grow, leading to a reduction in the capacitance. The device is found to be

robust for Vg–sd from –1 V to +1 V as illustrated in Fig.7.4. The C_{max}/C_{min} ratio is about 2, but Q value is more than 45.

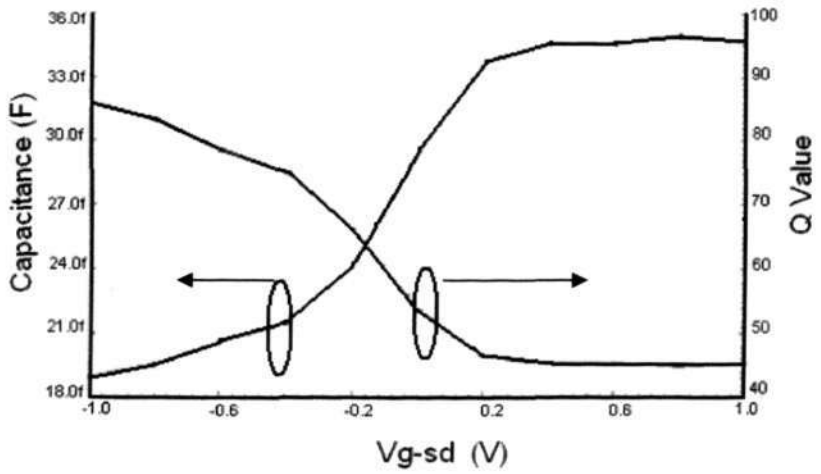


Fig. 7.4 Capacitance and Q versus Vg–sd for MosVaractor at the operation frequency of 54 GHz.

7.3 Effects on Implementation for 52GHz MMW LC VCO

The microstrip line inductor (also called inductor line) and the MosVaractor are used in the tank configuration. A pair of coupled nMOS transistors (M_{n1} and M_{n2}) and a pair of coupled pMOS transistors (M_{p1} and M_{p2}) are used in the positive feedback to provide a negative resistance. The other nMOS pair (M_{n4} and M_{n5}) with two 50 Ω resistors (R_1 and R_2) forms the buffer, the resistor of 50 Ω is adopted for matching during doing the measurements.

From the equivalent circuit of the complementary cross coupled VCO as given in Fig.5.1 (b), the capacitance of the tank (C_{tank}) at one of the output node of the core circuit is expressed by the following equation [45]:

$$C_{tank} = C_{var} + \frac{C_{nmos} + C_{pmos}}{2} \tag{7.1}$$

Where, C_{var} is the capacitance of a MosVaractor. The capacitance value of 23 fF with the Q value of 50 can be obtained from the capacitance extraction of the MosVaractor at the operation frequency of 54 GHz in Fig.7.4. C_{nmos} and C_{pmos} are the capacitances of nMOS and pMOS devices as described in a MOSFET small–signal model in Fig.7.5 [97]. C_{gs}, C_{gd} and C_{db} are the well–known capacitances associated the devices, and they impact the capacitance of the tank to cause the frequency of oscillator shift directly. The overall capacitance is calculated approximate as C_{tank} = 340.8 fF, in which the main capacitances of MOSFET, C_{gs}, C_{gd} and C_{db}, are calculated by (7.2), (7.3) and (7.4) respectively [97]:

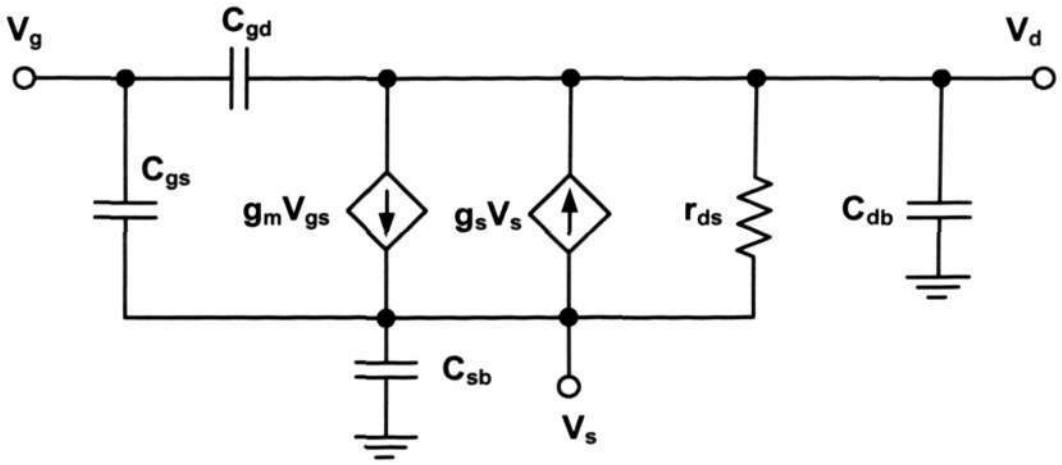


Fig. 7.5 MOSFET small–signal model at active region.

$$C_{gs} = \frac{2}{3} W_c L_c C_{ox} + W_c L_{ov} C_{ox} \tag{7.2}$$

$$C_{gd} = W_c L_{ov} C_{ox} \tag{7.3}$$

$$C_{db} = A_d C_{jd} + P_d C_{j-sw} \tag{7.4}$$

Here L_c and W_c are the effective gate length and width of the MOSFET, L_{ov} is overlap distance between gate and source/drain, and it is usually empirically derived. C_{ox}

is the gate oxide capacitance per unit area and given as $C_{ox} = \frac{K_{ox}\varepsilon_0}{t_{ox}}$, here, K_{ox} is the relative permittivity of SiO_2 (approximately 3.9) and t_{ox} is the thickness of the thin oxide under the gate. A_d and P_d are the drain area and perimeter respectively.

The inductance of the tank, L=50.6/2=25.3 pH with Q = 38, was determined from Fig.7.2 at the operation frequency of 54 GHz. The oscillator frequency, f_0 = 54.04 GHz is achieved for V_{cont}=2.4 V. To verify the calculated frequency, the VCO is simulated using Cadence SpectreRF Simulator for pre–layout schematic given in Fig.7.1 at the same controlled voltage, the simulation result is 54.08 GHz, which is in a good agreement with the theoretical calculation.

7.3.1 Tail Transistor

The bipolar tail transistor is used to improve the phase noise and to supply a constant current into the tank for the stable oscillation. Thus, the phase noise of LC VCOs with nMOS tail (nMOS–T) and bipolar tail transistor (Bipolar–T), respectively, is investigated at 53.5 GHz and the result is presented in Fig.7.6. The phase noise of the VCO with the Bipolar–T at 100 KHz offset frequency is 3 dB better than that of the VCO with nMOS–T. The bipolar tail transistor is also adopted in the design of the dual band LC VCO later.

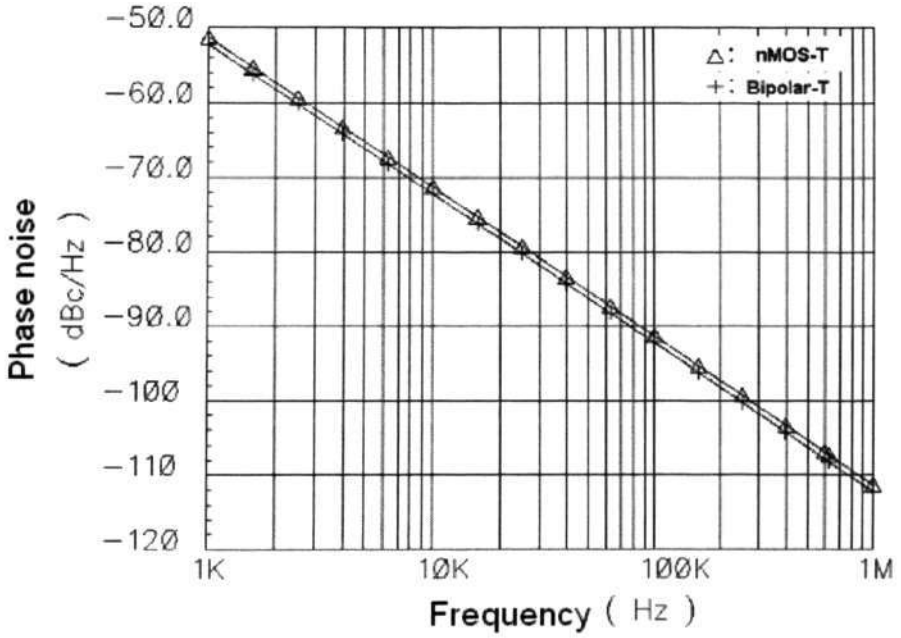


Fig. 7.6 Comparison of phase noise of the VCO with nMOS tail transistor and with bipolar tail transistor.

7.3.2 Cut–Off Frequency (f_T) of the MOSFET

The active device speed is also another concern for the high frequency operation. The single device gain cut–off frequency, f_T ($\omega_T = 2\pi f_T$), may sometimes be misleading. Expressed by $f_T = \frac{1}{2\pi}\frac{g_m}{(C_{gs}+C_{gd})}$, can be doubled for a differential transistor structure [46]. The fully complementary cross–coupled VCO topology is a differential structure where the gate–source and gate–drain capacitors that are viewed by each transistor, $C_{gs}+C_{gd}$, are reduced to be half that of a single transistor in (7.1). Hence, even though the cutoff frequency of the nMOS transistor is 55 GHz for the IBM BiCMOS–6HP technology [94], it is still possible to design an LC VCO that can operate above 100 GHz

because the cut–off frequency is doubled to 110 GHz when the complementary structure is utilized.

The relation between ω_T and ω_{max} for a source resistance of the transistor (R_{se}) much smaller than the effective gate resistance of the transistor (R_{ge}) can be given by [46]:

$$\omega_{max} \approx \frac{\omega_T}{\sqrt{4R_g(g_{sd} + \omega_T C_{gd})}} \tag{7.5}$$

where g_{sd} and C_{gd} are the source–drain transconductance and gate–drain capcictance, respectively. From equation (7.5), ω_{max} will, to first order, increase with ω_T. Thus, ω_{max} for a differential pair is higher than that of a single transistor, which shows that it is possible for a complementary cross–coupled LC VCO to operate beyond ω_{max} of a single transistor when the differential architecture is utilized.

7.3.3 Parasitic Extractions and the Optimizing Layout Technologies

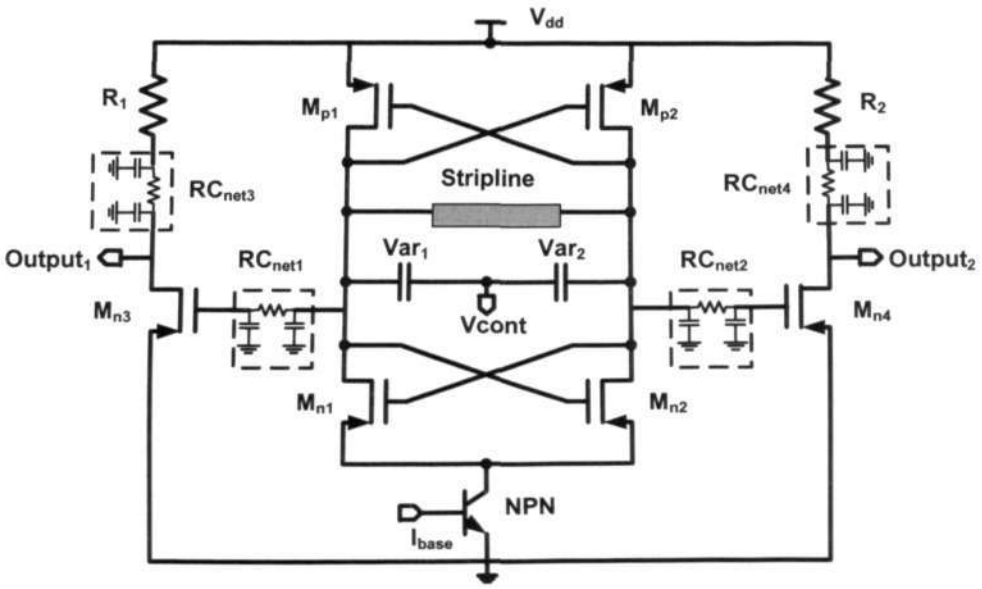


Fig. 7.7 Schematic of the VCO with parasitic components.

The parasitic components due to the interconnects and the devices in the layout affect the operation of the real circuit, usually degrading the performance. Parasitic coupling is inevitable, but it can be minimized by a carefully layout drawing. The parasitic capacitances and resistances are extracted, and the schematic is modified accordingly using special components, RCnet, to represent the extracted parasitics as presented in Fig.7.7. The effects of these parasitic components (RCnet) on the VCO performance are investigated.

Two connects of critical nodes have high parasitic effects: the connection of the output buffer transistor's gate and the VCO core (the cross–coupled nMOS transistor's drain terminal), i.e. RCnet1 and RCnet2. These parasitic components shift the operation frequency. The second critical connection is the one between a resistor of 50 Ω and the drain of the buffer transistor, i.e. RC_{net3} and RC_{net4}. The amplitude of the output voltage is reduced due to the parasitic resistances at this point. The layout is optimized as much as possible to obtain the minimum parasitic components at the nodes. The effects of those parasitic components on the oscillation frequency are given in Fig.7.10 and the phase noise degradation is presented in Fig.7.11.

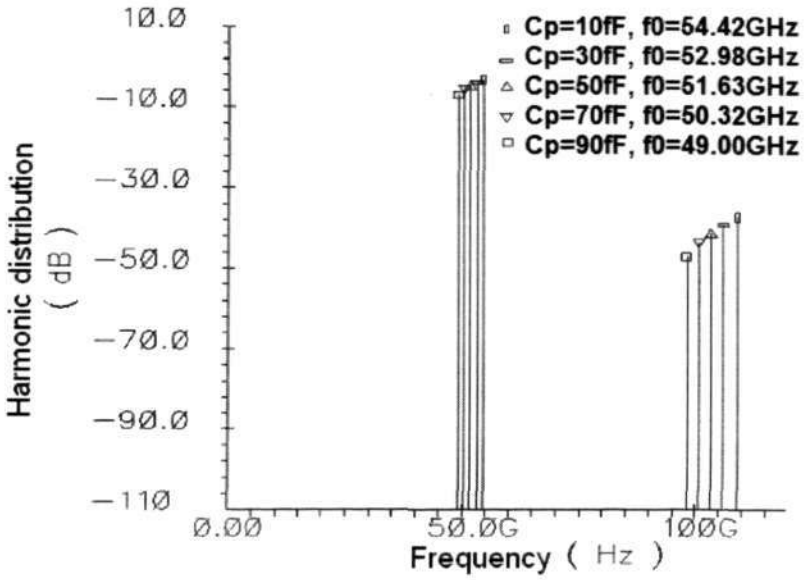


Fig. 7.8 Effects of the parasitic capacitance on the fundamental frequency and the second harmonic.

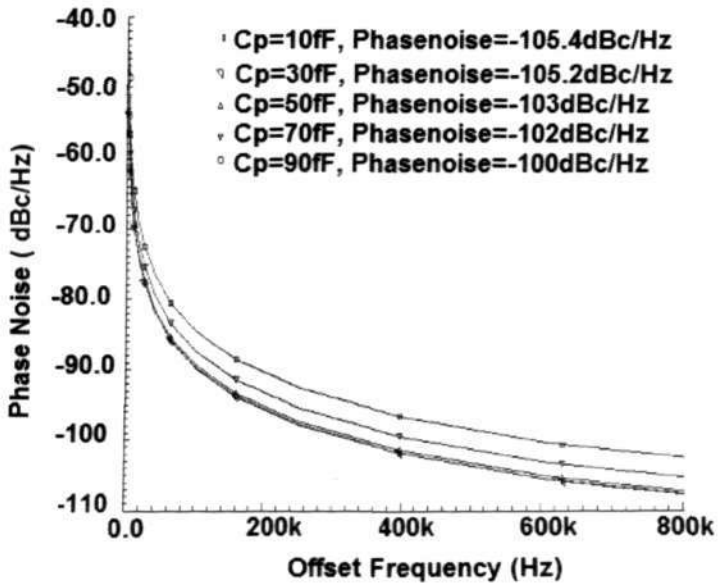


Fig. 7.9 Effects of the parasitic capacitance on the phase noise .

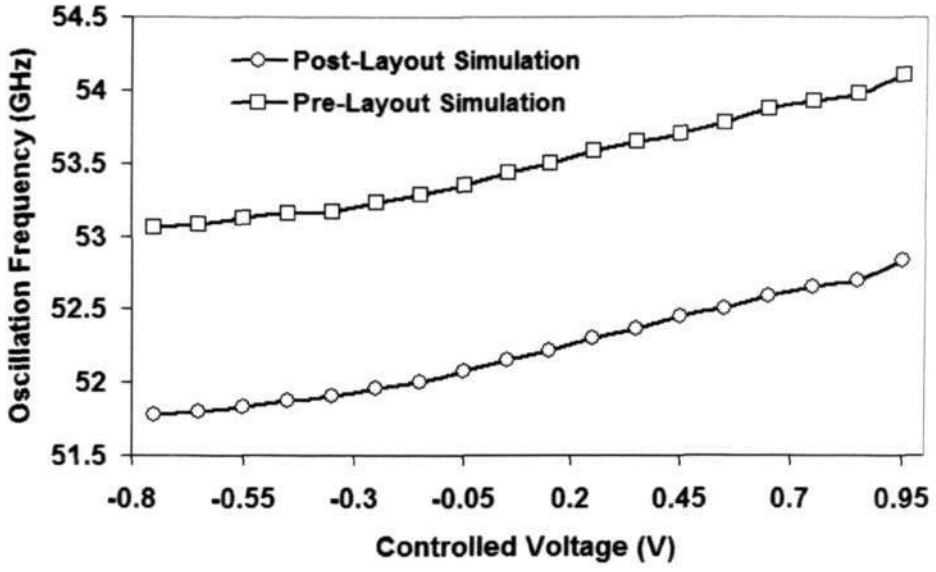


Fig. 7.10 Tuning characteristics of the VCO.

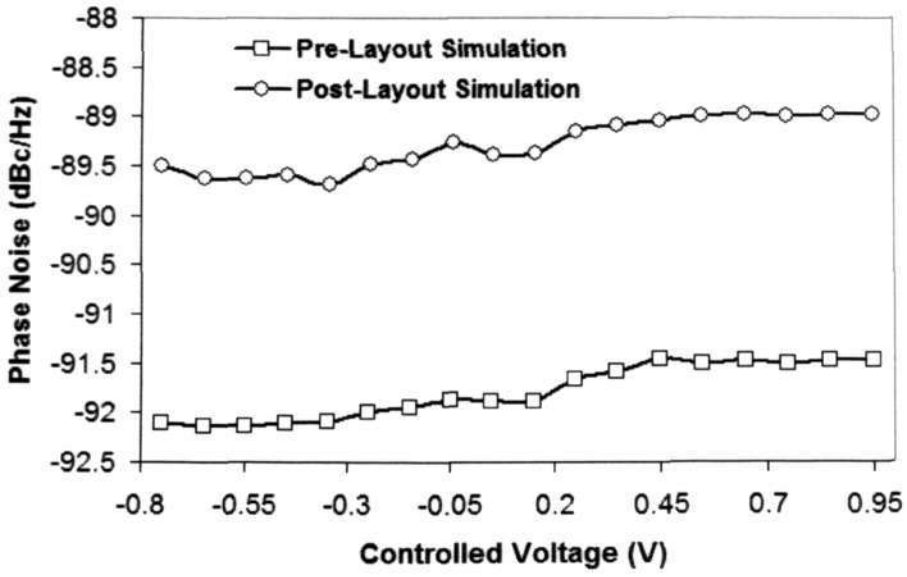


Fig. 7.11 Phase noise performance of the VCO.

The maximum oscillation frequency is lowed by 5 GHz, and the phase noise is increased by 5 dB/Hz at 600 kHz frequency offset when the parasitic capacitance (at $RCnet_1$ and $RCnet_2$) increases from 10 fF to 90 fF. The frequency tuning range also suffers slightly from the parasitics, and it is reduced by 150 MHz. Therefore, the parasitic components can be minimal even though it is unavoidable for RF IC Designer.

7.3.4 Comparison of the Pre–Layout Simulation and the Post–Layout Simulation

Based on above considerations, the optimized layout of the LC VCO is presented in Fig.7.12. The parasitic components "RCnet" are extracted and the post–layout simulation is done. The comparisons between the pre–layout and the post–layout simulation are demonstrated in Fig.7.10 and Fig.7.11. The maximum oscillation frequency is shifted down 1.28 GHz (from 54.11 GHz to 52.83 GHz), the phase noise is degraded by 2.5 dBc/Hz at 100 kHz offset frequency (from −91.48 dBc/Hz to −88.98 dBc/Hz at 100 kHz offset frequency away from the maximum oscillation frequency).

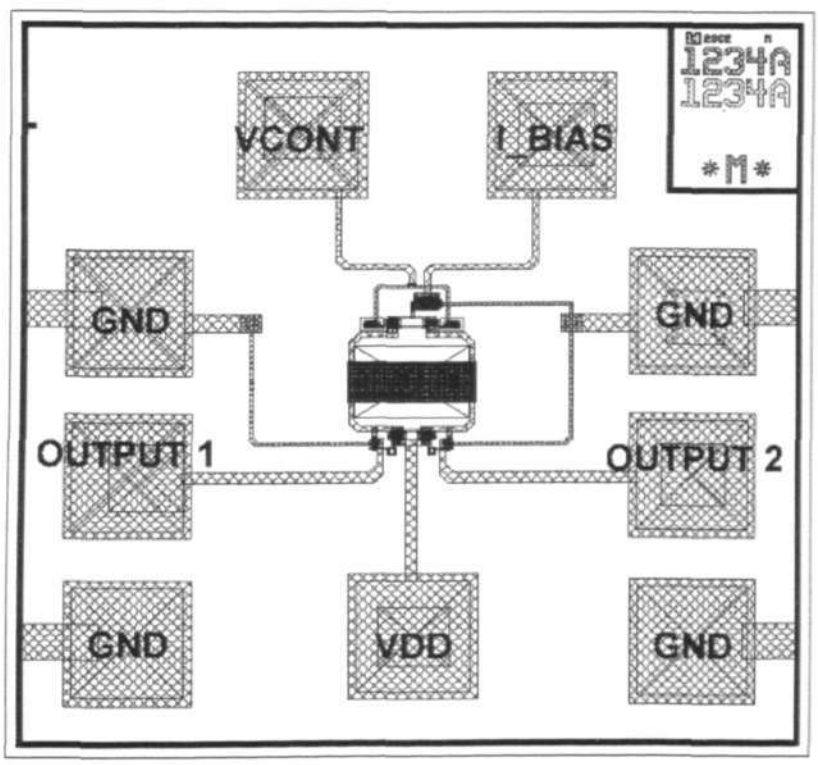


Fig. 7.12 Layout for 52 GHz.

A 52 GHz complementary cross–coupled LC VCO is designed, simulated and implemented on the IBM BiCMOS–6HP process. The power consumption of the VCO

core is 9 mW and the total power consumption including the buffer is about 15 mW. The VCO can be tuned from 51.78 GHz to 52.83 GHz with the tuning range 1.05 GHz, and the phase noise is about −91.88 dBc/Hz at 100 kHz offset frequency, −107.3 dBc/Hz at 600 kHz offset frequency and −111.7 dBc/Hz at 1 MHz offset frequency at the operation frequency of 52 GHz from the post−layout simulation respectively as shown in Fig.7.10 and Fig.7.11. To the best of my knowledge, this is the highest oscillation frequency with the best performance for a fully integrated LC VCO using a commercial BiCMOS technology at the time. The layout of the designed VCO is given in Fig.7.12 and the performance is summary in Table 7.1.

Table 7.1 Summary of VCO performances.

VCO Design	Complementary Cross−Coupled	
	Pre−layout	Post−layout
Maximum frequency	54.11 GHz	52.83 GHz
Phase noise @ 100KHz	−91 dBc/Hz	−89 dBc/Hz
Tuning range*	1.05 GHz	1.05 GHz
Tuning %	1.9	2.0
Max. output	1.6 Vp−p	1.5 Vp−p
Supply voltage	2.5 V	
Power consumption without buffer	9 mW	
Power consumption with buffer	15 mW	
Chip area without buffer	120 x 152 μm^2	
Chip Area with buffer	600 x 610 μm^2	

7.4 Design of the Frequency Harmonic Circuit

7.4.1 Harmonics of the Differential Signals

A VCO shows a strong nonlinear effect due to the large output swing in the resonator. Since the nonlinear effect is related to many different physical phenomena, it can not be modeled easily. Thus, the nonlinearity is modeled with polynomials empirically. The output of a VCO is modeled by [35]:

$$V_{out} = A_0 + A_1 X + A_2 X^2 + A_3 X^3 + \cdots\cdots \tag{7.6}$$

where A is the harmonic coefficients and X is the input signal. Here it is assumed: $X = \cos(\omega t + \theta)$, then equation (7.6) is rewritten by:

$$\begin{aligned} V_{out} &= (A_0 + \frac{A_2}{2} + \frac{A_4}{2}) + (A_1 + \frac{3}{4}A_3)\cos(\omega t + \theta) \\ &+ (\frac{A_2}{2} + \frac{A_4}{2})\cos(2\omega t + 2\theta) + \frac{A_3}{4}\cos(3\omega + 3\theta) + \cdots\cdots \end{aligned} \tag{7.7}$$

The above equation shows that the phase of the N^{th} harmonic is raised to N times. A differential VCO has two outputs, whose phases difference is 180°. Therefore, we have:

$$V_{out}\cos(\omega t) + V_{out}\cos(\omega t + \pi) \approx 2(A_0 + \frac{A_2}{2}) + A_2\cos(2\omega t) + \cdots\cdots \quad \text{or}$$

$$V_{out}\cos(\omega t - \frac{\pi}{2}) + V_{out}\cos(\omega t + \frac{\pi}{2}) \approx 2(A_0 + \frac{A_2}{2}) + A_2\cos(2\omega t + \pi) + \cdots\cdots \tag{7.8}$$

From equation (7.8), we note that the fundamental frequency components are canceled out and the harmonic frequencies are obtained theoretically. The exact 180° phase difference and the same power are required to cancel out the fundamental frequency. Thus a buffer is necessary to amplify the harmonic in generally.

7.4.2 Implementation of the Dual Band LC VCO

From the above theory, a 52/104 GHz dual–band oscillators is shown in Fig.7.13, which comprises a MMW complementary LC VCO designed in the last section and a harmonic frequency circuit (also namely, frequency doubler) formed by a differential NMOS pairs. The differential output (Q and $\overline{Q}$) of the complementary cross–coupled LC VCO connect to a differential buffer which consists of M_{n3} , M_{n4} and R_1=R_2=50 Ω as given in Fig.7.1, to forms the first output band, namely differential end ($Output_1$ and $Ouput_2$). At the same time, the differential outputs (Q and $\overline{Q}$) input the signal to the frequency doubler, the drains of the differential NMOS pairs (M_{n5} and M_{n6}) are connected together with an inductor (L) to form the second output through the node "$Node_m$" as in Fig.7.13. Similarly, a single end buffer consisted by M_{n7} and R_3=50 Ω are connected to the node "$Node_m$" to output the second band. Because the node "$Node_m$" is pulled up when each of the differential NMOS transistors turns on, the node "$Node_m$" moves at twice of the frequency of the differential output, just like the derivation in equation (7.7). Therefore, the frequency at $Output_3$ has a second harmonic frequency, which doubles the oscillation frequency of the MMW complementary LC VCO.

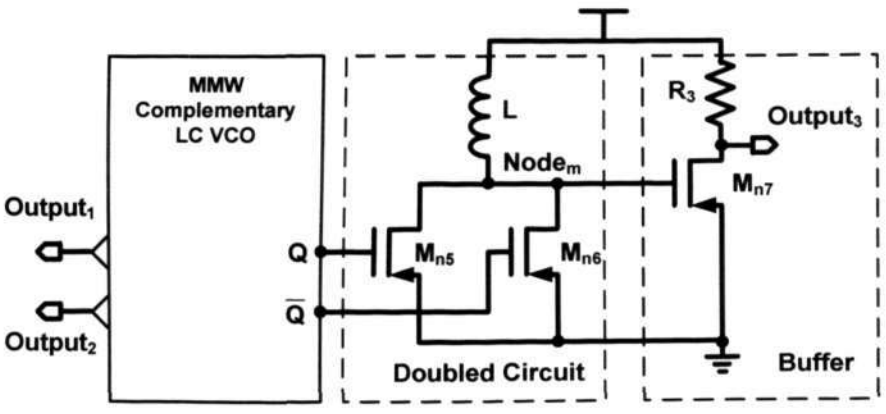


Fig. 7.13 Dual band LC VCO.

Two buffer circuits are used for the output because of the following advantages: 1) To amplify the amplitude of the output ($Output_1$, $Output_2$ and $Output_3$), 2) To match the 50 Ω for the exact measurements, 3) To isolate the noise from the previous stages. The transient simulation results of the doubled frequency circuit for the post–layout are shown in Fig.7.14. The output amplitude of the first band (52 GHz) is around 1.5 V and the second band (104 GHz) is around 0.5 V.

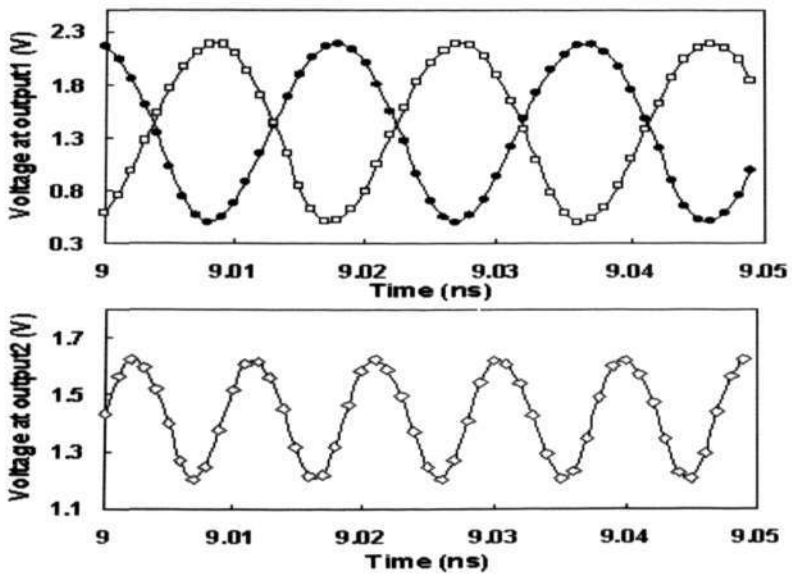


Fig. 7.14 Transient output for the dual–band VCO.

7.4.3 Simulation Results of the Dual Band MMW LC VCO

The simulation results for the dual band MMW LC VCO was presented in Fig.7.15, which gives the tuning range from 51.78 GHz to 52.83 GHz for the 52 GHz–band. The corresponding tuning ratio is 2%. The tuning range for the 104 GHz–band at the single output is from 103.46 GHz to 105.66 GHz, which corresponds to two times of the differential–end frequencies.

The phase noise performance of the dual–band VCO is simulated for the post–layout as given in Fig.7.16. For 52 GHz–band, the phase noise is –91.88 dBc/Hz at 100 kHz offset, –107.3 dBc/Hz at 600 kHz offset, –111.7 dBc/Hz at 1 MHz offset and –121 dBc/Hz at 3 MHz offset. For 104 GHz–band, the phase noise is around –85.3 dBc/Hz at 100 kHz offset, –101.44 dBc/Hz at 600 kHz offset, –105.9 dBc/Hz at 1 MHz offset and –115.1 dBc/Hz at 3 MHz offset. However, the phase noise of the 104 GHz–band is around 6 dB drop for 52 GHz band because of the harmonic frequency circuit, in which the sideband noise and spurious are increased by a factor of 2. The result is that the phase noise increased by 20log2 = 6 dB. The power consumption of the dual band VCO is about 22 mW with 2.5 V supply. The simulation results are summarized in Table 7.2. The phase noise performance is around 10 dB higher than those of previously reported VCOs [89] [98] [99]. The output spectrum for the 104 GHz band is shown in Fig.7.17.

Table 7.2 Performance summary of the dual–band 52/104GHz VCO.

Performance	This work (Simulated)		Reference		
Oscillation frequency (GHz)	52	104	47 [89]	38 [98]	62 [99]
Supply voltage (V)	2.5	2.5	5.5	3.5	2.5V
Phase noise @ Δf =1 MHz (dBc/Hz)	–111.7	–105.9	–108	–108	–104
Power consumption (mW)	15	22	280	NIL	NIL
Tuning range (GHz)	51.7 – 52.8	103.4 – 105.6	43.6 – 47.3	38.0 – 38.8	62.2 –62.5
Second harmonic distortion (dB)	–24.7	–36.65	NIL	NIL	NIL
Oscillation amplitude (Vp–p)	1.8	0.5	0.85	NIL	NIL
Technology @ materials	SiGe		SiGe	AlInAs /InGaAs	InP based HBT

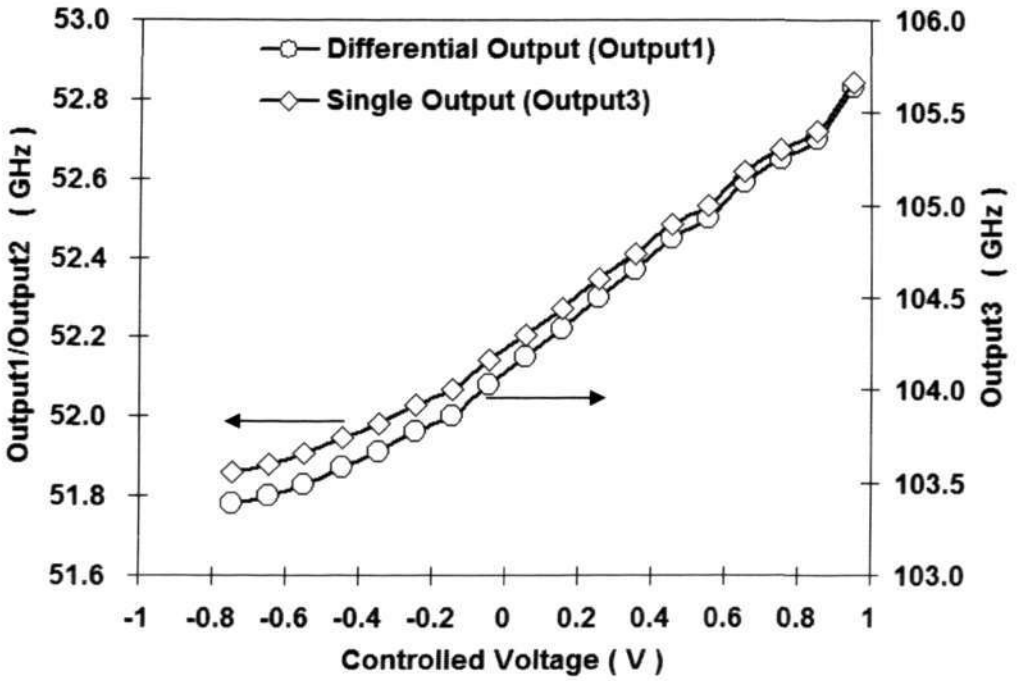


Fig. 7.15 Two output frequency versus to the controlled voltage.

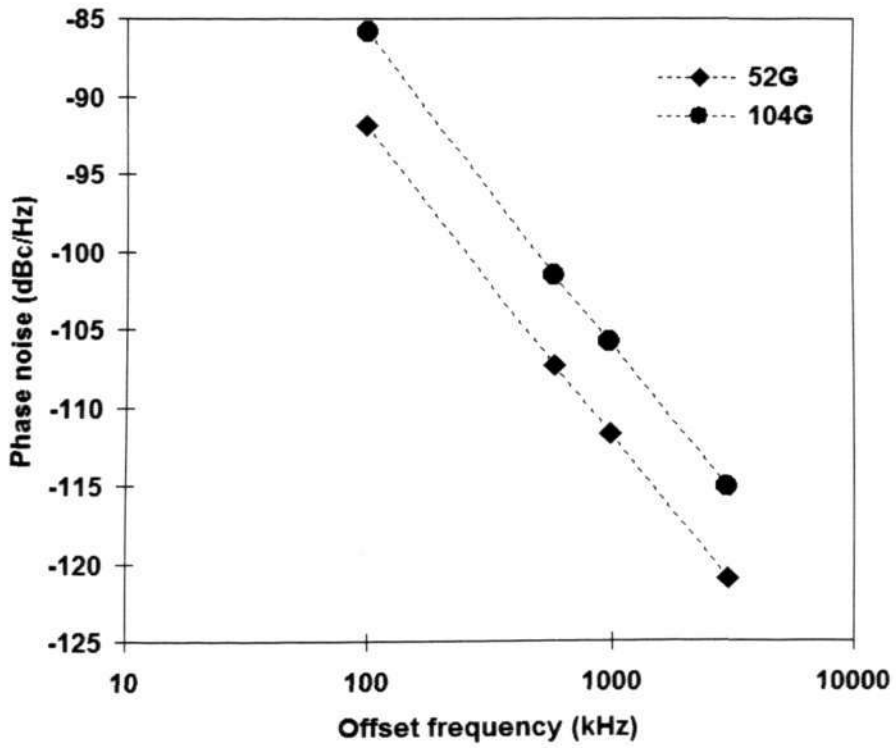


Fig. 7.16 Phase noise performance of the dual–band VCO.

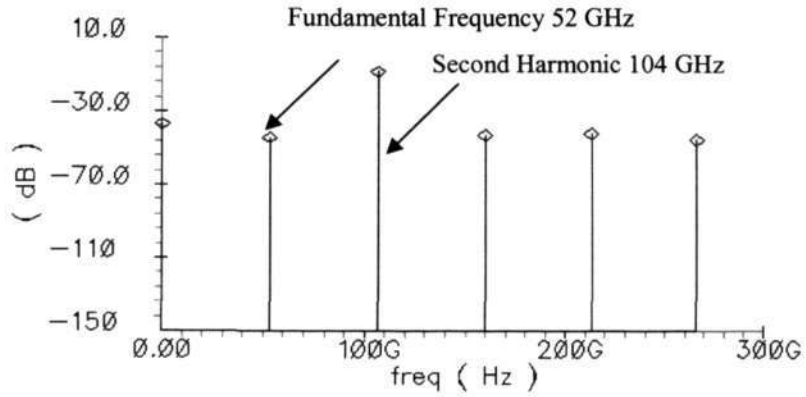


Fig. 7.17 Frequency spectrum of the harmonic components of the 104 GHz VCO.

7.5 Conclusion

A dual band MMW LC VCO operating at the frequencies of 52/104 GHz with good performance, low phase noise of −107.3 dBc/Hz at the 600 kHz offset frequency, low power consumption of 15 mW and a frequency tuning range of 1.05 GHz for 52 GHz–band, low phase noise of −101.4 dBc/Hz at the 600 kHz offset frequency, low power consumption of 22 mW and 2.1 GHz tuning range for 104 GHz–Band, is achieved by using the commercial IBM BiCMOS–6HP technology with the cutoff frequency of 55 GHz for MOSFET. It is possible to design a LC VCO with the above 100 GHz operation frequency. Fully integrated above 50 GHz VCO is the crucial block in SONET systems operating at speeds higher than 40 Gb/s and in the application of the satellite communication operating at V–band. The above 100 GHz VCO has wide applications in military utilization.

CHAPTER 8

Conclusions and Recommendations

8.1 Conclusions

This thesis describes methods to design LC VCOs with low phase noise and low power consumption and the design of a fully integrated frequency synthesizer with the high accurately frequency in the channel selection.

In Chapter 2, we reviewed the fundamentals of a frequency synthesizer and VCO. Firstly, the basic knowledge of a PLL based frequency synthesizer is introduced, the performance impacts caused by the phase noise and spurious tone were studied, and the dynamic parameters of the loop were introduced. Secondly, the operation theory of LC VCOs was introduced. The existing phase noise models were summarized. The advantages and disadvantages of the existing models were investigated. The direct optimization methodology to design LC VCOs with the low phase noise is necessary for the designers.

In Chapter 3, a methodology that achieves the minimal phase noise of the cross–coupled LC VCO was proposed. The fundamental relationship between the gate length and the thermal noise of the active devices used in the cross–coupled LC VCO was derived. An optimization gate length was achieved for the minimal phase noise of the LC VCO. This results in the minimal phase noise which is obtained by using the optimized gate length of the active devices. The steps to optimize the phase noise

performance of the LC VCO were summarized. It is very useful for the RF IC designer and also suitable for the other differential LC VCOs.

In Chapter 4, the proposed methodology was verified by two designs. One is a 2 GHz cross–coupled LC VCO, which had been designed and fabricated by CSM 0.18 μm technology. The measured phase noise performance is −103.3 dBc/Hz at 100 kHz offset frequency, −118.9 dBc/Hz at 600 kHz offset and −128 dBc/Hz at 3 MHz offset away from the carrier frequency of 1.968 GHz. The power consumption is 3.15 mW. The FoM is 186. The tuning range is 1.1 GHz from 9.3 GHz to 10.4 GHz. The VCO has a low phase noise of −89 dBc/Hz at 100 kHz offset, −110 dBc/Hz at 600 kHz offset from the carrier frequency of 9.83 GHz. It is designed and fabricated by using CSM 0.18 μm technology. The power consumption of the circuit is 5.8 mW, and the output peak–to–peak voltage is around 1.1 V. The design is intended for the 10–Gb/s Clock and Data Recovery IC used in the SONET communication application.

In Chapter 5, a methodology to find the relationship between the loop parameters and the noise transfer functions had been proposed. Based on the noise distribution model in the CPLL, three noise transfer functions in z–domain, namely, the input noise transfer functions, the noise transfer function from the loop filter and the noise transfer function from the VCO phase noise, were derived and simulated by using the behavioral model. A noise peak exists in the loop and the loop filter has no capability to depress it when the loop bandwidth is comparable with the reference frequency. The noise peak also causes the system to be unstable, which can be detected by the z–domain analysis only. The stability margin, which is dependent on the phase margin and the ratio of the reference frequency to the loop bandwidth, has been obtained and verified by the behavioral model

of RFHDL in Cadence. The proposed approach provides a useful insight into the investigations to derive the phase noise transfer functions.

In Chapter 6, we demonstrate a design of a fully integrated monolithic CMOS 2.45 GHz frequency synthesizer, which is designed for Bluetooth applications. The integer–N pulse swallow programmable divider with the division ratio ranges from 2402 to 2480, which employed a dual–modulus prescaler (divide–by–32/33), was utilized. A simulated phase noise performance of –112 dBc/Hz at the offset frequency of 3 MHz was achieved. The spurious tone is degraded to –68 dBc at the offset frequency of 1 MHz. The power consumption is brought down to 31 mW and the output peak–to–peak voltage is 1.4 V. The tuning range is from 2.4 GHz to 2.4835 GHz. The proposed frequency synthesizer was developed using CSM 0.18 μm CMOS technology, and the die area is 1.2×1.5 mm^2.

In Chapter 7, the design of a dual band 52 GHz/104 GHz MMW LC VCO is described. The post-layout simulation shows low phase noise of –107.3 dBc/Hz at the 600 kHz offset frequency, low power consumption of 15 mW, and a frequency tuning range of 1.05 GHz for the 52 GHz–band. The results also shows low phase noise of –101.4 dBc/Hz at the 600 kHz offset, low power consumption of 22 mW and a 2.1 GHz tuning range for the 104 GHz–Band. The design is achievable for the commercially IBM BiCMOS–6HP technology with f_T of 55 GHz. It is possible to design an LC VCO with an operating frequency higher than the cutoff frequency.

8.2 Recommendations

The dual band 52 GHz/104 GHz MMW LC VCO using the IBM BiCMOS 6HP technology should be fabricated and measured in order to verify the design.

The phase noise performance of a frequency synthesizer depends greatly on the phase noise performance of the VCO. With a proper design, noise from the active device in the VCO can be minimized as discussed in Chapter 4. Indeed, the active devices are present only to replenish the lost energy in the resonant tank. They cannot improve the overall Q of the circuit. It has been shown that a substantial improvement in the phase noise can be achieved by implementing a resonant tank with a high Q [100]. In the literatures [100], it has been shown that the Q of the inductor could, in theory reach about 100 for a gold bond-wire inductor. However, this method is costly and it is susceptible to the effect of the contact resistance and other parasitics, which will reduce the Q value significantly. Another method for improving the Q value of the resonant tank is through a crystal–like inductance–capacitance tank [101]. However, this does not help to improve Q because of the requirement that all inductors must be integrated on–chip. More work has to be done in order to provide a resonant tank with a high Q that can be easily integrated using a standard commercial process.

The power dissipation of the muti–modulus divider dominates that of the frequency synthesizer, further reduction of the frequency synthesizer power consumption must begin with this component. A promising avenue is to use alternative technologies, such as advance CMOS processes, to achieve the high speed requirements of the divider circuits at low power levels. From an architectural standpoint, new topologies can be examined for the divide–by–2 stages in the divider. Some interesting possibilities include the use of inductors to resonate out load capacitance, or entirely different structures such as dynamic frequency dividers [102].

PUBLICATION LIST

Published Journal Papers

(1).**Lin Jia,** Jianguo Ma, Kiatseng Yeo, Manhanh Do, "9.3–10.4 GHz–Band Cross–Coupled Complementary Oscillator with Low Phase noise Performance," *IEEE Transaction on Microwave Theory and Techniques*, Vol.52, No.4, pp.1273 – 1278, April 2004.
(2).**Lin Jia,** Jianguo Ma, Kiatseng Yeo, Xiaopeng Yu, Manhanh Do and Weimeng Lee "A 1.8-V 2.4/5.15-GHz Dual-Band LC VCO in 0.18 μm CMOS Technology," *IEEE Letter on Microwave Wireless Component*, Vol.16, No.4, pp.194 – 196, April 2005.
(3).**Lin Jia,** Jianguo Ma, Alper Cabuk, Kiatseng Yeo, Manhanh Do, "A 50 GHz VCO with Low Phase noise Implemented in SiGe BiCMOS Technology," *Microwave and Optical Technology Letters*, Vol.39, No.12, pp.414 – 418, Dec. 2003.
(4).**Lin Jia,** Jianguo Ma, Kiatseng Yeo and Manhanh Do, "Novel 53/106 GHz dual–band LC Oscillator implemented in SiGe BiCMOS Technology," *International Journal of Infrated and Millimeter Waves*, Vol. 25, No.1, pp.55–62, January, 2004.
(5). Xiaopeng Yu, Manhanh Do, **Lin Jia**, Jianguo Ma, Kiatseng Yeo, "Design of a low power wide band high resolution programmable frequency divider," *IEEE Transactions on Very Large Scale Integration*, Vol. 13, No. 9, pp. 1098- 1103, Sep. 2005.
(6). Jianjun Gao, Xiuping Li, **Lin Jia**, Hong Wang and Georg Boeck, " Direct Extraction of InP HBT Noise Parameters Based on Noise–Figure Measurement System," *IEEE Transaction on Microwave Theory and Techniques*, Vol.53, No.1, pp.330–335, Jan. 2005.
(7). Ahfatt Tong, Kiatseng Yeo, **Lin Jia**, Chunqi Geng, Jianguo Ma and Manhanh Do, " Simple and accurate extraction methodology for RF MOSFET valid up to 20 GHz," *IEE Proceeding on Circuit Device System*, Vol.151, No.6, pp.587–592, Dec. 2004.

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(1). **Lin Jia**, Jianguo Ma, Kiatseng Yeo, Manhanh Do, "A 51.8 GHz VCO With Low Phase noise Implemented in SiGe BICMOS Technology," *Proceedings of European Microwave Conference & European Wireless Technology Conference*, Oct. 2003, Germany.
(2). **Lin Jia**, Jianguo Ma, Kiatseng Yeo, Manhanh Do, "A Novel Methodology for the Design of LC VCO with Low Phase noise ," *IEEE International Symposium on Circuits and Systems*, Kobe, Japan, May, 2005.
(3). Kaixue Ma, Jianguo Ma, **Lin Jia**, Manhanh Do, and Kiatseng Yeo, "800 MHz~2.5 GHz Miniaturized Multi–layer Symmetrical Stacked Baluns for Silicon Based RF ICs," *IEEE Int. Microwave Symposium* 2005, 12~17, June 2005, Long Beach, CA, USA

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(1). **Lin Jia,** Jianguo Ma, Kiatseng Yeo ,Xiaopeng Yu and Manhanh Do, "A Novel Methodology for the Design of LC VCO with Low Phase noise ," *IEEE Transaction On Circuit& System —II, Analog and Mix Signal Processing.*
(2). **Lin Jia,** Kiatseng Yeo, Jianguo Ma, Xiaopeng Yu and Manhanh Do, "Noise Transfer Characteristics of a Charge–Pump PLL Based Frequency Synthesizer," *IEEE Transaction on Circuit& System —I, Theory and Systems.*

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