# Multiple-Pole Multilevel Diode Clamped Inverter for Permanent Magnet Synchronous Motor Drive

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***Abstract*—A five-level reduced device multilevel inverter is proposed for driving permanent magnet synchronous motor. The proposed multilevel inverter drive consists of lesser number of clamping diodes compared to the conventional five-level diode clamped inverter. An active balancing circuit is used to provide balanced voltages across the four dc-link capacitors to ensure five-level voltage waveform in all operating conditions. The field oriented control of a permanent magnet synchronous motor using space vector modulation technique is implemented to investigate the performance of the proposed inverter drive and results are presented based on simulation done in Matlab/Simulink® and PSIM environment.**

***Index Terms*—Active balancing circuit, five-level NPC Inverter, Multilevel Inverter, Neutral Point Potential, SVM.**

## I. INTRODUCTION

PERMENANT MAGNET SYNCHRONOUS MOTORS (PMSM) are used as an attractive alternative to induction motors for high performance drive applications because of their high torque to inertia ratio, power density and efficiency due to reduced rotor losses [1]. To improve the dynamics as well as steady-state response of the motor drive, a power electronic converter with a suitable control technique can be used as an interface between the supply source and the PMSM. The conventional two-level voltage source inverter (VSI) present in the motor drives can be replaced with multilevel inverters using semiconductor devices of smaller voltage ratings to improve the motor voltage and current harmonics, lower THD, reduced electromagnetic interference (EMI) problems [2-5]. Three-level converters can also be used for improving the input power factor as well as current THD in a rectifier-inverter drive system [6] . Five-level inverters when compared to three-level inverters generate lesser common mode currents at the motor shaft and bearings due to low voltage change rates (dV/dt) and hence give improved reliability and motor life. The neutral point clamped (NPC), cascaded H-bridge (CHB) and flying capacitor (FC) converters are considered as the three classical multilevel converter topologies which have made their way to industrial applications almost two decades ago [7, 8]. The new multilevel converter topologies proposed by the researchers [2] are derived from these three classical topologies to meet several challenges like high efficiency and reliability.

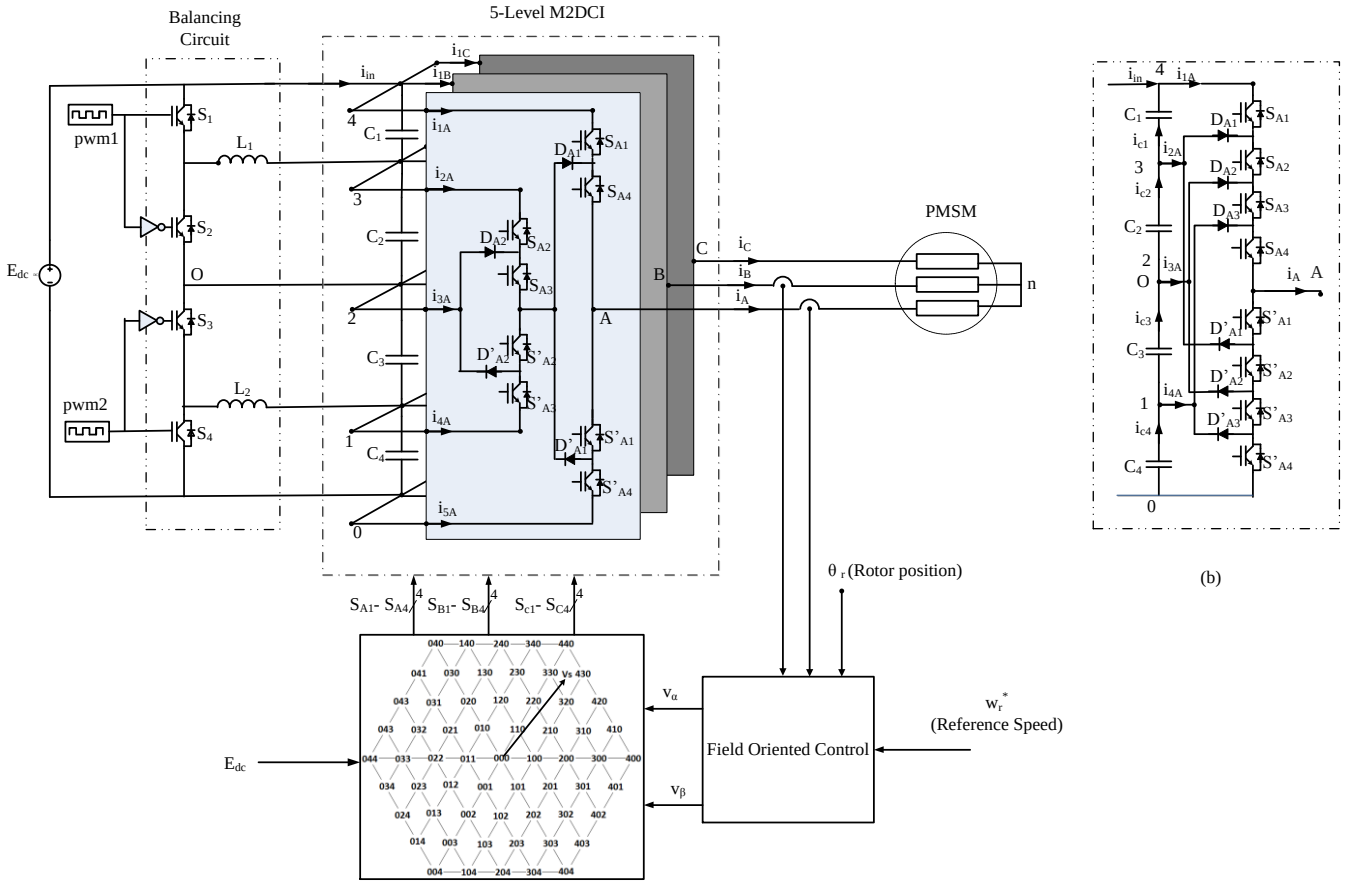
This paper proposes a five-level multiple-pole multilevel diode-clamped inverter (M2DCI) to drive PMSM motor. The new converter is derived from three-level diode-clamped multilevel inverter (DCMI) and uses lesser number of clamping diodes compared to classical 5-level DCMI [9]. The four capacitors connected in series across the dc-link are balanced using dc voltage-balancing circuit with neutral point potential control technique. The field oriented control of PMSM drive with space vector modulation (SVM) technique is co-simulated between Matlab/Simulink® and PSIM and the results are presented. The proposed drive is expected to give good performance by reducing the torque ripple, converter losses and THD.

## II. PROPOSED FIVE-LEVEL M2DCI DRIVE

Fig.1.(a) shows the schematic of the proposed PMSM drive using new five-level M2DCI. The field oriented control block generates the sinusoidal reference voltage required at the motor terminals based on the speed demand and space vector modulator provides the corresponding gating signals for 5-level M2DCI. The 5-level M2DCI [9] will convert the DC voltage to a stepped output voltage waveforms equivalent to the sinusoidal reference voltage which will drive the PMSM at a given reference speed. The function of the balancing circuit is to maintain a constant voltage of magnitude $E_{dc}/4$ across the individual dc-link capacitors during transient and steady state operating conditions. The modeling of 5-level M2DCI and also dc-link capacitor voltage balancing techniques are discussed below.

### *A. 5-Level M2DCI Modeling*

The inverter terminal voltage with respect to dc-link capacitor mid-point terminal '2' in fig.1.(a) can achieve 5 different voltage magnitudes corresponding to switching signals as given in Table I. Compared to the classical five-level DCMI shown in fig.1(b), the proposed inverter uses lesser number of clamping diodes and shares voltage stress equally ($E_{dc}/4$) while generating different levels of output voltages. If equal voltage rating diodes have to be used in classical DCMI, the total number of clamping diodes required




(a)

Fig. 1.(a) Proposed five-level multiple- pole multilevel diode-clamped inverter (M2DCI) PMSM Drive (b) Classical five-level diode-clamped multilevel inverter (DCMI) configuration showing phase A.

TABLE I
SWITCHING STATES AND POLE VOLTAGE OF A 5-LEVEL M2DCI
(X=A,B,C )

| Level $L_X$ | Switching states $S_{X1}$ | $S_{X2}$ | $S_{X3}$ | $S_{X4}$ | Pole Voltage ($V_{X2}$ or $V_{XO}$) |
|---|---|---|---|---|---|
| 4 | ON | ON | ON | ON | $E_{dc}/2$ |
| 3 | OFF | ON | ON | ON | $E_{dc}/4$ |
| 2 | OFF | OFF | ON | ON | 0 |
| 1 | OFF | OFF | OFF | ON | $-E_{dc}/4$ |
| 0 | OFF | OFF | OFF | OFF | $-E_{dc}/2$ |

per phase was 12 whereas in 5-level M2DCI is four.

Let $\lambda_{x1}, \lambda_{x2}, \lambda_{x3}, \lambda_{x4}, \lambda_{x5}$ represents the logic signals when the respective switching combinations $(S_{x1} \text{ to } S_{x4}), (S_{x2} \text{ to } S'_{x1}), (S_{x3} \text{ to } S'_{x2}), (S_{x4} \text{ to } S'_{x3}), (S'_{x1} \text{ to } S'_{x4})$ in fig.1(a) are true. Then the currents of the inverter (neglecting the balancing circuit) through the top and bottom terminals of the dc-link and mid- point between the capacitors are

$$\begin{aligned} i_1 &= \lambda_{A1} i_A + \lambda_{B1} i_B + \lambda_{C1} i_C \\ i_2 &= \lambda_{A2} i_A + \lambda_{B2} i_B + \lambda_{C2} i_C \\ i_3 &= \lambda_{A3} i_A + \lambda_{B3} i_B + \lambda_{C3} i_C \\ i_4 &= \lambda_{A4} i_A + \lambda_{B4} i_B + \lambda_{C4} i_C \\ i_5 &= \lambda_{A5} i_A + \lambda_{B5} i_B + \lambda_{C5} i_C \end{aligned} \quad (1)$$

And the dc-link capacitor currents can be written as

$$\begin{aligned} i_{C1} &= i_1 - i_{in} \\ i_{C2} &= i_1 + i_2 - i_{in} \\ i_{C3} &= i_1 + i_2 + i_3 - i_{in} \\ i_{C4} &= i_1 + i_2 + i_3 + i_4 - i_{in} \end{aligned} \quad (2)$$

from (2), the changes in capacitor voltages can be derived as

$$\begin{aligned} \Delta V_1 &= V_{C2} - V_{C1} = \frac{1}{C}\int i_2 dt \\ \Delta V_2 &= V_{C3} - V_{C2} = \frac{1}{C}\int i_3 dt \\ \Delta V_3 &= V_{C4} - V_{C3} = \frac{1}{C}\int i_4 dt \end{aligned} \quad (3)$$

Hence from (3) it can be noticed that, when the inverter is operating at any of the five valid switching conditions given in Table I which gives $(S_{X4}\text{-}S_{X1})=1$, there is a current flow at the mid-point of the dc-link capacitors which will create an unbalanced voltage across the capacitors. And this leads to an operation failure of the inverter. The main challenge in working with the proposed PMSM drive is to eliminate this voltage drift phenomena of neutral point clamped inverter during dynamic and steady state operating conditions. An auxiliary converter together with voltage balancing control is used here to maintain a balanced voltage across four dc-link capacitors in all conditions.

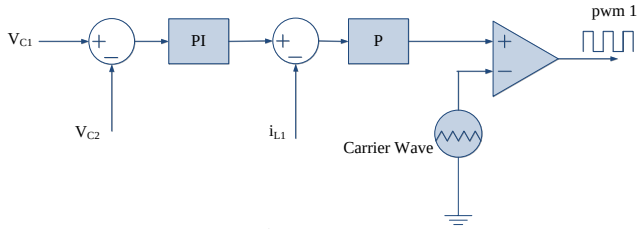



Fig. 2. Control schematic of positive chopper in voltage balancing circuit.

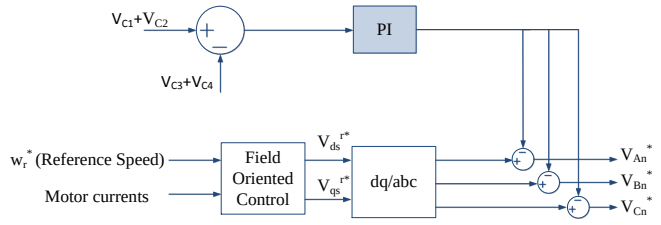



Fig. 3. Mid-point potential balancing control of M2DCI.

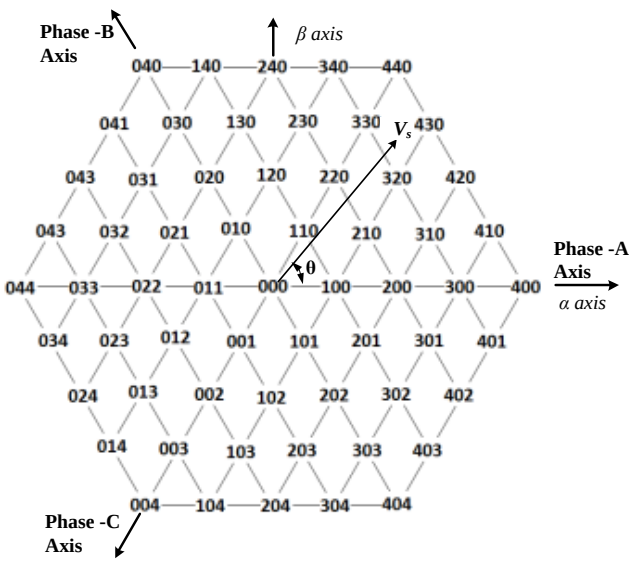



Fig. 4. Space vector representation of 5-level inverter

### *B. DC-Capacitor Voltage Balancing*

A voltage balancing circuit shown in fig.1 (a) consists of positive and negative buck-boost choppers which operate independently to provide constant voltage across the dc-capacitors [10] . The control block diagram of positive chopper is shown in fig.2. A similar control is done for negative chopper to reduce the voltage difference across capacitor $C_3$ and $C_4$. In addition to that, a mid-point balancing control shown in fig.3 is implemented to balance the neutral point potential.

## III. SPACE VECTOR BASED PWM TECHNIQUE FOR 5-LEVEL M2DCI

From fig.1.(a), the motor phase voltages can be expressed in terms of inverter pole voltages as

$$\begin{aligned} V_{An} &= V_{AO} - V_{nO} \\ V_{Bn} &= V_{BO} - V_{nO} \\ V_{Cn} &= V_{CO} - V_{nO} \end{aligned} \tag{4}$$

And its equivalent space vector generated is

$$\boldsymbol{V_s} = \frac{2}{3}\left( V_{An} + V_{Bn}e^{j\frac{2\pi}{3}} + V_{Cn}e^{j\frac{4\pi}{3}} \right) = V_r e^{j\theta} \tag{5}$$

Applying (4) in to (5)

$$\boldsymbol{V_s} = \frac{2}{3}\left( V_{AO} + V_{BO}e^{j\frac{2\pi}{3}} + V_{CO}e^{j\frac{4\pi}{3}} \right) = V_r e^{j\theta} \tag{6}$$

The $5^3$=125 permissible states generated for the 5-level M2DCI are represented by the 61 equivalent space vectors using (6) and are shown in fig.4. However, for simplicity the redundant switching states are not marked in fig.4. So at any instant for a fixed duration over one sampling period, the equivalent reference voltage vector $\boldsymbol{V_s}$ can be realized by switching the three nearest voltage vectors which are surrounding the tip of the reference vector as given below

$$\boldsymbol{V_s} = \left( d_1.\boldsymbol{V_1} + d_2.\boldsymbol{V_2} + d_3.\boldsymbol{V_3} \right) \tag{7}$$

Here $\boldsymbol{V_1}$, $\boldsymbol{V_2}$, $\boldsymbol{V_3}$ are the nearest three voltage vectors and $d_1$, $d_2$, $d_3$ are their respective duty ratios.

The theoretical voltage balance limits for classical diode clamped topology is given by

$$m = \sqrt{3} \Big/ \left( \pi \times |PF| \right) \tag{8}$$

where m is the modulation index and PF is the load power factor.

Hence the voltage balancing control utilizing redundant voltage vector property of space vector modulation cannot provide balanced voltage across the dc-link capacitors while driving the motor. The function of the SVPWM block in fig.1.(a) is to generate the gating pulses for the 5-level inverter switches to realize three phase reference voltage at the motor terminals as demanded by the controller.

## IV. FIELD ORIENTED CONTROL OF PMSM

The state space model of PMSM in rotor reference frame is given by [1]

$$\begin{aligned} pi_{ds}^r &= \frac{\left( V_{ds}^r - Ri_{ds}^r + w_r L_q i_{qs}^r \right)}{L_d} \\ pi_{qs}^r &= \frac{\left( V_{qs}^r - Ri_{qs}^r + w_r L_d i_{ds}^r - w_r \lambda_{af} \right)}{L_q} \\ pw^r &= \frac{\left( \left( P/2 \right)\left( T_e - T_l \right) - Bw_r \right)}{J} \\ p\theta^r &= w_r \end{aligned} \tag{9}$$

Where $i_{ds}^r$, $i_{qs}^r$ and $V_{ds}^r$, $V_{qs}^r$ are the direct and quadrature axis component of stator currents and voltages respectively. $L_d$ and $L_q$ are the stator inductances, $\lambda_{af}$ is the flux linkage due to rotor magnets linking the stator. R is stator resistance, $w_r$ is rotor speed in rad/s, $T_e$ and $T_l$ represents the electromagnetic torque developed by the motor and load

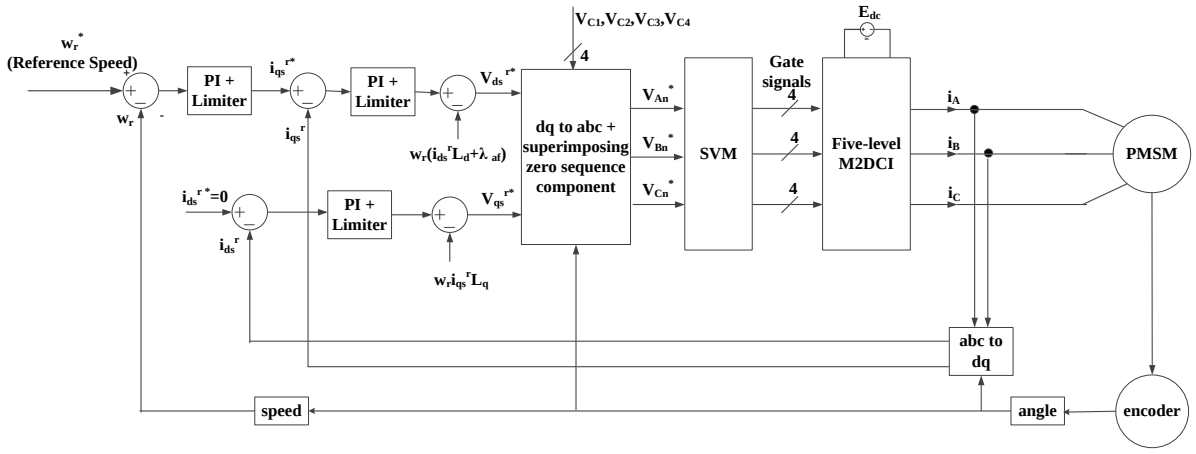



Fig. 5. Field oriented control of PMSM.

TABLE II
SPECIFICATION OF 5-LEVEL M2DCI SYSTEM

| | |
|---|---|
| DC-Link voltage, $E_{dc}$ | 500V |
| DC-Link capacitor, $C_j$ , j=1,2,3,4. | 2200μF±20% tolerance and ESR=100mΩ |
| Sampling Frequency, $f_s$ | 2.5kHz |
| Balancing circuit inductance $L_1$=$L_2$ | 6mH |
| PI controller and P controller of Balancing circuit | PI controller :Gain=0.5 and time constant =5s<br>P controller : Gain=15 |
| PI controller of mid-point voltage balancing | Gain=0.01 and time constant=1s |
| frequency | 50Hz |

toque in Nm respectively.

If $i_{ds}^r=0$ then $T_e = k_t i_{qs}^r$ where $k_t$ is the motor torque constant. Hence the torque can be controlled by controlling the quadrature component of stator current $i_{qs}^r$ . Also, a negative value of $i_{ds}^r$ will weaken the air-gap flux.

The control scheme for the speed FOC of PMSM drive is shown in fig.5. The outer loop generates the reference current $i_{qs}^{r*}$ to drive the motor in desired speed. To get an optimum torque, the flux reference is set to zero by forcing $i_{ds}^{r*}=0$. The output of the current controller gives the reference stator voltage in dq model. The three phase equivalent of stator voltage is calculated and a dc zero-sequence component which balances the mid-point potential (fig.3) is superimposed on this three phase voltage reference signal and given to the SV modulator.

## V. PERFORMANCE EVALUATION OF PROPOSED PMSM DRIVE

To evaluate the performance of the proposed five-level M2DCI PMSM drive, whole system is co-simulated between Matlab/Simulink® and PSIM environment. The system parameters are given in Table II. A PMSM which has parameters R=4.3Ω, $L_d$=23mH, $L_q$=67mH, J=1.79mkgm$^2$, B=0.179Nm/rad, and $\lambda_{af}$=0.2719V/rad/s is been selected for simulation. A load of 5Nm is applied at the motor and a rotor speed of magnitude 200rad/s is selected as reference speed.

The voltage at motor terminal with respect to inverter mid-point for phase 'A' and three phase motor currents are shown in figs.6 and 7 respectively. The pole voltage in fig.6 has 5 distinct levels. Figs.8 and 9 show the simulation results of rotor speed $w_r$ and developed electromagnetic Torque $T_e$ of the same PMSM drive with the given control technique. The motor is started from standstill with an applied load of 5Nm

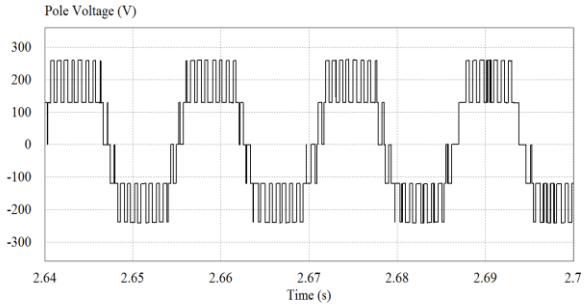



Fig. 6. Motor terminal voltage with respect to inverter mid-point '2' for phase 'A'..

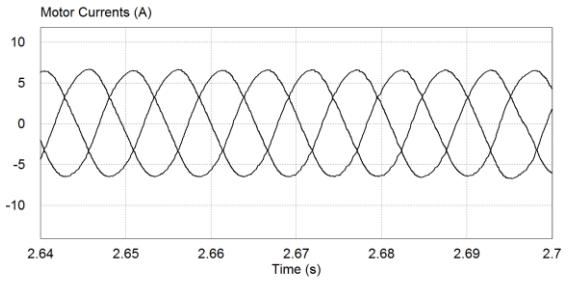



Fig. 7. Motor three phase line current waveforms.

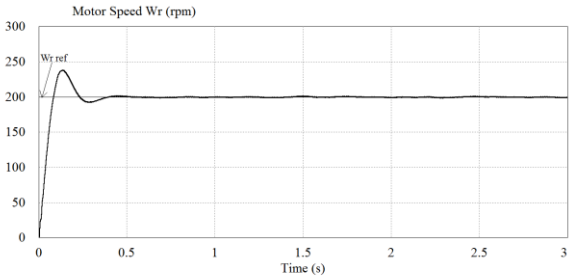



Fig. 8. Motor speed, '$w_r$' in rpm.

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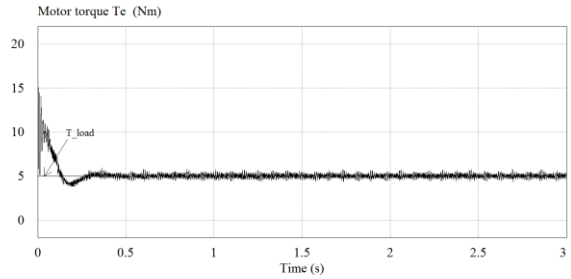


Fig. 9. Electromagnetic toque developed by the PMSM, '$T_e$' in Nm.

to a reference speed of 200 rad/sec. The PI speed controller and current controllers comes into action and track the reference speed. And motor develops a torque equal to the load torque.

## VI. CONCLUSION

Multilevel inverter fed motor drives produce low stress on motor bearings and windings due to its low common mode voltage, low dV/dt and nearly sinusoidal three phase currents characteristics when compared to conventional two-level VSI drives. Here a reduced device DCMI topology is proposed to drive the PMSM motor in a constant speed. An active balancing circuit with neutral point potential control is used to eliminate the voltage drift phenomena in five-level M2DCI. Simulation results presented in the paper ensure that the balancing circuit maintain a constant voltage of magnitude equal to $(E_{dc}/4)\pm3\%$ across the dc-link capacitors which provides five-level output voltage at the inverter terminals. And field oriented control with SVM is implemented to control the inverter and hence the motor. The proposed drive is expected to give good performance by reducing the torque ripple, converter losses and THD.

## ACKNOWLEDGEMENT

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