A 32kb 9T Near-threshold SRAM with Enhanced Read Ability at Ultra-low Voltage Operation

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Abstract— **Ultra-low voltage SRAMs are highly sought-after in energy-limited systems such as battery-powered and self-harvested SoCs. However, ultra-low voltage operation diminishes SRAM read bitline (RBL) sensing margin significantly. This paper tackles this issue by presenting a novel 9T cell with data-independent RBL leakage in combination with an RBL boosting technique for enhancing the sensing margin. The proposed technique automatically tracks process, temperature and voltage (PVT) variations for robust sensing margin enhancement. A test chip fabricated in 65 nm CMOS technology shows that the proposed scheme significantly enlarges the sensing margin compared to the conventional bitline sensing scheme. It also achieves the minimum operating voltage of 0.18 V and the minimum energy consumption of 0.92 J/access at 0.4 V.**

Highlights

- **A novel 9T SRAM cell is proposed for realizing data-independent bitline leakage.**
- **A bias control mechanism for enhancing bitline sensing margin is proposed.**
- **The proposed control enhances the bitline sensing window.**

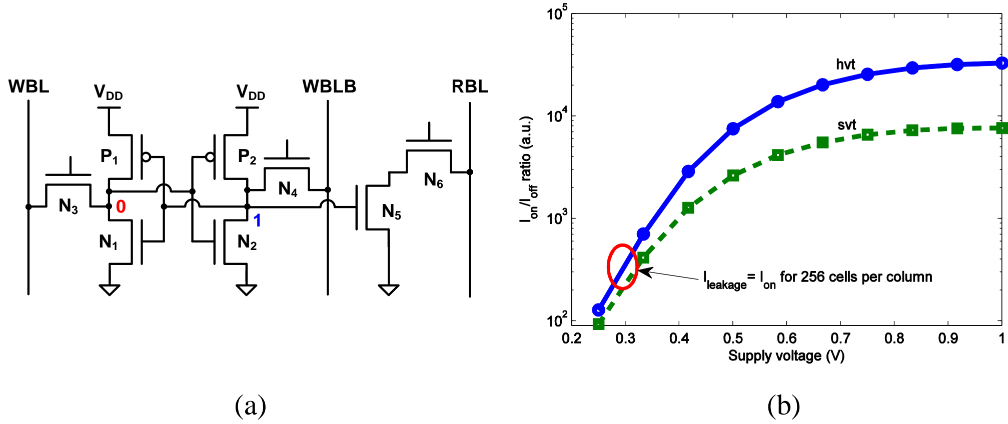
Keywords: Static random access memory (SRAM), bitline sensing, data-independent bitline leakage, MTCMOS.

I. INTRODUCTION

Ultra-low power circuits are highly demanded in many green computing systems where ultra-low voltage operation offers better energy efficiency with moderation in performance [1, 2]. However, ultra-low voltage operation suffers from degraded noise margin and large performance variations due to aggressively scaled supply voltages [3]. One of the most challenging functional blocks in ultra-low voltage operation is an SRAM because of various

design parameters such as stability, write margin, sensing margin, and bitline leakage. [4]. A number of design techniques have been presented to tackle the above challenges, focusing on enhancing SRAM's operation reliability at near or sub-threshold voltage regions. However, due to the conflicting nature of the read and write operations in the conventional 6T SRAM structure, most of these techniques are essentially compromising one factor to gain others. One prominent trend in the ultra-low voltage SRAM is adopting decoupled SRAM cells with additional devices [5]. Particularly, the 8T SRAM (Fig. 1(a)) is the most popular design thanks to its superior performance and compact footprint. The main benefit of the decoupled SRAM cells is the improved cell stability coming from the isolated cell storage nodes from the read bitlines (RBL). As a result, write and read operations can be optimized independently. Various write margin improvement techniques have been reported in [6] – [8]. Floating cell supply in [6] weakens the strength of the cell during write while boosted wordline (WL) voltage [7] and negative bitline voltage [8] increases the strength of the write access transistors. Regarding the read operation, Verma *et al.* proposed a sense amplifier redundancy technique [9] to mitigate the offset issue during bitline sensing. Finally, leakage reduction is another a topmost requirement in ultra-low power SRAMs since leakage dominates the overall power consumption [10].

As supply voltage scales aggressively in nano-scale CMOS technologies [9], the on-current (I_{on}) to off-current (I_{off}) ratio (i.e. the difference between reading "1" and "0") in SRAM RBLs diminishes, deteriorating RBL sensing margin. Fig. 1 explains the I_{on}-to-I_{off} ratio at different supply levels. It is obvious that the I_{on}-to-I_{off} ratio decreases exponentially as the supply lowers to the near- or sub-threshold region. For example, the I_{on}-to-I_{off} ratio becomes a few hundred at 0.3 or 0.4 V, as shown in Fig. 1(b). This indicates that an RBL with 256 cells per column will fail to operate reliably. In addition, since the RBL leakage is determined by data in bitlines, reliable RBL sensing becomes insurmountable in the conventional design.



(a) (b)

Fig. 1. (a) Conventional 8T SRAM cell. (b) Simulated I_{on}-to-I_{off} ratio the conventional 8T SRAM cell during a read operation. Two device options are used for comparison (i.e. high-V_{th} and standard V_{th} transistors).

This paper proposes techniques for tackling the aforementioned leakage issues on RBL sensing, and minimizing V_{DDmin} of the SRA M. They are (i) a multi-V_{th} (MTCMOS) 9T SRAM cell with constant RBL leakage regardless of its stored data and (ii) an RBL boosting scheme for expanding the RBL sensing margin and sensing window at ultra-low supply voltage.

Following this introductory section, Section II briefly examines basic operations of the conventional 8T SRAM and its associated RBL leakage issues. Section III presents our proposed RBL sensing scheme with a 9T SRAM cell that has data-independent leakage. In Section IV, we discuss the proposed biasing voltage generator that tracks the optimum biasing point of the RBL keeper. Section V presents the test chip measurement results. Finally, Section VI concludes our paper.

II. READ BITLINE SENSING CHALLENGES IN ULTRA-LOW VOLTAGE SRAMS

A. Decoupled 8T SRAM basics

Decoupled 8T SRAM cells improve stability substantially, which is the primary reason for their popularity in ultra-low voltage SRAMs [11]. A typical 8T SRAM macro consists of a row decoder, a memory array, a column decoder, read/write circuits and a control unit. Each column

has one RBL and two write-BLs (i.e. WBL and WBLB) while each row has one read-WL (RWL) and one write-WL (WWL) for read and write, respectively. The 8T SRAM cell (Fig. 1(a)) includes a typical 6T structure for storing and writing data while a dedicated read port is added for the disturb-free read operation. Since the read port is isolated from the cross-coupled structure of the 6T cell, the read and write access transistors can be concurrently optimized for better read and write stabilities.

Transient simulation waveforms of a typical SRAM during read, write and standby operations at 1.2 V, 500 MHz are illustrated in Fig. 2. Q and QB represent the data storage nodes of an SRAM cell. The 8T SRAM behavior in standby and write operation is identical to that of the conventional 6T SRAM [12]. In a read cycle, selected RWL is pulled high to select a row while a column decoder will select specific RBLs. Subsequently, the selected RBLs are conditionally discharged depending upon the read data. If a cell stores data "0" (i.e Q = 0), both N_5 and N_6 of the read port are turned on to discharge RBL from V_{DD} to ground (Fig. 2). Otherwise, N_5 is off and thus RBL remains unchanged. The difference in the RBL discharging speed is sensed by sense amplifiers.

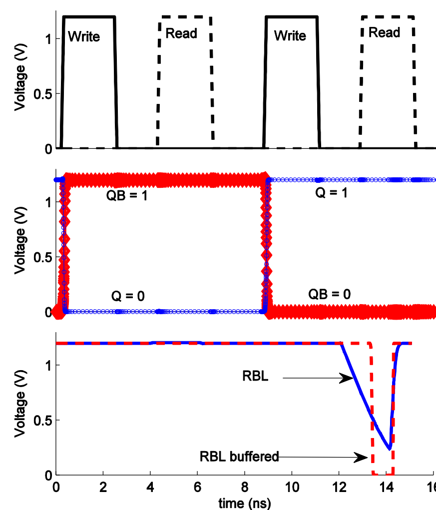


Fig. 2. Sample SRAM transient simulation waveforms at 1.2 V, 500 MHz.

B. Leakage components in 8T SRAMs and their impacts on RBL sensing

High density SRAMs implemented in nano-scale CMOS technologies suffer from significant leakage current due to the leaky device characteristics [13]. Majority of this leakage current comes from the enormous SRAM array. Although leakage per cell is small, total leakage power of a large capacity SRAM is considerably large and comparable to its dynamic power. Cell leakage in SRAM consists of three major components that are sub-threshold leakage, gate leakage, and junction leakage. The leakage in SRAMs is also temperature-dependent, increasing more than 30-fold when temperature changes from 27 °C to 100 °C (Fig. 3). Furthermore, this leakage current constantly drains out energy, regardless of the operation

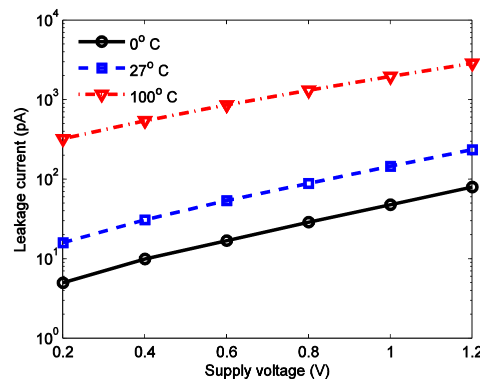
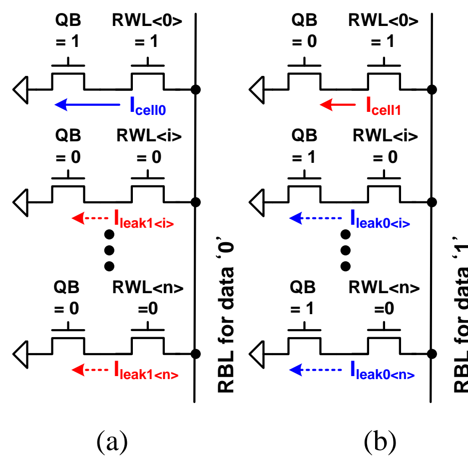


Fig. 3. Total cell leakage at different supply voltages and temperature using standard threshold voltage transistors (SVT).

mode. Therefore, reducing SRAM leakage current is crucial to any low-power design, especially in usually-off applications such as remote sensor nodes and portable devices.

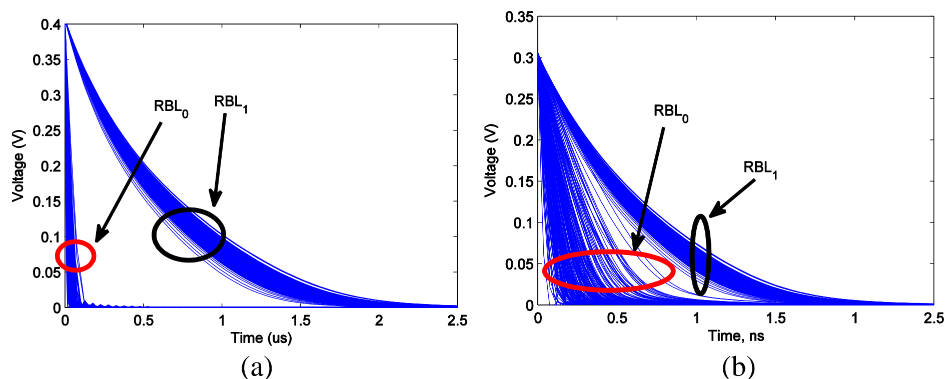
Scaling down V_{DD} is the most effective approach to reduce leakage current in SRAM design [14, 15]. For instance, in Fig. 3, the cell leakage reduces 5× when the supply voltage scales down from 1.2 V to 0.4 V. This leakage reduction comes at the cost of degraded noise margin. However, the 8T SRAM cell operating at ultra-low supply condition has a critical issue since the bitline leakage is data-dependent. The worst case RBL scenarios are depicted in Fig. 4. Ideally, RBL for data "1" (i.e. Q = 1) stays at V_{DD} while RBL for data "0" is formed by the cell current (I_{cell0}). However, it does not occur in actual operation. First, due to excessive leakage,

both RBLs of data "0" and "1" show similar discharging speed. In addition, unselected cells in the RBL produces data-dependent leakage, leading to sensing failure in worst-case scenarios. Fig. 4 describes the worst case RBLs for data "0" and "1". In the worst case RBL for data "1", the gate of N5 (Fig. 1(a)) in unselected cells is V_{DD} and thus its RBL leakage is maximized. As V_{DD} scales, the summation of the cell current and the RBL leakage in the worst case RBL for data "1" can be similar or larger than that in the worst case RBL for data "0". This makes the RBL for data "1" discharged at a similar rate or even faster than that for data "0". As illustrated in Fig. 5, RBL_1 and RBL_0 can be easily distinguished when V_{DD} is 0.4 V but hardly separable when V_{DD} is lowered to 0.3 V. In this case, the sense amplifiers cannot operate properly. This indicates that the SRAM fails to operate at or below 0.3 V. Therefore, leakage-aware RBL structures are highly desirable for further improving V_{DDmin} of low-voltage SRAMs.



(a) (b)

Fig. 4. Schematic of a conventional 8T SRAM read RBL structure: (a) worst case for reading data '0' and (b) worst case for reading data '1'.



(a) (b)

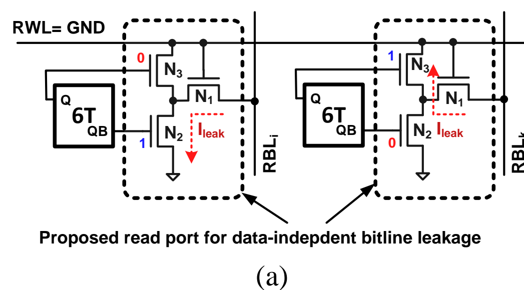
Fig. 5. Transient waveforms of the worst-case RBL_0 and worst-case RBL_1 during a read operation using Monte-Carlo simulation. (a) V_{DD} = 0.4 V. (b) V_{DD} = 0.3 V.

III. PROPOSED RBL SENSING SCHEME WITH 9T SRAM CELL FOR DATA-INDEPENDENT RBL LEAKAGE.

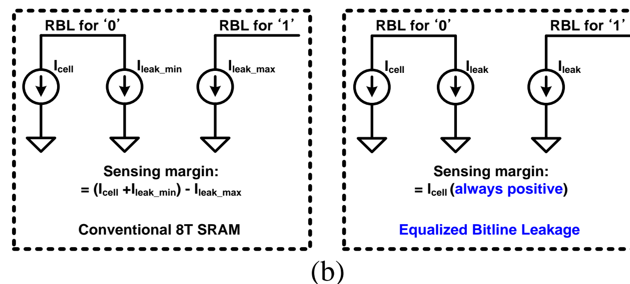
A. *9T SRAM cell for data-independent RBL leakage*

The 9T SRAM cell [16] achieves data-independent leakage by adding one transistor to the 8T SRAM cell read port. Fig. 6(a) highlights the leakage current flowing through the read port of unselected cells. The gate nodes of N1, N2, and N3 are connected to RWL, QB and Q, respectively. The source terminal of N3 is also connected to RWL. During standby, either N2 or N3 is connected to V_{DD} while the other is connected to ground. The RBL leakage passing through N1 will flow to ground through either N2 or N3, depending on the stored data. Since N2 and N3 are equally sized, the RBL leakage of each cell is constant. Note that the read current of the proposed 9T SRAM cell is similar to that of the SRAM 8T cell.

The principle of the proposed data-independent RBL leakage compared to the conventional RBL leakage is explained in Fig. 6(b). In the conventional 8T SRAM (Fig. 6(b)(Left)), the worst case RBL of reading data '0' occurs when all unselected cells in the same column store data "1". Its pull-down current is '$I_{cell} + I_{leak_min}$'. Similarly, the worst case RBL of reading data '1' is 'I_{leak_max}'. RBL can be correctly sensed only when '$I_{cell} + I_{leak_min}$' is significantly larger



(a)



(b)

Fig. 6. Proposed data-independent RBL leakage: (a) read port schematic and (b) principle.

than ‘I_{leak_max}’, which limits V_{DDmin}. However, in the proposed scheme (Fig. 6(b)(Right)), the amount of the RBL leakage is constant, regardless of the data in the unselected cells. Consequently, it always provides a positive sensing margin, which is equal to I_{cell}. As simulated in Fig. 7(a), I_{read0} is always larger than I_{read1} in the 9T cell while in the 8T cell, the worst case I_{read0} is smaller than I_{read1} at around 0.27 V. Since the data-independent RBL leakage always generates positive margins, acceptable sensing can be achieved even at ultra-low supply voltages. For example, Fig. 7(b) shows the Monte-Carlo simulation of the proposed 9T cell in a 256-cell per column configuration at 0.3 V. Unlike the result shown in Fig. 5(b), the proposed 9T cell offers a clear separation between RBL_0 and RBL_1, i.e. a better sensing margin.

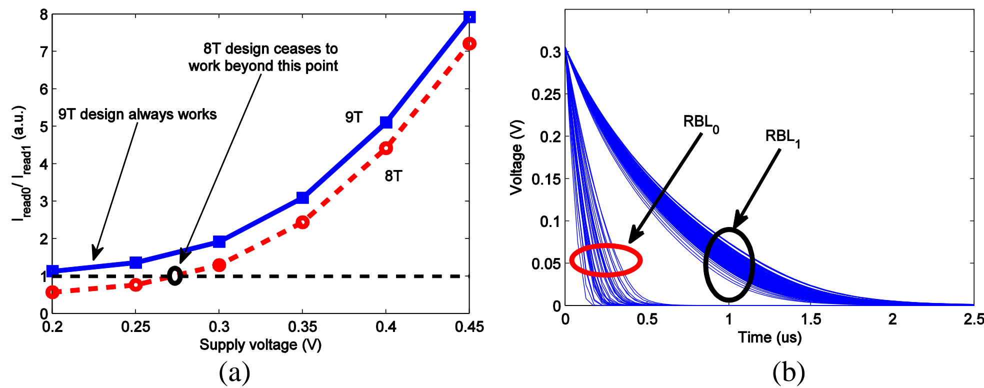
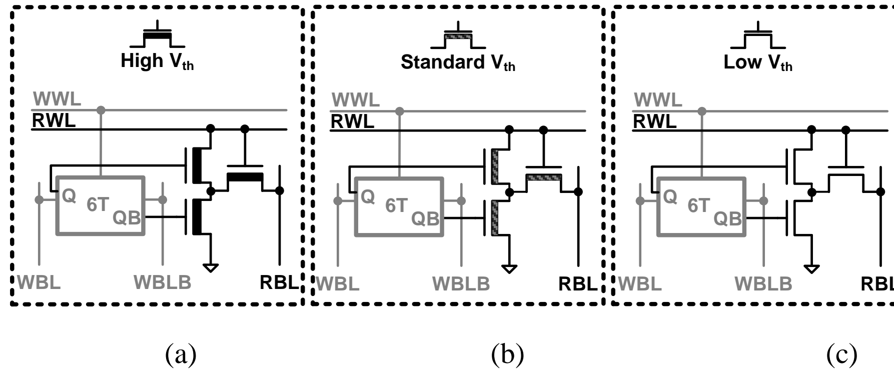


Fig. 7. (a) Comparison of I_{read0}/I_{read1} at different supply voltages and (b) Monte-Carlo simulation results of the RBL_0 and RBL_1 of the proposed read port at V_{DD} = 0.3 V.

B. Cell optimization using MTCMOS process for ultra-low voltage applications

MTCMOS is commonly available in modern CMOS process technology for embedded system design so that power and performance can be optimized concurrently by using proper types of transistors in each functional block or unit circuit. The objective of optimizing SRAM cell using MTCMOS transistors is to achieve both low total leakage current and reliable sensing at ultra-low voltage condition. In MTCMOS technology, various devices with different threshold voltages (V_{th}) are available. Since the operating characteristics of each transistor is very sensitive to V_{th} at ultra-low voltage operation, MTCMOS provides a much stronger impact on cell performance than transistor sizing alone. To reduce leakage current, high V_{th} transistors



(a) (b) (c)

Fig. 8. 9T SRAM cells with three different read-port configurations using MTCMOS technology: (a) HVT, (b) SVT (c) LVT. Note that HVT, SVT and LVT represent high-, standard- and low-V_{th} devices, respectively.

(HVT) are used in the 6T structure. Note that this does not slow down the SRAM performance because the critical delay is from the read path. At the read port, there are three options of using HVT, SVT or LVT as reading devices (Fig. 8). At ultra-low voltage, RBL sensing margin is the most important design requirement to ensure reliable operation. Given a fixed topology, RBL sensing margin is characterized by the I_{on}-to-I_{off} ratio of the SRAM cell. After evaluating the I_{on}-to-I_{off} ratios of the three configurations, we conclude that HVT gives the best I_{on}-to-I_{off} ratio while LVT is the worst. However, sensing delay of the HVT option is excessively higher when compared to the SVT and LVT ones. Furthermore, from the absolute current difference point of view, LVT gives the highest sensing margin (i.e. input gap), even though its I_{on}-to-I_{off} ratio is the smallest. Hence, LVT is used in the read port for read speed and reliable performance.

Using LVT at the read port increases the total cell leakage current with RBLs pre-charged to V_{DD}. To address this, we propose to pre-charge RBL to ground instead of V_{DD} to suppress the RBL leakage component. Fig. 9 compares the leakage current in the 9T cell using all SVT devices (base-line) and the proposed MTCMOS 9T cell (i.e. HVT in 6T and LVT in the read port) with high pre-charged RBL and low pre-charged RBL. The MTCMOS cell with low pre-charged RBL offers 17× leakage reduction at 1 V and 10× reduction at 0.4 V, respectively. The

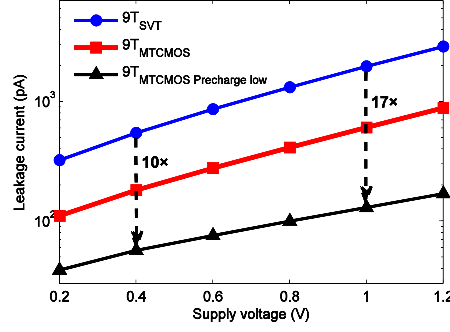


Fig. 9. Simulated I_{on}- I_{off} ratio of three different read ports options

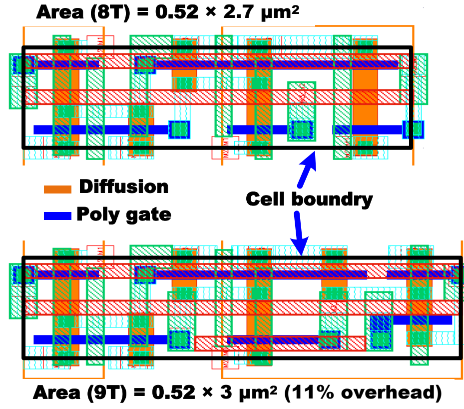


Fig. 10. Layout comparison of the proposed 9T cell and the conventional 8T cell.

detailed operation of the MTCMOS 9T SRAM cell with low pre-charged RBL will be further discussed in the next section.

The layouts of the proposed 9T and the conventional 8T cells are compared in Fig. 10. Because of one additional device at the read port, the proposed 9T cell layout is larger than the 8T one. Using standard logic design rules, the proposed cell layout has the same height as the 8T cell with 11% wider width.

IV. RBL Swing Boosting and PVT-tracking Bias Generation Scheme

A. Proposed RBL sensing margin enhancement technique

A larger RBL swing and a wider sensing window are desirable for reliable RBL sensing. In this section, we will discuss a novel RBL boosting current scheme to realize the above goals. Fig. 11 illustrates the principle of the proposed RBL boosting current technique. During non-

read operation, the RBL is pre-charged low (Fig. 12(a)) so that it eliminates the RBL leakage current. During read operation, pull-up boosting current (I_{boost}) through the strength-controlled PMOS devices, RBL leakage, and pull-down cell read current determines the RBL level. Since both pull-up and pull-down current components exist simultaneously, this forms two static RBL levels depending upon the read data. Therefore, unlike the conventional RBL sensing, the proposed scheme allows more reliable RBL sensing because of the static RBL levels (Fig. 12(b)), which improves the sensing window. Note that the final RBL swing of the proposed design does not depend on the pre-charge value of RBLs, which allows RBL to be pre-charged low and reduces the total leakage without scarifying the sensing margin. In the leakage compensation scheme in [18], leakage for compensation needs to be measured in each cycle, causing performance degradation and larger area overhead. However, the proposed technique uses V_{bias} only in the RBL boosters without precharge operation, which is more efficient in area and performance.

Fig. 12(b) contrasts the improvement of the proposed design (blue lines) over the conventional RBL (red lines) sensing scheme. In the conventional RBL sensing scheme, RBL_0 discharges faster than RBL_1 but since both are discharged, the RBL swing diminishes and become zeros after some delay. The RBL sensing should be executed within this short period of time, which is challenging when considering variations in the RBL swing development. However, in the proposed design, the RBL boosting current keep the RBL levels for data '1' and '0' at intermediate voltages over a wide sensing window. Furthermore, the RBL swing of the proposed design (75 mV– Fig. 12(b)) is also larger than the momentary maximum RBL swing of the conventional design (60 m V-Fig. 12(b)).

Even though the RBL boosting scheme enhances the sensing window significantly, the strength of the RBL boosters requires careful control to ensure an optimum RBL swing. If V_{bias} is too low, the RBL levels are raised, deteriorating the sensing margin for data "0". Similarly,

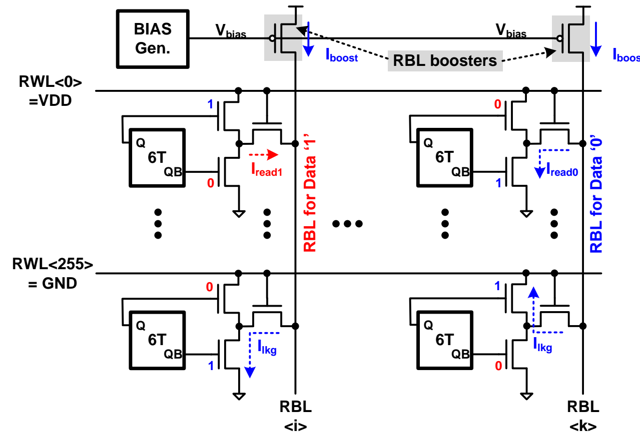


Fig. 11. Proposed RBL boosting current scheme for enhancing RBL sensing margin.

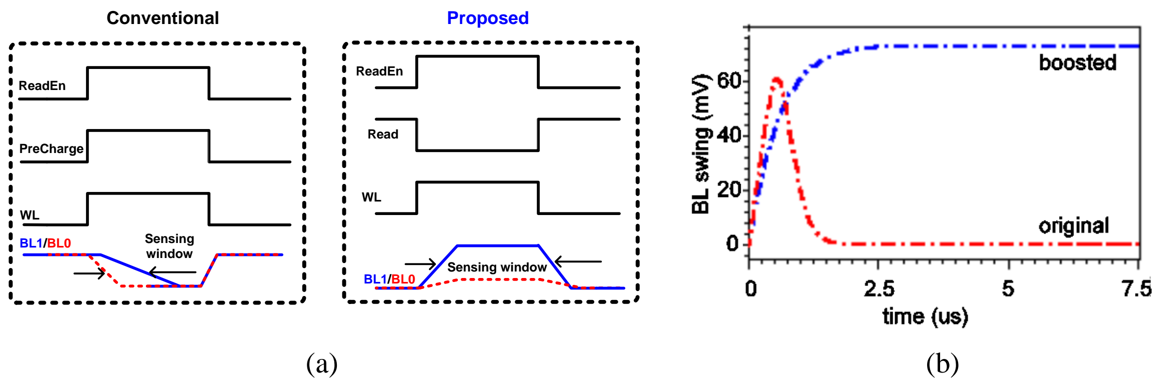


Fig. 12. Simulated RBL waveforms showing sensing margin improvement of the proposed boosting scheme. (a) control signals and RBL levels of data '1' and data '0', and (b) RBL swing (V(RBL of data '1') – V(RBL of data '0')). Note that 256 cells are used in each column.

if V_{bias} is too high, the RBL levels will be formed at lower levels, degrading the sensing margin for data "1".Therefore, V_{bias} needs careful control for maximizing RBL sensing margin.

Fig. 13 depicts the impact of V_{bias} on the RBL swing. When V_{bias} = 0 V, the boosting current strength is too strong. Although it helps to keep RBL_1 close to V_{DD}, RBL_0 is also close to V_{DD}. Thus, the RBL swing becomes almost zero. As we increase V_{bias} (i.e. V_{bias} = 40 mV and 80 mV), the RBL swing increases accordingly because the voltage level of RBL_0 drops faster than that of RBL_1. However, if V_{bias} is too high, the boosting current becomes too weak to hold RBL_1 and thus the RBL swing starts to reduce, as illustrated by the red line in Fig. 13. This is why RBL at V_{bias} = 100 mV is lower than that at V_{bias} = 80 mV. It indicates that the optimum voltage for biasing the boosting device is somewhere near 80 mV. A similar behavior is also

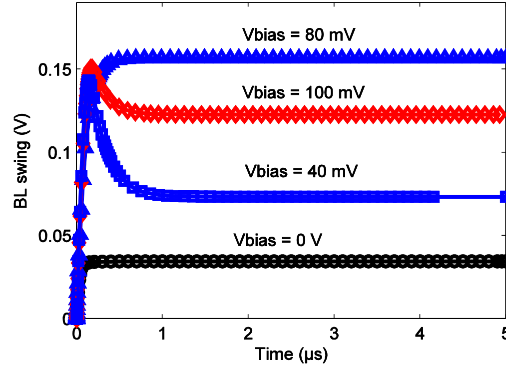


Fig. 13. Simulated RBL swing at different RBL boosting biasing voltages (i.e. V_{bias}).

observed at different operating voltages and temperatures. The optimal V_{bias} will be tracked by a PVT-tracking bias generator.

B. PVT-tracking bias generator for maximizing RBL swing

To generate optimum V_{bias}, a PVT-tracking bias generator is proposed (Fig. 14). It employs two dummy columns, four voltage reference ladders and two counters (one up-counter and one down-counter) (Fig. 14(a)). The first dummy column implements the read zero column (i.e. $I_{RBL} = I_{cell} + I_{leakage}$) while the other realizes the read one column. The down-counter (CT0) is initially set so that V_{ref0} is at V_{DD}. As the CT0 output decrements, V_{ref0} decreases, strengthening P1 (Fig. 14(b)). Once the RBL level is sensed as data "1", RBL0-buffered becomes high and stops CT0 through the clock. The lowest level of V_{bias0} is determined through this procedure.

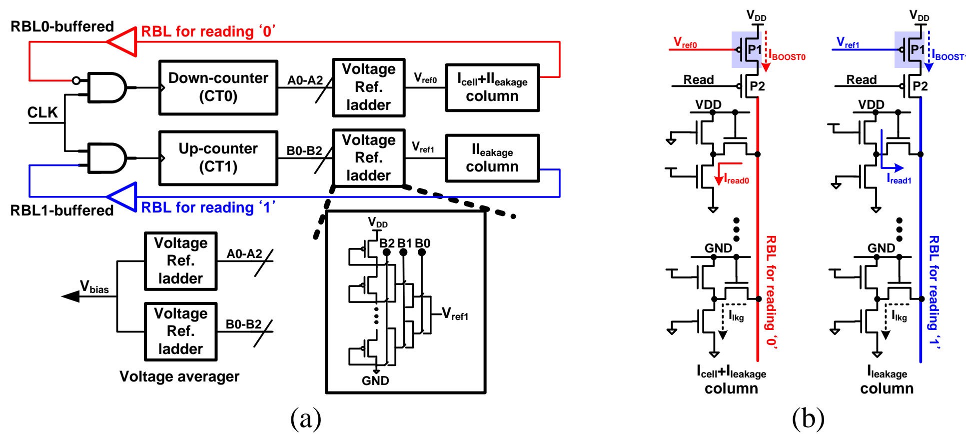


Fig. 14. (a) Simplified schematic of the proposed PVT-tracking biasing generator and (b) Schematic of hardwired dummy columns to replicate RBL_1 and RBL_0.

Similarly, the loop through the up-counter (CT1) estimates the highest level of V_{bias1} by incrementing V_{bias1} from the lowest level. Any voltage level between V_{bias0} and V_{bias1} can be used. However, the average of V_{bias0} and V_{bias1} is utilized to obtain balanced sensing margin. The average level is simply generated by merging the outputs of two reference ladders whose inputs are A0-A2 and B0-B2. The proposed bias generator occupies the area overhead less than 5%. It is independent of the array density, so it will decrease at a higher array density. The counters can be initialized again if V_{bias} needs to be updated due to an abrupt change in operating conditions. This work uses only 3 bits for demonstration. More bits can be used for better resolution.

C. Bias voltage quality evaluation

Even though the proposed scheme tracks $(V_{ref0} + V_{ref1}) / 2$, it may not be the optimum biasing voltage (i.e. $V_{optimum}$) for all the operating conditions. To verify this, the optimum biasing voltage is simulated and compared with V_{bias} generated by our scheme. Simulation results are plotted in Fig. 15(a). It can be seen that V_{bias} is not exactly the same as but closely tracks $V_{optimum}$. The maximum difference between $V_{optimum}$ and V_{bias} is only 5.6% at $V_{DD} = 0.6$ V. As a result, the generated RBL swing is at most 10 mV lower than that of the optimum RBL swing in the near- and sub-threshold voltage region, as shown in Fig. 15(b). At higher V_{DD}, the absolute gap between the optimum RBL swing and the actual RBL swing is wider. However, since the RBL swing is large enough for sensing, the sensing reliability is only marginally affected.

Although the proposed RBL boosting scheme provides superior performance at ultra-low voltage regime, it is slower than the conventional pre-charge high scheme at super-threshold regions. For example, as shown in Fig. 16(a), at $V_{DD} = 1.2$ V, the RBL delay is 20% larger than the conventional design. This is because the RBL boosting current must fight with I_{cell} which

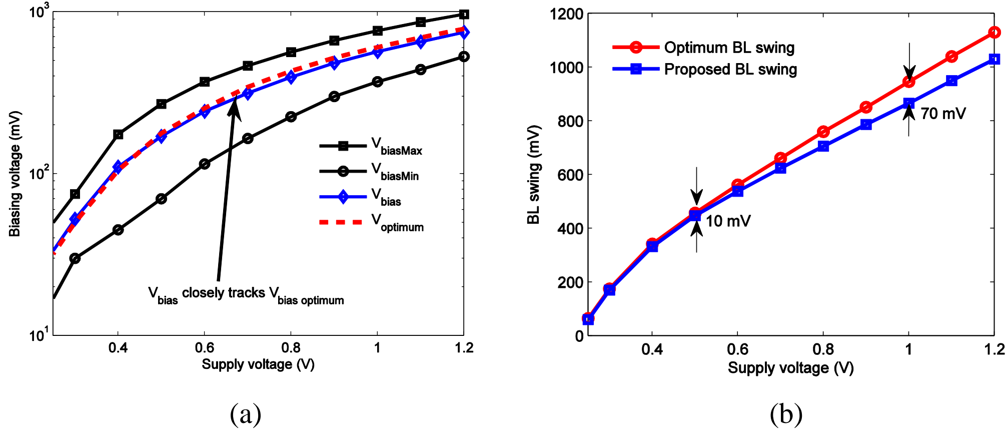


Fig. 15. (a) Optimum biasing voltage in comparison with V_{bias} generated by our proposed scheme and (b) comparison between the optimum RBL swing versus the RBL swing generated by our proposed scheme.

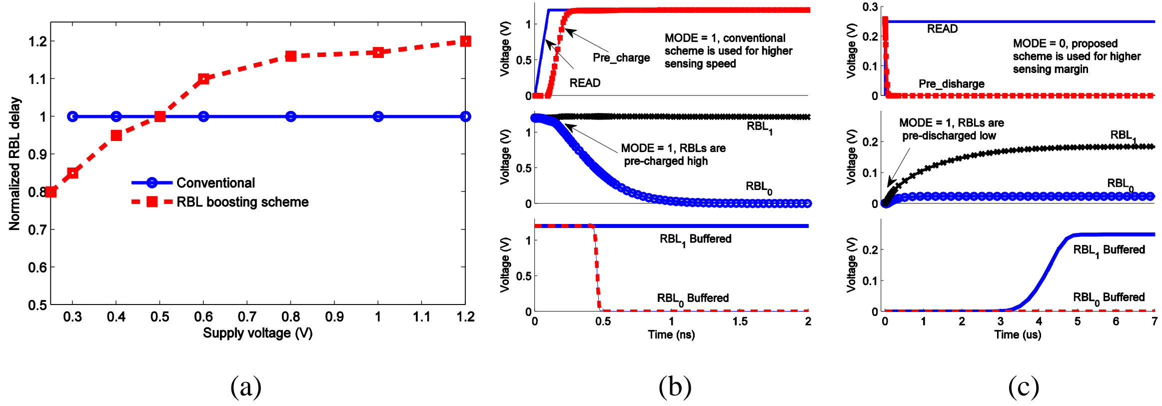


Fig. 16. (a) Normalized RBL delay of the boosting scheme when compared with the conventional design, (b) transient simulation waveforms during a read operation when MODE = 1, V_{DD} = 1.2 V, and (c) transient simulation waveforms during a read operation when MODE = 0, V_{DD} = 0.25 V.

is relatively strong at the nominal supply voltage. The proposed RBL boosting scheme shows its benefit at or below 0.5 V, also shown Fig. 16(a). In this region, the proposed scheme achieves not only faster sensing but also lower supply voltage. Thus, it is rational to switch the SRAM read operation back to conventional pre-charge high scheme at moderate or high V_{DD}. This can be easily done by a simple control circuit with two different operation modes as shown in Fig. 19(b-c). At higher V_{DD}, MODE is set to '1' and the RBL pre-charge signal is activated to pre-charge all RBLs high as the conventional scheme (Fig. 16(b)). At lower V_{DD}, MODE is set to '0' and the RBL pre-charge signal is deactivated to pre-discharges all RLBs low (Fig. 16(c)). Having two different modes allows the proposed design to operate over a wide range

of V_{DD}. The proposed technique can also be employed in more advanced technology where the I_{on}-to-I_{off} ratio and accordingly the bitline sensing margin degrade. Since the proposed technique improves the sensing margin at a given I_{on}-to-I_{off} ratio, a larger improvement in the sensing margin can be achieved in more advanced technology.

V. TEST CHIP IMPLEMENTATION AND MEASUREMENT

A. SRAM macro implementation

A 32K SRAM macro (128 columns × 256 rows) using the proposed 9T cell design has been fabricated in a 65 nm CMOS process. Its array configuration and the die photo are presented in Fig. 17. A similar 8T macro with the proposed RBL boosting technique is also fabricated for comparison. In each active cycle, an 8-bit row decoder activates one specific row while a 4-bit column decoder selects 8 out of 128 columns. Each column has its own local read buffer and write driver. Every 16 columns share a global output buffer and input data driver. The local write driver circuit is shown in Fig. 17(c) where COL_EN signal is activated by the column decoder and D and /D are complementary input data and are sent to WBL and WBLB. When a column is not selected, both WBL and WBLB are pre-charged high.

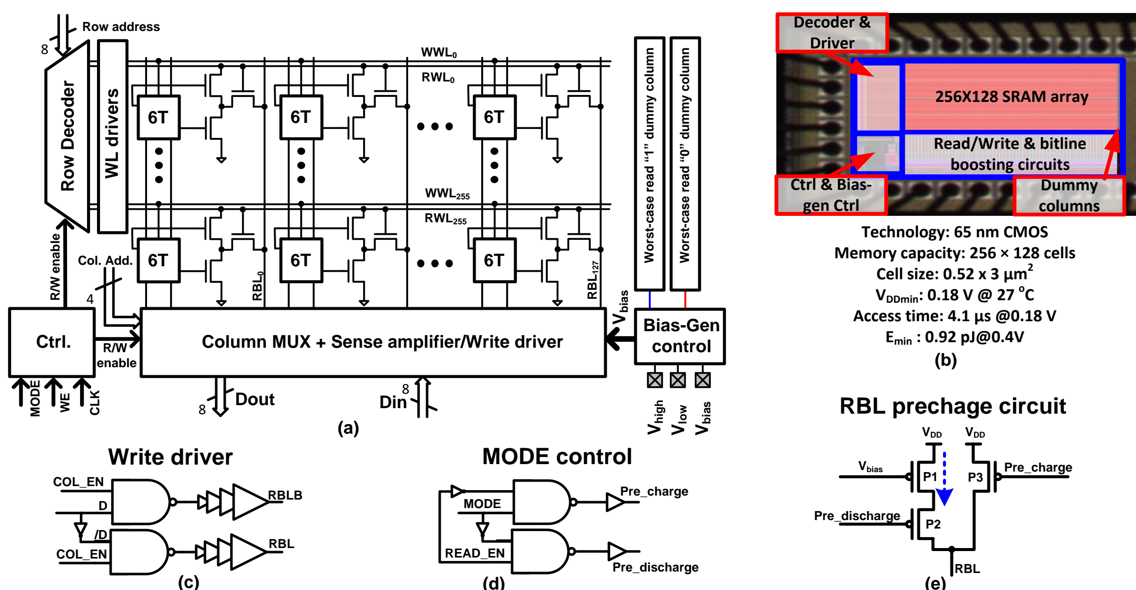


Fig. 17. Test chip micrograph in 65 nm CMOS technology

The Mode control circuit to switch between the conventional RBL scheme and the proposed RBL boosting scheme is shown in Fig. 17(d). When MODE = 1, Pre_discharge is deactivated (Pre_discharge = '1') and Pre_charge is activated (Pre_charge = '0'). As a result, P2 in Fig. 17(e) is turned off to block the boosting current and P3 is used in a similar fashion as in the conventional design. When MODE = 0, Pre_charge is deactivated (Pre_charge = '1') and Pre_discharge is activated (Pre_discharge = '0'). Thus, P2 is utilized for the RBL boosting current.

B. Measurement results

For the purpose of comparison, both random and worst-case data patterns are used when testing the proposed 9T SRAM and the 8T design. Measurement result confirms the minimum operating voltage (V_{DDmin}) of 0.18 V at room temperate. However, the conventional 8T SRAM with the proposed RBL boosting technique starts to fail from 0.25 V. At 0.18 V, The power consumption and the access time of the proposed SRAM are 1.2 μW and 4.1 μs, respectively.

Fig. 18(a) shows the impact of temperature variations on V_{DDmin}. V_{DDmin} of both designs increases with temperature. The proposed 9T SRAM lowers V_{DDmin} about 65 mV compared to the conventional one, proving the advantages of the data-independent RBL leakage. Fig. 18(b)

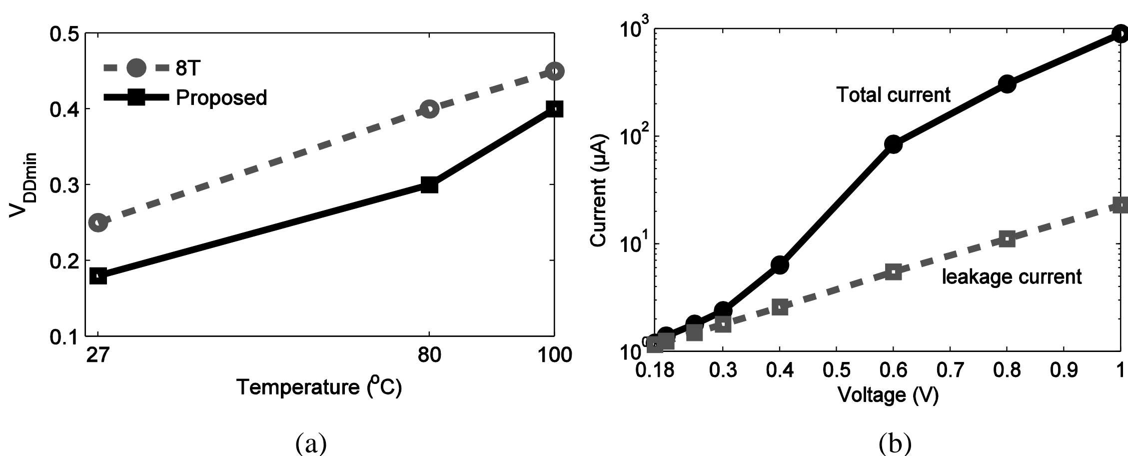


Fig. 18. (a) Minimum supply votlage of the proposed and conventional SRAM at different operating temperature and (b) measured total and leakage current of the proposed design at room temperature.

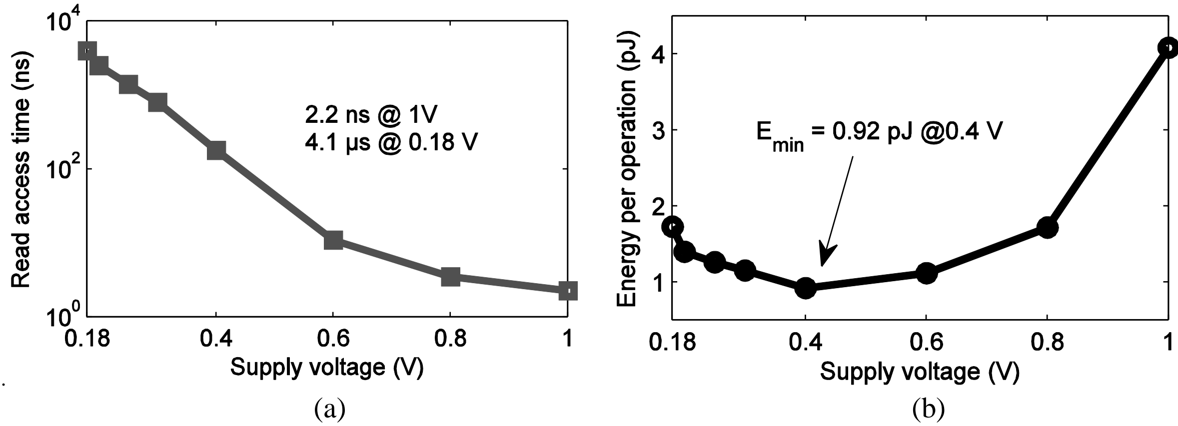


Fig. 19 (a) Measued read access time and (b) minimum energy point of the proposed design at room temperature.

presents the measured total and leakage current of the 9T design. At ultra-low supply (i.e. V_{DD} < 0.4 V), the total power is mostly dominated by the leakage power. Fig. 19(a) shows the read access time and the corresponding energy per access of the proposed 9T design across various voltage conditions. The access time increases exponentially when V_{DD} is scaled below 0.6 V. The minimum energy of the proposed SRAM is 0.92 pJ/access at 0.4 V, as shown in Fig. 19(b).

VI. CONCLUSIONS

This paper introduces several circuit techniques for SRAM RBL sensing margin enhancement at ultra-low voltage operation. The proposed design combines RBL boosting current with data-independent RBL leakage to enlarge the RBL swing and the sensing timing window for reliable sensing. By using the MTCMOS option in the cell topology and the RBL pre-discharge low scheme, the proposed design also reduces both total cell leakage and RBL leakage when compared the conventional 8T design even with LVT devices in the read port. It also improves the RBL swing by at least 35%. The proposed SRAM is successfully functional down to 0.18 V, 27°C with 256 cells per column. The minimum energy consumption is 0.92 J/access at 0.4 V.

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