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LUTETIUM OXIDE (Lu_2O_3) GATE DIELECTRIC FABRICATED BY PULSED LASER DEPOSITION

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A thesis submitted to the
Nanyang Technological University in partial fulfillment of the requirement for
the degree of Doctor of Philosophy

2010

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THESIS SUMMARY

The aim of this project is to investigate the suitability of rare-earth oxide as gate dielectric, in particular Lu_2O_3. There are three main chapters, in which the properties of Lu_2O_3 film, the effect of post-deposition treatments on Lu_2O_3 film as well as the properties of Lu_2O_3 on the next generation of semiconductor substrate are discussed in detail.

The first part covers the basic properties of Lu_2O_3 thin film on Si substrate. The thermal stability of Lu_2O_3 was investigated, in which it was able to remain thermally stable at least up to 900°C, which is close to the annealing step used in CMOS fabrication. The pulsed laser deposited (PLD) film was able to produce good electrical properties, comparable to reported work by other research groups albeit a higher interface density value. In addition, the leakage current conduction mechanism was established to be Poole-Frenkel and the effect capability of traps present in the film to trap and de-trap charges was investigated along with the effect of light illumination on the Lu_2O_3 MOS device.

The second part of this work covers the effect of various post deposition treatment on Lu_2O_3. The compositional changes in the film with the introduction of rapid thermal annealing (RTA) have been investigated by employing high-resolution Rutherford backscattering spectroscopy (HRBS) measurement along with the investigation on the changes on the strain resulting from the heat treatment. Further study on the effect of heat treatment on the band alignment for the interfaces of Lu_2O_3/Si was also investigated in which, an increasing trend on the conduction band offset (CBO) was found. In addition, for the first time the use of laser annealing was introduced as a post deposition treatment for high-κ gate dielectric film from which a significant improvement in the κ value of the Lu_2O_3 was obtained (about 4 times larger in magnitude). The use of laser annealing seemed to have opened up avenues for more materials to be suitable candidates for high-κ gate dielectric films.

The final part of this work investigates the properties of Lu_2O_3 on Ge, which is considered as the next generation substrate for high-speed devices due to the reported high mobility. The material properties of the Lu_2O_3 film were investigated thoroughly through high-resolution transmission electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS) and HRBS. From this study, the presence of Lu-based germanate was confirmed and it was proposed that a critical value of excess Ge present in the film may exist in which, exceeding this value led to the deterioration of the electrical property of the Lu_2O_3 based MOS device.

Lastly, additional works were proposed as part of the continuation of this project.

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ABSTRACT

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ABBREVIATIONS

The following abbreviations are used in this report.

ALD	Atomic Layer Deposition
CVD	Chemical Vapor Deposition
PLD	Pulsed Laser Deposition
RTA	Rapid Thermal Annealing
CMOS	complementary metal oxide semiconductor
MOS	Metal Oxide Semiconductor
AFM	Atomic Force Microscopy
HRBS	High-Resolution Rutherford Backscattering Spectroscopy
HRTEM	High-Resolution Transmission Electron Microscopy
XRR	X-Ray Reflectivity
XPS	X-Ray Photoelectron Spectroscopy
SIMS	Secondary Ion Mass Spectroscopy
C-V	Capacitance versus Voltage
J-V	Leakage current density versus Voltage

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Chapter 1 INTRODUCTION

The evolution of the microelectronic industry has been remarkable. The development of the first planar transistor in the late 1950s has opened up doors on transistors development, which has big impact on our way of life ever since. Owing to the strong demand of more powerful and complex devices to meet our need, we have witnessed the vast improvement on integrated circuit performance today since its introduction in the late 1950s. Gordon E. Moore was the first to predict on such large-scale development in the semiconductor industry. This prediction, which postulate that the number of transistors that can be placed on an integrated circuit has increased exponentially, doubling approximately every two-year is depicted in Figure 1-1 below.[1]

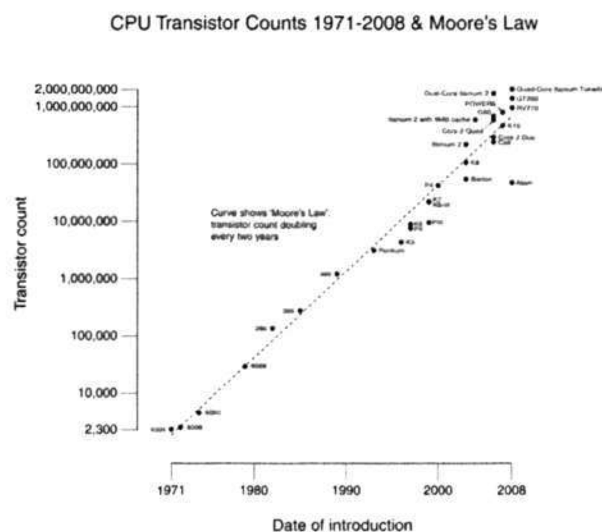

Figure 1-1 Plot of transistor counts against dates of introduction. The curve shows counts doubling every two years.[2]

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The development of the semiconductor industry has thus far followed closely to Moore's law through the shrinking of its critical feature size of the planar process. Therefore, the as the features are shrunk, the more transistors can be packed into a given area. In addition, with the minimization of its most critical feature size, the physical gate length, it has not only made the overall transistor smaller, but improved its speed performance as well. Unfortunately, we are approaching to the upper threshold of that can be done in further downscaling of the silicon dioxide gate dielectrics in order to obtain a better performance device. Presently, the downsizing trend is approaching to its ultimate limit, namely the size of atoms. Since 2005, the gate length of the most advanced commercial complementary metal-oxide semiconductor (CMOS) large-scale integration (LSI) devices is already sub-40 nm. The 2008 edition of the International Roadmap for Semiconductors (ITRS) calls for even more rapid scaling than previously anticipated. Table 1-1 and Table 1-2 show the equivalent physical gate oxide thickness for high performance and low standby power technology as a function of technology node respectively.[3]

Table 1-1. Equivalent physical gate oxide thickness with technology node for high performance devices as stated in 2008 ITRS edition.[3]

Year	2008	2009	2010	2011	2012	2013
Technology node (nm)	29	27	24	22	20	18
EOT (nm)	1.2	1.0	0.95	0.88	0.75	0.65

Table 1-2Equivalent physical gate oxide thickness with technology node for low standby power technology in 2008 IRTS road map.[3]

Year	2008	2009	2010	2011	2012	2013
Technology node (nm)	38	32	29	27	22	18
EOT (nm)	1.6	1.5	1.4	1.3	1.2	1.1

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The one main reason on why Si is a preferred semiconductor used is the fact that SiO_2 forms on Si surface naturally in an oxygen-containing environment. The SiO_2 film would significantly reduce the number of dangling bonds that usually lead to surface states by forming chemical bonds thus removing the states from the semiconductor band gap. This is more commonly known as "electronic surface passivation". Presently, no other semiconductor and film combination has been known to have the same effective electronic surface passivation to the extent of Si and SiO_2 combination. In addition, SiO_2 provides several important characteristics that have allowed its use as gate insulator.[4] Firstly is the excellent control in thickness and uniformity when SiO_2 is thermally grown on silicon, forming a very stable interface with silicon substrate with low density of intrinsic interface defects. Secondly, SiO_2 gives excellent thermal and chemical stability, which is important in the fabrication of transistors, which includes high temperatures annealing steps of up to 1000°C. Thirdly, SiO_2 has a fairly large band gap of ~ 9 eV which makes it an excellent electrical insulator. In addition, SiO_2 has very high breakdown fields, in the order of 13 MV cm^{-1}, which makes it an excellent choice as gate dielectric. Unfortunately, while SiO_2 has been the most popular choice for the Si device gate dielectric, there are a number of known issues associated with the continued scaling for sub 100 nm technology nodes.[4]

1.1 Limitations of SiO_2 as gate dielectric

The previous section has discussed the need of scaling in order to meet performance demand of transistor device. Unfortunately, the scaling of the presently used gate dielectric material is fast approaching its limit. In the research conducted by Muller *et al*,[5,6] it was discovered that the full band gap of SiO_2 is only obtained after two

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monolayers of SiO_2. This finding suggest that within two monolayers of the Si channel interface, oxygen atoms do not have the full arrangement of oxygen neighbors thus unable to form the full band gap that exist within the bulk SiO_2. It was found that the physical thickness limit of SiO_2 is 0.7 nm and if the thickness goes below this limit, it is likely that the Si-rich interfacial regions from the channel and polycrystalline Si gate interfaces used in metal-oxide-semiconductor field effect transistors (MOSFET) would overlap resulting in a short throughout the dielectric, making it useless as an insulator.

In addition, when the physical thickness of SiO_2 is scaled down to below 1.5 nm, the gate leakage current increases rapidly due to the quantum mechanical tunneling mechanism.[7,8] This mechanism involves tunneling of charge carriers through a trapezoidal energy barrier, as shown in Figure 1-2, commonly known as the direct tunneling process.[9] It was shown through the Wentzel-Kramers-Brilloin (WKB) approach that tunneling probability increases exponentially as the thickness of SiO_2 film decreases. This will eventually result in a large increase in the leakage current flowing through the device as SiO_2 layer decreases. In addition, another obstacle facing SiO_2 gate dielectric is its reliability issue. It is known that during the operation of MOSFETs in integrated circuits, charge carriers flow through the device, resulting in the generation of defects in the SiO_2 layer at the Si/SiO_2 interface.[10-12] Therefore, when a critical density of defects has been reached, breakdown (or quasi-breakdown) of gate layer occurs, resulting in the failure of the device.[13-15]

Also, DeGraeve *et al*[13,16] has reported on the fundamental mechanism for oxide breakdown in ultrathin SiO_2 reliability in order to investigate its reliability. The percolation model proposed the cause of ultrathin oxide breakdown could have been

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resulted from the buildup of many "defects" within the SiO_2 layer that could form a complete path of defects across the oxide thickness (percolation) and lead to failure.

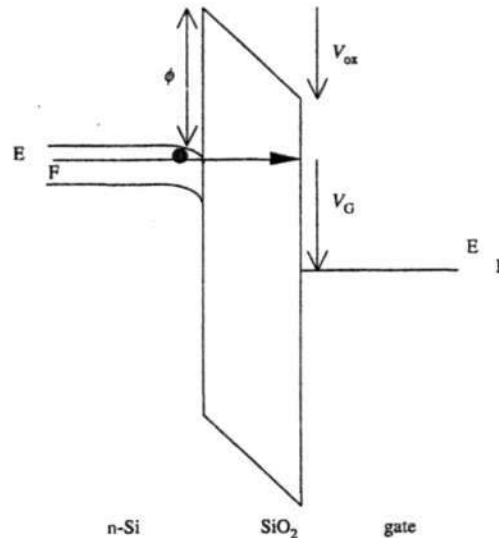

Figure 1-2 Schematic energy band diagram of an n-Si/SiO_2/metal gate structure showing direct tunneling of electrons from the Si substrate to the gate. ϕ is the energy barrier height at the Si/SiO_2 interface, V_{ox} the potential drop in the SiO_2 layer and V_G the applied gate Voltage.[4]

Additional possible problem that could be faced in scaling using SiO_2 would be the boron penetration through the oxide. This is caused by the large boron concentration gradient that exist between the heavily boron doped polysilicon gate and lightly doped Si channel sandwiched between an undoped oxide. This large concentration gradient would lead to rapid diffusion to boron through the thin sub 2 nm oxide layer into the channel. The change in boron concentration at the channel region would in turn alter the device properties such as its threshold voltage, which would make it unacceptable.[17,18]

Finally, we have to bear in mind two important limitations that are valid not only for SiO_2 based material, but for all dielectrics.[19] The first is the electrical thickness, which is defined as the distance between the centroids of charge in the gate and in the substrate.

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This thickness, which is also denoted by t_{eq}, would therefore include the effective thickness of the charge sheet in the gate and the inversion layer in the channel. These effects can therefore add to the expected t_{eq} typically derived from the physical thickness of the dielectric alone[20] which will be shown in the next section. What this mean is that for a given high-κ dielectric with the current CMOS processing techniques, a device should exhibit a t_{eq} value 4-8 Å larger than reported. The second concern is the way feature dimensions have been reduced much faster than operating voltage in device scaling. This has led to an increase of electric field across the gate dielectric. This is further enlarged from the continually decreasing oxide thickness due to scaling. The increased electric field across the dielectric field would eventually pull the carriers in the channel closer against the dielectric interface, which cause increased phonon scattering thus decreasing the channel mobility.

1.2 Alternative gate dielectric

Power consumption and reliability has been the two most important considerations while increasing the performance of transistors with continued scaling. Performance, which is referring to the speed of switching in the transistor, is measured by τ, the intrinsic gate delay. The intrinsic gate delay is related to the gate capacitance C, gate voltage V_g and the saturated drain current $I_{D,sat}$ by the following equation:[21]

$$\tau = \frac{CV_g}{I_{D,sat}}$$ **Equation 1-1**

Also, the saturated drain current is defined by the following equation:[21]

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$$I_{D,sat} = \frac{W}{L}\mu C_{ox}\frac{(V_g - V_t)^2}{2}$$ **Equation 1-2**

where W is the width of the transistor, L is the gate length, μ is the carrier mobility, C_{ox} is the oxide capacitance at inversion, V_g is the gate voltage and V_t is the threshold voltage. It has been known that in order to achieve faster transistor switching, $I_{D,sat}$ should be maximized. Looking at the terms in Equation 1-2 closely, we know that in order to achieve higher drain current, the transistor's width, length and carrier mobility could be optimized. This was already been done by groups working on strained channel regions. The subsequent term V_g-V_t, which is the gate overdrive is very much limited to the dielectric breakdown in high electric fields. It appears then that in order to achieve further improvement in the device, we have to zoom into ways that would help to increase the capacitance across the oxide, C_{ox}. The oxide capacitance is defined as shown below:[20]

$$C_{ox} = \frac{\kappa\varepsilon_o A}{t_{ox}}$$ **Equation 1-3**

where κ is the dielectric constant of the gate dielectric, ε_o is the permittivity of free space, A is the area of the gate electrode and t_{ox} is defined as the thickness of the oxide. Analyzing Equation 1-3 closely, it can be easily seen that in order to achieve a higher capacitance across the oxide, one approach would be to decrease the oxide thickness, while the other approach would be to increase the dielectric constant. It has been discussed in previous section that decreasing the oxide thickness has very much approached its threshold, and that further reduction could result in carrier tunneling through the oxide. Moreover, high leakage current degrades device performance in terms

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of its reliability, operation speed and standby power among others. The other possible and more plausible approach in this case would be to replace SiO_2 with a material with higher dielectric constant above 3.9, which is SiO_2 dielectric constant value. The expression in equation 3 can be re-written as t_{eq}, also known as equivalent oxide thickness and κ_{ox}, the dielectric constant of SiO_2 of the capacitor. The term t_{eq} represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric material assuming that issues such as leakage current and reliability are ignored. Therefore, the actual physical thickness needed from the alternative dielectric used can be found using the expression as shown:[18]

$$\frac{t_{eq}}{\kappa_{ox}} = \frac{t_{high-\kappa}}{\kappa_{high-\kappa}}$$ **Equation 1-4**

High-κ dielectrics have been hailed as a technology milestone that is likely to have an impact on future economics of the electronics industry. The use of high-κ material would not only involve material change in the gate dielectric, but possibly also the physical structure of the transistor as well as the substrate. The importance of having a reduced gate leakage current while keeping the same equivalent oxide thickness (EOT) is therefore emphasized.

High-κ dielectric films will play an integral part of the semiconductor device fabrication in the near future. Within the semiconductor industry itself, high-κ materials have already been extensively studied and replacements of SiO_2 as gate dielectric will be coming soon enough. High-κ dielectric films have also been studied to be used in Ge and III-V semiconductor substrates because the native oxides of substrates are found to be

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unsuitable for electronic applications. While it seems likely that high-κ materials will play a pivotal role in the semiconductor industry, there are still a number of critical issues that need to be addressed before an alternative gate dielectric can be integrated or selected in future generation devices and processes. Some of the most commonly known problems associated with high-κ dielectrics are:[4,18,22]

- Micro-crystallization and phase separation in silicates during heat treatment that is likely to cause increase in gate leakage current.
- Interfacial layer growth during deposition or post deposition heat treatment.
- Lateral oxidation or growth of silicates at the edge of the gate stack.
- Non-uniformity and defects in the deposited film.
- Fixed charges inside the high-κ film inducing large flat-band voltage shift and mobility degradation in the device.
- High interfacial states that may lead to Fermi level pinning.

Therefore the high-κ material chosen has to fulfill certain criteria. As a general outline, the material must have a high permittivity of more than 10. Another important consideration would be its conduction band offset ΔE_c. The ΔE_c would give a good indication whether the material chosen will be a good insulator and result in low leakage current value. Increased performance in a device is often met with a rising heat generation in the device. This heat is often generated partly due to the resistive heating from the resulting leakage current through the gate dielectric. In general, the conduction band offset value should be larger than 1 eV for the material to be considered for SiO_2 replacement.[18] It follows that the larger the offset, the less likely that carriers would tunnel through the oxide. As a rough guide, for high performance processors, leakage

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current density (J) values are typically below 2 A/cm^2, whereas for low standby power applications J should be below 10^{-3} A/cm^2.

Other important requirement for the suitable high-κ material is that it should give a low interface state densities when deposited on the substrate. Common problem found on substrate is that the termination of regular crystalline lattice at the surface often results in a large number of unsatisfied chemical bonds also known as dangling bonds. Typically the number of these dangling bonds is about 10^{15} $/cm^2$ [23] which is of the order of surface atoms. The resultant dangling bonds are undesirable because they give rise to states within the forbidden gap of the semiconductor.[23] Needless to say, these states could change the operating gate potential of the device. If a large number of states are present, this may prevent inversion of the surface and thus give rise to failure of the device. This is more commonly known as Fermi level pinning.

In addition, the chosen high-κ material should have minimal carrier mobility degradation due to physical scattering by defects that form in the film during deposition. More importantly, the high-κ material should be thermodynamically stable on Si during deposition and subsequent processing.[18] As part of transistor fabrication process involves a very high thermal budget of nearly 1000°C, we would want our high-κ material to be stable at high temperature with minimal alteration to its properties.

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1.3 Rare earth oxides as gate dielectric

Lanthanide oxides are desirable high-κ candidates for gate dielectric because of their fairly large band gap, high dielectric constant and low leakage current density.[24-27] Typical rare-earth oxides are shown in Figure 1-3.

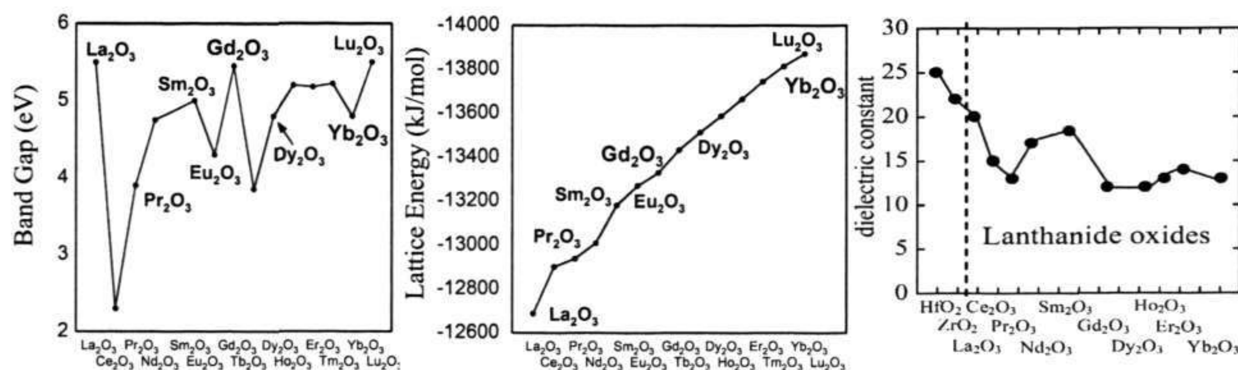

Figure 1-3 Properties of the Lanthanide group. The Lanthanide groups showing large band gap, high lattice energy and large dielectric constants.

Some of the lanthanide oxides show good characteristics without the pre-formed interfacial layer, and are regarded as possible candidates for next generation high-k dielectrics.[28] From Figure 1-3, it can be observed that among the lanthanide oxides, Lu_2O_3 has the highest lattice energy (-13871 kJ/mol) and the largest band gap (5.5 eV).[29-32] Based on the properties information of Lu_2O_3, we would expect Lu_2O_3 to have superior hygroscopic and thermal stability in addition to lower leakage current density when compared to other lanthanide oxides films. Previous report on Lu_2O_3 has shown relatively high κ value of around 11.[28] Numerous methods of the film deposition such as high-temperature oxidation of metallic film[33], ultrahigh vacuum electron beam deposition[28], and atomic layer deposition[34] have previously been explored.

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One common problem associated with rare earth oxide is its hygroscopic stability. It has been reported that lanthanide oxides react readily with moisture to form hydrides ($Ln_2O_3.H_2O$) and eventually hydroxides ($Ln(OH)_3$). In addition, lanthanide carbonate has been known to form on the surface upon exposure to CO_2 gas. Unfortunately, these hydride, hydroxide and carbonate are likely to have a low-k value and therefore there is a need to minimize contact of the samples with moisture/air so as not to degrade the dielectric quality.[35]

1.4 Objective

The objective of this research is to explore new materials, in particular rare-earth oxides as gate dielectric for nanoelectronics applications. This study can be achieved through in-depth study of the material and electrical properties on a MOS fabricated device using pulsed laser deposition as the thin film deposition technique.

1.5 Scope

This report discussed the possibility of using rare-earth oxide material as a suitable candidate for gate dielectric with more emphasis on Lu_2O_3. The dielectric properties of Lu_2O_3 are investigated through electrical and material characterizations. The microstructure characterizations conducted include x-ray photoelectron spectroscopy (XPS), high-resolution Rutherford backscattering spectroscopy (HRBS), transmission electron microscopy (TEM), electrical behaviors were characterized in terms of

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capacitance and leakage current density using LCR meter and semiconductor analyzer amongst others.

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Chapter 2 LITERATURE REVIEW

2.1 Background

The integration of high-κ dielectric into the industry has come sooner than expected. As early as 2003, Intel has announced its intention to integrate high-κ dielectric and metal gate into the 45 nm technology node.[36] Intel believes that in order to meet the demand of better performance but at the same time limiting the power consumption in devices, this is a necessary step to implement. 4 years later, in January 2007, Intel has announced an advanced fundamental transistor design, incorporating hafnium-based high-κ dielectric and metal gate inside its 45 nm technology transistor in the Core 2 Duo processor.[37] This should lead to intensifying the research for the next generation of high-κ materials, in which rare earth oxides should play a prominent role. The following sections will review the development of high-κ dielectrics over the years.

2.2 High-κ gate dielectric development

Many materials have been considered as potential candidates for application as alternative gate dielectrics to SiO_2. As mentioned in previous chapter, there are many criteria that the potential gate dielectric needs to fulfill. Therefore some materials have

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received more attention than others and these materials are summarized in Table 2-1. The properties that are of immediate interest to select the alternative gate dielectric would be its dielectric constant, band gap (the higher the better) and its thermal stability as indicated by the crystal structure at high temperature.

Table 2-1. Properties of high-κ candidates

Material	Dielectric constant	Band gap (eV)	Conduction band offset with Si (eV)	Crystal structure (900°C)	Drawbacks for application
SiO_2	3.9	8.9	--	Amorphous	
Al_2O_3	9	8.7	2.4 eV	Amorphous	low dielectric constant
Y_2O_3	15	5.6	2.2 eV	Cubic	relatively low dielectric constant, thermodynamic instability
					low band gap
Ta_2O_5	26	4.5	--	Orthorhombic	thermodynamic instability
					very low band gap
TiO_2	80	3.5	--	Tetragonal (rutile,anatase)	thermodynamic instability
ZrO_2	25	7.8	1.6 eV	Monoclinic	high oxygen diffusivity
HfSiO	11	5.3	--	Amorphous	relatively low dielectric constant
HfON	18	--	--	Amorphous	relatively low dielectric constant
HfSiON	14	--	--	Amorphous	relatively low dielectric constant
HfO_2	25	5.7	1.3 eV	Monoclinic	high oxygen diffusivity
HfAlO	16	--	--	Amorphous	relatively low dielectric constant

Inspection of the materials listed on Table 2-1 suggests that there is no one material that fulfills all criteria as a perfect replacement of SiO_2. One of the earliest material being investigated as suitable high-κ dielectric candidate is Al_2O_3. The most attractive property of Al_2O_3 is its thermal stability on Si even at high temperatures. Al_2O_3 as gate dielectric has been studied extensively by Chin *et al.*[38] One of the findings is that comparing a SiO_2 with 2.1 nm thickness and Al_2O_3 with an equivalent oxide thickness (EOT) of 2.1 nm, a leakage current density of ~10^{-1} A/cm^2 was obtained for the SiO_2 film whereas a leakage

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current density of 10^{-8} A/cm^2 was obtained for the Al_2O_3 film. This is a significant improvement of seven orders of magnitude. However, although the film showed a low stress-induced current (SILC) effects, calculations revealed a high interface trap density (D_{it}) of more than 10^{11} eV^{-1} cm^{-2}. Also, when a thinner physical thickness of about 2.1 nm Al_2O_3 film was deposited, an EOT of 0.96 nm was achieved with an improvement of the D_{it} to about 3×10^{10} eV^{-1} cm^{-2}. In addition, a flatband shift ΔV_{FB} of approximately +600 mV was observed, indicating negative fixed charges present in the film.

Another previously studied material is TiO_2. The high dielectric constant of TiO_2 (κ ~ 80-110) which is attributed to strong contribution from soft phonons involving Ti ions makes it very attractive material to investigate.[39-41] Unfortunately, TiO_2 also faces several problems such as mixed oxidation states of Ti^{3+} and Ti^{4+} that can lead to a reduced oxide. The main drawback from the reduced oxide state is the presence of oxygen vacancies that can act as carrier traps as well as high leakage current paths. In addition, TiO_2 starts to crystallize at temperatures exceeding 400°C and form polycrystalline morphology. Polycrystalline morphology is undesirable because the grain boundaries in the film can act as high-leakage current paths and moreover, the grain size along with orientation changes in the polycrystalline film may perturb the polarization arrangement in the film that lead to changes in its permittivity. Despite the problems that TiO_2 possess, it is still used in some pseudobinary oxides. For example, when lanthanide oxide is used in TiO_x films, it is able to maintain an amorphous state for capacitor applications, even though TiO_2 would typically crystallize at low temperature.[42] There are many encouraging results that show high-permittivity and low leakage currents, in which some of these approaches may be applicable to gate dielectrics.

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Hafnium oxide based dielectric is probably one of the most researched high-κ dielectric materials and it is currently at the forefront to succeed SiO_2. Already, Intel has adopted a hafnium-based material as its gate dielectric for its 45 nm node technology. The more attractive properties of HfO_2 are its high permittivity (κ> 20) and thermal as well as chemical stability in contact with Silicon. As mentioned earlier, Hf based silicates has been known to have dielectric constant of 10 to 15.[43,44] HfO_2 is commonly prepared by adopting chemical vapor deposition (CVD) or atomic layer deposition (ALD) for better control of thickness, conformality and lower temperature requirement.[45] Prior measurement on HfO_2 film using Pt electrode showed that a low EOT of 1.15 nm and leakage current of 1×10^{-2} A/cm^2 at bias of 1 V are obtainable.[46,47] Despite the fact that hysteresis was found to be negligible at certain processing condition, the flat band voltages observed was relatively high. Depending on processing conditions, the flat band voltages obtained ranges from -300 mV[48] to +600 mV.[46,47] The significant flat band shifts were attributed to the presence of positive fixed charge (for negative ΔV_{FB})) and negative fixed charge (for positive ΔV_{FB}) in the films. It was also found that breakdown occurs in HfO_2 layer at relatively low breakdown fields of E_{BD} ~4 MV/cm as was previously reported for thicker films.[49-52] One of the most well-known problem with HfO_2 thin dielectric film is the formation of interfacial layer during deposition and/or post annealing process, due to fast diffusion of oxygen through the HfO_2 film.[53] This has been observed for a CVD grown HfO_2 film, where they observed a growth of 6 – 9 Å thick interfacial layer for all the samples that has gone through post deposition annealing.[45]This was further confirmed by the work of B. H. Lee *et al*[46,47] in which it was observed that the growth of the interfacial layer would contribute an EOT value of approximately 0.5 nm. In addition, significant level of interface states was still observed in the C-V curves at low frequency as shown in Figure 2-1. Furthermore, X-ray diffraction (XRD) data has shown

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that although HfO_2 is amorphous in the as-deposited sample, crystallization has been observed when the film is annealed at 700°C. As mentioned previously, crystallization in the film is highly undesirable due to the higher leakage current. Most of the problems faced by HfO_2 was almost eliminated by using nitrogen-doped Hf-silicate of $HfSi_xO_yN_z$ and is poised to be adopted by the industry soon.[43] However, due to the presence of the interfacial layer, it has a relatively lower κ value and it is likely that this will be just a short-term solution. Nevertheless, Intel's adoption of hafnium-based high-κ dielectric has brought about significant improvement in device performance.[54] Intel's presentation in the year 2007 indicated that it provides more than 20% increase in drive current as well as reducing the source-drain leakage by five times or more thereby enhancing the energy efficiency of the transistor.[54] Moreover, the adoption of Hafnium-based high-κ gate dielectric has enabled the transistor density to be doubled as compared to previous generation. As a result of the smaller transistor, the switching time is improved by 30% and less energy in consumed by the device.[54]

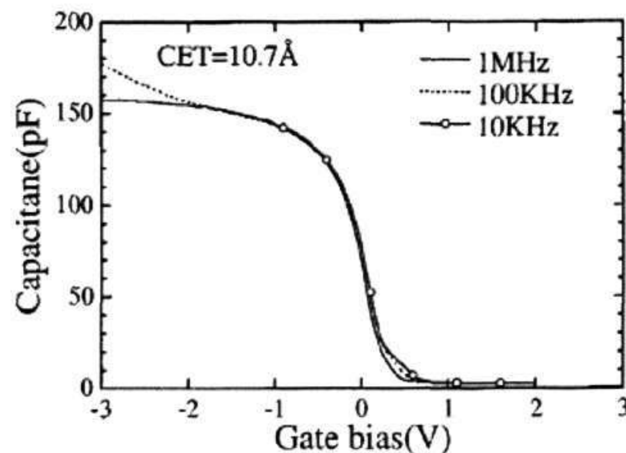

Figure 2-1 C-V curve of HfO_2 after rapid thermal anneal at 600°C. The dispersion for V_G< -2 V is attributed to higher leakage. Interface states are observed near V_G ~ 0.5 V.

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In order to realize an EOT of less than 1 nm, other materials such as rare earth oxides has been looked into. Lanthanide oxide films are known to be thermally stable and have shown potential in various fields of technology.[55] As such, lanthanide oxides are considered potential candidates for the next generation of gate oxides due to their high permittivity and stability. There are about 15 elements of rare earth in the periodic table, with atomic number ranging from 57 right up to 71. Characteristic of the rare-earth elements electronic configuration is that their $6s^2$ shell is always occupied, the $5d^1$ configuration is noted in La, Ce, Gd and Lu, and also the 4f shell is filled gradually with increasing atomic number. The extent of which the 4f shell is filled gives rare earth elements its unique characteristic.[56] Rare earth elements with half or fully filled 4f shell, in particular Gd and Lu respectively, seemed to be more stable. Another important property of rare earth elements is that all of these elements have the +3 oxidation state in the solid state. However, some of these elements for example Pr and Tm, are also stable in the +4 and +2 oxidation state respectively. Furthermore, it is noted that for +3 oxidation state atomic radii decreases as the atomic number increases. Table 2-2 below summarizes the value of the ionic radii of the trivalent rare earth element ions.[56]

Table 2-2 Values of the ionic radii in Å of the trivalent rare earth element ions[56]

La^{3+}	Ce^{3+}	Pr^{3+}	Nd^{3+}	Sm^{3+}	Eu^{3+}	Gd^{3+}	Tb^{3+}	Dy^{3+}	Ho^{3+}	Er^{3+}	Tm^{3+}	Yb^{3+}	Lu^{3+}
1.23	1.15	1.14	1.12	1.06	1.06	1.04	1.00	0.99	0.98	0.96	0.94	0.93	0.92

Again, one of the primary concerns for high-κ dielectric is its thermodynamical stability, especially in contact with silicon. What is meant by thermodynamical stability with Si is that at high annealing temperature, if a high-κ is considered unstable, there will be a reaction between the oxide itself and Si, leading to the formation of SiO_2 or SiO_x at the interface. On rare earth oxides, we need to bear in mind one important factor, in

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which, rare earth oxides easily breakdown O_2 found in air or supplied during post annealing processes into its atomic oxygen. This leads to the formation of SiO_x or Si-based compounds.[56,57] The reaction that followed is that SiO_2 or SiO_x would readily react with the rare-earth oxides to form rare earth oxide silicates, which has been proven theoretically and experimentally. This is confirmed in the work of Marsella and Fiorentini in which they calculated the formation enthalpies to ascertain the thermodynamical stability of some rare earth oxides in contact with Si. Their work concludes that the rare earth oxides (La and Lu) are shown to be stable against degradation into silica and metal component as well as into formation of silicide. However, for La in particular, it is not stable against the formation of silicate and this conclusion is very likely to apply to Lu as well, although it was not studied in the report.[58]

Table 2-3 Formation enthalpies (eV per formula unit) of oxides, silicides and silicates. The experimental formation enthalpy of silica is -8 eV.[58]

Cation	Oxide	Silicide	Silicate
Y	-19.41	-2.96	-29.41
La	-18.84	-3.87	-29.74
Lu	-20.18	-2.30	-

The formation of high-κ dielectric silicate formation of rare-earth oxide in particular may have formed through the consumption of the SiO_2 layer. Unlike the more common high-κ oxides such as HfO_2 or ZrO_2, rare earth based oxides readily form silicates.[59] Comparing the Gibbs free energy for ZrO_2 and Y_2O_3, the value for the rare-earth oxide (Y_2O_3) conversion into its silicate form by consuming a SiO_2 interfacial layer is much more spontaneous at -135 kJ/mol[60] as compared to ZrO_2 at -2.96 kJ/mol.[60] It has also been shown that Y_2O_3 and SiO_2 itself are reactive to form silicate layer and the silicate layer

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may react further with SiO_2 as shown in Equation 2-1 and Equation 2-2 below.[59] Another factor to bear in mind is that silicate formation layer is amorphous in nature, even though the rare earth oxide film has crystallized before the actual reaction.[61,62] The formation of the amorphous layer has been attributed to the significant mobility differences of atoms in the film.[63] Therefore, for example, in the case of Y_2O_3 and SiO_2, if Si in Y_2O_3 is able to diffuse freely as compared to Y in SiO_2 and/or Si, in that case Y_2O_3 would have become supersaturated with Si and Y silicate should start to nucleate. However, it forms an amorphous silicate instead if the nucleation barrier of crystalline silicate is high and also if the formation of the amorphous silicate leads to a large change in free energy.[59]

$$Y_2O_3 + SiO_2 \rightarrow Y_2SiO_5 \qquad \textbf{Equation 2-1}$$

$$Y_2SiO_5 + SiO_2 \rightarrow Y_2Si_2O_7 \qquad \textbf{Equation 2-2}$$

As mentioned earlier, +3 oxidation state is the stable state for most rare earth elements in the solid state. The advantage of this property is that the rare earth elements are likely to form a unique stoichiometry which lead to a simpler band structure as opposed to elements with more than one oxidation state which can lead to multiple stable stoichiometries.[56] The optically measured band gap (E_g) of rare earth oxides is shown in Figure 2-2. Previous investigation on single crystal rare earth oxides showed that for stable electronic configurations such as La, Gd and Lu has the highest E_g of approximately 5.5 eV.[30] In the case of Lu_2O_3 thin film, experimental measurement has shown the E_g to be 5.8 eV, which is close to the bulk single crystal measurement.[34]

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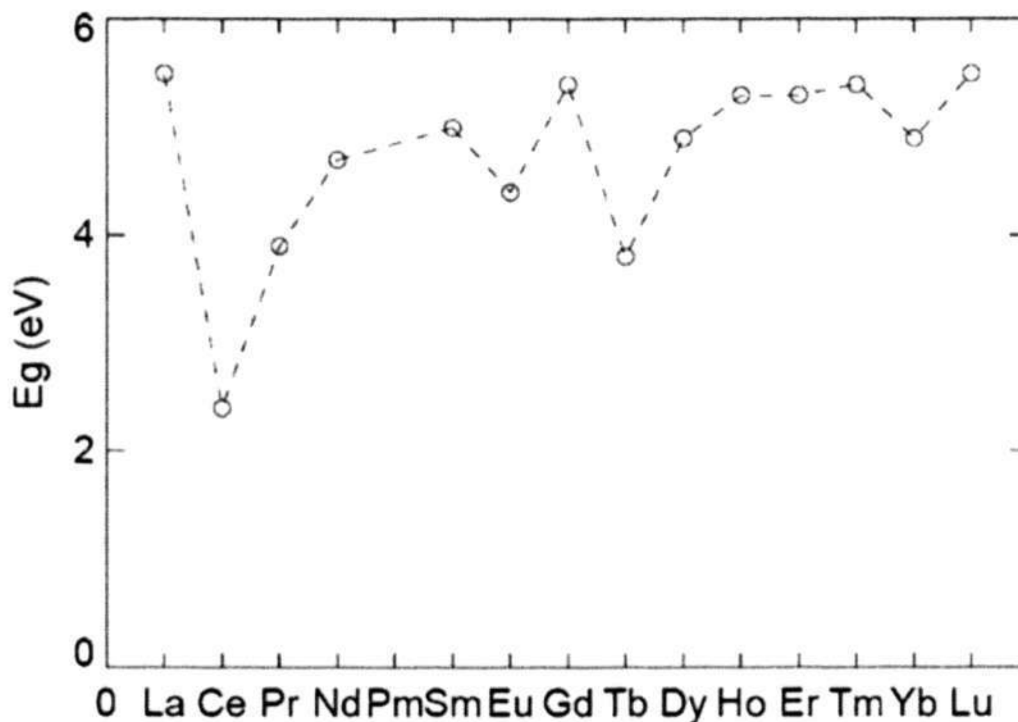

Figure 2-2 Optically measured values of rare earth oxides energy band gap.[56]

The conduction band offset (CBO) is also an important parameter to consider. This is because the conduction band offset is closely related to the leakage current density through the dielectric rare earth oxide film. The higher the CBO, the less leakage current density that we can expect from the rare earth oxide film. Rare-earth oxides have been shown to have a superior conduction band offset (CBO) as compared to HfO_2. Work by J. Robertson has shown that rare earth oxides such as La_2O_3, Y_2O_3 and Sc_2O_3 have a CBO of about 2.36 eV as compared to hafnium oxides' 1.3 eV.[64] This means that rare earth oxides should have a lower leakage current density as compared to HfO_2. This was attributed to the stoichiometry ratio of metal:oxygen, in which the 2:3 metal:oxygen ratio in rare earth oxides seemed to be more favorable as compared to the 1:2 ratio in HfO_2 on Si, promoting higher CBO value.[56] H. Nohira *et al* and T. Hattori *et al* have also studied the conduction band discontinuity of some rare earth materials on Si experimentally by

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X-ray photoelectron spectroscopy (XPS) by using depth profiling method.[65,66] Their findings revealed a CBO of about 2.3 eV for La_2O_3 and 3.1 eV for Gd_2O_3. These findings are consistent with the values obtained by J. Robertson's group. In addition, they have also determined the conduction band offset for Lu_2O_3 value of approximately 1.9 eV. The work on Lu_2O_3 band discontinuity by G. Seguini et al revealed a higher CBO of about 2.1 eV.[67] All these findings confirms that rare earth oxides showed better conduction band offset than HfO_2 and therefore are expected to show better leakage current density behavior. That being said, caution must also be exercised for rare earth oxides with lower E_g as compared to La_2O_3, Gd_2O_3 and Lu_2O_3 as whether the degree of the electron occupancy in the f shell affects the CBO value still needs to be clarified.[56] The leakage current densities of several rare earth capacitors plotted against its EOT and compared with some commonly used high-k dielectrics are shown in Figure 2-3.

The κ value of dielectric materials are very closely related to the frequencies of its main infrared optical modes, which lead to the materials crystalline structure.[68] The rare earth oxides with lower atomic number are stable in its hexagonal structure (La_2O_3 to Pr_2O_3). The middle element Nd_2O_3 is stable in a hexagonal or cubic structure, whereas the tailing group from Sm_2O_3 to Lu_2O_3 is stable in the cubic bixbyte structure, which is the most stable of the group. However, we need to bear in mind that distortion in the cubic structure is possible.[69] The κ value would very much depend on the intensity of the absorption band at lower frequencies. For instance, La_2O_3 who has hexagonal crystalline structure, showed the most intense transverse optical mode at around 200 cm^{-1} while Lu_2O_3 with cubic bixbyte crystalline structure showed intense traverse optical mode only at around 300 cm^{-1}. Expectedly, La_2O_3 showed a more superior κ value of about 17 - 20 whereas Lu_2O_3 κ value is about 12.[56,68] However, one very important factor to bear in

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mind is that the κ value has been known to vary largely with film deposition method, thickness, purity among other factors playing a major role.[56]

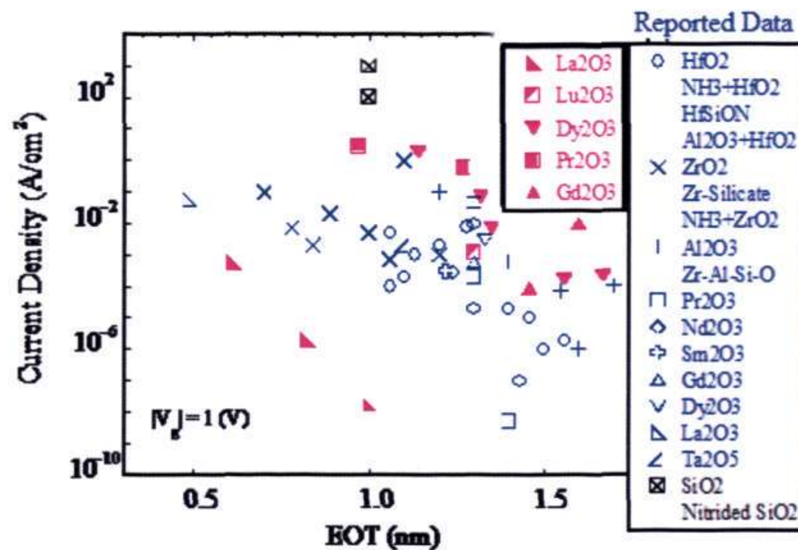

Figure 2-3 Summary of Leakage current densities against its EOT for rare earth oxides.[35]

For example, for La_2O_3 film that was prepared using electron beam deposition with thickness ranging from 2 nm to 7.8 nm would have an effective κ value ranging from 8 to 23,[70] while a La_2O_3 film prepared using metal-organic CVD shows a maximum κ value of just 19.[71]

Despite the issues and limitations discussed above, the investigation of the electrical characteristics of rare earth oxide film has recently been intensified. Works on various rare-earth oxides such as La_2O_3[72,73], Lu_2O_3[28,34], Nd_2O_3[72,74], Sm_2O_3[72,74-76], Y_2O_3[72,75,77,78], Pr_2O_3[72,74,79], Gd_2O_3[72,73,77,78,80-82], Er_2O_3[72,83-85] andHo_2O_3[72,86], have been reported. The calculated EOT in these works are typically in the range of 1 to 2.5 nm.[77-79,84] A low EOT of 0.5 nm has also been reported for La_2O_3[73] which makes rare-earth oxides an interesting material to be investigated for gate dielectric purposes.

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Päiväsaari *et al* has worked on a relatively thick rare-earth oxide films of about 50 nm.[55] The results of the capacitance-voltage (C-V) for Al/rare-earth oxide/native SiO_2/n-Si (100)/Al structure using a signal frequency of 500 kHz are shown in Table 2-4.

Table 2-4 Results of the C-V measurements for different materials of Al/Ln_2O_3/native SiO_2/n-Si (100)/ Al capacitor structures with ac signal frequency of 500 kHz.[55]

Material	T/°C	d/nm	C_{ACC}/fF μm^{-1}	V_{FB}/V	ΔV_{FB}/V	ε_r
Nd_2O_3	310	56	336	−2.2	0.70	10.4
Sm_2O_3	300	50	360	0.1	0.20	10.0
Eu_2O_3	300	51	394	−1.1	0.40	11.1
Gd_2O_3	300	50	321	3.9	0.05	8.9
Dy_2O_3	300	47	322	3.5	0.10	8.4
Ho_2O_3	300	50	357	6.1	0.25	9.9
Er_2O_3	300	51	355	6.9	0.30	10.0
Tm_2O_3	300	48	353	6.1	0.15	9.4

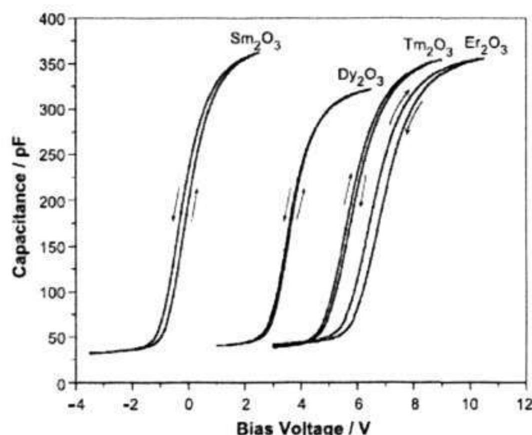

Figure 2-4 A collection of C-V curves of approximately 50 nm thick of some rare earth oxide materials.[55]

Both accumulation capacitance C_{acc} and flat band voltage V_{fb} can both be determined from the C-V curves itself. From the C-V curves of Sm_2O_3, Gd_2O_3, Er_2O_3 and Tm_2O_3 shown in Figure 2-4 taken from the work of Päiväsaari *et al*[55] revealed that apart from Sm_2O_3, the flat band voltages of the rare-earth oxides showed a deviation from the

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ideal flat band voltage for Al/insulator/n-Si (100)/Al capacitor of about -0.2 V.[87] Instead, the observed flatband voltages varied between -2.2 V for Nd_2O_3 to 6.9 V for Er_2O_3 as shown in Table 2-4. Varying the measurement frequency to 100 kHz does not seem to affect the accumulation capacitance significantly, apart from the observed shift in the V_{fb} towards a more negative value. The summarized result for the lower frequency measurement is summarized in Table 2-5. The calculated κ values showed little variance, ranging from 8.4 for Dy_2O_3 to 11.1 for Eu_2O_3, which is consistent with the findings shown in Figure 1-3. In addition, the leakage current densities for the relatively thick 50 nm films were in the order of 10^{-7} to 10^{-9} A/cm^2. The results obtained for the leakage current densities are summarized in Table 2-6.

Table 2-5 Summary of C-V results for different Al/Ln_2O_3/native SiO_2/n-Si (100)/Al capacitor structures with ac signal frequency of 100 kHz.[55]

Material	T/°C	d/nm	C_{ACC}/fF μm^{-1}	V_{FB}/V	ΔV_{FB}/V	ε_r
Nd_2O_3	310	56	338	−2.5	0.75	10.5
Sm_2O_3	300	50	364	−0.2	0.3	10.1
Eu_2O_3	300	51	394	−1.4	0.45	11.1

Table 2-6 Summary of leakage current densities taken at + 1V bias obtained from J-V measurements of various Ln_2O_3 films deposited on n-Si (100) substrate by atomic layer deposition.[55]

Material	T/°C	d/nm	J/A cm^{-2}	E_{BD}/MV cm^{-1}
Nd_2O_3	310	56	3.2×10^{-9}	1.32
Sm_2O_3	300	50	1.1×10^{-8}	0.38
Eu_2O_3	300	51	5.8×10^{-9}	0.37
Gd_2O_3	300	50	1.4×10^{-7}	1.04
Dy_2O_3	300	47	4.8×10^{-9}	1.40
Ho_2O_3	300	50	1.2×10^{-8}	2.06
Er_2O_3	300	51	7.4×10^{-8}	1.49
Tm_2O_3	300	48	1.1×10^{-7}	2.10

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S. Ohmi *et al*, has investigated thinner oxide films of La_2O_3 and Yb_2O_3.[70] In this work, La_2O_3 has shown excellent electrical properties with small EOT as well as low leakage current density with relatively smooth film surface and interface even after rapid thermal anneal (RTA) at 400-600°C. On the other hand, the surface for Yb_2O_3 was found to be easily roughened after the RTA process, even at low thermal budget of 400°C. In addition, the leakage current density for Yb_2O_3 was found to be higher as compared to La_2O_3. The difference in the electrical characteristic was attributed to the intrinsic material properties such as its band gap and its lattice energy. As discussed earlier in the section, the structural properties of the high-κ dielectric would have an effect in the κ value determination. A typical electrical characteristic of La_2O_3 is shown in Figure 2-5. The La_2O_3 sample that was deposited at an elevated temperature of 250°C followed by a 600°C anneal in oxygen ambient showed a leakage current of 1.7×10^{-8} A/cm^2 with a calculated EOT of 1.26 nm. The excellent leakage current density is attributed to the formation of high quality La-based silicate layer at the La_2O_3/Si interface along with densification of the film.[70] The hysteresis observed on the C-V curve was also significantly improved to less than 30 mV. On the other hand, the sample that was similarly prepared but rapidly annealed at 400°C in N_2 showed a higher leakage current of 5.5×10^{-4} A/cm^2 at +1V bias albeit its lower EOT of 0.88 nm. Despite the excellent electrical characteristics exhibited by La_2O_3, a significant negative flat band voltage shift of about 0.6 to 1 V is still observed, even after annealing at 600°C. The κ value of the 7 nm thick La_2O_3 film was found to be 23, which is close to the reported value elsewhere.[88] It was found however, that the κ value decreased significantly when the physical thickness is reduced. The κ value of La_2O_3 film decreased to just 9 when the physical thickness of the film is 2 nm. This was speculated to have been caused by the formation of low quality silicate layer and also due to the stress effect near the interface that may

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affect the dielectric properties in the film.[88] In the case of Yb_2O_3, the as deposited film, an EOT of 1.3 nm with leakage current density of 1.3×10^{-2} A/cm^2 at 1 V bias was obtained, along with hysteresis of approximately 50 mV, which disappeared when the sample was annealed at 400 and 600°C. The EOT of the Yb_2O_3 increased from 1.3 to 2.6 nm in 400°C RTA, 2.8 nm in 600°C RTA in oxygen ambient and 3.8 nm in 600°C RTA in nitrogen ambient. There is a large V_{fb} shift of about -1.8 V observed in the as-deposited film, which decreased to close to zero V by 600°C annealing process. The shift in the V_{fb} was indication of presence of positive fixed charge in the film. The relative dielectric constant of the thick Yb_2O_3 was calculated to be 14.[88]

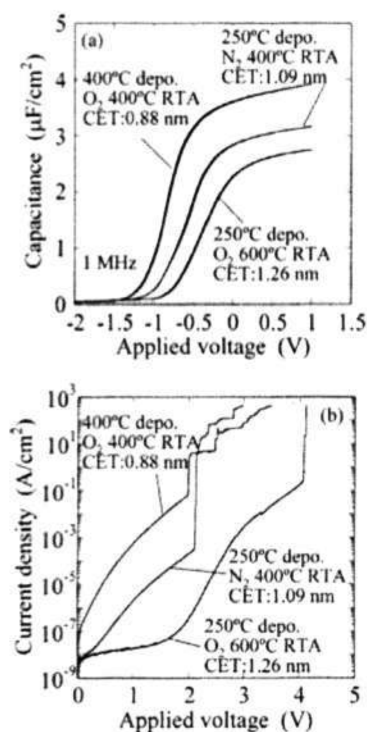

Figure 2-5 Typical electrical characteristic of La_2O_3 deposited on n-Si. (a) shows the C-V characteristic taken with ac signal of 1 MHz and(b) the J-V characteristic of La_2O_3.[70]

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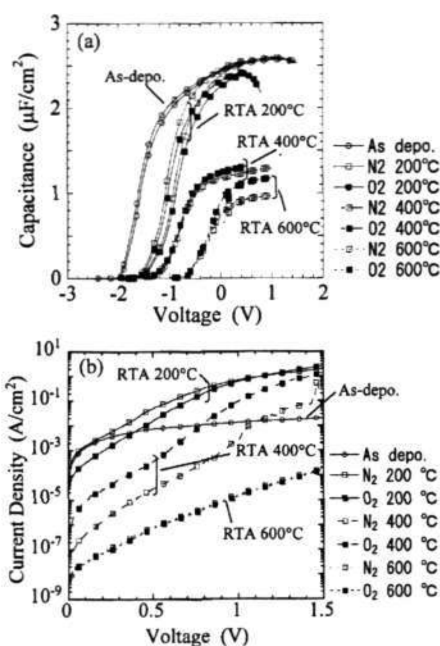

Figure 2-6 Typical electrical characteristic of Yb_2O_3 deposited on n-Si. (a) shows the C-V characteristic taken with ac signal of 1 MHz and (b) the J-V characteristic of La_2O_3.[70]

Lu_2O_3 have also been previously investigated using electron beam deposition as well as atomic layer deposition method.[28,34] It was described in the work of S. Ohmi *et al* that Lu_2O_3 with film thickness of 8 nm and above crystallizes easily after the RTA process at 400-600°C. In addition, it was observed that the surface roughened for 8 nm thick film while the film for the 4.5 nm thick film remained smooth, even after the RTA process.[28] From the C-V measurement data, no hysteresis was observed. In addition, a leakage current density of 2.5×10^{-3} A/cm^2 was obtained for the sample annealed in nitrogen ambient while a leakage current density of 4×10^{-3} A/cm^2 was obtained for the sample annealed in oxygen ambient, both at 600°C. A reduction of the EOT from 2.0 (600°C annealed sample) to 1.6 nm was achieved by annealing the sample at lower temperature at 400°C in nitrogen ambient. The dielectric constant was calculated to be 11, which was comparable to reported work elsewhere.[32,89] It was noted that the leakage current density for the sample annealed in O_2 was higher than the N_2 annealed sample at 1

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V bias voltage. This behavior was most likely due to the poorer film quality after the 400°C RTA in oxygen ambient, which lead to a decrease in the capacitance at the accumulation region as observed in the C-V curve.

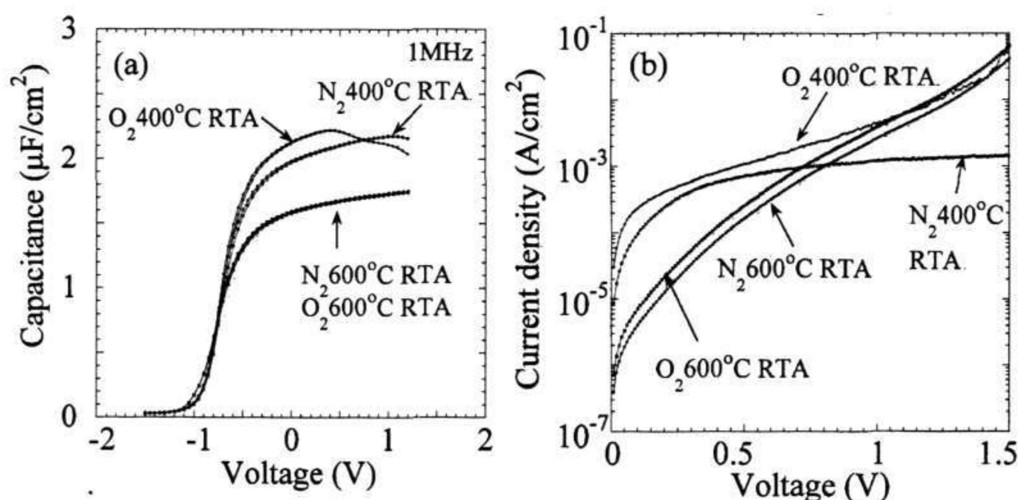

Figure 2-7 Electrical characteristics of 4.5 nm thick Lu_2O_3 on Si followed by RTA process. (a) shows the C-V behavior while (b) shows the J-V behavior.[28]

Although the obtained leakage current density was relatively higher compared to that of La_2O_3[74,90] it was five orders lower than that of thermally grown SiO_2 when compared at the same EOT, which is desirable for the high κ gate insulator application. From the X-ray photoelectron spectroscopy measurement, the lower leakage current densities at the lower electric field region for the MIS capacitor diodes annealed at 600°C could be attributed to the formation of thicker SiO_2-rich interfacial layer compared to that of the films after 400°C RTA.[66,91] From 10 kHz to 1 MHz measurements, no frequency dependence was observed for the film. However, the density of interface states was relatively high (3×10^{12} $eV^{-1}cm^{-2}$), and a significant negative V_{FB} was observed.[28]

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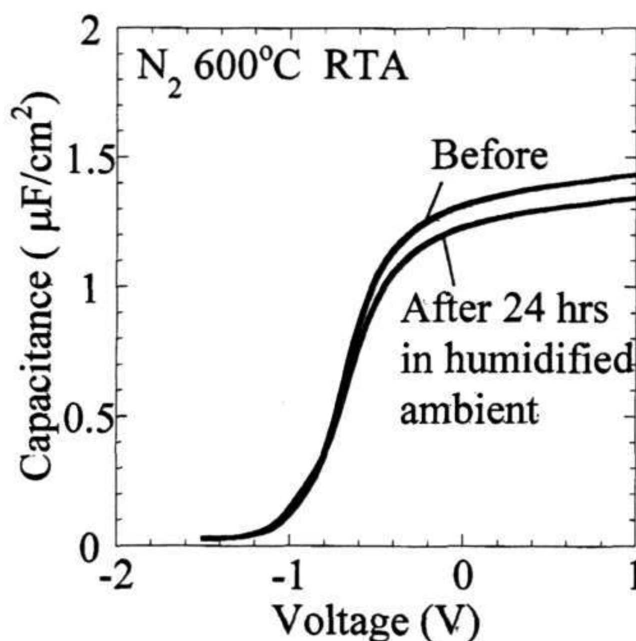

Figure 2-8 Effect of moisture on Lu_2O_3 on its C-V behavior after a 24 hour exposure to humid ambient.[28]

The hygroscopic properties of Lu_2O_3 film were also investigated.[28,35] A 6.5 nm thick Lu_2O_3 was deposited at room temperature followed by a 600°C RTA for ~ 5 minutes in N_2 ambient. The sample was then preserved in humidified environment (80%) at 23°C for 24 hour, after which the Al electrode was formed. The C-V curve revealed that there is a slight decrease in the accumulation capacitance, corresponding to a 0.1 nm increase in the CET for the film after preserving in humidified ambient. The hydroscopic immunity for the Lu_2O_3 film is shown to be more superior to that of the La_2O_3 thin film.[92,93] A more comprehensive study was conducted by Kakushima *et al*, in which an experiment was conducted on various rare earth oxide thin films were kept in acrylic containers with a 80% humidity.[35] It was observed in this experiment that the C-V curves showed significant decrease in the capacitance densities.[35]

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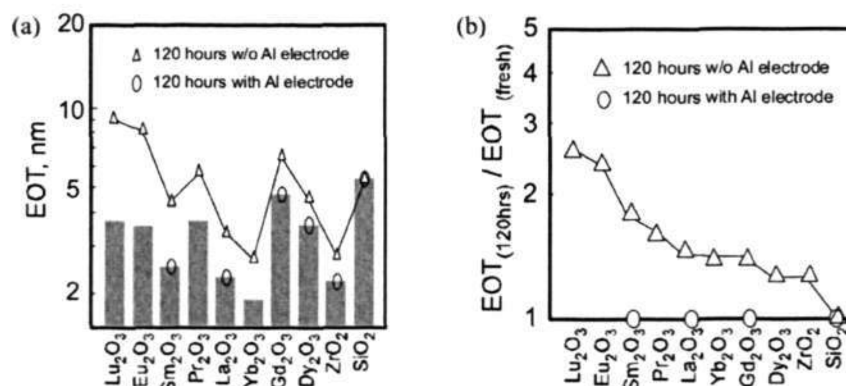

Figure 2-9 (a) A plot of EOT changes of the various rare earth oxides film after exposure to humid ambient for 120 hours. (b) Shows the plot of the EOT ratio of the after moisture exposure for samples between with and without Al electrode.[35]

As observed from Figure 2-9, all of the high-κ materials tested with the exception of SiO_2 suffer moisture degradation after exposure for 120 hours. This experiment suggests that there was a need for treatments or passivations in order to avoid the deteriorating effect from absorption of moisture. Surface analysis using atomic force microscopy (AFM) revealed that the films also suffer an increase in surface roughness after moisture absorption, which leads to an increase in leakage current as observed in Figure 2-10. It is to be noted that from Figure 2-10 that Lu_2O_3, Yb_2O_3, Eu_2O_3 and ZrO_2 appeared to be unaffected by the increase of leakage current and roughness due to moisture absorption. In fact, the data in Figure 2-10 suggests that there may be an improvement in surface roughness and leakage current resulting from moisture absorption. However, the reduction in capacitance remains a concern thus it was suggested that these films need to be coated with passivation layer in-situ right after deposition.[35]

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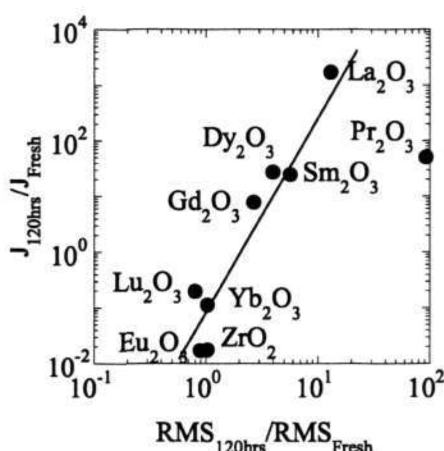

Figure 2-10 A plot showing the change in leakage current density of rare earth oxide materials as a ratio to the surface roughness after exposure to moisture for 120 hours.[35]

2.3 Conduction mechanism

The determination of direct current (DC) leakage current conduction mechanism in high-κ devices plays a pivotal role in the evaluation of device reliability. The understanding on the mechanism behind the DC conduction process would enable us to make good judgment on the device reliability and feasibility under various operation conditions. Therefore, we must not rely solely on the magnitude of the leakage current, although the knowledge of the leakage current magnitude would have been enough to determine the feasibility of the device.

There are several well-known basic DC conduction mechanisms. Several of them are summarized in Table 2-7, showing the mathematical expression for the current and the relationship and/or dependence on voltage and/or temperature is clearly expressed.[94] The conduction mechanism itself is related to the structure itself and therefore is

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dependent on many factors such as its material properties, physical thickness, deposition methodology, annealing or post deposition treatments and its electrodes.

Table 2-7 Basic conduction mechanisms commonly associated with insulators.[94]

Conduction Mechanism	Parameter Dependencies
Ohmic	$J \sim \frac{V}{d}\exp(-\frac{\Delta H_{ae}}{kT})$
Ionic	$J \sim \frac{V}{dT}\exp(-\frac{\Delta H_{ai}}{kT})$
Space-charge limited	$J \sim \frac{8\varepsilon_i \mu V^2}{9d^3}$
Schottky emission	$J \sim A \times T^2 \exp\left[\frac{-q(\phi_B - \sqrt{\frac{qV}{4\pi\varepsilon_i d}}}{kT}\right]$
Poole-Frenkel emission	$J \sim \frac{V}{d}\exp\left[\frac{-q(\phi_B - \sqrt{\frac{qV}{\pi\varepsilon_i d}}}{kT}\right]$
Tunneling emission	$J \sim \left(\frac{V}{d}\right)^2 \exp\left[-\frac{4\sqrt{2m^*}(q\phi_B)^{\frac{3}{2}}}{3q\hbar V/d}\right]$

A = effective Richardson constant, ϕ_B = barrier height, V = applied voltage, d = film thickness, ε_I = insulator dynamic permittivity (square index of refraction), m^* = effective mass, ΔH_{ae} = activation energy of electrons, ΔH_{ai} = activation energy of ions, k = Boltzmann constant, T = absolute temperature.

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One of the most commonly cited DC conduction mechanism in early developmental work is the Poole-Frenkel mechanism.[95] This is especially true for relatively thick film, typically 50 nm or above. Bearing in mind that the 45 nm technology node require the use of high-κ gate dielectric and that the physical thickness of these films are expected to be rather thin in addition to the fact that these materials have lower barrier height as compared to SiO_2, it was predicted that some form of tunneling transport will dominate.

In 1997, Lo *et al* of IBM has presented a quantum-mechanical model of inversion-layer-to-gate current and capacitance in ultra thin oxide NMOSFET's, based on self-consistent solutions of the Scrhodinger and Poisson equations.[96] Based on this approach, Mudanai *et al* extended it to include gate dielectric stacks,[97] using UTQUANT, a self-consistent Schrodinger and Poisson solver developed at the University of Texas, Austin. Fan *et al* has carried out modeling of specific high-κ structures using the same tool. The role of inelastic, trap-assisted tunneling in SiO_2 has been explored by Register, Rosenbaum, and Yang [98] while Houssa *et al* reported the trap-assisted tunneling in ZrO_2 and Ta_2O_5/SiO_2 gate stacks.

The accurate models of the J-V behavior of the high-κ gate stacks can only be accomplished with the sophisticated computer models mentioned earlier. However, the general attributes of the DC conduction can be estimated with the simple expressions as listed in Table 2-7. It is seen in the expression for tunnel emission in the table that the electric field in the dielectric is present in the denominator of the exponential term. This means that effectively, the physical thickness of the film is in the numerator. If we use high-κ film that are thin enough so that their DC conduction characteristic are dominated by direct tunneling, our ability to scale them downward in EOT will be limited by their

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rapidly increasing leakage currents, which will become comparable or even greater than that of SiO_2.

In view of the point above, for films that are thick enough for their DC conduction characteristics not to be dominated by direct tunneling, consideration needs to be given to identify other charge transport mechanisms. The dominant Poole-Frenkel conduction has been identified in recent high-κ films[99] as well as earlier works in similar materials. It is important to bear in mind to reiterate the conditions necessary for a valid determination of the Poole-Frenkel mechanism and the closely related Schottky injection mechanism.

The dominant charge transport mechanism in a film is the one that rate-limits the total conduction process. The establishment of charge transport across a film requires injection of carriers from the injection electrode, transport across the bulk of the film, which is a process that may or may not require recombination-generation processes, and finally a flow of carriers from the film into the second electrode. For example, Schottky emission is the injection of carriers into a film over the interfacial barrier between contact and the insulator, lowered by the image force of the injected carrier. For this interface-limited mechanism to be dominant, transport of the injected carriers across the bulk of the film and into the opposing electrode after its injection must proceed so rapidly and easily that it does not limit the transport. If this is not the case, injected carriers will begin to accumulate in the film, bringing about a bulk-limited space charge limited conduction or situation where the transport is limited by a field-aided hopping process, the Poole-Frenkel effect, or some other bulk-limited mechanism.

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An interesting aspect of the Schottky and Poole-Frenkel mechanism is that while one is interface limited and the other bulk-film limited, they have very similar J-V relationships as can be seen from the equations shown in Table 2-7. From these equations, it can be seen that both mechanisms yield linear characteristics on the J/E versus the square root of the voltage. The primary difference in the two relationships is that the slopes of the plots for the two effects differ by a factor of two, with the Poole-Frenkel effect plot having the steeper slope. The Poole-Frenkel effect, which is the hopping of carriers between the bulk trapping centers having barriers lowered by the applied field has the steeper slope because the distance between the hopping carrier and the center it is escaping is equal to the distance from the carrier to the center, while in the case of Schottky emission, the distance between the carrier and its image charge is twice the carrier's distance from the interface. The factor-of-two difference in slopes originates from this difference in interaction distance.

It is therefore important to consider the slope of the experimental Ln I – $V^{1/2}$ plot in the identification of the relevant conduction mechanism. In this simple form, the slopes for two effects contain only a few well-defined constants; the electronic charge, q, π, the dynamic dielectric constant (the square of the index of refraction of these rapid processes) and the film thickness. The calculation of these slopes is useful to differentiate between the two effects and the magnitude of the slope is a good way to check for the existence of the specified relationship. Also to be noted that Poole-Frenkel mechanism would be linear when Ln J/E is plotted against $E^{1/2}$ and Schottky mechanism would be linear when J/T^2 is plotted against $E^{1/2}$.

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Another important test to determine the validity of citing either Poole-Frenkel or Schottky emission is determining the temperature dependence of the conduction and the changes is the slope on the Ln I versus $V^{-1/2}$ plot. The temperature dependencies are important in differentiating the effects from tunneling phenomena, which is generally have weaker dependence as compared to Schottky or Poole Frenkel effect.

Also, there may be complications in determination the conduction mechanism due to parasitic series resistance, extrinsic film defects and the presence of interfacial layers, which affect the identification of a valid conduction mechanism.

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Chapter 3 EQUIPMENTS AND METHODOLOGY

3.1 Background

In the previous section, the research development on high-κ dielectric was outlined. In this chapter, information on the equipments used to prepare the samples is described. This chapter will focus largely on the deposition of Lu_2O_3 using pulsed laser deposition along with fundamental information on the equipments and/or methods of the sample characterization.

3.2 Thin film deposition technique discussion

Atomic layer deposition (ALD) is one of the most attractive thin film deposition techniques due to its highly desirable advantages such as excellent large area uniformity, comformality as well as strict control on the film composition and thickness in atomic level.[4] Unfortunately despite its many advantages, ALD suffers from the low deposition rate, which resulted from stepwise film growth, where only a fraction of a monolayer is deposited in one cycle. Other disadvantage is that the type of film that can be deposited is limited by the availability of precursors. This means that not every film can be deposited using the ALD as there are considerations on how well the precursors interact with each other which must be well thought out.[4]

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Another deposition technique use in chemical vapor deposition (CVD) in which, gaseous molecular precursors are converted to solid-state materials typically in the form of thin film on a heated substrate. What makes CVD attractive is that the process is simple, highly controllable deposition rates ranging from 1 to 1000 nm per minute, good conformality and the composition can be controlled relatively easily.[4] However, CVD also have its disadvantages. One drawback for CVD is that some of the process may involve complex chemistries, which may not be well understood. Another concern is that as CVD processes involve the decomposition of precursors, the use of proper precursors is therefore vital because a poorly chosen precursors/process may lead to high level of contaminations in the end product.[4]

Pulsed laser deposition (PLD) is versatile method which offers large flexibility in terms of target material, ablation characteristics, target-substrate geometry, ambient gas, pressure, and substrate temperature.[4] The deposition parameters of the PLD such as ambient pressure can be varied of several orders of magnitude. Also, the laser used in the PLD is short pulse length, which enables high laser power densities to be available for the ablation of a wide range of materials. An obvious advantage of the PLD is that it is fast, making it suitable to be used for research as wide range of materials and compositions could be investigated. The process parameters such as substrate temperature, energy density of laser beam, distance variation between substrate and target, and partial gas pressure, are independent variables which have a collective and individual influence on the direct results.[4] Most importantly, the stoichiometry can be maintained during ablation, which makes the adjustment of elements in the target unnecessary. This is the result of an extremely high heating rate of the target surface (10^8 K/s) due to pulsed laser irradiation. It leads to the congruent evaporation of the target irrespective to the evaporating point of

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the constituent elements or compounds of the target. Also, because of the high heating rate of the ablated materials, laser deposition of crystalline film demands a much lower temperature then other film growth techniques.[4] One major drawback on the PLD is the control of surface morphology. It is difficult for the PLD to control the thickness and the roughness of the deposited films down to an atomic scale.[4] Yet, the many advantages of PLD as a thin film deposition technique for research purpose outweigh the drawback and therefore we have decided to adopt PLD as our thin film deposition tool.

3.3 Brief background on pulsed laser deposition (PLD)

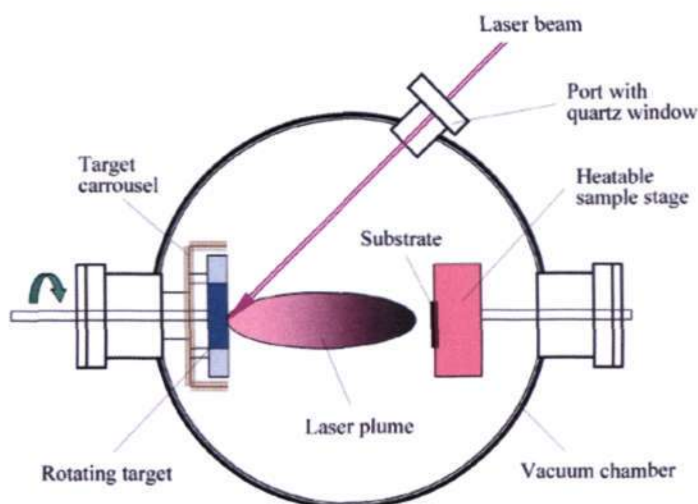

Figure 3-1 A schematic diagram of the pulsed laser deposition (PLD) setup.

Pulsed laser deposition is essentially a physical vapor deposition typically carried out under vacuum condition. The PLD system has been known to provide large flexibility as a thin film deposition technique in terms of availability of target materials, ablation characteristics, target to substrate geometry, choice of ambient gas and adjustable

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substrate temperature. Although the actual setup is rather simple (as shown in Figure 3-1), the principle of the PLD is rather complex. It involves the physical process of interaction between the laser beam and the material and also the formation of the plasma plume with high energetic species and the transfer of the ablated material through the plasma plume onto the substrate surface. The basic mechanism for the PLD can be described in four stages:

1. Laser irradiation interaction with the target.
2. Dynamic ablation of the target material(s).
3. Deposition of the ablated material(s) with the substrate.
4. Nucleation and growth of thin film on the substrate surface.

Each of these stages of the PLD process would contribute a critical role in the formation of a high quality film. The PLD has the advantage of fabricating thin film sample in a short time making it suitable for research as a wide range of materials and composition could be prepared easily. In the thin film preparation, the process parameters such as the substrate temperatures, energy density of the laser beam, partial gas pressure as well as the distance variation between the substrate and target must be optimized. Each of these parameters is independent variable and its individual influence may have a direct influence on the quality of the fabricated film. One of the biggest advantages of the PLD is that the stoichiometry of the target can be maintained during ablation, which makes adjustment of elements present in the target unnecessary. This resulted from the extremely high heating rate of the target surface (~ 10^8 K/s) from the laser irradiation. In addition, the high heating rate will result in a congruent evaporation of the target regardless to the evaporation point of the constituent elements or compounds of the target.

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3.4 Sample preparation methodology

In the preparation of the PLD target, the target material powder was cold pressed into 25 mm pellet and it was subsequently sintered at 1500°C for about 5 hours with slow ramping out rate of about 1°C/min.

Prior to thin film deposition, Si wafer substrates were thoroughly cleaned using the standard Radio Corporation of America (RCA) procedure. Si wafer substrates were subsequently cleaned by dipping inside standard cleaning (SC) solutions 1 and 2 mixtures to remove organic and metal contaminations followed by dipping into 1% hydrofluoric (HF) solution to remove the native oxide. In order to ensure and prevent the formation of SiO_2 interfacial layer before the thin film deposition, the chemically cleaned HF-last Si substrates were immediately loaded into the chamber for the thin film deposition.

The cleaned wafer and the target were loaded into the substrate holder and target holder respectively. After which, the chamber was pumped down to a base pressure of 4×10^{-7} to 5.0×10^{-8} Torr. The laser energy and its frequency were set to a suitable value. Upon reaching the required base pressure value, the target was rotated and the deposition of the film was started. The fabricated samples were then subjected to post deposition processes if required, such as rapid thermal annealing or others. Subsequently, the samples were characterized, for example surface morphology examination using transmission electron microscopy (TEM) or atomic force microscopy (AFM).

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In order to characterize the sample electrically, a metal-oxide-semiconductor (MOS) capacitor device needs to be fabricated. A physical mask was used for the fabrication of MOS capacitor device with circular holes of approximately 0.3 mm diameter. DC magnetron sputtering was used to deposit the gold electrodes. The deposited samples were placed on the substrate holder and covered by the physical mask. The sputtering chamber was pumped down up to 5.0×10^{-6} Torr, after which, a 20 sccm Ar gas was flown into the chamber and the sputtering process was carried out under 7.5×10^{-3}Torr process pressure. One minute long pre-sputter was performed before the sputtering of the metal electrode layer. After which, the back contact was sputtered using similar procedure, except that the back of the substrate was first cleaned using 1% HF solution to remove the native oxide of the Si wafer.

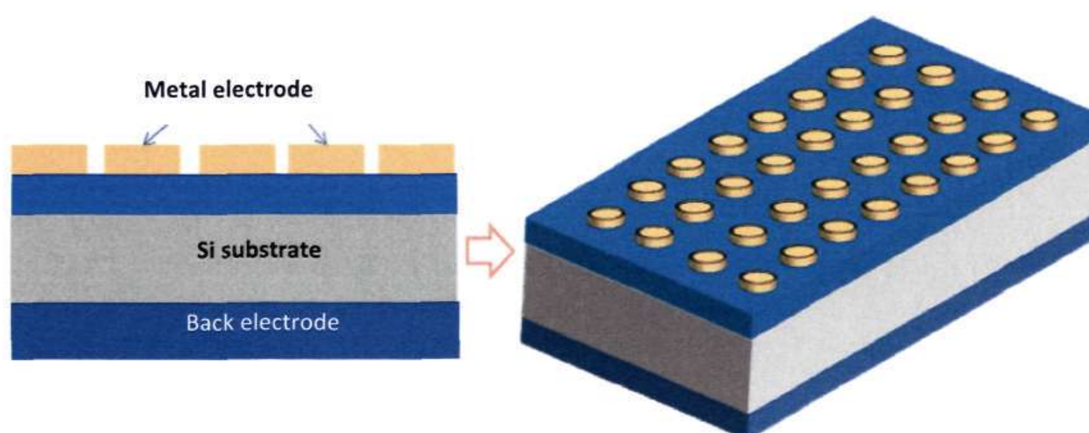

Figure 3-2 A schematic illustration of the fabricated MOS capacitor.

The fabricated MOS capacitor devices (as shown in Figure 3-2) were electrically characterized using precision LCR meter (HP 4284A or Agilent 4980A) at high frequency (100 kHz) and Keithley 236 source meter or Keithley 4200 semiconductor analyzer to measure the capacitance-voltage (C-V) and current density-voltage (J-V) curves respectively. A simplified flow chart of the device fabrication is shown in Figure 3-3.

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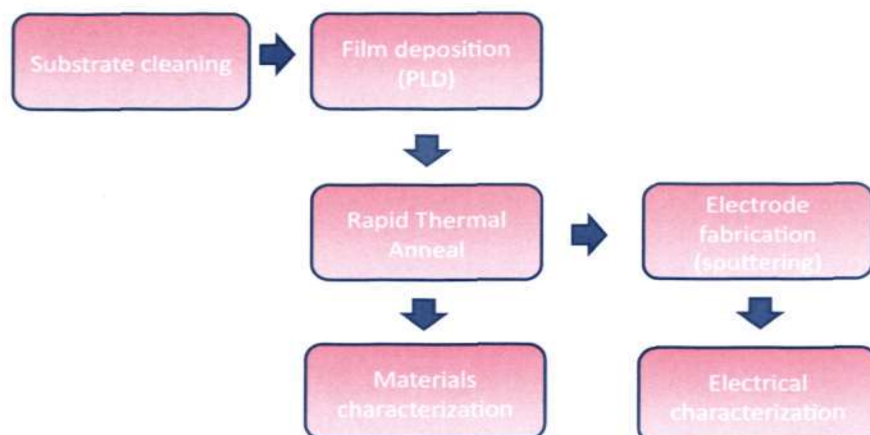

Figure 3-3 A typical flow chart of the MOS capacitor fabrication process and its characterization.

3.5 Post deposition processes

There are two common post-deposition processes that are carried out on the sample following thin film deposition. One of the processes is rapid thermal annealing that is usually done under flowing process gas (oxygen or nitrogen) with 2000 standard cubic centimeters per minute (sccm) flow rate at various temperatures. The temperature in the rapid thermal processor is controlled by a thermocouple and its ramping up rate is set at 40°C/s. The other process is laser annealing. This is done using a Lambda Physik laser that generates KrF excimer pulsed laser anneal with a wavelength of 248 nm and a full width half maxima of each pulse is approximately 23 ns. The laser used for laser annealing has gone through a beam homogenizer that is made up of 8 × cylindrical lens array that will convert the laser's initial profile to a flat top profile such that the resultant laser energy will be uniform across the laser spot size. In addition to the beam homogenizer, in order to ensure the uniformity of the energy density during laser anneal,

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a physical mask was placed following the beam homogenizer to block out the edge of the laser beam where laser intensity may be lower. The laser annealing done in this work was conducted at laser fluence ranging from 0.2 J/cm^2 to 0.3 J/cm^2 for either single or multi pulse(s). The sample was placed inside a mini chamber enclosed with quartz window coated with anti-reflective coating during the laser annealing with a continuous ambient gas purge. As the spot size of the laser beam after going through the focusing lens is 2 × 2 mm^2 and the sample size is much larger at approximately 15 × 15 mm^2, a single pulse of laser anneal would mean that a particular area (2 × 2 mm^2) of the sample is irradiated only once with a particular laser fluence, before exposing to an adjacent area. In a similar fashion, a multi-pulse laser anneal mean that a particular area (2 × 2 mm^2) of the sample is irradiated multiple times at 5 Hz pulse rate, before exposing to other area, also with several pulses.

3.6 Cross-sectional TEM sample preparation

In cross-sectional TEM sample preparation, the substrate with the deposited film was first cut by diamond scriber into 2 × 2 mm size. Two of such substrates were glued together with epoxy glue with the film-side facing the other substrate's film-side. The two slabs were clamped and left to cure on a hot plate (80°C) for about 15 minutes. The cured substrate was then mounted upright on a mechanical grinder, in which one side of the cross section was grinded and polished. The polished side was then mounted on TEM copper backing and the other side was similarly grinded and polished up to 100 μm thickness. The sample was then dimpled and Ar-ion milling was performed in a Gatan

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Precision Ion Polishing System (PIPS). An incident angle of 30° with ion milling time of 2 to 3 hours was typically used.

3.7 Equipment Resources

Several equipments and techniques were used to fabricate and evaluate the electrical as well as material characterizations of the samples. They include the following:

1. Vacuum furnace
2. Pulsed laser deposition (PLD)
3. Rapid thermal processor (RTP)
4. Laser annealing system
5. DC magnetron sputtering system
6. High resolution and analytical transmission electron microscopy (HRTEM) (JEOL 2010 and JEOL 2100)
7. X-ray electron microscopy (XPS)
8. High resolution Rutherford backscattering spectroscopy (HRBS). All work related to HRBS measurement and analysis is done in collaboration with Assoc. Prof. T. Osipowicz and Mr. Chan Taw Kuei from the Physics Department of National University of Singapore.
9. X-ray reflectivity (XRR)
10. Atomic force microscopy (AFM)
11. LCR Meters (HP4284A, Agilent 4980A)

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12. Keithley 236 source measurement unit and Keithley 4200 semiconductor analyzer
13. Secondary-ion mass spectroscopy (SIMS)

Vacuum furnace was chosen to minimize contamination during sintering process of the PLD target. Pulsed laser deposition was used to deposit various thin film materials on the substrate. Rapid thermal processor was used for rapid thermal annealing process for a post-deposition treatment process. Similarly, laser annealing is also used as a post deposition treatment. Metal electrodes and back contact used in the fabrication of MOS capacitor was done using DC magnetron sputtering. HRTEM, AFM, HRBS, XRR, XPS and SIMS were employed for the materials characterization of the samples, which include the surface morphology, thickness of film, depth profile composition analysis, inter-diffusion of elements in the film among others. Finally, the electrical characteristics of the samples were investigated using HP4284A or Agilent 4980A LCR meter as well as Keithley 236 source meter unit or Keithley 4200 semiconductor analyzer unit.

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Chapter 4 PROPERTIES OF Lu_2O_3 HIGH-κ GATE DIELECTRIC ON SILICON

4.1 Background

Back in chapter 2, rare-earth oxides have been shown to have great potential as gate dielectrics. Lu_2O_3 will be discussed in detail in this chapter. The sample preparations for experiments described in this chapter was detailed in chapter 3. Its properties such as thermal stability and electrical characteristics among others will be the main focus of this chapter.

4.2 Thermal Stability of Lu_2O_3

Thermal stability of high-κ material on Si remained one of the most important factors to consider when selecting the material for gate dielectric application. Ideally, there should not be a formation of SiO_2 or SiO_x at the interface, which may lower the overall κ value of the gate stack. The thermal stability of the Lu_2O_3 film was investigated by subjecting the deposited Lu_2O_3 film with thickness about 5 nm to various rapid thermal-annealing (RTA) temperatures. The samples were annealed at temperatures ranging from 500°C up to 900°C with 60 seconds holding time in oxygen ambient. A

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number of characterization tools such as the atomic force microscopy (AFM), x-ray diffraction (XRD) were employed to study the thermal stability of Lu_2O_3 on the Si substrate.

The AFM micrograph revealed a smooth film deposition topology across various annealing temperatures. The root mean square (rms) roughness value showed a downward trend with increasing annealing temperature as shown in Figure 4-1. A rough interface, be it at the high-κ/Si interface or high-κ/metal gate interface, is undesirable. Previous studies have shown that a rough interface at the high-κ dielectric with Si could lead to formation of scattering centers that could lead to reduction in the device mobility.[18] On the other hand, recent study has shown that an increase in the interface roughness at the high-κ and metal gate interface in particular has led to the decrease in the dielectric constant and also an increase in the leakage current density of the MOS stack.[100]

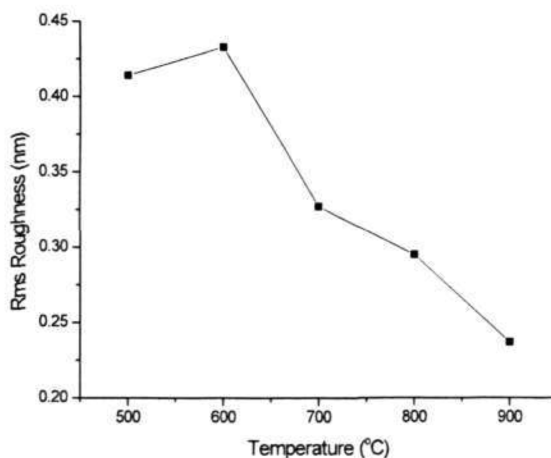

Figure 4-1The root mean square (rms) roughness of Lu_2O_3 film with increasing annealing condition.

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The roughness of the Lu_2O_3 film was expected to decrease with increasing annealing temperature due to the degree of defect alleviation as well as densification of the film associated with higher annealing temperature. The higher annealing temperature would provide higher thermal energy to the atoms, which was likely to cause more efficient migration of the deposited atoms that would in turn provide enhancement in the film densification.

The rms roughness of the 900°C-annealed sample was determined to be 0.24 nm, which is comparable to that of a thermally deposited SiO_2 film.[101] This indicates that the deposited film is both smooth and uniform, without any distinct grain structure. The AFM micrograph obtained from the samples obtained at various annealing condition did not reveal any evidence of crystallization.

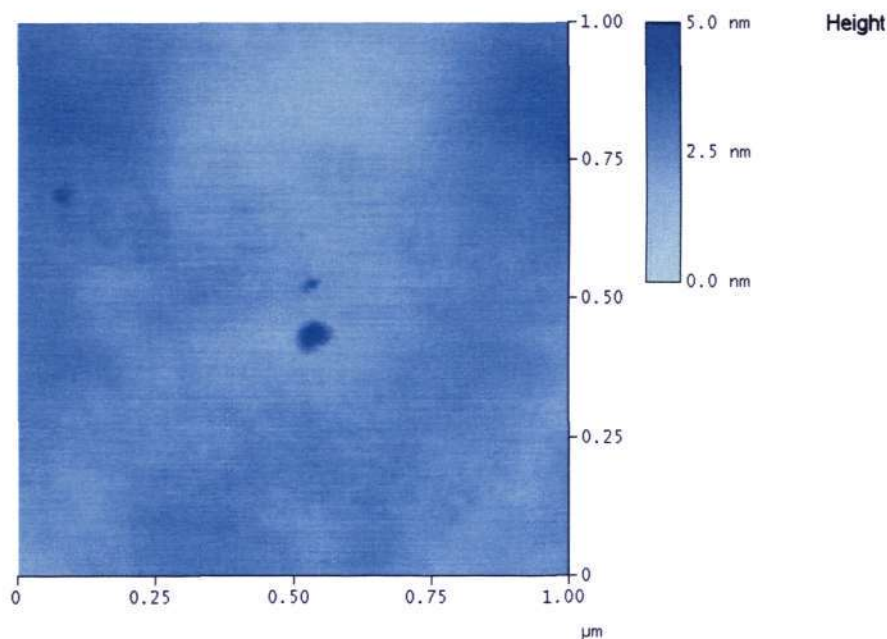

Figure 4-2 AFM micrograph of the Lu_2O_3 film annealed at 600°C in oxygen ambient.

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One of such AFM is shown in Figure 4-3 (a) for the 900°C-annealed sample. In the 3-D view of the AFM micrograph, it can be observed that the film surface was relatively smooth without distinct grain structure. This was further confirmed by the XRD spectra obtained from the same sample in which, no peaks could be detected (Figure 4-3 (b)). The results suggested that the 5 nm thick Lu_2O_3 film was is devoid of agglomeration and/or crystallization after the RTA process. Crystallization in the high-κ gate dielectric should be avoided as the grain boundaries may form leakage path, which would be deleterious to the device as it causes an increase in leakage current density and cause instability in the device.[28] It was speculated that the lattice energy of rare-earth oxides, which determine the crystallization behavior have an important role on the surface roughness property on the deposited thin film. Lu_2O_3 has the largest lattice energy among the rare-earth oxides and was reported to have the tendency to form rigid crystals that lead to agglomeration and/or crystallization.[28] However, it was observed in this work that the Lu_2O_3 films maintain their amorphous state and produce a relatively smooth surface, even after high temperature RTA process. Nucleation and growth of thin films depends on interfacial and strain energies of the nucleus. For a given nucleus cluster, the balance between growth and dissolution depends on the total free energy of the cluster, relative to an assembly of individual atoms. For a reasonably large cluster that can be treated as a continuum solid, the free energy can be written, using Greene's notation as:[102]

$$\Delta G = a_1 r^2 \Gamma_{c-v} + a_2 r^2 \Gamma_{s-c} + a_2 r^2 \Gamma_{s-v} + a_3 r^2 \Delta G_V$$ **Equation 4-1**

Where r is the radius of the cluster, Γ represent interface energies, ΔG_V is the change of volume free energy on condensation of the cluster and a's are constants, depending on the shape of the nuclei. For a three-dimensional crystalline growth, the surface free energy terms have to be positive, in which, unless satisfied, it will be more energetically

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favorable for the film to form as a single layer on the substrate leading to full monolayer growth.[102] In this case, as the film deposition is done on non-heated substrate (room temperature), it is likely that the surface energies of the Lu_2O_3 atoms are too high to allow a critical nucleus to form thereby forming an amorphous monolayer.

A cross-sectional high-resolution transmission electron microscope (HRTEM) micrograph taken for the 900°C-annealed sample as shown in Figure 4-4 revealed a uniform and amorphous film. It was also observed from the HRTEM micrograph that the interface between Si and the high-κ dielectric was abrupt, with little or no observable interfacial layer in between. The HRTEM micrograph had demonstrated that the Lu_2O_3 film would remain thermally stable up to 900°C, which is near the processing temperature of complementary metal oxide semiconductor (CMOS) device fabrication thermal annealing step. Given the fact that the Lu_2O_3 has the highest lattice energy and melting point among the rare earth oxides (2427°C),[103] it is very likely that upon annealing at 900°C, the film remains amorphous because the thermal energy supplied is insufficient to allow a critical nucleus to form and start the crystallization process. In addition, the cooling time for RTA is rather fast (5 – 10 °C/s and taper off at 2 °C/s) is unfavorable for crystallization to occur.

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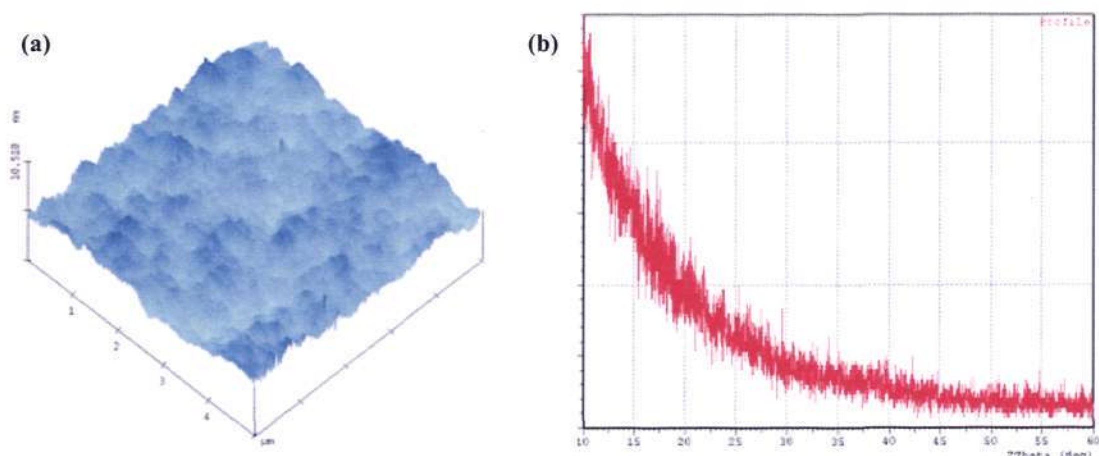

Figure 4-3 (a) AFM micrograph and (b) XRD spectrum of the 900°C-annealed sample of the Lu2O3 film.

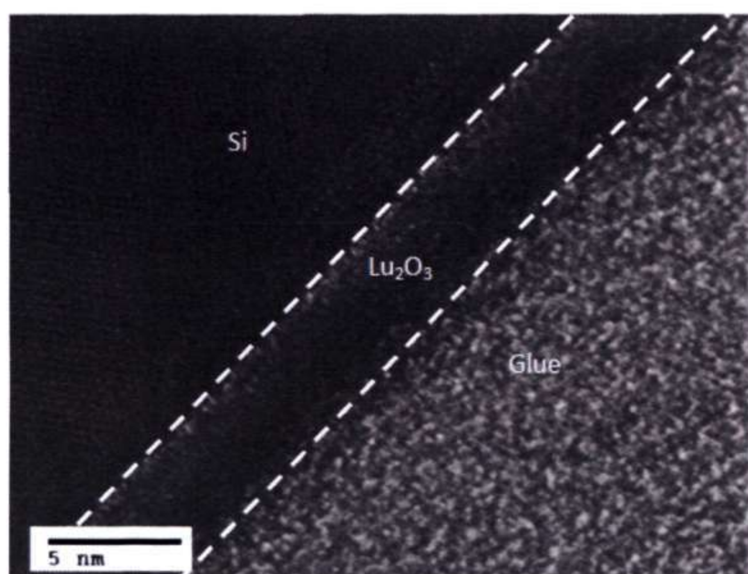

Figure 4-4 Cross-sectional HRTEM image of Lu_2O_3 films on n-type Si (100) revealing an amorphous structure after annealing at 900°C in oxygen ambient.

In order to understand the thermal stability of Lu_2O_3 film on Si, x-ray reflectivity (XRR) analysis was performed on the sample that was annealed at 800°C in nitrogen ambient. The advantage of using XRR is that it is precise, non-destructive analysis tool

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that is has relatively wide penetration depth up to 200 nm and is able to analyze non-transparent films as well. It is commonly used to analyze both single layer and multi layer films for its density, layer thickness, surface roughness as well as interface roughness. Through the analysis of the phase density, the composition of the layer could be analyzed. The XRR spectra the Lu_2O_3 film annealed at 800°C in nitrogen ambient is shown in Figure 4-5. The experimental data and the best-fit simulated spectrum are shown. The simulated spectrum best matched the experimental spectrum when modeled with two-layer structure. Based on the two-layer model structure, a silicate layer was likely to have been formed during the annealing process.

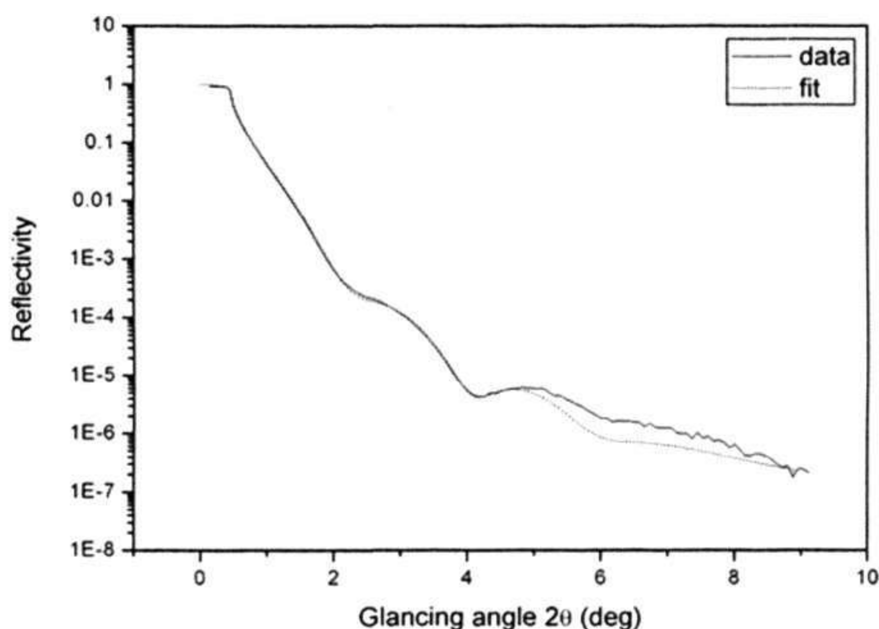

Figure 4-5 XRR spectra showing experimental and simulated data for Lu_2O_3 film annealed at 800°C in nitrogen ambient.

As mentioned in the literature review in chapter 2, rare earth oxides readily breakdown O_2 found in air or supplied during post-deposition process into its atomic

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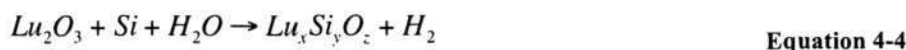
oxygen. Therefore in this case, it is possible that the Lu_2O_3 oxide has broken down residual O_2 found in the annealing chamber into its atomic O. These atomic O atoms will in turn readily diffuse through the film and readily react with Si to form SiO_x. Another possible reaction is that the excess oxygen could have been present in the Lu_2O_3 film in the hydroxide (OH) form. The excess oxygen has been reported to be in the range of several atomic percent therefore promoting the silicon oxidation reaction.[104] In addition, the presence of the excess oxygen in the film is said to shift the effective thermodynamic equilibrium to that which promotes the reactivity of metal oxide with silicon.[104] The following equations outline the possible reactions that might occur at the interface between Lu_2O_3 and Si:

$$Lu_2O_3 + Si + O_2 \rightarrow Lu_xSi_yO_z$$ **Equation 4-2**

$$Lu_2O_3 + SiO_2 \rightarrow Lu_xSi_yO_z$$ **Equation 4-3**



$$Lu_2O_3 + Si + H_2O \rightarrow Lu_xSi_yO_z + H_2$$ **Equation 4-4**

The simulated result from the two layer model in XRR revealed that there was indeed a silicate layer in the Lu_2O_3 film that was annealed at 800°C in nitrogen ambient. The simulated result of the silicate layer composition derived from its phase density analysis is shown in Table 4-1. As observed from Table 4-1, the top layer remained a stoichiometric Lu_2O_3 layer while there is indication of silicate layer growth near the interface for about 2.1 nm. The silicate layer, as shown schematically in Figure 4-6, could have been formed through the diffusion of oxygen from the residual oxygen found in the annealing chamber or excess oxygen present in the film due to absorption of moisture typically associated with rare-earth oxides. This oxygen may react readily with the Si surface to form SiO_x film. Following the formation of SiO_x layer, the Lu_2O_3 film may

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react with the SiO_2 film as shown in Equation 4-4 to form silicate layer. In certain cases, the whole Lu_2O_3 may become silicate layer. However, it was found in this experiment that for the 800°C annealed sample in N_2 ambient, a layer of stoichiometry Lu_2O_3 is still maintained. It was also observed from the XRR analysis that similar roughness was observed on both the top surface of the film (to be in contact with the metal gate) and the interface layer to Si. This showed that the interface roughness could be approximated rather closely from the surface analysis such as the AFM as the quality of the film deposited by the PLD is rather similar.

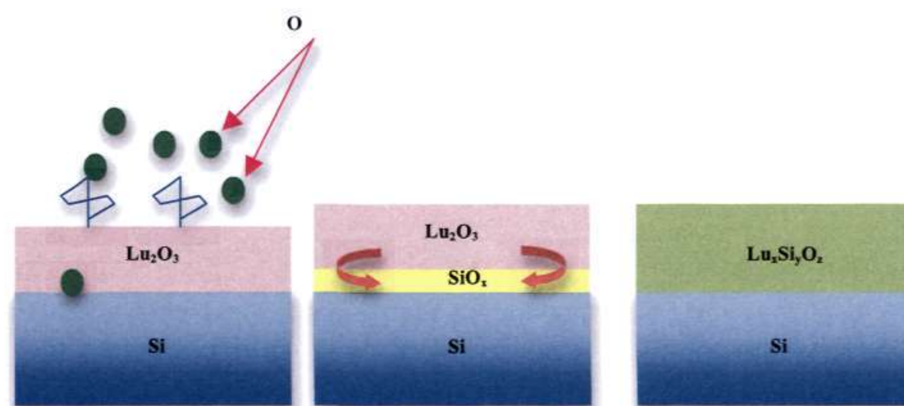

Figure 4-6 A schematic diagram showing the possible formation of Lu-based silicate layer in the annealed sample.

Table 4-1 XRR simulation results for Lu_2O_3 film sample annealed at 800°C in N_2 ambient.

Sample	Layers	Thickness (nm)	Roughness (nm)
800°C anneal	Lu_2O_3	2.2±0.1	0.65±0.08
	$(Lu_2O_3)_xSi_y$, inter-diffused	2.1±0.1	0.50±0.08
	Si substrate		0.1±0.1

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4.3 Basic electrical characteristics of Lu_2O_3

Electrical characterization of high-κ gate dielectric remained one of the most important factors to consider when selecting a material. Typically, a metal-oxide semiconductor (MOS) capacitor structure is fabricated in order to measure the electrical properties of the thin film. In high-κ dielectric research, electrical characterization typically involves two types of measurements. They are capacitance-voltage (C-V) and dc conduction (I-V) measurements. For the C-V measurement itself, important parameters such as the equivalent oxide thickness (EOT), the κ value of the gate dielectric and hysteresis among others can be extracted.

In order to understand the suitability of Lu_2O_3 as a high-κ dielectric film, a C-V measurement was conducted on the Lu_2O_3 MOS capacitor. The Lu_2O_3 MOS capacitor was prepared by depositing ~ 5 nm thick Lu_2O_3 film onto an n-type Si (100) substrate using the PLD. This film was then subjected to RTA at 900°C for about one minute holding time in oxygen ambient. Following the RTA process, a 100 nm thick gold electrode was sputtered on the post-annealed film. The C-V measurement on the Lu_2O_3 capacitor was conducted on a HP4284 LCR meter. In this measurement, a relatively high frequency of 100 kHz was used, along with a voltage sweep of -3 to 3 V bias in order to switch the capacitor from inversion to accumulation. The measured C-V curve for Lu_2O_3 MOS capacitor is shown in Figure 4-7. From the measured C-V curve, the dielectric constant of the deposited Lu_2O_3 film could be evaluated from the obtained accumulation capacitance value, as both thickness and the capacitor area are known.

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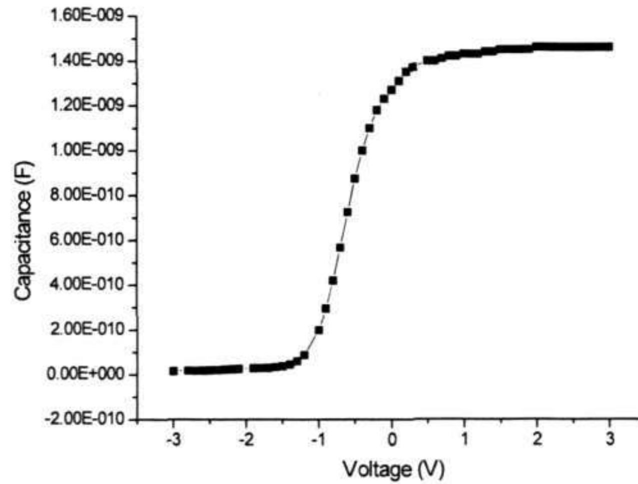

Figure 4-7 Capacitance-Voltage characteristic of approximately 5 nm thick Lu_2O_3 subjected to rapid thermal anneal at 900°C in oxygen ambient.

The capacitance area of the Lu_2O_3 MOS capacitor is 7.07×10^{-4} cm^2. The thickness was obtained from the HRTEM micrograph shown in previous section (Figure 4-4) and it is approximated to be about 5 nm. Without taking into account the quantum mechanical tunneling, the dielectric constant κ could be calculated by applying Equation 1-3 as shown below for convenience.

$$C_{ox} = \frac{\kappa \varepsilon_o A}{t_{ox}}$$ **Equation 1-3**

Where C_{ox} here would refer to maximum capacitance at accumulation derived from the high-frequency C-V measurement curve, κ is the relative dielectric constant of the high-κ thin film, ε_o refers to the relative permittivity of free space, A is the area of the capacitor, and t_{ox} pertains to the thickness of the high-κ thin film. Therefore, solving Equation 1-3 for κ, a dielectric constant of 11.59 was obtained. This value that we obtain experimentally, is comparable to the value previously reported for Lu_2O_3 by other

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research groups (G. Scarel *et al*) using ALD.[34] Assuming that the κ value obtained in the study by G. Scarel *et al* is absolute, the calculated κ value presented in this work gives a relative error of 0.03.

Another important parameter that could be obtained after obtaining the κ value is the EOT, in which, as mentioned in the introduction, gives an indication of the equivalent SiO_2 thickness that is required in order to achieve the same capacitance level as the high-κ dielectric. A low EOT will be preferred for high-κ gate dielectric. However, having a low EOT itself is not sufficient to qualify a material as a suitable high-κ gate dielectric. Other factors such as the leakage current density and interface traps density must also be considered. The equation used to calculate the EOT was found in chapter 1, Equation 1-4. In the equation, t_{eq} refers to the EOT that we are interested in, κ_{ox} refers to the standard SiO_2 dielectric constant, which in this case is approximately 3.9, $t_{high-\kappa}$ refers to the thickness of Lu_2O_3 thin film and $\kappa_{high-\kappa}$ is the Lu_2O_3 dielectric constant that was calculated earlier.

$$\frac{t_{eq}}{\kappa_{ox}} = \frac{t_{high-\kappa}}{\kappa_{high-\kappa}}$$ **Equation 1-4**

Therefore, inputting the parameters into Equation 1-4, an EOT of 1.68 nm was obtained for the 5 nm thick film. The calculated EOT in this experiment was lower that previously obtained by another work on Lu_2O_3 with similar thickness,[28] but annealed at lower annealing temperature of 600°C. The result suggested that the film deposition method and post deposition process chosen in this experiment seemed to provide better insulating properties for Lu_2O_3.

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The flat band voltage (V_{FB}) refers to the voltage that is required to bring the Fermi level of the electrodes and substrate, which is aligned by an energy difference into alignment. According to Wilk *et al*, substantial high-κ films reported in the literature showed a flat band shift away from the ideal C-V curve, which could cause significant issues for CMOS applications. The observed shift is undesirable and must be minimized given the scaling limitation on applied voltages due to power consumption. The gold gate has an accepted work function of 5.31 eV while the work function of n-type silicon with doping concentration ~ 1×10^{16} cm^{-2} is reported to be 5.13 eV,[105] which gives a work function difference of 0.18 eV. The amount of the fixed charge present in a high-κ dielectric film can be related to the measured V_{FB} value as shown in Equation 4-5, where ϕ_{ms} refers to the work function difference between the metal gate and the semiconductor, Q_f refers to the fixed charges in the high-κ dielectric film, and C_{acc} refers to the accumulation capacitance. Therefore, if there is no fixed oxide charge present in the film, the flat band voltage of the Lu_2O_3 film should be equal to the work function difference.

$$V_{FB} = \Phi_{MS} \pm \frac{Q_f}{C_{acc}}$$ **Equation 4-5**

As shown in Figure 4-8, assuming an ideal flat band condition at V = 0, presence of positive fixed charges ($+Q_f$) in the high-κ film would cause a negative flat band voltage shift, while presence of negative fixed charges ($-Q_f$) in the film would cause the flat band voltage to shift in the positive direction. The V_{FB} can be estimated from the C-V curve by first evaluating the estimated flat-band capacitance C_{FB} using the equation proposed by Motorola as shown in Equation 4-6.[106]

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$$C_{FB} = C_{\min} + 0.66(C_{\max} - C_{\min})$$ **Equation 4-6**

In Equation 4-6, C_{min} refers to the minimum capacitance in the inversion region of the C-V curve and C_{max} is the maximum capacitance in the accumulation region. Therefore, by applying Equation 4-6 on the 900°C annealed Lu_2O_3 sample, a flat band capacitance of 9.69×10^{-10} F is obtained. Relating this data on the C-V curve, the corresponding flat band voltage was found to be -400 mV. This shift is away from the ideal V_{FB}, which indicates presence of positive fixed charges (Q_F) in the Lu_2O_3 film, which resulted in a required applied voltage of -400 mV to achieve a flat band condition. The shift, although normally interpreted as presence of fixed charge in the film, could also arise from oxide damage associated with gate electrode deposition, as well as other forms of deposition treatment. However, considering that large ΔV_{FB} values have been measured by many independent groups using different processing conditions and electrodes, it is currently attributed to fixed charge within the film.[18]

The origin of the fixed charge, although not always positive, is believed to arise from excess Si (trivalent Si) and/or the loss of electron from excess oxygen center (non-bridging oxygen) near the Si/high-κ dielectric interface.[18] Therefore, due to the presence of defects at the Si interface, there are some localized states within the forbidden energy gap of Si because the silicon surface is where the properties of the bulk-Si associated with its periodicity terminate. These surface interface trap charges causing the surface potential to bend down below the Fermi level, resulting in the V_{FB} shift.[18]

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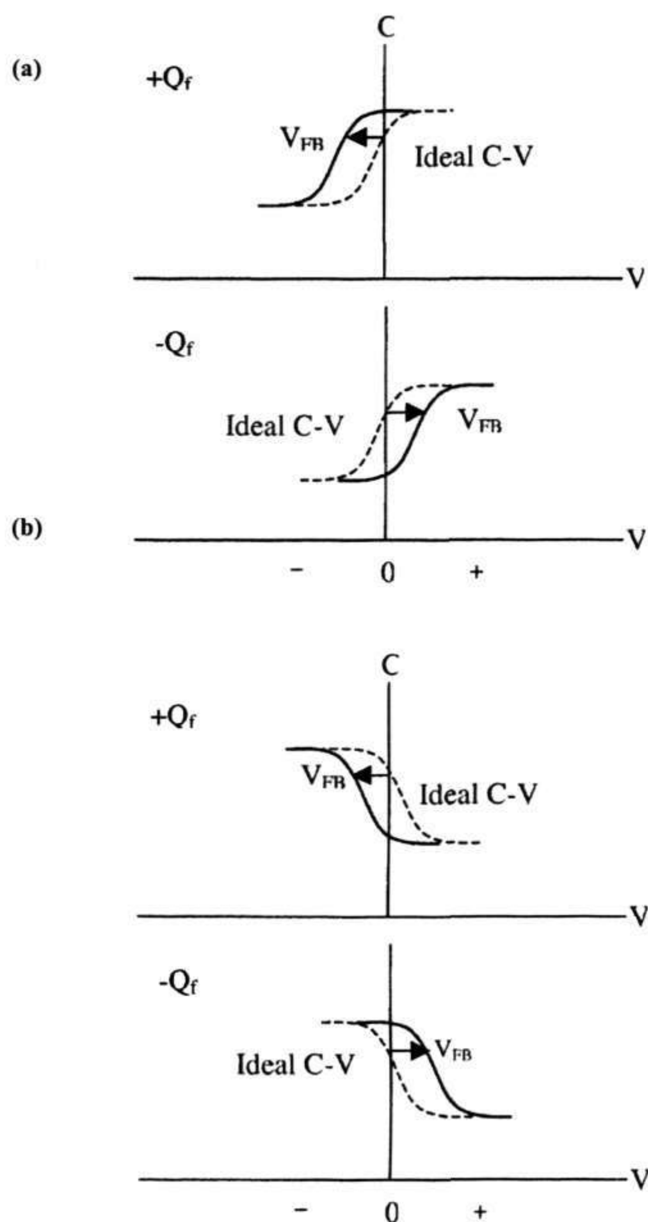

Figure 4-8 High frequency C-V curves in an ideal case (a) n-type (b) p-type.[18]

A large fixed charge in a gate dielectric can have serious outcome on the transistor performance. The reason is because a large fixed charges in the dielectric film could cause the threshold voltage V_T to become too large in order to be compensated with dopant implants. In addition, although it is still debatable whether the observed V_{FB} arise from fixed charges within the high-κ dielectric or some other phenomenon, a large

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amount of fixed charge could have an enormous influence on the viability of their insertion into a CMOS processing. If these high-κ dielectrics have indeed been proven to contain significant amount of fixed charges, then the sign of the charge would become very important as it could affect the device performance.[18] Studies are still on going to determine if indeed there are substantial fixed charges on these films and if so, how to remove it or make it more manageable. One possible solution to reduce the flat band voltage shift in the Lu_2O_3 film is perhaps through the introduction of Al_2O_3 layer into the film as it has been shown to have a flat band shift between +300 to +800 mV.[18] However, the relatively lower κ value of Al_2O_3 would need to be considered.

The interface state density (D_{it}) is evaluated by the density of the charge states located at the mid-gap of the forbidden energy band. The trapped charges would affect not only the C-V characteristics, but also the device as well. By trapping electron and holes, the surface states is able to reduce the drive current in MOSFETs in which, the trapped electrons and holes located at the interface will act as charge scattering centers that would lower the mobility of the mobile carriers traveling in the surface channel. In addition, interface states can behave like localized generation-recombination centers that may give rise to generation-recombination leakage currents and affect the gate dielectric reliability. The D_{it} near the mid-gap energy can be determined by taking into account the conductance-voltage characteristics of the MIS capacitor. The interface trap density can then be evaluated using the equation as proposed by Hill and Coleman.[107]

$$D_{it} = \frac{\left(\frac{2}{qA}\right)\left(\frac{G_m}{\omega}\right)}{\left[\left(\frac{G_m}{\omega C_{max}}\right)^2 + \left(1 - \frac{C_m}{C_{max}}\right)^2\right]}$$

Equation 4-7

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Where q correspond to electronic charge, A refers to the area of the capacitor, G_m is the maximum conductance, C_m refers to the corresponding capacitance at the maximum conductance C_{max} is the maximum capacitance at the accumulation region and ω is the angular frequency.

Therefore, applying the equation as proposed by Hill and Coleman, a D_{it} of 2.66×10^{13} cm^{-2} eV^{-1} was obtained for the 5 nm Lu_2O_3 on n-type Si (100) after annealing at 900°C in oxygen ambient. The calculated value of the interface trap density is about an order of magnitude higher than reported value for Lu_2O_3 deposited by atomic layer deposition (ALD), which typically has a D_{it} value of $0.9 - 1.0 \times 10^{12}$ cm^{-2} eV^{-1}. Comparing to other deposition methods, a thermally evaporated Al_2O_3 was reported to produce a D_{it} of > 10^{11} eV^{-1} cm^{-2}.[38] Y_2O_3/Gd_2O_3 film deposited using molecular beam epitaxy (MBE) produces a $D_{it} < 10^{12}$ eV^{-1} cm^{-2} while a sputtered Zr-Al-Si film produced a D_{it} in the range of $1 - 5 \times 10^{11}$ eV^{-1} cm^{-2}.[78,108] The higher D_{it} value reported in this work was probably due to the inherent lower quality of the film deposited by the laser pulsed deposition as compared to the ALD for example, in which layer by layer atomic deposition could be controlled precisely thereby eliminating or significantly reducing possible defects and/or vacancy at the interface that could result in the interface trap contribution. Comparatively, in this work, the calculated D_{it} for the 600°C and laser annealed samples (as will be discussed in chapter 5, section 5.4) are also in the range of 10^{13} cm^{-2} eV^{-1}.

In the selection of a suitable high-κ material for the gate dielectric application, one has to consider the charge-trapping issue. This was expected because in a gate-stack, we are expecting different material interfaces, which have been known as charge trapping

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sites.[94] Moreover, unlike SiO_2 gate dielectric that is typically thermally grown, high-κ films are deposited on the substrate and therefore have a higher tendency for trapping sites, even more so if crystallization occurs as well. Therefore, in addition to the κ value calculation, the hysteresis of Lu_2O_3 was also investigated. One of the simplest way to indicate charge trapping in a MOS capacitor structure is the hysteresis measurement from the C-V curve by using trace-retrace voltage sweep during the measurement.[94] In the Lu_2O_3 hysteresis measurement in this work, the measurement was made starting with negative voltage on the gate (inversion mode) sweeping to positive voltage (accumulation mode) while recording the forward C-V trace and proceed by sweeping the trace in the opposite direction to record the backward trace. The hysteresis C-V sweep of Lu_2O_3 thin film sample annealed at 900°C in oxygen ambient is shown in Figure 4-9.

Based on the hysteresis measurement, a fairly small hysteresis of 48 mV was obtained for the 900°C-annealed sample in the oxygen ambient. It is observed that the backward sweep is more negative as compared to the forward sweep. This indicates a counterclockwise hysteresis, in which it is associated with the trapping of positive charge in the area near the high-κ oxide and silicon interface. The observed hysteresis behavior in this work is smaller than that reported by other research groups.[34]

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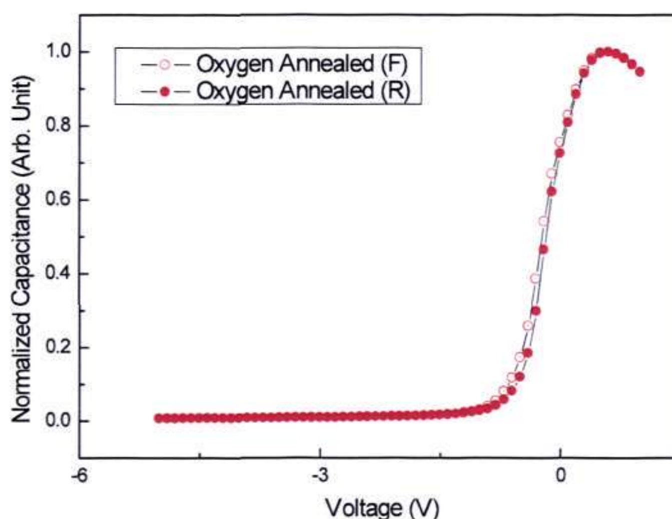

Figure 4-9 Normalized C-V curves for Lu_2O_3 samples annealed at 900°C in oxygen ambient. (F) denotes forward voltage sweep while (R) denotes reverse voltage sweep.

In order to further understand the electrical characteristic of the Lu_2O_3 film, C-V characteristics of the Lu_2O_3 MOS capacitor was acquired at different frequencies ranging from 300 kHz up to 1 MHz. The general observation is that the curves were well shaped with slight dispersion for the sample annealed at 900°C in oxygen ambient. The set of C-V curves obtained at various frequencies is shown in Figure 4-10.

The dependence of C-V curves to frequency is attributed to the effect of series resistance of the substrate and the gate in series with the measured capacitance in the work of M. Houssa *et al.*[109] On the other hand, S. Ohmi *et al* attributed the frequency dependency of the thin film C-V characteristics to the film quality that was obtained during processing.[70] In this work, it was observed that there was a slight dispersion of the C-V curves with varying frequency. As with the observation on the interface trap density,

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it is likely that the quality of the Lu_2O_3 film deposited using the PLD was not high enough for ensuring frequency-independent characteristics.

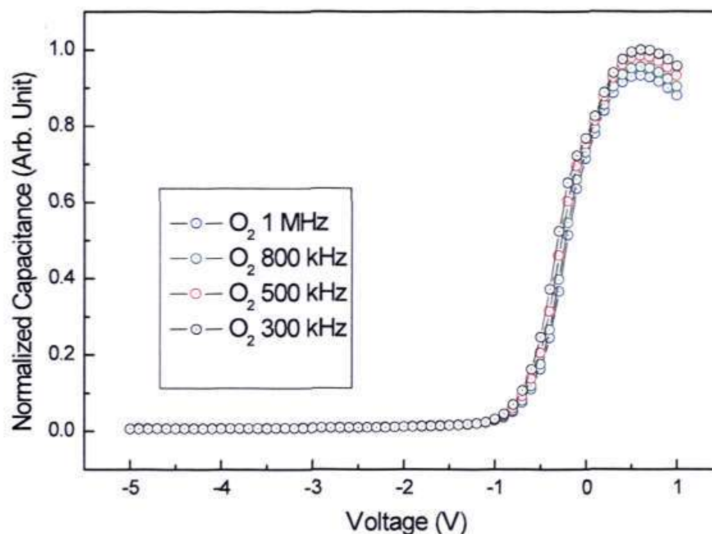

Figure 4-10 Normalized C-V curves for samples annealed at 900oC in oxygen ambient

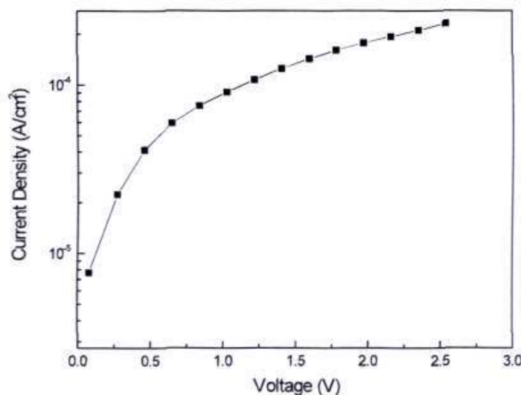

Figure 4-11 J-V characteristics of ~ 5nm thick Lu_2O_3 film subjected to rapid thermal annealing at 900°C in oxygen ambient.

Another important parameter to consider is the leakage current density value obtained from the Lu_2O_3 MOS capacitor stack. The leakage current density-voltage plot of the Lu_2O_3film (~ 5 nm thick) is shown in Figure 4-11. The leakage current density at

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the off state of n-type Si substrate at +1 V bias was found to be 1.0×10^{-4} A/cm^2. This is lower than the reported value by other research group with similar Lu_2O_3 thickness.[28] The lower leakage current density reported in this work is attributed to the better defect alleviation and film densification process resulting from the rapid thermal anneal along with an overall smoother surface thereby reducing the leakage current paths from both metal/high-κ dielectric interface as well as high-κ/Si interface. In addition, as the sample was annealed in oxygen ambient, the processed Lu_2O_3 film is likely to have a much reduced oxygen vacancy thus contributing to the lower leakage current density. Furthermore, as mentioned in previous section, in the presence of O_2, there is a high chance of the formation of silicate layer. This silicate layer would have contributed to the reduction in the leakage current density as it acts as a barrier layer. Note that the leakage current density reported in this work is several orders of magnitude lower as compared to thermally grown SiO_2 with similar EOT, which is highly desirable for high-κ gate dielectric application. With reference to the ITRS 2008 roadmap for low standby power devices, the leakage current density reported in this work has met the requirement for sub 38 nm technology nodes.

4.4 Leakage current conduction mechanism in Lu_2O_3 high-κ gate dielectric film

The determination of the D-C conduction mechanisms in Lu_2O_3 is very important in order to evaluate the device reliability. Therefore, in order to investigate the leakage current conduction mechanism two samples were prepared with thicknesses of 2 and 4.5

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nm. After deposition, these Lu_2O_3 films were subjected to post deposition annealing at 600°C for 60 seconds in either nitrogen or oxygen ambient. These samples are labeled A, B, C and D and this information is presented in Table 4-2 for easy reference.

Table 4-2 Samples prepared with different thickness and annealing conditions.

	A	B	C	D
Annealing ambient	N_2	N_2	O_2	O_2
Thickness (nm)	2.0	4.5	2.0	4.5

MOS capacitors were fabricated in order to characterize these samples electrically. DC magnetron sputtering was used to form the circular gold electrodes using physical shadow mask of approximately 0.3 mm in diameter. HRTEM micrograph was used to examine the film thickness and interfacial quality.

Figure 4-12 shows a cross-sectional HRTEM micrograph of he Lu_2O_3 thin film on n-type Si (100) substrate deposited at high vacuum condition and subjected to subsequent post deposition anneal at 600°C in oxygen ambient (sample C and D). It can be observed from the HRTEM micrographs that the Lu_2O_3 thin film remained amorphous as expected, even after annealing at 600°C in oxygen ambient. In addition, the interface between the high-κ film and the substrate seems abrupt, with no observable interfacial layer formation. However, we need to bear in mind that this does not mean that there is no silicate layer formation.

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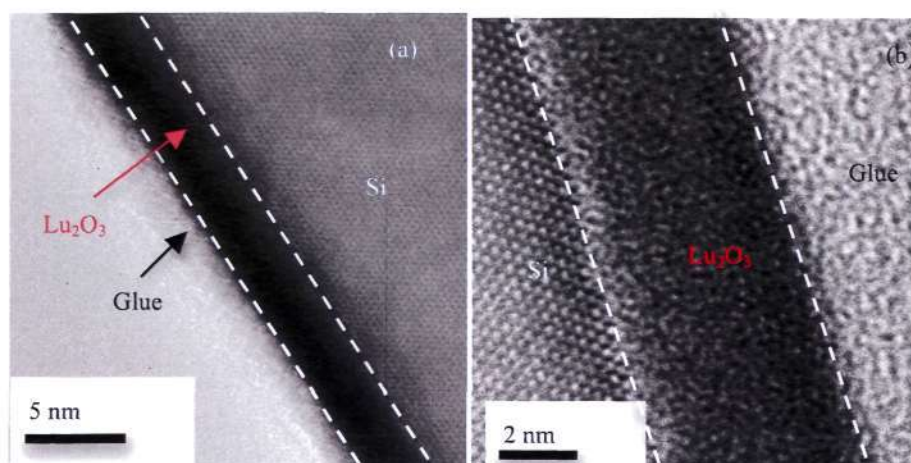

Figure 4-12 Cross-sectional TEM micrographs of Lu_2O_3 films on Si substrate: (a) ~ 2 nm thick sample annealed in oxygen (sample B) and (b) ~ 4.5 nm thick sample annealed in oxygen (sample D).

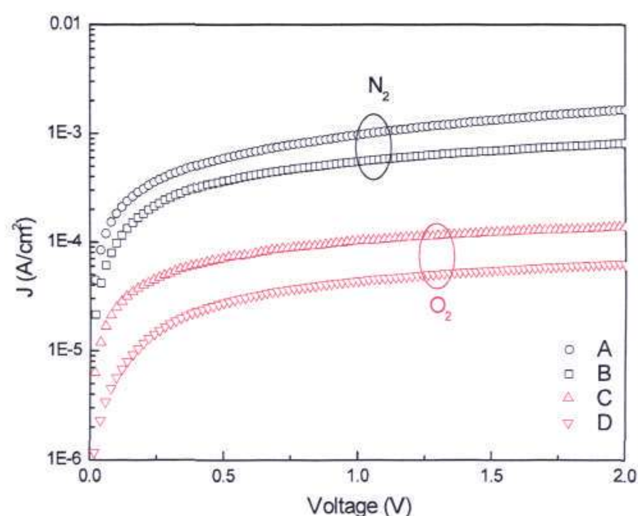

Figure 4-13 The current density versus gate voltage characteristics of MOS capacitor devices measured at room temperature for samples A, B, C and D.

The current density versus gate voltage characteristics of the MOS capacitor devices measured at room temperature is shown in Figure 4-13. The current density of the 4.5 nm thick Lu_2O_3 MOS capacitor annealed in oxygen ambient (sample D) was measured to be less than 4.5×10^{-5} A/cm^2, which is several orders lower than SiO_2 based gate dielectric

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devices with similar EOT. On the other hand, the leakage current density for the MOS capacitor device annealed in nitrogen ambient (sample B) was measured to be approximately 5 × 10^{-4} A/cm^2. It can be also observed in Figure 4-13 that the leakage current densities for the thicker samples are lower than their thinner counterparts. This is expected since it is harder for the defects in the thicker film to form leakage conduction path as opposed to a thinner film. That being said, the leakage current densities obtained in this work have met the requirement of sub 38 nm technology node for low standby power devices according to ITRS 2008.

Based on the observation of the J-V curves shown in Figure 4-13, a significant reduction in the leakage current density was found in the Lu_2O_3 MOS capacitor devices subjected to post-annealing process in oxygen ambient. Annealing in oxygen ambient is expected to reduce the leakage current density, as it is able to minimize the concentration of the ionized oxygen vacancies. In addition, at higher voltage region, the application of increased voltage did not result in any significant leakage current density in the Lu_2O_3 MOS capacitor devices thus indicating that the shallow trapped charges are fully excited by the high electric field and therefore it lead to saturation of the leakage current density.

In order to ascertain the conduction mechanism in the Lu_2O_3 MOS capacitor devices, further J-V measurements at different measurement temperatures are required. A set of J-V curves is obtained for each sample (A, B, C and D) at various measurement temperatures ranging from 25°C up to 150°C. For each of these measurements, the heating chuck was allowed to stabilize before the measurement is started. The J-V characteristic curves for the Lu_2O_3 MOS capacitors measured at various temperatures are shown in Figure 4-14. It can be observed from these curves that the leakage current

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density increases with increasing measurement temperature. This is expected because at higher temperatures, the charges are more energetic and thus have a much higher chance to overcome the energy barrier.

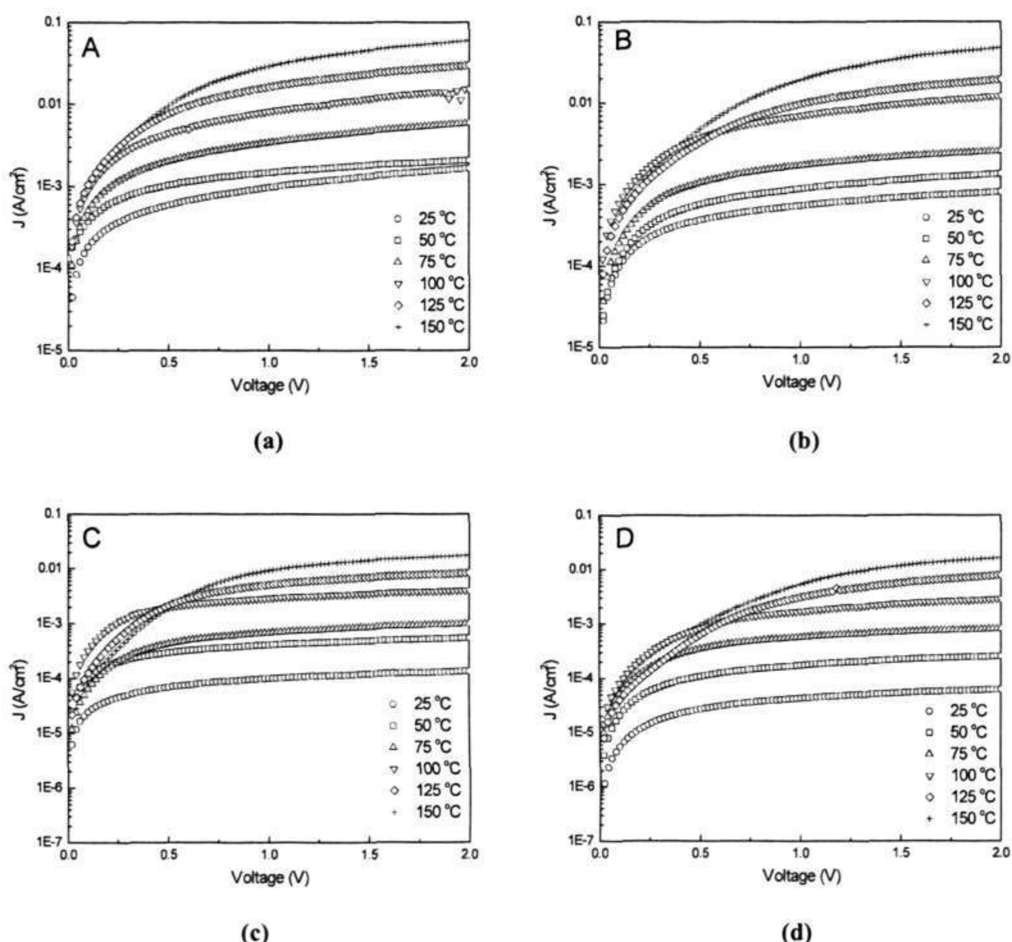

Figure 4-14 The J-V characteristics of the MOS capacitor devices measured at different temperatures for (a) sample A, (b) sample B, (c) sample C, and (d) sample D.

The leakage current density mechanism in the Au/Lu_2O_3/Si MOS capacitor devices was investigated by fitting the J-V curves to a conduction mechanism model, which in this case is the Poole-Frenkel emission mechanism. The Poole-Frenkel mechanism is one of the most commonly found leakage current conduction mechanism for high-κ dielectric

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stacks.[94] The Poole-Frenkel emission mechanism is due to the field-enhanced thermal excitation of trapped electrons into the dielectric conduction band.[87] The current density modeled by Poole-Frenkel mechanism can be expressed as shown.

$$J = BV\exp\left[-\frac{q\phi_{pf} - \gamma E^{1/2}}{kT}\right], \gamma = \left[\frac{q^3}{\pi\varepsilon_o\varepsilon_r}\right]$$

Equation 4-8

The expression can also be expressed as:

$$\ln(J/V) = \ln B + \frac{\gamma\sqrt{E} - q\phi_{pf}}{kT}$$

Equation 4-9

Where B represent constants, $q\phi_{pf}$ is the trap energy level, E is the applied electric field, q is the electronic charge, k in this expression is the Boltzman constant, ε_r represent the relative permittivity of the high-κ dielectric layer and lastly ε_o represent the permittivity of free space. From the expression given in **Equation 4-8**, it is clear to see that if the leakage current conduction mechanism at high electrical field is governed by the Poole-Frenkel emission, then the plot of Ln*(J/V)* versus $E^{1/2}$ should be a straight line.

It was described in chapter 2 that both Poole Frenkel and Schottky conduction mechanism are very similar and would exhibit a straight line in the Ln *(J/V)* versus $E^{1/2}$ and Ln J/T^2 versus $E^{1/2}$ plot respectively. Therefore, it is important to test the validity when citing either Poole Frenkel or Schottky emission by determining the temperature dependence of the conduction and the changes in the slope on the Ln *(J/V)* versus $E^{1/2}$ and Ln J/T^2 versus $E^{1/2}$ plot respectively. The temperature dependency is important to

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differentiate this effect from tunneling phenomena. As it can be seen from the equation below that both Schottky and Poole-Frenkel emission has similar expression:

Schottky:

$$J \sim A \times T^2 \exp\left[\frac{-q(\phi_b - \sqrt{qE/4\pi\varepsilon_o\varepsilon_r}}{kT}\right]$$ **Equation 4-10**

Poole-Frenkel:

$$J \sim E \exp\left[\frac{-q(\phi_b - \sqrt{qE/4\pi\varepsilon_o\varepsilon_r}}{kT}\right]$$ **Equation 4-11**

Therefore, both Schottky and Poole-Frenkel are related through the coefficient known as the field lowering coefficient β as shown below:[110]

$$2\beta_{pf} = \beta_{sc} = \sqrt{\frac{q}{4\pi\varepsilon_o\varepsilon_r}}$$ **Equation 4-12**

From the J-V curves, the data is fitted to the Poole-Frenkel conduction current mechanism and is shown to fit very linearly in the accumulation region. The field dependence of the Poole-Frenkel conduction behavior at high voltage bias (> 1 V) at different temperatures is shown in Figure 4-15. In addition, the temperature dependence of the Poole-Frenkel conduction behavior at high bias voltage (1 V) is shown in the inset. From these fitting, the field lowering coefficient need to be compared with the experimental data before we can confirm that the leakage conduction mechanism of Lu_2O_3 is indeed Poole-Frenkel. This method was suggested by D. Natarajet *et al.*[110]

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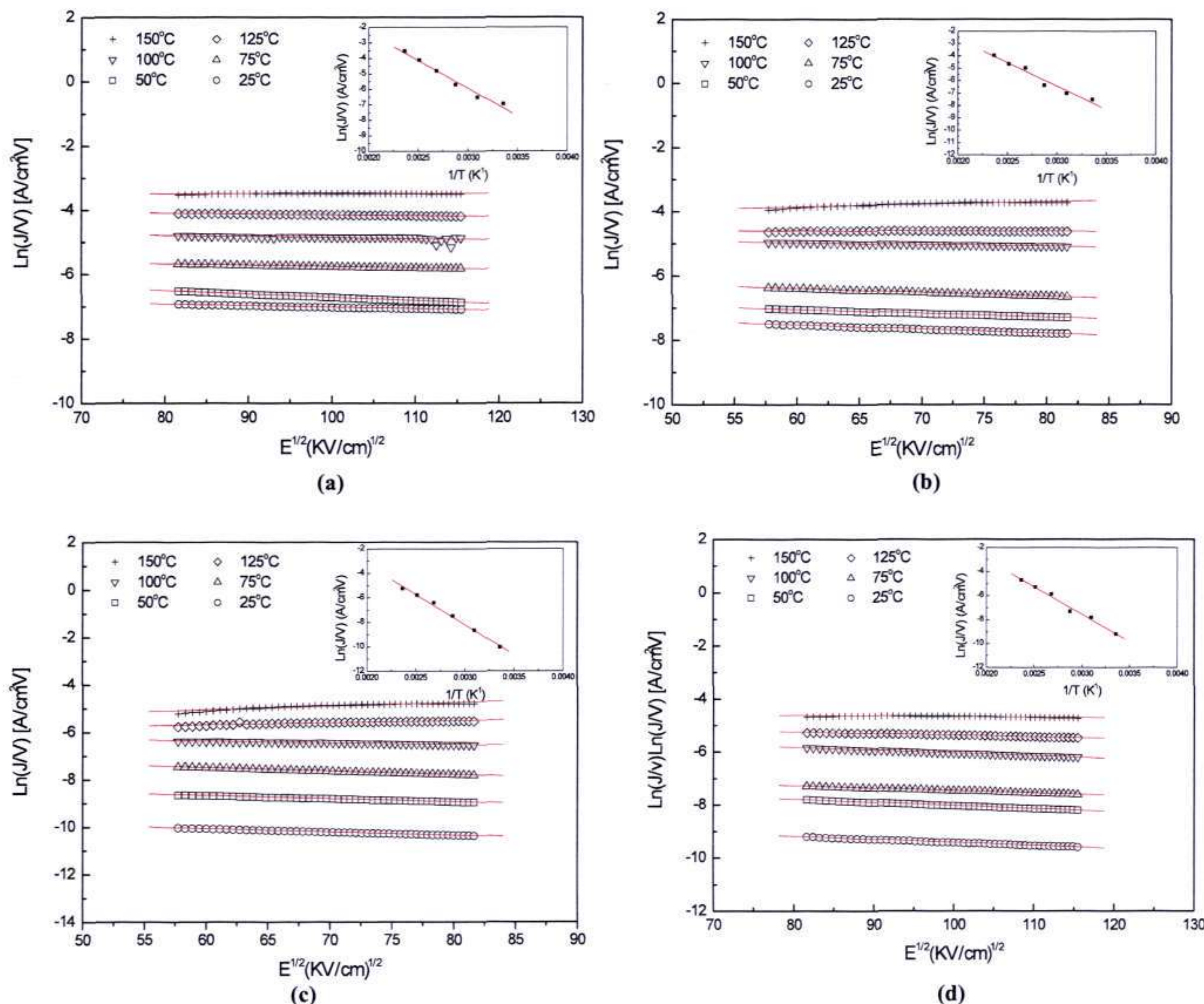

Figure 4-15The field dependence of the P-F conduction behavior at five temperatures for (a) sample A, (b) sample B, (c) sample (C) and (d) sample D. The inset shows the temperature dependence of the P-F conduction behavior at 1 V accumulation bias.

Therefore, based on equation 4-12, and taking the κ value of Lu_2O_3 to be 11.59, we could obtain a value of 8.79×10^{-4} and 4.40×10^{-4} eV $V^{-1/2}$ $m^{1/2}$ for β_{sc} and β_{pf} respectively. While the β experimental value obtained for sample D, obtained from the slope of the plots in Figure 4-15 (d) against e/kT was found to be 4.21×10^{-4}eV $V^{-1/2}$ $m^{1/2}$.

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As the experimental value is closest to the calculated β_{pf}, we can be sure that the dominant leakage current conduction mechanism in this case is Poole-Frenkel.

The trap energy levels $q\phi_{pf}$ is derived from the fitted data of the various J-V curves obtained at different temperatures. The results of the energy trap level are summarized in Table 4-3.

Table 4-3 Trap energy level calculated from the fitted data of J-V curves obtained at various temperatures.

	A	B	C	D
Annealing ambient	N_2	N_2	O_2	O_2
Trap energy level ($q\phi_{PF}$) (eV)	0.3	0.32	0.37	0.41

It is interesting to note that the trap energy level of the Poole-Frenkel conduction mechanism in Lu_2O_3 film MOS capacitor annealed in nitrogen ambient is lower as compared to Lu_2O_3 film MOS capacitor annealed in oxygen ambient. The observed result is coherent with the fact that the former has a higher leakage current density than that of the latter in the accumulation bias region. The result indicates that it is easier for the trap charge responsible for the high leakage current to be excited into the conduction band of the Lu_2O_3 thin films when annealed in nitrogen ambient.

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4.5 Trap controlled behavior in Lu_2O_3 high-κ gate dielectric film

More often than not, the gate dielectric examined appeared to have a substantial amount of fixed charge, which could present significant issues for CMOS device applications. The fixed charge is created in the dielectric through defect formation. When the charge was removed from the dielectric either through the substrate or the gate and it cannot be placed back into the defect through the application of voltage, a fixed charge is created. When this happen, a fixed dipole moment and a built-in voltage is created.[111] Therefore, as the magnitude of the built-in voltage is independent of the applied voltage, we would observe a shift in the C-V curve. As mentioned earlier, the build up of such fixed charges is undesirable, as the resulting built-in voltage would affect the electrical performance of the transistor. This is because the magnitude of the created built-in voltage would be comparable to the applied voltage that is used to switch the device ON and OFF.[111] Moreover, the electrical field that was created through randomly distributed charges in the dielectric has a chance to extend itself to the MOSFET channel thereby acting as scattering centers in the channel, reducing mobility, saturation current as well as the working speed of the transistor.[111] As such, the presence of fixed charges in the high-κ film would be highly undesirable. Relevant work on electron and hole traps has been studied previously on MgO, ZrO_2, HfO_2, ferroelectrics and many other materials,[112-116] although research on rare earth materials is still limited.[111] This lead to the motivation to investigate the trap-controlled behavior in the ultrathin Lu_2O_3 high-κ gate dielectrics.

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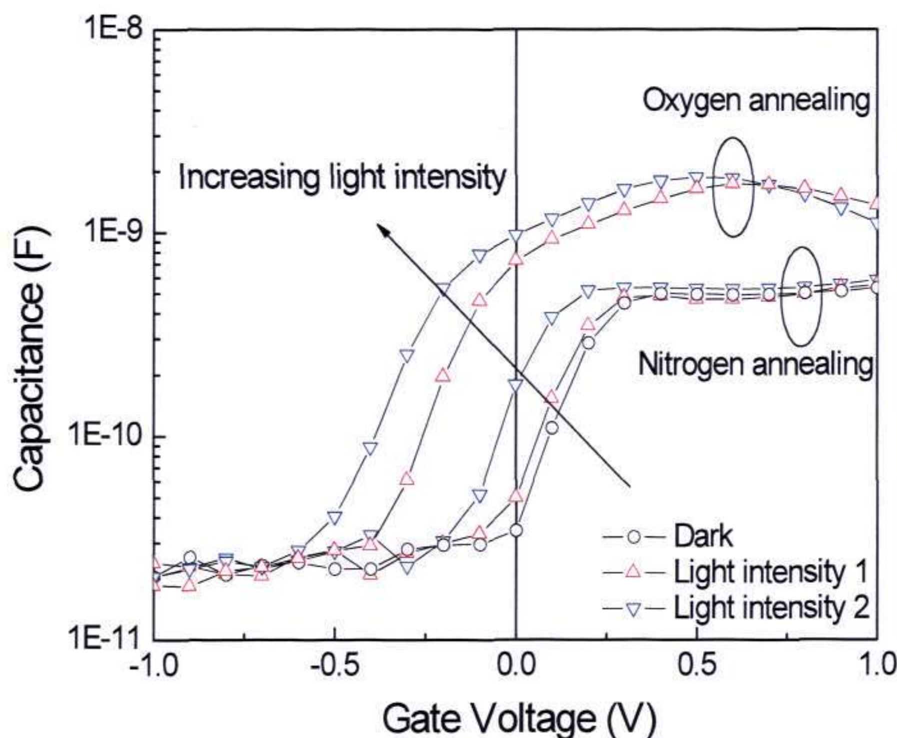

Figure 4-16 C–V characteristics of Lu2O3 thin film post-annealing in nitrogen ambient and oxygen ambient at 600°C with increasing the intensities of the light illumination.

In order to trace the trap generation and charging effect in Lu_2O_3 films, Lu_2O_3 MOS capacitors are fabricated with similar steps as described in previous experiments. The samples are both annealed in nitrogen and oxygen ambient at 600°C. The thickness of the Lu_2O_3 gate dielectric is approximately 4.5 nm thick. V_{fb} shifts observed during relatively high frequency (100 kHz) C-V measurements are then recorded. The experiments are first conducted in a dark box. The measured C-V curves are shown in Figure 4-16.

An EOT of 1.1 nm was obtained for the sample that was post annealed in oxygen ambient. A negative V_{fb} shift was obtained for the sample while a positive V_{fb} shift was observed for the nitrogen-annealed sample. Based on previous discussion, we know that a

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positive V_{fb} shift is related to negative fixed charge present in the film. We believed that this is attributed to the formation of ionized oxygen vacancies as shown below, where two electrons are trapped and considered delocalized into the conduction band.

$$Oo \rightarrow V\ddot{o} + 2e + \frac{1}{2}O_2$$ **Equation 4-13**

Post-annealing in oxygen was observed to decrease the net amount of negative fixed charge, possibly through the compensation of positive fixed charge, until eventually a net positive charge is observed. This reason for the above observation is that post-annealing in oxygen ambient will reduce the ionized oxygen vacancies and at the same time induced interstitial oxygen atoms with the increase in oxygen pressure, as was previously observed in hafnia.[117] In addition, the interstitial oxygen may in principle be ionized to yield electron holes and interstitial oxygen ions with negative effective charge as expressed in Equation 4-15 below:

$$\frac{1}{2}O_2(g) = O_i^{||} + 2h^{\bullet}$$ **Equation 4-14**

Based on the above reasoning, it is proposed that the net fixed charge density in the Lu_2O_3 film could be altered significantly, depending on post-annealing conditions.[118]

Another interesting aspect is the charge trapping and de-trapping property as a function of the intensity of light illumination. This study is done through the observation of the V_{fb} shift on the C-V curves, as shown in Figure 4-16. It was observed that when the MOS capacitor device was illuminated under a microscope white light, a negative flat band shift was observed. The higher the light intensity shone on the device, the larger is

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the V_{fb} shift observed on the C-V curve. The significant flat band shift has possibly resulted from a photodetrapping effect, in which electrons captured on shallow traps are excited back into the conduction band through photoexcitation effect.[119]

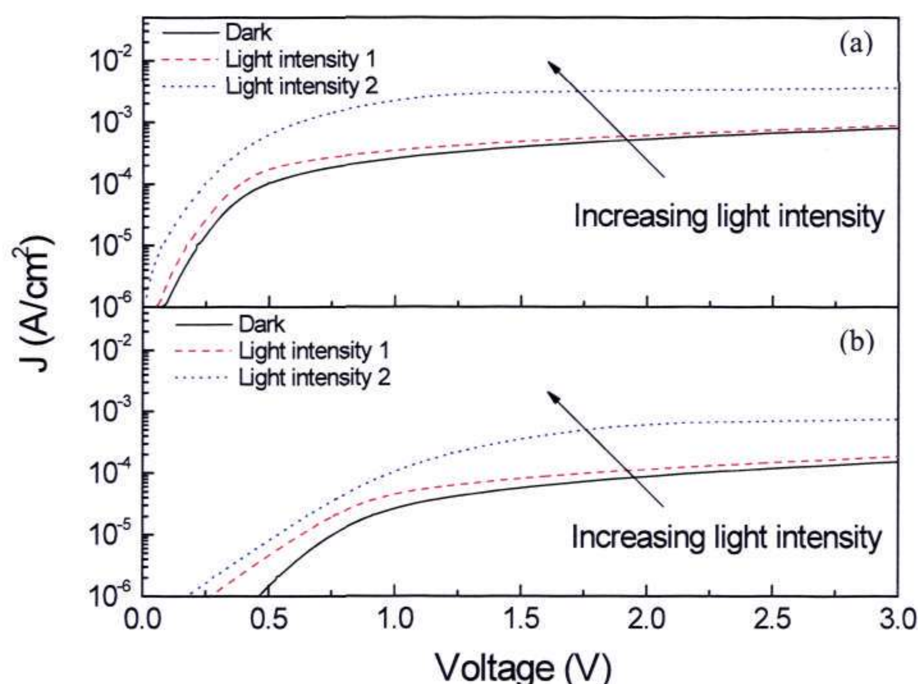

Figure 4-17 The current-voltage characteristics (*J-V*) of Lu_2O_3 MOS capacitor annealed at 600°C in (a) nitrogen and (b) oxygen ambient when illuminated with light. Light intensity 2 is higher than light intensity 1.

In addition to the C-V behavior, the J-V behavior of the device when illuminated with light is also investigated. The obtained J-V curve is shown in Figure 4-17. Based on the J-V curve observation, it was found that the leakage current density of Lu_2O_3 MOS-capacitor sample annealed in oxygen ambient is significantly lower than that annealed in nitrogen ambient. This behavior can be related to the result from the previous section in which we have obtained a higher trap energy level for the oxygen-annealed sample as compared to nitrogen-annealed sample. It was also observed in Figure 4-17 that with

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increasing intensity of light illumination, the leakage current density becomes higher as well. The excess current as a result of higher intensity of photodetrapping under stronger light illumination may have resulted in the photoexcitation of electrons captured in shallow traps back into the conduction band. It is likely that the capability of traps to trap and release charges is responsible for the observed leakage current density behavior.

4.6 Summary

In summary, Lu_2O_3 has been shown to have a relatively good thermal stability. The film was able to remain in amorphous state with little observable interfacial layer after a high temperature annealing process at 900°C, which is close to the annealing step used in CMOS fabrication. As with other rare-earth oxide, it appears that Lu_2O_3 would probably react with Si or formed SiO_x layer to form Lu-based silicate layer as has been shown through the XRR analysis. In addition, the electrical characteristics of Lu_2O_3 based on the C-V and J-V curve measurements have been investigated. From the C-V measurement, a relatively high κ value of 11.59 was obtained. Although the calculated D_{it} was on the high side, all other characteristics such as hysteresis and frequency dispersion behavior along with its leakage current density seem to indicate the potential of Lu_2O_3 to be used as a suitable gate dielectric material. Further investigation on the electrical behavior of Lu_2O_3 film revealed that the dominant leakage current conduction mechanism is Poole-Frenkel. Finally, the effect of light illumination was investigated. It was proposed that the net fixed charge density as well as its leakage current density could be modified significantly

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depending on the post-annealing condition, as well as the capability of traps present in the film to trap and de-trap charges.

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Chapter 5 INVESTIGATION ON THE EFFECT OF VARIOUS POST DEPOSITION TREATMENTS ON LU_2O_3 HIGH-κ DIELECTRIC FILM

5.1 Background

In the previous chapter, we have discussed in detail the behavior of Lu_2O_3 dielectric on Si. The thermal stability of Lu_2O_3 annealed at high temperature (900°C) was discussed, along with the electrical properties of Lu_2O_3 MOS-capacitor annealed at 600°C in oxygen ambient. In addition, the leakage current conduction mechanism dominant in Lu_2O_3 MOS-capacitor is the Poole-Frenkel mechanism. In this chapter, we are going to discuss further on the changes in the film properties and its behavior after subjected to the various post deposition treatments such as rapid thermal anneal at various temperatures at different gas ambient. In addition, novel way of treating high-κ gate dielectric film by incorporating laser anneal will be introduced and discussed.

5.2 Study on the effect of annealing on Lu_2O_3 thin film on Si using high resolution Rutherford backscattering spectroscopy (HRBS)

In order to advance our understanding of Lu_2O_3 high-κ dielectric film, a study of the effect of the various temperature anneal on Lu_2O_3 film, using HRBS was conducted. The motivation for this study is to investigate the compositional changes to the Lu_2O_3 film

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when post-annealed. Secondly, the study on the strain exerted on Si is of particular interest. This is because any strain exerted on the Si itself would have an effect on the mobility of the device. HRBS has been known to analyze sub-nanometer depth resolution, provided glancing scattering geometry is used. Therefore, in this section, the interfacial depth profiling as well as strain measurements conducted on the Lu_2O_3/Si interface stack will be discussed.

In this work, the Lu_2O_3 were first deposited on p-type Si (100) substrate directly using the PLD at a base pressure of 4.5×10^{-7} Torr. The Si substrate was cleaned using SC1 and SC2 as well as HF (1:100) solution prior deposition. Subsequently, the samples were annealed using RTA at temperatures ranging from 400 to 800°C for 1 minute in oxygen ambient. The samples were analyzed with HRBS using 500 keV He^+ beam, which was collimated into 2 mm × 2 mm size with a divergence angle of less than 1 mrad. The sample was mounted on a high-precision 5-axis goniometer in an ultrahigh vacuum scattering chamber, in which the beam was set to be incident on the sample. The backscattered ions (at 65° angle) were then collected by a focal plane detector and analyzed by a 90° sector magnet. The detector itself consisted of a 100 nm micro-channel plate stacked on a 1-D position detector placed at the focal plane of the spectrometer. In addition, random HRBS spectra of the samples were measured at angle tilt of 40°. SIMNRA software is then used to simulate and fit the obtained spectra in order to ascertain the elemental depth profiles. Furthermore, in order to measure the Si-interface lattice strain, angular scans across the [111] channeling direction along the (110) plane was also conducted.

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The measured and simulated spectra of the as-deposited, 400, 600 and 800°C sample is illustrated in the following Figures:

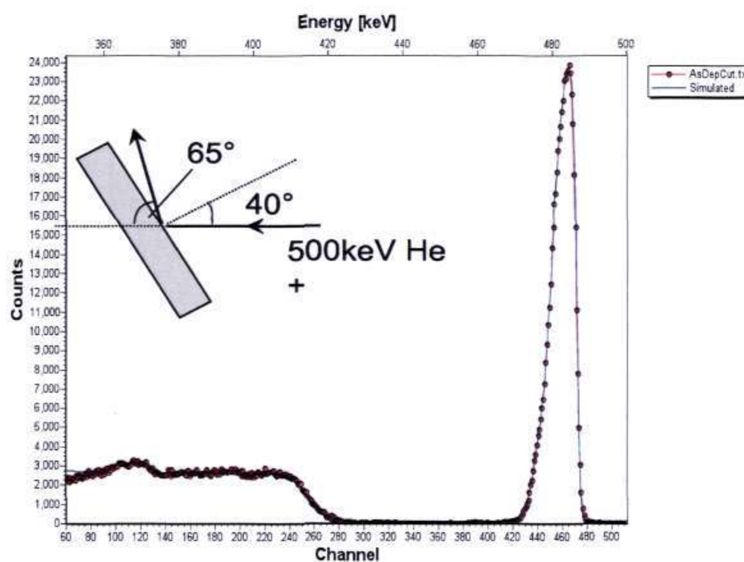

Figure 5-1 Random HRBS spectrum of the as-deposited Lu_2O_3 sample. Experimental data is shown in red, while simulated data is shown as solid blue line.

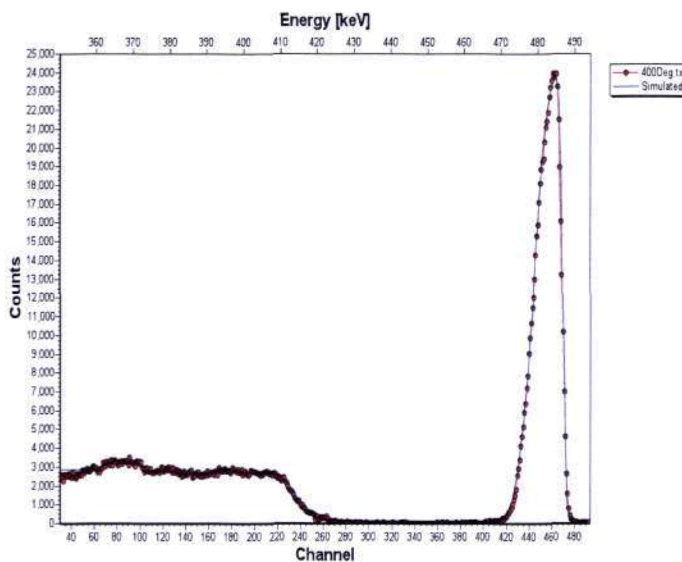

Figure 5-2 Random HRBS spectrum for Lu_2O_3 sample annealed at 400°C in oxygen ambient. Experimental data is shown in red, while simulated data is shown as solid blue line.

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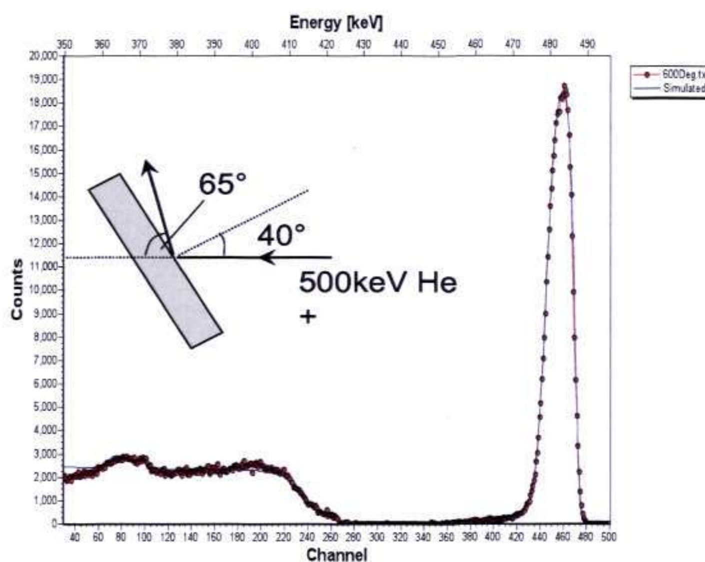

Figure 5-3 Random HRBS spectrum for Lu_2O_3 sample annealed at 600°C in oxygen ambient. Experimental data is shown in red, while simulated data is shown as solid blue line.

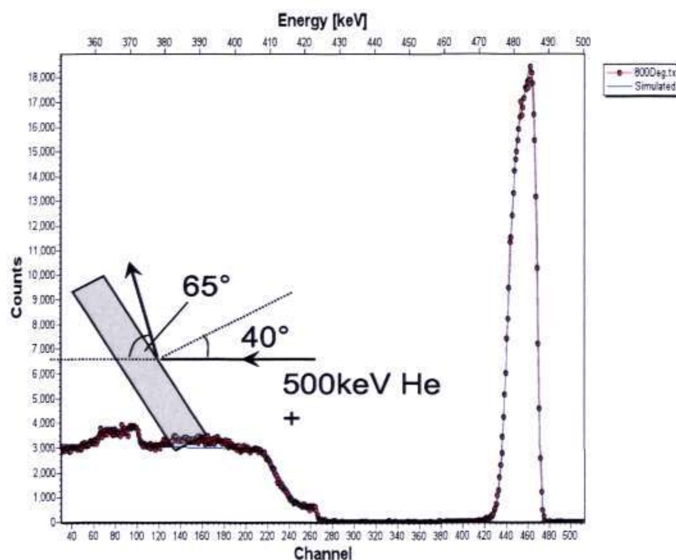

Figure 5-4 Random HRBS spectrum for Lu_2O_3 sample annealed at 800°C in oxygen ambient. Experimental data is shown in red, while simulated data is shown as solid blue line.

The obtained results were first corrected by subtracting a low-level linear background as well as adjusting the non-linear gain variation along the length of the

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MCP. Lu and O have surface energy signals at ~487 and 373 keV respectively. It was observed in the Lu signal's low energy edge and the leading edge of the Si signal that the slope of the signals are getting more gradual as the annealing temperature is increased. This suggests the formation of Lu silicate layer. The shift of the Si signal seems to imply the formation of SiO_x layer. The compositional analysis of the various annealing condition revealed that in the as-deposited sample, a Lu_2O_3 layer was found on the surface. Subsequent annealing appeared to have encouraged the formation of silicate layer as we have observed earlier on in Chapter 4 (section 4.2) where the thermodynamical stability of Lu_2O_3 was discussed. The compositional analysis of these samples also revealed that an interfacial SiO_x film might have been formed at the interface. This is expected for rare earth oxides as it readily dissociate the oxygen found in the annealing ambient into its elemental species and these oxygen may diffuse readily through the film and reacts with the Si substrate to form the SiO_x layer. These SiO_x layer might also react with Lu_2O_3 film to form Lu-based silicate layer. This was confirmed by the HRBS compositional analysis in which Lu-based silicate layer was found throughout the film after annealing was introduced. The film compositional analysis is shown in the following table.

Table 5-1 Compositional analysis of Lu_2O_3 film subjected to various annealing temperatures analyzed by HRBS.

As-deposited	Layers	Thickness (nm)	Lu	O	Si
	1	2.7	0.430	0.570	-
	2	2.1	0.340	0.540	0.120
	3	3.3	0.070	0.470	0.460
400	**Layers**	**Thickness (nm)**	**Lu**	**O**	**Si**
	1	2.1	0.420	0.510	0.070
	2	2.9	0.380	0.490	0.130
	3	3.1	0.080	0.520	0.400
600	**Layers**	**Thickness (nm)**	**Lu**	**O**	**Si**
	1	1.1	0.220	0.600	0.180

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	Layers	Thickness (nm)	Lu	O	Si
	2	2.5	0.390	0.530	0.180
	3	1.7	0.305	0.482	0.213
	4	1.3	0.070	0.550	0.380
	5	2.0	0.025	0.655	0.320
	6	5.0	0.005	-	0.995
800	**Layers**	**Thickness (nm)**	**Lu**	**O**	**Si**
	1	2.7	0.250	0.600	0.150
	2	3.2	0.215	0.580	0.205
	3	1.3	0.060	0.520	0.420
	4	2.7	-	0.330	0.670

Table 5-1 has shown that heat treatment to the samples has promoted the growth of the silicate layer. In the 600°C-annealed sample, it appeared that Lu might have diffused into the Si substrate. This was also indicated in the spectra shown in Figure 5-3 whereby a low energy tail was observed at the low energy region of the Lu signal.

In addition to the compositional analysis, the interfacial strain was also investigated. This study was conducted through angular scans on the as-deposited, 400, 600 and 800°C annealed sample. HRBS has been known as a useful tool in monolayer analysis and the use of HRBS analysis in strain profiling at the interface has been established.[120,121] This was done through the measurements of Si signal in the HRBS spectra at fixed angular position along the (110) plane across the [111] direction, in which it is divided into narrow strips with corresponding linear width of 1.5 nm. A graph is then plotted for the yield of these strips against the incident angle relative to the [111] direction. Strips at various depths from the film-substrate interface were plotted together and fitted with a polynomial function to determine the dip positions. These plots are shown in the following figures:

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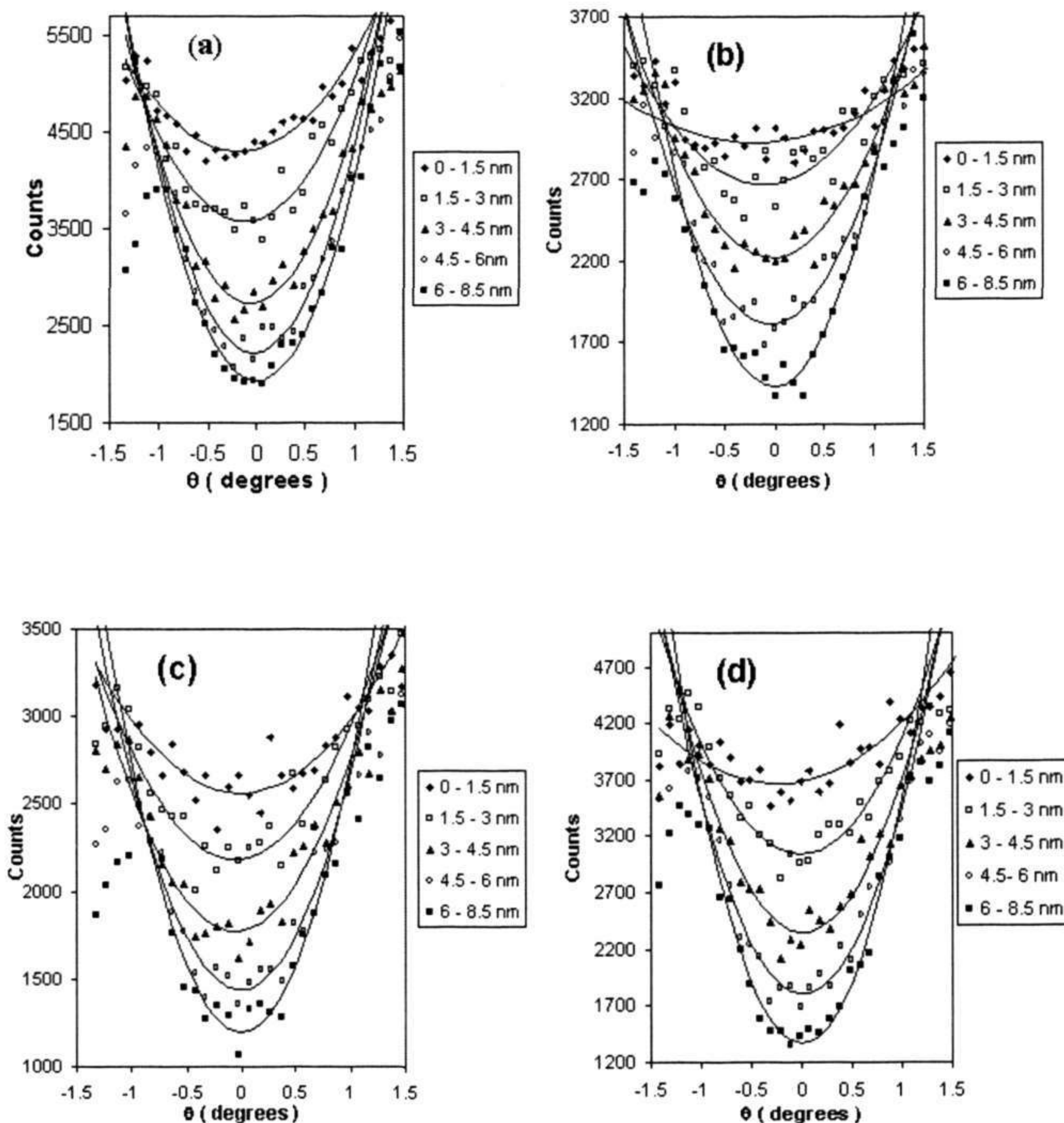

Figure 5-5 A plot of the angular scan conducted on the (a) as-deposited (b) 400°C (c) 600°C and (d) 800°C annealed sample. The plot indicated strain presence in the Si, which decreases with increased annealing.

The plot shown in Figure 5-5 have indicated a shift in the [111] channeling dip position towards a smaller incident angle as it approaches nearer to the interface. This

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shift suggests presence of local tensile stress present in the Si, at least up to a depth of approximately 6 nm below the interface. It was observed from Figure 5-5 that the largest magnitude of the dip shift is found on the as-deposited sample. The strain present in the Si could be correlated to the magnitude of the dip movement through the relation shown below:[122]

$$\varepsilon = 2\Delta\theta_i \operatorname{cosec}(2\theta_i)$$ **Equation 5-1**

where $\Delta\theta_i$ refer to the angular shift of the channeling dip and θ_i represent the angular position of the [111] axis. As such, the strain present in the as deposited sample could be calculated, and a strain value of about 0.7% was obtained. Subsequently, the strain present in the rest of the samples was also calculated and the results is plotted in the graph below:

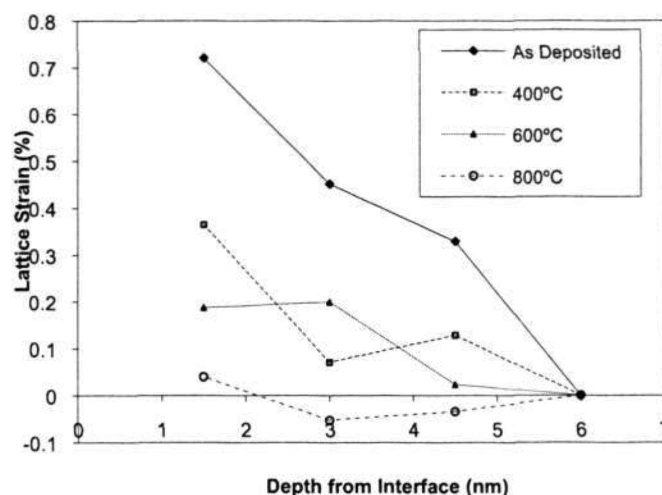

Figure 5-6 A plot of lattice strain approximated from HRBS dip shift analysis against depth from Si interface.

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It is observed from the graph that the strain presence in Si decreases with the introduction of heat treatment to the film. The strain near the interface decreases from ~0.7 % in the as-deposited sample to below the detection limit of 0.1 % when annealed at 800°C. This implies that as heat treatment is introduced in the film, the tensile strain decreases across the film, indicative of relaxation occurring. At 800°C, the data suggest that it was undergoing compression, although this needs to be ascertained further due to the low value. It was also noted from the graph that the effect of the Lu_2O_3 deposition has caused strain on the Si up to a penetration depth of approximately 6 nm. It is believed that the amount of strain present in the Si near the interface (channel region) would have an effect in terms of charge carrier mobility in the inversion layer of MOSFETs. It has been known that strain in the substrate near the channel region would enhance the drive current through the fundamental modification of the band structure of the channel thereby improving the performance of MOSFET devices.[123] The enhancement of mobility resulting from strain-induced modification has been widely reported.[124-129] It was reported in the work of Thompson et al that only 0.2% of uniaxial lattice displacement is needed for a 30% improvement in the mobility.[129]

5.3 Effect of annealing on band alignment of Lu_2O_3 high-κ gate dielectric by X-ray photoelectron spectroscopy

In MOSFET devices, the application of metal gate material and high-κ dielectric film would demand the understanding and control of the interface between the metal gate and the high-κ dielectric film, as well as the interface between the high-κ dielectric and

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its substrate. Therefore, in this case, the study of band alignments at the interfaces would form an important parameter for consideration. It has been known that in heterojunction devices, the transport behavior is governed by the electronic band profiles at the interfaces: the valance and conduction band offsets (VBO and CBO respectively) in the case of dielectric/semiconductor interface and Schottky barrier heights (SBH) in the case of metal/semiconductor interfaces.[130] In this work, the determination of the VBO and CBO is of particular interest. This is because, the information derived from the CBO of a dielectric/semiconductor system would determine whether the material is a suitable candidate to be used as a gate dielectric. A low CBO (< 1.0) would have a good chance to result in unacceptably high leakage current in the device rendering it unsuitable for most applications. Such study has been conducted for other materials such as Al_2O_3 and Y_2O_3 before. From the work of Robertson *et al*, it was determined that the CBO of Al_2O_3 and Y_2O_3 was 2.3 and 2.8 eV respectively.[131] In this section, a study is conducted on the band alignment of Lu_2O_3 when the samples are subjected to thermal processing at various temperatures by employing X-ray photoelectron spectroscopy (XPS) to provide some insights on the electrical behavior of Lu_2O_3.

In this work, the Lu_2O_3 film was deposited through PLD at a base pressure of 1.0×10^{-7} Torr. The laser used in the PLD is a KrF excimer laser with a wavelength of 248 nm, and laser energy of ~ 1.5 J/cm^2 with the frequency of the laser set at 5 Hz. The Si substrate used is p-type Si (100) which was cleaned prior to deposition by using SC1 and SC2 solutions as well as 1 % HF last solution to remove the native oxide present on the substrate itself. RTA was employed on the samples at 400 and 600°C for 1 minute holding time under nitrogen ambient. The XPS analysis used in this study was performed through the VG-ESCALAB 220i-XL system, which uses a monochromatic Al Kα 1

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source (1486.6 eV). In order to improve on the measurement accuracy, the pass energy of the analyzer was set at 10 eV. Pure gold, silver and copper were used to calibrate the binding energy scale through setting the Au $4f_{7/2}$, Ag $3d_{5/2}$ and Cu $2p_{3/2}$ at binding energy of 3.93, 368.26 and 932.67 eV respectively.

The spectra obtained from the XPS on the Lu_2O_3 film was shown in the following figures. The Lu 4d spectra for the as deposited, 400 and 600°C annealed samples is shown in Figure 5-7. The obtained spectra, was fitted using two peaks consisting of Lu $4d_{3/2}$ and $Lu_{5/2}$ doublet. It was observed from the Lu 4d spectra that there was no observable shift on the binding energy, even after the post deposition heat treatment done on the sample. In addition, the Si 2p spectra as shown in Figure 5-7 have exhibited a prominent Si-Si peak at binding energy position of 99.3 eV in the as-deposited sample. [132] Also, the O 1s peak as illustrated in Figure 5-7 exhibit different binding states of oxygen. As such, based on the analysis of Lu 4d, Si 2p and O1s spectra, we are able to deduce the presence of Lu_2O_3 in the film due to the peaks at Lu $4d_{5/2}$ and O 1s spectra with binding energies of 197.7 and 531.4 eV respectively. Furthermore, comparing between the as-deposited sample and 600°C-annealed sample, it appeared that the Si-Si bond peak showed a significant drop whereas the peak at binding energy of 102.1 eV was showed to be increasing as observed in the Si 2p spectra (Figure 5-7 (b)). The increment of the intensity at binding energy of 102.1 eV was attributed to the formation of SiO_x or silicates in the film.[132] Based on the analysis, it is deduced that heat treatment may have played a role in the formation of SiO_x or Lu-based silicate.

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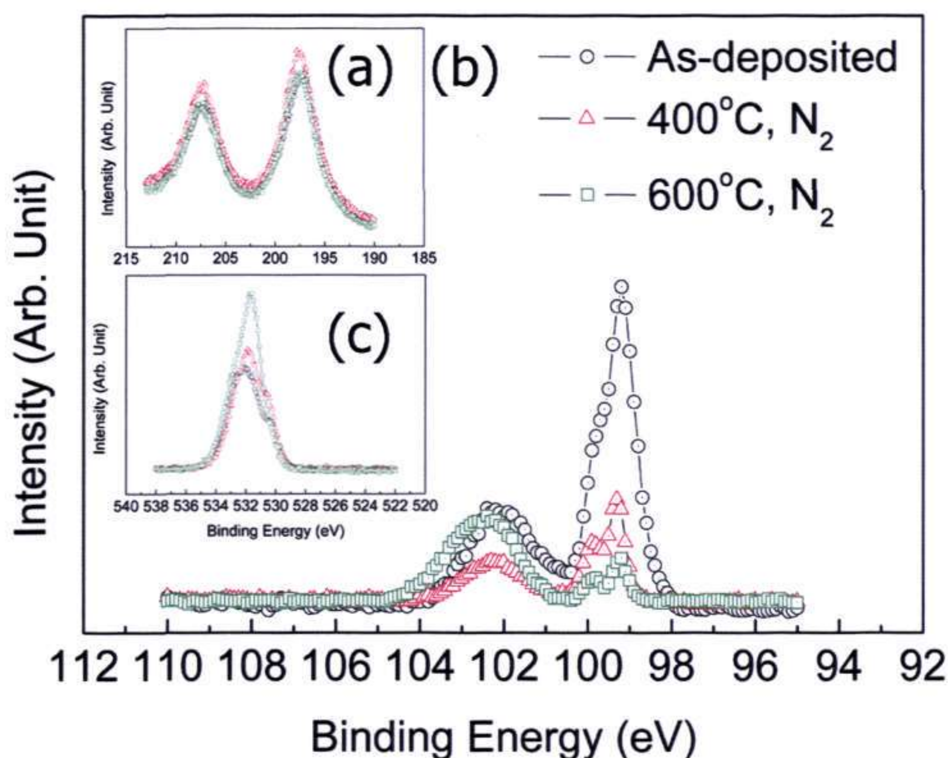

Figure 5-7 XPS spectra for (a) Lu 4d, (b) Si 2p and (c) O 1s for as-deposited, 400 and 600°C annealed samples.

In order to further validate our claim, the peak shift in the O 1s spectra was compared between the as deposited and the annealed samples. Therefore, by making reference to the NIST XPS database, it was found that the binding energies of Lu_2O_3 and SiO_2 peaks would lie in the binding energies of 531.4 and 533 eV respectively and hence any formation of silicate would be indicated by a peak in between of these values in the O 1s spectra. Also noted in our work, the O 1s spectra appeared to be narrowed with strong peaks at 531.4 -532 eV binding energy, which can be attributed to the presence of Lu_2O_3 and the co-existence of SiO_x and/or Lu-based silicate layer. Furthermore, we note that the intensity of the O 1s spectra is increasing with increasing annealing temperature, which supported our argument on silicate formation. This is because SiO_2 has higher oxygen ratio as compared to Lu_2O_3 and therefore any diffusion of the SiO_2 into the Lu_2O_3 layer

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would have increased the O 1s spectra intensity due to the higher oxygen concentration at the surface.

In the determination of band alignment of dielectric/semiconductor heterostructure using x-ray photoemission method, an assumption that the difference in energy between the valance-band edge and the core-level peak for the substrate is constant with/without the deposition overlayer must be made.[133] This method has been previously adopted in the calculation of the band discontinuities at the interfaces of insulator/semiconductor by several groups.[134-136] The method we are adopting developed by Kraut *et al.*,[133,137] described that the valance band offset, VBO (ΔE_v) and the conduction band offset, CBO (ΔE_c) can be determined by using the equations as shown:

$$\Delta E_V = (E_{Lu\ 4d} - E_{Si\ 2p})_{Lu_2O_3/Si} - [(E_{Lu\ 4d} - E_V)_{Lu_2O_3} - (E_{Si\ 2p} - E_V)_{Si}]$$ **Equation 5-2**

and

$$\Delta E_C = (E_g)_{Lu_2O_3} - (E_g)_{Si} - \Delta E_V$$ **Equation 5-3**

where $(E_g)_{Lu_2O_3}$ is the band gap of Lu_2O_3 and $(E_g)_{Si}$ is the band gap of silicon.

The plot of the valance band spectra both for bulk Si and Lu_2O_3/Si stack is shown in Figure 5-8 (a). From the plot shown, it was found that the leading edge of the valance band of the bulk Si was determined to be 0.51 eV. This was determined through the intersection of the regression-determined line segments that defines the edge and the flat energy distribution curve in the energy gap region. Similarly, the Si $2p_{3/2}$ and $2p_{1/2}$ doublet of the bulk Si was found to be 99.94 and 99.33 eV respectively through two-peak fitting.

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Therefore, the energy difference between the valance band edge and Si $2p_{1/2}$ was determined to be 98.82 eV for Si (100) substrate.[134-136] The x-ray photoelectron with energy of 1486.6 eV is able to penetrate up to 10.0 nm deep. As the thickness of the Lu_2O_3 film under study is only approximately 6.0 nm, information from both film and substrate could be extracted from the photoelectron spectra. As for the valance band spectra from the Lu_2O_3/Si stack, the Si 2p peak originated from the substrate itself could be detected. This peak was used to align the corresponding valence band spectrum.

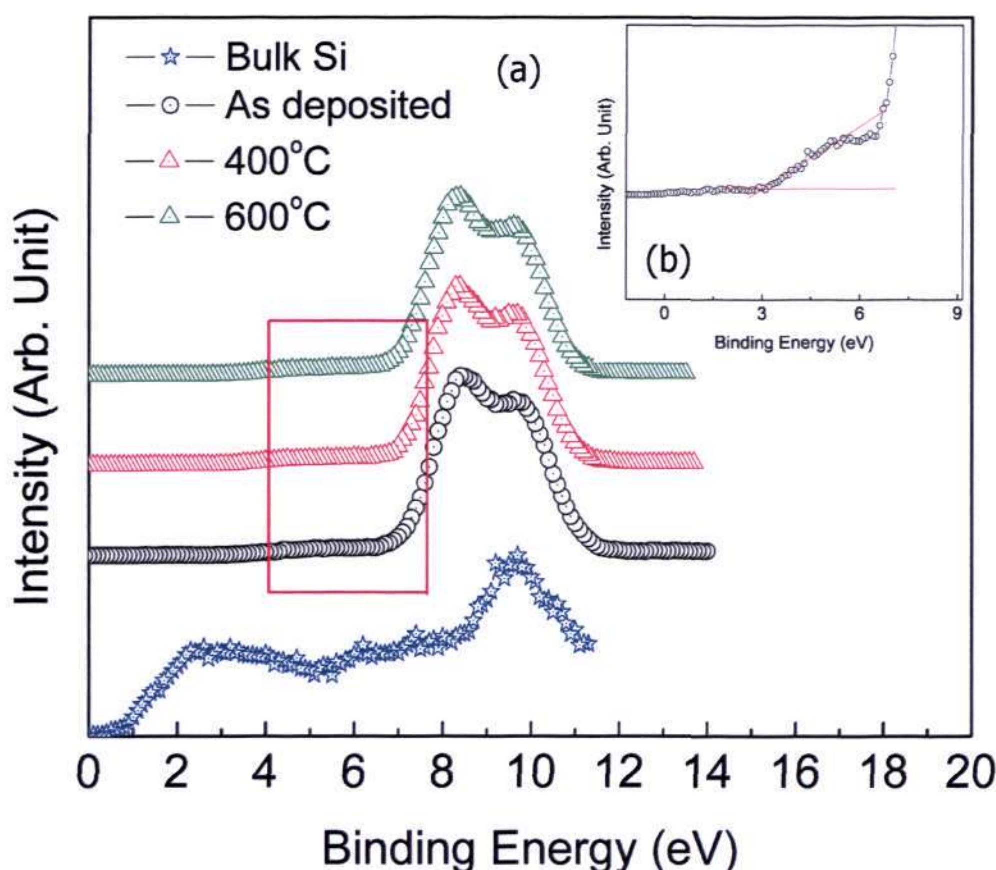

Figure 5-8 (a) A plot of the valance band spectra of bulk Si and Lu_2O_3/Si for the as-deposited, 400 and 600°C. The boxed region in red indicates the region in which the leading edge of the valence band could be found. (b) Showed the zoomed in region of the valence band leading edge for the as-deposited sample.

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Therefore, the valence band edge of the Lu_2O_3/Si for the as-deposited (as shown in Figure 5-8 (b)), 400 and 600°C annealed sample could be extracted from the plot and was found to be 3.04, 2.91 and 2.59 respectively. As such, the valence band offset for the Lu_2O_3/Si interface could be evaluated by applying Equation 5-2 and was calculated to be 2.53, 2.40 and 2.08 eV for the as-deposited, 400°C and 600°C respectively.

With the information obtained on the VBO, the CBO could be determined easily by applying Equation 5-3. One would have to bear in mind however that the accuracy of these value would be affected by the accuracy of the experimental XPS data previously obtained, in which we have determined the ΔE_v value. In addition, we are using the band gap of Lu_2O_3 that was previously obtained through the research work of Seguini *et al*, which was determined to be 5.8 eV.[138] Therefore, the CBO of the Lu_2O_3/Si interface was determined to be 2.15, 2.28 and 2.60 eV for the as-deposited, 400, and 600°C annealed samples respectively. The value obtained in our experiment was close to the reported value reported by G. Seguini's group which was 2.10 eV for the as-deposited sample.[138]

With the information obtained in the experiment, the energy band alignment of the samples at various condition could be plotted. This is shown in Figure 5-9.

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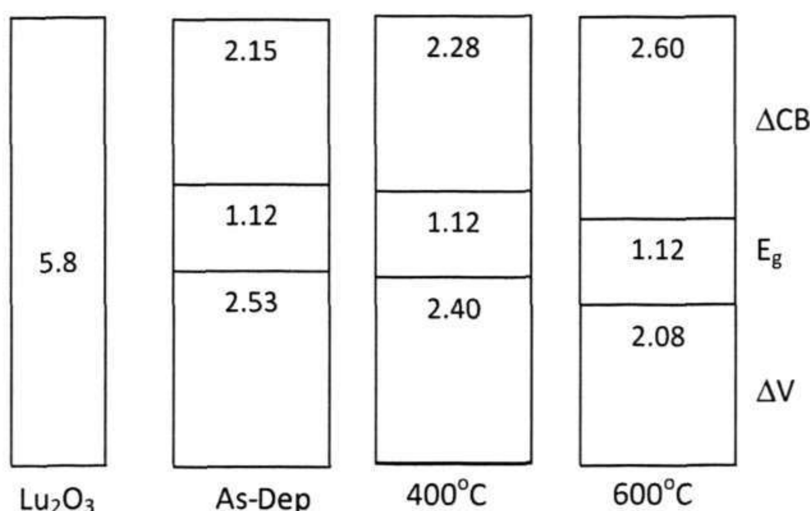

Figure 5-9 The energy band alignment plot for Lu_2O_3/Si interfaces at various annealing conditions.

A quick glance at the plot showed that both conduction and valance band offsets changes with the introduction of heat treatment to the system. The upward and downward shifts of the conduction and the valance band accounts for the difference in the energy band alignment. From Figure 5-9, it was interesting to note that the introduction of heat treatment to the Lu_2O_3 film did bring about changes to the energy band alignment and that the conduction band offset is getting larger with heat treatment while the valence band offset is getting smaller in comparison to the usual cases in oxides where by the CBO is usually smaller than the VBO.

It was postulated that the increase in the conduction band offset itself is related to a favorable band lineup due to a lowering in the charge neutrality level as well as reduction in the charge transfer across the interface.[131] This change was proposed to have resulted from the compositional changes in the Lu_2O_3 film itself. As discussed from the XPS data as well as supporting HRBS data, it was shown that post deposition heat treatment has

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encouraged the formation of SiO_x and Lu-based silicate. Therefore, the assimilation of silicon into the Lu_2O_3 film would have resulted in a suppressed charge transfer across the interface due to a reduction in interfacial dipole intensity associated with the high-κ metal/oxide bond. This would have allowed a larger conduction band offset due to the effect of SiO_x screening limit on the charge transfer phenomenon. This was also similarly observed by Widiez *et al*, in which the energy band alignment of its silicate compound differs from pure HfO_2 resulted from the difference in the dipole intensity.[139] The result that we have obtained on the change in the CBO can be related to the observed reduction in the leakage current density on Lu_2O_3 samples when heat treatment is introduced and further reduction in the leakage current density was obtained when heat treatment at higher temperature was introduced to the sample.[28] The reduction in the leakage current density is probably related to a large electron barrier height due to the reduction in the interfacial dipole that would effectively reduce the electron Schottky emission, which is dominant contribution on the gate leakage current density.

This section has provided an insight on the changes observed in the Lu_2O_3/Si interface energy-band alignment when heat treatment is introduced to the sample. It was suggested that the changes in CBO form one of the contributing factor in the reduction of the lower leakage current density, along with defect alleviation and better densification of the Lu_2O_3 film that is normally resulted from the heat treatment process.

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5.4 Novel high-κ gate dielectric post deposition treatment by using laser annealing

In the work of gate dielectric, RTA is typically the post deposition heat treatment used. RTA has been used to improve further the deposited film properties in order to achieve better electrical characteristics through defect alleviation, film densification among others. In this work, a novel way of post-deposition high-κ film treatment is explored. Since quite sometime ago, laser annealing has been used for ultra shallow junction formation[140] and until recently, it was used in the silicide formation for contact metallization in nanoscale devices.[141,142] However, the effect of laser annealing on high-κ dielectric is still not known. Therefore it forms the motivation to study on the effect of low fluence laser annealed on a high-κ dielectric film deposited by the PLD. In this work, the high-κ dielectric film used is Lu_2O_3. It is through this study that we hope to explore the possibilities of utilizing laser annealing for high-κ dielectric materials.

In this work, the Lu_2O_3 films were deposited on an n-type Si (100) substrate. The base pressure of the PLD used was 4.5×10^{-7} Torr. Prior to film deposition, the substrate was cleaned using standard solutions of SC1 and SC2, followed by HF (1:100) last solution in order to remove the native oxide present. The cleaned substrates were immediately loaded to the deposition chamber so as to prevent the growth of SiO_2 interfacial layer. The laser annealing is done using excimer laser with a wavelength of 248 nm and full width at half maximum of 23 ns. The samples were irradiated using a Lambda Physik laser generator under continuous purified N_2 purging. The top and back contact electrode were sputtered using gold with the top contact formed using a physical mask of 0.3 nm. In addition, according to SLIM (Simulation of Laser Interaction with

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Materials) simulation,[143] a 0.2 J/cm^2 laser fluence was approximated to generate surface temperature close to 500°C on a Si substrate. As the Lu_2O_3 film on the Si substrate is relatively thin ~ 5 nm we can safely assume that the effect of laser irradiation on the sample would be close to the simulated value. In this work, we would also make comparison with previously annealed sample using RTA at 600°C, which has shown good characteristics in previous reported works.[28,144]

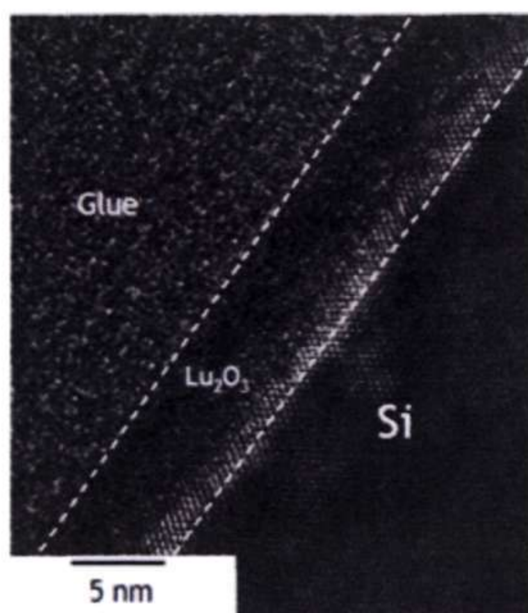

Figure 5-10 Cross sectional HRTEM micrograph of Lu_2O_3 film after subjected to laser thermal irradiation showing an epitaxial behavior at the interface.

The sample that was thermally irradiated using laser fluence at 0.2 J/cm^2 was observed under the HRTEM. Figure 5-10 showed a cross-sectional view of the Lu_2O_3 film HRTEM micrograph after it was thermally laser annealed. It can be observed from the HRTEM micrograph that the thickness of the Lu_2O_3 is about 4.5 nm thick. Furthermore, close inspection on the HRTEM micrograph revealed that there is a crystalline interfacial layer with certain degree of epitaxy. Disregarding the interfacial layer, the bulk of the film appeared to be amorphous in nature. In order to understand the

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nature of the film after subjected to laser thermal irradiation, the sample was analyzed using HRBS.

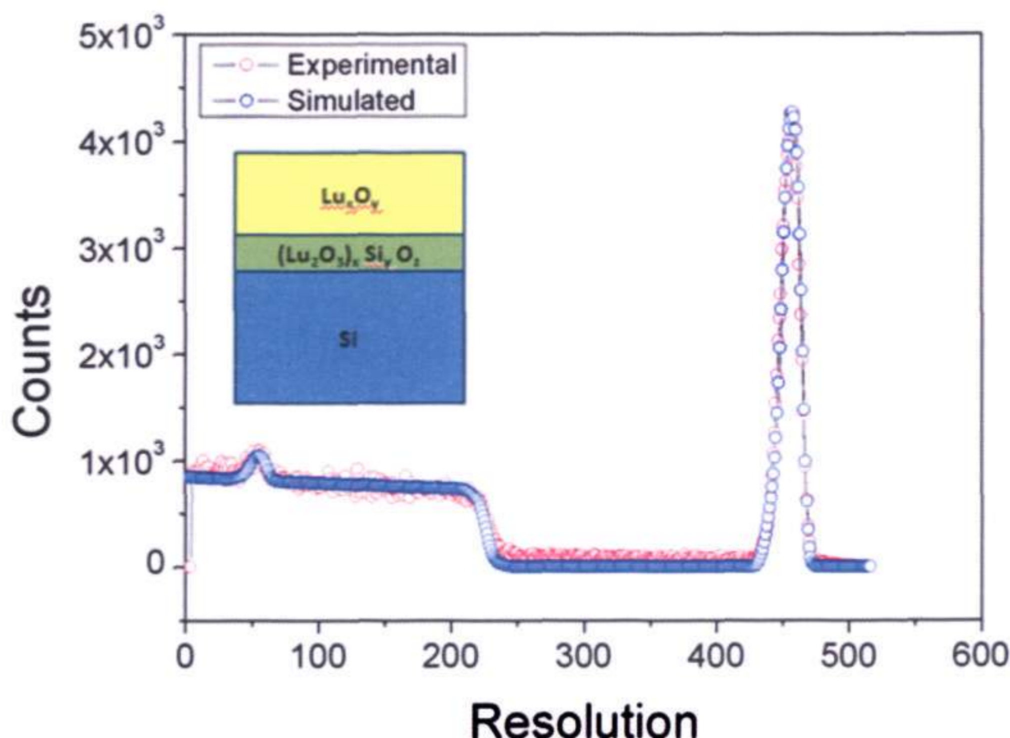

Figure 5-11 A plot of HRBS spectrum of Lu_2O_3/Si observed at scattering angle of 65°. The inset showed the simulated layers in the Lu_2O_3 stack, which correspond closely to the observed HRTEM micrograph.

In the HRBS analysis shown in Figure 5-11, the experimental data was fitted using HRBS simulation software SIMRA and the resulting simulated curve is shown in blue. Based on the simulation data, it was revealed that the stack was made up of two distinct layers, with an approximately 1 nm thick Lu-based silicate layer found near the interface. This corresponded well to the representation shown by the HRTEM micrograph shown in Figure 5-10. As mentioned earlier in this section the heat that is generated by the thermal laser annealing would have likely to be generated on the Si substrate itself, rather than

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trapped in the Lu_2O_3 film. This is because according to a study previously conducted on the optical properties of Lu_2O_3, the Lu_2O_3 film exhibited weak absorption for wavelength below 400 nm. In addition, the extinction coefficient of Lu_2O_3 film was approximated to be around 0.005.[145] The significance of this finding is that the low extinction coefficient of Lu_2O_3 would have translated to an absorption depth of approximately 3.94 μm. This is much thicker than the film that we have deposited, which is approximately 5 nm thick. Due to the heat generation being likely been on the Si substrate itself, the crystalline epitaxial-like layer found on the interface could have been formed via the silicate layer crystallization through local rearrangement of atoms at the interface with the thermal excitation generated through the laser irradiation. The sample was also electrically characterized. The typical capacitance-voltage curve obtained through the measurement is shown Figure 5-12 (a) and (b). A quick inspection on the C-V curve showed that that the curve was well-shaped with negligible hysteresis based on the forward and reverse sweep done on the sample, which suggests that there are minimal interface trapped charges in the film. In addition, we have made comparison of the C-V characteristic between the laser annealed sample and another sample annealed in oxygen ambient at 600°C. Based on the previous study conducted, 600°C annealed sample in oxygen ambient seemed to exhibit the best C-V curve, which makes it a suitable choice to benchmark against the laser annealed sample.[146] It can be seen from Figure 5-12 (b) that there was a significant difference in the accumulation capacitance value. The laser thermal irradiated sample has shown an improvement of the accumulation capacitance of about six times larger than its RTA counterpart. Based on the calculation done on the obtained results, without taking into account the quantum mechanical tunneling, a κ value of 45.0 and 12.2 was obtained for the laser annealed and RTA annealed samples respectively. Further calculation

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revealed that the EOT for the relatively thin Lu_2O_3 sample is about 0.39 and 1.44 nm for the laser annealed and RTA annealed sample respectively.

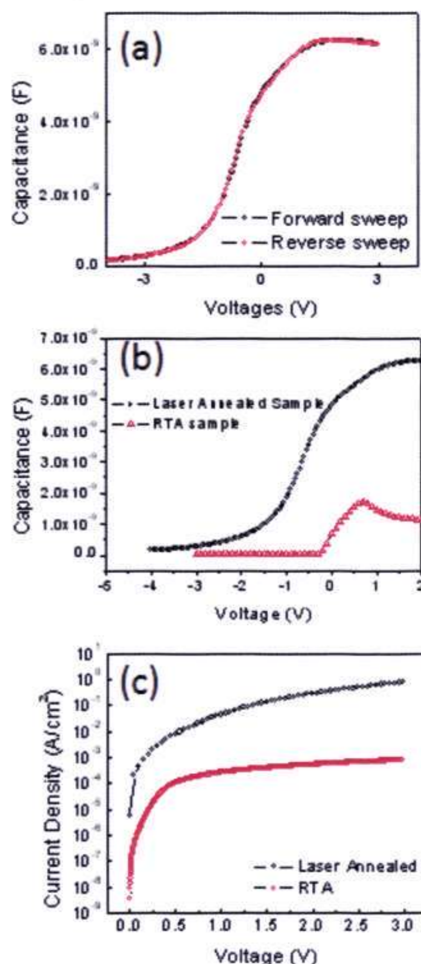

Figure 5-12 Electrical characterization of Au/Lu_2O_3/Si n-type MOS capacitors. (a) Capacitance-Voltage measurement at 100 kHz, (b) the Capacitance-Voltage curve comparison between laser annealed and conventional rapid thermal annealed sample, (c) Current density-Voltage curve comparison between laser annealed and conventional rapid thermal annealed sample

For the observed significant discrepancy in the accumulation capacitance and subsequently the κ value of the Lu_2O_3 dielectric, we attempt to explain the phenomena through the epitaxial layer[147] that was formed after the annealing step that was seen in the HRTEM micrograph. It is known that for insulating materials, there are two major factors

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that form the static dielectric function. These two factors are the ionic and the electronic contributions.[148] The bulk of the dielectric constant would come from the ionic contribution as the electronic contribution would typically be less than 16.[148] As such, we postulate the possibility of the formation of a higher degree of ionic polarizability that has come about due to the re-arrangement of atoms near the interface with highly regular crystallinity as a result of the laser irradiation as shown in Figure 5-13. The higher degree of the ionic polarization in the film would in turn lead to a higher dielectric constant in the film. Moreover, there may be a multiplying effect of the polarization in the crystalline interfacial region due to the long-range nature of crystalline material thereby giving a higher degree of polarization in the film.

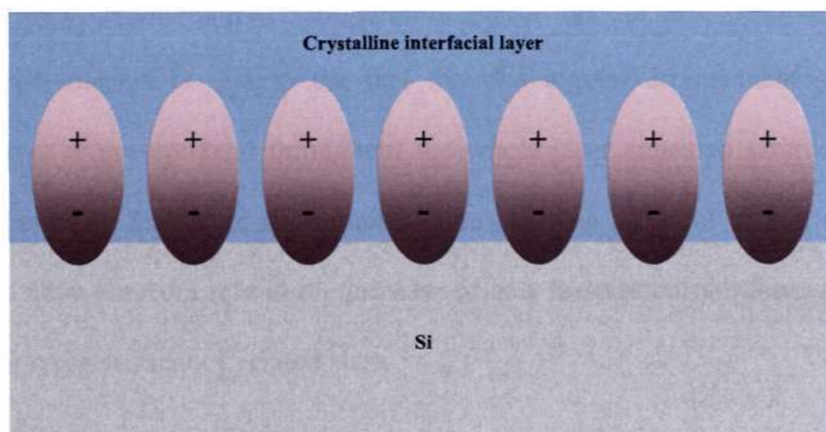

Figure 5-13 A schematic illustration showing that the regular crystalline arrangement in the interfacial layer might have resulted in better charge distribution in the dielectric film thereby causing higher degree of polarization.

The improvements seen after laser anneal treatment has been seen in other materials lately, such as $Hf_xZr_{1-x}O_2$.[149] In the work of Triyoso *et al*,[149] major improvement in the morphology of the film was observed, in which voids were not observed in all laser annealed films as opposed to the conventional rapid thermal annealing. Moreover, with

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laser annealing, it was found that the morphology of the films is smoother. More notably and significantly, only devices with film subjected to laser annealing is able to function and give good results whereas devices with rapid thermal annealed films cannot work.[149] Another recent report by Heo *et al* has shown that laser annealing is able to suppress the formation of interfacial layer growth significantly such that it improves the electrical performance of the device.[150]

The current density-voltage (J-V) behavior of the laser is shown in Figure 5-12 (c). From the plot, the leakage current density at + 1 V bias for the laser annealed sample and rapid thermal annealed samples are 4.34×10^{-2} A/cm^2 and 2.60×10^{-4} A/cm^2 respectively. We noted the increase in the leakage current density for the laser-annealed sample as compared to its RTA counterpart. One possible reason for the observed increase in the leakage current density is due to the fact that the regular arrangement seen at the interfacial layer is not epitaxial throughout the whole laser annealed sample. As such, there is a possibility that there are certain regions in with different crystal orientation, which would have played a role in the increase of gate leakage current through the grain boundaries or oxygen vacancy related sites.

Further study was conducted on the effect of laser irradiation on the samples. In this study, p-type Si (100) substrate was used, on which ~ 6 nm thick Lu_2O_3 film was deposited on. The laser fluence was varied from 0.2 J/cm^2 right up to 0.4 J/cm^2 under Ar gas purge. The obtained C-V curve for the samples subjected to various laser fluence for single pulse anneal is shown in Figure 5-14. From the C-V curve, it can be observed that laser anneal did improve the accumulation capacitance as has been previously observed, comparing to the as-deposited sample. Based on our observation, it was seen that for a

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single pulse laser fluence, the accumulation increased for laser fluence set at 0.2 and 0.3 J/cm^2 and dropped significantly when the laser fluence was increased further to 0.4 J/cm^2.

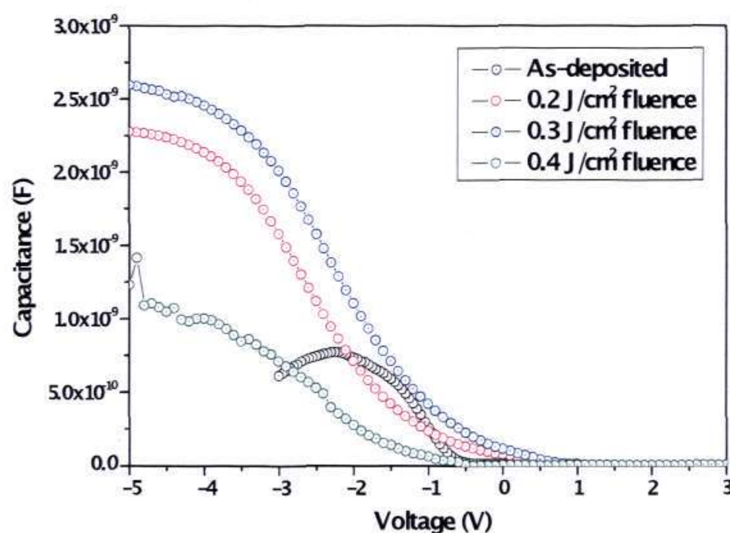

Figure 5-14 An electrical characterization of capacitance-voltage curve for Lu_2O_3 samples subjected to laser anneal under various laser fluence.

Based on the plot obtained in Figure 5-14, the κ value was calculated to be 7.4, 21.8, 25.0 and 10.5 for the as-deposited, 0.2 J/cm^2, 0.3 J/cm^2 and 0.4 J/cm^2 annealed sample respectively. From this work, it can be seen that 0.3 J/cm^2 seemed to have generated the highest κ value, which is about twice the value reported for Lu_2O_3 elsewhere using conventional RTA annealing. This suggest that 0.3 J/cm^2 laser fluence seemed to generate the optimum heat energy on the Si substrate such that it provides sufficient energy for an efficient atomic re-arrangement such that it gives a higher dielectric constant due to the increased ionic polarization contribution in the Lu_2O_3 film. The subsequent drop in the accumulation capacitance when the sample was annealed at 0.4 J/cm^2 probably resulted from damage of the film because the laser energy was set too high. This needs to be verified further in subsequent work. What is worth noting in this

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work is that the laser energy set to anneal the sample has a narrow window of only 0.1 J/cm^2 difference between an improvement in the electrical property of Lu_2O_3 and degradation of the Lu_2O_3 film. Selection on the suitable laser energy must therefore proceed with caution.

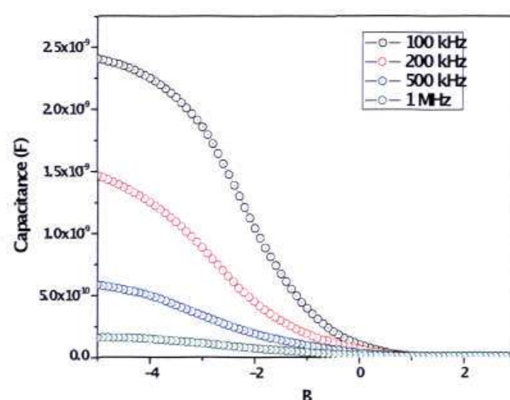

Figure 5-15 A capacitance-voltage measurement of Lu_2O_3 subjected to 0.3 J/cm^2 laser fluence during laser annealing, measured at various frequencies.

On the 0.3 J/cm^2 laser irradiated film; a family of C-V curve measured at various frequencies ranging from 100 kHz up to 1 MHz was also measured, as shown in Figure 5-15. Unfortunately, a large dispersion of the C-V curve was observed when measured under various frequencies unlike its RTA annealed counterpart shown in Figure 4-9, in which only a slight dispersion of the C-V curve is observed. The dispersion of the C-V curve could have had been resulted from series resistance, leakage current, surface roughness among others, including the quality of the film during deposition/post deposition treatment. In order to ensure parasitic effect and series resistance did not come to play, the gold electrodes were sputtered in better vacuum condition (at ~ 5.0×10^{-6} Torr) and the back electrode was deposited over large area of the substrate wafer.

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Connectors and cables were kept to the minimum to avoid parasitic effects. The test was only carried out after a dummy SiO_2 C-V behavior has been shown to have no dispersion with frequency thereby confirming that the subsequent tests are not affected by series resistance and parasitic effects. Thus, for the observed dispersion of C-V behavior with frequency could have been caused by the short duration of the laser anneal and the area that the laser covers during the single pulse anneal, which may not be able to alleviate defects present in the film effectively and uniformly (during the possible melt and re-crystallization stage), which result in the observed frequency dispersion in the measured C-V curves. In addition, the highly dispersed behavior of the capacitance versus voltage when swept at various frequencies suggests that the film is highly conductive, a typical behavior exhibited by space charge present in the film. This may explain the high "effective" calculated κ value from the laser annealed Lu_2O_3 film.

Another experiment was conducted to investigate the effect of laser anneal when the sample was irradiated by more than one pulse. The C-V curve obtained from the experiment is shown in Figure 5-16. It was observed from this experiment that there was severe degradation on the accumulation capacitance when the film was laser annealed more than one pulse. This was further confirmed when the sample was laser annealed for 3 pulses, where no proper C-V curve could be obtained (not shown in Figure). One possible explanation is similar to the one given for the 0.4 J/cm^2 laser fluence anneal, whereby the film is most likely to have been damaged due to the subsequent pulses, which might have cause the film to be ablated. Further work was needed to confirm this point, which was currently under progress.

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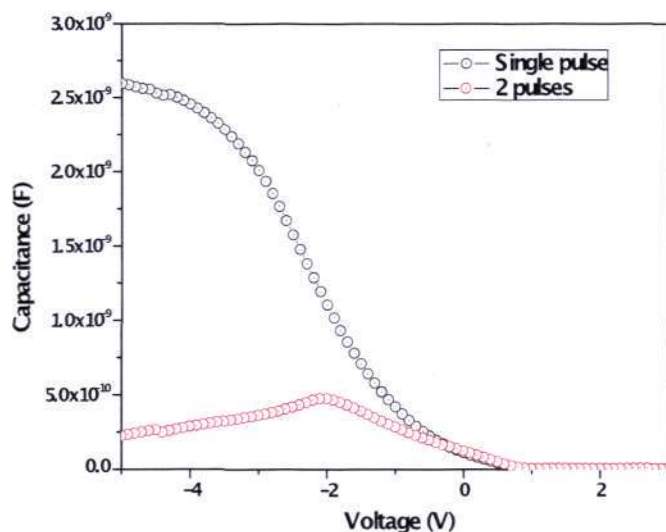

Figure 5-16 A capacitance-voltage measurement of Lu_2O_3 subjected to laser annealing with laser fluence set at 0.3 J/cm^2 with single or double pulse.

5.5 Summary

In summary, in this section we have seen the effect of rapid thermal annealing on the strain in the Si studied using HRBS. It was found that this strain was present up to a penetration depth of up to ~ 6 nm. The highest strain was found in the as-deposited sample at ~0.7%, and this were subsequently reduced with annealing introduced in the sample. Also, with HRBS analysis, the composition changes could be analyzed. The formation of Lu-based silicate layer was confirmed through this study. In addition, the effect of conventional rapid thermal annealing on the energy band alignment for the interfaces of Lu_2O_3/Si was also investigated. The conduction band offsets for the Lu_2O_3/Si interface was found to be 2.15, 2.28 and 2.60 eV for the as-deposited, 400 and 600°C samples respectively. This corroborates well with previously measured leakage

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current density data in which a smaller leakage current density was found with heat treatment introduced to the sample. Finally, in this chapter, a novel way of post-deposition treatment was introduced. When Lu_2O_3 film was subjected to laser thermal irradiation, good electrical properties could be obtained. A high-κ value of 45 and EOT of 0.39 nm was obtained. It is to be noted however that the high κ value could have been obtained due to the high conductivity as observed in Figure 5-15, a behavior typically exhibited by space charge. Laser annealing seemed to have opened another alternative post-deposition treatment in rare-earth dielectric film, which may bring about further improvements in the MOSFET processing and may allow the selection of wider choice of materials.

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Chapter 6 RARE EARTH OXIDE HIGH-κ GATE DIELECTRIC ON GERMANIUM SUBSTRATE

6.1 Background

In the previous chapters the properties of Lu_2O_3 on Si was discussed extensively. The focus of this chapter is to explore further the application of Lu_2O_3 on a different substrate, in this case is germanium. Germanium was previously found unsuitable to be used as a common substrate for MOSFET devices due to its unstable native oxide at a relatively low temperature of 400 to 450°C.[151] Moreover, as compared to silicon substrate in which the typical density of intrinsic defects is usually at 10^{12} cm^{-2} or less, the interface defects in germanium surface is usually in the range of 10^{13} cm^{-2}.[151,152] As such, in the recent year, especially with the evolvement of high-κ dielectrics, much progress have been made with regard to Ge surface passivation using various methods such as thermally grown GeON interfacial layer[153], H_2S surface treatments[154] and the use a capping layer of Si or other materials.[155]

6.2 Lu_2O_3 high-κ gate dielectric on germanium MOS device

In order to meet the requirement of device performance of the future, there is a need for MOSFET devices to be developed in other aspect for high-speed operation. One of the

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ways to improve further device performance is through stress-induced enhancement of the charge mobility in the semiconductor channel. Unfortunately, there is a limit in which the charge mobility can be enhanced trough straining the channel. Therefore, there is a need to look for an alternative channel material. The emergence of high-κ dielectrics has opened up possibilities for this substrate, which has been known to have high electron and hole mobility for carrier transport.[87]

Unfortunately, Ge is not without limitations. The native oxide of germanium is highly unstable and has been known to degrade easily in water as well as give a poor electrical properties.[156] Moreover, it has been known that the native germanium oxide could thermally decompose and desorbs from the surface at a relatively low temperatures and subsequently caused the formation of point defects on the surface.[157-159] This needs to be avoided because the defects that formed could act as recombination and generation centers due to the small bandgap of Ge.[160] This would certainly cause issues in the MOSFET device performance. Therefore, based on these issues that are faced by the native oxide of germanium, there is a motivation in looking at a suitable material to replace native germanium oxide as a gate dielectric. Through the introduction of high-κ dielectric on a Ge substrate as a replacement of the thermally oxidized layer of Ge, it has been shown that a thin EOT as well as high mobility in the device can be achieved.[161] This has escalated the interest in the research of a suitable dielectric material for the new channel materials, which can be germanium or gallium-arsenide. Rare-earth oxides such as La_2O_3, Yb_2O_3 and Lu_2O_3[28,34,70,144] have been shown by many research groups to show potential for the next generation of high-κ gate dielectric material, which is thermally stable on Si, even at high temperatures. The properties of Lu_2O_3 have been shown extensively in the previous two chapters. Therefore, in order for germanium to be

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developed as an alternative channel material, it is important that the interface of Ge to be passivated or deposited with a stable interfacial layer. Efforts to improve the stability of the interface include the nitridation of Ge surface[162] as well as by depositing intentionally a GeON interfacial layer.[163] This work explores the possibility on using Al_2O_3 as suitable passivation layer on Ge. Although the use of Al_2O_3 has been extensively used on Si based devices, its use in Ge is still limited.

In this work, an n-type (111) Ge wafer was used. Prior to film deposition on the Ge substrate, the Ge wafer was cleaned by conventional wet cleaning of cyclic diluted HF (1:100) dip, followed by rinsing in DI water after each dip. Subsequently, the substrate was treated with NH_3 plasma to encourage the formation of oxynitride layer. Following that, a thin Al_2O_3 layer was deposited on the substrate by atomic layer deposition (ALD) using trimethylaluminium (TMA) and O_2 plasma precursors. The ALD equipment used is Oxford FlexAL^{TM} system. After the Al_2O_3 deposition, Lu_2O_3 film was deposited ex-situ using the PLD under a base pressure of 1×10^{-7} Torr. This was done in order to effectively passivate the Ge substrate surface and to suppress the formation of the unstable Ge native oxides. Subsequently, a rapid thermal annealing was done on the sample in N_2 ambient for temperatures ranging from 300°C up to 600°C. MOS capacitor was then fabricated through the methodology outlined in chapter 3.

A cross sectional HRTEM micrograph was obtained for the Lu_2O_3/Al_2O_3 stack after the rapid annealing step at 600°C. This is shown in Figure 6-1. It can be observed from the micrograph that the film appeared continuous with no distinct layer to indicate the deposition of Lu_2O_3 or Al_2O_3. From the HRTEM micrograph, the thickness of the film was shown to be approximately 7-8 nm. In addition, it was noted from the micrograph

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that the interface between the substrate and the film is abrupt, indicating that there was absence of the formation of unstable interfacial layer.

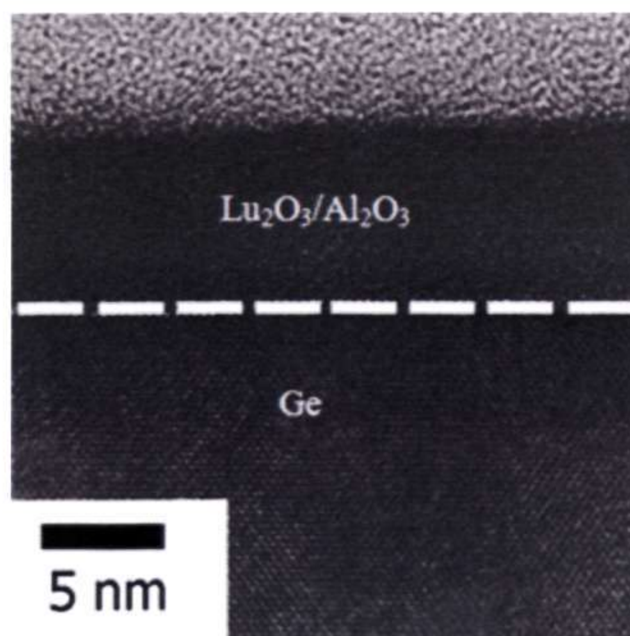

Figure 6-1 A cross sectional HRTEM micrograph of Lu_2O_3/Al_2O_3 stack after rapid thermal annealing at 600°C.

A secondary ion mass spectroscopy (SIMS) analysis was also conducted on the Lu_2O_3/Al_2O_3 stack annealed at 600°C. Based on the analysis of the SIMS spectra as shown in Figure 6-2, it was found that there was an out diffusion of both Ge and Al elements throughout the Lu_2O_3 film. This finding closely corroborates with the HRTEM micrograph, in which the supposedly 2-layered structure of Lu_2O_3 and Al_2O_3 is found as a single layer film. This observation is probably best explained through the intermixing model that was first proposed by Y. Kamata.[164] Similar to the mechanism based on this model, it is possible that both Al_2O_3 and Lu_2O_3 were able to intermix with residual GeO_x or through the formation of GeO_x at the deposition/annealing step. This is illustrated in Figure 6-3. This was previously observed in the case of ZrO_2 and Y_2O_3.[165,166] As such, it

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was plausible to consider that after the intermixing process, the $Lu_2O_3/Al_2O_3/GeO_x/Ge$ stack was converted to Lu/Al-based germanate without an observable interfacial layer after the annealing step.

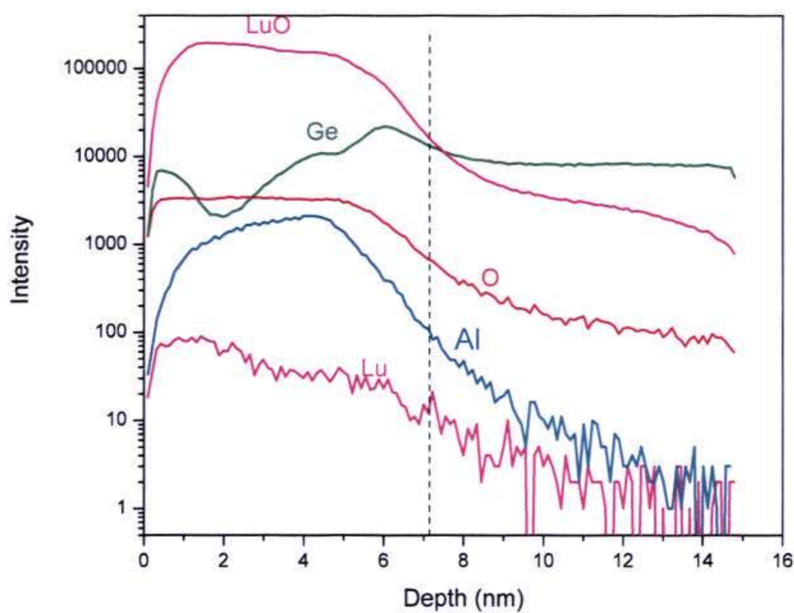

Figure 6-2 A secondary ion mass spectroscopy (SIMS) analysis of the Lu_2O_3/Al_2O_3 stack annealed at 600°C.

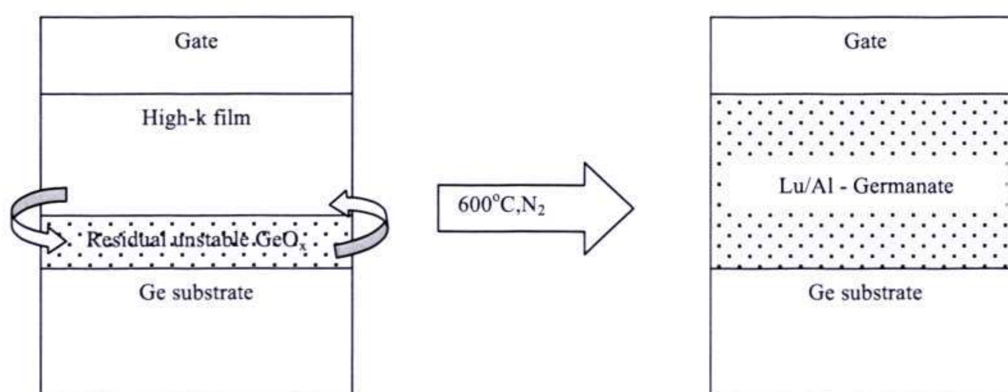

Figure 6-3 A schematic diagram of the possible reaction resulting from rapid thermal annealing done on the Lu_2O_3/Al_2O_3 thin film at 600°C in N_2 ambient. This model was first proposed by Y. Kamata *et al.*

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A HRBS analysis done on the sample (as shown in Figure 6-4) revealed that the Ge content found in the high-κ film increases with increasing annealing temperature. In addition, HRBS spectra fitting on the various annealed samples confirmed that annealing the samples promoted the growth of Lu-based germanate. Based on the fitting of the experimental data with the simulated curve using SIMNRA software, it was revealed that there was partial conversion on the 300°C sample and full germanate conversion for the 400 and 600°C samples; suggesting intermixing in the film stack. Further analysis on the HRBS data revealed that the presence of Ge in the high-κ film stack increases by approximately 4% (as shown in Table 6-1) in the 600°C annealed sample as compared to the as-deposited sample. This finding implies that the intermixing process with possible Ge out-diffusion and/or residual GeO_x in the stack seemed to be more efficient at higher annealing temperature.

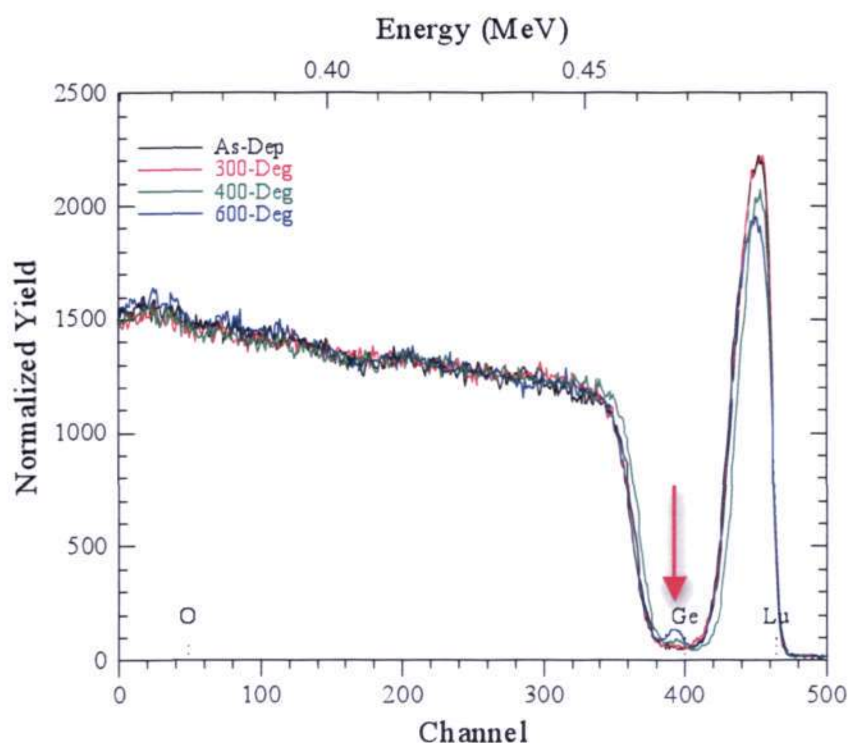

Figure 6-4 A HRBS spectra of $Lu_2O_3/Al_2O_3/Ge$ samples: as-deposited, 300, 400 and 600°C annealed samples in N_2 ambient. The red arrow indicates the increasing intensity of Ge with increasing annealing temperature in the high-κ stack.

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Table 6-1 Ge at% present at the film based on HRBS spectra fitting calculation

Sample	Total number of atoms in film	Total number of Ge atoms in film	Ge at% in film
As-deposited	3.030×10^{16}	1.50×10^{15}	4.95
300°C	3.340×10^{16}	1.65×10^{15}	4.95
400°C	2.800×10^{16}	1.91×10^{15}	6.83
600°C	3.500×10^{16}	3.09×10^{15}	8.82

Electrical characterizations were also done on the $Lu_2O_3/Al_2O_3/Ge$ samples. A capacitance-voltage measurement of the samples taken at a frequency of 100 kHz is shown in Figure 6-5. Based on the observation on the C-V data, the obtained curves were relatively well-shaped despite the presence of a number of humps, which was indication of the presence of slow traps as well as relatively large interface trap density as shown by the relatively stretched out C-V curve. It was noted from the C-V curve that the accumulation capacitance increases with increasing annealing temperature. Based on the obtained accumulation capacitance, a κ value of 11 .7 was calculated, without taking into account the quantum mechanical tunneling effect. This translates to an equivalent oxide thickness of 2.42 nm for the stack. The calculated value in this work is close to the reported value for Lu_2O_3 on Si substrate of about 11-12.[28,34,144] The electrical data shown by the C-V curve seemed to support earlier postulation that the intermixing was improved with higher annealing temperature and thereby improving the capacitance performance of the MOS stack with contributing factors of defect alleviation and densification of the film. The improvements in the κ value of the MOS stack is evident as the κ value obtained increases from 9.9, 10.8 and 11.7 for the as-deposited, 300 and 600°C annealed samples respectively. From the obtained C-V data, it suggests that the Al_2O_3 layer is an effective passivation layer. In this case, we believed that the Al_2O_3 layer might have aided in the prevention of the formation of low quality interfacial GeO_2[167,168] by acting as an

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effective oxygen reaction barrier. This is likely to be true because GeO_2 and Al_2O_3 have a heat of formation of 43.9 kJ/mol and 1675 kJ/mol respectively.

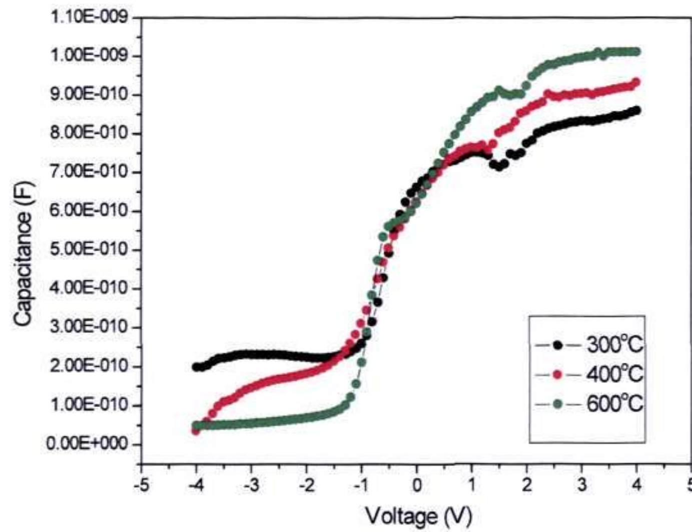

Figure 6-5 C-V curve of Au/(Lu/Al) Germanate/Ge capacitors measured at 100 kHz frequency.

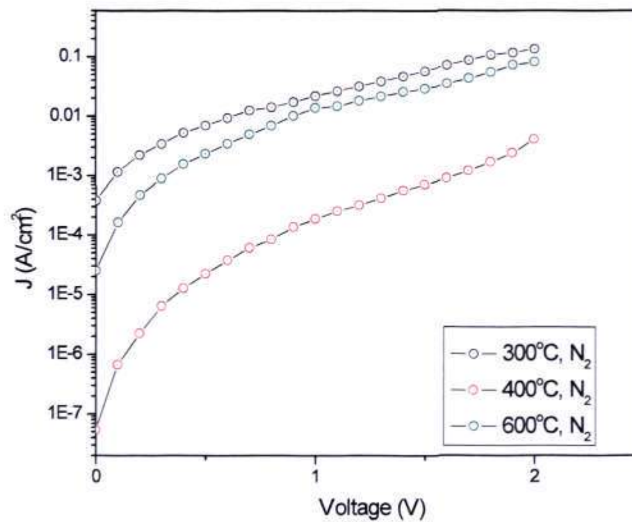

Figure 6-6 J-V curves of Au/(Lu/Al) Germanate/Ge capacitors of the samples annealed between 300°C to 600°C in N_2 ambient.

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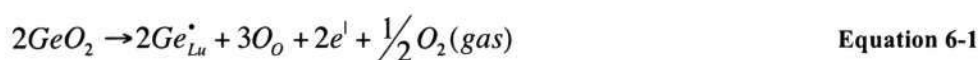
Figure 6-6 revealed the general trend of the J-V characteristics measured from the rapid thermal annealed samples. Based on the obtained data, the leakage current at +1 V bias is 2.19×10^{-2} A/cm^2, 1.87×10^{-4} A/cm^2 and 1.37×10^{-2} A/cm^2 for the 300°C, 400°C and 600°C samples respectively. It was noted from the data obtained that the leakage current density for the 600°C-annealed sample was higher as compared to the 400°C-annealed sample. One possible explanation for the observed phenomenon is that although intermixing is a necessary condition to stabilize the interface between the high-κ dielectric and Ge, the presence of excess Ge atoms in the high-κ dielectric could quickly lead to a poor electrical performance.[164] Therefore, it was observed in this work that intermixing was promoted with the increment of annealing temperature from 300°C to 600°C. However, it was suspected that the excess Ge content present in the high-κ layer at 600°C might have resulted in the poor leakage current density. As shown in Table 6-1, the Ge content present in the 300°C, 400°C and 600°C annealed sample is approximated to be 5.0 atomic% (at%), 6.8 at% and 8.8 at% respectively. Based on the data, it is plausible that in the 600°C annealed sample, the excess out-diffused Ge atoms in the film may have led to the creation of more defects in the film thereby providing more leakage path leading to the observed higher leakage current density. One possible defect creation equation is shown in below:



$$2GeO_2 \rightarrow 2Ge_{Lu}^{\bullet} + 3O_O + 2e^{\prime} + \tfrac{1}{2}O_2(gas)$$ **Equation 6-1**

Based on this work, although the critical Ge content in the film that will lead to the degradation of the leakage current density is not yet precisely determined, the current contribution of this work offers a reference window in which in between 6.8 at% and 8.8

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at%, degradation in the leakage current density is likely to occur. In order to determine the exact the critical Ge content in which degradation in the leakage current density could be observed, a more detailed experimental work need to be carried out. Therefore, based on the data obtained in this work, the 400°C annealing seems to be optimum for the $Au/Lu_2O_3/Al_2O_3/Ge$ stack in which an acceptable κ value of 10.8 and low leakage current density of 1.87×10^{-4} A/cm^2 can be obtained.

6.3 Summary

In this chapter, the incorporation of Lu_2O_3 on an alternate substrate is investigated. Lu_2O_3 was deposited on Ge substrate with a thin (~ 1 nm) Al_2O_3 film that acts as a passivation layer. HRTEM micrograph shows the absence of abrupt separation of Al_2O_3/Lu_2O_3 films region, which suggests that intermixing have taken place. This is confirmed by SIMS analysis, in which both Ge and Al elements out-diffusion seemed to be observed throughout the stack. The composition of the film is studied through HRBS spectra fitting and the presence of Lu-based germanate film is obtained throughout the stack. In addition, through the HRBS fit analysis, the amount of Ge found in the film could be quantified. It was found that the 600°C-annealed sample contained 4 at.% more Ge as compared to the as-deposited sample. Electrical measurements were also conducted on the $Lu_2O_3/Al_2O_3/Ge$ stack and it was found through the C-V data that a κ value of 11.7 and an EOT of 2.42 nm could be obtained for the 600°C-annealed sample. The κ value obtained in this work is also consistent with reported data of Lu_2O_3/Si system of about 12. [28,34,144] In addition, the absence of interfacial layer for Lu_2O_3 deposition on Ge is consistent with reports from other research group with ALD deposited Lu_2O_3 film,[152]

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which makes the Lu_2O_3/Ge system very attractive to obtain low EOT for future advanced high mobility devices. Unfortunately, an ideal C-V curve was not obtained with humps observed on the curves and it appeared stretched out suggesting presence of slow traps and high interface trap density, although in the ALD deposited Lu_2O_3 conducted by other research group has reported D_{it} of about 10^{12} eV^{-1} cm^{-2} (close to that of Si substrate) and shown hump-free C-V curves, indicating better quality of film as well as electrical performance.[152] The current-voltage characterization revealed that the leakage current density for the 600°C-annealed sample is higher than the 400°C-annealed sample while it was expected to be lower. It was postulated that the presence of excess Ge atoms in the high-κ dielectric could quickly lead to a poor electrical performance, as has been observed by other research group in the literature. The excess out-diffused Ge atoms in the film may have led to the creation of more defects in the film thereby providing more leakage path leading to the observed higher leakage current density.

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Chapter 7 CONCLUSIONS AND FUTURE WORK RECOMMENDATIONS

7.1 Conclusions

In this work, rare earth oxide Lu_2O_3 has been studied extensively as a possible candidate for gate dielectric. The films in this work have been deposited using pulsed laser deposition, a fast and effective deposition system that is able to produce smooth and stoichiometric films.

7.1.1 Properties of Lu_2O_3 high-κ dielectric on Si

As part of the detailed study of Lu_2O_3, the thermal stability of Lu_2O_3 was investigated by subjecting the deposited film with thickness of approximately 5 – 6 nm to various rapid thermal annealing (RTA). Through the morphology study by AFM and HRTEM, it was shown that the amorphous phase of the Lu_2O_3 was successfully maintained even at annealing temperature of 900°C, which is a typical temperature used for source and drain activation during CMOS device processing. The study conducted by XRR and HRBS was revealed that a silicate layer was formed. Formation of Lu-based silicate layer was formed consistently in all samples subjected to the various annealing condition. It indicates that the presence of silicate layer was inherent after film deposition and the growth was promoted through post deposition heat treatment. It was postulated that the formation of the Lu-based silicate layer has resulted from the breaking down of

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O_2 molecule found in air or ambient into its elemental O atoms, which subsequently diffused into the Lu_2O_3 film stack and react with the Si substrate to form SiO_x interfacial layer. Following that, an intermixing step between the SiO_x layer and Lu_2O_3 results in the formation of the Lu-based silicate layer as evidenced by the XRR and HRBS data.

The Lu_2O_3 film stack was electrically characterized after the capacitor device formation. It was found that for a 900°C-annealed sample in oxygen ambient, a κ value of about 11.59 and an EOT of 1.68 nm were obtainable. This result was in fact comparable to the atomic layer deposited Lu_2O_3 film (as-deposited) and electron beam deposited film with similar thickness, in which a κ value of about 11 – 12 was obtained.[28,34] This showed that for the PLD deposited Lu_2O_3 film, although there was evidence of formation of Lu-based silicate layer, the overall κ value of the gate stack did not show significant deviation to the as-deposited value as reported in the literature. The observed Lu-based silicate layer was not observed in the work of G. Scarel *et al*, on ALD deposited Lu_2O_3 film characterized by XPS and RBS.[34] The discrepancy could have resulted in the vacuum condition during the annealing step before the process gas was fed in the chamber. Any amount of oxygen present in the annealing chamber could have resulted in the formation of silicate layer, which would have intermixed readily with the Lu_2O_3 film to form the Lu-based silicate layer. In addition, with the PLD deposited Lu_2O_3, it was found that a D_{it} of about 2.66×10^{13} cm^{-2} eV^{-1} was obtained. This value is about one order higher as compared to the atomic layer deposited film reported by other research group. One possible reason to explain the higher D_{it} value was that it is likely that the film deposited by the PLD was lower in quality as compared to the film deposited by the ALD due to the high kinetic energy bombardment deposition nature of the PLD that may have caused defects on the surface of the deposited film that may have led to higher number of

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interface traps. Comparatively, for atomic layer deposition, which is a special modification of the chemical vapor deposition process, is a slow process with an accurate control of thickness through its self-limiting growth process.[169] The growth of film on an ALD is usually one monolayer.[169] Therefore, due to its chemical reaction nature and very controlled film growth, the formation of films using the ALD should be of high quality with little defects. As for the leakage current density (J-V) behavior, a leakage current density of 1.0×10^{-4} A/cm^2 was obtained. With reference to the ITRS roadmap 2008 for low standby power devices, the leakage current density obtained at +1 V bias for the PLD deposited film is able to meet the requirement for sub 38 nm technology node.

Also, the leakage current conduction mechanism in Lu_2O_3 was investigated through the careful study of the leakage current behaviors of various samples with different thickness, annealing conditions measured at a range of substrate temperatures. Through the fitting of the J-V curves obtained with a number of DC conduction mechanism models available, it was found that the Poole-Frenkel leakage current conduction mechanism best fitted the PLD deposited Lu_2O_3 sample. The obtained result corroborates well with the observed J-V characteristic in which, a lower leakage current density in samples annealed in oxygen ambient was found to be lower than that of nitrogen-annealed samples. Furthermore, it was found that the net fixed charge density as well as its leakage current density might be modified significantly, depending on the post annealing condition through the study of the effect of light illumination on the Lu_2O_3 MOS device. This would encompass the capability of traps present in the film to trap and de-trap charges through its interactions with photons.

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In a more comprehensive study of the effect of various post-deposition processes on the Lu_2O_3 film stack, it was found through the HRBS angular scans on the various annealed samples that strain modification on the Si substrate can be modified through the introduction of post deposition anneal. It was through this study that the effect of the post deposition annealing on the strain present in the Si was investigated. It was found that the highest strain exists on the as-deposited sample (~0.7 %) and was gradually decreased with increasing annealing temperature into below detection limit at the 800°C-annealed sample.

7.1.2 Investigation on the effect of various post deposition treatments on Lu_2O_3 high-κ dielectric film

The possible role of rapid thermal annealing on the band alignment of Lu_2O_3 was also investigated in this work through the valence band spectra of Lu_2O_3 film obtained through XPS. By the application of Kraut's method, it was found that the conduction band offsets for Lu_2O_3/Si interface was found to be 2.15, 2.28 and 2.60 eV for the as-deposited, 400°C and 600°C samples respectively. The obtained values of the conduction band offset obtained through this study corresponded well with the measured leakage current density data, in which a smaller leakage current density value was observed with larger annealing temperature performed on the samples.[28] The reduction in the leakage current density is likely related to a large electron barrier height due to the reduction in the interfacial dipole that would effectively reduce the electron Schottky emission, which is dominant contribution on the gate leakage current density.

A significant contribution of this work is the study conducted on the effect of laser treatment on a high-κ gate dielectric film. This is the first time (to our best knowledge)

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that laser annealing is used as a post-deposition treatment for gate dielectric film purposes. It was through this novel method that a significant improvement in the accumulation capacitance for laser energy not larger than 0.3 J/cm^2 was found. The best improvement of the gate dielectric behavior obtained through this study for ~ 6 nm thick Lu_2O_3 film irradiated with 0.2 J/cm^2 laser energy is a κ value of 45 and an EOT of 0.39 nm, which is four times improvement as compared to its rapid thermal annealed counterpart. This was likely to have been caused through the enhanced ionic polarization present in the film that has come about due to the re-arrangement of atoms near the interface with highly regular crystallinity as a result of the laser irradiation.

7.1.3 Rare earth oxide high-κ gate dielectric on germanium substrate

In our effort to investigate the suitability of Lu_2O_3 on a next-generation high-mobility substrate, the behavior of Lu_2O_3 on Ge substrate was investigated. The Ge substrate was pre-deposited with a thin layer of Al_2O_3, after which, a NH_3 plasma nitridation was performed. About ~ 6 nm of Lu_2O_3 film was deposited by the PLD followed by rapid thermal annealing at various annealing temperatures. Intermixing was suggested to have occurred in the Lu_2O_3/Al_2O_3 stack since there were absence of clear and abrupt separation between the Lu_2O_3 and Al_2O_3. Out-diffusion of Ge and Al elements were clearly illustrated in the SIMS analysis, and HRBS compositional analysis through spectra fitting suggested that presence of Lu-based germanate throughout the dielectric stack. Also in this study, the amount of Ge present in the film was quantified through HRBS spectra fit analysis. It was found that the Ge content in the film was 4 atomic% higher in the 600°C annealed sample as compared to the as-deposited sample. Correlations with the leakage current behavior were established, in which the leakage

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current density for the 600°C-annealed sample was found to be higher than the 400°C-annealed sample. This suggests that the presence of excess Ge atoms in the high-κ dielectric could quickly lead to poor electrical performance as had been observed by other research group in the literature.[164] The excess out-diffused Ge atoms in the film may have had led to the creation of defects in the film, thereby providing more leakage path in the film stack thus leading to the observed higher leakage current density. Furthermore, a κ value of 11.7 (result is comparable to ALD deposited Lu_2O_3 film on Si[28,34,144]) and EOT of 2.42 nm were obtained. The significance of this study is that we have shown that it is possible for Lu_2O_3 to be integrated into high mobility substrate such as Ge, which was previously plagued with issues due to the unstable native oxide of Ge. Also, the relatively low leakage current density of 1.87×10^{-4} A/cm^2 was obtained for the 400°C-annealed sample, which has met the requirement for sub 38 nm technology node in the ITRS roadmap (version year 2008). Through the quantification of Ge content in the Lu_2O_3/Al_2O_3 stack, it was deduced that the amount of Ge content might have played a role in the degradation of the leakage current density, in which if the critical value is exceeded, a degradation of the leakage current density could be observed. Therefore, this work has provided a reference window in which the degradation of the leakage current density could occur when the critical germanium content (likely to be between 6.8 and 8.8 atomic.%) is exceeded.

7.2 Future work recommendations

Several possible topics are worth exploring as continuation of this work. More in-depth study on the effect of strain resulting from Lu_2O_3 deposition on the Si channel is

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worth looking into in terms of its horizontal strain. The study described in this work only quantifies the vertical strain using the angular scan of HRBS. The Convergent Beam Electron Diffraction (CBED) method with could be employed for this purpose. Through the careful study of the HOLZ lines formed in the CBED pattern, the determination of local strain tensor with high spatial resolution within ± 0.01 %.[170] In this technique, CBED patterns from the Si substrate could be captured at various depths from the film interface as illustrated in Figure 7-1. The position A is the deepest in the Si substrate, which can be safely assumed as the unstrained (normal) condition. Subsequently, CBED patterns are captured at positions B, C and D, with D being the nearest to the Lu_2O_3/Si interface. Jems Microscopy Simulation Software is then used to simulate the exact CBED patterns that are captured from the various positions.

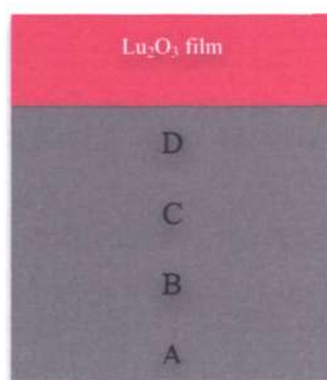

Figure 7-1 Location of captured CBED patterns on the Si substrate (in grey) at various depths from the interface.

When simulating the CBED patterns using Jems microscopy simulation software, one must bear in mind to input the correct microscope details and the zone axis. The patterns are then adjusted based on trial and error by adjusting the camera length, the half

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convergence, LOUE zone number or HOLZ threshold until the simulated CBED pattern matches exactly the one obtained experimentally. When the exact match is obtained, the atomic cell parameters can be obtained thus any strain in the Si substrate can be calculated. It would be interesting to be able to establish if there is any horizontal strain present in the Si substrate as well as in device configuration, and whether this strain will diminish as observed in the vertical strain when heat treatment is introduced.

The second recommendation, which is very closely related to the first, is on the integration of Lu_2O_3 gate dielectric on a working MOSFET device. This work is worth pursuing because it has been shown in this work on the potential of Lu_2O_3 as a suitable candidate for high-κ dielectric. The extension of this work on a transistor scale would form a more realistic picture on the suitability of Lu_2O_3 as a gate dielectric through the various device characterizations possible and benchmarked against SiO_2 as well as the current leading high-κ material, hafnia based dielectrics. In relation, the mobility data in the channel of the device can be collected and studied against the possible strain that is present in the Si substrate.

Thirdly, it is believed that the work on the laser annealing on Lu_2O_3 could be explored further. The laser annealing condition could be optimized further through precise laser energy determination. Furthermore, the effects of laser annealing on other oxide materials apart from rare-earth oxides are worth pursuing. The further improvements and optimizations on the laser annealing tools and equipments could possibly open up possibilities of unique materials to be explored. Moreover, the recent development on the use of laser annealing in the source/drain dopant activation makes the use of laser annealing in high-κ dielectric treatment even more attractive because the

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effect of materials that were previously found unsuitable for high temperature post deposition treatment (a condition necessary in MOSFET fabrication) could be re-examined.

The work on Lu_2O_3 on high mobility substrate could be explored further. It is noted that the electrical properties of Lu_2O_3 on germanium, in particular the C-V behavior is not ideal. It would be interesting to study and compare the electrical properties of Lu_2O_3 stack on a passivated Ge layer (through nitridation or through deposition of thin inter-layer) that was deposited through atomic layer deposition or molecular beam epitaxy that may produce better and higher quality films. In addition, the performance of Lu_2O_3 film on the next generation high mobility substrate: GaAs, is also worth looking into.

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