An Investigation Into the Parameters Affecting Total Harmonic Distortion in Low-Voltage Low-Power Class-D Amplifiers

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***Abstract*—We investigate the influence of two important practical design parameters on total harmonic distortion (THD) for the design of low-voltage (0.9–1.4 V) low-power analog Class-D amplifiers: the linearity of the carrier waveform and the impedance of the output stage. We show that the carrier nonlinearity results in THD and propose a novel mathematical analysis method to model the nonlinearity. We recommend a range of the parameter that describes the carrier nonlinearity and that results in a good compromise to the dynamic range of the pulsewidth modulator of the Class-D amplifier. We show that the impedance of the output stage has little effect on THD. We verify our analyses by means of MATLAB and HSPICE computer simulations, and on the basis of practical measurements.**

***Index Terms*—Class-D Amplifier, hearing aids, pulsewidth modulation (PWM), total harmonic distortion (THD).**

NOMENCALATURE

B	DC component of the modulating signal.
J_n	Bessel function of the first kind with integer order n.
k	Zero-input duty-cycle of the pulsewidth modulator (PWM) signal.
K_{mn}	Fourier coefficients of the PWM signal.
m	Carrier harmonic index.
M	Modulation index ($0 \leq M \leq 1$) or equivalently, the value of the signal level normalized to the maximum signal level.
n	Signal harmonic index.
Q	Magnitude of the modulating signal.
t_0	Time constant of the exponential carrier.
T_c	One period of the exponential carrier.
$v_c(t)$	Exponential carrier signal.
$v_{c\text{-}l}(t)$	Leading-edge exponential carrier signal.
$v_{c\text{-}t}(t)$	Trailing-edge exponential carrier signal.
$v_{cl}(t)$	*Linearized* exponential carrier signal.
$v_{cl\text{-}l}(t)$	*Linearized* leading-edge exponential carrier signal.
$v_{cl\text{-}t}(t)$	*Linearized* trailing-edge exponential carrier signal.
$v_{c\text{-}pp}$	Peak-to-peak amplitude of the exponential carrier.
$V_{C\mathrm{sat}}$	Saturation voltage of an exponential waveform (carrier).
$v_s(t)$	Sinusoidal modulating signal.
$v_{s\text{-}l}(t)$	Sinusoidal modulating signal for the leading-edge exponential carrier.
$v_{s\text{-}t}(t)$	Sinusoidal modulating signal for the trailing-edge exponential carrier.
$v_{st}(t)$	*Transformed* modulating signal.
$v_{st\text{-}l}(t)$	*Transformed* modulating signal for the *linearized* leading-edge exponential carrier.
$v_{st\text{-}t}(t)$	*Transformed* modulating signal for the *linearized* trailing-edge exponential carrier.
ω_s	Angular frequency of the modulating signal in rad/s.
ω_c	Angular frequency of the carrier in rad/s.
x_0	Degree of nonlinearity in the exponential carrier ($x_0 = \omega_c t_0$ for trailing-edge or leading-edge exponential carrier, and $x_0 = 2\omega_c t_0$ for double-sided exponential carrier).

Manuscript received October 10, 2001; revised August 14, 2002. This paper was recommended by Associate Editor H. S. H. Chung.

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Digital Object Identifier 10.1109/TCSI.2003.817770

I. INTRODUCTION

MANY current-art portable low-voltage low-power audio devices, including hearing instruments (hearing aids), employ a Class-D amplifier (amp) as the output power amplifier. This is primarily because when appropriately designed [1], Class-D amps can feature power efficiency greater than 90% over a large signal swing (or modulation index) range. This efficiency is substantially superior over classical linear amps, e.g., Class A, B, and AB designs, and is highly desirable in subminiature power sensitive audio applications and where the crest factor of the signal is large, e.g., 15 dB. These applications include portable audio devices, in particular hearing instruments where the power source is a small pill-size battery cell (0.9 –1.4 V operating voltage range) and the size is a premium for aesthetics.

The architecture of an analog Class-D amplifier may be classified into three types: 1) PWM modulation; 2) oversampled sigma-delta ($\sum\Delta$); and 3) "bang-bang control" approach. The Class-D based on PWM modulation is the Class-D amplifier of interest in this paper because of its circuit simplicity, micropower and low-voltage operation (see later).

The $\sum\Delta$ approach is essentially the design of an analog-to-digital converter and its architecture is well established [2]. In view of the critical parameters of a hearing instrument, the first-order $\sum\Delta$ modulator (as opposed to a multi-order $\sum\Delta$ modulator) may be considered. However, we can show that the first-order $\sum\Delta$ modulator consumes

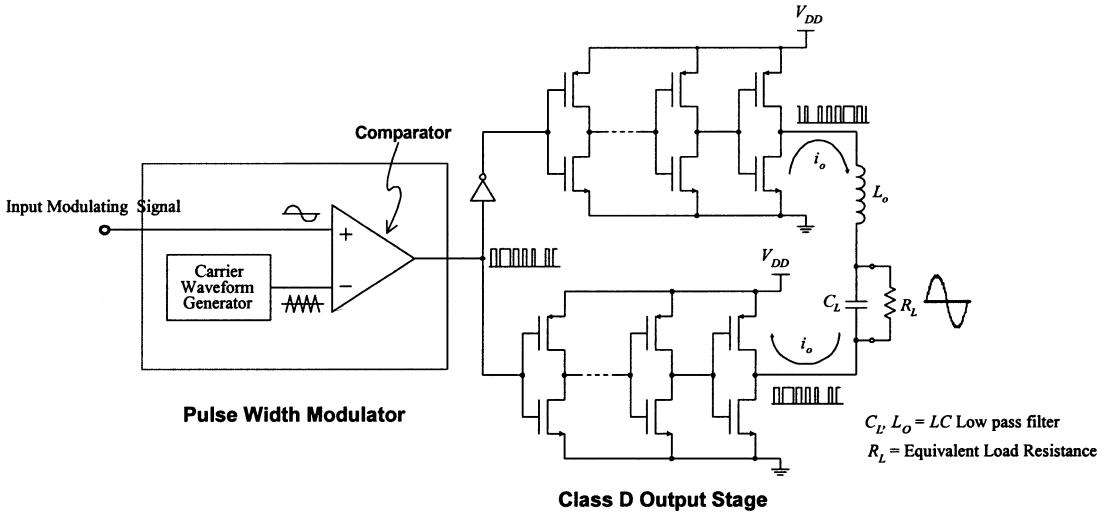

Fig. 1. Schematic diagram of a Class-D amplifier.

approximately 12 times more current and occupies approximately 2.6 times the IC area compared to the PWM modulator. This substantially increased power dissipation and hardware overheads are consequences of the increased circuit complexity and increased clocking frequency. In terms of nonlinearity, the $\sum \Delta$ modulator has improved total harmonic distortion (THD) over the PWM modulation at high modulation indexes (e.g., $M = 0.9$) but comparable THD at low modulation indexes (e.g., $M = 0.2$).

The "bang-bang control" approach [3], on the other hand, is based on an hysteresis band modulator that calculates the error between the desired output and measured output. When this error exceeds a certain bound (or leaves the hysteresis band), the controller will change state to drive the error back within that bound.

The bang-bang control approach typically requires a high clocking rate (depending on the hysteresis of the controller, e.g., 500 kHz–1 MHz) and the circuit complexity is also relatively complex (although somewhat simpler than the first-order $\sum \Delta$). The magnitude of its power dissipation is somewhat comparable to the first-order $\sum \Delta$ approach (and substantially larger than the PWM approach). Its THD is also comparable to the first-order $\sum \Delta$ approach.

In view of the earlier mentioned critical power (and low voltage) and IC area parameters, most analog Class-D amplifiers for hearing instruments are based on the PWM modulator. For these reasons, this class of Class-D amplifiers is the architecture of interest in this paper.

The Class-D amp depicted in Fig. 1 comprises a PWM, an output stage, and an *LC* low-pass filter. At the PWM, the comparator compares the input modulating signal with an internally generated carrier waveform, usually sawtooth-like or triangular-like [4]–[11], and generates a series of width-modulated pulses—the PWM signal. The Class-D output stage is essentially a low-impedance voltage source and is usually bridge configured in low-voltage applications (to increase the output power by a factor of four over the single-ended output). The *LC* low-pass filter attenuates the unwanted carrier signal component of the PWM signal, thereby retrieving an equivalent amplified analog input signal at the load. In some applications [8], it is possible to drive the load directly from the output. These applications, however, require a high frequency carrier ($\sim$256 kHz) and results in higher power dissipation.

The THD of an ideal Class-D amp is theoretically 0% [9], refer to (4) later. However, practical low-power low-voltage Class-D amps suffer from significant THD of the order of 3–5%; [4]–[7]; the reasons for this will be discussed later. Despite the early development [9] and recent interest [1], [4]–[14] in Class-D amps, the mechanisms responsible for nonlinearities such as THD in practical analog implementations, in particular low voltage (0.9 –1.4 V) operation, remain unreported in literature. In classical linear amps, negative feedback is usually applied to suppress the nonlinearities. However, Class-D amps being switch mode (nonclassical), are usually open loop (as opposed to feedback) circuits. The usual application of negative feedback in a Class-D amp is not straightforward because its output is a PWM signal and some of the carrier components remain at the output of the low-pass filter. To be specific, we require substantial PWM signal attenuation [of the order of 30 dB from $\sim$4 to $\sim$40 kHz (carrier clock frequency)] from the output to the summing node of the feedback loop and without excessive phase lag. Furthermore, this should be obtained without prohibitive hardware and power dissipation costs, bearing in mind the critical parameters of hearing instruments described earlier. Consequently, the majority of reported Class-D amp designs [4]–[6] including contemporary Class-D amps encapsulated within the subminiature receivers (loudspeakers) for hearing instruments [14] are open-loop designs and suffer from significant THD.

In this paper, we investigate two important practical parameters in the Class-D amplifier that may contribute to THD: the linearity of the carrier waveform and the finite output impedance (or on resistance) of the output stage. These parameters have implications to the complexity of the design and the resultant IC area [1], [4]–[7], and are usually heuristically chosen by circuit design engineers in the following manner.

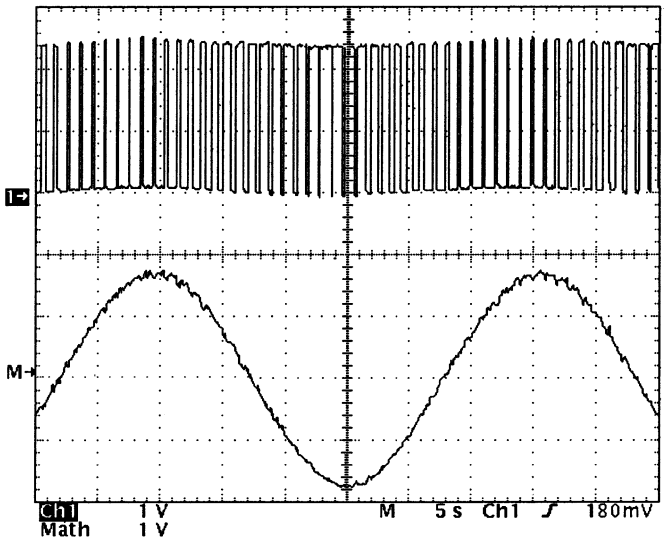

Fig. 2. Measured PWM signal (top) of a Class-D output stage and the demodulated output signal (bottom) across the load.

1) Make the carrier as linear as possible—any nonlinearity in the carrier may directly generate harmonic distortion at the PWM output.
2) Make the output impedance as low as possible—a nonzero output impedance in the Class-D output stage may cause the amplitude of the PWM signal to be slightly amplitude modulated as that depicted in Fig. 2. This may in turn generate harmonic distortion.

We derive, in this paper, a novel mathematical-analysis method to determine the THD with the linearity of the carrier waveform as a key parameter. We show that the nonlinearity of the carrier waveform results in THD and it is imperative to reduce the degree of this nonlinearity to suppress the THD. The analysis provides good insight into the degree of nonlinearity acceptable for a practical low-voltage Class-D amp design. We recommend a range for the parameter that describes the carrier nonlinearity that results in acceptable THD and that results in a good compromise to the dynamic range of the PWM. We also model the impedance of the output stage and show that the output impedance has little effect on THD; the design of the output impedance of the output stage described in [1] is therefore appropriate, especially given the compromise to the IC area. We verify our theoretical derivations and analyses by means of MATLAB and HSPICE computer simulations, and on the basis of practical measurements.

II. Effects of Carrier Nonlinearity and Output Stage On-Resistance on THD

In this section, we analytically investigate the effect of two parameters on harmonic distortion: 1) the degree of carrier nonlinearity in the PWM; and 2) the magnitude of output impedance of the output stage. In each case, we shall assume that all other parameters are ideal.

A. Review of Mathematical Analysis of an Ideal PWM Employing a Triangular Wave Carrier

We will first review the mathematical expression of an ideal PWM output employing a linear triangular wave carrier. This review will serve as a reference to our subsequent derivation of the expression for the output PWM signal of a practical PWM where the carrier is an exponential carrier (refer to Fig. 4 and Section II-B-1 later); it is worthwhile to note that this carrier is used in the majority of low-voltage Class-D amps for practical reasons [4]–[7]. With these analytical expressions, we will subsequently compare the effect of the nonlinearity of the carrier on harmonic distortion.

An input sinusoidal modulating signal can be represented by

$$\begin{aligned} v_s(t) &= B + Q\cos(\omega_s t) \\ &= 2\pi k + M\pi\cos(\omega_s t) \end{aligned} \tag{1}$$

where k is usually set to 0.5 (equivalent to 50% duty cycle at zero-input). We have shown in [6] that it is imperative to observe this in practical Class-D amp designs to obtain a low output bias current in a bridge output stage, thereby taking advantage of the efficiency of the Class-D amp.

There are two types of PWM sampling processes, namely the natural sampling and uniform sampling. The natural sampling process is used in analog PWMs whereas the uniform sampling process applies to digital PWMs. As the PWM of interest is analog, we will only investigate the THD where natural sampling process is used.

The three possible ways of conducting the natural sampling process are single-sided trailing-edge sampling, single-sided leading-edge sampling and double-sided sampling (refer to Fig. 7 later). We will denote the resultant PWM signals, respectively, as the trailing-edge PWM signal, the leading-edge PWM signal and the double-sided PWM signal.

The double-sided natural sampling process is used in the majority of commercial low-voltage Class-D amps [4], [5], [7], [14]. It is well established [9] that this PWM signal can be obtained by combining the trailing-edge and leading-edge PWM signals.

By means of the double Fourier series analysis [9] for the input modulating signal and the trailing-edge sawtooth carrier (represented by the line AA′) depicted in Fig. 3, the Fourier series of the trailing-edge PWM signal $F_T(t)$ is

$$\begin{aligned} F_T(t) = k + \frac{M}{2}\cos(\omega_s t) + \sum_{m=1}^{\infty}\left\{\frac{1}{m\pi}\sin(m\omega_c t)\right. \\ \left. - \frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t - 2m\pi k)\right\} - \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \\ \cdot \frac{J_n(m\pi M)}{m\pi}\sin\left(m\omega_c t + n\omega_s t - 2m\pi k - \frac{n\pi}{2}\right). \end{aligned} \tag{2}$$

The first term k represents the dc component of the PWM output and the second term represents the modulating signal. The third term represents the carrier and its associated harmonics. The last term represents the intermodulation products between the fundamental and harmonic components of the modulating signal, and the carrier.

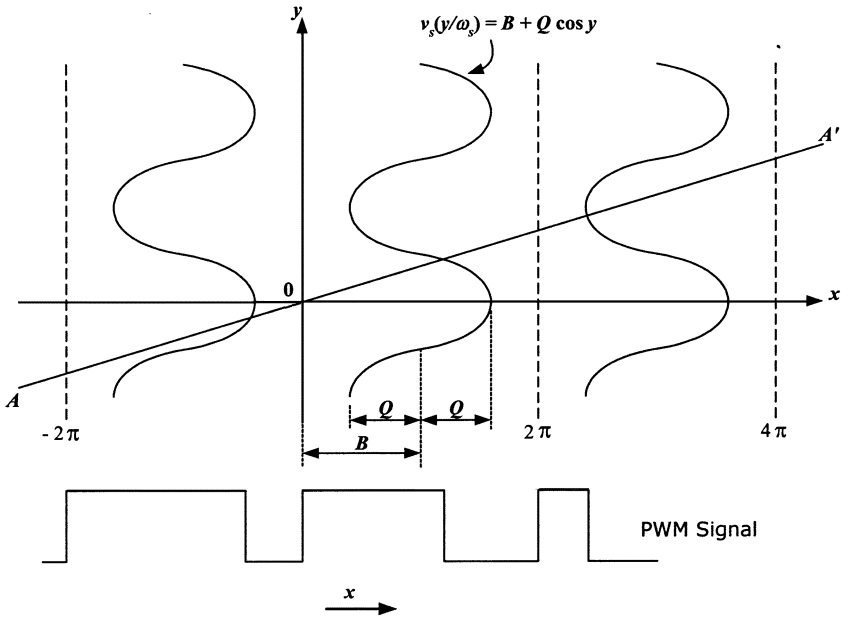

Fig. 3. A 2-D geometrical configuration of a single-sided PWM signal.

The Fourier series of the leading-edge PWM signal $F_L(t)$ [9] can be obtained by simply reversing the time scale of the trailing-edge PWM signal $F_T(t)$ as follows:

$$\begin{aligned} F_L(t) &= F_T(-t) \\ &= k + \frac{M}{2}\cos(\omega_s t) - \sum_{m=1}^{\infty}\left\{\frac{1}{m\pi}\sin(m\omega_c t)\right. \\ &\quad \left. + \frac{J_0(m\pi M)}{m\pi}\sin(m\omega_c t + 2m\pi k)\right\} + \sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty} \\ &\quad \cdot \frac{J_n(m\pi M)}{m\pi}\sin\left(m\omega_c t + n\omega_s t + 2m\pi k + \frac{n\pi}{2}\right). \end{aligned} \tag{3}$$

The terms in (3) can be similarly interpreted as above.

Consequently, the Fourier series of the double-sided PWM signal is

$$\begin{aligned} F_D(t) &= F_T(t) + F_L(t) \\ &= k + \frac{M}{2}\cos(\omega_s t) + 2\sum_{m=1}^{\infty}\frac{J_0\left(m\pi\frac{M}{2}\right)}{m\pi} \\ &\quad \cdot \cos m\omega_c t \sin(m\pi k) + 2\sum_{m=1}^{\infty}\sum_{n=\pm 1}^{\pm\infty}\frac{J_n\left(m\pi\frac{M}{2}\right)}{m\pi} \\ &\quad \cdot \cos(m\omega_c t + n\omega_s t)\sin\left(m\pi k + \frac{n\pi}{2}\right). \end{aligned} \tag{4}$$

We remark that as the trailing-edge and leading-edge sawtooth carriers intersect at half period to form a triangular carrier, the resultant amplitude of the triangular wave carrier is scaled by a factor of 0.5. Consequently, the modulation index M of the modulation signal for the trailing-edge and leading-edge carriers is also scaled by a factor of 0.5. The frequency of the triangular carrier, as expected, remains unchanged.

We make the following remarks on (4). The first term, the dc component, is usually of little consequence as it is eliminated by means of a bridge configured output stage. The third term (harmonics of the carrier) and the last terms (intermodulation products between the fundamental and harmonic components of the modulating signal and the carrier) are either negligible or effectively removed by the low-pass filter depicted in Fig. 1. Consequently, the double-sided modulated PWM output signal of an ideal Class-D amp will comprise only the second term in (4) where no harmonics of ω_s is present. To put it simply, the THD of the PWM generated from a triangular carrier is ideally zero since the THD of the PWM signal generated from the individual ideal trailing-edge sawtooth carrier and ideal leading-edge sawtooth carrier is zero.

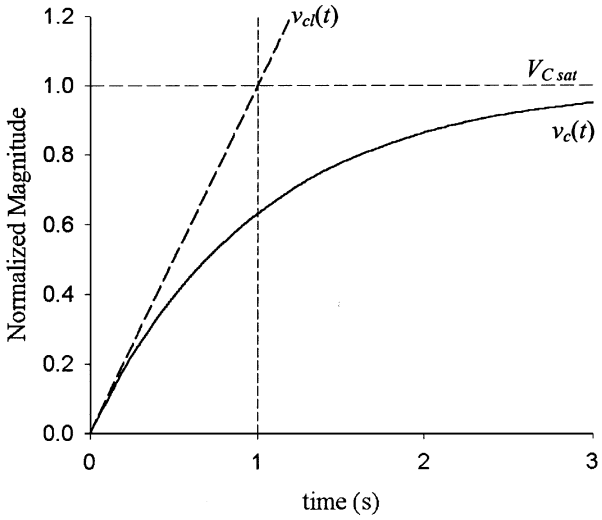

Fig. 4. Exponential carrier $v_c(t)$ and its derivative $v_{cl}(t)$ at the origin.

B. The Effect of Carrier Nonlinearity on THD

1) Derivation of Fourier Coefficients of the Double-Sided PWM Employing an Exponential Carrier: In practice, in particular low-voltage PWMs, the ideal triangular carrier is usually replaced by an exponential carrier which is generated by charging and discharging a simple *RC* integrator circuit with square pulses [4]–[7], [14]. The rising edge of the exponential carrier $v_c(t)$ is shown in Fig. 4 and an example of a popular

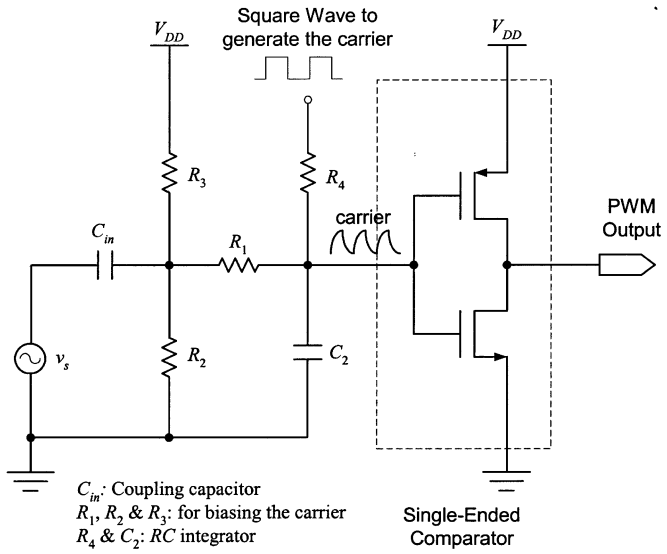

Fig. 5. PWM Circuit embodying the *RC* integrator for generating the exponential carrier.

simple PWM circuit employing an *RC* integrator is depicted in Fig. 5. This simple design is employed primarily for low-power, low-voltage, small IC area and noise considerations. However, the circuit simplicity advantage is realized at the expense of the carrier nonlinearity. We will now show by using the double Fourier series analysis that this nonlinearity results in harmonic distortion at the PWM output.

We first consider the trailing-edge PWM, and later the leading-edge PWM. As explained earlier, the double-edge PWM is simply a sum of the trailing-edge and leading-edge PWMs.

To model the nonlinearity of the trailing-edge exponential carrier and yet employ the double Fourier series analysis, we propose a novel mathematical methodology to shift the nonlinearity of the exponential carrier to the input modulating signal. Our proposed mathematical methodology involves three steps and is shown in Fig. 6. In step 1, we remove the nonlinearity of the trailing-edge exponential carrier in Fig. 6(a) by transforming the exponential carrier to a *linearized* exponential carrier (linear sawtooth carrier) in Fig. 6(b). In step 2, we account for the removal of the carrier nonlinearity by transforming the initially-linear modulating signal to a *transformed* (nonlinear) modulating signal, refer to Fig. 6(b) and (c). The *transformed* sinusoidal modulating signal is then normalized. We subsequently repeat steps 1 and 2 to the leading-edge PWM. In step 3, we derive the double Fourier coefficients of the double-sided PWM output by summing the Fourier coefficients of the trailing-edge and leading-edge PWM outputs. This is depicted in Fig. 7.

Step 1—Transformation of the Trailing-Edge Exponential Carrier $v_{c\text{-}t}(t)$ to "Linearized" Trailing-Edge Exponential Carrier $v_{cl\text{-}t}(t)$: We first express the trailing-edge exponential carrier $v_{c\text{-}t}(t)$ depicted in Fig. 6(a) as

$$v_{c\text{-}t}(t) = V_{C\,\mathrm{sat}}\left(1 - e^{-(t/t_0)}\right), \qquad 0 < t < T_c\left(=\frac{2\pi}{\omega_c}\right). \tag{5}$$

To model the trailing-edge exponential carrier, $v_{c\text{-}t}(t)$, as a *linearized* exponential carrier, $v_{cl\text{-}t}(t)$, we determine its gradient at $t = 0$ (refer to Fig. 4)

$$\left.\frac{dv_{c\text{-}t}(t)}{dt}\right|_{t=0} = \frac{V_{C\,\mathrm{sat}}}{t_0}. \tag{6}$$

Hence, the *linearized* trailing-edge exponential carrier is

$$v_{cl\text{-}t}(t) = \frac{V_{C\,\mathrm{sat}}}{t_0}\,t. \tag{7}$$

We now normalize these carriers to a maximum value of 2π. First, we find their maximum values for one period T_c

$$v_{c\text{-}t}(t)\big|_{\max,\,t=T_c} = V_{C\ \mathrm{sat}}\left(1 - e^{-(T_c/t_0)}\right) \tag{8}$$

$$v_{cl\text{-}t}(t)\big|_{\max,\,t=T_c} = \frac{V_{C\,\mathrm{sat}}}{t_0}\,T_c \tag{9}$$

$$\text{where } v_{cl\text{-}t}(t) \text{ ranges from } 0 \text{ to } \frac{V_{C\ \mathrm{sat}}}{t_o}\,T_c.$$

Subsequently, using the maximum value in (9), we normalize both carriers by applying a scaling factor of

$$\frac{2\pi t_0}{V_{C\,\mathrm{sat}}T_c} = \frac{\omega_c t_0}{V_{C\,\mathrm{sat}}} = \frac{x_0}{V_{C\,\mathrm{sat}}} \tag{10}$$

and obtain

$$v_{c\text{-}t}(t) = \omega_c t_0\left(1 - e^{-(t/t_0)}\right), \qquad 0 \le t \le T_c,$$
$$0 \le v_{c\text{-}t} \le \omega_c t_0\left(1 - e^{-(T_c/t_0)}\right) \tag{11}$$

$$v_{cl\text{-}t}(t) = \omega_c t, \qquad 0 \le t \le T_c,\ 0 \le v_{cl\text{-}t} \le 2\pi. \tag{12}$$

At this juncture, we have now removed the nonlinear component in the original nonlinear trailing-edge exponential carrier $v_{c\text{-}t}(t)$, resulting in a *linearized* trailing-edge exponential carrier $v_{cl\text{-}t}(t)$ as depicted in Fig. 6(a) and (b), respectively. Note that $v_{cl\text{-}t}(t)$ is now a sawtooth waveform. We shall now account for the nonlinearity of the trailing-edge exponential carrier by shifting it to the modulating signal in the next step.

Step 2—Transformation of the Sinusoidal Modulating Signal, $v_{s\text{-}t}(t)$, to the Transformed (Nonlinear) Modulating Signal, $v_{st\text{-}t}(t)$: In (1), the time dependency term of the sinusoidal signal can be removed and the sinusoidal modulating signal $v_{s\text{-}t}(t)$ for the trailing-edge exponential carrier can be re-expressed in x–y domain (refer to [9, p. 267] and Fig. 3) as

$$v_{s\text{-}t}\left(\frac{y_t}{\omega_s}\right) = B + Q\cos y_t \tag{13}$$
$$\text{where } 0 \le v_s(y_t/\omega_s) \le 2\pi.$$

From the exponential carrier range given in (11), we set the parameters B and Q as follows:

$$B = \omega_c t_0\left(1 - e^{-(T_c/t_0)}\right)\frac{k}{2}$$
$$= v_{c\text{-}pp}\,\frac{k}{2} \tag{14a}$$

$$Q = \frac{M}{2}\,\frac{\omega_c t_0}{2}\left(1 - e^{-(T_c/t_0)}\right)$$
$$= \frac{M}{4}\,v_{c\text{-}pp}. \tag{14b}$$

Note that for the same reason given in Section II-A earlier, we have scaled the modulating signal for the trailing-edge PWM by 0.5.

For analysis using the double Fourier series, the one-dimensional (1–D) trailing-edge PWM process in the time domain is

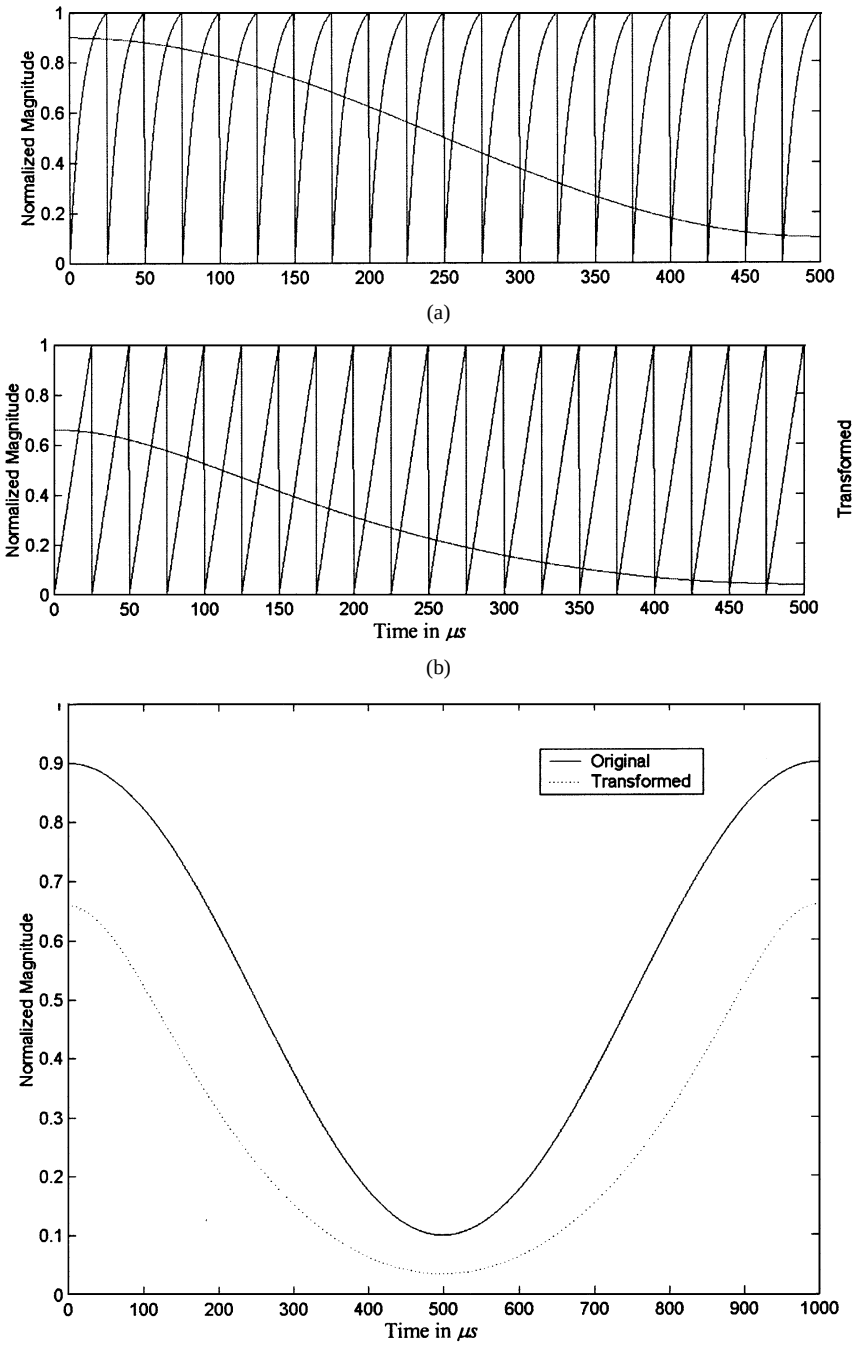

Fig. 6. (a) Original modulating signal $v_{s\text{-}t}(t)$ and the trailing-edge exponential carrier $v_{c\text{-}t}(t)$ at $M = 0.8$ and $x_0 = 0.7$ [refer to (10)]. (b)*Transformed* (nonlinear) modulating signal $v_{st\text{-}t}(t)$ and the *linearized* carrier $v_{cl\text{-}t}(t)$.(c) Original modulating signal $v_{s\text{-}t}(t)$ and the *transformed* (nonlinear) modulating signal $v_{st\text{-}t}(t)$.

transformed to a two-dimensional (2-D) x–y domain such that the x axis and y axis correspond to the carrier and modulating signal, respectively [9], that is

$$\begin{aligned} x_t &= \omega_c t \\ y_t &= \omega_s t. \end{aligned} \tag{15}$$

To derive the *transformed* modulating signal $v_{st\text{-}t}(y_t/\omega_s)$, for the trailing-edge PWM, we employ a two-y coordinate system, namely, y_t for the modulating signal and y_t' for the exponential and *linearized* carriers.

The normalized trailing-edge exponential carrier in (11) can subsequently be expressed as a function of y_t'

$$v_{c\text{-}t}\left(\frac{y_t'}{\omega_s}\right) = x_0\left(1 - e^{-(y_t'/y_0)}\right) \tag{16}$$

where the normalized maximum value of the carrier is $x_0 = \omega_c t_0$, and $y_0 = \omega_s t_0$ is a time constant along the y axis. Note that the extent of the nonlinearity of the exponential carrier depends on x_0.

Since the trailing-edge exponential carrier $v_{c\text{-}t}(y_t'/\omega_s)$ intersects the sinusoidal modulating signal $v_{s\text{-}t}(y_t/\omega_s)$ at the sam-

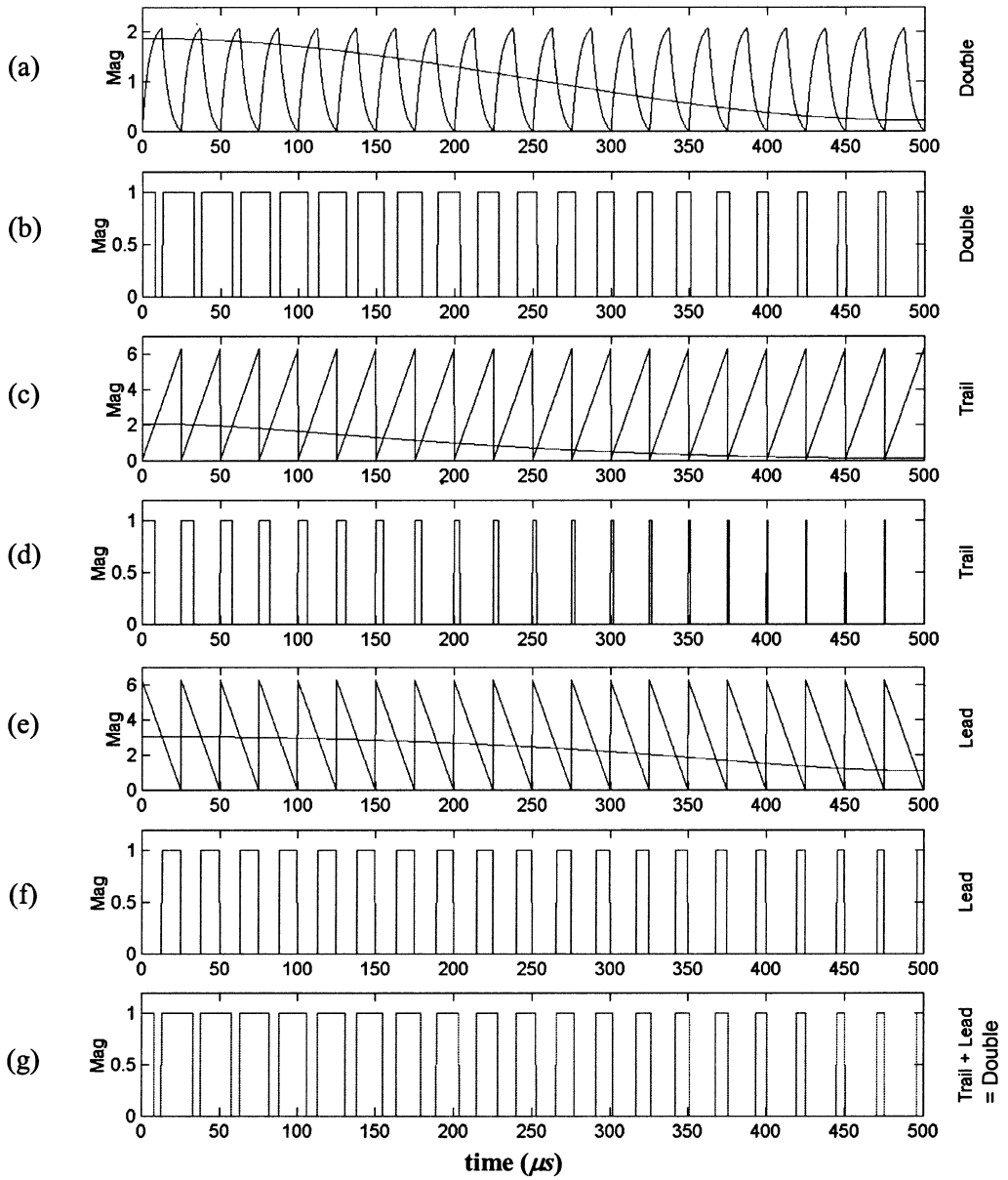

Fig. 7. (a) Double-sided exponential carrier and sinusoidal modulating signal. (b) Resultant PWM signal from the double-sided exponential carrier and the sinusoidal modulating signal. (c) *Linearized* trailing-edge exponential carrier $v_{cl\text{-}t}(t)$ and the *transformed* modulating signal $v_{st\text{-}t}(t)$. (d) Resultant PWM signal from the *linearized* trailing-edge exponential carrier $v_{cl\text{-}t}(t)$ and the *transformed* modulating signal $v_{st\text{-}t}(t)$. (e) *Linearized* leading-edge exponential carrier $v_{cl\text{-}l}(t)$ and the *transformed* modulating signal $v_{st\text{-}l}(t)$. (f) Resultant PWM signal from the *linearized* leading-edge exponential carrier $v_{cl\text{-}l}(t)$ and the *transformed* modulating signal $v_{st\text{-}l}(t)$. (g) Sum of trailing-edge and leading-edge modulated PWM signals in (d) and (f), and is identical to (b).

pling points, we can obtain an expression for y_t' by equating (13) and (16)

$$B + Q\cos(y_t) = x_0\left(1 - e^{-(y_t'/y_0)}\right)$$
$$y_t' = y_0 \ln\left(\frac{x_0}{x_0 - B}\right) + y_0 \ln\left(\frac{1}{1 - \alpha\cos(y_t)}\right) \tag{17}$$

where

$$0 \le \alpha\left(=\frac{Q}{x_0 - B}\right) < 1.$$

Similarly, since the *linearized* trailing-edge exponential carrier $v_{cl\text{-}t}(y_t'/\omega_s)$ intersects the *transformed* modulating signal $v_{st\text{-}t}(y_t/\omega_s)$ at the same sampling points, the *transformed* modulating signal for the trailing-edge modulated PWMs is

$$v_{st\text{-}t}\left(\frac{y_t}{\omega_s}\right) = v_{cl\text{-}t}\left(\frac{y_t'}{\omega_s}\right)$$
$$= \frac{\omega_c}{\omega_s} y_0 \left[\ln\left(\frac{x_0}{x_0 - B}\right) + \ln\left(\frac{1}{1 - \alpha\cos(y_t)}\right)\right]$$
$$= x_0 \ln\left(\frac{x_0}{x_0 - B}\right) + x_0 \ln\left(\frac{1}{1 - \alpha\cos(y_t)}\right) \tag{18}$$

where $0 \le \alpha\left(=\dfrac{Q}{x_0 - B}\right) < 1$ as before.

From (18), we note that the transformed modulating signal $v_{st\text{-}t}(y_t/\omega_s)$ depends on the values of B and Q of the sinusoidal

modulating signal and on the values of t_0 and x_0 of the carrier signal, refer to Figs. 3 and 4. We also note that the sinusoidal modulating signal comprising a dc component and a sinusoidal term has been transformed into an expression in logarithmic form without an expression for the dc component. However, the dc component of the transformed signal can be obtained by integrating the signal over a complete time period.

We have explained earlier that the double-sided PWM signal is obtained by summing the trailing-edge and leading-edge PWM signals. The *transformed* modulating signal for the trailing-edge exponential carrier, $v_{st\text{-}t}(y_t/\omega_s)$, was given in (18) earlier. By using the same steps (refer to the Appendix), we derive the *transformed* modulating signal for the leading-edge exponential carrier, $v_{st\text{-}l}(y_l/\omega_s)$, as

$$v_{st\text{-}l}\left(\frac{y_l}{\omega_s}\right) = v_{cl\text{-}l}\left(\frac{y_l'}{\omega_s}\right) = 2\pi + x_0 \ln\left(e^{-(T_c/t_0)} + \frac{B + Q\cos(y_l)}{x_0}\right). \tag{19}$$

At this juncture, we have now accounted for the nonlinearity in the trailing-edge and leading-edge exponential carriers $v_{c\text{-}t}(t)$ and $v_{c\text{-}l}(t)$, (thereby making these carriers linear) by making their respective sinusoidal modulating signals, $v_{s\text{-}t}(t)$ and $v_{s\text{-}l}(t)$, nonlinear.

Step 3—Compute the Double Fourier Series Coefficients of the PWM Output: By using (18) and (19), we derive the double Fourier series coefficients K_{mn} for a PWM signal resulting from a sinusoidal modulating signal and a double-sided exponential carrier depicted in Fig. 7 as

$$\begin{aligned} K_{mn} &= \frac{1}{4\pi^2}\int_{y_{t1}=0}^{y_{t2}=2\pi}\int_{x_1}^{x_2}\left(v_{st\text{-}t}\left(\frac{y_t}{\omega_s}\right)e^{-j(mx+ny_t)}\right)dx\,dy_t \\ &\quad + \frac{1}{4\pi^2}\int_{y_{l1}=0}^{y_{l2}=2\pi}\int_{x_1}^{x_2}\left(v_{st\text{-}l}\left(\frac{y_l}{\omega_s}\right)e^{-j(mx+ny_1)}\right)dx\,dy_l \\ &= \frac{1}{4\pi^2}\int_{y_{t1}=0}^{y_{t2}=2\pi}\int_{x_1}^{x_2}\left\{\left[x_0\ln\left(\frac{x_0}{x_0-B}\right) + x_0\ln\left(\frac{1}{1-\alpha\cos(y_t)}\right)\right]e^{-j(mx+ny_t)}\right\}dx\,dy_t \\ &\quad + \frac{1}{4\pi^2}\int_{y_{l1}=0}^{y_{l2}=2\pi}\int_{x_1}^{x_2} \cdot\left\{\left[2\pi + x_0\ln\left(e^{-(T_c/t_0)} + \frac{B+Q\cos(y_l)}{x_0}\right)\right] \cdot e^{-j(mx+ny_l)}\right\}dx\,dy_l. \end{aligned} \tag{20}$$

We described earlier that the THD of an ideal PWM is zero. Since the *linearized* exponential carrier in (20) is ideal, the THD of the PWM signal due to the nonlinearities of the *transformed* modulating signal is simply equivalent to the THD of the *transformed* modulating signal.

To obtain the Fourier coefficients of the *transformed* modulating signal, we set $m = 0$ in (20), that is, we remove the carrier component and its harmonics, and the intermodulation terms between the carrier and the modulating signal. Hence, we finally express the Fourier coefficients of the *transformed* modulating signal, that is, the Fourier coefficients of the PWM signal obtained from a sinusoidal modulating signal and the double-sided exponential carrier as

$$\begin{aligned} K_{0n} &= \frac{1}{4\pi^2}\int_{y_{t1}=0}^{y_{t2}=2\pi}\left\{\left[x_0\ln\left(\frac{x_0}{x_0-B}\right) + x_0\ln\left(\frac{1}{1-\alpha\cos(y_t)}\right)\right]e^{-jny_t}\right\}dy_t \\ &\quad + \frac{1}{4\pi^2}\int_{y_{l1}=0}^{y_{l2}=2\pi}\left\{\left[2\pi + x_o\ln\left(e^{-(T_c/t_0)} + \frac{B+Q\cos(y_l)}{x_0}\right)\right]e^{-jny_l}\right\}dy_l \qquad n \in \text{Integer} \\ &= \left[\frac{x_0}{4\pi^2}\ln\left(\frac{x_0}{x_0-B}\right) + \frac{1}{2\pi}\right]\int_{y_1=0}^{y_2=2\pi} e^{-jny}\,dy \\ &\quad + \int_{y_l=0}^{y_2=2\pi}\left[\ln\left(\frac{1}{1-\alpha\cos(y)}\right) + \ln\left(e^{-(T_c/t_0)} + \frac{B+Q\cos(y)}{x_0}\right)\right]e^{-jny}\,dy \end{aligned} \tag{21}$$

where $\displaystyle\int_{y_1=0}^{y_2=2\pi} e^{-jny}\,dy = \begin{cases} 0, & \forall n \neq 0 \\ 2\pi, & n = 0. \end{cases}$

We interpret (21) as follows. The first term is a dc component and the second term comprises the fundamental and harmonic components of the modulating signal. We note that the harmonics of input modulating signal are nonzero, thereby resulting in nonzero THD. We further note that the parameter x_0, which determines the nonlinearity of the carrier, shows that the harmonic distortion increases with the degree of nonlinearity of the exponential carrier; this observation is somewhat noted intuitively. This parameter x_0 and (21) is of particular interest to PWM designers as it provides an insight to the degree of THD distortion as a consequence of the nonlinearity of the carrier. We will later describe in Section III, a range of x_0 appropriate for a practical design. It is worthwhile to note that x_0 affects the dynamic range of the PWM and we will also discuss this in Section III later.

C. Effect of Output Stage On Resistance on THD

We shall now investigate the second parameter that may affect the THD: the on resistance of the final CMOS inverters at the output stage [1]. The primary reason why the Class-D amp is more power efficient than classical linear amplifiers is because its output PWM signal is essentially digital or switch mode. The MOS transistors of the inverters in the Class-D output stage dissipate very little power in the ohmic region when they are turned on. However, this on resistance is not negligible [1], [10] if the impedance of the load is relatively low, as in the case of hearing instruments (typically $\leq$600 Ω). This will result in a slightly "amplitude modulated" signal at the PWM output as shown in a PWM signal obtained experimentally in Fig. 2. This amplitude modulation becomes more pronounced at higher modulation indexes.

To investigate the effect of on resistance (with all other parameters assumed to be ideal) on THD, we model the output stage to a first-order approximation as a simple output source resistance, R_{on}, as that depicted in Fig. 8. We remark that this

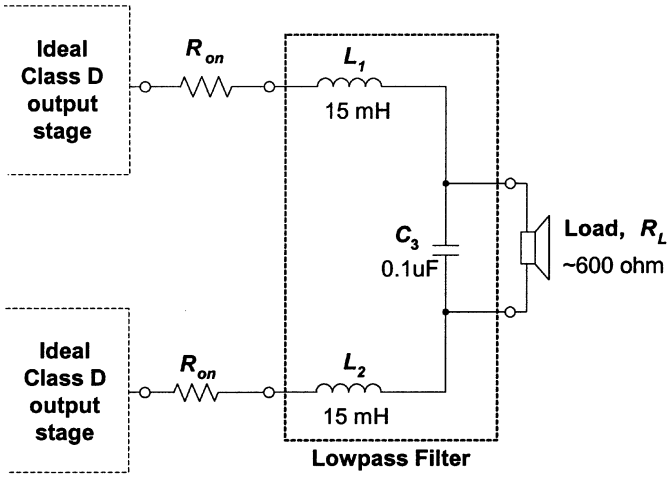

Fig. 8. Circuit model for simulating on resistance.

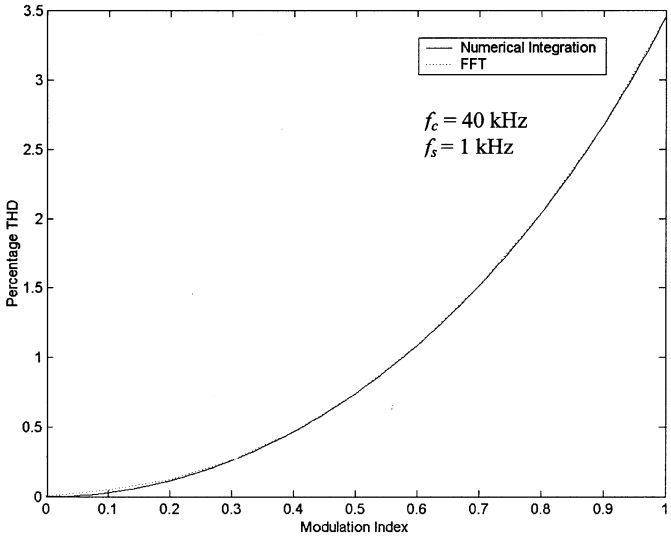

Fig. 9. Comparison of THD based on numerical integration and FFT.

model is true when the MOS transistors are operating in the ohmic region and where the drain-to-source voltage is small (<0.4 V). This model will be used in our MATLAB simulations. In HSPICE simulations, we will use practical output stage designs and we shall compare these MATLAB and HSPICE simulations with measurements on prototype ICs.

III. Simulation and Measurement Results

We will first verify our theoretical derivations of the Fourier coefficients in (21). We do this by comparing the THD obtained from (21) using numerical integration [15] in MATLAB with that obtained by performing a 1024-point fast Fourier transform (FFT) (also in MATLAB) on the PWM signal obtained from the original sinusoidal input modulating signal and the double-sided exponential carrier. Fig. 9 depicts the THD obtained from these two methods for $x_0 = 1.5\ \pi$ over the full-modulation index range. As the THDs agree well, our derivation of (21) is hence verified. We further remark from Fig. 9 that the THD increases when the modulation index increases. This is expected because when the modulation index is small, the part of the carrier that

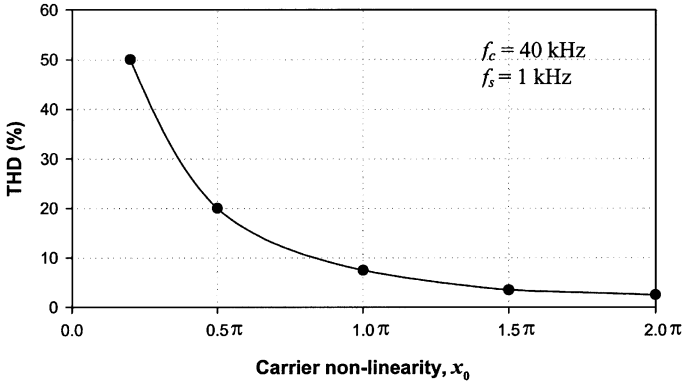

Fig. 10. THD based on MATLAB simulations [(21)] at modulation index $M = 0.99$ (or near full signal swing) with carrier nonlinearity ranging from $x_0 = 0.2\ \pi$ to $2\ \pi$.

is used to compare against the modulation signal to generate the PWM output is quasilinear. To put it differently, the greater the nonlinearity of the carrier during the process of comparing with the modulating signal to generate a PWM signal, the greater the deviation of the resulting pulses from ideal. This deviation results in harmonic distortion.

Using the theoretical Fourier series coefficient derivation in (21), we summarize in Fig. 10 the THD (at $M = 0.99$) as a function of x_0, the degree of nonlinearity of the carrier. We note here that, as expected, the THD increases with the nonlinearity of the carrier, i.e., with decreasing x_0. From this study, we recommend a range of 1.5 π to 2.0 π for x_0. Note that the maximum value of x_0 cannot be arbitrarily chosen because a large x_0 will reduce the maximum allowable input modulating signal range. This is the case because for a given carrier frequency, the more linear the exponential carrier, the lower is its peak-to-peak signal swing. This would in turn reduce the dynamic range of PWM. The maximum signal range of the input modulating signal for $x_0 = 1.5\ \pi$ to 2.0 π is approximately $(1/3)V_{DD}$, and results in acceptable signal swing in practical realizations. In hearing instruments and other low-voltage electronic instruments, the dynamic range is usually limited and needs to be preserved where possible. It is worthwhile to remark that we obtain the same results in Fig. 10 if we determine the THD by performing an FFT on the PWM signal output obtained from the original sinusoidal input modulating signal and the double-sided exponential carrier.

We summarize in Fig. 11 the THD obtained from MATLAB [(21)], HSPICE simulations and practical measurements for different modulation indexes for two carrier nonlinearities, $x_0 = 0.5\ \pi$ and $x_0 = 1.5\ \pi$. The HSPICE simulations are simulations of the practical circuit depicted in Fig. 5. The measurements, on the other hand, are based on circuits constructed from off-the-shelf devices connected to a prototype IC (Fig. 12) embodying Class-D output stages. We note from Fig. 11 that the THD determined from (21), HSPICE and measurements agree well, thereby verifying our analytical expressions in Section II-B earlier. Based on this study, we recommend that x_0 be chosen to be between 1.5 π and 2.0 π, and this range is consistent with our earlier recommendation. We further note, as before, that the THD increases when the modulation index increases.

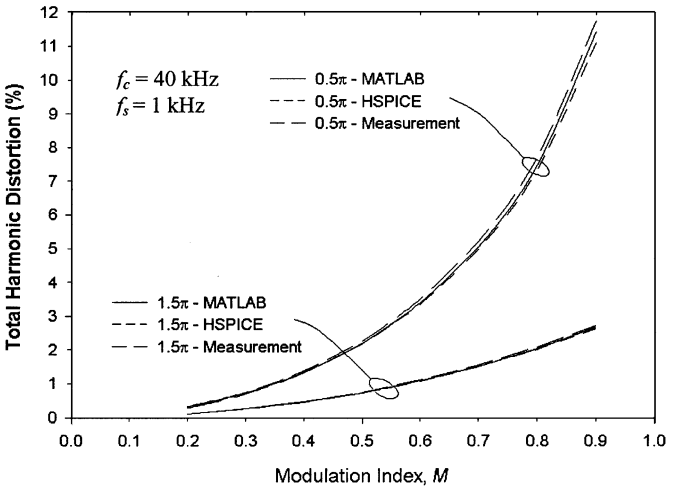

Fig. 11. Comparison of THD between MATLAB simulations [(21)], HSPICE simulations and measurements on prototype ICs for $x_0 = 0.5\pi$ and $x_0 = 1.5\pi$.

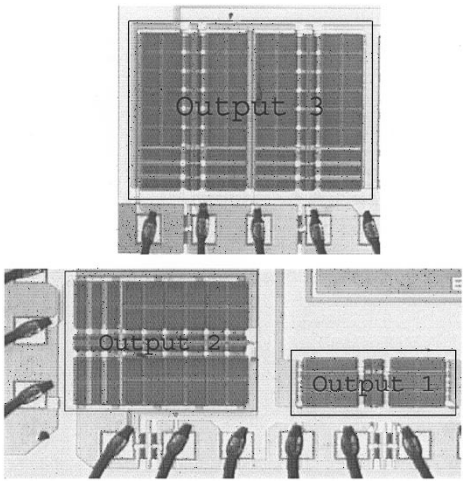

Fig. 12. Microphotographs of the 3 Class-D output stages: $R_{on}(\text{Output } 1) = 17\ \Omega$, $R_{on}(\text{Output } 2) = 5.3\ \Omega$ and $R_{on}(\text{Output } 3) = 2.9\ \Omega$.

TABLE I
W/L RATIO AND ON-RESISTANCE OF THE CLASS D OUTPUT STAGE pMOS TRANSISTORS ($W_n = W_p/2.77$) IN FIG. 12

	W_p/L		
	2997 μm/1.2 μm	9558 μm/1.2 μm	17873 μm/1.2 μm
R_{on}	17 Ω	5.3 Ω	2.9 Ω

We designed a prototype IC embodying three different Class-D amp output stages depicted in Fig. 12 whose W/L ratios of the final inverter transistors (or equivalent on resistance) are different as tabulated in Table I.

Fig. 13 depicts the THD for the three different output stages based on MATLAB, HSPICE simulations and on the basis of measurements on prototype ICs for two modulation indexes, $M = 0.5$ and $M = 0.8$. A linear triangular carrier is used and the MATLAB results are based on a 1024-point FFT analysis of the PWM signal.

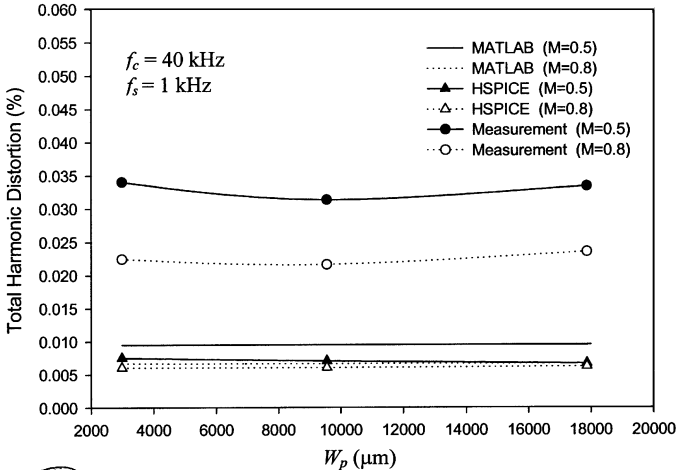

Fig. 13. Comparison of THD between MATLAB simulations, HSPICE simulations and measurements on prototype ICs for different output on resistances.

We note that the THD is small in all cases. The measured THD are somewhat larger than the simulated values and this is probably due to the nonperfect triangular carrier and other practical nonlinearities. Of particular interest, we note that the different on resistance have little effect on THD as predicted by our simple model in Section II-C. Nevertheless, it is probably worthwhile noting that the output PWM for a high output resistance (relative to the load) is slightly amplitude modulated. This modulation has little, if any, effect on THD. However, the maximum signal output is slightly reduced, and the reduction is less than 5% for the worst case condition of $R_{on} = 17\ \Omega$ in this experiment.

IV. CONCLUSION

We have investigated the effect of the nonlinearity of the carrier in the PWM circuit and the effect of on resistance of the output stage on THD. By means of a novel mathematical analysis method, we have shown that the nonlinearity of the carrier should be small to achieve a low THD. We have shown that the on resistance of the output stage has little effect on THD. Our analyzes have been verified by computer simulations and on the basis of experimental measurements.

APPENDIX

Step 1—Transformation of the Leading-Edge Exponential Carrier $v_{c\text{-}l}(t)$ to the "Linearized" Leading-Edge Exponential Carrier $v_{cl\text{-}l}(t)$: The leading-edge exponential carrier $v_{c-l}(t)$ can be expressed as

$$v_{c\text{-}l}(t) = V_{C\,\text{sat}}\left(e^{-(t/t_0)} - e^{-(T_c/t_0)}\right) \qquad 0 < t < T_c\left(=\frac{2\pi}{\omega_c}\right) \tag{A.1}$$

and the *linearized* leading-edge exponential carriers (for one period) is

$$v_{cl\text{-}l}(t) = -\frac{V_{C\,\text{sat}}}{t_0}(t - T_c) \tag{A.2}$$

where $v_{cl\text{-}l}(t)\big|_{t=0} = \dfrac{V_{C\,\text{sat}}}{t_0}T_c$.

After applying a scaling factor of $\omega_c t_0/V_{C\,\mathrm{sat}} = x_0/V_{C\,\mathrm{sat}}$, the respective normalized expressions for the leading-edge exponential carrier and the *linearized* leading-edge exponential carrier are

$$v_{c\text{-}l}(t) = \omega_c t_0 \left(e^{-(t/t_0)} - e^{-(T_c/t_0)}\right), \qquad 0 \le t \le T_c,$$
$$0 \le v_{c\text{-}l} \le \omega_c t_0 \left(1 - e^{-(T_c/t_0)}\right) \tag{A.3}$$
$$v_{cl\text{-}l}(t) = -\omega_c(t - T_c), \qquad 0 \le t \le T_c,\ 0 \le v_{cl\text{-}l} \le 2\pi. \tag{A.4}$$

Step 2—Transformation of the Sinusoidal Modulating Signal, $v_{s\text{-}l}$, to the Transformed Modulating Signal, $v_{st\text{-}l}$: The 1-D leading-edge PWM process in time domain is transformed to a 2-D x–y domain

$$x_l = -\omega_c(t - T_c)$$
$$y_l = \omega_s(t - T_c). \tag{A.5}$$

The normalized leading-edge exponential carrier expressed as a function of y_l' is

$$v_{c\text{-}l}\left(\frac{y_l'}{\omega_s}\right) = x_0 e^{-(T_c/t_0)}\left(e^{y_l'/y_0} - 1\right). \tag{A.6}$$

Since the leading-edge exponential carrier $v_{c\text{-}l}(y_l'/\omega_s)$ intersects the sinusoidal modulating signal $v_{s\text{-}l}(y_l/\omega_s)$

$$B + Q\cos(y_l) = x_0 e^{-(T_c/t_0)}\left(e^{-(y_l'/y_0)} - 1\right)$$
$$y_l' = -\omega_s T_c - y_0 \ln\left(e^{-(T_c/t_0)} + \frac{B + Q\cos(y_l)}{x_0}\right) \tag{A.7}$$

where $0 \le \alpha\left(=\dfrac{Q}{x_0 - B}\right) \le 1$.

Since the *linearized* leading-edge exponential carrier $v_{cl\text{-}l}(y_l'/\omega_s)$ intersects the *transformed* modulating signal $v_{st\text{-}l}(y_l'/\omega_s)$ at the sampling points as the leading-edge exponential carrier and the original modulating signal, the *transformed* modulating signal for the leading-edge modulated PWMs is

$$v_{st\text{-}l}\left(\frac{y_l}{\omega_s}\right) = v_{cl\text{-}l}\left(\frac{y_l'}{\omega_s}\right)$$
$$= 2\pi + x_0 \ln\left(e^{-(T_c/t_0)} + \frac{B + Q\cos(y_l)}{x_0}\right). \tag{A.8}$$

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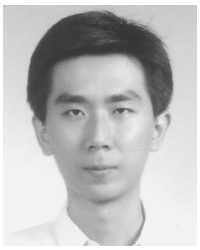

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