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ADVANCED DC-DC POWER CONVERSION TOPOLOGIES AND MATHEMATICAL ANALYTICAL METHODS

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Summary

In modern technology, power conversion equipment is very important and is now used in a great variety of products. The corresponding equipment can be divided into four groups, ac-ac converters, ac-dc rectifiers, dc-dc converters, dc-ac inverters. From recent reports, the production of dc-dc converters occupies the largest percentage of the total turnover of all conversion equipment production. However, in the traditional dc-dc converters (buck, boost, Cûk, SEPIC…), the effect of parasitic elements comes into picture at high duty ratio D, so the practical value of D has an upper limit. It is difficult to operate at higher duty ratios and hence to achieve high voltage transfer gains in those traditional dc-dc converters. With the fast development of technologies, this disadvantage limits the further applications of those traditional converters in some areas that require higher voltage transfer gains such as in communication equipment, aerospace electronics, portable devices and IC chips. Therefore, an in-depth research on advanced dc-dc power conversion topologies whose voltage transfer gains are higher than traditional dc-dc converters has been firstly performed in this thesis.

Voltage lift technique is an effective method that is widely applied in electronic circuit design, especially in the radio engineering. It also can be utilized to improve the performance and characteristics of dc-dc converters. This thesis introduces a set of positive output dc-dc converters (voltage-lift type SEPIC converters) applying series SEPIC implementing voltage lift techniques. Compared with the prototype of the SEPIC converter, these converters can perform positive to positive dc-dc voltage increasing conversion with higher positive voltage transfer gains. Additionally, this thesis also introduces a set of negative output dc-dc converters (voltage-lift type Cûk converters) applying series Cûk implementing voltage lift techniques. Compared with the Cûk converter prototype, these converters can perform positive-to-negative dc-dc voltage increasing conversion with higher negative voltage transfer gains. These two sets of advanced dc-dc conversion topologies are different from other existing dc-dc step-up converters and possess obvious advantages, mainly including fewer switches, clearer conversion processes and a higher output voltage with the small ripple. Since the proposed converters avoid using transformers and cascade connection, relative simple

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structures are beneficial to potential practical applications in future. They can be further improved in structures to obtain better output performance by the enhanced circuits (EC). A detailed theoretical analysis for the continuous conduction mode (CCM) and discontinuous conduction mode (DCM) is given, from which general principles and special performance phenomena have been discussed.

On the basis of foregoing research, a set of advanced mirror-symmetrical double-output transformerless dc-dc converters have also been proposed, which can convert the positive input source voltage to positive and negative output voltages by two conversion paths. Single switch structure is adopted in the proposed mirror-symmetrical double-output transformerless dc-dc converters, and the cost can be significantly decreased. Two different series of ECs, boost and super enhanced series, have been developed to further increase the voltage transfer gains. Furthermore, the general guidelines of positive output dc-dc topology construction using a series of output enhanced circuits are proposed.

The mathematical analytical method of dc-dc converters is a historical problem that has accompanied dc-dc power conversion technology since the 1940s. Traditional mathematical analytical methods are not available for complex structure converters because of the high-order differential equations involved. Therefore, in the thesis a developed graphical modelling method has been presented to cover all complex dc-dc converters. The high-order complex converters are taken as examples, and a thorough analysis is given with consideration of effects caused by parasitic parameters and diodes' forward voltage drop. The general guidelines of constructing and deriving graphical models are provided, from which it is seen that the classical graph reduction techniques and Mason rules are utilized to analyze the graphical models and perform the system calculation. Mason rules need the tedious searching for the different forward paths and loops in the flow graph, and graph reduction method requires a complicated node-movement transformation process. So a new method is presented to enrich the graphical mathematical modeling theory in this thesis, which is termed averaging binary tree structure representation. The proposed method, based on the switching signal flow graph (SSFG) models, describes the converters as a binary tree structure. The general construction principles of the binary tree for the complex flow graph system are summarized and developed. The proposed method has been applied to the analysis for 2nd

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order dc-dc converters, which shows the advantages of high convenience and practicability compared with the conventional flow graph analytical methods. Simulation and experimental observations are provided to validate the proposed algorithm.

Furthermore, to reduce the complexity of graphical analytical methods, new mathematical methods from the view of the system energy characteristics of dc-dc converters has been proposed. When the converter changes from one steady state to another, the corresponding stored energy changes. So does a dc-dc converter behave because it has several energy storing components. Therefore, there must be a transient process from one steady state to the new steady state. The thesis has theoretically defined a new concept, namely energy factor (EF), and researched the relationship between it and mathematical modeling for multi-state dc-dc converters. Various operation conditions have been analyzed to demonstrate the application of EF, pumping energy (PE), stored energy (SE), capacitor/inductor stored energy ratio (CIR), energy losses (EL), time constant τ and damping time constant τ_d. The EF and its associated parameters illustrate the unit-step response and interference recovery that may be helpful for system design and anticipating dc-dc converter characteristics.

Based on the system energy characteristics, a new explanation of DCM has also been proposed to enrich the knowledge of power electronics principles, and it can unify all complex discontinuous inductor currents phenomena existing in the complex dc-dc converters.

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List of Abbreviations

CCM	continuous conduction mode
CIR	capacitor/inductor stored energy ratio
DCM	Discontinuous Conduction Mode
DEC	double/enhanced circuit
EC	enhanced circuit
EF	energy factor
EL	energy losses
FACTS	flexible ac transmission systems
GTO	gate-turn-off thyristor
HVDC	high-voltage dc
IGBT	insulated gate bipolar transistor
PE	pump energy
MOSFET	metal-oxide-semiconductor field-effect transistor
PF	power factor
PFC	power factor correction
PWM	pulse-width modulation
SC	switched-capacitor
SE	stored energy
SEPIC	single ended primary inductor converter
SFG	signal flow graph
SSFG	switching signal flow graph
THD	total harmonic distortion
VL	voltage lift

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List of Principle Symbols

C_n	n^{th} capacitor
CIR	capacitors/inductors stored energy variation ratio
D	duty ratio
EF	Energy factor
E_{loss}	energy losses variation
f	switching frequency
f_c	filter corner frequency
H_n	transmittance of the n^{th} branch
i_L	inductor current
I_R	remaining inductor current
k	switching branch during switching-on
$\overline{k}$	switching branch during switching-off
L_n	n^{th} inductor
m	current filling efficiency
m_S	current filling efficiency of the self-lift circuit
m_R	current filling efficiency of the re-lift circuit
M	voltage transfer gain
M_{DCM}	voltage transfer gain in DCM
MAX	function of selecting one with the maximum value
n_o	number of VL cells existing in the output section
n_p	number of VL cells existing in the pump section
P	power
PE	pumping energy variation
r_L	equivalent series resistance of inductor
R	output load
R_+	output load of the positive conversion path
R_-	output load of the negative conversion path
s	operator in s-domain
SE	stored energy variation

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$G(s)$	large-signal transfer function
$\hat{G}(s)$	small-signal transfer function
T	switching cycle
v_C	capacitor voltage
V_D	forward voltage of a diode
v_{in}	source voltage
$\hat{v}_{in}$	Perturbations of the source voltage
V_{in}	average source voltage
v_o	output load voltage
$\hat{v}_o$	perturbations of the output voltage
V_o	average output voltage
v_X	instantaneous voltage of the component X
$\hat{v}_X$	voltage perturbations
V_X	average voltage of the component X
WC	stored energy variation of capacitor
WL	stored energy variation of inductor
Z_N	normalized load
$Z_{N\text{-}B}$	boundary normalized load
Δi_X	peak-to-peak current variation of the component X
Δv_X	peak-to-peak voltage variation of the component X
δ	final switching angle
ξ	variation ratio of the inductor current of the diode current
ε	variation ratio of the output voltage
η	power efficiency
η_{crt}	critical value of the efficiency
ς	variation ratio of the inductor current
τ	time constant
τ_d	damping time constant

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Chapter 1 Introduction

1.1 DC-DC Converters in Power Electronics

Advanced power conversion technique is a major research area in the field of power electronics. The equipment for conversion techniques have important applications in modern technology and are now used in a great variety of products [1-10], including heat controls, light controls, motor controls, switch-mode power supplies, vehicle propulsion systems, flexible ac transmission systems (FACTS), power factor correction (PFC) and high-voltage dc (HVDC) systems. The power conversion equipment can be divided into four technologies:

- ac-ac transformers and converters
- ac-dc rectifiers
- dc-dc converters
- dc-ac inverters

A dc-dc converter is a power electronics system, which converts one level of electrical energy into another level of electrical energy at the load. The dc-dc conversion technique was established in the 1920s. The simplest dc-dc converter is a voltage divider (such as rheostat, potential–meter, and so on), but it only transfers output voltage lower than input voltage with poor efficiency. The multiple-quadrant chopper is the second step in dc-dc power conversion. Much time has been spent trying to find equipment to convert the dc energy source of one voltage to another dc actuator with another voltage, as does a transformer employed in ac-ac conversion. Some preliminary types of dc-dc converters were used in industrial applications before the Second World War. Research was blocked during the war, but applications of dc-dc converters were recognized. After the war, communication technology developed very rapidly and required low voltage dc power supplies. This resulted in the rapid development of dc-dc power conversion techniques, and several preliminary prototypes were derived from choppers. Switching dc-dc

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converters have been in existence since the 1950s. However, the unavailability of reliable and low-cost power transistors had limited their applications primarily to the military and space applications. The advances and availability of modern power semiconductor devices in the early 1970s have made the switching dc-dc converter a popular choice in power supplies and dc motor drive.

Switching dc-dc power conversion technology is therefore a major subject area in the field of modern power engineering and drives, and has been under development for six decades. Switching dc-dc converters are widely used in industrial applications and computer hardware circuits, and dc-dc conversion techniques have developed very quickly. Statistics show that the dc-dc converter worldwide market has grown from U.S. $3336 million in 1995 to U.S. $5128 million in the year 2004 with a compound annual growth rate (CAGR) of 9%. This compares to the ac-dc power supply market, which will have a CAGR of only about 7.5% during the same period. In addition to its higher growth rate, the dc-dc converter market is undergoing dramatic changes as a result of two major trends in the power electronics industry: low voltage and high power density. From this investigation, it can be seen that the production of dc-dc converters in the world market is much higher than that of dc-ac inverters.

According to incomplete statistics, there have been more than 500 prototypes of dc-dc converters developed in the past six decades. All existing dc-dc converters were designed to meet the requirements of certain applications. They are usually termed by their function, for example, Buck converter, Boost converter and Buck-Boost converter, and zero current switching (ZCS) and zero voltage switching (ZVS) converters.

1.2 Basic Topologies Review of Switching DC-DC Converters

A simple switching dc-dc converter consists of one active power switch (usually one GTO/MOSFET/IGBT), one passive power switch (diode), one inductor and one capacitor, as shown in Fig. 1-1. Since there are two energy storage elements, we usually term them 2^{nd} order dc-dc converters. The different arrangement of these storage elements and switches generates the different topology of switching dc-dc converters, such as the buck converter, the boost converter and the buck-boost converter.

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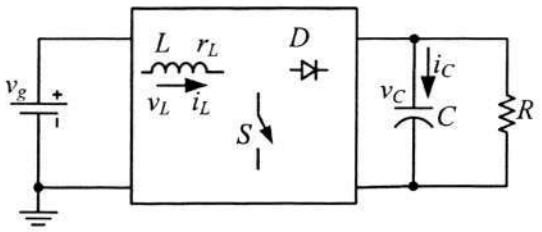

Fig. 1-1. The generalized representation of 2nd order dc-dc converters

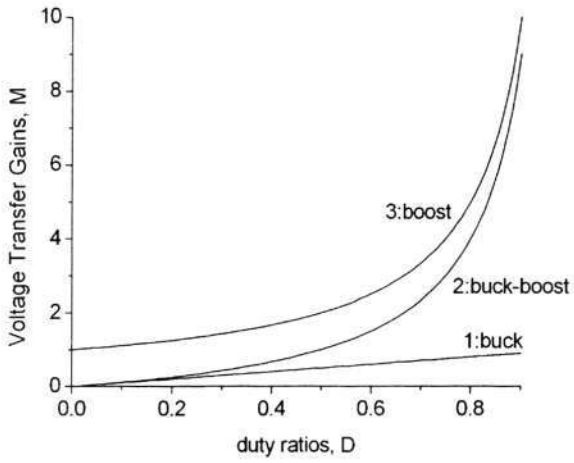

Fig. 1-2. Voltage transfer gains of 2nd order dc-dc converters

The principle merits of these 2nd order switching converters are their high conversion efficiency and high power density, which result in significant weight reduction. However, their voltage transfer gains are limited due to their simple structures. As shown in Fig. 1-2, the voltage transfer gain of the buck converter, M_{Buck} is equal to the duty ratio D, and it is a step-down converter. The buck-boost converter is a negative output converter, and the absolute value of the voltage transfer gain, $|M_{buck-boost}|$, is equal to $D/(1-D)$. The boost converter can provide a step-up function, and the voltage transfer gain M_{Boost} is equal to $1/(1-D)$.

The 4th order dc-dc converters can be considered as the development of simple 2nd order topologies. Each 4th order topology consists of one active power switch, one passive power switch, two inductors and two capacitors, as shown in Fig. 1-3. The different arrangement of these storage elements and switches generates the different topology of switching dc-dc converters. They are the buck converter with input filter, the SEPIC

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converter, the Cûk converter, the buck-boost converter with output filter and the boost converter with input filter, respectively.

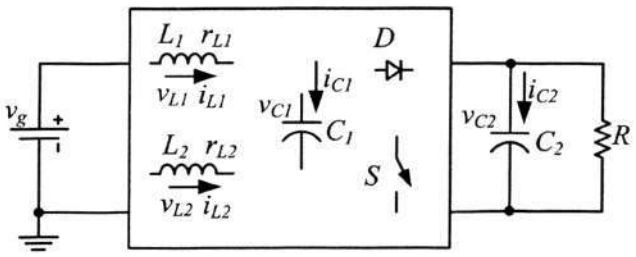

Fig. 1-3. The generalized representation of 4th order dc-dc converters

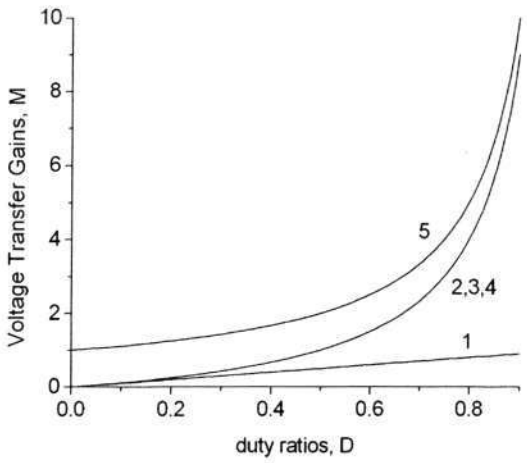

Fig. 1-4. Voltage transfer gains of 4th order dc-dc converters

(1: buck converter with input filter; 2: SEPIC converter; 3: Cûk converter; 4: Buck-boost converter with output filter; 5: Boost converter with input filter)

Applications of 4th order topologies has been fast developing in recent years; however, their voltage transfer gains are still not high, which has seriously limited their industrial applications in some high voltage transfer gains areas. As shown in Fig. 1-4, the voltage transfer gains of the buck converters with input filter, M_{Buck}, is equal to D, and it is a step-down converter. For the buck-boost converter with output filter, the SEPIC converter and the Cûk converter, all of their voltage transfer gains are equal to $D/(1-D)$. The boost converter with input filter can provide a step-up function, and its voltage transfer gain M_{Boost} is equal to $1/(1-D)$.

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1.3 Review of the High Performance DC-DC Converters

Recently the high performance converters with high voltage transfer gains have been widely studied for many industrial applications, such as car auxiliary power supplies, medical equipment, high intensity discharge headlamps, battery-discharged dc converter in UPS system and fuel-cell based dc converter [78-90]. New technologies are requiring a higher voltage transfer gain, which is usually greater than four. However, high voltage transfer gains cannot be easily realized by conventional step-up converters due to the narrow allowed duty cycles. In these converters, the voltage transfer gain is a function of the modulating control signal of the active switch. Therefore, the high voltage transfer gains can be obtained using conventional PWM converters by: (a) operating at extremely low or high duty ratios D with the corresponding limitations on the finite commutation times of the switching devices; or (b) using a step-down or step-up transformer with the corresponding difficulties in switching surges and operating frequencies.

In theory, higher voltage transfer gains can be obtained by properly adjusting the duty ratio. In practice, the maximum and the minimum attainable voltage transfer gains for the conventional converters are limited by the characteristics of the switching devices. The turn-on time and turn-off time of the active switch now play an important role for the attainable duty ratio and, consequently, in the conversion ratio. Also, when the duty ratio is close to *0* or *1*, great deterioration on the output voltage and inductor currents occur. For the above reasons, it is better to select an operating point in the midrange, i.e., $D = 0.5$. On the other hand, an often-used approach is to use step-down or step-up transformers; however, large switching surges are present that may damage the switching devices and to make the controller difficult to design. Also, the transformer itself would limit the switching frequency of the converter.

A scheme that provides high voltage transfer gains is the cascade connection of conventional converters. This scheme is a multistage approach that consists of two or more converters connected in cascade. One of the major advantages of these converters is a high gain; however, a drawback is that the total efficiency may be low if the number of stages is high, mainly by losses in the switching devices. Matsuo and Harada [78] proposed the cascade connection of buck and buck-boost converters to obtain low-voltage

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in power supplies. Maksimovic and Cuk [79] proposed several topologies of quadratic converters and discussed the DC operating conditions. A large voltage reduction can be obtained using two-stage topologies with a buck converter in the first stage, which regulates the output voltage, and an isolated converter in the second stage, which operates with 50% duty cycle like a "dc transformer" to step down the voltage. Additionally, J.A. Morales-Saldana [32] and M. Veerachary [24-26] performed the systematic research on theoretical modelling for the cascade connection.

The interesting scheme is to have *n* converters connected in cascade with a single active switch, which has been proposed mainly by F.L. Luo [3] and T.F. Wu [34-36]. This class of converters can be used only when the required number of stages is not very large, as the efficiency will be reduced. For example, two stages of boost converter with only one power switch can be adopted to achieve high voltage conversion. The group of B.R. Lin [80] used some active clamp circuits in the proposed converter to realize the zero voltage switching (ZVS) for both main and auxiliary switches and the high voltage transfer gains, in which the voltage stress of main switch can be effectively limited by the active clamp circuit.

The switched capacitor (SC) converters also can provide the high voltage transfer gains than the conventional topologies. Some new circuits of the SC converters were proposed by A. Ioinovici, F.L. Luo and K.W.E. Cheng [41-44, 81, 90]. An SC circuit can also be used in the structure of a ZCS converter. Theoretically, any voltage transfer gains can be achievable by increasing the number of capacitors. Therefore, this type of power electronic circuit may serve as another solution to new challenges of high voltage transfer gains and small size in low-power dc-dc converters.

In recent years an advanced dc-dc conversion enhancement method, *voltage lift* (VL) technique has been proposed by F.L. Luo [48-57]. The main objective is to construct the novel dc-dc topologies which can reach a high efficiency, high power density and simple structures. The positive/negative/double output Luo converters have been successfully constructed and termed by the name of their inventor F.L. Luo. The VL technique differs from current SC techniques. It is well known that the main advantage of SC techniques is the absence of inductors, making very small size and high power density possible. But more switches are required in SC-type converters than in magnetic-based converters.

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Both inductors and capacitors play important roles in the VL technique, and all inner capacitors are fully charged by the power source. Moreover, fewer power switches (usually single switch or two synchronous switches) are included in VL-type structures and avoid those complex multiple switches control schemes.

1.4 Review of Main Analysis Principles in DC-DC Converters

To perform a theoretical analysis for a given dc-dc topology, we usually assume that the circuit is operating in the steady state. This means that: i) the duty ratio D is held constant at a fixed switching frequency for a long time (over a large number of switching cycles). ii) the current and voltage waveforms become periodic with switching cycle T, i.e. $i((n+1)T) = i(nT)$ and $v((n+1)T)=v(nT)$. There are two important principles that describe the steady-state performance of dc-dc converters: *volt-second balance* of the inductor and *charges balance* of the capacitors. These two principles will be used throughout the thesis to analyze the steady-state performance of various new dc-dc topologies, and the following sub-section will give a brief introduction. In addition, classical analytical methods *state-space averaging* and *switching signal flow graph*, will also be introduced because these two methods are widely used in the mathematical modelling of dc-dc converters.

1.4.1 Volt-second balance and charges balance principles

The steady-state condition imposes a periodic behavior of the current flowing through the inductor. Thus, we have

$$i_L(nT) = i_L((n+1)T) \tag{1.1}$$

Also,

$$v_L = L\frac{di_L}{dt} \tag{1.2}$$

Integration over one switching cycle yields:

$$i_L((n+1)T) - i_L(nT) = \frac{1}{L}\int_{nT}^{(n+1)T} v_L(t)dt \tag{1.3}$$

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Since the left-hand side of (1.3) is zero, then the right-hand side must be zero too, i.e.,

$$0=\frac{1}{L}\int_{nT}^{(n+1)T} v_L(t)dt \tag{1.4}$$

Equation (1.4) states that the integral of the voltage across the inductor along a switching cycle must be zero for the steady state. This property is termed *volt-second balance* principle in the steady state.

A similar analysis can be applied to the capacitor. The relationship between the capacitor voltage and the current flowing through capacitor is defined by:

$$i_C(t)=C\frac{dv_C(t)}{dt} \tag{1.5}$$

The integration of (1.5) over one switching cycle yields:

$$v_C((n+1)T)-v_C(nT)=\frac{1}{C}\int_{nT}^{(n+1)T} i_C(t)dt \tag{1.6}$$

Since the left-hand side of (1.6) is zero, then the right-hand side must also be zero, i.e.,

$$0=\int_{nT}^{(n+1)T} i_C(t)dt \tag{1.7}$$

Equation (1.7) states that the integral of the current flowing through the capacitor along a switching cycle must be zero for the steady state. This property is termed *charges balance* principle in the steady state.

1.4.2 State-space averaging method

State-space averaging method is an approximation technique that approximates the switching converter as a continuous linear systems [11-21]. It was firstly proposed by R.D. Middlebrook and S. Cuk [11]. State-space averaging method requires that the effective output filter corner frequency f_c, to be much smaller than the switching frequency f (i.e. $f_c/f<<1$). The mathematical model derived from the state-space averaging permits the designer to determine the steady-state performance and small-signal transfer functions of the switching converter. Procedures for state-space averaging are as follows:

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1) Identify switched models over a switching cycle. Draw the linear switched circuit model for each sub-mode of the switching converter.
2) Identify state variables of the switching converter. Write state equations for each switched circuit model using Kirchoff's voltage and current laws.
3) Perform state-space averaging using the duty ratio as a weighting factor and combine state equations into a single averaged state equation. The state-space averaged equation is

$$\dot{x} = [A_1 d + A_2 (1-d)]x + [B_1 d + B_2 (1-d)]u \tag{1.8}$$

Where: x is the state vector and u is the input signal.

A_1 and A_2 are the state matrixes during switching-on and –off.

B_1 and B_2 are the input matrixes during switching-on and –off.

4) Perturb the averaged state equation to yield steady-state (dc) and dynamic (ac) terms and eliminate the product of any ac terms.

For example, the state-space averaging method is illustrated for an ideal buck converter shown in Fig. 1-5. The state-space averaged equations for the buck converter in matrix form are:

$$\begin{bmatrix} \dot{v}_o \\ \dot{i}_L \end{bmatrix} = \begin{bmatrix} 0 & -(1/L) \\ 1/C & -(1/RC_o) \end{bmatrix} \begin{bmatrix} v_o \\ i_L \end{bmatrix} + \begin{bmatrix} d/L \\ 0 \end{bmatrix} v_{in} \tag{1.9}$$

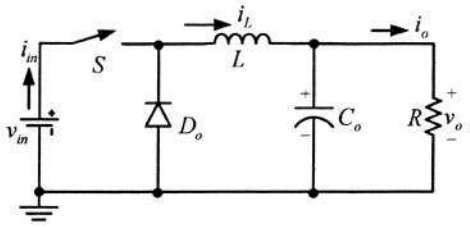

Fig. 1-5. The buck converter

1.4.3 Switching signal flow graph method

State-space averaging has proven in the past to be a very popular analysis technique for deriving various performance characteristics of PWM dc-dc converters. This general method has led to understanding of dynamic performance of PWM converters. However, the state-space method is sometimes tedious for the circuit designers, especially when the

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converter circuit contains a large number of elements or many power stages. Besides, the linearized models, derived from these traditional methods, can only predict the small-signal stability rather than the large-signal stability information. Therefore, the *switching signal flow graph* (SSFG) method has been introduced by K.M. Smedley and S. Cuk [22] for modelling some complex dc-dc topologies [22-27]. The advantages of this graphical method over other methods are:

1) It converts the switching converter (two or multi-state) into a unified dynamic model.
2) From unified model, it is possible to derive large-signal, small-signal and steady-state models.
3) It is easier to arrive at small-signal models with minimum mathematical manipulations.
4) It provides the designer an easy way of getting large signal global behavior when it is combined with TUTSIM and MATLAB simulators.
5) It is possible to derive various relationships among the circuit variables without any difficulty.
6) It is possible to incorporate the cause and effect relationship of the dynamics, etc.

With the SSFG, a given switching converter can be timely divided into two sub-modes corresponding to the switching states of the active switch. Since the sub-mode is linear, corresponding signal flow graphs G_1 and G_2 can be obtained. These two flow graphs can be combined to form an SSFG by the following:

$$G = kG_1 + \bar{k}G_2 \tag{1.10}$$

Where: k and $\bar{k}$ are switching functions

$$k = \begin{cases} 1 & 0 < t < dT \\ 0 & otherwise \end{cases}$$

$$\bar{k} = 1 - k$$

Equation (1.10) introduces two basic switching branches in G, k branch and $\bar{k}$ branch [22, 23]. The corresponding transmittance of the k branch is equal to the duty ratio d while the corresponding transmittance of the $\bar{k}$ branch is equal to $(1\text{-}d)$, which is usually expressed by $\bar{d}$. Since the switching branches are the only nonlinear components in an SSFG, replacing the switching branches with their models yields the unified steady-state,

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large-signal, and small-signal models for any given dc-dc converter. For example, the large-signal model of the buck converter in Fig. 1-5 is obtained and shown in Fig. 1-6.

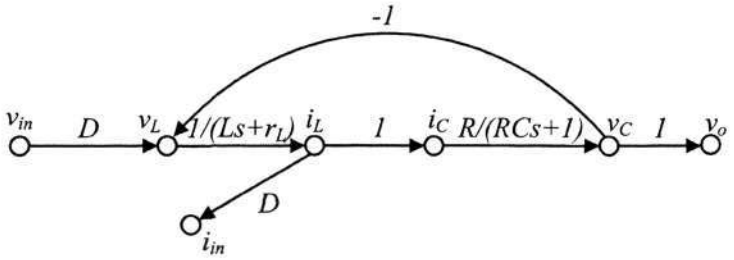

Fig. 1-6. The graphical large-signal model of the buck converter

1.5 Objectives, Research Plan and Major Contributions

1.5.1 Objectives

Reviewing the research work introduced in Section 1.3, we find that most research work for high performance dc-dc converters is based on the existing classical dc-dc topologies. F.L. Luo paved a new way to construct novel dc-dc topologies with high voltage transfer gains. Therefore, constructing novel dc-dc topologies becomes the emphasis in this thesis. The main objectives of this research project are as follows:

- To survey the current dc-dc power conversion techniques for high voltage transfer gains and propose the new dc-dc topologies that can improve output performance.
- To introduce the main characteristics of all dc-dc topologies proposed in the thesis and provide a theoretical support for their future industrial applications.
- To investigate steady and transient phenomena of complex dc-dc topologies which haven't been noticed in the past.
- To develop new analytical methods and concepts that can unify simple and complex dc-dc topologies.

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1.5.2 Research Plan

We have systematically classified the types of dc-dc converters into six categories according to their characteristics and development sequence. This classification grades all dc-dc converters and categorizes new prototypes, and it can be referred to in [3]. The simplified family tree of dc-dc converters is constructed and shown in Fig. 1-7. Following this principle, it is now easy to sort and allocate dc-dc converters and assess their technical features.

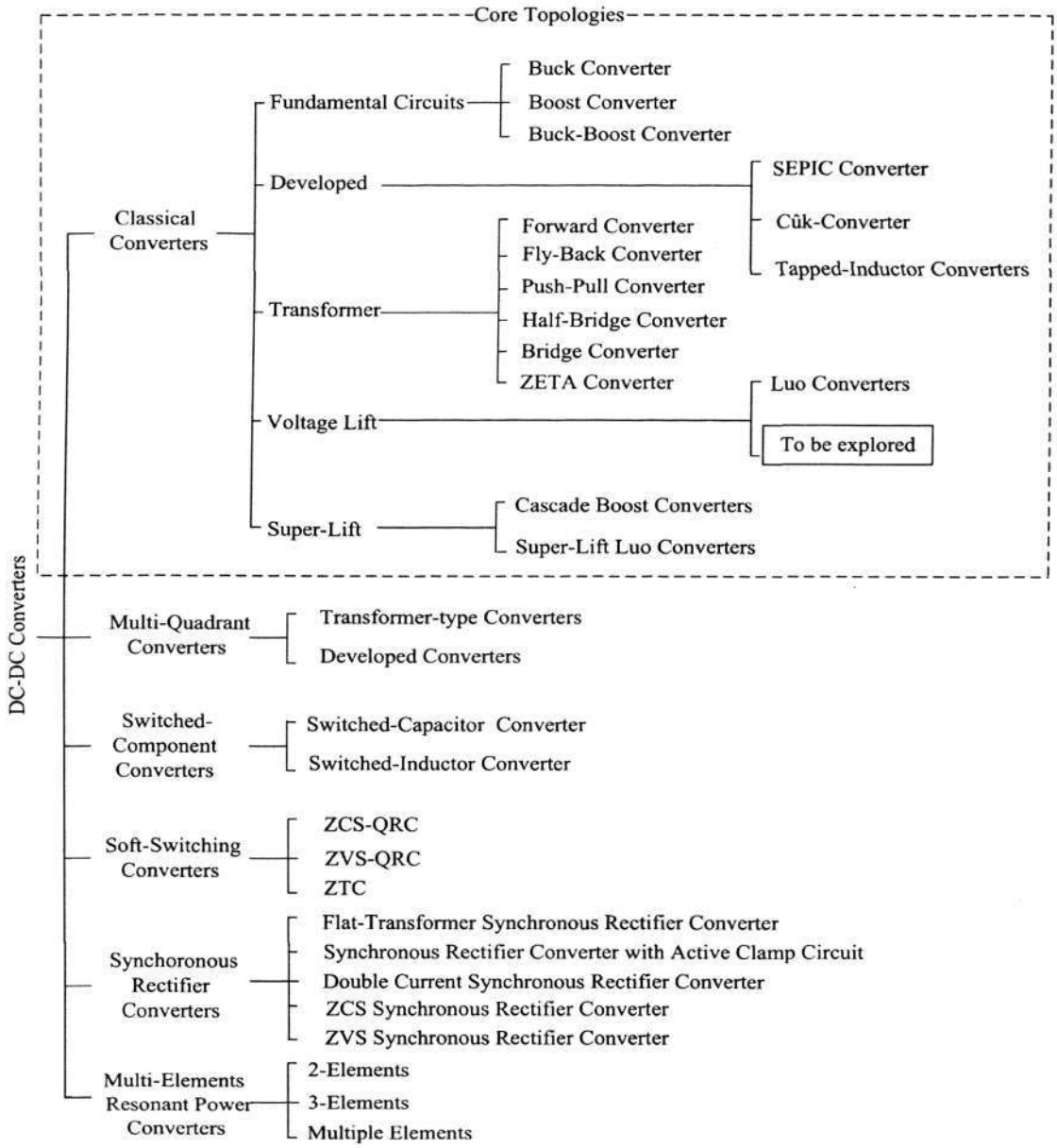

Fig. 1-7. Simplified d family tree of dc-dc power conversion topologies

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From Fig. 1-7, it is seen that development and application of the VL technique resulted in the derivation of Luo converters. However, at present, the research on this area is not enough. Therefore, the exploration of new dc-dc power conversion topologies based on the VL technique might be a potential and valuable area for the research on dc-dc converters.

Based on the aforesaid research objectives and ideas, the main research work in this thesis is divided into two steps as shown in Fig. 1-8. The first step is to perform the investigation on the classical dc-dc converters and to propose several advanced dc-dc power conversion topologies mainly including the positive, negative and double output topologies. Here, the VL technique has been utilized to construct the novel topologies. Based on the research results of the first step, mathematical analytical methods for simple and complex dc-dc topologies are to be explored in the second step.

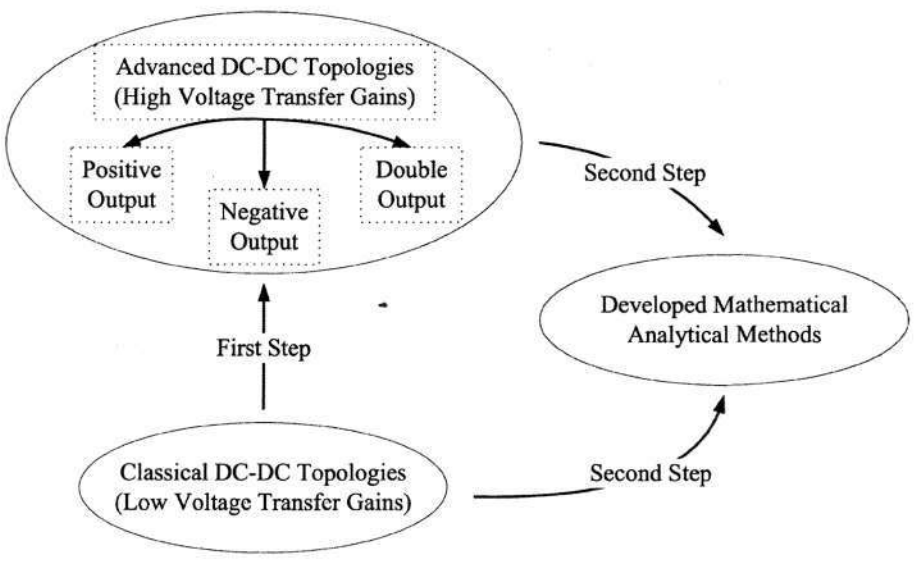

Fig. 1-8. Sketch map of the research plan

1.5.3 Major Contributions

The major contributions of the thesis are summarized as follows:

- The advanced VL technique are developed and applied to the SEPIC and Cûk prototypes, and several series of new dc-dc topologies are created. All of them

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can provide higher voltage transfer gains than the classical dc-dc topologies. In addition, the structures of these new topologies are feasible.

- A series of positive output dc-dc converters based on the SEPIC prototype are proposed, including re-lift circuit and multiple-lift circuits. Here, they are termed *positive output VL-type SEPIC converters*.
- A series of negative output dc-dc converters based on the Cûk prototype are proposed, including developed self-lift circuit, re-lift circuit and multiple-lift circuits. Here, they are termed *negative output VL-type Cûk converters*. In addition, the topology of *enhanced self-lift Cûk converter* is proposed, which can provide the negative-to-positive voltage conversion.
- A novel *mirror-symmetrical double output VL-type* topology is proposed. On the basis of cascade boost converters and super-lift converters [3], two series of enhanced circuits are also proposed. Here, they are termed *boost enhanced series* and *super enhanced series*.
- The applications of *output enhanced circuits [3]* are discussed, which are used to lift the voltage boost ability of dc-dc converters. The general guidelines and examples are given.
- Two graphical analytical methods are investigated in detail. They are *developed switching signal flow graph method* and *averaging binary tree structure representation*. Their general guidelines and concepts are given.
- *Remaining inductor current phenomena* in DCM are investigated. A new explanation for DCM based on the system energy characteristics is proposed, which can be applied to all dc-dc converter cases and can explain all different inductor current phenomena in DCM.
- A new transient modelling method based on the system energy characteristics is proposed. The new generalized concepts, *energy factor* and the sub-sequential other parameters are discussed and used to illustrate the system transient process.
- The parameter "current filling efficiency" proposed in [3] is reexamined during the DCM analysis. The obtained new results modify the corresponding results in [3].

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1.6 Organization of the Thesis

There are eight chapters in this thesis.

In Chapter 1, the background of power electronics, dc-dc converter and main analytical methods are introduced. The objective and main contributions of the research work are also given. The main contents are presented in Chapter 2, 3, 4, 5, 6 and 7, respectively.

In Chapter 2, on the basis of classical SEPIC converter and self-lift SEPIC converter [3], a series of positive output VL-type SEPIC converters are proposed. A detailed theoretical analysis for CCM and DCM is performed. The examples of the self-lift circuit and the re-lift circuit are given, respectively. Both simulation and experimental results are provided to verify the theoretical analysis.

In Chapter 3, on the basis of classical Cûk converter and self-lift Cûk converter [3], a series of negative output VL-type Cûk converters are proposed. A detailed theoretical analysis for CCM and DCM is performed. The examples of the elementary self-lift circuit, the developed self-lift circuit and the re-lift circuit are given, respectively. Both simulation and experimental results are provided to verify the theoretical analysis. A supplementary introduction on negative-to-positive voltage conversion is given at the end of this chapter, and a novel circuit termed enhanced self-lift Cûk converter is proposed with theoretical analysis and verification results.

In Chapter 4, a mirror-symmetrical double output dc-dc topology is proposed. A detailed theoretical analysis for CCM and DCM is performed. Then, two series of enhanced circuits are proposed, and a brief introduction is given. Both simulation and experimental results are provided to verify the theoretical analysis.

In Chapter 5, the general application guidelines of output enhanced circuits proposed in [3] are given to lift the voltage boost ability of positive output dc-dc converters. The applications to the boost converter and the VL-type SEPIC converters are discussed.

In Chapter 6, two graphical analytical methods, developed switching signal flow graph method and averaging binary tree structure representation method are investigated in

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detail. Their general guidelines and concepts are given. Both simulation and experimental results are provided to verify the theoretical analysis.

In Chapter 8, remaining inductor current phenomena existing in the complex dc-dc topologies are investigated in detail firstly. A new explanation of DCM based on the system energy characteristics is proposed, and all DCM cases can be unified into the proposed concepts. Furthermore, the concepts of system energy characteristics are developed and applied to the modelling for the multi-state dc-dc converters. Both simulation and experimental results are provided to verify this new method.

Finally, a summary of the research work and some suggestion for further developments are given in Chapter 8.

1.7 Convention of Symbols Used

For any component X in this thesis, its instantaneous current and voltage are expressed as i_X and v_X, and its average current and voltage during a switching cycle in the steady state are expressed as I_X and V_X. Their corresponding perturbations are represented by the lowercase letters with a hat symbol, such as $\hat{i}_X$ and $\hat{v}_X$. All reference directions of currents and voltages can be referred to in the corresponding figures.

For general description, each component is treated as ideal, and the converter output power is equal to its input power (i.e.$V_oI_o=V_{in}I_{in}$). The subscript $-B$ indicates the boundary value between continuous conduction mode (CCM) and DCM. The peak-to-peak variation value is always indicated by the symbol "Δ". The symbols ε, ζ and ξ are defined as output voltage variation ratios, inductor current variation ratios and diode current variation ratios, respectively.

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Chapter 2 Positive Output VL-type SEPIC Converters

This chapter introduces a set of positive output dc-dc converters applying series SEPIC implementing VL techniques. Compared with the prototype of the SEPIC converter, these converters can perform positive-to-positive dc-dc voltage conversion with higher voltage transfer gains. They are different from other existing dc-dc step-up converters and possess obvious advantages, mainly including fewer switches, clear conversion processes and a high output voltage with small ripple. Since the proposed converters avoid using transformers and cascade connection, relatively simple structures are beneficial to potential practical applications in the future.

2.1 Introduction

Dc-dc step-up converters are widely used in computer hardware and industrial applications such as computer periphery power supplies, car auxiliary power supplies, servo-motor drives and medical equipment. As a classical dc-dc topology, the SEPIC converter [28-31] has many industrial applications due to its good characteristics, and its prototype is shown in Fig. 2-1.

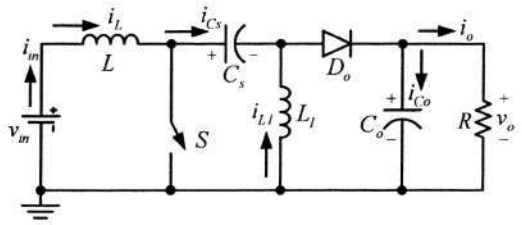

Fig. 2-1. Prototype of the SEPIC converter

This topology does not suffer from an output polarity inversion, and capacitor C_s can prevent unwanted current flow from v_{in} to v_o. Under the different values of duty ratio D, it can perform step-down and step-up dc-dc conversion according to its voltage transfer function expressed as:

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$$M_{SEPIC} = \frac{D}{1-D} \tag{2.1}$$

However, because of the effect of parasitic elements, the practical value of D has an upper limit and cannot be taken too high. So the output voltage and power transfer efficiency of the SEPIC converter have been seriously restricted below (2.1). With the fast technological development, this disadvantage limits the further applications of SEPIC converters in some areas that require higher voltage transfer gains such as in communication equipment, aerospace electronics, portable devices and IC chips.

Dc-dc converters may be developed by n-cell cascade connection or by adding transformers to obtain higher voltage transfer gains [32-39]. However, the resulting problems, energy losses, multiple power switches and large switching surges in transformers significantly increase the control complexity and the cost of these converters. In recent years advanced dc-dc conversion enhancement techniques such as SC [40-47] and VL techniques [48-57] have been greatly explored. The main objective is to reach a high efficiency, high power density and simple structures. Since SEPIC converters are widely used in power electronics as a classical topology, the combination with the SEPIC prototype and above-mentioned enhancement techniques could be a good solution for promoting its further application.

In [3], F.L. Luo proposed a developed SEPIC converter integrating the VL technique, and it is termed *the self-lift SEPIC converter*. As shown in Fig. 2-2, the self-lift SEPIC converter is derived from the SEPIC prototype by adding the components (D_1-C_1). The lift circuit consists of L_1-D_1-C_1, and it can be regarded as a basic VL cell. When switch S turns on, D_1 is on, and D_o is off. When S turns off, D_1 is off, and D_o is on. The capacitor C_1 performs a function to lift the output capacitor voltage V_{Co} by the capacitor voltage V_{Cs}.

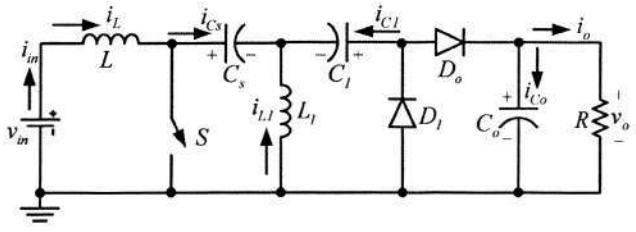

Fig. 2-2. Topology of the self-lift circuit

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From the analysis in [3], it is known that the voltage boost ability of this self-lift circuit is increased from $D/(1-D)$ to $1/(1-D)$. This circuit paves a new way to develop the classical SEPIC converter, and applying the VL technique might have the potential to derive more new SEPIC-based topologies.

In this chapter, a series of *positive output VL-type SEPIC converters* have been presented on the basis of the SEPIC prototype and the self-lift SEPIC converter. Due to the similar circuit mechanism and for the convenience of analysis, the self-lift SEPIC converter in Fig. 2-2 can be regarded as the elementary circuit of all proposed circuits. Therefore, *positive output VL-type SEPIC converters* can be categorized into:

- self-lift circuit (i.e. self-lift SEPIC converter [3])
- re-lift circuit
- multiple circuits (e.g. triple-lift and quadruple-lift circuit).

The VL-type SEPIC converters to be introduced in this chapter are different from any other existing dc-dc step-up converters and possess the advantage of high voltage lift ability as well as primary advantages in the SEPIC prototype. All circuits perform positive to positive dc-dc voltage conversion with higher voltage transfer gains, small ripple and high efficiency in simple structures. Therefore, they will be used in computer peripheral equipment and industrial applications, especially for high output voltage projects. The detailed analysis will be performed in the following sections.

2.2 Self-Lift Circuit

A very simple introduction on the self-lift circuit was given in [3]; however, the introduction and results in [3] are not enough for practical design and applications. This is because the following reasons:

- The results on DCM is wrong.
- Parameter "current filling efficiency" was proposed, but its usage during calculation is not correct.
- The voltage and current characteristics of each component have not been provided in detail.

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No more detailed analysis procedure and valuable results can be found in other opening literatures so far. As stated in Chapter 2.1, the self-lift circuit plays an important role for all proposed circuits, so it is necessary to give a detailed analysis to reexamine and reveal its main circuit characteristics before the introduction of the other new circuits.

The equivalent circuits during switching-on, switching-off and DCM are thus shown in Fig. 2-3(a-c), respectively. Switching diagrams with main steady-state waveforms for a switching cycle in CCM are shown in Fig. 2-4 to analyze the circuit operation, where reference directions are referred to in Fig. 2-2.

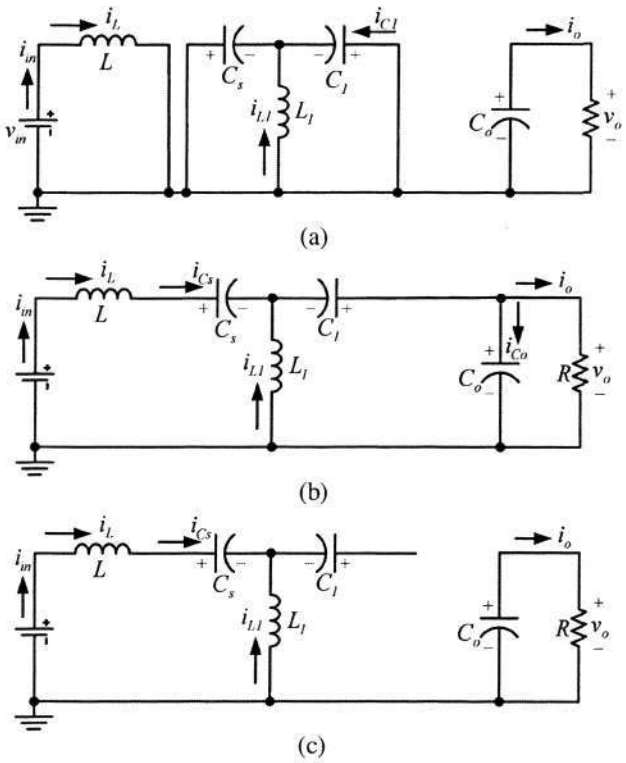

Fig. 2-3. Equivalent circuits of the self-lift circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

2.2.1 Circuit analysis in CCM

In the steady state, the average voltage across L over a cycle is zero. Thus

$$V_{Cs} = V_{in}$$

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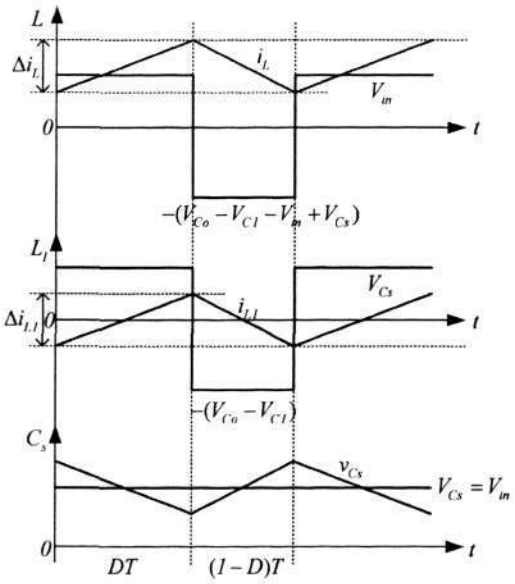

Fig. 2-4. Self-lift circuit: waveforms with enlarged variations

During switching-on, the voltage across C_1 is equal to V_{Cs}. Since C_s, and C_1 are sufficiently large, we have:

$$V_{C1} = V_{Cs} = V_{in}$$

The inductor current i_L increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{in} and $-(V_{Co} - V_{C1} - V_{in} + V_{Cs})$. Therefore, with the sec-voltage balance principle, we have

$$DTV_{in} = (1-D)T(V_{Co} - V_{C1} - V_{in} + V_{Cs}) \text{ or } DTV_{in} = (1-D)T(V_o - V_{in})$$

Hence,

$$V_o = \frac{1}{1-D} V_{in}$$

The voltage transfer gain in CCM is

$$M_S = \frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{2.2}$$

and the input current is

$$I_{in} = \frac{1}{1-D} I_o = I_L = I_{Cs-off} \tag{2.3}$$

Where: I_{Cs-off} is defined as the average current (charging current) during switch-off.

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The charges of C_o and C_s increase during switching-off and decrease during switching-on. We get:

$$Q_{Co+} = I_o DT \qquad Q_{Cs+} = I_{Cs-on} DT$$
$$Q_{Co-} = I_{Co-off}(1-D)T \qquad Q_{Cs-} = I_{Cs-off}(1-D)T$$

In a switching cycle, $Q_{Co+}=Q_{Co-}$ and $Q_{Cs+}=Q_{Cs-}$. Therefore,

$$I_{Co-off} = \frac{D}{1-D} I_o, \quad I_{Cs-on} = \frac{1}{D} I_o$$

During switching-off, $i_{Do}=i_{Co}+i_o$. Therefore,

$$I_{Do-off} = I_{Co-off} + I_o = \frac{1}{1-D} I_o \tag{2.4}$$

During switching-off, L_1 and C_1 form a path and transfer the stored energy through D_o. Therefore,

$$I_{C1-off} = I_{Do-off} = \frac{1}{1-D} I_o$$

In a switching cycle, $Q_{C1+}=Q_{C1-}$. Therefore,

$$I_{C1-on} = \frac{1-D}{D} I_{C1-off} = \frac{1}{D} I_o$$

During switching-on, L_1 and C_1 are connected in parallel and accept the stored energy from C_s. Therefore, with the KCL law,

$$I_{L1} = I_{Cs-on} - I_{C1-on} = 0 \tag{2.5}$$

Equation (2.5) is for the average value of a switching cycle in the steady state. It is noted that a practical instantaneous inductor current i_{L1} flows through L_1 during each cycle. The energy storing and transferring of L_1 are achieved by associate oscillation of i_{L1}.

Since the peak-to-peak current variation of i_L, Δi_L is equal to DTV_{in}/L, the variation ratio of the current i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2M_S^2} \frac{R}{fL} \tag{2.6}$$

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The variation of the current i_{Do} during switching-off is equal to Δi_{L1}, and Δi_{L1} is equal to DTV_{in}/L_1. Therefore, the variation ratio of i_{Do} is

$$\xi_{Do} = \frac{\Delta i_{L1}/2}{I_{Do-off}} = \frac{D}{2M_S^2}\frac{R}{fL_1} \tag{2.7}$$

The peak-to-peak voltage variation of v_o, Δv_o is equal to $I_o DT/C_o$. Therefore, the variation ratio of v_o is

$$\varepsilon_S = \frac{\Delta v_o/2}{V_o} = \frac{D}{2RC_o f} \tag{2.8}$$

2.2.2 Circuit analysis in DCM

The self-lift circuit operates in DCM if the current i_{Do} reduces to zero during switching-off. The condition for DCM is $\xi_{Do} \geq 1$, i.e.

$$\xi_{Do} = \frac{D}{2M_S^2} Z_N \geq 1 \tag{2.9}$$

where Z_N is defined as the normalized load $R/(fL_1)$.

As a special case, when i_{Do} decreases to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore, the boundary between CCM and DCM is obtained as below:

$$Z_{N-B} = \frac{2M_s^2}{D} = \frac{2}{D(1-D)^2} \tag{2.10}$$

When $Z_N > Z_{N\text{-}B}$, the circuit is operating in DCM. Under this condition, i_{Do} decreases to zero at $t = t_1 = [D+m_S(1\text{-}D)]T$, and i_{L1} decreases to zero at $t = t_k = [D+km_S(1\text{-}D)]T$ where

$$DT < t_k < t_1 < T \text{ and } 0 < k < 1,\ 0 < m_S < 1$$

Here, m_S is the current filling efficiency for self-lift circuit and defined as

$$m_S = \frac{t_1 - DT}{(1-D)T} \tag{2.11}$$

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In DCM, current i_{L1} increases during switching-on and decreases during the period from DT to $m_S(1-D)T$. The corresponding voltages across L_1 are V_{Cs} and $-(V_{Co}-V_{C1})$. Thus, using the volt-second balance principle, we have

$$DTV_{Cs} = m_S(1-D)T(V_{Co}-V_{C1}) \text{ or}$$
$$DTV_{in} = m_S(1-D)T(V_o-V_{in}) \tag{2.12}$$

Additionally, the transferred charges of L_1 during switching-off to compensate the total consumed charges of the load, are equal to $m_S k(1-D)T\Delta i_{L1}/2$, where, k is the modified coefficient and defined as $(t_k\text{-}DT)/(t_1\text{-}DT)$. So we have

$$I_o T = \frac{1}{2} m_S k(1-D)T\Delta i_{L1} \text{ or}$$
$$\frac{V_o}{R}T = \frac{1}{2} m_S k(1-D)T\frac{DTV_{in}}{L_1} \tag{2.13}$$

Combining (2.12) and (2.13), we obtain

$$m_S = \frac{1+\sqrt{k^2+2kD^2Z_N}}{D(1-D)Z_N} \tag{2.14}$$

From (2.12), we have

$$V_o = [1+\frac{D}{m_S(1-D)}]V_{in} \tag{2.15}$$

Therefore, substituting (2.14) into (2.15) yields the following voltage transfer gain in DCM:

$$M_{S-DCM} = 1+\frac{D^2Z_N}{1+\sqrt{k^2+2kD^2Z_N}} \tag{2.16}$$

Using (2.2), (2.10) and (2.16), we obtain the boundary curve between CCM and DCM. The voltage transfer gains versus the normalized load are thus shown in Fig. 2-5, which is beneficial for theoretical analysis and practical engineering design.

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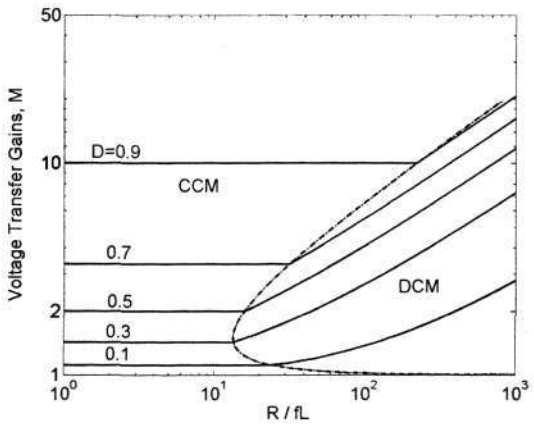

Fig. 2-5. Self-lift circuit: boundary between CCM and DCM and voltage transfer gains against Z_N

2.3 Re-Lift Circuit

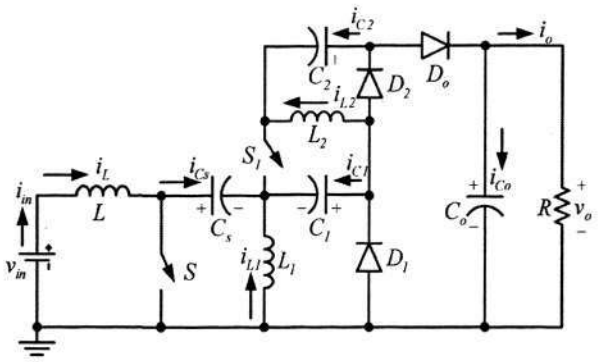

Fig. 2-6. Topology of the re-lift circuit

The re-lift circuit shown in Fig. 2-6 is derived from the self-lift circuit by adding the components (L_2-D_2-C_2). It consists of two static switches S and S_1 switching simultaneously. The lift circuit consists of L_1-D_1-C_1-L_2-D_2-C_2-S_1 and it can be divided into two basic voltage lift cells. When switches S and S_1 turn on, D_1 and D_2 are on, and D_o is off. When S and S_1 turn off, D_1 and D_2 are off, and D_o is on. Capacitors C_1 and C_2 perform characteristics to lift the output capacitor voltage V_{Co} by twice the capacitor voltage V_{Cs}. L_2 performs the function of a ladder joint to link the two capacitors C_1 and C_2 and lift V_{Co}.

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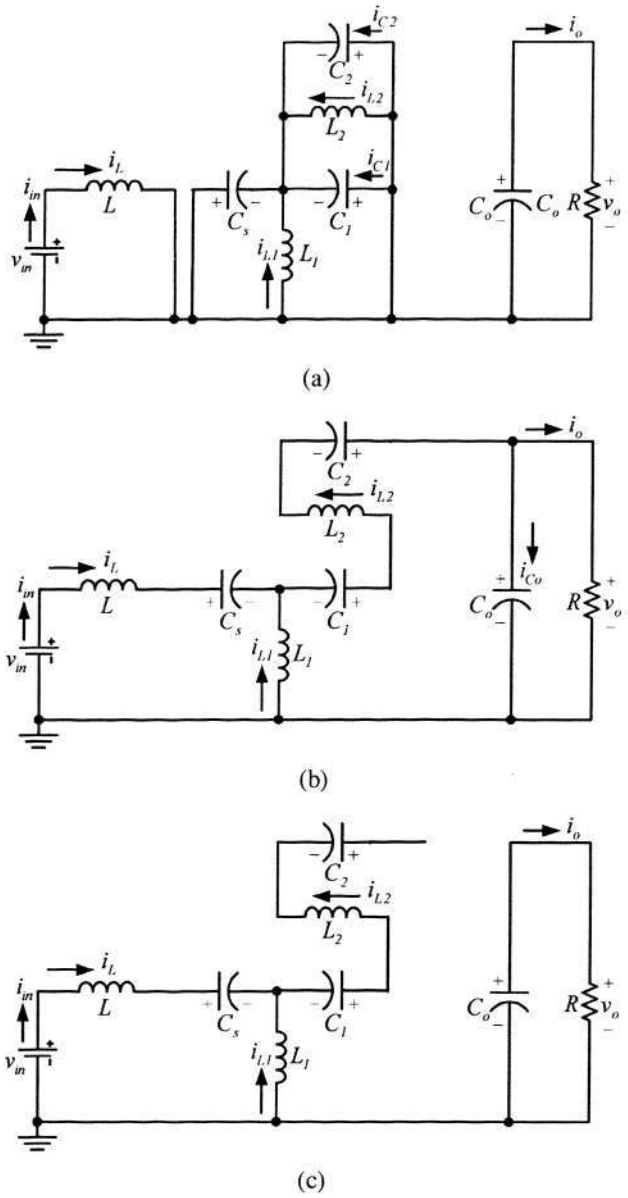

Fig. 2-7. Equivalent circuits of the re-lift circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

The equivalent circuits during switching-on, switching-off and DCM are shown in Fig. 2-7(a-c), respectively. In the following sub-sections, the circuit is assumed operating in CCM.

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2.3.1 Circuit analysis in CCM

Switching diagrams with main steady-state waveforms for a switching cycle are shown in Fig. 2-8 to analyze the circuit operation, where reference directions are referred to in Fig. 2-6.

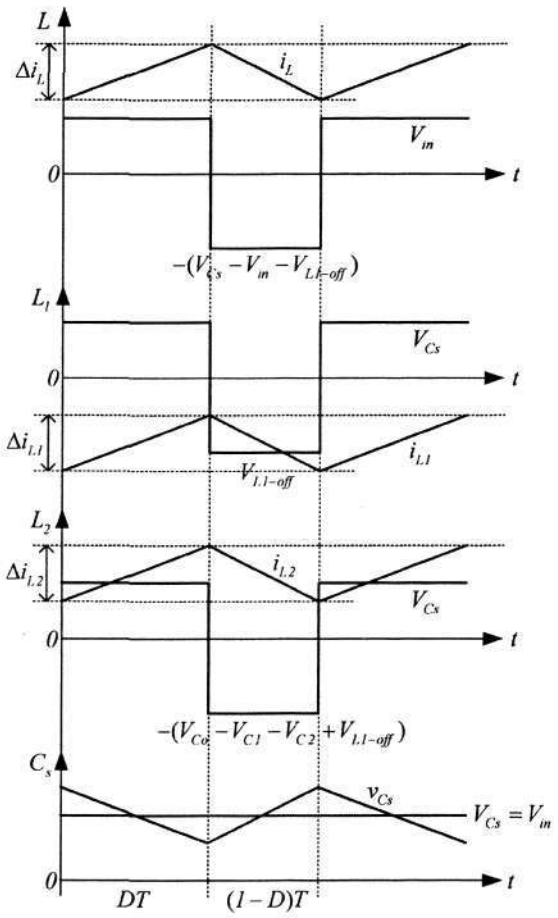

Fig. 2-8. Re-lift circuit: waveforms with enlarged variations

In the steady state, both the average voltages across L and L_1 over a cycle are zero. Thus,

$$V_{Cs} = V_{in}$$

During switching-on, both the voltages across C_1 and C_2 are equal to V_{Cs}. Since C, C_1 and C_2 are sufficiently large, we have:

$$V_{C1} = V_{C2} = V_{Cs} = V_{in}$$

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The voltage across L_1 is equal to V_{Cs} during switching-on. With the volt-second balance principle,

$$V_{L1-off} = -\frac{D}{1-D}V_{Cs} = -\frac{D}{1-D}V_{in}$$

The inductor current i_{L2} increases during switching-on and decreases during switching-off. The corresponding voltages across L_2 are V_{Cs} and $-(V_{Co} - V_{C1} - V_{C2} + V_{L1-off})$. Therefore, with the sec-voltage balance principle, we have

$$DTV_{Cs} = (1-D)T(V_{Co} - V_{C1} - V_{C2} + V_{L1-off}) \text{ or } DTV_{in} = (1-D)T(V_o - 2V_{in} + V_{L1-off})$$

Hence

$$V_o = \frac{2}{1-D}V_{in}$$

The voltage transfer gain in CCM is

$$M_R = \frac{V_o}{V_{in}} = \frac{2}{1-D} \tag{2.17}$$

and the input current is

$$I_{in} = \frac{2}{1-D}I_o = I_L = I_{Cs-off} \tag{2.18}$$

The charges of both C_o and C_s increase during switching-off and decrease during switching-on. Thus, we get:

$$Q_{Co+} = I_o DT \qquad Q_{Cs+} = I_{Cs-on}DT$$
$$Q_{Co-} = I_{Co-off}(1-D)T \qquad Q_{Cs-} = I_{Cs-off}(1-D)T$$

In a switching cycle, Q_{Co+}=Q_{Co-} and Q_{Cs+}=Q_{Cs-}. Therefore,

$$I_{Co-off} = \frac{D}{1-D}I_o, \quad I_{Cs-on} = \frac{2}{D}I_o$$

During switching-off, i_{Do}=i_{Co}+i_o. Therefore,

$$I_{Do-off} = I_{Co-off} + I_o = \frac{1}{1-D}I_o \tag{2.19}$$

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During switching-off, L_1, C_1, L_2 and C_2 form a path and transfer the stored energy through D_o. Therefore,

$$I_{L2} = I_{C1-off} = I_{C2-off} = I_{Do-off} = \frac{1}{1-D} I_o \tag{2.20}$$

In a switching cycle, $Q_{C1+}=Q_{C1-}$ and $Q_{C2+}=Q_{C2-}$. Therefore,

$$I_{C1-on} = I_{C2-on} = \frac{1-D}{D} I_{L2} = \frac{1}{D} I_o$$

During switching-on, L_1, C_1, L_2 and C_2 are connected in parallel and accept the stored energy from C_s. Therefore, with the KCL law,

$$I_{L1} = I_{Cs-on} - I_{C1-on} - I_{C2-on} - I_{L2} = -\frac{1}{1-D} I_o \tag{2.21}$$

Equation (2.21) indicates that the practical i_{L1} is flowing in an opposite direction, and reference positive direction of i_{L1} is shown in Fig. 2-6.

In a switching cycle, Δi_L is equal to DTV_{in}/L, therefore, the variation ratio of the current i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2M_R^2} \frac{R}{fL} \tag{2.22}$$

Analogously, Δi_{L1} and Δi_{L2} correspond to DTV_{in}/L_1 and DTV_{in}/L_2, respectively. Therefore, the variation ratios of i_{L1} and i_{L2} are

$$\varsigma_{L1} = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{D}{M_R^2} \frac{R}{fL_1} \tag{2.23}$$

$$\varsigma_{L2} = \frac{\Delta i_{L2}/2}{I_{L2}} = \frac{D}{M_R^2} \frac{R}{fL_2} \tag{2.24}$$

The variation of the current i_{Do} during switching-off is equal to Δi_{L2}, and Δi_{L2} is equal to DTV_{in}/L_2. Therefore, the variation ratio of i_{Do} is

$$\xi_{Do} = \varsigma_{L2} = \frac{D}{M_R^2} \frac{R}{fL_2} \tag{2.25}$$

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The peak-to-peak voltage variation of v_o, Δv_o is equal to $I_o DT/C_o$. Therefore, the variation ratio of v_o is

$$\varepsilon_S = \frac{\Delta v_o / 2}{V_o} = \frac{D}{2RC_o f} \tag{2.26}$$

Equations (2.23) and (2.24) indicate that inductor current variations during a switching cycle may be different due to the inductance difference. Because L_1 and L_2 are in series during switching-off, the same inductance is thus recommended in practical circuit design. In reality, although they will be slightly different, it will not affect the normal operation. This is because the practical inductor current variations (ripple) will be rather small under the high switching frequency and large inductance conditions.

2.3.2 Circuit analysis in DCM

From the foregoing explanation, it is assumed that L_1 and L_2 are the same, which can simplify the boundary analysis of CCM and DCM. The re-lift circuit operates in DCM if the current i_{Do} reduces to zero during switching-off. The condition for DCM is $\xi_{Do} \geq 1$, i.e.

$$\xi_{Do} = \frac{D}{M_R^2} Z_N \geq 1 \tag{2.27}$$

As a special case, when i_{Do} decrease to zero at $t=T$, the circuit operates at the boundary of CCM and DCM. Therefore, the boundary between CCM and DCM is obtained as below:

$$Z_{N-B} = \frac{M_R^2}{D} = \frac{4}{D(1-D)^2} \tag{2.28}$$

When $Z_N > Z_{N\text{-}B}$, the circuit is operates in DCM. Under this condition i_{Do} decreases to zero at $t = t_1 = [D+m_R(1\text{-}D)]T$ where

$$DT < t_1 < T \text{ and } 0 < m_R < 1$$

Here, m_R is the current filling efficiency for the re-lift circuit, and its definition is the same to (2.11).

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In DCM, because current i_{L2} increases during switching-on and decreases during the period from DT to $(1\text{-}D)m_RT$, we thus have

$$V_{L2-off} = -\frac{D}{(1-D)m_R}V_{in}$$

Current i_{L1} increases during switching-on and decreases during the period from DT to $m_R(1-D)T$. The corresponding voltages across L_1 are V_{Cs} and $-(V_{Co}-V_{C1}-V_{C2}+V_{L2-off})$. Thus, using the volt-second balance principle, we have

$$DTV_{Cs} = (1-D)m_RT(V_{Co}-V_{C1}-V_{C2}+V_{L2-off}) \quad \text{or}$$

$$DTV_{in} = (1-D)m_RT[V_o - 2V_{in} - \frac{D}{(1-D)m_R}V_{in}] \tag{2.29}$$

Additionally, the transferred charges of L_2 during switching-off are equal to $m_R(1-D)T\Delta i_{L2}/2$, which compensate the total consumed charges of the load. So we have

$$I_oT = \frac{1}{2}m_R(1-D)T\Delta i_{L2} \quad \text{or}$$

$$\frac{V_o}{R}T = \frac{1}{2}m_R(1-D)T\frac{DTV_{in}}{L_2} \tag{2.30}$$

Combining (2.29) and (2.30), we obtain

$$m_R = \frac{2+2\sqrt{1+D^2Z_N}}{D(1-D)Z_N} \tag{2.31}$$

From (2.29), we have:

$$V_o = [2+\frac{2D}{m_R(1-D)}]V_{in} \tag{2.32}$$

Therefore, substituting (2.31) into (2.32) yields the following voltage transfer gain in DCM:

$$M_{R-DCM} = 1+\sqrt{1+D^2Z_N} \tag{2.33}$$

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Using (2.17), (2.28) and (2.33), we can obtain the boundary curve between CCM and DCM. The voltage transfer gains versus the normalized load are thus shown in Fig. 2-9, which is beneficial for theoretical analysis and practical engineering design.

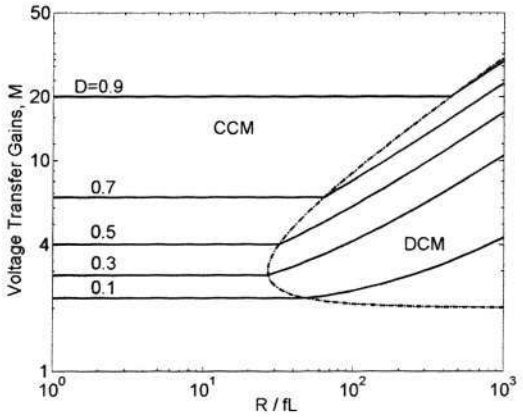

Fig. 2-9. Re-lift circuit: boundary between CCM and DCM and voltage transfer gains against Z_N

2.4 Multiple-Lift Circuit

2.4.1 General analysis

Referring to Fig. 2-6, it is possible to construct multiple-lift circuits by repeating adding the components (L_2-D_2-C_2-S_1). Assuming that there are n VL cells, the generalized multiple-lift circuit is shown in Fig. 2-10 with reference directions. All future active switches can be replaced by passive diodes. According to this principle, only two synchronous switches S and S_1 are required for each complex multiple-lift circuit, which simplify the control scheme and decrease the cost significantly. Hence, each circuit has two switches, $(n+1)$ inductors, $(n+2)$ capacitors and $(2n-1)$ diodes.

When switches S and S_1 turn on, D_1, D_2,…, D_{2n-1} are on, and D_o is off. When S and S_1 turn off, D_1, D_2,…, D_{2n-1} are off, and D_o is on. Capacitors C_1, C_2,…,C_n lift V_{Co} by n times of V_{Cs}. Inductors L_2, L_3,… L_n perform the same function of a ladder joint to link the adjacent capacitors. From the foregoing analysis and calculation, the general formulas for all multiple-lift circuits can be obtained according to the similar steps.

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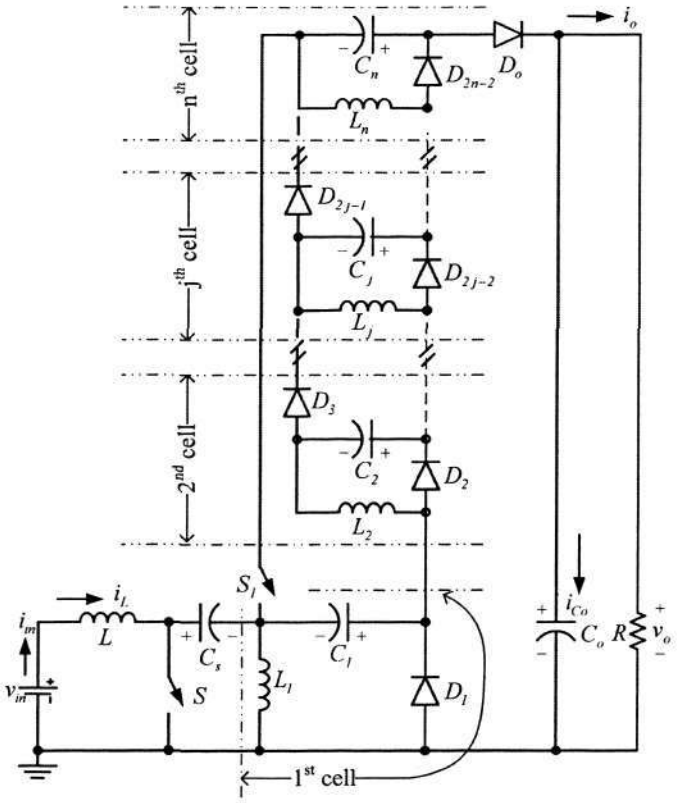

Fig. 2-10. Multiple-lift circuit possessing n voltage-lift cells

The generalized voltage transfer gain is

$$M = \frac{n}{1-D} \qquad n = 1,2,3,4,... \tag{2.34}$$

The generalized j^{th} inductor current is

$$I_{Lj} = \frac{(n-j)^{h(j)}}{1-D} I_o \tag{2.35}$$

where

$$h(j) = \begin{cases} 1 & j = 0\ ,\ 1 \\ 0 & 1 < j \le n \end{cases} \quad \text{and } 0^0 = 1$$

and the subscript 0 denotes the inductor L which is connected with the source in the circuit.

Therefore, the generalized variation of the j^{th} inductor current i_{Lj} is

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$$\varsigma_{Lj} = \frac{\Delta i_{Lj}/2}{I_{Lj}} = \frac{nD}{2M^2(n-j)^{h(j)}} \frac{R}{fL_j} \tag{2.36}$$

Analogously, the generalized variation ratio of the output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{D}{2RfC_o} \tag{2.37}$$

The generalized variation of the diode current i_{Do} is

$$\xi_{Do} = \frac{nD}{2M^2} \frac{R}{fL_n} \tag{2.38}$$

It is assumed that all inductors existing in the voltage lift cells are the same. Therefore, the generalized boundaries between the CCM and DCM for all circuits are

$$Z_{N-B} = \frac{2M^2}{nD} = \frac{2n}{D(1-D)^2} \tag{2.39}$$

The generalized current efficiency is

$$m = \frac{n + \sqrt{n^2 + 2nD^2Z_N}}{D(1-D)Z_N} \tag{2.40}$$

The generalized voltage transfer gain in DCM is

$$M_{DCM} = \frac{1}{2}(n + \sqrt{n^2 + 2nD^2Z_N}) \tag{2.41}$$

If the generalized circuit possesses three VL cells, it is termed the triple-lift circuit. If the generalized circuit possesses four VL cells, it is termed the quadruple-lift circuit. The main characteristics of these two multiple-lift circuits are given in Table 2-1 for ready reference.

The boundaries between CCM and DCM of all proposed circuits are shown in Fig. 2-11. The curves of all M versus Z_N indicate that the CCM area increases from the self-lift circuit via the re-lift circuit, the triple-lift circuit to the quadruple-lift circuit. There are minimum values of Z_N (*13.5, 27, 40.5* and *54*) at the boundaries, and all of them are under the condition of D = *1/3*. It means that the condition of D = *1/3* is the most possible for these converters to enter DCM. The corresponding extreme points are also marked in Fig. 2-11 for ready reference.

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Table 2-1. Main Characteristics of Proposed Multiple-lift Circuits

	Triple-Lift Circuit	Quadruple-Lift Circuit
M	$3/(1-D)$	$4/(1-D)$
M_{DCM}	$(3+\sqrt{9+6D^2Z_N})/2$	$2+\sqrt{4+2D^2Z_N}$
$Z_{N\text{-}B}$	$\frac{6}{D(1-D)^2}$	$\frac{8}{D(1-D)^2}$
m	$\frac{3+\sqrt{9+6D^2Z_N}}{D(1-D)Z_N}$	$\frac{4+2\sqrt{4+2D^2Z_N}}{D(1-D)Z_N}$
I_L	$[3/(1-D)]I_o$	$[4/(1-D)]I_o$
I_{L1}*	$-[2/(1-D)]I_o$	$-[3/(1-D)]I_o$
I_{L2} I_{L3}	$[1/(1-D)]I_o$	$[1/(1-D)]I_o$
I_{L4}	Nil	

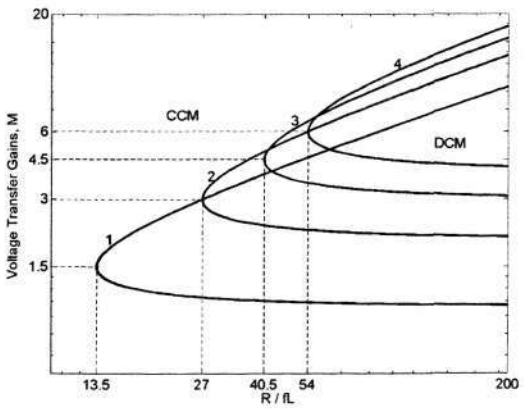

Fig. 2-11. Boundaries between CCM and DCM against the normalized load Z_N

(1: self-lift circuit; 2: re-lift circuit; 3: triple-lift circuit; 4: quadruple-lift circuit)

2.4.2 Steady-state performance summary

From the foregoing analysis, we can get an overview and main analytical results of proposed VL-type converters. Equation (2.37) indicates that the output voltage variation ratios are determined by the interactions caused by D, R, f and C_o. So increasing the capacitance of output capacitor can effectively decrease the ripper of output voltages.

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In order to show the high voltage transfer gains characteristics of proposed circuits over the conventional SEPIC converter, voltage transfer gains V_o/V_{in} in duty ratio D = *0.33, 0.5, 0.75* and *0.8* are listed in Table 2-2.

Table 2-2. Comparison of four proposed converters with conventional SEPIC converter

Topology		V_o/V_{in}			
		D=0.33	*D=0.5*	*D=0.75*	*D=0.8*
Conventional SEPIC prototype		*0.5*	*1*	*3*	*4*
Proposed converters	Self-lift circuit	*1.5*	*2*	*4*	*5*
	Re-lift circuit	*3*	*4*	*8*	*10*
	Triple-lift circuit	*4.5*	*6*	*12*	*15*
	Quadruple-lift circuit	*6*	*8*	*16*	*20*

The data in Table 2-2 indicate all proposed converters can get higher voltage transfer gains compare with traditional topologies. Although traditional n-cell cascade connection converters (quadratic converters) and transformer-type converters can achieve high voltage transfer gains, their efficiency η remains low. This is because η of n-cell cascade connection converters given by the product of the efficiencies of each cell belonging to the cascade connection, i.e. $\eta = \eta_1\eta_2..\eta_n$. And η of transformer-type converters would be limited by additional losses caused by transformer magnetic characteristics. Since all proposed converters avoid these problems, compact structures with a good efficiency might be achieved in the practical manufacture. The practical efficiency of a dc-dc converter equipment is usually concerned with the interactions caused by the components, layout, operation conditions, mechanical and thermal details, which may be further explored and improved by industrial companies.

2.5 General Guidelines of Parameters Selection

Three kinds of basic parameters, L, C_o and f, have to be chosen. The first design formula is the classical one based on a small ripple Δi_L of i_L, which is:

$$L = V_{in}\frac{DT}{\Delta i_L} \tag{2.42}$$

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The above design formula can be extended to the selection of other inductors, L_1, L_2...L_n, and consequently, we have:

$$L_n = V_{Ln} \frac{DT}{\Delta i_{Ln}} \tag{2.43}$$

Where: V_{Ln} is defined as the voltage across L_n during DT.

The first design formula for C_o and f is also the classical one, requiring for a small ripple in the output voltage ΔV_o (It is noted that this requirement comes not only from the desire of having clean dc load voltage, but mainly from the need of increasing the efficiency of the SC circuit and decreasing the peak of the capacitor current, i.e. decreasing the EMI). So we have:

$$C_o f = \frac{V_o}{2R(\Delta V_o / 2)} \tag{2.44}$$

Furthermore, in all circuits introduced in this chapter, L, C_o and f have to meet one more complicated constraint, the switching operation has to be calculated in such a way as to:1) allow for charging C_1, C_2...C_n at their nominal required value during the switching-on mode (similar to SC converters, the nominal operating point has to be on the linear part of the capacitor charging characteristic), and 2) avoid sensible discharging of the capacitors during the switch-off mode. Usually, we let:

$$C_1 = C_2 = ... = C_n < C_s \tag{2.45}$$

According to above-mentioned design formula and general guidelines, an elementary parameter selection can be performed. Then, the corresponding Z_N and $Z_{N\text{-}B}$ can be calculated to determine the operation mode, which is verified by the initial design objective. The criterion using Z_N and $Z_{N\text{-}B}$ is as follows:

$$\begin{cases} Z_N < Z_{N-B} : CCM \\ Z_N > Z_{N-B} : DCM \end{cases} \tag{2.46}$$

These requirements give an implicit constraint. By using the time-domain equations of each topology, the constraints have been applied to the steady-state cycle, and numerical solutions can have been obtained by computer simulation and calculation.

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It is noted that the general guidelines introduced in this part are applicable not only to the positive output VL-type SEPIC converters in this chapter, but also to the other circuits that will be introduced in the next chapters.

2.6 Simulation and Experimental Results

Simulation package PSIM was applied to self-lift and re-lift circuits. Inductor currents and output voltage are given to verify the theoretical analysis. All diodes and the switch in simulation cases are ideal. The corresponding hardware testing circuits were also constructed to compare with the simulation results. It is noted that v_o and v_{Cs} are demonstrated through channel 1 and 2 of the oscillograph, respectively.

2.6.1 Simulation verification of the self-lift circuit in CCM

The circuit parameters for simulation are: $V_{in}=10V$, $R=100\Omega$, $L=1mH$, $L_1=500\mu H$, $C_s=110\mu F$, $C_1=22\mu F$, $C_o=110\mu F$ and $D=0.6/0.75/0.4$. The switching frequency f is $100kHz$. Since the case is to be performed in CCM, we use (2.10) and get the boundary values of normalized load, $Z_{N-B}\big|_{D=0.6/0.75/0.4}=20.8/42.7/16.94$. The normalized load Z_N in this case is equal to 2 and located at the left CCM region of the boundary curve shown in Fig. 2-5. Therefore, it indicates that above parameters are appropriate for the CCM operation.

According to (2.2) and (2.5), we obtain the theoretical output voltage value V_o and inductor current value I_{L1} (average value), which are equal to $25V$ and $0A$ under the condition of $D=0.6$. The corresponding output voltage variation ratio ε is equal to $2.7e\text{-}4$ calculated by (2.8), and near-zero ripple is achieved.

The simulated startup traces (v_o and i_{L1}) under the zero initial condition are shown in Fig. 2-12(a), from which it can be seen that the startup process is quick and similar to other existing classical dc-dc converters. The simulated responses to the duty ratio step change from 0.6 to 0.75 and 0.4 are shown in Fig. 2-12(b) and (c), respectively. Although the transient processes are different in Fig. 2-12(b) and (c) due to the inner energy

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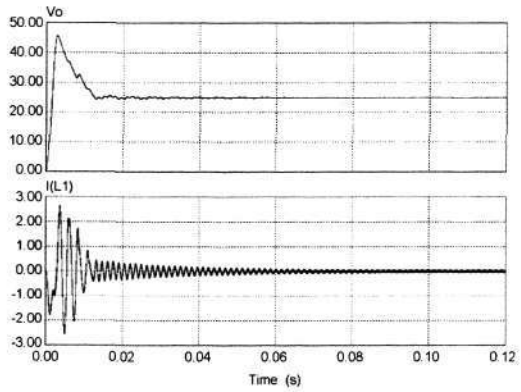
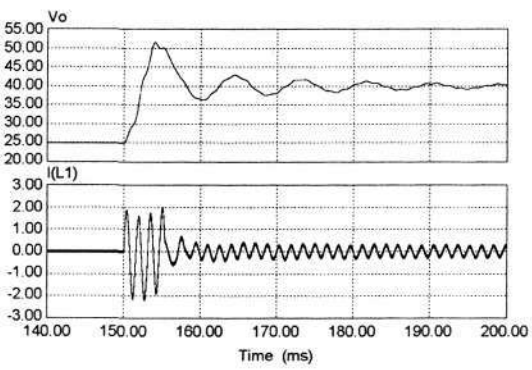
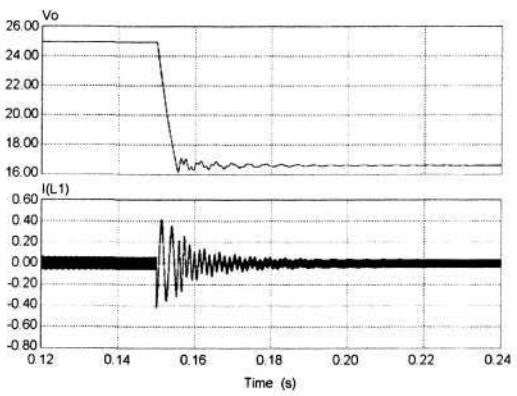
exchanging, both of the corresponding large-signal models are very close to 2nd order models. The steady-state performance in all simulation cases is identically matching the theoretical analysis.



(a)



(b)



(c)

Fig. 2-12. Simulation results of the self-lift circuit in CCM

(a) simulated startup traces under zero initial conditions
(b) simulated response to the duty ratio step change from *0.6* to *0.75*
(c) simulated response to the duty ratio step change from *0.6* to *0.4*

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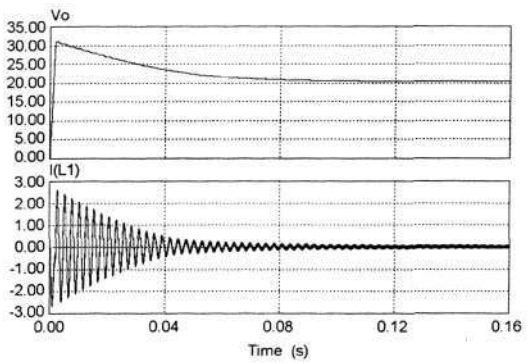
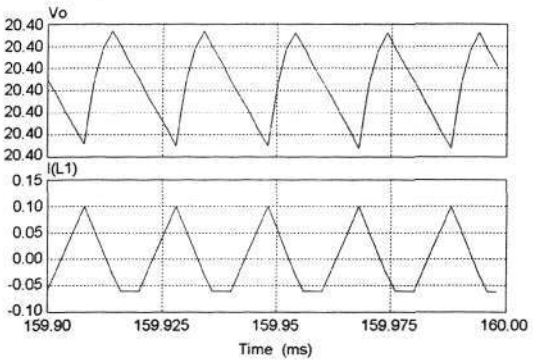
It is seen from Fig. 2-12(b) that there exists some low frequency ripples in i_{L1} (source current) after D is changed. This is a common phenomenon in dc-dc converters, because low frequency ripples are very easy introduced into source current when D and load are changed. This phenomenon can be eliminated by current-mode controllers.

2.6.2 Simulation verification of the self-lift circuit in DCM



(a)



(b)

Fig. 2-13. Simulation results of the self-lift circuit in DCM

(a) simulated startup traces under zero initial conditions
(b) Steady-state waveforms of (a)

On the basis of the simulation case given in Chapter 2.6.1, we let: $R=500\Omega$, $D=0.4$ and $f=50k$Hz. Z_N in this case is thus equal to 20 and located at the right DCM region of the boundary curve shown in Fig. 2-5. Therefore, under the interaction caused by R, L_1, D and f, the converter enters the DCM operation. The simulated startup traces (v_o and i_{L1}) under zero initial conditions are shown in Fig. 2-13(a), and the corresponding steady-state waveforms are shown in Fig.2-13(b). It can be measured from Fig. 2-13(b) that k is nearly equal to 0.66, and V_o is equal to 20.4V.

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Substituting $k=0.66$ to (2.16), we can obtain that the theoretical $V_o=20.13$V, which shows that the theoretical analysis results in DCM also have a good agreement with the simulation results.

2.6.3 Experimental results of the self-lift circuit

In the hardware testing circuit, we still choose the same parameters in Chapter 2.6.1. The n-channel MOSFET 2SK2267 is selected as the active power switch S. The drain-source on resistance is $8m\Omega$, which is near the ideal condition. All the diodes are realized by using MBR6045WT, the forward voltage drop of $0.6V$. Thus, the circuit will work in CCM, and the practical output voltage is smaller than the theoretical value due to the effects caused by parasitic parameters. Under the condition of $D=0.6$, the corresponding steady-state experimental curves are shown in Fig. 2-14(a). After careful measurement, we obtained $V_o=23.6V$ (shown in Channel 1with 10V/Div) and $V_{Cs}=9.9V$ (shown in Channel 2 with10V/Div), from which it is seen that the measured results are close to the theoretical analysis and simulation results.

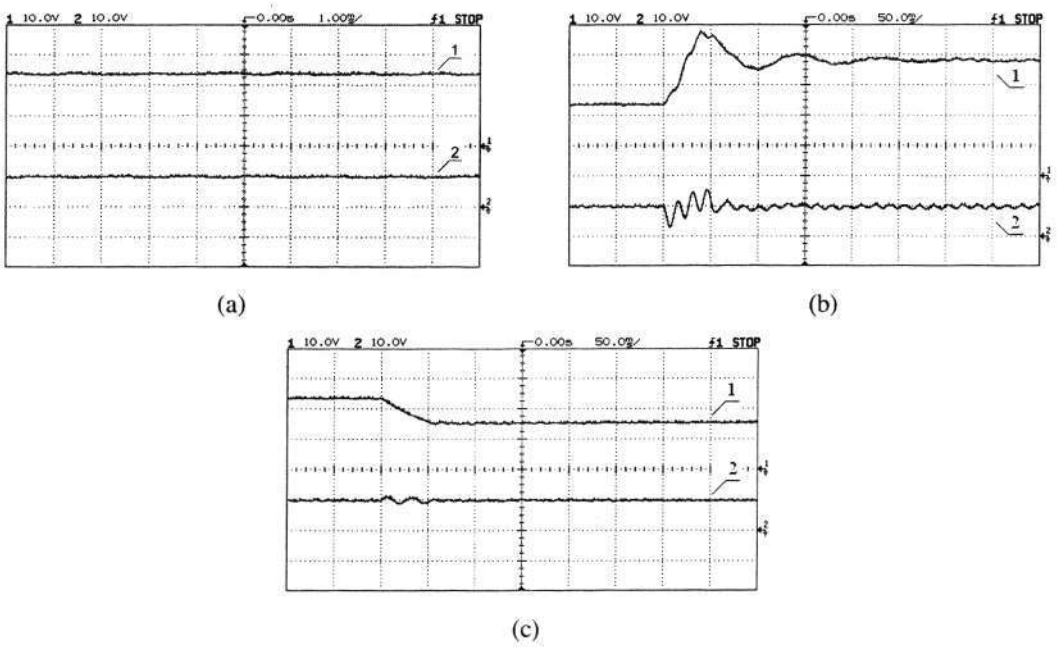

Fig. 2-14. Experimental results of the self-lift circuit case

(a) experimental results of steady-state performance
(b) experimental results of the duty ratio step change from 0.6 to 0.75
(c) experimental results of the duty ratio step change from 0.6 to 0.4

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Additionally, the experimental results of the duty ratio step change from *0.6* to *0.75* is shown in Fig. 2-14(b), and the experimental results of the duty ratio step change from *0.6* to *0.4* is shown in Fig. 2-14(c). The oscillation of v_{Cs} decays in a short time, and a fast constant voltage recovery is made. The open-loop transient processes are quick in only few milliseconds. The converter reaches the new steady state which has a good agreement with the simulation results as shown in 2-13(b) and (c).

2.6.4 Simulation verification of the re-lift circuit in CCM

The circuit parameters for simulation are: $V_{in}=10V$, $R=100\Omega$, $L=1mH$, $L_1=L_2=500\mu H$, $C_s=110\mu F$, $C_1=C_2=22\mu F$, $C_o=110\mu F$ and $D=0.6/0.75/0.4$. The other assumptions are the same with the above-mentioned self-lift circuit simulation case. Analogously, we use (2.28) and get the boundary values of normalized load, $Z_{N-B}\big|_{D=0.6/0.75/0.4}=41.7/85.3/27.7$. The normalized load Z_N in this case is equal to *2* and located at the left CCM region of the boundary curve shown in Fig. 2-9. Therefore, it indicates that above parameters are appropriate for the CCM operation.

According to (2.17), (2.20) and (2.21), we obtain the theoretical values of V_o, I_{L2} and I_{L1}, which are equal to *50V*, *1.25A* and *-1.25A* under the condition of $D=0.6$. The corresponding output voltage variation ratio ε is equal to *2.7e-4* calculated by (2.26), which is same with that of case 1. So near-zero ripple is achieved.

The simulated startup traces (v_o i_{L1} and i_{L2}) under zero initial conditions are shown in Fig. 2-15(a), from which it can be seen that the startup process is very quick and similar to other existing classical dc-dc converters. The steady-state performance (curve 1: i_{L1}; curve 2: i_{L2}) in the simulation is identically matching to the theoretical analysis. It is noted that the reference positive direction of i_{L1} in the simulation is the same with that in Fig. 2-6, so the simulation curve i_{L1} in the steady state is below the zero axis and symmetrical with respect to i_{L2}. The simulated responses to the duty ratio step change from *0.6* to *0.75* and *0.4* are shown in Fig. 2-15(b) and (c), respectively. Both of the corresponding large-signal models are close to 2nd order models, which is similar to the self-lift circuit case.

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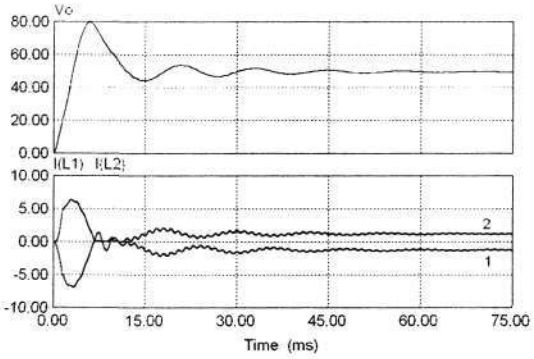
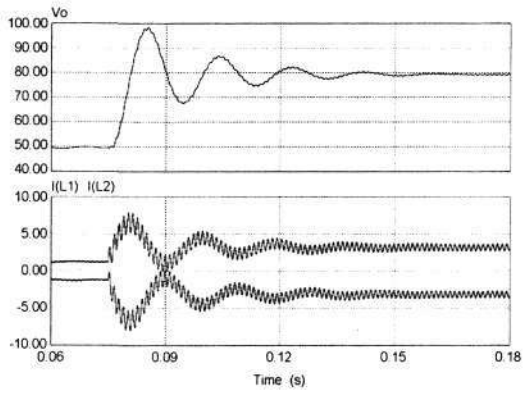


(a)



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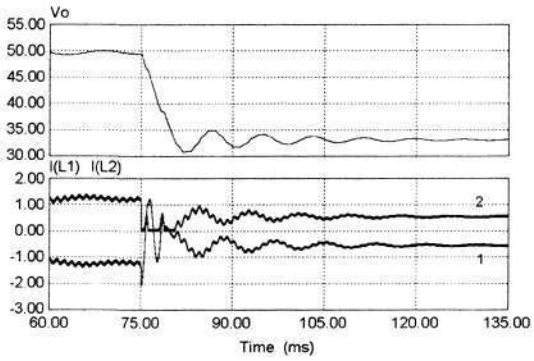

(c)

Fig. 2-15. Simulation results of the re-lift circuit in CCM

(a) simulated startup traces under zero initial conditions
(b) simulated response to the duty ratio step change from *0.6* to *0.75*
(c) simulated response to the duty ratio step change from *0.6* to *0.4*

2.6.5 Simulation verification of the re-lift circuit in DCM

On the basis of the simulation parameters given in 2.6.4, we let: $R=1000\Omega$, $D=0.4$ and $f=50k$Hz. Z_N in this case is thus equal to *40* and located at the right DCM region of the

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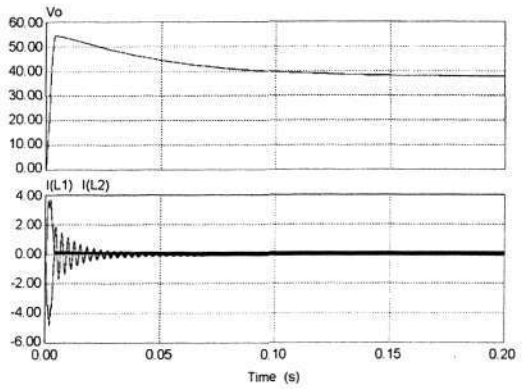
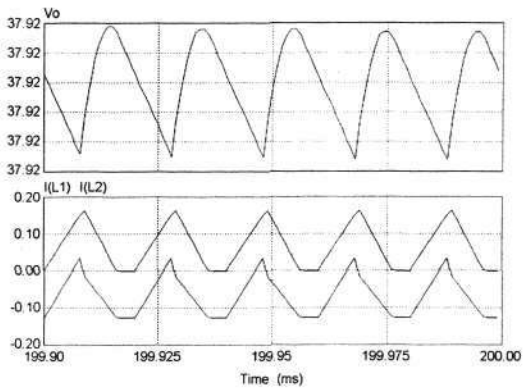
boundary curve shown in Fig. 2-5. Therefore, the circuit will work in DCM. According to (2.33), we can calculate the theoretical value of V_o, which is equal to *37.2*V.

To verify the theoretical calculation, the simulated startup traces (v_o and i_{L1}) under zero initial conditions are shown in Fig. 2-16(a), and the corresponding steady-state waveforms are shown in Fig.2-16(b). V_o is carefully measured and equal to *37.92*V, which has a good agreement with the theoretical analysis.



(a)



(b)

Fig. 2-16. Simulation results of the re-lift circuit in DCM

(a) simulated startup traces under zero initial conditions
(b) Steady-state waveforms of (a)

2.6.6 Experimental results of the re-lift circuit

The same parameters in Chapter 2.6.4 are chosen to construct a testing hardware circuit. Two n-channel MOSFETs are selected. All diodes and MOSFETS are the same with those adopted in the self-lift circuit. The circuit will work in CCM. Under the

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condition of $D=0.6$, the corresponding steady-state experimental curves are shown in Fig. 2-17(a). We obtained $V_o=46.2V$ (shown in Channel 1 with 10V/Div) and $V_{Cs}= 9.9V$ (shown in Channel 2 with 10V/Div) from which it is seen that the measured results are close to the theoretical analysis and simulation results. The output voltage drop might be caused by many reasons, mainly including the parasitic parameters, circuit board conditions, etc.

Additionally, the experimental results of the duty ratio step change from *0.6* to *0.75* is shown in Fig. 2-17(b), The oscillation of v_{Cs} decays in a short time, and a fast constant voltage recovery is made. The open-loop transient processes are quick in only few milliseconds. The converter reaches the new steady state, and a significant voltage degradation can be found. Considering the parasitic parameters and high values of D, the experimental results are acceptable. The experimental results of the duty ratio step change from *0.6* to *0.4* is shown in Fig. 2-17(c), in which the new steady state has a good agreement with the simulation results as shown in Fig. 2-15(c).

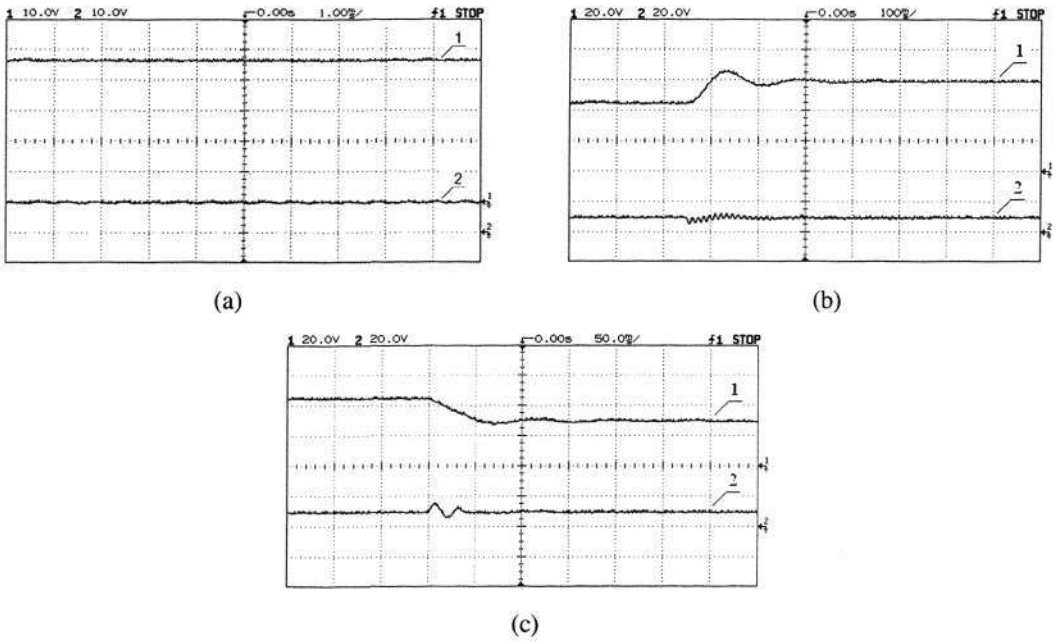

Fig. 2-17. Experimental results of the re-lift circuit case

(a) Experimental results of steady-state performance
(b) Experimental results of the duty ratio step change from *0.6* to *0.75*
(c) Experimental results of the duty ratio step change from *0.6* to *0.4*

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Chapter 3 Negative Output VL-type Cûk Converters

In Chapter 2, a series of positive output dc-dc converters have been introduced. This chapter will introduce a series of negative output dc-dc converters (VL-type Cûk converters) applying series Cûk implementing VL techniques. Compared with the Cûk converter prototype, these converters can perform positive to negative dc-dc voltage conversion with higher voltage transfer gains. Similar to the positive output VL-type SEPIC converters introduced in Chapter 2, all circuits proposed in this chapter are totally different from other existing dc-dc step-up converters. The main advantages, mainly including fewer switches, transformerless structures, clear conversion processes and high output voltages, will be analyzed in detail.

3.1 Introduction

The classical Cûk converter [58-60] shown in Fig. 3-1 has many industrial applications due to its good characteristics. This topology provides an output voltage with an opposite polarity to its input voltage. L and L_1 reduce EMI, and output voltage ripple is small. Under the different conditions of duty ratio D, it can perform the step-down and step-up dc-dc conversion due to its voltage transfer function as:

$$M_{Cûk} = -\frac{D}{1-D} = -M_{SEPIC} \tag{3.1}$$

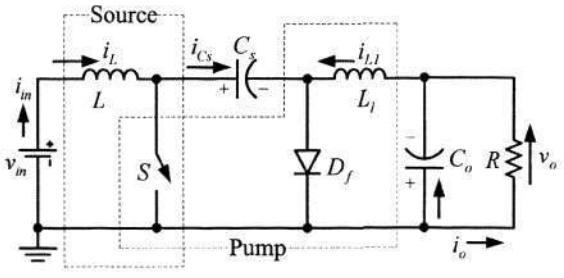

Fig. 3-1. Prototype of the Cûk converter

From (3.1), it is seen that the both the Cûk converter and the SEPIC converter are faced with the same difficulty of low voltage boost ability. Furthermore, because the

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classical Cûk converter is protected as an international patent, its practical applications have been seriously limited in present. Therefore, it is necessary to develop new topologies on the basis Cûk prototype for obtaining high voltage boost ability.

As introduced in Chapter 2, the VL technique has the potential to improve the performance of some classical dc-dc converters. In [3], F.L. Luo proposed a Cûk-based self-lift circuit integrating the VL technique, and it is termed *the self-lift Cûk converter*. As shown in Fig. 3-2, the self-lift Cûk converter is derived from the Cûk prototype by adding two components (diode D_1 and capacitor C_1) into the pump section. When S turns on, D_1 is on, and D_f is off. When S turns off, D_1 is off, and D_f is on. C_1 performs characteristics to lift the output capacitor voltage V_{Co} by the capacitor voltage V_{Cs}. Furthermore, a Π-type low-pass filter C_1-L_1-C_o is constructed and combined with the pump section. The voltage boost ability is thus increased from $-D/(1-D)$ to $-1/(1-D)$.

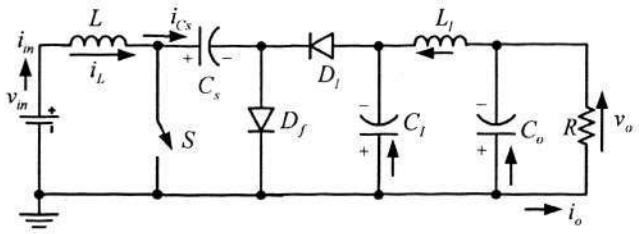

Fig. 3-2. Topology of the self-lift Cûk circuit (i.e. Elementary self-lift circuit)

In this chapter, the VL technique is applied to the Cûk prototype and the self-lift Cûk converter, and a new series Cûk implementing VL technique is developed. Consequently, a series of novel *negative output VL-type Cûk converters* have been created. Similar to Chapter 2, the self-lift Cûk converter in Fig. 3-2 is included into the proposed series as the elementary circuit. And consequently, *negative output VL-type Cûk converters* can be categorized into:

- elementary self-lift circuit (i.e. self-lift Cûk converter [3])
- developed self-lift circuit
- re-lift circuit
- multiple circuits (e.g. triple-lift and quadruple-lift circuit).

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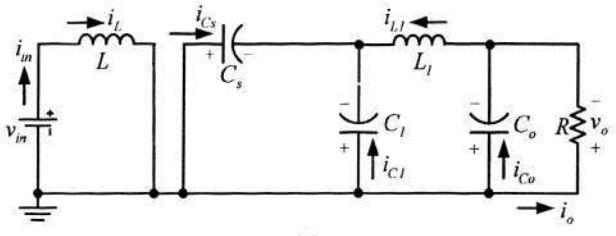
All above circuits are different from any other existing negative output dc-dc converters. They are featured with higher voltage transfer gains in simple structures. The detailed analysis will be performed in the following sections.

3.2 Elementary Self-Lift Circuit

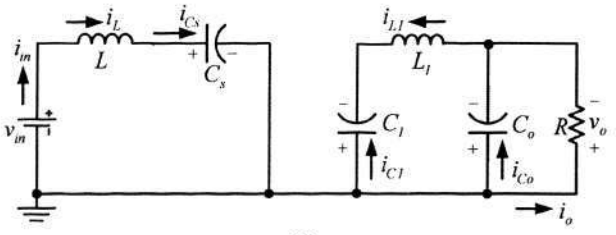
At present, the problems existing in the study of this circuit are the same to those of the self-lift SEPIC converter, and analysis results in [3] on this circuit is not enough and need to be reexamined. The detailed reasons are the same to those mentioned in Chapter 2.2, which are summarized again as follows:

- The results on DCM are not precise due to simplified calculation.
- Parameter "current filling efficiency" was proposed, but its usage during calculation is not correct.
- The voltage and current characteristics of each component have not been provided.

Therefore, a detailed circuit analysis is to be performed here. The equivalent circuits during switching-on, -off and DCM are shown in Fig. 3-3(a-c), respectively. Switching diagrams with main steady-state waveforms are shown in Fig. 3-4 to analyze the circuit operation, where reference directions are referred to in Fig. 3-2.



(a)



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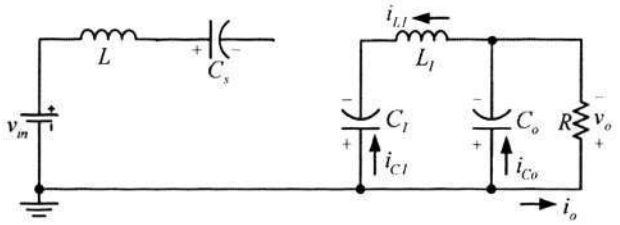

(c)

Fig. 3-3. Equivalent circuits of the elementary self-lift Cûk circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

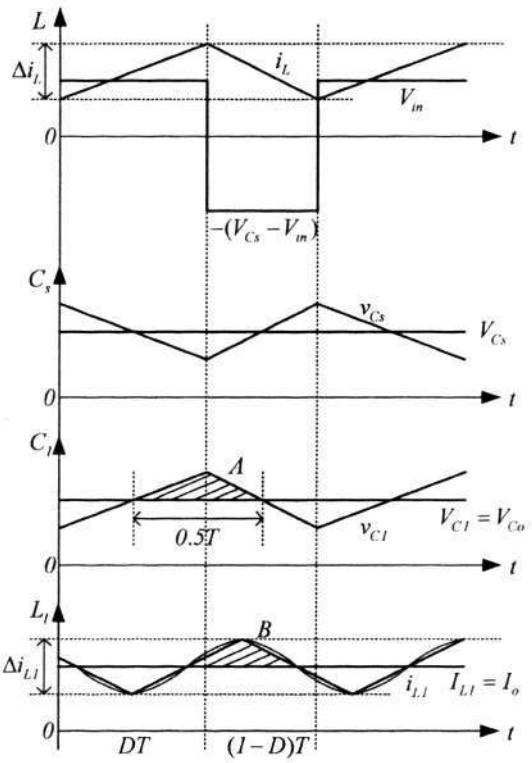

Fig. 3-4. Elementary self-lift circuit: waveforms with enlarged variations

3.2.1 Circuit analysis in CCM

In the steady state, the average voltage across L_1 over a period is zero. Thus

$$V_{C1}=V_{Co}=V_o$$

During the switch-on period, V_{C1} is equal to the voltage across C_s. Since C_s and C_1 are sufficiently large, we have:

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$$V_{Cs} = V_{C1} = V_o$$

The inductor current i_L increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{in} and $-(V_{Cs} - V_{in})$. Therefore, applying the inductor volt-second balance principle to L, we have:

$$DTV_{in} = (1-D)T(V_{Cs} - V_{in}) \text{ or } DTV_{in} = (1-D)T(V_o - V_{in})$$

Hence

$$V_o = \frac{1}{1-D} V_{in}$$

The voltage transfer gain in CCM is

$$M_S = \frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{3.2}$$

Therefore the input current is

$$I_{in} = \frac{1}{1-D} I_o = I_L = I_{Df-off} \tag{3.3}$$

Capacitor C_o acts as a lowpass filter so that

$$I_{L1} = I_o \tag{3.4}$$

Since the peak-to-peak current variation of $i_L, \Delta i_L$ is equal to DTV_{in}/L, the variation ratio of i_L is

$$\varsigma_L = \frac{\Delta i_L / 2}{I_L} = \frac{D}{2M_S^2} \frac{R}{fL} \tag{3.5}$$

The peak-to-peak voltage variation ratio of $v_{C1}, \Delta v_{C1}$ is approximate to

$$\Delta v_{C1} = \frac{I_o(1-D)T}{C_1}$$

Therefore, the variation ratio of v_{C1} is

$$\varepsilon_{C1} = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{1}{2M_S fRC_1} \tag{3.6}$$

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Because v_o varies very little, the peak-to-peak current variation of i_{L1} can be calculated by the area A of a triangle with width $T/2$ and the height $\Delta v_{C1}/2$, which is approximately

$$\Delta i_{L1} = \frac{\frac{1}{2}\frac{\Delta V_{C1}}{2}\frac{T}{2}}{L_1} = \frac{(1-D)I_o}{8f^2 L_1 C_1}$$

Therefore, the variation ratio of i_{L1} is approximate to

$$\varsigma_{L1} = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{1}{16 M_s f^2 L_1 C_1} \tag{3.7}$$

The variation of i_{Df} is equal to Δi_L during switching-off, so the variation ratio of i_{Df} is

$$\xi_{Df} = \varsigma_L = \frac{D}{2M_S^2}\frac{R}{fL} \tag{3.8}$$

To simplify the calculation, we treat the ripple waveform of i_{L1} as a triangle waveform as shown in Fig. 3-4 because the ripple of i_{L1} is very small. So the peak-to-peak voltage variation of v_o is calculated by the area B, which is approximately

$$\Delta v_o = \frac{\frac{1}{2}\frac{\Delta i_{L1}}{2}\frac{T}{2}}{C_o} = \frac{(1-D)I_o}{64 f^3 L_1 C_1 C_o}$$

Therefore, the variation ratio of v_o is approximate to

$$\varepsilon_S = \frac{\Delta v_o/2}{V_o} = \frac{1}{128 M_s f^3 L_1 C_1 C_o R} \tag{3.9}$$

3.2.2 Circuit Analysis in DCM

The elementary self-lift circuit operates in DCM if the current i_{Df} reduces to zero during switching-off. The condition for the DCM is $\xi_{Df} \geq 1$, i.e.

$$\xi_{Df} = \frac{D}{2M_S^2} Z_N \geq 1 \tag{3.10}$$

where Z_N is defined as the normalized load $R/(fL)$.

As a special case, when i_{Df} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary between CCM and DCM is obtained as below:

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$$Z_{N-B} = \frac{2M_S^2}{D} = \frac{2}{D(1-D)^2} \tag{3.11}$$

When $Z_N > Z_{N-B}$, the circuit operates in DCM. Under this condition i_{Df} decreases to zero at $t = t_1 = [D+m_S(1-D)]T$ where

$$DT < t_1 < T \text{ and } 0 < m_S < 1$$

Here, m_S is the current filling efficiency for the elementary self-lift circuit and defined as

$$m_S = \frac{t_1 - DT}{(1-D)T} \tag{3.12}$$

In DCM, i_L increases during switching-on and decreases during the period from DT to $m_S(1-D)T$. The corresponding voltages across L are V_{in} and $-(V_{Cs} - V_{in})$. Thus, utilizing the volt-second balance principle, we have

$$DTV_{in} = m_S(1-D)T(V_{Cs} - V_{in}) \text{ or}$$
$$DTV_{in} = m_S(1-D)T(V_o - V_{in}) \tag{3.13}$$

In addition, the transferred charges of L during switching-off are equal to $m_S(1-D)T\Delta i_L/2$, which compensate the total consumed charges of the load. So we have

$$I_o T = \frac{1}{2} m_S(1-D)T\Delta i_L \text{ or}$$
$$\frac{V_o}{R}T = \frac{1}{2} m_S(1-D)T\frac{DTV_{in}}{L} \tag{3.14}$$

Combining (3.13) and (3.14), we can obtain the filling efficiency of the elementary self-lift circuit as:

$$m_S = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{3.15}$$

From (3.13), we have

$$V_o = [1 + \frac{D}{m_S(1-D)}]V_{in} \tag{3.16}$$

Therefore, substituting (3.15) into (3.16) yields the voltage transfer gain in DCM as follows:

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$$M_{S-DCM} = \frac{1}{2}(1+\sqrt{1+2D^2 Z_N}) \tag{3.17}$$

Using (3.2), (3.11) and (3.17), we can obtain the boundary curve between CCM and DCM and voltage transfer gains versus the normalized load as shown in Fig. 3-5.

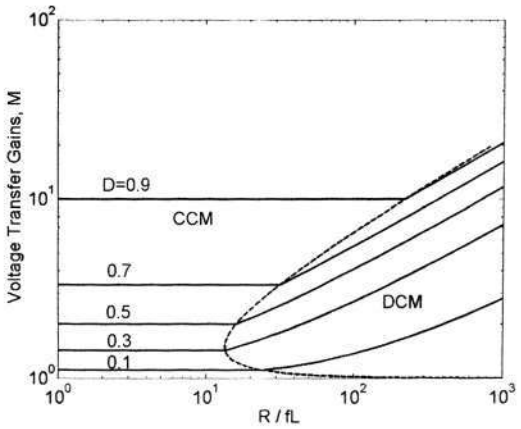

Fig. 3-5. Elementary self-lift circuit: boundary between CCM and DCM and voltage transfer gains against Z_N

3.3 Developed Self-Lift Circuit

The developed self-lift circuit is derived from the elementary self-lift circuit by adding the components (D_o-S_1) and redesigning the connection relations of L_1. The circuit diagram is shown in Fig. 3-6, and the subscript S'is used here to distinguish this topology from the elementary self-lift circuit. Static switches S and S_1 are switched simultaneously. The lift circuit consists of C_1-L_1-S_1-D_1, and it is a basic voltage lift cell. When S and S_1 turn on, D_1 is on, D_f and D_o are off. When S and S_1 turn off, D_1 is off, D_f and D_o are on. Capacitor C_1 performs its characteristics to lift the output capacitor voltage V_{Co} by the capacitor voltage V_{Cs}.

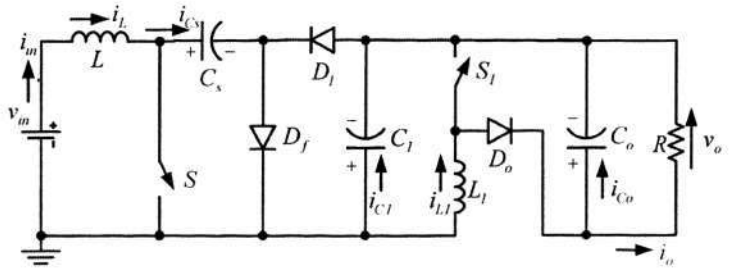

Fig. 3-6. Topology of the developed self-lift Cûk circuit

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The equivalent circuits during switching-on, switching-off and DCM are shown in Fig. 3-7(a-c), respectively. In the following sub-sections, the circuit is assumed operating in CCM.

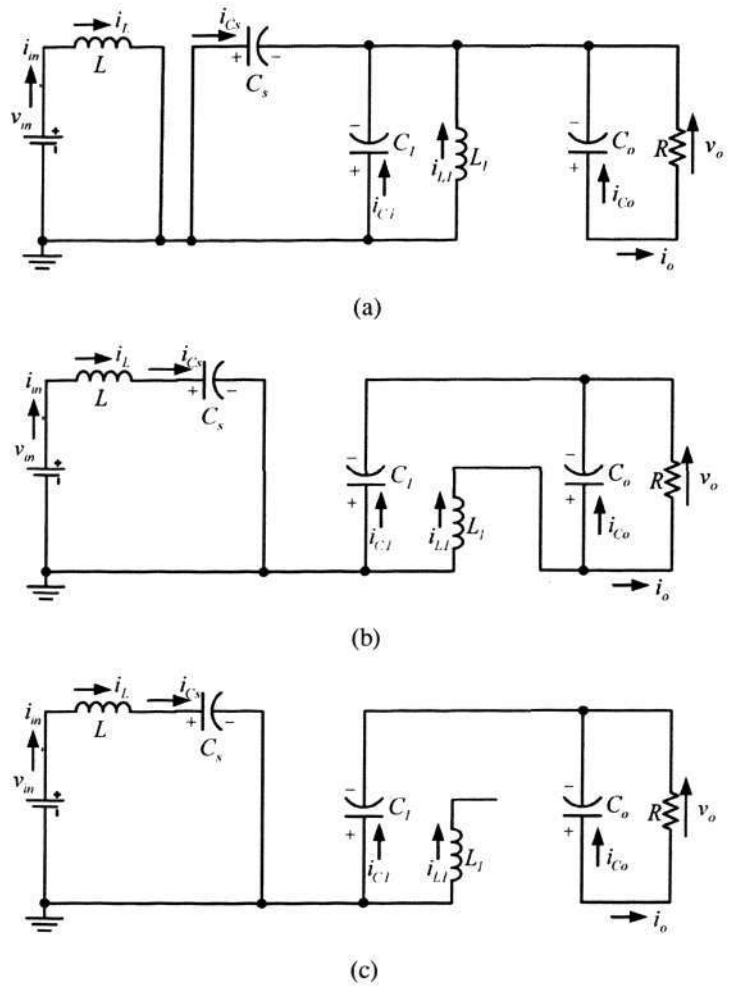

Fig. 3-7. Equivalent circuits of the developed self-lift Cûk circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

3.3.1 Circuit analysis in CCM

Switching diagrams with main steady-state waveforms are shown in Fig. 3-8 to analyze the circuit operation, where reference directions are referred to in Fig. 3-6.

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The inductor current i_L increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{in} and $-(V_{Cs}-V_{in})$, which is the same with the condition of the foregoing elementary self-lift circuit. Therefore, we get

$$V_{Cs}=\frac{1}{1-D}V_{in}$$

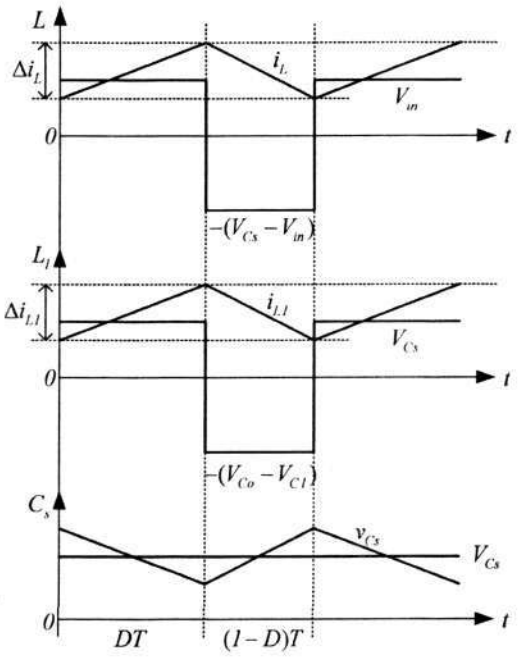

Fig. 3-8. Developed self-lift circuit: waveforms with enlarged variations

During switching-on, the voltage across C_1 is equal to V_{Cs}. Since C_s and C_1 are sufficiently large, we have:

$$V_{C1}=V_{Cs}=\frac{1}{1-D}V_{in}$$

The inductor current i_{L1} increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{Cs} and $-(V_{Co}-V_{C1})$. Therefore, with the sec-voltage balance principle, we have

$$DTV_{Cs}=(1-D)T(V_{Co}-V_{C1}) \text{ or } DTV_{Cs}=(1-D)T(V_o-V_{Cs})$$

Hence,

$$V_o=\frac{1}{(1-D)^2}V_{in}$$

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The voltage transfer gain in CCM is

$$M_{S'} = \frac{V_o}{V_{in}} = \frac{1}{(1-D)^2} \tag{3.18}$$

and the input current is

$$I_{in} = \frac{1}{(1-D)^2} I_o = I_L = I_{Cs-off} \tag{3.19}$$

The charges of C_o increase during switching-off and decrease during switching-on. We get:

$$Q_{Co+} = I_o DT$$
$$Q_{Co-} = I_{Co-off}(1-D)T$$

In a switching cycle, Q_{Co+}=Q_{Co-} Therefore,

$$I_{Co-off} = \frac{D}{1-D} I_o$$

During switching-off, i_{Do}=i_{Co}+i_o. Therefore,

$$I_{Do-off} = I_{Co-off} + I_o = \frac{1}{1-D} I_o \tag{3.20}$$

During switching-off, L_1 and C_1 form a path and transfer the stored energy through D_o. Therefore,

$$I_{L1} = I_{Do-off} = \frac{1}{1-D} I_o$$

Since the peak-to-peak current variation of $i_L, \Delta i_L$ is equal to DTV_{in}/L, the variation ratio of the current i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2(M_S')^2} \frac{R}{fL} \tag{3.21}$$

Since the peak-to-peak current variation of $i_{L1}, \Delta i_{L1}$ is equal to DTV_{Cs}/L_1, the variation ratio of the current i_{L1} is

$$\varsigma_{L1} = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{D}{2M_S'} \frac{R}{fL_1} \tag{3.22}$$

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The variation of the current i_{Do} during switching-off is equal to Δi_{L1}, and $I_{Do\text{-}off}$ is equal to I_{L1}. Therefore, the variation ratio of i_{Do} is

$$\xi_{Do} = \zeta_{L1} = \frac{D}{2M_{S'}} \frac{R}{fL_1} \tag{3.23}$$

The peak-to-peak voltage variation of v_o, Δv_o is equal to $I_o DT / C_o$. Therefore, the variation ratio of v_o is

$$\varepsilon_{S'} = \frac{\Delta v_o / 2}{V_o} = \frac{D}{2RC_o f} \tag{3.24}$$

3.3.2 Circuit analysis in DCM

The developed self-lift circuit operates in DCM if the current i_{Do} reduces to zero during switching-off. The condition for DCM is $\xi_{Do} \geq 1$, i.e.

$$\xi_{Do} = \frac{D}{2M_{S'}} Z_N \geq 1 \tag{3.25}$$

where Z_N is defined as the normalized load $R/(fL_1)$.

As a special case, when i_{Do} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore, the boundary between CCM and DCM is obtained as below:

$$Z_{N-B} = \frac{2M_{S'}}{D} = \frac{2}{D(1-D)^2} \tag{3.26}$$

When $Z_N > Z_{N\text{-}B}$, the circuit is operates in DCM. Under this condition i_{Do} decreases to zero at $t = t_1 = [D + m_{S'}(1-D)]T$ where

$$DT < t_1 < T \text{ and } 0 < m_{S'} < 1$$

Here, $m_{S'}$ is the current filling efficiency for the developed self-lift circuit, and its definition is the same to (3.12).

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In DCM, current i_{L1} increases during switching-on and decreases during the period from DT to $m_S(1-D)T$. The corresponding voltages across L_1 are V_{Cs} and $-(V_{Co}-V_{C1})$. Thus, using the volt-second balance principle, we have

$$DTV_{Cs} = m_{S'}(1-D)T(V_{Co}-V_{C1}) \text{ or}$$

$$DT\frac{1}{1-D}V_{in} = m_{S'}(1-D)T(V_o - \frac{1}{1-D}V_{in}) \tag{3.27}$$

Additionally, the transferred charges of L_1 during switching-off are equal to $m_S(1-D)T\Delta i_{L1}/2$, which compensate the total consumed charges of the load. So we have

$$I_oT = \frac{1}{2}m_{S'}(1-D)T\Delta i_{L1} \text{ or}$$

$$\frac{V_o}{R}T = \frac{1}{2}m_{S'}(1-D)T\frac{DT}{L_1}\frac{1}{1-D}V_{in} \tag{3.28}$$

Combining (3.28) and (3.29), we obtain

$$m_{S'} = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{3.29}$$

From (3.27), we have

$$V_o = [\frac{1}{1-D} + \frac{D}{m_{S'}(1-D)^2}]V_{in} \tag{3.30}$$

Therefore, substituting (3.29) into (3.30) yields the following voltage transfer gain in DCM:

$$M_{S'-DCM} = \frac{1+\sqrt{1+2D^2Z_N}}{2(1-D)} \tag{3.31}$$

Using (3.18), (3.26) and (3.31), we obtain the boundary curve between CCM and DCM. The voltage transfer gains versus the normalized load are thus shown in Fig. 3-9, which is beneficial for theoretical analysis and practical engineering design.

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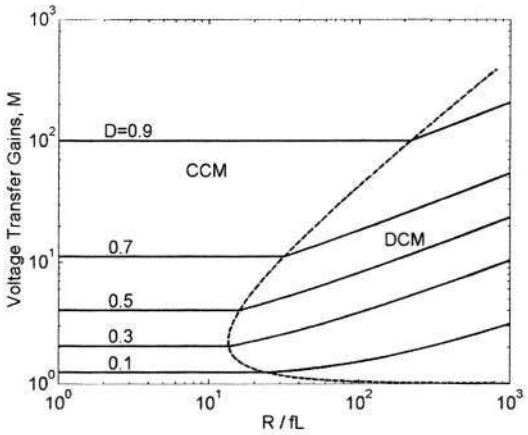

Fig. 3-9. Developed self-lift circuit: boundary between CCM and DCM and voltage transfer gains against Z_N

3.4 Re-Lift Circuit

The re-lift circuit shown in Fig. 3-10 is derived from the developed re-lift circuit by adding the components (D_2-C_2-D_3-L_2). The lift circuit consists of C_1-L_1-D_2-C_2- D_3-L_2 -S_1 and it can be divided into two basic voltage lift cells. When switches S and S_1 turn on, D_1, D_2 and D_3 are on, D_f and D_o are off. When S and S_1 turn off, D_1, D_2 and D_3 are off, D_f and D_o are on. Capacitors C_1 and C_2 perform characteristics to lift the output capacitor voltage V_{Co} by twice the capacitor voltage V_{Cs}. L_1 performs the function of a ladder joint to link the two capacitors C_1 and C_2 and lift V_{Co}.

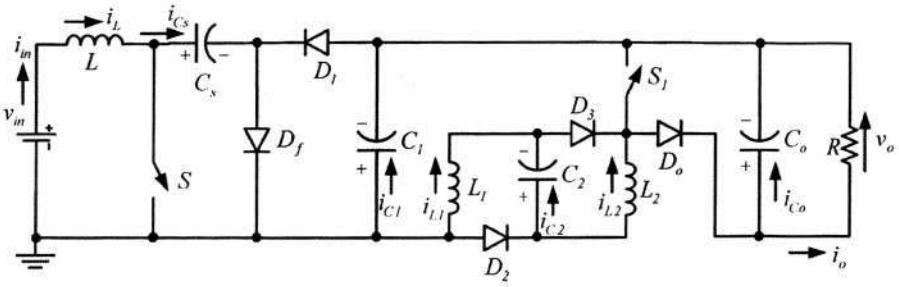

Fig. 3-10. Topology of the re-lift Cûk circuit

The equivalent circuits during switching-on, switching-off and DCM are shown in Fig. 3-11(a-c), respectively. In the following sub-sections, the circuit is assumed operating in CCM.

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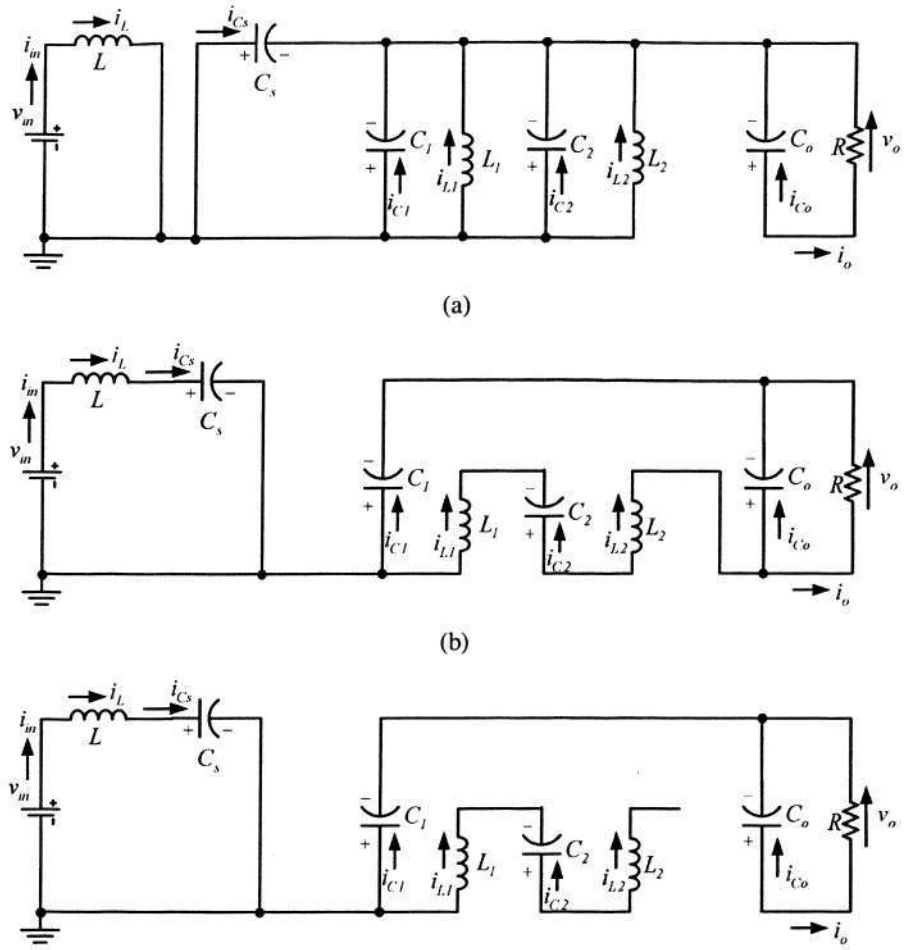

Fig. 3-11. Equivalent circuits of the re-lift Cûk circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

3.4.1 Circuit analysis in CCM

Switching diagrams with main steady-state waveforms are shown in Fig. 3-12 to analyze the circuit operation, where reference directions are referred to in Fig. 3-10.

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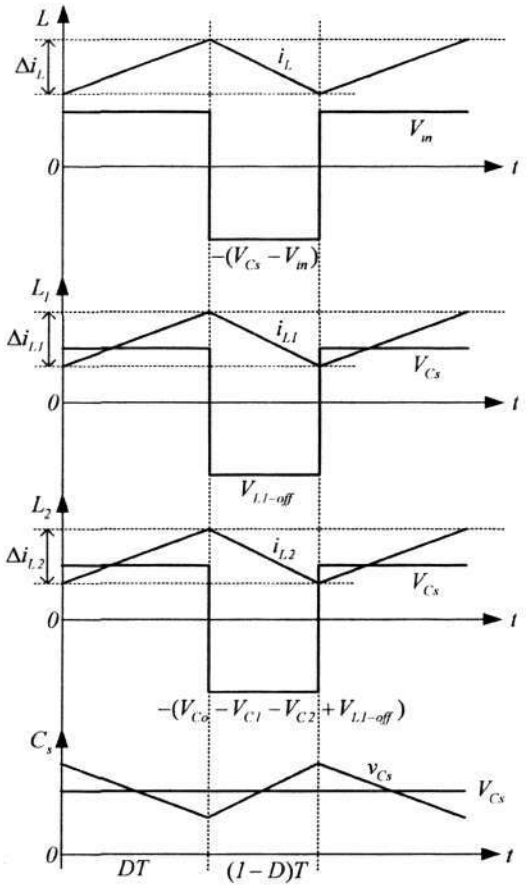

Fig. 3-12. Re-lift circuit: waveforms with enlarged variations

As is illustrated in the previous analysis, we get the same formula

$$V_{Cs} = \frac{1}{1-D} V_{in}$$

During switching-on, both the voltages across C_1 and C_2 are equal to V_{Cs}. Since C, C_1 and C_2 are sufficiently large, we have:

$$V_{C1} = V_{C2} = V_{Cs} = \frac{1}{1-D} V_{in}$$

The voltage across L_1 is equal to V_{Cs} during switching-on. With the volt-second balance principle, we get

$$V_{L1-off} = -\frac{D}{1-D} V_{Cs} = -\frac{D}{(1-D)^2} V_{in}$$

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The inductor current i_{L2} increases during switching-on and decreases during switching-off. The corresponding voltages across L_2 are V_{Cs} and $-(V_{Co}-V_{C1}-V_{C2}+V_{L1-off})$. Therefore, with the sec-voltage balance principle, we have

$$DTV_{Cs}=(1-D)T(V_{Co}-V_{C1}-V_{C2}+V_{L1-off}) \text{ or } DT\frac{1}{1-D}V_{in}=(1-D)T(V_o-\frac{2}{1-D}V_{in}+V_{L1-off})$$

Hence

$$V_o=\frac{2}{(1-D)^2}V_{in}$$

The voltage transfer gain in CCM is

$$M_R=\frac{V_o}{V_{in}}=\frac{2}{(1-D)^2} \tag{3.32}$$

and the input current is

$$I_{in}=\frac{2}{(1-D)^2}I_o=I_L=I_{Cs-off} \tag{3.33}$$

The charges of both C_o increase during switching-off and decrease during switching-on. Thus, we get:

$$Q_{Co+}=I_oDT$$
$$Q_{Co-}=I_{Co-off}(1-D)T$$

In a switching cycle, Q_{Co+}=Q_{Co-}. Therefore,

$$I_{Co-off}=\frac{D}{1-D}I_o$$

During switching-off, i_{Do}=i_{Co}+i_o. Therefore,

$$I_{Do-off}=I_{Co-off}+I_o=\frac{1}{1-D}I_o \tag{3.34}$$

During switching-off, C_1, L_1, C_2 and L_2 form a path and transfer the stored energy through D_o. Therefore,

$$I_{L1}=I_{L2}=I_{Do-off}=\frac{1}{1-D}I_o \tag{3.35}$$

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In a switching cycle, Δi_L is equal to DTV_{in}/L, therefore, the variation ratio of the current i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2M_R^2}\frac{R}{fL} \tag{3.36}$$

Analogously, Δi_{L1} and Δi_{L2} correspond to DTV_{Cs}/L_1 and DTV_{Cs}/L_2, respectively. Therefore, the variation ratios of i_{L1} and i_{L2} are

$$\varsigma_{L1} = \frac{\Delta i_{L1}/2}{I_{L1}} = \frac{D}{2M_R}\frac{R}{fL_1} \tag{3.37}$$

$$\varsigma_{L2} = \frac{\Delta i_{L2}/2}{I_{L2}} = \frac{D}{2M_R}\frac{R}{fL_2} \tag{3.38}$$

The variation of the current i_{Do} during switching-off is equal to Δi_{L2}, so the variation ratio of i_{Do} is

$$\xi_{Do} = \varsigma_{L2} = \frac{D}{2M_R}\frac{R}{fL_2} \tag{3.39}$$

The peak-to-peak voltage variation of v_o, Δv_o is equal to $I_o DT/C_o$. Therefore, the variation ratio of v_o is

$$\varepsilon_S = \frac{\Delta v_o/2}{V_o} = \frac{D}{2RC_o f} \tag{3.40}$$

Equations (3.37) and (3.38) indicate that inductor current variations during a switching cycle may be different due to the inductance difference. Because L_1 and L_2 are in series during switching-off, the same inductance is thus recommended in practical circuit design. In reality, although they will be slightly different, it will not affect the normal operation. This is because the practical inductor current variations (ripple) will be rather small under the high switching frequency and large inductance conditions.

3.4.2 Circuit analysis in DCM

From the foregoing explanation, it is assumed that L_1 and L_2 are the same, which can simplify the boundary analysis of CCM and DCM. The re-lift circuit operates in DCM if the current i_{Do} reduces to zero during switching-off. The condition for DCM is $\xi_{Do} \geq 1$, i.e.

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$$\xi_{Do} = \frac{D}{2M_R} Z_N \geq 1 \tag{3.41}$$

As a special case, when i_{Do} decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore the boundary between CCM and DCM is obtained as below:

$$Z_{N-B} = \frac{2M_R}{D} = \frac{4}{D(1-D)^2} \tag{3.42}$$

When $Z_N > Z_{N\text{-}B}$, the circuit is operates in DCM. Under this condition i_{Do} decreases to zero at $t = t_1 = [D+m_R(1\text{-}D)]T$ where

$$DT < t_1 < T \text{ and } 0 < m_R < 1$$

Here, m_R is the current filling efficiency for the re-lift circuit, and its definition is the same to (3.12).

In DCM, because current i_{L2} increases during switching-on and decreases during the period from DT to $(1\text{-}D)m_RT$, we thus have

$$V_{L2-off} = -\frac{D}{(1-D)m_R} V_{Cs}$$

Current i_{L1} increases during switching-on and decreases during the period from DT to $m_R(1-D)T$. The corresponding voltages across L_1 are V_{Cs} and $-(V_{Co} - V_{C1} - V_{C2} + V_{L2-off})$. Thus, using the volt-second balance principle, we have

$$DTV_{Cs} = (1-D)m_RT(V_{Co} - V_{C1} - V_{C2} + V_{L2-off}) \text{ or}$$

$$DTV_{Cs} = (1-D)m_RT[V_o - 2V_{Cs} - \frac{D}{(1-D)m_R} V_{Cs}] \tag{3. 43}$$

Additionally, the transferred charges of L_2 during switching-off are equal to $m_R(1-D)T\Delta i_{L2}/2$, which compensate the total consumed charges of the load. So we have

$$I_oT = \frac{1}{2} m_R(1-D)T\Delta i_{L2} \text{ or}$$

$$\frac{V_o}{R}T = \frac{1}{2} m_R(1-D)T \frac{DTV_{Cs}}{L_2} \tag{3.44}$$

Combining (3.43) and (3.44), we obtain

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$$m_R = \frac{2+2\sqrt{1+D^2 Z_N}}{D(1-D)Z_N} \tag{3.45}$$

From (3.43), we have:

$$V_o = [2+\frac{2D}{m_R(1-D)}]V_{Cs} \tag{3.46}$$

Therefore, substituting (3.45) into (3.46) yields the following voltage transfer gain in DCM:

$$M_{R-DCM} = \frac{1+\sqrt{1+D^2 Z_N}}{1-D} \tag{3.47}$$

Using (3.32), (3.42) and (3.47), we can obtain the boundary curve between CCM and DCM. The voltage transfer gains versus the normalized load are thus shown in Fig. 3-13, which is beneficial for theoretical analysis and practical engineering design.

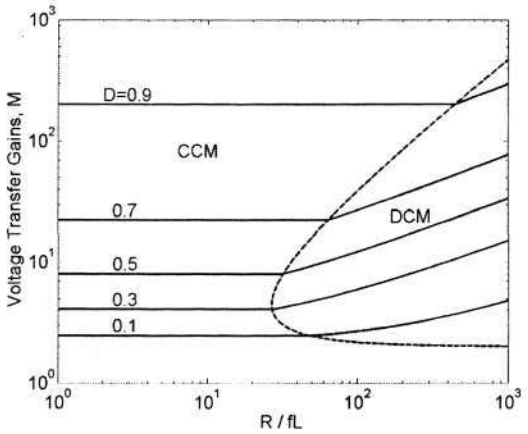

Fig. 3-13. Re-lift circuit: boundary between CCM and DCM and voltage transfer gains against Z_N

3.5 Multiple-Lift Circuit

3.5.1 General analysis

Referring to Fig. 3-10, it is possible to construct multiple-lift circuits by repeating adding the components (D_2-C_2-L_2-D_3). Assuming that there are n voltage lift cells, the

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generalized multiple-lift circuit is shown in Fig. 3-14 with reference directions. According to this principle, only two synchronous switches S and S_1 are required for each complex multiple-lift circuit, which simplify the control scheme and decrease the cost significantly. Hence, each circuit has two switches, $(n+1)$ inductors, $(n+2)$ capacitors and $(2n+1)$ diodes.

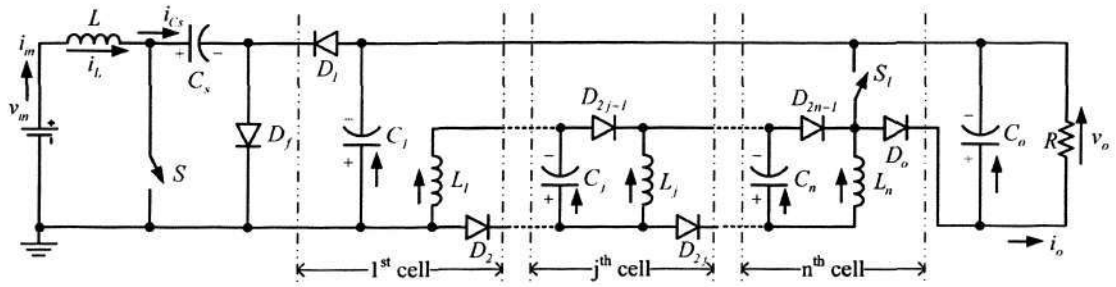

Fig. 3-14. Generalized representation of the multiple-lift circuit possessing n voltage-lift cells

When switches S and S_1 turn on, D_1, D_2,..., D_{2n-1} are on; D_f and D_o are off. When S and S_1 turn off, D_1, D_2,..., D_{2n-1} are off; D_f and D_o are on. Capacitors $C_1, C_2,\ldots,C_n$ lift V_{Co} by n times of V_{Cs}. Inductors L_1, L_2,... L_n perform the same function of a ladder joint to link the adjacent capacitors. From the foregoing analysis and calculation, the general formulas for all multiple-lift circuits can be obtained according to the similar steps.

The generalized voltage transfer gain is

$$M = \frac{n}{(1-D)^{h(n)}} \qquad n = 1,2,3,4,... \tag{3.48}$$

Where

$$h(n) = \begin{cases} 1 & elementary\ self-lift \\ 2 & others \end{cases}$$

The generalized current of L is

$$I_L = \frac{n}{(1-D)^{h(n)}} I_o \tag{3.49}$$

The generalized j^{th} inductor current is

$$I_{Lj} = \frac{1}{(1-D)^{h(n)-1}} I_o \tag{3.50}$$

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The following general analysis is for the developed self-lift circuit and its corresponding multiple-lift circuits. The generalized variation of the j^{th} inductor current i_{Lj} is

$$\varsigma_{Lj} = \frac{\Delta i_{Lj}/2}{I_{Lj}} = \frac{D}{2M}\frac{R}{fL_j} \tag{3.51}$$

Analogously, the generalized variation ratio of the output voltage v_o is

$$\varepsilon = \frac{\Delta v_o/2}{V_o} = \frac{D}{2RfC_o} \tag{3.52}$$

The generalized variation of the diode current i_{Do} is

$$\xi_{Do} = \frac{D}{2M}\frac{R}{fL_n} \tag{3.53}$$

It is assumed that all inductors existing in the voltage lift cells are the same. Therefore, the generalized boundaries between the CCM and DCM for all circuits are

$$Z_{N-B} = \frac{2M}{D} = \frac{2n}{D(1-D)^2} \tag{3.54}$$

The generalized current efficiency is

$$m = \frac{n+\sqrt{n^2+2nD^2Z_N}}{D(1-D)Z_N} \tag{3.55}$$

The generalized voltage transfer gain in DCM is

$$M_{DCM} = \frac{n+\sqrt{n^2+2nD^2Z_N}}{2(1-D)} \tag{3.56}$$

If the generalized circuit possesses three voltage lift cells, it is termed the triple-lift circuit. If the generalized circuit possesses four voltage lift cells, it is termed the quadruple-lift circuit. The main characteristics of these two multiple-lift circuits are given in Table 3-1 for ready reference.

Table 3-1 Main Characteristics of Proposed Multiple-lift Circuits

	Triple-Lift Circuit	Quadruple-Lift Circuit
M	$3/(1-D)^2$	$4/(1-D)^2$

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M_{DCM}	$(3+\sqrt{9+6D^2Z_N})/2(1-D)$	$2+\sqrt{4+2D^2Z_N})/(1-D)$
$Z_{N\text{-}B}$	$\frac{6}{D(1-D)^2}$	$\frac{8}{D(1-D)^2}$
m	$\frac{3+\sqrt{9+6D^2Z_N}}{D(1-D)Z_N}$	$\frac{4+2\sqrt{4+2D^2Z_N}}{D(1-D)Z_N}$
I_L	$[3/(1-D)^2]I_o$	$[4/(1-D)^2]I_o$
I_{Lj} $j=1...4$	$[1/(1-D)]I_o$	

The boundaries between CCM and DCM of all proposed circuits are shown in Fig. 3-15. The curves of all M versus Z_N indicate that the CCM area increases from the elementary self-lift circuit via the developed self-lift circuit, the re-lift circuit, the triple-lift circuit to the quadruple-lift circuit. There are minimum values of Z_N (*13.5, 13.5, 27, 40.5* and *54*) at the boundaries, and all of them are under the condition of D = *1/3*. It means that the condition of D = *1/3* is the most possible for these converters to enter DCM. The corresponding extreme points are also marked in Fig. 3-15 for ready reference.

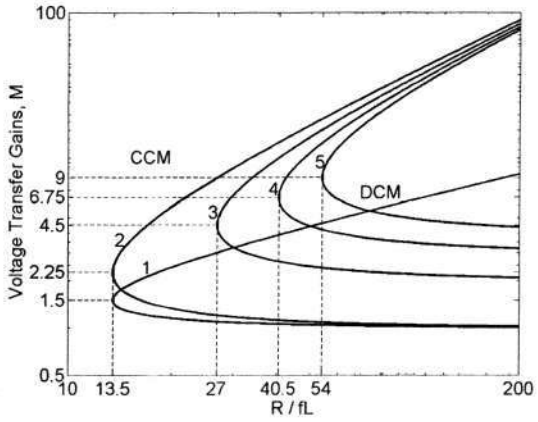

Fig. 3-15. Boundaries between CCM and DCM against the normalized load Z_N

(1: elementary self-lift circuit; 2: developed self-lift circuit; 3: re-lift circuit; 4: triple-lift circuit; 5: quadruple-lift circuit)

3.5.2 Steady-state performance summary

From the foregoing analysis, we can get an overview and main analytical results of proposed VL-type converters. Equation (3.52) indicates that the output voltage variation

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ratios are determined by the interactions caused by D, R, f and C_o. So increasing the capacitance of output capacitor can effectively decrease the ripple of output voltages.

In order to show the high voltage transfer gain characteristics of the proposed circuits over the conventional Cûk converter, voltage transfer gains V_o/V_{in} in duty ratio $D = 0.33$, 0.5, 0.75 and 0.8 are listed in Table 3-2.

Table 3-2 Comparison of five proposed converters with conventional Cûk converter

Topology		$M=V_o/V_{in}$			
		$D=0.33$	$D=0.5$	$D=0.75$	$D=0.8$
Conventional Cûk prototype		-0.5	-1	-3	-4
Proposed converters	Elementary self-lift circuit	-1.5	-2	-4	-5
	Developed self-lift circuit	-2.25	-4	-16	-25
	Re-lift circuit	-4.5	-8	32	-50
	Triple-lift circuit	-6.75	-12	-48	-75
	Quadruple-lift circuit	-9	-16	-64	-100

The data in Table 3-2 indicate all proposed converters can get higher voltage transfer gains compare with traditional topologies. Although traditional n-cell cascade connection converters (quadratic converters) and transformer-type converters can achieve high voltage transfer gains, their efficiency η remains low. This is because η of n-cell cascade connection converters given by the product of the efficiencies of each cell belonging to the cascade connection, i.e. $\eta = \eta_1\eta_2...\eta_n$. And η of transformer-type converters would be limited by additional losses caused by transformer magnetic characteristics. Since all proposed converters avoid these problems, compact structures with a good efficiency might be achieved in the practical manufacture.

For the circuit parameter selection, the general guidelines can be referred to the discussion in Chapter 2.5.

3.6 Simulation and Experimental Results

To verify the foregoing theoretical analysis results, Psim simulation package was applied to the proposed converters. All the diodes and the switch in simulation cases are

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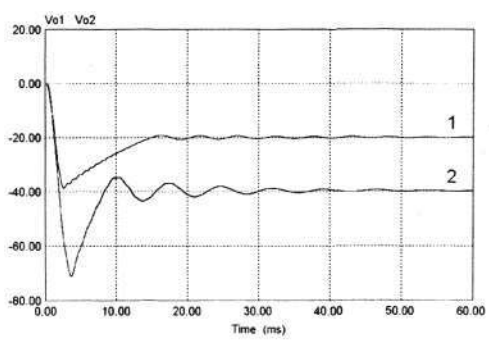
ideal. The corresponding hardware testing circuits were also constructed to compare with the simulation results.

3.6.1 Simulation verification of self-lift circuits in CCM

Referring to Fig. 3-2 and Fig. 3-6, both of these two circuits are under the same simulation condition that V_{in}=*10V*, R=*100Ω*, L=*1mH*, L_1=*500μH*, C_s=*110μF*, C_1=*22μF*, C_o=*47μF*, D=*0.5* and f=*100kHz*. Since simulation is to be performed in CCM, we use (3.11) and (3.26) to get the boundary value of normalized load, $Z_{N-B}|_{D=0.5}$. For these two cases, both $Z_{N-B}|_{D=0.5}$ are equal to *16*. Both the normalized load Z_N are equal to *2* and located at the left CCM region of their boundary curve. Therefore, it indicates that above parameters are appropriate for the CCM operation. According to (3.2) and (3.18), we obtain the theoretical output voltage values of V_o which are equal to *20V* (elementary) and *40V* (developed), respectively. From (3.9) and (3.24), the output voltage variation ratio ε_S and $\varepsilon_{S'}$ are equal to *7.5e-8* and *5.3e-4*, respectively. Therefore, near-zero ripple is achieved.

The simulated startup traces under zero initial conditions are shown in Fig. 3-16(a), from which it can be seen that the startup process is quick and similar to other existing classical dc-dc converter. It is noted that curves 1 and 2 correspond to v_o of the elementary self-lift circuit and the developed self-lift circuit, respectively. Additionally, the simulated responses to the duty ratio step change from *0.5* to *0.6* and *0.4* are shown in Fig. 3-16(b) and (c). The steady-state performance in all simulation cases is identically matching the theoretical analysis.



(a)

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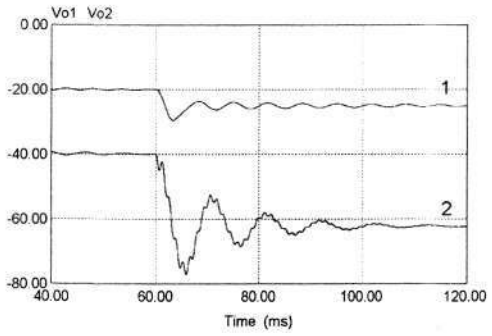
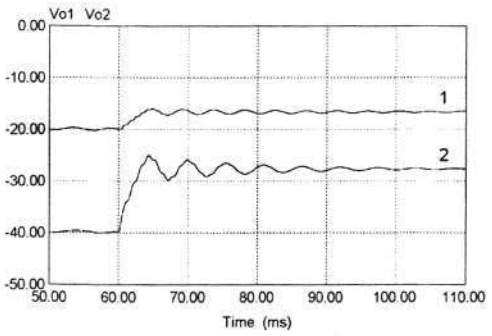


(b)



(c)

Fig. 3-16. Simulation results of the self-lift circuits in CCM

(a) simulated startup traces under zero initial conditions
(b) simulated response to the duty ratio step change from *0.5* to *0.6*
(c) Simulated response to the duty ratio step change from *0.5* to *0.4*

3.6.2 Simulation verification of self-lift circuits in DCM

To make the elementary self-lift circuit working under DCM, on the basis of the simulation parameters given in 3.6.1, we let: $R=1000\Omega$, $L=500\mu H$, $D=0.4$ and $f=50k$Hz. Z_N in this case is thus equal to *40* and located at the right DCM region of the boundary curve shown in Fig. 3-5. Therefore, the circuit will work in DCM. According to (3.17), we obtain that the theoretical value of V_o is equal to *23.58*V.

The simulated startup traces (v_o and i_L) under zero initial conditions are shown in Fig. 3-17(a), and the corresponding steady-state waveforms are shown in Fig.3-17(b). It is seen from Fig. 3-17 that the simulated value of V_o is about *23.62*V, which has a good agreement with the above theoretical analysis result.

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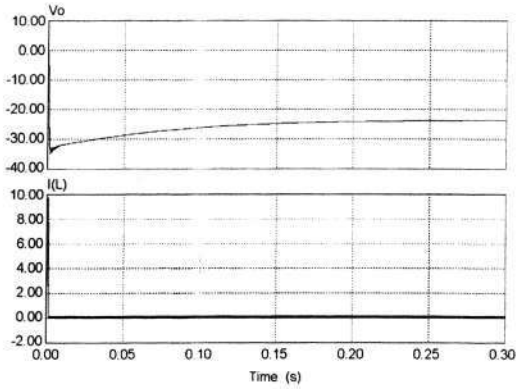
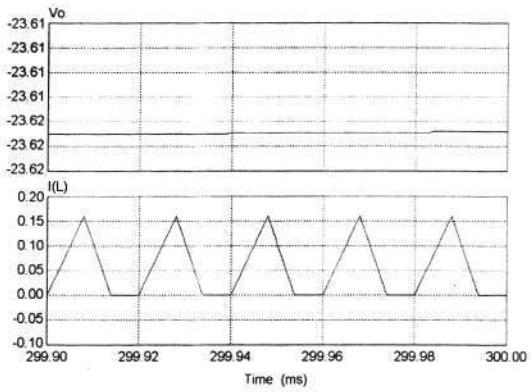


(a)



(b)

Fig. 3-17. Simulation results of the elementary self-lift circuit in DCM

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms of in (a)

Analogously, to make the developed self-lift circuit working under DCM, on the basis of the simulation parameters given in 3.6.1, we let: $R=1000\Omega$, $D=0.4$ and $f=50k$Hz. Z_N in this case is thus equal to *40* and located at the right DCM region of the boundary curve shown in Fig. 3-9. Therefore, the circuit will work in DCM. According to (3.31), we obtain that the theoretical value of V_o is equal to *39.3*V.

The simulated startup traces (v_o and i_{L1}) under zero initial conditions are shown in Fig. 3-18(a), and the corresponding steady-state waveforms are shown in Fig.3-18(b). It is seen from Fig. 3-18 that the simulated value of V_o is about *39.3*V, which has a good agreement with the above theoretical analysis result.

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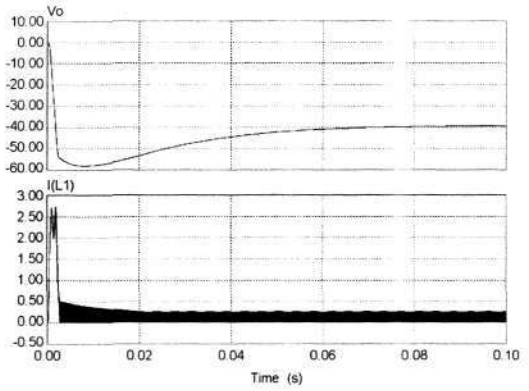
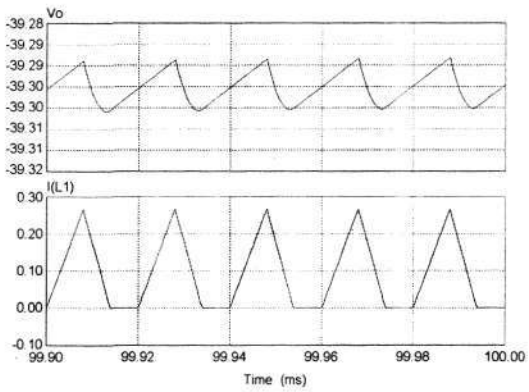


(a)



(b)

Fig. 3-18. Simulation results of the developed self-lift circuit in DCM

(a) simulated startup traces under zero initial conditions
(b) Steady-state waveforms of (a)

3.6.3 Experimental results of self-lift circuits (elementary and developed)

In the hardware testing circuits, we still choose the same parameters in Chapter 3.6.1. The n-channel MOSFET 2SK2267 is selected as the power switches *S*. The drain-source on resistance is $8m\Omega$, which is near the ideal condition. All the diodes are realized by using MBR6045WT, the forward voltage drop of *0.6V*. Thus, the practical output voltage is smaller than the theoretical value due to the effects caused by parasitic parameters. Under the condition of $D=0.5$, the corresponding steady-state experimental curves of the output voltages are shown in Fig. 3-19(a). After careful measurement, we obtained the practical output voltage value of the elementary self-lift circuit is about *19V* (shown in Channel 1 with 10V/Div), and the practical output voltage value of the developed self-lift

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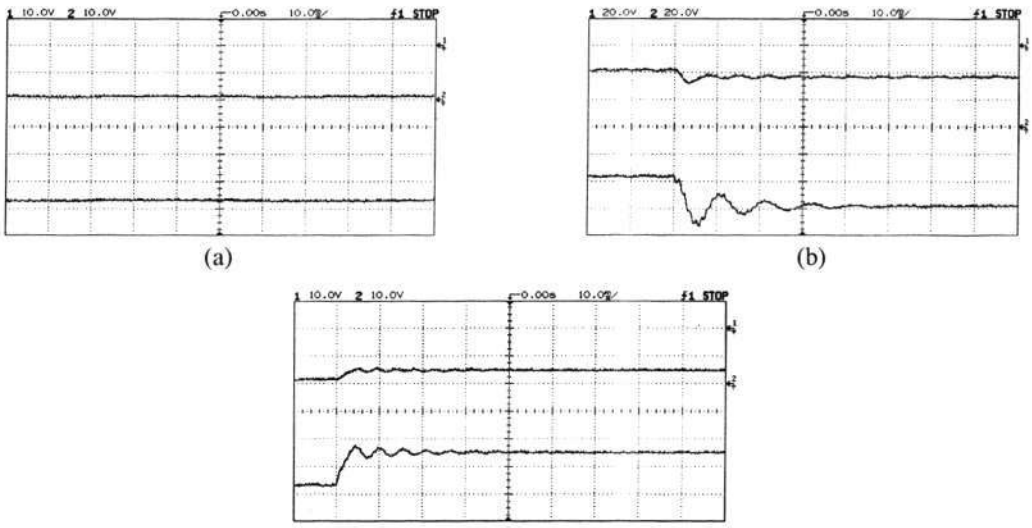
circuit is about *37V* (shown in Channel 2 with 10V/Div). It is seen that the measured results are very close to the theoretical analysis and simulation results.

Additionally, the experimental results of the duty ratio step change from *0.5* to *0.6* are shown in Fig. 3-19(b), and the experimental results of the duty ratio step change from *0.5* to *0.4* is shown in Fig. 3-19(c). The oscillation decays in a short time, and a fast constant voltage recovery is made. The open-loop transient processes are quick in only few milliseconds. Both of them reach their new steady states, which has a good agreement with the simulation results as shown in Fig. 3-16(b) and (c).



(a) (b)

(c)

Fig. 3-19. Experimental results of the self-lift circuits

(a) experimental results of steady-state performance
(b) experimental results of the duty ratio step change from *0.5* to *0.6*
(c) experimental results of the duty ratio step change from *0.5* to *0.4*

3.6.4 Simulation verification of the re-lift circuit in CCM

The circuit parameters for simulation are: $V_{in}=10V$, $R=100\Omega$, $L=1mH$, $L_1=L_2=500\mu H$, $C_s=110\mu F$, $C_1=C_2=22\mu F$, $C_o=110\mu F$ $D=0.5$ and $f=100kHz$. The other assumptions are the same with those for above-mentioned self-lift circuits. Analogously, we use (3.42) and get the boundary value of normalized load, $Z_{N-B}\big|_{D=0.5}=32$. The normalized load Z_N in this case is equal to 2 and located at the left CCM region of the boundary curve as shown in Fig. 3-13. Therefore, it indicates that above parameters are appropriate for the CCM operation. According to (3.32), we obtain the theoretical value of V_o, which is equal to

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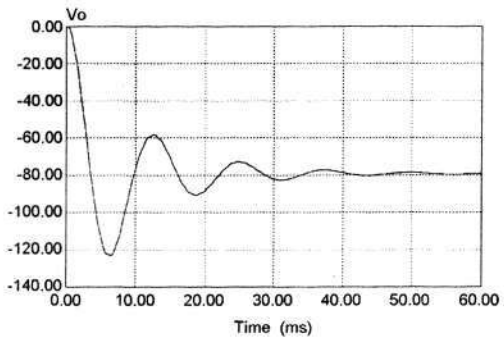
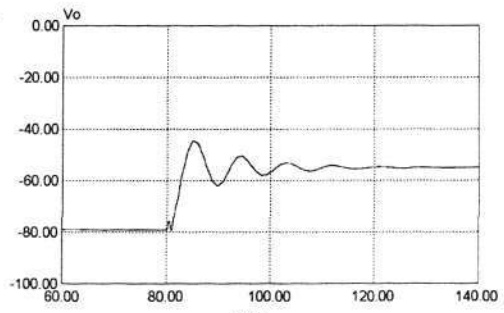
80V. Since the corresponding output voltage variation ratio ε is equal to *5.3e-4* calculated by (3.40), near-zero ripple is achieved.

The simulated startup trace of the output voltage under zero initial conditions is shown in Fig. 3-20(a), from which it can be seen that the startup process is quick and similar to other existing classical dc-dc converter. Additionally, the simulated responses to the duty ratio step change from *0.5* to *0.4* are shown in Fig. 3-20(b) and (c). The steady-state performance in the simulation is identically matching the theoretical analysis.



(a)



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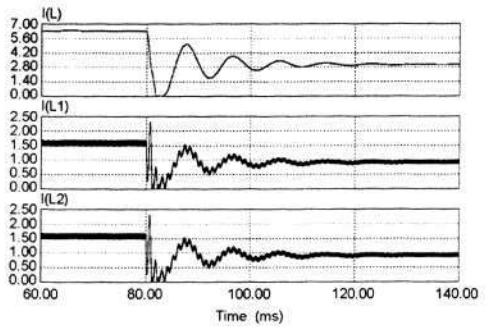

(c)

Fig. 3-20. Simulation and experimental results of the re-lift circuit case

(a) simulated startup traces under zero initial conditions
(b) simulated response to the duty ratio step change from *0.5* to *0.4* (output voltage)
(c) simulated response to the duty ratio step change from 0.5 to *0.4* (inductor currents)

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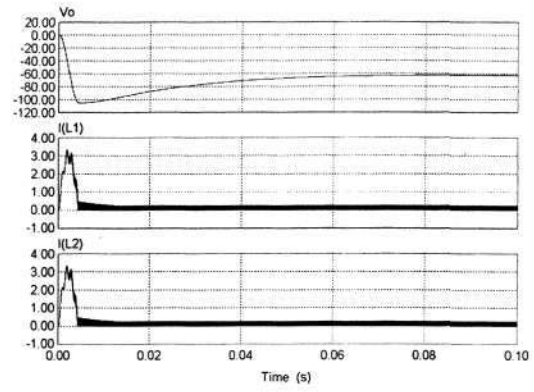
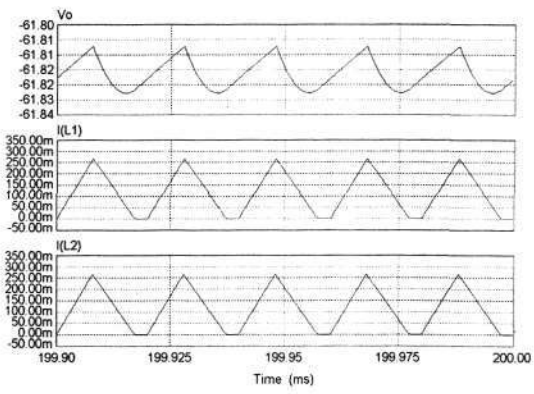
3.6.5 Simulation verification of the re-lift circuit in DCM

To make the elementary self-lift circuit working under DCM, on the basis of the simulation parameters given in 3.6.1, we let: $R=1000\Omega$, $D=0.4$ and $f=50k$Hz. Z_N in this case is thus equal to *40* and located at the right DCM region of the boundary curve shown in Fig. 3-13. Therefore, the circuit will work in DCM. According to (3.47), we obtain that the theoretical value of V_o is equal to -*62*V.

The simulated startup traces (v_o and i_L) under zero initial conditions are shown in Fig. 3-21(a), and the corresponding enlarged steady-state waveforms are shown in Fig.3-21(b). It is seen from Fig. 3-21 that the simulated value of V_o is about -*61.82*V, which has a good agreement with the above theoretical analysis result.



(a)



(b)

Fig. 3-21. Simulation results of the self-lift circuits in DCM

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms of (a)

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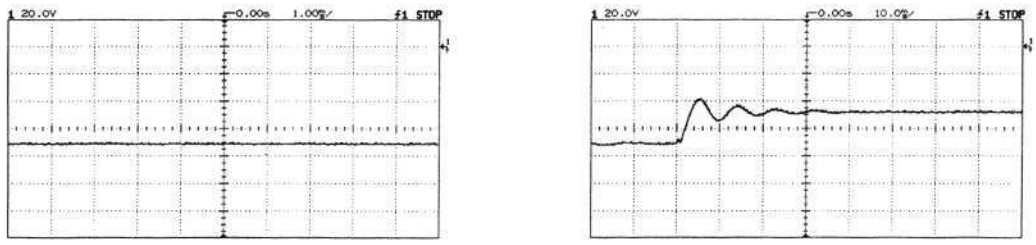
3.6.6 Experimental results of the re-lift circuit in DCM

The same parameters in Chapter 3.6.4 are chosen to construct a testing hardware circuit. Two n-channel MOSFETs are selected. All diodes and MOSFETS are the same with those adopted in the self-lift circuits. It is noted that v_{in} and v_o do not share the common ground. The corresponding v_o in the steady state is shown in Fig. 3-22(a). We obtained the practical average value of V_o=*72V* (shown in Channel 1 with 20V/Div). Considering the power losses, we see that the measured results are very close to the theoretical analysis and simulation results. Additionally, the experimental v_o curve of the duty ratio step change from *0.5* to *0.4* are shown in Fig. 3-22(b). The oscillation decays in a short time, and a fast constant voltage recovery is made. The open-loop transient process is quick in only few milliseconds, and it reach the new steady state which has a good agreement with the simulation results as shown in Fig. 3-20(b).



(a) (b)

Fig. 3-22. Simulation and experimental results of the re-lift circuit case

(a) experimental results of steady-state performance
(b) experimental results of the duty ratio step change from *0.5* to *0.4*

3.7 Exploration on Negative-to-Positive Voltage Conversion

From the foregoing statement, it is known that the classical Cûk converter, the buck-boost converter and all VL-type circuits above introduced are used to provide positive-to-negative voltage conversion paths. Negative-to-positive voltage conversion is another form of voltage polarity inversion. Sometimes, dc-dc converters that can perform the negative-to-positive voltage conversion play a vital role in industrial applications, especially in dc distributed power systems. As one type of power supply architectures widely used in automobiles, space stations and manufacture industries, the dc distributed

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power system sometimes needs a dc-dc converter to realize the polarity inversion for its negative dc voltage bus with respect to the common ground.

Through the foregoing analysis on the elementary self-lift circuit, it is found that this topology has the potential to be improved for obtaining the negative-to-positive voltage conversion ability. Therefore, a new circuit termed *enhanced self-lift circuit*, is proposed here, and its topology is shown in Fig. 3-23.

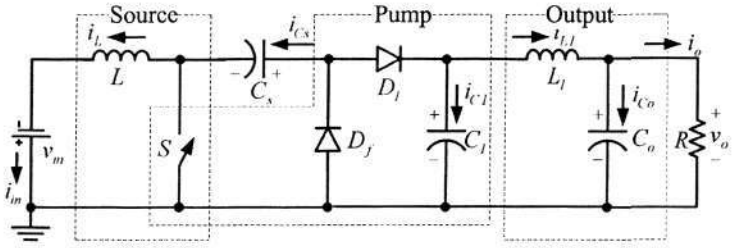

Fig. 3-23. Topology of the enhanced self-lift circuit

3.7.1 Enhanced Self-lift Circuit

The proposed enhance self-lift circuit is different from any other existing dc-dc step-up converters from the viewpoint of circuit topology. Compared with the elementary self-lift circuit as shown in Fig. 3-2, the polarities of D_1, D_f, C_1, C_o, C_s, V_{in} and S are changed; however, the relative positions of all components are kept invariant in the new circuit. Additionally, its voltage transfer gain is also equal to $-1/(1-D)$.

For the convenience of analysis, the whole circuit is divided into three different sections as described in Fig. 3-23. L_1 belongs to the Source section, and it performs the energy storing and transferring form the source voltage v_{in} to C_s under the switching operation of S. C_1, D_1 and D_f form a Pump section, in which C_1 is charged by C_s during each cycle and absorbs the energy stored in C_s like a pump. An Output section formed by L_1 and C_o is combined with the Pump section to perform the output filter function for the voltage of C_1.

The equivalent circuits during switching-on, switching-off and DCM are shown in Fig. 3-24(a-c), respectively. When S turns on, D_1 is on, and D_f is off. When S turns off, D_1 is off, and D_f is on. C_1 performs characteristics to lift the output capacitor voltage V_{Co} by the capacitor voltage V_{Cs}. Switching diagrams of main steady-state waveforms with enlarged

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variations are shown in Fig. 3-25 for the following circuit analysis, where reference directions are referred to in Fig. 3-23.

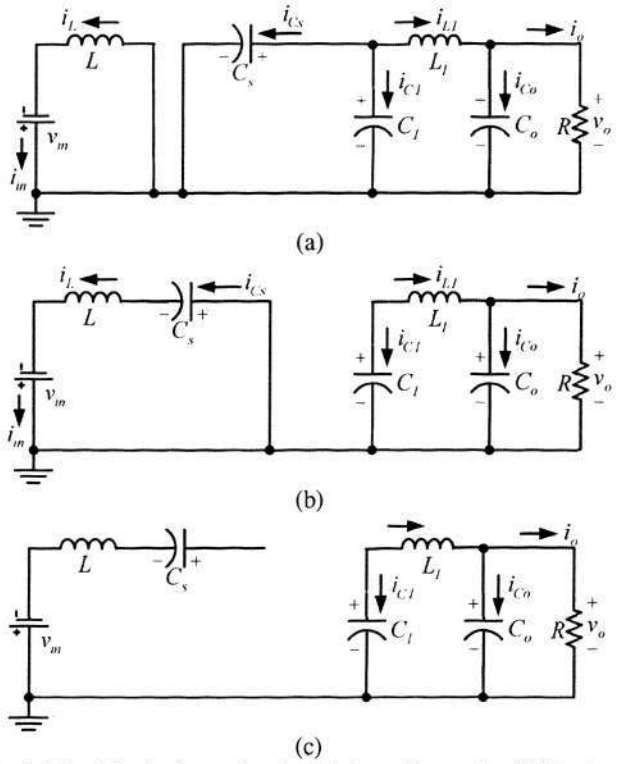

Fig. 3-24. Equivalent circuits of the enhanced self-lift circuit

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

3.7.2 Circuit Analysis in CCM and DCM

From Fig. 3-24, it is seen that the topology and equivalent circuits of the enhanced self-lift circuit are very close to those of the elementary self-lift circuit in Chapter 3.2, so the analysis procedure on the enhanced self-lift circuit can be referred to the content of Chapter 3.2. The detailed derivation process is thus omitted, and the main circuit characteristics are summarized as follows:

$$M_{CCM} = \frac{V_o}{V_{in}} = \frac{1}{1-D} \tag{3.57}$$

$$V_o = \frac{1}{1-D} V_{in} \tag{3.58}$$

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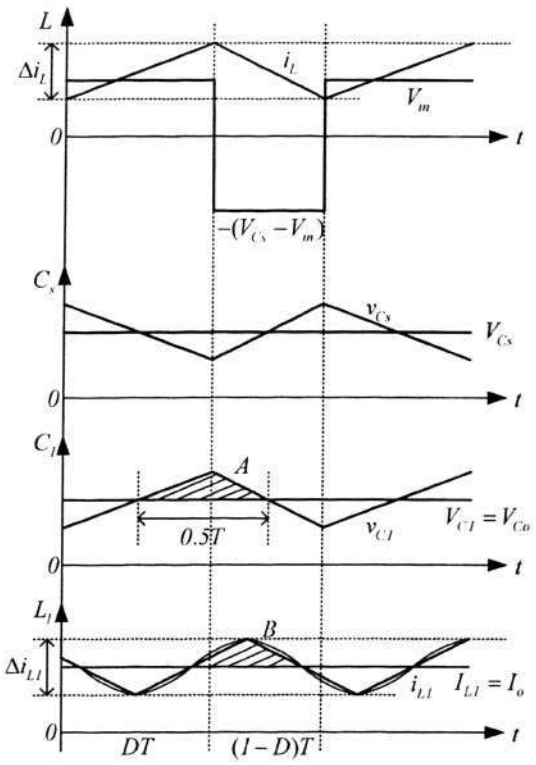

Fig. 3-25. Elementary self-lift circuit: waveforms with enlarged variations

$$V_{Cs} = V_{C1} = \frac{1}{1-D} V_{in} \tag{3.59}$$

$$\varsigma_L = \frac{\Delta i_L / 2}{I_L} = \frac{D}{2M_S^2} \frac{R}{fL} \tag{3.60}$$

$$\varepsilon_{C1} = \frac{\Delta v_{C1} / 2}{V_{C1}} = \frac{1}{2M_S fRC_1} \tag{3.61}$$

$$\varsigma_{L1} = \frac{\Delta i_{L1} / 2}{I_{L1}} = \frac{1}{16M_s f^2 L_1 C_1} \tag{3.62}$$

$$\varepsilon_S = \frac{\Delta v_o / 2}{V_o} = \frac{1}{128M_s f^3 L_1 C_1 C_o R} \tag{3.63}$$

$$Z_{N-B} = \frac{2M_s^2}{D} = \frac{2}{D(1-D)^2} \tag{3.64}$$

$$m_S = \frac{1+\sqrt{1+2D^2 Z_N}}{D(1-D)Z_N} \tag{3.65}$$

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{1}{2}(1+\sqrt{1+2D^2 Z_N}) \tag{3.66}$$

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Where: Z_N is defined as the normalized load $R/(fL)$.

The boundary curve between CCM and DCM, and relations of the voltage transfer gains versus Z_N are described in Fig. 3-26, which is beneficial for theoretical analysis and practical engineering design. It is derived that there is a minimum value of Z_N at the boundary curve under the condition of $D = 1/3$, and the corresponding Z_N is equal to 13.5. It means that the condition of $D = 1/3$ is the most possible for the converter to enter DCM.

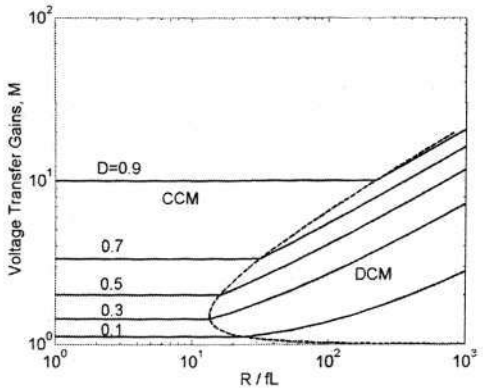

Fig. 3-26. Boundary between CCM and DCM and voltage transfer gains against Z_N

3.7.3 Performance Summary

From the foregoing analysis, it is known that the voltage transfer gain of the proposed circuit is significantly increased compared with that of the classical Cûk/Buck-boost converter.

Additionally, since v_{in}, S and R share the common ground, the proposed circuit has the potential of the further topology development, which may lead to the high order VL-type circuits with higher voltage transfer gains and single switch structure. The correlative work based on this circuit to derive high order circuits will be introduced solely in the future papers.

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3.7.4 Simulation and Experimental Verification

The main circuit parameters are chosen as follows: V_{in}= -12V, R=100Ω, L=L_1=500μH, C_s=110μF, C_1 =22μF, C_o=47μF and f =50kHz. The simulation objective is to obtain +36V output voltage.

It is obtained from (3.66) that Z_N is equal to 4. In CCM, D should be equal to 2/3 so that the converter can step up the output voltage to +36V. Since the boundary value of normalized load, $Z_{N-B}|_{D=2/3}$ is equal to 27 according to (3.64), Z_N is located at the left CCM region of the boundary curve as shown in Fig. 3-26. Therefore, it indicates that above parameters are appropriate for the CCM operation.

To verify the foregoing theoretical analysis results, the simulation is run under the open-loop and close-loop conditions, respectively. The reasons of presenting close-loop simulation results are as follow:

When a dc-dc converter is changed from one steady state to a new steady state due to duty ratio changing or load changing, the low-frequency oscillation is very easy to be introduced to the steady-state input current as ripples. This is a common phenomenon in dc-dc converters, which is the direct reason that current-mode control methods are widely accepted and used in practical industrial companies to improve steady-state current waveforms in dc-dc converter products. For example, the same phenomenon of low frequency ripples can be found in Fig. 2-12(b) and Fig. 2-15(b).

For the open-loop case, D is constant. For the close-loop case, the PWM technique integrating the dual-loop PI current-mode control algorithm is adopted to adjust D to compensate the perturbations. It is noted that in the curve 1 and 2 in the following figures correspond to the results of the open-loop case and the close-loop case, respectively.

The startup traces of v_o and i_{in} from the zero initial condition to the steady state are simulated and shown in Fig. 3-27(a), which is followed by the response to a step change from the light load to heavy load (R=9Ω). The responses (v_o and i_{in}) to a simulated small-signal perturbation of v_{in} are shown in Fig. 3-27(b). The steady-state performance in the simulation is identically matching to the theoretical analysis. It is also seen that the both the load changing and the input perturbation will cause a significant overshoot to the

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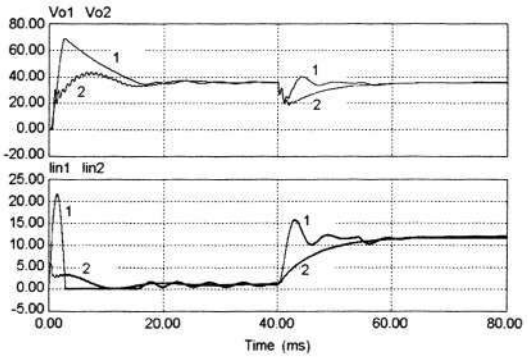
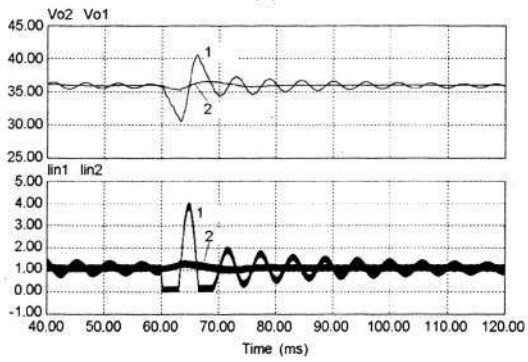
voltage and current in the open-loop operation. The resulting voltage and current stress to the components in the open-loop operation can be eliminated or be removed by introducing an effective close-loop current-mode controller in the close-loop operation.



(a)



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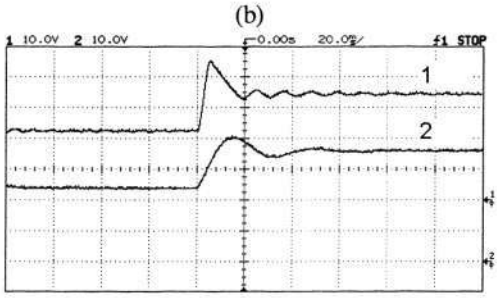

(c)

Fig. 3-27. Simulation and experimental results

(a) response to the step change from the light load to heavy load
(b) response to the small-signal perturbation of the source voltage
(c) experimental curves for the output voltage change

The same parameters are chosen to construct a testing hardware circuit. The low resistance MOSFET and fast-switching diodes are selected to decrease the power losses here. For the open-loop case, a step change of D is made from *0.5* to *0.67*, and the output voltage is recorded by Channel 1 as shown in Fig. 3-27(c). For the close-loop case, the reference voltage is changed from *24*V to *36*V, and the controller adjusts D. Channel 2

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shows the corresponding output voltages. It is seen that the transient processes are quick in only few milliseconds, and the output voltage ripple is negligible. Although the parasitic elements affect some performance, the converter reaches the new steady state that has a close agreement with the simulation and analysis results.

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Chapter 4 Mirror-Symmetrical Double Output VL-type Converters

Through the introduction and analysis of Chapters 2 and 3, the concepts of positive-to-positive and positive-to-negative voltage conversion are explained in detail. All circuits introduced in Chapters 2 and 3 are used to provide single output voltage. The circuits that can obtain double output voltages in simple structures will be discussed in this chapter. A novel mirror-symmetrical double-output dc-dc converter applying the VL technique will be proposed in this chapter together with its enhanced series. They are featured with high voltage transfer gains and single switch control method.

4.1 Introduction

Double-output dc-dc converters [61-65] can convert the positive input source voltage to positive and negative output voltages. They consist of two conversion paths. Usually, mirror-symmetrical double-output voltages are especially required in industrial applications and computer periphery circuits such as operational amplifiers, telecommunication equipment, computer periphery power supplies, differential servomotor drives and some symmetrical-voltage medical equipment. With the fast development of modern technology, the correlative research and applications of mirror-symmetrical double-output dc-dc power conversion techniques are becoming an important and promising area, which is expected to obtain the following aims:

- More extended voltage conversion range
- More compact structure with simple topologies
- Lower power losses
- Applicable easy and straightforward control methods

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At present, cascade connection and transformer isolation are usually utilized to develop double-output dc-dc converters with high voltage transfer gains [32-39]. However, multiple power switches and transformers in these converters increase the control complexity and the circuit cost significantly. Especially, magnetic flux and leakage inductance of the transformer will affect switching devices and regulation of the output voltage. Transformerless double-output dc-dc converters may be a good alternative to overcome the abovementioned problems, and they are usually derived from classical dc-dc topologies. For example, the positive and negative output Luo converters have been developed by F.L. Luo, which results in a novel transformerless double-output converter [61]. Additionally, the buck-boost and ZETA converters have also been explored to construct corresponding transformerless double-output converters [62].

The classical topologies, SEPIC and Cûk converters [28-31, 58-60] are shown in Fig. 2-1 and 3-1, respectively. Under different conditions of the duty ratio D, both SEPIC and Cûk converters can perform step-down and step-up dc-dc conversion due to their voltage transfer functions.

For the SEPIC converter, this topology does not suffer from an output polarity inversion. For the Cûk converter, it suffers an output polarity inversion. Their voltage transfer gains are as follows:

$$M_{SEPIC} = \frac{D}{1-D} \tag{4.1}$$

$$M_{Cuk} = -\frac{D}{1-D} \tag{4.2}$$

Reviewing their topologies, it is found that both of them are a derivative of the buck-boost converter in that the energy transferred from the input to the output is achieved by a capacitor C_s rather than by an inductor as in the buck-boost converter. C_s can prevent unwanted current flow from v_{in} to v_o. Furthermore, since the capacitive energy storage in them is more efficient than inductive energy storage in a buck-boost converter, a substantial weight and size reduction can be achieved. Therefore, the similar circuit mechanisms in these two converters provide the possibility to construct new circuits with double output voltages.

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Based on the prototypes of the SEPIC and Cûk converters, an in-depth study on the VL technique has been performed in this chapter. A family of novel *mirror-symmetrical double output VL-type converters* has been proposed. They are categorized into:

- mirror-symmetrical double output VL-type converter (elementary circuit)
- boost enhanced series
- super enhanced series

The detailed introduction will be performed in the following sections.

4.2 Mirror-Symmetrical Double Output VL-type Converter

We compare the SEPIC and Cûk prototypes. Each topology can be divided into two sections. One is the source section including the voltage source, the inductor L and the active switch S. The other is the pump section consisting of the rest components. Each topology can thus be considered as a special cascade connection of these two sections.

Since both of them have the same source sections (L-S) and the voltage transfer gains with opposite polarities, we combine the source section of SEPIC and Cûk converters at the input side. In addition, the VL technique is utilized in the pump sections to increases the voltage transfer gains, and combination is performed. The newly obtained topology shown in Fig. 4-1 is termed *mirror-symmetrical double output VL-type converter*. It is noted that four new components, D_{l+}, D_{l-}, C_{l+} and C_{l-} are added into the previous pump sections.

The proposed topology is a combination of the positive and negative conversion paths. The positive conversion path consists of three cascade sections, the source section $L-S$, the pump section $C_{s+}-(S)-L_{l+}-D_{l+}-C_{l+}$, and an output filter section D_o-C_{o+}. The negative conversion path also consists of three cascade sections, the source section $L-S$, the pump section $C_{s-}-(S)-D_f$, and an output Π-type filter section $D_{l-}-C_{l-}-L_{l-}-C_{o-}$. The detailed analysis will be performed in the following sub-sections, and the circuit is assumed operating in CCM.

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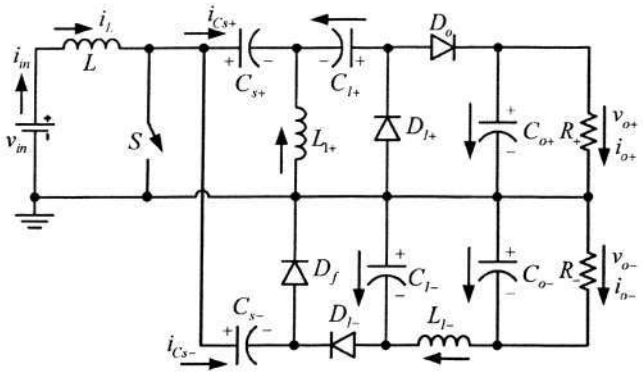


Fig. 4-1. Topology of the mirror-symmetrical double output VL-type converter

4.2.1 Positive conversion path

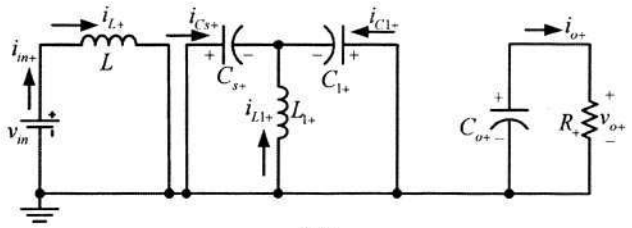
When switch S turns on, D_{l+} is on, and D_o is off. When S turns off, D_{l+} is off, and D_o is on. The capacitor C_{l+} performs characteristics to lift the output capacitor voltage V_{Co+} by the capacitor voltage V_{Cs+}. The equivalent circuits of the positive path during switching-on, switching-off and DCM are shown in Fig. 4-2(a-c), respectively.

Switching diagrams with main steady-state waveforms are shown in Fig. 4-3, where reference directions are referred to in Fig. 4-1. In the steady state, the average voltage across L over a cycle is zero. Thus,

$$V_{Cs+} = V_{in}$$

During switching-on, the voltage across C_{l+} is equal to V_{Cs+}. Since C_{s+} and C_{l+} are sufficiently large, we have:

$$V_{Cl+} = V_{Cs+} = V_{in}$$



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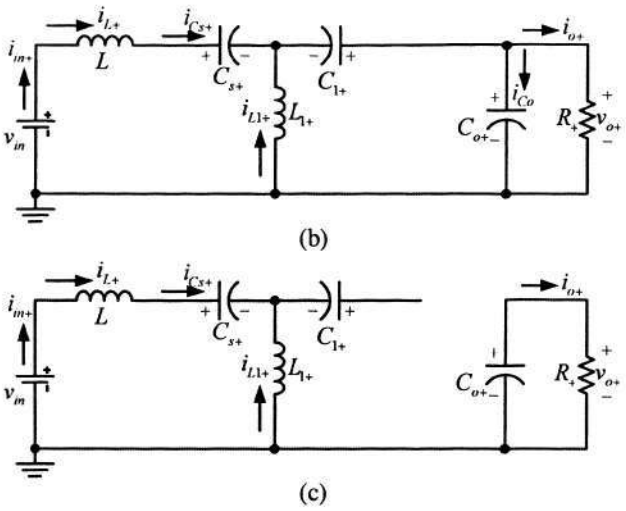

Fig. 4-2. Equivalent circuits of positive conversion path

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

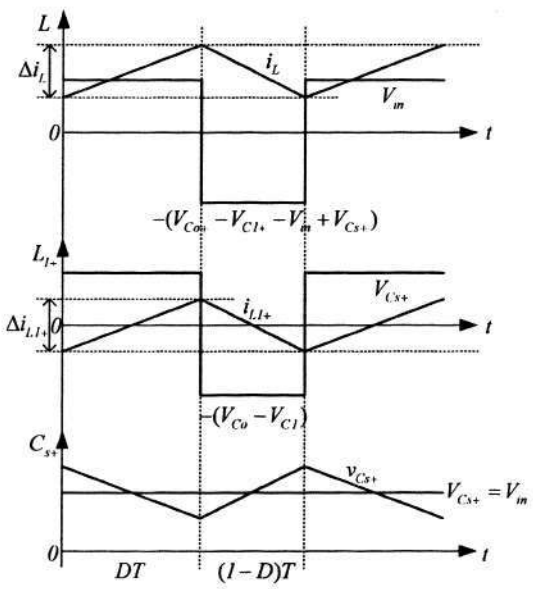

Fig. 4-3. Positive path: waveforms with enlarged variations

The inductor current i_L increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{in} and $-(V_{Co+}-V_{C1+}-V_{in}+V_{Cs+})$. Therefore, with the sec-voltage balance principle, we have

$$DTV_{in}=(1-D)T(V_{Co+}-V_{C1+}-V_{in}+V_{Cs+}) \text{ or } DTV_{in}=(1-D)T(V_{o+}-V_{in})$$

Hence,

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$$V_{o+} = \frac{1}{1-D} V_{in}$$

The voltage transfer gain in CCM is

$$M_{S+} = \frac{V_{o+}}{V_{in}} = \frac{1}{1-D} \tag{4.3}$$

and the input current is

$$I_{in+} = \frac{1}{1-D} I_{o+} = I_{L+} = I_{Cs+(off)} \tag{4.4}$$

The charges of C_{o+} and C_{s+} increase during switching-off and decrease during switching-on. We get:

$$Q_{Co+(on)} = I_{o+} DT \qquad Q_{Cs+} = I_{Cs+(on)} DT$$
$$Q_{Co+(off)} = I_{Co+(off)} (1-D)T \qquad Q_{Cs-} = I_{Cs+(off)} (1-D)T$$

In a switching cycle, $Q_{Co+(on)} = Q_{Co+(off)}$ and $Q_{Cs+(on)} = Q_{Cs+(off)}$. Therefore,

$$I_{Co+(off)} = \frac{D}{1-D} I_{o+}, \quad I_{Cs+(on)} = \frac{1}{D} I_{o+}$$

During switching-off, $i_{Do+}=i_{Co+}+ i_{o+}$. Therefore,

$$I_{Do+(off)} = I_{Co+(off)} + I_{o+} = \frac{1}{1-D} I_{o+} \tag{4.5}$$

During switching-off, L_{1+} and C_{1+} form a path and transfer the stored energy through D_o. Therefore,

$$I_{C1+(off)} = I_{Do(off)} = \frac{1}{1-D} I_{o+}$$

In a switching cycle, $Q_{C1+(on)} = Q_{C1+(off)}$. Therefore,

$$I_{C1+(on)} = \frac{1-D}{D} I_{C1+(off)} = \frac{1}{D} I_{o+}$$

During switching-on, L_{1+} and C_{1+} are connected in parallel, and they accept the stored energy from C_{s+}. Therefore, with the KCL law,

$$I_{L1+} = I_{Cs+(on)} - I_{C1+(on)} = 0 \tag{4.6}$$

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Equation (4.6) is for the average value of a switching cycle in the steady state. It is noted that a practical instantaneous inductor current i_{Ll+} flows through L_{l+} during each cycle. The energy storing and transferring of L_{l+} are achieved by associate oscillation of i_{Ll+}.

Since the peak-to-peak current variation of i_L, Δi_L is equal to DTV_{in}/L, the variation ratio of the current i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2M_{S+}^2}\frac{R_+}{fL} \tag{4.7}$$

The variation of the current i_{Do} during switching-off is equal to Δi_{Ll+}, and Δi_{Ll+} is equal to DTV_{in}/L_{l+}. Therefore, the variation ratio of i_{Do} is

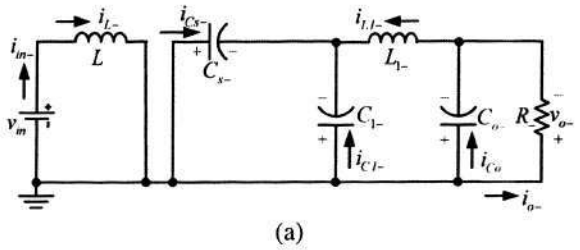
$$\xi_{Do} = \frac{\Delta i_{Ll+}/2}{I_{Do(off)}} = \frac{D}{2M_{S+}^2}\frac{R_+}{fL_{l+}} \tag{4.8}$$

The peak-to-peak voltage variation of v_{o+}, Δv_{o+} is equal to $I_{o+}DT/C_{o+}$. Therefore, the variation ratio of v_{o+} is

$$\varepsilon_S = \frac{\Delta v_{o+}/2}{V_{o+}} = \frac{D}{2R_+C_{o+}f} \tag{4.9}$$

4.2.2 Negative conversion path

When S turns on, D_{l-} is on, and D_f is off. When S turns off, D_{l-} is off, and D_f is on. C_{l-} performs characteristics to lift the output capacitor voltage V_{Co-} by the capacitor voltage V_{Cs-}. The equivalent circuits of the negative path during switching-on, switching-off and DCM are shown in Fig. 4-4(a-c), respectively.



(a)

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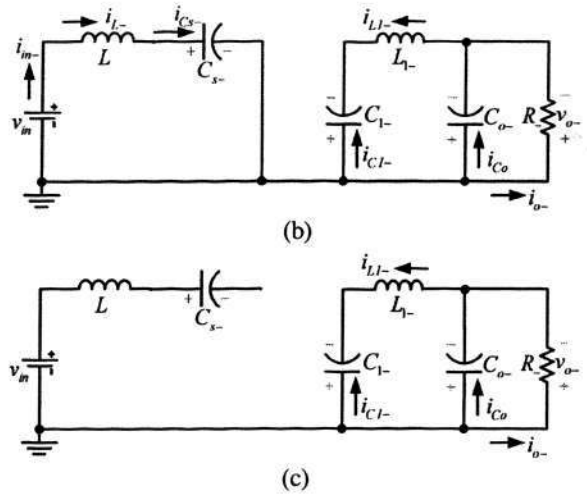

Fig. 4-4. Equivalent circuits of negative conversion path

(a) equivalent circuit during switching-on
(b) equivalent circuit during switching-off
(c) equivalent circuit during DCM

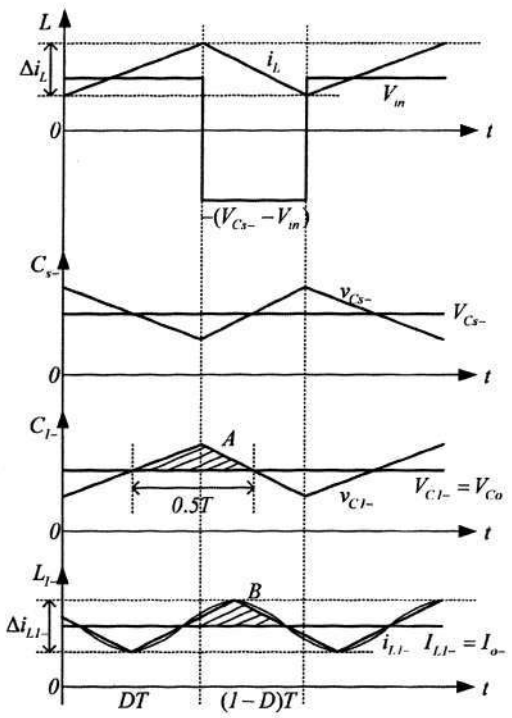

Fig. 4-5. Negative path: waveforms with enlarged variations

Switching diagrams with main steady-state waveforms are shown in Fig. 4-5, where reference directions are referred to in Fig. 4-1. In the steady state, the average voltage across L_{1-} over a period is zero. Thus

$$V_{C1-} = V_{Co-} = V_{o-}$$

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During the switch-on period, V_{C1-} is equal to the voltage across C_{s-}. Since C_{s-} and C_{1-} are sufficiently large, we have:

$$V_{Cs-} = V_{C1-} = V_{o-}$$

The inductor current i_L increases during switching-on and decreases during switching-off. The corresponding voltages across L are V_{in} and $-(V_{Cs-} - V_{in})$. Therefore, applying the inductor volt-second balance principle to L, we have:

$$DTV_{in} = (1-D)T(V_{Cs-} - V_{in}) \text{ or } DTV_{in} = (1-D)T(V_{o-} - V_{in})$$

Hence

$$V_{o-} = \frac{1}{1-D} V_{in}$$

The voltage transfer gain in CCM is

$$M_{S-} = \frac{V_{o-}}{V_{in}} = \frac{1}{1-D} \tag{4.10}$$

In addition, the input current is,

$$I_{in} = \frac{1}{1-D} I_{o-} = I_L = I_{Df-off} \tag{4.11}$$

C_o acts as a lowpass filter so that

$$I_{L1-} = I_{o-} \tag{4.12}$$

Since the peak-to-peak current variation of i_L, Δi_L is equal to DTV_{in}/L, the variation ratio of i_L is

$$\varsigma_L = \frac{\Delta i_L/2}{I_L} = \frac{D}{2M_{S-}^2} \frac{R_-}{fL} \tag{4.13}$$

The peak-to-peak voltage variation ratio of v_{C1-}, Δv_{C1-} is approximate to

$$\Delta v_{C1-} = \frac{I_{o-}(1-D)T}{C_{1-}}$$

Therefore, the variation ratio of v_{C1-} is

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$$\varepsilon_{C1-} = \frac{\Delta v_{C1-}/2}{V_{C1-}} = \frac{1}{2M_{S-}fR_{-}C_{1-}} \tag{4.14}$$

Because v_{o-} varies very litter, the peak-to-peak current variation of i_{L1-} can be calculated by the area A of a triangle with width $T/2$ and the height $\Delta v_{C1-}/2$, which is approximately

$$\Delta i_{L1-} = \frac{\frac{1}{2}\frac{\Delta V_{C1-}}{2}\frac{T}{2}}{L_{1-}} = \frac{(1-D)I_{o-}}{8f^2L_{1-}C_{1-}}$$

Therefore, the variation ratio of i_{L1-} is approximate to

$$\varsigma_{L1-} = \frac{\Delta i_{L1-}/2}{I_{L1-}} = \frac{1}{16M_{S-}f^2L_{1-}C_{1-}} \tag{4.15}$$

The variation of i_{Df} is equal to Δi_L during switching-off, so the variation ratio of i_{Df} is

$$\xi_{Df} = \varsigma_L = \frac{D}{2M_{S-}^2}\frac{R_{-}}{fL} \tag{4.16}$$

To simplify the calculation, we treat the ripple waveform of i_{L1-} as a triangle waveform as shown in Fig. 4-5 because the ripple of i_{L1-} is very small. So the peak-to-peak voltage variation of v_{o-} is calculated by the area B, which is approximately

$$\Delta v_{o-} = \frac{\frac{1}{2}\frac{\Delta i_{L1-}}{2}\frac{T}{2}}{C_{o-}} = \frac{(1-D)I_{o-}}{64f^3L_{1-}C_{1-}C_{o-}}$$

Therefore, the variation ratio of v_{o-} is approximate to

$$\varepsilon_S = \frac{\Delta v_{o-}/2}{V_{o-}} = \frac{1}{128M_{S-}f^3L_{1-}C_{1-}C_{o-}R_{-}} \tag{4.17}$$

From (4-3) and (4-10), we can define that $V_o=V_{o+}=|V_{o-}|$, $M_S=M_{S+}=M_{S-}= V_o/V_{in} = 1/(1-D)$, and the mirror-symmetrical double output voltages in CCM are obtained.

4.2.3 DCM

The free wheeling diode currents i_{Do} and i_{Df} become zero during switch off before the beginning of the next switching cycle, which means the converter is operating in DCM.

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The equivalent circuits of the DCM operation are shown in Figs. 4-2(c) and 4-4(c), respectively. In order to obtain the mirror-symmetrical double-output voltages in DCM, we purposely select: $L=L_{1+}$ and $R_+=R_-$. The normalized load of the positive conversion path, $R_+/(fL_{1+})$ is written as Z_{N+}, and the normalized load of the negative conversion path, $R_-/(fL)$ is written as Z_{N-}. Thus, we define that $Z_N=Z_{N+}=Z_{N-}$ and $\xi=\xi_{Do}=\xi_{Df}$. The condition for DCM is $\xi \geq 1$, i.e.

$$\xi=\frac{D}{2M_S^2}Z_N \geq 1 \tag{4.18}$$

As a special case, if i_{Do} and i_{Df} simultaneously decrease to zero at $t = T$, the circuit operates at the boundary of CCM and DCM. Therefore, the boundary between CCM and DCM is obtained as below:

$$Z_{N-B}=\frac{2M_s^2}{D}=\frac{2}{D(1-D)^2} \tag{4.19}$$

When $Z_N > Z_{N-B}$, the circuit operates in DCM. Under the DCM condition i_{Do} decreases to zero at $t = t_{1+} = [D+m_{S+}(1-D)]T$, where

$$DT < t_1 < T \text{ and } 0 < m_{S+} < 1$$

Here, m_{S+} is the current filling efficiency for the positive conversion path and defined as

$$m_{S+}=\frac{t_1-DT}{(1-D)T} \tag{4.20}$$

In DCM, i_L increases during switching-on and decreases during the period from DT to $m_{S+}(1-D)T$. For the positive conversion paths, the corresponding voltages across L are V_{in} and $-(V_{o+}-V_{in})$. Thus, utilizing the volt-second balance principle, we have

$$DTV_{in}=m_{S+}(1-D)T(V_{o+}-V_{in}) \tag{4.21}$$

Additionally, the transferred charges of L_{1+} during switching-off are equal to $m_S(1-D)T\Delta i_{L1+}/2$, which compensate the total consumed charges of the load. So we have

$$I_{o+}T=\frac{1}{2}m_{S+}(1-D)T\Delta i_{L1} \text{ or}$$

$$\frac{V_{o+}}{R_+}T=\frac{1}{2}m_{S+}(1-D)T\frac{DTV_{in}}{L_{1+}} \tag{4.22}$$

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Combining (4.21) and (4.22), we obtain

$$m_{S+} = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{4.23}$$

From (4.21), we have

$$V_{o+} = [1+\frac{D}{m_{S+}(1-D)}]V_{in} \tag{4.24}$$

Therefore, substituting (4.23) into (4.24) yields the following positive voltage transfer gain in DCM:

$$M_{S+(DCM)} = \frac{1}{2}(1+\sqrt{1+2D^2Z_N}) \tag{4.25}$$

Under the DCM condition i_{Df} decreases to zero at $t = t_{1\_} = [D+m_{S\_}(1\text{-}D)]T$ where

$$DT < t_1 < T \text{ and } 0 < m_{S\_} < 1$$

Here, $m_{S\_}$ is the current filling efficiency for the negative conversion path and defined as

$$m_{S\_} = \frac{t_1 - DT}{(1-D)T}$$

For the negative conversion paths, the corresponding voltages across L are V_{in} and $-(V_{o\_} - V_{in})$. Thus, utilizing the volt-second balance principle, we have

$$DTV_{in} = m_{S\_}(1-D)T(V_{o\_} - V_{in}) \tag{4.26}$$

In addition, the transferred charges of L to the positive conversion path during switching-off are equal to $m_{S\_}(1-D)T\Delta i_L/2$, which compensate the total consumed charges of the load. So we have

$$I_{o\_}T = \frac{1}{2}m_{S\_}(1-D)T\Delta i_L \text{ or}$$

$$\frac{V_{o\_}}{R_{\_}}T = \frac{1}{2}m_{S\_}(1-D)T\frac{DTV_{in}}{L} \tag{4.27}$$

Combining (4.26) and (4.27), we obtain

$$m_{S\_} = \frac{1+\sqrt{1+2D^2Z_N}}{D(1-D)Z_N} \tag{4.28}$$

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From (4.26), we have

$$V_{o-} = [1 + \frac{D}{m_{S-}(1-D)}]V_{in} \tag{4.29}$$

Therefore, substituting (4.28) into (4.29) yields the negative voltage transfer gain in DCM as follows:

$$M_{S-(DCM)} = \frac{1}{2}(1 + \sqrt{1 + 2D^2 Z_N}) \tag{4.30}$$

From the foregoing analysis, we can define that $m_S = m_{S+} = m_{S-}$, $V_o = V_{o+} = |V_{o-}|$, $M_{S(DCM)} = M_{S+(DCM)} = M_{S-(DCM)} = V_o/V_{in} = (1 + \sqrt{1 + 2D^2 Z_N})/2$, so the mirror-symmetrical double output voltages in DCM are obtained. Using (4.3), (4.10), (4.19), (4.25) and (4.30), we can obtain the boundary curve between CCM and DCM and voltage transfer gains versus the normalized load as shown in Fig. 4-6. We can see that a larger normalized load may cause a higher output voltage in DCM.

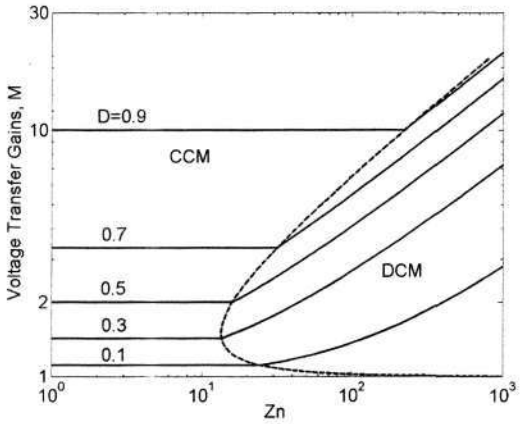

Fig. 4-6. Proposed topology: boundary between CCM and DCM, and voltage transfer gains against Z_N

4.3 Boost Enhanced Series

Since the positive and negative conversion paths in Fig. 4-1 share a common source section that can be regarded as a boost converter, we can construct corresponding enhanced circuits by using applying the VL technique to the source section of Fig. 4-1.

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The concept of cascade boost converter proposed by F.L. Luo [3] is utilized here, which results in much more energy transferred to C_{s+} and C_{s-} in each cycle. And consequently, V_{Cs+} and V_{Cs-} are increased stage-by-stage along the geometric progression. To explain conveniently, we call them *boost*^{1}, *boost*^{2} and *boost*^{M} enhanced circuits, respectively.

4.3.1 Boost^1 enhanced circuit

According to the cascade re-lift boost converter proposed in [3], the source section is redesigned by adding the components (L_{s1}-D_{s1}-D_{s2}-C_{s1}), which form a basic VL cell as shown in Fig. 4-7. This circuit is indicated by *boost*^{1}. Therefore, the newly-derived topology in Fig. 4-7 provides a single boost circuit enhancement using the supplementary components, and the concept of cascade boost converter is successfully integrated with the mirror-symmetrical double output converter. When S turns on, D_{s2} is on, and D_{s1} is off. When S turns off, D_{s2} is off, and D_{s1} is on. The capacitor C_{s1} performs its characteristics to lift the source voltage V_{in}. Therefore,

$$V_{Cs1} = \frac{1}{1-D} V_{in} \tag{4.31}$$

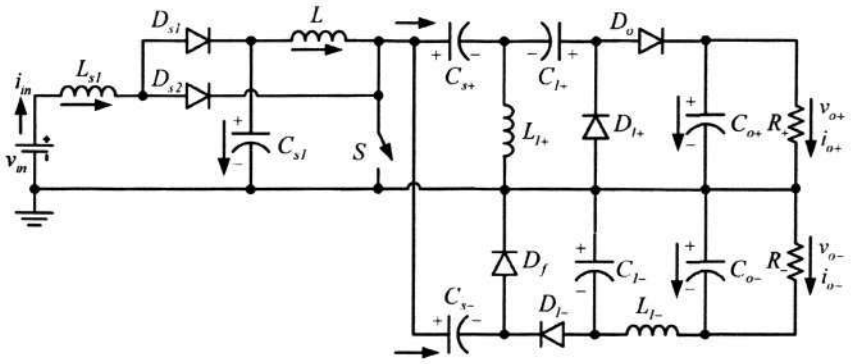

Fig. 4-7. Boost enhanced series: boost^1 enhanced circuit

The energy is transferred to C_{s+} and C_{s-} in each cycle from C_{s1}. Furthermore, V_{Cs+} and V_{Cs-} are increased significantly. Thus, in CCM, we get

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$$\begin{cases} V_{Cs+} = V_{Cs1} = \dfrac{1}{1-D} V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Cs1} = \dfrac{1}{(1-D)^2} V_{in} \end{cases} \tag{4.32}$$

Therefore, from the foregoing analysis and calculation in Section II and III, the voltage transfer gains of the boost[1] enhanced circuit in CCM are:

$$\begin{cases} M_{boost^1+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{1}{(1-D)^2} \\ M_{boost^1-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{1}{(1-D)^2} \end{cases} \tag{4.33}$$

Analogously, the voltage transfer gains of the boost[1] enhanced circuit in DCM are:

$$\begin{cases} M_{boost^1+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)} \\ M_{boost^1-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)} \end{cases} \tag{4.34}$$

4.3.2 Boost^M enhanced circuit

Referring to Fig. 4-7, it is possible to realize the boost^M enhanced circuit (i.e. multiple boost circuits enhancement) in the source section by applying the generalized cascade boost converter [3] to the source section (i.e. repeat the components L_{s1}-D_{s1}-D_{s2}-C_{s1}stage by stage). Assuming that there are n voltage lift cells (denoted by $boost^M$), the generalized representation of the boost enhanced series for the mirror-symmetrical double output VL-type converter is shown in Fig. 4-8. All circuits share the same power switch S, which simplifies the control scheme and decreases the cost significantly. Hence, each circuit has one switch, $(n+3)$ inductors, $(n+6)$ capacitors and $(2n+4)$ diodes. All the capacitors are sufficiently large. The energy is transferred to C_{s+} and C_{s-} in each cycle from C_{sn} and increase V_{Cs+} and V_{Cs-}. In CCM, we get:

$$V_{Csn} = \frac{1}{(1-D)^n} V_{in} \tag{4.35}$$

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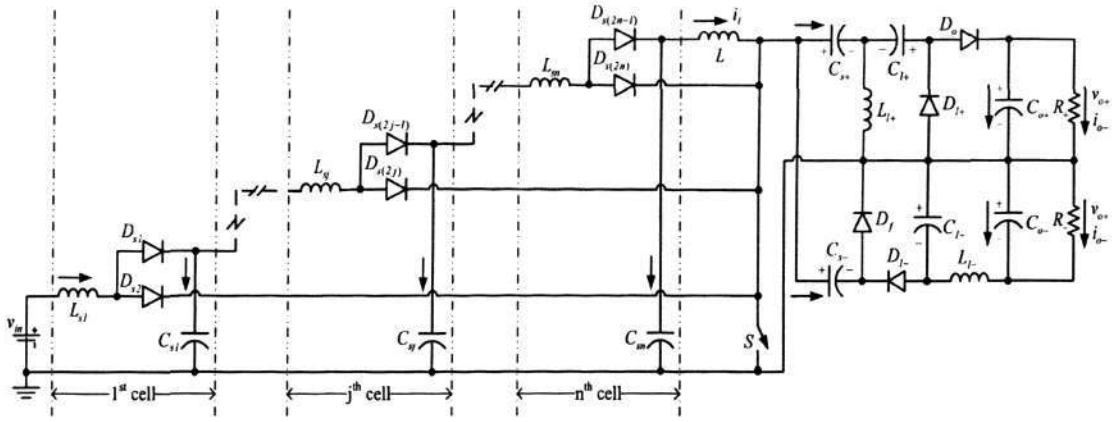

Fig. 4-8. Generalized representation of the boost enhanced series (the boost^M enhanced circuit)

$$\begin{cases} V_{Cs+} = V_{Csn} = \dfrac{1}{(1-D)^n} V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Csn} = \dfrac{1}{(1-D)^{n+1}} V_{in} \end{cases} \tag{4.36}$$

Therefore, from the foregoing analysis and calculation, the general voltage transfer gains of the boost series are

$$\begin{cases} M_{boost^M-S+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{1}{(1-D)^{n+1}} \\ M_{boost^M-S-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{1}{(1-D)^{n+1}} \end{cases} \tag{4.37}$$

Analogously, the general voltage transfer gains of the boost series in DCM are:

$$\begin{cases} M_{boost^M+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)^n} \\ M_{boost^M-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)^n} \end{cases} \tag{4.38}$$

From (4.37) and (4.38), it is seen that the mirror-symmetrical double output voltages in CCM and DCM are obtained.

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4.4 Super Enhanced Series

In [3], super lift converter as an series of improved cascade boost converters are introduced by F.L. Luo. Here, the concepts of the super lift converter are applied to the source section in Fig. 4-1 to improve the voltage lift ability of the source section. In each cycle, C_{s+} and C_{s-} can obtain absorb and transfer much more energy. A series of circuits are thus constructed. To explain conveniently, we call them *super*^{1}, *super*^{2} and *super*^{M} enhanced circuits, respectively.

4.4.1 Super^1 enhanced circuit

The circuit diagram is shown in Fig. 4-9, and D_{a1}-C_{a1}-L_{s1}-D_{s2} form a basic voltage super lift cell. Here, the circuit in the source section is the same to the super re-lift converter proposed in [3]. When switch S turns on, D_{s2} and D_{a1} are on, and D_{s1} is off. When S turns off, D_{s2} and D_{a1} are off, and D_{s1} is on. Because C_{a1} performs characteristics of a ladder joint to link L_{s1} and C_{s1} during switching-off, V_{Cs1} are lifted by V_{Ca1}.

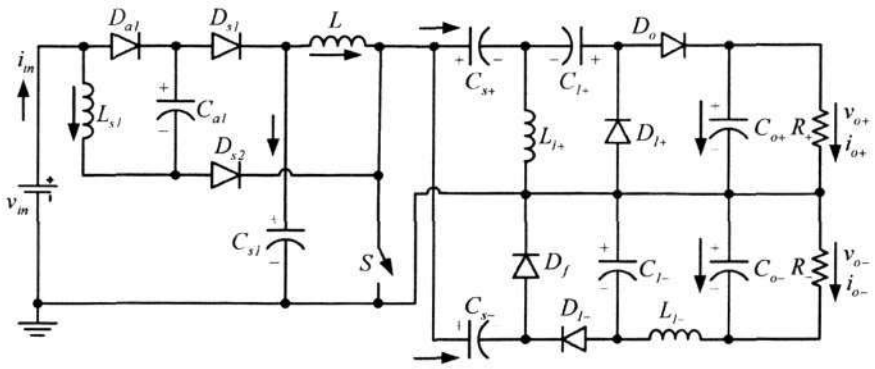

Fig. 4-9. Super enhanced series: super^1 enhanced circuit

Therefore,

$$V_{Cs1} = \frac{1}{1-D} V_{in} + V_{Ca1} = \frac{2-D}{1-D} V_{in} \tag{4.39}$$

The energy is transferred to C_{s+} and C_{s-} in each cycle from C_{s1}. Furthermore, V_{Cs+} and V_{Cs-} are increased significantly. Thus, in CCM, we get

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$$\begin{cases} V_{Cs+} = V_{Cs1} = \dfrac{2-D}{1-D} V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Cs1} = \dfrac{2-D}{(1-D)^2} V_{in} \end{cases} \tag{4.40}$$

Therefore, from the foregoing analysis and calculation in Section II and III, the voltage transfer gains of the super^{l} enhanced circuit in CCM are:

$$\begin{cases} M_{super^{l}+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{2-D}{(1-D)^2} \\ M_{super^{l}-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{2-D}{(1-D)^2} \end{cases} \tag{4.41}$$

Analogously, the voltage transfer gains of the super^{l} enhanced circuit in DCM are:

$$\begin{cases} M_{super^{l}+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(2-D)(1+\sqrt{1+2D^2 Z_N})}{2(1-D)} \\ M_{super^{l}-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(2-D)(1+\sqrt{1+2D^2 Z_N})}{2(1-D)} \end{cases} \tag{4.42}$$

4.4.2 Super^{M} enhanced circuit

Referring to Fig. 4-9, it is possible to construct the super^{M} enhanced circuit by applying the generalized super lift converter [3] to the source section (i.e. repeat the components L_{s1}-D_{a1}-C_{a1}-D_{s1}-D_{s2}-C_{s1}). Assuming that there are n voltage super lift cells, the generalized representation of the super enhanced series for the mirror-symmetrical double output VL-type converter is shown in Fig. 4-10. All circuits share the same power switch S, which simplify the control scheme and decrease the cost significantly. Hence, each circuit has one switch, $(n+3)$ inductors, $(2n+6)$ capacitors and $(3n+4)$ diodes. All capacitors are sufficiently large. The energy is transferred to C_{s+} and C_{s-} in each cycle from C_{sn}, and it can significantly increase V_{Cs+} and V_{Cs-}.

From the foregoing analysis and calculation, the general formulas for all super^{M} enhanced circuits can be obtained as below:

$$V_{Csn} = \left(\frac{2-D}{1-D}\right)^{n} V_{in} \tag{4.43}$$

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$$\begin{cases} V_{Cs+} = V_{Csn} = (\dfrac{2-D}{1-D})^n V_{in} \\ V_{Cs-} = \dfrac{1}{1-D} V_{Csn} = \dfrac{(2-D)^n}{(1-D)^{n+1}} V_{in} \end{cases} \tag{4.44}$$

Therefore, from the foregoing analysis and calculation in Section II and III, the general voltage transfer gains of the super enhanced series in CCM are:

$$\begin{cases} M_{super^M+} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(2-D)^n}{(1-D)^{n+1}} \\ M_{super^M-} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(2-D)^n}{(1-D)^{n+1}} \end{cases} \tag{4.45}$$

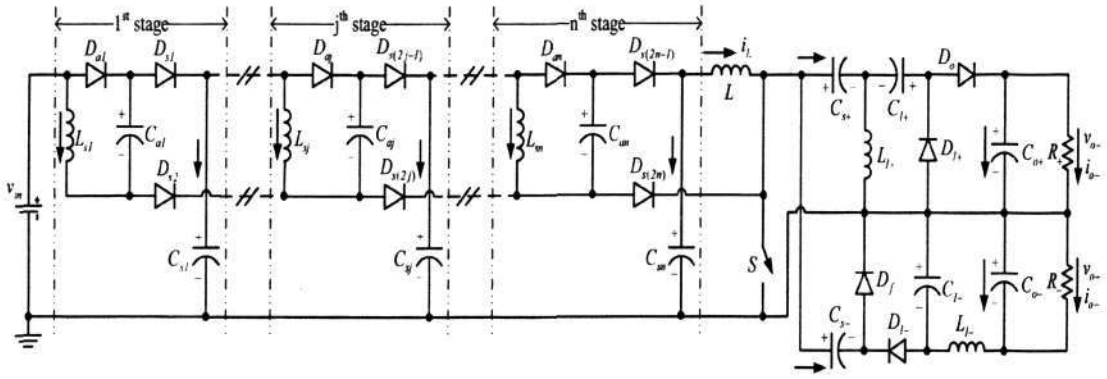

Fig. 4-10. Generalized representation of the super enhanced series (the super^M enhanced circuit)

Analogously, the general voltage transfer gains of the super enhanced series in DCM are:

$$\begin{cases} M_{super^M+(DCM)} = \dfrac{V_{o+}}{V_{in}} = \dfrac{(1+\sqrt{1+2D^2Z_N})}{2} (\dfrac{2-D}{1-D})^n \\ M_{super^M-(DCM)} = \dfrac{V_{o-}}{V_{in}} = -\dfrac{(1+\sqrt{1+2D^2Z_N})}{2} (\dfrac{2-D}{1-D})^n \end{cases} \tag{4.46}$$

From (4.45) and (4.46), it is seen that the mirror-symmetrical double output voltages in CCM and DCM are obtained.

From the foregoing analysis and calculation, the general formulas for two enhanced series are obtained and tabulated in Table 4-1 for reference.

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Table 4-1 Summary of two enhanced series (n is the number of VL cells)

	Boost Series	Super Series
No. of L	$n+3$	$n+3$
No. of C	$n+6$	$2n+6$
No. of D	$2n+4$	$3n+4$
V_{Csn}	$\frac{1}{(1-D)^n}V_{in}$	$(\frac{2-D}{1-D})^n V_{in}$
V_{Cs+}	$\frac{1}{(1-D)^n}V_{in}$	$(\frac{2-D}{1-D})^n V_{in}$
V_{Cs-}	$\frac{1}{(1-D)^{n+1}}V_{in}$	$\frac{(2-D)^n}{(1-D)^{n+1}}V_{in}$ $---CCM$ $\frac{(1+\sqrt{1+2D^2Z_N})}{2}(\frac{2-D}{1-D})^n$ $---DCM$
I_L	$\frac{V_{in}}{(1-D)^{n+2}}\cdot\frac{R_+ + R_-}{R_+R_-}$	$\frac{(2-D)^n V_{in}}{(1-D)^{n+2}}\cdot\frac{R_+ + R_-}{R_+R_-}$
I_{in}	$\frac{V_{in}}{(1-D)^{2n+2}}\cdot\frac{R_+ + R_-}{R_+R_-}$	$\frac{(2-D)^{2n} V_{in}}{(1-D)^{2n+2}}\cdot\frac{R_+ + R_-}{R_+R_-}$
M_{CCM}	$\pm\frac{1}{(1-D)^{n+1}}$	$\pm\frac{(2-D)^n}{(1-D)^{n+1}}$
M_{DCM}	$\pm\frac{(1+\sqrt{1+2D^2Z_N})}{2(1-D)^n}$	$\pm\frac{(1+\sqrt{1+2D^2Z_N})}{2}(\frac{2-D}{1-D})^n$

4.5 Simulation and Experimental Results

Simulation package PSIM was applied to three individual cases. The voltages of positive and negative paths are given to verify the theoretical analysis. The corresponding hardware testing circuits were also constructed to compare with the simulation results. It is noted that v_{o+} and v_{o-} are demonstrated through channel 1 and 2 of the oscillograph (share the common ground), respectively.

4.5.1 Simulation and experimental results of the elementary circuit

Referring to Fig. 4-1, the circuit parameters for simulation are: $V_{in}=10V$, $R_+ = R_- = 100\Omega$, $L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{1+}=C_{1-}=22\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=100kHz$. According to (4.3) and (4.10), we obtain the theoretical values of

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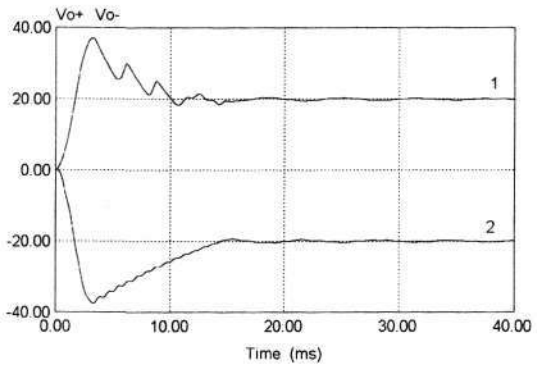
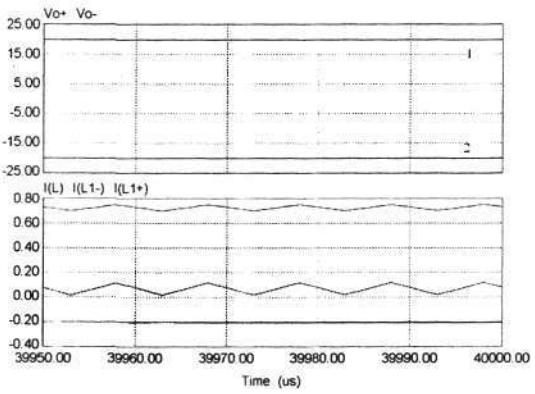
double output voltage V_{o+} and V_{o-}. They are equal to *20V* and *-20V*, respectively. The simulation results under zero initial conditions in Psim are shown in Fig. 4-11, where curve 1 is for v_{o+} of the positive conversion path and curve 2 is for v_{o-} of the negative conversion path. It can be seen that the startup process is quick and similar to other existing dc-dc converters. The steady-state values as shown in Fig. 4-11(b) are identically matching to the theoretical analysis.



(a)



(b)

Fig. 4-11. CCM Simulation results of the mirror-symmetrical double output VL-type converter

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms in (a)

On the basis of the above simulation parameters, we let: $R_+ = R_- = 1000\Omega$, $L = 500\ \mu H$, and $f = 50$kHz in order that $Z_{N+} = Z_{N-} = Z_N$. Under the condition of $D = 0.4$, Z_N in this case is equal to *40* and located at the right DCM region of the boundary curve shown in Fig. 4-6. Therefore, when $D = 0.4$, the circuit will work in DCM. According to (4.30), we obtain that the theoretical values of V_{o+} and V_{o-} are equal to +*23.5*V and -*23.5*V, respectively.

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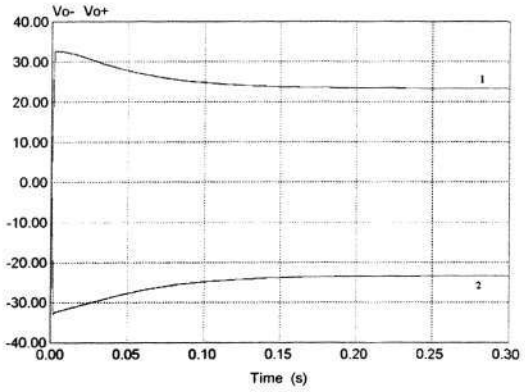
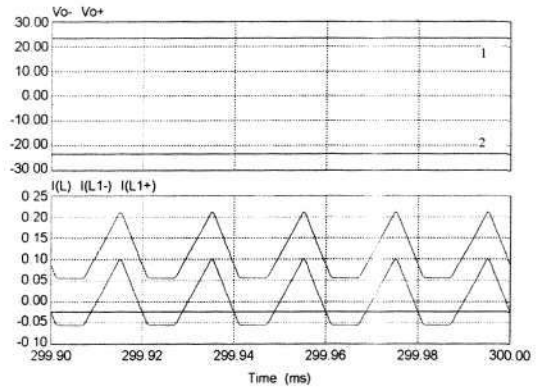
The simulated startup traces (v_o and i_L) under zero initial conditions are shown in Fig. 4-12(a), and the corresponding steady-state waveforms are shown in Fig.4-12(b). It is seen from Fig. 4-12 that the simulated values of V_o *and* V_{o-} are about ±*23.4*V, which has a good agreement with the above theoretical analysis results.



(a)



(b)

Fig. 4-12. DCM Simulation results of the mirror-symmetrical double output VL-type converter

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms in (a)

The parameters of the CCM case are chosen to construct the testing hardware circuit. Only a single n-channel MOSFET is used in the circuit. The corresponding experimental curves in the steady state are shown in Fig. 4-13 respectively. The curve shown in Channel 1 with 10V/Div corresponds to positive output v_{o+}, which is about *18.7V*. The curve shown in Channel 2 with 10V/Div corresponds to the negative output v_{o-}, which is also about *18.7V*. Considering the effects caused by the parasitic parameters, we can see that the measured results are very close to the theoretical analysis and simulation results.

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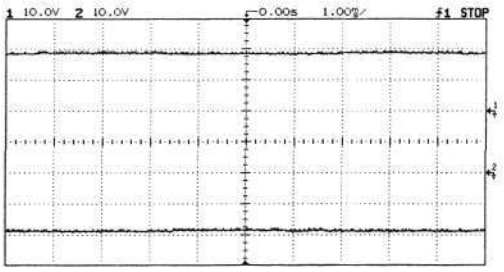
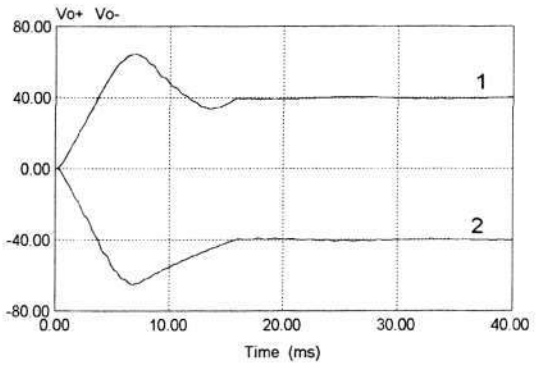


Fig. 4-13. Experimental results of the mirror-symmetrical double output VL-type converter

4.5.2 Simulation and experimental results of a boost[1] enhanced circuit

Referring to Fig. 4-7, the circuit parameters for simulation are: $V_{in}=10V$, $R_+ = R_- =100\Omega$, $L_{s1}=L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{s1}=C_{1+}=C_{1-}=22\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=50kHz$. According to (4.33), we obtain the theoretical values of double output voltage V_{o+} and V_{o-}. They are equal to $40V$ and $-40V$, respectively. The simulation results in Psim are shown in Fig. 4-14, where curve 1 is for v_{o+} of the positive conversion path and curve 2 is for v_{o-} of the negative conversion path. It is seen that the steady-state values in the simulation are identically matching the theoretical analysis.



(a)

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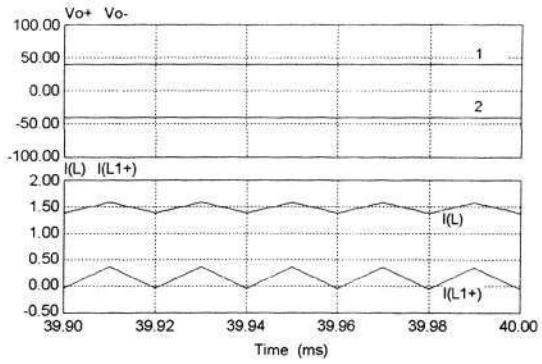


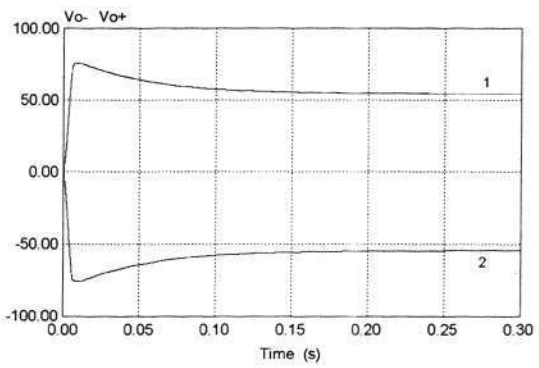
(b)

Fig. 4-14. CCM Simulation verification for the proposed converter

(a) simulated startup traces under zero initial conditions
(b) waveforms in the steady state

On the basis of the above simulation parameters, we let: $R_+ = R_- = 1000\Omega$ and $L=500\ \mu H$, in order that $Z_{N+} = Z_{N-} = Z_N$. Under the condition of $D=0.5$, Z_N in this case is equal to 40 and located at the right DCM region of the boundary curve shown in Fig. 4-6. Therefore, when $D=0.5$, the circuit will work in DCM. According to (4.34), we obtain that the theoretical values of V_{o+} and V_{o-} are equal to $+55.8V$ and $-55.8V$, respectively.

The simulated startup traces (v_o and i_L) under zero initial conditions are shown in Fig. 4-15(a), and the corresponding steady-state waveforms are shown in Fig. 4-15(b). It is seen from Fig. 4-15 that the simulated values of V_o *and* V_{o-} are about $\pm 54.6V$, which has a good agreement with the above theoretical analysis results.



(a)

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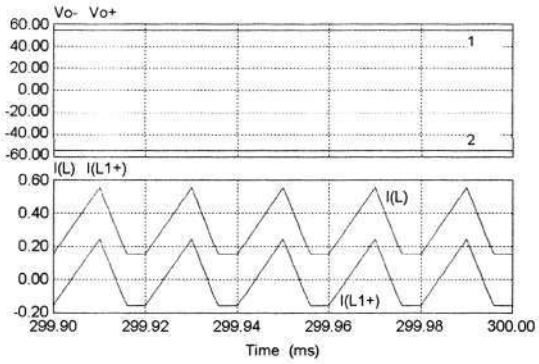

(b)

Fig. 4-15. DCM Simulation verification for the proposed converter

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms in (a)

The parameters of the CCM case are chosen to construct the testing hardware circuit. Only a single n-channel MOSFET is used in the circuit. The corresponding experimental curves in the steady state are shown in Fig. 4-16 respectively. The curve shown in Channel 1 with 20V/Div corresponds to positive output v_{o+}, which is about *37V*. The curve shown in Channel 2 with 20V/Div corresponds to the negative output v_{o-}, which is also about *37V*. Considering the effects caused by the parasitic parameters, we can see that the measured results are very close to the theoretical analysis and simulation results.

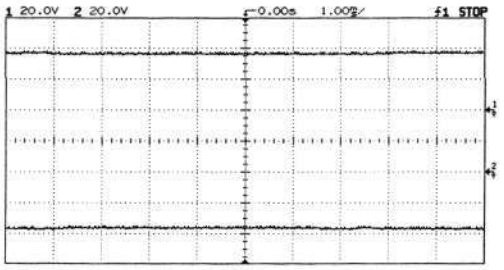

Fig. 4-16. Experimental verification for the proposed converter

4.5.3 Simulation and experimental results of a super[1] enhanced circuit

Referring to Fig. 4-9, the circuit parameters for simulation are: $V_{in}=10V$, $R_+ = R_- =100\Omega$, $L_{s1}=L=1mH$, $L_{1+}=L_{1-}=500\mu H$, $C_{s1}=C_{1+}=C_{1-}=22\mu F$, $C_{a1}=220\mu F$, $C_{s+}=C_{s-}=110\mu F$, $C_{o+}=C_{o-}=47\mu F$, $D=0.5$ and $f=50kHz$. According to (4.41), we obtain the theoretical values of double output voltage V_{o+} and V_{o-}. They are equal to *60V* and *-60V*.

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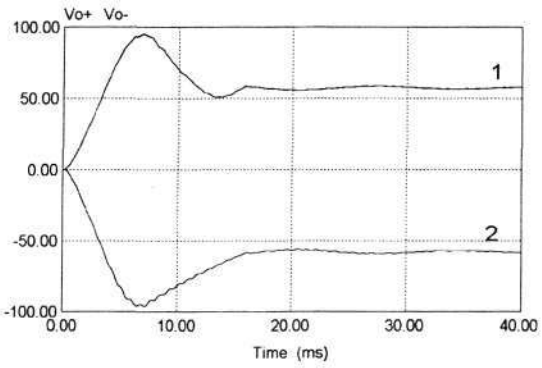
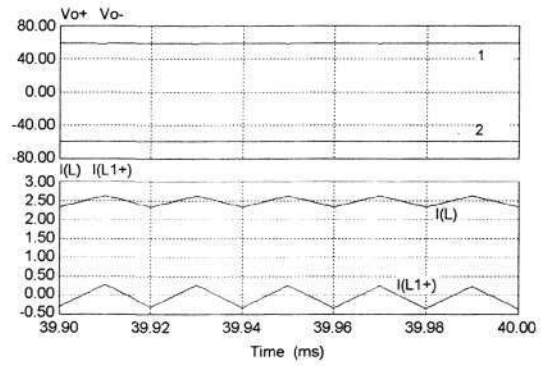
The simulation results in Psim are shown in Fig. 4-17, where curve 1 is for v_{o+} of the positive conversion path and curve 2 is for v_{o-} of the negative conversion path. The steady-state values in the simulation are identically matching to the theoretical analysis.



(a)



(b)

Fig. 4-17. CCM Simulation verification for the proposed converter

(a) simulated startup traces under zero initial conditions
(b) steady-state waveforms in (a)

On the basis of the above simulation parameters, we let: $R_+ = R_- = 1000\Omega$ and $L=500\ \mu H$, in order that $Z_{N+} = Z_{N-} = Z_N$. Under the condition of $D=0.5$, Z_N in this case is equal to 40 and located at the right DCM region of the boundary curve shown in Fig. 4-6. Therefore, when $D=0.5$, the circuit will work in DCM. According to (4.42), we obtain that the theoretical values of V_{o+} and V_{o-} are equal to $+83.7V$ and $-83.7V$, respectively.

The simulated startup traces (v_o and i_L) under zero initial conditions are shown in Fig. 4-18(a), and the corresponding steady-state waveforms are shown in Fig.4-18(b). It is seen from Fig. 4-18 that the simulated values of V_o *and* V_{o-} are about $\pm 83.3V$, which has a good agreement with the above theoretical analysis results.

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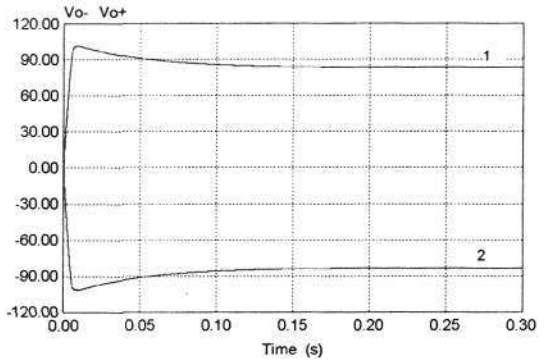
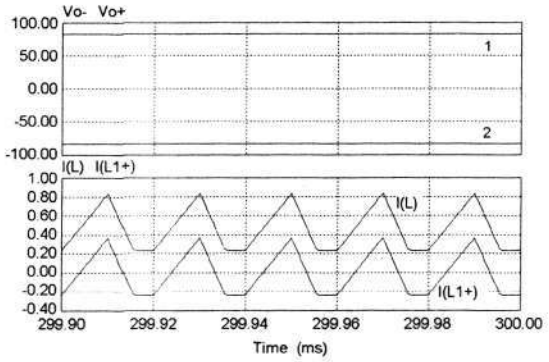


(a)



(b)

Fig. 4-18. DCM Simulation verification for the proposed converter

(a) simulated startup traces under zero initial conditions
(b) waveforms in the steady state

The parameters in the CCM case are chosen to construct the testing hardware circuit. Only a single n-channel MOSFET is used in the circuit. The corresponding experimental curves in the steady state are shown in Fig. 4-19 respectively. The curve shown in Channel 1 with 20V/Div corresponds to positive output v_{o+}, which is about *54V*. The curve shown in Channel 2 with 20V/Div corresponds to the negative output v_{o-}, which is also about *54V*. Considering the effects caused by the parasitic parameters, we can see that the measured results are very close to the theoretical analysis and simulation results.

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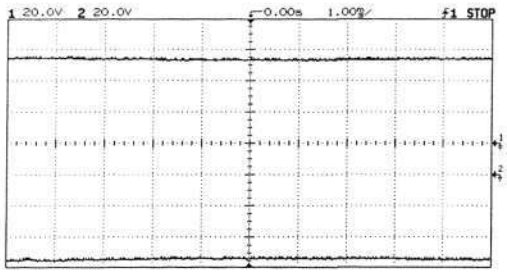

Fig. 4-19. Experimental verification for the proposed converter

4.5.4 Supplemental discussion on dynamics and control strategy

Similar to most dc-dc power converters, there exists a distinct voltage/current oscillation in all proposed circuits because of the absence of the close-loop controller, which will increase additional voltage/current stress of components. This will also cause low frequency current ripples in the source, and increase additional stability problems.

Take the CCM simulation case in Chapter 4.5.1 as the example. When D is changed from *0.5* to *0.66*, simulated curves of v_{o+}, v_{o-} and i_L of the elementary circuit are shown in Fig. 4-20. The steady-state results match the expected values, but the peak value of i_L is much higher than its average value during the steady state. In addition, some low frequency ripples are introduced into the inductor current i_L (source current), which decays very slowly. Therefore, all proposed circuits are advised to work with the close-loop control approaches to improve their practical transient performance, which is similar to the practical applications of classical dc-dc converters.

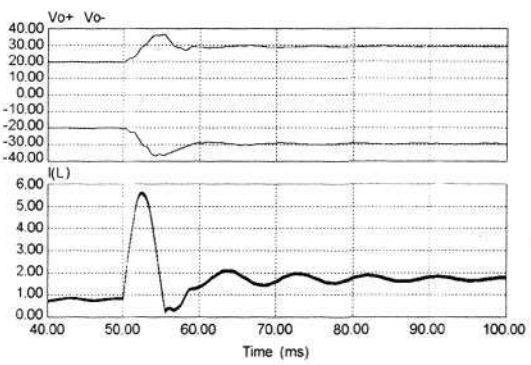

Fig. 4-20. Open-loop simulation results for the elementary circuit: response of v_{o+}, v_{o-} and i_L to the duty ratio change from *0.5* to *0.66*.

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For the convenience of the further study and applications, a brief introduction on simplified control strategies is given here. Since the symmetrical circuit structures and parameters of the positive and negative path with the same voltage conversion ratios may bring the symmetrical dynamics as previously stated, the mirror-symmetrical double outputs can be obtained by a single-switch control scheme in theory. Two basic dual-loop PI control schemes as shown in Fig. 4-21 have potentials for practical applications of proposed circuits. The classical dual-loop PI control method is adopted because that the inner inductor-current loop and the output-voltage loop has the advantage of very good voltage regulation.

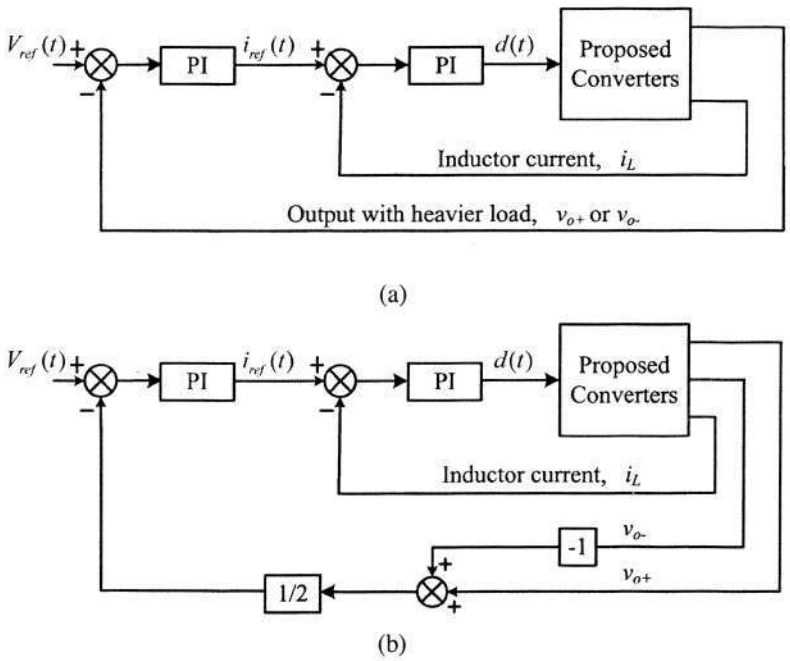

Fig. 4-21. General Description of dual-loop PI control schemes for proposed circuits.

(a) semi-regulated approach
(b) averaging voltage-mode approach

If the components of both paths are selected carefully, good symmetrical circuit parameters like as in the simulation cases can be obtained. Therefore, we can use the semi-regulated approach as shown in Fig. 4-21(a) directly to regulate one output with heavier load current through feedback control, and leave the other output unattended. The output with lighter load is cross-regulated through the output with heavier load, which may results in a dc regulation error. This error can be ignored due to the symmetrical characteristics of the circuit.

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If the circuit parameters of two paths have distinct differences that may lead to different dynamics and power losses, the approach shown in Fig. 4-21(b) can be applied to overcome the problems caused by the imbalanced load and circuit parameters. None of the output voltages can be precisely regulated, but the errors between the v_{o+}, v_{o-} and V_{ref} are redistributed according to the weighting factor *0.5*. For most cases, this approach can be regarded as an improved scheme of the semi-regulated approach [107-109].

Therefore, the close-loop regulation of proposed circuits can be easily implemented by above-mentioned two simple and straightforward approaches. They are helpful to decrease the complexity of the whole power converter system. The extensive studies into their effects and design considerations will be introduced in the future papers as a special topic.

For the CCM simulation case in Chapter 4.5.1, the circuit parameters of two paths are symmetrical. The semi-regulated approach (v_{o-} is used as the feedback variable) and the averaging voltage-mode approach are added, respectively. And the PI parameters are the same. It can be seen from Fig.4-22 that the response curves are basically in coincidence.

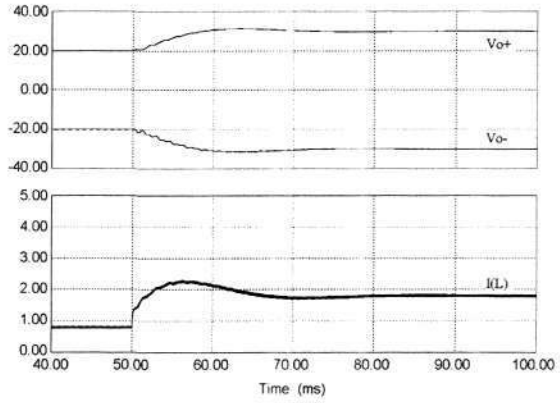

Fig. 4-22. Close-loop simulation results for the elementary circuit: response of v_{o+}, v_{o-} and i_L to the duty ratio change from *0.5* to *0.66*.

Therefore, only the semi-regulated control scheme in Fig. 4-21(a) is applied to the hardware prototype as the example. The reference output voltage V_{ref} is set as *20*V. During the startup process, we let $R_+ = R_- = 100\Omega$. Fig. 4-23(a) illustrates the experimental start-up curves of v_{o+} and v_{o-}. The curve shown in Channel 1 with 10V/Div corresponds to v_{o+}, and the curve shown in Channel 2 with 10V/Div corresponds to v_{o-}. We can see that

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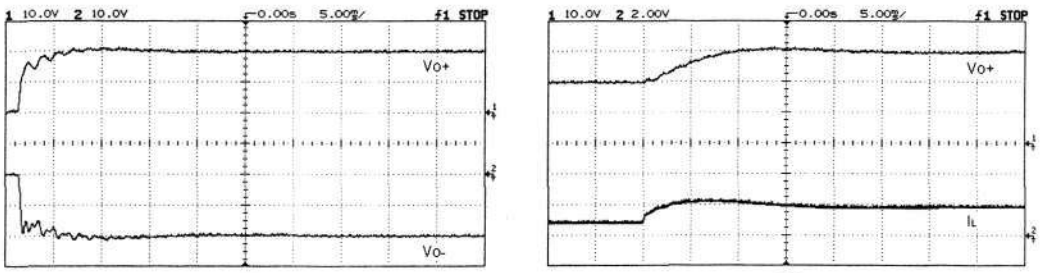
the oscillation as exhibited in Fig. 4-20 has been eliminated successfully. The steady-state output voltages have a good agreement with the expected results.

V_{ref} is increased from *20*V to *30*V to observe the voltage and current stress. The transient curves of v_{o+} and i_L are shown in Fig. 4-23(b), where Channel 1 with 10V/Div corresponds to v_{o+}, and Channel 2 with 2V/Div corresponds to i_L (*1:1*). Compared with the simulation curves shown in Fig. 4-20, it is seen that the transient performance of v_{o+} and i_L has been significantly improved, and the expected new steady state can be obtained smoothly and quickly.



(a) (b)

Fig. 4-23. Experimental results of response to V_{ref} with close-loop regulation.

(a) experimental start-up curves with close-loop regulation.
(b) experimental results of response to V_{ref} with close-loop regulation.

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Chapter 5 Positive Output Topology Construction Using Output Enhanced Circuits

From Chapter 2 to Chapter 4, novel positive, negative and double output dc-dc converters have been introduced, respectively. Since the positive output voltages are widely required in the various industrial areas, this chapter will specially introduce the applications of output enhanced circuits to the constructions of positive output topologies.

5.1 Introduction

Reviewing the energy conversion processes of the classical positive output dc-dc converters, we can see that output capacitor C_o widely exists in all kinds of topologies. The energy is transferred from the voltage source v_{in} to output capacitor C_o through the pump circuit in each cycle. The pump circuit is a major section of all dc-dc converters, and it consists of switches, diodes and passive components. Therefore, the general representation of a positive output converter can be referred to in Fig. 5-1. It is seen that the converter performs the characteristics of voltage conversion through two sections, the pump section and the output section. Usually, the output section consists of no component, and delivers the energy to load R from C_o directly in each cycle. The corresponding voltage transfer gains of each section are expressed by M_p and M_o, respectively. Hence, the voltage transfer gain of the whole converter is:

$$M = \frac{V_o}{V_{in}} = M_p M_o \tag{5.1}$$

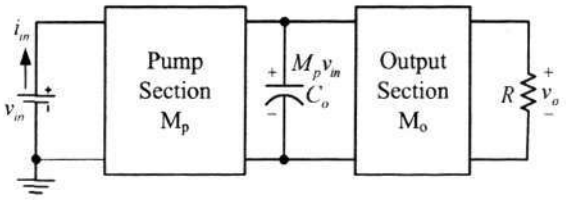

Fig. 5-1. General representation of a positive output dc-dc converter

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For example, the classical SEPIC converter is shown in Fig. 5-2. The pump section consists of S, D_o, L, L_1 and C_s, and M_p is equal to $D/(1-D)$. Since the output section consists of no component, M_o is equal to 1. Therefore, the voltage transfer gain of the whole SEPIC converter as shown in Fig. 5-2 is equal to the product of M_p and M_o.

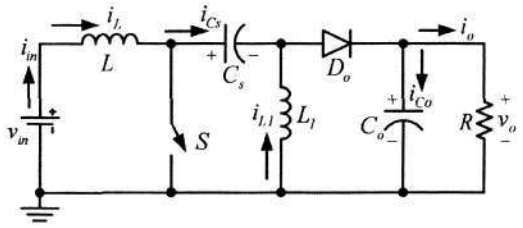

Fig. 5-2. Prototype of the SEPIC converter

For a given positive output dc-dc converter, if we maintain the relative position of each component and add several new components into the output section, the evolution of output section with higher voltage transfer gains will be obtained. The new topologies will keep basic advantages of the converter, and the voltage transfer gain of the entire circuit will be increased significantly according to (5.1).

To avoid the problems of the control complexity and the cost caused by multiple power switches and transformers, the evolution of the output section is realized by the VL technique in this chapter. A series of *output enhanced circuits* in the output section are utilized to the output improvement. They consist of capacitors and diodes, and share the same power switch with the pump section.

5.2 Review of Output Enhanced Circuits

In [3], F.L. Luo proposed a VL scheme using two diodes and two capacitors (D_1-D_2-C_1-C_2), and these components construct the prototype of a series of enhanced circuit (EC) as shown in Fig. 5-3.

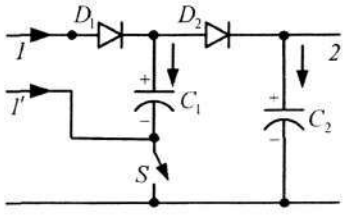

Fig. 5-3. Prototype of the enhanced circuit

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According to Fig. 5-3, C_1 is charged via node 1 during switch-on. During switch-off, the energy stored in C_1 is transferred via the path from node 1' to node 2, and the capacitor voltage V_{C2} will be $2V_{C1}$. It is a very powerful VL technique for enhancing the dc-dc converters' voltage transfer gains. Hence, based on the circuit in Fig. 5-3, a series of novel circuits connected with C_o are obtained in the output section in [3]. The first two circuits are shown in Figs. 5-4 and 5-5. To explain them conveniently, we call them double EC and triple EC, respectively. Fig. 5-6 corresponds to the generalized circuit for ready reference. A detailed introduction will be given in the following parts.

5.2.1 Double EC

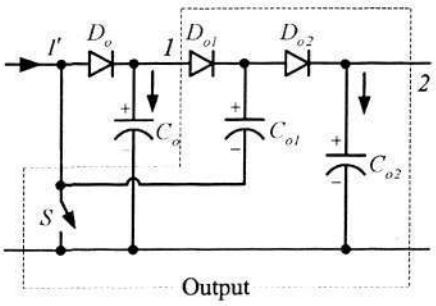

Fig. 5-4. Double EC

The double EC [3] is a basic VL cell, and circuit diagram is shown in Fig. 5-4. When switch S turn on, D_{o1} is on, D_o and D_{o2} are off. When S turn off, D_{o1} is off, D_o and D_{o2} are on. During switching-on, the voltage across capacitors C_{o1} is charged to V_{Co}. During switching-off, the potential of node *1'*, $V_{1'}$ is equal to V_{Co}, and the output capacitor voltage V_{Co2} is equal to $V_{1'}+V_{Co1}$. Since C_{o1} performs characteristics to lift V_{Co2} by V_{Co}, we have:

$$\begin{aligned} V_{Co1} &= V_{Co} \\ V_{Co2} &= 2V_{Co} \end{aligned} \tag{5.2}$$

From (5.2), it can be seen that the transfer gain of the output section M_o has been increased successfully from *1'* to *2*.

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5.2.2 Triple EC

The triple EC [3] is derived from the double EC by adding the components (D_{o3}-C_{o3}-D_{o4}-C_{o4}). It can be divided into two basic VL cells, and its circuit diagram is shown in Fig. 5-5. When switch S turn on, D_{o1} is on, D_o and D_{o2} are off. When S turn off, D_{o1} is off, D_o and D_{o2} are on.

During switching-on, the voltage across capacitors C_{o1} is charged to V_{Co}, and the voltage across capacitors C_{o3} is charged to V_{Co2}. During switching-off, the potential of node *1'*, $V_{1'}$ is equal to V_{Co}, and the capacitor voltage V_{Co4} is equal to $V_{1'}+V_{Co3}$. Since C_{o3} performs characteristics to lift V_{Co4} by V_{Co2}, we have:

$$\begin{aligned} V_{Co1} &= V_{Co} \\ V_{Co2} &= V_{Co3} = 2V_{Co} \\ V_{Co4} &= 3V_{Co} \end{aligned} \tag{5.3}$$

From (5.3), it can be seen that the transfer gain of the output section M_o has been increased successfully from *1'* to *3*.

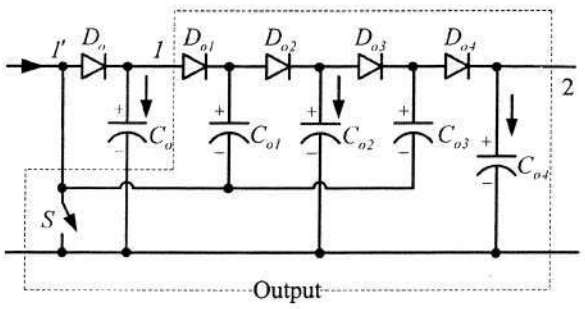

Fig. 5-5. Triple EC

5.2.3 Multiple EC

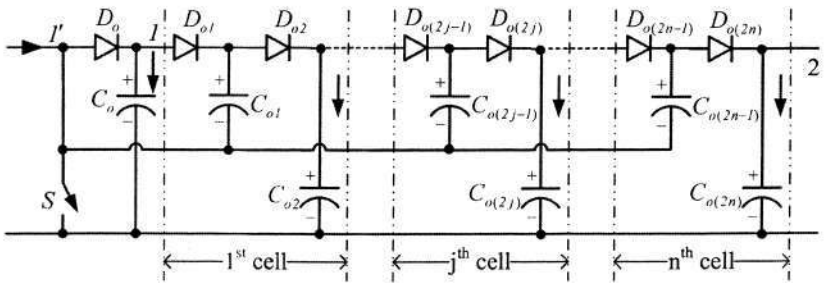

Fig. 5-6. Multiple EC

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Referring to Fig. 5-4 and 5-5, it is possible to construct the multiple EC by repeating the components (L_2-D_2-C_2-S_1). Assuming that there are n voltage lift cells, the generalized EC [3] is shown in Fig. 5-6. All circuits share the same power switch S, which simplify the control scheme and decrease the cost significantly. Hence, each circuit has one switch, $2n$ capacitors and $2n$ diodes. All the capacitors are sufficiently large. From the foregoing analysis and calculation, the general formulas for all ECs can be obtained as below:

$$\begin{aligned} V_{Co(2n-1)} &= nV_{Co} \\ V_{Co(2n)} &= (n+1)V_{Co} \end{aligned} \tag{5.4}$$

The voltage transfer gains of the output section for all ECs are equal to $(n+1)$. The evolution of the output section has been realized successfully.

5.2.4 On the power switch of ECs

Through the foregoing review of output ECs, it is seen that the single switch structure is a main advantage of all ECs. As shown in Fig. 5-6, switch S is paralleled with D_o-C_o. When an EC is integrated with a dc-dc converter, how can we obtain a single switch structure by merging them? In practical applications, the position of the active power switch in the dc-dc converter should be considered before an EC is applied to the dc-dc converter. Therefore, the general guidelines for new circuit construction with ECs are given as follows:

- In some cases, if the active power switch in the dc-dc converter is paralleled with D_o-C_o, the EC can share this active power switch with the dc-dc converter.
- In some cases, if a passive power switch (diode) in the dc-dc converter is anti-paralleled with D_o-C_o, the active power switch in the dc-dc converter can not be used directly in the ECs. S as shown in Fig. 5-6 can be replaced by the anti-paralleled diode of the dc-dc converter to obtain the single switch structure.

In the following parts, two different cases are given to demonstrate the above guidelines of ECs.

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5.3 Applications to the Boost Converter

The classical boost converter is shown in Fig. 5-7. The pump section of the boost converter consists of L, S and D_o. Since S in the pump section is paralleled with D_o-C_o, according to the general guidelines introduced in Section 5.2, S in the EC can be the same active power switch power of the boost converter. Combining the pump section with the double EC, we can get a developed dc-dc topology as shown in Fig. 5-8.

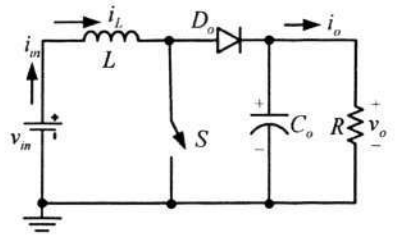

Fig. 5-7. The boost converters

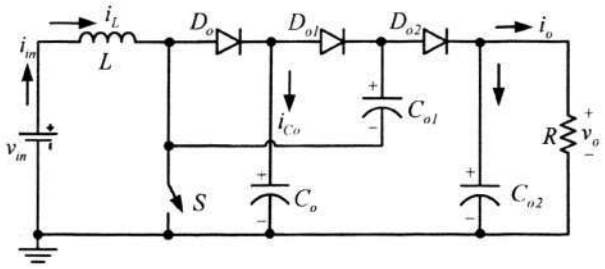

Fig. 5-8. The boost converter with a double EC

Therefore, according to (5.1) and (5.2) the voltage transfer gain of the boost converter with a double EC is

$$M = \frac{V_{Co2}}{V_{in}} = \frac{1}{1-D} \times 2 = \frac{2}{1-D} \tag{5.5}$$

Analogously, the boost converter with a triple EC is proposed and shown in Fig. 5-9. Therefore, the voltage transfer gain of the boost converter with a triple EC is

$$M = \frac{V_{Co4}}{V_{in}} = \frac{1}{1-D} \times 3 = \frac{3}{1-D} \tag{5.6}$$

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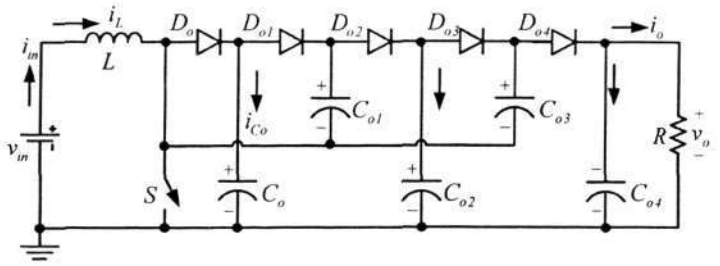

Fig. 5-9. The boost converter with a triple EC

5.4 Applications to the VL-type SEPIC Converters

The self-lift circuit of the VL-type SEPIC converters is shown in Fig. 5-10, and it has been analyzed in detail in Section 2. The pump section of the self-lift converter consists of L, S, C_s, L_1, C_1, D_1 and D_o. However, for the combination of the pump section and output section, there is no overlap for these two sections, and two separate active power switches are required.

According to the general guidelines introduced in Chapter 5.2, it is found that D_1 in the pump section is anti-paralleled with D_o-C_o, so S in the EC can be replaced by D_1 directly. Combining the pump section with the double EC, we can get the new dc-dc topology as shown in Fig. 5-11. Here, D_1 can be regarded as a synchronous passive power switch.

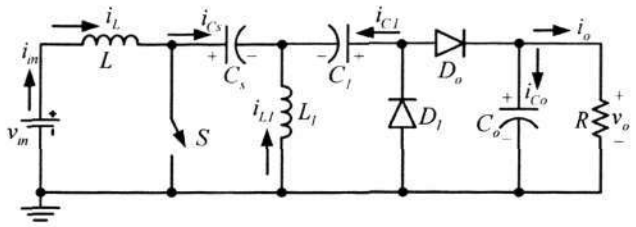

Fig. 5-10. Topology of the self-lift circuit

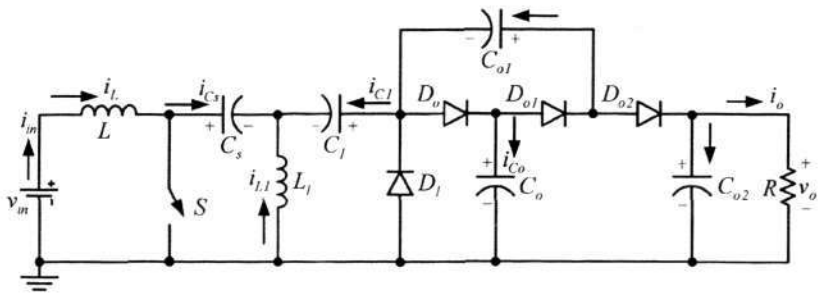

Fig. 5-11. Self-lift circuit of VL-type SEPIC converters with a double EC

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Therefore, according to (5.1) and (5.2), the voltage transfer gain of the self-lift circuit of VL-type SEPIC converters with a double EC is

$$M = \frac{V_{Co2}}{V_{in}} = \frac{1}{1-D} \times 2 = \frac{2}{1-D} \tag{5.7}$$

Analogously, triple-lift circuit of VL-type SEPIC converters with a double EC is proposed and shown in Fig. 5-12. The pump section of the triple-lift circuit consists of C_s, S, S_1, D_o and three VL cells. Since D_1, D_2 and D_4 are connected in series, they can be regarded as an equivalent active power switch when an EC is applied to the pump section. Then, S in the EC is replaced by the equivalent passive power switch of D_1-D_2-D_4. Therefore, according to (5.1) and (5.2), the voltage transfer gain of the triple-lift circuit of VL-type SEPIC converters with a double EC is

$$M = \frac{V_{Co2}}{V_{in}} = \frac{3}{1-D} \times 2 = \frac{6}{1-D} \tag{5.8}$$

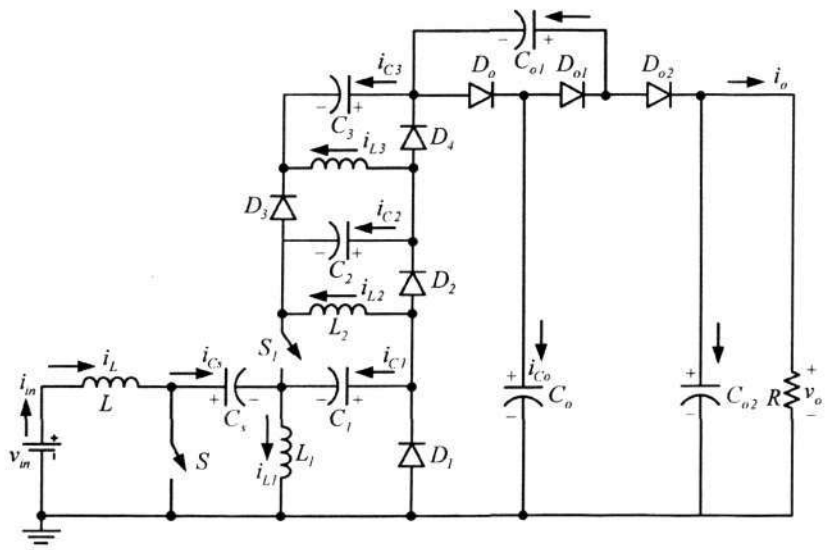

Fig. 5-12. Triple-lift circuit of VL-type SEPIC converters with a double EC

Since the evolution of the output section has been realized, the different configuration of each section and their combination will result in several new dc-dc topologies, which can be referred to in Fig. 5-13.

Assuming that the numbers of VL cells existing in the pump and output sections are n_p and n_o, respectively. All the new topologies can be unified and termed VL-type SEPIC

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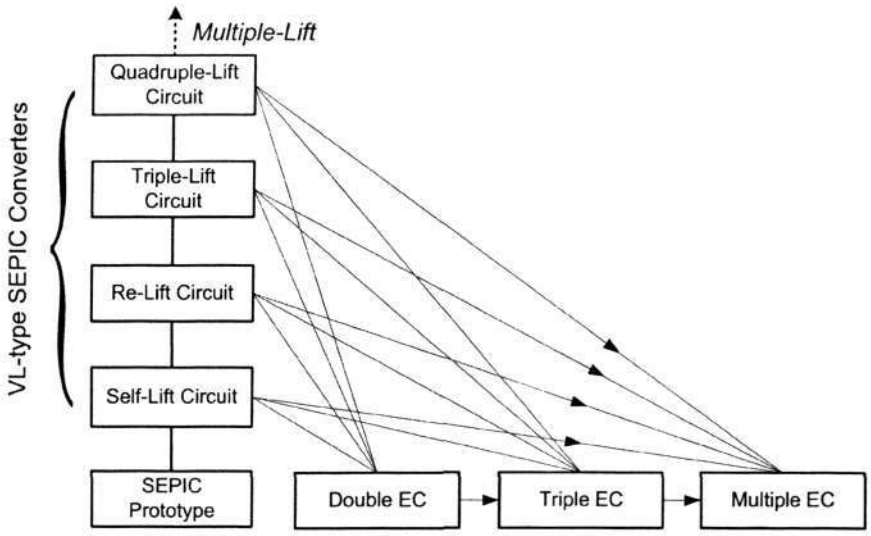

Fig. 5-13. Combination of VL-type SEPIC converters with output enhanced circuits

converters. From the analysis in previous Sections we have the common formula to calculate the voltage transfer gain as below:

$$M = \frac{V_o}{V_{in}} = M_p M_o = \frac{[n_p + h(n_p)D^{h(n_p)}](n_o + 1)}{(1-D)} \tag{5.9}$$

Where: $h(n_2) = \begin{cases} 1 & n_p = 0 \\ 0 & n_p > 0 \end{cases}$

When $n_p = n_o = 0$, the unified topology degenerates to the prototype of the SEPIC converter as shown in Fig. 5-1. Hence, from (5.9) we get

$$M = \frac{V_o}{V_{in}} = \frac{D}{1-D} = M_{SEPIC} \tag{5.10}$$

When $n_o = 0$ and $n_p \geq 1$, the generated converters can be termed main series of VL-type SEPIC converters. Hence, from (5.9) we get

$$M = \frac{V_o}{V_{in}} = \frac{n_p}{(1-D)} = M_{main} \tag{5.11}$$

The other generated converters can be termed enhanced series.

Therefore, the total number of components is:

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Active power switch: $\begin{cases} 1 & n_p = 0,1 \\ 2 & n_p > 1 \end{cases}$

Passive switches (diodes): $2n_p + 2n_o - 1$

Inductors: $n_p + 1$

Capacitors: $n_p + 2n_o + 2$

5.5 Simulation and Experimental Results

To verify the design and theoretical calculation results, Psim simulation package was applied to these converters. The testing circuits for typical topologies were constructed to compare with simulation results.

5.5.1 The boost converter with a triple EC

The generated topology is shown in Fig. 5-8. The circuit parameters for simulation are: V_{in}=10V, R=100Ω, L=500μH, C_{o1}=C_{o2}=22μF, C_o=47μF and D=0.6. The switching frequency f is 100kHz. All the diodes and the switch are ideal. From the analysis in the previous parts, the theoretical values are

$$V_o = MV_{in} = \frac{2}{1-D} V_{in}\Big|_{D=0.6} = 50V \tag{5.12}$$

$$V_{Co} = M_p V_{in} = \frac{1}{1-D} V_{in}\Big|_{D=0.6} = 25V \tag{5.13}$$

The simulation results are shown in Fig. 5-14, where curve 1 and 2 are for v_o and v_{Co}, respectively. The steady-state performance in the simulation is identically matching the theoretical analysis.

In the hardware testing circuit, we still choose the same parameters. The n-channel MOSFET 2SK2267 is selected as the power switches S. The drain-source on resistance is 8mΩ, which is near the ideal condition. The diodes are realized by using MBR6045WT and MBRB20200CT. Thus, the practical output voltage is smaller than the theoretical value due to the effects caused by parasitic parameters. The corresponding experimental

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curves in the steady state are shown in Fig. 5-15. After careful measurement, we obtained the output voltage value of V_o shown in Channel 1 (50V/Div) and capacitor value of V_{Cs} shown in Channel 1 (50V/Div). It is seen that the measured results are very close to the theoretical analysis and simulation results.

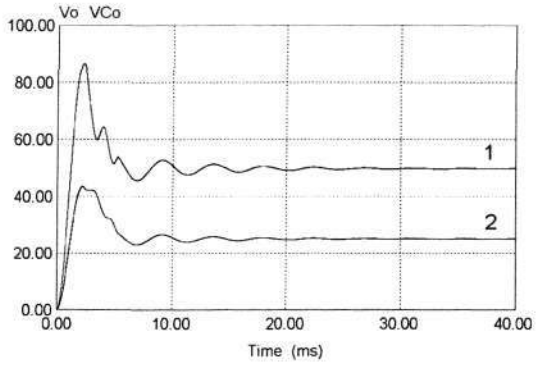

Fig. 5-14. Simulation verification for the proposed converter

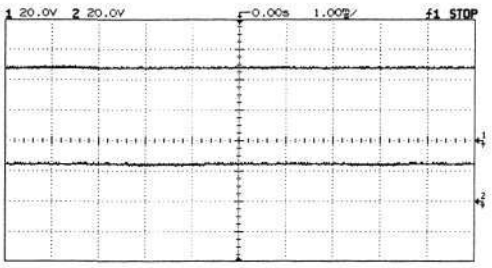

Fig. 5-15. Experimental verification for the proposed converter

5.5.2 Triple-lift circuit of VL-type SEPIC converters with a double EC

The generated topology is shown in Fig. 5-12. Since $n_p>1$, two active power switches are configured. The circuit parameters for simulation are: $V_{in}=10V$, $R=1k\Omega$, $L=L_1=L_2=L_3=500\mu H$, $C_s=110\mu F$, $C_1=C_{o1}=C_{o2}=22\mu F$, $C_o=47\mu F$, and $D=0.6$. The switching frequency f is $100kHz$. All the diodes and the switch are ideal. From the analysis in previous Sections, the theoretical values are

$$V_o = MV_{in} = \frac{6}{1-D}V_{in}\Big|_{D=0.6} = 150V \tag{5.14}$$

$$V_{Co} = M_p V_{in} = \frac{3}{1-D}V_{in}\Big|_{D=0.6} = 75V \tag{5.15}$$

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The simulation results are shown in Fig. 5-16, where curve 1-3 are for v_o, v_{Co} and v_{Cs}, respectively. The steady-state performance in the simulation is identically matching the theoretical analysis.

In the hardware testing circuit, we still choose the same parameters. The n-channel MOSFET 2SK2267 is selected as the power switches S and S_1. The drain-source on resistance is $8m\Omega$, which is near the ideal condition. The diodes are realized by using MBR6045WT and MBRB20200CT. Thus, the practical output voltage is smaller than the theoretical value due to the effects caused by parasitic parameters. The corresponding experimental curves in the steady state are shown in Fig. 5-17. After careful measurement, we obtained the output voltage value of V_o shown in Channel 1 (50V/Div) and capacitor value of V_{Cs} shown in Channel 2 (50V/Div). It is seen that the measured results are very close to the theoretical analysis and simulation results.

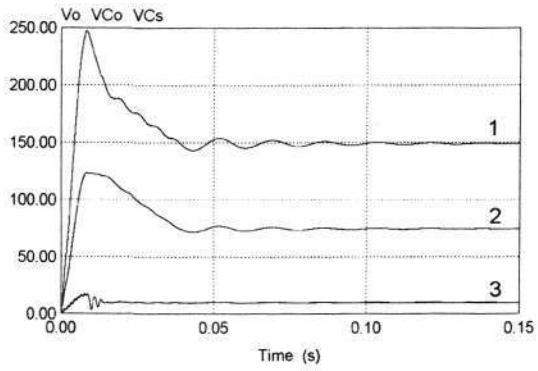

Fig. 5-16. Simulation verification for the proposed converter

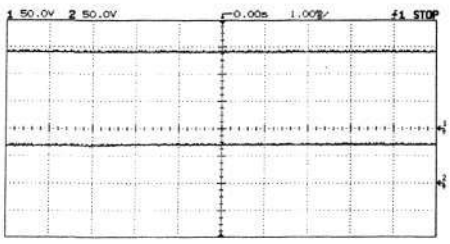

Fig. 5-17. Experimental verification for the proposed converter

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Chapter 6 Graphical Analytical Methods of Complex Topologies

6.1 Introduction

Many analytical and modelling methods for power dc-dc converters have been reported in recent decades. The main methods include state-space averaging, the equivalent duty ratio method, the average-switch model, and the loss-free resistor model [11-21, 66-70]. Although all of these modelling methods have been discussed and applied to many cases, they are still rather tedious for the circuit designers, especially when the converter circuit contains a large number of elements or many power stages. Besides, the linearized models, derived from these traditional methods, can only predict the small-signal stability rather than the large-signal stability information. Therefore, graphical analytical methods have been introduced for modelling some complex dc-dc topologies.

Signal flow graph (SFG) is a classical analytical approach. It consists of a number of "nodes" representing system variables or signals, and they are connected by "branches" that are the dynamic connections between these nodes. The branches are labeled with signal gains or transfer functions.

For a variable-structure nonlinear system, sub-flow graphs can be drawn according to the corresponding sub-networks. Then these sub-flow graphs will be combined together by weighted summation. This is so-called *switching-signal flow graph* (SSFG) method, and it is applied successfully into the modeling of simple dc-dc topologies in the past ten years [22-27].

For a given switching converter operating in CCM, there are only two switching sub-networks in each cycle. According to the basic rules of SSFG theory for switching networks, two SFGs G_1 and G_2 are drawn from the operation modes of the converter,

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which correspond to switching-on and switching-off respectively. Then these two sub-graphs are combined to form such a switching SFG as follows:

$$G = kG_1 + \bar{k}G_2 \tag{6.1}$$

Where: k and $\bar{k}$ are switching functions

$$k = \begin{cases} 1 & 0 < t < dT \\ 0 & otherwise \end{cases}$$

$$\bar{k} = 1 - k$$

Equation (6.1) introduces two basic switching branches, k branch and $\bar{k}$ branch. The corresponding transmittance of the k branch is equal to the duty ratio d while the corresponding transmittance of the $\bar{k}$ branch is equal to (1-d), which is usually expressed by $\bar{d}$. The steady-state model, large- and small-signal models of the converter can be obtained from G by the systematic procedure. It is noted that the transmittance labeled on the branch is a real gain or complex gain between two nodes. Such gains can be expressed in terms of the transfer function between two nodes.

6.2 SSFG and Complex DC-DC Topologies

The requirement for high voltage transfer gains with transformerless structures stimulates the development of high order complex dc-dc topologies. According to the voltage conversion mechanism, complex transformerless dc-dc converters are classified into two kinds as follows:

- Multiple-switch cascade converters
- VL-type converters

The general representation of multi-switch cascade converters is shown in Fig. 6-1(a), in which classical low order dc-dc converters such as boost and buck converters are usually utilized as series power stages. In recent years, the SSFG modeling method for multiple-switch cascade dc-dc converters has been explored by Veerachary [24, 25], and generalized graphical models are successfully derived to describe the steady-state information and dynamics.

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The general representation of VL-type converters integrating multiple functional VL cells is shown in Fig. 6-1(b) for comparison with multi-switch cascade converters. The functional cells in Fig. 6-1(b) can be various VL cells. As introduced in Chapter 2, 3, 4 and [3], advanced VL cells perform the function to boost the output voltage in proposed circuits, and the number of required active power switch is *1* or *2*. Can we utilize the SSFG method directly to model these VL-type complex dc-dc converters? In the following parts of this chapter, this question will be discussed.

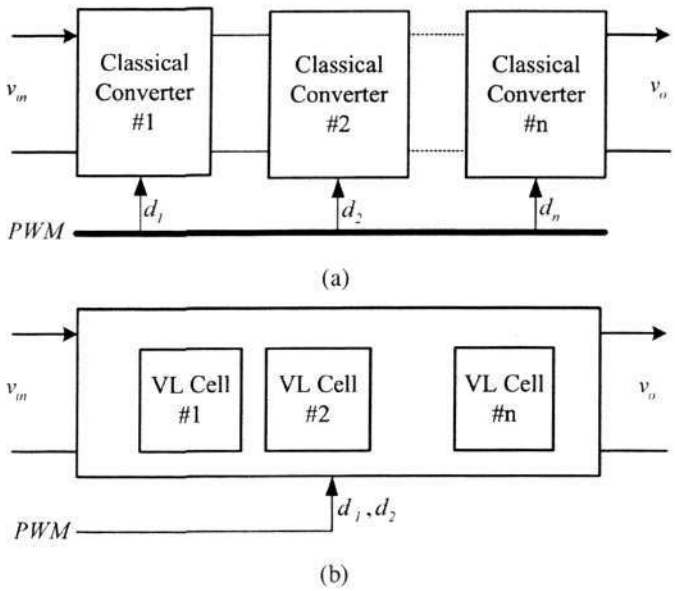

Fig. 6-1. Comparison of complex dc-dc converters

(a) multiple-switch cascade converter
(b) VL-type converter integrating multiple functional cells

It is unfortunately that above SSFG method developed by Veerachary cannot be applied to VL-type complex dc-dc topologies. The reasons are as follows:

- The VL-type topologies avoid the complex control schemes, but more diodes are introduced. The decreasing of the active power switches result in the increasing of passive power switches in theory. The effects caused by diodes have not been considered in Veerachary's SSFG method.
- The functional cells in VL-type topologies are totally different from those classical low order dc-dc converters utilized as power stages in multiple-switch topologies. For example, the VL cell is usually a switched-mode charge-discharge circuit consisting of inductors and capacitors, but Veerachary's SSFG method didn't discuss this special problem.

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Therefore, it is necessary to develop Veerachary's SSFG method to provide a systemic procedure for VL-type complex dc-dc topologies. In the following parts, as a series of typical VL-type complex dc-dc topologies, *super-lift dc-dc converters* are to be taken as the example.

A *developed SSFG* method is thus presented based on the operation characteristics of the VL cells existing in the super-lift converters. Since the developed SSFG method is a combination of conventional SSFG and the special characteristics of VL cells, the following discussion and analysis are carried out under such assumptions as:

(a) The converter is working in the continuous conduction mode (CCM). The power losses are represented by the equivalent series resistance (ESR) of each inductor.
(b) The ESR of the capacitor and stray capacitances are neglected except the output capacitor.
(c) All capacitors are large enough that the ripple voltage across the capacitors can be negligible in one cycle for the average value discussion.
(d) The switching operation of the power switch is ideal.
(e) All the forward voltage drop values of diodes are the same and defined as V_D.
(f) The filter corner frequency is much smaller than the switching frequency f.

6.3 Developed SSFG Method for Super-Lift Converters

The super-lift dc-dc converters [51] are a series of advanced step-up dc-dc power conversion topologies that are based on the VL technique. Compared with the conventional dc-dc converters, super-lift converters can implement the output voltage increasing stage by stage along the geometric progression and obtain the higher voltage transfer gain. They are divided into many categories according to the number of VL cells, such as the elementary circuit (single VL cell), re-lift circuit (two VL cells), triple-lift circuit (three VL cells) etc. Assuming that there are n VL cells connected in series for voltage lift, we get the generalized topology of the super-lift converters as shown in Fig. 6-2(a). The circuit has only one switch, n inductors, $2n$ capacitors, and $(3n-1)$ diodes.

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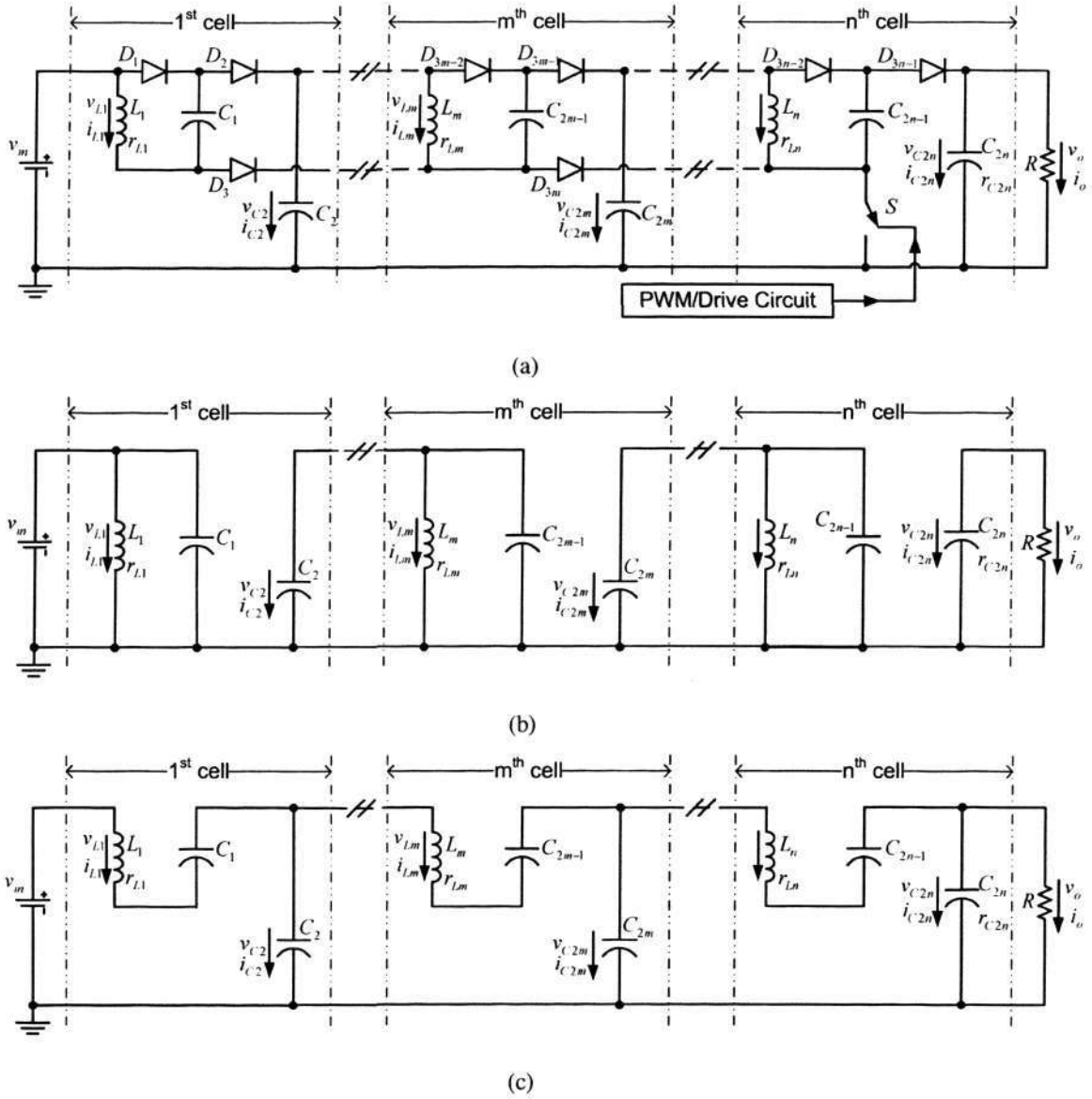

Fig. 6-2. Generalized topology of the super-lift converter with *n* VL cells

(a) topology
(b) equivalent circuit during switching-on
(c) equivalent circuit during switching-off

Obviously, it is different from the topology of conventional cascade boost converters due to its topology and operation principles. The number of active power switches in the conventional cascade boost converters is n (n power stages); however, only one active power switch is required in this circuit. In addition, more diodes (passive switches) are involved in the process of network switching. When switch S turns on, D_1, D_3, D_4, $D_6 \ldots D_{3m-2}$, $D_{3m} \ldots D_{3n-2}$ are on, and D_2, $D_5 \ldots D_{3m-1} \ldots D_{3n-1}$ are off. When S turns off, D_1,

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D_3, D_4, D_6…D_{3m-2}, D_{3m}… D_{3n-2} are off, and D_2, D_5…D_{3m-1}… D_{3n-1} are on. The equivalent circuits during switching-on and –off are shown in Fig. 6-2(b) and (c), respectively.

6.3.1 General Principles for Super-Lift Converters

For drawing the SSFG of a super-lift converter with n VL cells, the developed method presents the following several general guidelines:

A. Guidelines for nodes configuration

Neglecting the definition for the voltage and current nodes of each storage capacitor (C_1, C_3…C_{2n-1}) in the pump circuits, we define the sequence of the basic nodes, which are determined according to the sequence of the elements appearing in the circuit, inductor (L_1, L_2…L_n) or support capacitor (C_2, C_4…C_{2n}). Each inductor current node i_{Lm} is connected from its corresponding inductor voltage node v_{Lm} and the transmittance has considered the ESR of each inductor expressed by $1/(sL_m + r_{Lm})$. Each capacitor voltage node v_{C2m} is connected from its corresponding capacitor current node i_{C2m}, and the transmittance is expressed by $1/(sC_{2m})$.

B. Guidelines for drawing SFG of switching-on

The corresponding SFG for switching-on, G_1 is shown in Fig. 6-3(a). For the switching-on mode shown in Fig. 6-2(b), the charging process of each capacitor in the pump circuit can be neglected. It is due to the above-mentioned assumption (c). Therefore, these storage capacitors, C_1, C_3,…,C_{2n-1}, are taken as voltage controlled voltage sources (VCCS) in the SFG and the voltage values across them are defined as a series of voltage nodes. These nodes are determined directly by the input source node v_{in} and the corresponding voltage nodes of support capacitors (C_2, C_4,…C_{2n-2}). Then the number of the capacitors considered in the SFG has been reduced by *50%*.

Check the connection branches existing in the switching-on mode. Since the capacitor charging current of in each pump circuit is neglected, this neglected current should be reconsidered when the current feedback loop from the node of i_{Lm} to the node $i_{C(2m-2)}$ is being constructed. The support capacitor C_{2m-2} charges L_m and C_{2m-1} simultaneously, so a

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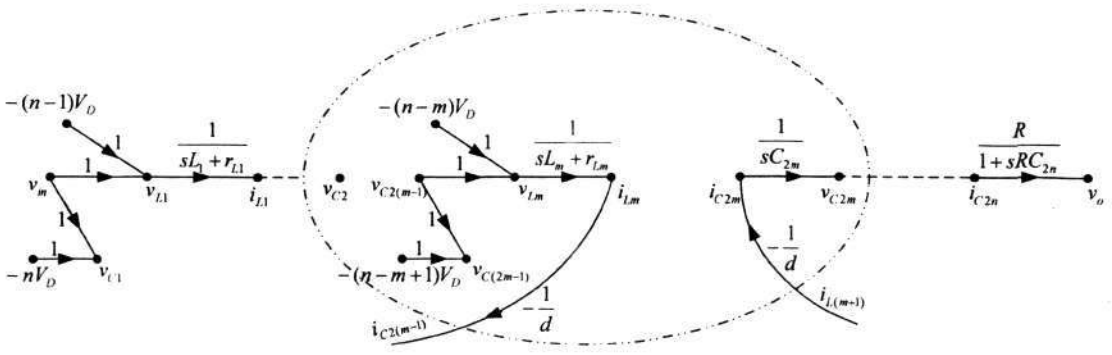
transmittance labeled on the current feedback branch is added to reflect the summation of charging current i_{Lm} and $i_{C(2m-1)}$. For super-lift converters, we have $I_{C2(m-1)} = D^{-1} I_{Lm}$ in the steady state. So the proposed transmittance is equal to $-d^{-1}$.

In addition, the effects caused by the forward voltage drop of diodes are defined as a series of dc source voltage nodes. They are used to modify the practical voltage value of each passive element. For example, the voltage node $-(n-1)V_D$ is added and connected with the node v_{L1} because the total voltage drop caused by diodes during the process of charging L_1 is equal to $(n-1)V_D$.

C. Guideline for drawing SFG of switching-off

The corresponding SFG for switching-off, G_2 is shown in Fig. 6-3(b). For the switching-off mode shown in Fig. 6-2(c), the effects caused by the forward voltage drop of diodes are defined as some another source nodes. This is due to the different conduction paths in the switching-on and switching off modes, which contain different diodes. For example, a new voltage node, $-V_D$ is added and connected with the node v_{L1} which has never been considered by the conventional methods.

Check the connection branches existing in the switching-off mode. The transmittance labeled on the current feedback branch is changed to -1 because L_m and C_{2m-1} are connected in series during switching-off. It means neglecting i_{C2m-1} need not any additional correction on the current feedback branch from the node of i_{Lm} to the node $i_{C(2m-2)}$.



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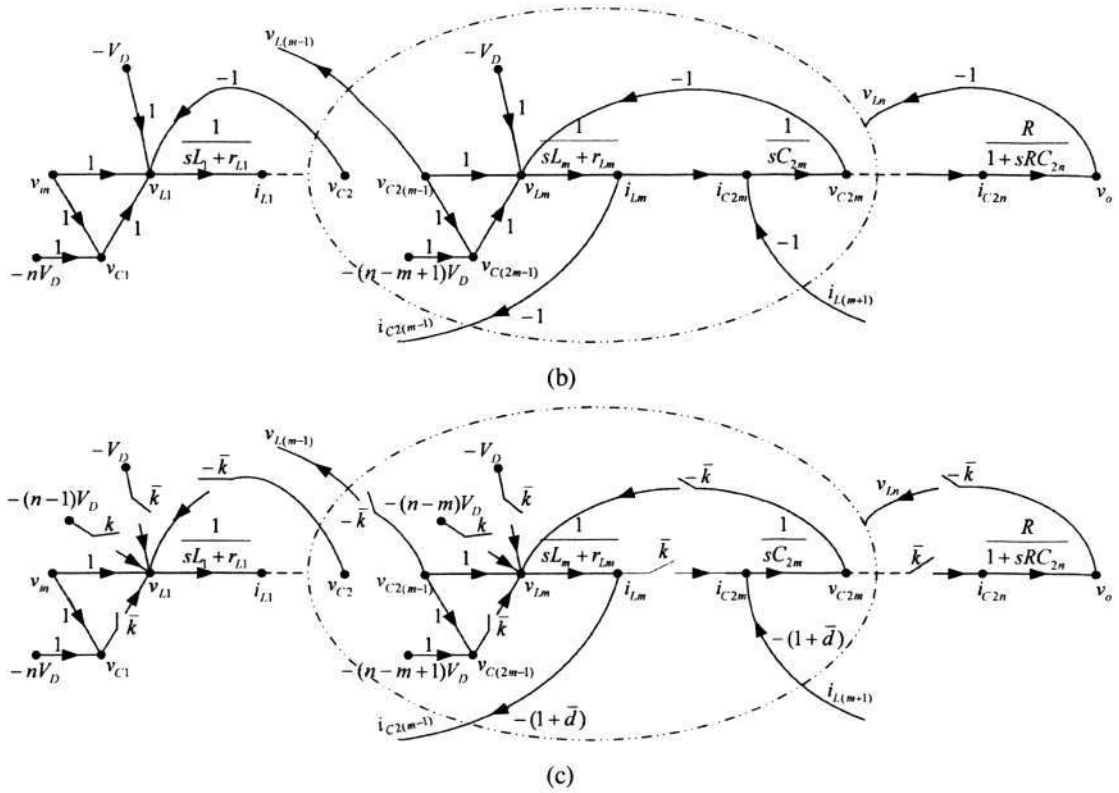

Fig. 6-3. Unified SSFG of the super-lift converter with *n* VL cells

(a) switching-on
(b) switching-off
(c) unified SSFG

D. Guidelines for drawing the SSFG

The unified SSFG is drawn by merging G_1 and G_2 according to (6.1), and is shown in Fig. 6-3(c). Many source nodes are added due to the modelling of diodes. Then we can check and perform some primary predigestion such as branch moving or reducing the parallel braches that shares the same nodes. Two sorts of source nodes, v_{in} and $-V_D$ are distributed in the different positions of the graph. Furthermore, it will result in several new switching branches which can be described by the generalized expressions, $(\alpha k+\beta)$ and $(\alpha \bar{k}+\beta)$. Here, α and β are two generalized and fixed parameters. α is produced by the predigestion of diodes' voltage nodes and β is produced by the predigestion of sharing branches in sub-graphs. They will be illustrated in the following sub-section about modelling examples. Because we have $(-d^{-1})\times d+(-1)\times \bar{d}=-(1+\bar{d})$, the transmittance labeled on the current feedback branch is merged to $-(1+\bar{d})$.

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E. Guidelines for graph analysis

In the obtained SSFG, the source nodes correspond to the source voltage and voltage drop caused by diodes. The mixed nodes correspond to the state variables. Each mixed node can be regarded as a sink node to perform the graph analysis when the relations between this variable and source voltage are investigated. The main computer simulation packages are TUTSIM and Matlab. The detailed graph analysis depends on the derivation of steady-state, large- and small-signal models from the SSFG, which will be introduced in the following parts.

F. Derivation of large-signal models and steady-state model

The SSFG can be utilized to derive the graphical representation of large-signal and steady-state model by substituting for switching branches existing in the graph. Here, the switching branches in the SSFG will be developed to the branches with the averaging transmittance. For super-lift converters, the averaging transmittance of their generalized switching branches are $(\alpha d + \beta)$ and $(\alpha \bar{d} + \beta)$, respectively. Hence, the corresponding large-signals carried through the switching branches can be expressed by:

$$y(s) = (\alpha d + \beta)x(s) \qquad \text{for } \alpha k + \beta \text{ branch} \tag{6.2}$$

$$y(s) = [\alpha(1-d) + \beta]x(s) \qquad \text{for } \alpha \bar{k} + \beta \text{ branch} \tag{6.3}$$

Where: x and y represent the input and output nodes (signals) of the switching branch.

The graphical representations of (6.2) and (6.3) are substituted for the switching branches in the SSFG as shown in Fig. 6-3(c). Then, the graphical representation of the linear large-signal model in the s-domain is obtained directly.

It is convenient to obtain the steady-state model from the aforementioned large-signal model. In the graphical representation of the large-signal model, all the source nodes are assumed constant and all the mixed nodes (state variables) are fixed to their average values. In addition, all the transmittances labeled on the branches are simplified by setting $s \rightarrow 0$. Then the graphical representation of the steady-state model is obtained, which are used to derive the steady-state information.

G. Derivation of small-signal models

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From the large-signal expressions (6.2) and (6.3) presented in the previous part, the corresponding small-signal expressions for the generalized switching branches can be derived. It is assumed that there exist small perturbations $\hat{x}(t)$, $\hat{d}(t)$ and $\hat{y}(t)$ near the operating point X, D and Y, i.e.

$$d(t) = D + \hat{d}(t) \tag{6.4}$$

$$x(t) = X + \hat{x}(t) \tag{6.5}$$

$$y(t) = Y + \hat{y}(t) \tag{6.6}$$

The time domain expression of (6.2) and (6.3) are

$$y(t) = (\alpha d + \beta)x(t) \qquad \text{for } \alpha k + \beta \text{ branch} \tag{6.7}$$

$$y(t) = [\alpha(1-d) + \beta]x(t) \qquad \text{for } \alpha\bar{k} + \beta \text{ branch} \tag{6.8}$$

Substituting (6.4), (6.5), and (6.6) into (6.7) and (6.8), we get the following equations:

$$Y + \hat{y}(t) = (X + \hat{x}(t))[\alpha(D + \hat{d}(t)) + \beta] \tag{6.9}$$

$$Y + \hat{y}(t) = (X + \hat{x}(t))[\alpha(1 - D - \hat{d}(t)) + \beta] \tag{6.10}$$

Neglecting the second-order perturbations and performing Laplace transformation, we get the corresponding small-signals carried through the switching branches expressed by:

$$\hat{y}(s) = \alpha X\hat{d}(s) + (\alpha D + \beta)\hat{x}(s) \qquad \text{for } k + \lambda \text{ branch} \tag{6.11}$$

$$\hat{y}(s) = -\alpha X\hat{d}(s) + [\alpha(1-D) + \beta]\hat{x}(s) \qquad \text{for } \bar{k} + \lambda \text{ branch} \tag{6.12}$$

The graphical representations of (6.11) and (6.12) are substituted for the switching branches in the SSFG, which can obtain the graphical representation of the linear small-signal model in the s-domain.

6.3.2 Example: modelling and analysis of the elementary circuit

In this sub-section, the proposed method will be applied to the modelling and analysis of the elementary circuit. Both the parasitic parameters and forward voltage drop of diodes are considered. Both the simulation results in Pspice and experimental results are given to verify the analytical results of proposed method.

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A. Derivation

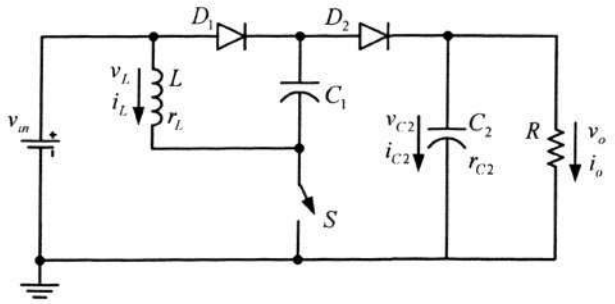
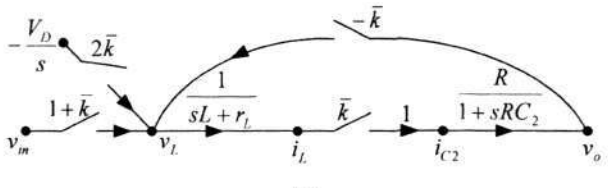


Fig. 6-4. Topology of the elementary circuit of super-lift converters (with one VL cell)

The elementary circuit is shown in Fig. 6-4, where state variables and directions are indicated. The SSFG of the elementary circuit is drawn from Fig. 6-3(c), which has been predigested as shown in Fig. 6-5(a). There are two generalized switching branches in Fig.6-5(a). One is $(\bar{k}+1)$, where the corresponding parameters $\alpha=\beta=1$. The other is $(2\bar{k})$, where the corresponding parameters $\alpha=2$ and $\beta=0$. In addition, there are two source nodes, v_{in} and $-V_D$ ($-V_D/s$ is the expression in the s-domain) distributed in it. We get the graphical expression of the large-signal model according to the proposed method as shown in Fig. 6-5(b). It can be programmed in the TUTSIM or Matlab to observe the large-signal transient performance directly. For example, to get the steady-state information of V_o/V_{in}, assuming $s\to 0$ and using graph reduction techniques, we analyze the graph from two individual paths which start from different source nodes and end at the same mixed node. We have:

$$\frac{V_o}{V_{in}}=\frac{v_o(s)}{v_{in}(s)}\bigg|_{s\to 0}+\frac{v_o(s)}{-v_D(s)}\bigg|_{s\to 0}\times(-\frac{V_D}{V_{in}}) \tag{6.13}$$

The result obtained from (6.13) is tabulated in Table 6-1 with the other main steady-state information. The ideal performance of the elementary circuit is also provided for the reference.



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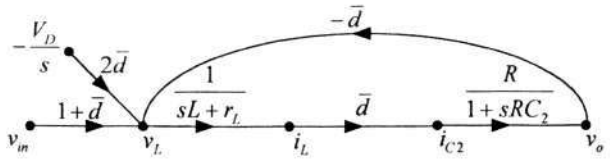

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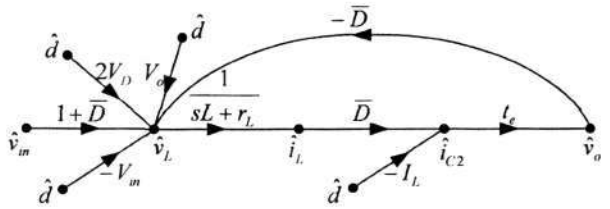

Where: $t_e = \frac{R(1+sCr_{C2})}{1+sC(R+r_{C2})}$

(c)

Fig. 6-5. Modelling of the Elementary Circuit of Super-lift converters

(a) SSFG
(b) large-signal model
(c) small-signal model

Table 6-1 Steady-state performance of the elementary circuit (super-lift converters)

	Nonideal Performance	Ideal Performance
$\frac{V_o}{V_{in}}$	$\frac{1+\bar{D}}{\Phi_E}-\theta\frac{2\bar{D}}{\Phi_E}$	$\frac{1+\bar{D}}{\bar{D}}$
$\frac{I_L}{V_{in}}$	$\frac{1+\bar{D}}{\bar{D}R\Phi_E}-\theta\frac{2}{R\Phi_E}$	$\frac{1+\bar{D}}{\bar{D}^2R}$

Where: $\theta=\frac{V_D}{V_{in}}$ and $\Phi_E=\frac{r_L}{R\bar{D}}+\bar{D}$

Since switch S will have large current rating, from Table 6-1, the averaging current of S during switching-on, $I_{S\text{-}on}$ is obtained for ready reference. We have:

$$I_{S-on}=I_L=(\frac{1+\bar{D}}{\bar{D}R\Phi_E}-\theta\frac{2}{R\Phi_E})V_{in} \tag{6.14}$$

The graphical expression of the small-signal model is shown in Fig. 6-5(c), which has two different sorts of source nodes, which include one node of $\hat{v}_{in}(s)$ and four nodes of $\hat{d}(s)$ distributed in the different positions. Different from the large-signal model as shown in Fig. 6-5(b), Fig. 6-5(c) considers the effects caused by the ESR of the output filter r_{C2} by changing the transmittance labeled on the branch $<\hat{i}_{C2}, \hat{v}_o>$ from the previous $R/(1+sRC_2)$ to $R(1+sCr_{C2})/[1+sC(R+r_{C2})]$. Neglecting all the source nodes $\hat{d}(s)$ and

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the branches connected form them, we can easily get the analytical form of input-to-output transfer function by graph reduction techniques as below:

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_i \bar{D}^2 R(1+sr_{C2}C_2)}{(SL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2 R(1+sr_{C2}C_2)} \tag{6.15}$$

Where: $M_i = \frac{(1+\bar{D})}{\bar{D}}$

It is noted that the obtained transfer function consider the different parasitic parameters except the forward voltage drop of diodes. This is because the transmittances labeled on the branches from the source node $\hat{v}_{in}(s)$ to any mixed node don't cover the forward voltage drop of diodes. Since the diodes will decrease the practical steady-state performance significantly as referred to in Table 6-1, we modify (6.15) by substitution of a modified voltage transfer gain M_p for the ideal value M_i, which is shown as below:

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_p \bar{D}^2 R(1+sr_{C2}C_2)}{(SL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2 R(1+sr_{C2}C_2)} \tag{6.16}$$

Where: $M_p = \frac{1+\bar{D}}{\Phi_E} - \theta \frac{2\bar{D}}{\Phi_E}\Big|_{r_L=0} = \frac{(1+\bar{D})}{\bar{D}} - 2\theta$

Similarly, neglecting the source nodes $\hat{v}_{in}(s)$ and the branch connected from it, the analytical form of control-to-output transfer functions ($\hat{v}_o/\hat{d}$ and $\hat{i}_L/\hat{d}$) also can be obtained by the graph reduction techniques. Because there are several source nodes $\hat{d}(s)$ in the different positions of the graph, we can derive the relations between the output node and the different nodes $\hat{d}(s)$ respectively, which are summed up to get the entire control-to-output transfer function. Both Mason rules and graph reduction techniques are effective calculation approaches. Because the transmittances labeled on the branches from each node $\hat{d}(s)$ to the output node include the forward voltage drop of diodes, the obtained control-to-output transfer functions reflect the effects caused by diodes and need no modification. The main analytical forms of small-signal transfer functions are tabulated in Table 6-2 for ready reference.

Table 6-2 Analytical forms of small-signal models of the elementary circuit

$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_p \bar{D}^2 R(1+sr_{C2}C_2)}{(SL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2 R(1+sr_{C2}C_2)}$

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$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{(1+sr_{C2}C_2)[(V_o+2V_D-V_{in})\bar{D}R - I_L R(SL+r_L)]}{(SL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2R(1+sr_{C2}C_2)}$$

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{[1+s(R+r_{C2})C_2](V_o+2V_D-V_{in})+I_L\bar{D}R(1+sr_{C2}C_2)}{(sL+r_L)[1+s(R+r_{C2})C_2]+\bar{D}^2R(1+sr_{C2}C_2)}$$

B. Verification

To illustrate the comprehensive application of the proposed method, the following design examples are considered. Referring to elementary circuit shown in Fig. 6-4, we choose the circuit parameters $f=50kHz$, $d=0.5$, $L=500\mu H$, $C_1=220\mu F$, $C_2=50\mu F$, $R=10\Omega$ and $v_{in}=5V$, which make the converter operated in CCM. Some power losses occur assuming that the ESR of the inductor $r_L=0.1\Omega$. and the forward voltage drop of the diodes $V_D=0.85V$. In the previous part, the theoretical results of steady-state performance are derived by the proposed method and tabulated in Table 6-1, from which we get the steady-state performance. The averaging load voltage $V_o=12.77V$ and the averaging inductor current $I_L=2.55A$.

The elementary is simulated in the Pspice with the above-mentioned parameters to verify the theoretical results. All the parasitic parameters are included. The corresponding simulation results are shown in Fig. 6-6. In addition, the experimental testing circuits are constructed and the corresponding experimental results are shown in Fig. 6-7. Both simulation and experimental results are in agreement with the theoretical results derived from the proposed method.

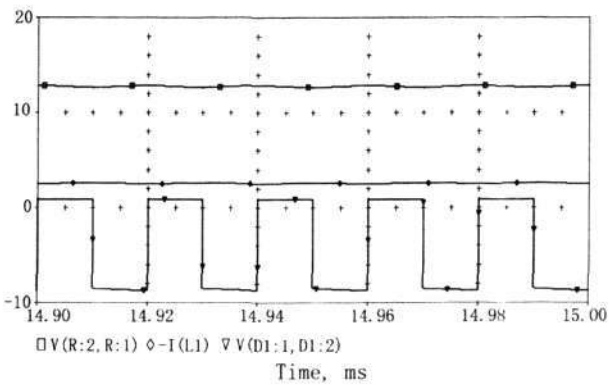

Fig. 6-6. The simulation results in Pspice of the elementary circuit: load voltage, inductor current and voltage across the diode

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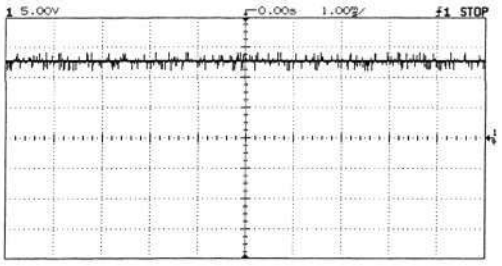
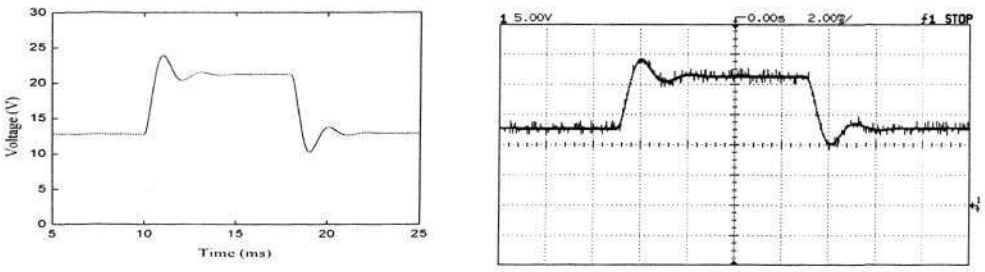


Fig. 6-7. The experimental results of the elementary circuit: the output load voltage



(a) (b)

Fig. 6-8. Transient process of the elementary circuit

(a) simulation curve obtained from proposed SFG method
(b) Experimental curve

For illustration of the transient performance, the theoretical large-signal SFG models described by Fig. 6-5(b) are programmed into the TUTSIM simulator or Matlab to observe the large-signal global behaviors. For the case that the input voltage is changed from *5V* to *8V* and back to *5V* after an interval, the simulation curve for output voltage is shown in Fig. 6-8(a). Under the above conditions, the circuit is simulated as an underdamped 2nd order system. The experimental curve is shown in Fig. 6-8(b) to validate the SFG simulation results. From Fig. 6-8, it can be seen that the actual transient performance can be simulated by the proposed SFG analytical method exactly.

6.3.3 Example: modelling and analysis of the re-lift circuit

A. Derivation

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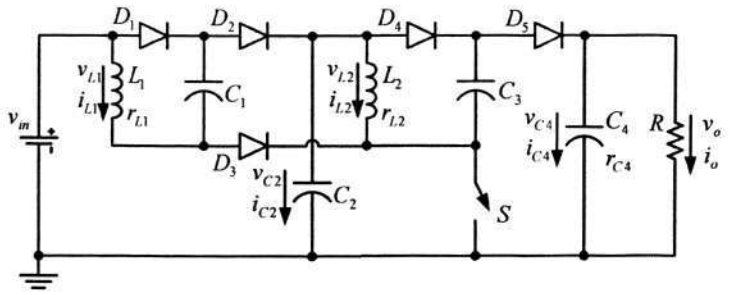


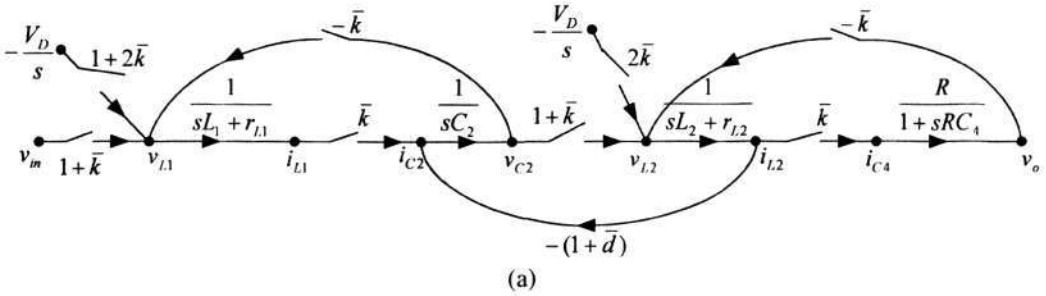
Fig. 6-9. Topology of the re-lift circuit of super-lift converters (with two VL cells)

The re-lift circuit is shown in Fig. 6-9, where state variables and directions are indicated. Its SSFG is drawn from Fig. 6-3(c), which has been predigested as shown in Fig. 6-10(a). There are three close loops and five generalized switching branches in Fig. 6-10(a). In addition, there are one source nodes v_{in} and two source nodes $-V_D$ in it. We get the graphical expression of the large-signal model shown in Fig. 6-10(b) according to the proposed method, which is similar to the analytical procedure of the elementary circuit. Therefore, the complicated calculation difficulties existing in the conventional methods are avoided through constructing the flow graph. For example, to get the steady-state information of V_o/V_{in}, assuming $s \to 0$ and using Mason rules, we analyze the graph from three individual paths that start from different source nodes and end at the same mixed node. We have:

$$\frac{V_o}{V_{in}} = \frac{v_o(s)}{v_{in}(s)}\bigg|_{s\to 0} + \sum_{n=1}^{2}\left[\frac{v_o(s)}{-v_D(s)}\bigg|_{s\to 0} \times \left(-\frac{V_D}{V_{in}}\right)\right]_n \tag{6.17}$$

Where: n is the number of the node $-V_D$ in the large-signal model

The steady-state information is then obtained by Mason rules as tabulated in Table 6-3. In addition, the ideal performance of the elementary circuit is also provided for the reference.



(a)

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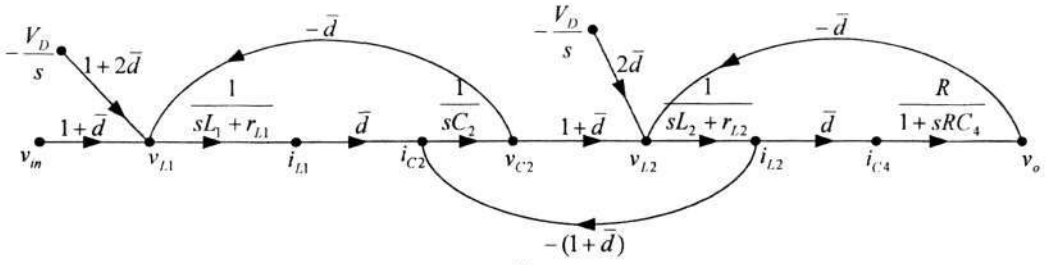
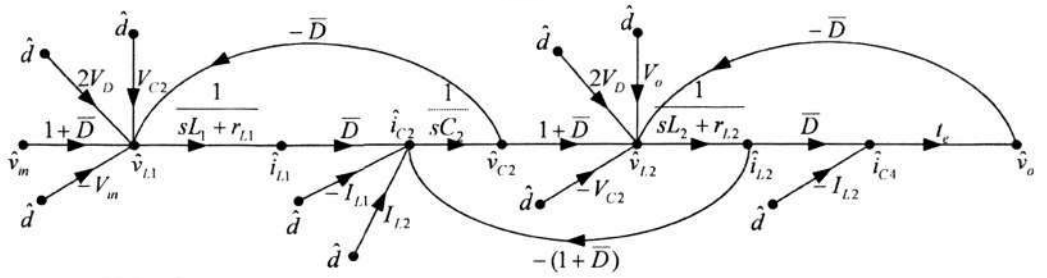


(b)



Where: $t_e = \dfrac{R(1+sCr_{C4})}{1+sC(R+r_{C4})}$

(c)

Fig. 6-10. Modelling of the re-lift circuit of the super-lift converters

(a) SSFG
(b) large-signal model
(c) small-signal model

Table 6-3 Steady-state performance of the re-lift circuit (super-lift converters)

	Nonideal Performance	Ideal Performance
$\frac{V_o}{V_{in}}$	$\frac{(1+\bar{D})^2}{\Phi_R} - \theta[\frac{4\bar{D}^2+3\bar{D}+1}{\Phi_R}]$	$(\frac{1+\bar{D}}{\bar{D}})^2$
$\frac{V_{C2}}{V_{in}}$	$\frac{\bar{D}(1+\bar{D})(\frac{r_{L2}}{R\bar{D}^2}+1)}{\Phi_R} - \theta[\frac{\bar{D}(1+2\bar{D})+\frac{r_{L2}}{R}\frac{(1+2\bar{D})}{\bar{D}}-\frac{r_{L1}}{R}\frac{2(1+\bar{D})}{\bar{D}}}{\Phi_R}]$	$\frac{1+\bar{D}}{\bar{D}}$
$\frac{I_{L2}}{V_{in}}$	$\frac{(1+\bar{D})^2}{R\bar{D}\Phi_R} - \theta[\frac{4\bar{D}^2+3\bar{D}+1}{R\bar{D}\Phi_R}]$	$\frac{(1+\bar{D})^2}{\bar{D}^3R}$
$\frac{I_{L1}}{V_{in}}$	$\frac{(1+\bar{D})^3}{R\bar{D}^2\Phi_R} - \theta[\frac{(1+\bar{D})(4\bar{D}^2+3\bar{D}+1)}{R\bar{D}^2\Phi_R}]$	$\frac{(1+\bar{D})^3}{\bar{D}^4R}$

Where: $\theta = \frac{V_D}{V_{in}}$ and $\Phi_R = \frac{r_{L2}}{R} + \frac{r_{L1}}{R}(\frac{1+\bar{D}}{\bar{D}})^2 + \bar{D}^2$

Since diode D_3 and switch S will have large current rating, from Table 6-3, the averaging current of D_3 during switching-on, $I_{D3\text{-}on}$ is obtained for ready reference. We have:

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$$I_{D3-on} = I_{L1} = \left\{ \frac{(1+\bar{D})^3}{R\bar{D}^2\Phi_R} - \theta[\frac{(1+\bar{D})(4\bar{D}^2+3\bar{D}+1)}{R\bar{D}^2\Phi_R}] \right\} V_{in} \tag{6.18}$$

The averaging current rating of S during switching-on, $I_{S\text{-}on}$ is obtained as

$$I_{S-on} = I_{L1} + I_{L2} = \frac{1+2\bar{D}}{\bar{D}} \left\{ \frac{(1+\bar{D})^2}{R\bar{D}\Phi_R} - \theta[\frac{4\bar{D}^2+3\bar{D}+1}{R\bar{D}\Phi_R}] \right\} V_{in} \tag{6.19}$$

Because multi-loops make SFG more complex, the graph reduction technique is not appropriate computation approach. The detailed analytical procedure of using Mason rules to analyze the graph will be demonstrated in the following part about small-signal models. The graphical expression of the small-signal model is shown in Fig. 6-10(c) and the analytical forms of small-signal transfer functions are tabulated in Table 6-4. The ESR of the output filter r_{C4} is considered. So the transmittance labeled on the branch $<\hat{i}_{C4}, \hat{v}_o>$ is changed from the previous $R/(1+sRC_4)$ to $R(1+sCr_{C4})/[1+sC(R+r_{C4})]$. The application of Mason rules need searching forward paths and close loops exactly. For example, the derivation of input-to-output transfer function is demonstrated here. From the source node $\hat{v}_{in}$ to the mixed node $\hat{v}_o$, the forward path is searched and defined as P_1 ($<\hat{v}_{in}\ \hat{v}_{L1}\ \hat{i}_{L1}\ \hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C4}\ \hat{v}_o>$). The transmittance of this forward path P_1 is obtained as:

$$P_1 = \frac{(1+\bar{D})^2\bar{D}^2R(1+sr_{C4}C_4)}{[1+s(R+r_{C4})C_4](sL_1+r_{L1})(sL_2+r_{L2})sC_2}$$

There are three individual loops L_1 ($<\hat{v}_{L1}\ \hat{i}_{L1}\ \hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L1}>$), L_2 ($<\hat{i}_{C2}\ \hat{v}_{C2}\ \hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C2}>$) and L_3 ($<\hat{v}_{L2}\ \hat{i}_{L2}\ \hat{i}_{C4}\ \hat{v}_o\ \hat{v}_{L2}>$) in the graph. The corresponding loop transmittances are:

$$L_1 = \frac{-\bar{D}^2}{(sL_1+r_{L1})sC_2} \qquad L_2 = \frac{-(1+\bar{D})^2}{(sL_2+r_{L2})sC_2} \qquad L_3 = \frac{-\bar{D}^2R(1+sr_{C4}C_4)}{(sL_2+r_{L2})[1+s(R+r_{C4})C_4]}$$

Note that since all three loops have a common branch and there are no nontouching loops. Hence, the determinant Δ is equal to $(1\text{-}L_1\text{-}L_2\text{-}L_3\text{+}L_1L_3)$. The cofactor of defined forward path, Δ_1 is equal to 1. Therefore, the overall gain between $\hat{v}_o$ and $\hat{v}_{in}$, or the transfer function is given by

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$$\left.\frac{\hat{v}_o}{\hat{v}_{in}}\right|_{d(s)=0} = \frac{1}{\Delta}\sum_k P_k\Delta_k = \frac{P_1\Delta_1}{\Delta} \tag{6.20}$$

The final result obtained from (6.20) also doesn't reflect the effects caused by diodes because of the same reason discussed in Chapter 6.3.2. So the modified voltage transfer gain M_p shown in Table 6-3 is used. The derivation for the analytical form of control-to-output transfer functions ($\hat{v}_o/\hat{d}$, $\hat{i}_{L2}/\hat{d}$ and $\hat{i}_{L1}/\hat{d}$) can refer to the procedure for the elementary circuit. The detailed analytical forms of small-signal transfer functions of the re-lift circuit are tabulated in Table 6-4.

Table 6-4 Analytical forms of small-signal models of the re-lift circuit

$$\frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{M_p\bar{D}^4R(1+sr_{C4}C_4)}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\bar{D}^2+(sL_1+r_{L1})(1+\bar{D})^2]+\bar{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\bar{D}^2]}$$

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{A_1+A_2(sL_1+r_{L1})+A_3[\bar{D}^2+(sL_1+r_{L1})sC_2]-A_4[(sL_1+r_{L1})(sL_2+r_{L2})sC_2+(sL_2+r_{L2})\bar{D}^2+(sL_1+r_{L1})(1+\bar{D})^2]}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\bar{D}^2+(sL_1+r_{L1})(1+\bar{D})^2]+\bar{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\bar{D}^2]}$$

$$\frac{\hat{i}_{L2}(s)}{\hat{d}(s)} = \frac{A_5(1+\bar{D})\bar{D}+A_6(sL_1+r_{L1})+(A_7+A_4\bar{D})[\bar{D}^2+(sL_1+r_{L1})sC_2]}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\bar{D}^2+(sL_1+r_{L1})(1+\bar{D})^2]+\bar{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\bar{D}^2]}$$

$$\frac{\hat{i}_{L1}(s)}{\hat{d}(s)} = \frac{A_5(sL_2+r_{L2})[sC_2+(1+\bar{D})^2]+A_1sC_2-A_2\bar{D}^2-A_6\bar{D}(sL_2+r_{L2})+(A_7+A_4\bar{D})(1+\bar{D})\bar{D}}{\Delta_p+[1+s(R+r_{C4})C_4][(sL_2+r_{L2})\bar{D}^2+(sL_1+r_{L1})(1+\bar{D})^2]+\bar{D}^2R(1+sr_{C4}C_4)[(sL_1+r_{L1})sC_2+\bar{D}^2]}$$

Where:

$$M_p = \frac{(1+\bar{D})^2}{\Phi_R} - \theta\left.\frac{4\bar{D}^2+3\bar{D}+1}{\Phi_R}\right|_{r_{L1}=r_{L2}=0} = \left(\frac{1+\bar{D}}{\bar{D}}\right)^2 - \theta\frac{4\bar{D}^2+3\bar{D}+1}{\bar{D}^2}$$

$$\Delta_p = [1+s(R+r_{C4})C_4](sL_1+r_{L1})(sL_2+r_{L2})sC_2\,,$$

$$A_1 = (V_{C2}+2V_D-V_{in})(1+\bar{D})\bar{D}^2R(1+sr_{C4}C_4)$$

$$A_2 = (I_{L2}-I_{L1})(1+\bar{D})\bar{D}R(1+sr_{C4}C_4)$$

$$A_3 = (V_o+2V_D-V_{C2})\bar{D}R(1+sr_{C4}C_4)$$

$$A_4 = I_{L2}R(1+sr_{C4}C_4)$$

$$A_5 = (V_{C2}+2V_D-V_{in})[1+s(R+r_{C4})C_4]$$

$$A_6 = (I_{L2}-I_{L1})[1+s(R+r_{C4})C_4]$$

$$A_7 = (V_o+2V_D-V_{C2})[1+s(R+r_{C4})C_4]$$

B. Verification

Referring to re-lift circuit as shown in Fig. 6-9, we choose the circuit parameters f=50kHz, d=0.5, L_1=L_2=500μH, C_1=C_2=C_3=220μF, C_4=50μF, R=10Ω and v_{in}=5V. There are some power losses, assuming that the ESR of the inductor r_{L1}=r_{L2}=0.1Ω. The

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forward voltage drop of the diodes $V_D=0.85V$. We get the steady-state performance by the calculation equations in Table 6-3.The averaging load voltage $V_o=23.64V$. The averaging inductor current $I_{L2}=4.73A$ and $I_{L1}=14.18A$.

The re-lift circuit is simulated in the Pspice with the above-mentioned parameters to verify the theoretical results. All the parasitic parameters are included. The corresponding simulation results are shown in Fig. 6-11. In addition, the experimental testing circuits are constructed and the corresponding experimental results are shown in Fig. 6-12. Both simulation and experimental results are in agreement with the theoretical results derived from the proposed method.

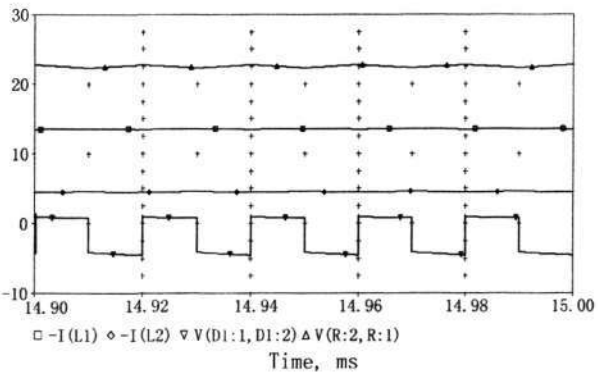

Fig. 6-11. The simulation results in Pspice: load voltage, inductor current and voltage across the diode

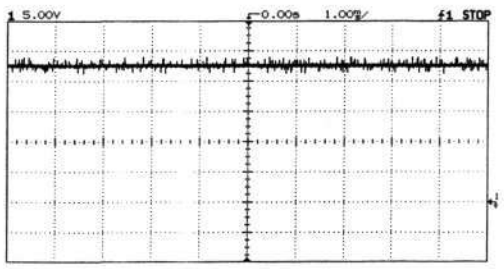

Fig. 6-12. The experimental results: the output load voltage

For illustration of the transient performance, the theoretical large-signal models described by Fig. 6-10(b) are programmed into the TUTSIM simulator or Matlab to observe the large-signal global behaviors. For the case that the input voltage is changed from *5V* to *8V* and back to *5V* after an interval, the simulation curve of the output voltage are shown in Fig. 6-13(a). Under the above conditions, the re-lift circuit is close to an overdamped high order system. The experimental curve is shown in Fig. 6-13(b) to

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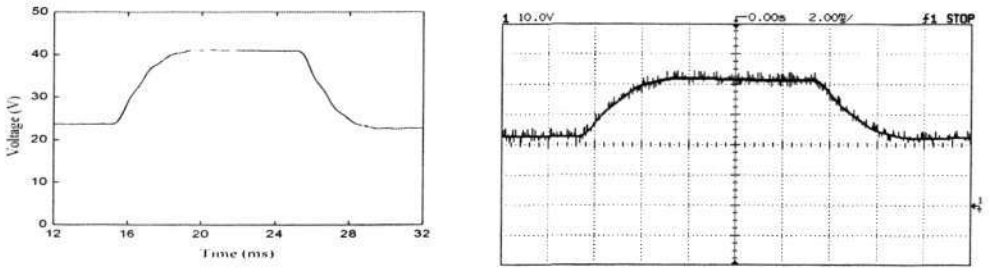
validate the SFG simulation results. From Fig. 6-13, it can be seen that the actual transient performance of super-lift converters can be simulated by the proposed SFG analytical method exactly.



(a) (b)

Fig. 6-13. Transient process of the re-lift circuit

(a) simulation curve obtained from proposed SFG method
(b) Experimental curve

6.4 Averaging Binary Tree Structure Representation Method

The SSFG method has been successfully applied to the modeling of complex dc-dc converters in forgoing sections. For a given converter operating in CCM, there are two sub-networks in each switching cycle. These are described by two different SFGs. These two SFGs can be combined through averaging to get an SSFG model. Classical graph reduction techniques and Mason rules are utilized to analyze the SSFG models and perform system calculations. For topologies (cascade/parallel) with multiple feedback loops in their SSFGs or under an operation condition of high complexity:

- Mason rules need tedious searching for the different forward paths and loops in the flow graph.
- Graph reduction techniques also require a complicated node-movement transformation process.

However, it is still a strenuous process [71-76]. So a more convenient and effective analytical method is needed.

For a linear system represented by the flow graph, an effective computational approach developed from conventional graph reduction techniques has been introduced in [77].

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This constructs a binary tree structure to replace the original flow graph. The SSFG models of power dc-dc converters are typical flow graphs with feedback loops.

Therefore, The concept of constructing a binary tree structure is introduced into the modeling and analysis of dc-dc converters in this sub-chapter. General construction rules for graphs with feedback loops are summarized firstly. Then the proposed method for power dc-dc converters is presented, together with theoretical analytical results and experimental data. The conclusion and discussion are given at the end of the sub-section.

6.4.1 General Principles

Fundamentals of the binary tree structures and flow graphs have been introduced in [77]. However, only simple flow graphs have been discussed, and it is difficult to construct the correct binary tree presentation for complex graphs under the rules in [77]. Therefore, an in-depth introduction is given here for complex flow graphs with multiple feedback loops (similar to dc-dc converter models). To aid understanding, the basic definition is reexamined.

A. Basic Definition of Nodes and Binary Tree

Each branch in SFG is labeled with a signal gain or a transfer function which denotes the dynamic characteristics between the input and output signals of this branch. Such a branch with its dynamic information can be represented by a node in a tree structure. The entire information expression of a tree node is denoted from four aspects, which correspond to four fields, as shown below:

$$(Name, Type, Weight)^{Step} \tag{6.21}$$

The combination of input and output signals is used as the content in the *Name* field. For example, the node name of *A.B* shows that the prefix *A* and the postfix *B* correspond, respectively, to input and output signals on the branch. The *Type* field is then defined as *TF*, which indicates that the nodes correspond to the basic branches of the graph. The signal gain or transfer function labeled on the basic branch is taken as the content in the

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Weight field. The *Step* field is a supplement to the original node expression structure of [77], and indicates the node appearance order.

Two adjacent basic branches in the flow graph will be merged into a new branch by graph reduction techniques. The corresponding two *TF* type nodes can then be regarded as the left and right children of a new father node. The mapping from the flow graph to the binary tree structure representation is then established and is illustrated in Fig. 6-14. Three new types of father nodes, *CA* (cascade), *PA* (parallel) and *LO* (self-loop) are defined, respectively, according to the connection relations of their two adjacent branches. The name of the father node is a string of the left child's prefix and the right child's postfix. The corresponding weight is calculated by the following rules:

$$Weight(CA) = Weight(Left\_child) \times Weight(Right\_child) \tag{6.22}$$

$$Weight(PA) = Weight(Left\_child) + Weight(Right\_child) \tag{6.23}$$

$$Weight(LO) = \frac{Weight(Left\_child)}{1 - Weight(Right\_child)} \tag{6.24}$$

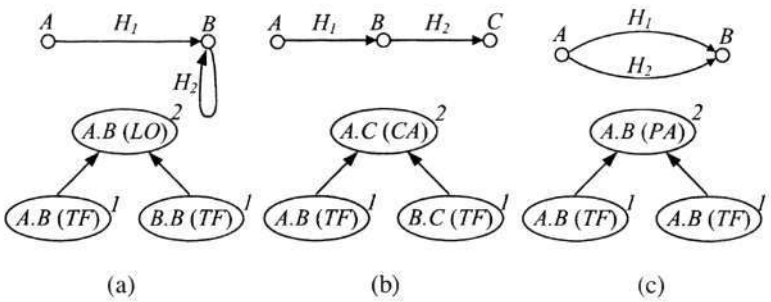

Fig. 6-14. Construction and reduction of binary tree structures

(a) cascade reduction
(b) parallel reduction
(c) self-loop reduction

B. General construction principles for complex flow graphs

For most of complex linear systems, there exist multiple feedback loops. Rules in [77] may make their binary tree construction processes confused. So the general principles for those complex flow graphs are explored and presented as follows:

1) First check all the individual branches from input to output and create the corresponding *TF*-type nodes. All of them will be the leaves of the finally obtained tree.

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2) For those branches that are located in the loops, the corresponding *TF*-type nodes will be considered firstly in the whole tree construction process.

3) If there exists such a node whose postfix (prefix) is equal to the prefix (postfix) of other nodes, this node will be duplicated and reduced earlier than the other nodes.

4) At any level of the tree, if a certain node is replicated, its duplicate node should be used for reduction in this level and cannot be left to the next level. In addition, if the node is taken as the left or right child, the corresponding duplicate node should be taken as the same child.

5) By reduction for the nodes located in the loops, some new nodes are created. When there appears such a node whose prefix is the same as its postfix and the same as the postfix of a certain node located outside the loops, then we can deal with the reduction of these two nodes.

6) At any level of the tree, the reduction of the corresponding nodes should follow the same construction algorithm. First, all possible parallel reductions are performed. Then all possible cascade reductions are performed. Finally, all possible loop reductions are performed.

7) Note that the graph finally obtained is a strongly binary tree, which means the root is adjacent to two nodes, and all non-root nodes are adjacent to either one or three nodes.

The above principles may be utilized to get the correct mapping from a complex flow graph to the binary tree structure representation. For example, the graph shown in Fig. 6-15 has two individual feedback loops which possess a common branch. It needs five steps to realize the mapping as shown in Fig. 6-15.

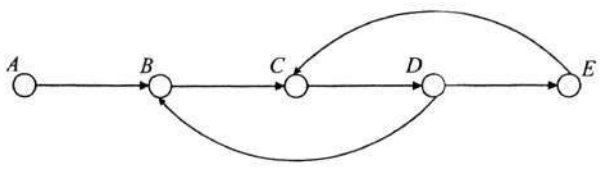

Fig. 6-15. Example of the mapping: a flow graph system

The 1st step: According to principle 1, the individual branches in the graph correspond to the tree leaves *A.B*(*TF*), *B.C*(*TF*), *C.D*(*TF*), *D.E*(*TF*), *E.C*(*TF*), and *D.B*(*TF*). All of

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them are indicated by *1* in the *Step* field. According to principles 2, 3 and 4, we find the postfix of *C.D(TF)* is equal to the prefixes of nodes *D.E(TF)* and *D.B(TF)*. A duplicated node *C.D(TF)* is thus created. By the check of principle 6, the cascade reductions of (*C.D, D.B*) and (*C.D, D.E*) are performed firstly at the bottom of tree.

The 2nd step: Since new nodes *C.B(CA)* and *C.E(CA)* are created, both of them are indicated by 2 in the *Step* field. In this new tree level, the duplicated nodes of *C.B(CA)* and *C.E(CA)* are created respectively due to the same reason as explained in the principle 3 and 4. By the check of principle 6, the cascade reduction of (*E.C, C.B*) and (*E.C, C.E*) are performed.

The 3rd step: Because step 2 creates a new father node *B.B(CA)* in this level, the tree leaf *A.B(TF)* will be considered. It can be explained by principle 5. The *Step* field for *B.B(CA)*, *E.B(CA)* and *B.E(CA)* is indicated by *3*. In addition, the duplicated nodes of *B.B(CA)* are created because of principle 3. By the check of principle 6, the self-loop reductions of (*A.B, B.B*) and (*E.B, B.B*) are performed.

The 4th step: In the new tree level, the duplicated nodes of *B.E(LO)* are created because of principle 3. By the check of principle 6, the cascade reductions of (*A.B, B.E*) and (*E.B, B.E*) are performed.

The 5th step: Only two nodes are left, and the self-loop reduction is performed to obtain the root *A.E(LO)*. The final binary tree should accord with principles 4 and 7.

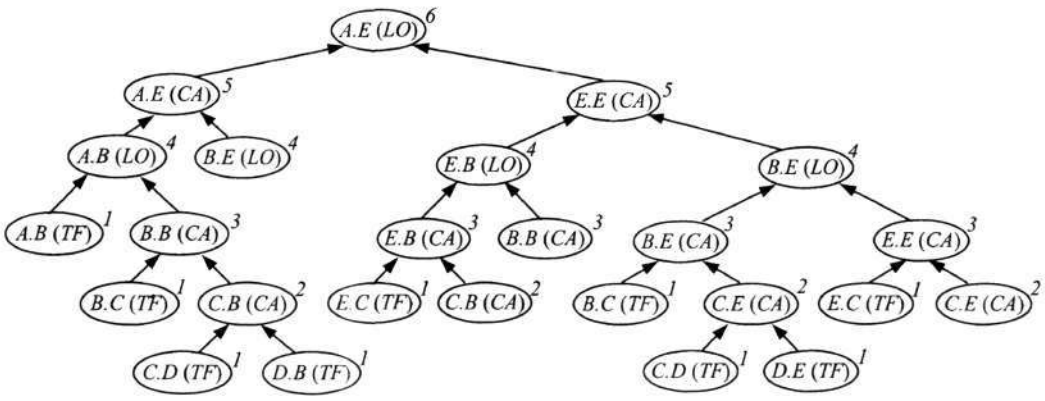

Fig. 6-16. Example of the mapping: the binary tree structure representation of Fig. 6-15

C. Computation rules of the weight

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The weight of the root node can be calculated by (6.22), (6.23) and (6.24). The computational process is clear, especially for the application of the CAD program. The result can be regarded as the transfer function of input to output. If we need to calculate transfer functions of input to any other state variables, the same binary tree will be utilized to obtain what we want. It is called a sub-weight derivation and can be referred to in [77] for details. The key of the derivation is to find a node nearest to the root whose postfix is just what we need. Starting from this node, we can quickly obtain the sub-weight. For the tree structure representation, there may be several replicated nodes at the same level which belong to different sub-trees. We can choose anyone among them as the intermediate node, and the same sub-weights will be obtained.

The above rules are valid only under the condition that the root node type is *CA* or *LO*. When the root node type is *PA*, we should check the left and right sub-trees of the root node and find the corresponding intermediate nodes. If the root of a sub-tree is also a *PA*-type node, the above steps should be repeated. Each sub-tree corresponds to only one intermediate node. The general computational rules in [77] are still valid. Finally, the corresponding sub-weights based on the general rules should be summed. This special point will be used in the following sub-section.

6.4.2 Application on dc-dc converters and case study

The proposed method, which can be termed averaging binary tree representation, is a combination of SSFG and binary tree structure here. The 2^{nd} order dc-dc converters are chosen as examples. The same procedure can be applied to converters with higher order numbers. 2^{nd} order dc-dc converters consist mainly of one inductor L, one active switch S, one passive switch D (diode).and one capacitor C (output filter). Different locations of the above-mentioned elements correspond to different topologies. The generalized representation is shown in Fig. 6-17(a). Note that the equivalent series resistance of the inductor r_L is considered here. Every converter concerned is operated in CCM.

Large-signal SSFG models are unified into a generalized form as shown in Fig. 6-17(b). Branch transmittances H_1 to H_9, are tabulated in Table 6-5 for ready reference. For dc-dc converters, there are multiple input/output pairs in SSFG. Input signal v_g can be

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selected as the prefix of the root node. State variable v_C can be selected as the postfix of the root node. Then we need to construct a tree with the root node $v_g.v_C$. Using principles 1 to 7 introduced in the forgoing part, we get the binary tree structure representation for large-signal models, as illustrated in Fig. 6-18. The derivation of the large-signal transfer function (v_g to v_C) is an evaluation process for the root node weight. It starts from the bottom of the tree and ends at the root node. From Fig. 6-18, the generalized analytical form of large-signal transfer functions is derived by using (6.22), (6.23) and (6.24). We have:

$$\frac{v_C}{v_g} = \frac{H_1 H_2 H_3 H_4}{1 - H_2 H_3 H_4 H_5} \tag{6.25}$$

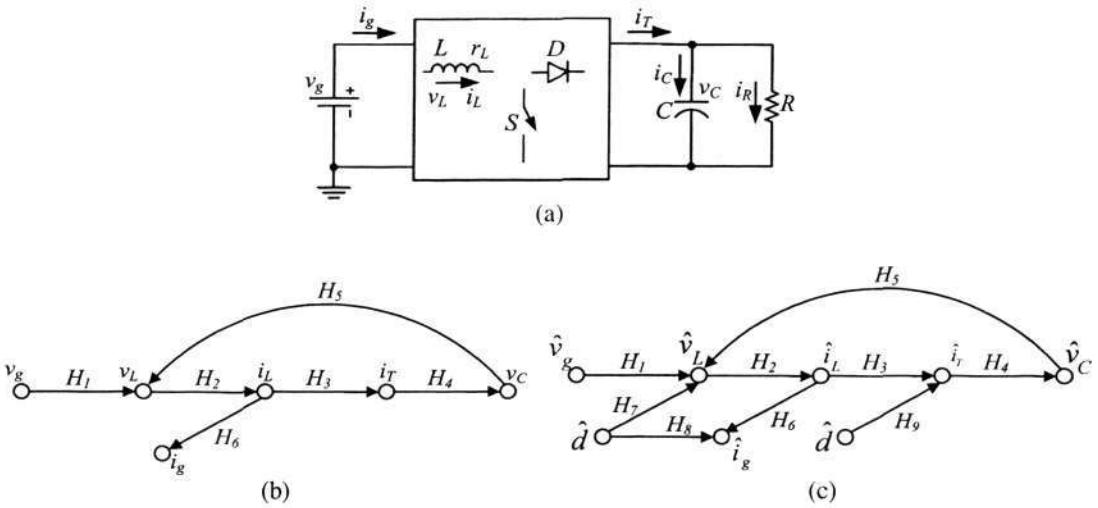

Fig. 6-17. Generalized 2nd order dc-dc converters

(a) topology
(b) large-signal SSFG
(c) small-signal SSFG

Table 6-5 Branch transmittances of the generalized SSFG for 2ND order dc-dc converters

	H_1	H_2	H_3	H_4	H_5	H_6	H_7	H_8	H_9
Buck	D	$\frac{1}{Ls + r_L}$	1	$\frac{R}{RCs + 1}$	-1	D	V_g	I_L	0
Buck-Boost	D	$\frac{1}{Ls + r_L}$	$(1-D)$	$\frac{R}{RCs + 1}$	$-(1-D)$	D	(V_g+V_C)	I_L	$-I_L$
Boost	1	$\frac{1}{Ls + r_L}$	$(1-D)$	$\frac{R}{RCs + 1}$	$-(1-D)$	1	V_C	0	$-I_L$

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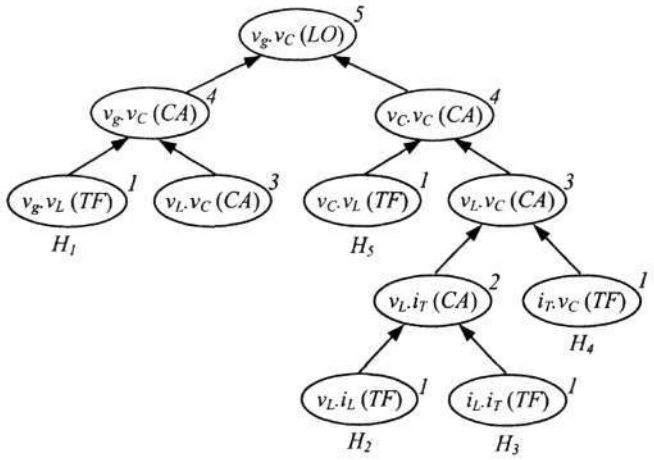

Fig. 6-18. The generalized binary tree structure for large-signal models of 2nd order dc-dc converters

If we want to derive the transfer functions of the v_g to any other state variable, the binary tree in Fig. 6-18 can again be utilized. This process is a computational derivation for the sub-weight of the binary tree. For example, the generalized analytical form of large-signal transfer functions for v_g to the inductor current i_L needs to be calculated. Node $v_L.i_L(TF)$ is selected as the intermediate node. Then we have:

$$\frac{i_L}{v_g}=\frac{H_1H_2}{1-H_2H_3H_4H_5} \tag{6.26}$$

Small-signal SSFG models are also unified to a generalized form as shown in Fig. 6-17(c). Duty ratio d is the control signal. Because there exist two input ports of $\hat{d}$ and only one output port of $\hat{v}_C$ in the SSFG, two pairs of $\hat{d}/\hat{v}_C$ need to be considered. Each pair corresponds to a sub-tree with the sub-root node $\hat{d}.\hat{v}_C$. Hence, a PA-type root node $\hat{d}.\hat{v}_C(PA)$ should be created to sum the weights of the two sub-trees. This represents the total effects caused by the control signal in the circuit. The binary tree structure representation for small-signal models is then illustrated in Fig. 6-19. The prefix and postfix of the root node correspond to control signal $\hat{d}$ and output voltage $\hat{v}_C$, respectively. The generalized analytical form of small-signal transfer functions is obtained as follows:

$$\frac{\hat{v}_C}{\hat{d}}=\frac{H_2H_3H_4H_7}{1-H_2H_3H_4H_5}+\frac{H_4H_9}{1-H_2H_3H_4H_5} \tag{6.27}$$

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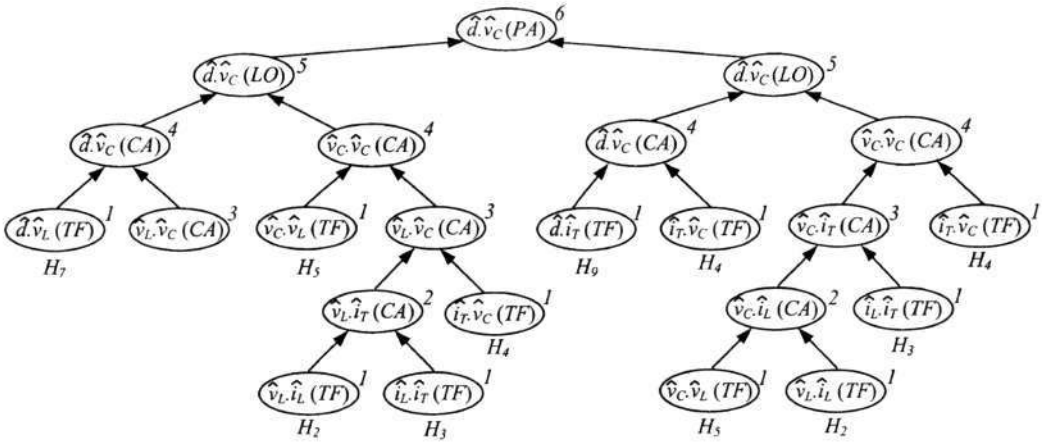

Fig. 6-19. The generalized binary tree structure for small-signal models of 2nd order dc-dc converters

If we want to derive the small-signal transfer function of $\hat{d}$ to any other state variable, the binary tree in Fig. 6-19 can again be utilized. This process is a computational derivation for the sub-weight of the binary tree. Take as an example that the transfer function of $\hat{d}$ to state variable $\hat{i}_L$ needs calculating. We should consider the left and right sub-tree, respectively, because the root is a *PA*-type node. In the left sub-tree, the intermediate node is $\hat{v}_L.\hat{i}_L(TF)$, and we obtain the partial transfer function from the control signal. In the right sub-tree, the intermediate node is $\hat{v}_C.\hat{i}_L(CA)$, and we obtain the partial transfer function from a control signal port. The different sub-weights are summed. Thus the entire analytical form is as follows:

$$\frac{\hat{i}_L}{\hat{d}} = \frac{H_2 H_7}{1 - H_2 H_3 H_4 H_5} + \frac{H_2 H_4 H_5 H_9}{1 - H_2 H_3 H_4 H_5} \tag{6.28}$$

To verify the proposed method, the following example of a 2nd order boost converter is considered. The circuit parameters are: switching frequency f=*50*kHz, duty ratio d=*0.5*, inductor L=*800*μH, capacitor C=*110*μF, load R=*20*Ω and input voltage v_g=*5*V. There are some power losses, assuming that the inductor resistance r_L=*0.5*Ω.

Referring to the branch transmittances listed in Table 6-5 and substituting the corresponding values in the generalized model representation illustrated in Fig. 6-18, we obtain the binary tree structure representation of the boost converter directly. Hence, the

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large-signal transfer functions can be obtained by computing the root node weight or sub-weight in the binary tree structure models as follows:

$$\frac{v_C}{v_g} = \frac{R(1-D)}{s^2LRC + s(L+RCr_L) + r_L + R(1-D)^2} \tag{6.29}$$

$$\frac{i_L}{v_g} = \frac{RCs+1}{s^2LRC + s(L+RCr_L) + r_L + R(1-D)^2} \tag{6.30}$$

Assuming the operator s→ 0, (6.29) and (6.30) yield the steady-state performance:

$$V_C = \frac{R(1-D)}{r_L + R(1-D)^2} V_g \tag{6.31}$$

$$I_L = \frac{1}{r_L + R(1-D)^2} V_g \tag{6.32}$$

Similarly, small-signal transfer functions also can be obtained by using the generalized model representation illustrated in Fig. 6-19. We calculate the root node weight and sub-weight in the binary tree structure models. These are expressed as follows:

$$\frac{\hat{v}_C}{\hat{d}} = \frac{R(1-D)V_C - RI_L(Ls+r_L)}{s^2LRC + s(L+RCr_L) + r_L + R(1-D)^2} = \frac{14.87 - 2.65\times10^{-3}s}{3.2\times10^{-7}s^2 + 3.45\times10^{-4}s + 1} \tag{6.33}$$

$$\frac{\hat{i}_L}{\hat{d}} = \frac{(RCs+1)V_C + R(1-D)I_L}{s^2LRC + s(L+RCr_L) + r_L + R(1-D)^2} = \frac{3.64s + 3.3}{3.2\times10^{-7}s^2 + 3.45\times10^{-4}s + 1} \tag{6.34}$$

For the large-signal transfer functions (6.29) and (6.30) derived from the binary tree structure models, the expressions are the same as those obtained from the approaches of conventional state-space averaging or SSFG. But the derivation process has been predigested. According to (6.31) and (6.32), the theoretical steady-state performance of the example is V_C=*9.1*V and I_L=*0.91*A. Simulation for models (6.33) and (6.34) is performed under the condition that $\hat{d}$ is *0.1* and the perturbation lasting time is *1*ms. The simulation curves are shown in Fig. 6-20.

Experimental verification is performed. The duty ratio is changed from 0.5 to *0.6* and then back to *0.5* after about *1*ms. The experimental curves (Channel 1: v_C and Channel 2: i_L) are provided in Fig. 6-21 along with an enlarged partial view, which shows a good agreement with the response of (6.33) and (6.34). The practical steady-state values are also very close to the theoretical performance of (6.31) and (6.32).

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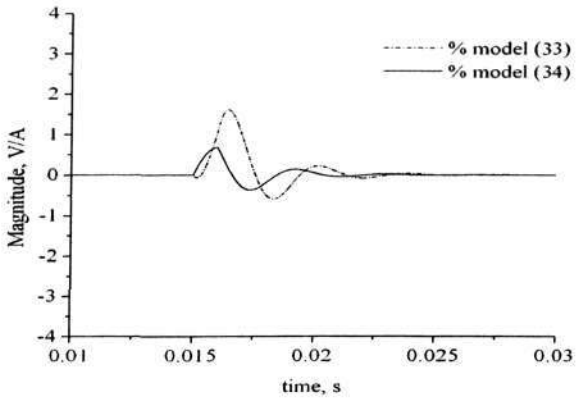

Fig. 6-20. Simulation curves of model (6.33) and (6.34)

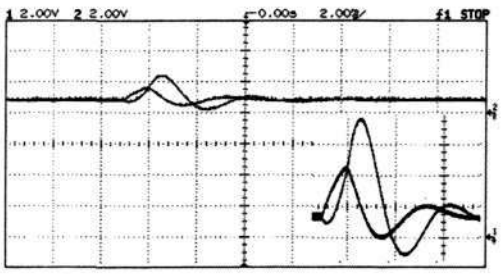

Fig. 6-21. experimental curves of duty ratio small-signal disturbance

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Chapter 7 Analytical Methods Based on System Energy Characteristics

7.1 Introduction

Dc-dc converters are nonlinear dynamic systems due to switching actions in each switching cycle T. Mathematical analytical methods of power dc-dc converters have been an important problem that has accompanied dc-dc conversion technology development since 1940s. Many traditional parameters such as power factor (PF), power transfer efficiency (η), total harmonic distortion (THD) and ripple factor (RF) have been successfully applied in power electronics and conversion technology. As power dc-dc converters usually possess dc input and dc output, some parameters such as PF and THD are not feasible to describe the characteristics of power dc-dc converters. Therefore, the existing knowledge in dc-dc converters is not completed. Traditional knowledge cannot describe the general characteristics of various dc-dc converters.

All switched-mode power circuits work under the switching condition with high frequency f. It is thoroughly different from traditional continuous work condition. The obvious technical feature is that all parameters perform in a switching cycle T, then gradually change period-by-period. T is the clue to investigate all switching power circuits. Catching this clue, some new concepts and parameters to describe the characteristics of dc-dc converters can be defined and developed.

Because dc-dc converters consist of several energy-storage elements, they are likely an energy container to store certain energy during each switching cycle. The stored energy will vary if the working condition changes. For example, once the power supply is on, the output voltage starts from initial zero state because the container is not filled. The transient process from one steady state to another depends on the pumping energy and stored energy. Same reason affects the DCM performance, since the current discontinuous phenomena are related to the system energy characteristics.

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Despite the long duration spent in researching on the energy storage in power dc-dc converters, there was no clear concept to describe the phenomena and to reveal the relationship between the stored energy and the main characteristics of power dc-dc converters.

In this chapter, on the basis of the investigation results on system energy characteristics and practical inductor current waveforms, a new explanation of DCM is proposed so that all discontinuous cases can be unified by the proposed concepts. Furthermore, according to the general transient performance of multi-state dc-dc converters, a unified modelling method is developed based on the system energy characteristics. The proposed method focuses on the output transient performance (output voltage) and is released from the analysis on the inner nonlinear switching behaviors. The concepts of system energy parameters and the corresponding canonical definition are presented, by which the system model parameters of dc-dc converters are deduced. They are very helpful for the system design and dc-dc converters characteristics foreseeing.

7.2 Remaining Inductor Current Phenomena and DCM New Concepts

Under different circuit configurations and load conditions, a dc-dc converter can be operated either in CCM or in DCM. According to the conventional definition in power electronics, if the current flowing through a given inductor has fallen to zero before the beginning of the next switching cycle, the converter is said to be operating in DCM. Each cycle is thus divided into three periodic switched sub-modes $[0, dT]$, $[dT, t_1]$ and $[t_1, T]$, where d is the duty ratio and $dT < t_1 < T$.

However, with the fast development of dc-dc power conversion techniques, DCM phenomena in some high-order dc-dc converters do not mean that the inductor current will also go to zero before the next switch cycle begins. In other words, a remaining current I_R still flows through during sub-mode 3 after t_1. These special phenomena are generalized and shown in Fig. 7-1. Hence, the conventional definition of DCM is only based on a special case of the inductor current waveform and cannot reflect the internal

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physical nature by a unified form. Moreover, the conventional analytical methods for DCM are usually based on the state-space averaging equations, which are tedious for the circuit designers. Since the in-depth theoretical analysis on DCM phenomena is important and valuable for many practical industrial applications, a reexamination on all kinds of phenomena in DCM is needed.

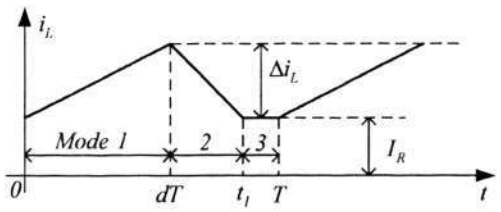

Fig. 7-1. General waveform of DCM cases with the remaining inductor current I_R

The analytical and modelling method based on energy characteristics has been proven to be effective in power electronics [102-106]. There are some energy-storing components in a dc-dc converter, and the corresponding stored energy will change during different sub-modes. Therefore, to unify all discontinuous phenomena (with or without I_R) into a canonical form, an explanation from the view of energy variation characteristics concerning the original DCM concepts is proposed in the following sub-section. The general principles of fast solving the steady-state performance are also given. Finally, two high order converter examples are provided to validate the proposed DCM concepts.

7.2.1 DCM and energy characteristics

A. New explanation of DCM

Referring to Fig. 7-1, we can find that the inductor current i_L may be continuous but its stored energy will not vary during the sub-mode 3. Therefore, from the view of energy variation during a switching cycle, if the transmission of energy stored in L ends off before the next turn-on of S, the converter is said to be operating in DCM.

According to this new explanation, all the DCM phenomena can be unified. If I_R exists during sub-mode 3, it means the transferred inductor energy (stored energy variation) is less than the maximum stored inductor energy during a whole cycle. Conversely, if I_R

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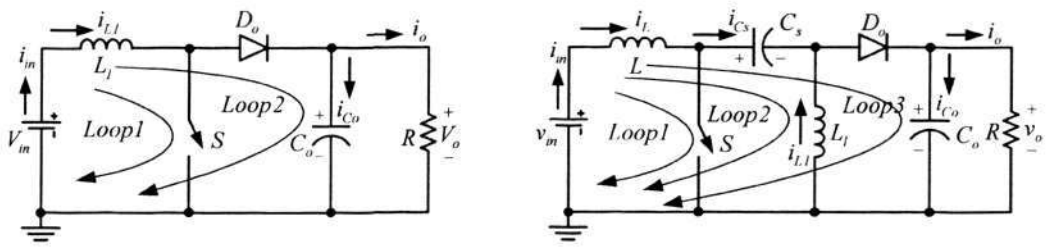
does not exist, i.e. i_L has fallen to zero before the beginning of sub-mode 3, it means all stored inductor energy has been transferred to the load and capacitors.

The proposed new explanation on DCM applies to all complex discontinuous cases. No matter whether I_R exists or not, the energy transmission ends at the end of sub-mode 2. The ending of the energy transmission process means the inductor current variation Δi_L will not change any more at t_1. Therefore, the voltage across L, v_L is equal to zero during sub-mode 3. Moreover, it suggests that a certain diode whose current must has decreased to zero at the end of sub-mode 2. The discontinuous diode current relates the proposed new explanation to the conventional DCM definition based on the inductor waveforms.

B. Existence conditions

Since there may be multiple inductors in a complex dc-dc converter, we should analyze each inductor to judge the existence of I_R using the following criterion:

Existence conditions of I_R during sub-mode 3 in DCM are simultaneously satisfied: (i) Inductor L is included in a certain close-loop with the source or load. (ii) There is no active switch (power switch) or passive switch (diode) in above-mentioned close-loop.



(a) (b)

Fig. 7-2. Simple examples

(a) the boost converter
(b) the SEPIC converter

For a simple example, the classical boost converter is shown in Fig. 7-2(a) for ready reference. There is a single inductor L_1 in the topology. Searching the possible close-loops containing L_1, we find Loop 1 (source-L_1-S) and Loop 2 (source-L_1-D_o-C_o||R). An active switch exists in Loop 1, and a passive switch exists in Loop 2. Therefore, it can be known that I_R will not exist in the sub-mode 3 when the converter is operated in DCM.

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Reviewing the other classical dc-dc topologies, I_R phenomenon occurs in the classical Cûk/ZETA/SEPIC converters and disappears in the classical buck/buck-boost converters. For a 4th order example, the SEPIC converter is shown in Fig. 7-2(b). There are two inductors, L and L_1 in the topology. Searching the possible close-loops containing L or L_1, we find Loop 1 (source-L-S), Loop 2 (source-L-C_s-L_1) and Loop 3 (source-L-C_s-D_o-C_o||R). An active switch exists in Loop 1, and a passive switch exists in Loop 3. Loop 2 satisfies the existence conditions, and it contains L_1 simultaneously. Therefore, it can be known that I_R will exist in both L and L_1 during the sub-mode 3. Since a lot of in-depth study has been performed on this topology, the relative research results validate this phenomenon. Two more complex cases will be given in the following sub-sections, and their analysis procedure can be applied to the classical SEPIC converter.

C. Solving principles

Because the third sub-mode is determined by interactions caused by multiple parameters in the converter, the derivation of inductor current waveforms and output voltage V_o in the steady state is usually complicated. To perform a fast steady-state analysis, current filling efficiency m [3] is used here and it is defined as:

$$m = \frac{t_1 - dT}{(1-d)T}, \ (0 < m < 1) \tag{7.1}$$

Sub-modes 1-3 are thus expressed by $[0, dT]$, $[dT, dT+m(1-d)T]$ and $[dT+m(1-d), T]$, respectively. The current filling efficiency indicates the shape of steady-state waveform of i_L. It is an unknown and should be worked out. Considering the other unknown V_o, we should construct a set of two binary equations to obtain the steady-state performance. There are two general principles that describe the steady-state operation of dc-dc converters: the volt-second balance on inductors and the charge balance on capacitors. Applying inductor volt-second balance to L, we have:

$$\int_0^{dT} v_L dt + \int_{dT}^{m(1-d)T} v_L dt = 0 \tag{7.2}$$

During the sub-mode 2, partial or all of the energy stored in L is transferred to the capacitor C. It states that i_L is related to the capacitor current i_C. Applying the capacitor charges balance to C, we have:

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$$\int_{dT}^{m(1-d)T} i_C dt + \int_{0}^{dT} i_C dt + \int_{m(1-d)T}^{T} i_C dt = 0 \tag{7.3}$$

Usually (7.3) needs to be simplified to separate the unknowns m and V_o, and this step can be obtained by utilizing constraints between the average currents (I_{in} and I_o) and i_L (or Δi_L or I_R). Equations (7.2) and (7.3) can thus be combined and can derive a system of two binary equations as follows:

$$\begin{cases} f_1(m, V_o) = 0 \\ f_2(m, V_o) = 0 \end{cases} \tag{7.4}$$

The solution of (7.4) is the steady-state performance in DCM, and it is more convenient to compare the solving procedure with the conventional state-space method. The current filling efficiency parameter can also be utilized to solve the boundary condition between CCM and DCM. The physical meaning of the current filling efficiency is now independent of detailed inductor current values. The converter will operate in DCM as long as the current filling efficiency is smaller than *1*.

According to incomplete statistics, there have been more than *500* prototypes of dc-dc converters developed in the past six decades. All existing topologies were designed to meet the requirements of certain applications. In the following sub-sections, two novel high order dc-dc converter topologies are presented as examples, and an in-depth DCM analysis is performed to show the existence of the remaining inductor current phenomena.

7.2.2 Case Study: 5th order self-lift Luo converter

The 5th order self-lift Luo converter [48] shown in Fig. 7-3(a) contains two inductors, and the VL technique has been successfully applied to this topology. Its voltage transfer gains in CCM is equal to $1/(1-d)$. Here, it is assumed that the converter is operating in DCM. During sub-mode 1 (S is on), D_1 is on, while D_2 is off. The main inductor L_1 absorbs energy from the source V_{in}. In the mean time, the output inductor L_o absorbs energy from C_s. During sub-mode 2 (S is off), D_1 is off, while D_2 is on. C_s is charged by i_{L1} through D_2, and L_1 transfers its stored energy to C_s. Once stored energy of L_1 is invariable, D_2 will be off, and the converter enters sub-mode 3.

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Searching the possible close-loops containing L_1 or L_o, we find one loop (L_o-C_s-L_1-C_o||R-L_o) which satisfies the existence conditions of I_R. Therefore, the DCM analysis should consider effects caused by I_R. Since this close-loop contains two inductors, it means both of them have the phenomena of I_R. This converter provides a positive output voltage, so I_R flowing through L_1 is negative with respect to the reference direction shown in Fig. 7-3(a). Analogously, I_R flowing through L_o is positive. The corresponding steady-state waveforms with enlarged variations can be derived and shown in Fig 7-3(b) and (c), respectively.

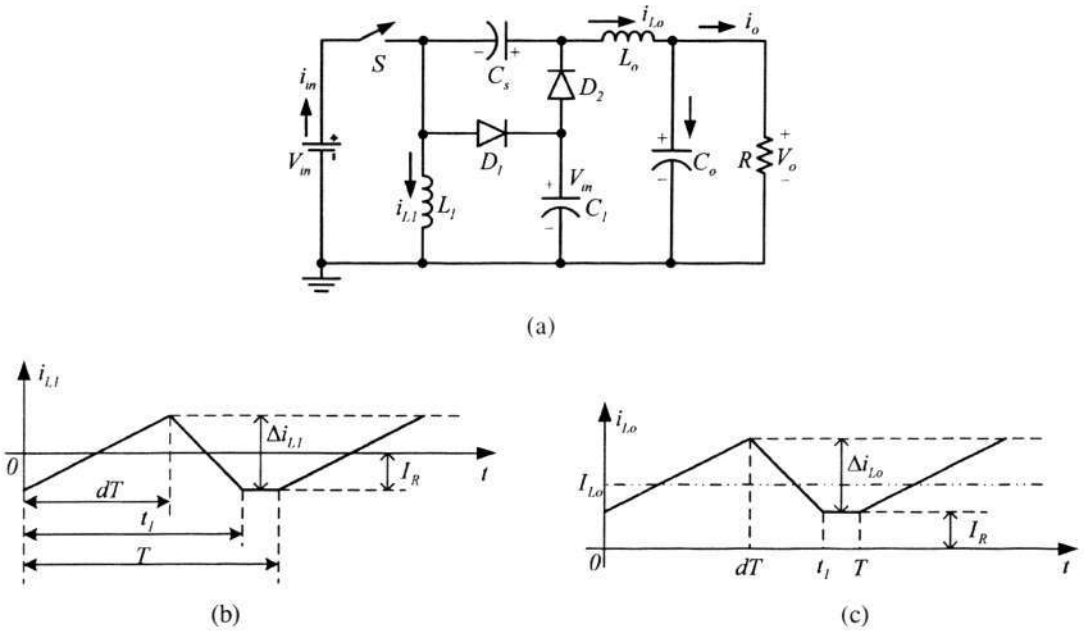

Fig. 7-3. The 5th order self-lift Luo converter

(a) topology
(b) waveform of i_{L1} with enlarged variations
(c) waveform of i_{Lo} with enlarged variations.

The voltages across L_1 are V_{in} during sub-mode 1 and $-(V_o - V_{in})$ during sub-mode 2. Thus, utilizing the volt-second balance principle and (7.2), we have

$$f_1(m, V_o) = dV_{in} - m(1-d)(V_o - V_{in}) = 0 \tag{7.5}$$

In addition, the transferred charges of L_1 during $[dT,\ dT+m(1-d)T]$ are equal to $m(1-d)T\Delta i_{L1}/2$, which compensate the total discharges of C_s. Thus, utilizing the charges balance principle and (7.3), we have

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$$\frac{\Delta i_{L1}}{2} m(1-d)T = I_R T + \frac{\Delta i_{L1}}{2} dT \tag{7.6}$$

Furthermore, the current constraint between I_R and I_o reflects the effects on the 5th order Luo converter caused by I_R. Since L_o is the main energy-stored component for load, we can ignore the effects caused by C_o, and can consider that the steady-state waveform of instantaneous output current i_o is the same to Fig. 7-3(c). In practical design, L_o is usually the same with L_1 to simplify analysis. Hence, integration of i_o over one switching cycle yields I_o , and it is expressed by

$$I_o = \frac{V_o}{R} = I_R + \frac{\Delta i_{L1}}{2}[m(1-d)+d] \tag{7.7}$$

Combining (7.6) and (7.7), we eliminate I_R and get a canonical binary equation as follows:

$$f_2(m, V_o) = \frac{V_o}{R} - m(1-d)\Delta i_{L1} = 0 \tag{7.8}$$

It can be known from the foregoing analysis on sub-mode 1 that Δi_{L1} is equal to $V_{in} dT / L_1$. Combining (7.5) and (7.8), we can obtain the following steady-state performance:

$$\begin{cases} m = \dfrac{1+\sqrt{1+4d^2 Z_{N1}}}{2d(1-d)Z_{N1}} \\ V_o = \dfrac{1}{2}(1+\sqrt{1+4d^2 Z_{N1}})V_{in} \end{cases} \tag{7.9}$$

where Z_{N1} is defined as the normalized load $R/(fL_1)$.

We can substitute (7.9) into (7.7) and work out the following remaining inductor current I_R:

$$I_R = \frac{V_{in}}{4R}[1+\sqrt{1+4d^2 Z_{N1}} - 2d^2 Z_{N1}] \tag{7.10}$$

When the converter is operating under the boundary condition between CCM and DCM, m will be equal to 1. Consequently, we can get the boundary normalized load $Z_{N1\text{-}B}$ from (7.9) as:

$$Z_{N1-B} = \frac{1}{d(1-d)^2} \tag{7.11}$$

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Using (7.9), (7.11) and CCM performance, we can draw the boundary curve between CCM and DCM, which is shown in Fig. 7-4 for ready reference. When the operating point is on the boundary curve of Fig. 7-4, the boundary remaining inductor current $I_{R\text{-}B}$ can be derived from (7.10). The derived $I_{R\text{-}B}$ can be regarded as the minimum value of instantaneous inductor currents under the given duty ratio. Choosing V_{in}/R as the base current, we define the pu boundary remaining inductor current, $I_{R\text{-}B(pu)}$, and the curve of $I_{R\text{-}B(pu)}$ against duty ratio d is shown in Fig. 7-5. It is seen that $I_{R\text{-}B(pu)}$ will be zero when d is *0.5*. Therefore, only at this event, will the inductor current decrease to zero at the beginning of the next switching cycle.

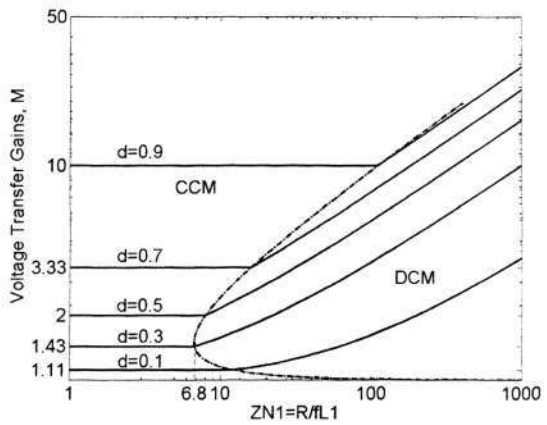

Fig. 7-4. The 5th order self-lift Luo converter: boundary curve (dash-dot line) between CCM and DCM, and voltage transfer gains against Z_{N1}

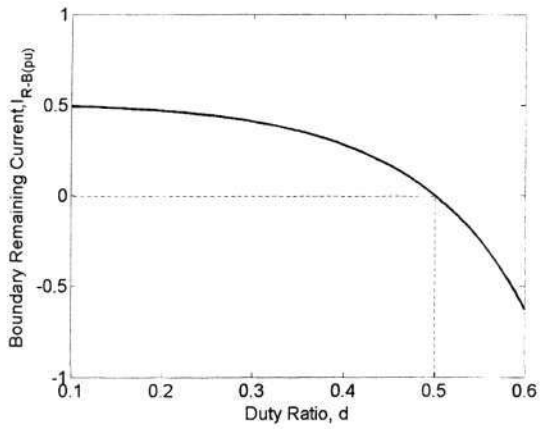

Fig. 7-5. The 5th order self-lift Luo converter: curve of pu boundary remaining inductor current, $I_{R\text{-}B(pu)}$ against duty ratio d

For this case, if the parameters are chosen as follows: V_{in}=*20V*, R=*100Ω*, L_1=L_o=*500μH*, C=C_1=*22μF*, C_o=*11μF*, d=*0.3* and f=$1/T$=*20kHz*, the boundary

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normalized load $Z_{N1\text{-}B}$ will be *6.8* according to (7.11). Normalized load Z_{N1} of this case is *10*, the corresponding operation point will be located in the right area of the boundary curve shown in Fig. 7-4. So the converter will be operating in the energy DCM. According to (7.9) and (7.10), we obtain $m=0.749$ $V_o=31.44V$ and $I_R=0.067A$.

To verify the theoretical analysis, the same parameters are chosen, and PSIM simulation software was applied to the circuit shown in Fig. 7-3 (a). The simulation results are shown in Fig. 7-6, where curves in the subwindows stand for i_{L1}, V_o and i_{Lo}, respectively. It states that I_R exists during sub-mode 3. And the practical simulation waveforms accord with the estimated current shapes described in Fig. 7-3(b) and (c). Using the measurement tool of PSIM, we get $m=0.75$ $V_o=31.25V$ and $I_R=0.065A$. The steady-state performance in the simulation is identically matching the theoretical analysis.

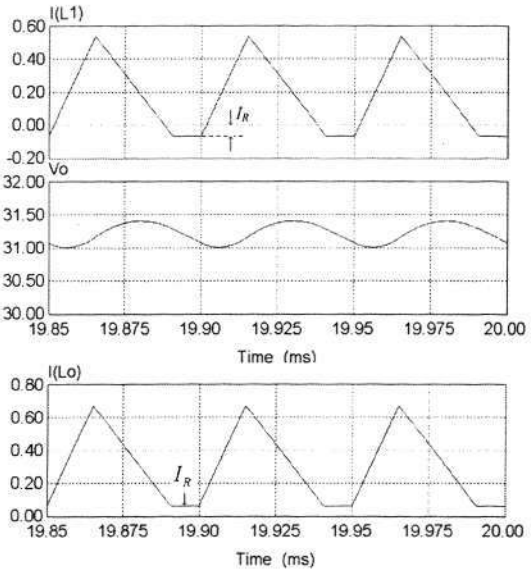

Fig. 7-6. The 5th order self-lift Luo converter: steady-state simulation waveforms in PSIM

7.2.3 Case Study: 7th order re-lift VL-Type SEPIC converter

The 7th order re-lift VL-type SEPIC converter shown in Fig. 7-7(a) has been introduced in Chapter 2. It is more complex in terms of structure and component number. Its voltage transfer gain in CCM is equal to $2/(1\text{-}d)$. Since this converter can provide higher voltage transfer gains than the conventional SEPIC converter, it has many potential industrial applications. Here, we assume it is operating in DCM. During sub-

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mode 1 (synchronous switches S and S_1 are on), both D_1 and D_2 are on, while D_o is off. L_1 and L_2 absorb energy from C_s. In the mean time L absorbs energy from the source. During sub-mode 2 (S and S_1 are off), both D_1 and D_2 are off, while D_o are on. C_s is charged by i_L. L_1, C_1, L_2, C_2 and D_o are in series and transfer stored energy to C_o and R. It is noted that L_1 and L_2 are usually the same to simplify the practical engineering design. Once stored energy of L_1 is invariable, D_o will be off, which make the converter enter into sub-mode 3. The analysis of the conventional SEPIC converter can also refer to the following procedure.

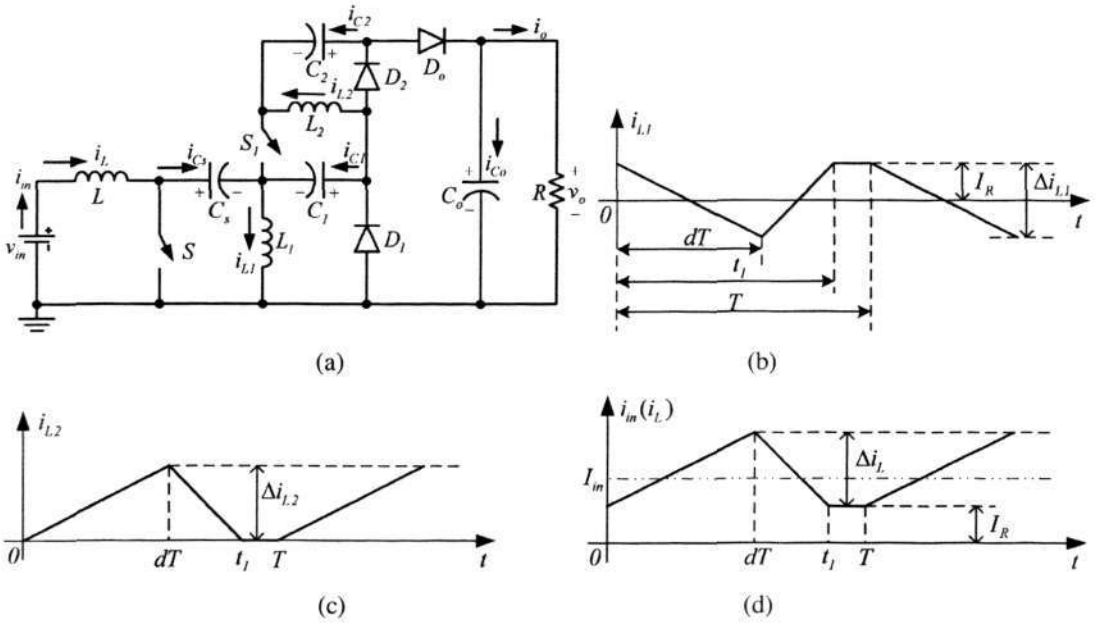

Fig. 7-7. The 7th order re-lift VL-type SEPIC converter

(a) topology
(b) waveform of i_{L1} with enlarged variations
(c) waveform of i_{L2} with enlarged variations
(d) waveform of i_{in} (i_L) with enlarged variations.

Searching the possible close-loops containing L, L_1 and L_2, we find one loop (source-L-C_s-L_1-source) which satisfies the existence conditions of I_R. Therefore, the DCM analysis should consider effects caused by I_R. Since this close-loop contains L and L_1, it means both of them have the phenomena of I_R. For L_2, no close-loop which satisfies the existence conditions of I_R can be found, so i_{L2} will be decreased to zero during the sub-mode 3. The source provides a positive input current, so I_R flowing through L_1 is positive with respect to the reference direction shown in Fig. 7-7(a). Analogously, I_R flowing through L is positive. It is noted that C_s charges L_1 during sub-mode 1 in a reverse

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direction, which will makes i_{L1} decrease. The corresponding steady-state waveforms with enlarged variations can be derived and shown in Fig 7-7(b-d), respectively.

In DCM, because current i_{L2} increases during switching-on and decreases during the period from dT to $(1\text{-}d)mT$, we thus have

$$V_{L2-off} = -\frac{d}{(1-d)m}V_{in}$$

The voltages across L_1 are V_{in} during sub-mode 1 and $-(V_{Co}-V_{C1}-V_{C2}+V_{L2-off})$ during sub-mode 2. Thus, utilizing the volt-second balance principle and (7.2) to L_1, we have

$$f_1(m,V_o) = dV_{in} - m(1-d)(V_o - 2V_{in} - \frac{D}{(1-D)m}V_{in}) = 0 \tag{7.12}$$

In addition, the transferred charges of L_1 during $[dT,\ dT+m(1\text{-}d)T]$ are equal to $m(1-d)T\Delta i_{L1}/2$, which compensate the total consumed charges of the load. Thus, utilizing the charges balance principle and (7.3), we have

$$I_o T = \frac{1}{2}m(1-d)T\Delta i_{L1} \tag{7.13}$$

Rewriting (7.13) results in a canonical binary equation as follows:

$$f_2(m,V_o) = \frac{V_o}{R} - \frac{1}{2}m(1-d)\Delta i_{L1} = 0 \tag{7.14}$$

It can be known from the foregoing analysis on sub-mode 1 that Δi_{L1} is equal to $V_{in}dT/L_1$. Combining (7.12) and (7.14), we can obtain the following steady-state performance:

$$\begin{cases} m = \dfrac{2+2\sqrt{1+d^2Z_{N1}}}{d(1-d)Z_{N1}} \\ V_o = (1+\sqrt{1+d^2Z_{N1}})V_{in} \end{cases} \tag{7.15}$$

where Z_{N1} is defined as the normalized load $R/(fL_1)$.

Furthermore, the current constraint between I_R and I_{in} reflects the effects on the 7th order VL-type SEPIC converter caused by I_R. Assuming C_s is sufficiently large, we can

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consider that the steady-state waveform of instantaneous current i_{in} is the same to Fig. 7-7(d). Integration of i_{in} over one switching cycle yields I_{in}, and it is expressed by

$$I_{in} = I_L = \frac{V_o}{R} \cdot \frac{V_o}{V_{in}} = I_R + \frac{\Delta i_L}{2}[m(1-d)+d] \tag{7.16}$$

We can substitute (7.15) into (7.16) and work out the following remaining inductor current I_R:

$$I_R = \frac{V_{in}(1+\sqrt{1+d^2 Z_{N1}})}{R}(1+\sqrt{1+d^2 Z_{N1}} - \frac{Z_N}{Z_{N1}}) - \frac{V_{in} d^2 Z_{N1}}{2R}\frac{Z_N}{Z_{N1}} \tag{7.17}$$

Where: $Z_N = R/(fL)$ and $Z_{N1} = R/(fL_1)$

When the converter is operating under the boundary condition between CCM and DCM, m will be equal to 1. Consequently, we can get the boundary normalized load $Z_{N1\text{-}B}$ from (7.15) as:

$$Z_{N1-B} = \frac{4}{d(1-d)^2} \tag{7.18}$$

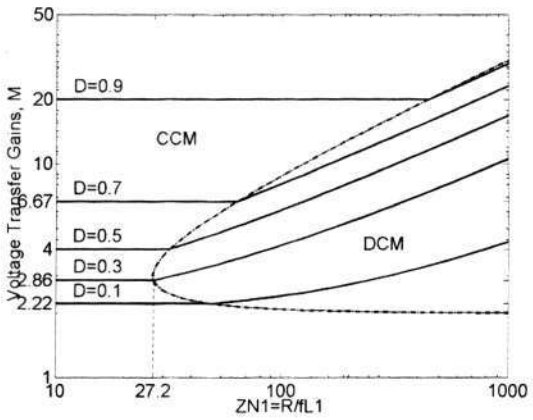

Fig. 7-8. The 7th order re-lift VL-type SEPIC converter: boundary curve (dash-dot line) between CCM and DCM, and voltage transfer gains against Z_{N1}

Using (7.15), (7.18) and CCM performance, we can draw the boundary curve between CCM and DCM, which is shown in Fig. 7-8 for ready reference. When the operating point is on the boundary curve of Fig. 7-8, the boundary remaining inductor current $I_{R\text{-}B}$ can be derived from (7.17). The derived $I_{R\text{-}B}$ can be regarded as the minimum value of instantaneous inductor currents under the given duty ratio. Choosing V_{in}/R as the base

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current, we define the pu boundary remaining inductor current, $I_{R\text{-}B(pu)}$, and the curve of $I_{R\text{-}B(pu)}$ against duty ratio d under the assumption of $Z_N=Z_{N1}$ is shown in Fig. 7-9. The monotonic increase of $I_{R\text{-}B(pu)}$ in Fig. 7-9 indicates that in any event the inductor currents, i_L and i_{L1} will never be discontinuous.

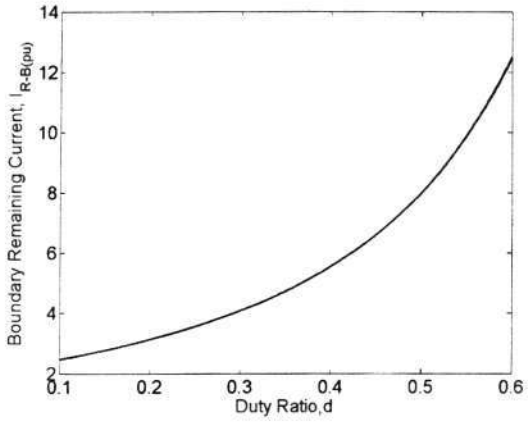

Fig. 7-9. The 7th order re-lift VL-type SEPIC converter: curve of pu boundary remaining inductor current, $I_{R\text{-}B(pu)}$ against duty ratio d

For this case, if the parameters are chosen as follows: $V_{in}=10V$, $R=1000\Omega$, $L=10mH$, $L_1=L_2=500\mu H$, $C_1=C_2=C_o=22\mu F$, $d=0.3$ and $f=1/T=20kHz$, the boundary normalized load $Z_{N1\text{-}B}$ will be 27.2. Since the normalized load Z_{N1} of this case is 100, the corresponding operation point will be located in the right area of the boundary curve shown in Fig. 7-8. So the converter will be operating in the energy DCM. According to (7.15) and (7.17), we obtain $m=0.396$, $V_o=41.63V$ and $I_R=0.17A$.

To verify the theoretical analysis, the same parameters are chosen, and PSIM simulation software was applied to the circuit shown in Fig. 7-7(a). The simulation results are shown in Fig. 7-10, where curves in the four subwindows stand for i_{L1}, V_o, i_L and i_{L2}, respectively. It states that I_R exists during sub-mode 3. And the practical simulation waveforms accord with the estimated current shapes described in Fig. 7-7(b-d). Using the measurement tool of PSIM, we get $m=0.4$ $V_o=41.83V$ and $I_R=0.17A$. The steady-state performance in the simulation is identically matching the theoretical analysis.

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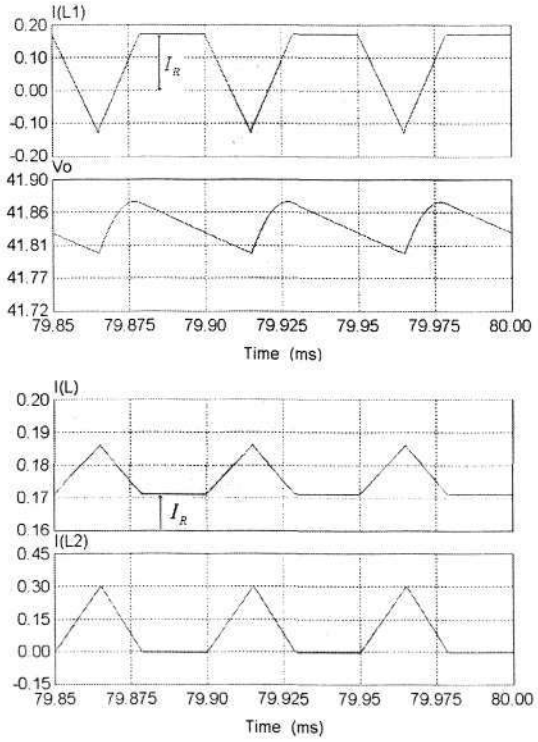

Fig. 7-10. The 7th order re-lift VL-type SEPIC converter: steady-state simulation waveforms in PSIM

7.3 Transient Analysis of Multi-State Converters Using System Energy Characteristics

The study of multi-state dc-dc power conversion techniques is restricted by the complicated inner switching behaviors. This section presents a general and unified transient analysis for various sorts of multi-state dc-dc converters from a viewpoint of their system energy characteristics.

7.3.1 Multi-State conversion techniques

A PWM dc-dc converter is generally operated in CCM, in which two states are usually switched periodically by actions of the switch. With the development of dc-dc conversion techniques, multi-state dc-dc conversion techniques have been proposed to overcome some disadvantages of conventional two-state dc-dc converters. For a dc-dc converter, multi-state operation in a cycle can be implemented by adding some additional switching

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devices [26]. An additional state is then produced. This can be regarded as an active approach because each state is determined by actions of the switches. Usually, the main inductor current in the converter is kept continuous during the whole cycle [26]. Here, this approach is termed *multi-state CCM conversion technique.* Another main implementation approach for multi-state operation is to make the conventional two-state converter operated in DCM. This can be regarded as a passive approach because the third state is determined by the discontinuous characteristics of main inductor current. Therefore, it can be termed *multi-state DCM conversion technique.*

Both of these two multi-state conversion techniques have higher voltage/current conversion capacity than two-state converters. They can also provide the control-to-output small-signal transfer function without zeros. So an appropriate and effective analytical method for multi-state dc-dc converters will stimulate their practical industrial application in future. Unfortunately, the multi-state operation increases the complexity in the inner circuit and causes much more complicated switching behaviors. So the transient performances of multi-state converters are difficult to be described accurately and conveniently.

7.3.2 Energy factor and modelling

There are some energy-storing components in a dc-dc converter and the corresponding stored energy will change during the transient process. Hence, the modelling method based on system energy characteristics is a novel approach in power electronics. Despite the long duration spent in researching on the energy storage characteristics in power dc-dc converters, there had been no clear understanding to reveal the relationship between the stored energy and the dynamics of dc-dc converters until a new concept, namely *energy factor* (*EF*) was proposed by F.L. Luo [104-106].

Using *EF* and its associated parameters, a conventional dc-dc converter in CCM (with two states) can be approximately described by a 2nd order transfer function $G(s)$ to reflect its transient performance.

$$G(s) = \frac{M \cdot \eta}{\tau \tau_d s^2 + \tau s + 1} \tag{7.19}$$

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The damping time constant τ_d and the time constant τ are concerned with the energy transfer process of every energy-stored element. They can be deduced from *EF* and its associated parameters. M is the ideal voltage transfer gain and η is the power transfer efficiency caused by the parasitic parameters. Since a linear transfer function is utilized to describe the transient performance of two-state dc-dc converters accurately, all the state variables should be averaged firstly. Hence, the harmonics yielded by the nonlinear switching networks will be eliminated, which is similar to the averaging models. The theoretical proof of this model has been introduced in [104-106] and supported by a large number of simulation and experimental results. Therefore, the study of system characteristics and introduction of new concept *EF* paved a new way for the modelling of dc-dc converters.

Based on the above-mentioned investigation of system energy characteristics for conventional two-state converters, we try to develop this energy-based method into the modelling process of multi-state dc-dc converters. The following sub-section focuses on the output transient performance (output voltage) and is released from the analysis on the inner nonlinear switching behaviors. According to the general transient performance of multi-state CCM and DCM converters, a unified modelling method is developed. The concepts of system energy parameters and the corresponding canonical definition are presented, by which the system model parameters of multi-state converters are deduced.

7.3.3 Switching operations and general transient performance

When a converter changes from one steady state to another, the corresponding stored energy changes. Therefore, there must be a transient process from one steady state to the new steady state. For the convenience of theoretical analysis hereafter, we choose the multi-state boost converters as the discussion objects. The multi-state CCM and DCM boost converters are discussed respectively here. Because these two sorts of boost converters are typical for the multi-state conversion technique, the analytical results can be extended to the other multi-state dc-dc converter topologies.

The topology of the multi-state CCM boost converter is shown in Fig. 7-11(a). This circuit was proposed by R. Omganti [110, 111] in 2001. Its typical inductor current

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waveform and switching signal waveforms are shown in Fig. 7-11(b) respectively. This converter is different from the classical boost converter operated in CCM, whose additional state is caused by the freewheeling of the main inductor current i_L. When the first state (energy storing mode, S_f and S_m are ON) and the second state (energy pumping mode, S_f and S_m are OFF) are completed, the freewheeling switch S_f and freewheeling diode D_f form a freewheeling loop, L-S_f-D_f, before the beginning of next cycle, which brings the third state (energy freewheeling mode, S_f is ON and S_m is OFF). The first duty ratio d_1, the second duty ratio d_2 and the last duty ratio d_3 are determined by the control signals, so there are no duty ratio constraints in each cycle.

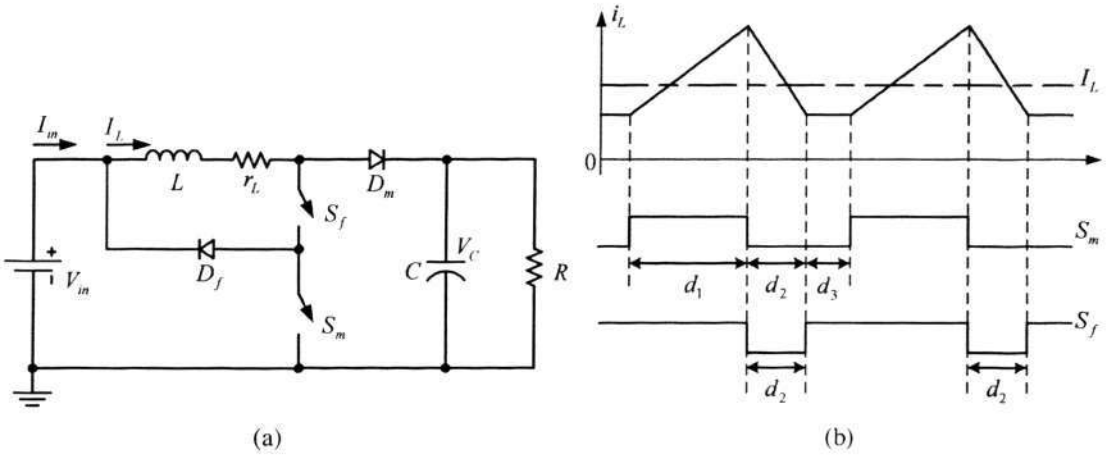

Fig. 7-11. The multi-state CCM boost converter.

(a) topology
(b) typical inductor waveform (r_L=0) and control signals.

The topology of the multi-state DCM boost converter is shown in Fig. 7-12(a). Its typical inductor current waveform and switching signal waveforms are shown in Fig. 7-12(b) respectively. The converter is operated in DCM due to the interactions caused by the load, switching frequency and the inductance. Because the second duty ratio d_2 has algebraic dependency on state and control variables, the complex duty ratio constraints have become the main difficulty in the conventional modelling methods.

From the above analysis, it can be seen that the nonlinear switching operation in above-mentioned multi-state conversion techniques are totally different. To find a unified modelling method, we carefully investigated the output transient performance of these two topologies. The circuit parameters' selection and power transfer efficiency η are two main factors which determine the output transient performance.

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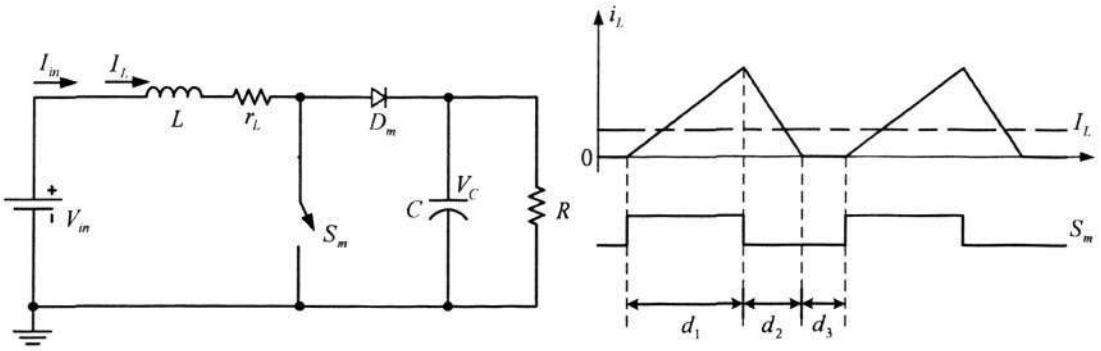
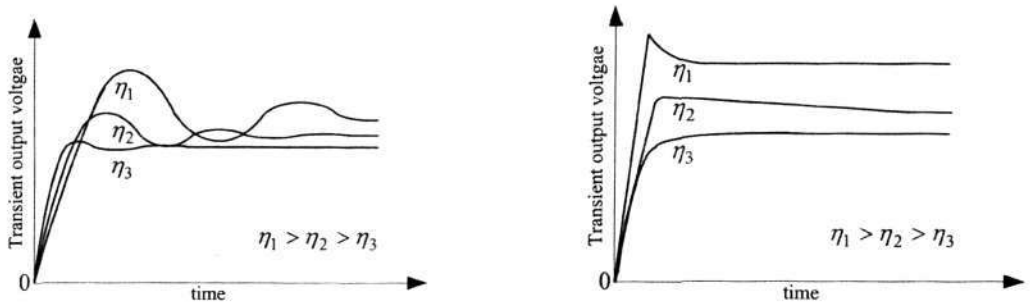


(a) (b)

Fig. 7-12. The multi-state DCM boost converter.

(a) topology
(b) typical inductor waveform (r_L=0) and control signals.



(a) (b)

Fig. 7-13. The general unit-step response curves with different values of η

(a) the multi-state CCM boost converter
(b) the multi-state DCM boost converter

Assuming that the topology and elements have been selected, the effects caused by the power efficiency are investigated. Under the different η conditions, the general time-domain unit-step response curves of the multi-state CCM boost converter can be referred to in Fig. 7-13(a). The responses indicate that the converter is similar to a 2nd order system (including underdamped, critically damped or overdamped system) and η can not change the system similarity. However, the general time-domain unit-step response curves of the multi-state DCM boost converter indicate that the converter under the different efficiency conditions has not the system similarity. It can be referred to in Fig. 7-13(b), and the derivation of the critical value, η_{crt} is given in the Appendix. When η is lower than η_{crt}, the DCM converter is much closer to a 2nd order overdamped system (can be downgraded to a 1st order inertia system). Hence, using a 2nd order transfer function,

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we can unify the modelling of CCM and DCM boost converter now. It is possible to describe the mathematical models of these two sorts of multi-state boost converters with 2^{nd} order transfer functions.

7.3.4 General rules and generalized system energy parameters

The crux of this unified modelling method for multi-state converters is to obtain the accurate time constant τ and damping time constant τ_d for its 2^{nd} order transfer functions. For a given dc-dc converter circuit, these two parameters can be termed *system model parameters*. The time constant τ is available to estimate the multi-state converter transient operation. The damping time constant τ_d is utilized to estimate the multi-state converter response with oscillation. *EF* and its associated parameters mentioned in [104-106] can be termed *system energy parameters*. They are used to reflect the energy-transferred characteristics during the whole transient process.

The steady-state information of each element needs to be examined before the beginning of transient process. After the ending of transient process, the corresponding steady-state information also needs to be examined. They include the averaging values of each state variable in the steady state, which are obtained as below:

$$I_L = \frac{1}{T}\int_0^T i_L(t)dt \qquad V_C = \frac{1}{T}\int_0^T v_C(t)dt \qquad I_{in} = \frac{1}{T}\int_0^T i_{in}(t)dt$$

It is similar to a "black box". We focus on the input and output information and neglect the complicated nonlinear switching behaviours in the inner circuit. The input and output information is the reflection of interactions caused by nonlinear characteristics.

The transient performance of a converter indicates that the stored and transferred energy in the circuit have been changed. If the converter is operated from the beginning zero state to the steady state, it can be called *the starting process*. We use the symbol "*_0*" in the subscript of the corresponding state variables for this steady–state. Assuming that the converter is in a normal steady state, when the converter is changed from the original steady state to the new steady state due to a certain operation or disturbance, it can be regarded as *the generalized transient process*. We use the symbol "*_1*" and "*_2*" in the subscript of the corresponding state variables to differentiate these two different

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steady states. The next part will give the detailed definition and generalized expressions of system energy parameters for dc-dc converters. They are the theoretical basis of the proposed modelling method. Based on the application of system energy parameters, the system model parameters can be obtained consequently.

Different from the original definition in [104-106], the physical meaning of every system energy parameter is modified here. They are the stored energy variation of inductor (*WL*), stored energy variation of capacitor (*WC*), stored energy variation (*SE*), pumping energy variation (*PE*), energy factor (*EF*) and capacitor/inductor stored energy variation ratio (*CIR*), energy losses variation (E_{loss}) and power efficiency (η). Here, the power losses are simulated by the series equivalent resistance of the inductor r_L to simplify the derivation. In addition, it is assumed that there are n_L inductors and n_c capacitors in a given converter. The generalized calculation expressions are shown in Table 7-1, respectively.

Table 7-1 Generalized expressions of system energy parameters

Parameters	Starting Process	Generalized Transient Process
W_{Lj}	$\frac{1}{2}L(I_{Lj\_0}^2-0)$	$\frac{1}{2}L(I_{Lj\_2}^2-I_{Lj\_1}^2)$
W_{Cj}	$\frac{1}{2}C(V_{Cj\_0}^2-0)$	$\frac{1}{2}C(V_{Cj\_2}^2-V_{Cj\_1}^2)$
SE	$\sum_{j=1}^{n}W_{Cj}+\sum_{j=1}^{n}W_{Lj}$	
PE	$V_{in\_0}I_{in\_0}T$	$(V_{in\_2}I_{in\_2}-V_{in\_1}I_{in\_1})T$
EF	SE/PE	
CIR	$\sum_{j=1}^{n}W_{Cj}\Big/\sum_{j=1}^{n}W_{Lj}$	
P_{loss}	$\sum_{j=1}^{n}I_{Lj\_0}^2r_{Lj}$	$\sum_{j=1}^{n}(I_{Lj\_2}^2-I_{Lj\_1}^2)r_{Lj}$
E_{loss}	$P_{loss}T$	
η	$\eta=(PE-E_{loss})/PE$	

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7.3.5 System model parameters for multi-state boost converters

The generalized system energy parameters of dc-dc converters in Table 7-1 can deduce the system model parameters of multi-state boost converters (including multi-state CCM and DCM boost converters). They are written as:

$$\tau = \frac{2T \cdot EF}{1+CIR}\left(1+\frac{1-\eta}{\eta}\cdot CIR\right) \tag{7.20}$$

$$\tau_d = \frac{2T \cdot EF}{1+CIR}\frac{CIR}{\eta+CIR(1-\eta)} \tag{7.21}$$

The detailed derivation can be referred to in Appendix.1. Theoretically, τ and τ_d are invariable. Then the mathematical models of multi-state converters can be obtained quickly. The large-signal transfer function for the generalized transient process can be written as:

$$G(s) = \frac{(V_{o\_2} - V_{o\_1})/(V_{in\_2} - V_{in\_1})}{\tau\tau_d s^2 + \tau s + 1} \tag{7.22}$$

The time constant ratio ξ of a dc-dc converter is defined as:

$$\xi = \frac{\tau_d}{\tau} = \frac{CIR}{\eta(1+CIR\frac{1-\eta}{\eta})^2} \tag{7.23}$$

ξ is used to estimate transient response with oscillation. In addition, it is an index for the variation of stored energy. When ξ is very small, the oscillation of the response will disappear. The model is approximately similar to a 1st order inertia element. Then τ_d can be omitted (i.e. $\tau_d = 0$) and the generalized large-signal transfer function (7.22) is downgraded from 2nd to 1st order as below:

$$G(s) = \frac{(V_{o\_2} - V_{o\_1})/(V_{in\_2} - V_{in\_1})}{1+\tau s} \tag{7.24}$$

Small-signal models reflect the dynamics caused by the small perturbations of a steady state, and they can be described by 2nd order models with the same eigenvalues. Hence, referring to the traditional models in Table A.I, we can use the above-derived system model parameters to rewrite the characteristic equation and derive the new small-signal transfer functions of the multi-state CCM boost converter which are tabulated in Table

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7-2. Owing to energy freewheeling mode added, there is no zero in the control-to-output transfer function. There exist the zeros in the output impedance transfer function and input admittance transfer function. They also can be expressed by the system energy parameters. Analogously, we refer to traditional models in [11-15] and use the above-derived system model parameters to derive the new small-signal transfer functions of the multi-state DCM boost converter tabulated in Table 7-3.

Table 7-2 New small-signal transfer functions of the multi-state CCM boost converter

Proposed Small-Signal Models		
$\frac{\hat{v}_o}{\hat{v}_{in}} = \frac{M_T\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_T\eta = \frac{V_o}{V_{in}}$
$\frac{\hat{v}_o}{\hat{d}_1} = \frac{M_C\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_C\eta = \frac{V_g}{D_2}\eta$
$\frac{\hat{v}_o}{\hat{i}_o} = \frac{M_o\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_o\eta = \frac{r_L}{D_2^2}(1 + s\frac{2T \cdot EF}{(1-\eta)(1+CIR)})$
$\frac{\hat{i}_{in}}{\hat{v}_{in}} = \frac{M_i\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_i\eta = \frac{(D_1+D_2)^2}{RD_2^2}(1 + s\frac{2T \cdot EF \cdot CIR}{\eta(1+CIR)})$

Table 7-3 New small-signal transfer functions of the multi-state DCM boost converter

Proposed Small-Signal Models		
$\frac{\hat{v}_o}{\hat{v}_{in}} = \frac{M_T\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_T\eta = \frac{V_o}{V_{in}}$
$\frac{\hat{v}_o}{\hat{d}_1} = \frac{M_C\eta}{\tau\tau_d s^2 + \tau s + 1}$	Where:	$M_C\eta = \frac{2MV_{in}\eta}{2M-1}\sqrt{\frac{\rho M}{M-1}}$ and $\rho = \frac{2Lf}{R}$

7.3.6 Qualitative analysis

From the analysis in the above parts, it is known that the large-signal transfer function of multi-state converters (including CCM and DCM) can be described by a normalized 2nd order model as below:

$$G(s) = \frac{M}{\tau\tau_d s^2 + \tau s + 1} = \frac{M}{\xi\tau^2 s^2 + \tau s + 1} \tag{7.25}$$

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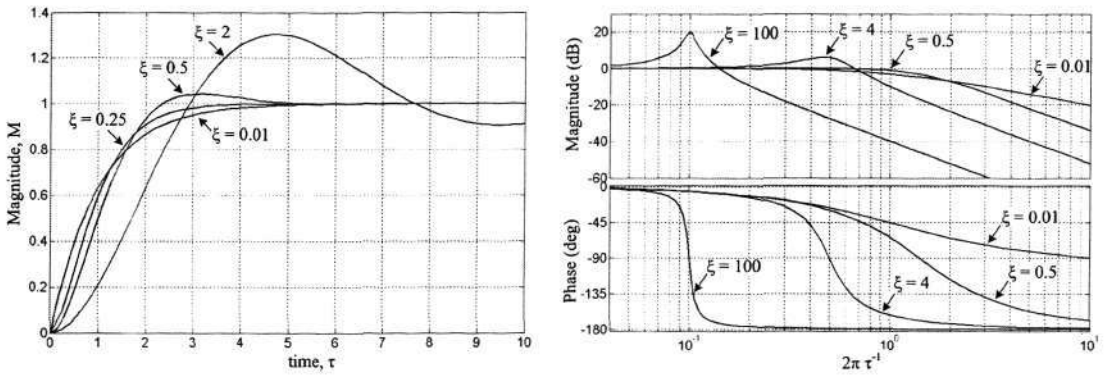
The basic small-signal transfer functions (input-to-output and control-to-output) of multi-state converter also can be unified to a normalized 2nd order model expression without zeros, which is written as:

$$\hat{G}(s)=\frac{M\eta}{\tau\tau_d s^2+\tau s+1}=\frac{M\eta}{\xi\tau^2 s^2+\tau s+1} \tag{7.26}$$

The qualitative analysis curves of the above normalized 2nd order system with various ξ are illustrated in Fig. 7-14. Referring to Fig. 7-14(a), the critical value of ξ in the time-domain, ξ_t is equal to *0.25*. This value is useful for the analysis of large-signal models and its calculation process can be referred to in the Appendix. 3. The power efficiency η has the mathematical relation with ξ, which is described by (7.23). If η makes the corresponding ξ lower than *0.25*, the large-signal model will be likely a 1st order function. If we improve the performance of the converter, the corresponding ξ will be higher than *0.25* along with the increasing of η. The oscillation will appear in the transient process. The corresponding large-signal model will be a typical 2nd order function.

Referring to Fig. 7-14(b), the critical value of ξ in the frequency-domain, ξ_f is equal to *0.5*. This value is useful for the analysis of small-signal models and its calculation process can also be referred to in the Appendix.3. For a CCM converter, experimental data indicate that the frequency response curve of its small-signal model usually has a resonance hump at the corner frequency. In the contrary, the resonance hump doesn't exist in the bode plot for a DCM converter.



(a) (b)

Fig. 7-14. Qualitative analysis of normalized the normalized 2nd order system

(a) time-domain analysis: unit-step response curves.
(b) frequency-domain analysis: bode plot curves.

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The above qualitative analysis is based on the fact the multi-state CCM/DCM converters are close to a 2nd order system. It is noted that the transient performance of the DCM converter may deviate from the general 2nd order system response if η is larger than η_{crt} (usually near *100%*). Therefore, there is a power efficiency constraint for modelling DCM converters using a 2nd order transfer function. According to (7.23), we let:

$$\frac{CIR}{\eta_{crt}(1+CIR\frac{1-\eta_{crt}}{\eta_{crt}})^2}=\xi_t=0.25\text{, thus}$$

$$\eta_{crt}=\frac{CIR}{(\sqrt{CIR}+1)^2} \tag{7.27}$$

Equation (7.27) indicates that η_{crt} is not a constant and determined by *CIR* of different DCM converters. For a given DCM converter, if $\eta>\eta_{crt}$, the practical transient process will exhibit the nonlinear characteristics with an overshoot as shown in Fig. 7-13(b). Since this special phenomenon is concerned with some nonlinear characteristics of dc-dc converters, it is not to be considered in this chapter.

We compare the classical method, signal flow graph and state space averaging with the proposed method here. The signal flow graph method is derived from the state space averaging method, and in fact they are equivalent. When the signal flow graph method is applied to multi-state dc-dc converters, three individual graphs, G_1, G_2 and G_3 should be drawn for the combination. Analogously, for the state-space averaging method, three individual state-space equations Q_1, Q_2 and Q_3, should be constructed before weight averaging. Both of the combined graph G and combined equation Q need much more procedures to obtain the transient model compared with the proposed method. This is because the proposed method needs only two system model parameters, which can be worked out according to the presented equations. Additionally, it is noted that the system model parameters' derivation is based on the preliminary work of classical methods (see Appendix). The accuracy of the proposed method is very close to that of the classical methods under the second order condition. Therefore, the main advantage of our method is a faster and clearer derivation process against classical methods. Furthermore, when the multi-state converter consists of a large number of elements, the proposed method will significantly reduce the order of the system.

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7.3.7 Analysis Example: The multi-state CCM boost converter

Fig. 7-11 shows the multi-state CCM boost converter with conduction duty ratio d_1, d_2.and d_3. The parameters are: $V_{in}=10V$, $f=50\ kHz$, $d_1=0.55$, $d_2=0.3$, $L=300\mu H$, $C=110\mu F$ and $R=10\Omega$. There are some power losses, assuming that the inductor resistance $r_L=0.15\Omega$. The following modelling examples are considered.

A. The starting process

The initial state of every parameter is zero. After the starting process, the converter will be operated in a steady state. We then obtain $V_{in\_0}=10V$, $V_o=24.15V$, $I_{L\_0}=7.889A$, $I_{in\_0}=6.767A$ and $P_{loss}=r_L I_{L\_0}^2=9.335W$. The corresponding system energy parameters are calculated and given in Table 7-4.

Therefore, the system model parameters are:

$$\tau=\frac{2T\cdot EF}{1+CIR}(1+\frac{1-\eta}{\eta}\cdot CIR)=427.5\mu s \tag{7.28}$$

$$\tau_d=\frac{2T\cdot EF}{1+CIR}\frac{CIR}{\eta+CIR(1-\eta)}=709.4\mu s \tag{7.29}$$

Since $\xi=\tau_d/\tau=1.66>0.25$, the large-signal transfer function of this converter for this given transient process has two poles ($-s_1$ and $-s_2$) that are located in the Left-hand half plane (LHHP). The large-signal transfer function is:

$$\frac{v_o}{v_{in}}=\frac{M_T\eta}{\tau\tau_d s^2+\tau s+1}=\frac{M_T\eta/\tau\tau_d}{(s+s_1)(s+s_2)}$$

where: $s_1=\sigma+j\omega$ and $s_2=\sigma-j\omega$ with

$$\sigma=\frac{1}{2\tau_d}=\frac{1}{2\times709.4\times10^{-6}}=704.82Hz \text{ and}$$

$$\omega=\frac{\sqrt{4\tau\tau_d-\tau^2}}{2\tau\tau_d}=\frac{1015\times10^6}{606537}=1.674krad/s$$

Hence, the step response (transient process from initial zero state to the steady state) is:

$$v_o(t)=M[1-e^{-\frac{t}{2\tau_d}}(\cos\omega t-\frac{1}{\sqrt{4\tau_d/\tau-1}}\sin\omega t)]v_{in}$$

$$=24.15[1-e^{-\frac{t}{0.0014188}}(\cos 1674t+0.421\sin 1674t)] \tag{7.30}$$

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Referring to Table 7-2, the impulse responses (interference recovery process) for input-to-output and control-to-output small-signal models can be written in a normalized form. i.e.

$$\Delta v_o(t) = \frac{2U}{\sqrt{4\tau_d/\tau - 1}} e^{-\frac{1}{2\tau_d}} \sin \omega t = 0.842U e^{-\frac{1}{0.0014188}} \sin 1674t \tag{7.31}$$

Where: U is the normalized interference signal.

The generalized transient process

If the input voltage is changed from the above mentioned state to a new one, $V_{in\_2}=15V$ ($V_{in\_1}=10V$, $I_{in\_1}=6.767A$) owing to a step signal at a certain instance, we then obtain $V_{o\_2}=36.51V$, $I_{L\_2}=12.085A$, $I_{in\_2}=10.305A$ and $P_{loss}=r_L(I_{L\_2}^2-I_{L\_1}^2)=12.572W$. The corresponding system energy parameters are also calculated and given in Table 7-4.

Table 7-4 System energy parameters of the multi-state CCM boost converter

	PE	W_C	W_L	E_{loss}	SE	η	EF	CIR
The starting process	1.353mJ	32.077m	9.335mJ	0.186mJ	41.412m	0.862	30.6	3.44
The generalized transient	1.738mJ	41.237m	12.572m	0.251mJ	53.809m	0.856	30.9	3.28

Therefore, the system model parameters are:

$$\tau = \frac{2T \cdot EF}{1+CIR}\left(1+\frac{1-\eta}{\eta}\cdot CIR\right) = 448.1\mu s \tag{7.32}$$

$$\tau_d = \frac{2T \cdot EF}{1+CIR}\frac{CIR}{\eta + CIR(1-\eta)} = 713.1\mu s \tag{7.33}$$

Since $\xi = \tau_d/\tau = 1.6 > 0.25$,

$$\sigma = \frac{1}{2\tau_d} = \frac{1}{2\times 713.1\times 10^{-6}} = 701.16Hz \text{ and}$$

$$\omega = \frac{\sqrt{4\tau\tau_d - \tau^2}}{2\tau\tau_d} = \frac{1038\times 10^6}{639080} = 1.624krad/s$$

Hence, the step response (transient process from steady state 1 to the steady state 2) is

$$v_o(t) = 24.15 + (36.51 - 24.15)[1 - e^{-\frac{1}{0.0014262}}(\cos 1624t + 0.43\sin 1624t)] \tag{7.34}$$

The impulse responses (interference recovery process) for input-to-output and control-to-output small-signal models can be written in a normalized form. i.e.

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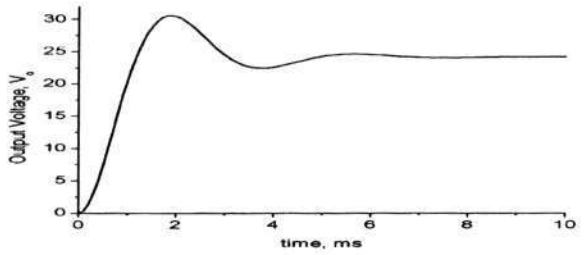
$$\Delta v_2(t) = 0.86Ue^{-\frac{t}{0.001426}} \sin 1624t \tag{7.35}$$

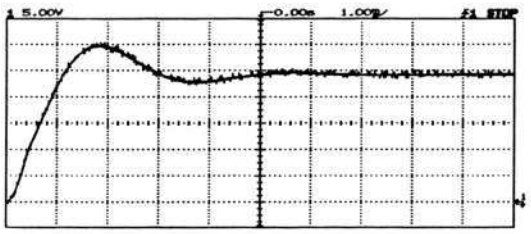
Where: U is the normalized interference signal.

Comparing (7.30, 7.31) with (7.34, 7.35), we find they are very close. Theoretically, τ and τ_d are constants. If the parasitic parameters of the converter vary due to the long-time operation, the modelling calculation based on the different processes will result in the different sets of τ and τ_d.

B. Model verification



(a)



(b)

Fig. 7-15. Large-signal step response of multi-state CCM boost converter

(a) Response curve described by the proposed model (7.30)
(b) Experimental curve

To verify the proposed models, the experimental circuit with the above-mentioned parameters has been constructed. The diodes are fast switching diodes so that the effects of reverse recovery are negligible for the analysis and calculation. The switches are comprised of several MOSFET devices in parallel so that the equivalent drain-source ON resistance can be negligible. The step response described by the proposed large-signal model is shown in Fig. 7-15(a), which is compared with the experimental curve in Fig. 7-15(b). The impulse response described by the proposed small-signal model is shown in

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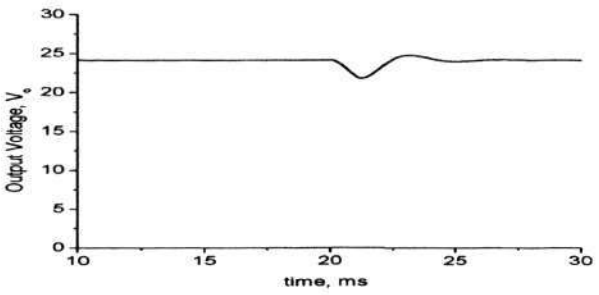
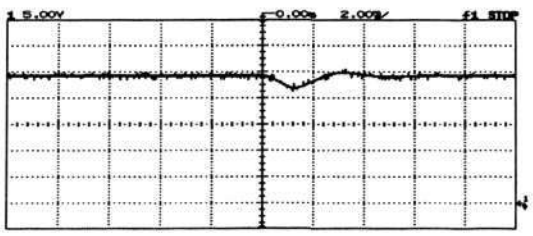
Fig. 7-16(a), which is compared with the experimental curve in Fig. 16(b). On the main indexes such as settling time, rising time and peak time, the experimental results have a good agreement with the simulation curves of proposed models.



(a)



(b)

Fig. 7-16. **Small-signal impulse response of multi-state CCM boost converter**

(a) Response curve described by the proposed model (7.31)
(b) Experimental curve

7.3.8 Analysis Example: The multi-state DCM boost converter

Fig. 7-12 shows the conventional three-state DCM boost converter with conduction duty ratio d_1, d_2.and $(1\text{-}d_1\text{-}d_2)$. The parameters are: $V_{in}=5V$, $f=50kHz$, $d_1=0.5$, $L=10\mu H$, $C=110\mu F$ and $R=20\Omega$. Duty ratio d_2 and d_3 are determined by the circuit configuration and load condition. There are some power losses, assuming that the inductor resistance $r_L= 1\Omega$.

A. The starting process

In the initial state of the converter, all the parameters are zero. After the transient process, the converter will be operated in a steady state. We then obtain $V_{in\_0}=5V$,

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V_o=8.719V, I_{L_0}=I_{in_0}=1.356A and $P_{loss} = r_L I_{L\_0}^2 = 1.8387W$. The corresponding system energy parameters are calculated and given in Table 7-5.

Table 7-5 System energy parameters of the multi-state DCM boost converter

PE	W_C	W_L	E_{loss}	SE	η / η_{crt}	EF	CIR
0.1356mJ	4.2mJ	0.009194mJ	0.03677mJ	4.2mJ	0.73 / 0.91	30.9	454.79

The example meets the requirement of $\eta < \eta_{crt}$, so the proposed method can be used. Therefore, the system model parameters are:

$$\tau = \frac{2T \cdot EF}{1+CIR}(1+\frac{1-\eta}{\eta} \cdot CIR) = 462\mu s \tag{7.36}$$

$$\tau_d = \frac{2T \cdot EF}{1+CIR}\frac{CIR}{\eta + CIR(1-\eta)} = 10\mu s \tag{7.37}$$

Since $\xi = \tau_d / \tau = 0.022 << 0.25$, τ_d can be omitted (i.e. $\tau_d = 0$). Under such a condition, the mathematical model of DCM converter can be regarded as an inertia element. According to (7.24), the step transient response (transient process from initial state to the steady state) is derived:

$$v_o(t) = Me^{-\frac{t}{\tau}} v_{in} = 8.719(1 - e^{-\frac{t}{462\times10^{-6}}}) \tag{7.38}$$

The ideal impulse interference response (interference recovery process) is:

$$\Delta v_o(t) = Ue^{-\frac{t}{\tau}} = Ue^{-\frac{t}{462\times10^{-6}}} \tag{7.39}$$

Where: U is the normalized interference signal.

B. Model verification

To verify the proposed models, the experimental circuit under the small time constant ratio condition has been constructed according to the same principles as introduced in foregoing sub-section. The above-mentioned parameters are selected. The step response described by the proposed large-signal model is shown in Fig. 7-17(a), which is compared with the experimental curve in Fig. 7-17(b). The impulse response described by the proposed small-signal model is shown in Fig. 7-18(a), which is compared with the

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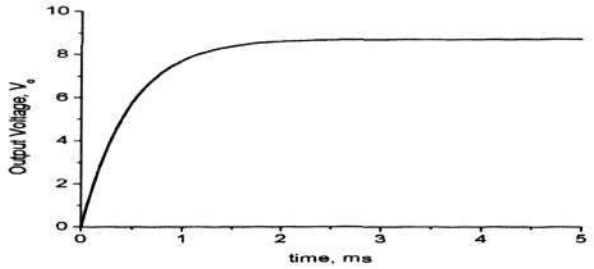
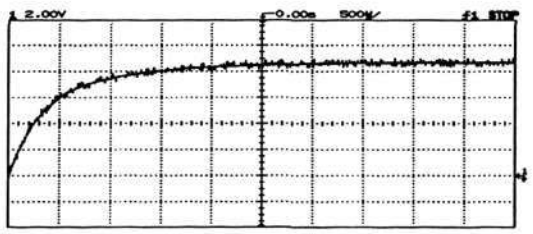
experimental curve in Fig. 7-18(b). All the experimental results accord with the simulation curves of proposed models on the main response indexes.



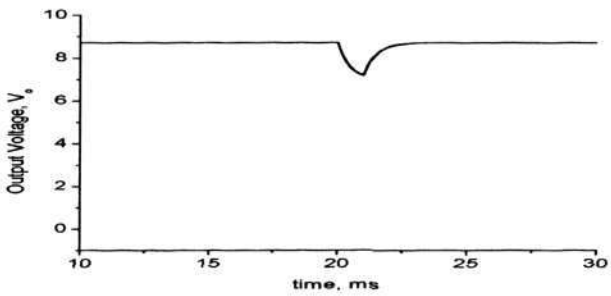
(a)



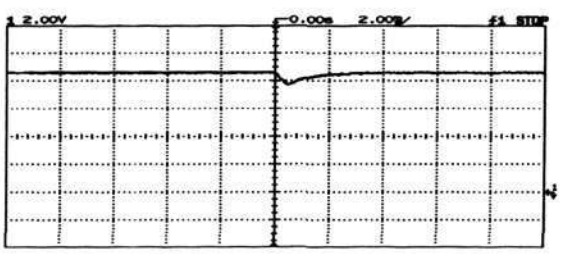
(b)

Fig. 7-17. Large-signal step response of the multi-state DCM boost converter

(a) Response curve described by the proposed model (7.38)
(b) Experimental curve



(a)



(b)

Fig. 7-18. Small-signal impulse response of the multi-state DCM boost converter

(a) Response curve described by the proposed model (7.39)
(b) Experimental curve

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Chapter 8 Conclusion and Recommendation

8.1 Conclusions

The thesis gives an in-depth research on advanced dc-dc power conversion topologies and mathematical analytical methods. In Chapter 1, the background of the research work is introduced firstly, and the basic concepts of dc-dc power conversion techniques are then reviewed. The detailed research work is given in Chapter 2-7, respectively.

In Chapter 2, to achieve positive output voltages with high voltage transfer gains in transformerless structures, a series of new switching topologies are proposed, which are termed ***positive output VL-type SEPIC converters***. The proposed topologies are based on the VL techniques and the SEPIC prototype, and they are different from any other existing dc-dc step-up converters. All circuits perform positive-to-positive dc-dc voltage increasing conversion with higher voltage transfer gains, small ripple and high efficiency in simple structures.

In Chapter 3, to achieve the negative output voltages with high voltage transfer gains in transformerless structures, a series of new switching topologies are proposed, which are termed ***negative output VL-type Cûk converters***. The proposed topologies are based on the VL techniques and the Cûk prototype, and they are different from any other existing dc-dc step-up converters. All circuits perform negative to positive dc-dc voltage increasing conversion with higher voltage transfer gains, small ripple and high efficiency in simple structures.

In Chapter 4, to achieve the mirror-symmetrical output positive and negative voltages with high voltage transfer gains in transformerless structures, a new topology is proposed, which is termed ***mirror-symmetrical double-output VL-type converter***. Additionally, the evolution of this topology results in ***the boost enhanced series*** and ***the super enhanced series***. All topologies are different from any other existing multiple output step-up

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converters. They perform positive to positive/negative dc-dc voltage increasing conversion with higher voltage transfer gains, small ripple and high efficiency in simple structures.

In Chapter 5, to achieve higher voltage transfer gains, the concept of evolution in the output section is introduced. The general guidelines **using *output enhanced circuits*** in the output section are presented and analyzed. They can be utilized in some positive output dc-dc converters. All derived topologies avoid adding accessorial active power switcher and transformers. The detailed topology construction guidelines are helpful for circuit design and engineering education.

In Chapter 6, to give a thorough analysis with consideration of effects caused by parasitic parameters and diodes' forward voltage drop, the ***developed switching signal flow graph method*** is proposed. The general guidelines of constructing and deriving graphical models are introduced. Furthermore, the ***averaging binary tree structure representation method*** of dc-dc converters is proposed, which paves a new way for graphical analysis of dc-dc converters.

In Chapter 7, to unify the analysis of complex and simple dc-dc topologies, the concepts and analytical methods based on ***the system energy characteristics*** are proposed. By investigating ***the remaining inductor current phenomena*** in DCM, a new explanation of DCM is proposed so that all discontinuous cases can be unified by the proposed concepts. Furthermore, a unified transient modelling method for various sorts of multi-state dc-dc converters from a viewpoint of their system energy characteristics is proposed. The proposed method ignores the complex switching state analysis and nonlinear characters in the inner circuit. It turns to system energy investigation of different steady states and tries to describe transient processes by 2^{nd} order transfer functions. Hence, the analytical difficulty is decreased significantly.

Following the theoretical analysis in Chapter 2 to 7, both simulation and experimental verification have been carried out. It can be seen that all the simulation results are identically matching the theoretical results. The reason is that we are using the ideal switching and passive component in the simulation. However, in the practical experimental circuits, the parasitic parameters affect the performance of the circuits.

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Nevertheless, the experimental results are quite close to the theoretical and simulation results.

All dc-dc topologies proposed in the thesis could be widely used in the areas of computer peripheral circuits, medical equipment, semiconductor industry, especially in applications that require high voltage transfer gains. They enrich the family of advanced dc-dc switching power converters and are helpful for the practical industrial applications and engineering education. The analytical methods proposed here provide a useful and convenient way for analyzing and utilizing these advanced dc-dc topologies.

8.2 Recommendation

All dc-dc topologies proposed in the thesis are circuit prototypes. The discussion in this thesis could explain main fundamental principles of these topologies. More research work needs to be performed in future, and it can be classified into the following parts:

- Protection circuits for complex dc-dc converters including various snubber circuits and soft switching techniques.
- Reliability theories of complex dc-dc converters.
- Control techniques based on the high-order models and low-order models.

All analytical methods and corresponding concepts proposed in this thesis are based on the averaging techniques, which ignore the nonlinear characteristics of switching circuits. The following research work could be classified into two parts:

- To relate the proposed analytical methods in this thesis with the nonlinear system theories.
- To develop a more convenient analytical method that could unify the CCM and DCM theories.

Above-mentioned contents should be considered for practical applications, and they will be carried out step by step in the future. The theoretical research and case study would be attractive in the areas such as electrical drive systems, new generation power sources applications and dc distributed power systems.

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Appendix

1. Time constant τ and damping time constant τ_d of multi-State CCM converters

Referring to Fig. 7-11, the preliminary work in [26] gave a theoretical analysis on the mathematical modelling of the multi-state dc-dc converter. It is based on the switching signal flow graph method, a typical conventional method developed from state-space averaging techniques. The small-signal transfer functions with power losses ($r_L \neq 0$) are tabulated in Table A.I for ready reference.

Table A.I Traditional small-signal transfer functions of multi-state CCM boost converter [26]

Small-Signal Transfer Functions		
$\frac{\hat{v}_o}{\hat{v}_{in}} = \frac{M_T}{\frac{LC}{D_2^2}s^2 + (\frac{r_L C}{D_2^2} + \frac{L}{RD_2^2})s + \frac{r_L}{RD_2^2} + 1}$	Where:	$M_T = \frac{D_1 + D_2}{D_2}$
$\frac{\hat{v}_o}{\hat{d}_1} = \frac{M_C}{\frac{LC}{D_2^2}s^2 + (\frac{r_L C}{D_2^2} + \frac{L}{RD_2^2})s + \frac{r_L}{RD_2^2} + 1}$	Where:	$M_C = \frac{V_{in}}{D_2}$
$\frac{\hat{v}_o}{\hat{i}_o} = \frac{M_o(1 + \frac{L}{r_L}s)}{\frac{LC}{D_2^2}s^2 + (\frac{r_L C}{D_2^2} + \frac{L}{RD_2^2})s + \frac{r_L}{RD_2^2} + 1}$	Where:	$M_o = \frac{r_L}{D_2^2}$
$\frac{\hat{i}_{in}}{\hat{v}_{in}} = \frac{M_i(1 + sCR)}{\frac{LC}{D_2^2}s^2 + (\frac{r_L C}{D_2^2} + \frac{L}{RD_2^2})s + \frac{r_L}{RD_2^2} + 1}$	Where:	$M_i = \frac{(D_1 + D_2)^2}{RD_2^2}$

Obviously, the models in Table A.I are relevant with each component. By mathematical transformation, they can be developed to the new expressions based on the system energy parameters as introduced in Section 7.3. The detailed deviation can start from the generalized transfer function $G(s)$, which can be written as follows:

$$G(s) = \frac{M \cdot \eta}{\frac{LC}{D_2^2}\eta s^2 + (\frac{rC}{D_2^2} + \frac{L}{RD_2^2})\eta s + 1} \tag{A.1}$$

where: $\eta = \frac{RD_2^2}{RD_2^2 + r_L}$ (A.2)

From the definition of (A.2), we can get the following equations, which will be used in the deviation process.

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$$r_L = \frac{1-\eta}{\eta} R D_2^2 \tag{A.3}$$

$$D_2^2 = \frac{\eta}{1-\eta} \frac{r_L}{R} \tag{A.4}$$

In addition, we get the output energy E_o and energy loss E_{loss} in a cycle using the system energy parameters.

$$E_o = \eta V_{in} I_{in} T = \eta \frac{W_L + W_C}{EF} \tag{A.5}$$

$$E_{loss} = (1-\eta) V_{in} I_{in} T = (1-\eta) \frac{W_L + W_C}{EF} \tag{A.6}$$

Firstly, according to the denominator of (A.1), τ can be written as:

$$\tau = \eta \left(\frac{r_L C}{D_2^2} + \frac{L}{R D_2^2} \right) \tag{A.7}$$

Substituting (A.3) and (A.4) to the (A.7), we can obtain:

$$\tau = (1-\eta) \left(\frac{2TW_C}{E_o} + \frac{2TW_L}{E_{loss}} \right) \tag{A.8}$$

Then substituting (A.5) and (A.6) to the (A.8), we can obtain τ expressed by the system energy parameters:

$$\tau = \frac{2T \cdot EF}{1+CIR} \left(1 + \frac{1-\eta}{\eta} \cdot CIR \right) \tag{A.9}$$

From the denominator of (A.1) and (A.9), we get:

$$\tau_d = \frac{\eta \frac{LC}{D_2^2}}{\tau} = \frac{(1-\eta) \frac{LI^2 \cdot CV^2}{r_L I^2 \cdot V^2 / R}}{\tau} = \frac{\frac{4T^2 \cdot EF^2 \cdot CIR}{\eta (1+CIR)^2}}{\tau} = \frac{2T \cdot EF}{1+CIR} \cdot \frac{CIR}{\eta + CIR(1-\eta)} \tag{A.10}$$

2. Time constant τ and damping time constant τ_d of multi-State DCM converters

The stored and transferred energy characteristics in each cycle determine whether a converter is in CCM or in DCM. τ and τ_d will be changed significantly once the converter is operated from CCM to DCM. The expressions of τ and τ_d derived from the boost converter in CCM (only two states) are applied into DCM, which can indicate the

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transient performance from a new point of view. The corresponding derivation procedures for τ and τ_d in CCM boost converter is the same with the buck converter discussed in [104-106]. Consequently, the expressions of τ and τ_d is same with (A.9) and (A.10).

Hence, the system model parameters of multi-state CCM and DCM converters can be unified to a generalized form based on the system energy parameters. The modelling and analysis on their transient performance can be carried out conveniently.

3. Critical value of ξ for a normalized 2nd order system

Consider the normalized 2nd order large-signal transfer function as shown in (7.25),

$$G(s) = \frac{M}{\xi\tau^2 s^2 + \tau s + 1} = \frac{M}{(s+s_1)(s+s_2)} \tag{A.11}$$

where: $s_{1,2} = \dfrac{-\tau \pm \sqrt{\tau^2 - 4\xi\tau^2}}{2\xi\tau^2}$ (A.12)

Let $\sqrt{\tau^2 - 4\xi\tau^2} = 0$ and the critical value of ξ in the time-domain is obtained as

$$\xi_t = 0.25 \tag{A.13}$$

Consider the normalized 2nd order small-signal transfer function as shown in (7.26),

$$|G(j\omega)| = \left|\frac{M}{\xi\tau^2 (j\omega)^2 + j\omega\tau + 1}\right| = \frac{M}{\sqrt{(1-\omega^2\tau^2\xi)^2 + \omega^2\tau^2}} \tag{A.14}$$

Then, take the following derivative

$$\frac{d}{d\omega}[(1-\omega^2\tau^2\xi)^2 + \omega^2\tau^2] = [2(1-\omega^2\tau^2\xi)(-2\omega\tau^2\xi) + 2\omega\tau^2] \tag{A.15}$$

Let (A.15) be equal to zero, we have:

$$[2\xi(1-\omega^2\tau^2\xi) - 1] = 0 \quad \Rightarrow \quad \omega = \sqrt{\frac{2\xi - 1}{2\xi^2\tau^2}} \geq 0$$

Therefore, the critical value of ξ in the frequency-domain is obtained as

$$\xi_f = 0.5 \tag{A.16}$$