

**A NOVEL HIGH-FIDELITY ANALOG
CLASS-D AMPLIFIER BASED ON SELF-
OSCILLATION FOR EARPHONES/HEADPHONES**

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Summary

The specifications of an earphone/headphone audio amplifier typically include high-fidelity (including Signal-to-Noise Ratio $\geq 90\text{dB}$, Total Harmonic Distortion + Noise $\geq 80\text{dB}$ and Power Supply Rejection Ratio $\geq 70\text{dB}$), in part due to the psychoacoustic effects of donning earphones/headphones and to the requirement of the single-ended output. Despite the power-efficiency (η) advantage of Class D amplifiers (CDAs) and their increasing acceptance in general audio applications, they remain largely unacceptable as earphone/headphone amplifiers because their fidelity are insufficient. Not unexpectedly, earphone/headphone amplifiers, at this juncture, are presently predominately Class AB amplifiers, and to the best of the author's knowledge, there is no reported commercial CDA appropriate for earphones/headphones (for mobile applications).

We propose the design of a novel single-ended output Class D earphone/headphone amplifier based on the complete-feedback self-oscillation architecture. The complete feedback approach is advantageous over conventional ('incomplete feedback') CDAs because the LC lowpass filter now constitutes part of the feedback loop, and the nonlinearities thereof are mitigated by $(\text{Loop Gain} + 1)$. The self-oscillation approach exploits the phase lag of the LC lowpass filter, thereby reducing the hardware complexity of the CDA. The novelty of the proposed design includes an integrator-cum-control block that provides high loop gain and a well-defined oscillation frequency. These attributes effectively mitigate the nonlinearities, including the high

nonlinearities at high modulation indexes of reported CDAs based on the same design architecture.

We further analytically derive the parameters pertinent to the proposed CDA to depict the mechanisms of and the pertinent parameters that affect the nonlinearities. This analytical work is useful as it provides insight to the design of the proposed CDA.

By means of simulations on the proposed design based on a commercial 0.35 μm CMOS process and physical measurements on the same CDA built with discrete components, we show that the proposed CDA meets the specifications required of earphone/headphone applications. We also show that its power-efficiency is significantly higher than its competing (commercial) Class AB amplifiers ($\eta_{\text{CDAmax}} = 90\%$ vs $\eta_{\text{ClassABmax}} = 65\%$), a very worthy advantage in portable audio applications. When benchmarked against reported CDAs for earphone/headphone applications, the proposed design is advantageous in terms of lower nonlinearity, lower cost (a cheaper inductor may be employed) and lower load variance. The shortcomings of the proposed design are the higher switching frequency, higher sensitivity to variations of the passive components and higher component count. These shortcomings are discussed and are not serious, particularly when viewed in terms of the merits of the proposed design.

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Chapter 1 Introduction

1.1 Motivation

Audio Class D amplifiers (CDAs) have become increasingly prevalent in the audio industry due to their high power-efficiency, typically >90% [1, 2] over a large range of modulation indexes (equivalent to signal swing and defined as $M = V_{out}/V_{DD}$ where V_{out} and V_{DD} are the output voltage and the supply voltage respectively). This high power-efficiency is largely obtained from the modus operandi of the output transistors in the output stage of CDAs. This modus operandi is akin to digital circuits, functioning only in the ohmic or cut-off regions, as opposed to the active region in classical linear amplifiers (Class A, Class B and Class AB). The high power-efficiency is a very worthy attribute as it translates to substantially longer battery lifespan. This is particularly advantageous in mobile applications where the energy capacity of the battery therein is limited. A low drain on the battery by the CDA is also highly desirable because the battery is also the power source for other functions, and users of mobile devices expect a long battery lifespan (between recharging).

It is interesting to note that despite the high power-efficiency advantage of CDAs, manufacturers of mobile devices remain hesitant to employ them as earphone/headphone amplifiers [3-5]; an earphone/headphone amplifier is a low power (usually up to $\leq 100\text{mW}$) audio amplifier driving an earphone/headphone load (typically 16Ω or 32Ω) [6, 7]. This is largely because the fidelity of the CDAs is typically lower (e.g., SNR is $\sim 20\text{dB}$ lower) [5, 8] than their linear amplifiers counterparts (Class AB or Class G amplifiers) in low power earphone/headphone applications, especially with the single-

ended output stage topology (imposed by 3-pin earphone/headphone connector (TRS, Tip (Left audio channel), Ring (Right audio channel) and Sleeve (Ground); or 4-pin TRRS, Tip (Left audio channel), Ring (Right audio channel), Ring (Microphone) and Sleeve (Ground)), see Section 2.3 later). The ‘poorer’ fidelity is arguably somewhat a misnomer for earphone/headphone applications in part because from a psychoacoustical viewpoint, the masking effect from the external environmental background noise is lower than that perceived when external loudspeakers are used, thereby accentuating the effect of perceived nonlinearities. In other words, the noise from the earphone/headphone appears to be more ‘perceptually apparent’ to a user who dons a pair of earphones/headphones than that of listening from an external loudspeaker (not placed near the pinna of the user). Put simply, for the same perceived fidelity, the fidelity demands of an earphone/headphone amplifier are typically higher than that of a regular audio amplifier.

A high-fidelity linear earphone/headphone amplifier is typically qualified by a number of parameters and three parameters are typically quoted/specified: high Signal-to-Noise Ratio (SNR), $\text{SNR} \geq 90\text{dB}$, low Total Harmonic Distortion+Noise (THD+N), $\text{THD+N} \leq 0.01\%$ (or $\geq 80\text{dB}$), and high Power Supply Rejection Ratio (PSRR), $\text{PSRR} \geq 70\text{dB}$ [9-12]. In view of the psychoacoustics associated with earphones/headphones, the parameters of the CDA would need to be at least equal these parameters to be acceptable, yet with substantially higher power-efficiency, η (e.g., $\eta_{\text{max}} \geq 90\%$ for CDAs vis-à-vis $\eta_{\text{max}} \approx 65\%$ for linear Class AB amplifiers).

The most effective and universally acceptable technique to mitigate the nonlinearities is to apply negative feedback. Figure 1.1 depicts a conventional CDA with negative feedback driving an earphone/headphone load. The conventional CDA comprises a modulator, an output stage, an LC lowpass filter and a feedback network.

The modulator (see Section 2.2 later), embodying a loop filter and a comparator, modulates the audio input signal to a train of pulses (typically Pulse-Width-Modulated (PWM) [1]) at carrier frequency (the carrier is either externally or internally generated).

The output stage [1] consists of a chain of inverters (which buffers the pulse signals and the final inverters having sufficient power to drive an earphone/headphone load) and control circuits (including protection circuits). In Figure 1.1, the earphone/headphone amplifier output stage is configured as a single-ended topology (the earphone/headphone load R_L terminals are connected between the amplifier output and ground) as opposed to the more prevalent Bridge-Tied-Load (BTL) topology (where the load R_L terminals are connected to two single-ended outputs of the same amplifier, one being 180° out of phase of the other (see Section 2.3 later)). The BTL topology is advantageous in low power audio applications because the output power is increased by four times compared to the single-ended output, and some noise is cancelled to the first order [13]. However, because the earphone/headphone connector is either the 3-pin TRS or 4-pin TRRS connector where the left and right channels share a common ground, the left channel and the right channel amplifiers of a portable device would need to be

single-ended. Consequently, in addition to the ‘added’ fidelity requirement due to psychoacoustical effect of donning earphones/headphones, the earphone/headphone amplifiers would suffer the drawbacks of reduced output power (for the same M) and higher noise due to their single-ended output.

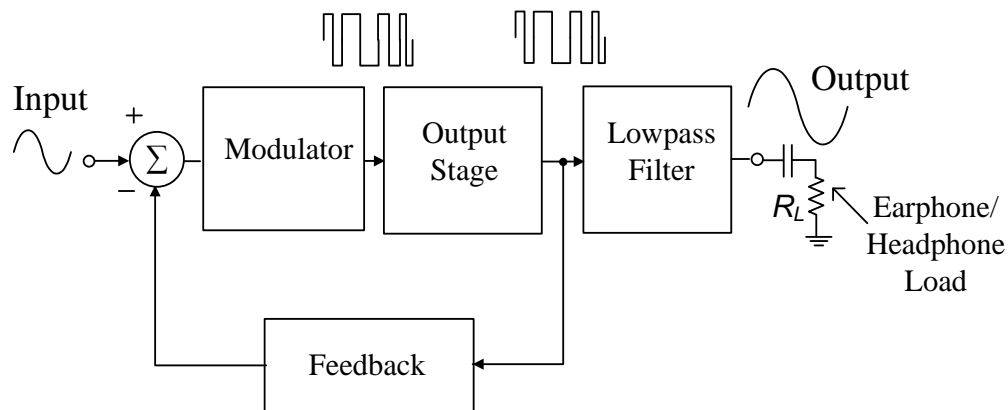


Figure 1.1 Block diagram of a conventional CDA with a single-ended output stage driving an earphone/headphone load

The LC lowpass filter in Figure 1.1 is usually employed to attenuate the high frequency carrier to retrieve the audio band analog signal from the pulse trains output. The input of the feedback network is sampled at the output of the output stage. As the modulator and the output stage blocks are within the feedback loop, their nonlinearities would be reduced by a factor of (Loop Gain+1) due to feedback mechanism. However, as the LC lowpass filter is not a constituent part of the feedback loop, nonlinearities arising therefrom remain unattenuated.

The nonlinearities arising from the LC lowpass filter can be unacceptably large, for example, up to 1% [14, 15], leading to a THD $>0.1\%$ ($\leq 60\text{dB}$).

The mechanism for the nonlinearities is largely due to the non-linear inductor which has imperfect core material (typically an iron core) or imperfect winding; practical capacitors are relatively linear.

In view of the required fidelity of CDAs for earphones/headphones and in view of the psychoacoustical aspect thereto, the nonlinearities arising from the *LC* lowpass filter would need to be addressed (before CDAs can be accepted as earphone/headphone amplifiers).

A reported approach to address the *LC* lowpass filter nonlinearities is to adopt the ‘filterless’ CDA approach [16, 17] where the *LC* filter is not required. Other than the advantage of no nonlinearity from the *LC* filter, the added advantages are the cost saving arising from the absence of the *LC* filter (~10% reduced cost) and the reduction of form factor on the Printed Circuit Board (30% - 70% smaller area) [18].

Unfortunately, the ‘filterless’ CDA has serious shortcomings rendering them inapplicable to earphone/headphone applications. First, the ‘filterless’ CDA has high frequency components (at the carrier frequency) at the output of the output stage and at the input of the load. Second, the ‘filterless’ CDA relies on a highly inductive load (highly inductive loudspeakers are typically expensive, unlike general purpose earphones/headphones and speakers) to effectively attenuate the high switching frequency. The high frequency components result in higher switching noise and ultimately higher Electro-Magnetic Interference (EMI), and they may interfere with radio frequency

functions such as communications receivers in mobile phone, GPS or FM radio in mobile devices [19]. In addition, the long wire from the ‘filterless’ CDA output to the earphone/headphone load increases the probability of transmitting high frequency components and thus higher EMI. In general, these shortcomings are sufficiently severe such that filterless CDAs are not considered appropriate for mobile applications, rendering the conventional (‘filtered’) CDA as the preferred choice, despite the nonlinearities introduced by the *LC* filter.

To mitigate the nonlinearities from the *LC* lowpass filter, the most obvious technique is to embody the *LC* lowpass filter within the feedback loop, i.e. sampling the output of the *LC* filter (as opposed to the output of the output stage in Figure 1.1) as the input of feedback network. We denote this as ‘complete feedback’ in this dissertation [20, 21] and the conventional CDA (Figure 1) as ‘incomplete feedback’.

Figure 1.2 depicts the CDA with ‘complete feedback’ and with ‘incomplete feedback’ (dashed line). There are several advantages to employ the complete feedback. First, as the *LC* filter now constitutes part of the feedback loop, the nonlinearities thereof are now mitigated as that of the nonlinearities of the modulator and output stage. Second, there is increased output control and immunity to load variations because there is now more constant impedance from the feedback network (in parallel with the load impedance). Third, as the nonlinearities of the *LC* filter could be reduced by $(\text{Loop Gain}+1)$,

there is the possibility of employing a lower quality inductor (see Section 2.3 later) yet retaining sufficient fidelity, thereby the opportunity for reduced cost.

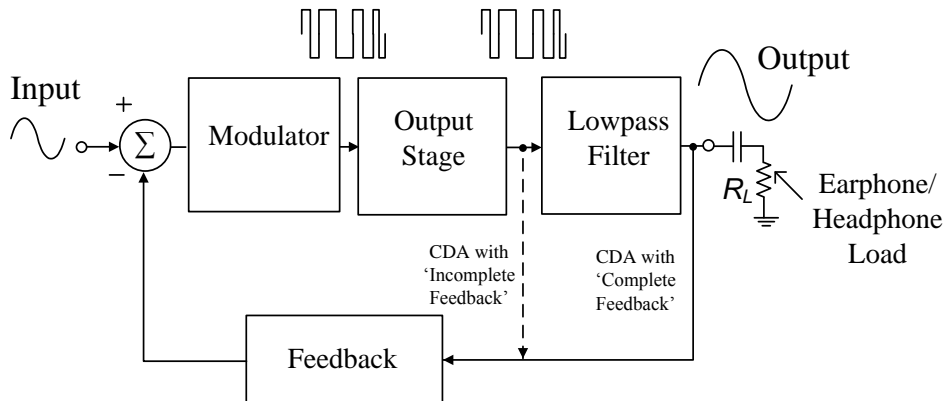


Figure 1.2 Block diagram of the CDA with ‘Complete Feedback’

From a simplistic perspective, the inclusion of the LC filter as a constituent part of the feedback loop seems somewhat obvious and/or trivial. However, due to the excessive phase lag (180°) arising from the LC lowpass filter, the implementation of the complete feedback in the conventional PWM CDA is difficult due to stability. Specifically, in virtually all amplifiers, stability must be assured – typically $>45^\circ$ phase margin, or $>10\text{dB}$ gain margin, and this likewise applies to CDAs with incomplete and complete feedback.

In the complete feedback PWM CDA, the 2nd-order LC lowpass filter contributes $\sim 180^\circ$ phase lag and this excessive phase lag may cause the total phase lag (in addition to negative feedback) in the circuit to be $> 360^\circ$, thereby rendering the CDA unstable. This phase lag would hence need to be circumvented – noting that the loop filter itself has phase lag; this loop filter typically has gain - needed to improve the loop gain, see Section 2.2 later. To

compensate for the phase lag to maintain sufficient phase margin [22] introduced by the *LC* lowpass filter, a complicated hardware-intensive phase compensation circuit is required. Put simply, the conventional CDA with complete feedback is not only difficult to design and not operationally robust, it is largely inappropriate for cost-sensitive consumer electronics.

To circumvent the limitations of the conventional CDA with compensation, the self-oscillating approach [21, 23-25] is arguably more advantageous. First, the self-oscillating approach relaxes the design constraint, thereby simplifying the design complexity. This is because the self-oscillating approach does not require an additional phase compensation circuit to maintain stability – the self-oscillating CDAs, conversely, operate as an oscillator, a positive feedback system. The phase lag introduced by a 2nd-order *LC* lowpass filter is now useful as its phase lag constitutes part of the total phase lag required for positive feedback - it contributes to the oscillation of the CDA and hence the phase lag due to the *LC* lowpass filter need not be compensated. Second, the self-oscillating approach generates the carrier internally as opposed to the PWM approach where the carrier is typically externally generated. This hence reduces the hardware and power consumption arising from the external carrier generator. Third, the self-oscillating approach intrinsically provides higher loop gain (at least 3-4dB) [26] (compared to the conventional PWM approach) to mitigate the nonlinearities and noise, thereby providing higher fidelity [21]. Ideally, the PSRR of the self-oscillating approach at DC is infinite. However, practically, due to mismatch and other practical limitations, its PSRR is not infinite but a high PSRR (>60dB) is easily achieved, rendering

this approach very robust towards perturbations such as 217Hz burst noise in the supply rail of GSM mobile phones [27].

At this juncture, there are only a few reported designs of analog CDAs embodying the self-oscillating approach for general high-fidelity audio applications [21] [28] and interestingly, to the author's knowledge, yet to be employed/reported for low-power earphone/headphone applications; there is however a reported CDA with incomplete feedback [27]. As delineated earlier, low-power earphone/headphone amplifiers today are dominated by linear amplifiers; note that conventional 'filtered' CDAs with incomplete feedback are also not generally accepted for high-fidelity low-power earphone/headphone applications.

In order to design a CDA embodying the self-oscillating approach, two important considerations would need to be addressed. First, the complete feedback embodying the self-oscillating approach generally suffers from relatively high nonlinearities at high modulation indexes [29] [30], thereby generally unacceptable for high-fidelity audio applications. This shortcoming is also unacceptable because the power-efficiency of the CDA (as in an audio amplifier) is highest at high modulation indexes, thereby somewhat defeating the advantages of a CDA if operation in high modulation indexes were to be avoided. In the intended application, the effect of this nonlinearity is exacerbated due to the psychoacoustical effect and 3-pin TRS (or 4-pin TRRS) connector limitation (single-ended output) delineated earlier. Second, the self-oscillating approach generates the switching frequency internally by the

entire circuit as opposed to the PWM where the switching frequency is externally applied. As the switching frequency is dependent on the phase lag from each block, it is important to properly design each block in the CDA to avoid undesirable switching frequencies which may adversely affect the functionality of the CDA (for example, excessively high frequencies that would in turn reduce the power-efficiency) and hence the performance of the design.

In summary, in view of the high power-efficiency attributes of the CDAs for earphone/headphone amplifiers in mobile applications, it is of interest to investigate the potential of CDAs, particularly CDAs embodying the complete feedback approach and with a single-ended output, to achieve high-fidelity (throughout the full range of modulation indexes) that could be comparable to the linear amplifiers (yet higher power efficiency).

1.2 Objectives

In view of the aforesaid motivations, the overall objective of this Master of Engineering research program is to design an analog CDA with complete feedback based on self-oscillating approach for earphone/headphone applications.

The specific objective is the design of the aforesaid analog CDA that embodies:

- (i) Complete feedback topology, where the LC filter constitutes part of the feedback loop, thereby potentially higher fidelity as the nonlinearities of the LC filter are reduced by $(\text{Loop Gain}+1)$ due to the negative feedback mechanism, and cost-effective due to the possibility of employment of a low cost (high nonlinearity) inductor;
- (ii) The self-oscillating approach, thereby not requiring an externally generated carrier generator and a complicated phase compensation circuit (to maintain the stability due to the phase lag of the LC lowpass filter), hence hardware simplicity;
- (iii) Single-ended output to enable its application as a (low-power) earphone/headphone amplifier, as constrained by the TRS or TRRS connection;
- (iv) Sufficient loop gain (see Section 2.2) in the loop filter to achieve fidelity comparable to the linear amplifiers for earphone/headphone applications:
 - (a) $\text{SNR} \geq 90\text{dB}$,
 - (b) $\text{THD+N} \leq 0.01\%$, and
 - (c) $\text{PSRR} \geq 70\text{dB}$; and
- (v) High power-efficiency, $\eta > 90\%$ at $M = 0.9$.

In summary, the objective is to design a low-power power-efficient low-nonlinearity analog CDA for earphones/headphones, whose specifications are tabulated in Table 1.1 below.

Table 1.1 Specifications of the CDA

Parameter	Value
Supply Voltage, V_{DD}	5V
Maximum Modulation index, M_{max}	0.9
Load	32 Ω
SNR	≥ 90 dB
THD+N	$\leq 0.01\%$
PSRR	≥ 70 dB
Power-Efficiency	$\geq 90\%$ @ M_{max}
Audio Bandwidth	20 Hz - 20 kHz
Switching Frequency	≤ 1 MHz
Maximum Rated Power	80mW

1.3 Contributions

The contributions of the Master of Engineering research program pertain to the objectives outlined above. Specifically, they are:

- (i) A high-fidelity single-ended output CDA embodying the complete feedback architecture and based on self-oscillating approach is proposed. The proposed design features high loop gain and well controlled switching frequency (≤ 1 MHz). A novel integrator-cum-control block proposed in the modulator of the proposed CDA includes a 2nd-order lossy integrator that features high loop gain (200 dB at DC) to further attenuate the nonlinearities of the blocks (the modulator, the

output stage and the *LC* lowpass filter in the feedback loop) and to suppress the noise across the entire audio frequency range (20 Hz-20 kHz).

- (ii) The suppression of nonlinearities is sufficient such that at high modulation indexes, the fidelity of the proposed CDA exceeds/meets the requirements of the earphone/headphone amplifiers, e.g. $\text{THD+N@M=0.9} \leq 0.01\%$. From a manufacturing perspective, the high nonlinearities suppression provides the potential of lower cost as a lower quality (higher nonlinearity) inductor may be employed.
- (iii) The control block is designed with lead-lag phase characteristics to compensate for the intrinsic delay of the circuit and tuned to establish the desired switching frequency.
- (iv) Further to (i), analytical work is performed to model the functionality of the blocks of the proposed CDA to depict the pertinent parameters of the design that affect the fidelity (loop gain of the comparator and switching frequency). This analytical work provides meaningful insight to the design of the proposed CDA.
- (v) On the basis of HSPICE simulations and hardware measurements of the proposed CDA, the proposed CDA is verified to meet the specifications of a low-power high-fidelity audio amplifier for earphones/headphones: $\text{SNR} > 95 \text{ dB}$, $\text{THD+N} \leq 0.01\%$ and PSRR

≥ 70 dB. These parameters are comparable to the state-of-the-art linear amplifiers and yet substantially more power-efficient, for example, $\eta = 90\%$ at maximum modulation index (vis-á-vis $\eta \approx 65\%$ for a class AB amplifier at the same signal swing). In addition, PS-IMD, a parameter that is pertinent to fidelity (although seldom quoted for CDAs) is characterized at $f_n = 217$ Hz (with amplitude 250mV_{pp}) and $f_{in} = 1$ kHz ($M = 0.9$); the PS-IMD $\approx 98\text{dB}$, is high. The IMD of the proposed CDA is also characterized and is low (IMD $< 0.5\%$) over the entire range of modulation indexes.

- (vi) As in many engineering solutions, improving certain parameters of a given design typically involves compromises to other parameters of said design. In the proposed design, the high-fidelity is achieved with three compromises which are slightly disadvantageous and are not dilapidating. Specifically, the compromises are the higher switching frequency, possibly higher sensitivity to components variations and higher component count compared to the more conventional PWM CDAs. These shortcomings, nevertheless, applies to all CDAs based on the self-oscillation architecture and in this sense, the proposed CDA is not disadvantaged.

1.4 Organization of the Dissertation

The remainder of this dissertation is organized as follows:

In Chapter 2, the literature pertaining to high-fidelity earphone/headphone amplifier designs is presented. First, an overview of analog audio amplifiers is presented. The specifications, including the power-efficiency and the fidelity parameters, are described and the output stage topologies are delineated. Second, the classifications of the audio amplifiers - classical linear amplifiers (Class A, Class B and Class AB amplifiers), non-conventional Class G amplifiers and switching CDAs - are presented. The differences between linear and switching amplifiers, in particular the power-efficiency advantage of the latter, are presented. Following this, a comprehensive review of analog CDA modulations with incomplete and complete feedback is presented.

In Chapter 3, the system level design considerations of the proposed high-fidelity CDA design, including that for the modulator, output stage and lowpass filter, are presented. Analytical expressions for the design (the loop gain of the comparator) have also been derived, providing useful insight into the design. Furthermore, the proposed design is verified on the basis of simulations and physical measurements. The results of the proposed CDA in terms of SNR, THD+N, PSRR, PS-IMD, IMD and power efficiency are presented. The merits and shortcomings of the proposed CDA are identified.

Chapter 4 concludes this dissertation and suggests the recommendation for the future works.

Chapter 2 Literature Review

2.1 Introduction

This chapter reviews the literature pertaining to high-fidelity earphone/headphone amplifier designs. This literature review is arranged in the following fashion. First, an overview of analog audio amplifiers is presented. The specifications, including the power-efficiency and the fidelity parameters, are described and the output stage topologies are delineated. Second, the classifications of the audio amplifiers - classical linear amplifiers (Class A, Class B and Class AB amplifiers), non-conventional Class G amplifiers and switching CDAs - are presented. The differences between linear and switching amplifiers, in particular the power-efficiency advantage of the latter, are presented. Following this, a comprehensive review of analog CDA modulations with incomplete and complete feedback is presented.

2.2 Overview of Audio Amplifiers

An audio power amplifier [31, 32] serves to amplify an electronic audio input signal (typically 20 Hz-20 kHz) and provides power drive to an audio load, e.g. a loudspeaker or an earphone/headphone. The audio power amplifier is typically placed at the final stage of the audio system.

The typical audio system, comprising a transducer microphone, a pre-amplifier, an Analog-to-Digital Converter (ADC), a Digital Signal Processor (DSP), a Digital-to-Analog Converter (DAC), an analog power amplifier and a transducer load, is depicted in Figure 2.1. The microphone is a transducer which converts an acoustical signal to an electronic (voltage) signal. The

preamplifier amplifies the low-level electronic output of the microphone. The ADC subsequently converts the pre-amplified microphone signal to the digital signal that is to be processed by a DSP. The DAC converts the processed digital output from the DSP to the analog signal. The analog power amplifier finally amplifies the analog signal from DAC to the load.

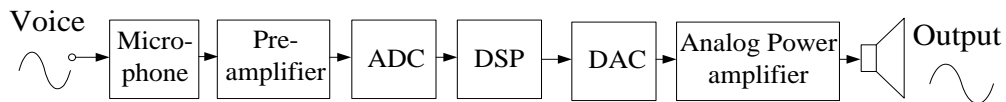


Figure 2.1 Block diagram of a general audio system with an analog power amplifier

Analog audio power amplifiers can be found in a myriad of audio applications [33] including micropower hearing aids, low-power earphone/headphone amplifiers, mid-power home entertainment systems, automotive audio, high-power public address sound systems, etc. The selection of the audio power amplifier is typically based on a number of parameters, including output power requirement. For low-power audio applications such as earphones/headphones, the output power is typically $\leq 100\text{mW}$.

2.2.1 Specifications

The general performance of an analog audio power amplifier is specified by two main parameters – power efficiency and fidelity. Power efficiency is defined as the ratio of the useful power (the power consumed by the load) to the total power drawn from the (DC) power supply. In general, a high power-

efficient audio amplifier is desirable because it leads to lower power dissipation.

Fidelity, on the other hand, often refers to the preciseness (or linearity) of the audio amplification process. In general, a high-fidelity audio amplifier is attractive because its distortion is low and the linearity high – ‘high’ quality output. However, high power-efficiency and high-fidelity are often opposing attributes where many contemporary high-fidelity amplifiers are not power-efficient. For example, very high-fidelity (Class A) amplifiers are typically <10% power-efficient.

2.2.1.1 Power Efficiency

The power-efficiency, η , is defined as

$$\eta = \frac{P_{load}}{P_{load} + P_{dissp}} \times 100\% . \quad (2-1)$$

where P_{load} is the power consumed by the load, and

P_{dissp} is the power dissipated by the amplifier.

The total power consumed by the load is

$$P_{load} = \frac{V_{opp}^2}{8R} . \quad (2-2)$$

where P_{load} is the power consumed by the load,

V_{opp} is the peak-to-peak output voltage, and

R is the load resistance.

2.2.1.2 Fidelity Parameters

The fidelity is qualified by a number of parameters and Table 2.1 tabulates these parameters. Of these parameters, the three primary fidelity parameters typically quoted are: Signal-to-Noise Ratio (SNR), Total Harmonic Distortion+Noise (THD+N) and Power Supply Noise (quantified by Power Supply Rejection Ratio, PSRR) and; sometimes THD rather than THD+N is quoted but the latter is more precise (see below).

Table 2.1 The list of fidelity parameters

	Name
1	Signal-to-Noise Ratio (SNR)
2	Total Harmonic Distortion +Noise (THD+N)
3	Power Supply Rejection Ratio (PSRR)
4	Power Supply-induced Intermodulation Distortion (PS-IMD)
5	Intermodulation Distortion (IMD)
6	Foldback Distortion (FBD)

SNR is a measurement of the maximum output signal voltage relative the floor noise level at zero-input, usually expressed in decibels (dB) [34]. The noise level is calculated in the specified bandwidth (20Hz - 20 kHz in audio amplifier). Analytically, SNR is

$$\text{SNR} = 20 \log \frac{V_{\max}}{V_n} . \quad (2-3)$$

where V_{\max} is the maximum output signal voltage, and

V_n is the root-mean-square floor noise voltage.

THD [35] is a classical measure of fidelity, and is defined as

$$\% \text{THD} = \frac{\sqrt{V_{o@2f_o}^2 + V_{o@3f_o}^2 + V_{o@4f_o}^2 + \dots}}{V_{o@f_o}} \times 100\% . \quad (2-4)$$

where $V_{o@f_o}$ is the output component at fundamental frequency, f_o , and $V_{o@2f_o}$, $V_{o@3f_o}$ and $V_{o@4f_o}$ are the output harmonic components at harmonic frequencies, $2f_o$, $3f_o$ and $4f_o$ respectively.

In many cases, the noise floor is considered within the THD parameter and this is a more precise definition of THD, more correctly defined as THD+N, where N refers to noise floor.

PSRR is a very important parameter in the mobile applications because power supply noise may be introduced from the DC-DC conversion process. Further, in the case of cellular phones, significant 217Hz GSM burst noise is also introduced to the power supply[27]. The analytical definition of PSRR is

$$\text{PSRR} = 20 \log \frac{V_{n_out@f_n}}{V_{n_in@f_n}} . \quad (2-5)$$

where $V_{n_in@f_n}$ is the amplitude of the ripple noise signal appearing at the power supply, and $V_{n_out@f_n}$ is the amplitude of the ripple noise signal appearing at the output of the amplifier.

In general, the low power earphone/headphone amplifiers require high-fidelity (SNR \geq 90dB, THD+N \leq 0.01% and PSRR \geq 70dB).

Other fidelity parameters for audio amplifier include PS-IMD, IMD and FBD. Note that in headphone/earphone amplifiers, the other fidelity parameters are not generally quoted in the earphone/headphone amplifier datasheet. For completeness, the parameters will also be reviewed.

PS-IMD [36] is proposed by our research group, and is referring to the nonlinearities arising from the intermodulation between the power supply noise and the input signal. The 2nd-order PS-IMD refers to the PS-IMD whose components are at the input signal frequency plus/minus the supply noise frequency. The higher-order PS-IMD refers to PS-IMD whose components are at the input signal frequency plus/minus the multiple-integers of the supply noise frequency.

IMD [37] is another well accepted measure of fidelity, and arises from the intermodulation between two or more frequency components of the input signal. Two slightly different definitions for IMD are commonly used, one defined by the Society of Motion Picture and Television Engineers (SMPTE) and the other known as the twin-tone IMD. The SMPTE and twin-tone IMDs are defined as

$$\% \text{IMD} = \frac{\sqrt{[V_{out}(mf_1 + nf_2) + V_{out}(mf_1 - nf_2)]^2 + \dots}}{V_{out}(f_2)} \times 100\% . \quad (2-6)$$

where $m, n = 1, 2, 3, \dots$,

in the case of the SMTPE IMD, the output voltages $V_o(f_1) = 4V_o(f_2)$ at input frequencies $f_1=60\text{Hz}$ and $f_2=7\text{kHz}$, and

in the case of the twin-tone IMD, output voltages $V_o(f_1) = V_o(f_2)$ at high input frequencies (typically $f_1, f_2 > 10\text{kHz}$).

IMD is often considered an equally pertinent parameter to THD. The IMD in commercial Class-D amplifiers can be high, for example 1% [37] and is usually undisclosed. The dominant mechanism for this high IMD is largely attributed to the nonlinear iron/ferrite core inductor L and capacitor C of the LC lowpass filter.

Similar to THD, IMD can be suppressed by means of negative feedback. To suppress the dominant IMD due to the LC lowpass filter, the input of the negative feedback is taken at the output of the lowpass filter [14, 22] (instead of the output of the output stage). This approach however substantially increases the complexity of CDAs. Another approach is to remove the LC lowpass filter, and subsequently realizing a filterless CDA. In this latter approach, the IMD due to the LC lowpass filter is completely removed.

FBD [38, 39] is a distortion (whose components are within the frequency band of interest) arising from the intermodulation between the carrier and other signals. At this juncture, the FBD in CDAs is not well understood, remains unreported and the mechanisms thereof are unknown. According to our

research group [40], FBD is less significant in the amplifier with higher carrier frequency (>250 kHz).

Of these nonlinearities, the PS-IMD and the PS-FBD are specific to CDAs (they are absent in linear amplifiers). FBD is a nonlinearity unique to switching amplifiers such as CDAs and is absent in other audio amplifiers that do not embody a carrier. These nonlinearities are required to be sufficient low to be acceptable in the high-fidelity earphone/headphone amplifiers.

As delineated in Chapter 1, the earphone/headphone amplifiers require special output stage topologies (single-ended output) to be compatible with the 3-pin TRS and 4-pin TRRS connector.

Next, the two types of output topologies will be delineated in turn.

2.2.3 Output Stage Topologies

The output stage is the final stage of a power amplifier. It serves to provide (power) driving functionality and to deliver the power (current) to the load. The topology of the output stage is important for the appropriate load connection for a given application.

There are two types of output stage topologies for general audio amplifiers - single-ended topology and Bridge Tied Load (BTL) topology [1, 41].

The single-ended topology is depicted in Figure 2.2(a) where the load terminals are connected to the amplifier output and to ground. As the signal swing of the amplifier is between voltage supply and ground, a (ac coupling) capacitor (C_o) is usually placed between the output stage and the load. This prevents a DC current from flowing into the load which otherwise damages the transducer load. As audio frequencies are relatively low (< 20 kHz), the ac coupling capacitor (C_o) is usually large ($100\mu\text{F}$ - $1000\mu\text{F}$).

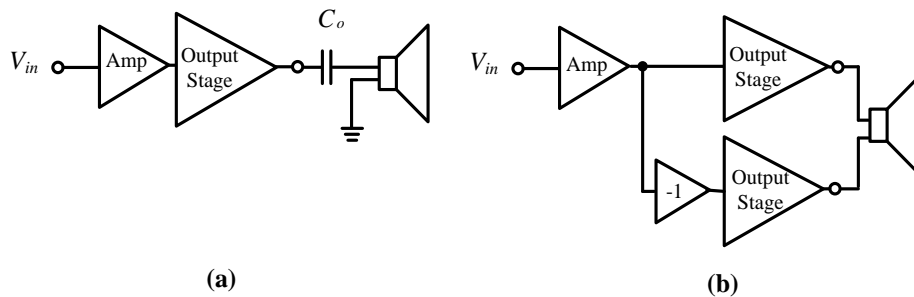


Figure 2.2 (a) Single-ended topology and (b) BTL topology

The BTL topology is depicted in Figure 2.2(b) where the load terminals are connected to two single-ended outputs of the same amplifier, each being 180° out of phase. Compared to the single-ended topology, the advantages of the BTL are that the signal swing is doubled (the power is hence four times higher) and the ac coupling capacitor is unnecessary. Besides, this topology, in general, provides better noise performance because the common noise from the two amplifiers is to a first-order cancelled at the load. These advantages are obtained at the expense of increased hardware due to the two output stages.

In summary, the BTL is advantageous in general audio applications due to higher power and better fidelity performance. However, in the low power

earphone/headphone amplifiers, the 3-pin connector (TRS or 4-pin TRRS) requires a common ground between the left and right channel of the audio device, thereby demanding the application of the single-ended topology.

2.3 Analog Audio Amplifier Classification

Analog audio amplifiers are generally classified as either linear amplifiers (e.g. Class A, Class B, and Class AB amplifiers) or switching amplifiers (e.g. CDAs). The linear amplifier ideally outputs an amplified replica of its input signal, and this process is achieved by the linear operation of its output transistors (in the active region). The conventional linear amplifiers include Class A, Class B and Class AB; the ‘non-conventional’ Class G amplifiers are a derivative of the Class AB linear amplifier. On the other hand, the switching amplifiers, CDAs, have their output transistors functioning as switches and operating in ohmic or cut-off regions.

2.3.1 Conventional Linear Amplifiers

Linear amplifiers have been prevalent for decades. The primary reasons for their ubiquity are hardware simplicity and high-fidelity (with the exception of Class B amplifiers due to severe crossover distortion, see later), for example, many commercial Class A and Class AB amplifiers routinely achieve $\leq 0.01\%$ THD. For earphone/headphone applications, Class AB amplifiers (and Class G, see later) are dominant due to their high-fidelity and relatively higher power-efficiency (compared to Class A amplifiers).

The main drawback of linear amplifiers is low power-efficiency (compared to switching CDAs), for example, the theoretical maximum power-efficiency of a Class A amplifier with a single-ended output is as low as 25%. This drawback often leads to the requirement for heat sinks (large form-factor in practical mid-high power realizations) to safely dissipate the heat, and in the case of portable instruments, reduced battery lifespan.

2.3.1.1 Class A Amplifiers

The output stage of a single-ended Class A amplifier [42] driving a loudspeaker load is depicted in Figure 2.3(a). It consists of a power transistor (emitter follower Q_1) and a biasing transistor Q_2 . Q_2 provides a constant DC current I_B to bias Q_1 in the active region. As Q_1 is biased in the active region, Q_1 operating in the linear region will deliver power to the load. Figure 2.3(b) depicts the output current from Q_1 which conducts for the entire signal cycle. In other words, Q_1 , the power transistor of the Class A amplifier, conducts over the entire cycle - the conduction angle is 360° . Consequently, the distortion is typically low (THD $\leq 0.01\%$).

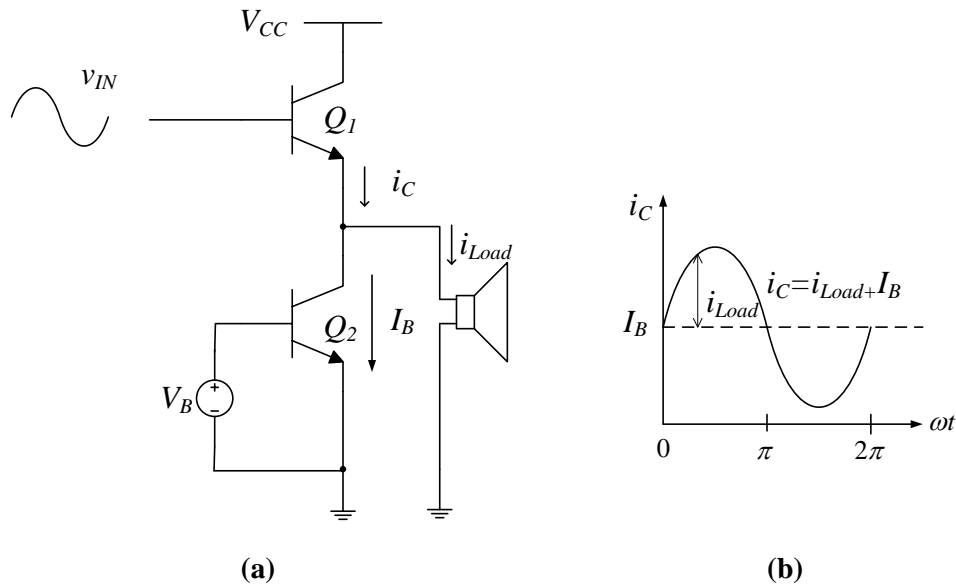


Figure 2.3 (a) Class A output stage, and (b) Class A output current waveform

The drawback of the Class A amplifier nevertheless is the high power dissipation due to the constant biasing current, resulting in very low power-efficiency. For single-ended Class A amplifiers, the maximum efficiency is a paltry 25%, thereby unacceptable in many present-day audio applications.

2.3.1.2 Class B Amplifiers

The output stage of a single-ended push-pull Class B amplifier [42] is depicted in Figure 2.4(a). It consists of two power transistors, Q_1 and Q_2 , each delivering power to the load for approximately half a cycle. Figure 2.4(b) shows the output current waveform for Q_1 , i_{CQ1} , and for Q_2 , i_{CQ2} . Unlike the Class A amplifier, there is no biasing current so there is less power dissipation and the maximum theoretical power-efficiency could reach 78.5% which is much higher than that of Class A amplifiers. However, to be operational, the

input must be larger than the turn-on voltage of the transistor ($\sim 0.7V$ for silicon process) to allow the linear operation of the transistor. When the input voltage is not sufficient to turn on the transistors, a dead zone where both transistors, Q_1 and Q_2 , are off and the Class B amplifier not operating is formed. The resulting dead zone contributes to crossover distortion, which is a severe and often unacceptable problem in high-fidelity audio amplifiers.

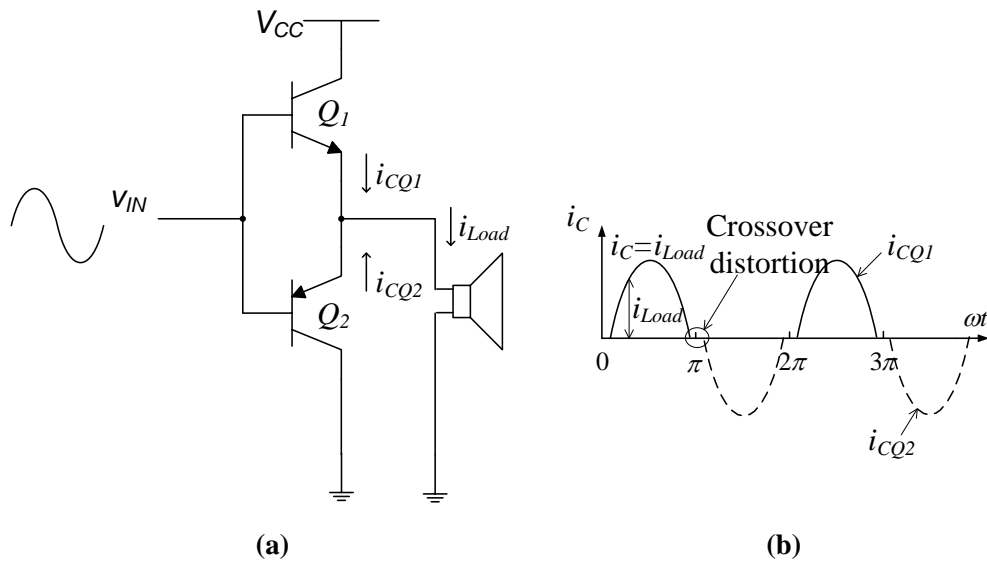


Figure 2.4 (a) Class B output stage, and (b) Class B output current waveform

2.3.1.3 Class AB Amplifiers

The output stage of a single-ended Class AB amplifier [43] is depicted in Figure 2.5(a). This amplifier is formed when a biasing circuit is added to the Class B amplifier to provide a means to eliminate the severe crossover distortion thereof. The biasing circuit ensures that at least one of the output transistors is active in the dead zone. In this fashion, the fidelity of the Class

AB is substantially superior to the Class B amplifier, and if appropriately design, its fidelity approaches that of the Class A amplifier.

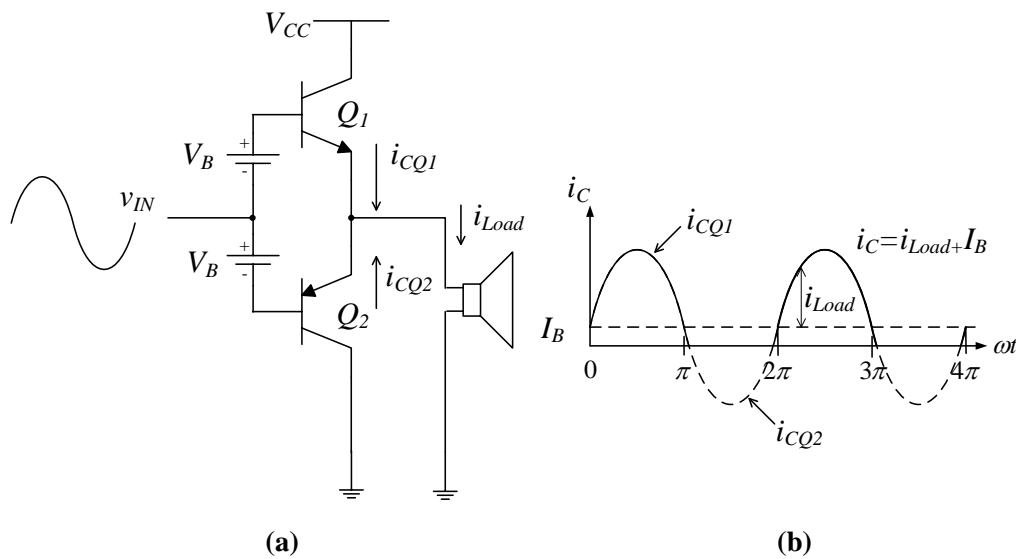


Figure 2.5 (a) Class AB output stage, and (b) Class AB output current waveform

Figure 2.5(b) depicts the output current of each power transistor. The conduction angle of each power transistor is slightly more than 180° and usually much less than 360° [2, 44]. There is a short period where both transistors are on at the same time which results in a compromise to the power-efficiency. The power-efficiency of the Class AB amplifier is somewhere in between the Class A amplifier (25%) and the Class B amplifier(78.5%), depending on the biasing condition.

2.3.2 Non-conventional Linear Amplifiers: Class G amplifiers

The output stage of a single-ended Class G amplifier [45, 46] is depicted in Figure 2.6(a). It consists of a basic Class AB amplifier with two voltage supply rails (HV_{CC} is the high voltage supply rail and LV_{DD} is the low voltage

supply rail) and a control circuit (typically a transistor operating as a switch). The control circuit serves to connect the appropriate voltage supply rail according to the instantaneous output voltage level. In this fashion, its power-efficiency is higher than that of the Class AB amplifier whose voltage supply rail is HV_{CC} .

Figure 2.6 (b) depicts an example of a Class G amplifier output voltage signal where the dotted lines are the two voltage supply rails. When the output signal swing approaches or exceeds the lower voltage rail, LV_{CC} , the control circuit enables the higher voltage rail HV_{CC} to be connected as the supply rail. On the other hand, when the output voltage swing is low, HV_{CC} is disconnected and the LV_{CC} is connected as the voltage supply rail.

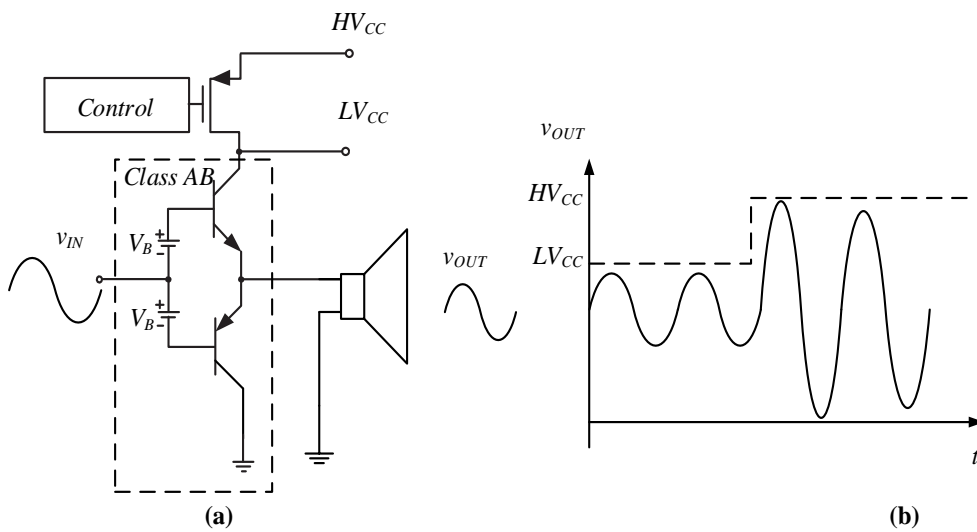


Figure 2.6 (a) Class G output stage based on Class AB output stage with two voltage supply rails, and (b) Class G output voltage waveform

In summary, in the context of low-power high-fidelity earphone/headphone amplifiers, the Class AB amplifier is not unexpectedly the amplifier of choice. This is because its power-efficiency exceeds that of the Class A amplifier while its fidelity is nearly comparable. The Class B amplifier is unacceptable due to its severe distortion despite its superior power-efficiency. The Class G, on the other hand, is not usually considered because in the earphone/headphone application, the multiple power supply rails increase the complexity of the design.

2.3.3 Switching Amplifiers: CDAs

CDAs have recently been increasingly accepted as a viable alternative to classic linear amplifiers largely because of their substantially higher power-efficiency (>90% over a large range of modulation indexes). The high power-efficiency attribute is worthwhile as it translates to smaller form-factor, arising from the elimination of the heat sink or at least a significantly reduced heat sink in mid-high power realizations, and an increased battery lifespan in portable applications.

Figure 2.7 depicts the typical power-efficiency of CDAs across the entire modulation index range. The power-efficiency of Class A, Class B and Class G amplifiers are plotted for comparison. It can be seen that CDAs offer the highest power-efficiency (>90% at $M=0.9$) compared to the linear amplifiers (the theoretical maximum power-efficiency of Class A amplifiers is 25% and that of Class B amplifiers (with serious crossover distortion) is 78.5%). The

power-efficiency of Class G amplifiers has two regions of power-efficiency which corresponds to the two voltage supply rails as discussed earlier.

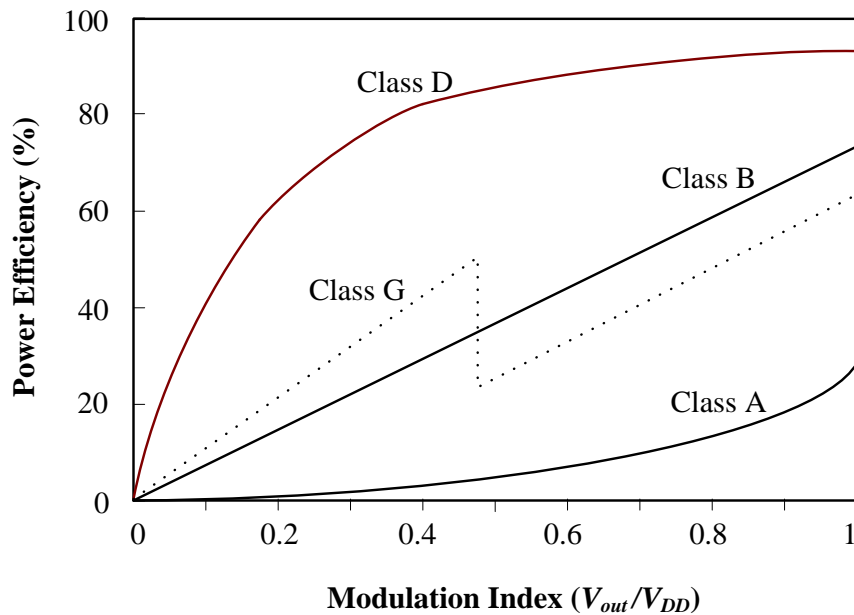


Figure 2.7 Power-efficiencies of different amplifiers

Despite the high power-efficiency attribute of CDAs, their fidelity is typically inferior to their linear Class A and AB counterparts. For example, the THD of many CDAs is relatively large ($> 0.1\%$), and hence, not unexpected, CDAs are still unacceptable for some sectors of high-fidelity audio applications, including earphone/headphone amplifiers. The nonlinearities of the CDAs may arise from various functional blocks [1, 47, 48]. In the modulator, the nonlinearity arises from pulse width error in the pulses due to non-ideal carrier generator. In the output stage where most of the nonlinearities occur, the nonlinearities are caused by the power supply noise, mismatch of rise and fall time of the output pulses and dead-time (the timing errors added by the gate drivers). The LC lowpass filter contributes to the nonlinearities due to imperfect winding and imperfect core material. The nonlinearities arising

from the LC filter could be estimated from the inductance droop [15] ($\Delta L/L_o$ where ΔL is the variation of the inductance and L_o is the nominal inductance) of the inductor when the inductance droop at the rated current is the only known parameter (given in inductor datasheets) – 1% of the inductance droop could give rise to 0.05% of THD and 10% of the inductance droop could give rise to 0.2% THD.

As delineated earlier, the conventional CDA comprises a modulator, an output stage, a LC lowpass filter and a feedback network as depicted in Figure 2.8. The modulator modulates the analog input signals into a train of pulses, and the modulation modality may be of several approaches, including PWM and PDM, etc (see Section 2.4 later). The output stage consists of a chain of inverters (which buffers the pulse signals and the final inverters having sufficient power to drive the load) and control circuits (including protecting circuits). The LC lowpass filter is usually employed to attenuate the high frequency carrier to retrieve the audio band analog signal from the pulse train output.

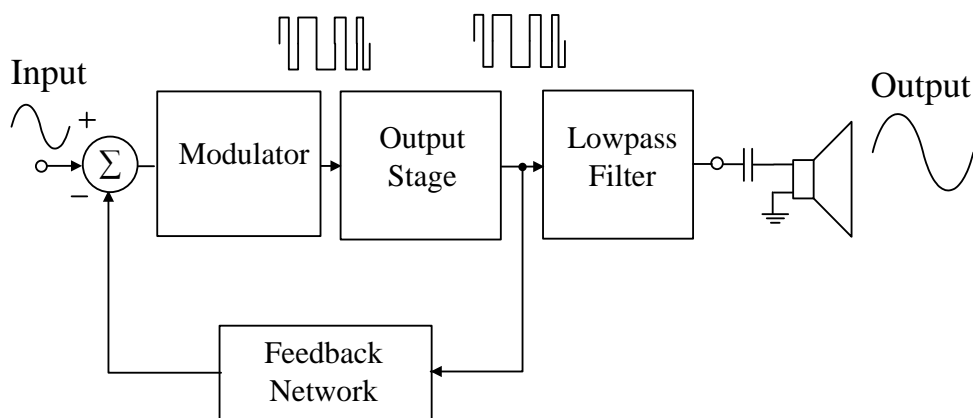


Figure 2.8 Block diagram of a conventional CDA with a single-ended output stage driving a loudspeaker load

The design of the output stage and choice the LC lowpass filter [49] are well established. The schematic of the single-ended output stage and the LC lowpass filter are depicted in Figure 2.9. As opposed to the linear operation of the output transistors (in the active region) of the output stage of the linear amplifiers, the output transistors in the output stage of the CDAs operate in switching-mode (in the triode or cut-off regions), hence the higher power-efficiency. As the output transistors are controlled by a train of ‘digital format’ pulses instead of the continuous analog signal, the conduction angle for the CDA is theoretically 0° .

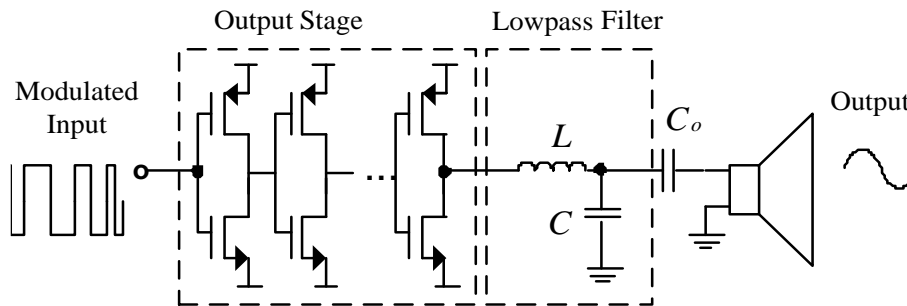


Figure 2.9 Single-ended CDA output stage

The power-efficiency of the CDA output stage is ideally 100%. Nonetheless, in practice, some power is dissipated at the output stage, and it can be significant in some cases. The mechanisms of power dissipation are well established [1, 50, 51]:

- (i) Power dissipated due to parasitic capacitance, P_c

$$P_c = \frac{1}{2} f_c C_P V_{DD}^2 \cdot \quad (2-7)$$

where f_c = switching frequency or carrier frequency, and

C_P = total parasitic capacitance.

- (ii) Power dissipated due to on-resistance of transistors, P_r

$$P_r = \frac{1}{T_s} \int_0^{T_s} i_o^2 R_{on} dt . \quad (2-8)$$

where T_s = period of the input signal,

i_o = instantaneous output current, and

R_{on} = on-resistance of the output transistor, typically small, 0.1-0.3m Ω for 32 Ω loads.

- (iii) Power dissipated due to short-circuit current (when two output transistors are simultaneously turned on) during the transitions due to the finite rising/falling time, P_s

$$P_s = I_{mean} V_{DD} . \quad (2-9)$$

where I_{mean} = mean value of the short-circuit current

The total power dissipation of the CDA output stage, P_{dissip} , is hence

$$P_{dissip} = P_c + P_s + P_r . \quad (2-10)$$

To reduce the power loss due to the non-ideal output stage, we can decrease the switching frequency f_c , and better optimize the value of C_P , and R_{on} . The short circuit current, on the other hand, can be mitigated by a dead-time or control scheme to avoid the two transistors (p -type and n -type transistors of the inverter of the output stage) turning on at the same time during the voltage

transitions. In some reported designs, by properly optimizing the above parameters, the power-efficiency of the CDAs can reach 97% [52].

2.4 A Review of CDA Modulation

In CDA design, the modulator is a critical analog signal processing block, and this block converts the analog input signal to a pulse-modulated signal with respect to a high frequency (~100 kHz-1 MHz) carrier signal. The most ubiquitous modulation is PWM. The PWM modulation is based on the carrier obtained from an additional carrier generator circuit to generate the modulated pulse signals. Another modulation approach is based on Pulse Density Modulation (PDM) which is less ubiquitous. The PDM modulation is based on the carrier typically generated through self-oscillation by the circuit itself. These modulation schemes will now be reviewed in turn.

2.4.1 Pulse Width Modulation (PWM)

PWM is probably the most prevalent modulation approach for analog CDAs and its prevalence is largely due to its hardware simplicity, low switching frequency (~350 kHz to 500 kHz), and high stability at near 100% modulation depth [53].

The PWM CDAs topologies include the open-loop topology and the closed-loop topology with incomplete feedback and complete feedback.

2.4.1.1 Open-loop PWM CDAs

A single-ended open-loop PWM CDA is depicted in Figure 2.10. The pulse width modulator comprises a comparator with two inputs, an input signal (V_{in}) and a triangular carrier signal (V_c). The triangular carrier is typically obtained from an additional carrier generator circuit and the associated hardware is an overhead (compared to the self-oscillating approach).

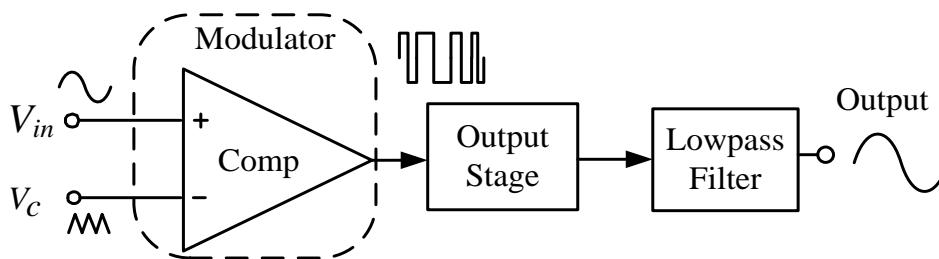


Figure 2.10 Block diagram of an open-loop PWM CDA

A typical PWM output depicted in Figure 2.11 is generated by comparing the magnitude of V_{in} (the modulating sinusoid signal) and V_c . The ensuing pulse width of the PWM output is proportional to the magnitude of V_{in} . The carrier frequency of the PWM output is determined by the frequency of V_c , and is constant.

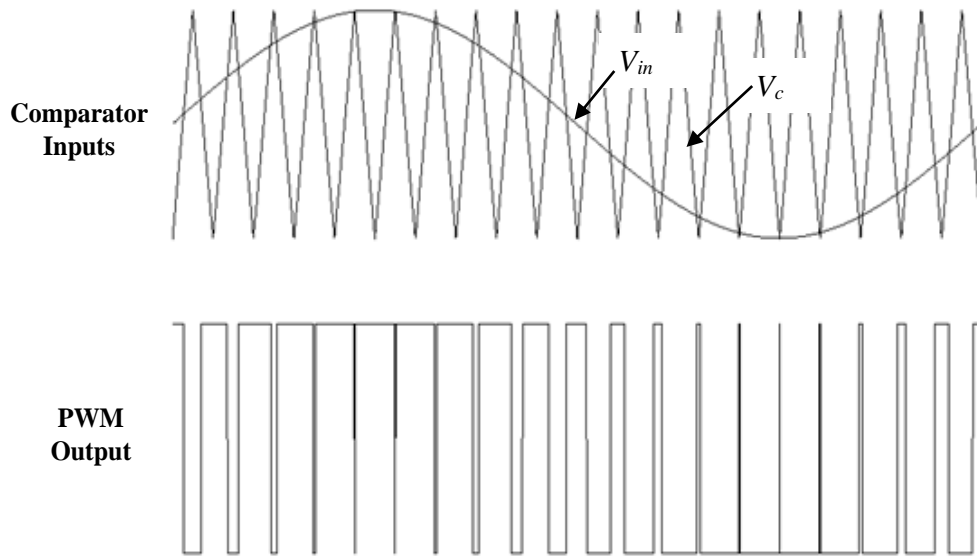


Figure 2.11 Waveforms of the PWM CDA

The well established linear model of the open-loop CDA [54, 55] is depicted Figure 2.12. In this model, H_{PWM} is the gain of the modulator (the modulator is assumed to be ideal) and V_N represents the nonlinearities of the modulator, the output stage and the LC lowpass filter.

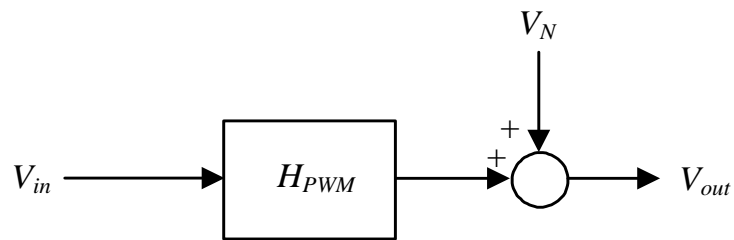


Figure 2.12 Linear model of an open-loop PWM CDA

In this linear model, the pulse width modulator is assumed to be a constant gain stage, and the signal gain at the PWM modulator is expressed as

$$H_{PWM} = \frac{V_{DD}}{V_{C_peak}}. \quad (2-11)$$

where V_{C-peak} = peak value of the triangular carrier signal V_c .

It can be seen from the linear model that the nonlinearities appear directly at the load without any attenuation – this is because feedback is not applied. The nonlinearities can be high, for example the THD+N > 1% [55]. Further, it has been shown that the PSRR is 6dB [55], a value inappropriate for practical applications.

Overall, in view of these serious shortcomings, the open loop PWM CDA is not practical, save in applications that are highly hardware- and power-critical, for example in some early hearing aid applications [56, 57].

2.4.1.2 Closed-loop PWM CDAs with Incomplete Feedback

Closed-loop PWM CDAs can be generally classified based on the feedback topology - incomplete feedback or complete feedback. These closed-loop CDAs offer substantially lower nonlinearities than the open-loop counterparts due to the well-known negative feedback mechanisms.

The closed-loop PWM CDAs with incomplete feedback depicted in Figure 2.13 is presently the most ubiquitous architecture adopted for CDAs. The input of the feedback is sampled at the output of the output stage and fed back to the modulator comprising an integrator (equivalent to a loop filter) and a comparator. The integrator functions as a summing circuit and attenuates the high frequency carrier signals. The integrator serves to provide a high loop

gain for audio-band signals, thereby attenuating the nonlinearities from the feedback mechanism.

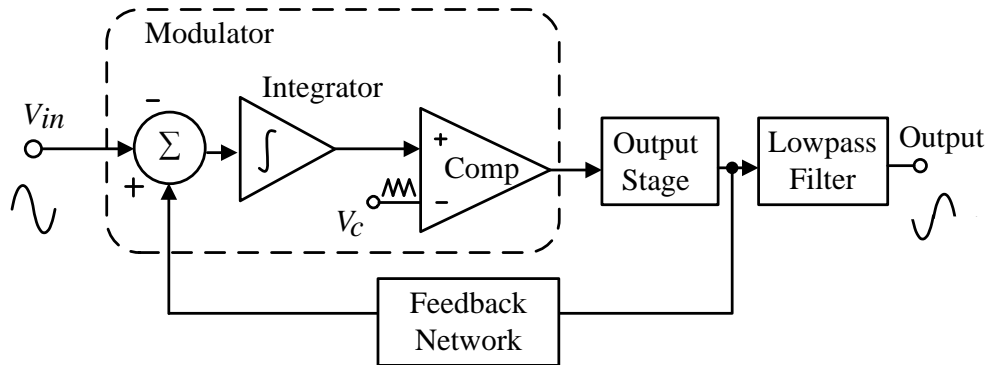


Figure 2.13 Block diagram of a closed-loop PWM CDA with incomplete feedback

To delineate the feedback, Figure 2.14 depicts the linear model for the PWM CDAs where $H_{loop-filter}$ is the gain of the loop filter, $H_{feedback}$ the feedback factor and H_{PWM} the gain of the comparator. In PWM CDAs with feedback, the nonlinearities (V_N) from the modulator and output stage are attenuated by a factor of $(Loop_Gain+1)$, $Loop_Gain = H_{loop-filter} \times H_{PWM} \times H_{feedback}$. To further attenuate these nonlinearities, a higher order loop filter could be employed to increase the loop gain[58]. Note that as the LC lowpass filter is not a constituent part of the feedback loop, nonlinearities arising from the LC lowpass filter remain unattenuated. This, as delineated in Chapter 1, is the major drawback of CDAs with incomplete feedback.

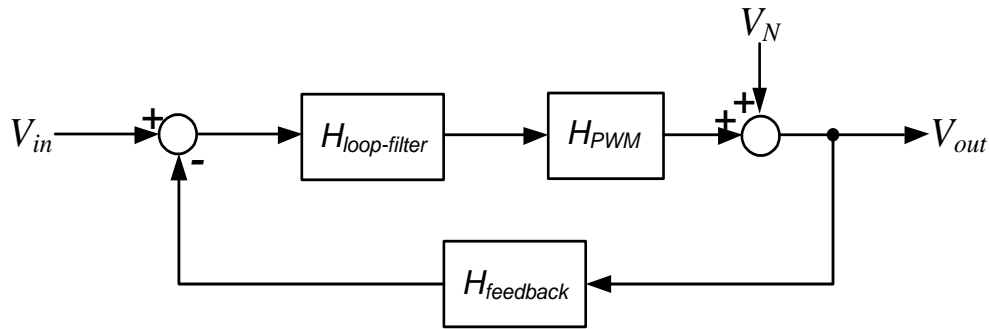


Figure 2.14 Linear model of a closed-loop PWM CDA

Unlike the PWM CDAs with ‘Incomplete Feedback’, PWM CDAs with ‘Complete Feedback’ have all their feedforward blocks constituents of their feedback path, including the *LC* filter where pertinent. In some PWM designs, the *LC* filter is unnecessary and in such designs, they are also classified within the PWM CDA with complete feedback if their remaining blocks are constituents of the feedback loop.

2.4.1.3 Closed-loop PWM CDAs with Complete Feedback

2.4.1.3.1 ‘Filterless’ PWM

Examples of ‘filterless’ CDAs include work described in [16, 17] [43, 59]. Other than the absence of the nonlinearities of the *LC* filter (due to its absence), the added advantage is the cost saving (~10% reduced cost) and the reduction of form factor on the Printed Circuit Board (30%-70% smaller area) [60]. Not unexpectedly, the filterless CDAs lend itself to lower-cost and potentially to higher-fidelity audio applications than most other CDAs [61, 62].

A typical filterless CDA with a BTL output stage topology is depicted in Figure 2.15. The loudspeaker is typically required to be inductive [63] and is modeled as an inductor and a resistor in series as depicted Figure 2.16. The output of the filterless PWM CDA is usually based on the tri-state modulation [64] architecture where the differential output of the CDA has three signal levels. The tri-state modulation results in reduced high frequency energy (compared to the regular two-state modulation (e.g. Figure 2.13)). As the loudspeaker is inductive, the loudspeaker remains undamaged (as long as the output is within its rated output).

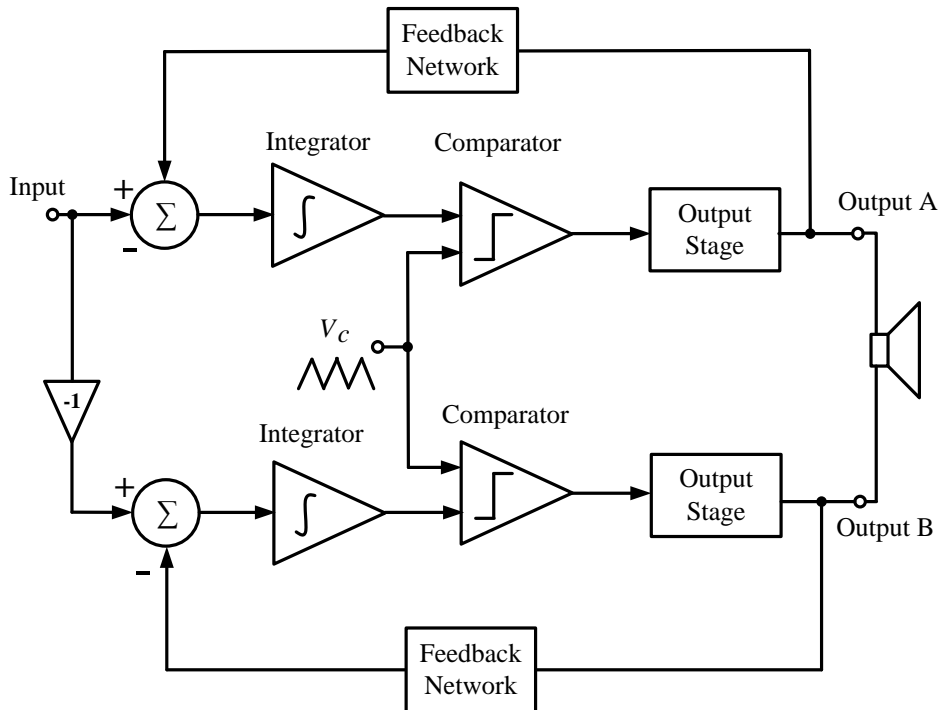


Figure 2.15 Block diagram of a closed-loop filterless PWM CDA

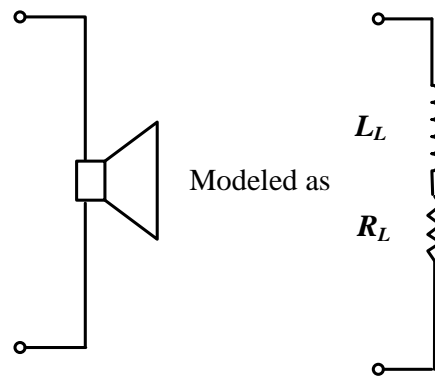


Figure 2.16 The model of the speaker

Unfortunately, the ‘filterless’ CDA has serious shortcomings rendering them inapplicable to earphone/headphone applications. First, the tri-state ‘filterless’ CDAs requires a BTL output stage which is incompatible to the 3-pin (TRS) or 4-pin (TRRS) earphone/headphone connector. Second, despite its lesser high frequency components (at the carrier frequency) at the output of the output stage, the magnitude of these components remain large (larger than at the output of the LC lowpass filter). Third, the ‘filterless’ CDA relies on a highly inductive load (highly inductive loudspeakers are typically expensive, unlike general purpose earphones/headphones) to effectively attenuate the high switching frequency. The high frequency components result in higher switching noise and higher Electro-Magnetic interference (EMI), and they may interfere with radio frequency functions such as communications in the mobile phone, GPS, or FM radio, etc, in the mobile devices [19]. In addition, the long wire from the ‘filterless’ CDA output to the earphone/headphone load increases the probability of interference from the high frequency components, resulting in higher EMI. In general, these shortcomings are sufficiently severe such that filterless CDAs are not considered appropriate for mobile applications.

2.4.1.3.1 ‘Filtered’ PWM with Complete Feedback

The conventional (‘filtered’) CDA is the preferred choice to the ‘filterless’ CDAs in view of the EMI sensitive mobile applications. The block level design of a closed-loop PWM CDA with complete feedback is depicted in Figure 2.17. In this ‘filtered’ CDA with complete feedback, the input of the feedback is sampled at the output of the *LC* lowpass filter. As the *LC* lowpass filter is now included in the feedback loop, the nonlinearities arising from the *LC* lowpass filter could be now attenuated. However, the phase lag arising from the *LC* lowpass filter presents some design difficulties particularly stability.

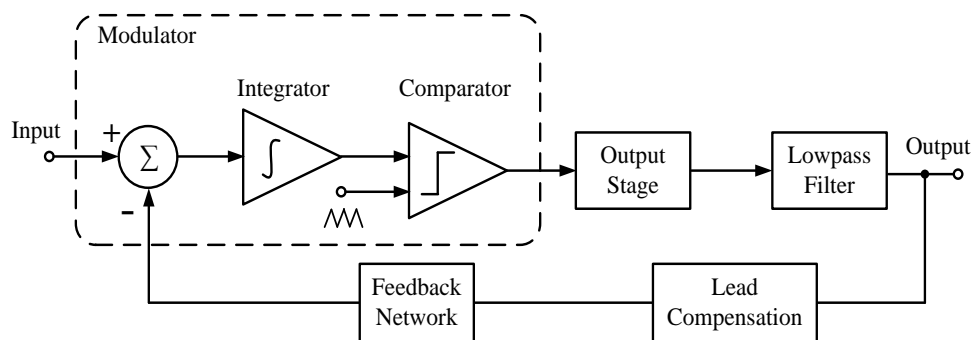


Figure 2.17 Block diagram of a closed-loop PWM CDA with complete feedback

The stability issue involves compensating not only the 180° phase lag caused by the *LC* lowpass filter, but also ensuring a 45° phase margin and/or 10dB gain margin. This design is not trivial in view of the general need to keep the hardware overheads low. For example, a reported design in [14] employs an extra inductor (two inductors in one design) to compensate the phase lag,

thereby increasing the hardware and cost, and hence incompatible with mass-market earphone/headphone applications.

Despite the design challenges and hardware overheads, the ‘filtered’ PWM CDA with complete feedback offers increased circuit immunity to the load variations as the *LC* lowpass filter is a constituent part of the feedback. To address the hardware overheads, the complete feedback ‘filtered’ CDAs can be implemented as self-oscillating CDAs (with Pulse Density Modulation, PDM).

2.4.2 Pulse Density Modulation (PDM)

Figure 2.18 depicts a waveform of the PDM output. Figure 2.18 depicts a waveform of the PDM output. The information in PDM output includes both its pulse density and its pulse width. As opposed to the PWM output, the carrier frequency of the PDM output is not constant - the carrier frequency changes when the instantaneous magnitude of the input signal changes. The maximum switching frequency is the idling switching frequency when the input signal is at zero-input ($M = 0$). The minimum switching frequency occurs when the input is at maximum amplitude ($M = 0.9$). This varying carrier frequency characteristic of the PDM output is often undesirable for high-fidelity purpose because the loop gain decreases with the decreasing switching frequency.

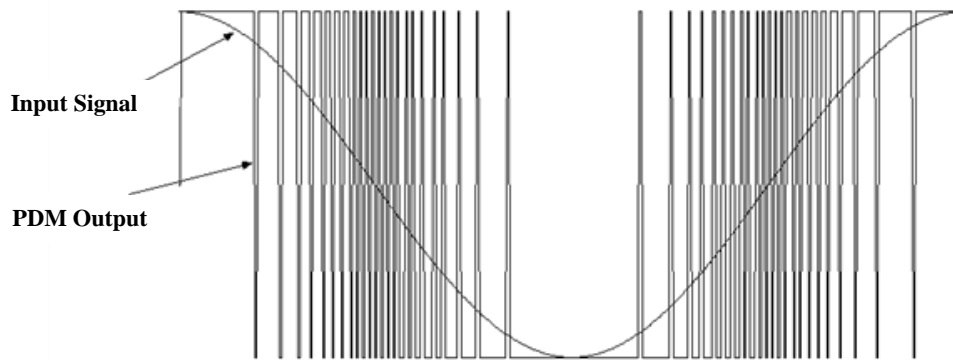


Figure 2.18 Waveforms of the self-oscillating CDA with PDM output

PDM is typically realized by the self-oscillating approach where the idling switching frequency is the innate self-oscillation frequency of the CDA (as an oscillator). The oscillation occurs at the frequency where the total phase shift of the entire loop network is 360° (positive feedback). Put simply, CDAs based on self-oscillating approach embodies a closed-loop topology (with feedback).

Figure 2.19 depicts a generic self-oscillating CDA [24, 58-68] comprising a modulator, an output stage, a *LC* lowpass filter and a feedback network. Note that there is no external carrier applied to the CDA (the comparator is connected to a DC reference voltage (typically signal ground or $V_{DD}/2$) as opposed to the triangular carrier in the PWM CDA. The carrier is ‘generated’ by the oscillation of the CDA when the total phase shift of the entire loop network is 360° . This oscillation frequency is the switching frequency of the CDA, for example 1MHz as depicted in Figure 2.20 [15, 16, 20, 24]. Note that the phase starts from -180° - this is contributed from negative feedback network.

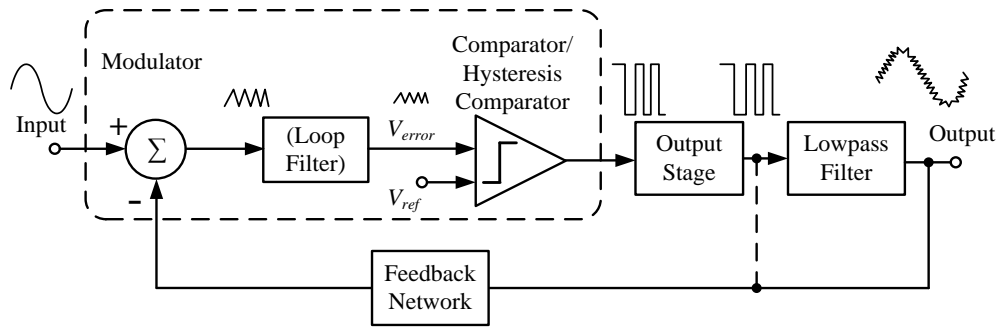


Figure 2.19 A typical self-oscillating CDA

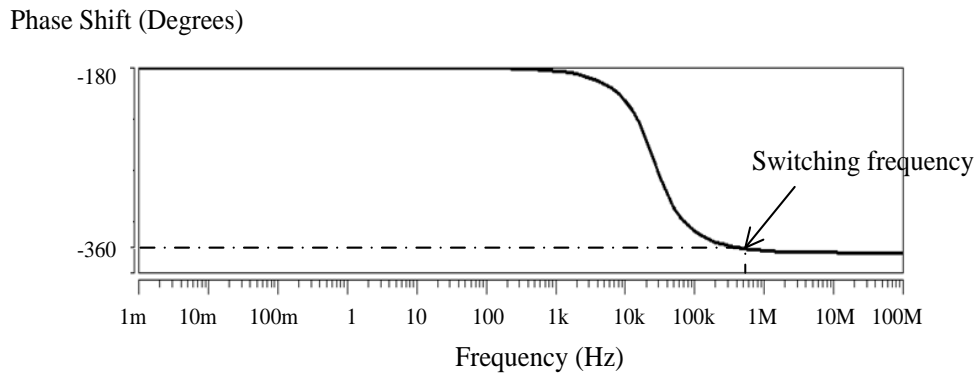


Figure 2.20 The switching frequency of Self-oscillating CDA

The total phase shift is sum of the phase lag from each block in the feedback loop of the CDA. There are a number of implementations of different combinations of the blocks in the feedback loop to generate the oscillation frequency of the CDA. Reported implementations include the Sigma-Delta CDA [69], Bang-Bang Control CDA [73], Sliding Mode Control CDA [76], Controlled Oscillating CDA [21], etc.

Self-oscillating CDAs with PDM output are advantageous over the PWM CDAs in a number of ways. First, as the self-oscillating CDA is a positive feedback system, the phase margin requirement (in usual feedback CDAs) is irrelevant and the stability issue is not of concern. Second, due to the higher

loop gain provided by the comparator (and the high switching frequency (>500 kHz)) [26], the self-oscillating approach inherently provides for a CDA with lower nonlinearities appropriated for the high-fidelity earphone/headphone amplifier applications. Third, as the switching frequency of the self-oscillation CDA spreads across a wider frequency range, and less EMI [29, 77, 78] is emitted compared to PWM CDAs whose switching frequency is constant. Overall, the self-oscillating CDA potentially offers higher fidelity with reduced design constraints for complete feedback high-fidelity earphone/headphone applications.

The various reported implementations of self-oscillating CDA can generally be classified as either incomplete feedback or complete feedback. These will now be reviewed in turn.

2.4.2.1 Self-oscillating CDA with Incomplete Feedback

Figure 2.21 depicts a CDA based on the self-oscillating approach with incomplete feedback – the *LC* lowpass filter is not constituent of the feedback loop. In place of the regular comparator in the modulator, a hysteresis comparator is generally employed. This topology exploits the phase shift of the hysteresis comparator to generate a self-oscillation condition. The loop filter in the form of an integrator is usually designed to increase the loop gain of the CDA.

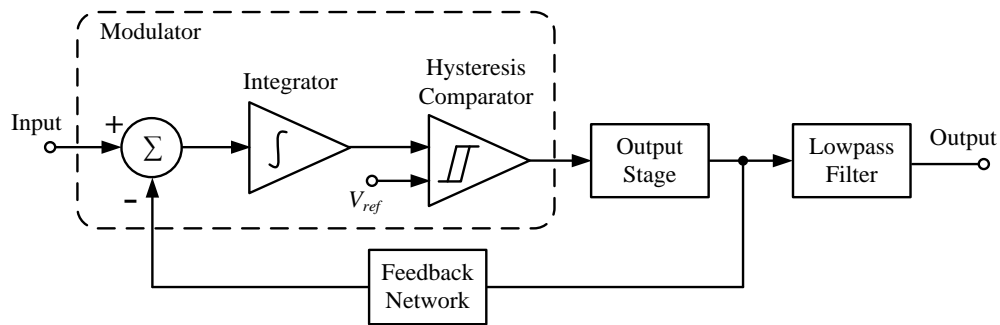


Figure 2.21 Block diagram of a self-oscillating CDA with incomplete feedback

In this CDA, the input signal and the feedback signal from the output of the output stage are fed to the modulator. The modulator includes an integrator (a loop filter) and a hysteresis comparator via a summing circuit. The hysteresis comparator herein continuously outputs the PDM output.

Typical Sigma-Delta CDAs [71] and Bang-Bang Control CDAs [72] both rely on the phase lag contributed by the hysteresis comparator to generate the oscillation condition. Note that the loop filter could be placed in the modulator (as in the Sigma-Delta CDAs) or in the feedback network (as in the Bang-Bang Control CDAs).

The fidelity of the Sigma-Delta CDAs and Bang-Bang Control CDAs is typically higher than the PWM CDAs due to the higher loop gain of the comparator (and higher switching frequency (>300 kHz)). In general, these CDAs are well accepted as high-fidelity analog CDAs where a high quality *LC* lowpass filter is employed.

2.4.2.2 Self-oscillating CDA with Complete Feedback

The self-oscillating approach with complete feedback addresses the nonlinearities of the *LC* lowpass filter as the filter is a continuant/component of the feedback loop. The sliding mode CDA and the controlled self-oscillating CDA are both embodiments of the self-oscillating CDA with complete feedback architecture.

This architecture leverages on the inherent phase shift of the *LC* lowpass filter to generate a self-oscillation condition - the phase lag introduced by 2nd-order *LC* lowpass filter is now hence useful as its phase lag constitutes part of the total phase lag required for positive feedback. In this sense, the self-oscillating CDA does not require an additional phase compensation circuit.

Figure 2.22 depicts the general block diagram of self-oscillating approach with complete feedback. This comparator could be a hysteresis comparator or a normal comparator. A controller is required within the feedback loop to tune the switching frequency. In the circuit, the modulator sums the input signal and the feedback signal from the *LC* lowpass filter, and the comparator outputs the PDM output.

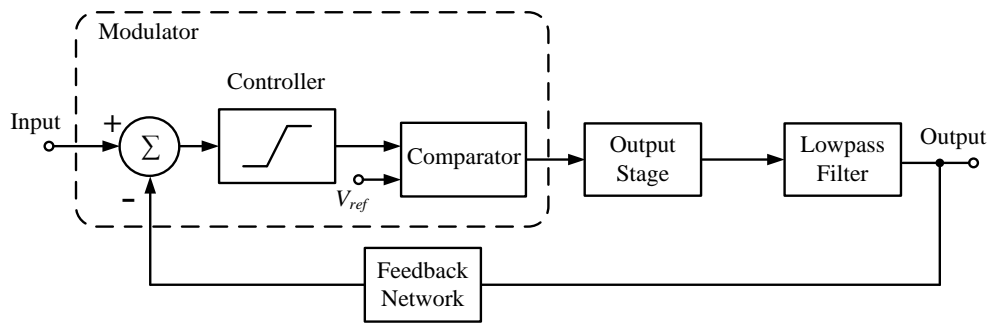


Figure 2.22 Block diagram of a self-oscillating CDA with complete feedback

The controller embodies phase lead-lag characteristics to allow sufficient headroom to tune the switching frequency. In the sliding mode CDA, the controller is placed within the modulator and in the controlled self-oscillating CDA, it is placed within the feedback network.

The comparator contributes minimum or negligible phase shift to the CDA. In the sliding mode CDA, the phase lag contributed by the hysteresis comparator in the complete feedback configuration is much smaller than that in the incomplete configuration – the hysteresis band is a few mV [73] in the former compared to hundreds of mV in the latter [79]. In the case of controlled self-oscillating CDA, the comparator is a normal comparator (instead of the hysteresis comparator) to reduce the phase lag contribution.

The fidelity of sliding mode CDAs and controlled self-oscillating CDAs is typically high at low modulation index (e.g. THD+N < 0.01% in [21, 76] at $M=0.1$). However, the fidelity may be unsatisfactory at high modulation index (e.g. THD+N = 1.1% in [76] at $M=0.9$ and THD+N = 0.9% in [21] at

$M=0.9$) due to insufficient loop gain provided by the controller (and the spreading of the switching frequency to a lower frequency at high M). To mitigate the nonlinearities, a higher loop gain is required. This is one of the important considerations that will be addressed in the proposed CDA in the next Chapter.

2.5 Conclusions

This chapter has reviewed the classical linear amplifiers (Class A, Class B, Class AB and Class G amplifier) and CDAs, and the review has delineated the merits and shortcomings of the different classes in terms of fidelity and power efficiency. CDAs can be generally classified according to their modulation modalities - either PWM or PDM, and a review of the different CDA architectures within their classifications has been delineated. Among the various modulations and architectures, the PDM CDA based on self-oscillating approach with complete feedback provides higher potential for lower nonlinearities due to the high loop gain and high switching frequency compared to the PWM modulation with incomplete feedback configurations. In addition, PDM with complete feedback features better robustness and less design constraint in terms of stability issues.

**Chapter 3 Design of the
Proposed High-fidelity CDA
with Complete Feedback**

3.1 Introduction

It was delineated in Chapters 1 and 2 that low-power earphone/headphone amplifiers are presently dominated by linear amplifiers (Class AB or Class G). At this juncture, although there are a few reported analog CDA designs embodying the self-oscillating approach with complete feedback (as delineated in Chapter 2) for general high-fidelity audio applications, to the author's knowledge, there are to date none reported for low-power high-fidelity earphone/headphone applications. This chapter delineates the system level and circuit level design of a novel single-ended output low-power high-fidelity power-efficient analog CDA with complete feedback based on the self-oscillating approach for earphones/headphones – possibly the first such an attempt for earphones/headphones.

To meet the high-fidelity and high power-efficiency requirements, the proposed design features high loop gain and well controlled switching frequency ($<1\text{MHz}$) by means of a novel integrator-cum-control block embodied in the modulator (of the proposed CDA). The proposed 2nd-order lossy integrator therein features high loop gain ($>150\text{dB}$ at DC). This is to attenuate the nonlinearities of the blocks (the modulator, output stage and the *LC* lowpass filter in the feedback loop) and to suppress the noise across the entire audio frequency range (20 Hz-20 kHz). The proposed control block therein is designed with phase lead-lag characteristics to compensate for the intrinsic delay of the overall design and tuned to establish the desirable switching frequency.

This chapter also delineates analytical work to model the functionality of the blocks of the proposed CDA to depict the pertinent parameters thereof that affect the fidelity and the switching frequency. This analytical work is useful as it provides meaningful insights to the design of the proposed CDA.

On the basis of HSPICE simulations and physical measurements on the proposed CDA built with discrete components on the Vero Board, the proposed CDA is verified to meet the specifications of a low-power high-fidelity audio amplifier for earphones/headphones: SNR \geq 90dB, THD+N \leq 0.01% and PSRR \geq 70dB. These parameters are comparable to state-of-the-art linear (Class AB) amplifiers and yet substantially more power-efficient, for example, $\eta=90\%$ at the maximum modulation index (vis-a-vis 65% for the linear amplifier).

3.2 System Level Design

The operation of the self-oscillating CDAs is substantially different from conventional closed-loop CDAs. In the design of the latter, stable negative feedback is achieved by obtaining sufficient phase margin, typically $>60^\circ$ or gain margin, typically >10 dB. The self-oscillating CDA, on the other hand, is a positive feedback CDA (essentially an oscillator), and its innate switching frequency is the oscillating frequency when the overall phase shift reaches -360° . Hence, the phase margin requirement, in this sense, is irrelevant and this CDA is inherently robust – stability issues are not of concern.

As delineated in Chapters 1 and 2, the design of a CDA embodying the self-oscillating approach is challenging for two reasons. First, current-art complete feedback CDAs embodying the self-oscillating approach generally suffers from relatively high nonlinearities at high modulation indexes, thereby generally is unacceptable for high-fidelity audio applications. In the intended earphone/headphone application, the effect of this nonlinearity is exacerbated due to the psychoacoustical effects of donning earphones/headphones and in part due to 3-pin TRS or 4-pin TRRS connectors which requires the use of single-ended output amplifiers. Second, the self-oscillating approach being largely an oscillator, innately generates its switching frequency internally as opposed to the PWM modulation approach whose switching frequency is generated by a carrier generator elsewhere. As the switching frequency is dependent on the phase lag from all blocks in the CDA, it is imperative that the phase of each block is properly designed to ensure ‘optimal’ switching frequency and power efficiency.

Figure 3.1 depicts the block diagram of the proposed self-oscillating CDA with complete feedback. The feedback is sampled at the output of the *LC* lowpass filter (as opposed to the output of the output stage in the incomplete feedback). From a block diagram perspective, it is the same as reported designs – comprising four major blocks: a modulator, an output stage, an *LC* lowpass filter and a feedback network. The delay in Figure 3.1 is not a dedicated hardware block in the CDA but simply a model to model the phase lag due to propagation delay. The novelty is in the design of the modulator.

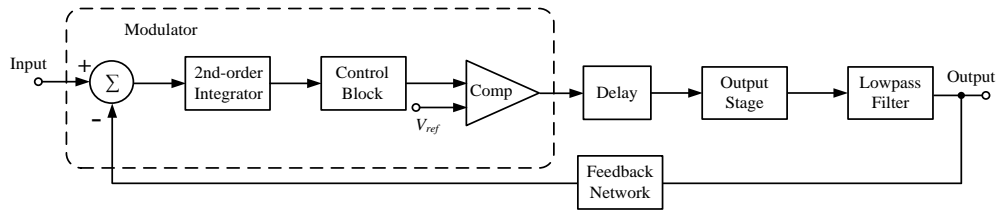


Figure 3.1 Block diagram of the proposed CDA

The proposed novel modulator comprises three sub-blocks: a 2nd-order integrator, a control block and a comparator. At the system level design, the novel modulator addresses two concerns. The first concern is the high nonlinearities at high modulation indexes and this is addressed by designing a 2nd-order integrator to provide high loop gain in the audio band. Note that the integrator is designed without compromising the optimal switching frequency (see later). The second concern is the tuning of an ‘optimal’ switching frequency. The control block is designed to compensate the propagation delay of the design to allow (better) control of the switching frequency. These two concerns are related - the switching frequency to be designed to be sufficiently high for the high loop gain of the comparator and hence low nonlinearities.

3.2.1 Oscillation Condition

As delineated in Chapter 2, oscillation arises at the frequency where the total phase shift of the entire loop network is 360°. The blocks that contribute to the phase lag are the 2nd-order integrator, the control block, comparator, delay block, output stage, *LC* lowpass filter, and feedback network.

The overall phase ϕ is

$$\phi_{Overall} = \phi_{Integrator} + \phi_{Control_Block} + \phi_{Comparator} + \phi_{Delay} + \phi_{Output_Stage} + \phi_{Lowpass_Filter} + \phi_{Feedback} \quad (3-1)$$

In the proposed design, the switching frequency is designed at ~1MHz to meet the high-fidelity requirements of earphone/headphone amplifiers. Among these phase shifts, ϕ_{Delay} and $\phi_{Lowpass_Filter}$ have limited design margin, while $\phi_{Integrator}$ and $\phi_{Control_Block}$ are the main design parameters; the phase shift introduced by the comparator is zero at $M=0$ and the phase shift introduced by the feedback network and output stage is assumed to be zero (as the delays are taken into consideration in the propagation delay). The detailed frequency response of each block will be illustrated in the next section.

3.2.2 Overall Loop Gain

The overall loop gain of the CDA is determined by

$$H_{Overall} = H_{Integrator} \times H_{Control_Block} \times H_{Comparator} \times H_{Delay} \times H_{Output_Stage} \times H_{Lowpass_filter} \times H_{Feedback} \quad (3-2)$$

where $H_{Delay}=H_{Output_Stage}=H_{Feedback}=1$ within audio band, and

$H_{Integrator}$, $H_{Control_Block}$, $H_{Comparator}$ and $H_{Lowpass_Filter}$ are given

by eqns. (3-3), (3-5), (3-10) and (3-14) later respectively.

The overall loop gain of the CDA is high in part, due to the high loop gain of the 2nd-order integrator (see next section), and is not constant throughout the audio band (see equation (3-3) later). The comparator further provides substantial loop gain and is not constant - it varies with the switching frequency (see equation (3-10) later). Note that $H_{Lowpass_Filter}=1$ within the audio band. The loop gain (and the phase shift) for each block will now be delineated.

3.3 Individual Block Schematic Design

Figure 3.2 depicts the schematic of the proposed self-oscillating CDA with complete feedback. The schematics of the major blocks, the 2nd-order lossy integrator consisting of two 1st-order lossy integrators, control block, comparator, output stage, *LC* lowpass filter and the feedback network, are depicted.

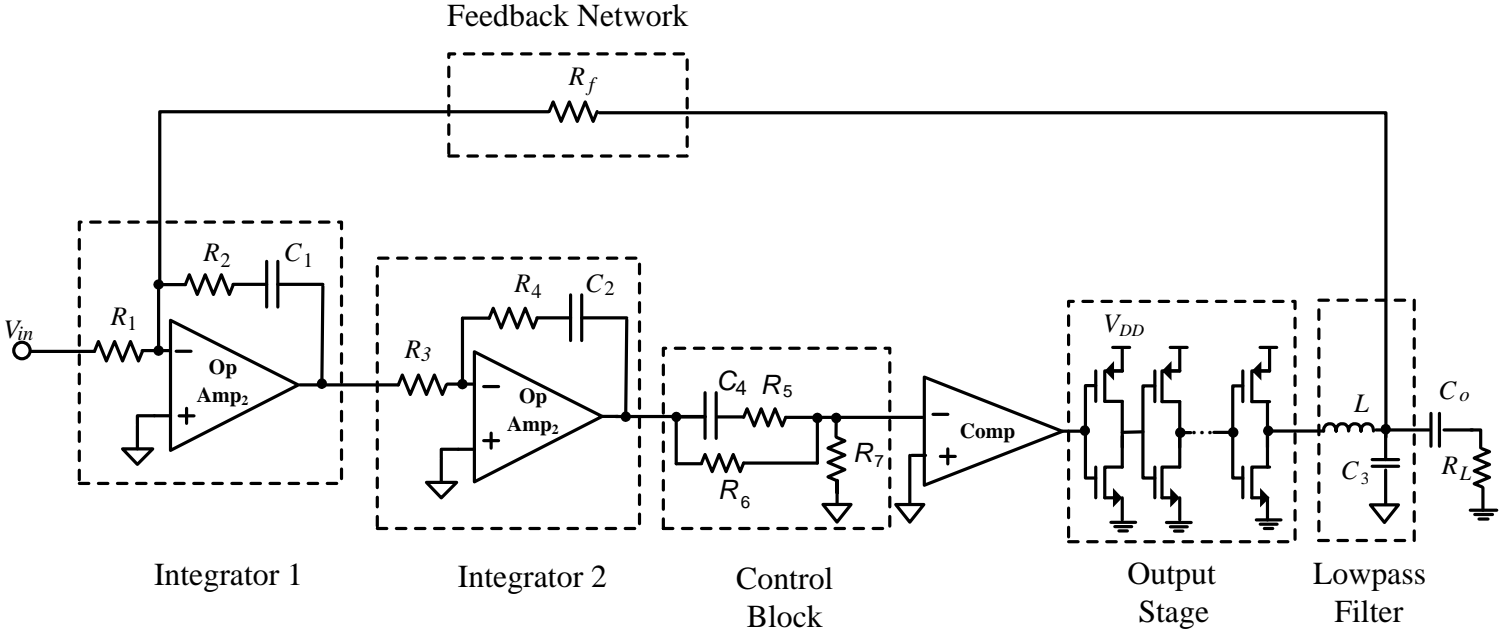


Figure 3.2 Circuit implementation of the proposed CDA

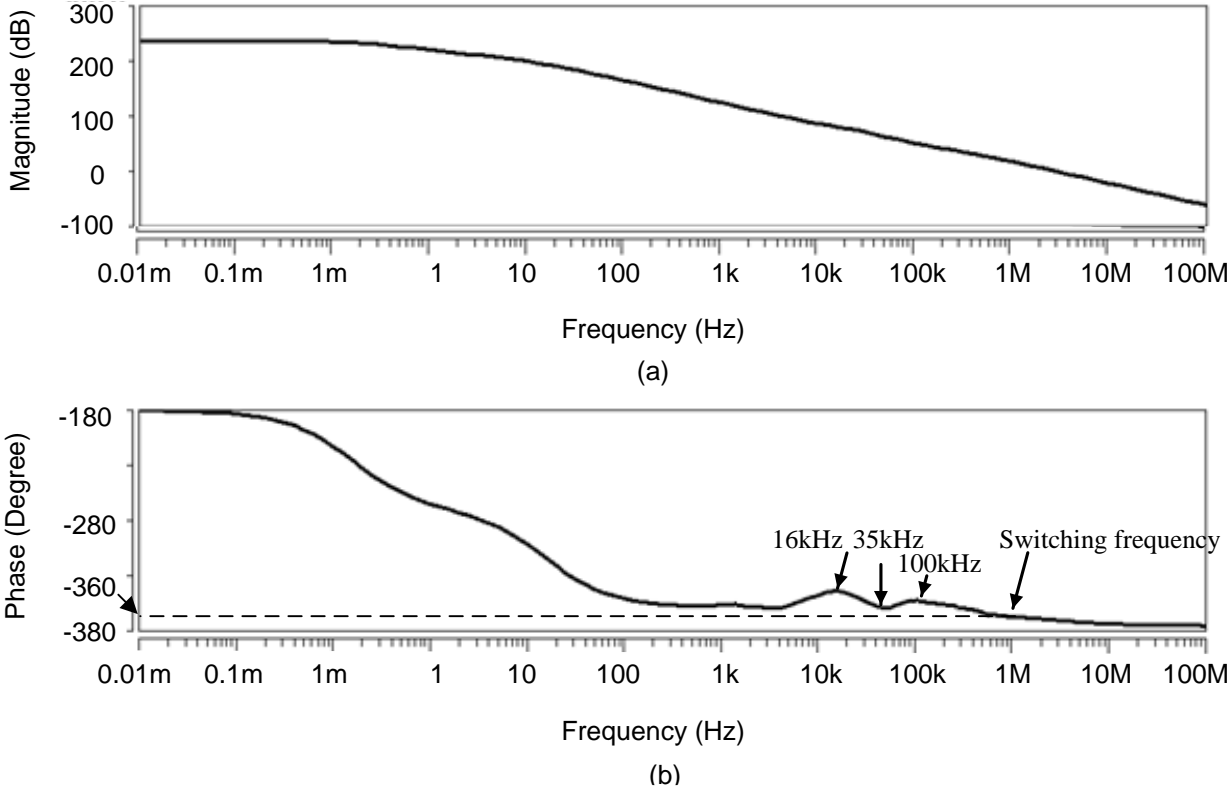


Figure 3.3 (a) Overall loop gain, $H_{Overall}$, and (b) phase shift, $\phi_{Overall}$

Figure 3.3 depicts the overall frequency response from simulations including loop gain and phase shift. The contributions of the various blocks to the loop gain and phase shift are also depicted; the contributions by the individual blocks are delineated in the next sections. The overall loop gain is a high $>200\text{dB}$ at DC and the switching frequency is designed at $\sim 1\text{MHz}$.

3.3.1 Modulator Design

The 2nd-order modulator consists of a 2nd-order integrator, control block and a comparator. These individual blocks are now delineated in turn.

3.3.1.1 2nd-order Integrator

The 2nd-order integrator design is a cascade two 1st-order lossy integrators as depicted in Figure 3.4. Functionally, it is an adder to sum the input signal and the feedback signal. It then integrates the summed signal with gain, and provides a lead-lag phase.

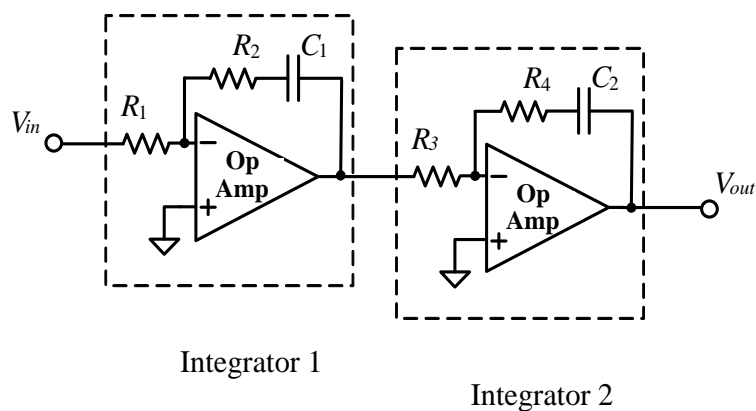


Figure 3.4 Schematic of the 2nd-order integrator

The frequency response of the proposed 2nd-order integrator is depicted in the Figure 3.5.

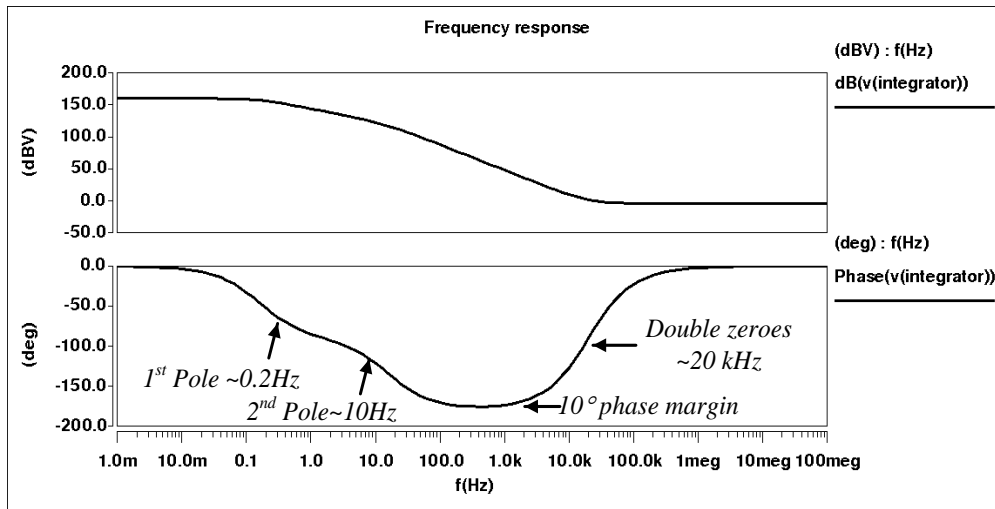


Figure 3.5 The frequency response of the 2nd-order integrator

There are two design considerations. First, to ensure that the original pole of the integrator does not affect the overall phase shift of the CDA, an additional zero at ~20 kHz is added instead of a single-pole integrator. Second, to avoid early oscillation with the addition of the phase lag from the propagation delay, a sufficient phase margin (10°) is designed within the audio band. The 2nd-order integrator is designed with two separate poles in the low frequency of the audio band to allow slower phase drop in the audio band and maintain a reasonable phase margin.

The transfer function of the 2nd-order integrator (without input from the output of the feedback network) is derived as

$$H_{Integrator} = \frac{1 + sR_2C_1}{sR_1C_1} \cdot \frac{1 + sR_4C_2}{sR_3C_2} \quad (3-3)$$

$$\phi_{Integrator} = \tan^{-1} \frac{1}{\omega C_1 R_2} + \tan^{-1} \frac{1}{\omega C_2 R_4} . \quad (3-4)$$

By means of adjusting the values of R_2C_1 and R_4C_2 , the zeroes of the first and second integrators are at $1/R_2C_1$ and $1/R_4C_2$ and are both ~ 20 kHz. The gain is largely determined by R_2R_4/R_1R_3 .

Note that different open loop gain of the amplifier could affect the overall loop gain of the CDA[80]. Thus, the operation amplifier is required to have open loop gain of at least 100dB and bandwidth of 20MHz to 30MHz. Usually a generic operational amplifier could provide required 100dB open loop gain and 20-30 MHz bandwidth.

3.3.1.2 Control Block

The control block is a phase lead-lag network (zero - pole) - network comprising only passive components depicted in Figure 3.6.

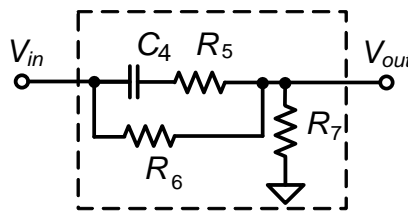


Figure 3.6 Schematic of control block

The frequency response of the proposed control block is depicted in Figure 3.7. This block serves to adjust the overall phase to tune the switching frequency.

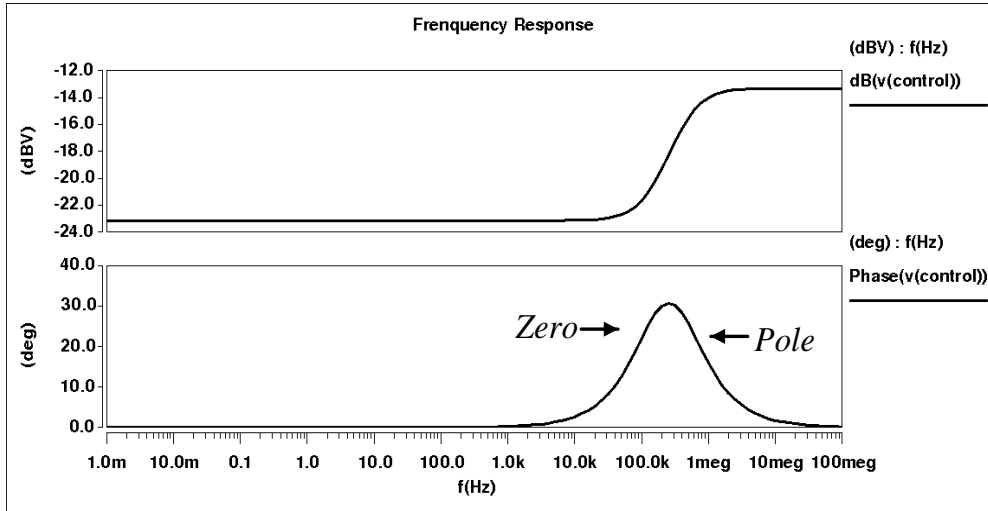


Figure 3.7 The frequency response of the control block

The transfer function of the control block is derived as

$$H_{Control_Block} = \frac{R_7(sR_5C_4 + sR_6C_4 + 1)}{sC_4(R_7R_6 + R_4R_5 + R_5R_6) + R_7 + R_5} \quad (3-5)$$

$$\phi_{Control_Block} = \tan^{-1} \frac{(R_5C_4 + R_6C_4)C_4(R_5R_7 + R_6R_7 - R_5R_6) + (R_5 + R_6)}{\omega(R_5C_4 + R_5C_2)(R_6 + R_7) - \omega C_4(R_5R_7 + R_6R_7 - R_4R_6)} \quad (3-6)$$

where the pole is determined by $(R_5+R_7)/C_4(R_7R_6+R_7R_5+R_5R_6)$ and zero is determined by $1/C_4(R_5+R_6)$.

The zero is designed to be near the cutoff frequency of the LC lowpass filter to avoid the total phase from reaching 360°. The zero is used to compensate the phase shift due to delay. The pole, on the other hand, is designed to be near the switching frequency.

The values of the passive components that determine the pole and zero are also derived above. If the value of R_6 and C_4 are increased or R_5 is decreased, the pole occurs at a lower frequency and the ensuing switching frequency is lowered.

3.3.1.3 Comparator

In the self-oscillating CDA, the comparator (depicted in Figure 3.8 as part of the CDA in Figure 3.2 and note that V_{ref} is usually applied as half of the voltage supply ($V_{DD}/2$)) provides some loop gain that contributes towards the (high) overall loop gain of the feedback. This loop gain of the comparator is significantly higher than that of the same comparator in the PWM CDA. This will now be shown.

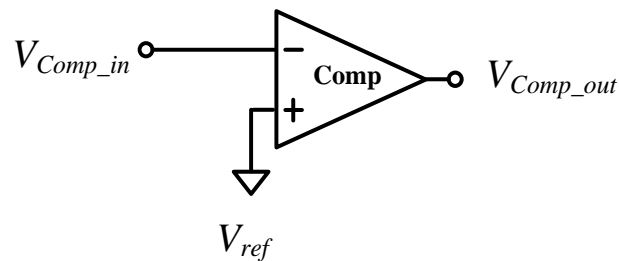


Figure 3.8 Schematic of the comparator

Figure 3.9 depicts the waveforms of the input (V_{comp_in}) and the output (V_{comp_out}) of the comparator. V_{comp_in} comprises the input modulating frequency component (audio band) and the carrier frequency component (~1MHz). In Figure 3.9, the audio frequency modulating input component is not apparent due to the depiction of only two cycles of waveforms of the

carrier component. For sake of illustration and ease of analysis, all signal waveforms are normalized with respect to V_{DD} .

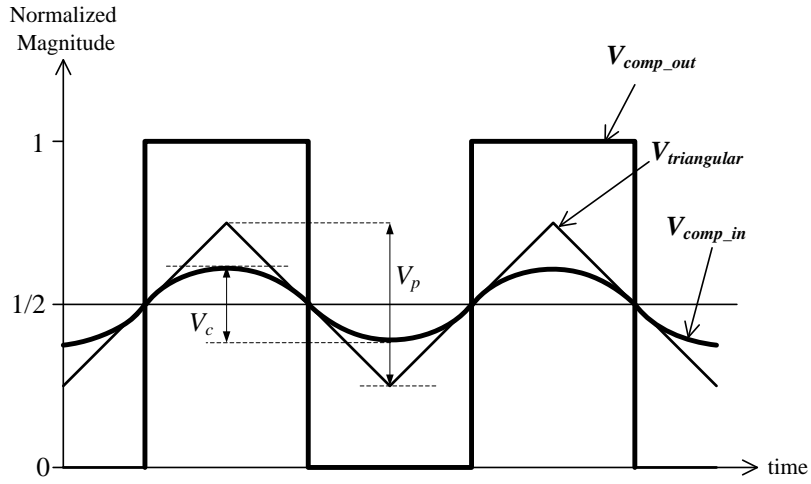


Figure 3.9 Waveforms of V_{comp_in} , V_{comp_out} and $V_{triangular}$

In Figure 3.9, V_{comp_in} is a quasi-sinusoid and a triangular carrier signal, $V_{triangular}$, can be constructed therefrom where it is tangential to V_{comp_in} at V_{ref} (which is equal to $V_{DD}/2$). V_c is the amplitude of the V_{comp_in} and V_p is the amplitude of the triangular wave.

As delineated in Chapter 2, in the linear model of the open loop PWM CDA, the pulse width modulator is assumed to be a constant gain stage and the gain is the ratio of the power supply V_{DD} to the amplitude of the triangular wave. In the proposed design, the gain of the combined comparator can also be estimated to be ratio of the amplitude of the square wave before the output filter (equals the supply voltage) to the amplitude of the triangle wave. The gain is expressed as

$$H_{Comparator} = \frac{V_{DD}}{V_p}. \quad (3-7)$$

In the proposed CDA, the reference waveform is the signal found at the comparator inputs V_{comp_in} as a result of the self-oscillation. Note that as the V_{comp_in} carrying the carrier information is not a conventional triangle waveform, the modulation becomes more nonlinear. For small signal use, V_{comp_in} can be approximated by $V_{triangular}$ that has the same slope at the zero crossings (i.e. is tangential). By trigonometry, the peak-to-peak voltage of $V_{triangular}$ is

$$V_p = \frac{\pi}{2} V_c . \quad (3-8)$$

where V_c is the peak-to-peak voltage of V_{comp_in}

Of the square wave produced by the power stage, only a fundamental is considered for simplicity. The amplitude at the comparator input becomes

$$V_c = \frac{4}{\pi} \left| H_{Integrator}(f_{sw}) \times H_{Control_Block}(f_{sw}) \times H_{Lowpass_Filter}(f_{sw}) \times H_{Feedback}(f_{sw}) \right| . \quad (3-9)$$

Hence, the loop gain of comparator is

$$\begin{aligned} H_{Comparator} &= \frac{V_{DD}}{V_p} = \frac{2}{\pi V_c} \\ &= \frac{1}{2 \left| H_{Integrator}(f_{sw}) \times H_{Control_Block}(f_{sw}) \times H_{Lowpass_Filter}(f_{sw}) \times H_{Feedback}(f_{sw}) \right|_c} \end{aligned} \quad (3-10)$$

It can be seen from equation (3-10) that $H_{Comparator}$ decreases as f_{sw} decreases so it is important to keep the switching frequency reasonably high; noting that $H_{Comparator}$ is a constituent part of the overall loop gain, necessary for reducing

nonlinearities due to negative feedback. At $f_{sw} = \sim 1\text{MHz}$, the comparator loop gain would reach a high value, $\sim -70\text{dB}$.

Note that in conventional PWM CDA, the comparator loop gain is typically 6-10dB [40] This is largely because the triangular carrier applied to the PWM CDA (V_p is $\sim V_{DD}/2$ or $V_{DD}/3$) has larger amplitude than the amplitude in self-oscillating CDA (V_p is in the range of tens of mV and $\ll V_{DD}$ (5V)). Thus, by applying equation 3-7, the comparator loop gain can be estimated and the loop gain of the PWM is generally much smaller (50-60dB) than that of the self-oscillating CDA.

3.3.2 Output Stage Design

As earlier delineated, in view of the 3-pin TRS or 4-pin TRRS connector of the audio device, the earphone/headphone amplifier therein would need to embody a single-ended output (BTL). Also delineated earlier, the single-ended configuration has poorer noise performance and less output power than the BTL configuration, and the former could be mitigated by the high loop gain of the feedback loop.

Chapter 2 earlier delineated that the output stage is designed as a chain of inverters. The aspect ratio of the transistors from the first inverter to the next inverter increases by ~ 10 times until the final inverter can provide the sufficient current drive to the load (32Ω). As the number of inverters in the inverter cascade is large (typically $> 8-10$), there is hence substantial propagation delay

introduced. The delay arising from the output stage can be expressed as the phase shift and is a linear function of f_{sw}

$$\phi_{Delay} = \Delta t \times 360^\circ \times f_{sw} \cdot \quad (3-11)$$

where Δt is the propagation delay, and

f_{sw} is the switching frequency.

Based on the author's experience and based on simulations of several output stage designs, the time delay is typically ~150ns. For simulations, the delay is emulated by inserting a RC network in between comparator and the output stage as depicted in Figure 3.10.

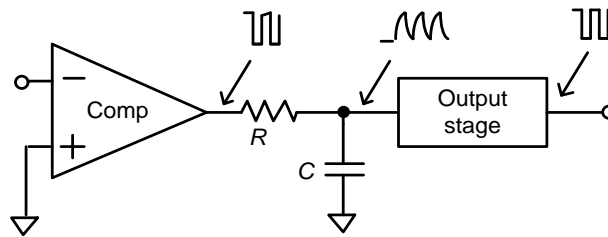


Figure 3.10 Model of output stage delay

3.3.3 LC Lowpass Filter Design

The LC lowpass filter serves to attenuate the carrier frequency signal from the output of the output stage and retrieve the amplified audio-band replica of the input signal to the load. Figure 3.11 depicts the LC_3 filter, ac coupling capacitor C_o and load (earphone/headphone transducer) R_L .

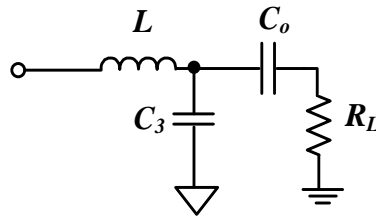


Figure 3.11 The schematic of the lowpass filter

The frequency response of the designed *LC* lowpass filter is depicted in Figure 3.12 where the cutoff frequency is designed to be ~25kHz (slightly above the audio frequency band). In terms of the phase, the lowpass filter, being 2nd-order, contributes approximately 180° phase lag after the cutoff frequency.

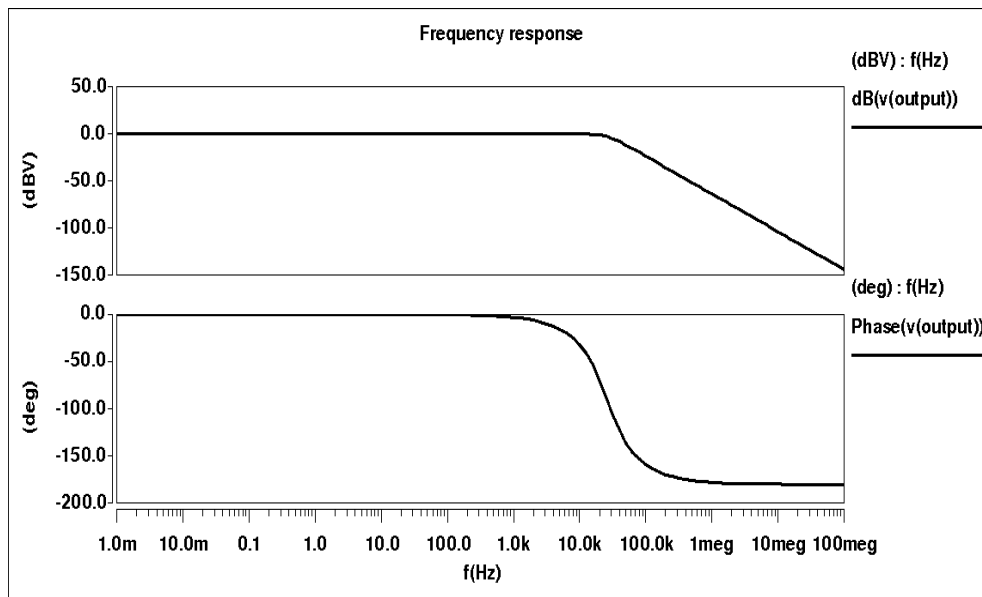


Figure 3.12 The frequency response of the *LC* lowpass filter

The transfer function of the 2nd-order *LC* lowpass filter without a load is expressed as

$$H_{Lowpass_Filter} = \frac{1}{1 + s^2 LC_3} \quad (3-12)$$

For completeness, the damping factor Q is also considered due to the combination of L , C_3 and load R_L , and Q is generally recommended to be within 0.6-0.8. It is easy to show that the damping factor can be expressed as

$$Q = R_L \sqrt{\frac{C_3}{2L}}. \quad (3-13)$$

To ensure the aforesaid Q for a given earphone/headphone load, the value of L and C_3 can hence be ascertained.

The transfer function of the 2nd-order LC filter with load is

$$H_{Lowpass_Filter} = \frac{R_L + sC_3}{s^2 LC_3 + sC_3 + R_L}. \quad (3-14)$$

$$\phi_{Lowpass_Filter} = \tan^{-1} \frac{R_L^2 - C_3}{\omega(2R_L - \omega^2 LC_3)}. \quad (3-15)$$

For the reasons delineated earlier, we choose the cutoff frequency of the LC filter ($L = 200\mu\text{H}$, $C = 0.2\mu\text{F}$) to be ~ 25 kHz and the damping factor ~ 0.7 .

The feedback circuit is implemented with a single resistor, R_f , which is the same value as $R_1 = 10\text{k}\Omega$. The closed-loop gain of the proposed CDA is designed to be 0dB.

3.4 Proposed Design: Discussions

On the basis of the aforesaid analyses and derivations (equations (3-2) to (3-15)), the proposed self-oscillating CDA with complete feedback offers two highly desirable attributes: lower nonlinearities and high load invariance; these

attributes will be benchmarked against reported designs later. Nevertheless, as in most engineering solutions, designs that offer generally improved attributes may compromise other specific characteristics and/or introduce new shortcomings. The proposed design has three limitations: high switching frequency, possibly high sensitivity to components variations and more components counts. The advantages and the disadvantages will now be delineated in turn.

3.4.1 Merits of the Proposed Design

As mentioned previously, the two main advantages of the proposed design are low nonlinearities and high load invariance and they will now be delineated in turn.

(i) Low Nonlinearities

The nonlinearities of the proposed self-oscillating CDA are low largely because of its high overall loop gain provided in the modulator (due to the integrator and the comparator). As delineated earlier, the high loop gain of the comparator (when the switching frequency is properly designed to be sufficiently high) has significant contribution to the overall loop gain of the self-oscillating CDA – the comparator loop gain is designed to $\sim 70\text{dB}$ and is substantially higher than the loop gain (typically $< 10\text{dB}$) of the comparator in typical PWM CDAs.

Due to the high loop gain, noise is commensurably heavily attenuated (by $(1+\text{Loop Gain})$) due the feedback mechanism. Noise attenuation will now be delineated based on the linear model of the proposed CDA depicted in Figure 3.13.

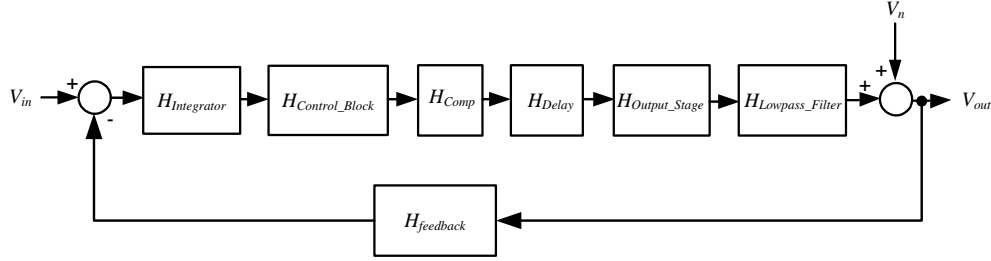


Figure 3.13 Linear model of the proposed CDA

Based on the linear model of the proposed CDA, the transfer function of the noise from the output stage and the lowpass filter could be expressed as

$$H_n = \frac{V_{out_n}}{V_n} = \frac{1}{H_{Overall} + 1} \quad (3-16)$$

where $H_{Overall} = H_{Integrator} \times H_{Control_Block} \times H_{Comp} \times H_{Delay} \times H_{Output_Stage} \times H_{Feedback}$, which is the same as equation (3-2), V_n is the noise from the output stage and lowpass filter, and V_{out_n} is the output signal when $V_{in} = 0$.

As expected, the noise is attenuated by a factor of $(1+\text{Loop Gain})$ (where $\text{Loop Gain} = H_{Overall}$). For the proposed CDA, the noise attenuation as a function of frequency is depicted in Figure 3.14. Of specific interest, the low frequency noise as desired is heavily attenuated, and most noise is

pushed (shaped) to the frequency range beyond the audio band, hence, high-fidelity (see benchmarking later).

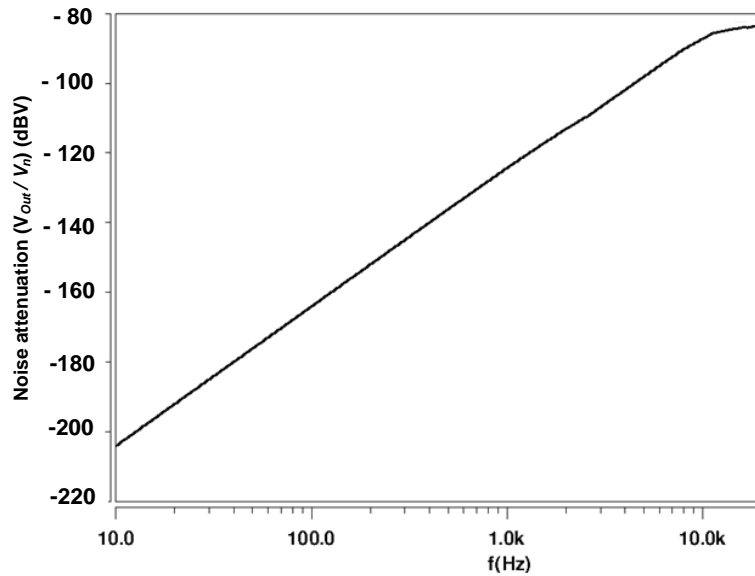


Figure 3.14 Noise attenuation of the proposed design

For completeness, note that in the audio band, H_{Delay} , H_{Output_Stage} and $H_{Feedback}$ are unity and are not the main contributors to the overall loop gain, the desirable high loop gain here is largely due to a high switching frequency (hence a high H_{Comp}) and a high $H_{Integrator}$.

(ii) High Load Invariance

As delineated in Chapter 2, the proposed design with complete feedback offer increased circuit immunity to the load variations as the LC lowpass filter is a constituent part of the feedback. Figure 3.15 depicts the overall loop gain ($H_{Overall}$) and the closed-loop gain ($H_{Closed-loop}$) of the self-oscillating designed CDA at both conditions of no-load and 32Ω -load.

It can be seen that for $H_{Overall}$, the load variance is very large for the condition without load ($H_{Overall}$ without load) to the condition with load ($H_{Overall}$ with resistive load). Conversely, the load variance for $H_{Closed-loop}$ is substantially smaller for the condition without load ($H_{Closed-loop}$ without load) to the condition with load ($H_{Closed-loop}$ with resistive load).

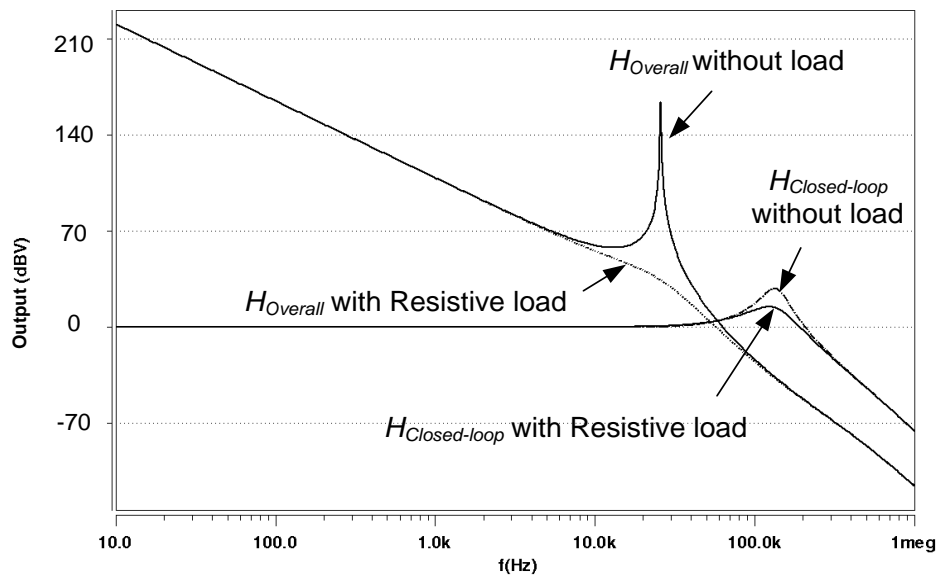


Figure 3.15 Overall loop gain and closed-loop gain of the proposed CDA

The reduced load variance attribute is practically useful. With the added impedance from the feedback network, the total effective output impedance is reduced (R_L) and a smaller inductance could be used to achieve the same damping factor (see equation 3-13). A smaller inductance is preferred in the target application in earphone/headphone amplifiers due to the reduction of the inductor size and the cost arising from it. Thus, the load invariance enables the circuit to be less sensitive to the resistive load damping.

In summary, the two desirable attributes (low nonlinearities and high load invariance) of the proposed self-oscillating CDA design render the proposed design appropriate for high-fidelity earphone/headphone amplifiers. The two attributes are also arising from the complete feedback configuration which enables the nonlinearities from *LC* filter to be attenuated by the feedback mechanism and the proposed design is insensitive to the resistive load damping.

3.4.2 Shortcomings of the Proposed Design

In many engineering designs, improving certain parameters of a given design typically involves compromises to other parameters of said design. In the proposed design, the high-fidelity is achieved with three compromises. In the author's view, the compromises are slightly disadvantageous and not dilapidating. Specifically, the compromises are the higher switching frequency, possibly higher sensitivity to components variations and higher component count – these are with respect to PWM CDAs (with incomplete feedback). They will now be delineated in turn.

(i) Switching Frequency

The proposed CDA was designed with a switching frequency of ~1MHz (at zero-input) to meet the high-fidelity requirements of earphone/headphone amplifiers. From the perspective of CDA

architectures based on the self-oscillation approach, this frequency is typical and, the proposed design is hence not disadvantageous. However, when compared to the more ubiquitous PWM approach, this switching frequency is relatively high (e.g. PWM CDAs typically have switching frequencies in the range of ~350 kHz to 500 kHz as delineated in Chapter 2). Higher fidelity PWM CDAs typically have higher switching frequencies.

The shortcoming of this higher switching frequency translates to higher switching loss in the output stage of the CDA (see equation (2-7)) and consequently lower power efficiency. Practically, the shortcoming is somewhat mitigated because the switching frequency of self-oscillation CDAs, including the proposed CDA, is a function of modulation index – the higher the modulation index, the lower the switching frequency. At nominal modulation index of $M = 0.1$, the switching frequency ranges from 700 kHz – 1MHz; the nominal modulation index is $M = 0.15$ is to allow ~16dB headroom for signal swing and accounting for the crest factor of music. In view of the higher fidelity PWM CDAs typically having higher switching frequencies, the difference in the switching frequency is hence not large.

Not unexpectedly, in part due to the other attributes of the proposed CDA for low power operation, it can be seen from the benchmarking

in Table 3.3 the proposed CDA features amongst the best power efficiency for reasons already delineated.

(ii) Variations of Components

The proposed design is based on the self-oscillating approach and in the author's view, without proof (and the author's anecdote), this configuration is more prone to the variations of the embodied components than the conventional PWM CDA. This is because, as delineated in Chapter 2, the conditions for self-oscillation of the former is ascertained by the phase shift (contributed from all blocks in the feedback loop) vis-à-vis a predetermined carrier frequency generated externally in the latter. As there are a number of blocks (in the feedback loop) whose transfer function is determined by the specific values of the passive components therein, the phase shift is hence a function of values of these passive components – see equations (3-4), (3-6), (3-11), (3-15)). Consequently, we conjecture that the oscillation/switching frequency of the proposed CDA is more sensitive to the variations of the components; note that all CDAs based on the self-oscillation architecture would likewise suffer the same.

In the highly unlikely worst case, the overall phase deviates so excessively from the nominal values such that there is no oscillation. We recommended that the variation of the components purchased in discrete realization is within 1% to minimize the variations of the

switching frequency instead of the more general 5% - 10%. In Section 4.2, we suggest an investigation to mitigate this sensitivity.

(ii) Component Count

The proposed design requires eleven passive components, comprising eight resistors and three capacitors (excluded the L and C of the LC lowpass filter). From the perspective of a CDA architecture based on the self-oscillation approach with complete feedback, this component count is typical and in this sense, the proposed design is not disadvantageous. However, when compared to the more ubiquitous PWM with incomplete feedback, the component count in the proposed design is almost doubled. For example, the passive component count is five in the 2nd-order PWM CDA [81] without accounting for the components in the carrier generator therein.

In the discrete implementation, the higher component count translates to higher cost and large PCB area. However, in monolithic realization which is the case if the proposed design were to be practically realized, some of these passive components (excluding the large valued capacitors, e.g. >100pF) can be realized monolithically on-chip, thereby reducing the external passive component count.

This shortcoming will be further discussed in Section 4.2.

In summary, this proposed self-oscillating CDA is appropriate for high-fidelity earphone/headphone applications due to the low nonlinearities arising from

the high loop gain. In addition, the proposed design is insensitive to resistive load damping due to the complete feedback configuration. The shortcomings of the proposed design are slightly disadvantageous and not dilapidating - a slightly higher switching frequency, higher sensitivity to the component variations and higher passive component count.

3.5 Results and Discussion

In this section, the design and the ensuing attributes of the proposed high-fidelity 2nd-order CDA based on self-oscillation with complete feedback for earphone/headphone applications are verified by means of simulations and physical measurements.

The proposed design is simulated using HSPICE and based on a commercial CMOS process, the Austria Micro Systems 0.35 μ m process, AMS035. The physical measurements, on the other hand, are based on measurements on the same CDA design realized on a vero board using discrete components. These physical measurements are obtained using an oscilloscope for obtaining time-domain responses and the *Briel & Kjaer* PULSE Analyzer (Fast Fourier Transform (FFT) analysis) to obtain parameters pertaining to fidelity, including SNR, THD+N, PSRR PS-IMD, and IMD.

The proposed CDA with the designed passive component values is depicted in Figure 16; for ease of readability, these component values are also tabulated in the Table 3.1 below. The overall loop gain $H_{Overall}$ and phase shift $\phi_{Overall}$

depicted previously in Figure 3 were obtained from this design. The tolerance level of the component values are 1%.

Table 3.1 Selected passive component values

R_1	10k Ω	R_6	1.5k Ω	C_2	1nF
R_2	8k Ω	R_7	0.3k Ω	C_3	0.2 μ F
R_3	10k Ω	R_f	10 k Ω	C_4	0.2nF
R_4	8k Ω	R_L	32 Ω	L	200 μ H
R_5	4k Ω	C_1	1nF		

The proposed CDA constructed on the vero board is depicted in Figure 3.17. General purpose op-amps [82] and a comparator [83] are employed in the design and a commercially output stage IC [84] is employed for the output stage switching at ~1MHz. The inductor employed is a relative cheap inductor, the Maruka Power Solutions 1300R Series [85] inductor whose nonlinearities (THD+N) estimated to be ~0.05% [15].

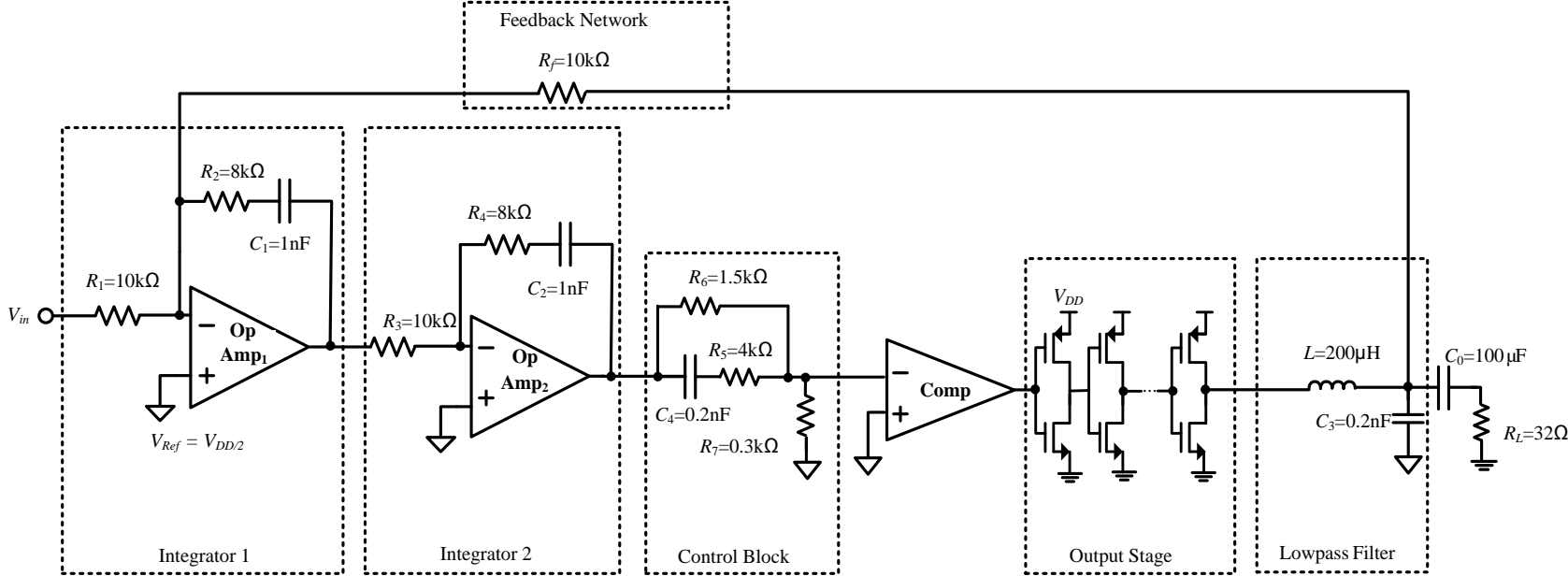


Figure 3.16 The complete design (with passive component values) of the proposed CDA

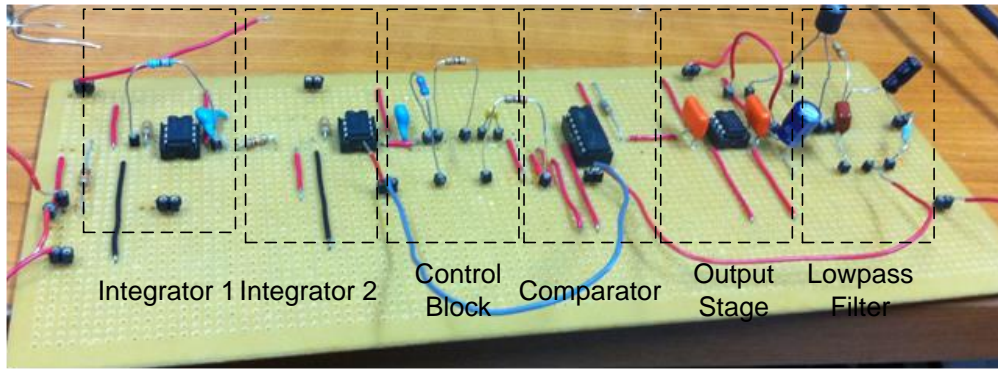


Figure 3.17 The proposed CDA built on the vero board

Figure 3.18 depicts the test setup of proposed CDA and the equipment used.

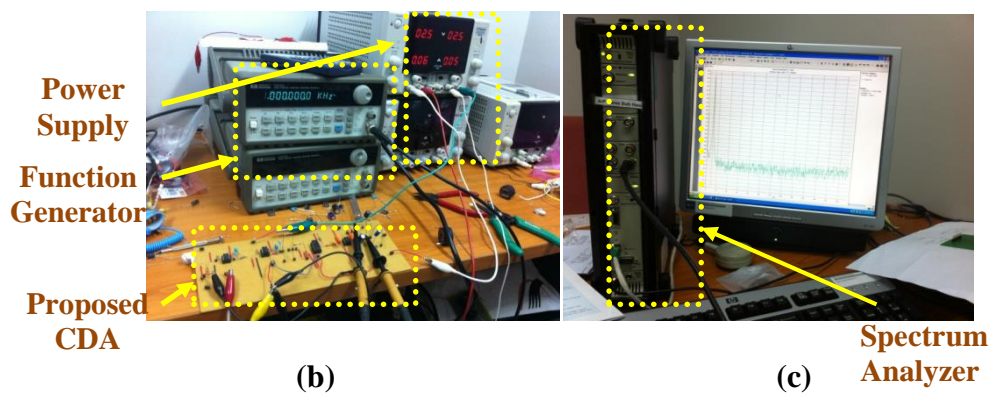
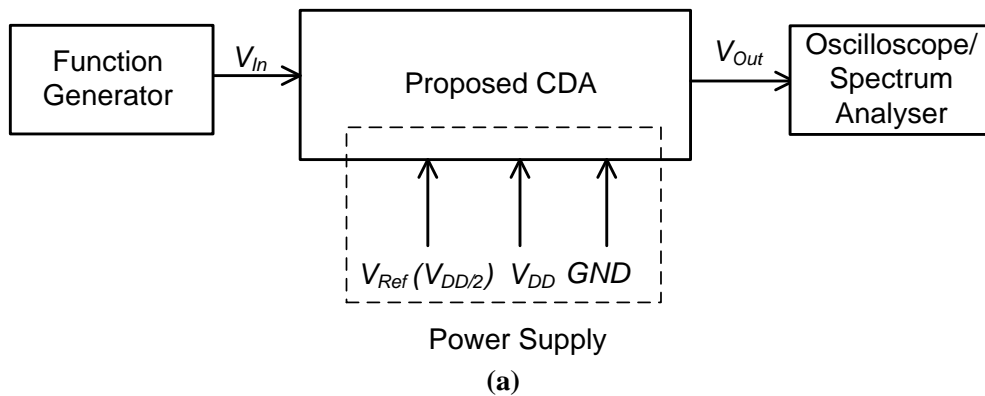
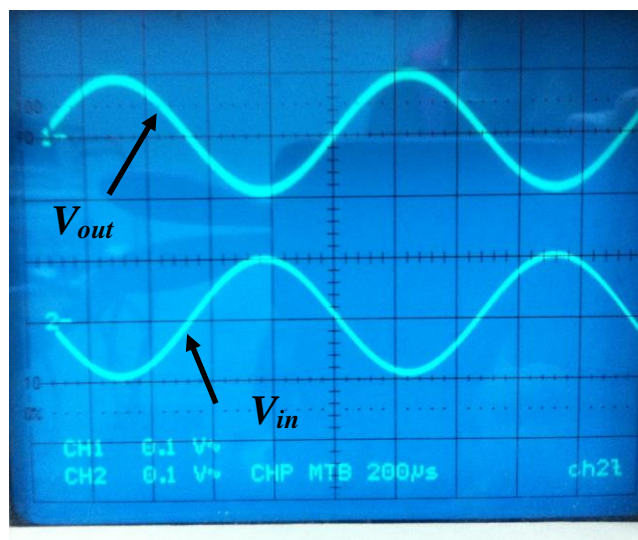
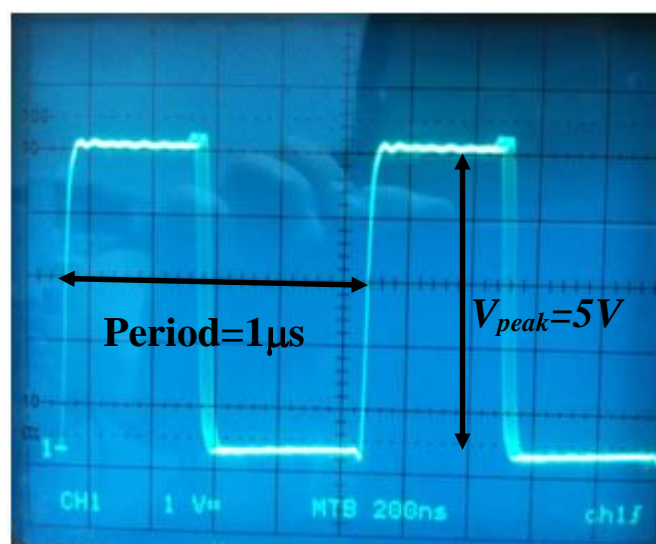


Figure 3.18 Test setup for the proposed CDA: (a) Schematic, (b) Power Supply, Function Generator and Proposed CDA, and (c) Spectrum Analyzer

The measured input and output waveforms of the proposed CDA are shown in the Figure 3.19(a). As expected, the output is a sinusoidal wave with opposite phase and of equal magnitude to the input sine. In Figure 3.19(a), the output waveform at the output of the output stage at zero-input ($M = 0.1$) is shown. As expected, the switching output switches at 1 MHz (period is $1\mu\text{s}$).



(a)



(b)

Figure 3.19 (a) Input waveform and output waveforms at the output of the LC lowpass filter (b) Output waveform at the output of the output stage (input of the LC lowpass filter)

Table 3.2 tabulates the overall performance of the proposed CDA, with the major parameters specified and that obtained from simulations and from physical measurements.

Table 3.2 Performance of the proposed CDA

Parameter	Specifications	Simulated	Measured
Supply Voltage, V_{DD}	5V	5V	5V
Maximum Modulation Index, M_{max}	0.9	0.9	0.9
THD+N @ $P_{out}=1\text{mW}$, 1kHz	<0.01%	0.0082%	0.009%
THD+N @ $P_{out}=1\text{mW}$, 6kHz	<0.01%	0.008%	0.0083%
PSRR (20 Hz – 20 kHz)	>70dB	≥73dB	≥73dB
PSRR@217Hz	>70dB	106dB	100dB
SNR	> 90dB	102dB	97dB
IMD	-	≤0.4%	≤0.5%
PS-IMD	-	≥90dB	≥80dB
Power efficiency, η	>90%	91% @ M_{max} *	90% @ M_{max} *
Maximum Output Power	≤100mW	80mW	80mW

* The power efficiency largely depends on the components selected (op amps and comparators –see section 3.5.2 later.

It can be seen that the parameters obtained by simulations agree with that obtained experimentally. Further, the proposed design meets all

specifications and is high-fidelity, hence appropriate for an ear phone/headphone application. Put simply, the simulation/measurement results verify that the proposed design is highly competitive to the fidelity performance of the linear amplifiers: high SNR >90dB, low THD+N <0.01% and high PSRR >70dB, and yet exhibit high power efficiency $\eta = 90\%$ @ $M = 0.9$.

3.5.1 Fidelity

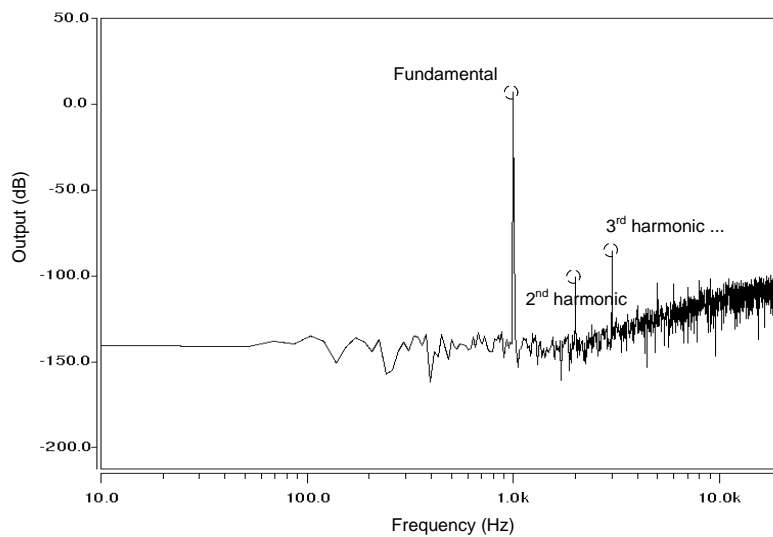
The fidelity parameters of the proposed CDA including SNR, THD+N, PSRR, PS-IMD and IMD, will be delineated in turn. Following that, the proposed design is benchmarked against the state-of-the-art linear amplifiers and with reported CDAs for earphone/headphones.

3.5.1.1 SNR

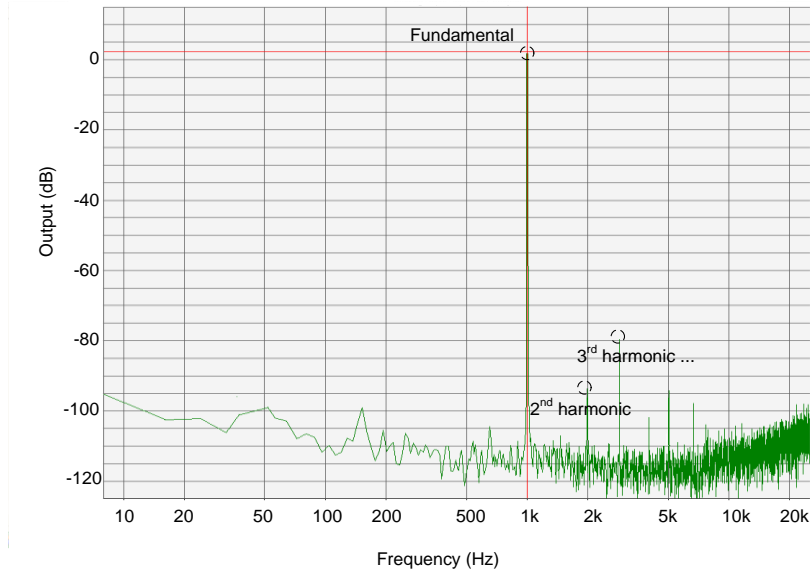
SNR was previously defined in equation (2-3), a ratio of the maximum output signal relative to the floor noise level at zero-input. The test setup is the same as that depicted in Figure 3.18. The SNR of the proposed design is simulated/measured in 3 steps.

- (i) The maximum output signal (V_{max}) is obtained where $M = 0.9$ for 32Ω load and the input is (typically) set at 1 kHz. The simulated and measured FFT plots of the output at the *LC* lowpass filter are performed and are shown for references (depicted in Figure 3.20). The maximum output signal determined as ~7dB (2.25V).

- (ii) The noise voltage (V_n) is obtained by performing the FFT analysis at the output at the LC lowpass filter with zero input signal where $M = 0$. The spectrum output data is imported to Excel to calculate the RMS value of the integrated noise floor in the audio bandwidth (20 Hz-20 kHz): $\sim 18\mu\text{V}$ (simulated) and $\sim 30\mu\text{V}$ (measured). The difference is expected because the practical noise floor in the measurement environment is higher than that in the simulation environment.
- (iii) The signal voltages (V_{max}) and the noise voltages (V_n) are substituted to equation (2-3), and the SNR is obtained. The SNR as the ratio between V_{max} and V_n is calculated as 102dB (simulated) and 97dB (measured).



(a)



(b)

Figure 3.20 FFT plot of the output of the *LC* lowpass filter at 1 kHz input and $M = 0.9$: (a) Simulated (b) Measured

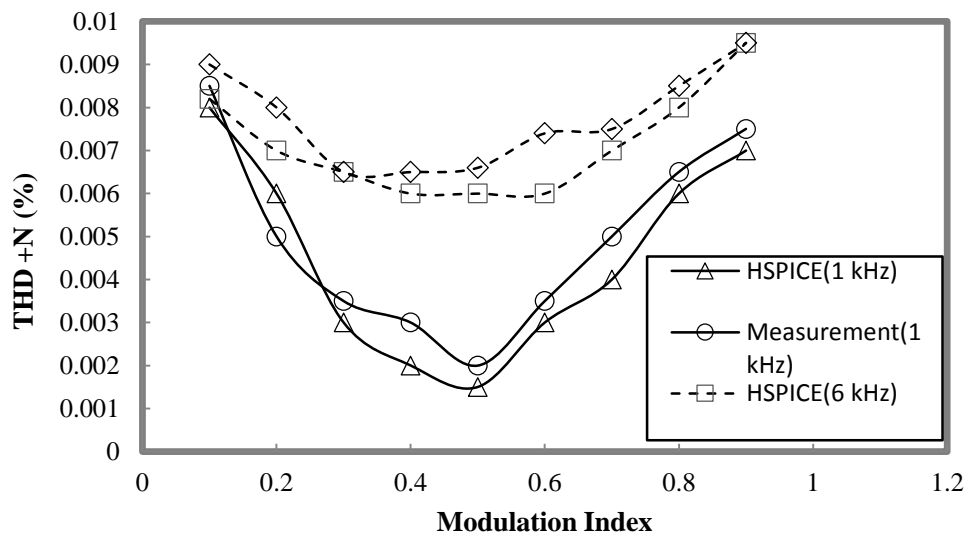
The simulated/measured SNR could satisfy the requirements for the high-fidelity earphone/headphone amplifiers ($\text{SNR} > 90\text{dB}$). In our proposed CDA, the high SNR is achieved due to the large loop gain (see Figure 3.3 and Figure 3.14) designed to attenuate the noise floor.

3.5.1.2 THD+N

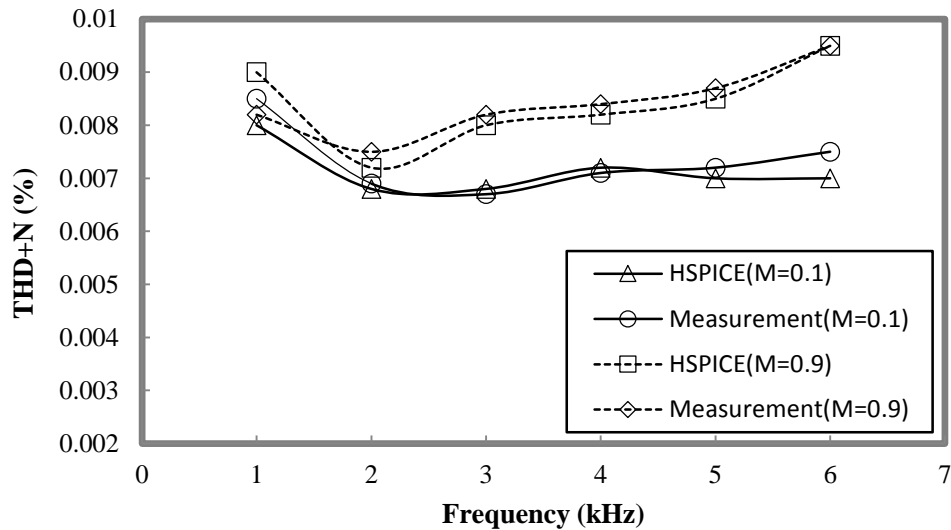
THD+N was previously defined in equation (2-4) in Chapter 2, and is a classical measure of fidelity. Generally, CDAs reported in literature (and in data sheets) quote THD+N only at 1 kHz. However, research from our research group has previously shown that measurement at this single frequency measurement is insufficient as THD+N is a function of frequency (and a function of modulation index) - the worst case being at $f_{in} = 6$ kHz [35]. Consequently, the THD+N measurement here will include $f_{in} = 1$ kHz and 6

kHz. For earphone/headphone amplifiers, the nominal output power $P_{out} = 1\text{mW}$ ($M = 0.1$) at 1 kHz is generally specified. For completeness, the THD+N will also be measured at maximum power - $P=80\text{mW}$ ($M = 0.9$).

The test setup is the same as that depicted in Figure 3.18. The THD+N of the proposed design is characterized in Figure 3.21(a) with respect to entire range of modulation indexes and at $f_{in} = 1\text{ kHz}$ and $f_{in} = 6\text{ kHz}$. For completeness, the THD+N of the proposed CDA is also plotted in Figure 3.21 (b) as a function of the input frequency, f_{in} , for $M = 0.1(1\text{mW})$ and $0.9 (80\text{mW})$. Note that the THD+N beyond 6 kHz is of little interest as the THD+N is very low because their 2nd or 3rd harmonics (and beyond) are out of the audio band.



(a)



(b)

Figure 3.21 (a) THD+N against modulation index for the proposed CDA and, (b) THD+N against the input frequency

The following observations and remarks are made:

- (i) In Figure 3.21(a), the THD+N in the proposed design satisfies the fidelity requirement for earphone/headphone amplifiers (THD+N < 0.01%). Specifically, the THD+N < 0.01% over the entire modulation indexes for $f_{in}=1$ kHz (conventional measure), and for $f_{in}=6$ kHz (worst-case).
- (ii) The worst-case THD+N in observation (i) above is corroborated in Figure 3.21(b) where for maximum modulation, the worst-case THD+N is for $f_{in}=6$ kHz. As delineated earlier, this measurement point is interesting as the THD+N of CDAs are typically quoted only for $f_{in}=1$ kHz, and this can be misleading in the sense that it is optimistic. We

attribute the increased THD+N at higher frequencies to the reduced loop gain, see Figure 3.3.

- (iii) For $f_{in}=1$ kHz, at low modulation indexes ($M < 0.5$), the THD+N reduces as the modulation index increases. This is because at low modulation indexes, the signal to noise ratio is small and as the signal level increases, this ratio rises until $M = 0.5$. This observation is also noted for $f_{in}=6$ kHz, as expected. It is likely that the noise dominant rather than harmonic distortion.
- (iv) For $f_{in}=1$ kHz, at higher modulation indexes ($0.5 \leq M \leq 0.9$), the THD+N increases with modulation index. This is the same phenomenon observed in typical audio amplifiers. In this modulation index range, the dominant mechanism of the THD+N is harmonic distortion. This is corroborated from the FFT analysis depicted in Figure 3.20 where the 3rd harmonic is, as expected, the dominant harmonic distortion.
- (v) The THD+N from the perspective of Figure 3.21(b) also depicts, as expected, that the THD+N is more severe for $M = 0.9$ than for $M = 0.1$ for the pertinent frequency ranges. For $M = 0.9$, the worst-case THD+N is, as delineated earlier, for $f_{in}=6$ kHz; note again that THD+N is typically quoted for $f_{in}=1$ kHz, and this value is perhaps somewhat optimistic. Nevertheless, for $M = 0.1$, the worst-case THD+N is for $M = 0.1$ and the dominant mechanism is likely the floor noise as delineated earlier.

3.5.1.3 PSRR

PSRR is a critical parameter in the mobile phone applications because the power supply noise may be introduced from the DC-DC conversion process, from the digital circuits therein, or from EMI. Further, in the case of cellular phones, significant 217Hz GSM burst noise is also introduced in to the power supply.

PSRR was previously defined in equation (2-5), a ratio of the power supply noise at the supply rail to the power supply noise appearing at the load at the frequency of the power supply noise. In this section, PSRR will be characterized from low frequency (100 Hz) to high frequency (up to 20 kHz), hence including the important 217Hz burst noise frequency.

The testing setup for PSRR is depicted in Figure 3.22. The simulation and measurement of PSRR are performed by augmenting a frequency swept ac sinusoidal noise signal (v_n) whose amplitude is 0.25mV ($N = 0.1$, N is normalized amplitude of the injected noise signal with respect to $V_{DD/2}$) to the V_{DD} (5V) power supply rail. The input is zero-input.

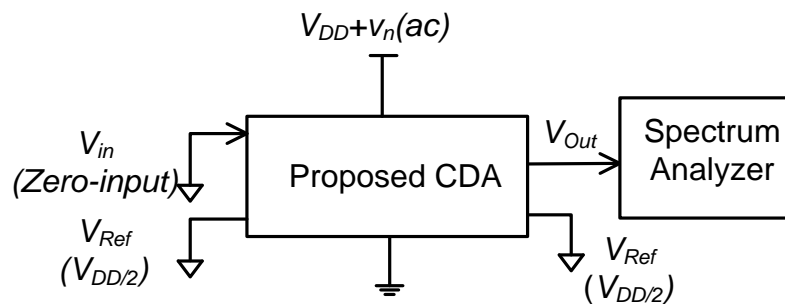


Figure 3.22 The PSRR testing setup

Figure 3.23 depicts the simulated and measured PSRR of the proposed CDA against the supply noise frequency (100 Hz – 20 kHz).

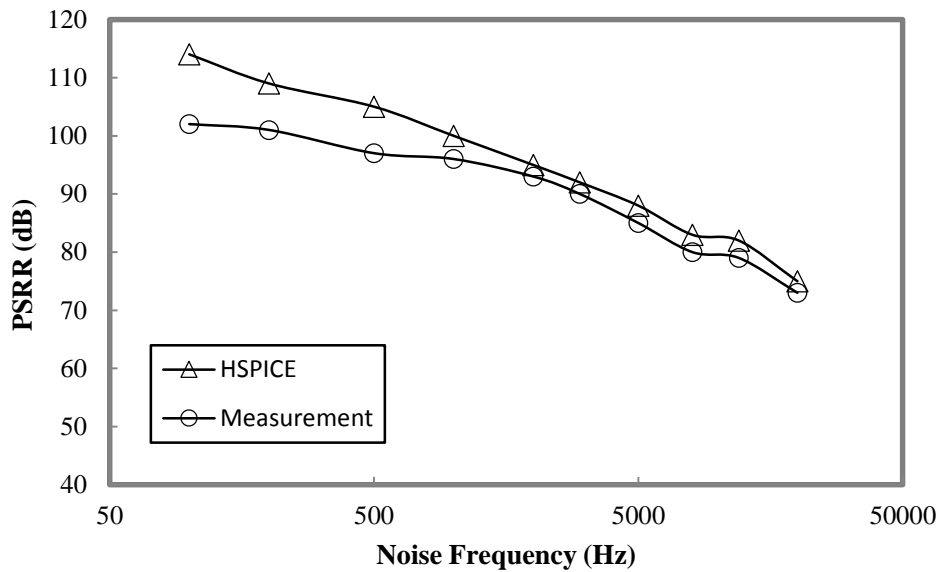


Figure 3.23 PSRR of the proposed design

On the basis of Figure 3.23 the following observations and remarks are made:

- (i) The PSRR across the supply noise frequency range (within audio band) in the proposed design satisfies the fidelity requirements for earphone/headphone amplifiers (PSRR >70dB). Specifically, the worst-case PSRR in both simulations and measurements is ~73dB at 20 kHz.
- (ii) The PSRR of the proposed CDA decreases as the supply noise frequency increases. That is expected as the attenuation of the supply noise largely depends on the loop gain (equation (3-14)) and the loop gain is a function of frequency (Figure 3.14) where the loop gain reduces as frequency increases.

- (iii) In the low noise frequency range ($f_n < 1$ kHz), the PSRR obtained from the measurement is lower than that obtained from simulations (by ~ 10 dB). This is probably due to the higher noise floor in the measurement environment. In the higher noise frequency range ($1 \text{ kHz} \leq f_n \leq 20 \text{ kHz}$), the PSRR from simulations and measurements agree well.

- (iv) The PSRR@217Hz obtained from simulations and experimentally is 106dB and 100dB respectively. This high PSRR is highly desirable in a GSM mobile phone application.

3.5.1.4 PS-IMD

Another parameter, PS-IMD, to qualify power supply noise is also characterized – it was already delineated in Chapter 2. Generally, CDAs reported in literature (and in data sheets) only report PSRR to qualify their immunity to power supply noise. However, our research group has previously shown that there are nonlinearities arising from the intermodulation between the power supply noise and the input signal, qualified by PS-IMD. The PS-IMD here will be characterized for the condition: at $f_{in} = 1$ kHz and $f_n = 217$ Hz, this frequency of f_n is arguably the most pertinent point for GSM mobile phones (GSM burst noise).

Our research group previously showed that the dominant PS-IMD component is the 2nd-order PS-IMD. This refers to the PS-IMD whose components are at

$f_{in} \pm f_n$. The higher-order PS-IMD is usually non-dominant, referring to PS-IMD whose components are $f_{in} \pm nf_n$, where $n=2, 3 \dots \infty$.

Figure 3.24 depicts the test setup for PS-IMD. Similar to the PSRR test setup, a noise signal, V_n , is applied to supply rail of the proposed CDA. However, unlike the PSRR test setup, the input is at maximum signal swing ($M=0.9$).

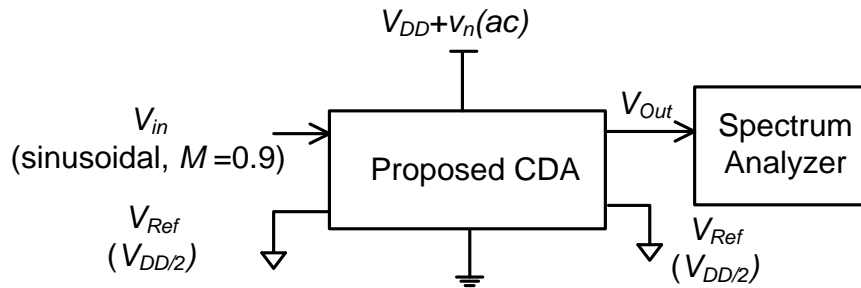


Figure 3.24 The PS-IMD testing setup

Figure 3.25 depicts the FFT plot of the PS-IMS obtained experimentally for $f_n = 217\text{Hz}$, $N = 0.1$, $f_{in} = 1\text{ kHz}$ and $M = 0.9$.

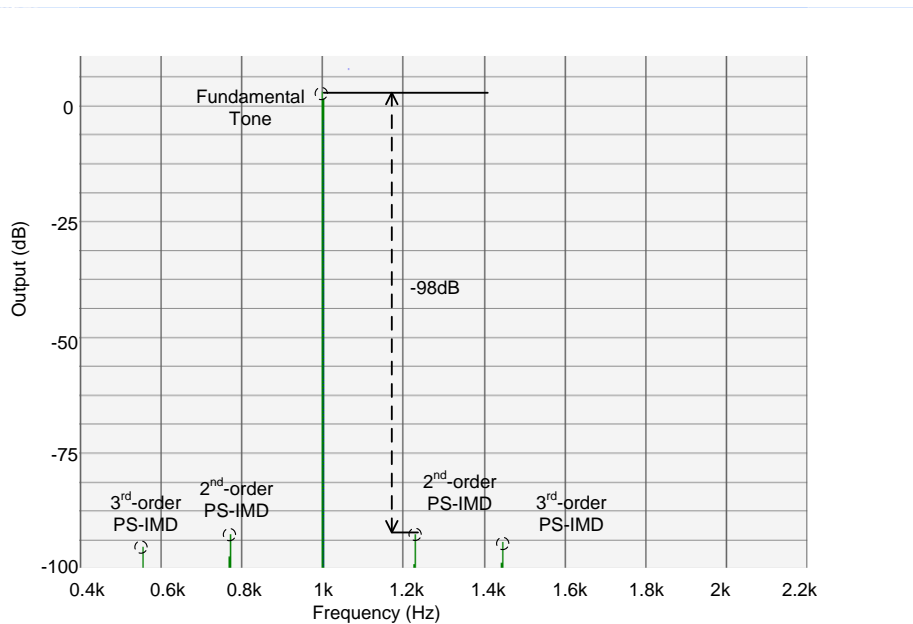


Figure 3.25 Measured PS-IMD of the proposed CDA. Conditions:

$$f_n = 217\text{Hz}, N = 0.1, f_{in} = 1\text{kHz} \text{ and } M = 0.9.$$

On the basis of Figure 3.25, the following observations and remarks are made:

- (i) The difference between the 2nd-order PS-IMD (at 783 Hz and 1217 Hz) and the fundamental (at 1 kHz) is approximately 98 dB. As this PS-IMD is low, the intermodulation products contribute very little nonlinearities to the proposed CDA.
- (ii) As expected, the 3rd-order PS-IMD is less significant than the 2nd-order PS-IMD and the higher order PS-IMD components are even lower. They are inconsequential.

3.5.1.4 IMD

As delineated in Chapter 2, IMD is another well accepted measure of fidelity, and arises from the intermodulation between two or more frequency components of the input signal. This was defined in equation (2-6).

Figure 3.26 depicts the test setup for ascertaining IMD. It consists of two input sources V_1 ($f_1 = 60$ Hz) and V_2 ($f_2 = 7$ kHz) and $M_1 = 4M_2$.

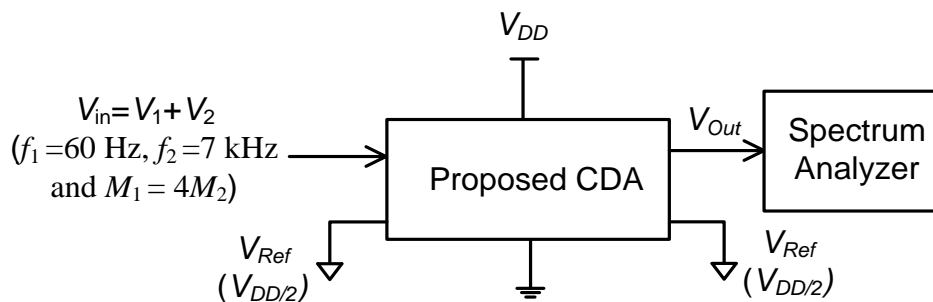
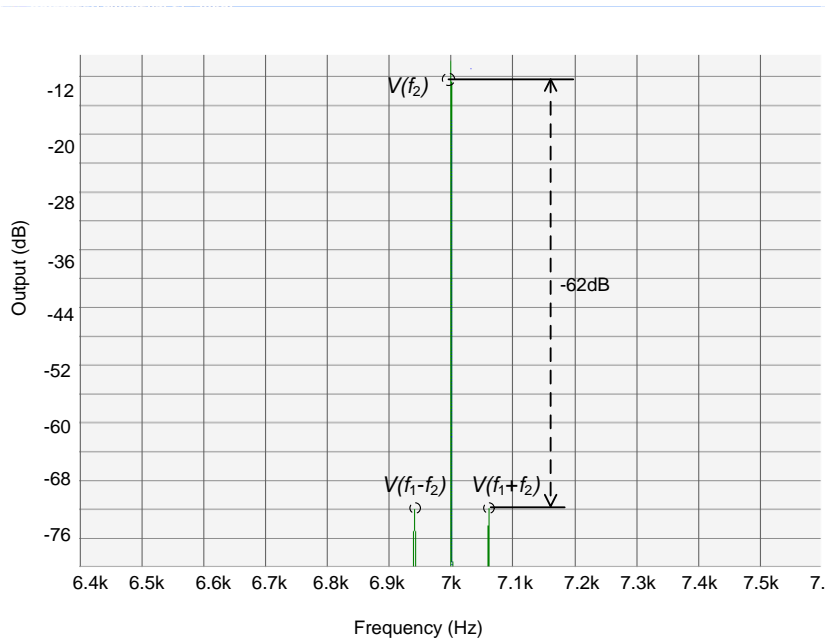
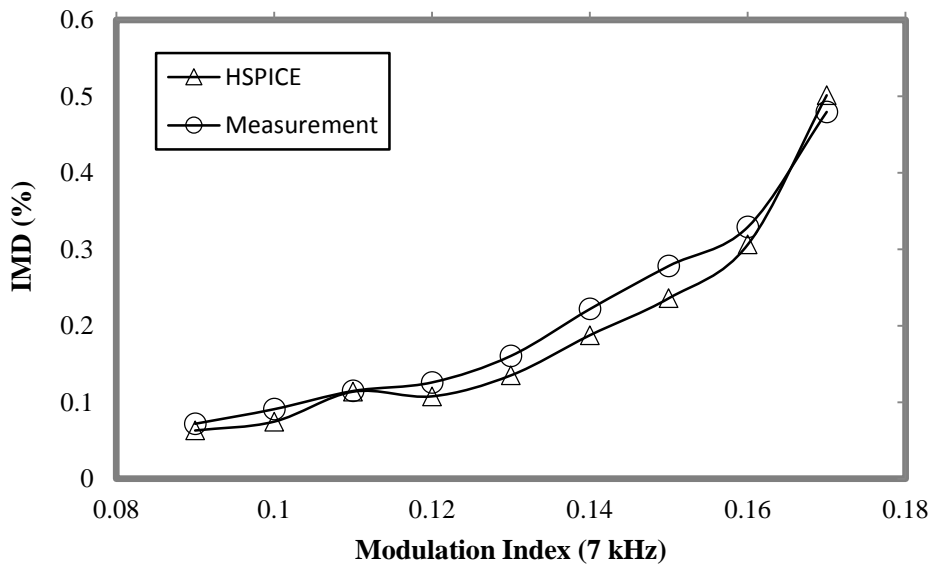


Figure 3.26 The IMD testing setup

Figure 3.27(a) depicts the FFT plot obtained experimentally at the output of the LC lowpass filter. Figure 3.27(b), on the other hand, depicts the IMD obtained from simulations and experimentally of the proposed CDA as a function of modulation index.



(a)



(b)

Figure 3.27 (a) FFT plot of the output of the LC lowpass filter from the IMD test setup (b) IMD of the proposed self-oscillating CDA against modulation index

On the basis of Figure 3.27(a) and (b), the following observations and remarks are made:

- (i) From Figure 3.27(a), the difference between the magnitude of f_2 and f_1+f_2 (or f_1-f_2) is 62dB. Hence, the IMD is determined to be $<0.1\%$.
- (ii) From Figure 3.27(b), the IMD of the proposed CDA is low, $<0.5\%$, over the entire modulation indexes range. For completeness, the modulation index of the V_1 (7 kHz) component ranges from 0.025 to 0.175, or equivalently, the composite modulation index (including both V_1 (60Hz) and V_2 (7 kHz) components) ranges from 0.125 to 0.875- the upper limit to avoid signal clipping.
- (iii) As expected, the IMD increases as the modulation index increases. That is probably due to the reduced loop gain as the switching frequency reduces when the modulation index increases.

3.5.2 Power Efficiency

Power efficiency was previously defined in equation (2-1), the ratio of the useful power (the power consumed by the load) to the total power drawn from

the (DC) power supply. As delineated in chapters, a high power-efficient audio amplifier is desirable because it leads to lower power dissipation and longer battery lifespan. In general, for audio amplifiers based on CDAs, most power dissipation occurs in the output stage [86] (also see section 2.3.5). The power dissipation due to the non-ideal output stage could be reduced by decreasing the switching frequency f_c , and better optimizing the value of parasitic capacitance, C_P , and on-resistance R_{on} (see equations (2-7) - (2-10)).

The standard test setup for measuring power efficiency is depicted in Figure 3.28. An ammeter reads average value of the current from power supply.

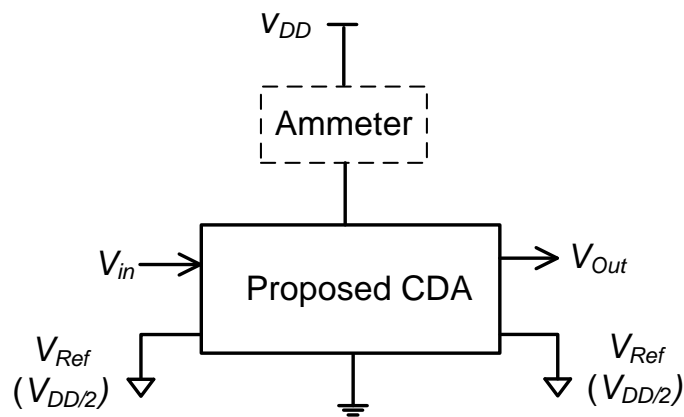


Figure 3.28 The schematic of power efficiency testing setup

In the perspective of a monolithic realization, the measurement results here for CDAs realized using discrete components are only slightly meaningful. The power dissipation may vary with discrete components selected (op amps and a comparator) and the actual implementation (layout) of the output stage. In other words, the power efficiency would be more efficient if the proposed CDA was realized monolithically and with higher power efficient op amps,

comparator and output stage. Using the equation (2-1) and (2-2) in Chapter 2, the power efficiency can be ascertained.

The measured power efficiency of the CDAs (including two op amps, comparator and output stage) as a function of modulation indexes is depicted in Figure 3.29.

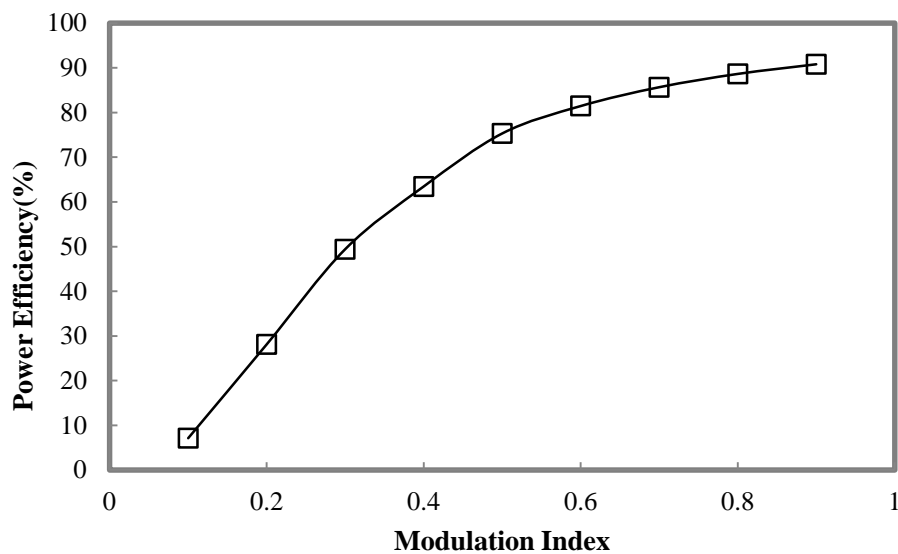


Figure 3.29 Power efficiency against modulation index for the proposed CDA

On the basis of Figure 3.29, the following observations and remarks are made:

- (i) The power efficiency of the proposed CDA could achieve a max of 90% at $M = 0.9$. Compared to the linear amplifiers (where the theoretical maximum power-efficiency of Class A amplifiers is 25% and that of Class B amplifiers (with serious crossover distortion) is 78.5%), the obtained power efficiency is much better. Note that the maximum

power efficiency of the linear amplifiers (Class AB or Class G) is practically much less than the theoretical values (e.g. < 66% [45]).

- (ii) The power efficiency increases as the modulation index increases. This is due to two reasons. First, the power consumed by the load increases as the modulation index increases (see equation (2-2)). Second, because the corresponding switching frequency decreases at high modulation index (see Chapter 2, section 2.2.4) and the switching loss at the output stage reduces (see section 2.3.5).

3.5.3 Benchmarking

For purpose of benchmarking, the proposed CDA is first compared against the state-of-the-art linear amplifiers and thereafter, against reported CDAs for earphone/headphone amplifiers. The earphone/headphone amplifiers reported are driving 32Ω earphone/headphone load.

Table 3.3 tabulates the performance comparison with state-of-the-art linear amplifier designs.

Table 3.3 Benchmarking proposed CDA against linear amplifiers for earphones/headphones

Key Parameters	Proposed	[5]	[87]	[88]	[89]
Amplifier	CDA	Class G	Class AB	Class AB	-
Process Technology	0.35 μm^{Δ}	0.13 μm	0.13 μm	65nm	-
	Discrete Components ⁺				
SNR	102dB ^{Δ}	101dB	92dB	68dB	105dB
	97dB ⁺				
THD+N	<0.009% ^{Δ}	0.01% @ $P_{out}=16\text{mW}$	0.009% @ $P_{out}=10\text{mW}$	0.04% @ $P_{out}=27\text{mW}$	0.05% @ $P_{out}=10\text{mW}$
	<0.009% ⁺				
PSRR @217Hz	106dB ^{Δ}	~60dB	-	-	89dB
	100dB ⁺				
Power Efficiency	91% ^{Δ}	~65%	-	-	<50%
	90% ⁺				

* Commercial chip ^{Δ} Simulation results

⁺ Measurement results - Unspecified/Unreported

It can be noted that on the basis of SNR, THD+N and PSRR, the proposed design is highly competitive as an amplifier for earphones/headphones. Its measured SNR meets fidelity standards while the simulated SNR is close to that reported in [5] and [89]. Its THD+N and PSRR are highest of that tabulated in Table 3.3. As its architecture is a CDA, it is not unexpected that it features the highest power efficiency.

For completeness of benchmarking, Table 3.4 tabulates the comparison between the proposed design against other CDAs for earphone/headphone applications. Note that the competing CDAs do not embody the complete feedback architecture – as delineated earlier, to the best of our knowledge, this is the first CDA with complete feedback for earphones/headphones.

Table 3.4 Benchmarking proposed CDA against the reported CDAs for earphones/headphones

Key Parameters	This design	[8]*	[27]	[90]	[86]	[91]
Configuration	Complete Feedback	Incomplete feedback	Incomplete feedback	Incomplete Feedback	Incomplete feedback	Incomplete feedback
Process Technology	0.35 μm^{Δ}	-	0.13 μm	0.25 μm	0.3 μm	Discrete Components
	Discrete Components ⁺					
SNR	102dB $^{\Delta}$	70dB	97dB	-	92dB	-
	97dB ⁺					
THD+N	<0.009% $^{\Delta}$	<1%	<0.08%	0.05%	-	<0.1%
	<0.009% ⁺					
PSRR@ 217Hz	106dB $^{\Delta}$	60dB	70dB	84dB	-	90dB
	100dB ⁺					
Power Efficiency	91% $^{\Delta}$	76%	90%	-	81%	-
	90% ⁺					
Switching frequency	1MHz	-	700kHz	2MHz	1.4112MHz	300kHz

* Commercial IC, BTL output $^{\Delta}$ Simulation results

⁺ Measurement results- Unspecified/Unreported

From Table 3.4, it can be seen that the proposed CDA is the most competitive of all CDAs benchmarked against. SNR, THD+N (measured equal to [27]) and PSRR all simultaneously superior yet with improved power efficiency. As explained earlier, the higher fidelity is largely due to the high loop gain boosted by the 2nd-order integrator and the comparator. The higher efficiency, on the other hand, is largely due to the simpler hardware – the switching frequency is desirable on the low side; only design [27] has a lower switching rate.

3.6 Conclusions

This chapter has presented the system level design considerations of the proposed high-fidelity CDA design, including that for the modulator, output stage and lowpass filter. Analytical expressions for the design have also been derived, providing useful insight into the design. The complete proposed design has been provided, including all components values, and the ensuing simulated and measured parameters on the basis of a realization using discrete components. Finally, the proposed CDA has been benchmarked against state-of-the-art linear amplifiers and other CDAs for earphone/headphone applications. Overall, the proposed CDA has been shown to be the most competitive amplifier.

Chapter 4 Conclusions and Recommendations for Future Work

4.1 Conclusions

The overall research objective of this Master of Engineering research program pertains to design of a high-fidelity analog CDA with complete feedback based on self-oscillating approach for earphone/headphone applications. At this juncture, low-power earphone/headphone amplifiers are dominated by linear amplifiers (Class AB or Class G). Interestingly, there are only a few reported analog CDA designs embodying the self-oscillating approach with complete feedback for general high-fidelity audio applications but not for low-power high-fidelity earphone/headphone applications. Reported self-oscillating approach generally suffers from relatively high nonlinearities at high modulation indexes. In earphone/headphone application, noise nonlinearities are of specific concern because its perceived presence. It is hence not unexpected that there are very few CDAs reported for this application.

In this dissertation, we have proposed a novel single-ended-output low-power high-fidelity power-efficient analog CDA with complete feedback based on the self-oscillating approach for earphones/headphones – to the author’s knowledge, the first such an attempt (for a CDA with complete feedback) for earphones/headphones.

In Chapter 2, linear and switching audio amplifiers have been comprehensively reviewed, and the salient differences between the modalities of these amplifiers delineated in terms of fidelity and power efficiency. A

comprehensive review on analog CDAs, including the various analog modulation approaches and architectures within their classifications, has been delineated. Amongst the various modulations and architectures, the PDM CDA based on self-oscillating approach with complete feedback provides potential of lower nonlinearities due to its high loop gain and high switching frequency. In addition, PDM with complete feedback features better robustness and less design constraints in terms of stability issues. On this basis, this class of analog CDAs is the amplifier of interest in this dissertation for the design of a high-fidelity earphone/headphone amplifier.

In Chapter 3, the proposed design for the high-fidelity earphones/headphones has been delineated. The salient features of the proposed design are as follows. First, the proposed design embodies a complete feedback topology, where the *LC* filter constitutes part of the feedback loop, thereby potentially higher fidelity as the nonlinearities of the *LC* filter are reduced by $(\text{Loop Gain} + 1)$ due to negative feedback mechanism. Further, it is potentially more cost-effective due to the possibility of employing a low cost inductor (with higher nonlinearities). Second, the proposed design employs the self-oscillating approach, thereby not requiring an externally generated carrier generator and a complicated phase compensation circuit (to maintain the stability due to the phase lag of the *LC* lowpass filter), hence hardware simplicity. Third, the proposed design employs a single-ended output to enable its application as a low-power earphone/headphone amplifier, as constrained by the 3-pin TRS or 4-pin TRRS connection.

In addition, the proposed design features high loop gain and well controlled switching frequency (≤ 1 MHz). The novel integrator-cum-control block proposed in the modulator of the proposed CDA included a 2nd-order lossy integrator that features high loop gain (200dB at DC) to further attenuate the nonlinearities of the blocks (the modulator, output stage and the *LC* lowpass filter in the feedback loop) and suppresses the noise across the entire audio frequency range (20 Hz – 20 kHz). The suppression of nonlinearities is sufficient such that at high modulation indexes, the fidelity (SNR > 90dB, THD+N >0.01% and PSRR > 70dB) of the proposed CDA meets the requirements of the earphone/headphone amplifiers. From a manufacturing perspective, as delineated above, the high nonlinearities suppression provides the potential of lower cost as a lower quality (higher nonlinearity) inductor maybe employed. Further, the control block is designed with phase lead-lag characteristics to compensate the intrinsic delay of the circuit and tuned to establish the desirable switching frequency.

Analysis to model the functionality of the blocks of the proposed CDA to depict the pertinent parameters of the design that affect the fidelity (loop gain of the comparator and switching frequency) has been derived. This analytical work provides meaningful insights to the design of the proposed CDA.

Chapter 3 has also presented the verification of the proposed design on the basis of HSPICE simulations and hardware measurements on a prototype realized using discrete components. The proposed CDA is verified to meet all specifications of a low-power high-fidelity audio amplifier for

earphones/headphones SNR = 97dB, THD+N \leq 0.009% PSRR \geq 73dB. These parameters are comparable to state-of-the-art linear amplifiers and yet substantially more power-efficient, for example, $\eta = 90\%$ at maximum modulation index. In addition, PS-IMD, a parameter that is pertinent to fidelity, seldom quoted, has been characterized at $f_n = 217\text{Hz}$ (with amplitude 250mV_{pp}) and $f_{in} = 1\text{ kHz}$ ($M = 0.9$) - PS-IMD is high $\sim 98\text{dB}$. The IMD of the proposed CDA has also been characterized and is low (IMD $< 0.5\%$) over the entire range of modulation indexes.

In conclusion, this dissertation has delineated the successful design and realization of a high-fidelity CDA based on self-oscillation with complete feedback for low-power earphone/headphone amplifiers.

4.2 Recommendations for Future Research

In view of the investigative work and proposed CDA design in this dissertation, we recommend the following future work:

- (i) To accommodate the single-ended output (see Figure 1.1 earlier) due to the limitation of the 3-pin TRS or 4-pin TRRS plug to the earphone/headphone socket, the coupling from the LC filter output to acoustic load is ac coupled; this is common to all amplifiers (linear and CDAs). This coupling requires a large valued capacitance (due to the low audio frequency), typically hundreds of μF .

We suggest an investigation into the design of our CDA such that this large valued coupling capacitor can either reduced or completely eliminated. This would ultimately reduce the form factor of the CDA and hence the ensuing cost.

- (ii) In a typical earphone/headphone application, a stereo amplifier is required - two mono CDAs. One of the attributes of a CDA based on self-oscillation is the variation of the switching frequency as a function of modulation index where the switching frequency reduces with higher modulation indexes. As the inputs to left channel and right channel of a stereo amplifier are different, the modulation indexes therein are likewise different. Consequently, as the switching frequencies of the two mono channels would be different, the possibility of beating (beating tones) arises. This is common to all CDAs amplifiers based on self-oscillation. The beating would be unacceptable in the high-fidelity earphone/headphone application.

We suggest an investigation to mitigate/eliminate beat tones issues of a stereo earphone/headphone amplifier embodying CDAs based on self-oscillation.

- (iii) As delineated in Chapter 2, the switching frequency of the proposed CDA is relatively high compared to PWM CDAs. This relatively high switching frequency results in higher switching losses in the output stage of the CDA (see equation (2-7)). This consequently results in

lower power-efficiency, thereby somewhat defeating the advantages of the high power-efficiency of CDAs.

We suggest an investigation to reduce the switching frequency of the CDA, thereby mitigating the power losses in the output stage, whilst retaining high-fidelity.

- (iv) As delineated in Chapter 3, the proposed design is probably more sensitive to the variations of the components than the ubiquitous PWM CDAs. This applies to all CDAs based on the self-oscillation architecture.

We suggest investigation with Monte Calo simulations to analytically derive the sensitivity of several CDA designs (including the proposed CDA) and compare them. We further suggest that the analysis include an investigation into methods to reduce said sensitivity.

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