

Ultra Low Power CMOS Phase-Locked Loop Frequency Synthesizers

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I hereby certify the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other University or Institution.

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ABSTRACT

With the increasing demand for low cost and high integration of wireless transceiver building blocks, the low-power performance is a great concern for radio-frequency integrated circuit (RFIC) designers. Intensive effort has been made to develop RF integrated circuits and systems in the gigahertz range using the low-cost CMOS process. The commonly used frequency synthesizer based on the phase-locked loop (PLL) is an important building block of the transceiver.

The frequency synthesizer, which performs the main role of carrier generation for the down-conversion/up-conversion operations, is a major and critical block of a wireless transceiver because it operates at high frequency and consumes a very large portion of the total power consumption in the transceiver. The performance in power consumption and channel selection of frequency synthesizer are limited by the two most important building blocks, namely the voltage-controlled oscillator (VCO) and the high frequency divider. The objective of this research work is to design the critical blocks for the frequency synthesizer with low power consumption.

In this thesis, we have carried a detailed analysis on the speed and power consumption of the digital dividers and developed low power prescalers based on the dynamic logic. A CMOS fully programmable 1 MHz resolution divider for Zigbee and IEEE 802.15.4 applications is implemented based on pulse-swallow topology which uses the proposed ultra-low power $2/3$ prescaler, low power $47/48$ prescaler and a reloadable D flip-flop for the counters. A detailed design of wide-band $2/3$ prescaler

based on dynamic logic is presented which is suitable for IEEE 802.11 a/b/g applications and also verified in the design of fully programmable Multi-band divider which provides flexible resolution.

We also performed a detailed study on the phase noise and power consumption of the CMOS VCO and designed a low power cross coupled LC-VCO with optimized phase noise. A detailed analysis on the charge-pump is carried and introduced a low spur gain boosting charge-pump to reduce the reference spurs. We also presented the detailed design of the 2nd and 3rd loop filters with mathematical equations and Matlab simulations.

In this report, we first discuss the basics and performance requirements of frequency synthesizer and we then discuss the state-of-the-art prescalers and PLL's in literature. In the next few chapters, we will discuss detailed design and analysis of low power dividers, low spur charge pump, cross-coupled LC VCO, phase frequency detector and implementation of the multi-band flexible divider with measured results. Finally we present the implemented PLL synthesizer architecture using the proposed low power building blocks and results of our low power PLL frequency synthesizer.

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LIST OF ACRONYMS

BAN	Body Area Network
BPSK	Binary Phase Shift Keying
CML	Current Mode Logic
DDS	Direct Digital Synthesizer
DAC	Digital to Analog Converter
DMP	Dual Modulus Prescaler
DFF	D Flip-Flop
DSSS	Direct Sequence Spread Spectrum
E-TSPC	Extended True Single Phase Clock
GSM	Global System for Mobile Communications
GFSK	Gaussian Minimum Shift Keying
ISM	Industry Scientific Medical
ISF	Impulsive Sensitive Function
ILFD	Injection Locked Frequency Divider
LPF	Low Pass Filter
OFDM	Orthogonal Frequency Division Multiplexing
PLL	Phase Locked Loop
PFD	Phase Frequency Detector
QPSK	Quadrature Phase Shift Keying
ROM	Read only Memory
RFIC	Radio Frequency Integrated Circuit
SSB	Single Side Band
SOC	System on Chip
TSPC	True Single Phase Clock
VCO	Voltage Controlled Oscillator
WLAN	Wireless Local Area Network

CHAPTER 1

INTRODUCTION

1.1. Introduction and Motivation

Over the last two decades, the continuous shrinking in the feature size of MOSFETs has increasingly attracted the research and development of low-power radio frequency CMOS integrated circuits [1], [2]. For mobile wireless communications, low-power operations are of crucial importance for the mobile units as the battery lifetime is limited by the power consumption and the low power consumption also helps to reduce the operating temperature resulting in more stable performance. For the modern transceiver architecture, a fully integrated frequency synthesizer with low power voltage-controlled oscillators (VCO) for quadrature signal generation and low power frequency dividers with multi-channel selection is always a topic of interest in research.

Phase-locked loops (PLLs) are widely used in radio frequency synthesis. The PLL based frequency synthesizer is one of the key building blocks of an RF front-end transceiver. The PLL frequency synthesizer system is mainly designed to ensure the accuracy of its output frequency under operating conditions. Phase noise is one of the most critical performance parameters of the frequency synthesizer. The goal to meet strict phase noise, spurious-level performance and fine frequency resolution with

reasonable levels of power consumption remains a challenging task for the circuit designer.

The need for mobile communications computing and networking has become more than ever important. Over the last decade, various wireless standards have been developed primarily for applications over short distances. These wireless standards are intended to provide fast and low cost connections to the internet and between the portable devices with communication range between 1 and 100 meters. Examples of such standards include IEEE 802.11a/b/g, Bluetooth, Zigbee and IEEE 802.15.4 [3]-[8]. Table 1.1 gives a comparison between these standards.

Table 1.1 Specifications of different popular WLAN standards

Specifications	Bluetooth	802.11b	802.11g	802.11a
Data Rate	1 Mbps	11 Mbps	54 Mbps	54 Mbps
Band	2.4 GHz ISM	2.4 GHz ISM	2.4 GHz ISM	5 GHz UNII
Range	10m	100m	100m	50m
Channel Bandwidth	1 MHz	25 MHz	25 MHz	20 MHz
RX Sensitivity	-70 dBm	-76 dBm	-76 to -74 dBm	-82 to -65 dBm
Modulation	GFSK	11Mbaud QPSK	OFDM 64+	COFDM BPSK
TX Output power	0- 20 dBm	30 dBm	30 dBm	17-24 dBm
Settling time	<259 us	<224 us	<224 us	<224 us

It has been realized that successful existing wireless standards like Bluetooth and 802.11a/b/g offer relatively high data rates at the expenses of high power consumption and high cost. The IEEE 802.15.4 standard [6] has been developed to cater the needs of low cost, low power, low data rate and short range wireless networks. The standard addresses the need of network applications requiring high density of transceivers with low data-rate. These transceivers need to have a long battery life to be an attractive option for applications pertaining to sensor based network systems, home automation, automotive and medical solutions. The performance requirements of an IEEE 802.15.4 compatible transceiver are based on the physical layer specifications described in [6] as given in Table 1.2.

Table 1.2 Specifications of the 2450 MHz IEEE 802.15.4 PHY Layer

Performance Metrics	Specifications
Spectrum	2400-2483.5 MHz
Modulation	O-QPSK using DSSS
Data rate	250 Kb/s
Channel Bandwidth	2 MHz
Channel Spacing	5 MHz
No. of Channels	16 (11-26 of the PHY layer)
Sensitivity	-85 dBm
BER	5e-5
SNR	2 dB
Settling Accuracy	+/- 40 ppm (96 KHz)
Alternate Channel Rejection	30 dB at 10 MHz offset
Adjacent Channel Rejection	0 dB at 5 MHz offset

The IEEE 802.15.4 standard has been specifically designed to cater for the needs of low cost, low power, low data rate and short range wireless networks. Few frequency synthesizers based on this standard have been reported in literature [7]-[11] and the frequency synthesizer reported in [9] has the power consumption of 2.4 mW at 1.2-V power supply. Most synthesizers have not scaled down the supply voltage to reduce the power consumption of digital blocks. We believe that power consumption of the frequency synthesizer (mainly VCO and frequency divider) can be reduced significantly by further simplifying the circuit structures, and adapting some power saving techniques to the digital blocks such as frequency dividers.

1.2. Contributions

This research study gives detailed analysis, specifications and design of low power fully integrated, integer-N frequency synthesizers for IEEE 802.15.4. Much of the work in the implemented synthesizer is focused on fully programmable low power dividers, and low power VCOs. The new contributions of this thesis are as follows:

Design and Analysis of ultra-low power 2/3 TSPC prescaler

A detailed analysis of power consumption and propagation speed of the dynamic logic flip-flops is carried out and an ultra-low power True-single-phase clock (TSPC) 2/3 prescaler is proposed which is verified in the design of TSPC 32/33 prescaler in

01.8 μ m CMOS technology.

A low power TSPC 47/48 prescaler

The design of a fully programmable 1 MHz resolution divider for the 2.4 GHz frequency synthesizer using a 32/33 prescaler, a 7-bit programmable P-counter and a 5-bit swallow S-counter results in 1 MHz output with duty cycle less than 25%. In order to improve the duty cycle, a low power TSPC 47/48 prescaler is implemented without an additional flip-flop. This new design is similar to the design of 32/33 prescaler with an additional inverter.

A wide-band 6.5 GHz CMOS prescaler

Due to the speed limitation, most of the dynamic logic based prescalers reported in literature are restricted below 5 GHz applications. However, by embedding the logic gates in to the flip-flop and optimizing the device sizes results in improvement of speed. Based on this optimization, a wide-band 2/3 prescaler based on single-phase clock is proposed which has maximum operating speed of 6.5 GHz and silicon verified in the 0.18 μ m CMOS technology.

CMOS Multi-band flexible divider

Most of the frequency synthesizers reported in literature adopted current mode logic (CML) dividers as the first stage divider and dynamic latches are not yet implemented

for multi-band frequency synthesizers. With the proposed single phase clock 6.5 GHz prescaler, a multi-band dynamic logic divider with flexible resolution is designed and verified in 0.18 μ m CMOS technology which provides a solution to low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4 and IEEE 802.11a/b/g WLAN applications.

A low power CMOS Cross-coupled VCO

The first stage divider and voltage controlled oscillator (VCO) are the most power hungry blocks in the frequency synthesizer. We will present the detailed design of the low power cross-coupled VCO in a 0.18 μ m CMOS technology. Also a VCO with a filtering technique is implemented to filter the low frequency noise and to improve the phase noise. The design is fabricated in a 0.18 μ m CMOS technology.

A low spur gain-boosting charge pump

The cause of mismatches in the design of charge pump is analyzed. Based on this analysis, a low spur gain-boosting charge pump is implemented which reduces the mismatch between charging and discharging currents to improve the spur levels in the output of PLL spectrum.

A low power fully integrated CMOS 2.4GHz frequency synthesizer

Based on the proposed low power fully programmable divider with 1 MHz resolution,

a low power cross-coupled VCO and a low spur gain-boosting charge pump, a 2.4 GHz fully integrated frequency synthesizer is implemented in a 0.18 μm CMOS technology and the measurement results are presented. A detailed design of the 3rd order loop filter is also described.

1.3. Organization of thesis

In Chapter 2, the fundamentals of the frequency synthesizer and its building blocks such as the phase frequency detector (PFD), the loop filter, the dividers and the charge pump are discussed. Some of the existing VCO phase noise models are discussed and a detailed comparison of existing frequency synthesizers for 2.4 GHz ISM band is given.

In Chapter 3, a detailed analysis of power consumption and propagation speed of the dynamic logic flip-flops mainly, true-single phase clock (TSPC) and extended true-single phase clock (E-TSPC) is presented. A low power TSPC 2/3 prescaler is proposed and verified in the design of 32/33 prescaler.

In Chapter 4, the design of a fully programmable divider with 1 MHz resolution is presented with 25 % duty-cycle. A 47/48 TSPC prescaler and low power reloadable bit-cell for swallow S-counter is proposed which is implemented in the design of fully programmable divider with an output duty cycle close to 50%.

In Chapter 5, a low power wide-band 2/3 prescaler is proposed. Based on this

design, a fully programmable multi-band flexible divider for multi-band frequency synthesizers is presented.

In Chapter 6, different kinds of mismatches in the charge pump design are discussed and a low spur gain boosting charge pump is designed to reduce the spurs level and is verified through simulations. A detailed design of low power cross-coupled CMOS VCO is presented and compared with the literature work.

In Chapter 7, two fully integrated PLL frequency synthesizers are presented. Firstly, a low power fully integrated frequency synthesizer based on quadrature-VCO (Q-VCO) and conventional fully programmable divider at 1.8 V power supply with measured results is presented. Secondly, a detailed design of low power fully integrated frequency synthesizer based on proposed low power $2/3$ prescaler, $47/48$ prescaler, low power VCO and low spur charge pump at 1.5 V power is presented. Finally, Chapter 8 gives a summary of the work in this thesis and the proposed future work.

CHAPTER 2**PHASE LOCKED LOOP FREQUENCY SYNTHESIZERS**

In this Chapter, the fundamentals of frequency synthesizers are discussed. First we define the PLL frequency synthesizer and introduce the concept of phase noise and its effect on the transceiver. We then discuss the theory behind the phase locked loops (PLL) and the integer-N charge pump frequency synthesizer based. Subsequently, all the building blocks of the frequency synthesizer such as phase frequency detector (PFD), charge pump (CP), Voltage-controlled oscillator (VCO), divider and loop filter (LF) are discussed.

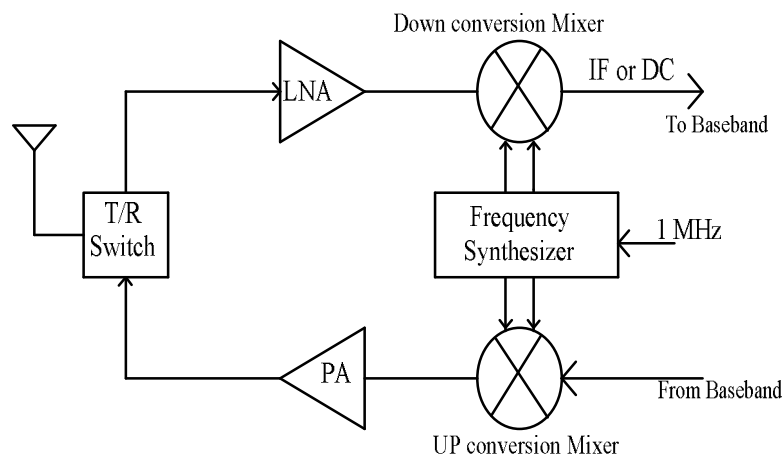
2.1. Frequency synthesizers in the transceivers

Fig. 2.1 The role of frequency synthesizer in a transceiver

The frequency synthesizer generates a set of signals (usually sinusoidal) of given frequencies with the stability and precision referred to a single frequency reference source. It is regarded as one of the most critical modules in modern wireless

communications systems. Fig.2.1 shows the architecture of a typical modern transceiver [12]. The output signal generated by the frequency synthesizer is normally termed as the local oscillator (LO) signal, since it is used as the reference oscillator for frequency translation and channel selection in communication systems.

At the receiver side, the high frequency LO signal is used to down-convert the incoming signal into a lower frequency (baseband or intermediate frequency (IF)) where it can be processed to extract the information it is carrying. The same LO signal can be used to up-convert the baseband signal to an RF frequency, so that it can be transmitted over the medium. The frequency synthesizer is mainly designed to ensure the accuracy of its output signal under the operating given conditions. The frequency synthesizer is normally implemented using phase-locked loop (PLL).

2.2. Phase Noise

An ideal output spectrum of a frequency synthesizer should be a single tone at the desired frequency in order to provide a stable channel frequency. A delta function in the frequency domain is equivalent to a pure sinusoidal waveform in the time domain.

The random amplitude and phase deviations from the desired values produce the energy in the side-bands of the desired frequency. When this energy is mixed with the received RF signal or modulated baseband signal, undesired sidebands are created.

Phase noise and spurious tones are the two key parameters indicating the performance

of a synthesizer. The output of an ideal frequency synthesizer has a pure sinusoidal, which is given by

$$V(t) = V_0 \cos(2\pi f_0 t) \quad (2.1)$$

where V_0 and f_0 are amplitude and frequency of the signal. With the amplitude and phase noise fluctuations, the waveform becomes

$$V(t) = (V_0 + v(t)) \cos(2\pi f_0 t + \phi(t)) \quad (2.2)$$

Where $v(t)$ and $\phi(t)$ represent amplitude and phase fluctuations respectively. Because the amplitude fluctuations can be removed or greatly reduced in well designed, high performance oscillators, we concentrate on phase fluctuation effects in a frequency synthesizer output only. The spectral density of the phase variation is [13]

$$S_\phi(f) = \int_{-\infty}^{+\infty} R_\phi(\tau) e^{-j2\pi f\tau} d\tau \quad (2.3)$$

where $R_\phi(\tau)$ is the auto-correlation of the random phase variation $\phi(t)$

$$R_\phi(\tau) = E[\phi(t)\phi(t-\tau)] = \int_{-\infty}^{+\infty} \phi(t)\phi(t-\tau) dt \quad (2.4)$$

When the root-mean square (rms) value of $\phi(t)$ is much smaller than 1 radian, the output signal of the frequency synthesizer can be written as

$$V(t) = V_0 \cos(2\pi f_0 t + \phi(t)) = V_0 \cos(2\pi f_0 t) - \phi(t)V_0 \sin(2\pi f_0 t) \quad (2.5)$$

The power spectrum density of $V(t)$ can be written as

$$S_V(f) = \frac{V_0^2}{2} [\delta(f - f_0) + S_\phi(f - f_0)] \quad (2.6)$$

It consists of the carrier power at f_0 and the phase noise at frequency offset $\Delta f = f - f_0$. The single side-band (SSB) phase noise $L\{\Delta f\}$ is defined as the ratio of noise power in 1Hz bandwidth at frequency offset Δf from the carrier to the carrier power.

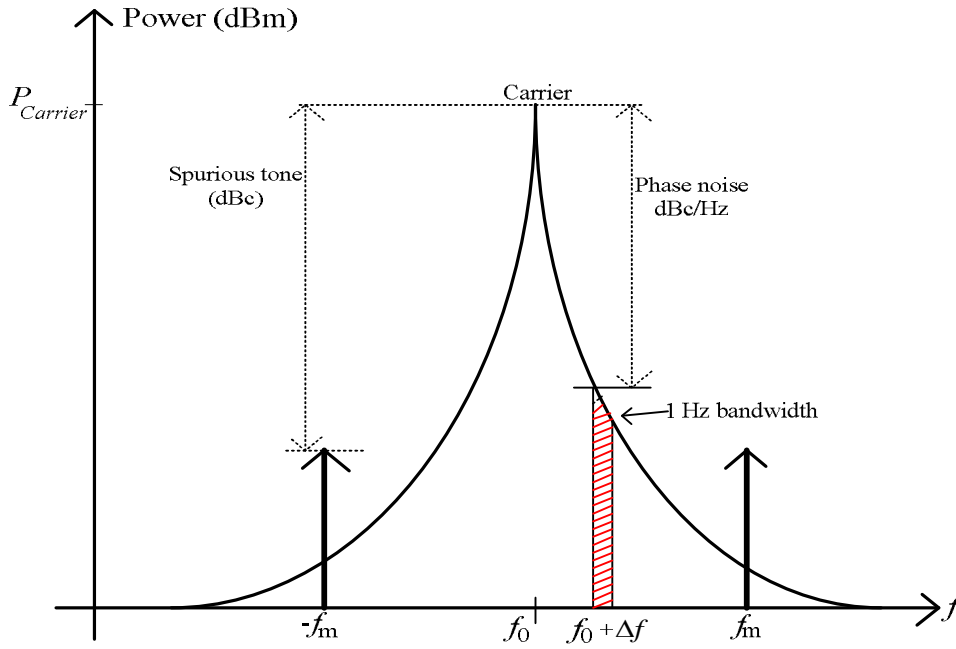


Fig. 2.2 Spectral purity definitions

$$L\{\Delta f\} = 10 \log \frac{P_{noise}(f_0 + \Delta f, 1Hz)}{P_{carrier}} = 10 \log \frac{S_\phi(\Delta f)}{2} \quad (2.7)$$

Where $P_{noise}(f_0 + \Delta f, 1Hz)$ is the noise power in 1Hz bandwidth at offset frequency Δf from the carrier frequency f_0 and $P_{carrier}$ is the carrier power. Fig.2.2 illustrates the phase noise of the synthesized signal of frequency f_0 . Since the phase noise

spectrum can be seen as a sum of sines, the total noise skirt is directly translated to noise side lobes at both sides of the carrier frequency.

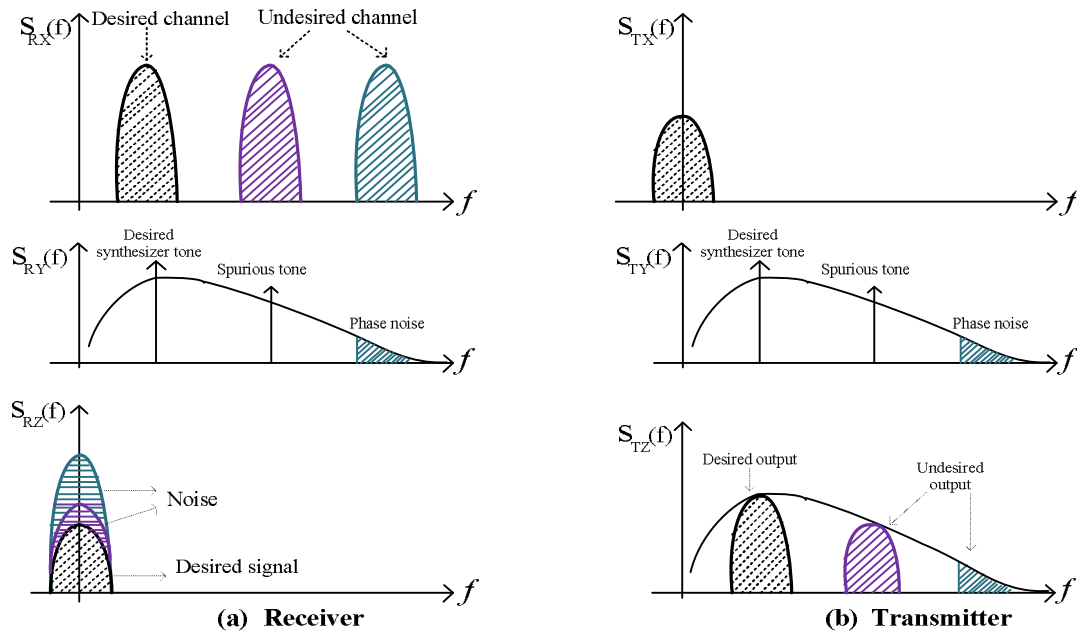


Fig. 2.3 Effect of the phase noise and spurious tones in (a) receiver (b) transmitter

As shown in Fig. 2.3, any noise in the circuit will create phase disturbance. Due to the phase disturbance, the output is no longer a single frequency tone but rather than a smeared version, where the spectrum is spread over a continuous range of frequencies, but the primary concentration of energy is still near the center frequency. In a receiver, the phase noise and spurious tones of the frequency synthesizer mix with various RF signals and produce interferences to the desired signal as shown in Fig. 2.3a. In a transmitter, these spurious tones and phase noise can mix with the modulated baseband signal and produce undesired spectral emissions as shown in Fig. 2.3b. Therefore, the phase noise and the spurious tones are the critical parameters which decide the performance of a frequency synthesizer.

2.3. Basics of phase-locked loops (PLL)

Phase-locked loops are widely used in the design of frequency synthesizers of RF transceivers. Before going in to the detailed discussion of PLL, we first discuss the concept of phase locking. Consider two signals $x_1(t) = \cos(\omega_1 t + \phi_1 t)$ and $x_2(t) = \cos(\omega_2 t + \phi_2 t)$, the instant phases and frequencies are given by

$$\beta_1(t) = \omega_1 t + \phi_1(t) \quad (2.8)$$

$$\beta_2(t) = \omega_2 t + \phi_2(t) \quad (2.9)$$

$$\Omega_1(t) = \delta[\beta_1(t)]/\delta t = \omega_1 + \delta[\phi_1(t)]/\delta t \quad (2.10)$$

$$\Omega_2(t) = \delta[\beta_2(t)]/\delta t = \omega_2 + \delta[\phi_2(t)]/\delta t \quad (2.11)$$

Phase locking means the phase difference between the two signals is constant with time and almost negligible. Therefore, under the locked condition

$$\beta_1(t) - \beta_2(t) = \text{constant} \quad (2.12)$$

$$\delta[\beta_1(t) - \beta_2(t)]/\delta t = \omega_1 - \omega_2 = 0 \quad (2.13)$$

This means that once the loop achieves the locking, there is no frequency difference between the two signals which are compared. By using a feedback loop, a constant phase difference of two periodic signals is ensured when the loop reaches its steady state.

2.3.1 Operation of phase-locked loop

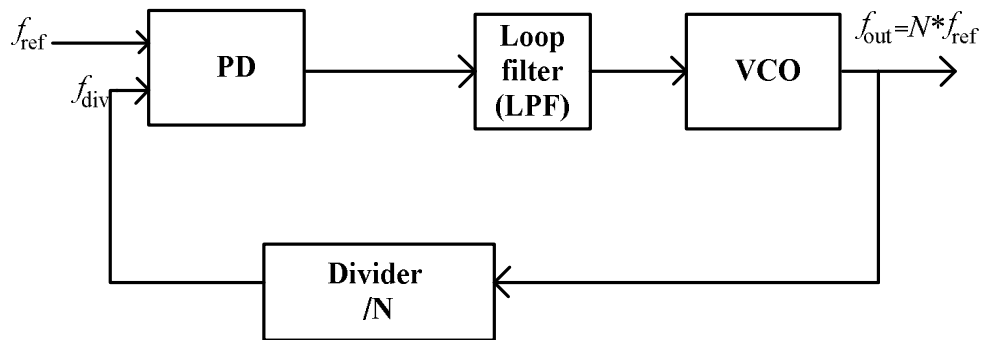


Fig. 2.4 Basic structure of a phase-locked loop

Fig. 2.4 shows the basic topology of a simple phase-locked loop. A PLL is a feedback system which minimizes the phase difference between the reference input f_{ref} and the feedback signal f_{div} . Here, a phase detector (PD) generates a phase error whose DC value is proportional to the difference between the phases of the reference and feedback signals. The low pass filter (LPF) extracts the DC value and applies it to the voltage controlled oscillator (VCO), which changes the output frequency f_{out} . Since frequency synthesizer is required to produce a programmable output frequency, a frequency divider (FD) of programmable division ratio N is employed in the feedback path to divide down the VCO output frequency to the one comparable to the input reference frequency [14]-[16]. When the loop reaches steady state, the phase difference between the reference input f_{ref} and feedback signal f_{div} is constant over time and the relation $f_{out} = Nf_{ref}$ holds true. By changing the value of N , the VCO output frequency can be changed.

2.3.2 Type-I PLL

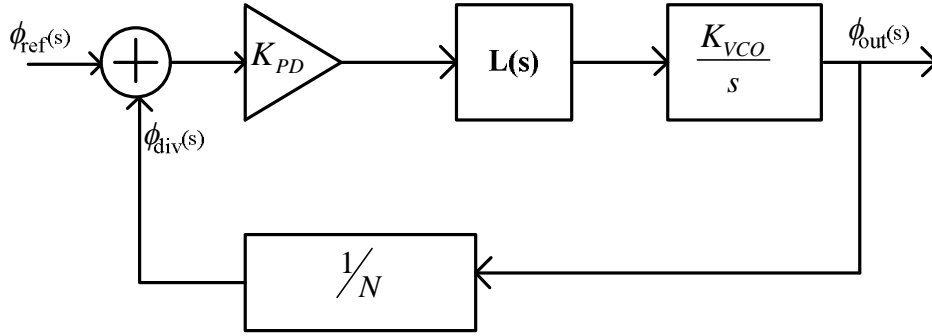


Fig. 2.5 Linear model of a type-I PLL

A simple PLL is analyzed by the phase transfer function as the PD compares the phase difference between the input $\phi_{ref}(s)$ and feedback signal $\phi_{div}(s)$. Fig.2.5 shows the linear model of a type-I PLL with the respective transfer functions of the building blocks. If the loop filter is a simple first order low pass filter (LPF), the transfer function is given by [16]

$$L(s) = \frac{1}{1 + s/\omega_{LPF}} \quad (2.14)$$

where ω_{LPF} denotes the -3 dB bandwidth. The open-loop transfer function is given by

$$H_O(s) = \frac{\phi_{out}(s)}{\phi_{ref}(s)} = \frac{K_{PD}K_{VCO}}{N} \frac{1}{s(1 + s/\omega_{LPF})} \quad (2.15)$$

Since open-loop transfer function contains only one pole at origin, this type of PLL is called type-I PLL. If the input phase varies slowly, owing to the pole at origin, the loop gain goes to infinity as s approaches zero. Thus, the PLL under locked condition ensures that the change in ϕ_{out} is exactly equal to the change in ϕ_{ref} as s

goes to zero. The closed-loop transfer function is written as

$$H_C(s) = \frac{\phi_{out}(s)}{\phi_{ref}} = \frac{K_{PD}K_{VCO}}{s^2/\omega_{LPF} + s + K_{PD}K_{VCO}/N} \quad (2.16)$$

The second order closed-loop transfer function suggests the system can be over-damped, under-damped or critically damped. If we compare (2.16) with standard second order equation from control theory which is given by

$$H(s) = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2} \quad (2.17)$$

$$\omega_n = \sqrt{\omega_{LPF}K_{PD}K_{VCO}} \quad (2.18)$$

$$\xi = \frac{1}{2} \sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}} \quad (2.19)$$

Where ξ is the damping ratio and ω_n is the natural frequency. The two poles of the closed-loop system are given by

$$S_{1,2} = \frac{1}{2} (\omega_{LPF} \pm \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \quad (2.20)$$

$$\xi\omega_n = \frac{1}{2} \omega_{LPF} \quad (2.21)$$

If $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N > 0$, the two poles are real and the transient step response is given by

$$\omega_{out}(t) = \left[\begin{array}{l} \frac{2K_{PD}K_{VCO}}{\sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}} \times \frac{1}{\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}(\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}})t} \right] \\ \frac{1}{\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}} \left[1 - e^{-\frac{1}{2}(\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}})t} \right] \end{array} \right] u(t)\Delta\omega \quad (2.22)$$

(2.21) shows that the step response includes two exponential terms decaying with time constants τ_1 and τ_2 as,

$$\tau_1 = \left[\frac{1}{2}(\omega_{LPF} - \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \right]^{-1} \quad (2.23)$$

$$\tau_2 = \left[\frac{1}{2}(\omega_{LPF} + \sqrt{\omega_{LPF}^2 - \frac{4K_{PD}K_{VCO}}{N}}) \right]^{-1} \quad (2.24)$$

Since $\tau_1 > \tau_2$, the settling time is determined by τ_1 , which decreases with the increase in $K_{PD}K_{VCO}/N$. But, having larger gain degrades the stability. Thus there is a trade-off between the settling time and stability for the type-I PLL. If $\omega_{LPF}^2 - 4K_{PD}K_{VCO}/N < 0$, the two poles are complex and the transient step response is given by

$$\omega_{out}(t) = \left[\begin{array}{l} 1 - e^{-\frac{1}{2}\omega_{LPF}t} \cos\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2}t\right) + \\ \frac{\omega_{LPF}}{\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2}} \sin\left(\sqrt{\frac{4K_{PD}K_{VCO}}{N} - \omega_{LPF}^2}t\right) \end{array} \right] Nu(t)\Delta\omega \quad (2.25)$$

If the damping factor is greater than one ($\xi > 1$), the system is over-damped and from (2.25), the step response contains only one exponential term with the time constant

equal to $2/\omega_{LPF}$, which is less than the time constant for real pole case. The larger is the bandwidth, the faster the settling time. In addition to the trade-off between settling time, phase error and bandwidth, type-I PLL suffers from the acquisition range. These problems are addressed by type-II PLL which is called charge pump PLL [17].

2.3.3 Dynamics of Type-II PLL

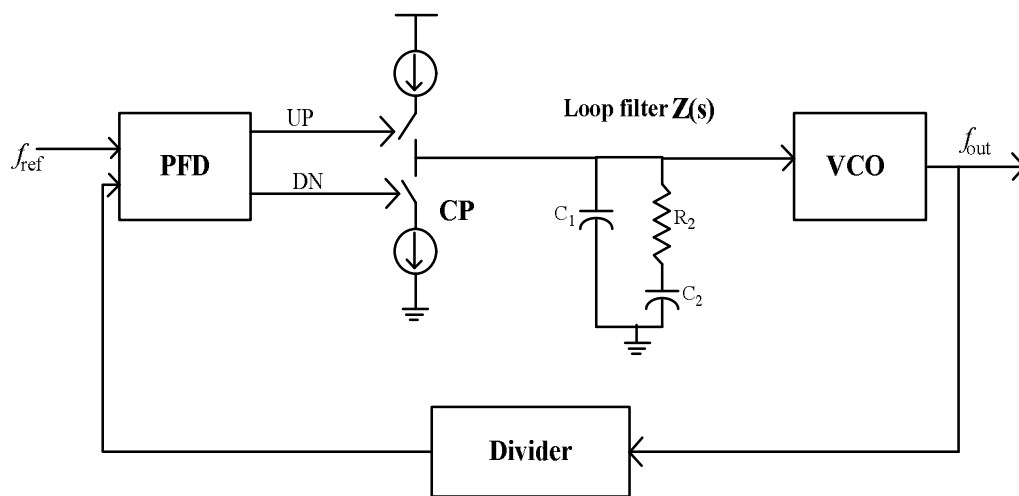


Fig. 2.6 Type-II charge pump PLL

Fig. 2.6 shows the typical type-II charge pump PLL with a 2nd order loop filter. In this architecture the charge pump is used to either sink or source a current with the help of the switches driven by the phase frequency detector (PFD). As a result, the PLL becomes a discrete system rather than a continuous system and strictly, the analysis cannot be performed in s-domain. However, Gardner [17] has proposed a limit that states, as long as the loop bandwidth is less than one-tenth of the reference frequency, the s-domain analysis holds true. Since the PD is replaced by the PFD, the locking range increases. Since the VCO acts as an integrator and the combination of PFD with

the charge pump and the LPF results in another integrator in the loop. Thus there exists two poles at the origin and this type of PLL is called as type-II PLL. Fig. 2.7 shows the linearized model of type-II PLL with their respective transfer functions.

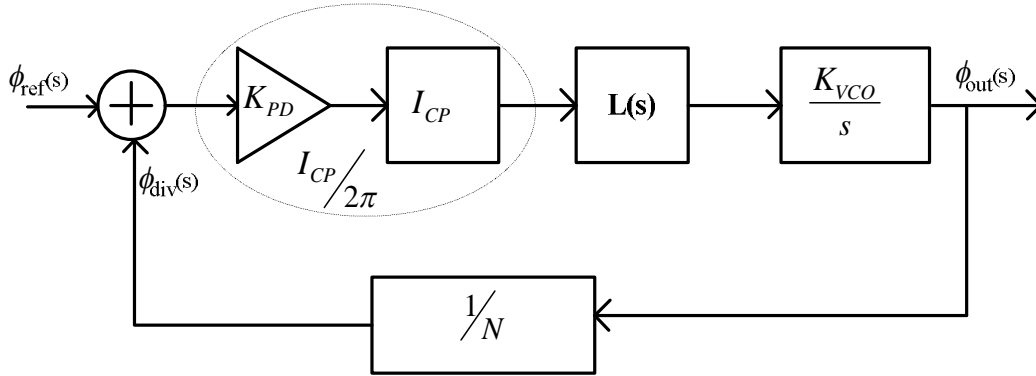


Fig. 2.7 Linear model of a type-II PLL

The open-loop transfer function is given by

$$H_o(s) = \frac{I_{CP} K_{VCO}}{2\pi N} \frac{L(s)}{s} \quad (2.26)$$

Where the transfer function of the 2nd order loop filter is given by

$$L(s) = \frac{1 + sR_2C_2}{s^2R_2C_1C_2 + s(C_1 + C_2)} \quad (2.27)$$

Here, C_2 together with charge pump generates a pole at the zero frequency while R_2 and C_2 generates a zero at the left half plane to stabilize the system. The location of the zero has to be less than the unity-gain frequency. The additional capacitor C_1 is introduced to generate a pole with R_2 to suppress high frequency components at the VCO control line. For stability, this pole has to be much larger than unity-gain frequency ω_c . The zero and pole frequencies are given by

$$\omega_{z1} = \frac{1}{R_2 C_2} = \frac{1}{T_2} \quad (2.28)$$

$$\omega_{p1} = \frac{C_2 + C_1}{R_2 C_2 C_1} = \frac{1}{T_1} \quad (2.29)$$

The closed-loop transfer function is given by

$$H_C(s) = \frac{I_{CP} K_{VCO}}{2\pi N(C_2 + C_1)} \frac{1 + sR_2 C_2}{s^3 \frac{R_2 C_2 C_1}{C_2 + C_1} + s^2 + s \frac{I_{CP} K_{VCO} R_2 C_2}{2\pi N(C_2 + C_1)} + \frac{I_{CP} K_{VCO}}{2\pi N(C_2 + C_1)}} \quad (2.30)$$

Since the pole ω_{p1} is far behind the unity gain frequency and $C_2 > C_1$, the closed loop transfer function can be re-written as

$$H_C(s) = \frac{I_{CP} K_{VCO}}{2\pi N C_2} \frac{1 + sR_2 C_2}{s^2 + s \frac{I_{CP} K_{VCO} R_2}{2\pi N} + \frac{I_{CP} K_{VCO}}{2\pi N C_2}} \quad (2.31)$$

This can be compared with the standard 2nd order negative feedback system from the control theory given by (2.17) and the critical loop parameters are obtained as,

$$\omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi N C_2}} \quad (2.32)$$

$$\xi = \frac{R_2}{2} \sqrt{\frac{K_{VCO} I_{CP} C_2}{2\pi N}} \quad (2.33)$$

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p1}}\right) \quad (2.34)$$

Here, ω_n is natural frequency, ω_c is loop bandwidth (unity-gain cross over frequency), ξ is the damping factor and ϕ_m is the phase margin. The poles of the

closed-loop system are given by

$$S_{1,2} = \frac{1}{2} \left(-\frac{I_{CP} K_{VCO} R_2}{2\pi N} \pm \sqrt{\left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^2 - \frac{4I_{CP} K_{VCO}}{2\pi N C_2}} \right) \quad (2.35)$$

Similar to type-I PLL, the system will have a higher settling time when the two poles are complex, which means

$$\left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^2 - \frac{4I_{CP} K_{VCO}}{2\pi N C_2} < 0 \Rightarrow \frac{I_{CP} K_{VCO}}{2\pi N} < \frac{4}{R_2^2 C_2} \quad (2.36)$$

Based on this, the transient response for the system with complex poles is given by

$$\omega_{out}(t) = \left[1 - e^{-\frac{1}{2} \left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right) t} \right] \left[\frac{\cos\left(\sqrt{\frac{4I_{CP} K_{VCO}}{2\pi N C_2} - \left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^2} t} + \frac{R_2 C_2}{2 \sqrt{\frac{4I_{CP} K_{VCO}}{2\pi N C_2} - \left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^2}} \sin\left(\sqrt{\frac{4I_{CP} K_{VCO}}{2\pi N C_2} - \left(\frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^2} t} \right) \right] Nu(t) \Delta\omega \quad (2.37)$$

The step response contains only one exponential term with the time constant τ expressed as,

$$\tau = \left(\frac{1}{2} \frac{I_{CP} K_{VCO} R_2}{2\pi N} \right)^{-1} \quad (2.38)$$

From the above study, the settling time is minimized by increasing $I_{CP} K_{VCO}$, thus there is no trade-off between critical specifications in the selection of $I_{CP} K_{VCO}$.

However, the increase of $I_{CP} K_{VCO}$ is bounded by the unity gain frequency, which is no more than one-tenth of the reference frequency as stated by the Gardner [17].

2.3.4. Phase noise analysis of PLL

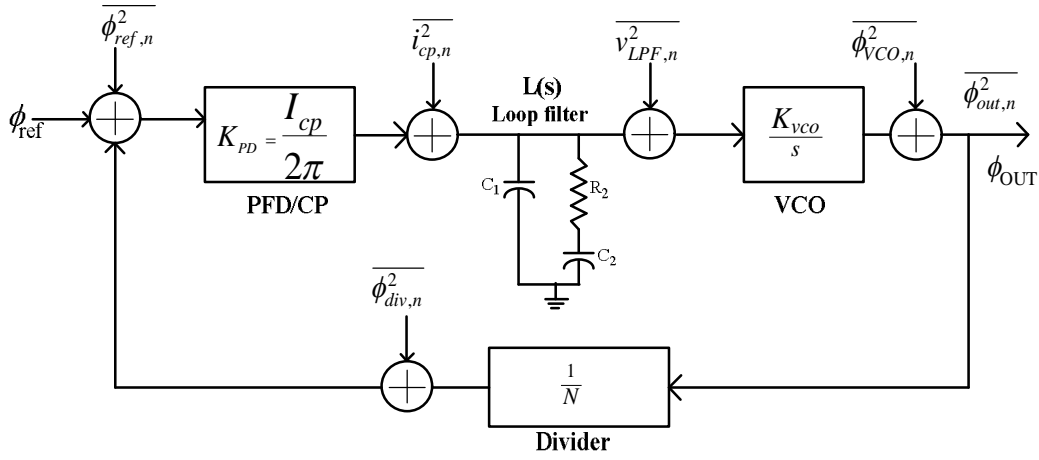


Fig. 2.8 Noise model of type-II charge pump PLL

An important advantage of using PLL for frequency generation is that, if the noisy VCO output is compared with a clean source through the feedback loop, the phase noise at the oscillator output is suppressed. Fig. 2.8 shows the noise model of a charge pump PLL. The noise sources can represent either the noise created by individual blocks due to intrinsic noise sources, or the noise coupled into the blocks from external sources, such as noise from power supplies and substrate noise. The noise transfer functions from the various sources to the PLL output noise can be expressed as follows.

$$\frac{\phi_{out,ref}(s)}{\phi_{ref,n}(s)} = N \cdot \frac{H_O(s)}{1 + H_O(s)} = \frac{NK_{PD}K_{VCO}L(s)}{Ns + K_{PD}K_{VCO}L(s)} \quad (2.39)$$

$$\frac{\phi_{out,cp}(s)}{i_{cp,n}(s)} = \frac{N}{K_{PD}} \cdot \frac{H_O(s)}{1 + H_O(s)} = \frac{NK_{VCO}L(s)}{Ns + K_{PD}K_{VCO}L(s)} \quad (2.40)$$

$$\frac{\phi_{out,LPF}(s)}{v_{LPF,n}(s)} = \frac{K_{VCO}}{s} \cdot \frac{1}{1 + H_O(s)} = \frac{K_{VCO}}{s(Ns + K_{PD}K_{VCO}L(s))} \quad (2.41)$$

$$\frac{\phi_{out,VCO}(s)}{\phi_{VCO,n}(s)} = \frac{1}{1+H_O(s)} = \frac{1}{Ns + K_{PD}K_{VCO}L(s)} \quad (2.42)$$

$$\frac{\phi_{out,div}(s)}{\phi_{div,n}(s)} = -N \cdot \frac{H_O(s)}{1+H_O(s)} = \frac{-NK_{PD}K_{VCO}L(s)}{Ns + K_{PD}K_{VCO}L(s)} \quad (2.43)$$

Where $\phi_{out,ref}$, $\phi_{out,cp}$, $\phi_{out,LPF}$, $\phi_{out,VCO}$ and $\phi_{out,div}$ are the PLL output phase noise caused by the reference, the PFD/CP, the low pass filter, the VCO and the divider. (2.42) shows that the VCO phase noise is high-pass filtered by PLL. This means that the noise from the VCO at lower frequencies can be corrected relatively fast by the PLL. When the frequency goes higher and higher, the loop gain of the PLL becomes so small that it cannot correct any noise-induced phase deviations from VCO. In this case the loop is not fast enough and is essentially an open loop.

On the other hand, noises from the reference, the PFD, the charge pump and the divider are low-pass filtered at the PLL output. This means the noise contributions from these sources are referred to the output enhanced in effect by N at low offset frequencies from the carrier, and suppressed at high offset frequencies from the carrier.

Thermal noise of resistor R_2 is the only noise source inside the loop filter. The thermal noise of a resistor R can be modeled by a series voltage source, with the one-sided spectral density given by

$$\overline{V_n^2}(f) = 4kTR \quad (2.44)$$

where k is the Boltzmann constant. By expanding (2.41), the noise due to R_2 is given by

$$\phi_{VCO} = \frac{sK_{VCO}\sqrt{4kTR_2}}{s^2 + s\frac{I_{CP}K_{VCO}R_2}{2\pi N} + \frac{I_{CP}K_{VCO}R_2}{2\pi NC_2}} \quad (2.45)$$

(2.45) shows that the thermal noise of R_2 is band-pass filtered at the PLL output, which is proportional to the square root of R_2 . As the value of R_2 increases, the noise gets increased. However, for the same phase margin, an increase of R_2 results in the reduction of the loop filter capacitors. Therefore, there is a trade-off between phase noise and chip area in the selection of R_2 . The practical criterion is that the phase noise of R_2 should not be larger than phase noise of the VCO outside the loop bandwidth. The thermal noise on the VCO control voltage is given by,

$$\sqrt{V_{n,ctrl}^2} = \frac{C_2}{C_1 + C_2} \sqrt{\frac{1}{1 + \left(\omega R_2 \frac{C_1 C_2}{C_1 + C_2}\right)^2}} \cdot \sqrt{V_{n,R_2}^2} \quad (2.46)$$

In the narrow-band frequency modulation [18], when a sinusoid signal with amplitude A_m and frequency ω_m modulates a VCO, the output sidebands fall at ω_m away from the carrier. The amplitude of the sidebands is expressed as $A_m K_{VCO} / (2\omega_m)$. Therefore, the phase noise at VCO due to R_2 is given by,

$$\phi_{R_2} = \left(\frac{C_2}{C_1 + C_2} \right)^2 \frac{1}{1 + \left(\omega R_2 \frac{C_1 C_2}{C_1 + C_2} \right)^2} \cdot 2kTR_2 \cdot \left(\frac{K_{VCO}}{2\omega} \right)^2 \quad (2.47)$$

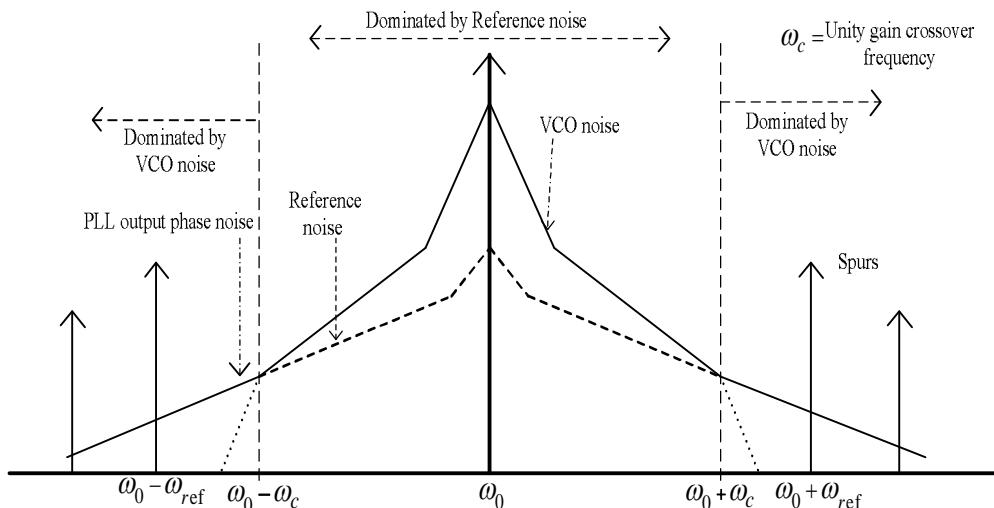


Fig. 2.9 PLL output spectrum

Generally a high quality reference source should be used in a PLL synthesizer which has better noise performance than that of the oscillator. The possible output spectrum of the PLL with both reference noise and VCO noise is shown in Fig. 2.9. It shows that noise close to carrier is dominated by the CP, the reference signal, the PFD and the divider, where the noise far away from the carrier is dominated by the VCO. To obtain better noise performance, the loop filter should be properly optimized. Reference spurs are other undesirable signals besides phase noise which can severely affect the performance of the synthesizer. As shown in Fig. 2.9, the output has some sidebands which are mainly created due to the sampling by the PFD block during the phase comparison. The locations of these sidebands depend on the input reference signal frequency.

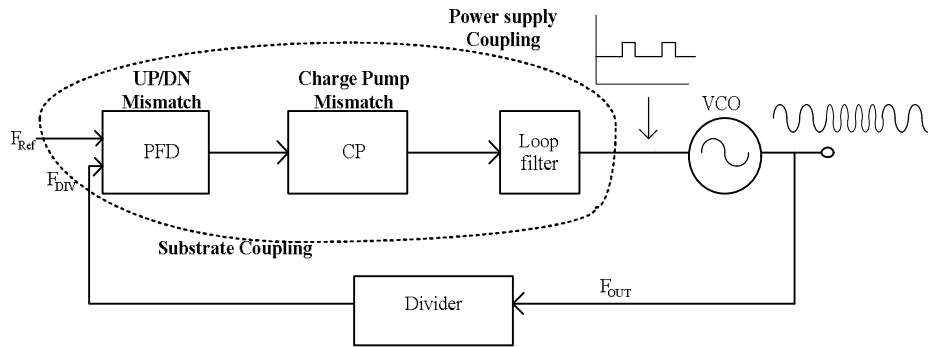


Fig. 2.10 Sources of Reference spur in synthesizer

Reference spurs [19] appear in the sidebands mainly due to the coupling of the reference frequency to the VCO control voltage, the UP and DN mismatch of the PFD, the charge injection mismatch of charge pump, the substrate and power supply coupling as shown in Fig. 2.10. Due the coupling of the reference signal to the control voltage, the VCO output is modulated by the periodic disturbance from the coupling.

2.4. Types of Frequency Synthesizers

From the above study and analysis, the PLL output frequency could be programmed by setting frequency division ratio to different values. Indeed, the PLL based frequency synthesizer is the most widely used frequency synthesizer approach in modern wireless communications systems.

2.4.1. Integer-N Frequency Synthesizer

An integer-N frequency synthesizer consists of integer-N divider with integer division ratios. The advantage of this type of synthesizer is the robust design of the frequency dividers. The most commonly used integer-N divider is pulse-swallow divider as

shown in Fig. 2.11.

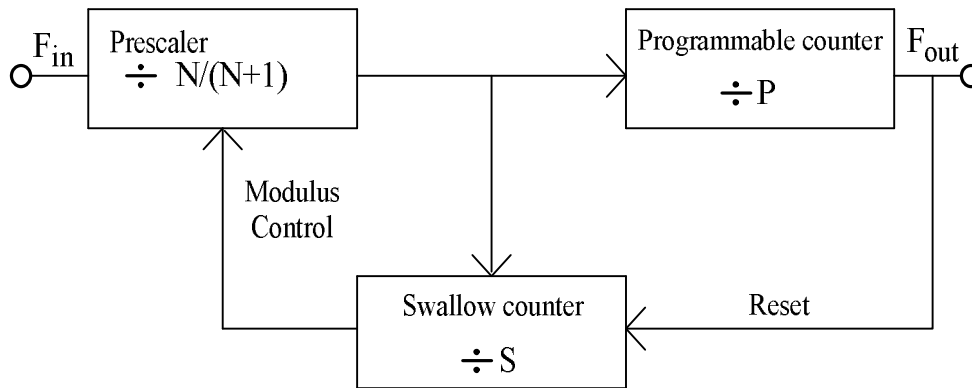


Fig. 2.11 Pulse-swallow frequency divider

A detailed analysis of the pulse-swallow divider [16] is discussed in the Chapter 3. Here, the PLL output is the integer multiple of the reference frequency and the finest PLL output frequency change equals to the reference frequency. Therefore, the required frequency spacing sets the upper-limit of the reference frequency. This results in the limited bandwidth, larger settling time and high close-in output phase noise.

2.4.2. Fractional-N Frequency Synthesizer

In a fractional-N frequency synthesizer [15], the smallest frequency step can be a fraction of the reference frequency. A simple fractional divider is shown in Fig. 2.12 which consists of a $N/(N+1)$ dual-modulus divider and a modulus control unit. The modulus control unit sets the instantaneous division ratio to either N or $N+1$ ratio so that the division ratio is a fractional number between N and $N+1$. If the division ratio is N for P cycles of the output and $N+1$ for Q cycles of the output, the equivalent

division ratio is equal to $(PN+Q(N+1))/(P+Q)$.

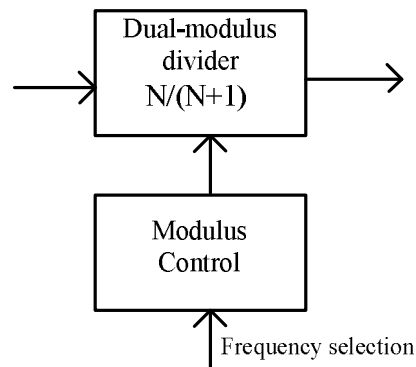


Fig. 2.12 A fractional frequency divider

Since the output is obtained by averaging instant ratios over time, the spectrum of divider output contains spurious tones called fractional spurs at the output of the PLL. The problem is severe when P and Q are constant over time. To address this issue, a delta-sigma modulator has introduced in place of modulus control unit which transforms the fractional spurs to random noise. However, this approach increases the complexity and power consumption.

2.4.3. Direct Digital Synthesizer

A direct digital synthesizer (DDS) generates carrier frequency very fast by removing the feedback as shown in Fig.2.13. A DDS generates the signal in the digital domain through an accumulator and a read-only memory (ROM), which is converted to analog waveform by digital-to-analog converter (DAC). Spurious harmonics at the output of DAC are filtered out by low pass filter (LPF). Since this architecture employs no feedback, settling time is very fast. The main advantages of DDS are low

phase noise, fine frequency steps and no stability issues.

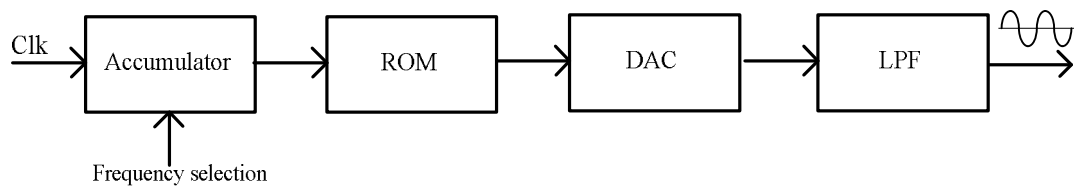


Fig. 2.13 A direct digital synthesizer

The main drawback of DDS is its low output frequency due to the practical speed limit of the DAC. To reconstruct the analog waveform correctly, the clock frequency has to be no less than twice of the output frequency (Nyquist's theorem). In RF applications, to have all the digital blocks of DDS work at least twice the carrier frequency is very difficult to achieve. The non-idealities of DAC are also major concerns.

2.5. Frequency Synthesizer Building Blocks

2.5.1. Phase detector/Phase Frequency Detector (PD/PFD)

A phase detector (PD) is a circuit whose average output ($\overline{V_{out}}$) is linearly proportional to the phase difference ($\Delta\phi$) between its two inputs. In an ideal case, the relationship between $\overline{V_{out}}$ and $\Delta\phi$ is linear, crossing the origin for $\Delta\phi=0$. The gain of the PD is K_{PD} expressed in V/rad.

A. XOR Based PD

A familiar example of phase detector is the exclusive OR (XOR) gate [16] as shown in Fig.2.14. As the phase difference between the inputs varies, so does the

width of the output pulses, thereby providing a dc level proportional to $\Delta\phi$. The XOR PD produces error pulses on both rising and falling edges. Fig.2.14c shows the transfer characteristics of the XOR PD.

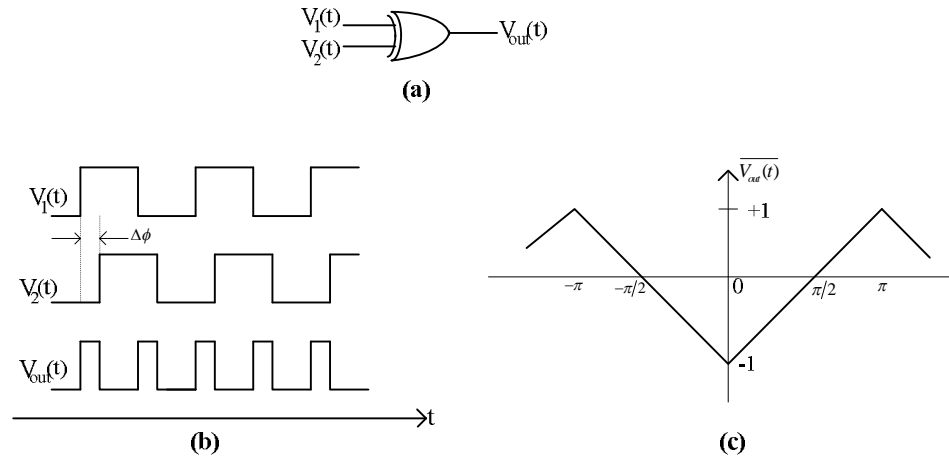


Fig. 2.14 XOR phase detector and phase characteristics

The major drawback of XOR PD is its inability to detect frequency difference. As any frequency difference exists, the phase difference would be accumulated either in a positive direction (reference frequency slower than divider frequency) or in a negative direction (reference frequency faster than divided frequency). As shown in Fig. 2.14c, the transfer function of PD is symmetrical over y-axis due to which it fails to differentiate the polarity of phase difference, and thus the frequency difference. The second issue is that, when the PLL is locked, the average of XOR PD output is zero. This zero voltage is averaged from a square wave of twice the reference frequency. Therefore, the pole of LPF has to be low enough to attenuate this reference spur. The XOR PD is sensitive to the duty cycle of the input signals.

B. D flip-flop Based PD

A simple D flip-flop (DFF) could also be used as a phase detector. Here, the reference signal serves as a clock to sample the divided VCO signal. When reference leads the feedback divider signal, the output remains at logic '1' and if the reference lags the feedback divider signal, the output switches to logic '0'. Therefore, the DFF based PD operation is highly nonlinear and leads to the stability issue and phase error. This PD also fails to detect any frequency difference.

C. Tri-State Phase Frequency Detector (PFD)

The EXOR and DFF based PD's fail to detect the frequency difference and are not suitable for PLL applications where initial VCO oscillation frequencies are far away from reference. A tri-state PFD [20] detects both phase and frequency difference.

Fig.2.15 shows the state diagram and the implementation of the PFD.

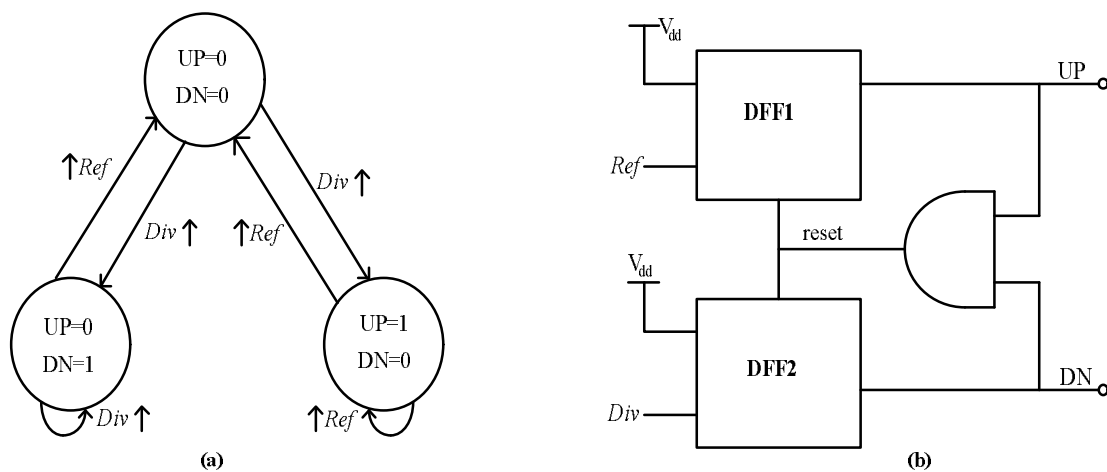


Fig. 2.15 Tri-state PFD a) state diagram b) implementation

Let Ref be the reference signal, and Div the divider output signal. If Ref leads Div , the rising edge of Ref triggers DFF1 and the UP signal is switched from 0 to 1 and DN signal remains at 0. The UP signal remains at 1 until the occurrence of rising edge of Div which triggers DFF1 and the UP signal is reset to 0 by the AND gate. A similar behavior happens when Ref lags Div . The phase difference between Ref and Div is indicated by the difference between UP and DN signals.

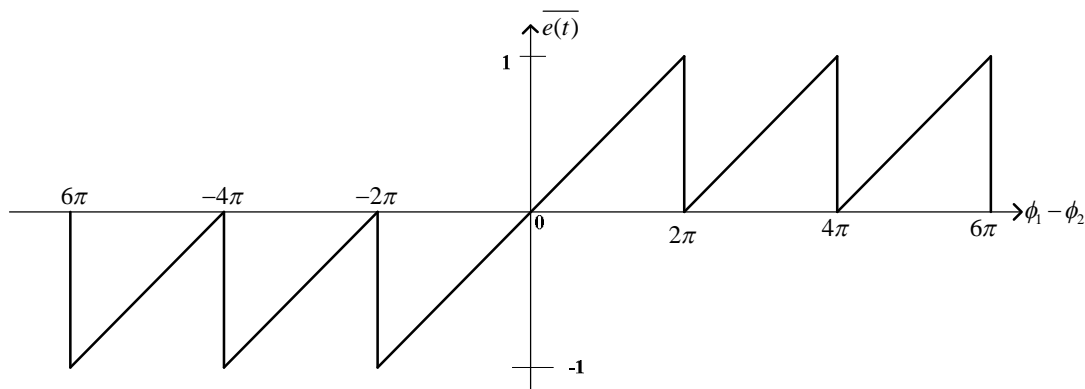


Fig. 2.16 Transfer characteristics of a tri-state PFD

Fig.2.16 shows the transfer characteristics of a tri-state PFD which is unsymmetrical over y-axis and the output has the same sign as that of the phase difference. Therefore, the output would be in opposite polarities between positive and negative frequency difference. When Ref leads Div ($f_{Ref} > f_{Div}$), the resulting positive pulses appear at UP while DN stays at 0. When Ref lags Div ($f_{Ref} < f_{Div}$), the resulting positive pulses appear at DN while UP stays at 0. Thus, the average of $UP-DN$ suggests the frequency difference.

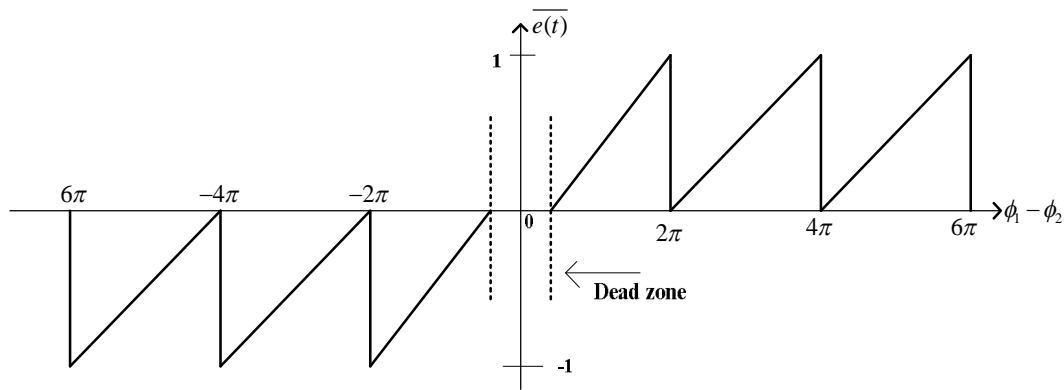


Fig. 2.17 Dead zone in tri-state PFD

However, tri-state PFD suffers from the “dead zone” problem [19]. The transfer function curve under the dead zone is given in Fig.2.17. When the phase difference between Ref and Div is close to zero, the width of the UP and DN pulses would approach to a minimal, which is set by the delay of the AND gate in the feedback path. However, the charge pump may not be to detect such narrow pulses, resulting to no current injecting to the LPF, which is almost similar to the case of zero phase difference. As a result, the PFD gain is down to zero and the PLL loop would not function and there would be an unpredictable phase error between the two inputs so the jitter at output of the PLL accumulates. The dead zone in the PFD is avoided by introducing delay after the AND gate in the feedback path to increase the propagation delay as shown in Fig.2.18. However, this technique increase the charge pump mismatch current causing reference spurs.

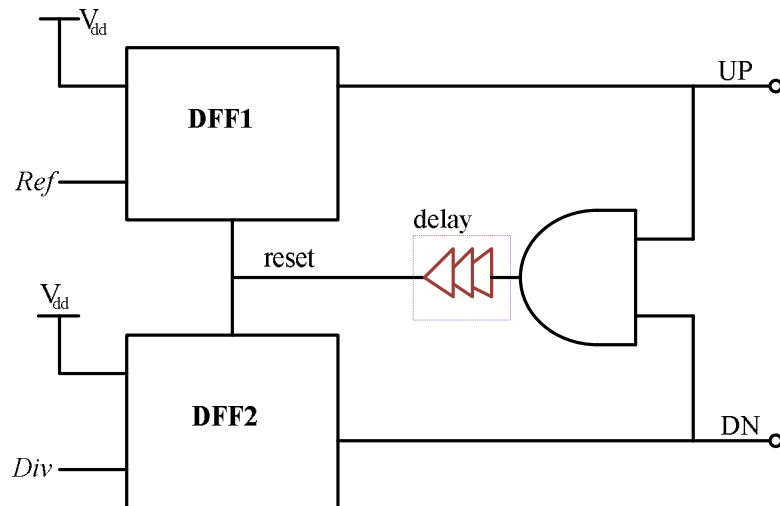


Fig. 2.18 Dead zone free PFD

2.5.2. Charge Pump

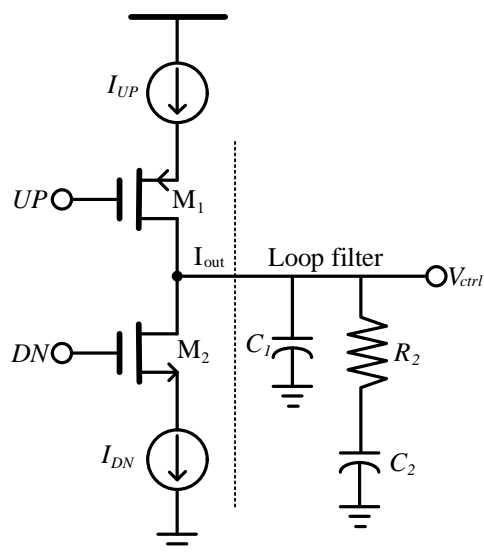


Fig. 2.19 Charge pump with loop filter

A charge pump [21] generally consists of two current sources that are switched on and off at the proper instance of time. When Ref leads Div ($f_{Ref} > f_{Div}$), the resulting positive pulses appear at UP while DN stays at 0. Under this condition, M_1 is turned-on and M_2 is turned-off such that the current I_{UP} charges the loop filter to pull-up the VCO frequency as shown in Fig.2.20a. When Ref lags Div ($f_{Ref} < f_{Div}$),

the resulting positive pulses appear at UP while DN stays at 0. Under this condition, M_1 is turned-off and M_2 is turned-on such that the current I_{DN} discharges the loop filter to pull-down the VCO frequency as shown in Fig.2.20b. Under locked condition when Ref is equal to Div ($f_{Ref} = f_{Div}$), both switches M_1 and M_2 are on for a short period equal to the dead zone pulse width and net current flowing into the loop filter is negligible.

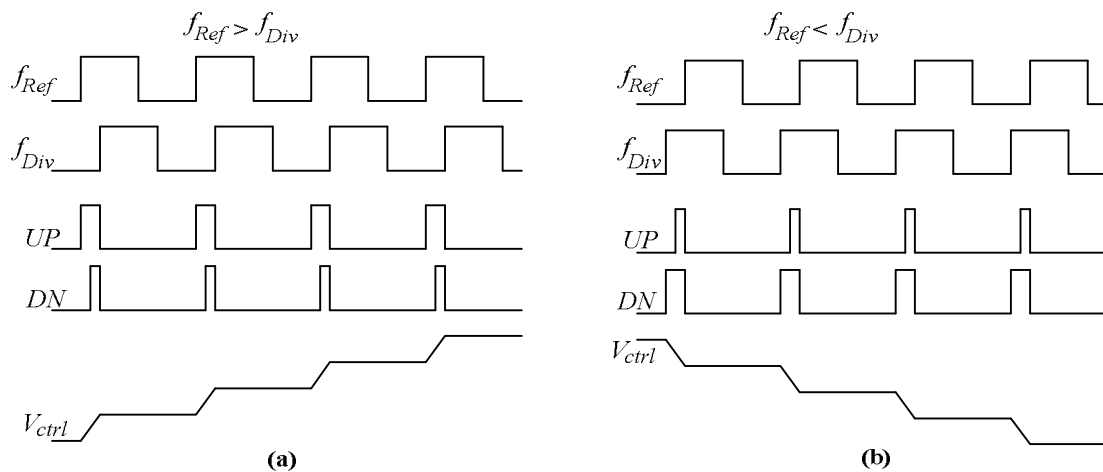


Fig. 2.20 Charge pump transient analysis a) Ref leads Div b) Ref lags Div

Most charge pumps are based on single ended architectures [22] and the UP and DN switches can be implemented in various positions as shown in Fig.2.21. In Fig.2.21a, the switches are placed at the gate of the current mirror transistors M_2 and M_3 . When DN switch is turned-on, M_3 is turned-off. As the switch DN is not ideal and has some finite on-resistance, a bias current flows through it. Since the gate voltage of M_3 is not at the virtual ground, the transistor M_3 is not completely turned-off, but operates in the sub-threshold region causing a leakage current through M_3 . One way to reduce the leakage current is to minimize the charge pump current (I_{cp}) and this

results in the degradation of switching time as the trans-conductance (g_m) of bias transistors M_1 and M_4 are decreased. Another issue with this architecture is the charge sharing between drain capacitances of M_2 and M_3 and loop filter capacitances.

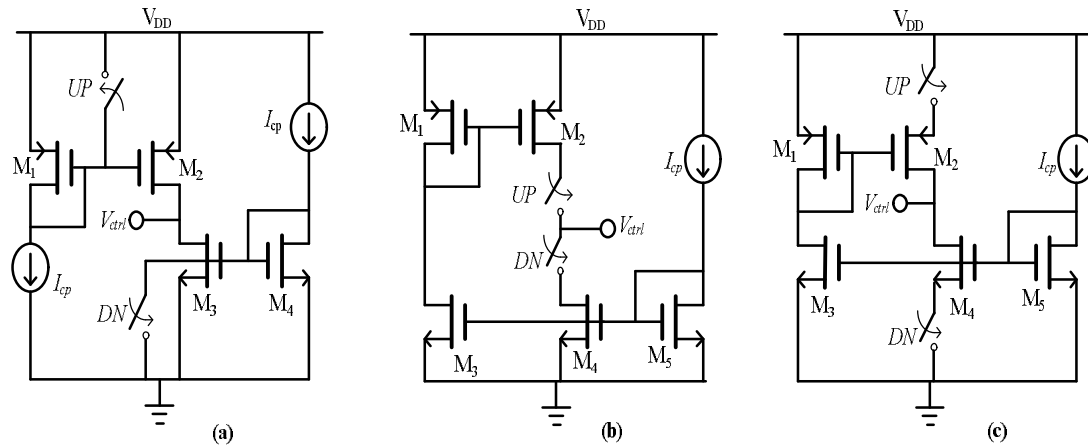


Fig. 2.21 Charge pump architectures with switches at a) gate b) drain c) source

In Fig.2.21b, the switches are placed at the drain of the current mirror transistors M_2 and M_4 . This architecture also suffers from the charge sharing problem and also the switches are not fast as they are directly connected to the loop filter. If switch DN is turned-on, M_4 is triode region initially leading to a low impedance path between the output and ground, which draws a large current and produces large current spikes.

In Fig.2.21c, the switches are placed at the source of the current mirror transistors M_2 and M_4 . In this architecture, the charge pump current can be very small since the switching time is not affected as the bias transistors M_3 and M_5 are not connected to the switches. In the off-state, DN switch could be at virtual ground and output impedance is larger than other mentioned architectures since it results from

series connection two off transistors and thus the leakage current is minimal. Since M_2 and M_4 are always in saturation, there exist no current spikes. However, all the above discussed architectures suffer from skew problems as the *UP* and *DN* switches are implemented PMOS and NMOS transistors. This skew problem can be solved by using similar kind of switches as shown in Fig.2.22 where the *UP* and *DN* switches are implemented by NMOS transistors. The main drawback of this architecture is the increased power consumption.

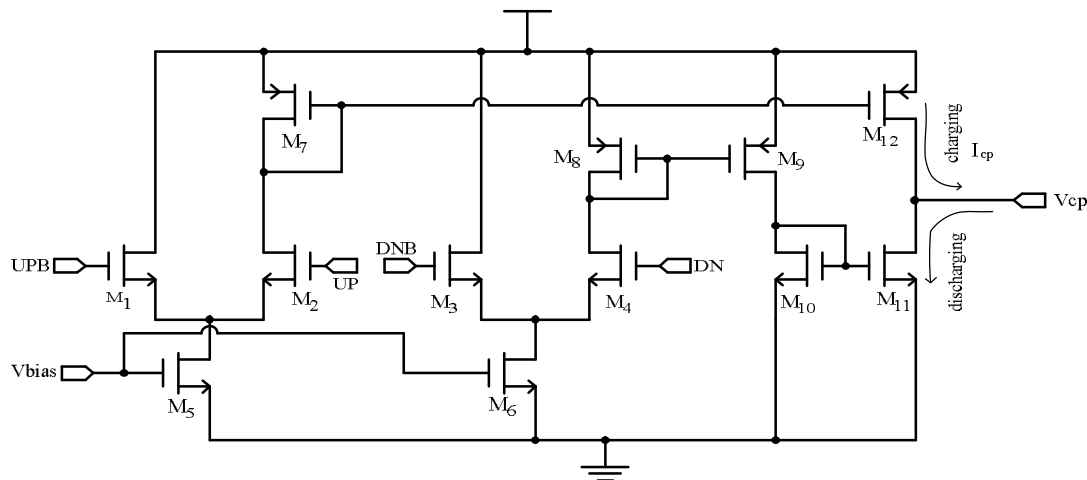


Fig. 2.22 Schematic of the charge pump

2.5.3. Voltage Controlled Oscillator (VCO)

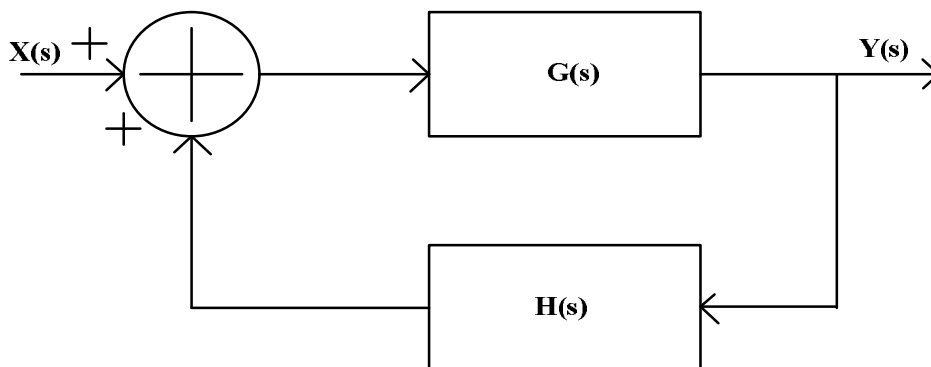


Fig. 2.23 Feedback oscillatory system

The voltage controlled oscillator (VCO) is an important building block of a PLL

synthesizer which generates periodic signals. Consider a linear feedback system shown in Fig.2.23 and its transfer function is given by [16],

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 - G(s)H(s)} \quad (2.48)$$

Oscillation happens if a stable periodic signal is produced and in the steady state, Barkhausen's criteria must be satisfied at ω_0 [16]:

- (1) The loop gain $|G(s)H(s)| \geq 1$
- (2) The total phase shift around the loop, $\angle G(s) + H(s) = 0^\circ$ or 360°

While Barkhausen's criteria explain the steady state of the VCO, it does not give hints on how the VCO converts its own noise in to periodic signal with certain amplitude. Actually, during oscillation start-up, the loop gain $|G(s)H(s)|$ must be larger than unity to amplify noise at ω_0 . The nonlinearity of VCO would eventually limit the amplitude of the signal to a certain level, arriving at the steady state when the average loop gain is unity. Commonly, both ring oscillators and LC oscillators are used in GHz range applications [23]-[26]. However, ring oscillators suffer from poor phase noise compared to that of LC oscillators and are less suitable for high-end wireless communication systems. LC oscillators are more attractive due to their better phase noise performance and lower power consumption. However, they occupy larger area compared to that of ring oscillators.

2.5.3.1. LC Oscillator

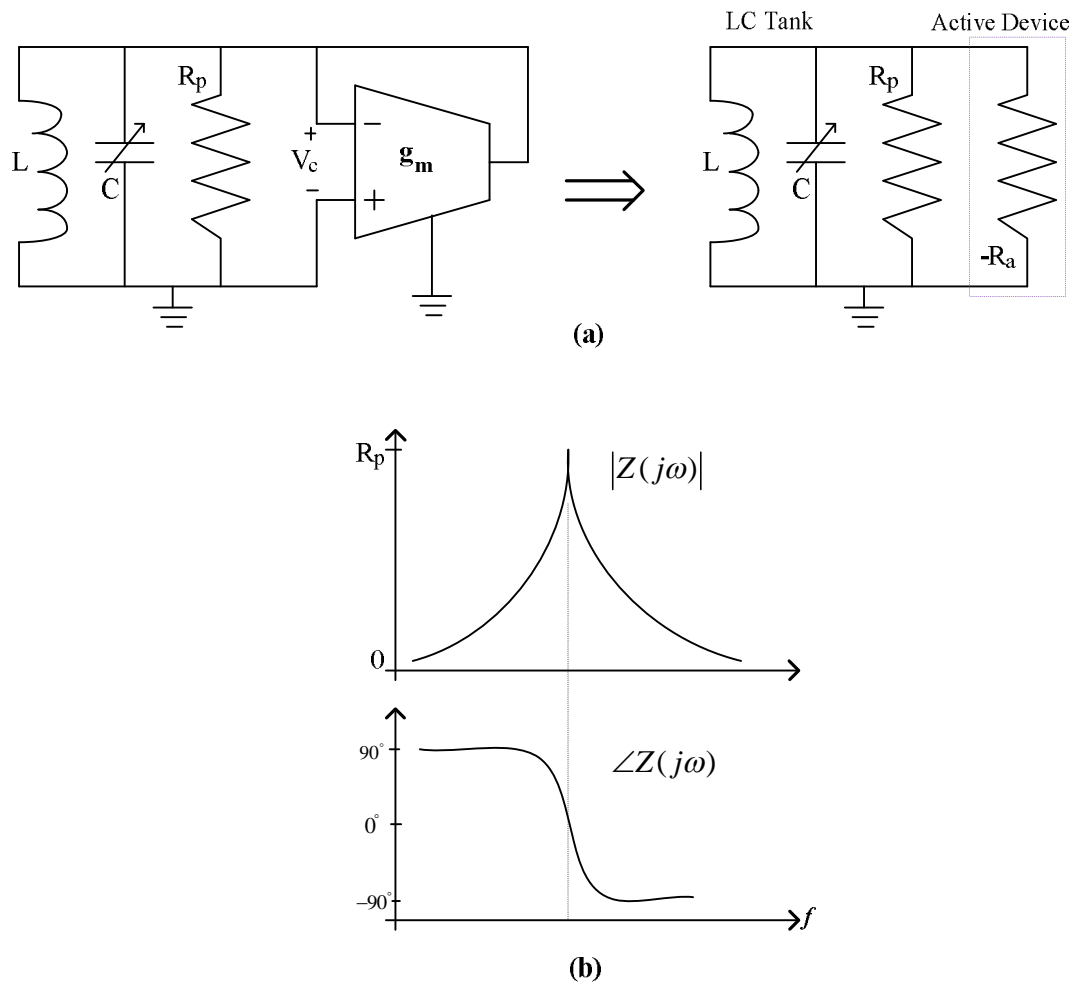


Fig. 2.24 LC VCO a) parallel LC model b) magnitude and phase of the tank

A resonator based LC VCO has a LC tank as a frequency selective circuit consisting of inductors and capacitors. The energy loss in the tank is compensated by the active devices. Fig.2.24a shows a model of a parallel LC oscillator where R_p is the equivalent parallel resistor of the LC tank and C is a varactor whose capacitance is controlled by the voltage V_c . Here, the positive resistor R_p models the resistive loss of the tank, and the negative resistor $-R_a$ models the active device. Once the energy loss is equal to the energy provided by the active device, a stable oscillation can be

sustained [27]. The resonant characteristics of $Z(j\omega)$ are shown in Fig.2.24b and it is observable that the effective impedance of the LC tank is purely real at resonance, which is equal to the effective resistance of the tank R_p . The resonant frequency ω_0 is given by,

$$\omega_0 = \frac{1}{2\pi\sqrt{LC}} \quad (2.49)$$

The phase conditions of Barkhausen's criteria are satisfied and the magnitude condition can be achieved by setting $R_a/R_p \geq 1$. In general, R_a is kept at least 2 times higher than R_p for start-up oscillation and stable oscillation [28]. The quality factor Q of the LC tank is given by,

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy dissipated per cycle}} = \frac{R_p}{\omega_0 L} \quad (2.50)$$

The higher quality factor Q means lower VCO phase noise. A good phase noise model is the most important specification for low phase noise VCO design.

2.5.3.2 Inductors

The inductor is a key element in determining the performance of an LC oscillator. The requirement for a good inductor is its inductance, low series resistance, low substrate losses, small area and high self-resonance frequency. A smaller series resistance along with lower substrate losses improves the Q value and thus the phase noise of a VCO.

On-chip inductors for LC VCOs are widely been reported in the literature [29]-[31].

The most popular approach is the spiral inductor made of the metal track available in the standard digital CMOS process.

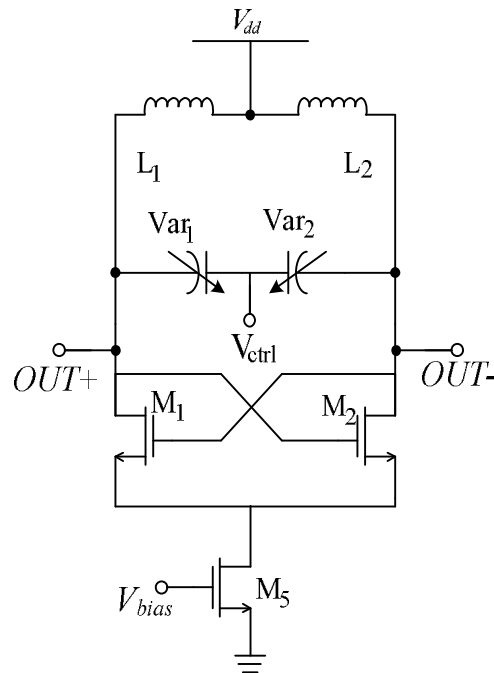


Fig. 2.25 Schematic of an LC VCO

A spiral inductor can be made of a single metal layer or multiple metal layers.

The multi-layer series spiral inductor has been used due to its smaller chip area compared with the single layer spiral inductor. The substrate coupling effect is alleviated with smaller chip area and also reduces the series resistance of the metal tracks. If a single metal layer is opted, top metal is used since it is the farthest metal layer from the conductive substrate and also thickest metal layer. The top metal has smallest resistance due to its thickness and also reduced magnetic coupling with conductive substrate. These are the two factors that help to increase the quality factor.

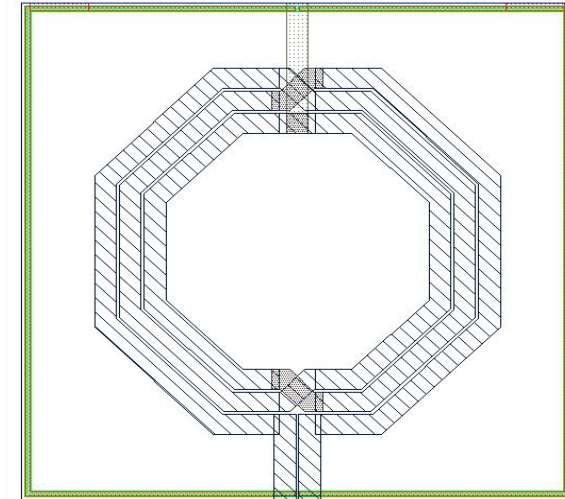


Fig. 2.26 An octagonal differential inductor

Most of the LC VCOs reported in literature use the cross-coupled differential pair architecture which requires two separate inductors [25] as shown in Fig.2.25. If the distance between the inductors is large, the mutual coupling between inductors reduces and the common mode impedance increases which leads to an increment of common mode noise. Alternatively, the two inductors can be replaced by a single differential inductor. A differential inductor offers a higher quality factor than two independent spiral inductors in series do. A typical differential inductor layout is shown in Fig.2.26 and it occupies about the same area of a single inductor. The common mode impedance is reduced by the strong coupling between the windings [29], which consequently improves the signal symmetry and reduces the flicker noise [32].

2.5.3.3 Varactors

The two most popularly used varactors in the design of LC VCO are the diode

varactor and MOS varactor. The diode varactors are less attractive for two reasons. Firstly, the p-n junction suffers from a limited tuning range due to non-linearity in the C-V characteristics. The capacitance varies slowly under the reversed bias and sharply under the forward bias. Secondly, at low supply voltages, it becomes increasingly more difficult to select the oscillator common-level and signal swings so as to avoid forward biasing the diodes.

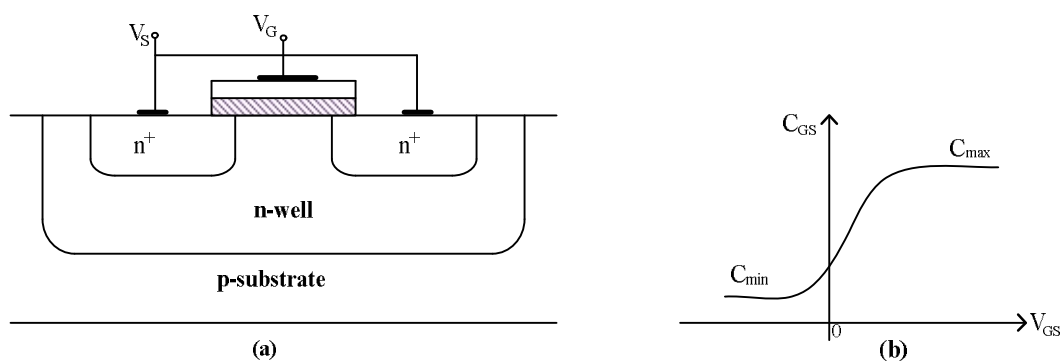


Fig. 2.27 MOS varactor a) structure b) C-V characteristics

The other commonly used varactor is accumulation-mode MOS varactor (A-MOS). The A-MOS varactor is implemented by using a P-channel MOSFET in a p-well/substrate or an n-channel MOSFET in an n-well. As shown in Fig.2.27a, both the drain and source are connected together and by varying the gate-to-well voltage from positive to negative value, the device goes from the deep accumulation to the deep depletion region while the capacitance of the varactor drops. If V_G is below V_S , the electrons in the n-well are repelled from the silicon/oxide interface and a depletion region is formed. Under this condition, the equivalent capacitance is given by the series combination of the oxide and depletion capacitances. If V_G exceeds V_S , the

interface attracts electrons from the n+ source and drain terminals, creating a channel between them. Fig.2.27b shows the C-V characteristics of A-MOS varactor. To achieve a good Q, more gate fingers should be used and the gate length should be minimized. The A-MOS varactor is however less linear over the tuning voltage than the PN-junction varactor. As a result, the disadvantage of the using the A-MOS varactor is the non-linearity [33].

2.5.3.4 LC VCO Topologies

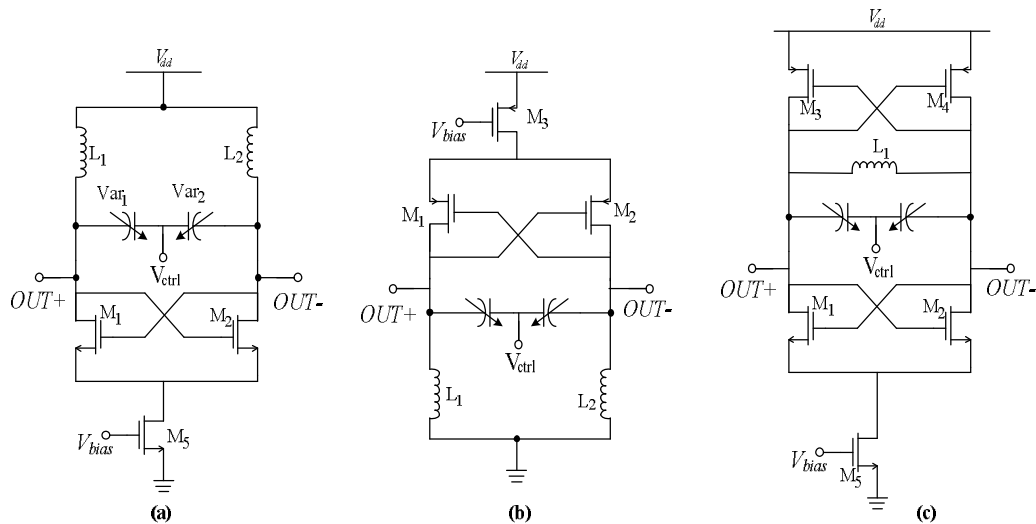


Fig. 2.28 LC VCO a) NMOS only b) PMOS only c) complementary VCO

Cross-coupled LC oscillators play an important role in high frequency circuit design. It includes either NMOS-only or PMOS-only, or complementary cross-coupled structures as shown in Fig.2.28. The inductors and varactors forming the LC tank have to be symmetrical from both sides in order to ensure a true differential circuit. The single differential NMOS-only or PMOS-only oscillators operate in the current limited region [26] for low power supply voltage. Here, the tail current source

determines and keeps the oscillation amplitude not beyond the supply voltage.

The complementary differential topology as shown in Fig.2.28c uses cross-coupled PMOS in addition to the NMOS. Here, the LC tank is connected to the output nodes to ensure symmetry. The complementary topology offers several advantages.

- (1) For the same amount of bias current, g_m of this architecture is doubled compared to NMOS or PMOS only topology, which results in the better phase noise performance. It also improves the switching of the cross-coupled pair [27].
- (2) The cut-off frequency f_T of NMOS and PMOS transistors can be improved since the gate capacitors of both NMOS and PMOS are reduced to half.
- (3) Due to symmetrical architecture (better rise and fall time), the up conversion of $1/f$ noise improves.

However, this architecture suffers from headroom issues and is less suitable for operation with low supply voltages.

2.5.3.5 VCO Phase Noise Model

A. Leeson's Model

One of the most well-known models of the phase noise in oscillators is Leeson's model proposed by D.B. Leeson in 1966 [34]. This model is heuristically derived

without any formal proof and is based on linear time invariant analysis. From Fig.2.23a, if $\Delta\omega \ll \omega_0$, the impedance of the parallel RLC is given by,

$$Z(j\omega) = Z(j(\omega_0 + \Delta\omega)) = -jR_p \frac{\omega_0}{2Q\Delta\omega} \quad (2.51)$$

The total equivalent parallel resistance of the tank has an equivalent mean square noise current of $\overline{i_n^2}/\Delta f = 4kT/R_p$, where k is Boltzmann constant and T is absolute temperature. Considering all noise sources rather than thermal noise, Leeson gave a multiplicative factor F . The phase noise is given by,

$$L\{\Delta\omega\} = 10 \log \frac{\overline{v_n^2}/\Delta f}{2v_{sig}^2} = 10 \log \frac{4FkTR_p}{V_0^2} \cdot \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (2.52)$$

The factor $1/2$ is based on the equal partition of AM and PM noise. Finally Leeson modified the phase noise equation as to [34]:

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{4FkTR_p}{V_0^2} \cdot \left[1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right] \right\} \quad (2.53)$$

where an additive factor of unity inside the bracket is to account for the noise floor.

Leeson's phase noise model predicts the phase noise spectrum, which includes $1/(\Delta\omega)^3$, $1/(\Delta\omega)^2$, $1/\Delta\omega$ and the noise floor regions as given in Fig.2.29. In

Leeson's model, F is empirical varying significantly from oscillator to oscillator. With

the unspecified noise factor F , the model cannot predict phase noise from circuit noise analysis.

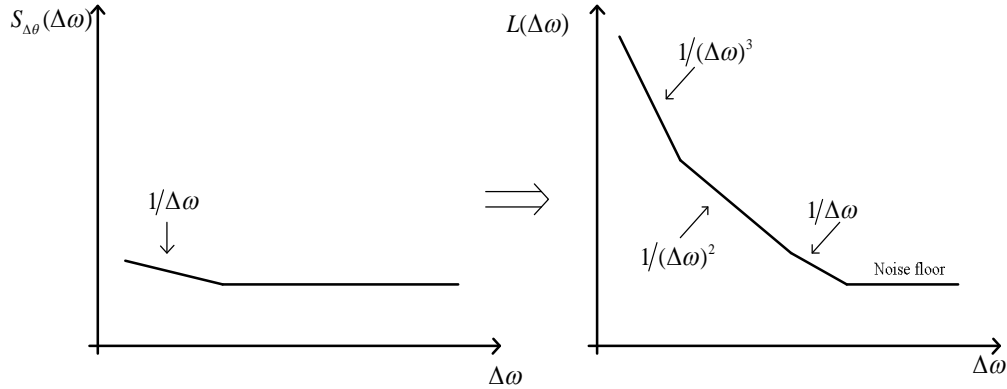


Fig. 2.29 Power spectral density of the input noise and the phase noise

B. Hajimiri's Model

A more precise analysis was proposed by A. Hajimiri and T. Lee in 1998 [32] which introduces the impulse sensitivity function (ISF) to consider the effects of nonlinearity, time-variance and cyclostationary noise. ISF describes how much phase shift results from applying a unit impulse at any point in time. The phase shift response to a unit impulse can be expressed as

$$h_{\phi}(t, \tau) = \frac{\Gamma(\omega_0\tau)}{q_{\max}} u(t - \tau) \quad (2.54)$$

Where $\Gamma(\omega_0\tau)$ is the ISF function, q_{\max} is the maximum charge displacement across the injected node capacitor and $u(t)$ is the unit step function. The excess phase is given by,

$$\phi(t) = \int_{-\infty}^{\infty} h(t, \tau) i(\tau) d\tau = \frac{1}{q_{\max}} \int_{-\infty}^t \Gamma(\omega_0 \tau) i(\tau) d\tau \quad (2.55)$$

where $i(\tau)$ is the injected current. Since ISF is periodic, the Fourier series is given by,

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau) \quad (2.56)$$

The injection of a sinusoidal current is written as $\Gamma(\tau) i(t) = I_m \cos((m\omega_0 + \Delta\omega)t)$, where m is integer. Ignoring other terms other than $n=m$, (2.55) can be re-written as,

$$\phi(t) = \frac{I_m c_m \sin(\Delta\omega t)}{2q_{\max} \Delta\omega} \quad (2.57)$$

By performing phase to voltage conversion, the sideband phase noise is given by,

$$L\{\Delta\omega\} = 10 \log \left\{ \frac{\overline{i_n^2} / \Delta f \sum_{m=0}^{\infty} c_m^2}{8q_{\max}^2 \Delta\omega^2} \right\} \quad (2.58)$$

where $\overline{i_n^2}$ is the spectral density of the input noise current and $\Delta\omega$ is the frequency offset from the carrier frequency. Hajimiri's ISF function provides a good way of modeling phase noise. Meanwhile this model has some practical limitations such as the complicated simulation process. However, it is highly simulation-based and it doesn't trace the phase noise to its original sources.

2.5.4 Frequency dividers

The frequency divider is one of the building blocks of a PLL frequency synthesizer

which converts the oscillator high output frequency to a lower frequency which can be compared to a reference source. As the VCO is operated in the multi-GHz range, the PLL requires high frequency dividers. However, the requirement of the channel selection in the frequency synthesizer demands a programmable frequency divider.

The four key design issues related to the design of the programmable dividers are the high input frequency, programmability of the division ratio, power consumption and input sensitivity (minimum amplitude of the input signal). In general, the power consumption of the divider is linearly proportional to the operating frequency. Its maximum operating frequency depends on the architecture style, supply voltage and output load. Dividers are classified into two types mainly, analog and digital dividers. The design of analogue dividers are based on the injection locking technique where as digital dividers are implemented using dynamic or static latches and flip-flops.

2.5.4.1. Analog Dividers

Analog frequency dividers are termed as injection locked frequency divider's (ILFDs) which are designed based on the injection locking technique proposed by Miller [35] in 1939. ILFDs can operate at relatively higher frequencies compared to that of static and dynamic dividers at the expense of the narrow locking range [36]. The main idea behind the injection locking division is to create an oscillator operating at the sub-harmonic of the input signal. Fig.2.30 shows a simple ILFD which consists of

mixer (injector), and a low pass filter. Miller divider can achieve a division ratio higher than two by using a frequency multiplicative element $X(N-1)$ in the feedback loop. The frequency multiplicative element represents the non-linearity present in the circuit.

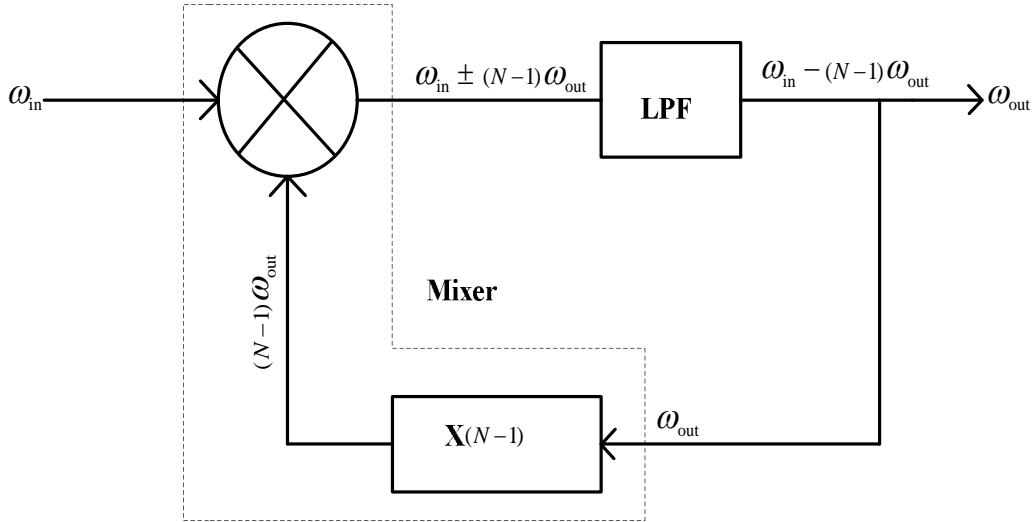


Fig. 2.30 Simplified injection-locked frequency divider

The mixer multiplies the input signal ω_{in} with the output signal (ω_{out}) and generates ($\omega_{in} \pm (N-1)\omega_{out}$). The high frequency component is filtered out by the LPF. If the total gain and the phase shift in the loop are respectively 1 and multiples of 2π , the output is given by (2.59).

$$\omega_{in} - (N-1)\omega_{out} = \omega_{out} \Rightarrow \omega_{out} = \frac{\omega_{in}}{N} \quad (2.59)$$

When the loop is locked, the output frequency (ω_{out}) will be synchronized with sub-harmonics of the input signal (ω_{in}/N). Hence, the output frequency follows the input frequency within locking range. As division ratio increases, the input frequency also increases and the injection efficiency decreases and degrades the

locking range. An ILFD can be designed using either a ring based VCO [37] or an LC VCO structure [38], [39]. However, there is no injection locked dual-modulus implemented in the design of divider in the literature thus far due to its poor locking range and complexity. Since our interest lies in 2.4 GHz band of operation, we have chosen to work on digital dividers. Thus power consumption and programmability are the two main design parameters for our design.

2.5.4.2. Digital Dividers

Digital frequency dividers which divide the input signal by N times are normally termed as modulo- N counters which can be classified as ring or binary counters. Binary counters are designed using memory elements such as either edge triggered J-K flip-flops which are decremented or incremented at each clock cycle. Ring counters are implemented using shift registers (D flip-flops). Here, the output of each shift register is connected in feedback to their input. Ring counters provide an individual digit output rather than a binary output.

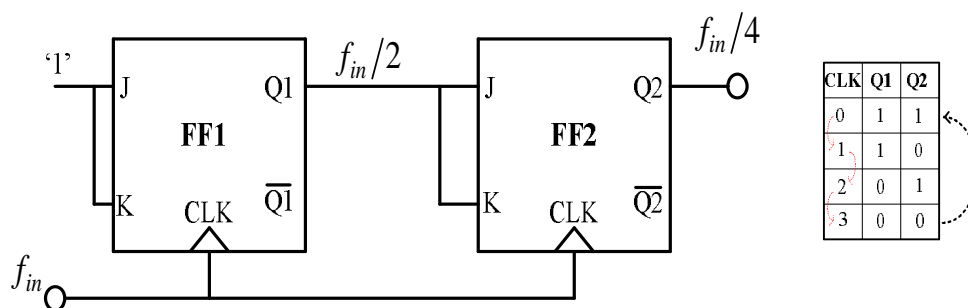


Fig. 2.31 Modulo-4 J-K flip-flop binary counter

Fig.2.31 shows the J-K flip-flop (FF) based modulo-4 binary counter with

each state following the sequential order. In FF1, J and K inputs are tied together to form a toggle flip-flop (T-FF) [40], [41] and connected to logic '1'. FF1 toggles its state at positive or negative edge of the clock (CLK) and divides the input frequency by 2. The J and K inputs of FF2 are connected to the output of the FF1 which toggles only when Q1 is high. Therefore, its output frequency is equal to the 1/4th of the input frequency. This counter is referred to as synchronous counter since both the flips are driven by the same clock.

Fig.2.32 shows the D flip-flop (DFF) based modulo-4 twisted ring or Johnson counter which produces 50% duty cycle unlike normal ring counter which needs four S-R flip-flops and uses only four states out of 16 possible states [19]. The inverted output of DFF2 is connected in feedback to the input of DFF1 such that the resulting Q1 is in quadrature with Q2. In this modulo-4 twisted ring counter, FF presetting is avoided since all the possible states are used. Since no additional logic gates are used, the maximum operating speed is higher than that of the normal ring counter.

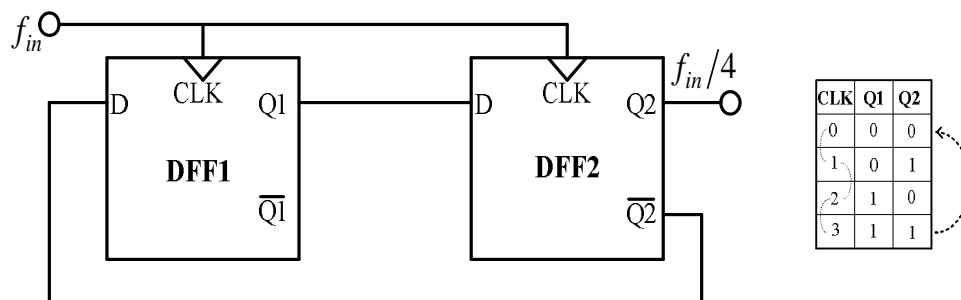


Fig. 2.32 Modulo-4 D flip-flop twisted ring (Johnson) counter

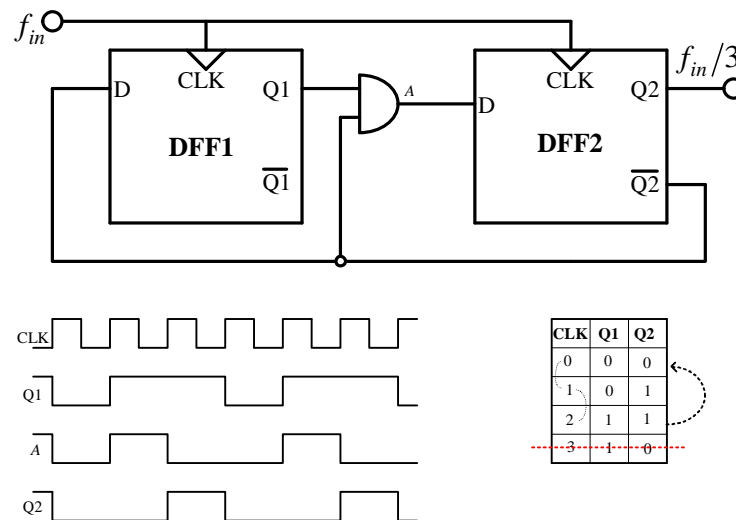


Fig. 2.33 Modulo-3 D flip-flop twisted ring (Johnson) counter

However, the Johnson counter requires additional logic gates to override unwanted states. For example, to achieve a frequency division by three an additional AND gate is required in between the two DFF's as shown in Fig.2.33. The AND gate added in the critical path overrides state "10" and yields only 3 valid states. The outputs of Q1 and Q2 are equal to $1/3^{\text{rd}}$ of input frequency with duty cycles equal to $2/3$ and $1/3$ respectively. If the counter begins with an invalid state (Q1Q2='10'), the following state will be valid and the counter will never enter the invalid state again. Since an additional gate is added in the critical path, the maximum operating speed of this counter is reduced.

In general, binary counters require additional logic gates to determine the change of state of each flip-flop even if the modulus is a power of two. If the division ratio is larger, the counter architecture becomes complex and impractical. The ring counter is preferred over the binary counter as it uses simple logic with no pre-settable

logic. Counters are generally built with flip-flops which are edge-triggered compared to latches which are level-triggered. The flip-flops are constructed using latches in master-slave configuration [41], [42]. Alternatively, counters can be designed using a single latch which results in higher speed and low power consumption. However, this approach has limited range of input frequencies [43].

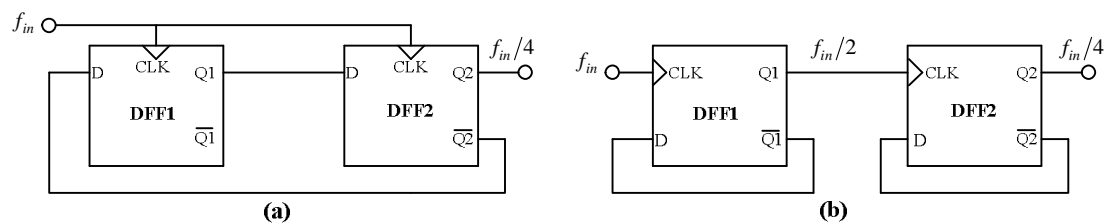


Fig. 2.34 Modulo-4 ring counter a) synchronous b) asynchronous

Fig.2.34 shows the modulo-4 ring counter based on synchronous and asynchronous architectures. In the synchronous counter, all the FF's are driven by the same clock which results in a lower operating speed and a high power consumption. In the asynchronous counter, the output of the first FF acts as clock for the second FF, which results in low power consumption and the maximum operating frequency is determined by the first FF. However in the asynchronous counter, the jitter accumulates as it passes through more FFs. In the synchronous counter, the jitter at the input propagates to the output since all FFs are clocked by the same clock signal.

2.5.4.3. Pulse-Swallow Divider

The counters described in section 2.5.4.2 are based on fixed integers while frequency

followed by the presettable modulo- P counter to give a total division ratio of $N \cdot P$. However, this technique limits the resolution of the programmable frequency divider to N . The best approach to design a fully programmable divider is based on the combination of both synchronous and asynchronous dividers as in the pulse-swallow divider [16] shown in Fig.2.36.

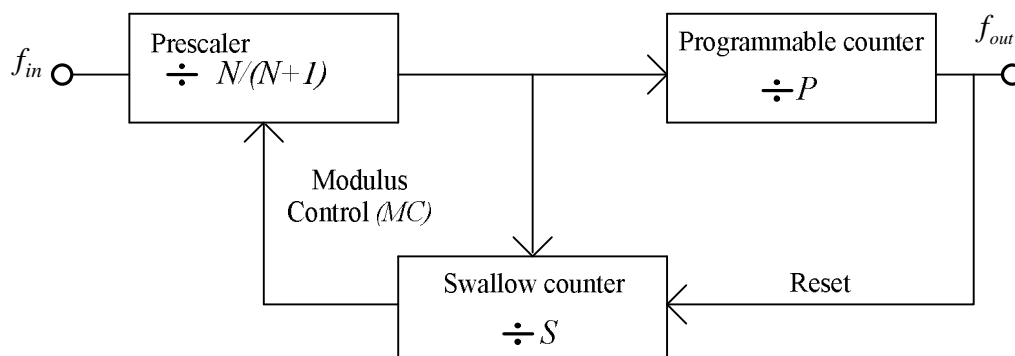


Fig. 2.36 Pulse-swallow frequency divider

The pulse-swallow frequency divider consists of a dual-modulus prescaler (DMP), a programmable (P) counter and a swallow (S) counter. The dual-modulus prescaler is based on both synchronous and asynchronous divider which scales the input frequency to a lower frequency to ease the complexity of asynchronous presettable modulo- P and modulo- S counters. In this technique, S input pulses are swallowed in the preceding arrangement such that the output period becomes longer by S reference periods. In the initial state, the modulus control (MC) signal remains at logic '0' and allows the DMP to operate in the divide-by- $(N+1)$ mode and the programmable P -counter and swallow S -counter are loaded to their initial states.

Since $P > S$, the S -counter reaches the final state earlier than P -counter and the end-of-count logic of the S -counter changes the MC to logic '1' allowing the DMP to switch to divide-by- N mode where the P -counter counts the remaining $(P-S)$ input periods of ' N '. Thus the total division ratio is given by

$$f_{out} = ((N + 1)S + N(P - S))f_{in} = (NP + S)f_{in} \tag{2.60}$$

From the circuit topology view point, prescalers and presettable counters are often implemented using different logic families, owing to their different speed specifications and a level shifter is required after the DMP to compensate different voltage rails.

2.6. Synthesizer specifications

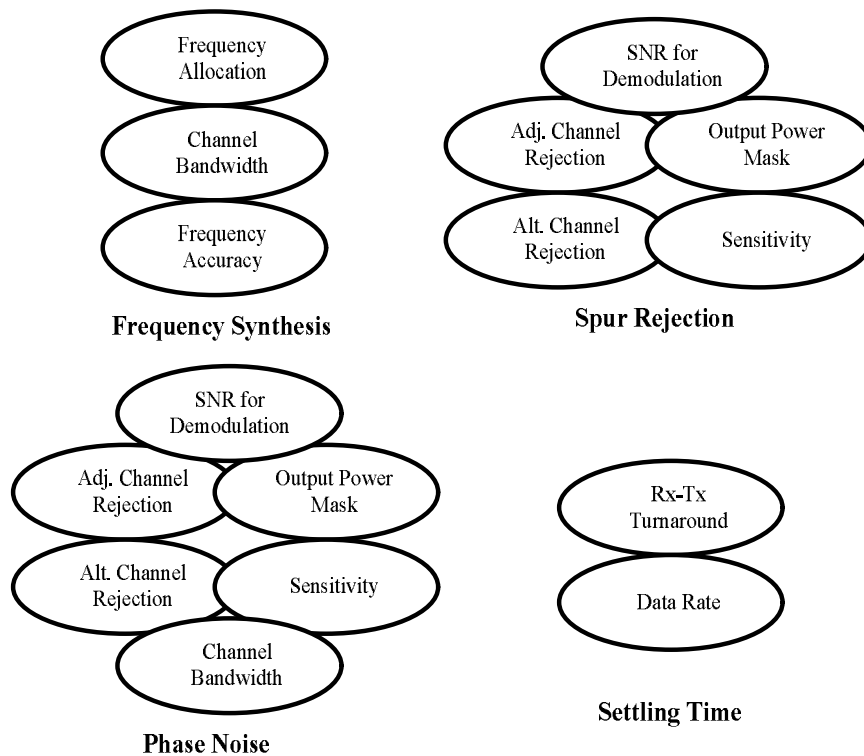


Fig. 2.37 mapping standard to synthesizer specifications

The mapping of key specifications from the standard is shown in Fig.2.37 and the specifications for the 802.15.4 synthesizer are derived below:

A. Frequency synthesis

The IEEE 802.15.4 standard has 16 channels, spaced 5 MHz apart from 2405 MHz to 2480 MHz. The synthesizer needs to synthesize 16 channel selection frequencies with 40-ppm frequency accuracy. If direct conversion is used in both the TX and RX, then the 16 channel selection frequencies would be from 2405 MHz to 2480 MHz in steps of 5 MHz. If a low IF architecture is used for the RX, then the channel selection frequencies could be different for the both TX and RX. In order to have more flexibility to accommodate channel selections for both kind of architecture, the resolution of the divider and reference frequency chosen is 1 MHz which give a resolution of 1 MHz to the channel selection frequency. For example, if the IF frequency is chosen to be 2 MHz, the divider is programmed to have the channel frequencies equal to 2403, 2408....2478 MHz or 2407, 2412....2482 MHz. For the IEEE 802.15.4 standard, the channel bandwidth is 2 MHz.

B. Phase Noise

In wireless systems, it is necessary to switch from one channel to another in time using multiple access approach. Depending on the LO frequency, the desired channel is down-converted with the LO signal and its phase noise. Since the power of the

blocking signal is much larger than that of the desired signal, the phase noise power falls into the IF frequency and degrades the signal to noise ratio (SNR). In the Zigbee PHY layer, the maximum contribution to co-channel interference is from the adjacent and alternate channels, spaced 5 MHz and 10 MHz apart from the channel of interest. According to [43], the required phase noise at a frequency offset determined by the frequency offset of P_{int} can be calculated by,

$$L_{req}(\Delta\omega) = ((P_{sig} - P_{int}) - SNR_{req} - 10\log(BW))(dBc/Hz) \quad (2.61)$$

Where P_{sig} is the power content of the carrier, P_{int} is the power content of the interferer and BW is the bandwidth of the channel. The system simulations in [44] shows that SNR_{out} should be at least 14 dB. The channel spacing is 5 MHz, so there would be a guard band on either side of the channel to prevent aliasing and minimize co-channel interference. The channel bandwidth is 2 MHz and the required phase noise is given by,

$$L_{req}(5MHz) = (0 - 0) - 14 - 10\log(2.10^6) = -77 dBc/Hz \quad (2.62)$$

$$L_{req}(10MHz) = (0 - 30) - 14 - 10\log(2.10^6) = -107 dBc/Hz \quad (2.63)$$

The required phase noise at 5 MHz offset and 10 MHz offset is found to be -77dBc/Hz, and -107dBc/Hz respectively. Assuming a margin of 10 dB due to non-idealities of the system, the required phase noise at 5 MHz offset and 10 MHz offset is -87dBc/Hz and -117dBc/Hz respectively.

C. Spur Rejection

Because of the feed-through and modulation of the reference signal, two spurious tones appear at the $\pm f_m$ away from the desired output frequency as shown in Fig.2.9. The down-converted spur contributes to the interference and worsens the SNR at the input of IF section. The required SNR at the input of the IF section is set at 14dB in our calculations. For IEEE 802.15.4 standard the channel spacing is 5 MHz and there is guard band on either side of the channel to prevent aliasing and minimize co-channel interference. In this design of integer-N PLL, the reference spurs occurs at an offset of 1 MHz, equal to reference frequency. The IEEE 802.15.4 standard specifies the adjacent channel interference of 0dB at an offset of 5 MHz, equal to channel spacing. We calculate the minimum reference spur level below the carrier (LO) required to obtain the SNR required at the input section of IF. Here, the spur is considered as a single tone and not as an integrated noise and expressed as,

$$\left(P_{spurs}\right)_{5MHz} = (P_{sig} - P_{int}) - SNR_{req} = (0 - 0) - 14 = -14 \text{ dBc} \quad (2.64)$$

$$\left(P_{spurs}\right)_{10MHz} = (P_{sig} - P_{int}) - SNR_{req} = (0 - 30) - 14 = -44 \text{ dBc} \quad (2.65)$$

Normally, the SNR_req is not combined in the calculation of spur and phase noise requirement. For the IEEE 802.15.4 standard, the required spur suppression is -14 dBc at 5 MHz offset, and -44 dBc at 10 MHz offset respectively.

D. Settling time

The IEEE 802.15.4 supports a data rate of 250 Kbps with each symbol consisting of 4-bits giving a symbol rate of 62.5 Ksymbols/sec. The maximum TX-Rx turn-around time is 12 symbol periods, which is equivalent to 192 us. Thus the worst case settling time of the synthesizer is estimated to be 192 us.

2.7. Literature Review

Table.2.1 Synthesizer performance comparison

Reference	[45]	[46]	[47]	[48]	[49]	[10]	[50]
Process	0.18um	0.2 um	0.25 um	0.18 um	90 nm	0.18 um	0.18um
Channel spacing	5 MHz	1 MHz	1 MHz	5 MHz	5 MHz	5 MHz	3 MHz
Frequency Range (GHz)	2.4-2.48	2.4	2.4-2.527	2.4-2.475	2.4-2.48	2.29-2.64	2.44-2.47
Loop filter	On-chip	Off-chip	On- chip	Off- chip	On-chip	On- chip	On- chip
Phase noise (dBc/Hz)	-108.55 @1 MHz	-104 @1 MHz	-112 @1 MHz	-116.5 @1 MHz	-106 @1 MHz	-130 @10MHz	-112 @1 MHz
Settling time	25 us	600 us	60 us	120 us	49 us	55 us	500 us
Power consumption	7.95 mW at 1.8V	17mW at 1.0V	20 mW at 2.5V	4.2 mW at 1.2V	5.1 mW at 1.2V	15 mW at 3 V, 1.8V	8.2 mW at 1.8 V

After having discussed briefly about the fundamentals of phase-locked loop, we now compare the state of the art 2.4 GHz frequency synthesizers. Table.2.1 shows the

performance of the state of the art frequency synthesizers around 2.4 GHz applications.

Reference #45

This work reports the implementation of a frequency synthesizer for system-on-chip (SOC) design. The 2.4 GHz synthesizer has been implemented in 0.18 um CMOS technology and consumes 7.95 mW from a 1.8 V supply. The synthesizer achieved a phase noise of -108.55dBc/Hz at 1 MHz offset and settling time of 25 us. The VCO implemented in this design provides only differential signal with power consumption of 4.68 mW. The dividers are implemented using current-mode logic (CML) circuits to provide a division ratio from 480 to 496 with a power consumption of 2.7 mW.

Reference #46

In this work, a 1 V 2.4 GHz frequency synthesizer for Bluetooth applications has been implemented using CMOS/SOI process. The design uses a novel differential prescaler which consumes 11.5 mW and low-off-leakage charge pump (CP). The power consumption of the fully integrated synthesizer is 17 mW at 1 V power supply.

Reference #47

In this work, a stabilization technique is presented to improve the settling time and magnitude of output sidebands for Bluetooth applications. The synthesizer settles in 60 us with 1 MHz channel spacing and is implemented in 0.25 um CMOS. The

synthesizer achieves a phase noise of -112 dBc/Hz at 1 MHz offset and consumes 20 mW from 2.5 V power supply.

Reference #48

This work reports a low power and short settling time (almost zero) synthesizer for Zigbee applications by using two-point channel controls. The design is implemented in 0.18 μm CMOS process and achieves a phase noise of -116.5 dBc/Hz at 1 MHz offset. The dividers are implemented by dynamic logic circuits and synthesizer consumes a power of 4.2 mW from 1.2 V power supply.

Reference #49

This design uses 90 nm CMOS technology and the synthesizer consumes a power of 5.14 mW from a 1.2 V power supply. In this work, the in-phase and quadrature-phase (I/Q) signals are generated using a CML logic divide-by-2 circuit and the synthesizer achieves a phase noise of -105.9dBc/Hz at 1 MHz offset.

Reference #10

In this work, a 2.4 GHz frequency synthesizer for IEEE 802.15.4/ Zigbee compliant transceivers is implemented using 0.18 μm CMOS technology. Frequency dividers employ hybrid circuits including both CML and True-single-phase logic (TSPC) types. The synthesizer consumes a total of 15 mW from 3 V, 1.8V and 1.2 V power supplies.

Reference #50

This work reports a fully differential Quadrature PLL using a Quadrature-VCO (Q-VCO) and a differential charge pump in 0.18 μm RFCMOS process. The measured phase noise is -112 dBc/Hz at 1 MHz offset and the synthesizer consumes 14.76mW from a 1.8 V power supply.

2.8. Summary

In this Chapter, the concept of phase locking and details of phase locked loops and its building blocks are briefly discussed. The theory of phase-locked loop based frequency synthesizers is much matured and still more research is going on to improve the performance and optimize the implementations for the newer and emerging technologies and standards. The main driving force for research in synthesizers is to generate increasingly higher frequencies and different ways to generate quadrature signals while reducing the power consumption. From the literature survey; it is found that the VCO and the first stage divider are power hungry blocks in the frequency synthesizer. Since the specifications are relaxed for IEEE 802.15.4 standard, this research work mainly focus on the implementation of the ultra-low power fully integrated frequency synthesizer with ultra-low power fully programmable dividers and low power VCO.

CHAPTER 3

DESIGN AND ANALYSIS OF ULTRA-LOW POWER PRESCALER

3.1. Introduction

The prescaler is one of the most critical blocks in the synthesizer since it operates at the highest frequency and consumes a large amount of power. Thus the power reduction in the first stage of the prescaler is important in realizing a low power frequency synthesizer. A dual-modulus ($N/N+1$) prescaler such as divide-by-32/ 33, divide-by-64/ 65 and divide-by-128 / 129 [51]-[53] usually consists of a synchronous divide-by-2/3 [54] or divide-by-4/5 [55] circuit combined with several asynchronous divide-by-2 circuits. The state of art CMOS $N/(N+1)$ prescalers have been designed using different topologies such as injection-locked frequency dividers (ILFDs) described in section 2.5.4, current-mode logic latches [55]-[58] and dynamic logic circuits [59]- [62].

3.2. Design of synchronous 2/3 prescaler

An $N/N+1$ DMP consists of a synchronous prescaler followed by a series of asynchronous divide-by-2 circuits and additional logic gates to control the switching between the two different division ratios. Fig.3.1 shows the evolution of a simple 2/3 synchronous prescaler from divide-by-2 and divide-by-3 circuits.

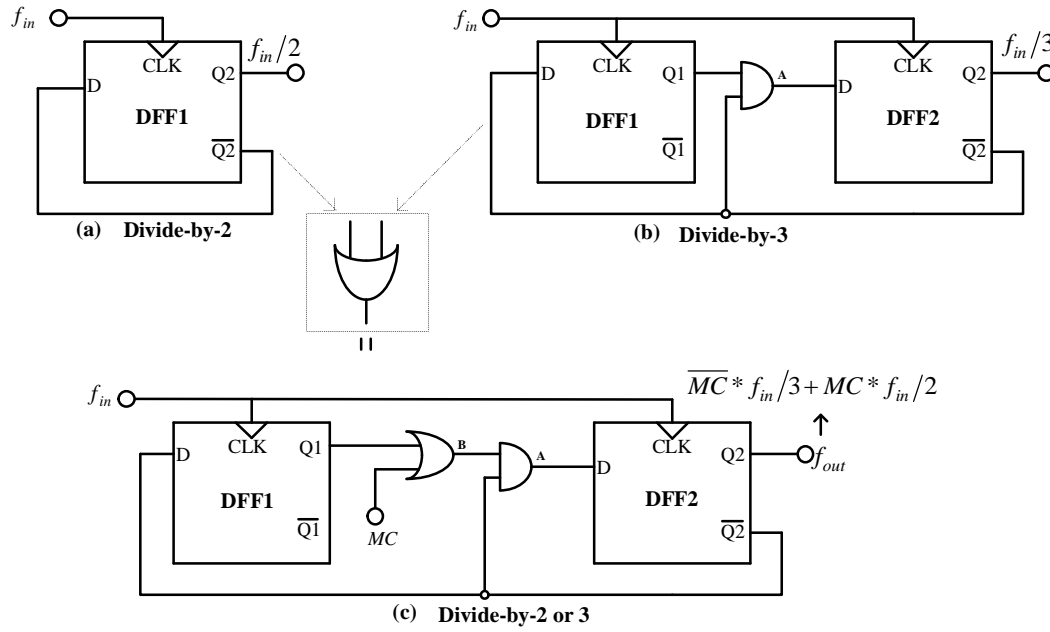


Fig. 3.1 a) Divide-by-2 circuit b) Divide-by-3 circuit c) Divide-by-2/3 circuit

When control logic signal ‘ MC ’ goes high, the output of OR gate is always equal to logic ‘1’ and the output of AND gate is always equal to the inverted output of DFF2 ($\overline{Q2}$) such that the prescaler operates in the divide-by-2 mode as shown in Fig.3.1a. When control logic signal ‘ MC ’ goes low, the output of OR gate is always equal to ‘ $Q1$ ’, such that prescaler operates in the divide-by-3 mode as shown in Fig.3.1b. The output of the synchronous 2/3 prescaler is given by

$$f_{out} = \overline{MC} * f_{in}/3 + MC * f_{in}/2 \quad (3.1)$$

Frequency dividers designed based on digital counters cannot be implemented by standard digital circuits. These digital counters cannot be synthesized directly using register-transfer-level (RTL) description which relies on standard cells as high frequency of operation requires accurate design and optimization. The main building

block of the frequency dividers is D type edge-triggered flip-flop which are constructed using level triggered latches. The most commonly used logic circuits for high frequency dividers is either source-coupled logic (SCL) or current-mode logic (CML) circuits [55]-[58].

3.2.1 Current-mode logic (CML) dividers

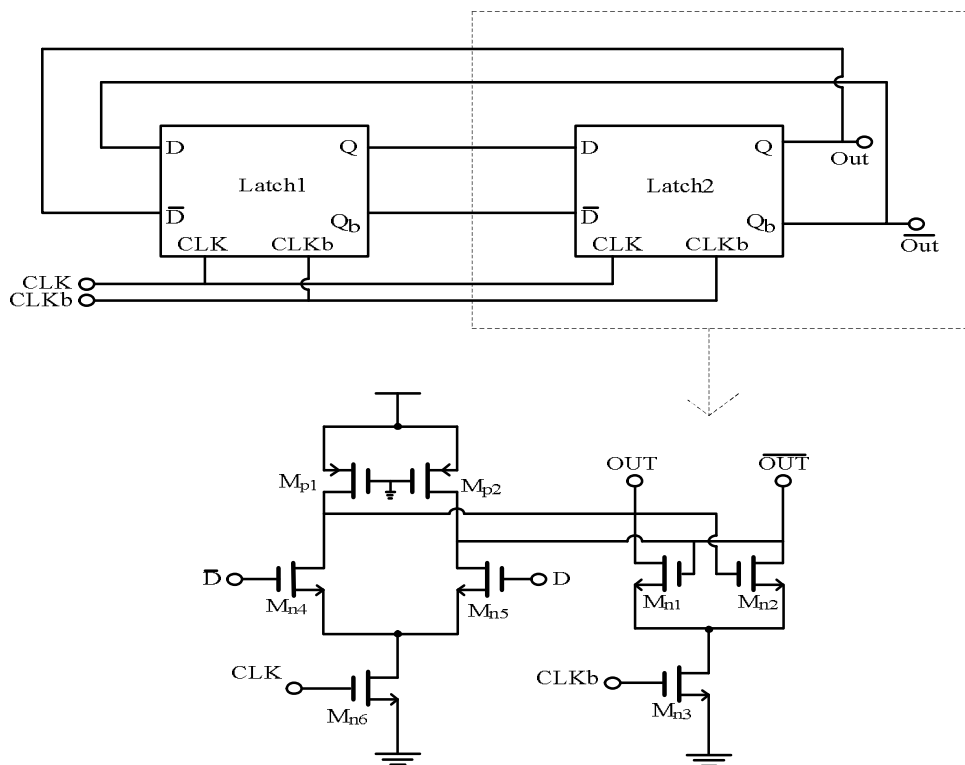


Fig. 3.2 CML divide-by-2 and gate level schematic of CML latch

The CML circuit is based on the use of differential stages with current steering topology. A divide-by-2 circuit implemented using the CML logic type is shown in Fig.3.2 along with its equivalent transistor level schematic. A CML latch consists of NMOS differential pair transistors (M_{n4} , M_{n5}) and a regenerative pair (M_{n1} , M_{n2}). The loads are PMOS transistors (M_{p1} , M_{p2}) which are always operated in the triode region.

When 'CLK' is high, M_{n6} turns-on and the differential pair transistors compare the input amplitudes at gate terminals and pass the result to the output nodes. When 'CLK' is low, M_{n3} turns-on and the regenerative pair transistors hold the output. The maximum operating frequency is decided by the differential pair transistors since they decide how fast the input amplitudes are sensed and transferred to the output nodes.

The CML dividers have higher speed of operation and higher power consumption compared to that of the dynamic logic dividers. One of the main advantages of CML logic circuits over dynamic logic circuits is the use of the differential topology, which makes the current drained by the supply less variable. Moreover, differential circuits reject disturbances coming from the substrate and power supply due to other blocks. The current steering topology as shown in Fig.3.2 helps in lowering the voltage head room. However, the current of the clock transistors are not controllable which results in larger power consumption. Most of the synthesizers reported in literature thus far have used CML fixed dividers or CML based prescalers [51], [52], [55] as the first stage of the divider. The CML logic circuit is very sensitive to the input amplitude and also requires buffers or level shifters at the output to drive the low frequency dynamic logic counters. Since this project main interest lies in the design of low power synthesizer operating below 5 GHz, dynamic logic dividers are preferred over CML logic dividers.

3.2.2 Dynamic logic dividers

The CMOS latches eliminate the static current consumption and use fewer transistors than the CML latches do. They are slow due to the positive feedback (memory element) which introduces additional delay to the switching time. The switching speed of the static circuits depends on two factors namely, the current conduction level through a MOS transistor and parasitic capacitances. Since the parasitic capacitances cannot be controlled, the switching speed is only improved by the use of new and improved process. Alternatively, the memory element formed by a positive feedback can be replaced by a charge storing capacitance, which is called as dynamic memory. The dynamic logic circuit, instead of fighting the time constant limits induced by the RC parasitics, accepts the presence of capacitances and uses them as integral parts of the circuit.

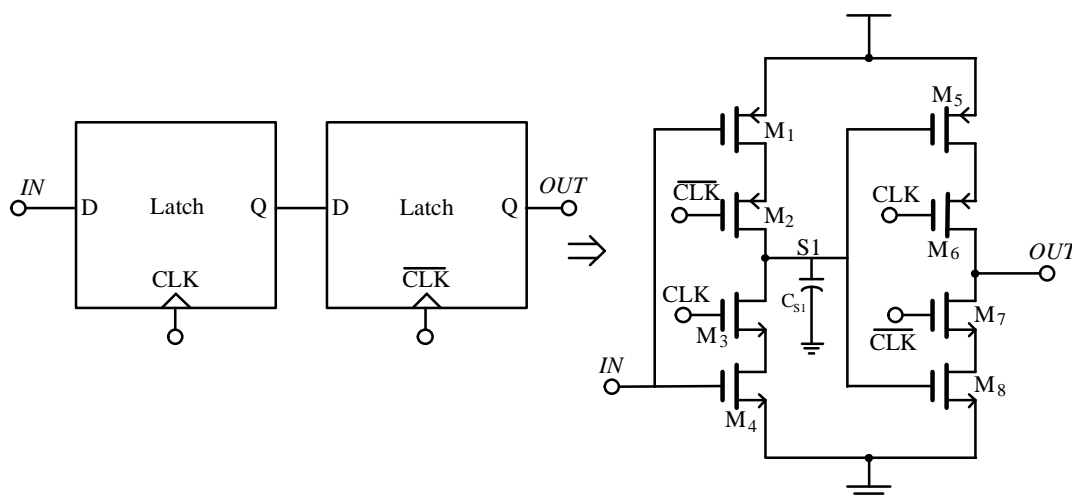


Fig. 3.3 Clocked-CMOS (C²MOS) logic latch

Fig.3.3 shows a clocked-CMOS (C²MOS) logic latch. When CLK='1', both

M_3 and M_2 are active and the input “ IN ” controls the transistors M_1 and M_4 . If input “ IN ”=’0’ (’1’), the node $S1$ charges to ’1’ (’0’). When CLK =’0’, the first stage goes into high-impedance state and the second stage accepts the data at node $S1$ and passes it to the output node. Hence the output data is same as the input data. However, the output voltage can only be maintained so long as the voltage across node $S1$ remains within an appropriate range. The main drawback of this topology is the requirement of complementary clock inputs for a single-phase output. In an asynchronous chain, when a divide-by-2 is implemented, an additional inverter is need at the output to provide differential signals thus causing clock skew.

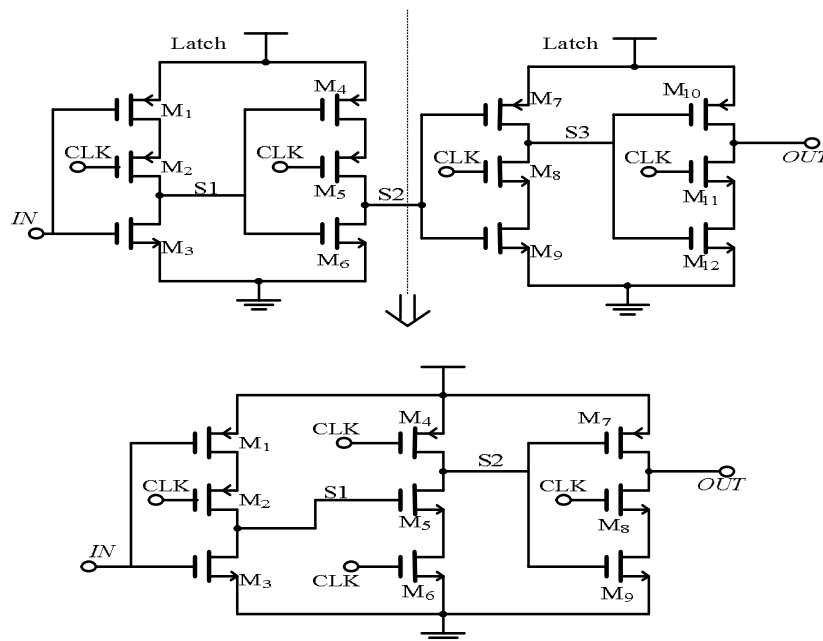


Fig. 3.4 Evolution of TSPC flip-flop from doubled p-C²MOS latch

For this reason, domino logic circuits also parts of the dynamic logic circuit family are developed which use only a true single-phase clock (TSPC) [59]-[61]. The original domino logic circuit requires a dual-phase clock, but a single-phase clock is

developed using doubled p-C²MOS latch as shown in Fig.3.4 which avoids the need of the dual-phase clock and clock skew problems. This architecture has higher speed and higher input sensitivity.

The TSPC flip-flop has two modes of operation namely; hold mode and evaluation mode as shown in Fig.3.5. In the hold mode (pre-charge phase), CLK="0" and node S1 is pre-charged to a value depending on the input signal "IN" and node S2 is pre-charged to "V_{DD}". As transistors M₇ and M₈ are turned-off, output node "OUT" becomes floating. In the evaluation mode, CLK='1' and if the node S1 is pre-charged to "V_{DD}" in the hold mode, node S2 is discharged and output node is pulled up by the transistor M₇. If the node S1 is pre-charged to "0" during the hold mode, node S2 is not discharged, and output node is pulled down by the transistors M₈ and M₉ respectively.

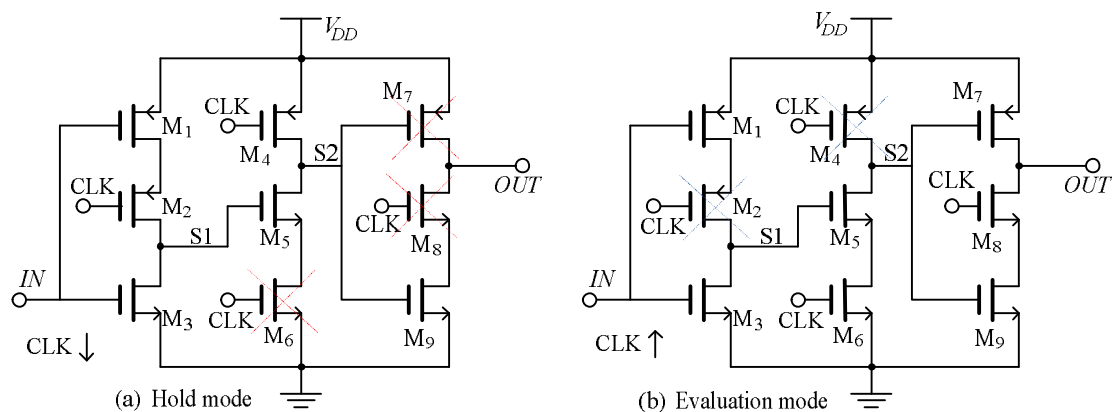


Fig. 3.5 Operation of TSPC flip-flop a) hold mode b) evaluation mode

A further modification of the TSPC circuit, which increases the achievable speed by a reduction of the stacked transistors as described in the next section, is the

extended TSPC (E-TSPC) logic circuit reported in [62]. However, this logic circuit has all the drawbacks of pseudo-nMOS logic circuit. The E-TSPC circuit has static current, noise immunity problem which requires additional care in the design. Our following research shows that dynamic logic circuits such as TSPC and E-TSPC are most suitable in the design of low power dividers for frequencies below 6 GHz applications. However, the choice between TSPC and E-TSPC circuits is very critical since the TSPC circuit has lower power consumption but operates at a lower frequency compared to that of the E-TSPC logic circuit as discussed in the next section.

3.2.3 Propagation speed analysis of TSPC and E-TSPC flip-flops

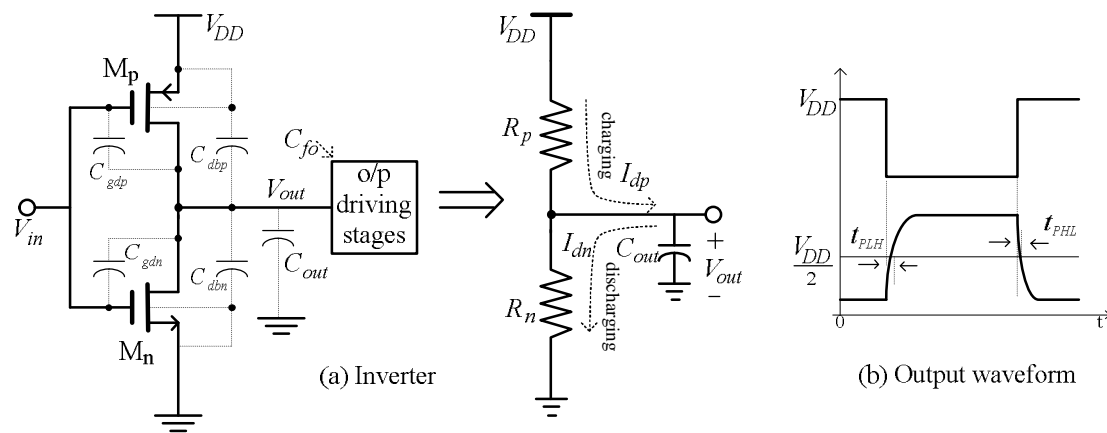


Fig. 3.6 (a) Inverter and its RC model (b) Output waveform

In this section, the maximum operating frequency of the E-TSPC and TSPC flip-flops are analyzed. In each stage, an E-TSPC flip-flop uses only two transistors while a TSPC flip-flop uses three stacked transistors. Of various dynamic logic CMOS circuits, TSPC and E-TSPC circuits operate with the single-phase clock to avoid clock

skew problems. Before performing the analysis of TSPC and E-TSPC logic circuits, an analysis of the simple inverter with its equivalent RC model for the propagation delay is performed as shown in Fig.3.6.

The load capacitance at the output node of the inverter is manually calculated using a method described in [63], [64] and is given by

$$C_{out} = C_{dbp} + 2C_{gdp} + C_{dbn} + 2C_{gdn} + C_{fo} \quad (3.2)$$

Where C_{fo} is fan-out capacitance which is equal to the gate capacitance of driving stage. When M_p is on and M_n is off, the voltage buildup is given by

$$V_{out}(t) = V_{DD}(1 - e^{-t/\tau_p}) \quad (3.3)$$

Where the time constant τ_p and PMOS equivalent resistance R_p is given by

$$\tau_p = R_p C_{out} \quad (3.4)$$

$$R_p = \frac{2}{\mu_p C_{ox}} * \frac{L_p}{W_p} * \frac{1}{(V_{DD} - |V_{tp}|)} \quad (3.5)$$

Similarly, When M_p is off and M_n is on, the voltage buildup is given by

$$V_{out}(t) = V_{DD}(e^{-t/\tau_n}) \quad (3.6)$$

Where the time constant τ_n and PMOS equivalent resistance R_n is given by

$$\tau_n = R_n C_{out} \quad (3.7)$$

$$R_n = \frac{2}{\mu_n C_{ox}} * \frac{L_n}{W_n} * \frac{1}{(V_{DD} - |V_{tn}|)} \quad (3.8)$$

The propagation delay (t_p) which is a logic delay through a gate is the average of

low-to-high (t_{PLH}) and high-to-low (t_{PHL}) transition delays and is given by

$$t_p = \frac{t_{PHL} + t_{PLH}}{2} \quad (3.9)$$

The high-to-low propagation delay represents the time needed for the output to fall from V_{DD} to 50% of V_{DD} and is given by

$$t_{PHL} = C_{out} \int_{V_{DD}-V_m}^{V_{DD}} \frac{dV_{out}}{I_{dn(sat)}} + C_{out} \int_{V_{DD}/2}^{V_{DD}-V_m} \frac{dV_{out}}{I_{dn(non-sat)}} \quad (3.10)$$

Evaluating the integrals in (3.10) yields,

$$t_{PHL} = S_n \tau_n \quad (3.11)$$

$$S_n = \frac{2V_m}{(V_{DD} - V_m)} + \ln\left(\frac{4(V_{DD} - V_m)}{V_{DD}} - 1\right) \quad (3.12)$$

Similarly, the low-to-high propagation delay represents the time needed for the output to rise from '0' to 50% of V_{DD} and is given by

$$t_{PLH} = S_p \tau_p \quad (3.13)$$

$$S_p = \frac{2|V_{tp}|}{(V_{DD} - |V_{tp}|)} + \ln\left(\frac{4(V_{DD} - |V_{tp}|)}{V_{DD}} - 1\right) \quad (3.14)$$

However, by using the RC model, the total propagation delay analysis becomes simpler as described in [63] and is given by,

$$t_p = \frac{0.69(\tau_n + \tau_p)}{2} \quad (3.15)$$

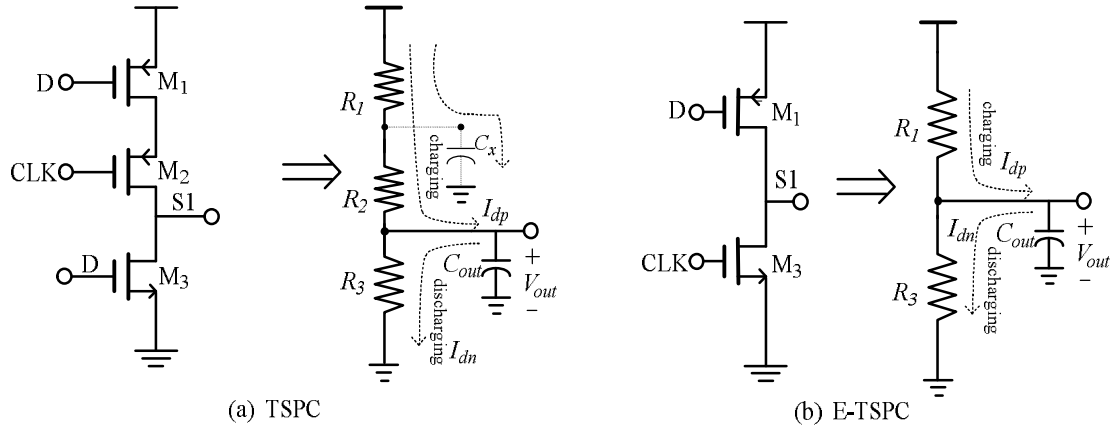


Fig. 3.7 First stage and equivalent RC model of (a) TSPC (b) E-TSPC flip-flops

To compare the speed performance of TSPC and E-TSPC circuits, the first stage of both TSPC and E-TSPC circuits with their equivalent RC models are analyzed as shown in Fig.3.7. The charging and discharging time constants of the first stage of the TSPC flip-flop are manually calculated using the RC ladder method described in [63], as follows:

$$\tau_{n1} = R_3 C_{out} \quad (3.16)$$

$$C_{out} = C_{db3} + 2C_{gd3} + C_{db2} + 2C_{gd2} + C_{fo} \quad (3.17)$$

$$\tau_{p1} = (R_2 + R_1)C_{out} + R_1 C_x \quad (3.18)$$

$$C_x = C_{gs2} + C_{gs1} + C_{p+} \quad (3.19)$$

where C_{p+} is the total depletion capacitance between the series PMOS transistors and C_{fo} is the fan-out capacitance. The propagation delay of the first stage TSPC flip-flop is

$$t_{p_TSPC} = \frac{0.69(\tau_{p1} + \tau_{n1})}{2} \quad (3.20)$$

Similarly, the charging and discharging time constants of the first stage E-TSPC flip-flop are given by

$$\tau_{n2} = R_3 C_{out} \quad (3.21)$$

$$\tau_{p2} = R_1 C_{out} \quad (3.22)$$

The propagation delay of the first stage TSPC flip-flop is given by

$$t_{p_E-TSPC} = \frac{0.69(\tau_{p2} + \tau_{n2})}{2} \quad (3.23)$$

The output load capacitance of E-TSPC stage is lower than that of TSPC due to the reduced fan-out. The charging time constant of E-TSPC is smaller than TSPC from (3.18) and (3.22), the propagation delay of TSPC stage is higher than that of the E-TSPC stage and thus it proves TSPC flip-flop has a lower operating frequency compared to that of the E-TSPC flip-flop. If speed is the critical parameter in the design, E-TSPC logic circuits are chosen over other dynamic logic circuits. However, it suffers from static power dissipation which is discussed in the next section.

3.2.4 Power consumption analysis of TSPC and E-TSPC flip-flops

In this section, the power consumption of the E-TSPC and TSPC flip-flops are analyzed. In digital circuits, the power consumption is divided into three parts namely; switching power, short-circuit power and leakage power. The total power consumption of a digital circuit is given by

$$P_{avg} = P_{switching} + P_{short-circuit} + P_{leakage} = \alpha_{0 \rightarrow 1} C_L V_{dd}^2 f_{clk} + (I_{sc} + I_{leak}) V_{dd} \quad (3.24)$$

The first term represents the switching power consumption, where C_L is the load capacitance, f_{clk} is the clock frequency and $\alpha_{0 \rightarrow 1}$ is the node transition activity factor, the average number of transitions in one clock period. The second term is due to conduction of current directly from the supply to ground when PMOS and NMOS are active simultaneously. The third term is due to the leakage current, which arises from the substrate injection and sub-threshold effects, and depends on the technology used.

Of the three sources of power consumption, switching power and short-circuit power are significant and will be considered here as the power consumption due to leakage current is technology dependent and is not within the scope of this analysis. Furthermore, for the targeted frequency of operation the targeted technology of 0.18 μ m, the leakage current is quite smaller than the other two. It is known that E-TSPC [62] circuits suffer from static power dissipation due to non-complementary structure. Fig.3.8 shows the schematics of the TSPC and E-TSPC circuits in divide-by-2 mode. The load capacitance at each output node of TSPC flip-flop in divide-by-2 mode is given by

$$C_{S1} = C_{dbM_3} + 2C_{gdM_3} + C_{dbM_2} + 2C_{gdM_2} + C_{gM_5} \quad (3.25)$$

$$C_{S2} = C_{dbM_4} + 2C_{gdM_4} + C_{dbM_5} + 2C_{gdM_5} + C_{gM_7} + C_{gM_9} \quad (3.26)$$

$$C_{S3} = C_{dbM_7} + 2C_{gdM_7} + C_{dbM_8} + 2C_{gdM_8} + C_{gM_1} + C_{gM_3} \quad (3.27)$$

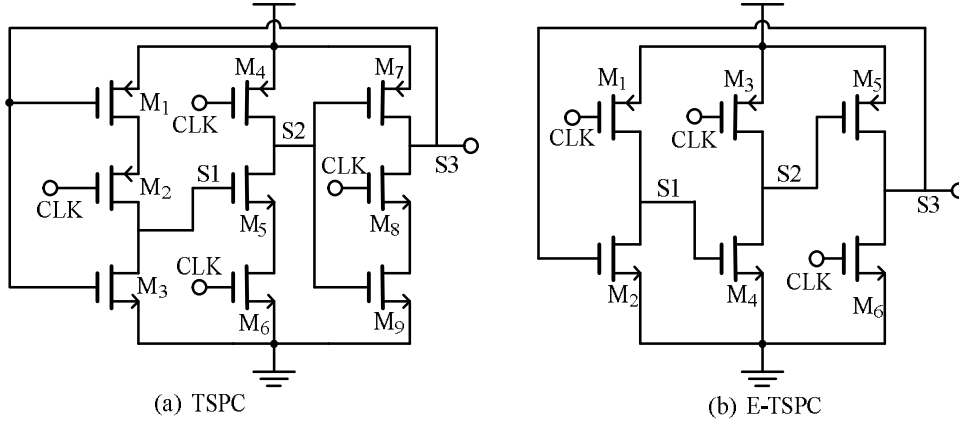


Fig. 3.8 Divide-by-2 circuit (a) TSPC (b) E-TSPC

Similarly, the load capacitance at each output node of E-TSPC flip-flop in divide-by-2 mode is given by

$$C_{S1} = C_{dbM_1} + 2C_{gdM_1} + C_{dbM_2} + 2C_{gdM_2} + C_{gM_3} \quad (3.28)$$

$$C_{S2} = C_{dbM_4} + 2C_{gdM_4} + C_{dbM_3} + 2C_{gdM_3} + C_{gM_6} \quad (3.29)$$

$$C_{S3} = C_{dbM_5} + 2C_{gdM_5} + C_{dbM_6} + 2C_{gdM_6} + C_{gM_1} \quad (3.30)$$

The above equations clearly show that the capacitance at the each output node of the TSPC circuit is higher than that of the E-TSPC circuit. Since the switching power is linearly related to the load capacitance, TSPC circuits cause more switching power than E-TSPC circuits. However, the switching power can be reduced by optimization techniques such as reducing the number of switching stages and the width of the transistors. In TSPC circuits, one of the transistors in each stage is always off, there exists no short-circuit power in principle.

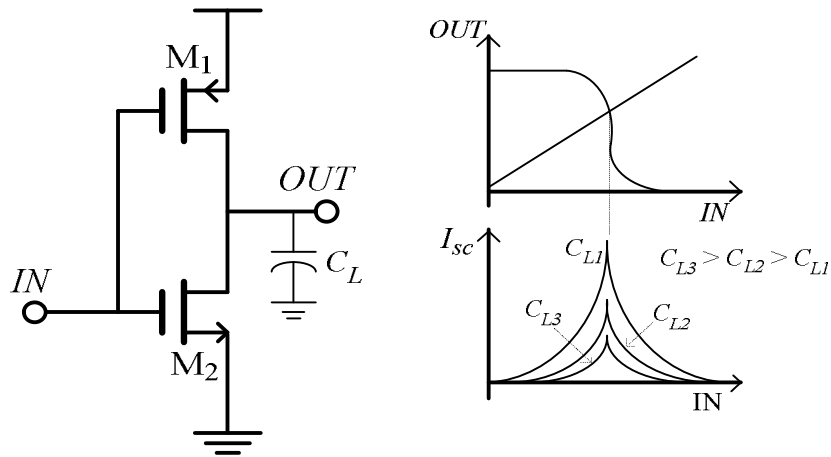


Fig. 3.9 CMOS inverter and variation of short-circuit current with load

In general, there exists a short-circuit power for a short interval during the rise and fall periods of the input data and clock signals. Since the capacitance of a TSPC circuit at each output node is large, the rise and fall times are significant and result in a low peak short-circuit current [65]. Fig.3.9 shows a simple inverter and its simulated output current with different loads. It is seen that as load capacitance increases, the peak short-circuit current decreases. From this we can deduce that the TSPC short-circuit power is smaller than the E-TSPC short circuit power.

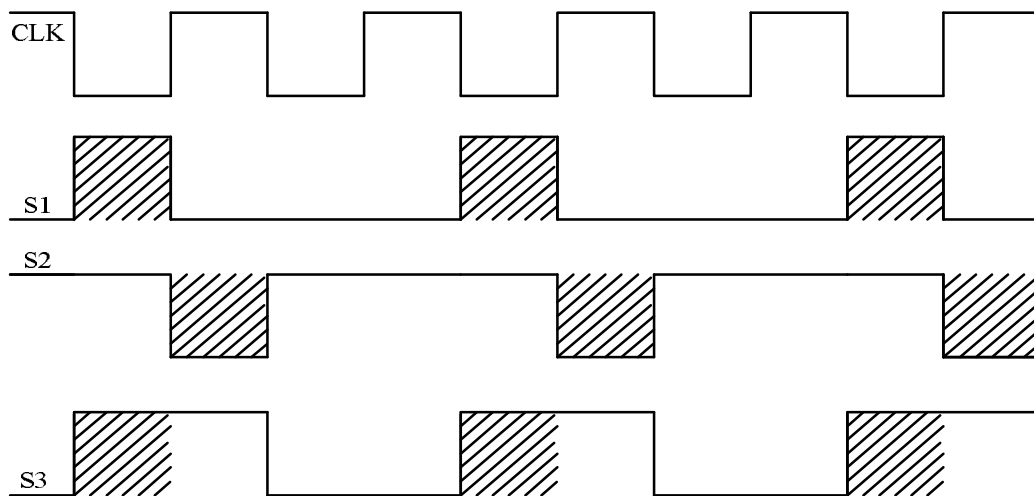


Fig. 3.10 Divide-by-2 operation of an E-TSPC circuit

The timing diagram of Fig.3.10 illustrates the operation of a divide-by-2 E-TSPC circuit. The shaded part shows the duration where the short-circuit current exists in the E-TSPC divide-by-2 circuit. To analyze E-TSPC short-circuit, a single stage of an E-TSPC circuit is simulated with PMOS and NMOS transistors active and the PMOS transistor width is increased for a constant NMOS transistor width in 0.18 μ m technology. Fig.3.11 shows the schematic set-up and the short-circuit power consumption for different ratios of PMOS to NMOS transistor width. As the ratio increases, both the short-circuit power and the output voltage increases.

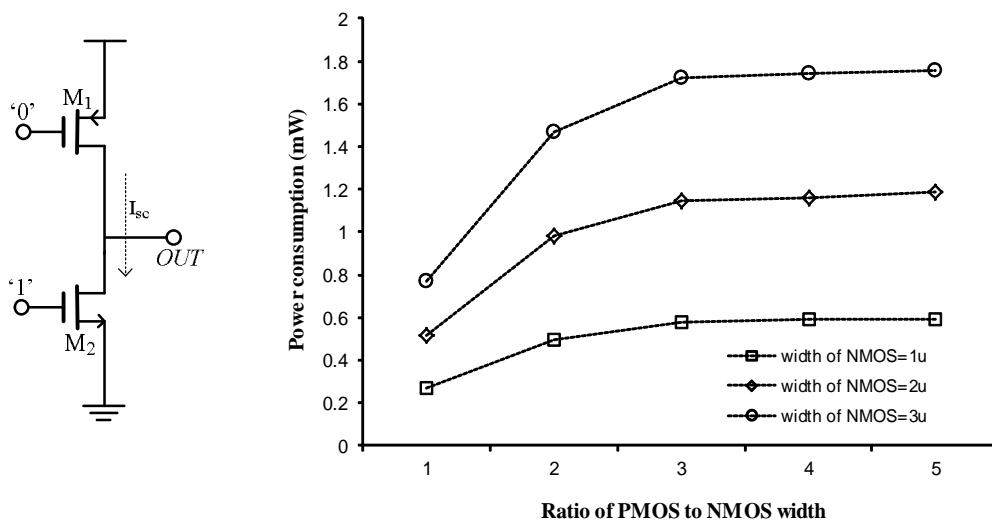


Fig. 3.11 Short-circuit power in a single stage of E-TSPC circuit

Fig.3.12 shows the variation in output amplitude of the single stage E-TSPC circuit with the variation in the ratio of PMOS to NMOS width. The output amplitude remains almost constant with respect to width of the NMOS transistor as long as the

ratio between PMOS to NMOS is constant. For example in Fig.3.8b, if PMOS transistor M_1 width is increased, the voltage at node S1 increases and changes the region of operation of M_4 (triode or saturation).

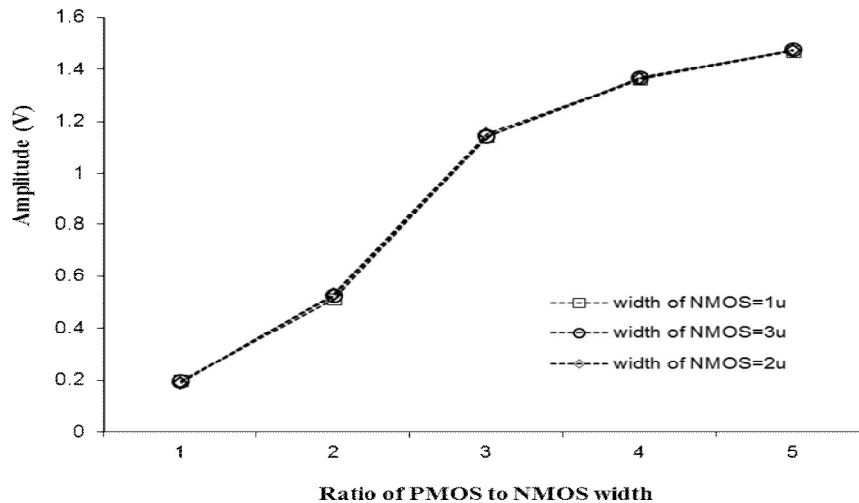


Fig. 3.12 Output amplitude in single stage of E-TSPC logic

If CLK is low, M_3 is turned-on which results in a direct path between the supply and ground, causing a short-circuit power consumption. The amount of short-circuit power dissipated depends on the region of operation of transistor M_4 . The short circuit power mainly depends on the transistor sizes as briefly discussed in [66] with a comparison of the switching and the short-circuit power of TSPC and E-TSPC circuits. However, most of the analysis is based on square wave input signal.

In reality at the GHz frequency and in many applications, the VCO output is not a full swing signal and the output signal has certain DC level which affects the power consumption of both logic types. To verify the dependence of power

consumption against the DC level and amplitude of the sinusoidal clock waveform, single stages of both circuits as shown in Fig.3.13a are simulated. Here TSPC PMOS transistors are twice the width of the E-TSPC PMOS transistors to have same driving capability and fair comparison. For each fixed DC level (0.7 V - 1.2 V), the amplitude of the clock signal (normally from VCO) is varied from 400-600 mV and input D is switched from logic “0” to logic “1”.

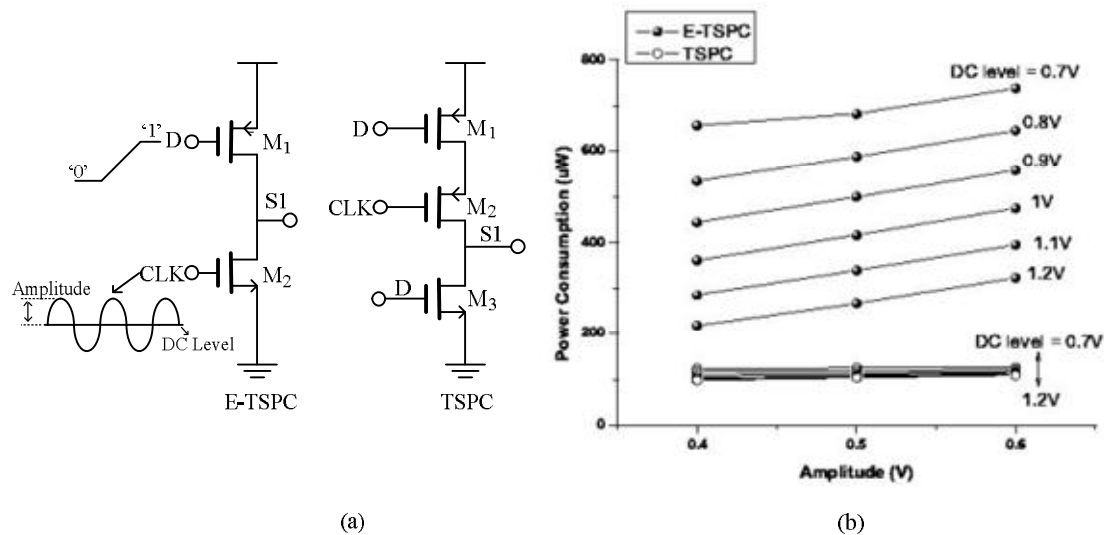


Fig. 3.13 (a) First stage of E-TSPC and TSPC flip-flops (b) Power consumption against DC level and amplitude of clock signal

The main aim here is to show how the power consumption is affected by the variation in the DC level and the amplitude of the clock signal obtained from the VCO which is sinusoidal. The simulation results in Fig.3.13b indicate that for the E-TSPC circuit, the DC level should be high (negative edge triggered clock circuit) to obtain low power consumption and its power consumption is significantly varied from 200-700 μ W with respect to the DC level and amplitude of the clock signal. For

TSPC, the power consumption remains almost constant for the same variation of DC level and amplitude of the clock signal. The TSPC circuit can be directly driven by the VCO with amplitude as low as 250 mV and high DC level for low power consumption.

The analysis above suggests that the TSPC circuit is less sensitive to the variations in the output amplitude of VCO compared to that of E-TSPC circuits. Even though the propagation delay of E-TSPC logic is lower than that of TSPC logic, its large short-circuit power and considerable amount of switching power makes the E-TSPC logic less suitable of low power applications compared to TSPC below 5 GHz operation. Based on this analysis, we have chosen TSPC logic for the design of low power divider in this project.

3.3. Conventional synchronous TSPC 2/3 prescaler

The conventional TSPC 2/3 prescaler consists of two D flip-flops, an OR gate and a AND gate as shown in Fig.3.14. Due to the large load on DFF2 and difficulty to embed the OR, AND gates into the DFF which introduces additional delay limits the speed of conventional 2/3 prescaler and also causes substantial power dissipation. The total load capacitance at the output node Q_b of the conventional 2/3 prescaler (not considering gate capacitance of next stage is given by

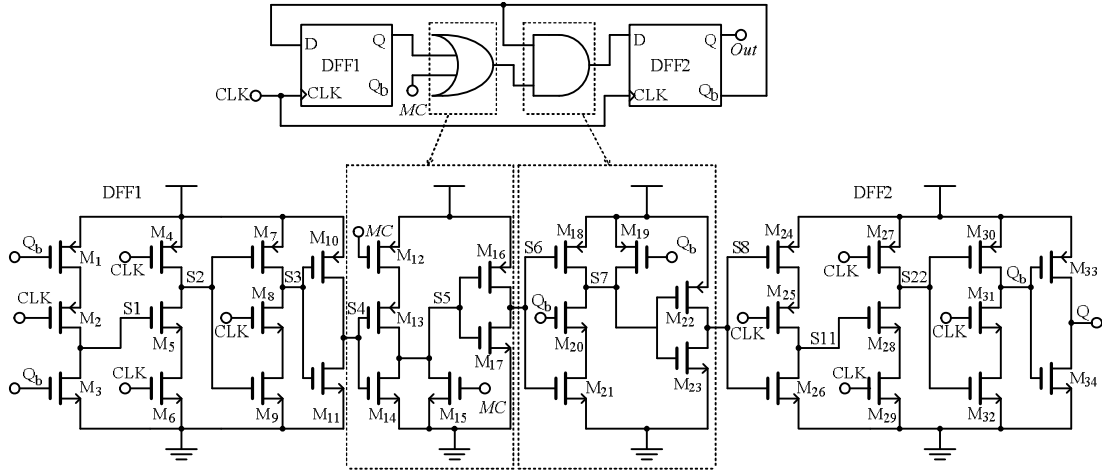


Fig. 3.14 Conventional TSPC 2/3 prescaler and its equivalent gate level schematic

$$C_L = C_{dbM30} + C_{dbM31} + 2(C_{gdM30} + C_{gdM31}) + C_{gM3} + C_{gM1} + C_{gM19} + C_{gM20} \quad (3.31)$$

As discussed in section 2.5.4, the addition of an OR gate and an AND gate in the critical path introduces the additional delay and limits the maximum operating speed of the circuit. The propagation delay of the TSPC 2/3 prescaler is equal to the sum of propagation delay of DFF1 (t_{p_DFF1}), DFF2 (t_{p_DFF2}) and logic gates (t_{p_OR}, t_{p_AND}), where the propagation delay of each DFF is equal to the sum of delay of the each stage. The total propagation delay is given by

$$t_{p_TSPC} = t_{p_DFF1} + t_{p_DFF2} + t_{p_OR} + t_{p_AND} \quad (3.32)$$

By using the RC delay model described in section 3.2.3, the propagation delay of DFF1 is calculated as given below:

$$t_{p_DFF1} = \frac{0.69}{2} (\tau_{p_S1} + \tau_{n_S1} + \tau_{p_S2} + \tau_{n_S2} + \tau_{p_S3} + \tau_{n_S3} + \tau_{p_S4} + \tau_{n_S4}) \quad (3.33)$$

$$\tau_{p_S1} = (R_2 + R_1)(C_{db3} + 2C_{gd3} + C_{db2} + 2C_{gd2} + C_{g5}) + R_1(C_{gs2} + C_{gs1} + C_{p+}) \quad (3.34)$$

$$\tau_{n_S1} = R_3(C_{db3} + 2C_{gd3} + C_{db2} + 2C_{gd2} + C_{g5}) \quad (3.35)$$

$$\tau_{p_S2} = R_4(C_{db4} + 2C_{gd4} + C_{db5} + 2C_{gd5} + C_{g7} + C_{g9}) \quad (3.36)$$

$$\tau_{n_S2} = (R_5 + R_6)(C_{db4} + 2C_{gd4} + C_{db5} + 2C_{gd5} + C_{g7} + C_{g9}) + R_5(C_{gs5} + C_{gs6} + C_{n+}) \quad (3.37)$$

$$\tau_{p_S3} = R_7(C_{db7} + 2C_{gd7} + C_{db8} + 2C_{gd8} + C_{g10} + C_{g11}) \quad (3.38)$$

$$\tau_{n_S3} = (R_8 + R_9)(C_{db7} + 2C_{gd7} + C_{db8} + 2C_{gd8} + C_{g10} + C_{g11}) + R_8(C_{gs8} + C_{gs9} + C_{n+}) \quad (3.39)$$

$$\tau_{p_S4} = R_{10}(C_{db10} + 2C_{gd10} + C_{db11} + 2C_{gd11} + C_{g13} + C_{g14}) \quad (3.40)$$

$$\tau_{n_S4} = R_{11}(C_{db10} + 2C_{gd10} + C_{db11} + 2C_{gd11} + C_{g13} + C_{g14}) \quad (3.41)$$

The equivalent resistance is calculated by (3.5) and (3.8). Similarly, the propagation delay of each stage of DFF2 is calculated. The worst case propagation delays of the both logic OR and logic AND gate is given below:

$$t_{p_OR} = \frac{0.69}{2}(\tau_{p_S5} + \tau_{n_S5} + \tau_{p_S6} + \tau_{n_S6}) \quad (3.42)$$

$$\tau_{p_S5} = (R_{12} + R_{13})(C_{db13} + 2(C_{gd13} + C_{gd14}) + C_{db14} + C_{g16} + C_{g17}) + R_{13}(C_{gs12} + C_{gs13} + C_{p+}) \quad (3.43)$$

$$\tau_{n_S5} = R_{14}(C_{db13} + 2C_{gd13} + C_{db14} + 2C_{gd14} + C_{g16} + C_{g17}) \quad (3.44)$$

$$\tau_{p_S6} = R_{16}(C_{db16} + 2C_{gd16} + C_{db17} + 2C_{gd17} + C_{g18} + C_{g21}) \quad (3.45)$$

$$\tau_{n_S6} = R_{17}(C_{db16} + 2C_{gd16} + C_{db17} + 2C_{gd17} + C_{g18} + C_{g21}) \quad (3.46)$$

$$t_{p_AND} = \frac{0.69}{2}(\tau_{p_S7} + \tau_{n_S7} + \tau_{p_S8} + \tau_{n_S8}) \quad (3.47)$$

$$\tau_{n_S7} = (R_{20} + R_{21})(C_{db18} + 2(C_{gd20} + C_{gd18}) + C_{db20} + C_{g22} + C_{g23}) + R_{20}(C_{gs20} + C_{gs21} + C_{n+})$$

(3.48)

$$\tau_{p_S7} = R_{18}(C_{db18} + 2(C_{gd20} + C_{gd18}) + C_{db20} + C_{g22} + C_{g23}) \quad (3.49)$$

$$\tau_{p_S8} = R_{22}(C_{db22} + 2C_{gd22} + C_{db23} + 2C_{gd23} + C_{g24} + C_{g26}) \quad (3.50)$$

$$\tau_{n_S8} = R_{23}(C_{db22} + 2C_{gd22} + C_{db23} + 2C_{gd23} + C_{g24} + C_{g26}) \quad (3.51)$$

The propagation delay equations shows that the maximum operating frequency of the conventional 2/3 prescaler is limited due to the logic OR and logic AND gates. The conventional TSPC 2/3 prescaler has 12 stages and each stage has a switching output node. The switching power with 12 switching nodes is given by

$$P_{Switching} = \sum_{i=1}^{12} f_{CLK} C_{Li} V_{dd}^2 \quad (3.52)$$

Where C_{Li} is the capacitance of the each output node of DFF1, DFF2 and logic gates.

As discussed in section 3.2.4, the short circuit power of the conventional 2/3 prescaler is almost negligible and power consumption is mainly due to the switching power due to large capacitance at the output of each stage. TSPC-based 4/5, 8/9 prescalers are presented in [67] which improves the speed by 13% compared to that of the conventional 2/3 prescaler. The switching power and the propagation delay can be reduced by the techniques described in [59], [60], [68]. One of the main advantages of domino logic is that the logic gates can be embedded into the flip-flop, which can reduce the additional propagation delay, which is discussed briefly in the section 2.5.4.

3.4. Proposed TSPC 2/3 Prescaler: Design-I

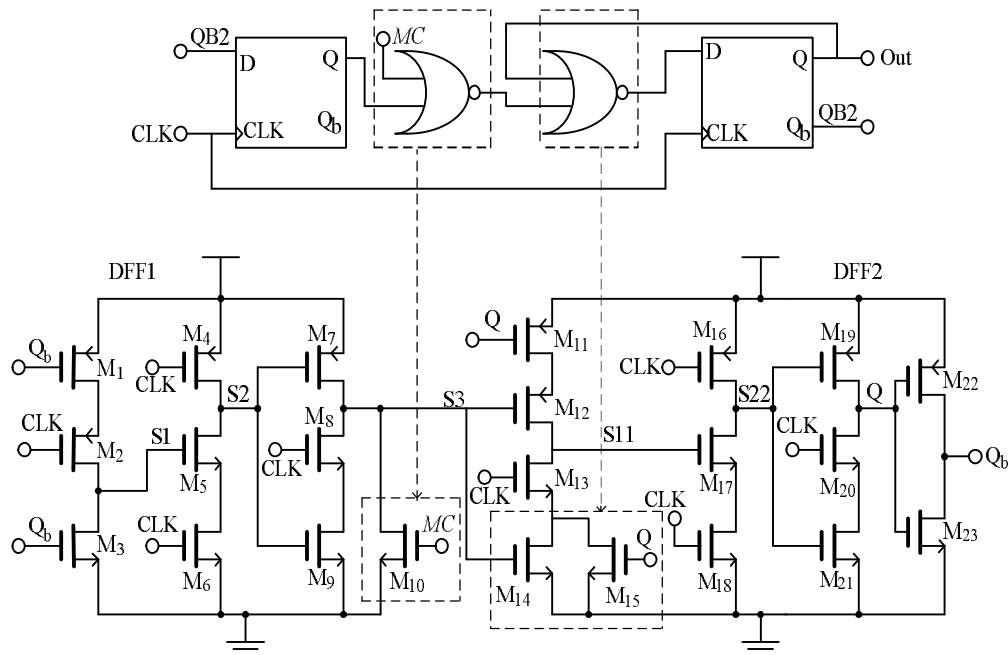


Fig. 3.15 Proposed Design-I TSPC 2/3 prescaler circuit and equivalent gate level schematic

The conventional TSPC 2/3 prescaler consumes large power and has low operating frequency due to its large load capacitance. An improved speed and low power 2/3 prescaler implemented in TSPC logic style is proposed in this work, which consists of two D flip-flops and two NOR gates embedded into the flip-flops as shown in Fig.3.15. In the proposed 2/3 prescaler, the first NOR gate is embedded into the third stage of DFF1 using a single NMOS transistor M_{10} , whose drain is connected to node S3 of DFF1 and the other NOR gate is embedded into the first stage of DFF2. By doing so, an extra inverter driven by node S3 of DFF1 and additional stages introduced by the logic gates between DFF1 and DFF2 of the conventional TSPC 2/3 prescaler is eliminated, reducing the number of switching nodes to 7 in the proposed prescaler. The substantial reduction of the nodes reduces the load capacitance and

switching power consumption of the proposed 2/3 prescaler. The load capacitance of the proposed 2/3 prescaler is given by

$$C_{L_Design-1} = C_{dbM19} + C_{dbM20} + 2(C_{gdM19} + C_{gdM20}) + C_{gM15} + C_{gM11} \quad (3.53)$$

3.4.1. Divide-by-2 operation

When $MC='1'$, transistor M_{10} turns-on and node S3 switches to logic '0' irrespective of the data at node S2. The second NOR gate output is always equal to the inverted output of DFF2 as shown in Fig.3.16, which is equivalent to simple DFF with its complimentary output connected to the input as shown in Fig.3.8a. Thus the prescaler act as divide-by-2 when $MC='1'$. Here, even though the output of DFF2 is connected in feedback to the input of DFF1, the switching data at node S1 and S2 is blocked by the transistor M_{10} to reach to the node S3. Thus the switching power at the node S3 is always zero.

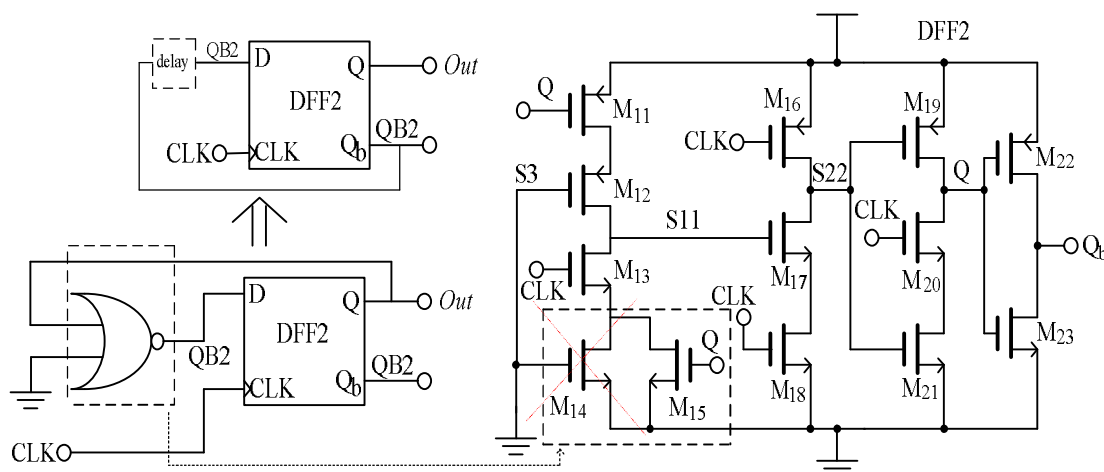


Fig. 3.16 Divide-by-2 operation of the proposed 2/3 prescaler unit

However, there exists switching power in the first two stages of the DFF at nodes S1

and S2 due to the feedback action of the DFF2 output which switches continuously.

The total power of the prescaler in divide-by-2 mode of operation is equal to the sum of switching power of DFF2 and the switching power of first two stages of DFF1 which is less than the conventional 2/3 prescaler.

3.4.2. Divide-by-3 operation

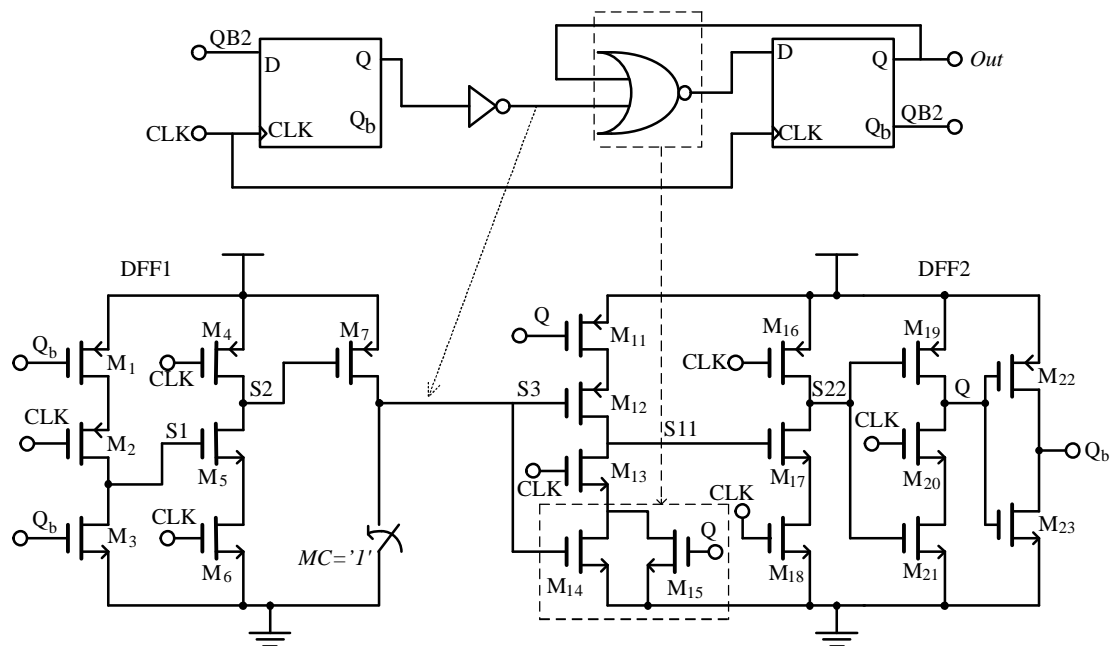


Fig. 3.17 Divide-by-3 operation of the proposed 2/3 prescaler unit

When $MC=0$, transistor M_{10} turns-off and the inverted data at node S2 is passed to the node S3. The second NOR gate output is always equal to the inverted output of DFF2. Fig.3.17 shows the equivalent circuit of the proposed 2/3 prescaler unit in divide-by-3 mode of operation which is equivalent to the schematic shown in Fig.3.1b. The combination of inverter and NOR gate is equivalent to logic AND gate with the other input inverted as shown in Fig.3.17. Thus the prescaler act as divide-by-3 when $MC=0$. There is continuous switching activity at each node and the switching power

is given by the sum of switching power of both the DFF1 and DFF2 respectively.

3.4.3. Propagation delay of the proposed 2/3 prescaler

The propagation delay of the proposed 2/3 prescaler is calculated using the RC delay model method which is used to calculate the propagation delay of the conventional 2/3 prescaler as discussed in section 3.2. However, in divide-by-2 mode of operation, since the node S3 always remains at logic '0' and blocks the data from DFF1 to propagate to the DFF2. The total propagation delay of the proposed 2/3 prescaler in divide-by-2 mode of operation is equal to the propagation delay of DFF2 which is given by

$$t_{p_divide-by-2} = t_{p_DFF2} \quad (3.54)$$

$$t_{p_DFF1} = \frac{0.69}{2} (\tau_{p_S11} + \tau_{n_S11} + \tau_{p_S21} + \tau_{n_S21} + \tau_{p_Q} + \tau_{n_Q} + \tau_{p_Qb} + \tau_{n_Qb}) \quad (3.55)$$

$$\tau_{p_S11} = (R_{11} + R_{12})(C_{db13} + 2(C_{gd13} + C_{gd12}) + C_{db12} + C_{g17}) + R_{12}(C_{gs12} + C_{gs11} + C_{p+}) \quad (3.56)$$

$$\tau_{n_S11} = (R_{13} + R_{14})(C_{db13} + 2(C_{gd13} + C_{gd12}) + C_{db12} + C_{g17}) + R_{13}(C_{gs13} + C_{gs14} + C_{n+}) \quad (3.57)$$

The propagation delay of the remaining stages of the DFF2 is similar to the propagation delay of the DFF2 in conventional 2/3 prescaler. In divide-by-3 mode of operation, since both DFF1 and DFF2 are active, the propagation delay is equal to the sum of propagation delay of embedded NOR gate DFF1 and DFF2 respectively,

which is given by

$$t_{p_divide-by-3} = t_{p_DFF1} + t_{p_DFF2} \quad (3.58)$$

Since the NOR gates are embedded in to the flip-flop, the propagation delay of entire

2/3 prescaler is reduced by delay equal to 7 stages as proved by the RC delay model.

Since the number of stages in the proposed Design-I prescaler is reduced to 7, the

switching power is given by

$$P_{Switching_Design-I} = \sum_{j=1}^7 f_{CLK} C_{Lj} V_{dd}^2 \quad (3.59)$$

where C_{Li} is the load capacitance at each output node of DFF1 and DFF2. The

reduction of the switching power in the proposed design compared to that of the

conventional 2/3 prescaler when both circuits are designed with same transistor sizes

is given by

$$P_{Switching_saved} = \sum_{i=1}^{12} f_{CLK} C_{Li} V_{dd}^2 - \sum_{j=1}^7 f_{CLK} C_{Lj} V_{dd}^2 \quad (3.60)$$

In this analysis, both the conventional 2/3 prescaler and Design-I prescaler are

designed using same width of 3 um for PMOS and 2 um for NMOS transistors. The

node capacitances at each output node for both circuits are assumed to be same, since

all the devices has same aspect ratio. Based on this assumption, the switching power

saved by Design-I prescaler is almost 42% and its speed is improved by 1.3 times

compared to that of the conventional 2/3 prescaler which are also verified by

simulation and measurement results. Apart from the reduction of propagation delay and power consumption, the proposed prescaler reduces the area since it uses only 23 transistors to perform divide-by-2 and divide-by-3 compared to the conventional 2/3 which uses as many as 32 transistors. The output “Q” drives transistors M_{11} and M_{14} of DFF2 and “Q_b” drives transistors M_1 and M_3 such that loading on “Q” is reduced compared to conventional prescaler.

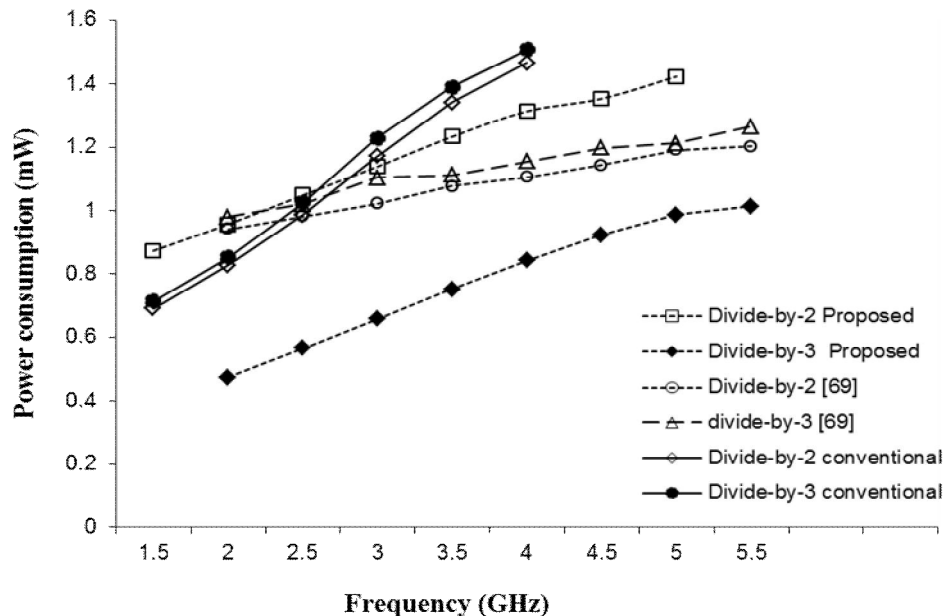


Fig. 3.18 Frequency versus power consumption of different prescalers

Fig.3.18 shows the power consumption against different frequencies for E-TSPC based prescaler in [69] at 1.5V power supply, the conventional and Design-I 2/3 prescaler at 1.8 V power supply to have a fair comparison, since the maximum operating frequency of the E-TSPC based prescaler is higher than that of the TSPC based prescaler. The simulation results show that the conventional TSPC 2/3 prescaler

can operate up to maximum frequency of 4.2 GHz. The Design-I 2/3 prescaler has maximum operating frequency of 5.5 GHz and at 2.4 GHz, it draws a current of 549 μ A, 251 μ A in the divide-by-2 and divide-by-3 modes respectively. The power consumption of the Design-I prescaler is 2.7 and 2.2 times less than the power consumption of the E-TSPC prescaler in [69], [54] and 1.6 times lesser than conventional TSPC 2/3 prescaler.

3.4.4. Short-circuit power of the Design-I 2/3 prescaler

From the short-circuit power analysis of E-TSPC and TSPC, we assumed that the short-circuit power in TSPC is almost negligible since one of the transistors in each stage is always off. However, this is not true when a logic gate is embedded in to the TSPC logic. During the divide-by-2 mode when control logic signal $MC = '1'$, the transistor M_{10} turns-on as shown in Fig. 3.15 and Fig. 3.17, allowing a direct path from supply to ground when transistor M_7 turns-on. This direct path results in the high short circuit power in the third stage of DFF1. In the Fig.3.19a, it is shown that node S2 goes low for half of the input clock period during which M_7 turns-on, creating a direct path from supply to ground since M_{10} is always turned-on during the divide-by-2 operation. The shadow lines indicate the period during which short circuit power is exhibited in the 3rd stage of DFF1.

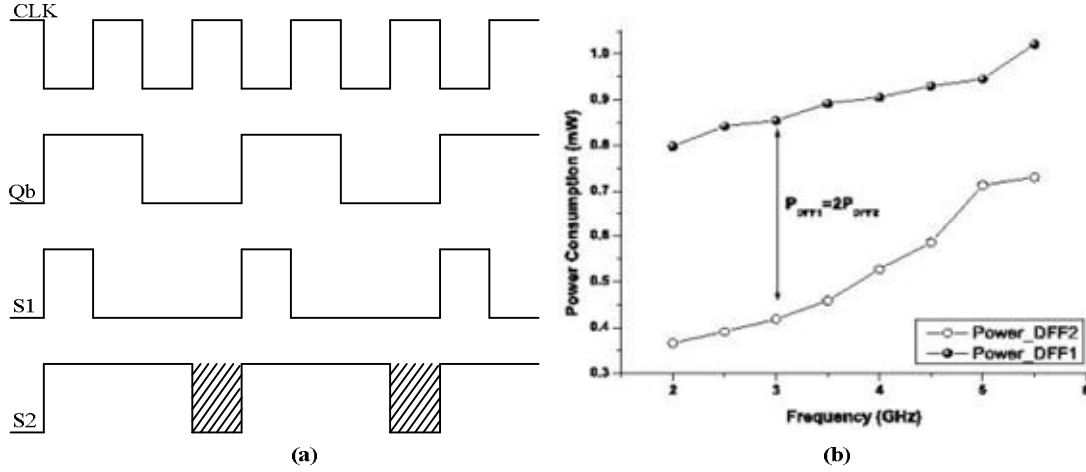


Fig. 3.19 (a) Short circuit power analysis (b) Power consumption of Design-I prescaler during divide-by-2 operation

However in divide-by-2 mode, the power consumption of the prescaler is given by the sum of switching power in DFF1 and DFF2, short circuit power in 3rd stage of DFF1 and short circuit power in DFF2. Since short circuit power is very small in TSPC circuits, the power consumption in divide-by-2 mode is given by

$$P_{2/3_Design-I} = P_{switching_DFF1_Design-I} + P_{switching_DFF2_Design-I} + P_{short_S3_DFF1_Design-I} \quad (3.61)$$

Where,

$$P_{Switching_DFF1_Design-I} = \sum_{i=1}^3 f_{CLK} C_{Li} V_{dd}^2 \quad (3.62)$$

$$P_{Switching_DFF2_Design-I} = \sum_{i=1}^4 f_{CLK} C_{Li} V_{dd}^2 \quad (3.63)$$

Based on the short-circuit power analysis of single stage discussed in the section 3.2.4, a simple simulation is done to analyze the power consumption of DFF1 and DFF2. DFF1 of the Design-I prescaler consumes double the power consumed by DFF2 during the divide-by-2 operation due to the large short circuit power in the 3rd stage of DFF1 which is shown in Fig.3.19b. The simulation results indicate that the Design-I prescaler saves nearly 50% power in divide-by-3 mode and nearly 25%

power in divide-by-2 mode respectively. In order to overcome the short circuit power problem in 3rd stage of DFF1, an improved 2/3 prescaler is proposed in the next section which we call it as Design-II 2/3 prescaler.

3.5. Proposed TSPC 2/3 Prescaler: Design-II

Fig.3.20 shows the proposed ultra-low power 2/3 prescaler (Design-II), a further improved version of Design-I prescaler. In the Design-II prescaler, an extra PMOS transistor M_{1a} is connected between the power supply and DFF1 whose input is the controlled by the logic signal MC . As discussed in the section 3.3.1, during the divide-by-2 operation, one of the inputs of second NOR gate is always zero since transistor M_{10} blocks the data at the input of DFF1 to propagate to the output node. Here, DFF1 is not actively participating in the divide-by-2 operation; however, it contributes to the power consumption due to the continuous switching at the nodes S1 and S2 respectively.

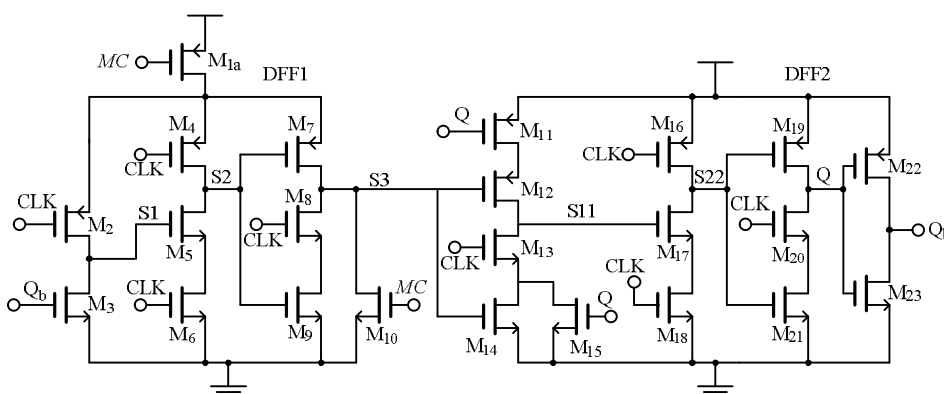


Fig. 3.20 Proposed Design-II TSPC 2/3 prescaler

3.5.1 Divide-by-2 operation

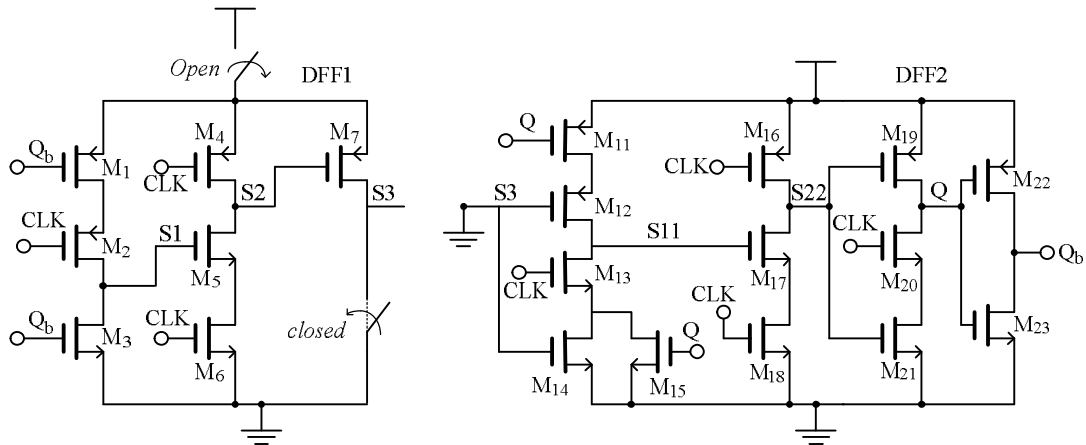


Fig. 3.21 Design-II TSPC 2/3 prescaler: divide-by-2 operation

In this new design, when the control logic signal MC is '1' during the divide-by-2 mode, the PMOS transistor M_{1a} is turned-off and DFF1 is disconnected from the power supply. Fig.3.21 shows the simplified schematic of the Design-II prescaler in the divide-by-2 mode of operation. Even though M_{10} is always turned-on, the source of M_7 is at virtual ground and short-circuit power is completely avoided. Even if the output ' Q_b ' switches continuously, the nodes S1 and S2 and S3 always remain at logic '0' and thus the switching activities are blocked in DFF1 resulting in zero switching power. The total power consumption of the Design-II prescaler is equal to the switching power of DFF2 which is given by

$$P_{2/3_Design-II} = P_{switching_DFF2_DesignII} \quad (3.64)$$

$$P_{Switching_DFF2_Design-II} = \sum_{i=1}^4 f_{CLK} C_{Li} V_{dd}^2 \quad (3.65)$$

3.5.2 Power saving Analysis in Divide-by-2 operation

The percentage of power saved by the Design-II prescaler in the divide-by-2 mode is

ratio of the difference in power consumed by Design-I and Design-II prescalers to the power consumed by Design-I prescaler given by

$$P_{2/3_ \% \text{ saved}} = \frac{P_{2/3_ \text{DesignI}} - P_{2/3_ \text{DesignII}}}{P_{2/3_ \text{DesignI}}} \times 100 \quad (3.66)$$

Since both circuits use same flip-flop DFF2, which consumes the same power in both the circuits during divide-by-2 and divide-by-3 modes, the power saved by the Design-II prescaler is given by subtracting (3.64) from (3.61).

$$P_{\text{Saved_Design-II}} = P_{\text{switching_DFF1_DesignI}} + P_{\text{short_S3_DFF1_DesignI}} \quad (3.67)$$

The flip-flops DFF1, DFF2 of Design-I prescaler are simulated with separate power supply to find out the approximate relation between the power consumption of both D flip-flops during the divide-by-2 operation. Fig.3.19b shows the simulated power consumption of the both the D flip-flops and the results indicate that the power consumed by DFF1 is approximately twice the power consumed by the DFF2. Moreover, from the theoretical analysis it is found that the power consumed by the DFF1 during divide-by-2 operation is almost twice of the power consumed by DFF2. This assumption makes (3.67) simplified and the power consumed in the divide-by-2 mode is rewritten as

$$P_{\text{switching_DFF1_DesignI}} + P_{\text{short_S3_DFF1_DesignI}} = 2(P_{\text{switching_DFF2_DesignI}} + P_{\text{short_DFF2_DesignI}}) \quad (3.68)$$

$$P_{2/3_ \text{Design-I}} = 3(P_{\text{switching_DFF2_DesignI}} + P_{\text{short_DFF2_DesignI}}) \quad (3.69)$$

Thus substituting (3.68) and (3.69) in (3.66), the amount of power saved by the Design-II $2/3$ prescaler in divide-by-2 mode is equal to 67%. Thus the Design-II prescaler saves more than 50% of power compared to other prescalers reported in the literature by switching of the DFF1 during the divide-by-2 operation.

3.6. Measurement results: Design-I and Design-II Prescaler

A complete analysis and comparison of the performance of the proposed TSPC $2/3$ prescalers, the conventional TSPC $2/3$ and E-TSPC based prescalers in [69], [54] is carried out. The prescalers in [54] and [69] are re-simulated at supply voltage of 1.5 V compared to that of the proposed prescalers which is simulated at 1.8 V to have same driving capability for fair comparison. The simulations are performed using Cadence SPECTRE RF for a $0.18 \mu\text{m}$ CMOS process. For silicon verification, the proposed $2/3$ prescalers are fabricated using the chartered 1P6M $0.18 \mu\text{m}$ CMOS process and the PMOS and NMOS transistor sizes are fixed to $3 \mu\text{m}/0.18 \mu\text{m}$, $2 \mu\text{m}/0.18 \mu\text{m}$ respectively. On-wafer measurements are carried out using an 8 inch RF probe station.

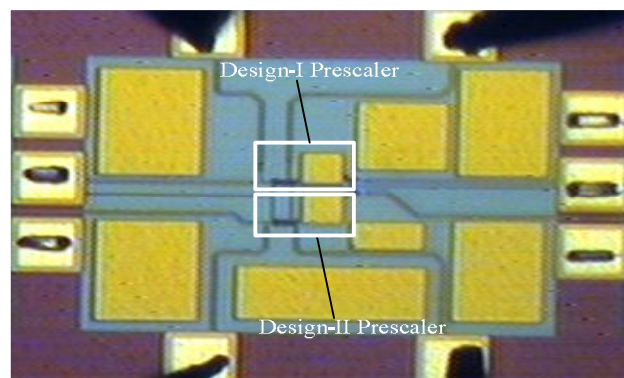


Fig. 3.22 Die photograph of the Design-I and Design-II prescaler

The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wave master 8600A 6G oscilloscope. The phase noise of the prescaler unit is measured using the Agilent E4407B 9 kHz-26.5 GHz spectrum analyzer. Fig.3.22 shows the die photograph of both the proposed Design-I and Design-II prescaler. The measured maximum operating frequency of both proposed 2/3 prescalers is 4.9 GHz. The power consumption of the Design-II prescaler during the divide-by-2 and divide-by-3 modes is 0.6 mW, 0.922 mW respectively, while the power consumed by the Design-I prescaler is 1.33 mW, 0.86 mW respectively when the input frequency is 4.8 GHz.

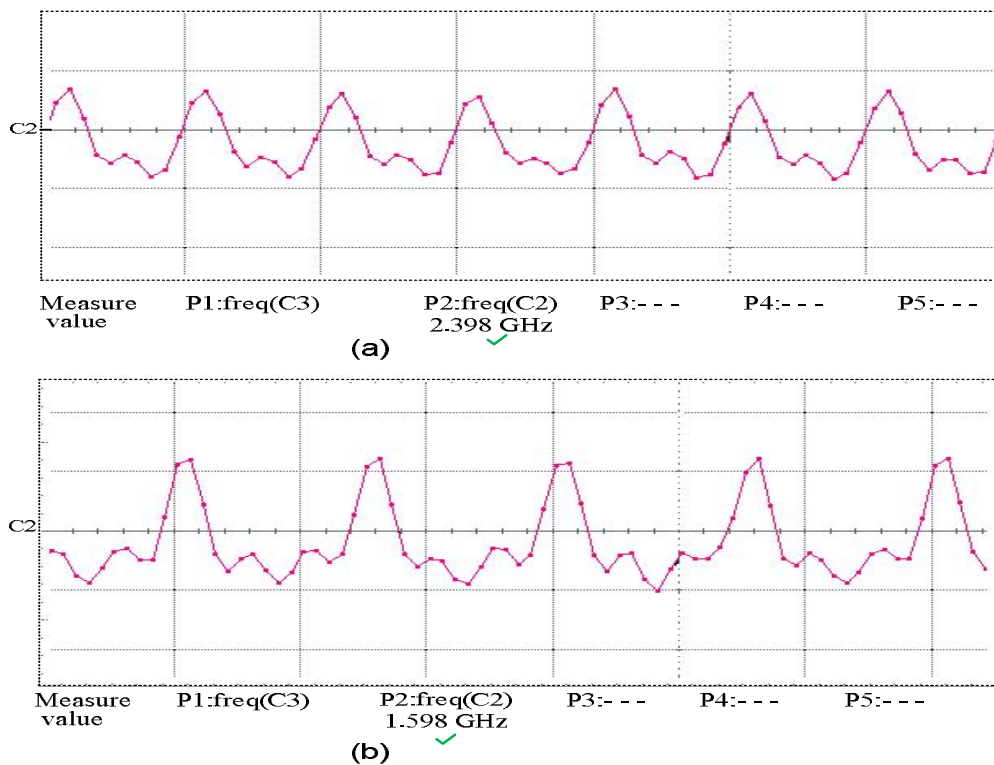


Fig. 3.23 Measured waveforms of the proposed prescaler at 4.8 GHz (a) divide-by-2 mode, (b) divide-by-3 mode

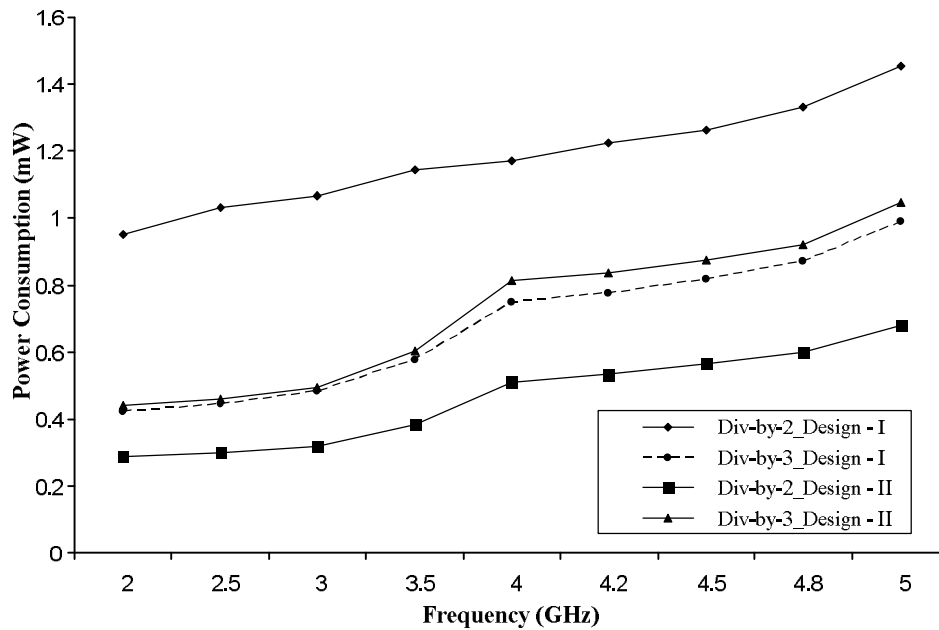


Fig. 3.24 Measured power consumption against frequency of proposed prescalers

Table.3.1 Performance of different prescalers at 2.5 GHz

Design Parameters	Prescaler in [54]	Prescaler in [69]	Design-I Prescaler	Design-II Prescaler
Process	0.18 um	0.18um	0.18um	0.18um
supply voltage	1.5 V	1.5 V	1.8 V	1.8 V
Max.Frequency (GHz)	5.5 / -	6.7 / -	5.5 / 4.9	5.5 / 4.9
(Sim/Measured)				
Power(mW)				
(sim/measured)	1.78 / -	1.43 / -	0.92 / 1	0.25 / 0.3
Divide-by-2 mode				
Power(mW)				
(sim/measured)	1.64 / -	1.54 / -	0.37 / 0.45	0.39 / 0.46
Divide-by-3 mode				

Fig.3.23 shows the measured waveforms of the proposed prescalers at 4.8 GHz during the divide-by-2 and divide-by-3 modes respectively Fig.3.24 shows the

measured power consumptions of the proposed 2/3 prescalers for different frequency of operation.. Table 3.1 compares the performance of the proposed prescalers and the prescalers reported in [69] and [54] at 2.5 GHz respectively. The proposed Design-II prescaler has low power consumption compared to other dynamic logic prescalers reported in the literature.

3.7. Design and Analysis of TSPC 32/33 (N/N+1) Prescaler

To verify the advantages of the proposed ultra-low power prescaler of Design-II, a divide 32/33 dual modulus unit [53], [70] is implemented with the 2/3 prescaler of Design-II as shown in Fig.3.25. In this 32/33 prescaler, the proposed 2/3 prescaler unit is followed by four stages of the toggled TSPC divide-by-2 units.

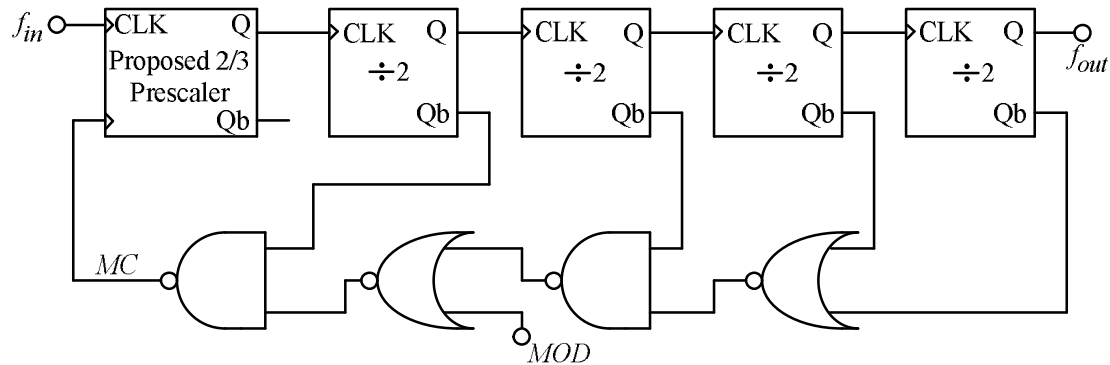


Fig. 3.25 TSPC 32/33 prescaler using Design-II 2/3 prescaler

3.7.1. Divide-by-32 operation (MOD='1')

When the control signal *MOD* is '1', the output of NOR2 always remains at logic '0' and forces the output of NAND2 to logic '1' irrespective of data on Q_{b1} . Since *MC* is always equal to logic '1', the Design-II prescaler remains in divide-by-2. Thus the

32/33 prescaler acts as divide-by-32 circuit. Since control logic signal MC is logically high, DFF1 in the Design-II 2/3 prescaler is completely turned-off for the entire 32 input clock cycles. The 32/33 prescaler consists of both the synchronous (Design-II prescaler) and asynchronous (toggle divide-by-2) circuits and thus the power and speed is traded-off as discussed in the design of digital counters earlier. If we denote the synchronous 2/3 prescaler as $M/M+1$ and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio in this mode ($MOD='1'$) is given by

$$f_{32} = (AD - \overline{MOD}) \times M + \overline{MOD} \times (M + 1) = 32 \quad (3.70)$$

The total power consumed by the 32/33 prescaler using Design-I 2/3 prescaler during divide-by-32 is equal to the sum of switching and short circuit power of the DFF1, DFF2 over 32 clock cycles, power consumed by four asynchronous divide-by-2 circuits, and the power consumed by the logic gates.

$$P_{32_DesignI} = P_{switching_DFF2} + P_{switching_DFF1} + P_{short_S3_DFF1} + P_{div_by-16} + P_{Logicgates} \quad (3.71)$$

The power consumed by the four asynchronous divide-by-2 circuits is given by

$$P_{div_by-16} = \frac{\sum_{i=1}^4 f_p C_{Li} V_{dd}^2}{2^{i-1}} + \sum_{i=1}^4 I_{sci} V_{dd} \quad (3.72)$$

Here, f_p is the frequency of the output signal from the 2/3 prescaler which can be half or one-third of the input clock signal and I_{sci} is the total short-circuit current

of the each asynchronous divide-by-2 circuit. Each of the asynchronous divider toggles at half the operating frequency of the preceding divide-by-2 circuit. Similarly, the power consumed by the 32/33 prescaler during the divide-by-32 operation using the Design-II prescaler is equal to the sum of switching and short circuit power of DFF2 over 32 clock cycles (DFF1 turned-off) and the power consumed by the 4 asynchronous dividers and logic gates. The power saved by the 32/33 prescaler during the divide-by-32 mode using Design-II prescaler is equal to the amount of power consumed by DFF1 of the Design-I prescaler. Here, the power consumed by DFF1 always refers to the Design-I prescaler since power consumed by DFF1 of Design-II prescaler is always zero.

$$P_{32_saved} = P_{switching_DFF1} + P_{short_S3_DFF1} \quad (3.73)$$

3.7.2. Divide-by-33 operation ($MOD='0'$)

The dual-modulus 32/33 prescaler operates as divide-by-33 when $MOD='0'$. By using the combination of logic NOR and NAND gates, the asynchronous divide-by-16 counter is made to count an extra input clock. The control signal MC is given by

$$MC = \overline{Q_{b4}} + \overline{Q_{b3}} + \overline{Q_{b2}} + Q_{b1} + MOD \quad (3.74)$$

In the initial state, the Design-II 2/3 prescaler will be in divide-by-2 mode ($MC='1'$) and the asynchronous divide-by16 starts counting the output pulses of 2/3 prescaler from “0000” to “1111”. When the asynchronous counter value reaches

“1110”, the logic signal MC goes low ($MC='0'$) and the Design-II 2/3 prescaler operates in divide-by-3 mode, where the asynchronous counter counts an extra input clock pulse. During this operation, the 2/3 prescaler operates in divide-by-2 mode for 30 input clock cycles and for the remaining 3 input clock cycles; it operates in divide-by-3 mode. The division of the 32/33 prescaler in this mode is given by

$$f_{33} = (AD - \overline{MOD}) \times M + \overline{MOD} \times (M + 1) = 33 \quad (3.75)$$

where $AD=16$, $MOD='0'$ and $M='2'$. The total power consumed by the 32/33 prescaler using Design-I prescaler during the divide-by-33 operation is equal to the sum of switching power of the flip-flops DFF1, DFF2, short circuit power in the 3rd stage of DFF1 over 30 clock cycles, power consumed by four asynchronous divide-by-2 circuits and the power consumed by the digital gates.

$$P_{32_DesignI} = \frac{30}{33} (P_{short_S3_DFF1}) + P_{switching_DFF2} + P_{switching_DFF1} + P_{div_by-16} + P_{Logicgates} \quad (3.76)$$

Similarly, the power consumed by the 32/33 prescaler using Design-II prescaler during the divide-by-33 operation is equal to the sum of the switching, of DFF2; switching power of DFF1 over 3 clock cycles, power consumed by the 4 asynchronous dividers and digital logic gates.

$$P_{32_DesignII} = \frac{3}{33} (P_{switching_DFF1}) + P_{switching_DFF2} + P_{div_by-16} + P_{Logicgates} \quad (3.77)$$

Since power consumed by DFF2, 4 asynchronous dividers and the logic gates

are same in both cases, the total amount of power saved by the 32/33 prescaler during the divide-by-33 using Design-II prescaler is equal to 0.9 times the power consumed during divide-by-32. The 32/33 prescaler consumes a power of $788 \mu\text{W}$, $807 \mu\text{W}$ during divide-by-32, and divide-by-33 modes respectively at 2.5GHz. The simulations show that the asynchronous stage and logic gates account for about 56% of total power consumption.

3.8. Measurement results: 32/33 Prescaler

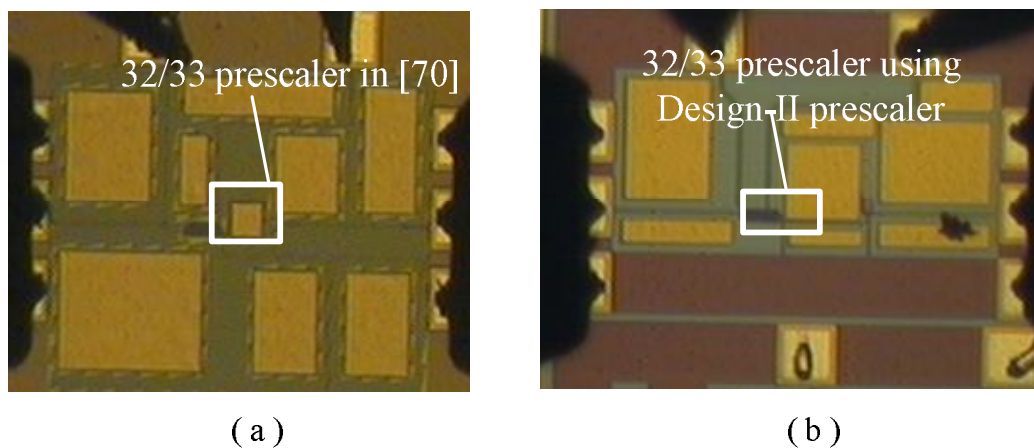


Fig. 3.26 Die photograph of a) 32/33 prescaler in [74] b) 32/33 prescaler using Design-II 2/3 prescaler

The measured results show that the 32/33 prescaler in [70] has maximum operating frequency of 3.2 GHz with a power consumption of 1.7 mW, while the 32/33 prescaler using Design-II 2/3 prescaler has maximum operating frequency of 4.5 GHz with a power consumption of 1.4 mW. The die photograph of the both the 32/33 prescalers is shown in Fig.3.26 and, Fig.3.27 shows the measured waveform of the 32/33 prescaler using Design-II prescaler at 2.5 GHz in divide-by-32, and

divide-by-33 modes respectively.

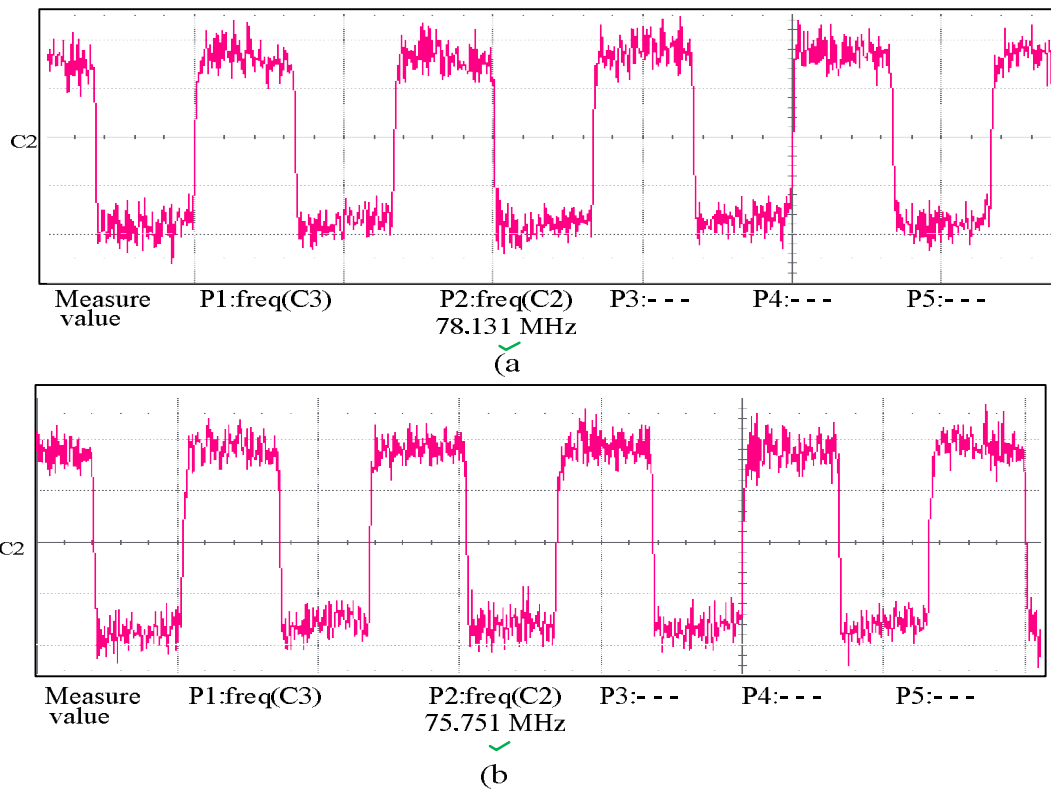


Fig. 3.27 Measured waveforms of the 32/33 prescaler (a) divide-by-32 mode, (b) divide-by-33 mode at 2.5 GHz

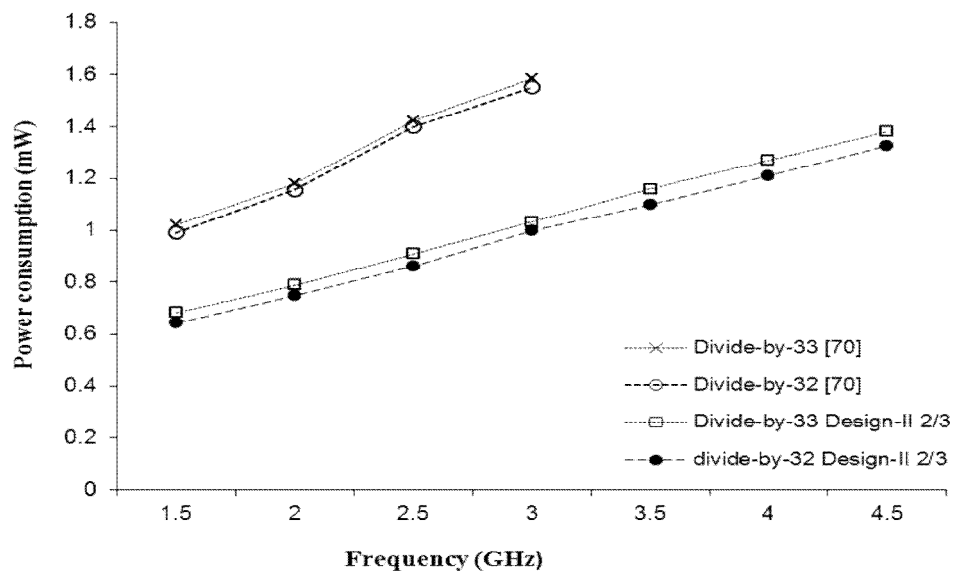


Fig. 3.28 Measured power consumption of the 32/33 prescaler

Fig.3.28 shows the measured power consumption against different frequencies.

This analysis clearly shows the Design-II 2/3 prescaler lowers the power consumption and improves the speed of 32/33 prescaler compared to that of 32/33 prescaler using conventional 2/3 prescaler reported in [53], [70].

3.9. Summary

In this chapter, detailed analysis of digital dividers is performed. Of all the possible digital dividers, dynamic logic dividers are chosen because of their low power and single phase clock. The propagation speed and power consumption analysis between TSPC and E-TSPC is performed and based on this analysis, an ultra-low power Design-I and Design-II TSPC 2/3 prescalers are proposed. The proposed prescalers are silicon verified in the design of dual modulus 32/33 prescaler. The 32/33 prescaler is the critical block in the design of fully programmable divider discussed in the next chapter.

CHAPTER 4

DESIGN OF LOW POWER FULLY PROGRAMMABLE DIVIDERS

4.1. Introduction

Chapter 3 discusses briefly the design of dividers and prescalers. Most integer-N frequency synthesizers are implemented using the pulse-swallow divider topology as discussed in the section 2.5.4.3. The IEEE 802.15.4 and Zigbee standard has 16 channels, spaced 5 MHz apart from 2405 MHz to 2480 MHz. If direct conversion is used in both the TX and RX, then the 16 channel selection frequencies would be from 2405 MHz to 2480 MHz in steps of 5 MHz. If a low IF architecture is used for the RX, then the channel selection frequencies could be different for the both TX and RX. In order to have more flexibility to accommodate channel selections for both kind of architecture, the resolution of the divider and reference frequency chosen is 1 MHz which gives a resolution of 1 MHz to the channel selection frequency. For example, if the IF frequency is chosen to be 2 MHz, the divider is programmed to have the channel frequencies equal to 2403, 2408....2478 MHz or 2407, 2412....2482 MHz.

4.2. Fully Programmable Divider: Design-I

For PLL synthesizers operating in the 2.4 GHz ISM band [9], [10], with a resolution of 1MHz and division ratios of 2400-2484 can be achieved with a 32/33 prescaler, a 7 bit P-counter and a 5 bit S-counter. Fig.4.1 shows the Design-I fully programmable

divider with a division ratio from 2400 to 2484 in steps of 1. In this design, only bits P_1 , P_2 and P_3 of the P-counter are used programming and the bits P_4 , P_5 , P_6 and P_7 are fixed at '1', '0', '0' and '1' respectively to have P-values between 74-77. Here all the bits of S-counter are used for programming. The P and S counter's programmable value for the division ratios between 2400-2484 is shown in Table 4.1. This chapter briefly discusses the design of a fully programmable 1MHz resolution divider based on pulse swallow divider [16] topology.

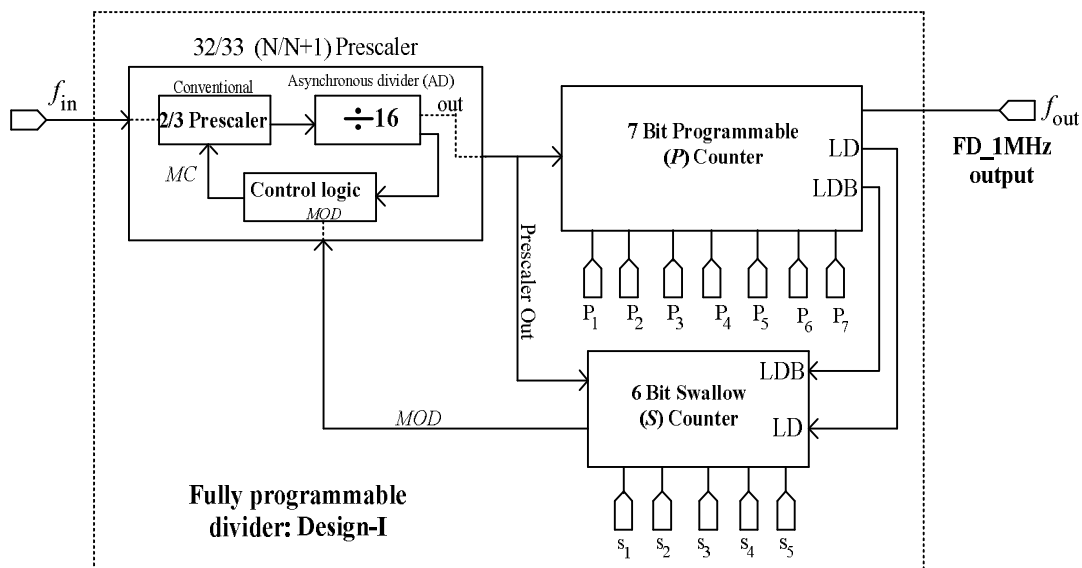


Fig. 4.1 Fully programmable divider: Design-I

Table 4.1 Programmable values of the programmable counters

Frequency division ratio	Prescaler (N/N+1)	Programmable counter (P)	Swallow counter (S)
2400-2431	N=32	P=75	S=0-31
2432-2463	N=32	P=76	S=0-31
2464-2484	N=32	P=77	S=0-20

4.2.1. Prescaler ($N/N+1$)

A 32/33 prescaler is used in this project for the design of the fully programmable divider. To provide a 1 MHz resolution, the maximum programmable value of the swallow S-counter should be less than the value of the prescaler ($S < N$) and the value of S-counter value should be always less than P-counter value ($S < P$) to satisfy the conditions of pulse-swallow topology. So, a 64/65, 128/129 [51], [52] prescaler cannot be used for the implementation of 1 MHz resolution divider with division ratio between 2400 and 2484. A 16/17 prescaler can be used, but this will increase the complexity of the programmable P-counter and the input frequency at which the two counters operate. If a 32/33 prescaler, which is briefly discussed in the chapter 3 is used, the maximum programmable value of swallow S-counter is equal to 31 ($S = N - 1$).

4.2.2. Programmable P-counter

The 32/33 prescaler scales the input 2.4 GHz signal by a value of 32 or 33 such that the P and S counters will be working in the frequency range of 72 - 78 MHz in order to obtain the 1 MHz frequency output [70]. The design requirements of the P-counter in the design of 2.4 GHz fully programmable divider are as follows:

- Operate at frequencies of up to several 100 MHz with low power consumption.
- Able to program the desired P values from 74 to 77.
- To generate full-swing output, which is fed to the phase frequency detector block

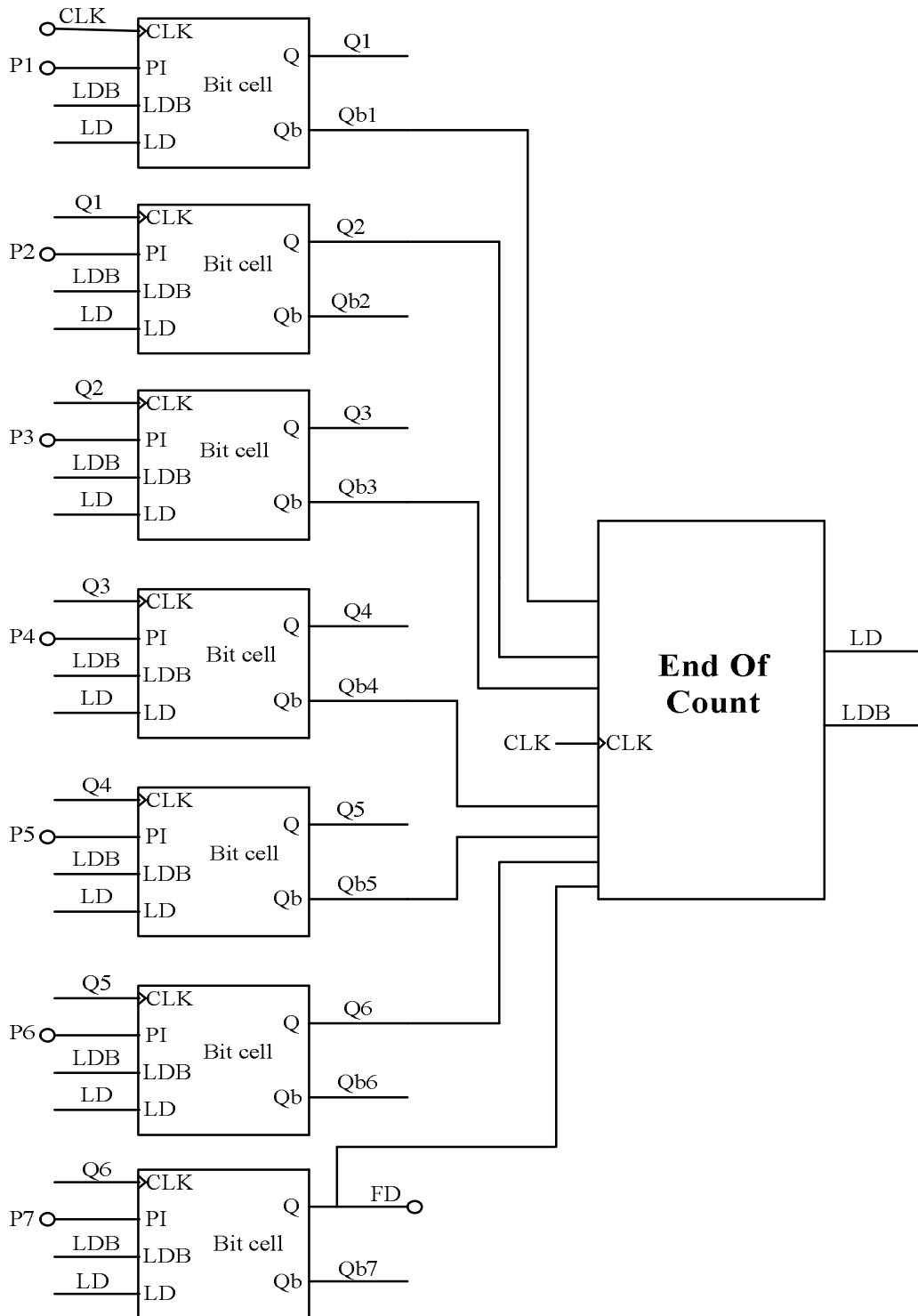


Fig. 4.2 A 7-bit programmable P-counter

The programmable P-counter used in the design of the fully programmable divider is a 7-bit asynchronous down counter as shown in Fig.4.2. The P-counter is designed with 7 reloadable TSPC D flip-flops (DFF) and an end-of-count (EOC) detector

which has reload circuit in it [71]. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF's are loaded by the programmable pins P₁-P₇. As the counter is triggered by the output of the prescaler, the P-counter starts down counting till the state "0000000" is reached. Once this state is detected by the EOC logic circuit, the load (LD) signal goes high to reset all loadable FF's to the initial state.

4.2.2.1. Operation of EOC logic

The EOC logic circuit is used to detect when the P-counter reaches the state " $Q_1Q_2Q_3Q_4Q_5Q_6Q_7=0000000$ ", and preset the reloadable FF's to the initial state so that P-counter starts down counting again from the loaded value to the final state. The EOC logic circuit is built with a 2-input NOR, two 3-input NAND and an embedded NOR DFF as shown in Fig.4.3a and the Fig.4.3b shows the equivalent transistor level schematic of the embedded NOR-DFF. Here all the complementary outputs of the reloadable FF's are given to EOC logic circuit to detect the state " $Q_{b1}Q_{b2}Q_{b3}Q_{b4}Q_{b5}Q_{b6}Q_{b7}=1111111$ " to simplify the EOC circuit. Fig.4.4 shows the timing diagram of the EOC logic circuit. When the P-counter reaches the penultimate state (" $Q_1Q_2Q_3Q_4Q_5Q_6Q_7=0000001$ "), the following events occur during the next rising edge of the clock:

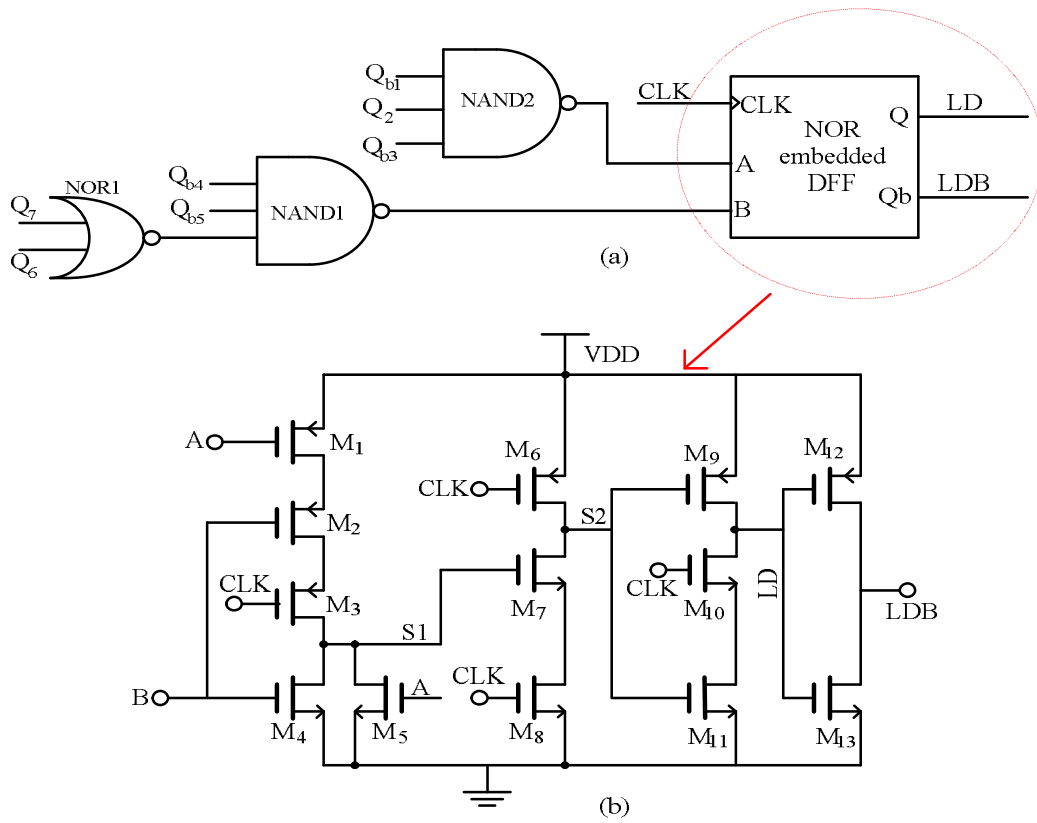


Fig. 4.3 a) EOC logic circuit for P-counter b) NOR embedded TSPC DFF

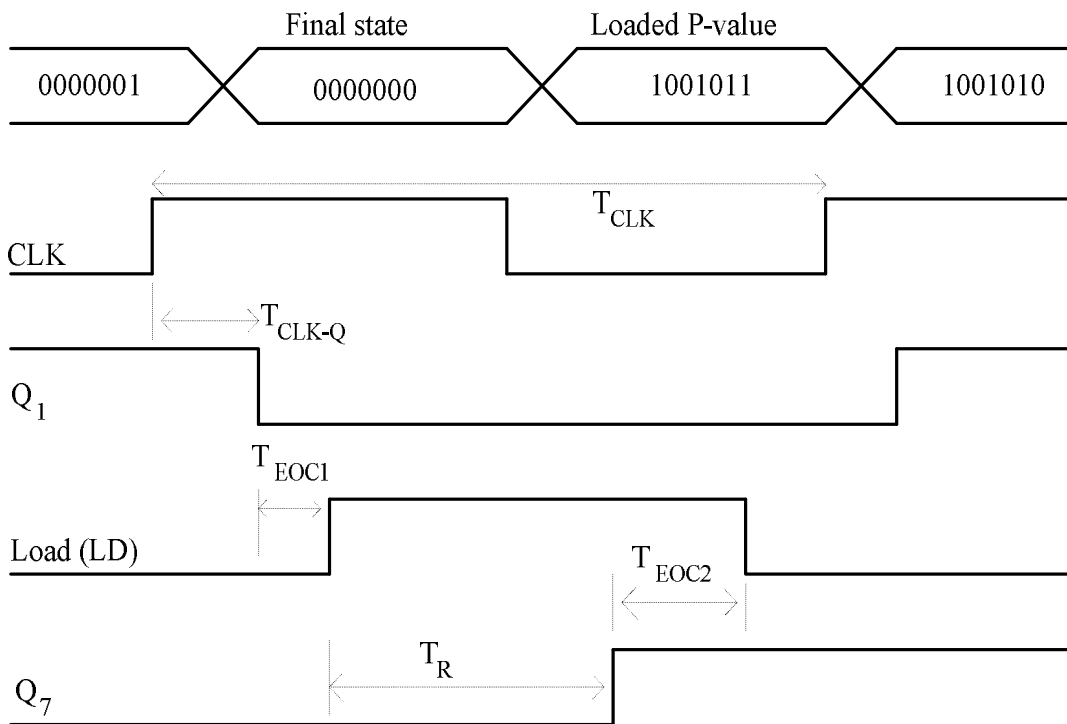


Fig. 4.4. Timing diagram of 7-bit P-counter

- The counter enters the final state “0000000” after a CLK-to-Q delay T_{CLK-Q} where the input to the EOC is “1111111”.
- The delay of EOC logic circuit is T_{EOC1} after which the EOC logic circuit output goes high (LD='1') to reload the FF's with initial programmable values. In this case P=75 or “1001011”.
- There is a reloading delay time of T_R for the P-counter to reload the initial state.
- The output of EOC logic circuit goes low only after a delay of T_{EOC2} after the P-counter is loaded with the preset value.
- There exists a time delay of T_{EN} where the LD goes low and the counter starts counting from the loaded value.

From the above timing diagram, it is found that all the delays must be less than a single clock period for the counter to function correctly. The relation between all the delays and clock period is given by

$$T_{CLK} > T_{CLK-Q} + T_{EOC1} + T_{EOC2} + T_R + T_{EN} \quad (4.1)$$

From the above delay analysis, it is found that the counter speed can be increased by reducing the CLK-to-Q (T_{CLK-Q}) delay. For the counter to function correctly, instead of detecting all zero's state, a previous state is made to detect by the EOC logic circuit to avoid the delays introduced by the reloadable FF's and logic gates of the EOC circuit. The logic gates introduce glitches since all the outputs from the reloadable

FF's are not arrived at the same time. To avoid all the glitches passing to the input of reloadable FF's, a TSPC DFF is introduced between the logic gates and the reloadable FF's. The NOR gate is embedded in to the DFF to reduce the delay.

By introducing NOR-embedded DFF, the signals A and B are latched to output "LD" only at the rising edge of the clock signal. In this design we chose to detect the state "0000010". When the state "0000010" is reached, the signals A and B go low after a delay introduced by the logic gates which is assumed to be less than half of the input clock cycle. However, the output of the embedded-NOR gate is latched to output only at the next rising edge of clock after the state "0000001" is reached. This output "LD" signal will initialize the P and S counters and the counting process continues. If the state "0000001" is chosen to detect, then it results in the undercounting due to the delays.

4.2.2.2. Reloadable TSPC DFF for P-Counter

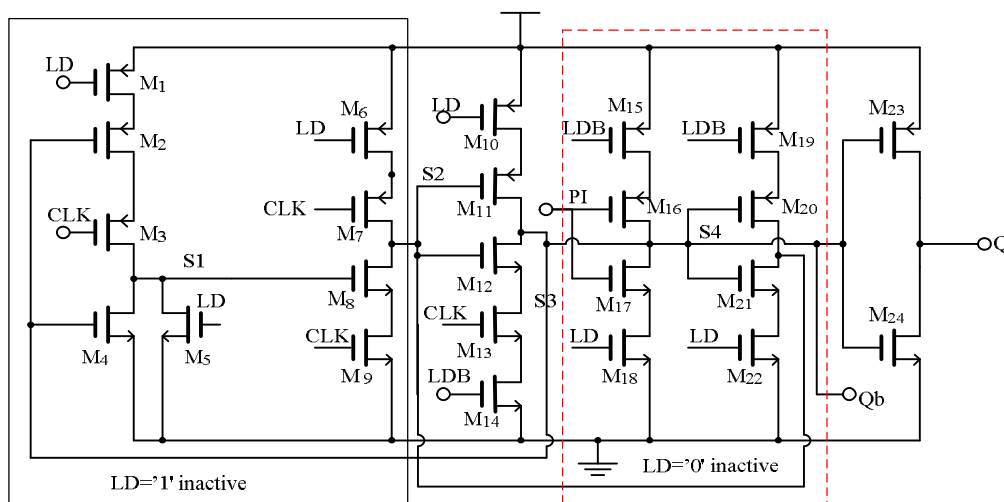


Fig. 4.5 Reloadable DFF for P-counter

Fig.4.5 shows the schematic of reloadable TSPC DFF [72] used in the design of the 7-bit P-counter. This reloadable FF is similar to the original nine transistors TSPC DFF [59], [60] with reloadable functions added to it. The reloadable FF is programmed through the input 'PI'. The signals 'LD' and 'LDB' are used to reload the programmable state of the FF.

Operation of Reloadable DFF

Once the programmable input (PI) of the each reloadable FF is loaded with a value and LD signal goes low, the P-counter begins to count down. Under this condition, the right hand side of the reloadable DFF as highlighted in Fig.4.4 is deactivated and transistor M_5 is turned-off such that the FF acts as a divide-by-2 circuit where node S3 is complimentary of the divide-by-2 output. The FF remains in the divide-by-2 mode until the counter reaches the state "0000010".

When $LD='1'$, the first two stages of the reloadable FF is deactivated and node S1 always remains at logic '0' since the transistor M_5 is turned-on. Since node S1 is at logic '0', node S2 should be at logic '1'. However, node S2 is overridden by the complimentary value of node S4. Under this condition ($LD='1'$), if the programmable input $PI='0'$, nodes S4 and S2 switch to logic '1' and '0' respectively. The value at node S2 is latched to the output node Q on the next rising edge of the clock. Similarly, if $PI='1'$, the output Q switches to '1' on the clock rising edge.

However when LD='0', the bit-cell acts as a divide-by-2 circuit irrespective of the PI value. Fig.4.6 shows the transient simulation results of the P-counter with a 100MHz input signal. Table 4.2 shows the operation of the reloadable FF.

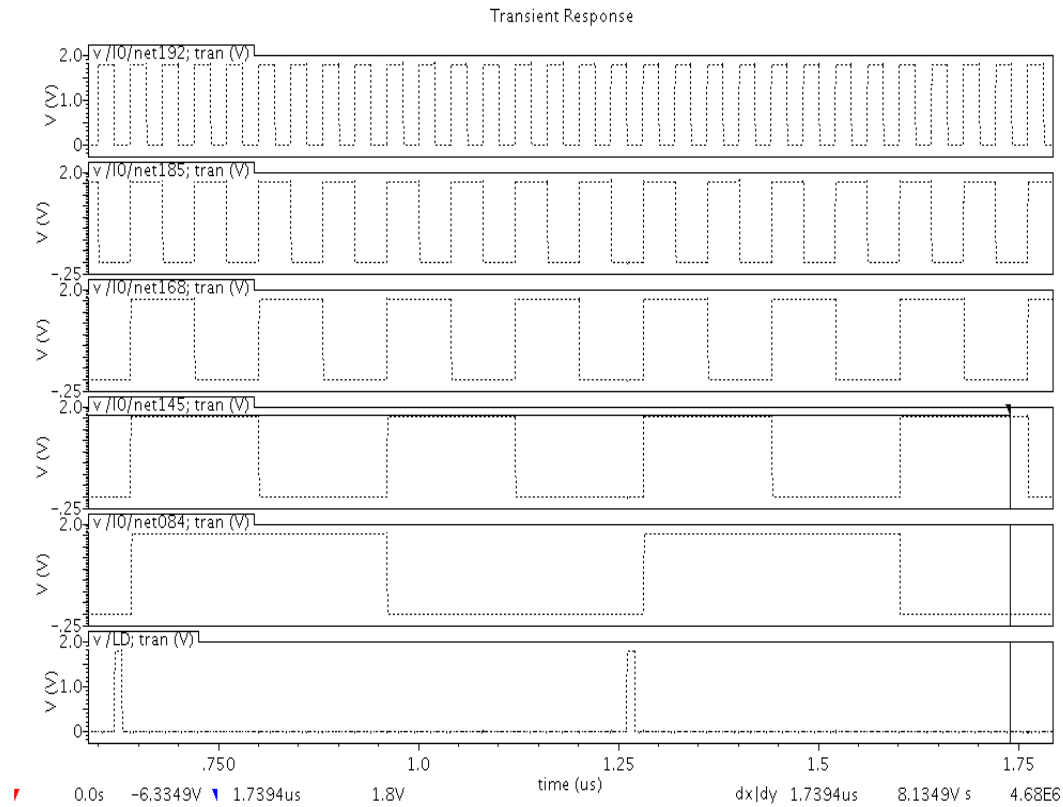


Fig. 4.6 Transient simulation results of the 7-bit P-counter

Table 4.2 Operation of the Reloadable DFF of the P-counter

Load (LD)	Programmable Input (PI)	Output (Q)
0	0	CLK/2
0	1	CLK/2
1	0	0
1	1	1

4.2.3. Swallow S-counter

The fully programmable divider also consists of a 5-bit swallow S-counter whose design requirements are as follows:

- To operate at frequencies of up to several 100 MHz with low power consumption.
- To load the programmable S values from 0 to 31 in steps of one and stop the operation when S counting is finished.
- To generate a full-swing output, this is given as feedback signal to phase frequency detector block.

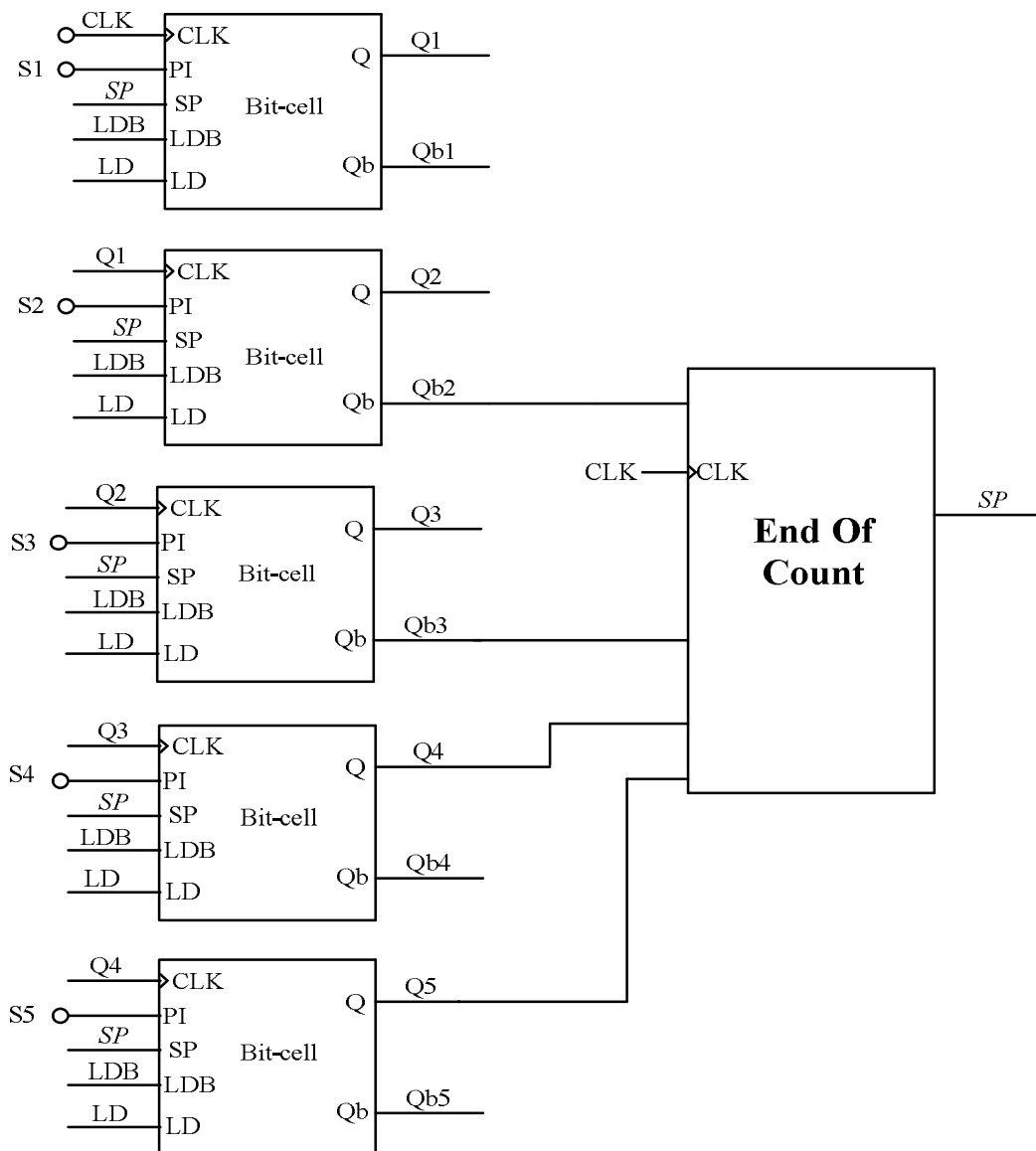


Fig. 4.7 A 5-bit Swallow S-counter

The swallow S-counter used in the design of the fully programmable divider is a 5-bit asynchronous down counter as shown in Fig.4.7. The S-counter is designed with 5 reloadable TSPC D flip-flops and an end-of-count (EOC) detector with the reload circuit [71]. Since the counter is asynchronous and based on the ring topology, the complementary output of the first DFF is fed as clock to the input of next flip-flop. In the initial state, all the reloadable FF's are loaded by the programmable value set by pins S_1 - S_5 . In the S-counter all states from 0-31 are usable and adjustable in steps of 1 to obtain a resolution of 1MHz. Once the counter is triggered by the output of the prescaler, the S-counter starts down counting till the final state is reached, which is detected by the EOC logic circuit and the stop (SP) signal goes high until the P-counter finishes its counting. Since the value of 'P' is always greater than value of 'S' in pulse-swallow divider, the S-counter remains idle for a period of $(P-S)*N$ clock cycles. The EOC logic circuit for the S-counter is shown in Fig.4.8.

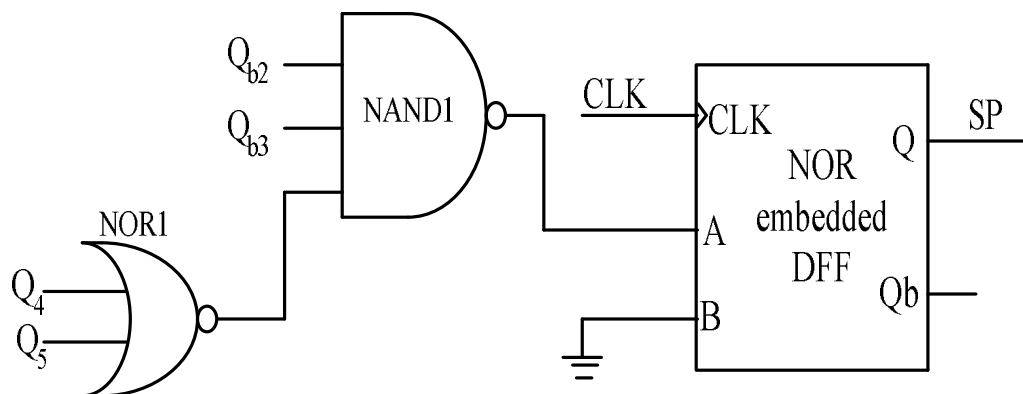


Fig. 4.8 EOC logic circuit for S-counter

As discussed earlier, the signal SP goes high only when the outputs of all the

reloadable DFF in the S-counter go low and remain in the same state until the LD signal from the P-counter goes high. The state where SP remains at logic high indicates the S-counter has finished counting. The S-counter cannot use the EOC logic circuit of the P-counter since SP has to remain high until the P-counter reaches the state “0000010” when the LD signal goes high for one clock cycle. Moreover in the S-counter, all zero state is detected by EOC circuit unlike in the P-counter.

Since the S-counter uses all available states from 0-31 and the EOC circuit detects the state “00000”, SP signal goes high only during the next clock cycle which results in the counting of an extra clock cycle. In order to avoid to the counting of extra clock cycle, state “ $Q_5Q_4Q_3Q_2=0000$ ” is detected and the least significant bit (Q_1) is neglected. The output of the NAND2 gate switches to logic ‘0’ as soon as the S-counter reaches the state “0000”. Since the other input of the embedded NOR gate is always ‘0’, SP goes high during the next rising edge of the clock cycle and the S-counter remains idle until it is triggered by LD signal from the P-counter.

4.2.3.1. Reloadable TSPC DFF for S-Counter

Fig.4.9 shows the schematic of an improved reloadable TSPC DFF used in the design of 5-bit S-counter. This reload DFF is similar to the reloadable DFF used in the design of P-counter [72]. However, the reloadable DFF for the S-counter needs an extra logic function SP to be incorporated.

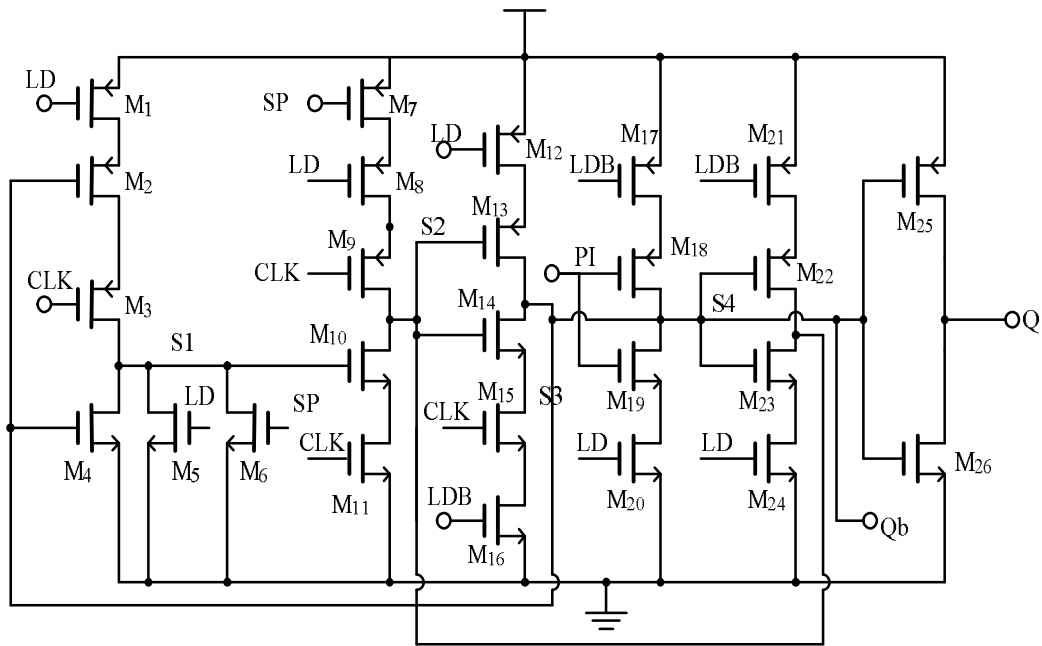


Fig. 4.9 Reloadable DFF for S-counter

Operation of reloadable DFF for S-counter:

When SP goes high, the S-counter remains idle for a period of $N*(P-S)$ clock cycles and the reloadable DFF of the S-counter consumes some switching power. In the improved design, transistors M_6 and M_7 are added to reduce the switching activities in the reloadable DFF. When the state “0000” is reached, SP goes high, M_6 is turned-on and M_7 is turned-off such that node S1 and S2 remain at logic ‘0’ for the remaining $N*(P-S)$ clock cycles until LD becomes high. During this period, since $LD=’0’$, the right hand side portion of the circuit is de-activated similar to the reloadable DFF of the P-counter. Thus there is no switching activity at any node during the idle state of the S-counter and switching power is saved for a period of $N*(P-S)$ clock cycles.

In other conditions, the operation of the improved reloadable DFF for

S-counter is similar to the operation of the reloadable DFF in P-counter described earlier. Fig.4.10 shows the transient simulation results of the S-counter with a 100MHz input signal. Table 4.3 shows the operation of reloadable DFF used in the S-counter.

Table 4.3 Operation of the Reloadable DFF of the S-counter

Stop (SP)	Load (LD)	Programmable Input (PI)	Output (Q)
1	X	X	1
0	0	0	CLK/2
0	0	1	CLK/2
0	1	0	0
0	1	1	1

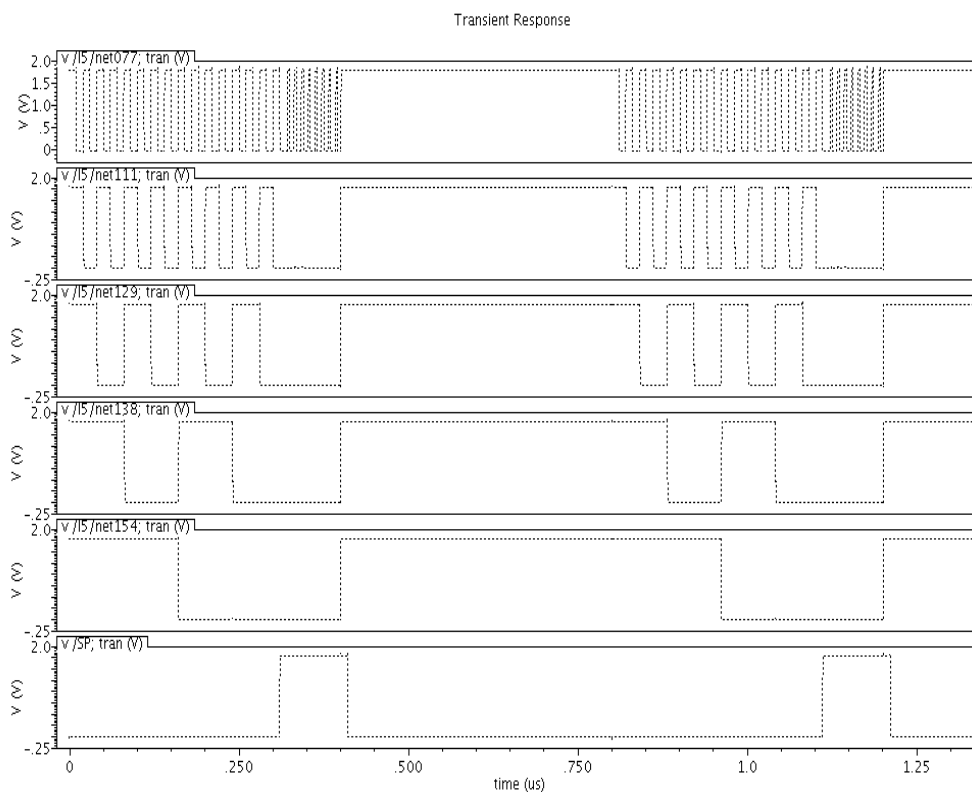


Fig. 4.10 Transient simulation results of the 5-bit S-counter

4.3. Simulation and Measured results

The simulations of the fully programmable divider with 1MHz resolution are

performed using Cadence SPECTRE RF for a 0.18 μ m CMOS process. Fig.4.11 shows the post layout simulation results of the fully programmable divider. The post-layout simulations are performed by giving a 2.4GHz sinusoidal signal with amplitude of 450 mV (peak) to the prescaler. Here the programmability of the divider is set to 2400 and the results indicate that the output of the fully programmable divider is 1MHz with duty cycle less than 25%.

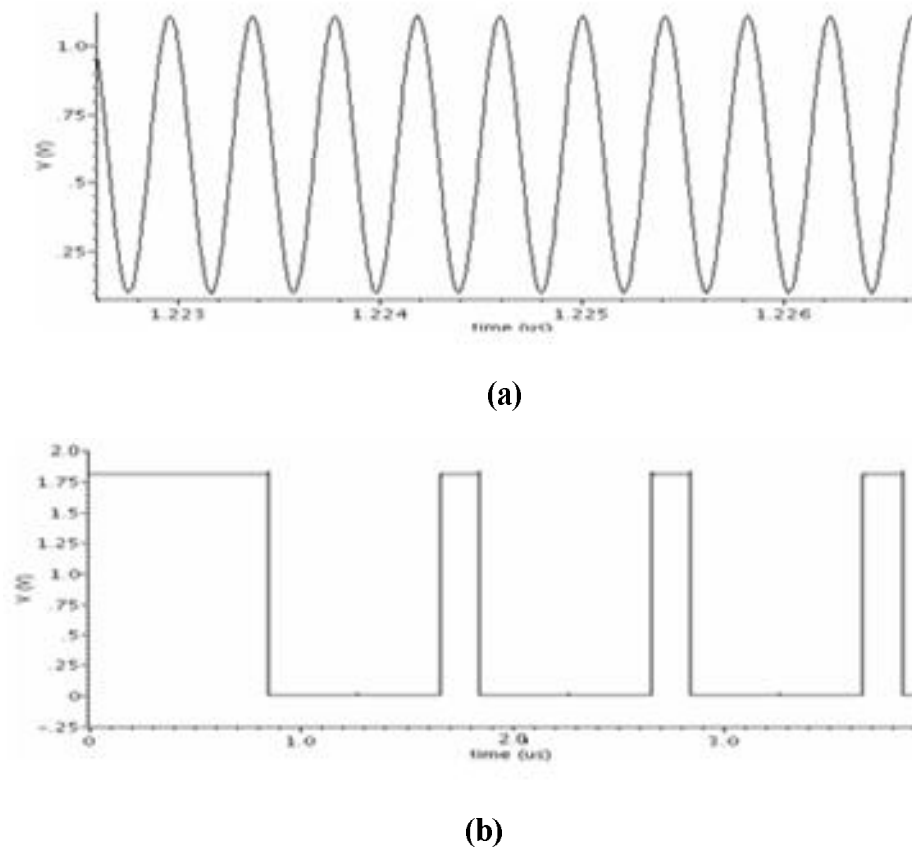


Fig. 4.11 Post layout transient simulation results with division ratio of 2400 a) input 2.4 GHz signal b) output 1 MHz signal

The low duty cycle is due to the large difference between programmability P value, prescaler N value and the S -counter S value ($P \gg N$ and $P \gg S$). For silicon verification, the proposed fully programmable divider along with VCO is fabricated

using the Global Foundries 1P6M 0.18 μm CMOS technology. Fig.4.12 and Fig.4.13 shows the die photograph and the measured output waveform of the proposed fully programmable divider respectively.

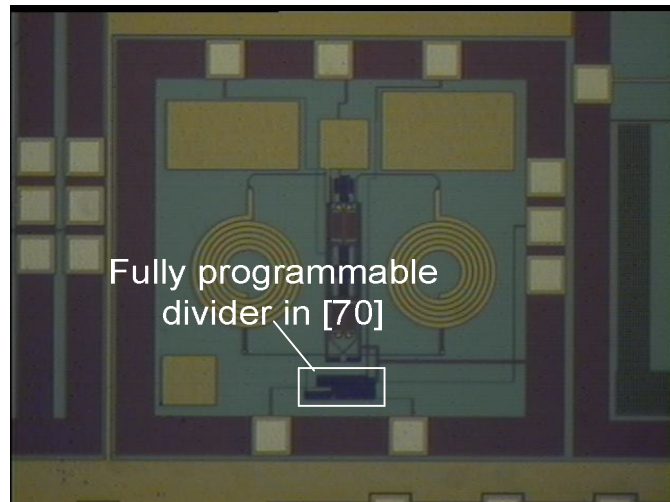


Fig. 4.12 Die photograph of the proposed fully programmable divider



Fig. 4.13 Measured results of the proposed fully programmable divider

4.4. Proposed TSPC 47/48 prescaler

To overcome the problem of low duty cycle of the 1 MHz output signal of the programmable divider discussed in the previous section, the gap between P and N

values should be reduced satisfying the condition $P > S$ and $S_{max} = N - 1$. Since the designed fully programmable divider uses a 32/33 prescaler ($N = 32$), the next possible prescaler is 64/65 ($N = 64$) [51] which makes P value smaller than S for the division ratio between 2400 and 2484. One of the options is to design a prescaler with N value greater than 32 and lesser than 64 ($32 < N < 64$) and holding the condition $P > S$ and $N > S$ true. To design a prescaler with N value between 32 and 64, an additional FF is required which increases the power consumption, complexity and reduces the maximum operating speed. To avoid all the complexity in designing a prescaler with N value between 32 and 64 without an additional FF, we have proposed a 47/48 prescaler as shown in Fig.4.14.

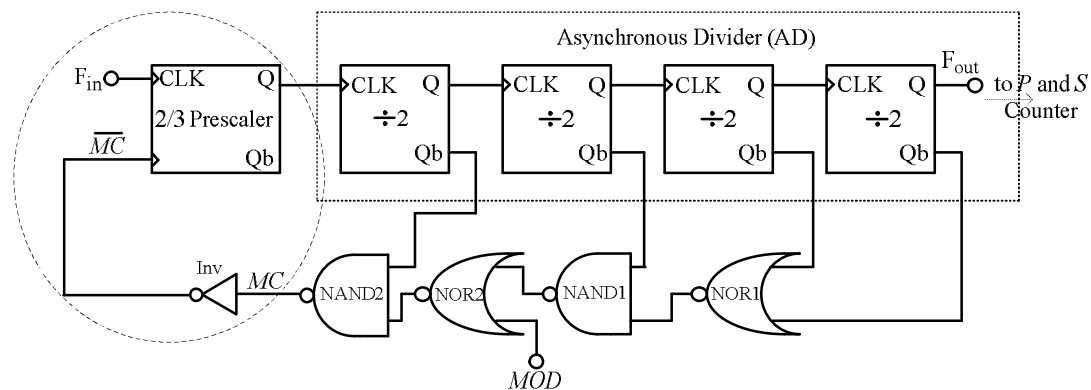


Fig. 4.14 Proposed TSPC 47/48 prescaler

The proposed 47/48 prescaler circuit is similar to the 32/33 prescaler except for an additional inverter which is added between the output of the NAND2 gate and the control signal (MC) input of the 2/3 prescaler. The 47/48 prescaler consists of Design-II 2/3 prescaler [73], four asynchronous divide-by-2 circuits and additional

logic gates to control the division ratio between 47 and 48. When $MC='0'$, the $2/3$ prescaler of the $32/33$ prescaler operates in divide-by-3 mode whereas the $2/3$ prescaler in the proposed $47/48$ prescaler operates in divide-by-2 mode. Thus the inverter swaps the operation modes of the $2/3$ prescaler.

4.4.1. Divide-by-48 operation ($MOD='1'$)

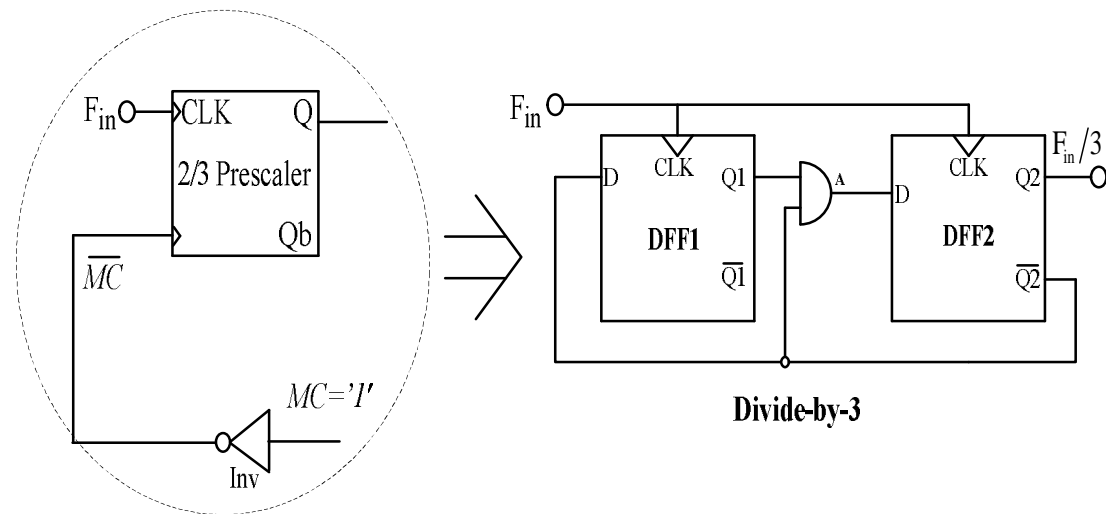


Fig. 4.15 Divide-by-48 mode of operation

When the control signal MOD is '1', the output of NOR2 in Fig.4.14 always remains at logic '0' and forces the output of NAND2 to logic '1' irrespective of data on Q_{b1} . Since MC is always equal to logic '1' ($\overline{MC} = '0'$), the $2/3$ prescaler remains in divide-by-3 mode. The equivalent circuit of inverter and the $2/3$ prescaler is equal to divide-by-3 counter as shown in Fig.4.15. Thus the $47/48$ prescaler operates in divide-by-48 mode when $MOD='1'$. The transient simulation of divide-by-48 mode of operation is shown in Fig.4.16. If we denote the synchronous $2/3$ prescaler as $M/M+1$

and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio of the 47/48 prescaler in this mode ($MOD='1'$) is given by

$$f_{48} = (AD - \overline{MOD}) \times (M + 1) + \overline{MOD} \times M = (16 - 0) \times (2 + 1) + 0 \times 2 = 48 \quad (4.2)$$

4.4.2. Divide-by-47 operation ($MOD='0'$)

The proposed 47/48 prescaler [74] operates as divide-by-47 when $MOD='0'$. By using the combination of logic NOR and NAND gates, the asynchronous divide-by-16 counter is made to count an extra input clock. The control signal MC is given by (3.76). In the initial state, the 2/3 prescaler will be in divide-by-3 mode ($MC='1'$) and the asynchronous divide-by16 starts counting the output pulses of 2/3 prescaler from "0000" to "1111". When the asynchronous counter value reaches "1110", the logic signal MC goes low ($MC='0'$) and 2/3 prescaler operates in divide-by-2 mode, where the asynchronous counter counts an extra input clock pulse. During this operation, the 2/3 prescaler operates in the divide-by-3 mode for 45 input clock cycles and in the divide-2 mode for 2 input clock cycles. The transient simulation of divide-by-47 mode of operation is shown in Fig.4.17. The division ratio of the 47/48 prescaler in this mode is given by

$$f_{47} = (AD - \overline{MOD}) \times (M + 1) + \overline{MOD} \times M = (16 - 1) \times (2 + 1) + 1 \times 2 = 47 \quad (4.3)$$

The Post layout simulation results shows that the proposed dual modulus 47/48 prescaler consumes a current of 269.3 uA and 262.8 uA during the divide-by-47 and

divide-by-48 modes respectively and the maximum operating frequency is 4.8 GHz.

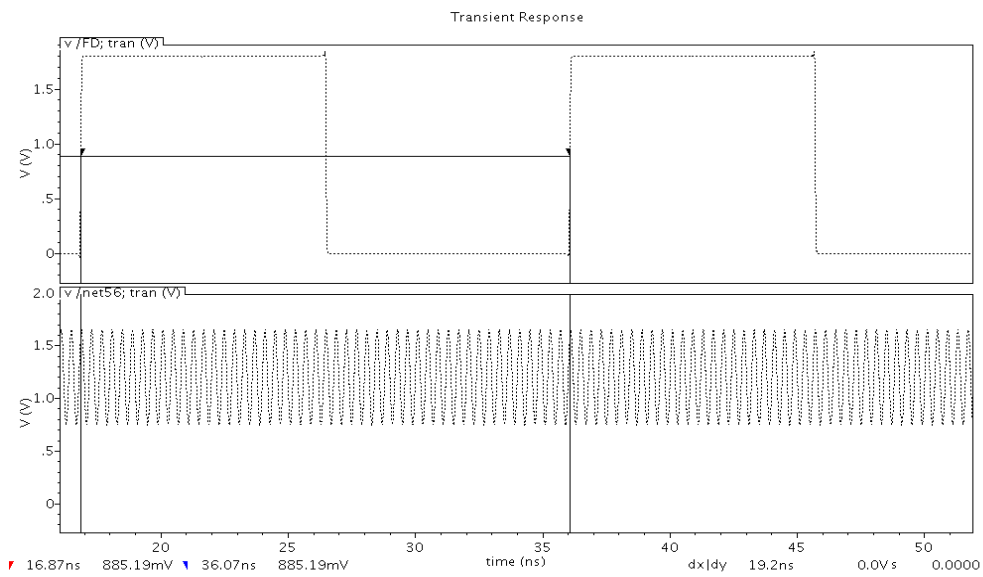


Fig. 4.16 Transient simulations of divide-by-48 mode of operation

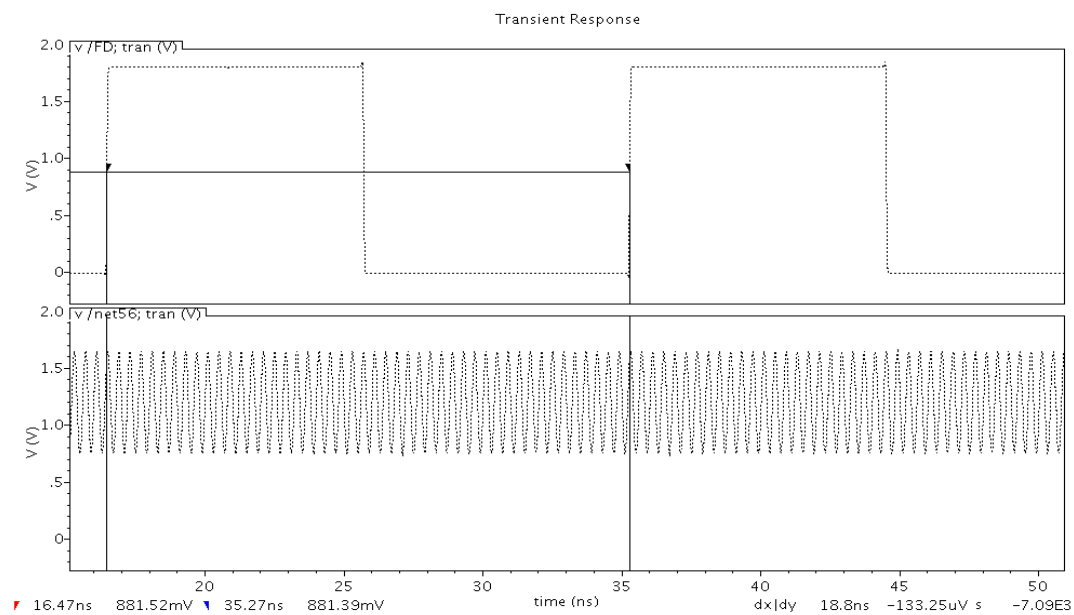


Fig. 4.17 Transient simulations of divide-by-47 mode of operation

4.5. Fully programmable divider: Design-II

For the IEEE 802.15.4 standard, to obtain a 1 MHz resolution for division ratios between 2400-2484 with a 47/48 prescaler, a 6-bit P-counter and a 6-bit S-counter is required as shown in Fig.4.18. In this design-II, the P-counter is programmable from

51 to 52 (P_1 and P_2 are only programmable) and the S-counter is programmable from 0 to 47 (S_1 to S_6) in steps of 1 to accommodate division ratios from 2400 to 2484. The frequency division (FD) performed by the programmable divider is given

$$FD = N \times S + ((N + 1) \times (P - S)) = ((N + 1) \times P) - S \quad (4.4)$$

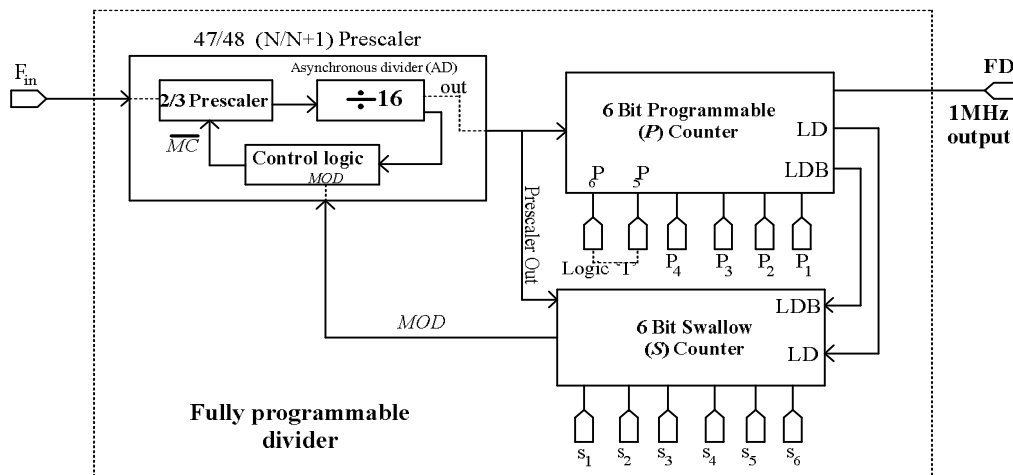


Fig. 4.18 Fully programmable divider: Design-II

The frequency division (FD) in (4.4) is different to the conventional division ratio ($NP+S$) performed by pulse-swallow divider discussed in the previous sections [70] due to the dual-modulus 47/48 prescaler. When $P_1=$ ”1”, $P_2=$ ”1” and $P_3=$ ”0”, the P-counter is loaded to a value of 51 and S-counter is programmed from 0 to 47 to accommodate division ratio from 2400 to 2448 in steps of “1”. When $P_1=$ ”0”, $P_2=$ ”0” and $P_3=$ ”1”, the P-counter is loaded to a value of 52 and S-counter is programmed from 14 to 47 to accommodate division ratio from 2448 to 2483 in steps of “1”. The P and S counter’s programmable value for the division ratios between 2400-2484 is shown in Table 4.4.

Table 4.4 Programmable values of the programmable counters

Frequency division ratio	Prescaler ($N/N+1$)	Programmable counter (P)	Swallow counter (S)
2400-2448	$N=47$	51	0-47
2449-2484	$N=47$	52	14-47

4.5.1. Programmable P-counter and S-counters: 6-bit version

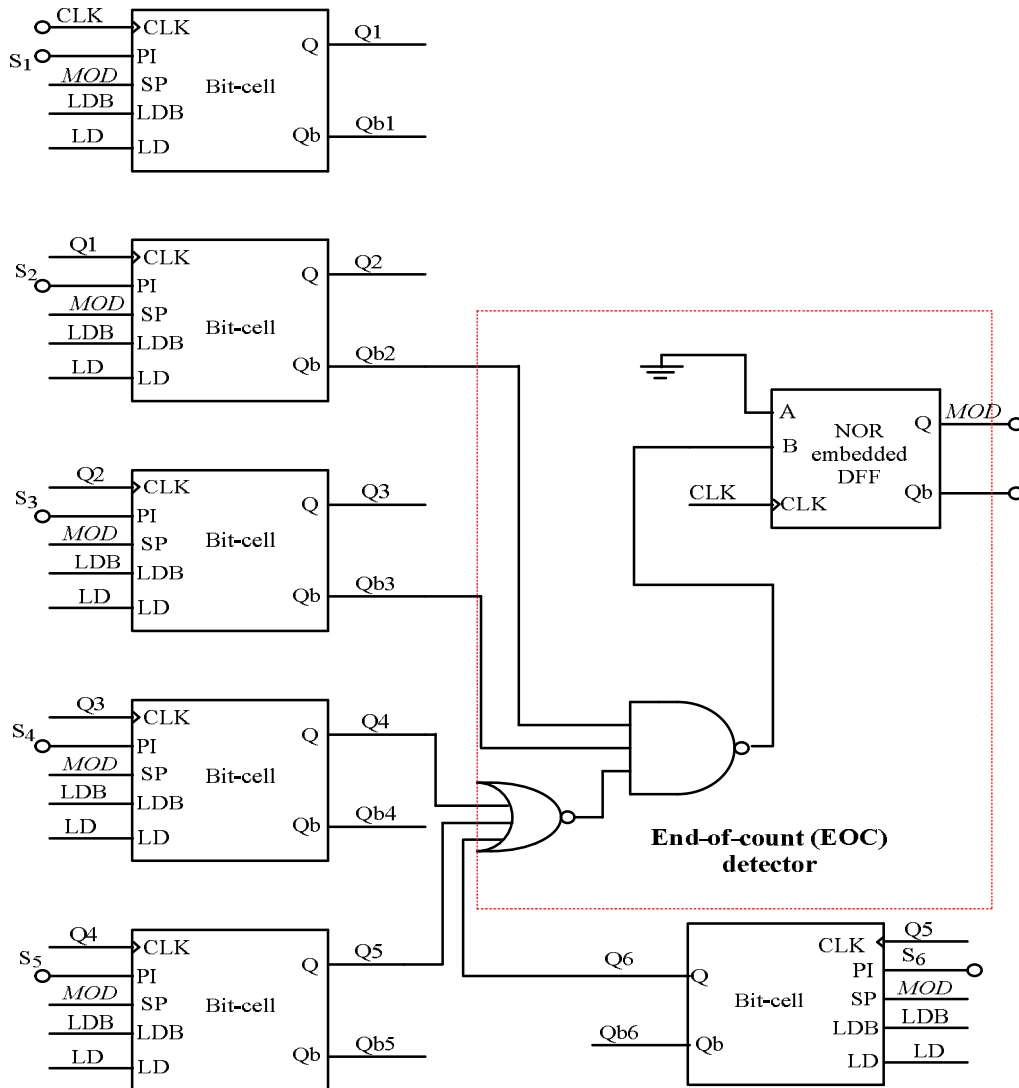


Fig. 4.19 A 6-bit Swallow S-counter with EOC logic circuit

The 6 bit swallow S-counter used in the fully programmable divider is shown in Fig. 4.19 which is similar to the S-counter shown in Fig.4.7 except an additional reloadable DFF. Here the state $Q_6Q_5Q_4Q_3Q_2=$ ”000000” is detected by the EOC logic

circuit. The S-counter in this programmable divider can be programmed from 0-47 in steps of 1 for a fixed value of the P-counter.

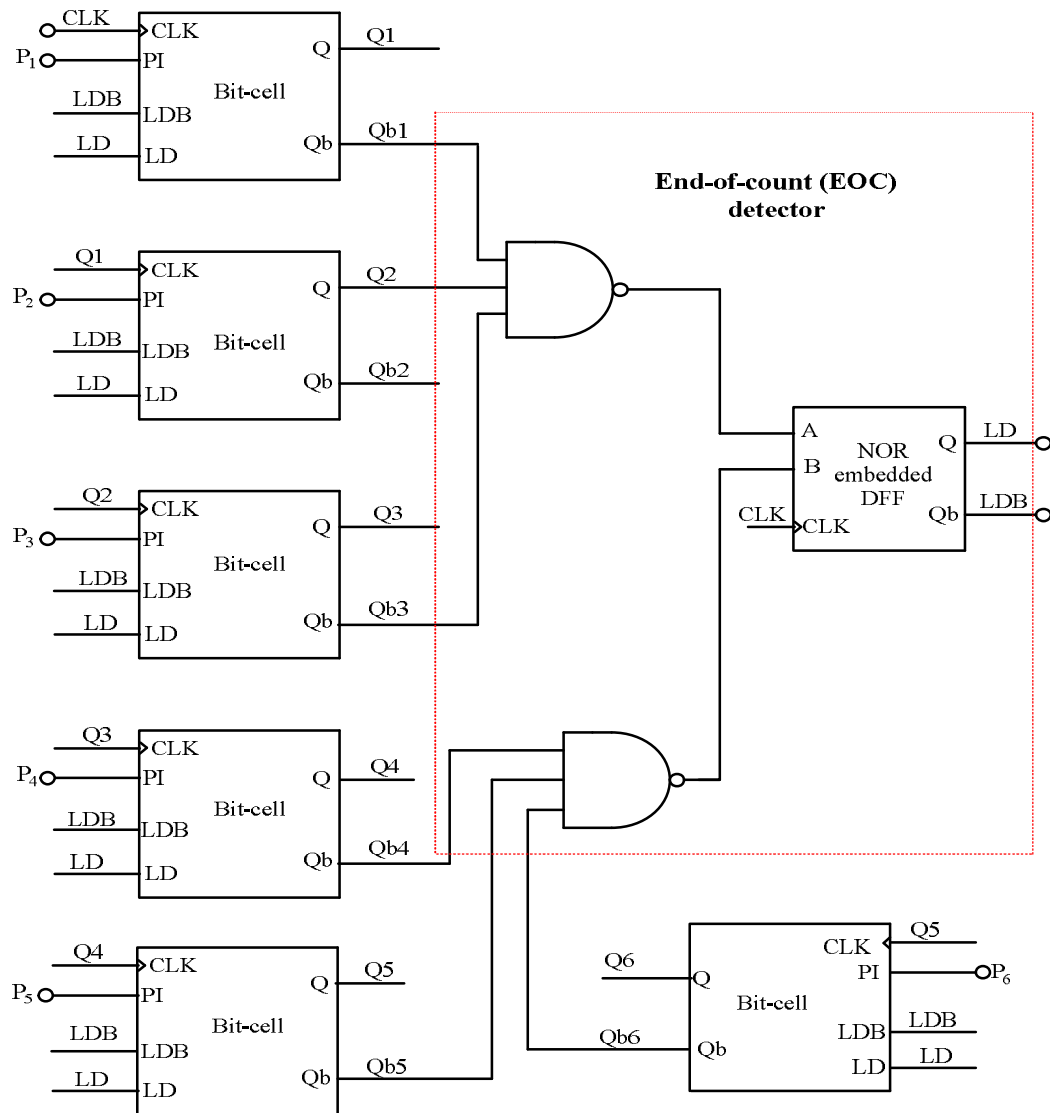


Fig. 4.20 A 6-bit Programmable P-counter with EOC logic circuit

The 6-bit programmable P-counter used in the design-II programmable divider is shown in Fig.4.20 which is similar to the P-counter shown in Fig.4.2 with a reduced number of reloadable DFFs. The EOC logic circuit is modified according to the design of the P-counter to detect the state $Q_6Q_5Q_4Q_3Q_2Q_1 = "000010"$. Here, bit P_6 and P_5 are always at logic '1' and bit P_4 at logic '0' to have a programmable values of 51

and 52. By choosing a fixed value of 51 and 52, the swallow S-counter is programmed in steps of one-bit to provide a division ratio from 2400 to 2484 with 1 MHz resolution.

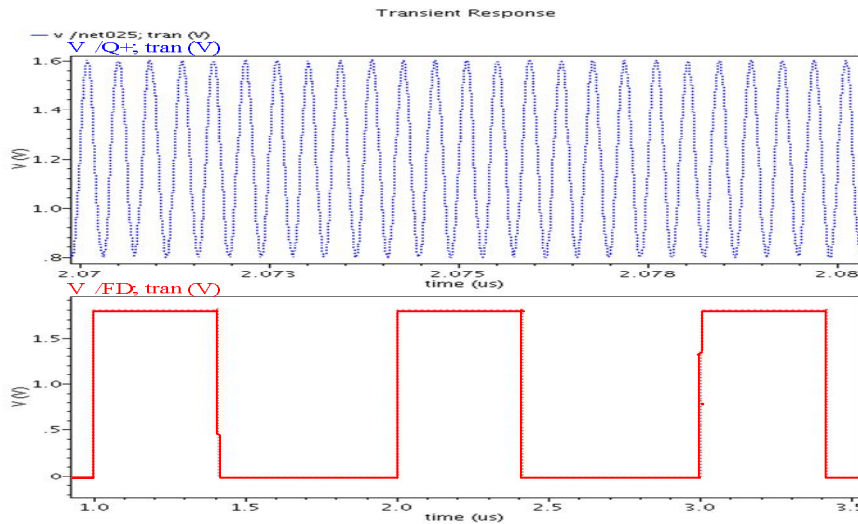


Fig. 4.21 Post layout results of the fully programmable divider with 2400 division ratio

4.6 Simulation and Measured results of the programmable divider: Design-II

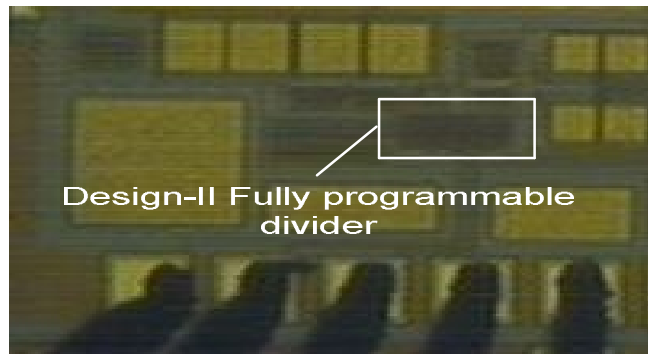


Fig. 4.22 Die photograph of the fully programmable divider: Design-II

The Design-II fully programmable divider at 2.4 GHz consumes a power of 0.6 mW.

Fig. 4.21 shows the post layout results of the fully programmable divider at 2.4 GHz with 1 MHz output signal of the divider having nearly 45% duty cycle. Fig.4.22 shows the die photograph of the fabricated Design-II fully programmable divider in

Global foundries (GF) RFCMOS 0.18 μ m technology. The divider consumes a power of 0.62 mW at 1.8V power supply and Fig.4.23 shows the measured 1 MHz output of the Design-II fully programmable divider.

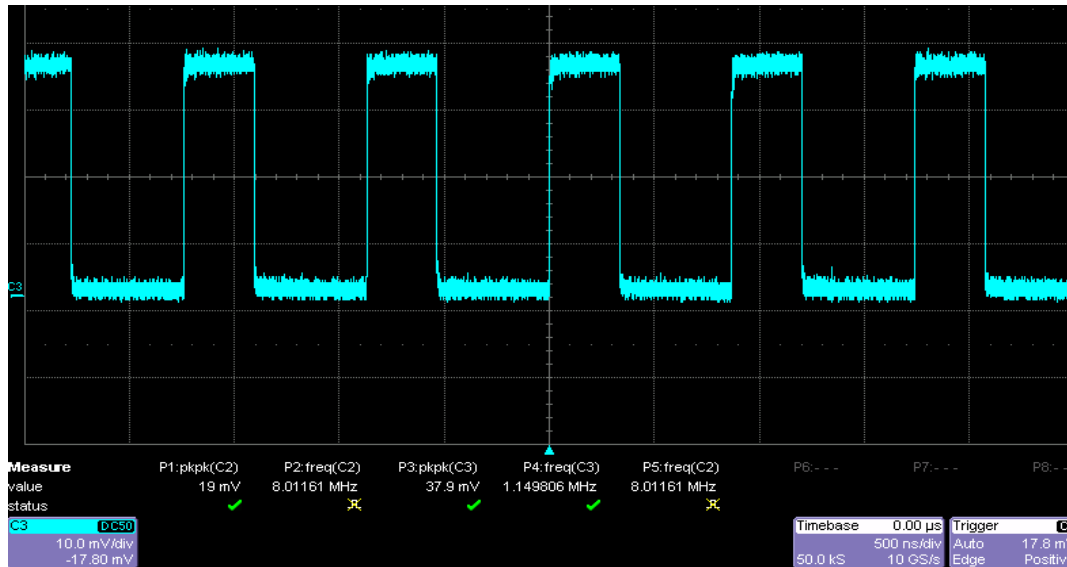


Fig. 4.23 Measured 1MHz output of the fully programmable divider: Design-II

4.7. Summary

In this chapter, detailed designs of the fully programmable divider with 1 MHz resolution are presented along with the detailed design of the programmable P-counter and swallow S-counter. A 47/48 TSPC dual modulus prescaler is proposed which improves the output signal duty cycle of the fully programmable divider. An improved reloadable TSPC DFF for the S-counter is introduced which reduces the switching power of the counter during the idle state when the P-counter is still active. The implemented fully programmable divider consumes a power of 0.62mW at 1.8 V power supply.

CHAPTER 5

LOW POWER MULTI-BAND FLEXIBLE DIVIDER

5.1. Introduction

Intensive efforts have been made to develop the high-performance WLAN chipsets using the low-cost CMOS process. The frequency synthesizer designed for WLAN transceivers reported in [3] consumes a power in the range of several hundred mW and uses off-chip components, which is not suitable for monolithic applications. Low power consumption is the key performance which helps to increase the battery life and to reduce the operating temperature. In particular, the power reduction in the first stage of the divider is necessary in realizing a low power frequency synthesizer.

The best published frequency synthesizer at 5 GHz consumes 9.7 mW at 1V power supply where its complete divider consumes power around 6 mW [75] and the first stage divider is implemented using the current-mode logic (CML) [56] circuit, which allows higher operating frequencies but uses more power. The TSPC [59] and E-TSPC [62] dividers described in the Chapter 3 use less power but has a lower operating frequency than CML dividers. However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs for applications below 5 GHz [40], [70].

The frequency synthesizer reported in [54] uses an E-TSPC prescaler as the

first stage divider, but the divider consumes around 6.25 mW. Most of the IEEE 802.11a/b/g frequency synthesizers employ CML dividers as their first stage [75], [76],[77] while dynamic latches have not yet been adopted for multi-band synthesizers. In this Chapter, we present the design of a proposed wide-band 2/3 prescaler, a multi-modulus 32/33/47/48 prescaler and a multi-band flexible divider.

5.2. E-TSPC 2/3 Prescaler

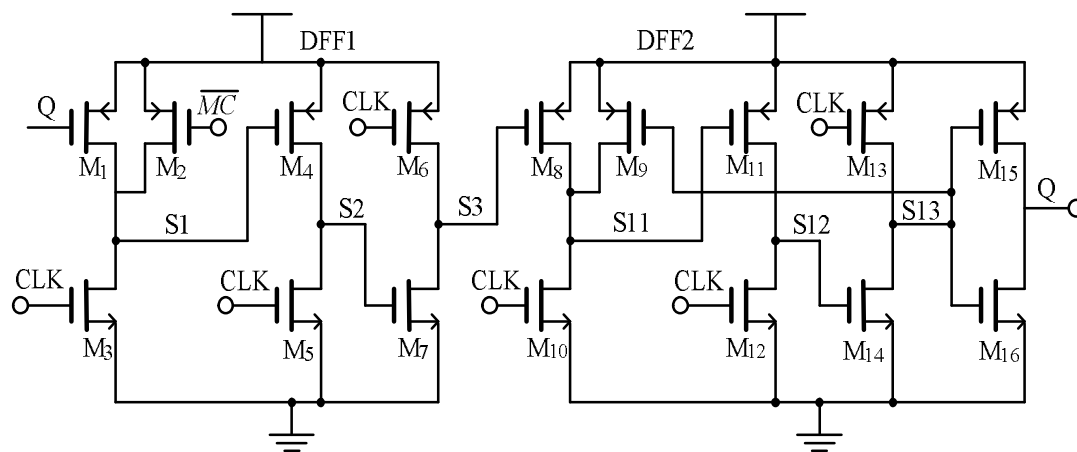


Fig. 5.1 E-TSPC 2/3 prescaler in [69]

The TSPC 2/3 prescaler [73] described in Chapter 3 consumes very low power and has the maximum operating frequency of 5 GHz. However, its operating frequency drops to 4.5 GHz when it is used in the design of 32/33 or 47/48 prescaler. The E-TSPC 2/3 prescaler reported in [54] has a maximum operating of 2.8 GHz at 2.5 V power supply in CMOS 0.25 μm technology. The E-TSPC 2/3 and 8/9 prescaler reported in [69] which is improved version of [54] has a maximum operating frequency of 4.5 GHz at 1.8-V power supply in CMOS 0.18 μm technology. However,

our re-simulation with optimized transistors in CMOS RF 0.18um technology shows that its operation can be extended up to 7.5 GHz. The 2/3 prescaler in [69] consists of two DFFs and two NAND gates embedded in the flip-flops as shown in Fig.5.1. The total load capacitance of the 2/3 prescaler is given by (5.1), which is calculated by using the methods described in [63], [64].

$$C_{S13} = C_{dbM_{13}} + 2C_{gdM_{13}} + C_{dbM_{14}} + 2C_{gdM_{14}} + C_{gM_1} + C_{gM_{15}} + C_{gM_{16}} \quad (5.1)$$

The control logic signal \overline{MC} changes the operation between divide-by-2 and divide-by-3 modes. If $\overline{MC} = '1'$, the 2/3 prescaler operates in the divide-by-3 mode where the two DFFs actively participate in the operation. If $\overline{MC} = '0'$, the 2/3 prescaler operates in the divide-by-2 mode, where PMOS transistor M_2 is always turned-on suppressing the switching activities in DFF1 such that the nodes S1, S2 and S3 remain at logic '1', '0' and '1' respectively. Thus the switching power is saved in DFF1 during the divide-by-2 operation. However, there always exists very high short-circuit power in the first stage of the DFF1 and improper device sizing can still result in switching activities in the DFF1 during the divide-by-2 operation.

5.2.1. Short-Circuit Power Analysis: Divide-by-2 mode

During the divide-by-2 operation, \overline{MC} is '0', the PMOS transistor M_2 is turned-on for the entire duration of the divide-by-2 operation and M_3 is *ON* for half of the input clock period during which there exists a direct path between the supply and ground

resulting in high short-circuit power as shown in Fig.5.2. The shaded region indicates the short circuit period. A further increase in short-circuit power in the first stage occurs when M_1 is also turned-on. Let I_{sc1} be the short-circuit current that flows from the supply to ground when M_2 and M_3 are turned-on and I_{sc2} , I_{sc3} be the short-circuit currents due to the finite rise time (t_r) and fall time (t_f) of the clock signal. The total short-circuit power in the first stage is estimated by the methods in [63], [64], which is given by

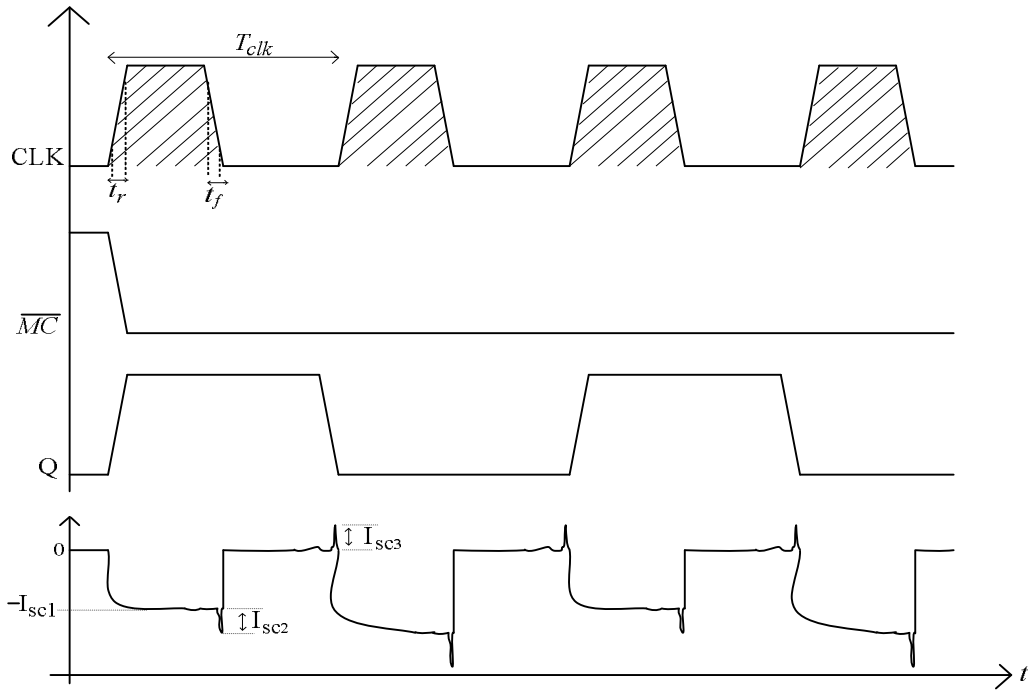


Fig. 5.2 Short circuit power analysis of prescaler in [69]

$$P_{sc1} = \frac{V_{dd}}{T_{clk}} \left(\int_0^{t_r} I_{sc2} + \int_{t_r}^{\frac{T_{clk}-t_f}{2}} I_{sc1} + \int_{\frac{T_{clk}}{2}}^{\frac{T_{clk}-t_f}{2}} I_{sc3} \right) \quad (5.2)$$

where T_{clk} is the input clock signal period. Assuming that the rise-time and fall-time are equal and $I_{sc1}=I_{sc2}$, (5.2) can be rewritten as

$$P_{sc1} = \frac{2V_{dd}}{T_{clk}} \left(\int_0^{t_r} I_{sc2} \right) + \frac{V_{dd}}{T_{clk}} \int_{t_r}^{\frac{T_{clk}}{2}-t_f} I_{sc1} \quad (5.3)$$

Since nodes S1, S2 of DFF1 respectively remain at logic '1' and '0' during the divide-by-2 mode, M₄ and M₇ are always *OFF*, so the short-circuit power in second and third stages of DFF1 exists only for short period of rise-time and fall-time which is negligible. From (5.3), it is found that the short circuit power in DFF1 occurs mainly in the first stage during every half period of the input clock cycle. Hence, a reduction of the short-circuit power in the E-TSPC circuit is necessary.

5.2.2. Switching Power Analysis: Divide-by-2 mode

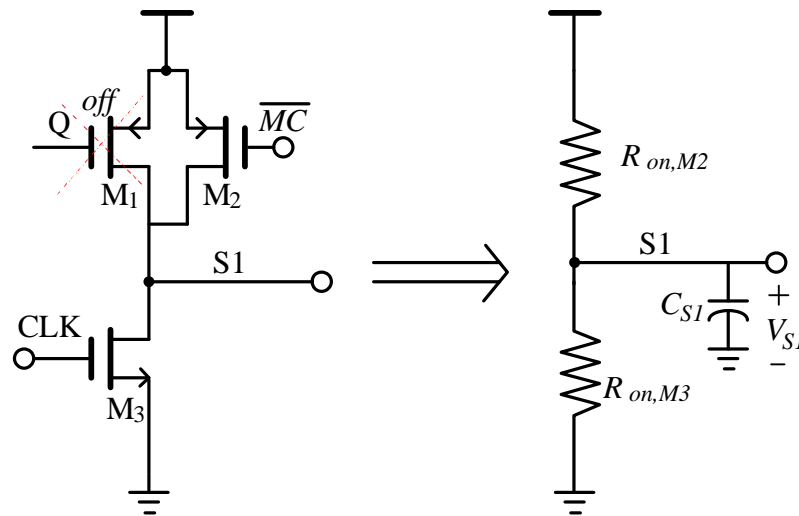


Fig. 5.3 Case-I: schematic of first stage DFF1 in [69]

When \overline{MC} switches from '1' to '0', M₂ turns-on and irrespective of the logic value at the input of M₁, nodes S1, S2, S3 switch to logic '1', '0', '1' respectively and remain unchanged during the entire divide-by-2 operation, thus saving the switching power consumption of DFF1. However, this is not always true as node S1 may not settle to

logic '1' and its value depends on the sizing of the transistors M_1 , M_2 and M_3 . Due to the continuous charging and discharging at node S1, there exists switching power in the first stage. Let us examine the following cases where there exists switching power in DFF1 during the divide-by-2 operation.

Case-I: M_2, M_3 ON and M_1 OFF

Fig.5.3. shows the first stage of DFF1 where M_2, M_3 are turned-on for half of the input clock period and M_1 turned-off completely. Since M_2 and M_3 have finite ON resistance, the node voltage V_{S1} is decided by the sizing of transistors M_2 and M_3 as given by (5.4), (5.5). The load capacitance C_{S1} at node S1 is given by (5.6).

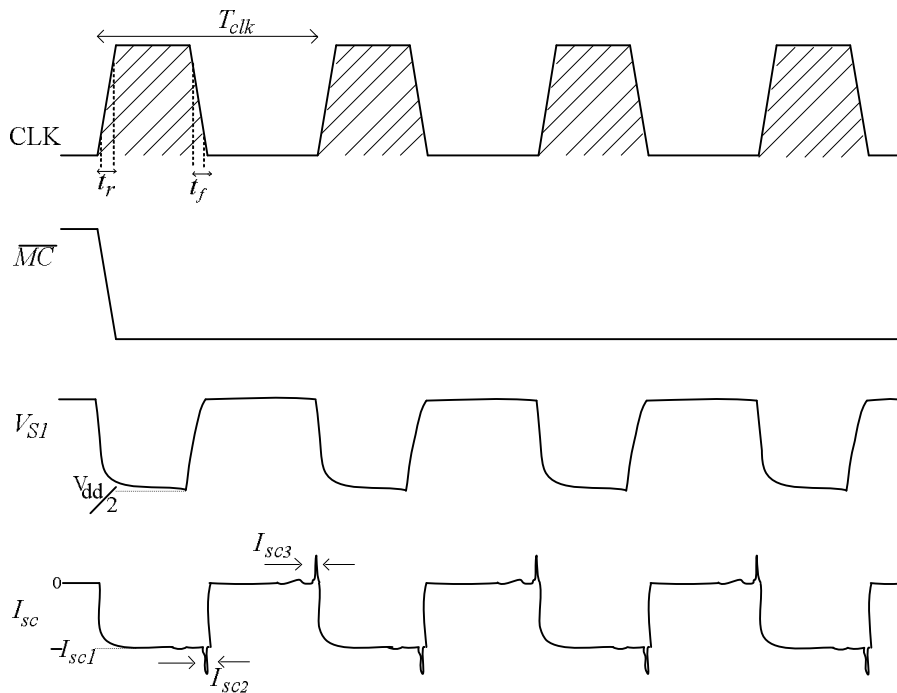


Fig. 5.4 Case-I: switching power analysis of first stage of DFF1 in [69]

$$V_{S1} = \frac{R_{ON,M3}}{R_{ON,M3} + R_{ON,M2}} \times V_{dd} \tag{5.4}$$

$$V_{S1} = \frac{W_{M2}\mu_p}{W_{M2}\mu_p + W_{M3}\mu_n} \times V_{dd} \quad (5.5)$$

$$C_{S1} = C_{dbM2} + C_{dbM3} + 2(C_{gdM2} + C_{gdM3}) + C_g \quad (5.6)$$

where W_{M2} , W_{M3} are the widths of the transistors M_2 , M_3 and C_g is the gate capacitance of the next stage transistor connected to node S1. From (5.5), if $W_{M2}\mu_p = W_{M3}\mu_n$, the voltage at S1 continuously charges and discharges between V_{dd} and $V_{dd}/2$ as shown in Fig.5.4 and thus causes switching power in the first stage.

There is also a high possibility that M_2 turns-on causing the short-circuit power in the second stage of DFF1 for a period equal to half of the clock period and also a considerable amount of switching power. The worst case would be when $W_{M2}\mu_p < W_{M3}\mu_n$ where node S1 settles to a voltage lesser than $V_{dd}/2$ turning-on M_4 completely and causes continuous switching activities and high short-circuit power in the second stage of DFF1.

Case-II: M_2 , M_3 and M_1 ON

Fig.5.5 shows the first stage of DFF1 when M_2 is always *ON*, M_3 turns-on for every half of the input clock period and M_1 turns-*ON* for half clock period for every 2 clock cycles. Since M_1 , M_2 and M_3 have finite *ON* resistances and the widths of M_1 and M_2 are the same (assuming $R_{ON,M2} = R_{ON,M1}$), the voltage at node S1 is given by (5.7), (5.8). The load capacitance C_{S1} at node S1 is given by (5.9).

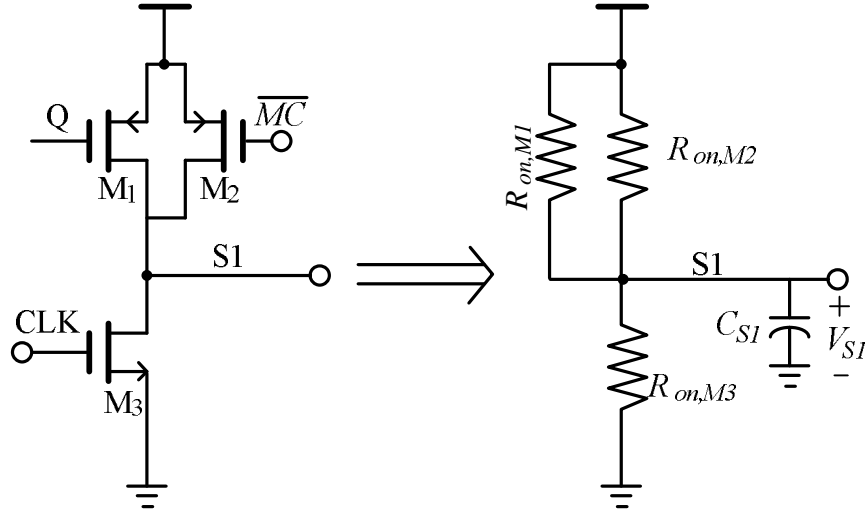


Fig. 5.5 Case-II: schematic of first stage DFF1 in [69]

$$V_{S1} = \frac{R_{ON,M3}}{R_{ON,M3} + \frac{R_{ON,M2}}{2}} \times V_{dd} \quad (5.7)$$

$$V_{S1} = \frac{W_{M2}\mu_p}{W_{M2}\mu_p + 2W_{M3}\mu_n} \times V_{dd} \quad (5.8)$$

$$C_{S1} = C_{dbM2} + C_{dbM3} + C_{dbM1} + 2(C_{gdM1} + C_{gdM2} + C_{gdM3}) + C_g \quad (5.9)$$

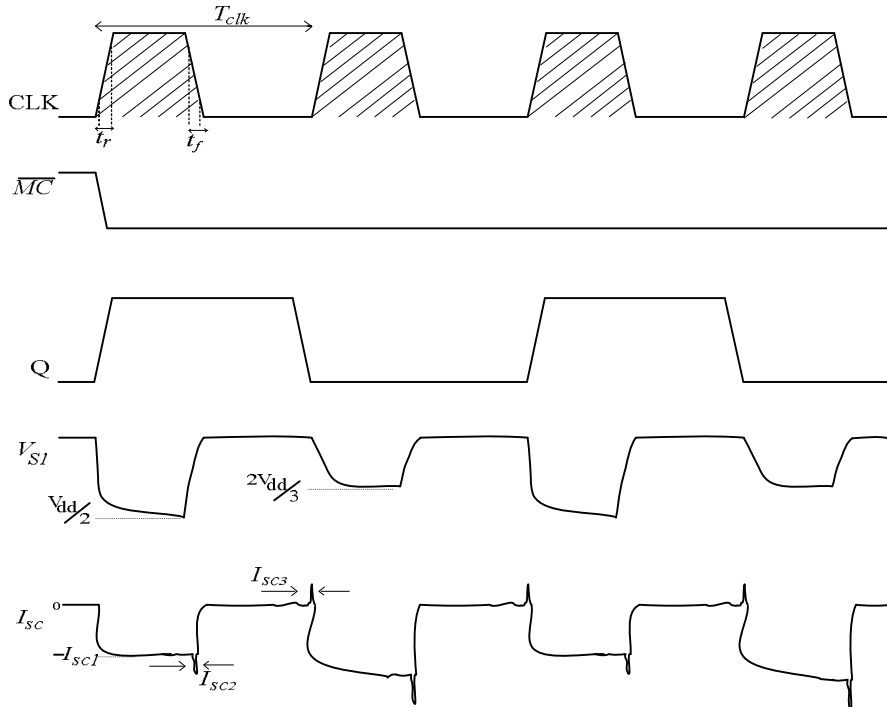


Fig. 5.6 Case-II: switching power analysis of first stage of DFF1 in [69]

Fig.5.6 shows that if the design uses ratio logic, node S1 discharges to a voltage of $2/3V_{dd}$ when both M_1 and M_3 are ON and to a voltage of $V_{dd}/2$, when M_1 is OFF and M_3 is ON. Since node S1 continuously charges and discharges between V_{dd} , $V_{dd}/2$ and $2/3V_{dd}$, there exists switching power in the first and second stages of DFF1 during the divide-by-2 operation. Finally, the total power consumption of DFF1 during the divide-by-2 operation is given as follows:

If $W_{M2} \mu_p = W_{M3} \mu_n$, the total power consumption of DFF1 is the sum of switching and short circuit power of the first and second stages (assuming short circuit power due to rise time and fall time of all stages are same), which is given by

$$P_{DFF1} = \frac{6 \times V_{dd}}{T_{clk}} \left(\int_0^{t_r} I_{sc} \right) + \int_{t_{r1}}^{\frac{T_{clk}}{2} - t_{f1}} I_{sc1} + \int_{t_{r2}}^{\frac{T_{clk}}{2} - t_{f2}} I_{sc2} \Big) + f_{clk} V_{dd}^2 (C_{S1} + C_{S2}) \quad (5.10)$$

where C_{S1}, C_{S2} are load capacitances at nodes S1 and S2 and I_{sc1}, I_{sc2} are the short circuit currents through the first and second stages for half of the clock period and I_{sc} is the short-circuit current in all the 3 stages due to finite rise and fall times which are assumed to be same.

If $W_{M2} \mu_p > W_{M3} \mu_n$, the voltage at node S1 discharges from V_{dd} to a value greater than $V_{dd}/2$, thus turning-off M_4 completely and eliminates the switching and short circuit power in the second stage of DFF1. In this case, the total power consumption in DFF1 is given by

$$P_{DFF1} = \frac{6 \times V_{dd}}{T_{clk}} \int_0^{t_r} I_{sc} dt + \frac{T_{clk} - t_{f1}}{2} \int_{t_{r1}} I_{sc1} dt + f_{clk} V_{dd}^2 C_{s1} \quad (5.11)$$

From the above analysis, it is found that the switching power is not zero in DFF1 during the divide-by-2 operation and there also exists the high short-circuit power in the first two stages of DFF1 for every half of the input clock period. To overcome all these problems, a new low power, wide band 2/3 prescaler is proposed based on the dynamic logic flip-flop which is discussed in the next section.

5.3. Wide-band E-TSPC 2/3 Prescaler

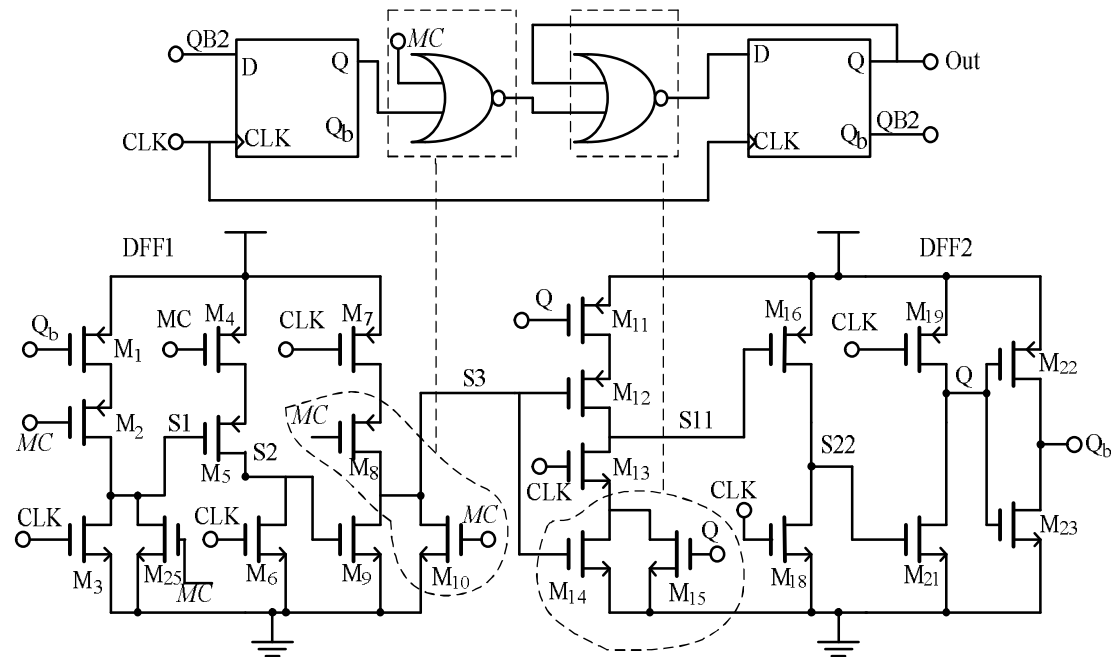


Fig. 5.7 Proposed wide band 2/3 prescaler

The Proposed wide band 2/3 prescaler consists of two D flip-flops and two NOR gates embedded in the flip-flops as shown in Fig.5.7. The first NOR gate is embedded in the last stage of DFF1 and second NOR gate is embedded in the first stage of DFF2 similar to the Design-I TSPC 2/3 prescaler. Here, additional transistors M_{2a} , M_{25} , M_8

and M_4 are added in DFF1 to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC . The total load capacitance of the proposed prescaler is given by

$$C_{L_wideband} = C_{dbM19} + C_{dbM21} + 2(C_{gdM19} + C_{gdM21}) + C_{gM1} \quad (5.12)$$

By embedding the two NOR gates in to the DFF's, the number of stages has been reduced to 7, which consequently reduces the propagation delay from the input node to output node. However, the RC delay in the each stage of the prescaler reported in [54] is lesser than that of the proposed wide-band prescaler as the proposed prescaler is combination of both TSPC and E-TSPC logic. Since the E-TSPC prescaler suffers from the problem of short circuit power, in the proposed wide-band prescaler extra transistors are added in the critical stage to reduce the short circuit power at the cost of speed. By reducing the width of the transistors, the speed of operation is further optimized. The detailed operation of power reduction is given in the next section.

5.3.1. Analysis of divide-by-2 operation

When logic signal MC switches from '0' to '1', the proposed prescaler switches to divide-by-2 mode. At the rising edge of first clock cycle, nodes S1, S2 and S3 switch to logic '0' and remain at same level for the entire divide-by-2 operation, thus removing the switching power contribution of the DFF1. Fig.5.8 shows the first stage

of DFF1 during the divide-by-2 operation of the proposed prescaler. During this

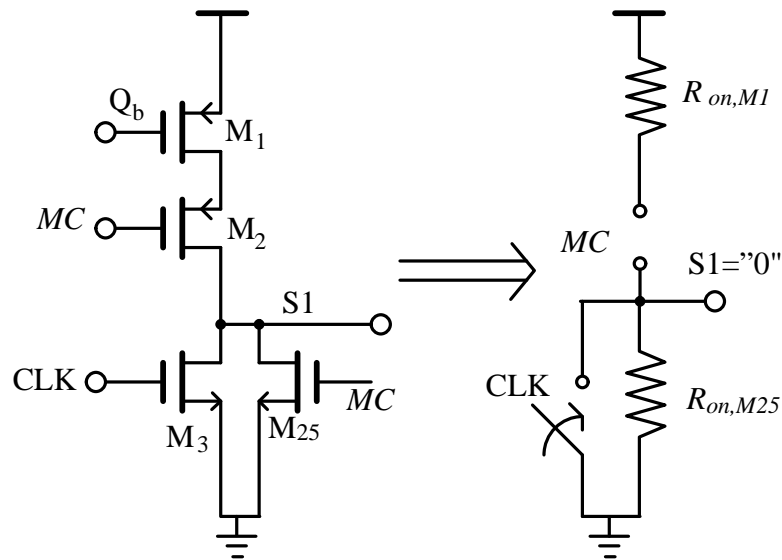


Fig. 5.8 First stage of the proposed wide band 2/3 prescaler

operation, transistors M_{2a} , M_5 and M_8 turn-off completely at the first rising edge of the clock signal. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power contributed by DFF1 is almost negligible. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus the proposed prescaler has benefit of saving more than 50% of the power compared to the prescaler in [69].

5.4. Simulation and Measured Results of Wide-band 2/3 Prescaler

A complete analysis and comparison of the performance of the proposed wide-band 2/3 prescaler and E-TSPC based prescaler in [69] is carried out on the ground that the prescaler in [69] has the best performance in literature that is designed using

single-phase clock flip-flops. The simulations are performed using Cadence SPECTRE RF for a 0.18 μm CMOS process. The simulation results shows that the proposed 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 mW, 1.73 mW during the divide-by-2 and divide-by-3 modes respectively. The 2/3 prescaler in [69] has maximum operating frequency of 7.5 GHz with a power consumption of 1.67 mW, 1.77 mW during the divide-by-2 and divide-by-3 modes respectively. Fig.5.9 shows the post-layout power consumption against different input frequencies for the proposed wide-band 2/3 prescaler and the E-TSPC 2/3 prescaler reported in [69].

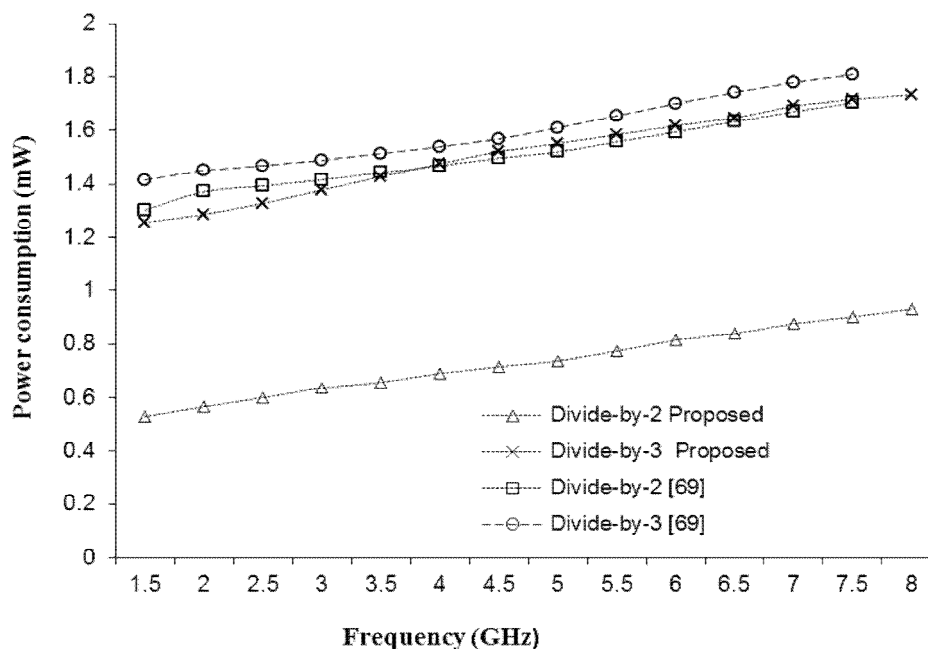


Fig. 5.9 Post-layout results: power consumption of wide band prescaler and prescaler in [69]

For silicon verification, the proposed 2/3 wide-band prescaler and the 2/3

prescaler in [69] are fabricated using the Global Foundries 1P6M 0.18 μm CMOS process. The measurement results shows that the proposed wide-band $2/3$ prescaler has a maximum operating frequency of 6.5 GHz slightly higher than that of the $2/3$ prescaler in [69], whose maximum operating frequency is measured at 6 GHz. The maximum frequency of operation measured is lower than the simulated result due to the large parasitics and the buffer at the output stage. Fig.5.10 shows the die photograph of both the wide-band $2/3$ prescaler and E-TSPC $2/3$ prescaler in [69].

Fig.5.11 shows the measured output waveform of the proposed wide-band $2/3$ prescaler at an input frequency of 6.5 GHz in divide-by-2 and divide-by-3 modes respectively. Fig.5.12 shows the measured power consumption of the proposed prescaler and the prescaler in [69] at different input frequencies. Table.5.1 compares the performance of the proposed $2/3$ prescaler and the $2/3$ prescaler reported in [16] at 6 GHz.

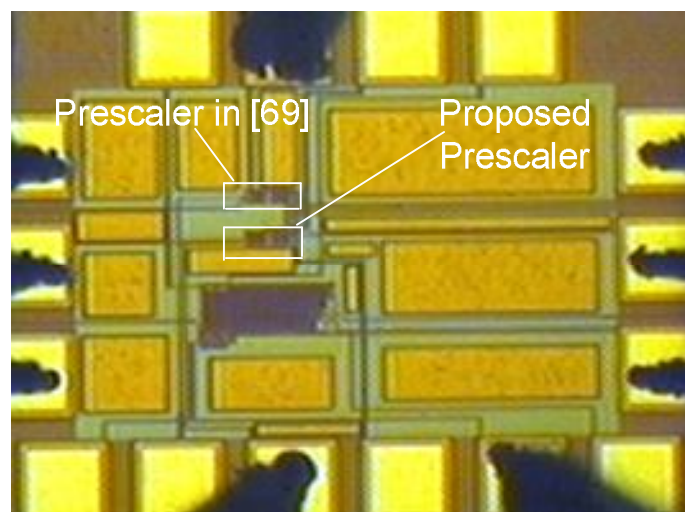


Fig. 5.10 Die photograph of wide band $2/3$ prescaler and E-TSPC $2/3$ prescaler in [69]

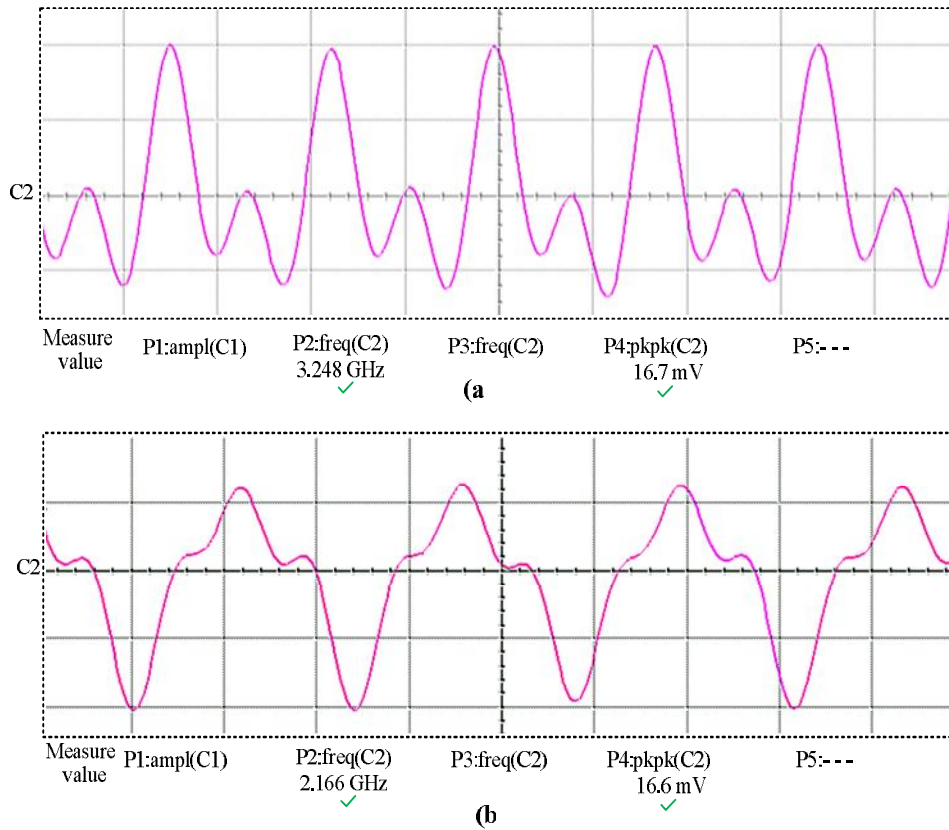


Fig. 5.11 Measured waveforms a) divide-by-2 mode b) divide-by-3 mode

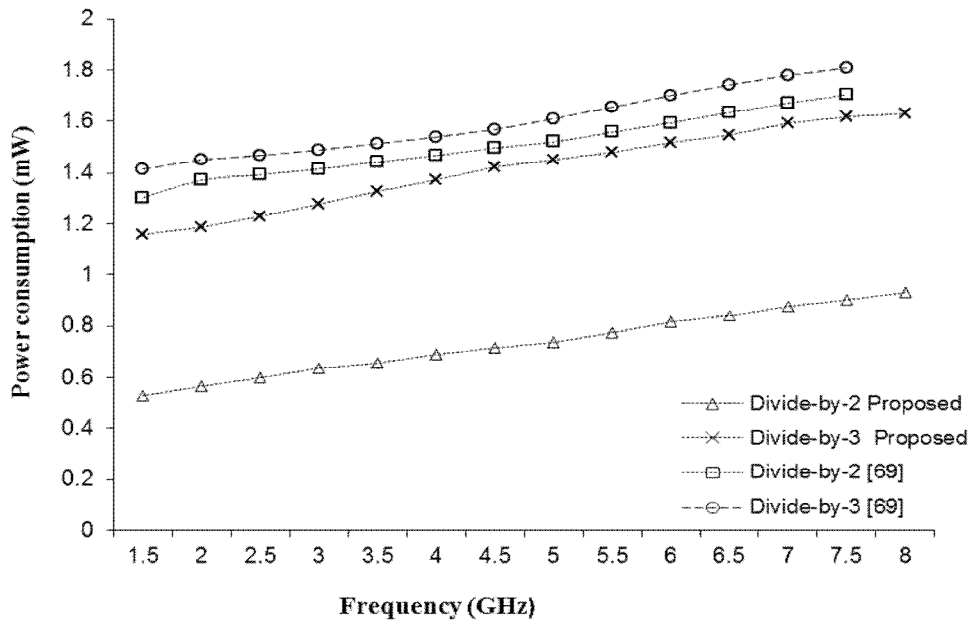


Fig. 5.12 Measured results: power consumption of wide band prescaler and prescaler in [69]

Table 5.1 Performance of different prescalers at 6 GHz

Design Parameters	Prescaler in [69]	Proposed prescaler
Process	0.18 um	0.18um
supply voltage	1.8 V	1.8 V
Max.Frequency (GHz) (Sim/Measured)	7.5 / 6	8 / 6.5
Power(mW) (sim/measured)	1.63 / 2.2	0.82 / 0.97
Divide-by-2 mode		
Power(mW) (sim/measured)	1.85 / 2.62	1.61 / 1.78
Divide-by-3 mode		

5.5. Multi-Band Flexible Divider

Most of the CMOS frequency synthesizers reported in the literature use CML logic dividers as first stage dividers [76], [77], since the single-phase clock dividers are limited to below 5 GHz applications. With the proposed wide-band 2/3 prescaler which operates up to frequency of 6.5 GHz on silicon, it is possible to implement a fully programmable divider for 2.4 GHz ISM band and 5 GHz WLAN band with low power single-phase clock dividers. Fig.5.13 shows the multi-band fully programmable divider for the 2.4 GHz ISM band and the 5 GHz WLAN band with a flexible resolution. The multi-band divider consists of the proposed multi-modulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter.

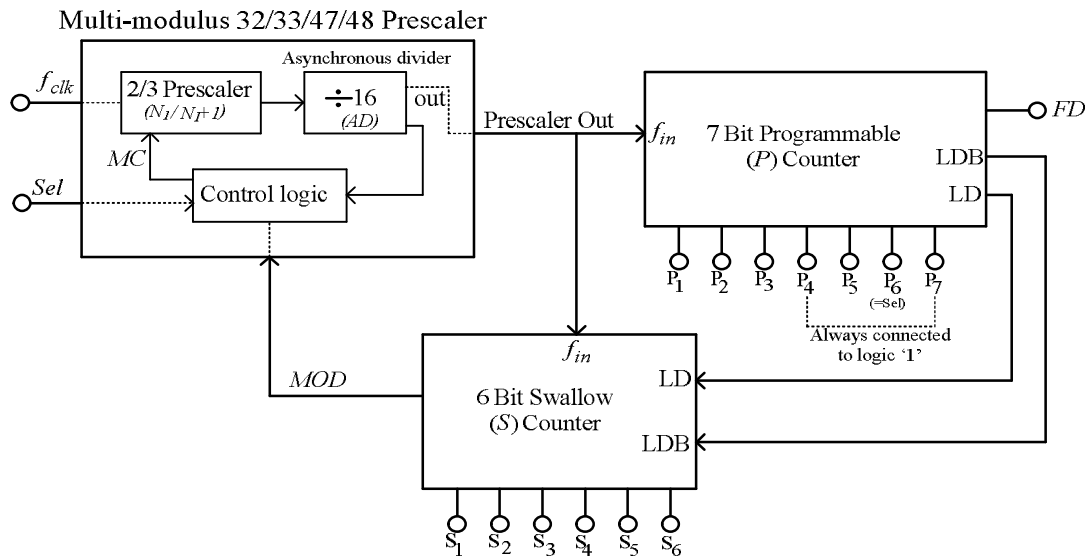


Fig. 5.13 Multi-band fully programmable divider with flexible resolution

5.5.1. Multi-Modulus 32/33/47/48 prescaler

The proposed wide-band multi-modulus 32/33/47/48 prescaler which can divide the input frequency by 32, 33, 47 and 48 respectively is shown in Fig.5.14. The multi-modulus prescaler is a critical block in the design of multi-band divider since the first stage prescaler should be able to operate up to 6 GHz. The multi-modulus prescaler is similar to the 32/33 [53], [70] and 47/48 prescaler, but with an additional multiplexer to control the switching between 32/33 and 47/48 modes. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and design complexity. The multi-modulus prescaler consist of the proposed wide-band 2/3 prescaler, four asynchronous TSPC [59] divide-by-2 circuits, and combinational logic circuits to achieve multiple division ratios. Besides the usual *MOD* signal for controlling the division ratios ($N/N+1$), the additional control signal *Sel* is used to switch the

prescaler between 32/33 and 47/48 modes.

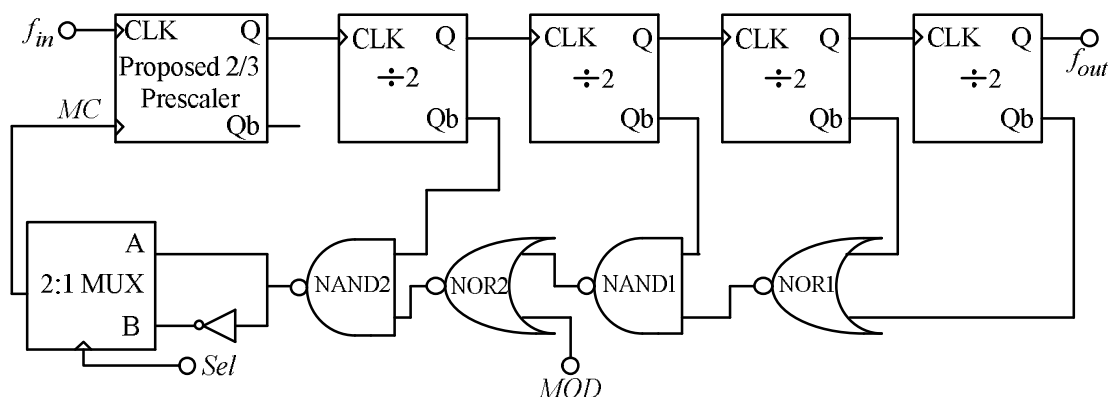


Fig. 5.14 Proposed Multi-modulus 32/33/47/48 prescaler

Case-I: $Sel='0'$

When $Sel='0'$, the output from the NAND2 gate is selected by the 2:1 MUX and transferred to the input of 2/3 prescaler and the multi-modulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD . If $MOD='1'$, the prescaler acts as divide-by-32 as discussed in Chapter 3. If we denote the wide-band 2/3 prescaler as $M/M+1$ and the four asynchronous dividers whose division ratio equal to 16 by 'AD', the division ratio in this mode ($MOD='1'$, $Sel='0'$) is given by

$$f_{32} = (AD - \overline{MOD}) \times M + \overline{MOD} \times (M + 1) = (16 - 0) \times 2 + 0 \times (2 + 1) = 32 \quad (5.13)$$

If $MOD='0'$, the prescaler acts as divide-by-33 as discussed in Chapter 3. The division ratio in this mode ($MOD='0'$, $Sel='0'$) is given by

$$f_{33} = (AD - \overline{MOD}) \times M + \overline{MOD} \times (M + 1) = (16 - 1) \times 2 + 1 \times (2 + 1) = 33 \quad (5.14)$$

Case-III: Sel='1'

When $Sel='1'$, the inverted output from the NAND2 gate is selected by the 2:1 MUX and transferred to the input of 2/3 prescaler and the multi-modulus prescaler operates as 47/48 prescaler, where the division ratio is controlled by the logic signal MOD . Here, when $MC='0'$, the wide-band 2/3 prescaler operates in the divide-by-2 mode and when $MC='1'$, the 2/3 prescaler operates in the divide-by-3 mode as shown in Fig.4.14 of chapter 4. If $MOD='1'$, the prescaler acts as divide-by-48 as discussed in section 4.6.1. If we denote the wide-band 2/3 prescaler as $M/M+1$ and the four asynchronous dividers whose division ratio equal to 16 by ' AD ', the division ratio in this mode ($MOD='1'$, $Sel='1'$) is given by

$$f_{48} = (AD - \overline{MOD}) \times (M + 1) + \overline{MOD} \times M = (16 - 0) \times (2 + 1) + 0 \times 2 = 48 \quad (5.15)$$

If $MOD='0'$, the prescaler acts as divide-by-47 as discussed in section 4.6.2.

The division ratio in this mode ($MOD='0'$, $Sel='1'$) is given by

$$f_{47} = (AD - \overline{MOD}) \times (M + 1) + \overline{MOD} \times M = (16 - 1) \times (2 + 1) + 1 \times 2 = 47 \quad (5.16)$$

5.5.2. 6-bit Swallow S-counter

The proposed multi-band divider uses a 6-bit swallow S-counter as shown in Fig.4.19.

The S-counter is designed with 6 reloadable DFFs [20] and an EOC circuit [66], [71]

which is similar to the S-counter discussed in Section 4.7.1 of Chapter 4. However,

the programmability of the counter is different as compared to the S-counter described

in the previous chapter. Here the programmable inputs S_1 - S_6 are used to program from 0-31 or 0-47 depending on the frequency of interest.

For the 2.4 GHz ISM frequency band, $Sel='0'$ and the multi-modulus prescaler operates in divide-by-32 or divide-by-33 depending on the logic signal MOD where the S-counter is programmed from 0-31 in order to satisfy the condition ($S < N$). For the 5 GHz WLAN frequency band, $Sel='1'$ and the multi-modulus prescaler operates in divide-by-47 or divide-by-48 depending on the logic signal MOD where the S-counter is programmed from 0-47 in order to satisfy the condition ($S < N$). Here, the S-counter can be programmed in steps of $1-K$, where K is the channel spacing for integer- N frequency synthesizers with 1 MHz reference signal.

5.5.3. 7-bit Programmable P-counter

The proposed multi-band divider uses a 7-bit programmable P-counter as shown in Fig.4.2. The P-counter is designed with 7 reloadable DFFs [72] and EOC circuit which is similar to the P-counter discussed in Section 4.3 of Chapter 4. However, the programmability of the counter is different as compared to the P-counter described in the previous chapter. The programmable inputs P_1 - P_7 are used to program from 75 to 77 or from 105 to 122 depending on the frequency of interest. Here, bit P_7 is tied to the Sel signal of the multi-modulus prescaler and bits P_4 and P_7 are fixed to logic '1'.

If a fixed 32/33 ($N/N+1$) dual-modulus prescaler is used for the design of the

multi-band divider, a 7 bit P-counter is needed for low frequency band (2.4 GHz) while an 8 bit P-counter would be needed for the high frequency band (5-5.825 GHz) with a fixed 5 bit S-counter. Thus the multi-modulus 32/33/47/48 prescaler eases the design complexity of the P-counter.

Case-I: Sel='0' (2.4-2.484 GHz)

When $Sel='0'$, the multi-modulus prescaler acts as a 32/33 prescaler, the P-counter is programmable from 64 to 127 (bit P_7 of the P-counter always remain at logic '1'), and the S-counter is programmable from 0-31 to accommodate division ratios from 2048 to 4095 with finest resolution of 1 MHz. However, since we are interested in 2.4 GHz ISM band, bit P_6 of the P-counter always remain at logic '0', since it is tied to the logic signal Sel , allowing it to be programmable from 75 to 77. Bit S_6 of the S-counter is kept at logic '0' (to satisfy the condition $N>S$), allowing it to be programmable from 0 to 31 for the low frequency band of operation to accommodate division ratios between 2400 and 2484 with a resolution of 1 MHz for Blue-tooth [2], [5] and 5 MHz for Zigbee and IEEE 802.15.4 applications [10], [70] with a fixed reference frequency of 1 MHz.

Since the finest resolution and reference frequency is 1 MHz, different channel spacing can be achieved by programming S-counter in steps of '1'. For example, 5 MHz channel spacing is achieved by programming S-counter in steps of '5' keeping

the flexible divider resolution and reference frequency to 1 MHz. Table.5.2 shows the programmable values of the P-counter and S-counter of the multi-band divider. The frequency division ratio (FD) of the multi-band divider in this mode is given by

$$FD = (N + 1) \times S + N \times (P - S) = (N \times P) + S \quad (5.17)$$

Table 5.2 Programmable values of the programmable counters (2.4 GHz band)

Frequency division ratio	Sel	Prescaler (N/N+1)	Programmable counter (P)	Swallow counter (S)
2400-2431	0	N=32	P=75	S=0-31
2432-2463	0	N=32	P=76	S=0-31
2464-2484	0	N=32	P=77	S=0-20

Case-II: Sel='1' (5-5.825 GHz)

When $Sel='1'$, the multi-modulus prescaler acts as a 47/48 prescaler, the P-counter is programmable from 64 to 127 (bit P_7 of the P-counter always remain at logic '1'), and the S-counter is programmable from 0-47 to accommodate division ratios from 3024 to 6096 with the finest resolution of 1 MHz. However, since we are interested in 5-5.825 GHz band, bit P_6 of the P-counter always remain at logic '1', allowing it to be programmable from 105 to 122. The S-counter is programmable from 0 to 47 for the high frequency band of operation to accommodate division ratios between 5000 and 5825 with a resolution of 5MHz, 10 MHz or 20 MHz for IEEE 802.11a/b/g synthesizers [3], [54], [75].

Since the finest resolution and reference frequency is 1 MHz, different channel

spacing can be achieved by programming S-counter in steps of ‘1’, ‘5’, ‘10’ or ‘20’, and P-counter programmed from 105-122 in steps of ‘1’. Table.5.3 shows the programmable values of the P-counter and S-counter of the multi-band divider.

Table 5.3 Programmable values of the programmable counters (5 GHz band)

Frequency division ratio	Sel	Prescaler (N/N+1)	Programmable counter (P)	Swallow counter (S)
5150-5184	0	N=47	P=108	S=0-34
5185-5232	0	N=47	P=109	S=0-47
5233-5280	0	N=47	P=110	S=0-47
5281-5328	0	N=47	P=111	S=0-47
5329-5350	0	N=47	P=112	S=26-47
5725-5760	0	N=47	P=120	S=0-35
5761-5808	0	N=47	P=121	S=0-47
5809-5825	0	N=47	P=122	S=31-47

The frequency division ratio (FD) of the multi-band divider in this mode is given by

$$FD = N \times S + ((N + 1) \times (P - S)) = ((N + 1) \times P) - S \quad (5.18)$$

5.6. Simulation and Measurement Results

The simulations of the designs are performed using Cadence SPECTRE RF for a 0.18 μ m CMOS process at 1.8-V supply voltage. The proposed wide band multi-modulus prescaler has the maximum operating frequency of 7.2 GHz (post-layout simulation) with a power consumption of 1.52 mW, 1.60 mW, 2.1 mW and 2.13 mW during the divide-by-32, divide-by-33, divide-by-47 and divide-by-48 modes respectively. For silicon verification, the multi-band divider is fabricated using the Global Foundries

1P6M 0.18 μ m CMOS process and the die photograph is shown in Fig.5.15.

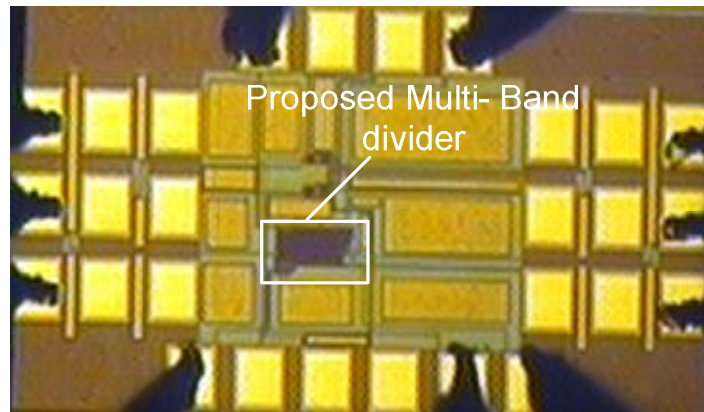


Fig. 5.15 Die photograph of the Multi-band divider

On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wave master 8600 6G oscilloscope. The measured results show that the proposed multi-modulus 32/33/47/48 prescaler has a maximum operating frequency of 6.2 GHz. However, the maximum operating frequency that can be achieved by the multi-modulus 32/33/47/48 prescaler is limited by the wide-band 2/3 prescaler.

The performance of the multi-band flexible divider is measured in both the lower frequency and higher frequency bands by programming the P and S counters. Fig.5.16 shows the measured output waveform of the multi-band divider at an input frequency of 2.47 GHz where P, S counters are programmed to have values 77 and 6 respectively ($FD=2470$). Fig.5.17 shows the measured output waveform of the multi-band divider at an input frequency of 5.818 GHz where P, S counters are

programmed to have values 122 and 38 respectively ($FD=5818$).

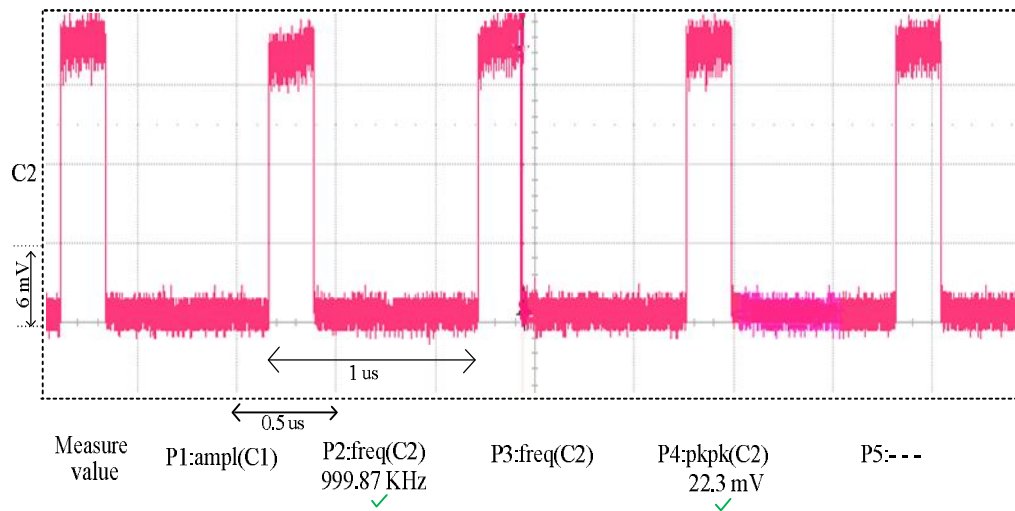


Fig. 5.16 Measured results of the Multi-band divider: 2.4 GHz band

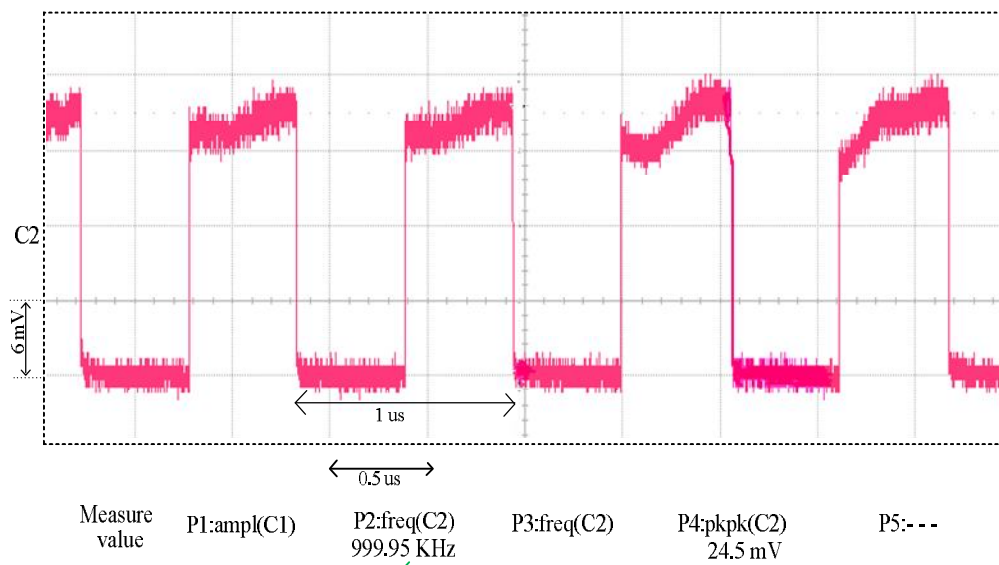


Fig. 5.17 Measured results of the Multi-band divider: 5 GHz band

The proposed multi-band flexible divider consumes an average power of 0.96 mW for the operation at the lower frequency band (2.4-2.484 GHz), and consumes 2.2 mW for the operation at the high frequency band (5-5.825 GHz). It out-performs the dual-band divider reported in [78], which consumes 2.7 mW at 1V power supply in both modes of operation. The proposed multi-band divider also has a variable resolution of in

steps of 1 MHz for both the lower (2.4-2.484 GHz), and the higher frequency band (5-5.825 GHz). Table 5.4 shows the performance of different dividers.

Table .5.4 Performance of different multi-band dividers

Reference	[78]	[54]	This work
Process (um)	0.18	0.25	0.18
Supply voltage (V)	1.0	1.8	1.8
Frequency (GHz)	2.4-2.7/5.14-5.7	5.14-5.7	2.4-2.484/5-5.825
Resolution (MHz)	9.375/20	20	1,2,5,10,20
Power (mW)	2.7	6.25	0.96/2.2

5.7. Summary

In this chapter, a wide-band $2/3$ prescaler based on single-phase clock is proposed which has maximum operating frequency of 6.5 GHz on silicon. The proposed $2/3$ prescaler is silicon verified in the design of the proposed multi-modulus 32/33/47/48 prescaler whose maximum operating frequency is 6.2 GHz. A dynamic logic multi-band flexible integer-N divide is designed which uses the wide-band $2/3$ prescaler, and a new multi-modulus 32/33/47/48 prescaler and is silicon verified using the 0.18 μm CMOS technology. Since the interest lies in the 2.4 GHz and 5 GHz band of operation, the P and S-counters are programmed accordingly. The proposed multi-band divider provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4 and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

CHAPTER 6

DESIGN OF CHARGE PUMP AND LOW POWER VCO

6.1. Introduction

Frequency dividers and VCOs are the power hungry and critical blocks in the PLL frequency synthesizer. Chapter 3, 4 briefly discusses the design of a low power fully programmable divider. The charge pump PLL synthesizer architecture is widely used since it offers several advantages such as infinite pull in range and zero steady state phase error [79], [80]. In this chapter we discuss the design and analysis of the low spur charge pump, low phase noise LC VCO and phase frequency detector.

6.2. Design and Analysis of Charge Pump

The main functionality of the charge pump circuit is to convert the logic states of the PFD to voltage related information by generating charging and discharging currents that enter the loop filter which controls the VCO. A simple charge pump topology with capacitive load is shown in Fig.6.1. When UP signal is high, the capacitor C_I is charged and the control voltage at input of VCO changes to pull up the VCO frequency. When DN signal is high, the capacitor C_I is discharged and the control voltage at input of VCO changes to pull down the VCO frequency. The critical parameters involved in the design of charge pump are the dynamic range, charge pump current, spurs.

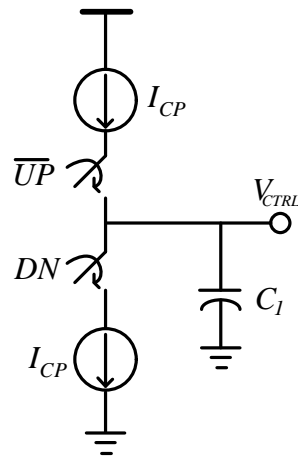


Fig. 6.1 Simple charge pump with capacitive load

6.2.1. Charge Pump Non-idealities

Ideally under the locked condition, there is no mismatch between the charge pump charging and discharging currents. But in reality there exists non-idealities such as the current mismatch and leakage current at the output node of charge pump which modulates the control voltage of the VCO and appears as spurs in the PLL output spectrum. In this section, we analyze the non-idealities of charge pump and its effects on the PLL performance.

A. Leakage current:

One of the main issues in the charge pump is the leakage current caused by the charge pump itself and the on-chip varactor [22]. The leakage current exists when both UP and DN currents are expected to be off. The phase offset due to the leakage current is negligible, but the reference spurs caused by the leakage current is substantial in frequency synthesizers. A certain amount of phase error has to be presented to

compensate the control line offset as shown in Fig.6.2. The average current of the charge pump over one period should be zero under the locked condition. If we ignore the reset time, the output charge pump current is shown in Fig. 6.3.

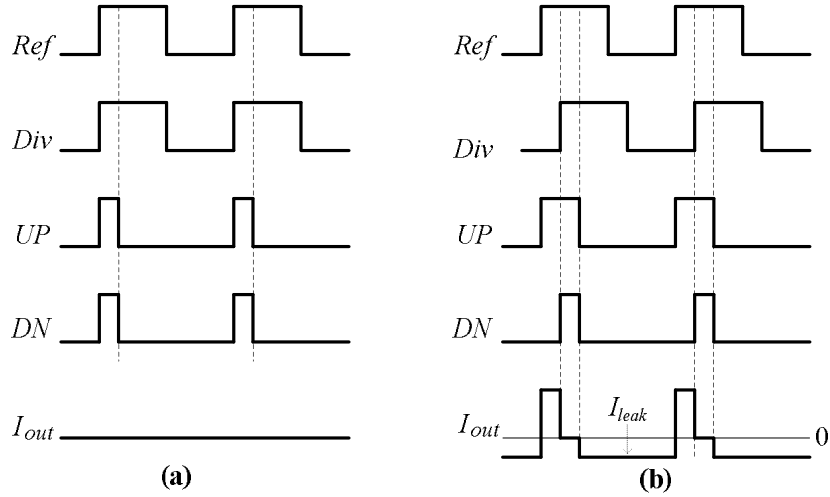


Fig. 6.2 Leakage current of charge pump a) without offset b) with offset

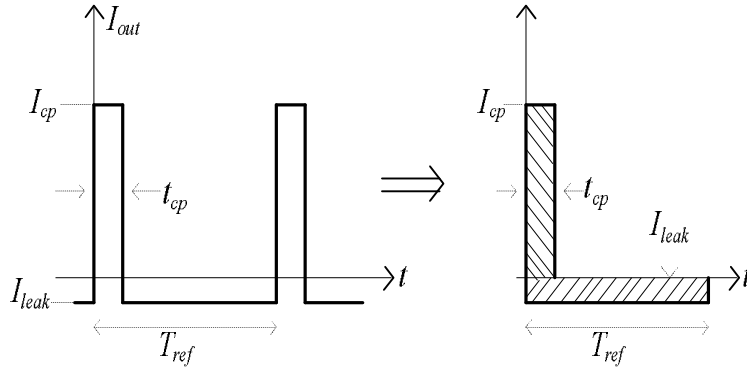


Fig. 6.3 Simplified charge pump out current with offset

If I_{cp} is the charge pump current, t_{cp} is the on-time period for the UP and DN signals and T_{ref} is the period of the input reference signal to the PFD, then the following equation holds true, which is given by

$$I_{cp} \times t_{cp} - I_{leak} \times (T_{ref} - t_{cp}) = 0 \quad (6.1)$$

which results in $t_{cp} = (T_{ref} \times I_{leak}) / (I_{cp} + I_{leak})$. Thus the charge pump output current

$I_{out}(t)$ over one reference period is given by

$$I_{out}(t) = \begin{cases} I_{cp} & \rightarrow 0 \leq t < t_{cp} \\ I_{leak} & \rightarrow t_{cp} \leq t < T_{ref} \end{cases} \quad (6.2)$$

By performing Fourier transform on the charge pump output current $I_{out}(t)$, the

coefficient C_N for N^{th} harmonic is calculated as,

$$C_N = -\frac{I_{leak} + I_{cp}}{2\pi N} \left[\sin 2\pi N \frac{I_{leak}}{I_{leak} + I_{cp}} + 2 \sin^2 \left(\pi N \frac{I_{leak}}{I_{leak} + I_{cp}} \right) \right] \quad (6.3)$$

Since $I_{leak} \ll I_{cp}$, C_N can be approximated as,

$$C_N \approx -\frac{I_{leak}}{N} \quad (6.4)$$

Since the loop bandwidth is about one-tenth of the input reference frequency, the

harmonics contained in the charge pump output current $I_{out}(t)$ are far out of the loop

bandwidth, which are attenuated by the loop filter. If the loop filter is of a second

order, the amplitude of the N^{th} harmonic appearing at VCO control line is given by

[81], [82].

$$A_N \approx -\frac{I_{leak}}{N^2} \frac{R}{f_{ref} / f_p} \quad (6.5)$$

Where f_{ref} is the reference frequency to the PFD, f_p is the pole of loop filter outside the

bandwidth. Using narrow-band FM theory [22], [83], the amount of the reference spur

due to the leakage current is given by

$$A_{leak-spur} \approx -\frac{I_{leak}}{2f_{ref}} \frac{K_{VCO}R}{f_{ref}/f_p} \tag{6.6}$$

(6.6) shows that if f_{ref}/f_p and I_{leak} remains constant, the reference spurs can be improved by reducing the VCO gain, the loop filter resistor value (R) and increasing the reference frequency f_{ref} .

B. Mismatch current:

Another major problem with charge pump is mismatch current which arises due to mismatch between UP and DN signals. Normally mismatch current originates due to the different type of devices used for sourcing (P-type) the current from supply to the output node and sinking (n-type) the current from the output node to ground. When this mismatch occurs, it is important to reduce the turn-on time delay (t_{on}) of the PFD to avoid the dead-zone.

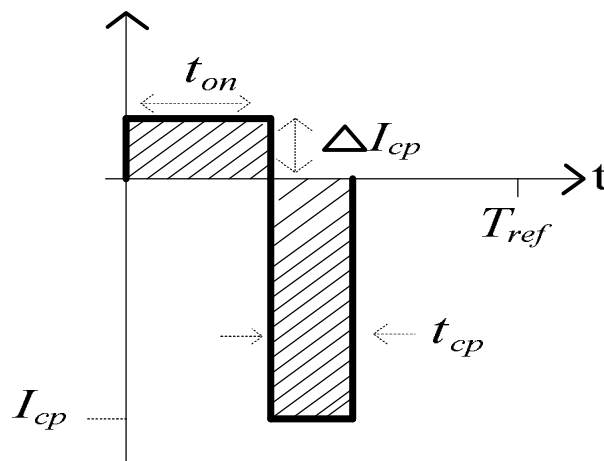


Fig. 6.4 Charge pump output current in the locked state due to mismatch

Fig.6.4 shows the charge pump output current due to mismatch in UP and DN in the locked state. By using the similar procedure used to calculate the spurs due to

leakage current, the amount of reference spur due to mismatch current is given by

$$A_{mismatch-spur} \approx -t_{on} \times \frac{\Delta I_{cp}}{2f_{ref}} \frac{K_{VCO}R}{f_{ref}/f_p} \quad (6.7)$$

Where ΔI_{cp} is the current difference between the *UP* and *DN* current and t_{on} is the reset time of the PFD. (6.7) shows that for a constant f_{ref}/f_p and ΔI_{cp} , the reference spurs due to the mismatch current are reduced by minimizing the reset time.

6.2.2. Implementation of the Charge pump: Design-I

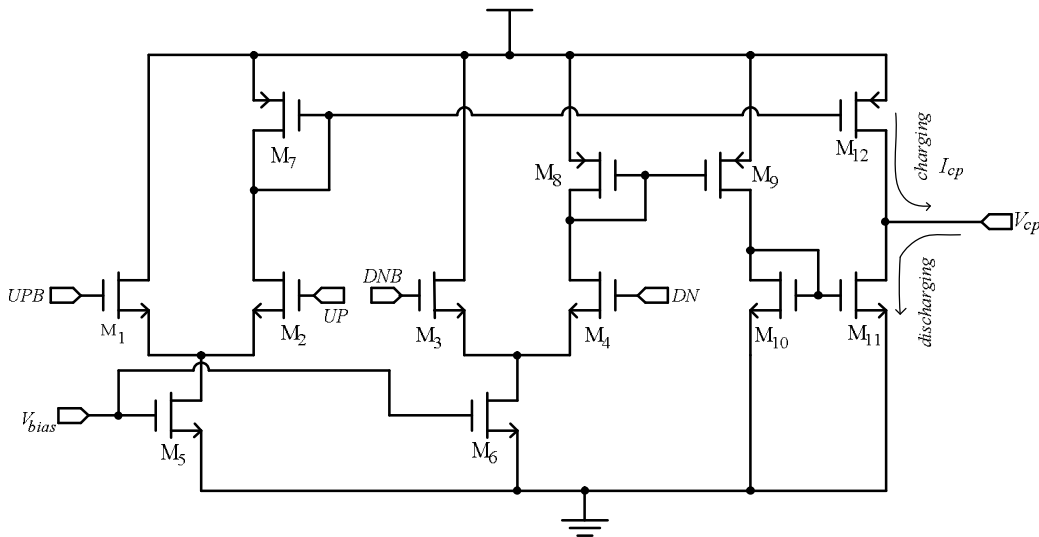


Fig. 6.5 Schematic of the charge pump

The schematic of the charge pump used in the design of the PLL synthesizer is shown in Fig.6.5. The charge pump circuit consists of two input differential pairs M_1 - M_2 and M_3 - M_4 which act as the switches, two current sources M_5 and M_6 supply stable current to the differential switches, a pump-up sub circuit formed by M_7 and M_{12} outputs the charge current I_{charge} and a pump-down sub-circuit formed by M_8 , M_9 , M_{10} and M_{11} which helps to discharge the current $I_{discharge}$.

Case-I: UP='1' and DN='0'

When the UP signal is high ($UP='1'$) and the DN signal is low ($DN='0'$), M_4 is turned-off, M_2 is turned-on and the pump-up sub-circuit is switched on. Hence the charge current I_{charge} flows from M_{12} and the loop filter is charged up. Since M_4 is turned-off, the pump-down sub-circuit is turned-off and no discharge current $I_{discharge}$ current flows in M_{11} .

Case-II: UP='0' and DN='1'

When the UP signal is low ($UP='0'$) and the DN signal is high ($DN='1'$), M_2 is turned-off, M_4 is turned-on and the pump-down sub-circuit is switched on. Hence the discharge current $I_{discharge}$ flows from M_{11} to the ground and the loop filter is discharged. Since M_2 is turned-off, the pump-up sub-circuit is turned-off and no charge current I_{charge} current flows in M_{12} .

Case-III: UP='1' and DN='1'

When both the UP and DN signal are driven high ($UP='1'$ and $DN='1'$), M_4 and M_2 are turned-on and both the pump-up and pump-down sub-circuits are switched on, allowing the currents to steer through them. If both charging (I_{charge}) and discharging ($I_{discharge}$) currents are equal, the charge stored on the loop filter remains same and doesn't affect the control voltage at the input of VCO. However, there exists a mismatch between charging and discharging currents through devices M_{11} and M_{12} ,

and a net current of $(I_{charge} - I_{discharge})$ leaks in to the loop filter and alters the control voltage. This is one of the serious issues in the design of the charge pump as discussed in the section 6.2.1.

Case-IV: UP='0' and DN='0'

When both the *UP* and *DN* signals are driven low (*UP*='0' and *DN*='0'), M_4 and M_2 are turned-off and both the pump-up and pump-down sub-circuits are switched off.

The charging (I_{charge}) and discharging ($I_{discharge}$) currents are equal to zero.

6.2.3. Simulations Results: Design-I

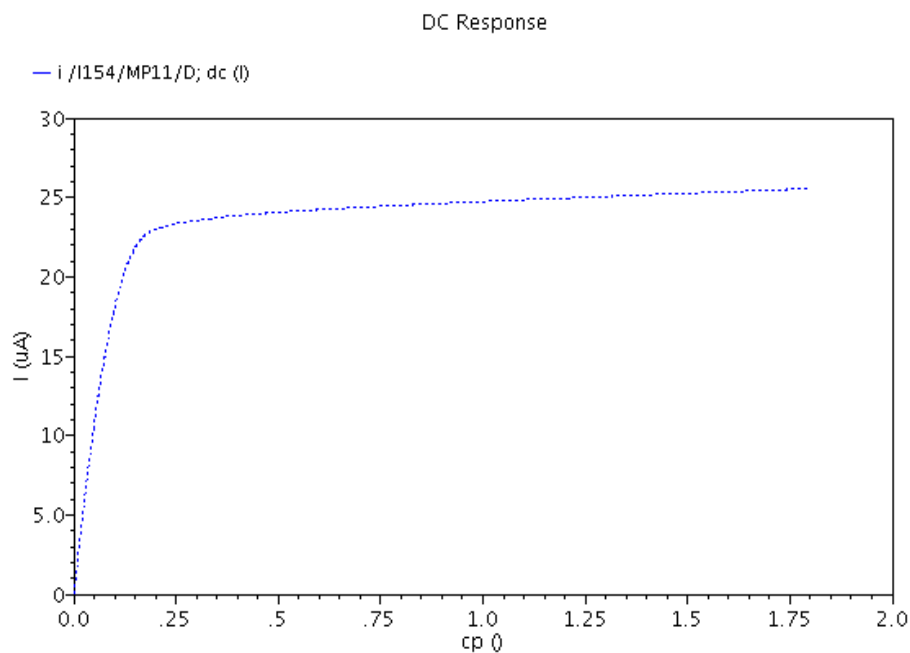


Fig. 6.6 Discharging current from charge pump when *UP* is low and *DN* is high

In this design, both the differential switches M_1 - M_2 and M_3 - M_4 are implemented by NMOS transistors to avoid the switching mismatches. To have precise matching in the charging and discharging currents, the length of the output stage transistors are kept

high to increase the output impedance. Fig 6.6 and Fig.6.7 shows the simulated DC simulations of *UP* and *DN* currents of the charge pump. Here the charge pump current chosen is 25 μA .

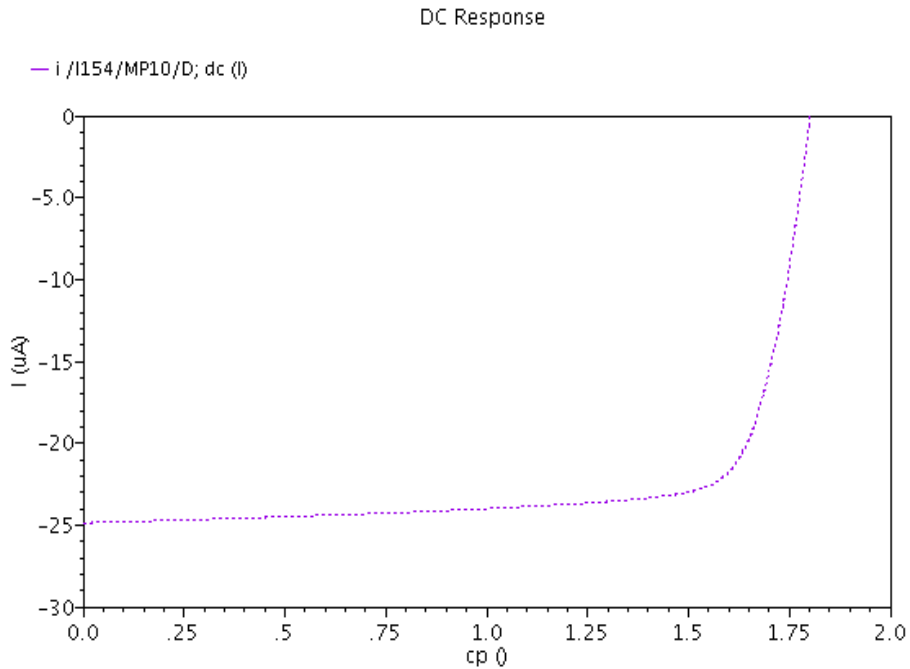


Fig. 6.7 Charging current from charge pump when *UP* is high and *DN* is low

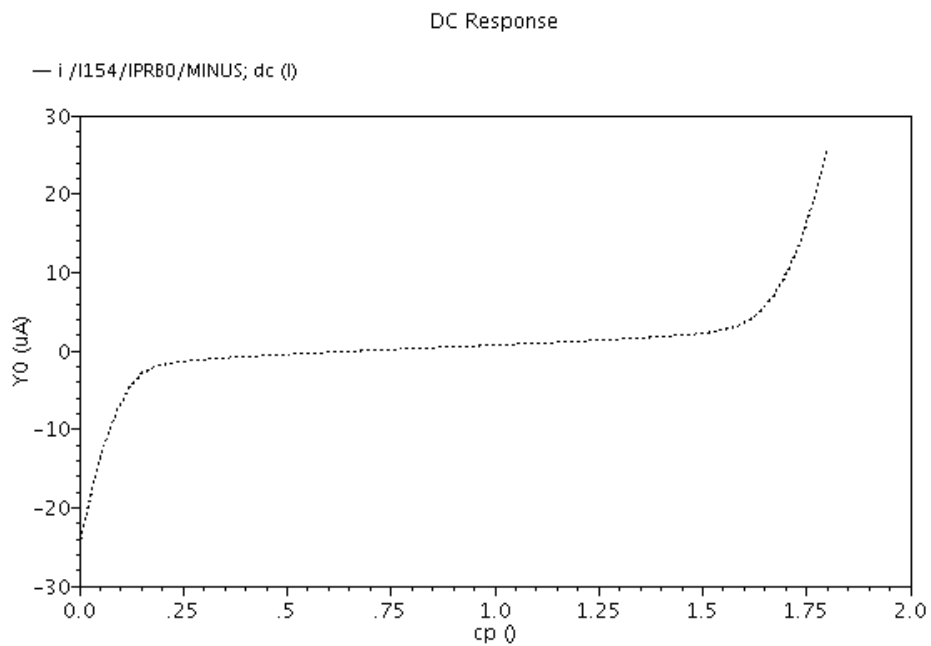


Fig. 6.8 Mismatch current from charge pump when *UP* and *DN* are high

Fig.6.8 shows the mismatch current between the *UP* and *DN* currents at 0.9 V is around $1.4 \mu\text{A}$. Based on the design values in [70], the reference spur is around -38.7dBc. One way to improve the spur level is either to reduce the reset time or increase the charge pump current. In the modified design, the charge pump current is increased to $100 \mu\text{A}$. Fig.6.9 and Fig.6.10 shows the charge pump charging and discharging currents.

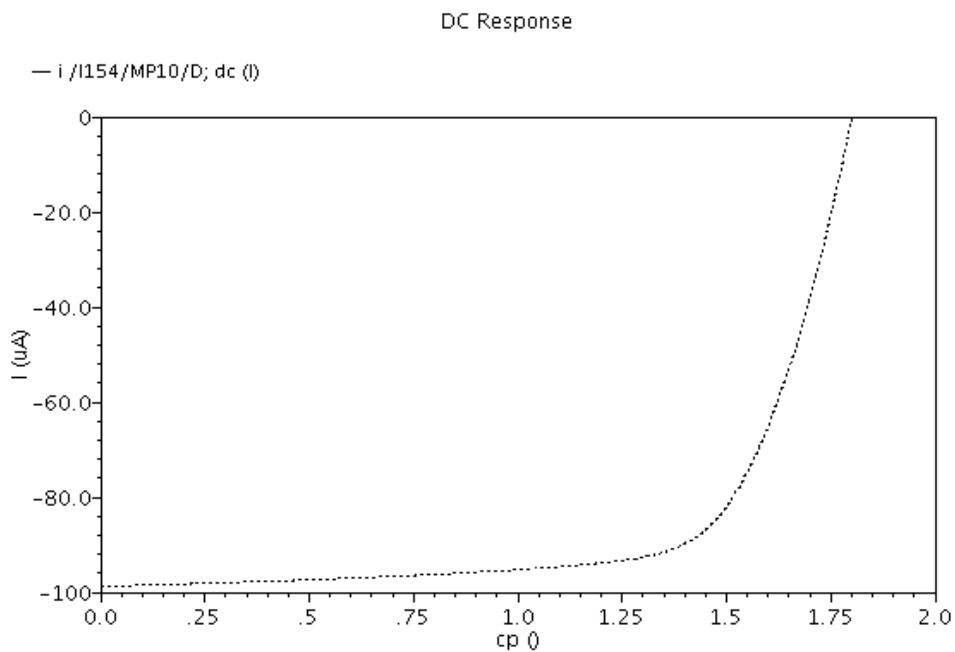


Fig. 6.9 Discharging current from charge pump when *UP* is high and *DN* is low

Fig.6.11 shows the mismatch current between the *UP* and *DN* currents at 0.9 V is around $1.2 \mu\text{A}$. Based on the design values in [70], the reference spur is around -46.8dBc. As the charge pump current value is increased, the loop filter capacitance increases which will be discussed in the Chapter 7. A new charge pump with gain boosting in the output stage is discussed in the next section which reduces the mismatch current and allows using a small charge pump current.

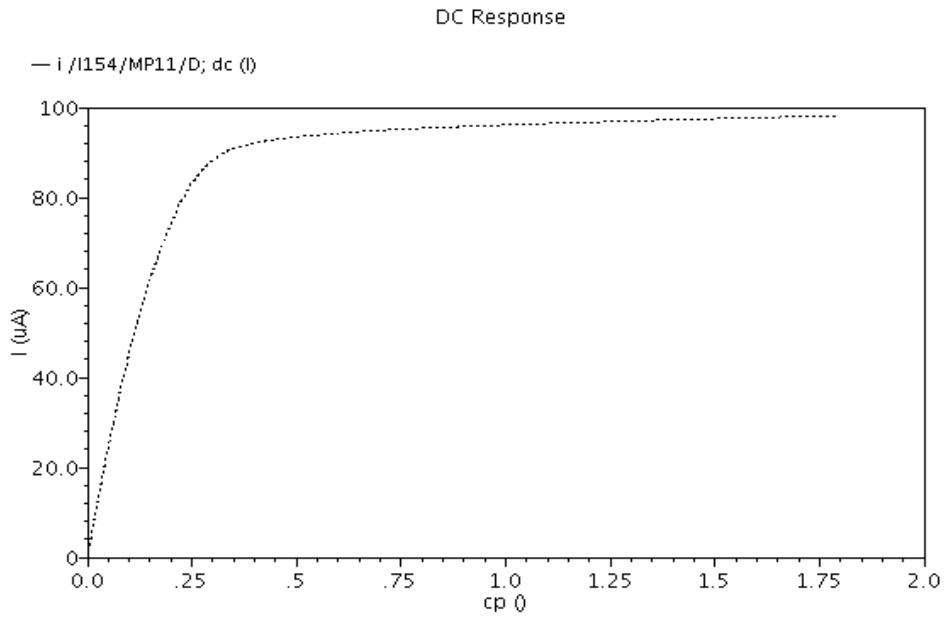


Fig. 6.10 Discharging current from charge pump when UP is low and DN is high

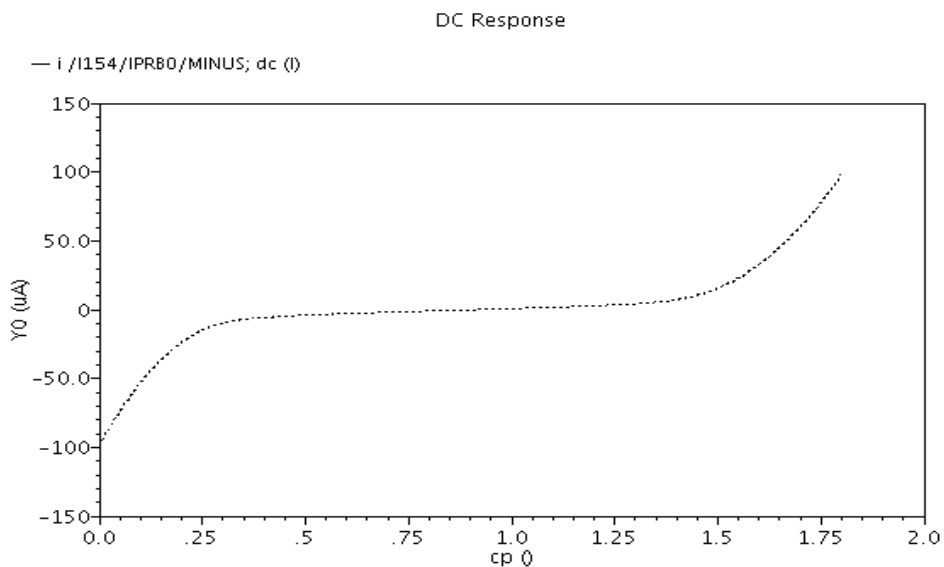


Fig. 6.11 Mismatch current from charge pump when UP and DN are high

6.2.4. Technique for reducing mismatch currents:

One of the common techniques used for reducing the mismatch currents is increasing the length of transistors in the output stage or increasing output impedance. The most popular technique is gain boosting structure at the output [84] as shown in Fig.6.12.

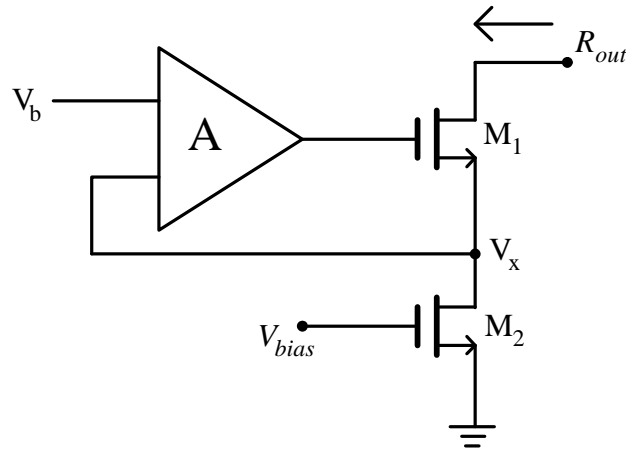


Fig. 6.12 Gain boosting circuit

The main idea here is to drive the transistor M_1 by an amplifier with gain “A” which forces node V_x to be same as V_b . Thus, any voltage variation at the drain of M_1 affects V_x to a lesser extent. Due to the small variation of voltage at node V_x , the output current remains constant. If g_{m1} , g_{m2} are transconductances of M_1 and M_2 respectively and if we assume $g_m = g_{m1} = g_{m2}$, the output impedance R_o is given by [85]

$$R_o \approx g_m r_o^2 A \quad (6.8)$$

6.2.5. A Low Spur Charge pump: Design-II

Fig.6.13 shows the improved charge pump design which is similar to the charge pump discussed in the section 6.2.2 with an additional gain boosting stages in the pump-up and pump-down sub-circuits. In the pump-up sub-circuit, transistors M_{14} , M_{20} and M_{19} are used for gain boosting while the transistors M_{18} , M_{21} and M_{22} are used for gain boosting in the pump-down sub-circuit. The charging and discharging operation is similar to the operation of the charge pump described in the section 6.2.2.

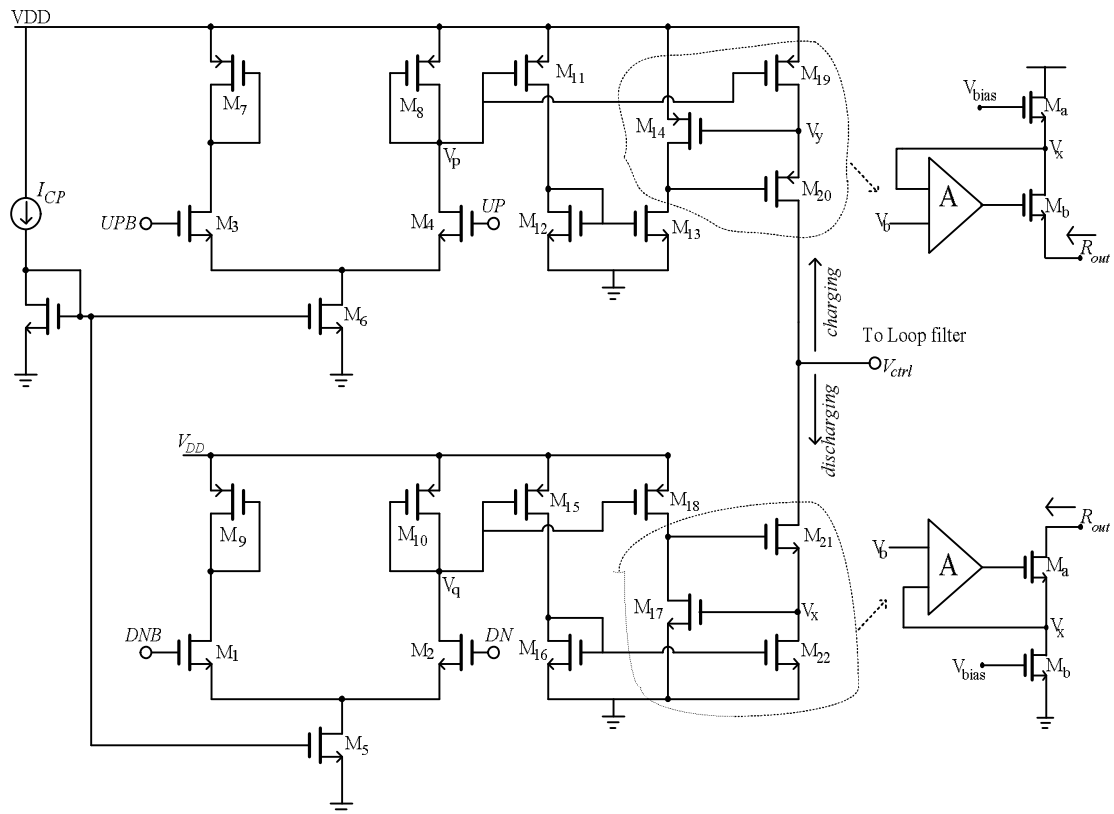


Fig. 6.13 An improved charge pump design with gain boosting stage in the output

During the discharging mode ($DN='1'$ and $UP='0'$), the charge pump current I_{cp} is steered through M_2 to the output with the help of M_{10} , M_{15} , M_{16} and M_{22} . The output impedance in the proposed charge pump is increased with the help of the gain boosting stage at the output. Here, the drain voltage of M_{22} is held at V_{GS} by M_{17} . If the drain voltage of M_{22} starts to decrease, M_{17} starts shutting-off, causing the gate voltage of M_{17} to increase, and pulls back the drain voltage of M_{21} . Thus, the drain current of M_{21} remains constant and the same applies to the gain boosting stage of pump-up sub-circuit. This technique allows the charging and discharging currents to be constant and reduces the mismatch current flowing in to the passive filter.

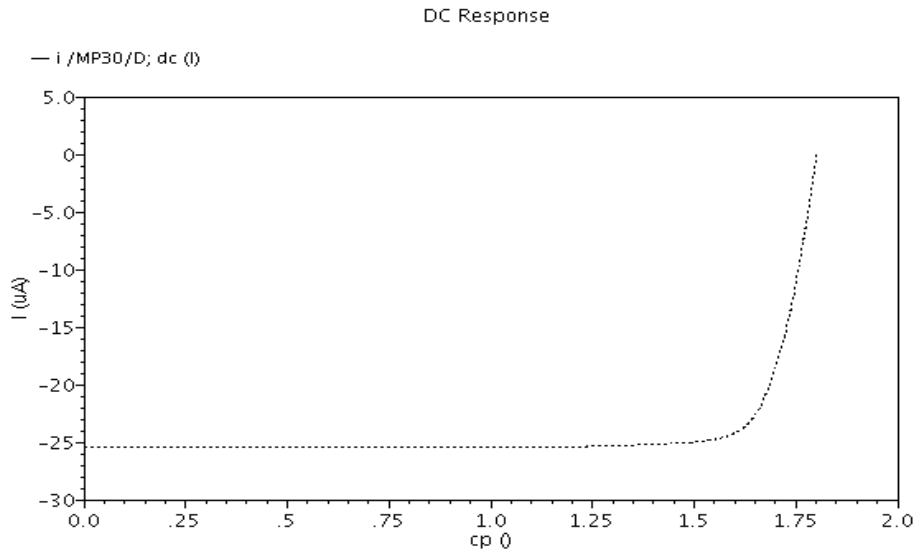


Fig. 6.14 Charging current of the proposed charge pump

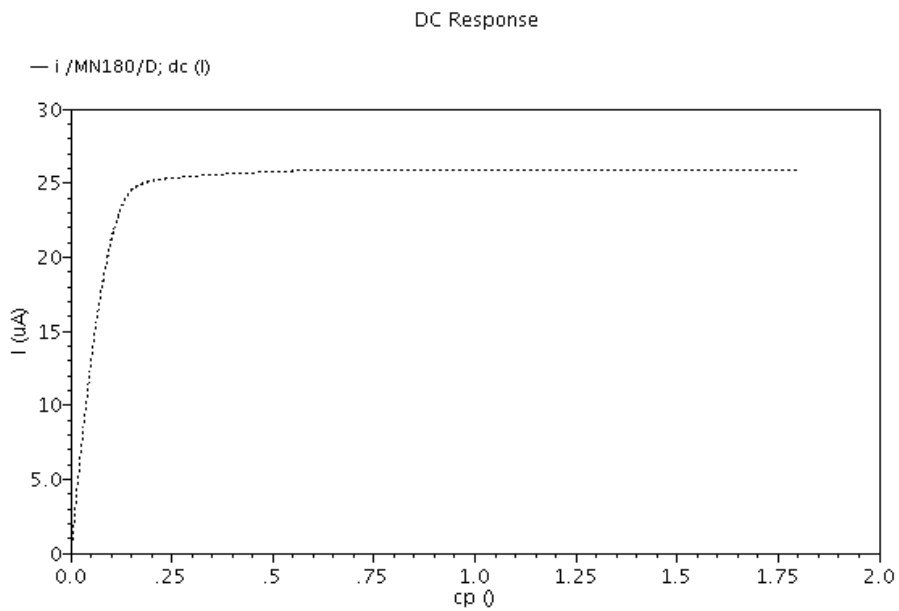


Fig. 6.15 Discharging current of the proposed charge pump

Fig.6.14 and Fig.6.15 shows the charging and discharging currents of the charge pump with a current (I_{CP}) of $25 \mu A$. Fig.6.16 shows the mismatch current where the mismatch is almost constant between 0.5 V -1.3 V. The average mismatch current is found to be around 350 nA for a charge pump current of $25 \mu A$. The reference spur

due to mismatch current is around -47.8dBc which is nearly 10 dB lower than that of the Design-I charge pump with the current of $25\ \mu\text{A}$. Thus the improved charge pump design helps to improve the spur level due to the mismatch current and also helps to reduce the on-chip loop filter area with a smaller charge pump current which will be discussed briefly in the next chapter.

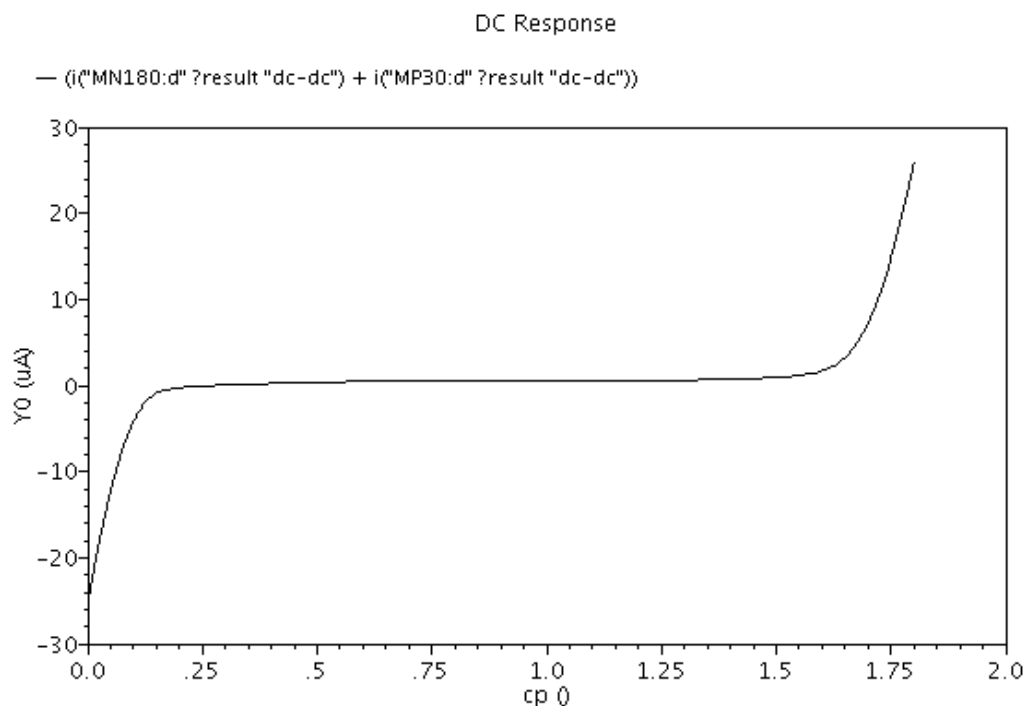


Fig. 6.16 Mismatch current of the proposed charge pump

6.3. CMOS Cross-Coupled LC VCO

The voltage controlled oscillator (VCO) is one of the critical blocks in the PLL synthesizer. One of the most critical design parameter of VCO is phase noise and much effort has been done in the past to improve the VCO phase noise performance [24], [86]-[88]. These papers summarize that to achieve a low phase noise, the bias

current has to be increased or maximize the oscillation amplitude or increase the tank inductance quality factor (Q) or filter the tail current noise. Increasing the bias current is not a feasible option since it increases the power consumption of the circuit while increasing the quality factor of the tank inductance leads to a narrow tuning range. In this section we have analyzed the cross-coupled complementary LC VCO and its phase noise performance. Based on this analysis, a detailed design of 2.4 GHz cross-coupled LC VCO is presented.

6.3.1. Operation of the cross-coupled LC VCO

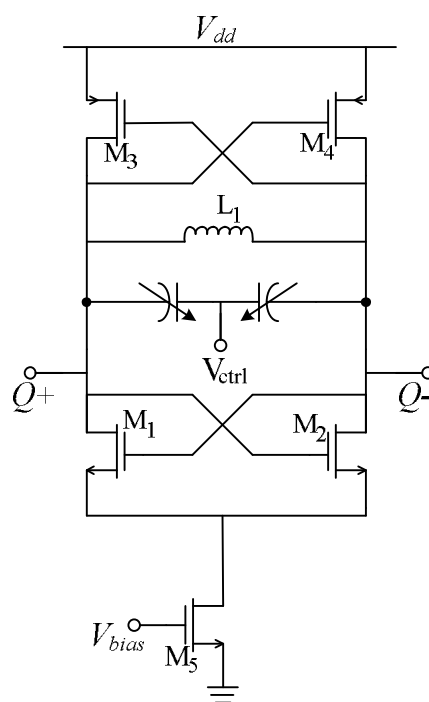


Fig. 6.17 Schematic of the cross-coupled complementary LC VCO

The schematic of the cross-coupled complementary LC VCO is shown in Fig.6.17. It has several advantages over NMOS only VCO and PMOS only VCO [86], [89]. The VCO has a cross-coupled structure made up of a pair of N type MOSFETs, a pair of P

type MOSFETs forming a positive feedback loop with LC resonators in the loop to select the operating frequency. The control voltage is utilized to tune the varactors capacitance value and hence the operating frequency of the VCO. The bias condition of the VCO is determined by the size of M_5 . To circumvent the asymmetry problem introduced by a single inductor, the inductor used in the VCO is split into two identical ones, and one is the mirror image of the other; thus the two output nodes are made symmetrical.

The small-signal voltage gain of the amplifier M_1 - M_2 is calculated by $A_v = g_m Z_p$. From this equation, we can deduce that the Barkhausen's Criteria is probably satisfied only at the resonant frequency, because the magnitude of the gain is maximized and its phase is equal to zero when the LC tank is resonating. Therefore, if the transconductance of the amplifying transistor is designed to be large enough to ensure its gain is larger than or equal to unity at the resonant frequency, the oscillation will be maintained. With the noise at any other frequency suppressed, the noise component at the resonant frequency is amplified, passed into the positive feedback loop and further amplified till the transistor enters the saturation region so that the oscillation amplitude is maintained.

6.3.2. A Model for Complementary Cross-coupled LC VCO Phase Noise Analysis

Fig.6.18 shows the equivalent circuit of the complementary LC VCO with its noise

sources. For symmetry, the inductor is modeled as two inductors with the inductance of $L/2$ and conductance of $g_L/2$. The varactor is modeled in a similar way in Fig.6.18. g_{mn} and g_{mp} are small signal transconductances of the cross-coupled NMOS and PMOS with output transconductances of g_{on} and g_{op} respectively. The equivalent capacitances associated to the gates of NMOS and PMOS transistors are given by (6.9) and (6.10) [90],

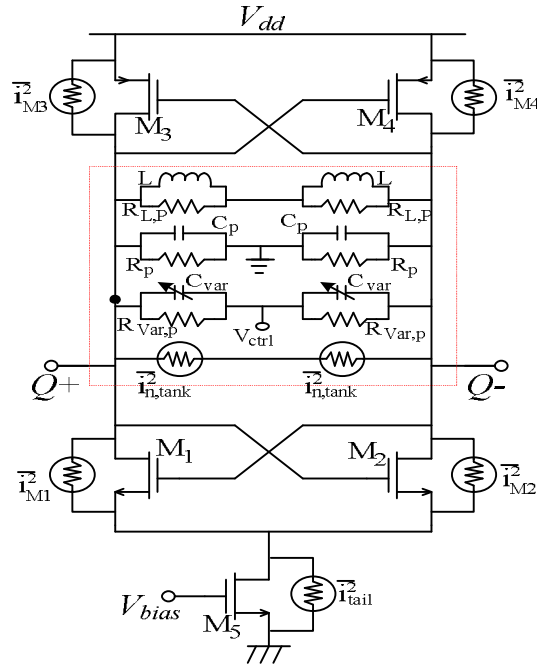


Fig. 6.18 Complementary LC VCO with noise sources

$$C_{NMOS} \approx C_{gs,n} + C_{db,n} + 2C_{gd,n} \quad (6.9)$$

$$C_{PMOS} \approx C_{gs,p} + C_{db,p} + 2C_{gd,p} \quad (6.10)$$

Here R_p and C_p model the parasitics due to interconnects and will impact the oscillation frequency. The phase noise models described in [91] and [92] mainly focus on single cross-coupled LC VCO (NMOS only or PMOS only). The phase noise model in [82] focuses on the complementary cross-coupled LC VCO. From Fig.6.18,

we can see that noises in LC oscillator are mainly from the tank, differential pairs and the tail transistor.

A. Phase noise of the tank

Based on Lesson's Model [34], the phase noise of the tank which is mainly due to the varactors and inductor is given by

$$L\{\Delta\omega\} = \frac{4kTR_p}{A_0^2} \times \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \quad (6.11)$$

Where R_p is the equivalent resistance of the tank and V_0 is the differential output voltage. The peak amplitude V_0 increases as the bias current (I_{bias}) increases in the current limited regime [27] and is given by

$$V_0 = \frac{4}{\pi} \times I_{bias} R_p \quad (6.12)$$

B. Phase noise from the differential pairs

As seen in Fig.6.18, each transistor is modeled by its equivalent noise source and if we assume $\overline{i_{M1}^2} = \overline{i_{M2}^2} = \overline{i_n^2}$ and $\overline{i_{M3}^2} = \overline{i_{M4}^2} = \overline{i_p^2}$, the transistor noise densities are given by

$$\frac{\overline{i_n^2}}{\Delta f} = 4kT\gamma g_{mn} \quad (6.13)$$

$$\frac{\overline{i_p^2}}{\Delta f} = 4kT\gamma g_{mp} \quad (6.14)$$

Where g_{mn} and g_{mp} are transconductances of NMOS and PMOS transistors respectively and γ is 2/3 long channels and is between 2 and 3 for a short channel device. The total noise power due to the transistors M₁-M₄ is given by

$$\frac{\overline{i_{o,n}^2}}{\Delta f} = \frac{1}{2} \left(\frac{\overline{i_n^2} + \overline{i_p^2}}{\Delta f} \right) = 4kT\gamma \left(\frac{g_{mp} + g_{mn}}{2} \right) \quad (6.15)$$

The phase noise due to differential pair transistors is given by

$$L\{\Delta\omega\} = \frac{\overline{i_{o,n}^2} \cdot |Z(j(\omega_0 + \Delta\omega))|^2}{V_0^2 / 2 \Delta f} = \frac{4kTR_p^2}{V_0^2} \left(\frac{g_{mp} + g_{mn}}{2} \right) \times \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (6.16)$$

Based on the noise model for mixer given in [93] and the analysis in [82], the simplified phase noise due to the four transistors M₁- M₄ is given by

$$L\{\Delta\omega\} = 4 \frac{\overline{i_{o,n}^2} \cdot |Z(j(\omega_0 + \Delta\omega))|^2}{V_0^2 / 2 \Delta f} = \frac{32kT\gamma R_p^2}{\pi V_0^3} \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \quad (6.17)$$

C. Phase noise from the tail transistor

The conversion of the tail transistor noise into phase noise at the oscillator output is a two-step process. The bias current noise $\overline{i_{tail}^2}$ is translated in frequency by the switching action of the differential pair. Low frequency bias noise ($\omega_n \ll \omega_0$) is mixed with oscillation frequency to create two correlated sidebands at $\omega_0 + \omega_n$ and $\omega_0 - \omega_n$, resulting in amplitude modulation (AM) noise. High frequency bias noise ($2\omega_0 + \Delta\omega$) down converts into a single noise sideband in the pass-band of the

LC tank containing both AM and PM noise. The resulting output noise current is then amplified and shaped by the positive feedback of the switching transistors and LC tank filter. This process implies that AM noise is suppressed and only PM noise arising from high frequency bias noise contributes to the phase noise. However, the AM noise can be potentially converted into PM noise due to the presence of the non-linear components [86].

According to the analysis in [82], the phase noise due to the tail transistor is given by

$$L\{\Delta\omega\} = \frac{128kT\gamma_{bias}g_{mbias}R_p^2}{\pi^2V_0^2} \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \quad (6.18)$$

By combining (6.11), (6.17) and (6.18), the phase noise of the complementary cross-coupled LC VCO is given by

$$L\{\Delta\omega\} = \frac{4kT\gamma R_p}{V_0^2} \left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \left(1 + \frac{8\gamma I_{bias}R_p}{\pi V_0} + \frac{32\gamma_{bias}g_{mbias}R_p}{\pi^2}\right) \quad (6.19)$$

6.3.3. Design of low power LC VCO

For Zigbee and IEEE 802.15.4 standard applications, the frequency synthesizer needs to generate channel frequencies in the spectrum of 2400-2483 MHz. Thus, the minimum required tuning range for the VCO is 83 MHz. However, keeping in mind the process variations, parasitics and other issues, we restricted the tuning range of VCO to less than 250 MHz such that the VCO sensitivity (K_{VCO}) is relatively small.

As discussed in the previous section of charge pump design, the mismatch and leakage currents increase the ripples on the control voltage and modulate it to appear as spurs at the PLL output. Having higher sensitivity leads to high spurs and degrades the phase noise performance [86]. The sensitivity is directly related to capacitance of the loop filter. To have less impact on phase noise and smaller loop filter capacitance, we tried to keep the required sensitivity of the VCO minimum.

In the complementary cross-coupled VCO design, matching PMOS and NMOS devices provide better symmetry properties to the oscillating waveform, which decreases the up-conversion of $1/f$ of the devices to the $1/f^3$ noise region [32], [94]. Table 6.1 gives the design parameters of an inductor used in this design.

Table 6.1 Design parameters of an inductor

Metal	Width/space	diameter	Turns	Q	L	r_s
Metal6	15um/3um	116um	5	8.5	6.77nH	12.25

The equivalent tank parallel resistance is given by

$$R_p = Q^2 \times r_s = 885\Omega \quad (6.20)$$

The analysis in Chapter 3 and Chapter 5 shows that minimum amplitude of the input signal required for the $2/3$ prescaler is around 300 mV. Considering the parasitics, prescaler input load and mixer load, the required VCO differential amplitude is 800 mV (400 mV peak). From (6.12), the bias current required to generate differential output amplitude of 800 mV is given by

$$I_{bias} = \frac{V_0 \times \pi}{4R_p} = 0.709mA \quad (6.21)$$

The tank transconductance is $g_{mtank} \geq 1/R_p = 1.12$ mS for the startup condition. From [95], the startup coefficient α is set to 3.5. The total transconductance of a single NMOS and PMOS is given by

$$g_m = g_{mn} + g_{mp} = \alpha(2g_{mtank}) = 7.84mS \quad (6.22)$$

For 0.18 μ m CMOS RF technology, $\mu_n c_{ox}$ and $\mu_p c_{ox}$ values are 356.3 μ A/V² and 78.49 μ A/V² respectively. To reduce 1/f noise, we choose $g_{mn} = g_{mp} = 3.92$ mS. Assuming the transistors are operated in saturation the region, the sizes of the devices are given by

$$\left(\frac{W}{L}\right)_{1,2} = \frac{g_{mn}^2}{I_{bias} \mu_n c_{ox}} = 61.61 \quad (6.23)$$

$$\left(\frac{W}{L}\right)_{3,4} = \frac{g_{mp}^2}{I_{bias} \mu_p c_{ox}} = 279.6 \quad (6.24)$$

For the minimum device length of 0.18 μ m, the widths of both NMOS and PMOS transistors are found to be 11 μ m and 51 μ m. For an overdrive voltage of 0.3V for the tail transistor having the length of 1 μ m, the width is found to be 44 μ m. Since the tuning range is 250 MHz, the lowest operating frequency is 2.325 GHz and highest operating frequency is 2.575 GHz. Considering the post-layout parasitics and other non-linearity properties, we have over designed the VCO by 150 MHz such that

VCO tuning range is from 2.475-2.725 GHz.

At $f_{\min}=2.475$ GHz,

$$C_{\max} = \frac{1}{(2\pi f_{\min})^2 L} = 0.611 \text{ pF} \quad (6.25)$$

At $f_{\max}=2.725$ GHz,

$$C_{\min} = \frac{1}{(2\pi f_{\max})^2 L} = 0.504 \text{ pF} \quad (6.26)$$

The varactor minimum and maximum capacitances are 0.504pF and 0.611pF respectively. However, due to the presence of device parasitics and tank parasitics, the actual minimum and maximum capacitances of varactor are smaller than the calculated values in (6.25) and (6.26) respectively. The total capacitance at each output node of the VCO is given by

$$C_{tot} \approx C_{\text{var}} + C_{p,NMOS} + C_{p,PMOS} + C_{load} \quad (6.27)$$

Where C_p 's are the parasitic capacitances of the NMOS and PMOS transistors, C_{load} is the load capacitance. From Chapter 3, it is found that the divider load is around 25fF and the parasitic capacitances of both the NMOS and PMOS devices based on their sizing is around 100fF. Based on this, the minimum and maximum capacitances of the varactor are 0.381pF and 0.491pF. For a minimum capacitance of 0.381 pF, the width of the MOS varactor is 210 μm .

6.3.4. Simulation results

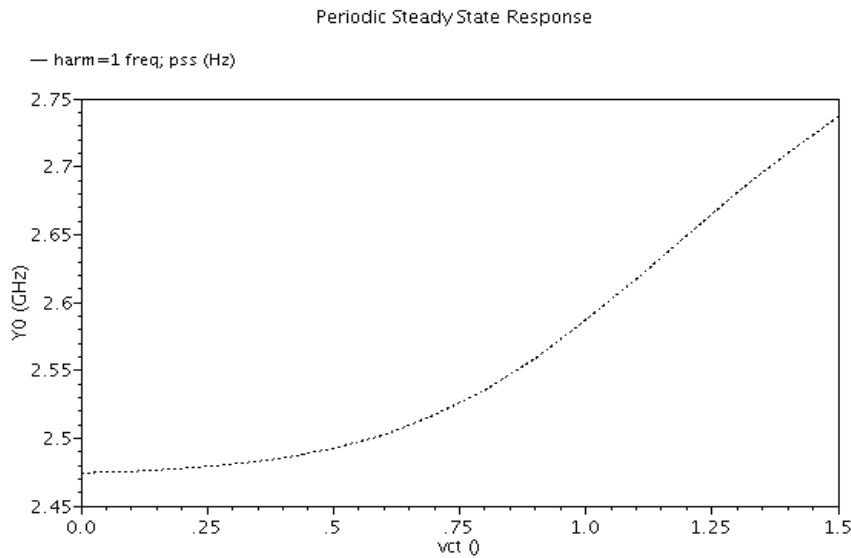


Fig. 6.19 Tuning range of implemented LC-VCO

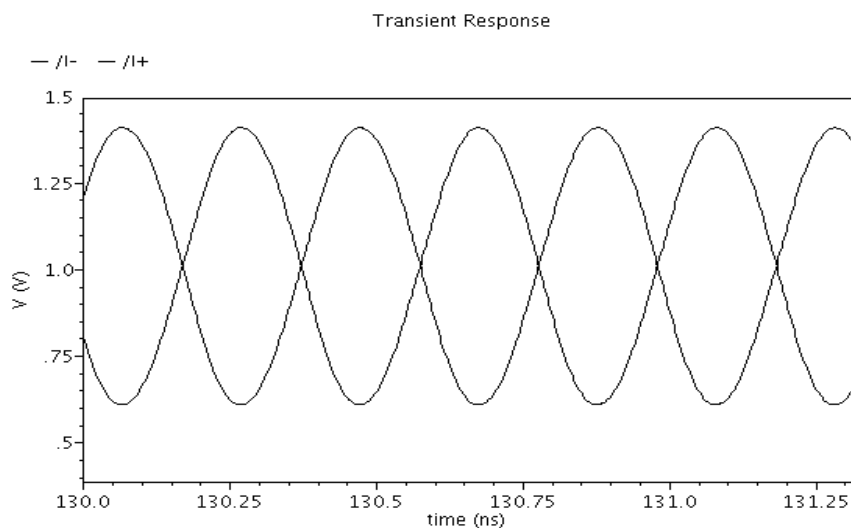


Fig. 6.20 Transient output waveform of the VCO

The complementary cross-coupled LC VCO shown in Fig.6.17 is simulated with values calculated in the previous section using Cadence RF Spectre at supply voltage of 1.5 V. Fig. 6.19 shows the tuning characteristics of the VCO which is around 260 MHz. Fig.6.20 shows the simulated transient output waveform of the VCO whose amplitude is around 750 mV. The VCO consumes a current of 705 μ A and the phase

noise is -96.17 dBc/Hz, -120.25 dBc/Hz at 100 KHz and 1 MHz offset respectively as shown in Fig.6.21.

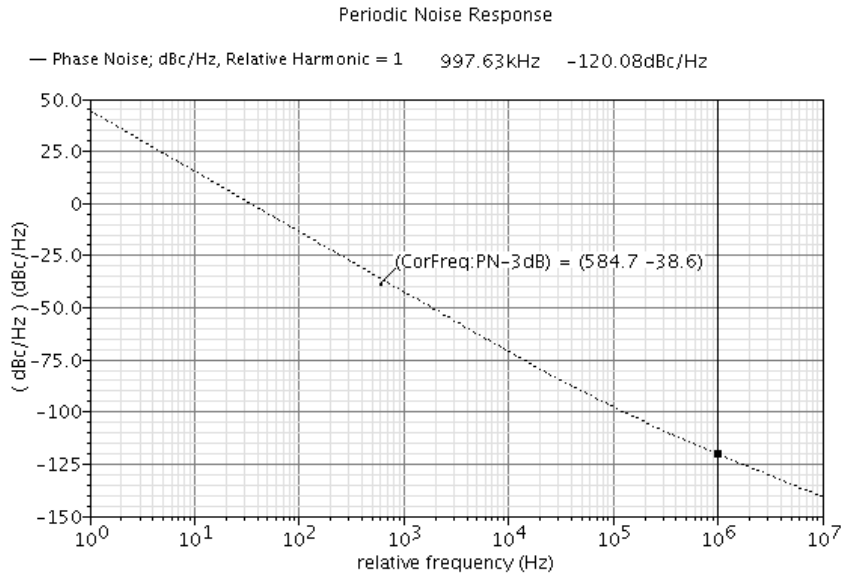


Fig. 6.21 Phase Noise performance of the VCO

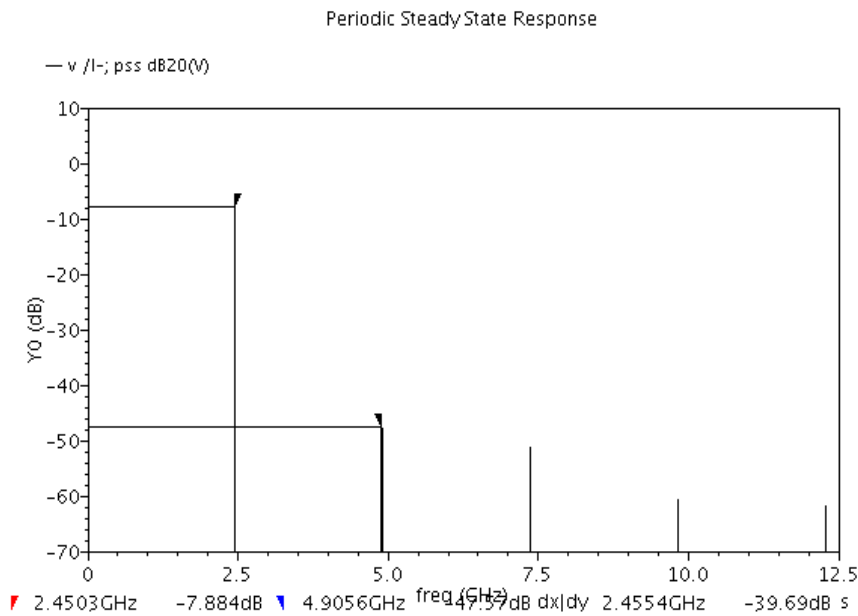


Fig. 6.22 Harmonic contents of the VCO output

Fig.6.22 shows the harmonic contents of the VCO output where the 2nd harmonic component is 39.7 dB below the fundamental component. The integrated

noise contribution (1 KHz to 1 MHz) of each PMOS, NMOS and tail transistor are 0.45%, 7.87% and 81% respectively.

6.3.5. Design of low power LC VCO: Tail current noise suppression [96]

The noise summaries of the complementary cross-coupled VCO design discussed in the previous section shows that tail transistor contribute 85% of the total noise. This means, the phase noise performance of the VCO is also affected by the low-frequency noise sources present in the VCO, of which largest contribution is coming from the tail current. A number of effects have been identified, such as AM-PM conversion of the varactor (basically non-ideal characteristic) [97], modulation of the tail capacitance [92] and other possible mechanisms.

The design reported in [27] uses a single capacitor in parallel with the tail transistor which prevents the up-conversion of the low frequency tail noise into phase noise. However, this technique lowers the high frequency impedance at the drain of tail transistor M_5 which is directly connected to the source of switching transistors. This node should be kept at a high impedance level for even harmonics of the oscillating frequency, in order not to degrade the quality factor of the oscillator [87]. The design reported in [96] uses inductive degeneration and capacitive filtering which suppress both the high frequency and low frequency tail current noise. Fig.6.23 shows the schematic of LC VCO with filtering technique where an inductor is added

between tail transistors M_5 and switching transistors M_1 - M_2 to remove the $2\omega_0$ component.

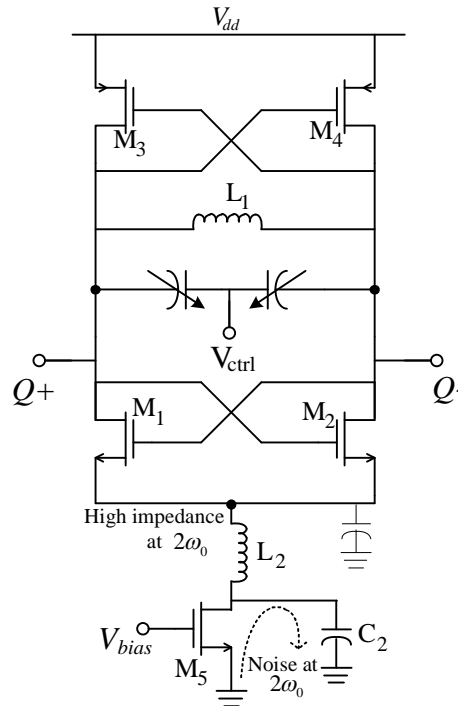


Fig. 6.23 Schematic of the complementary LC VCO with tail noise filtering technique

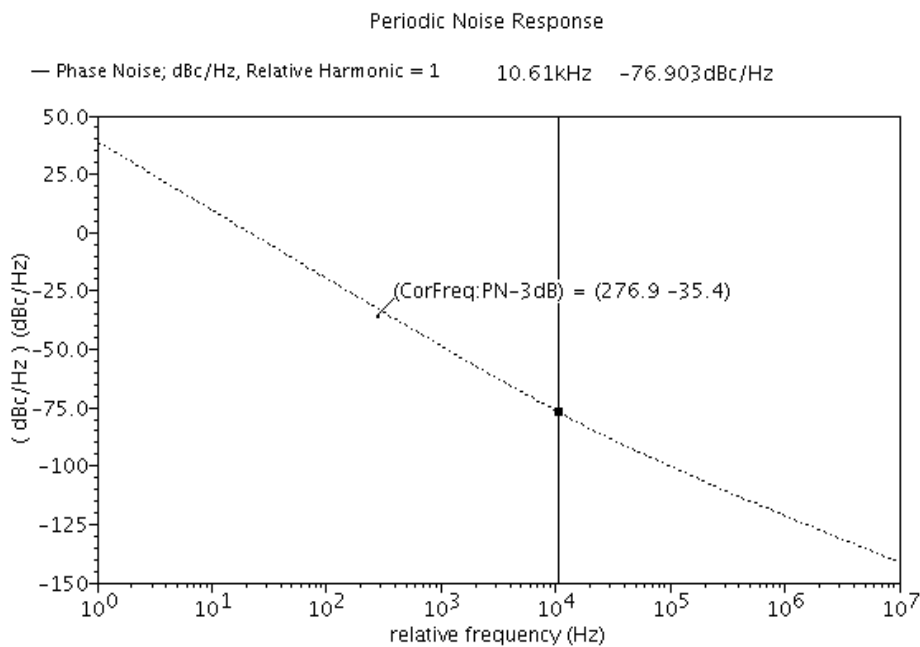


Fig. 6.24 Phase noise of the complementary LC VCO with tail noise filtering technique

The simulation results show that the phase noise of the VCO with filtering

technique improves and is about -100.48 dBc/Hz, -121.96dBc/Hz at 100 KHz and 1 MHz offset respectively as shown in Fig.6.24. The harmonic contents of the VCO output is shown in Fig.6.25 where the second harmonic is 43.36dB lower than the fundamental component. The integrated noise contribution (1 KHz to 1 MHz) of each PMOS, NMOS and tail transistor are 4.2%, 42% and 2% respectively. A widely used figure of merit (FOM) for the VCO is defined as [98],

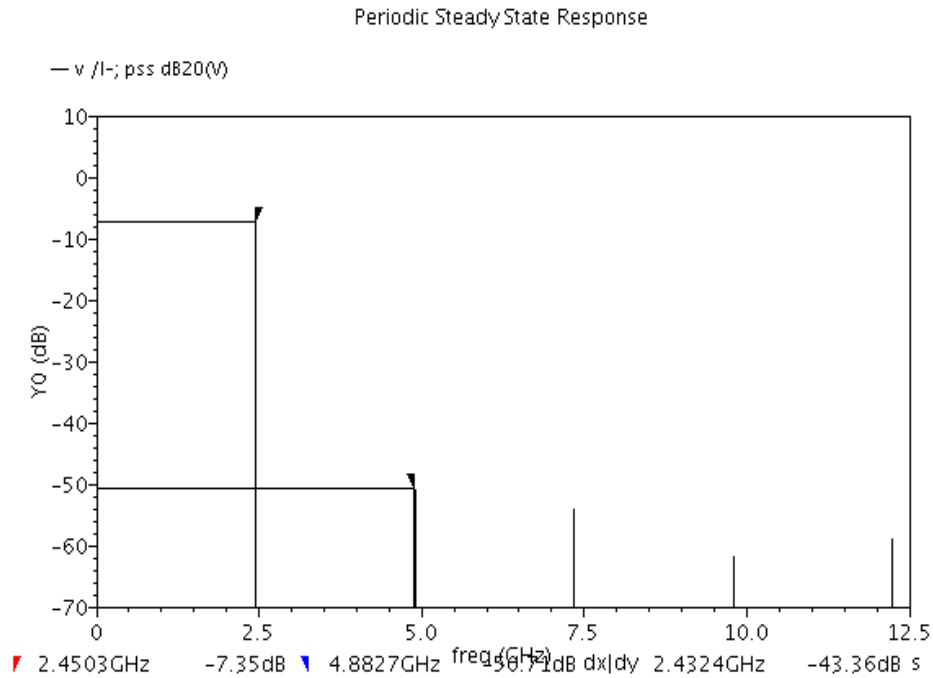


Fig. 6.25 Harmonic contents of the VCO output with filtering technique

$$FOM = L\{f_{offset}\} - 20\log\left(\frac{f_o}{f_{offset}}\right) + 20\log\left(\frac{P_{DC}}{1mW}\right) \quad (6.28)$$

where $L\{f_{offset}\}$ is the measured phase-noise at offset frequency f_{offset} from the carrier frequency f_o . P_{DC} is VCO power consumption in mW. Table 6.2 gives the performance of the implemented VCO.

Table 6.2 Performance of VCO design

Parameters	This Design
Power supply	1.5V
Technology	RF CMOS 0.18um
Frequency	2.42 -2.66 GHz
Tuning range	240 MHz
VCO gain (KVCO)	160 MHz/V
Phase Noise	-100.48 dBc/Hz @ 100 KHz offset -121.96 dBc/Hz @ 1 MHz offset
Output amplitude	800 mV (peak-peak)
Power consumption	1 mW
FOM	-189.74

6.4. Summary

In this Chapter, we have analyzed the non-idealities of the charge pump which are mainly the leakage current and mismatch current. Based on the mismatch current analysis and spur level calculations a new charge pump design is proposed which uses a gain boosting technique in the output stage to improve the matching between the charging and discharging currents. The implemented charge pump shows a 10 dB improvement in spur level due to the mismatch current. Subsequently, a detailed analysis of the complementary cross-coupled LC VCO is performed and implemented an LC VCO with tail current noise suppressing technique whose phase noise is -121.96dBc/Hz at 1 MHz offset. The designed VCO consumes 1 mW at 1.5-V voltage supply.

CHAPTER 7

IMPLEMENTATION OF 2.4 GHz FREQUENCY SYNTHESIZER

7.1. Introduction

The design and implementation of each building blocks of the frequency synthesizer has been briefly presented in the earlier Chapters. This Chapter deals with integration and implementation of a fully integrated 2.4 GHz frequency synthesizer in CMOS 0.18 μm technology. In this Chapter, we have presented two designs of fully integrated 2.4 GHz frequency synthesizer. The first design consists of optimized low power programmable divider (Design-I) and a series Q-VCO implemented at a supply voltage of 1.8-V for a reference study as there is no 2.4 GHz frequency synthesizer reported in literature with fully programmable divider based on single-phase clock logic. This design is successfully fabricated in a CMOS 0.18 μm technology and the measured results are presented. In this design, a conventional TSPC 2/3 prescaler [73] is used for constructing the programmable divider whose maximum operating frequency is 3.2 GHz at 1.8-V power supply and scaling the supply voltage for low power consumption is not a good option since the maximum operating speed of the divider reduces to 2.5 GHz and is not sufficient for 2.4 GHz applications.

In the second design, the fully integrated 2.4 GHz frequency synthesizer is implemented with proposed low power building blocks such as, ultra-low power 2/3

prescaler, a 47/48 prescaler, a low-spur gain boosting charge pump and a low power VCO at a reduced supply voltage of 1.5-V. Since the maximum operating frequency of the proposed 2/3 prescaler is 4.9 GHz at 1.8-V power supply, its speed performance is expected to be sufficient for the 2.4 GHz operation at 1.5-V supply while the power consumption is significantly reduced. This design is implemented in a CMOS 0.18 μm technology and the on-wafer measured results have been presented. However, individual blocks used in this design such as the low power divider and VCO were fabricated and their measured results were presented earlier.

7.2. Integration of 1.8-V, 2.4 GHz Frequency synthesizer: Design-I

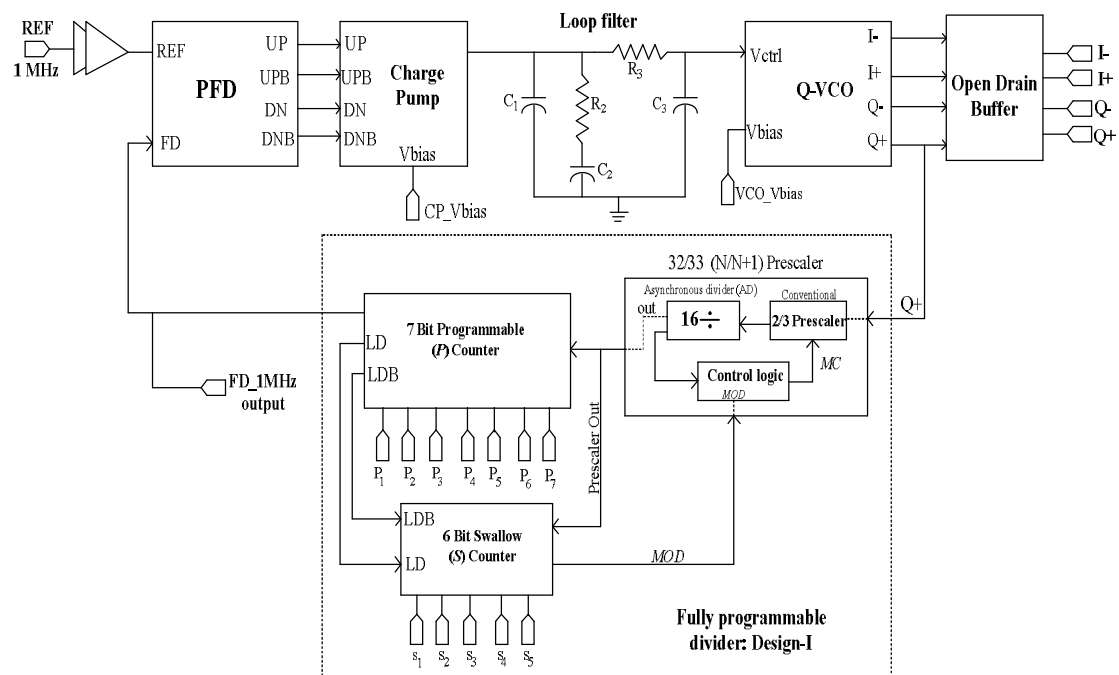


Fig. 7.1 Implemented 1.8-V 2.4 GHz PLL frequency synthesizer: Design-I

The implemented Design-I 1.8-V fully integrated 2.4 GHz PLL frequency synthesizer is shown in Fig.7.1. The synthesizer consists of a phase-frequency detector (PFD), a

charge pump (CP), a series Q-VCO, a 3rd order loop filter and a fully programmable 1 MHz resolution divider designated as Design-I in the section 4.2. The programmable divider consists of a 32/33 dual modulus prescaler constructed using a TSPC 2/3 prescaler, a 5-bit S-counter and a 7-bit P-counter. The P-counter is programmable from 74 to 77 and the S-counter is programmable from 0 to 31 in steps of 1 bit to accommodate division ratios from 2400 to 2483 in steps of 1. The charge pump implemented in this design is shown in Fig.6.5 and discussed in the section 6.2.2.

7.2.1. Circuit Implementation: Phase Frequency Detector (PFD)

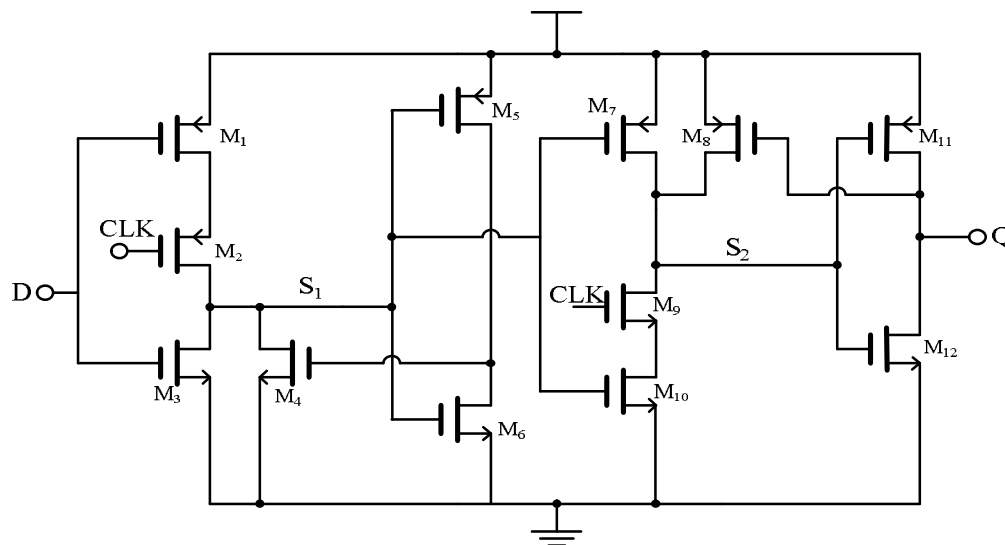


Fig. 7.2 TSPC half-transparent D flip-flop

The PFD used in this design is a conventional NAND based tri-state PFD described in the Chapter 2. The PFD consists of two DFF flip-flops (DFFs), a NAND gate and an inverter. The DFF is implemented by a half transparent D flip-flop (HTDFF) as shown in Fig.7.2 [71]. The HTDFF is transparent to D="1" and has a one clock delay to

$D=0$. Since the PFD operates at a low frequency of 1 MHz in the synthesizer, there exists a leakage at the pre-charge nodes S_1 and S_2 . Transistors M_3 , M_4 , M_5 and M_8 help to maintain the pre-charged node voltages [50]. The main advantages of this PFD are its high speed, low power and low phase sensitivity errors.

The PFD is simulated using Cadence Spectre for three different combinations: *Ref* leading *Div*, *Ref* lagging *Div* and both the *Ref* and *Div* having same frequency and phase. Fig.7.3, Fig.7.4 and Fig.7.5 shows the corresponding simulation results. The PFD consumes draws a current of $25.2 \mu\text{A}$ from 1.8-V power supply.

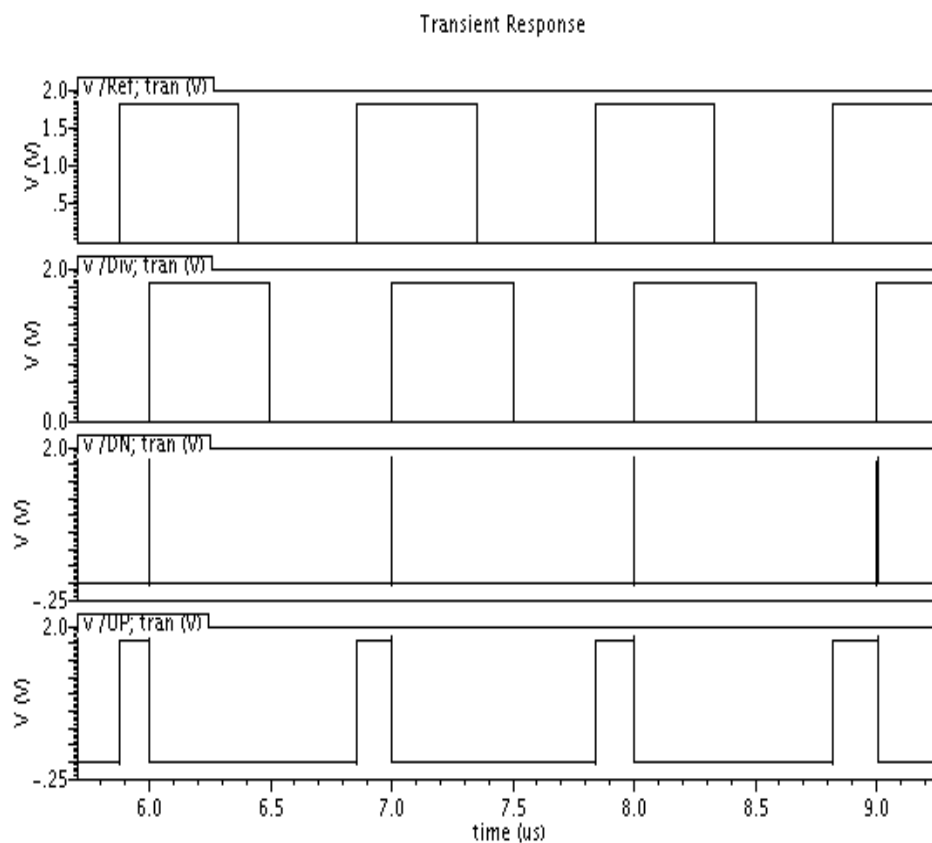


Fig. 7.3 Simulation results when Reference signal is greater than frequency divider output

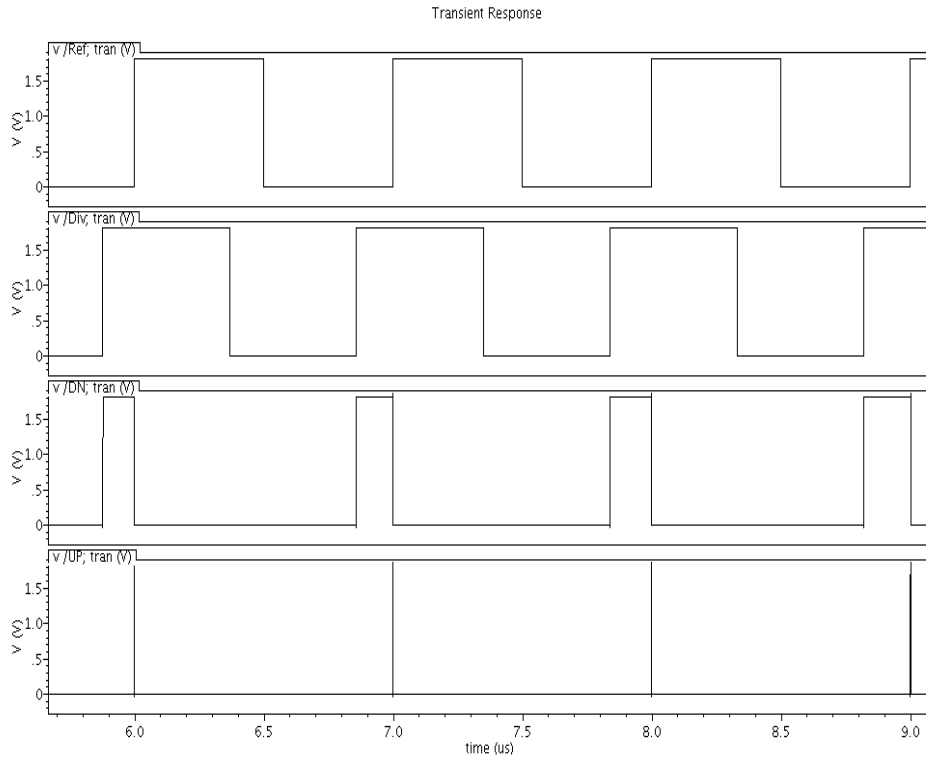


Fig. 7.4 Simulation results when Reference signal is less than frequency divider output

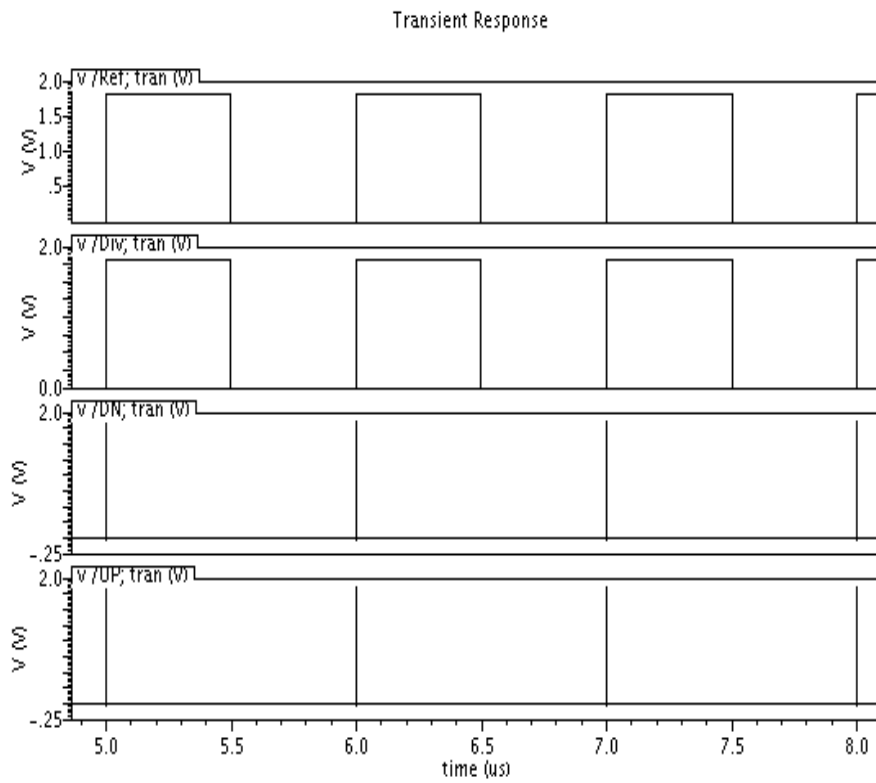


Fig. 7.5 simulation results when Reference signal is equal to frequency divider output

7.2.2. Circuit Implementation: Series Q-VCO

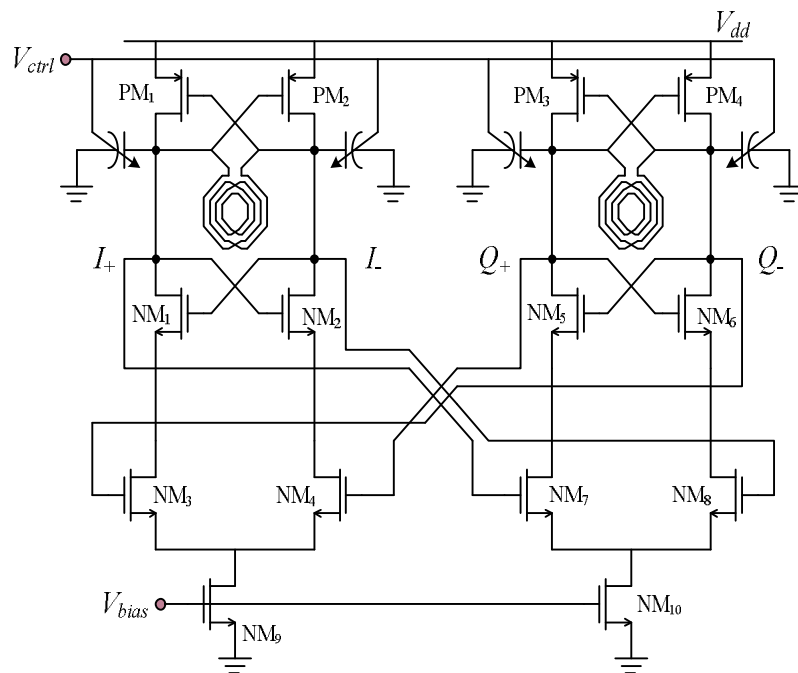
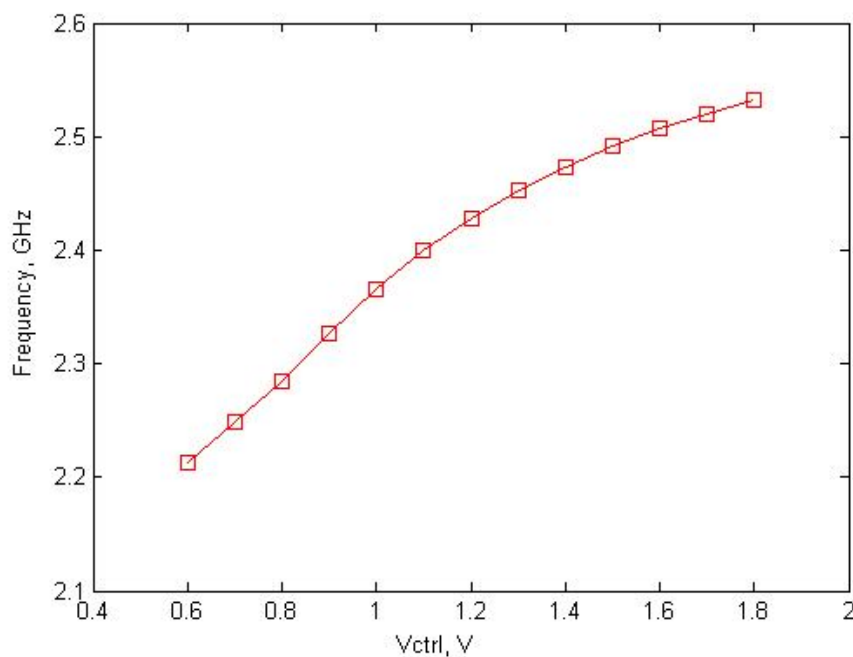


Fig. 7.6 Schematic of Series quadrature voltage controlled oscillator

The S-QVCO has been proven to eliminate the trade-off between phase noise and I/Q mismatch [99]. Therefore, the design can be optimized for phase noise performance, while keeping I/Q mismatch low. Compare to the Parallel-QVCO, the coupling transistors NM₃-NM₄ and NM₇-NM₈ are in series with the switching transistors NM₁-NM₂ and NM₅-NM₆. The current-reuse technique is used to reduce the current consumption of the S-QVCO by adding cross-coupled PMOS transistors on top of the cross-coupled NMOS transistors. The design procedure of LC tank for the Series QVCO is similar to what has been presented in Chapter 6. Table 7.1 is a summary of the dimensions of the devices of S-QVCO. Fig.7.7 shows the measured frequency tuning range of the quadrature generator.

Table 7.1 Series QVCO components dimensions

NM ₁ -NM ₂ , NM ₅ -NM ₆	30 μ m/0.18 μ m
PM ₁ -PM ₄	60 μ m/0.18 μ m
NM ₃ -NM ₄ , NM ₇ -NM ₈	60 μ m/0.18 μ m
Inductor (L)	2.77nH
Varactor	Tunable from 0.5pF

**Fig. 7.7 Measured frequency tuning range of the quadrature generator**

Open-drain transistors are added to the output nodes of the S-QVCO to serve as the buffer to the testing equipment. The S-QVCO is fabricated in CMOS 0.18 μ m technology. The measured tuning range of the S-QVCO is 2.2 GHz- 2.5 GHz and the amplitude of the VCO is around 400mV. Table 7.2 summarizes the performance of S-QVCO at a power supply of 1.8-V.

Table 7.2 Performance of Series QVCO

Parameters	S-QVCO
Power supply	1.8-V
Technology	RF CMOS 0.18um
Frequency tuning	2.2 -2.5 GHz
Amplitude	400 mV
Amplitude mismatch	0.3 dB
Phase Noise	-118 dBc/Hz @ 1 MHz offset
Phase error	2.5°
Power consumption	2.88 mW
FOM	-175.8

7.2.3. Design of Loop filter

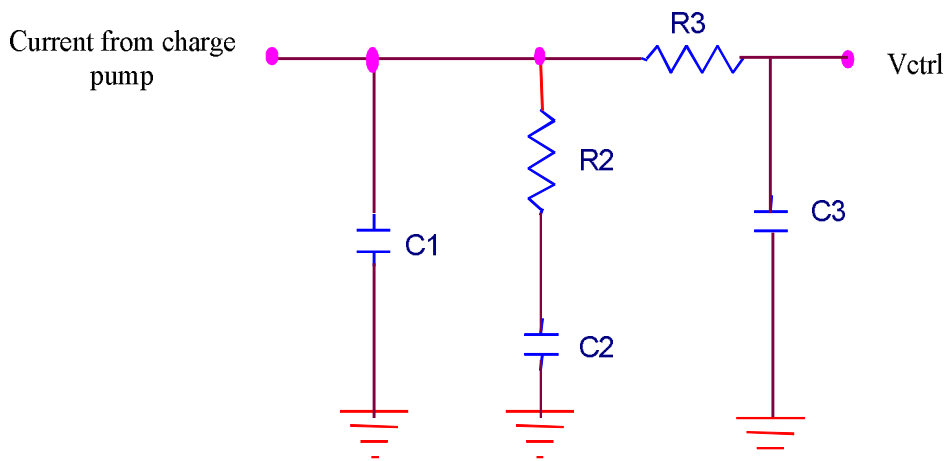


Fig. 7.8 3rd order passive loop filter

The loop filter used in this design is of a 3rd order as shown in Fig. 7.8. The loop filter parameters are imposed by the system level performance specifications such as settling time, phase noise and spur suppression. Initially a 2nd order filter is designed and later a RC low-pass section is added to improve the spurs and reduce the ripples on control voltage. The component values of the loop filter are designed based on the equations provided in the Chapter 2. The reference frequency used in this design is 1

MHz and loop bandwidth chosen is 100 KHz ($1/10^{\text{th}}$ of the reference). With a VCO gain (K_{VCO}) of 243 MHz/V and charge pump current of $100 \mu\text{A}$, the 2^{nd} order loop filter parameters are calculated and simulated using Matlab. Table 7.3 is summary of loop filter parameters.

Table 7.3 Loop filter parameters

Parameters	Values
Phase margin	55°
Unity gain frequency(ω_c)	0.628 Mrad/s
R_2	66.9 k Ω
C_2	95.2 pF
C_1	5.95 pF
R_3	68.85 k Ω
C_3	3.96 pF

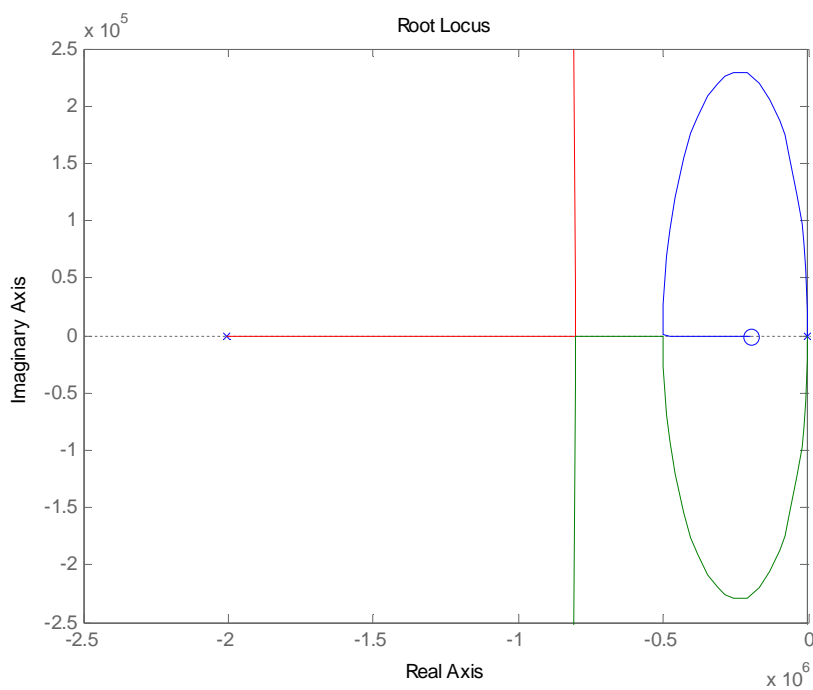


Fig. 7.9 Root locus of open loop Design-I PLL

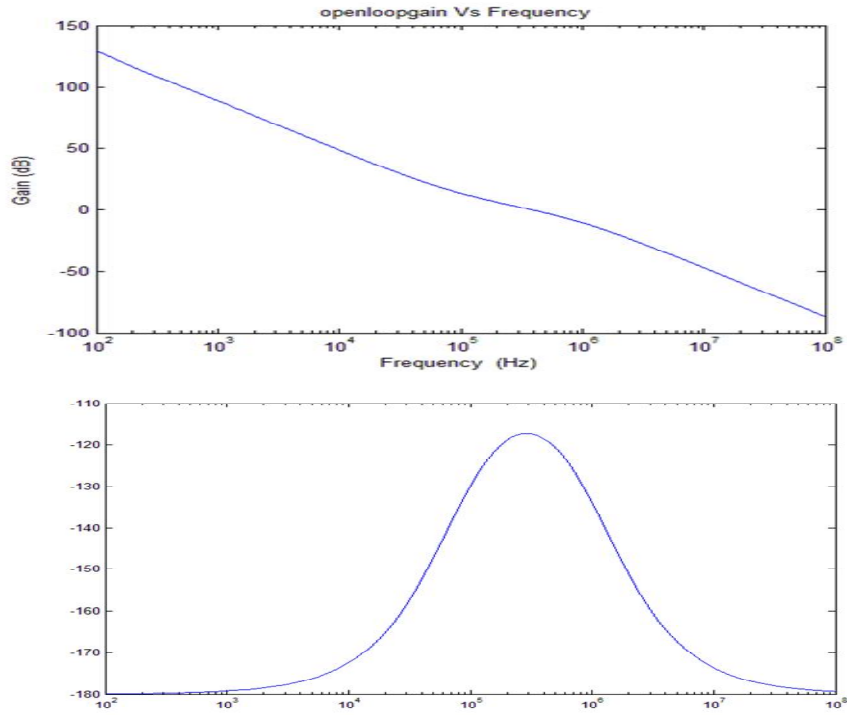


Fig. 7.10 Open loop gain and phase of Design-I PLL

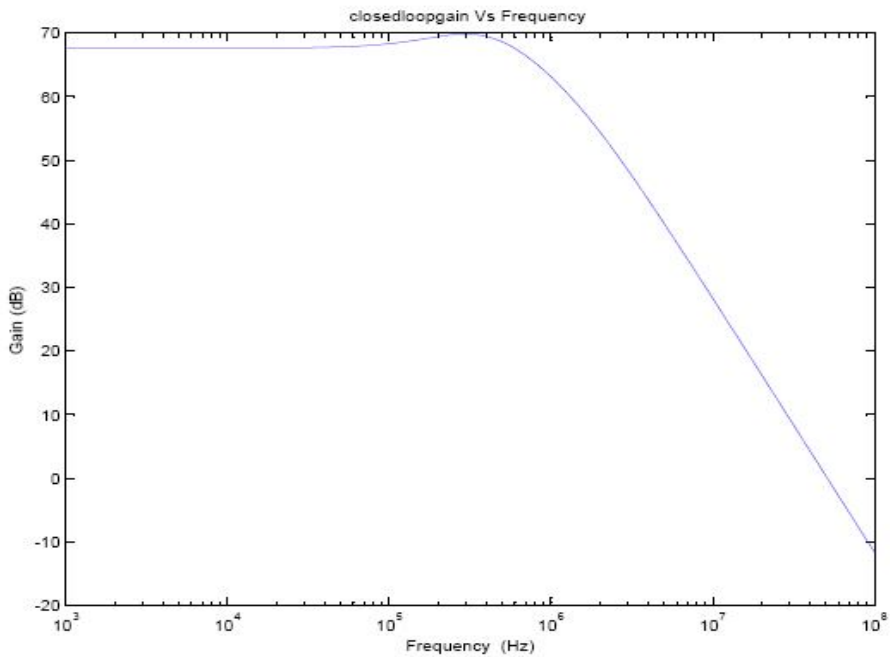


Fig. 7.11 Closed loop gain of Design-I PLL

The open loop PLL is simulated in Matlab and Fig.7.9 shows the root locus plot of the open loop PLL. Fig.7.10 shows the open loop gain and phase margin which is around

55°. Fig. 7.11 and Fig.7.12 shows the closed loop gain and step response of the PLL.

An additional RC low pass section is added to reduce the amount of reference spurs at the cost of reducing the phase margin and increasing the settling time.

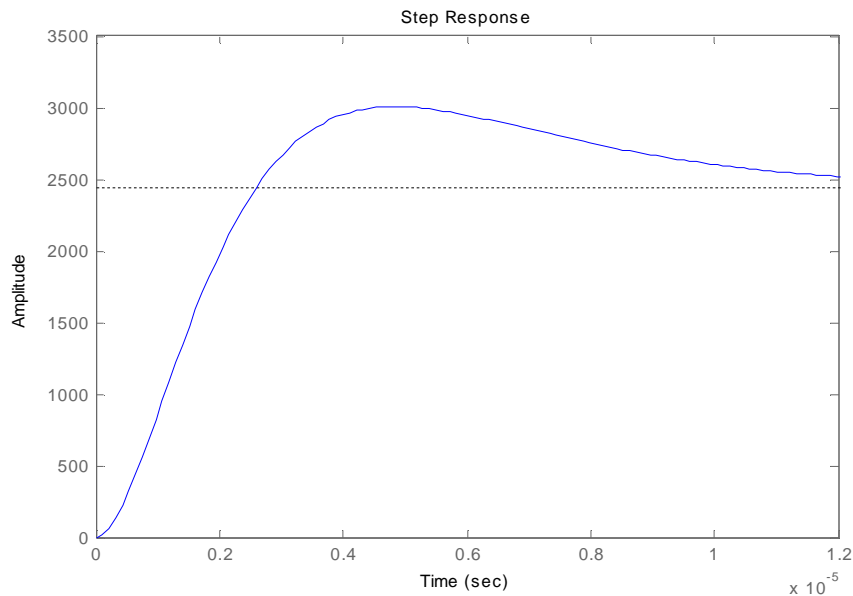


Fig. 7.12 Step response of the closed loop Design-I PLL

7.3. Measurement Results: Design-I Frequency Synthesizer

For silicon verification, the 2.4 GHz frequency synthesizer is fabricated using the Global Foundries 1P6M 0.18 μ m CMOS process. On-wafer measurements are carried out using an 8 inch RF probe station shown in Fig.7.13. The input 1 MHz reference square wave signal for the measurement is provided by the Agilent 33120A arbitrary signal generator and the output signals are captured by the Lecroy Wave master 8600A 6G oscilloscope. The output spectrum and phase noise of the frequency synthesizer is measured using the Agilent E4407B 9 kHz-26.5 GHz spectrum analyzer.

Fig.7.14 shows the die photograph of the implemented 2.4 GHz Design-I frequency

synthesizer.



Figure. 7.13 Bench setup

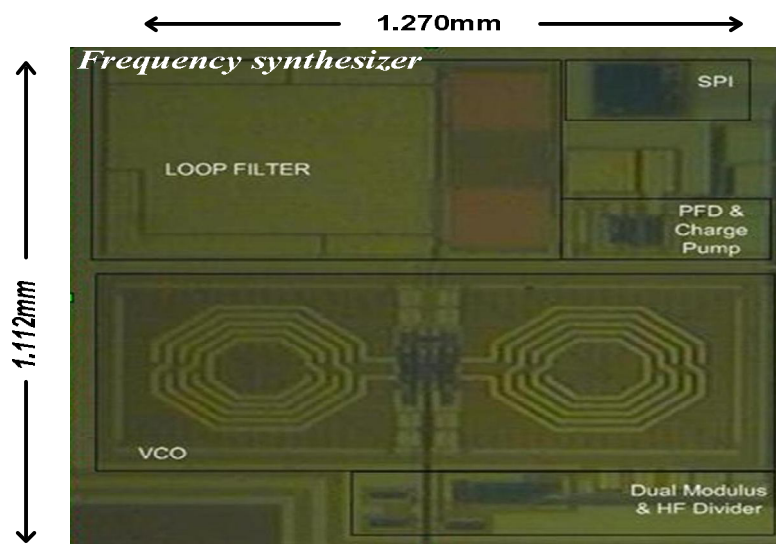


Figure. 7.14 Die photograph of the Design-I frequency synthesizer

Fig.7.15 shows the PLL synthesizer output spectrum. The VCO tuning range is from 2.2 GHz-2.5 GHz (300 MHz). The output amplitude captured by the Lecroy digital oscilloscope is around 300 mV as shown in Fig.7.16. The phase difference between I/Q signals is measured directly by the digital oscilloscope, which is 90.13°. The power consumption of S-QVCO is 2.9 mW and the power consumption of the divider,

charge pump and PFD is around 2 mW at 1.8 V power supply. Fig.7.17 shows the 1 MHz output from the Design-I fully programmable divider whose duty cycle is around 25%. The phase noise of the PLL is -111.4dBc/Hz at 1 MHz offset as shown in Fig.7.18. The reference spurs are -43 dB below the carrier.

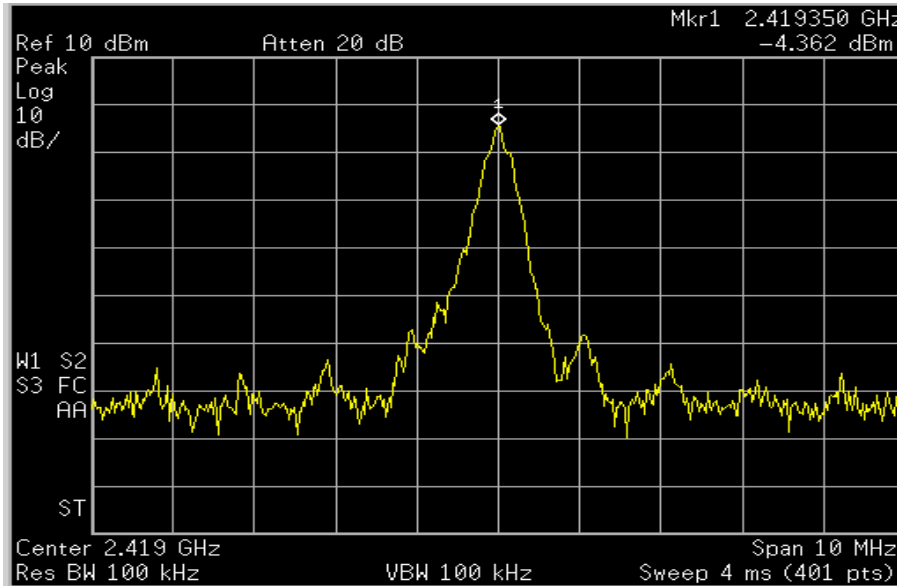


Figure. 7.15 Design-I PLL synthesizer output spectrum

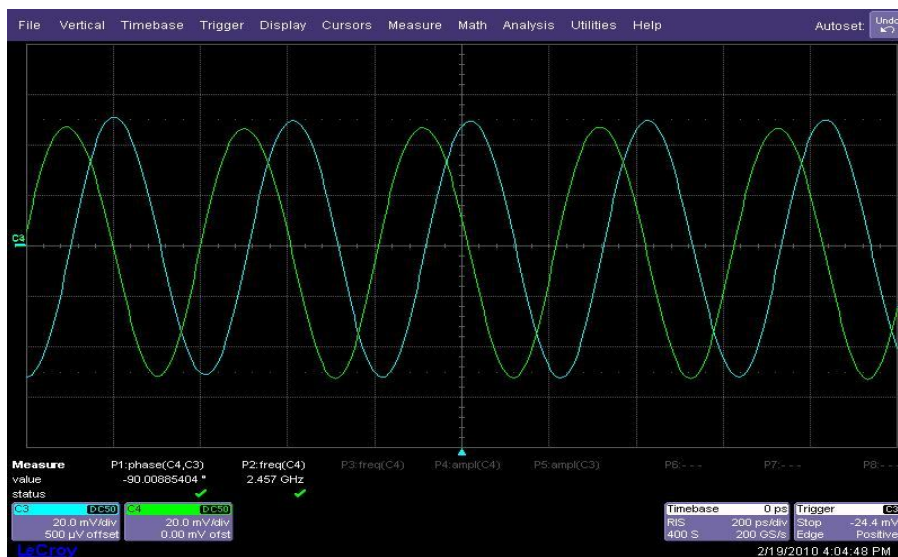


Figure.7.16 Measured I/Q signal at PLL output



Fig. 7.17 Measured 1 MHz output of the Design-I fully programmable divider

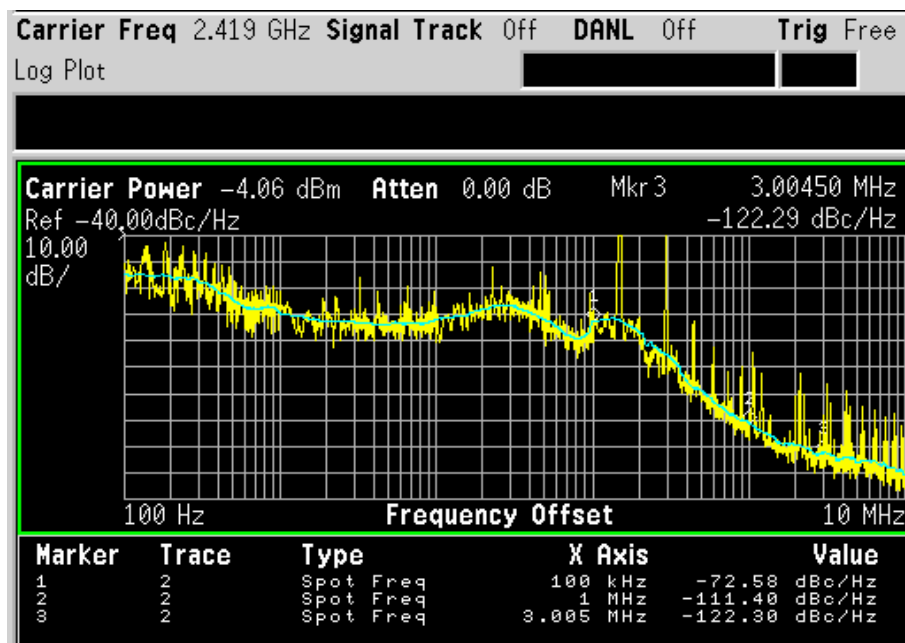


Fig. 7.18 Measured Phase noise of Design-I PLL synthesizer

7.4. Implementation of 1.5-V, 2.4 GHz Frequency synthesizer: Design-II

The implemented Design-II 1.5-V low power fully integrated 2.4 GHz PLL frequency synthesizer is shown in Fig.7.19. The synthesizer consists of a phase-frequency detector (PFD), the proposed low-spur gain boosting charge pump (CP), and a low power VCO using a tail noise suppression technique, a 3rd order loop filter and the

proposed ultra-low power fully programmable 1 MHz resolution divider discussed in the Chapter 4. The proposed programmable divider consists of a 47/48 dual modulus prescaler implemented using proposed ultra-low power Design-II TSPC 2/3 prescaler [73], a 6-bit S-counter and a 6-bit P-counter. Here the S-counter uses improved low power re-loadable bit-cell. The P-counter is programmable from 51 to 52 and S-counter is programmable from 0 to 47 in steps of 1 bit to accommodate division ratios from 2400 to 2483 in steps of 1. The low spur gain boosting charge pump implemented in this design of frequency synthesizer is discussed in the Chapter 6.

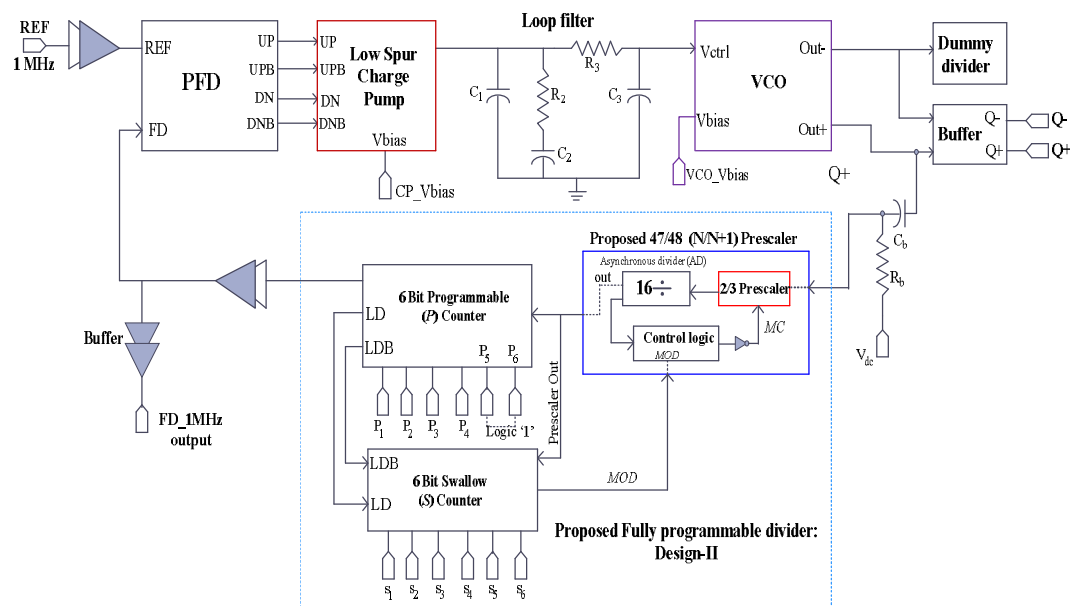


Fig. 7.19 Implemented 1.5-V 2.4 GHz PLL frequency synthesizer: Design-II

7.4.1. Circuit Implementation: Phase Frequency Detector (PFD)

The tri-state PFD implemented in this design [100] is shown in Fig.7.20. The flip-flop (FF) used in this design is a modified TSPC flip-flop. For the explanation of the FF

operation, consider the upper FF and when *Ref* and reset signals are low, node S_1 is connected to V_{DD} through M_1 , M_2 and charged to V_{DD} . At the rising edge of the *Ref* signal, output node Q_b is connected to ground through M_5 and M_6 . Once the node S_1 is charged to V_{DD} , the output node Q_b is not affected by input *Ref* signal. Because the charge at node S_1 turn-off M_5 and this prevents the output node from pulled up. Therefore, the output node is disconnected from the input node. When the reset signal is applied, node S_1 is disconnected from V_{DD} by M_2 and connected to ground by M_3 . As soon as the node S_1 is discharged, the output node is pulled up through M_4 .

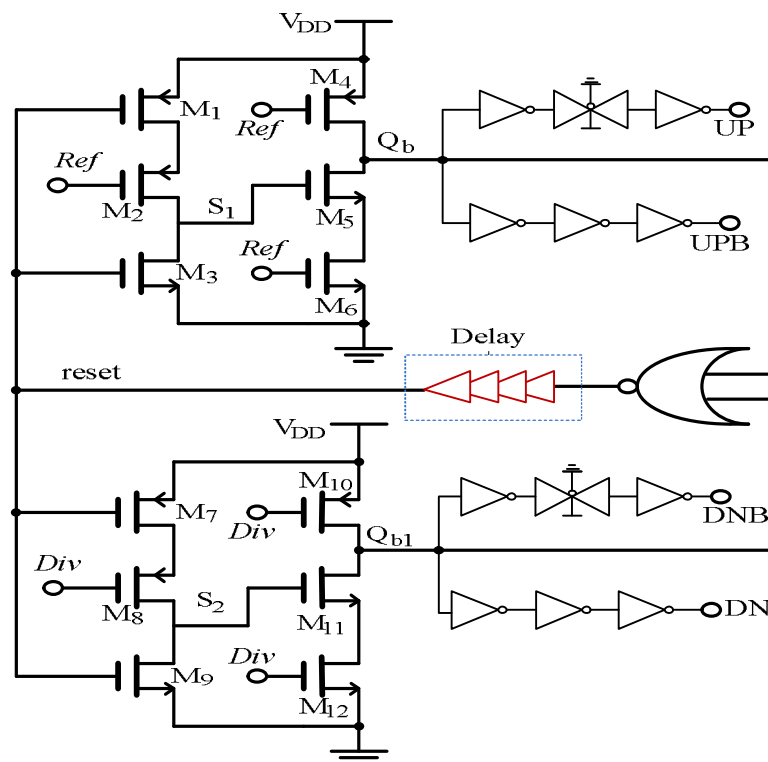


Fig. 7.20 Implemented tri-state high speed PFD

The PFD is simulated using Cadence Spectre with three different combinations: *Ref* leading *Div*, *Ref* lagging *Div*, and the *Ref* and *Div* having same frequency and phase.

Fig.7.21, Fig.7.22 and Fig.7.23 shows the corresponding simulation results. The PFD consumes draws a current of $12 \mu\text{A}$ from 1.5-V power supply.

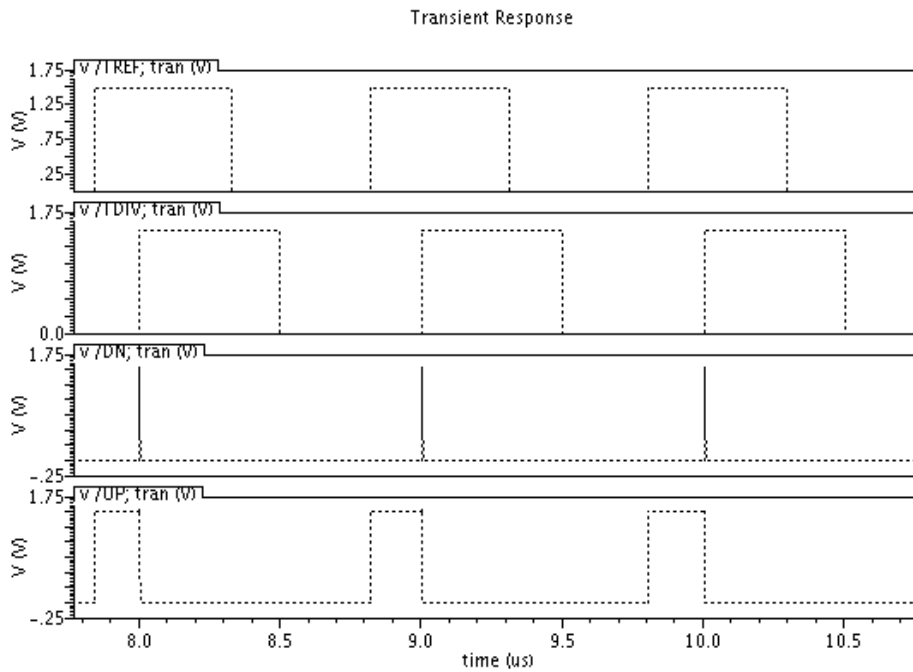


Fig. 7.21 Reference signal is leading frequency divider output (*Ref>Div*)

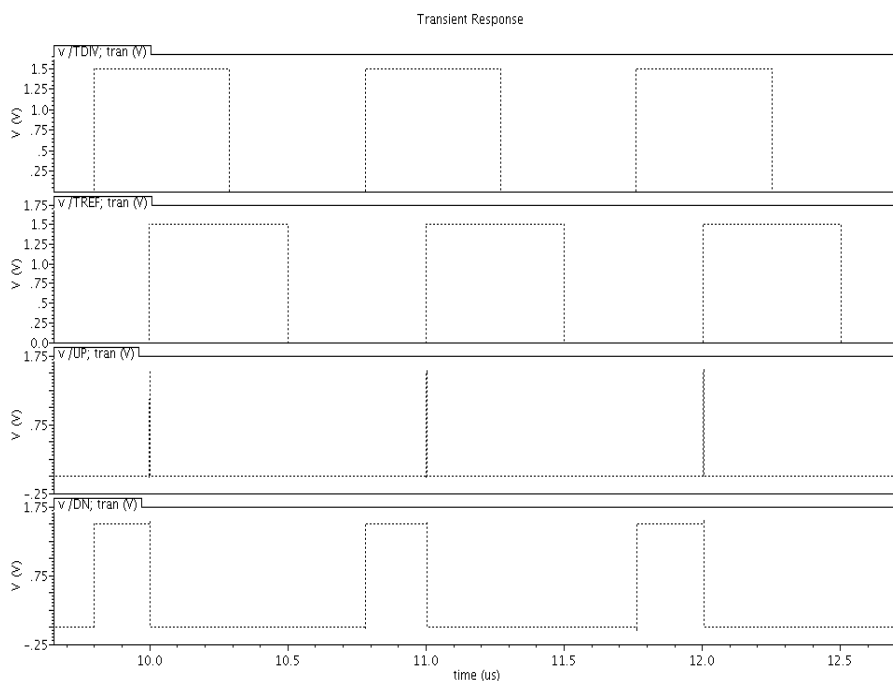


Fig. 7.22 Reference signal is lagging frequency divider output (*Ref<Div*)

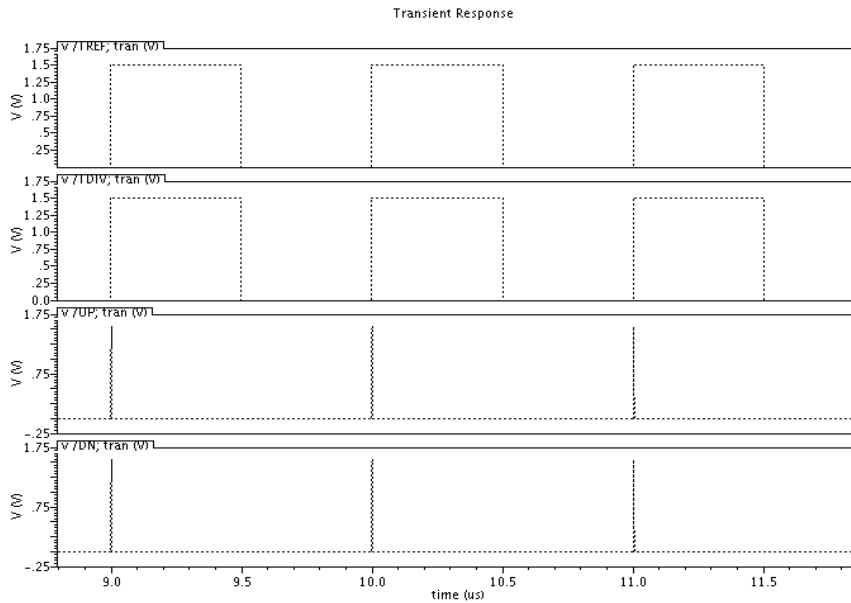


Fig. 7.23 Reference signal is same as frequency divider output ($Ref=Div$)

7.4.2. Circuit Implementation: Low power VCO

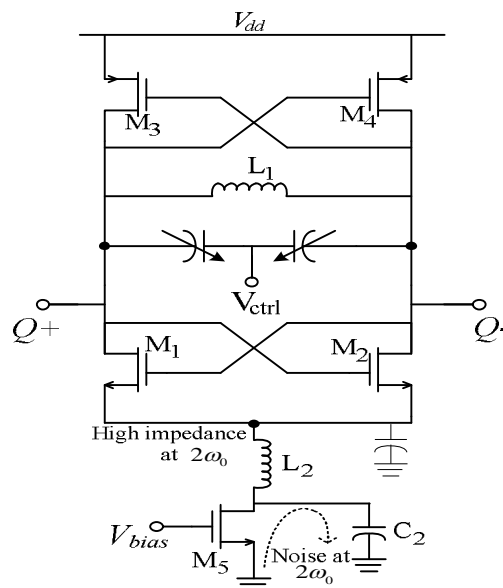


Fig. 7.24 Implemented LC VCO with tail noise suppression

Fig.7.24 shows the schematic of the LC VCO where an inductor is added between tail transistors M_5 and switching transistors M_1 - M_2 to remove the $2\omega_0$ component.

Fig.7.25 shows the layout of the implemented LC VCO in Global Foundries $0.18 \mu m$ RF CMOS technology.

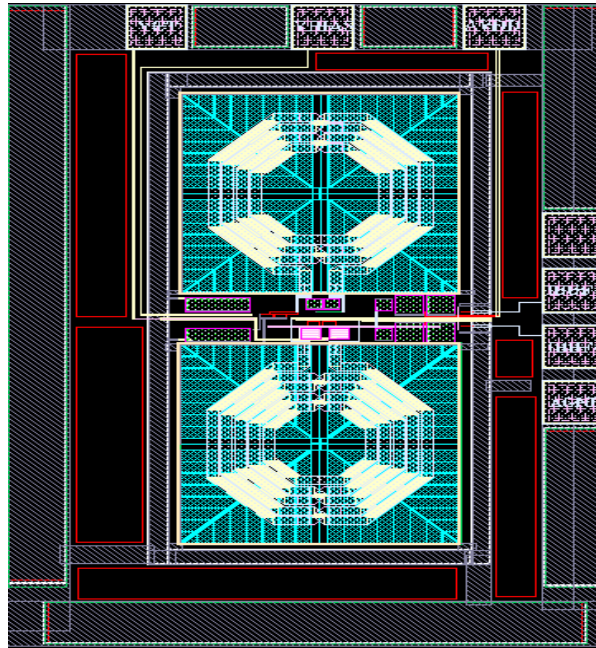


Fig. 7.25 Layout of implemented LC VCO

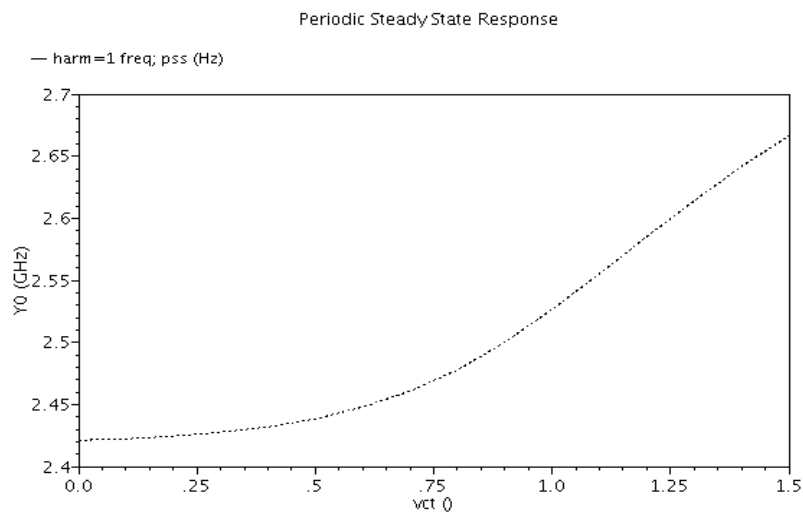


Fig. 7.26 Tuning range of implemented LC-VCO

The simulations are performed using Cadence RF Spectre at a supply voltage of 1.5 V.

Fig.7.26 shows the tuning range of the VCO which is around 240 MHz. The

amplitude of the VCO output signal is around 750 mV. The phase noise is

-100.48dBc/Hz, -121.16dBc/Hz at 100 KHz and 1 MHz offset respectively as shown

in Fig.7.27.

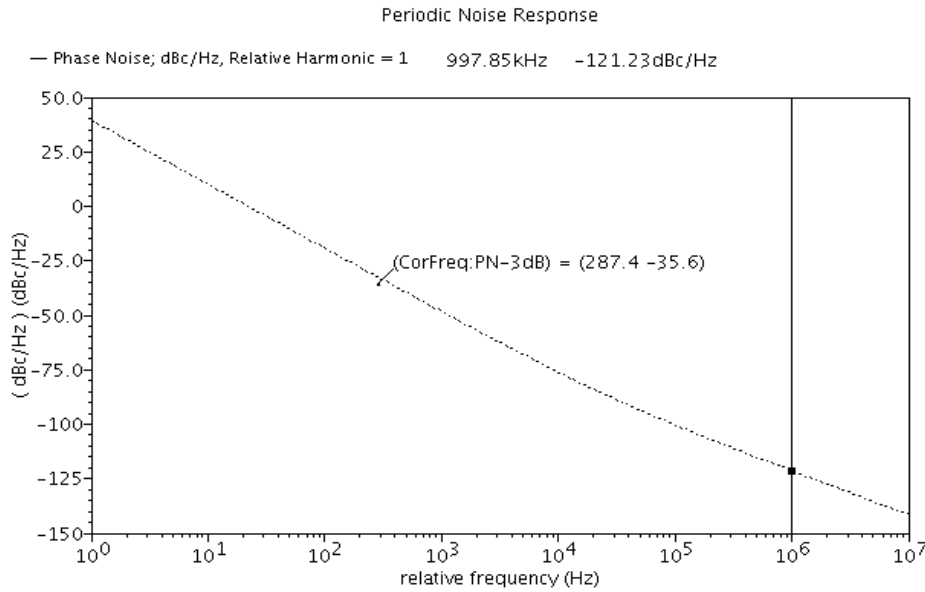


Fig. 7.27 Phase Noise performance of the implemented LC VCO

7.4.3. Design of Loop filter

The loop filter used in this design is 3rd order as shown in Fig. 7.8. Initially a 2nd order filter is designed and later a RC low-pass section is added to improve the spurs and reduce the ripples on control voltage. The reference frequency used in this design is 1 MHz. The 2nd order filter is assumed to be a critically damped with a loop bandwidth (f_c) of 45 KHz (satisfy the Gardner's stability criterion [21]), a charge pump current of 100 μ A (I_{cp}) and a VCO gain (K_{vco}) of 160 MHz/V. This loop filter design is different to the loop filter design presented in section 7.2.3. In this designed, the phase margin and the location of the poles and zeros are calculated based on the damping factor and loop bandwidth. The detailed design of the 3rd order filter is given below.

The damping factor in (2.33) can be further simplified as

$$\xi = \frac{T_2}{2} \sqrt{\frac{K_{vco} I_{cp}}{2\pi N(C_1 + C_2)}} \quad (7.1)$$

The phase margin in (2.34) can be further simplified as

$$\phi_m(\omega) = \tan^{-1}(\omega T_2) - \tan^{-1}(\omega T_1) + 180^\circ \quad (7.2)$$

Unity gain cross over frequency ω_c is found by differentiating (7.2) and equating it to the zero as given below [101]:

$$\frac{\partial(\phi(\omega))}{\partial\omega} = \frac{T_2}{1 + (\omega T_2)^2} - \frac{T_1}{1 + (\omega T_1)^2} \quad (7.3)$$

$$\frac{\partial(\phi(\omega))}{\partial\omega} \Big|_{\omega=\omega_c} = 0 \quad (7.4)$$

$$\omega_c = \frac{1}{\sqrt{T_2 T_1}} \quad (7.5)$$

The open loop transfer function in (2.26) can be re-written as

$$H_{ol}(s) = \frac{K_{vco} \times I_{cp}}{s^2 \times 2\pi \times N \times C_1} \times \left(\frac{1 + sT_2}{1 + sT_1} \right) \times \left(\frac{T_1}{T_2} \right) \quad (7.6)$$

For loop stability, the phase margin is maximum when the magnitude of the open loop gain is equal to unity. Equating (7.6) to unity gives us the following:

$$\left| \frac{K_{vco} \times I_{cp}}{(j\omega_c)^2 \times 2\pi \times N \times C_1} \times \left(\frac{1 + (j\omega_c)T_2}{1 + (j\omega_c)T_1} \right) \times \left(\frac{T_1}{T_2} \right) \right| = 1 \quad (7.7)$$

$$C_1 = \frac{K_{vco} \times I_{cp}}{(\omega_c)^2 \times 2\pi \times N \times C_1} \times \left(\frac{T_1}{T_2} \right) \times \frac{\sqrt{1 + (\omega_c T_2)^2}}{\sqrt{1 + (\omega_c T_1)^2}} \quad (7.8)$$

We know that,

$$C_1 + C_2 = \left(\frac{T_2}{T_1}\right) \times C_1 \quad (7.9)$$

By substituting (7.8) in to (7.9), we get the following:

$$C_1 + C_2 = \frac{K_{vco} \times I_{cp}}{(\omega_c)^2 \times 2\pi \times N \times C_1} \times \frac{\sqrt{1 + (\omega_c T_2)^2}}{\sqrt{1 + (\omega_c T_1)^2}} \quad (7.10)$$

By simplifying (2.32) and comparing (7.11) with (7.10), we get the following:

$$C_1 + C_2 = \frac{K_{vco} I_{cp}}{2\pi N \omega_n^2} \quad (7.11)$$

$$\frac{K_{vco} I_{cp}}{2\pi N \omega_n^2} = \frac{K_{vco} \times I_{cp}}{(\omega_c)^2 \times 2\pi \times N \times C_1} \times \frac{\sqrt{1 + (\omega_c T_2)^2}}{\sqrt{1 + (\omega_c T_1)^2}} \quad (7.12)$$

$$\frac{\omega_c^2}{\omega_n^2} = \frac{\sqrt{1 + (\omega_c T_2)^2}}{\sqrt{1 + (\omega_c T_1)^2}} \quad (7.13)$$

From (2.32) and (7.1)

$$T_2 = \frac{2\xi}{\omega_n} \quad (7.14)$$

$$T_1 = \frac{1}{\omega_c^2 T_2} = \frac{\omega_n}{(\omega_c)^2 \times 2\xi} \quad (7.15)$$

Re-writing (7.13) using (7.14) and (7.15) gives us the following:

$$\frac{\omega_c^4}{\omega_n^4} = \frac{1 + (\omega_c \times \frac{2\xi}{\omega_n})^2}{1 + (\omega_c \times \frac{\omega_n}{\omega_c^2 2\xi})^2} \quad (7.16)$$

$$\omega_c = 2\xi\omega_n \quad (7.17)$$

For a critically damped system $\xi = 1$, the cross over frequency (ω_c) is twice the natural frequency (ω_n) and the relation between pole, zero and cross over frequency is given by,

$$\frac{\omega_c}{\omega_{z1}} = 4 = \frac{\omega_{p1}}{\omega_c} \quad (7.18)$$

From (7.17) and (7.18), the zero (f_{z1}) and pole (f_{p1}) are placed at 11.25 KHz ($f_c/4$) and 180 KHz ($f_c \times 4$) respectively. With a natural frequency (f_n) of 22.5 KHz, average division ratio (N) of 2450, the values of R_2, C_2 and C_1 are calculated as follows:

$$C_2 = \frac{I_{cp} \times K_{vco}}{2\pi \times N \times \omega_n^2} = 261.6 pF \quad (7.19)$$

$$R_2 = \frac{1}{2\pi \times f_{z1} \times C_2} = 49.6 k\Omega \quad (7.20)$$

$$C_1 = \frac{C_2}{16} = 16.3 pF \quad (7.21)$$

The open loop PLL with a 2nd order loop filter is simulated in Matlab and Fig.7.28 shows the root locus plot of the open loop PLL. Fig.7.29 shows the simulated Bode diagram of the open loop PLL where the phase margin is around 62°. Fig.7.30 shows the open loop gain and phase margin.

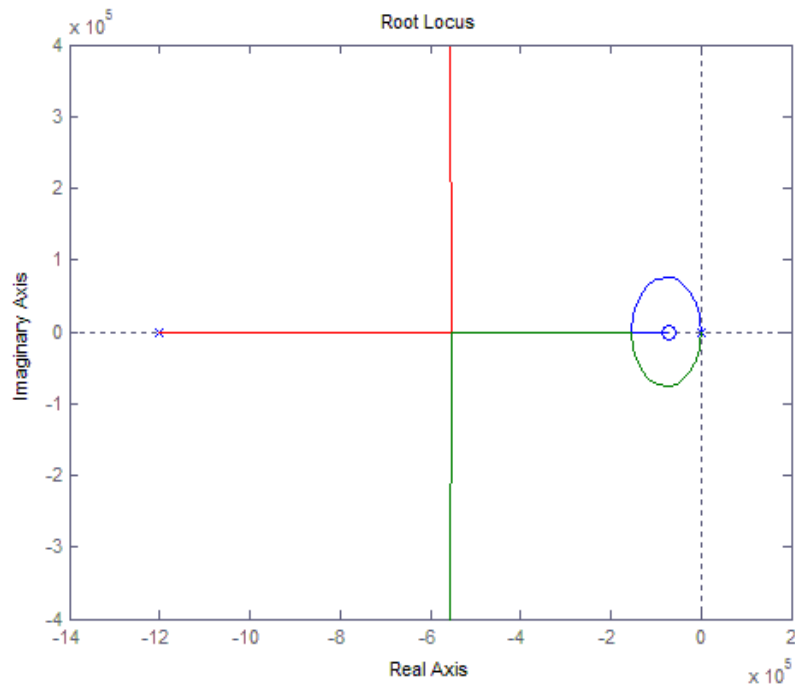


Fig. 7.28 Root locus of open loop PLL with 2nd order filter

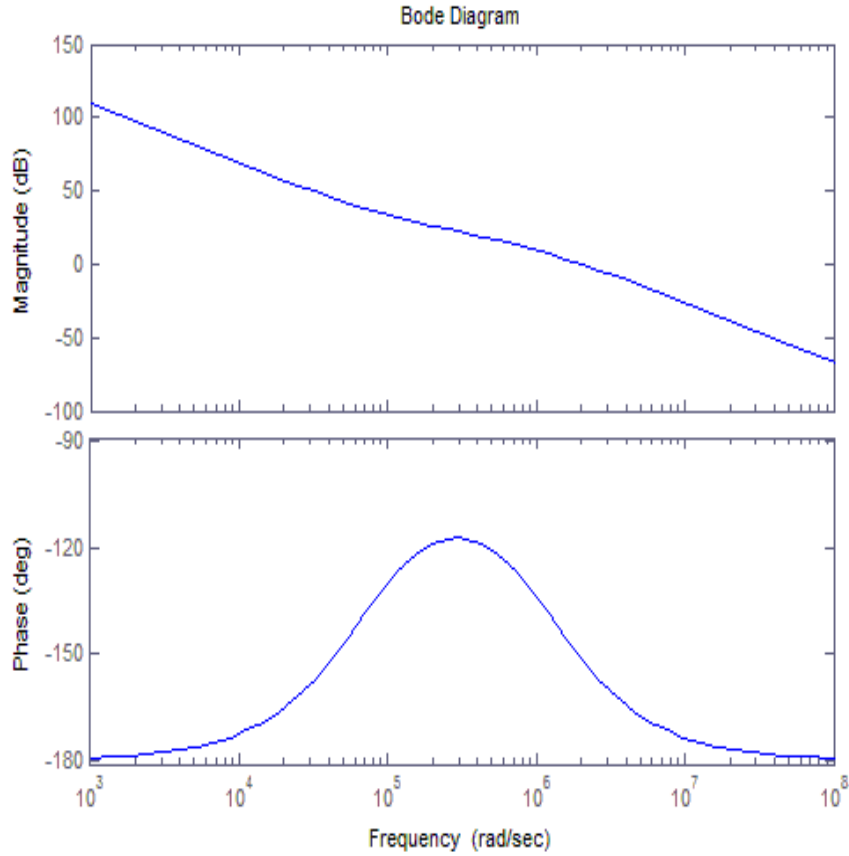


Fig. 7.29 Bode plot with 2nd order filter

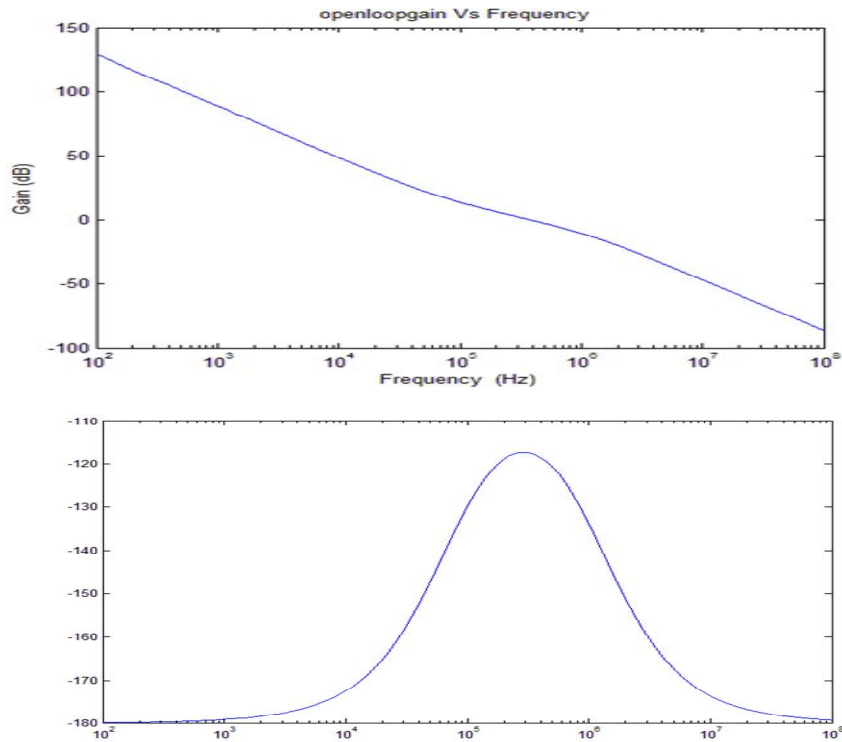


Fig. 7.30 Open loop gain and phase margin of Design-II PLL

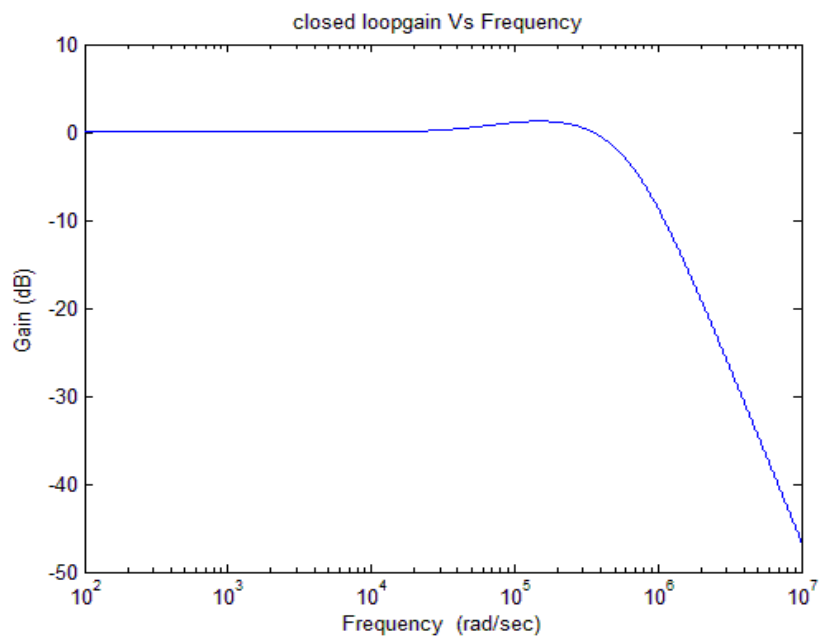


Fig. 7.31 Closed loop gain of Design-II PLL

Fig.7.31 and Fig.7.32 shows the closed loop gain and step response of the PLL. The additional RC low pass section added to the 2nd order filter such that the phase margin won't reduce to lesser value than 55 degrees.

$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p1}}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) \quad (7.22)$$

$$\phi_m = 62^\circ - \tan^{-1}\left(\frac{\omega_c}{\omega_{p2}}\right) = 55^\circ \quad (7.23)$$

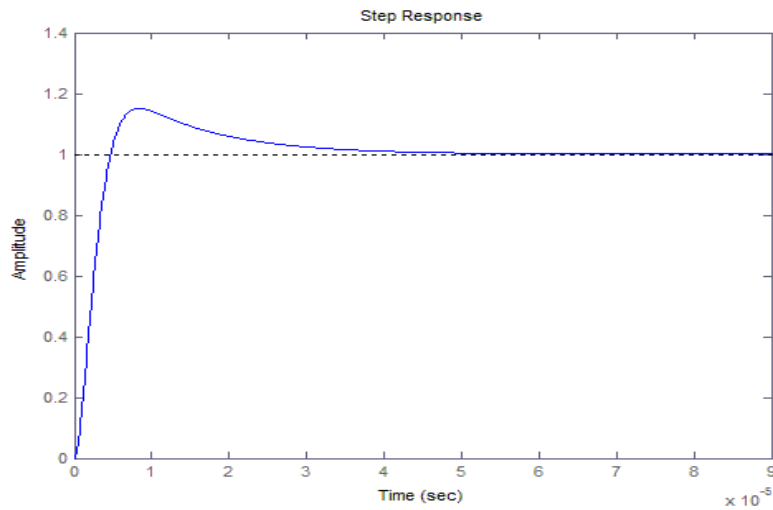


Fig. 7.32 Step response of Design-II PLL

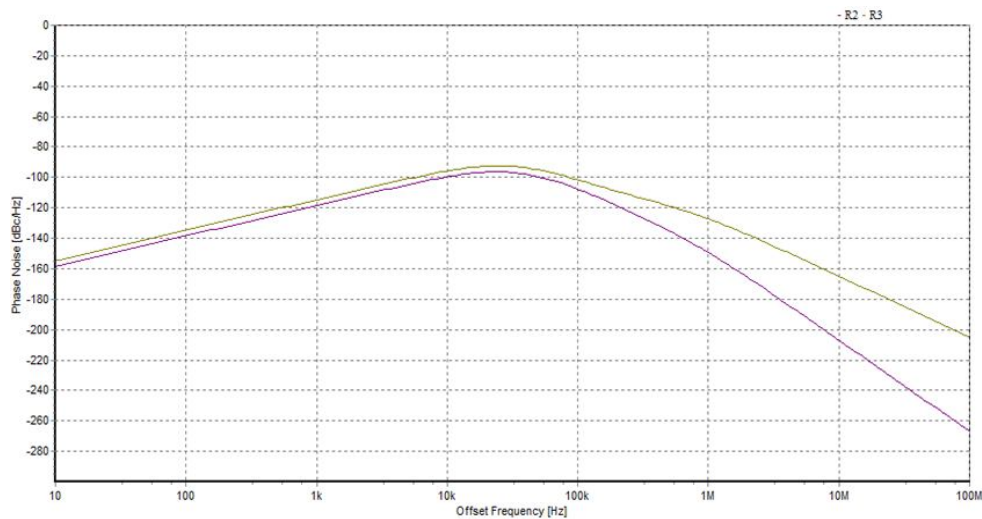


Fig. 7.33 Phase noise of loop filter resistors

The value of R_3 is kept same as R_3 for better layout matching. From (7.23), the values of R_3 and C_3 are found to be 49.6 K Ω and 9.72 pF respectively. With additional RC section, damping factor reduces to slightly lesser value than 1. Fig.7.33

shows the phase noise performance of loop filter resistors. With frequency accuracy of 40 ppm, the calculated settling time is $47.4 \mu\text{s}$, which is nearly four times less than the required settling time for IEEE 802.15.4 standard ($192 \mu\text{s}$).

7.5. Measured and Simulation Results: Design-II Frequency Synthesizer

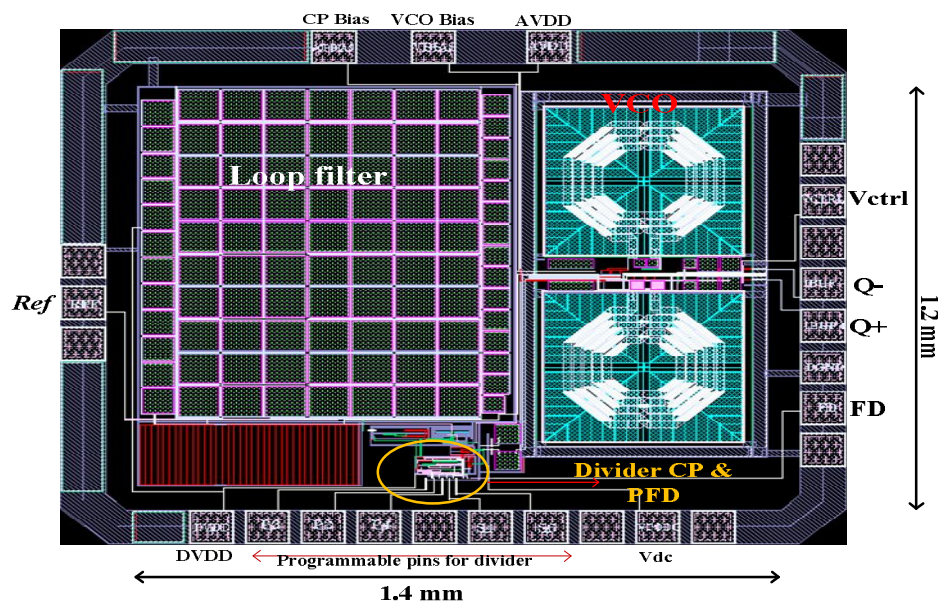


Fig. 7.34 Layout of design-II synthesizer with testing pads

For silicon verification, the fully programmable low power 2.4 GHz frequency synthesizer is fabricated using the Global Foundries 1P6M $0.18 \mu\text{m}$ CMOS process.

Fig.7.34 shows the layout of frequency synthesizer with testing pads for on-wafer testing. The synthesizer occupies an area of $1.4 \times 1.2 \text{ mm}^2$ with testing pads and the core area is $0.95 \times 1.0 \text{ mm}^2$. The simulations are performed using Cadence SPECTRE RF for a $0.18 \mu\text{m}$ CMOS process. The settling time for the synthesizer is around $72 \mu\text{s}$ which is nearly 3 times smaller than the value required by IEEE 802.15.4 standard.

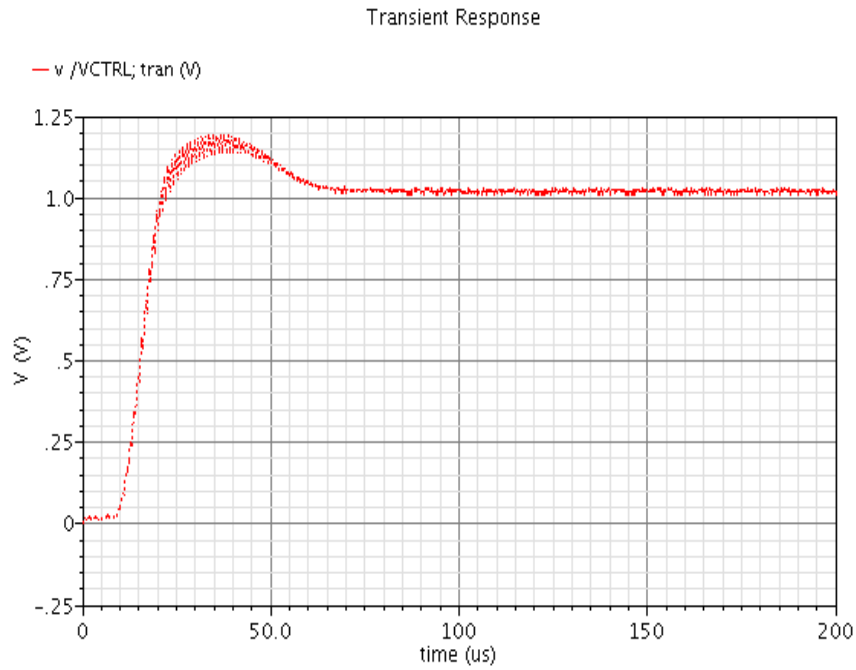


Fig. 7.35 settling behavior of Design-II PLL synthesizer

Fig.7.35 shows the settling behavior of the synthesizer for fixed channel. The VCO tuning range is from 2.42 GHz-2.66 GHz (323 MHz) and output amplitude is around 800 mV as shown in Fig.7.36. The power consumption of VCO is 0.94 mW.

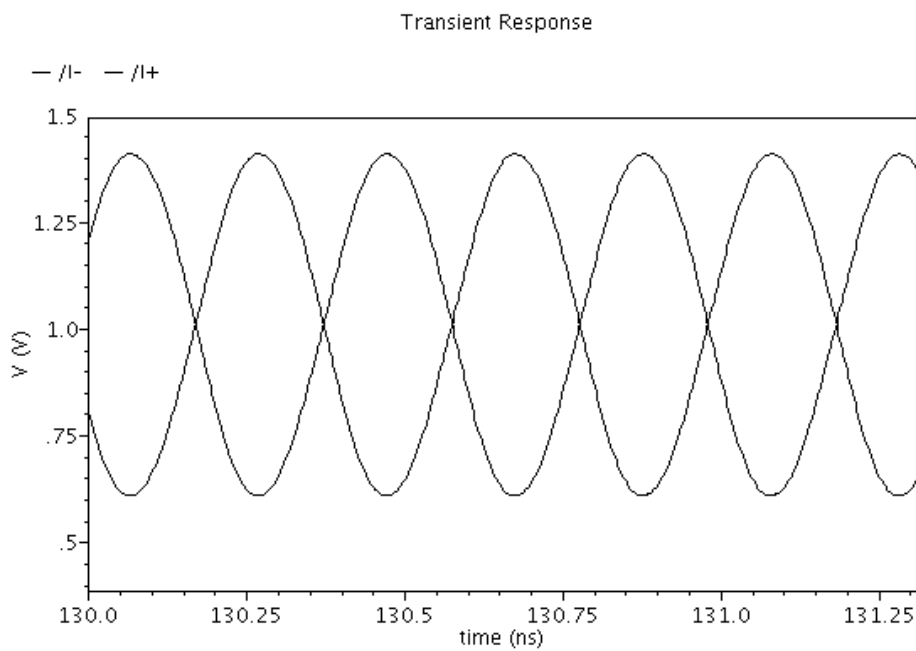


Fig. 7.36 Output waveform of implemented LC-VCO

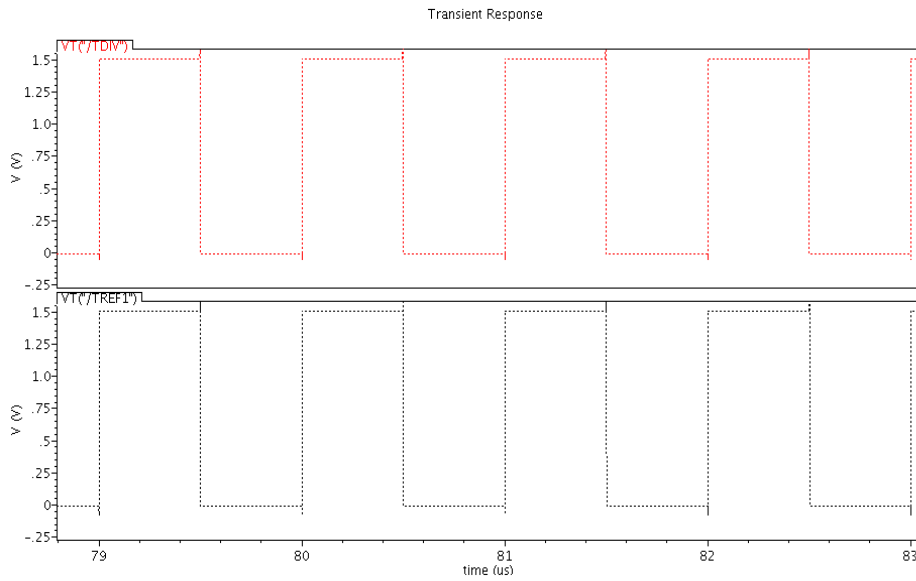


Fig. 7.37 Phase and frequency of *Ref* and *Div* signals under locked condition

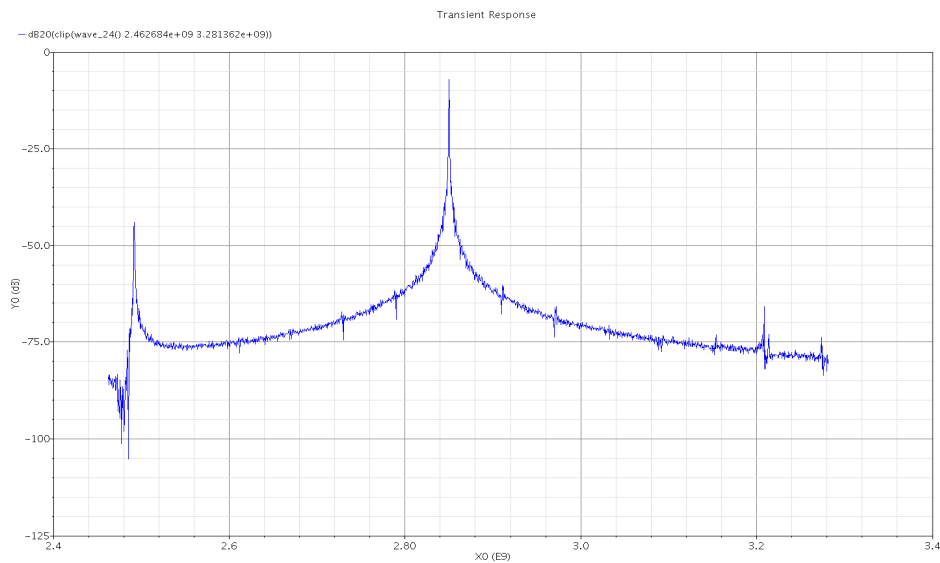


Fig. 7.38 Simulated output spectrum of the synthesizer

The ripples on the control voltage is less than 0.5 mV and power consumption of divider, charge pump and other blocks is around 0.7 mW. The duty cycle of 1 MHz output from the fully programmable is around 43% is discussed in Chapter.4. The simulated output spectrum of the frequency synthesizer in a locked state is given in Fig.7.38.

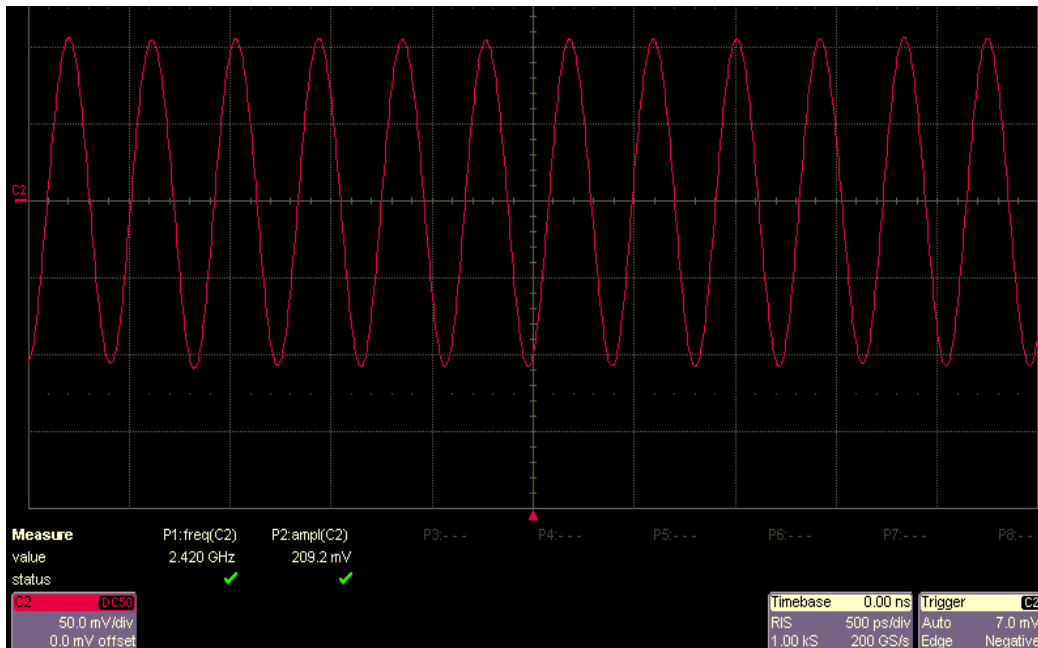


Fig. 7.39 Measured output waveform of low power VCO

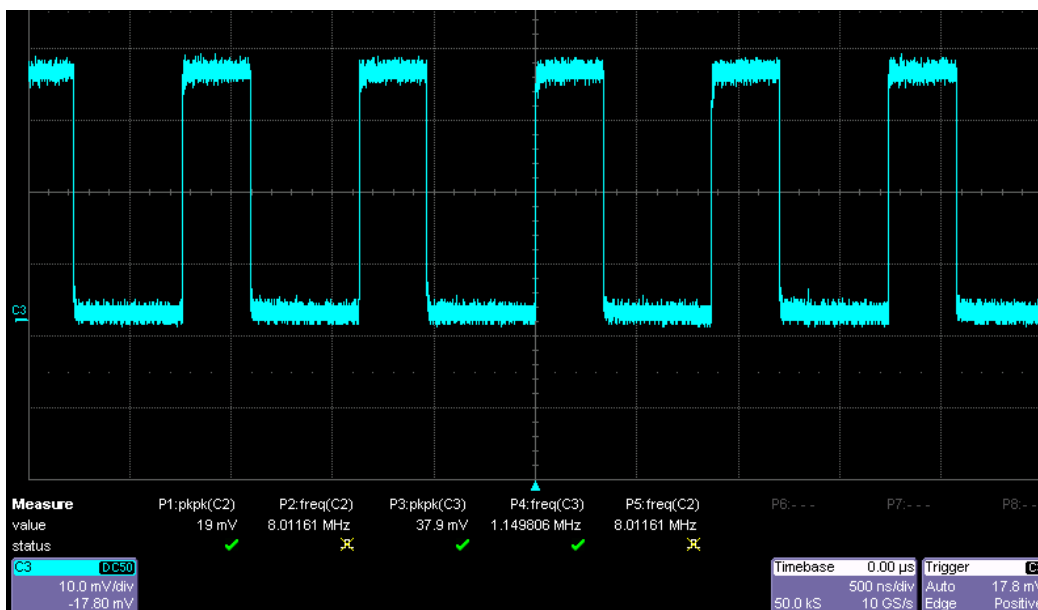


Fig. 7.40 Measured output of 1 MHz resolution programmable divider

On-wafer measurements are carried out using an 8 inch RF probe station shown in Fig.7.13. Fig.7.39 and Fig.7.40 show the measured output waveforms of the low power VCO and 1 MHz resolution divider at 1.5 V power supply. Fig. 7.41 shows the measured output spectrum of the PLL. The measured VCO tuning range is

2.29-2.495 GHz. The measured phase noise of the Design-II PLL is -111.72dBc/Hz at 1 MHz offset as shown in Fig. 7.42.

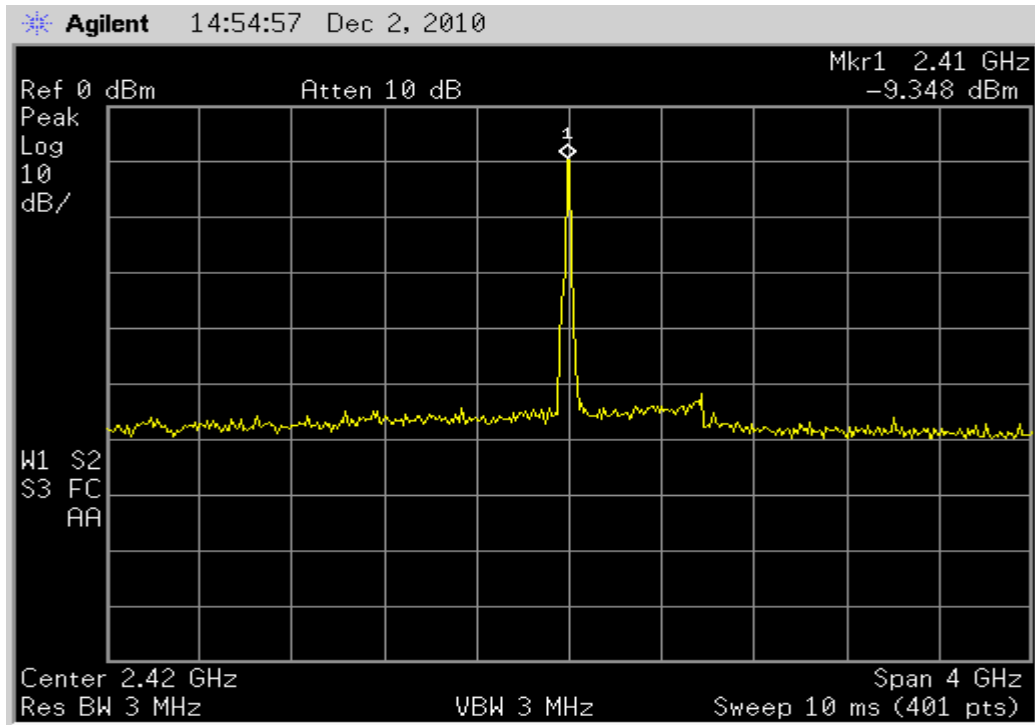


Fig. 7.41 Measured output spectrum of the Design-II PLL

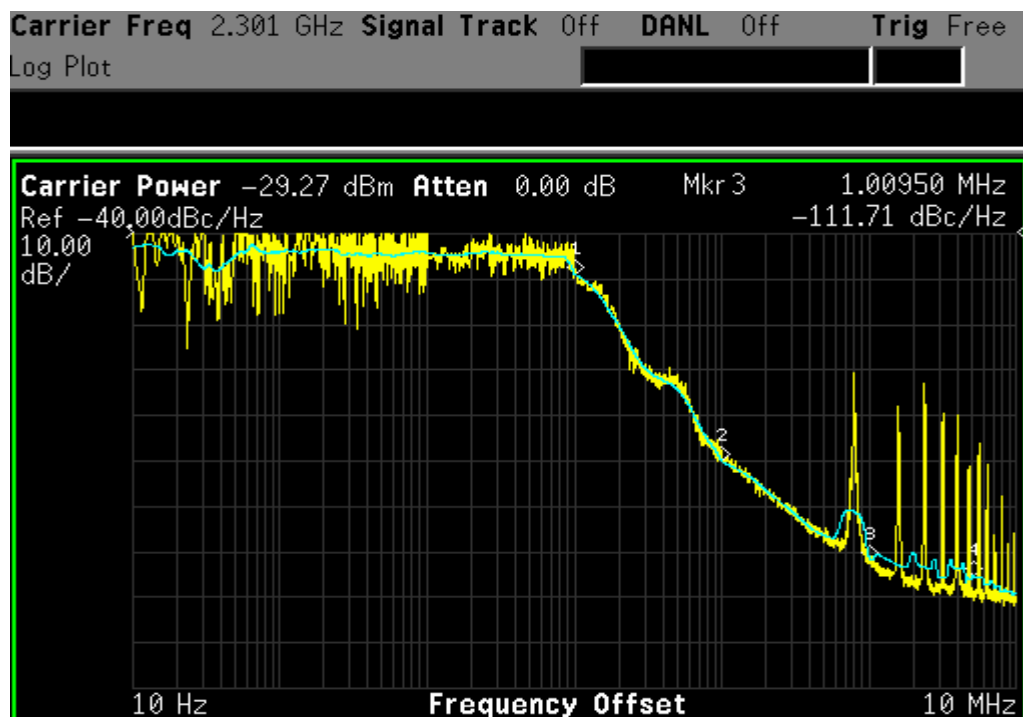


Fig. 7.42 Measured Phase noise of the Design-II PLL

The proposed low power 2.4 GHz synthesizer consumes a power of 1.8 mW from a power supply of 1.5 V. The performance of the implemented low power 2.4 GHz frequency synthesizers (Design-I and Design-II) are analyzed with 2.4 GHz synthesizers reported in literature in Table 7.4.

Table.7.4 Synthesizer performance comparison

Reference	[37]	[39]	[40]	[10]	Design-I (Measured)	Design-II (Measured)
Process	0.18 μ m	0.25 μ m	0.18 μ m	0.18 μ m	0.18 μ m	0.18 μ m
Channel spacing	5 MHz	1 MHz	5 MHz	5 MHz	1 MHz	1 MHz
Frequency Range (GHz)	2.4-2.48	2.4-2.527	2.4-2.475	2.29-2.64	2.2-2.5	2.29-2.495
Loop filter	On- chip	On- chip	Off- chip	On- chip	On- chip	On- chip
Phase noise (dBc/Hz)	-108.55 @1 MHz	-112 @1 MHz	-116.5 @1 MHz	-130 @10MHz	-111.4 @1MHz	-111.7 @1MHz
Settling time	25 us	60 us	120 us	55 us	35us	72 us
Power consumption	7.95 mW at 1.8V	20 mW at 2.5V	4.2 mW at 1.2V	15 mW at 3 V, 1.8 V	4.9 mW at 1.8V	1.8 mW at 1.5V

7.6. Summary

In this Chapter, we have presented the integration of building blocks. The Design-I frequency synthesizer is implemented in RF CMOS 0.18 μ m technology at 1.8-V power supply using conventional programmable divider discussed in the Chapter.4

and a series Q-VCO. The synthesizer consumes 4.9 mW of power and has a phase noise of -111.4dBc/Hz at 1 MHz offset. The Design-II frequency synthesizer is implemented in RF CMOS 0.18 μ m technology at 1.5-V power supply using proposed low power building blocks such as low power 2/3 prescaler, 47/48 prescaler, low spur gain boosting charge pump and low power VCO with tail noise suppressing technique. The synthesizer consumes 1.8 mW of power from on-wafer measurement results.

CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1. Introduction

This research focuses on the design techniques of low power frequency dividers and PLL frequency synthesizer. Using the theory and circuits developed, a 2.4 GHz fully integrated and fully programmable frequency synthesizer prototype is designed in Global Foundries (GF) 0.18 μ m CMOS technology. Efforts have been put on the new design of low power prescaler, wide band prescaler, reloadable DFF, low spur charge pump and low power VCO.

In Chapter 2, we review the fundamentals of a phase-locked loop and perform a literature survey on the 2.4 GHz PLL synthesizer's performance. Firstly, the performance impacts caused by the phase noise and spurious tone are studied, and the dynamics of type-I and type-II PLLs are introduced. Secondly, the operation of each individual blocks in the PLL are explained and the existing phase noise models are summarized. Finally, the specifications of the frequency synthesizer are derived under the IEEE 802.15.4 standards.

In Chapter 3, a detailed study of different kind of divider topologies is given and the propagation speed and power consumption of dynamic logic dividers such as TSPC and E-TSPC circuits are investigated. Based on this study, a new low

power and improved speed TSPC 2/3 prescaler is proposed and verified on silicon in the design of a 32/33 prescaler on silicon. Compared with the existing TSPC architectures, the proposed 2/3 prescaler is capable of operating up to 5 GHz and ideally, a 67 % reduction of power consumption is achieved when compared under the same technology at supply voltage of 1.8-V. The extremely low power consumption is achieved by radically decreasing the sizes of transistors, reducing the number of switching stages, and blocking the supply to one of the DFF's during the divide-by-2 mode of operation. The implemented 32/33 prescaler in the GF 0.18 μ m CMOS technology is capable of operating up to 4.5 GHz with a power consumption of 1.4-mW.

In Chapter 4, a fully programmable divider with 1 MHz resolution is presented using 32/33 prescaler, a 7-bit P-counter and a 5-bit S-counter. This divider suffers from low output duty cycle of 25% mainly due to the large difference between P and S values. To overcome the low duty cycle problem, a low power TSPC 47/48 is proposed whose maximum operating speed is 4.8 GHz with power consumption of 0.48 mW at a supply voltage of 1.8-V. An improved reloadable DFF is implemented in the design of S-counter which reduces the switching power of S-counter during its idle state. A new fully programmable divider using the proposed 47/48 prescaler, a 6-bit P-counter and a 6-bit S-counter are implemented in the GF

0.18 μ m CMOS technology. The divider consumes a power of 0.62 mW at 1.8-V power supply and the duty cycle of the output 1 MHz signal is close to 47 %.

In Chapter 5, the switching and short-circuit power consumption and the operating frequency of the E-TSPC based 2/3 prescaler are investigated. Based on this analysis, a new ultra-low power wide band 2/3 prescaler is proposed and implemented using GF 0.18 μ m CMOS technology. Compared with the existing E-TSPC architectures, the proposed 2/3 prescaler is capable of operating up to 6.5 GHz and eliminates the switching and short circuit power of the first DFF during the divide-by-2 mode of operation and also the short-circuit power consumption in the first stage of second DFF. The prescaler consumes a power of 1 mW and 1.8 mW during the divide-by-2 and divide-by-3 modes respectively. With the help of proposed 2/3 prescaler, a low power multi-band flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g frequency synthesizers is implemented using GF 0.18 μ m CMOS technology. The flexible divider consumes power of 0.96 mW and 2.2 mW in 2.4 GHz and 5 GHz bands respectively, when operated at 1.8-V power supply.

In Chapter 6, the design of a low spur charge pump and low power VCO is presented. Firstly, the mismatches in the charge pump due to leakage current and mismatch currents are analyzed. Based on this analysis, a low spur charge pump using gain boosting technique is proposed and implemented. Secondly, the design of

low power VCO using tail noise suppression technique is presented. The post layout simulation results show that the phase noise of the VCO with filtering technique improves and is about -100.48 dBc/Hz, -121.96dBc/Hz at 100 KHz and 1 MHz offset. The VCO consumes a power of 1 mW at 1.5-V power supply.

In Chapter 7, we have demonstrated a design of two fully integrated and fully programmable monolithic CMOS 2.4 GHz frequency synthesizers, which are designed for IEEE 802.15.4 applications. Firstly, a 1.8-V 2.4 GHz frequency synthesizer is implemented using low duty cycle fully programmable divider (Design-I) and a series Q-VCO in GF 0.18 μ m CMOS technology. The measured phase noise of the frequency synthesizer is -111.4dBc/Hz at 1 MHz offset. The PLL synthesizer consumes only 4.9 mW at 1.8-V power supply. Secondly, a 1.5-V low power 2.4 GHz frequency synthesizer is implemented using the proposed low power 2/3 prescaler, a low power 47/48 prescaler, a low spur charge pump and a low power VCO in GF 0.18 μ m CMOS technology. The measured phase noise of the frequency synthesizer is -111.7dBc/Hz at 1 MHz offset. The 1.5-V frequency synthesizer consumes only 1.8 mW at 1.5-V power supply which is 2.7 times lesser than implemented 1.8-V frequency synthesizer.

8.2. Future work

The Design-I and Design-II PLL synthesizers are fabricated in Global Foundries 0.18 μ m technology and measured using 8 inch RF probe station. Major building blocks such as TSPC 2/3 prescaler, 47/48 prescaler, fully programmable divider and VCO are fabricated individually and the results are silicon verified. As discussed earlier, VCO and the first stage divider are the major power hungry blocks of the PLL frequency synthesizer. The 1.8-V frequency synthesizer consumes 4.9 mW and the divider consumes 1.7 mW, which is around 34.6 % of the total power consumption. The 1.5-V frequency synthesizer consumes 1.8 mW and the divider consumes 0.45 mW, which is around 26.4 % of the total power consumption.

In our proposed 2/3 prescaler, wide band 2/3 prescaler, 47/48 prescaler and the fully programmable divider, only the switching, short-circuit power and propagation speed are analyzed. We haven't performed noise analysis of these dividers as fully programmable divider noise contributes to the close-in phase noise of the PLL. The proposed dynamic dividers maximum operating frequency is limited below 8 GHz and in future more work has to be done in improving the maximum operating frequency at lower power levels in alternative technologies. The simulation results show that the implemented low spur charge pump improves spur levels due mismatch currents by 10 dB. However, measurement results are required to verify this.

In this research work we have successfully reduced the power consumption and improved the performance of the dividers. However, we have only partially succeeded in lowering the power consumption of the VCO. The phase noise performance of a frequency synthesizer depends greatly on the phase noise of the VCO. Reducing the power consumption by decreasing the bias current only degrades the phase noise performance and also the output amplitude. In this design, we have improved phase noise by minimizing the noise from the active devices and tail noise filtering technique at the cost of chip area. The substantial improvement in the phase noise can be achieved by implementing a resonant tank with a high Q. In future more work has to be done in order to provide a resonant tank with a high Q that can be easily integrated using a standard commercial process and the techniques for reducing $1/f$ noise should be properly analyzed.

In Chapter 5, we have implemented fully programmable multi-band flexible divider for Bluetooth, Zigbee, IEEE 802.15.4 and 802.11 a/b/g frequency synthesizers. However, implementing frequency synthesizer which covers 2.4 GHz ISM band and 5-6 GHz WLAN using multi-band divider is very challenging as it requires low power, low phase noise dual-band VCO. In future, more work has to be done in exploring better ways of implementing the low power dual-band VCO with better phase noise performance.

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