

0.77 fJ/bit/search Content Addressable Memory Using Small Match Line Swing and Automated Background Checking Scheme for Variation Tolerance

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Abstract

This work reports a fully parallel match-line (ML) structure with an automated background checking (ABC) scheme. MLs are pre-charged to an intermediate level by a pulsed current source to minimize power. The proposed ABC scheme uses two dummy rows for digitally adjusting the pulse width and the delay of the sense amplifier enable signals of the CAM without disturbing the normal operation. Therefore, it can continuously track the optimum ML swing, making the CAM tolerant to variations. The proposed ABC scheme achieves the power reduction of $5.5\times$ compared with the conventional ML sensing scheme. In addition, multi- V_t transistors are used in the CAM cell to reduce the leakage by $15\times$ while improving the ML discharging speed by $2\times$ when compared with the standard- V_t devices at

1.2V, 80 °C. A test chip was prototyped using a standard 65 nm CMOS process. The average energy consumption is 0.77 fJ/bit/search at 1.2V/500 MHz.

Keywords: CAM, small match line swing, match-line, variation tolerant design.

I. INTRODUCTION

Content Addressable Memory (CAM) is a special type of solid-state memory which is accessed by contents rather than physical locations. When an input word (i.e. search data) arrives, a new search operation starts by sending the search data to all locations available in the memory through a network of search lines (SLs and SLBs). Fig. 1 illustrates the conceptual view of a CAM array. Search and stored data are compared bit-by-bit simultaneously due to the comparison circuit built in every single bit cell. Thus, search operation can complete in a single clock cycle and return the location that stores the search data [1]. This attractive feature makes CAMs popular in hardware-based search engine implementations where throughput is the most important requirement [2-5]. CAMs have been widely employed in high-speed network routers [6, 7] where IP addresses of outgoing data packages are used to quickly allocate the index of the destination port. It is also widely used in look-up tables [8, 9], data compression and image processing [9-11]. However, their superior search speed comes at the cost of huge dynamic power consumption [11-13]. This is because of three main reasons: (i) rapidly growing memory capacity (more words stored in the memory and more bits per word) to catch up with the exploding internet traffic; (ii) non-stop increasing of the clock speed; (iii) high speed parallel search operation.

CAM cells can be broadly categorized into the NOR-type and the NAND-type. NAND-type architecture connects CAM cells in serial to create a long pass-transistor chain. In case of a match, all transistors in the chain are on to pass a voltage level from one end to the other. In case of a miss, at least one transistor is off and thus the signal from one end is not transferred to the other. Since only one or a few MLs are matched, signal transfer does not occur in most MLs, resulting in low power consumption. However, the search delay of NAND-type cells increases quadratically with the word length [13]. Thus, even though NAND-type cells are known to consume less power, NOR-type cells have gained higher popularity due to faster sensing speed and higher array compactness, especially at a longer word length [1]. In a NOR-type CAM, each ML is connected to one of the power supply rails (i.e. ground or VDD) through a network of parallel paths, each contributed by one single CAM cell. In a match case, all paths are turned off and thus the ML is isolated from the supply rail. In a mismatch case, ML voltage will follow the supply rail. A sense amplifier (SA) is required at each ML to quickly sense the change in the ML voltage so that the location of the match result is quickly identified.

Conceptual view of a NOR-type CAM is shown in Fig. 1. Each CAM is an array of $M \times N$ CAM cells where M is the depth of the memory and N is the length of each word. Cells on a row share a common match line (ML) which carries the search result. Each column has vertical SL and SLB to transfer the complementary data from the search word. Each row has a match line sense amplifier (SA) for quickly obtaining a search result and reducing power consumption. Each CAM cell normally consists of a 6T-SRAM and a comparison circuit. Fig. 2 (a-b) shows two widely used NOR-type topologies in the literature. The back-to-back inverters are the storage element of the SRAM. N1-N7 are comparison transistors. Similar to SRAMs, CAMs also have vertical BLs for writing and retrieving data, which is omitted in Fig. 1 for simplicity.

In the conventional CAM design, ML is precharged to V_{DD} prior to any search operation. Subsequently, search bits are broadcasted to the entire memory through SLs and SLBs. Search operation is performed within each CAM cell simultaneously. Assuming that the 10T cell in Fig. 2(a) stores data “1” (i.e. $Q = “1”$ and $QB = “0”$). When a miss happens (i.e. $SL = “0”$ and $SLB = “1”$), both M2 and M4 are fully on and sink a DC current to discharge ML. If it is a match (i.e. $Q = “1”$, $QB = “0”$, $SL = “1”$ and $SLB = “0”$), M1 and M4 are off and thus there is no discharge current. A row of cells is said to be matched if all cells on that row are matched and ML stays at V_{DD} . Otherwise, ML is discharged to ground. Note that PMOS comparison circuits can be used as well but with slightly lower sensing speed due to its weaker current drive capability.

Similarly, in the 9T cell design (Fig. 2(b)), if a miss happens (i.e. $Q = “1”$, $QB = “0”$, $SLB = “1”$ and $SL = “0”$), transistor N5 is on to charge node B up to $V_{DD}-V_{th}$. As a result, M7 is turned on and discharge ML to ground. Otherwise, ML is kept intact. Compared to the 10T design, the 9T offers less ML capacitance but larger SL capacitance. Furthermore, the capacitance and the rising delay of SLs and SLBs strongly depend on the data pattern of the column. This is because either N5 or N6 is on and charge sharing happens between SL/SLB and node B. In the worst case scenario, all cells in a column store the same data (e.g. $Q = ‘1’$ and $QB = ‘0’$). As a consequence, charge sharing happens between SLB and node B off all cells, leading to much slower SLB rising time (i.e. search for data ‘1’) when compare to SL rising time (i.e. search for data ‘0’). Fig. 2(c) shows the simulated SL/SLB rising delays of the 10T and the 9T NOR-type CAM cells, respectively. It can be seen that the best case of the 9T cell has a slightly longer delay when compared to the 10T cell. However, in the worst scenario, the SL/SLB rising delay of the 9T cell can be 60% slower. Therefore, we choose the 10T design to minimize the timing variation.

The rest of the paper is organized as follow: Section II discusses previous low-power CAMs. Details of the proposed low leakage CAM cell using multi- V_t transistors are discussed in Section III. Section IV explains the sensing scheme for small ML swing. The proposed automated background checking (ABC) scheme is introduced in Section V, followed by the simulated and measured performance of the prototype chip Section VI. Section VII concludes the paper.

II. PREVIOUS MATCH LINE SCHEMES FOR LOW POWER CAMS

Frequent switching activities of heavily loaded MLs and SLs lead to excessive power dissipation of high speed CAMs. Therefore, low power is the topmost concern in state-of-the-art CAM design. Improvement in ML sensing is by far the most effective way to lower the total energy consumption because it contributes 40% to 60% of the overall CAM power. From the architecture point of view, ML can be divided into multiple segments [14]. Sensing of a segment is activated only if its previous segment returns a match. Since most MLs are mismatched, majority of ML segments in an array will remain idle during search and hence save power. However, this approach requires additional area overhead and complicated wiring in the layout. To mitigate these drawbacks, the number of ML segments in many CAMs is set to two with only a few bits (e.g. $k=8$) in the first segment and the rest (i.e. $N-k$ bits) in the second segment. The result of the first segment will selectively activate the second segment in each ML. Statistically, only $1/2^k$ of the second ML segments are activated, saving significant amount of energy. This shows that the actual power saving depends on the input data pattern. Furthermore, the search delay is still largely determined by the second segment sensing, which is similar to the un-segmented ML. Therefore, circuit techniques for reducing search power and improving search speed are highly sought after to ensure superior CAM performance regardless of actual data patterns.

Various circuit techniques have been proposed [15-22] to lower the ML sensing power. Arvovski *et. al.* proposed a circuit technique to inject less current in a missed row and more current in a matched row [20]. Since most rows are missed, it saved a significant amount of power consumption. In [15], a capacitor is employed in each ML to limit the amount of charges per search transaction for energy reduction (Fig. 3(a)). This approach requires more area overhead due to the physical capacitor and suffers from row-to-row capacitor variations which have a negative impact on the sensibility of the latch-based comparator. Tyshchenko *et al.* injects a small current to each ML prior to the sensing phase which acts as an excitation charge to observe the stability of the R-C ML model (Fig. 3(b)) [16]. However, a level shifter required at each ML comparator makes its sensing speed inferior to that of the latch-based comparator. Besides, in addition to the initial charges, each ML consumes extra power depending on the sensing outcome. In [18], input data pattern to reduce the switching probability of the ML segments is exploited. Although this design reduces power consumption and sensing speed, it has a significant area overhead of the eleven NOR gates inserted in each ML structure (Fig. 3(c)). [19] proposed a self-reference sense amplifier that stops the ML charging (ML and SN nodes in Fig. 2-3 of Ref. [19]) around the threshold voltage of the output inverter. Subsequently, the voltage of these nodes will be developed depending on the match result. As they are pre-charged close to the trip point of the inverter, sensing output can be obtained quickly. However, this approach leaves the inputs to the two inverters of each SA around the switching threshold during sensing operation, which leads to significant direct current flowing from V_{DD} to ground. This situation is not desirable when multiple rows have a small number of misses or operating frequency is not at maximum, resulting in unwanted direct current during sensing period.

In view of that, we propose a power efficient ML sensing technique that achieves both low power consumption and process variation tolerance while requires minimal area overhead.

Details of our proposed multi- V_t CAM cell design and ML sensing scheme are presented below.

III. MULTI- V_t CAM CELL FOR LEAKAGE REDUCTION AND SEARCH SPEED ENHANCEMENT

With the rapid increase in memory depth due to the vast amount of search data, CAMs are usually partitioned into multiple banks to improve speed and reduce power. As a result, most of the CAM cells are kept in the idle state, continuously consuming leakage current. As technology scales down to sub-65nm CMOS technology nodes, the leakage current increases significantly and thus has a substantial impact on the overall power consumption of CAMs. One of the options to avoid leakage in these cells is to use non-volatile memories such as magnetic tunnel devices [23, 24]. However, these processes are not mature and not yet ready for low-cost, high capacity implementation. In this work, we will use circuit techniques to suppress the unwanted leakage current in the SRAM cells.

Fig. 4 shows the employed 10T NOR-type CAM cell topology in the standby state where BLs are pre-charged to V_{DD} and SLs are pre-charged to ground. Since ML is pre-charged low (i.e. $V_{ML} = 0$), the comparison circuit (i.e. N1-N4) consumes no leakage power. As a result, the CAM's total leakage is primarily determined by the 6T SRAM element. To minimize the amount of leakage, we deployed high- V_t devices in the 6T SRAM part. The arrows in Fig. 4 depict the sub-threshold leakage currents when the cell data (Q) is '0'. Fig. 5 compares the total CAM leakage using different V_t options at different operating voltage and temperature. Using high- V_t devices reduces the leakage by more than 15 \times and 100 \times when compared to standard- V_t devices and low- V_t devices at 1.2V, 80 °C, respectively. Note that the CAM is normally operated at nominal supply voltage, and read and write operations are not as critical

as the search operation. Consequently, high- V_t devices are adopted in the SRAM element to reduce the leakage of the CAM.

The device type for the comparison circuit (i.e. N1-N4) should be selected for better search performance. Fig. 6 shows the I_{on}/I_{off} ratios of three NMOS types. Since the sense amplifier should distinguish the ML level with single-miss from that with match, a larger I_{on}/I_{off} ratio is desirable. Fig. 6 indicates that high- V_t devices are more favorable than low- V_t devices due to the much higher I_{on}/I_{off} ratio. However, the transient waveforms of the MLs in Fig. 7 explain that using low- V_t devices is a better option in terms of performance. It can be seen that while the matched ML using low- V_t indeed ‘leaks’ more charges when compared with standard- and high- V_t cases, its impact on the ML sensing power is insignificant. This is because the ML sensing is very fast and thus the amount of leaked charge ($Q_{leak} = I_{leak} * T_{sense}$) in ML is negligible. On the other hand, using low- V_t leads to much faster discharging of the single-miss ML. Simulation shows that low- V_t devices improve the ML discharging speed by $2\times$ when compared to the high- V_t counterpart (Fig. 7). Consequently, we adopt high- V_t devices in the SRAM element while low- V_t devices are used in the comparison circuit as shown in Fig. 4. This combination allows us to concurrently minimize the cell leakage and achieve high speed ML sensing. Note that employing low- V_t devices in the comparison circuit have no impact on the leakage power of the CAM design due to grounded ML in the pre-charging phase.

IV. PROPOSED SENSING SCHEME FOR SMALL ML SWING

A. Small ML swing

The conceptual timing diagram and the schematic of a NOR-type CAM row are shown in Fig. 8 (a-b). Similar to the above mentioned power saving designs, the proposed small swing sensing scheme precharges ML to ground (Fig. 8(a)) to eliminate the need for discharging SLs. Prior to a search cycle, both *Pulse* and *Precharge* are high to keep ML at ground by turning on NMOS transistor N1 and turning off PMOS transistor P1. When sensing starts,

Precharge goes low to release ML. After a short delay, an internally generated pulse is sent to the gate of P1 to charge up the ML. In a matched case, ML and its associated comparison circuits are modeled as a capacitor as shown in Fig. 8(c). The ML capacitance is modeled as follows:

$$C_{ML} = 2 \times N \times C_0$$

where C_0 is the drain capacitance of the comparison transistor (N3 in Fig. 2) and N is the number of cells. The voltage developed on a matched ML can be approximated as:

$$V_{ML\text{-matched}} = \frac{I_{pulse} \times T_{pulse}}{C_{ML}}$$

By carefully engineering I_{pulse} and T_{pulse} , the amount of charge injected to ML is controlled so that $V_{ML\text{-matched}}$ is lower than V_{DD} to save power but high enough for reliable sensing. In a mismatched case, at least one current path is formed from ML to ground. It can be modeled by a lump-sum capacitor in parallel with two cascaded NMOS transistors as depicted in Fig. 8(d). After the pulsed current stops, $I_{discharge}$ will eventually pull the mismatched ML to zero. Reference voltage ($V_{ref} = 0.5 \times V_{ML\text{-matched}}$) can be used in differential sense amplifiers to differentiate the mismatched case from the matched case. A dummy row with match is used to generate this reference voltage with the capability of process-temperature-voltage (PVT) variation tracking, which will be described later.

Fig. 9 illustrates the operations of the proposed small ML swing sensing scheme on a matched and a 1-mismatch cases. Once a search operation starts and search data is loaded on the SLs/SLBs, a short pulse is generated and applied to P1 (in Fig. 8) to charge up all MLs and the ML_{ref} simultaneously. MLs with different numbers of mismatches have different rising time. In a matched case, ML remains at the charged-up level when the pulse signal (*Pulse*) is turned off and onward. The reference ML (i.e. ML_{ref}) is also charged to V_{ref} , a voltage level lower than that of the matched ML. Since ML_{ref} is generated from a dummy row with match, it

also remains at a certain voltage level after the short pulse stops. In a 1-mismatch case, ML_{miss} initially rises slowly by the charging short pulse. After the charging phase, it is gradually discharged to ground by the comparison circuits in the CAM cells with mismatch as shown in Fig. 9. Subsequently, the sense amplifier (SA) at each ML is enabled by an enable signal (EN goes high and ENB goes low). Final sensing results are generated after a short delay of the latch comparator.

B. V_{ref} Generation Circuit

Fig. 8(e) explains the V_{ref} generation circuit for the proposed ML sensing scheme. A dummy row with hard-wired data to a matched state is used to mimic C_{ML} . In addition, ML_{Ref} is connected to the input transistors of all sense amplifiers in the array. As a result, $C_{\text{ML-Ref}}$ is modeled as:

$$C_{\text{ML-Ref}} = 2 \times N \times C_0 + M \times C_{\text{gate}}$$

where M is the number of rows and C_{gate} is the gate capacitance of the input transistor of each sense amplifier. If M and N are the same and C_{gate} is similar to $2 \times C_0$, then:

$$C_{\text{ML-Ref}} = 2 \times C_{\text{ML}}$$

Thus:

$$V_{\text{ML-ref}} = \frac{I_{\text{pulse}} \times T_{\text{pulse}}}{C_{\text{ML-REF}}} = 0.5 V_{\text{ML-matched}}$$

To ensure a good matching, the PMOS transistor used in the ML_{Ref} is set to have the same size as normal ML. Note that $C_{\text{ML-Ref}}$ can be slightly higher or lower than $2 \times C_{\text{ML}}$ as long as V_{MLref} is close to $0.5 \times V_{\text{ML-matched}}$, which provides enough input margins to the sense amplifier. Furthermore, the number of dummy cells in the dummy ML can be adjusted to generate $2 \times C_{\text{ML}}$ since M is fixed by the size of the CAM array.

C. ML Sense Amplifier:

A latch-type comparator is used in our design to provide fast sensing speed and low power consumption (Fig. 10). C_P is the total gate capacitance contributed by all M sense amplifier ($C_P = M \times C_{gate}$). PMOS input transistors are used because the ML levels are lower than $0.5 \times V_{DD}$. During standby, both ML and ML_{Ref} are pre-discharged to ground, thus both P3 and P4 are on. At the same time, N3 is disabled by pulling the EN signal to ground. Intermediate output nodes D and DB are equalized by closing the switch S1. As a result, D and DB are floating around the switching point to improve the sensing time. It also mitigates the kick-back noise of the comparator. However, this floating level is neither strong one nor strong zero, leading to significant leakage through two output buffers. To prevent this, D and DB are disconnected from the output buffers by S2 and S3 during standby. Concurrently, inputs to these buffers (i.e. nodes X and XB) are pre-discharged to ground by N1 and N2.

Fig. 11 demonstrates the simulation waveforms of the ML sense amplifier during standby and active durations. When the sense amplifier is activated by EN signal, S1 is opened while S2 and S3 are closed. The cross-coupled structure quickly develops the voltage difference between ML and ML_{ref} . The delay from EN to Out is 133ps at room temperature. Fig. 12 shows how this delay varies at different temperatures and process corners. It can be seen that the worst delay of 155ps happens at the highest temperature and the SS corner. The best delay is 115ps at -25°C and the FF corner. The maximum sensing delay variation is $\pm 14\%$ across different process corners.

D. Offset-aware Comparator Design for Power Reduction

Comparators in the array have intrinsic input offset voltage because of process variations. Input offset of a comparator is defined as minimum required input voltage for correct comparison. Offset voltage is unavoidable in nano-scale CMOS process. Therefore, it is desirable to minimize the offset as much as possible. The magnitude of input offset of a

comparator is inversely proportional to the square-root of the gate area (i.e. $1/\sqrt{WL}$) of the input transistors. Larger input transistors are employed to reduce the offset voltage. However, it increases power consumption due to the increased current through the comparator as well as the gate capacitance associated with each ML. Theoretical minimum ML swing and ML power depend on the offset voltage of the comparator. Increasing the gate area reduces the offset voltage and thus the required ML swing while it leads to more power consumption by the comparator (Fig. 13). On the other hand, reducing the gate area decreases the comparator power while resulting in larger ML swing. Consequently, there is an optimum point to minimize the total power consumption of the ML and the comparator, as illustrated in Fig. 13.

As mentioned, input voltage to a comparator must be no less than V_{offset} for correct sensing. In a mismatch case, assuming that V_{MLmiss} is close to zero, hence V_{MLRef} must be larger than V_{offset} . Similarly, in the match case, $(V_{\text{MLmatch}} - V_{\text{MLRef}})$ must be at least V_{offset} . Therefore, the theoretical minimum required voltage for the matched ML voltage is $2 \times V_{\text{offset}}$ (Fig. 14). In short, the following conditions must be satisfied when the SA is enabled to ensure a correct ML output:

$$V_{\text{in1}} = V_{\text{MLmatch}} - V_{\text{ref}} > V_{\text{offset}} \quad (1)$$

$$V_{\text{in2}} = V_{\text{ref}} - V_{\text{MLmiss}} > V_{\text{offset}} \quad (2)$$

where V_{in1} and V_{in2} are the sense amplifier input voltage when sensing a matched ML and a 1-miss ML, as depicted in Fig. 14. Since the ML power consumption is proportional to the ML voltage swing, it is directly determined by the offset voltage of the comparator. In addition, the charged-up level of each ML also varies due to process variation as shown in Fig. 14. For variation tolerance, the most straightforward methods are: (i) increasing the size of the input transistor pair to reduce V_{offset} ; (ii) imposing a large margin on the pulse width for P1 and P2 in Fig. 10 to inject more charge to the MLs and thus increase V_{in1} and V_{in2} , and (iii) providing

more delay to allow the missed ML to discharged further before enabling the sense amplifier. Fig. 15 illustrates the relationship between V_{in1} and the pulse-width of *Pulse* (in Fig. 10), and V_{in2} and the *EN* delay. While it is highly desirable to reduce V_{offset} as small as possible, there is a certain limit in the size of the input devices of the sense amplifier. Therefore, a large voltage margin must be set to cover possible variations, which leads to significant extra power consumption. To tackle this, we propose a circuit technique that can track the minimum required ML swing, which will be discussed in the next section.

V. AUTOMATED BACKGROUND CHECKING (ABC)

In this section, we explain the proposed automated background checking (ABC) scheme for setting a minimum margin on the above-mentioned ML sensing and adjusting it automatically. The operation principle of the proposed ABC scheme is illustrated in Fig. 16. The reference row is shared by all SA and has an additional parasitic C_p , which is formed by the device parasitic capacitance and the interconnection between the reference row and the SAs. As a result, the pre-charged level of V_{ref} is lower than that of matched MLs. The conditions described in (1) and (2) can be violated in the following two scenarios: (i) when the pre-charged voltage is too small, the condition in (1) is violated; (b) when the sense amplifier is enabled too early and hence V_{MLmiss} is not yet discharged to a low voltage, the condition in (2) is violated. The proposed ABC scheme uses two dummy MLs as guard bands to protect the main array from these two sensing errors and simultaneously maintain the power consumption at the ML as low as possible.

Fig. 17 shows the circuit implementation of the pulse-width generator. If the condition in (1) is violated, the dummy ML_{match} creates a rising edge at its output to clock the shift-register. This register shifts the “1” bit to a more significant bit, weakening the strength of the pull-up

PMOS devices and resulting in a wider pulse width. Thus, in the next cycle, MLs will be pre-charged to a higher level, inducing larger V_{in1} . Similarly if the condition in (2) is violated, EN must wait longer so that ML with mismatch is discharged further. The dummy ML_{miss} in Fig. 16 will signal to the adjustable delay generator to extend the delay of the EN signal for larger V_{in2} . When the proposed CAM is enabled, the first few search operations can be used to calibrate these two blocks. In this work, the pulse width and the EN delay is implemented so that the equivalent sensing margin of the main array is 10% higher than that of the dummy rows by transistor sizing. Even if the condition (1) or (2) is violated at the two dummy rows, the main array can still work without sensing margin failures. This means that sensing errors are always detected at the dummy rows first and can be corrected without interrupting the CAM operation. Fig. 18 illustrates how the adjustable pulse width generator operates. We force the matched dummy ML to a wrong state by holding the V_{ref} at 300 mV and the offset voltage of the SA is assumed to be 100 mV. For correct sensing, $V_{MLmatch}$ must be charged-up to 400 mV at least. Initial $V_{MLmatch}$ is lower than 400 mV and the register shifts the data (first 3 cycles) until $V_{MLmatch}$ is sensed as logic '1'. The adjustable EN delay generator works in a similar way.

Our 1000-point Monte-Carlo simulation showed that the maximum offset, $OffsetMax$, of the comparator is about 75 mV. Due to random process variation, it is impossible to perfectly match the offset of the comparator in the dummy row to that of the comparator in the main array. In fact, if we assume perfect sizing and layout matching, the offset of the dummy and the real comparators can be anywhere in the range of $[0, OffsetMax]$. It is possible, however, to reduce $OffsetMax$, at the cost of power consumption and silicon area using larger input transistor pair. To further improve the matching of the SAs, we also used two SAs in the dummy row as a redundancy check. The sensing output is considered to be correct if and only if both of them provide a correct sensing result.

VI. PERFORMANCE EVALUATION AND TEST CHIP IMPLEMENTATION

A 128x128 prototype chip with row decoder, read/write/SL driver and priority encoder is fabricated in a 65 CMOS process. The microphotograph and layout of the test chip is shown in Fig. 19. Three separate supply pads are used to measure the currents consumed by the SRAM cells, the ML sensing circuits and the other peripheral circuits, respectively. Due to the limited number of pads, we only utilized five pads for the input data (DataIn₀₋₄) and five pads to probe the sensing results (ML₀, ML₁, ML₂, ML₃ and ML₁₂₇). During write and search operation, DataIn₀, DataIn₁, DataIn₂, DataIn₃ are routed to 0th, 3rd, 5th and 9th respectively while DataIn₄ is routed to the rest of the columns. This arrangement allows us to induce match, 1-miss, 2-miss, 3-miss, 4-miss and all-miss scenarios. Since the most critical cases are the matched and 1-mismatch cases, we assume that rows with more than 4 misses will be correctly detected. To evaluate our design, its performance is compared with the conventional design using simulated data. Both designs were simulated using the same input data patterns and operating conditions. According to our simulation, when the number of misses per row is higher than 6, ML power does not increase with number of missed as the ML is firmly held at ground. Thus, the average power consumption of the chip is measured and simulated only considering matched cases, 1-miss cases, and all-miss cases. The test chip occupies an active area of only 0.125 mm². The cell size is 3.8 μm² using low-power, standard logic rules while the array area is 480μm×130μm. Overhead of the ABC scheme is 5%, including the two dummy rows. Note that when this scheme is applied to a larger array, area occupied by this ABC circuit is still the same and thus the overhead is even smaller. Fig. 20 and Fig. 21 compare the speed and power performance of the proposed design and the conventional one. Sensing delay is the delay from the rising edge of the Search command until output is available. At nominal supply voltage, both designs have a similar search delay of 1.07 ns. However, as supply voltage reduces, the proposed design proves to be less sensitive to supply

voltage scaling. At 0.8 V, search delay of the proposed design is only 1.45 ns while that of the conventional design is 1.78 ns. Fig. 20 also shows that the proposed sense amplifier is less sensitive to temperature variations. Regarding the power consumption, the proposed design consumes $5.5\times$ less power when compared to the conventional design at 1.2 V operating voltage (Fig. 21). As supply voltage scales down, the full ML swing in the conventional design reduces significantly, making the benefit of the proposed scheme less attractive. Nevertheless, at 0.8V the power consumption of the new design is only one-third of the conventional design. The chip has been tested successfully with an average FOM of 0.77 fJ/bit/search.

The power breakdown of the test chip is shown in Fig. 22. The ML and SL power consumption contributes 37% and 41% of the total power, respectively. Note that this work focuses on ML sensing and we employed a conventional SL design without hierarchical structures. In our test chip, a large number of buffers are added at the input and output nodes to drive the analog pads, which consumes 22% of the total chip power. However that this 22% should not be counted as the a part of CAM performance as it is used to drive analog pads for purpose of testing. Leakage power was measured (Fig. 23) which showed that SRAM leakage is the dominant part. It accounts for 50% of the total leakage power, even with our multi- V_t cell design. Note that the density of the current CAM design is rather small and thus the amount of the leakage is insignificant when compared to the dynamic counterpart. However, with a higher capacity and banking architecture, dynamic search power will decrease and leakage will become an important factor. Therefore, reducing leakage is crucial to maintain overall power consumption low.

In this work we use the conventional figure-of-merit (FOM) formula for evaluating the performance of the design, as below:

$$FOM = \frac{Power \times ClockPeriod}{Total\ number\ of\ bits}$$

Table I compares the test chip performance with prior works which have similar capacity as our design. Our design offers the best FOM with similar or better search delay except for the design in [10]. When normalized FOM is used, it is 35% worse than that of [20] but has 3×better sensing delay. Note that FOM of our design can be reduced even further if hierarchical or pre-computational ML architecture is used.

VII. CONCLUSION

Faster and lower-power CAM designs for state of the art network routers are highly required to meet the demands of recent booming of internet traffic. In view of that, this work proposes an energy efficient CAM design for very large array implementation. The SRAM element uses high- V_t devices to reduce leakage by 100× while the comparison circuits inside the CAM cell uses low-threshold devices to enhance the search speed. A latch-based differential comparator is employed to realize high speed sensing while an automated background checking is proposed to silently track the minimum required ML swing for saving power. A 128×128 binary CAM prototype chip has been implemented using a standard 65 nm CMOS process. When compared to the conventional design, it reduces the power consumption by 5.5× while maintain a similar sensing delay. It achieves 1.07 ns delay, 0.77 fJ/search/bit at 500 MHz, 1.2 V supply voltage. Note that we focus on the main ML sensing and if pipeline or selective pre-charge architecture is used, its FOM can be further improved.

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Table I: Performance comparison of prior works

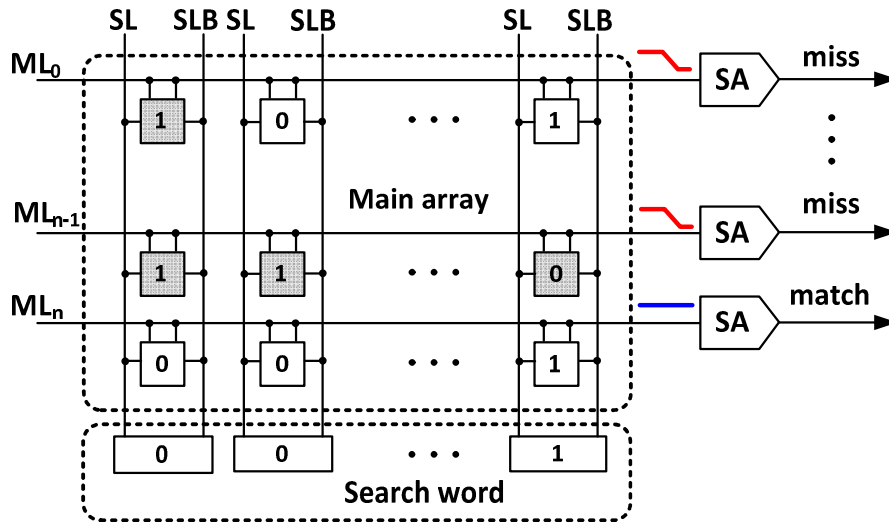
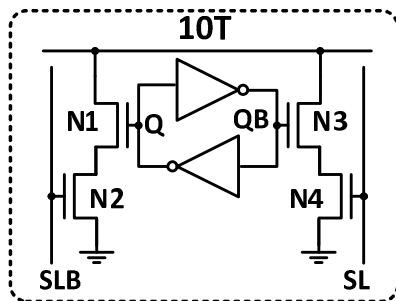
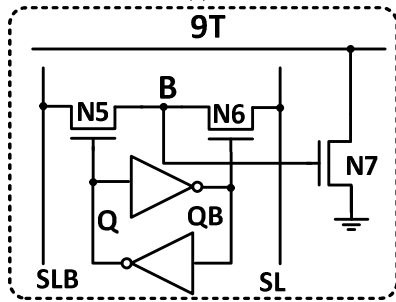


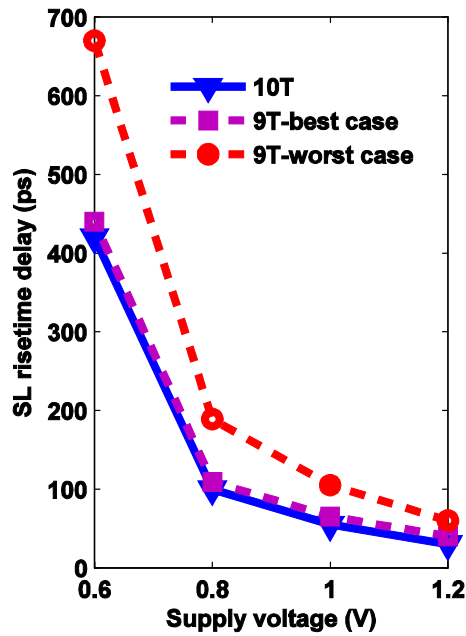
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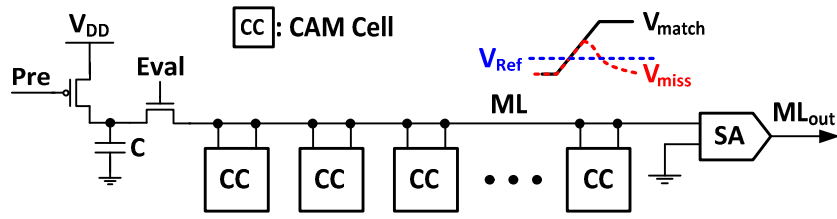


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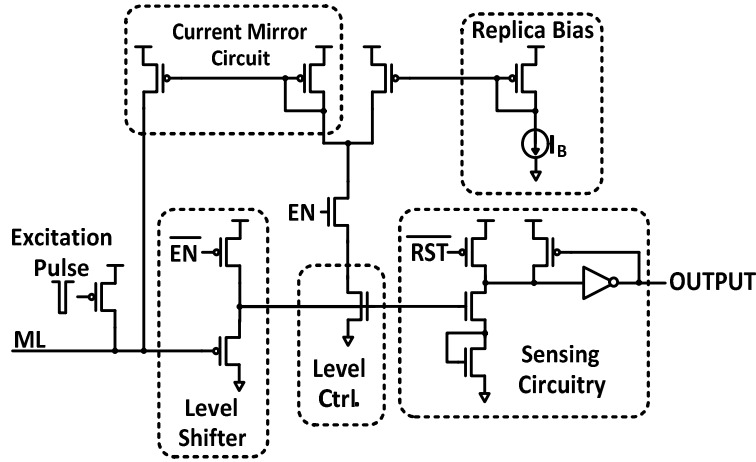


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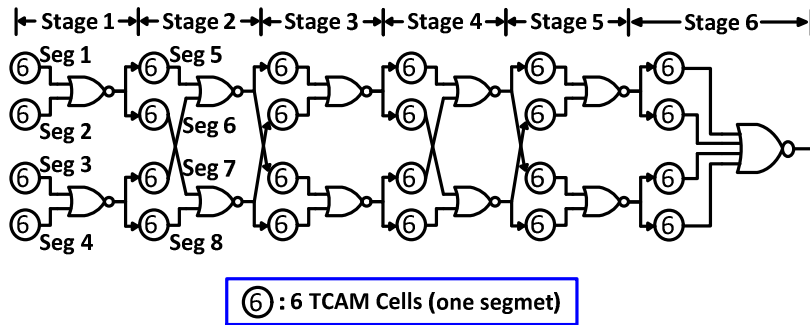
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(b)



(c)

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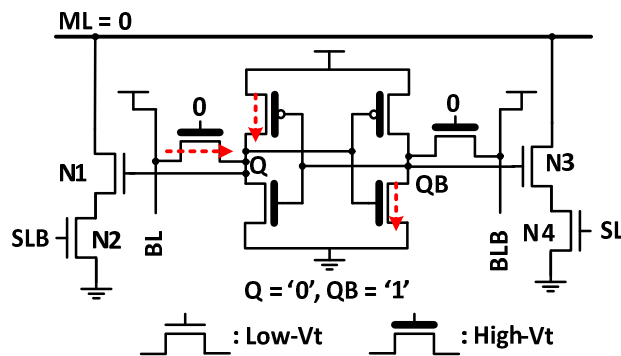


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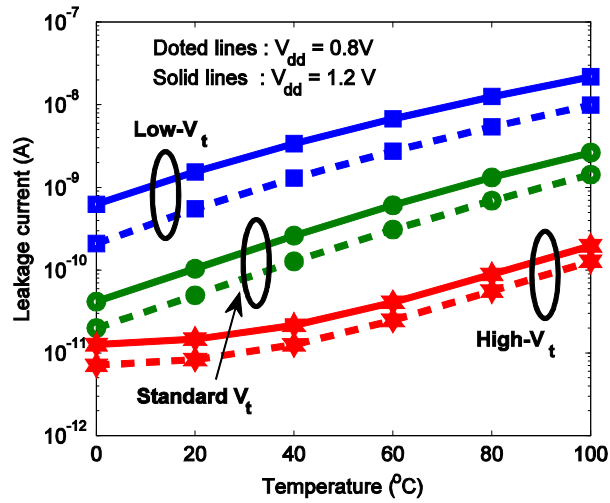


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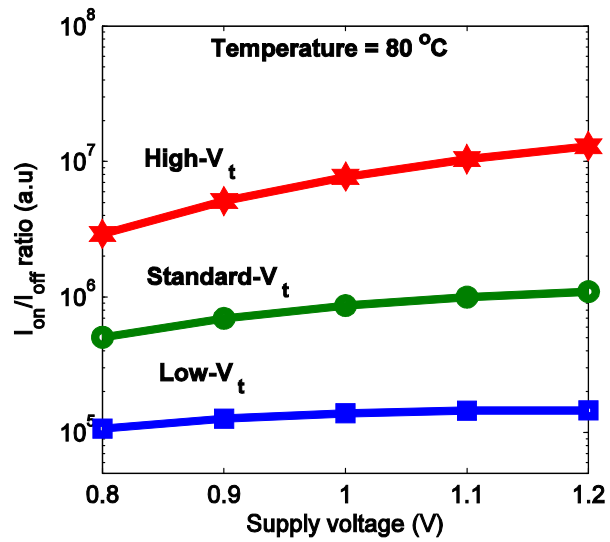


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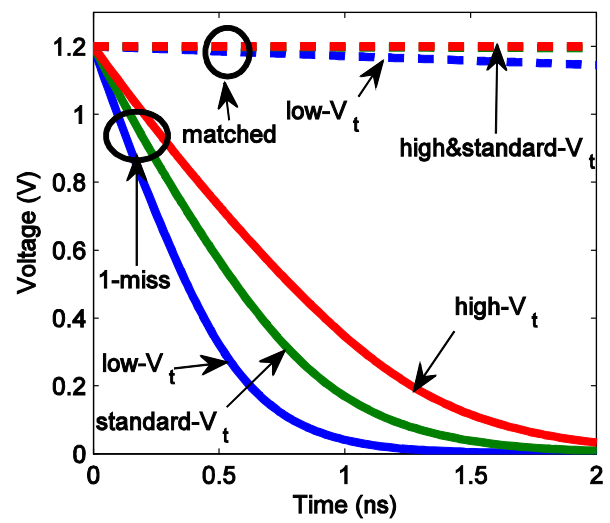


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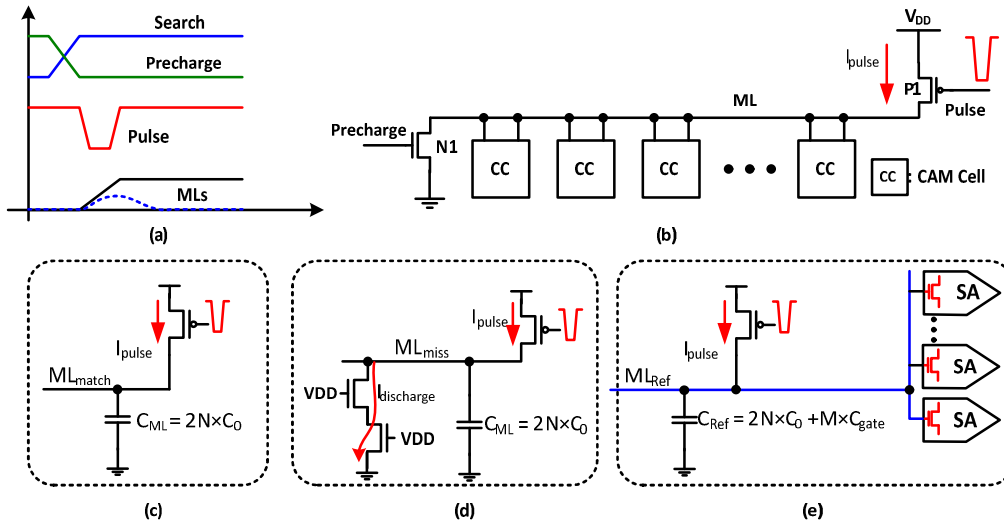


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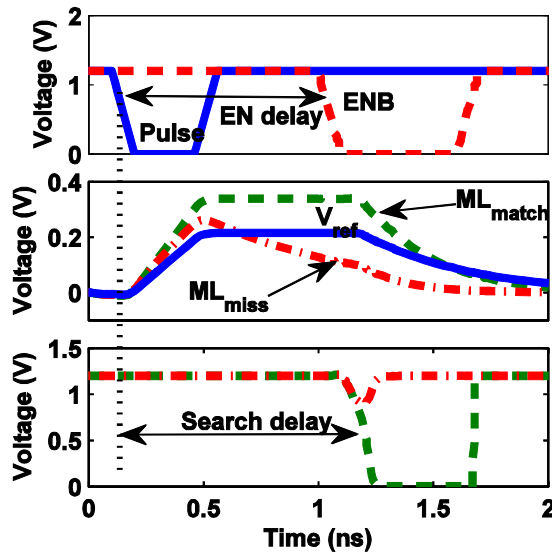


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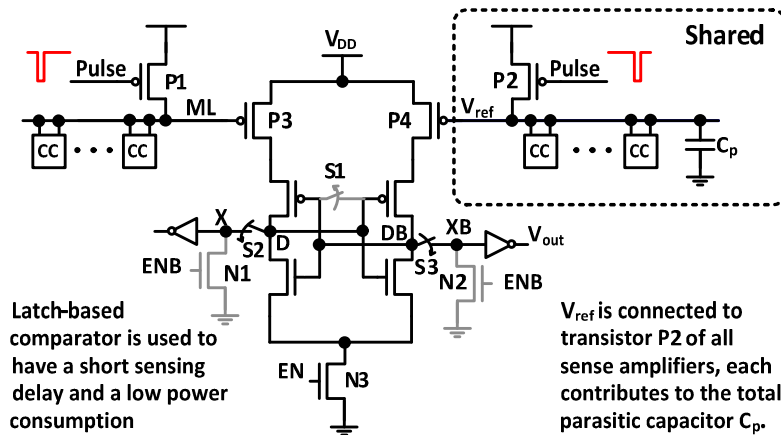


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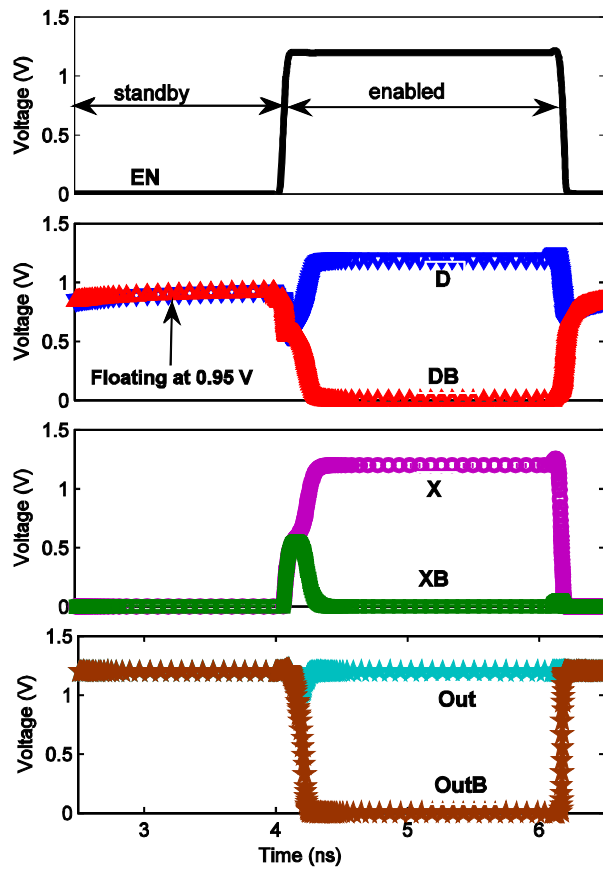


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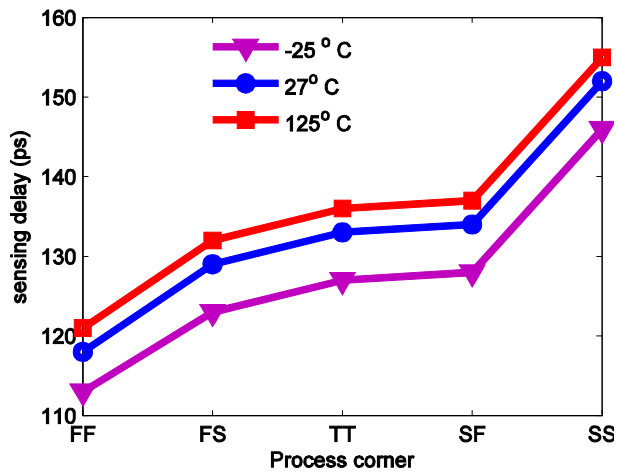


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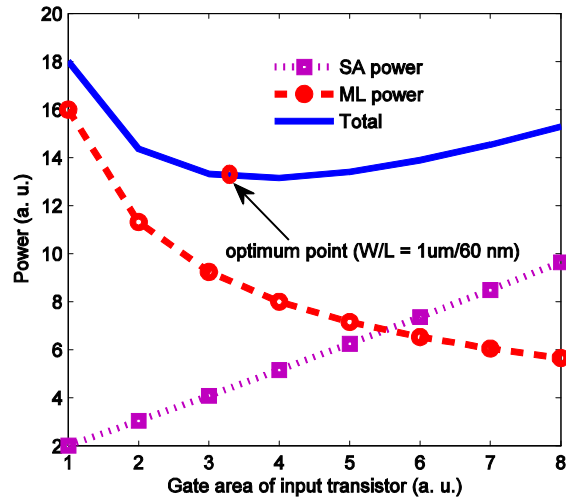


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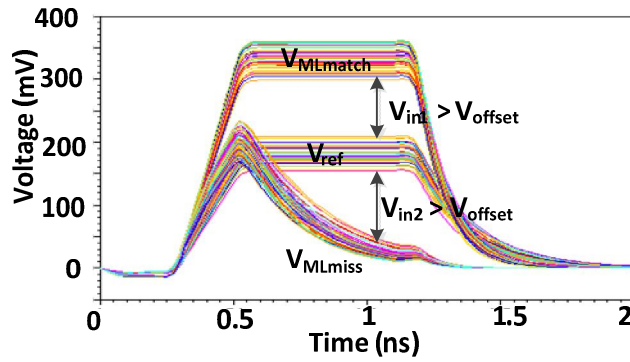


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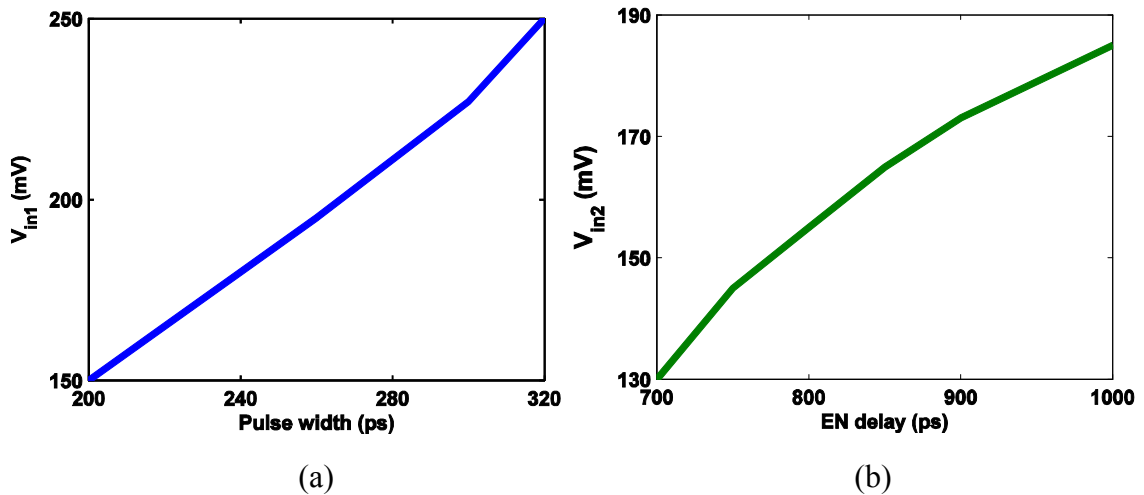


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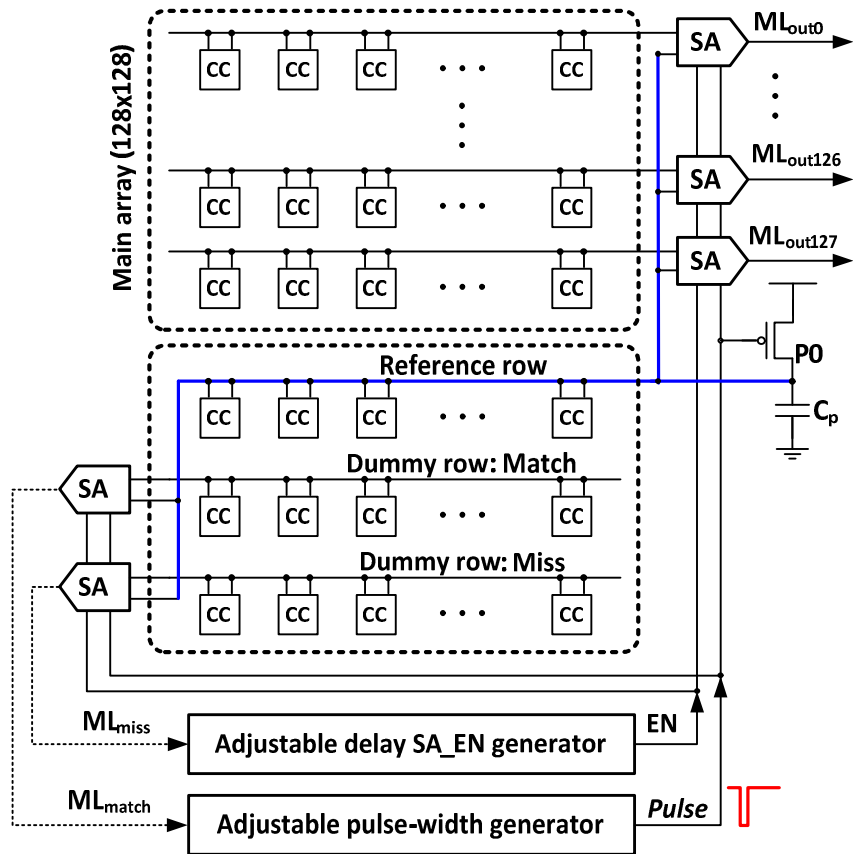


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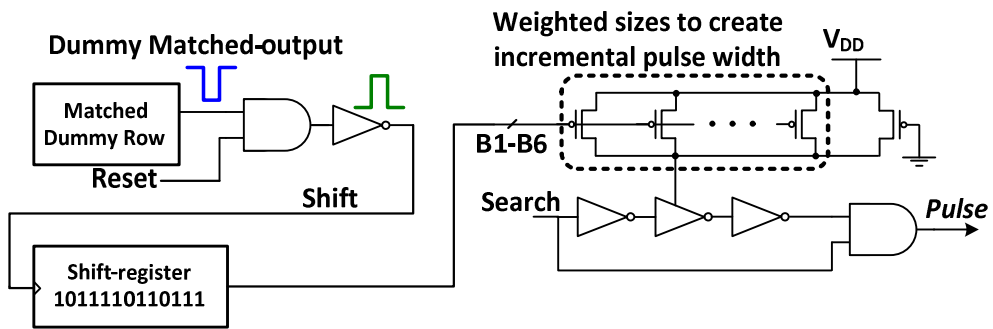


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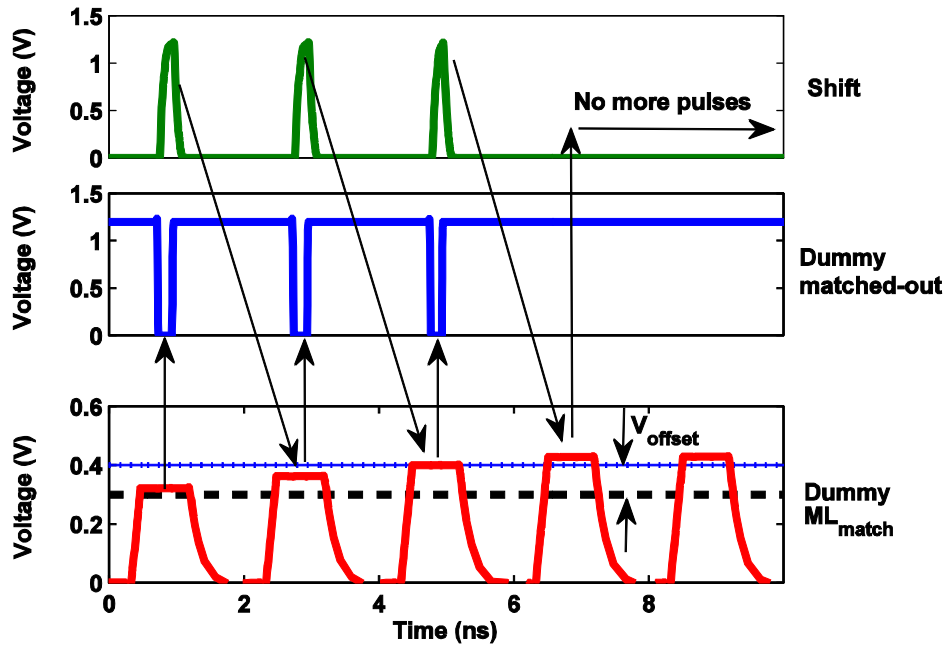


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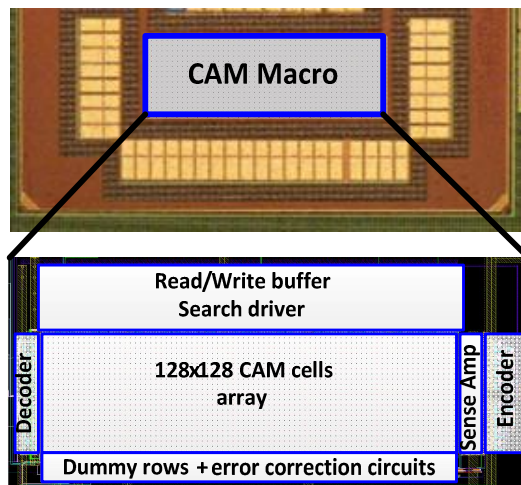
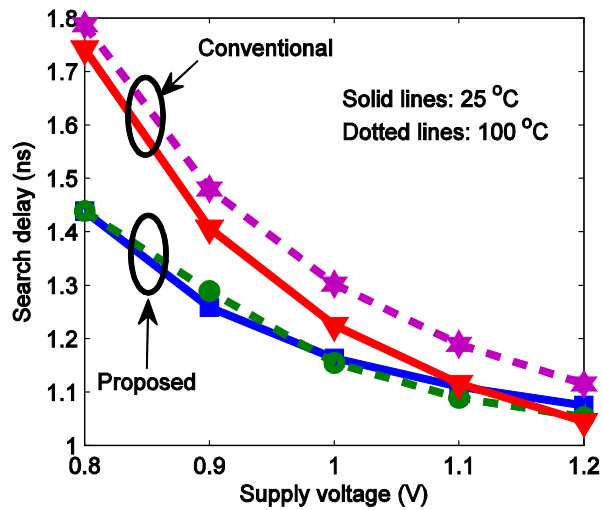
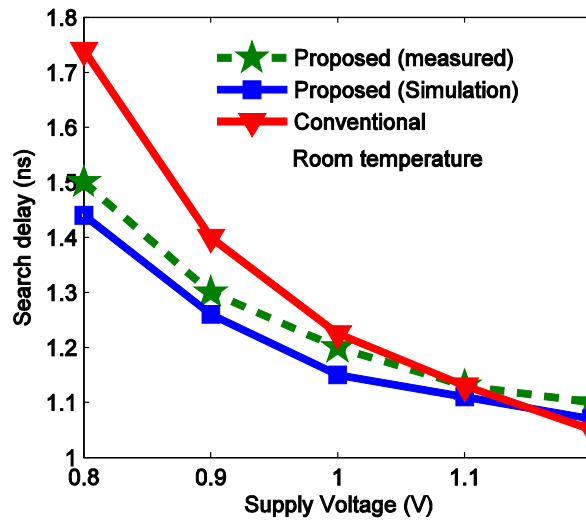


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(a)



(b)

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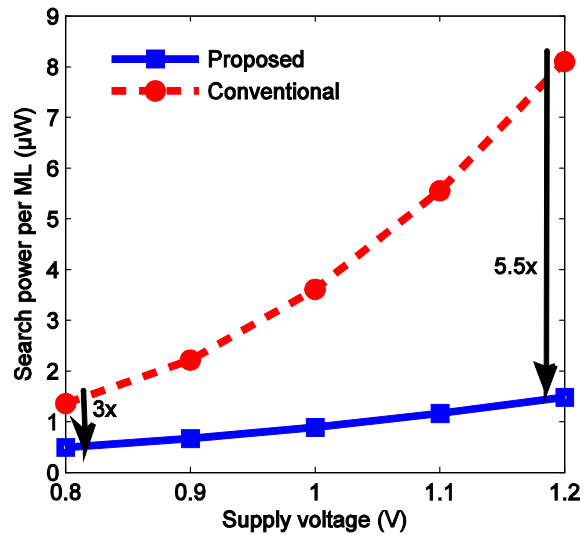


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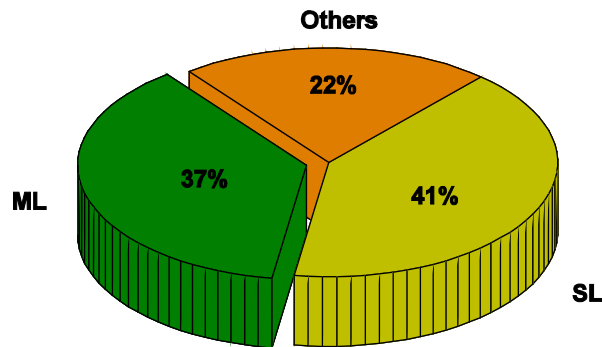


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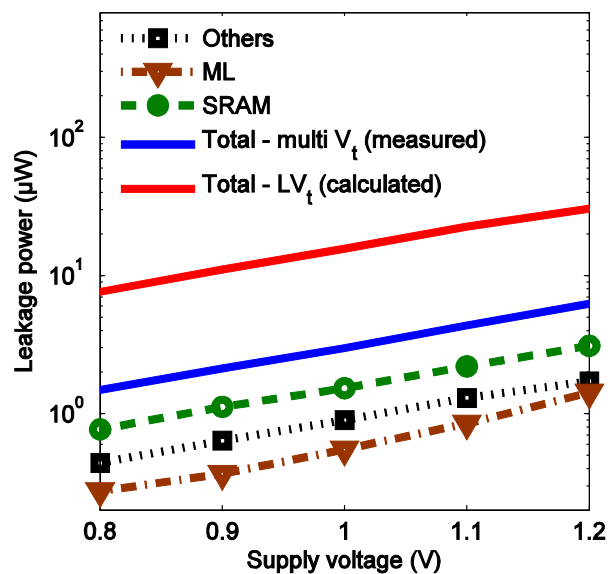


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TABLE I. PERFORMANCE COMPARISON OF PRIOR WORKS

	This work	[25]	[10]	[3]	[19]	[20]
Technology /Supply	65 nm /1.2V	130nm /1V	32nm/1V	65 nm/ 1V	65 nm/ 1V	130nm /1.2V
Search delay (ns)	1.07	0.9	0.145	1.92	0.6 (72 bits) 2.2 (240 bits)	3.5 ns
FOM (fJ/bit/search)	0.77	1.827	1.07	1.98	0.99	1.3
Normalized FOM*	1	1.09	2.48	2.37	1.2	0.65
Frequency	500 MHz	250 MHz	N.A	250 MHz	450	N.A
Chip area(mm ²)	0.125	1.4	N.A	99	0.078	N.A
Capacity	128×128	128×32	128×128	18 Mb	64x72	256x144

$$*\text{Normalized FOM} = \text{FOM} \times \frac{65 \text{ nm}}{\text{technology node}} \times \frac{1.2V}{VDD}$$