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Fabrication of silicon-embedded low resistance high-aspect ratio planar copper microcoils

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Abstract. Low resistance is an important requirement for microcoils which act as a signal receiver to ensure low thermal noise during signal detection. High-aspect ratio (HAR) planar microcoils entrenched in blind silicon trenches have features that make them more attractive than their traditional counterparts employing electroplating through a patterned thick polymer or achieved through silicon vias. However, challenges met in fabrication of such coils have not been discussed in detail until now. This paper reports the realization of such HAR microcoils embedded in Si blind trenches, fabricated with a single lithography step by first etching blind trenches in the silicon substrate with an aspect ratio of almost 3:1 and then filling them up using copper electroplating. The electroplating was followed by chemical wet etching as a faster way of removing excess copper than traditional chemical mechanical polishing. Electrical resistance was further reduced by annealing the microcoils. The process steps and challenges faced in the realization of such structures are reported here followed by their electrical characterization. The obtained electrical resistances are then compared with those of other similar microcoils embedded in blind vias. [DOI: 10.1117/1.JMM.17.1.014501]

Keywords: microcoil; copper electroplating; high-aspect ratio silicon trench.

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1 Introduction

An area where the current aggressive miniaturization trend has been less successful is the miniaturization of inductive components, i.e., spiral mini- and microcoils. The key reason for this is that the size of a planar mini- or microcoil is typically dictated by the desired inductance, which in turn determines the outer diameter and number of turns. Mohan et al. described many expressions of inductances for planar inductors of different shapes and sizes.[1] All of them show that the inductance increases with the number of turns N which also increases the surface area and hence also the parasitic capacitance. The two most popular microcoil structures achieved in microfabrication are the three-dimensional (3-D) coils and the planar coils. The 3-D coils consist of through silicon via (TSVs) or through polymer vias (TPVs)[2] pillars filled with Cu followed by planar metalized strips connecting the adjacent TSV (or TPVs) in both front and backside of the substrate to realize the solenodial-type 3-D microcoils. In these coils in order to define the horizontal interconnects, complex and double photolithographic steps are required on both front and backside of the wafer through backside and frontside alignment which increases the number of fabrication steps and hence the process complexity. The other variety of microcoils is the planar ones defined on the surface of the substrate or embedded inside substrate trenches. In almost all cases, the planar coil's conductor has a rectangular cross section that is placed horizontally, i.e., with the long side of the rectangle representing the width of the conductor, and the short side of the rectangle representing the thickness of the conductor. The ratio of this thickness of the conductor to its width defining the coil turns is called the aspect ratio. With a high aspect ratio (HAR), defined as >1 two advantages are obvious: first, HAR increases the conductor cross-sectional area, which reduces the coil resistance—essential for signal detecting to reduce thermal noise and second this reduces the area occupied by the coil on the substrate and hence helps in miniaturization. From existing literature reports, it can be seen[3–6] that coils are achieved on top (not embedded) of Si substrate with thin sputtered metal layers whereas similar planar coils are achieved on the surface of GaAs substrates in Refs. 7–9 and on glass substrates in Ref. 10.

Table 1 summarizes the most relevant planar microcoils realized through copper electroplating inside trenches of different substrates. It can be seen from Table 1 that coils embedded in silicon substrate have been reported in Refs. 11–15 and these employ a Cu-electroplating process to achieve thick copper depositions in the Si substrate. Similarly, planar microcoils embedded inside other polymer-based substrate have also been reported such as inside SU8,[18,21] parylene,[20] polymide,[17] and even inside trenches defined by photoresists.[19] Coil embedded inside thick silicon dioxide is reported in Ref. 16. Achieving a planar microcoil inside Si substrate, however, has advantages of its own such as better heat dissipation compared to the other polymer-based substrates. References 12, 22, and 23 show that currents up to 250 mA could be used without any problems, and other unreported tests we did showed that we could easily inject currents up to 500 mA, and for an extremely short time we even tried 1 A. A Si substrate also gives a highly planar top surface that allows realizing polymer-based microfluidics or other structures fabricated by subsequent postprocessing. In addition, achieving microcoils in Si has the greatest

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Table 1 Comparison of various on-chip planar microcoils realized through Cu electrodeposition inside trenches of various substrates (N.R. = not reported).

Reference	Coil type	AR value	Resistance (Ω)	*Q* factor
Kim et al.[11]	Double rectangular spiral inductor with 10 turns covered with a NiFe film inside silicon substrate	10:92	2.88	15.9 (5 MHz)
Ramadan et al.[12]	Circular spiral of 35 turns Cu coil inside silicon substrate	10:3	20.25	N.R.
Pan et al.[13]	Rectangular spiral Cu coil inside low resistivity Si substrate	5:6	N.R.	60 (30 to 40 MHz)
Wang et al.[14]	Rectangular spiral coil achieved using TSV by bottom to top growth Cu electroplating	1:1	0.023	N.R.
Jiang et al.[15]	Circular spiral coil achieved using TSV by bottom to top growth Cu electroplating	16	0.037	85 (1.6 GHz)
Tang et al.[16]	3 to 7 turn circular spiral coil embedded in thick SiO_2 layer	5:4	N.R.	43.1 (6.9 GHz)
Lee et al.[17]	10 turns spiral copper coil inside polymide mold on a glass substrate	1:5	2	N.R.
Massin et al.[18]	Three turns circular, spiral, Cu coils inside SU8 molds on a glass substrate	3:10	0.7	23.5 (300 MHz)
Li et al.[19]	Single turn rectangular Cu coil electroplated inside PR mold on a silicon dioxide layer above Si substrate	1:10	N.R	5.06 (1 GHz)
Walker et al.[20]	Rectangular spiral Cu coils electroplated within parylene mold with NiFe core above and below the Cu coil	3:5	N.R.	14.5 (10 MHz)
Schroeder et al.[21]	Circular multilayer spiral Cu coil, electroplated inside SU8 molds	N.R.	N.R.	N.R.

advantage in that it is an IC compatible process.[14] It can start with silicon wafers with ICs already built by a commercial IC foundry. Therefore, it is possible that fully integrated other CMOS-based circuitry can be fabricated by an IC foundry. Such a CMOS-MEMS process capable of fabricating DRIE Si trenches has been developed for making integrated inertial sensors.[24,25] This advantage of CMOS-compatibility possible through using only Si as the substrate for microcoils has also been reiterated in Ref. 13. Therefore, Si substrate has been our choice for fabricating the embedded microcoils reported in this paper. Our microcoils reported here are also embedded in Si substrate and are obtained through Cu electrochemical deposition (ECD) inside HAR Si blind vias obtained through DRIE. Reference 13 also reports such microcoils; however, the aspect ratio of such coils is <1 and no detailed analysis of Cu ECD inside these low aspect ratio Si blind vias is given. Moreover, they use chemical mechanical polishing (CMP) to achieve their microcoils while in our case we omit the time consuming CMP step and use a controllable, fast Cu wet-etching technique instead. Our previous group,[12] however, reports HAR microcoils embedded in Si but gave no details of the blind trench filling process due to proprietary concerns. When it comes to HAR among the reported planar microcoils embedded in Si trenches, Refs. 14 and 15 achieved very HAR but there exists a very stark difference between their reported microcoil and ours reported here. The microcoils achieved by them are fabricated using Cu electroplating inside through silicon trenches that uses seed layer only at the bottom of the trenches achieved by pasting a separate wafer with the seed layer in its surface at the backside of the TSV wafer. This gives dedicated bottom to top Cu electrodeposition unlike our microcoils where the trenches in Si are not through but are blind trenches and the seed layer is present both at the bottom and the sidewalls of the trenches. Such a bottom-up method has also been reported in Cu ECD inside TSVs in Ref. 26, where it is clearly shown that the Cu deposition from electroplating occurs only along the length of the trenches (TSVs) from the bottom "contact wafer" attached at the backside of the "device" wafer. This type of electroplating has been the most successful for TSVs but for coils achieved through deposition of Cu inside blind Si vias this technique is not possible and the seed layer is deposited in the side walls as well as the bottom of the blind via. Therefore, the Cu electroplating inside through silicon trenches (both isolated TSVs and microcoils through TSVs) is less challenging since the Cu deposition is from the bottom compared to the electroplating in blind vias where the growth happens laterally from the sidewalls as well as from the bottom. Yung et al. also analyzed this difference[27] of Cu electroplating in open namely through silicon trenches and blind silicon trenches while Ref. 26 has also mentioned this difference between bottom up electroplating in TSVs and electroplating with the seed layer present in all the trench sidewalls. In addition, not only the fabrication procedure is different but also achieving coils through TSVs does not allow any backside processing of the Si substrate wafer later such as backside bulk wet etching of Si substrate and followed by deposition of magnetic materials as reported previously by our group.[12] The features and challenges of electroplated copper used in damascene processing for typical multilayer interconnections in ICs or different types of copper corrosion

in microstructures filled with Cu have also been characterized.[28–30] For TSVs, the underlying mechanism, issues, and challenges have also been detailed earlier.[31–35] Hence, the challenges and solutions proposed in these reports might not necessarily extend to Cu ECD inside long HAR blind vias of Si to realize planar microcoils as in our case.

This paper will detail the problems met along the fabrication steps of microcoils buried in HAR blind trenches etched by DRIE in a Si substrate. We start photolithography for HAR trenches followed by smoothening of the scalloped walls of Si trenches realized by DRIE which is already reported in Ref. 36 and hence we do not detail the process further here. The difficulties of the major fabrication step, the ECD of copper in long continuous spiral-shaped HAR silicon blind trenches are next presented. Such challenges include optimization of the copper electroplating parameters (electroplating time and current density, effect of seed layer thickness) using an orthogonal design of experiments (DoE) to eliminate voids and achieve proper filling of the silicon trenches with copper. Unlike the Cu ECD optimization procedure reported by Refs. 37–39 inside their TSVs where they modify the additive contents of the electrolyte, we have used only premixed electrolytic solution without any variation or modification of additive contents. The recipe that gave us best filling was obtained by modifying only the external nonchemical parameters determined by orthogonal DoEs and the Taguchi analysis method. Hence, our method is more straightforward without the need for the electrolyte to have go through chemical analysis frequently to determine additive concentration and modifying them accordingly. Second, an entirely unique and original contribution is using wet etching using only sodium persulfate instead of conventional CMP to remove the postelectroplated copper overburden. Also, this wet-etching procedure has been compared with existing wet etching of Cu and the advantages of it are highlighted. The process has been optimized using orthogonal DoE to achieve controllability. Then, the resistance of the microcoils was extracted from I–V characteristics using nanoprobing. Initial high resistance was minimized after annealing in a hydrogen-rich reducing ambience which both increases the grain sizes and removes the nonconductive copper oxides. Finally, the resistances are compared with those reported in other works.

2 Fabrication of Copper Microcoils

The microcoils used in our tests had an internal radius of 25 μm, trace width of 7 μm, height (i.e., trench depth) of 20 μm, and interturn spacing of 3 μm. Three microcoil variants were realized, with 3.5, 15.5, and 40.5 turns, respectively. In the first step, the spiral shape of the microcoil was patterned using photolithography and DRIE to define the HAR microcoil trenches which are subsequently filled up with copper using ECD. Finally, the excess copper is removed to reveal the embedded microcoils inside the silicon trenches. This fabrication process flow is shown in Fig. 1. Cross section of the spiral coil structure after realization of DRIE trenches in the silicon substrate is shown in Fig. 2.

The major challenge faced post-DRIE was the scallop formation on the walls of the Si trenches which prohibited uniform deposition of a combined Ti–Cu adhesion-seed layer, necessary for the subsequent Cu ECD. This problem was solved by repeated thermal oxide growth and oxide

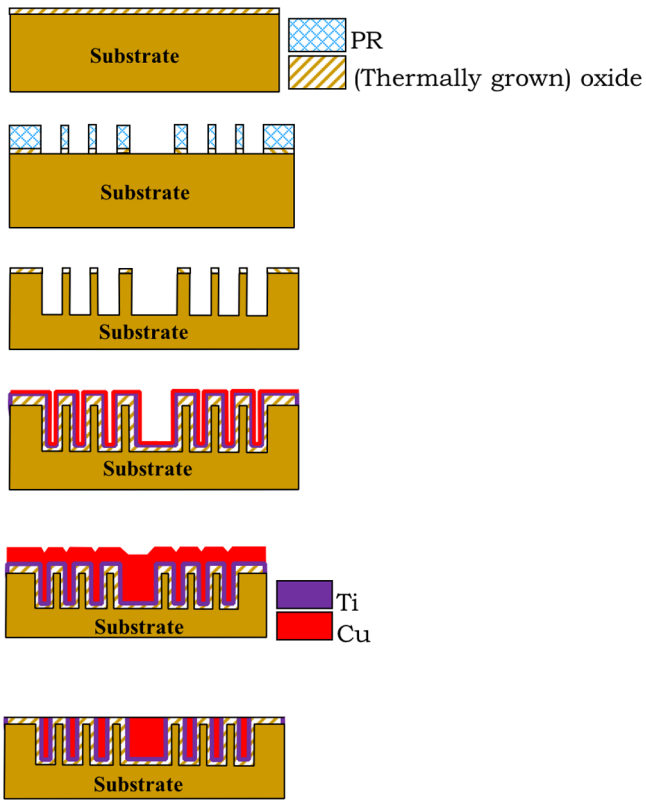

Fig. 1 Process flow steps for realizing the silicon-embedded HAR microcoils.

removal inside the trenches. The details of this process have been explained in a previous work reported in Ref. 36. After the sidewalls were smoothened out, a last layer of thermal silicon dioxide was grown for two purposes, viz. to provide electrical insulation and to make the trench walls hydrophilic. This latter feature makes the trench walls easily filled in and wetted by the aqueous electrolyte, which is beneficial for ECD of copper in HAR trenches.

2.1 *ECD of Copper*

Copper sulfate was used in our ECD work, as it is the most common commercially available electrolyte used in copper

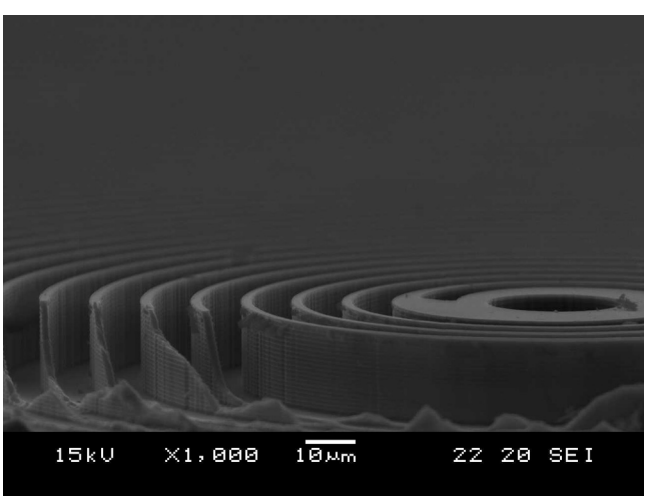

Fig. 2 Cross section of DRIE trenches successfully etched into the Si substrate before filling up with Cu.

Table 2 Composition of the commercially available PC 81 electrolyte.

Constituents of PC 81 electrolyte	Concentration
Copper sulfate	75 gm/L
Sulfuric acid	180 gm/L
Chlorine ions (from HCl)	60 mg/L
Additives	2 ppm
Total plating bath volume	8 L

electroplating and it is also cheap, nontoxic, and has a high throwing power. The solution used for copper ECD typically consists of copper sulfate pentahydrate, sulfuric acid, hydrochloric acid, and organic additives. Copper sulfate provides the copper ions, the sulfuric acid enhances the conductivity of the solution, and the hydrochloric acid provides chlorine ions which help in the uniform dissolution of the copper anode. The additives generally consist of organic compounds that are denominated by the industry as levelers and brighteners. The levelers are needed for electroplating in trenches as they reduce the probability of void formation, while the brighteners are used to increase plating uniformity. The experiments and the final electroplating in our case were done using 6-in. silicon wafers and the electrolyte used was the commercially available PC 81 solution from Slotocoup. PC 81 comes with a premixed concentration of additives and its composition is given in Table 2.

2.1.1 *Orthogonal DOE of ECD: analysis using Taguchi method*

The orthogonal DoE followed by statistical analysis through the Taguchi method have been introduced and used previously to optimize complex multidimensional processes, e.g., to determine the optimal recipe for dry-etching parameters. Similarly for our electroplating experiment, we use an orthogonal DoE followed by the Taguchi analysis method to optimize the process.[40] Similarly, we used an orthogonal DoE followed by Taguchi analysis to optimize the electroplating process parameters. An orthogonal array L_3^4 for four control parameters with three levels each was used for our experiments. The four main control parameters considered for the DOE were current density, temperature, agitation of the solution in the bath, and plating time. However, two sets of experiments were planned using DOE; one with plating time of up to 60 min (referred here as shorter time) and the other up to 120 min (referred here as extended time). The different levels for all these parameters are detailed in Table 3 for both sets of experiments. All these experiments were carried out using the Slotocoup PC 81 electrolyte, on 6-in. silicon wafers with a copper seed layer of 100 nm on 20 nm of Ti acting as an adhesive layer. For each combination of control parameters represented in the rows of Table 3, we carried out three experiments and measured the average thickness of deposited copper, hence calculating the deposition rate. From these values, a mean signal-to-noise ratio (SNR) was calculated, corresponding to each control parameter which is shown in Fig. 3. The SNR value of the i'th experiment is calculated as

Table 3 Different levels of the selected process variables; experiments with shorter time (above), experiments with longer time (below).

Exp #	Current (A)	Time (min)	Temperature (°C)	Agitation (rpm)
		Shorter time		
1	0.01	30	25	0
2	0.01	45	40	100
3	0.01	60	65	300
4	0.1	30	40	300
5	0.1	45	65	0
6	0.1	60	25	100
7	0.05	30	65	100
8	0.05	45	25	300
9	0.05	60	40	0
		Longer time		
1	0.01	60	25	0
2	0.01	90	40	100
3	0.01	120	65	300
4	0.1	60	40	300
5	0.1	90	65	0
6	0.1	120	25	100
7	0.05	60	65	100
8	0.05	90	25	300
9	0.05	120	40	0

$$\mathrm{SNR}_i = -10 \log\left(\frac{1}{N_i} \cdot \sum_{u=1}^{N_i} \frac{1}{y_u^2}\right), \tag{1}$$

where y is the performance characteristic of the experiment, which in our case is the plating rate. N_i is the number of trials for the i'th experiment as indicated in the first column of Table 3. And u is the trial number. For our case for each experiment (i), we have three trials hence $N_i = 3$ and $u = 1$, 2, and 3. Next, for each of these parameters, the difference between the maximum and minimum values of SNR is plotted in Fig. 4. The largest values Δ in SNR for a certain parameter indicate that it is the most influential control parameter in controlling the electrodeposition rate. As expected current (or current density) has the highest influence on the electrodeposition rate followed by the plating time. However, Fig. 4 shows that the deposition rate's dependence on the plating current is smaller for the longer plating time, indicating a slight saturation effect. Both agitation and temperature are the least important parameters and, therefore, may have a significant effect only if the experiment runs for a longer time, otherwise their effect is negligible for a short plating time.

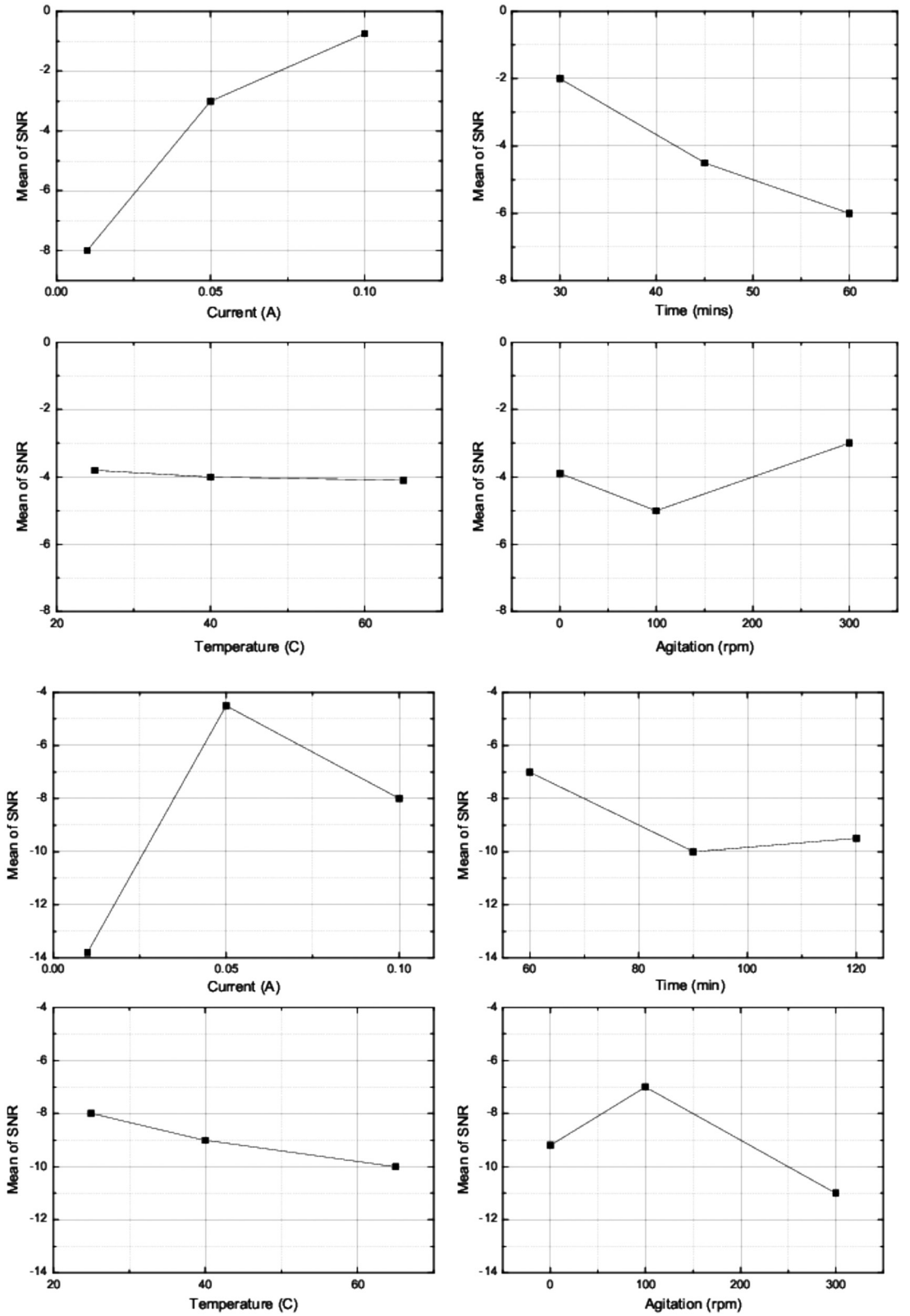

Fig. 3 Mean SNR values corresponding to each control parameter.

2.1.2 *ECD of Cu into trenches*

In order to promote faster plating, we started with the highest current of 100 mA selected from the control parameter values introduced in Table 3. No increased temperature or agitation were used since they had little influence over the deposition rate. Initially, a seed layer of 20 nm Ti (acting as an adhesive layer) and a 100-nm Cu layer were deposited through e-beam evaporation before performing the ECD of Cu into the trenches. This resulted deposition is shown in Fig. 5. The copper has grown only at the top of trenches with

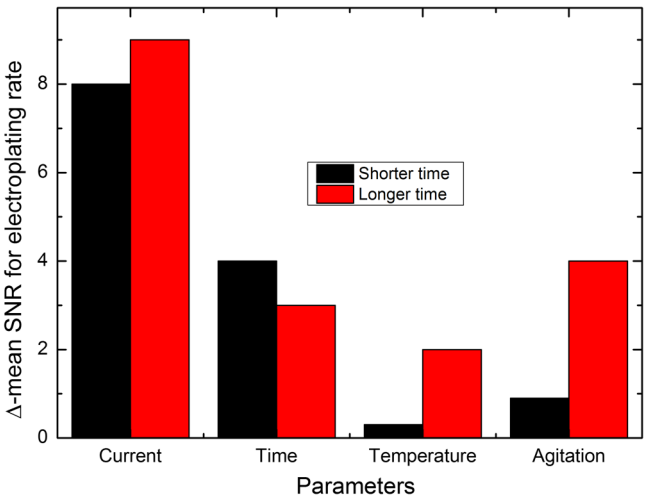

Fig. 4 Difference in mean SNR values for each parameter in the copper electrodeposition experiment with orthogonal design and analyzed using Taguchi method.

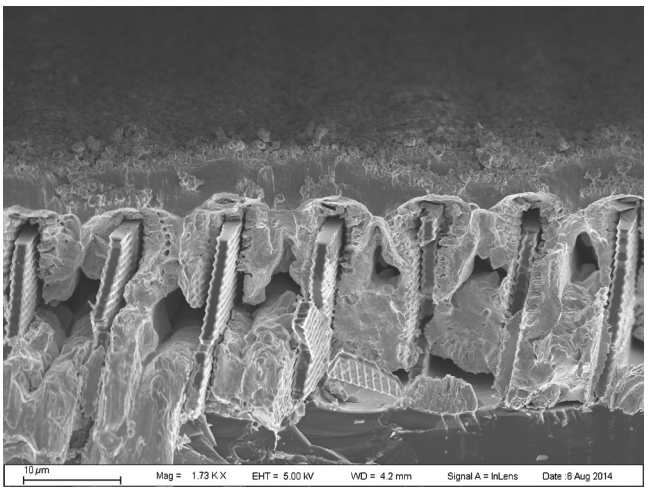

Fig. 6 Filled trenches after using a thicker seed layer with agitation during ECD, but voids were still present inside the filled trenches.

no deposition at the bottom or from the trench side walls. Subsequent investigations showed that this was due to poor seed layer coverage throughout the trenches. Unlike TSVs, in our case the trench is a blind via in which the electrical connection is ensured by good coverage of the seed layers over both the trench walls and the bottom of the trench as mentioned in Sec. 1. This led to the deposition of copper on the top of the trench walls with almost no deposition inside the trenches where the seed layer was almost absent, resulting in the mushroom-like formations at the top of trenches. Additionally, because there was very little bottom-up growth, it was suspected that the electrolyte was having difficulty in accessing these HAR trenches since no agitation was provided.

For the second iteration, a thicker Cu seed layer of 300 nm was used, together with agitation at 100 rpm during electroplating using a magnetic stirrer. This solved the problem of the trenches being unfilled; however, voids still appeared, as shown in Fig. 6. These voids are due to unequal potential distribution caused by varying seed layer thickness along the trench length. The Cu deposition rates are higher at the places with a larger potential drop, such as at the edges and the corners at the top of the trench where the seed layer thickness is thinner than at the trench sidewalls. The lateral growth at the mouth of the trenches is thus faster resulting in sidewall growth at the mouth of the trench that pinches off the trench and finally causes the void at the center.

To solve the problem of poor coverage resulting in varying resistance, the seed layer deposition was done using sputtering instead of e-beam evaporation. Additionally, the thickness of the seed layer was also increased to 500 nm to ensure a more conformal deposition with better step coverage. Properly filled trenches were finally obtained as shown in Fig. 7. This recipe guaranteed balanced lateral and bottom growth causing proper filling up of the trench walls.

In order to further accelerate the deposition rate, it was decided to increase the current to 500 mA but this again caused internal voids, as shown in Fig. 8. This can be again attributed to higher deposition rates at the top and opening of the trenches which has increased now due to the higher current (which translates to higher current density). However,

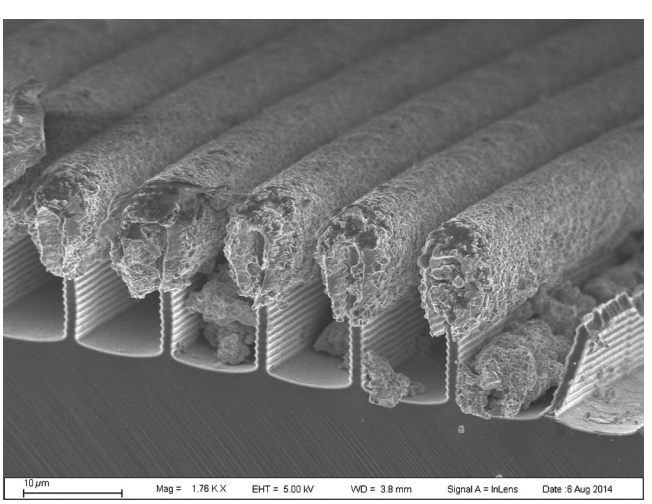

Fig. 5 Deposition of copper only at the top of the trenches indicating lack of Cu seed layer inside the trenches.

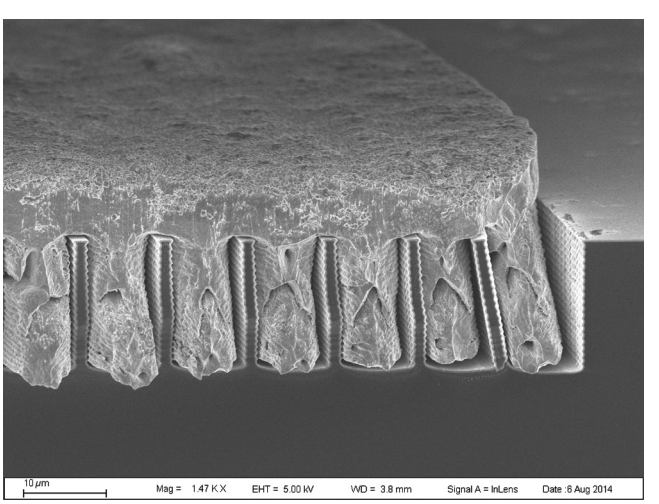

Fig. 7 Properly filled trenches after increasing the Cu seed layer thickness to 500 nm.

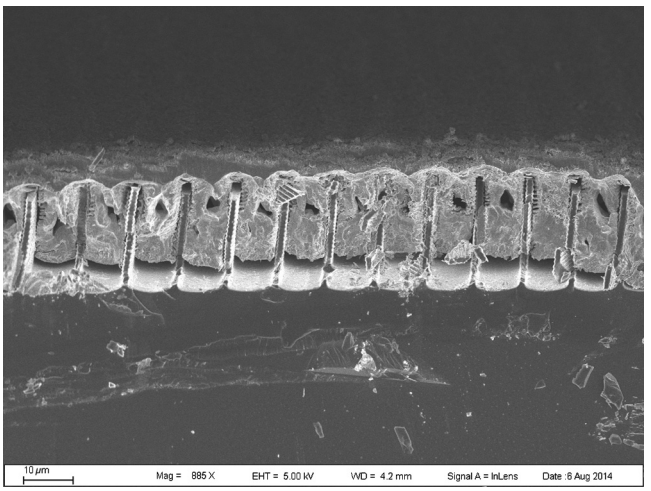

Fig. 8 Voids reappear once the current value is increased to 500 mA.

it can be noticed in Fig. 8 that the voids are now near the top of the trenches. This indicates that although initially the bottom and lateral growth was quite balanced for most of the trench depth, near the top the lateral growth was higher due to higher current (density) thus resulting in the observed voids.

2.2 *Wet Etching to Remove the Cu Overburden*

The removal of excess Cu resulting after electroplating is generally done through CMP with a Cu removal rate of around 10 nm/min.[41] However, this process requires complex optimization of many parameters, is time consuming and cannot be used by those who do not have a CMP setup at their disposal. Here, we present a procedure of Cu overburden removal using industry grade sodium persulfate where the etching is as high as 3 to 8 nm/s, depending on the specific process parameters, as will be seen later. The reaction involved in the etch process is given as

$$Cu + Na_2S_2O_8 = CuSO_4 + Na_2SO_4. \quad (2)$$

Although other procedures of Cu wet etch have been reported in Refs. 42–45 before, ours is the first one that reports wet etching using sodium persulfate solution alone avoiding the usage of any toxic or acidic agents. Reference 44 has reported controlled wet etching of copper overburden obtained from electroplating of TSVs, their etching solution consisted of sulfuric acid and also required special arrangement of a capsule chamber for the Cu-etching process. However, in our case, we avoided the use of any acid as determined from the orthogonal DoE as described below and no special chamber-typed design was required. Our

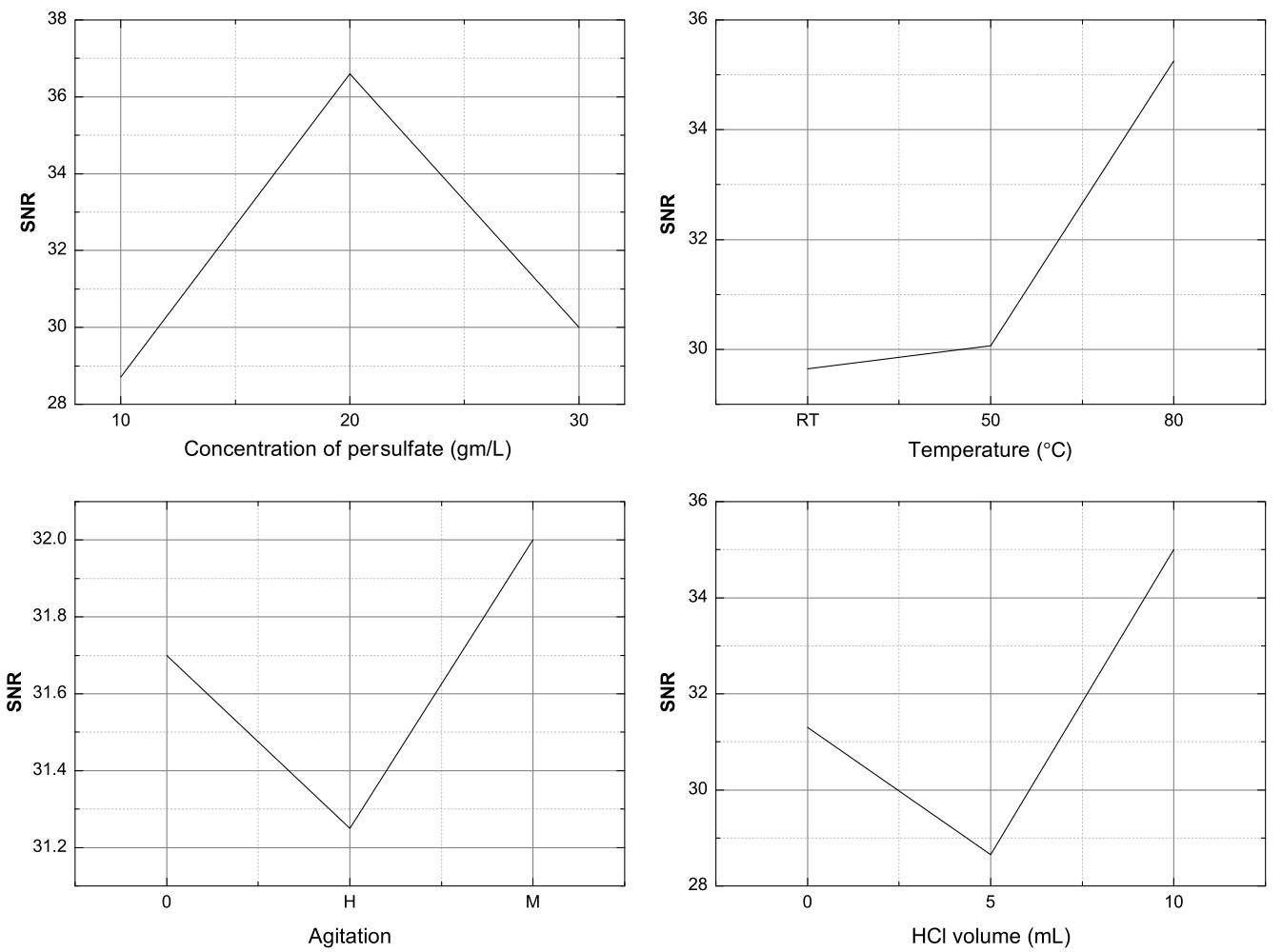

Fig. 9 Mean SNR value corresponding to each control parameter.

process involves immersing of the wafer in the etchant solution and after a specific time taking out the wafer followed by thorough rinsing. Furthermore, the process described in Ref. 44 involves differential etch rate between Cu protrusion from TSVs and Cu over burden outside TSVs to achieve the selectivity while in our case the scenario is totally different where a blanket universal cover of Cu overburden is formed over the Cu microcoil and this has been removed by sodium persulfate etching the parameters of which has been determined precisely using the orthogonal DoE. The comparison table for existing Cu wet etchants given in Ref. 42 shows the common Cu etchants such as $FeCl_3$ and $CuCl_2$ act effectively above the room temperature while in our case it will be seen successful controlled etching has been achieved at room temperature. Furthermore, Ref. 43 shows that between the two most common Cu wet etchants viz. $FeCl_3$ and $CuCl_2$ though $FeCl_3$ has a higher etch rate it produces a rough surface while for $CuCl_2$ the toxicity is high and etch rate drastically reduces with time. Reference 45 reports a Cu-etching solution that is rather complex consisting of organic complexing agents, peroxide, and acids. Therefore, compared to these reported Cu wet-etching processes, our etching process is extremely simple, controlled, happening at a room temperature, and nontoxic with formation of copper sulfate as the biproduct.

However, due to lack of the literature in the wet etching of copper using sodium persulfate first, the optimum recipe to etch Cu was determined using orthogonal DoE. The DoE was carried out by considering four input parameters as seen in Table 4 and the etching rate was determined by noting the time of etching for a Cu layer 2 μm thick. For the agitation, three levels were set, viz. no agitation (0), medium agitation (M), and high agitation (H). The value of M is half of the maximum rotational speed of the magnetic stirrer that was possible and H is the highest speed. The results obtained from this orthogonal DoE using the Taguchi method is given in Fig. 9. The SNR is again calculated according to the equation mentioned in Eq. (1). The performance parameter y in this case is the etch rate of Cu. Here also for each experiment i indicated in the first column of Table 4, three trial experiments are performed and hence $N_i = 3$ and $u = 1$, 2, and 3. Figure 10 shows the difference in SNR of etching rate for the DoE results obtained with the different values considered for the control parameters. As seen from Fig. 10, agitation has the least effect on the etching rate, while the addition of HCl and temperature have the second and third strongest effects. The persulfate concentration (gm/L) has the highest effect, as expected.

Unfortunately, any microvoids present in the Cu filling of the trenches allowed seeping in of the etchant causing enlargements of the voids and dissolving the Cu traces.

This was due to the fact that the highest level of persulfate concentration was chosen along with the highest amount of HCl from Table 4 and the solution was heated at 80°C. This aggressive etching, though fast, also removed the copper inside trenches, as shown in Fig. 11. In order to eliminate this

Table 4 Different levels of the selected process variables and their combination used in orthogonal DoE to determine etch rat of copper using sodium persulfate.

Exp #	Persulfate concentration (gm/L)	Temperature (°C)	Agitation	Volume of HCl (ml)
1	10	*RT*	0	0
2	10	50	*M*	5
3	10	80	*H*	10
4	20	*RT*	*M*	10
5	20	50	*H*	0
6	20	80	0	5
7	30	*RT*	*H*	5
8	30	50	0	10
9	30	80	*M*	0

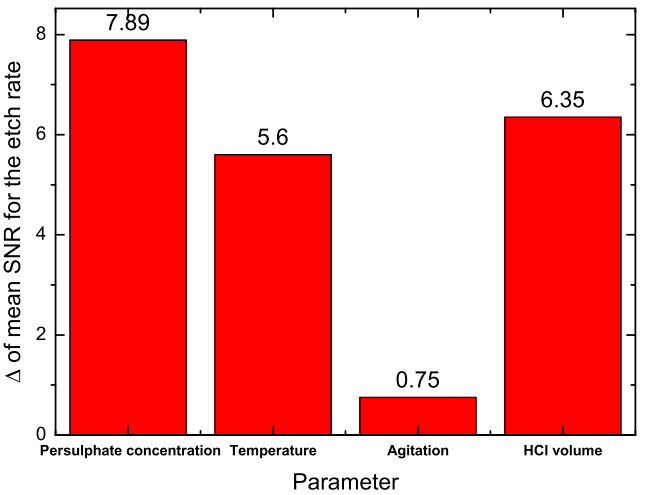

Fig. 10 Difference in SNR values for the parameters of the persulfate wet-etching DoE results evaluated through the Taguchi method.

Fig. 11 Uncontrollable over etching by sodium persulfate inside coil trenches.

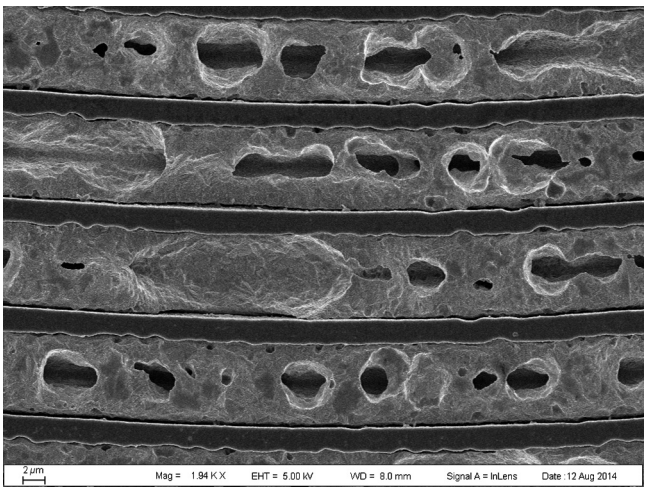

Fig. 12 Wet etch through existing holes or voids on the Cu trace.

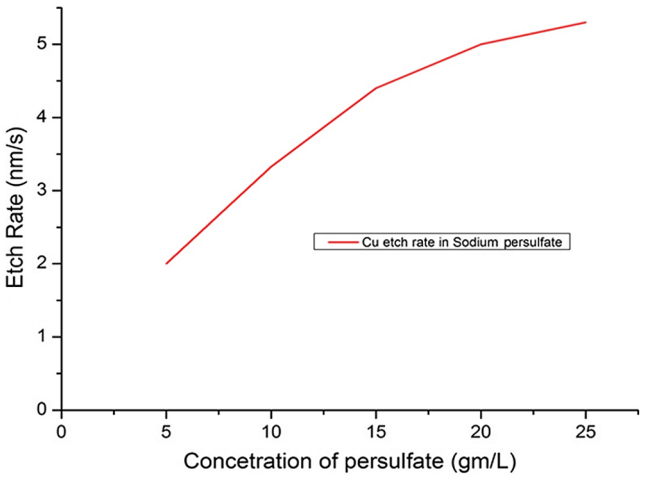

Fig. 14 Etch rate of Cu with different persulfate concentrations.

problem, the HCl addition was avoided, amount of persulfate was reduced to 10 gm/L (the lowest level as in Table 4), and the temperature was kept constant at 80°C. Still, due to the agitation and the high temperature, the persulfate solution seeped into any voids or cracks present in the copper filled trenches as shown in Fig. 12. Next, only room temperature was used, which yielded good results with controlled etching and well-defined traces for the microcoils with 3.5 and 15.5 turns, as shown in Fig. 13.

For this optimized recipe of the Cu-wet etch using sodium persulfate with no agitation and added HCl at room temperature, the etch rate with persulfate concentration is given in Fig. 14. We used the 10 gm/L of persulfate concentration to achieve the desired controlled etching of Cu overburden corresponding etch rate of which is 3.5 nm/s. The persulfate tends to oxidize the underlying thin adhesive metal layer of Ti which is seen during resistance measurement as it shows a high electrical resistance indicating Ti was effectively oxidized and hence the adjacent coil turns were not electrically short.

3 Electrical Measurements

I–V measurements were performed on microcoils of both 3.5 and 5.5 turns. A first set of *I–V* measurements was done under SEM through nanoprobing. The measurement setup is shown in Fig. 15.

The measurements were carried out both before and after annealing at 400°C in the presence of argon and hydrogen which would chemically reduce any copper oxide present and also enlarge the grain size. Previous reports[46,47] documented the formation of copper (II) and (I) oxide in deposited copper which significantly increases their sheet resistance to high values in the range of 10^6 to 10^8 Ω/square. Hence, hydrogen was selected to reduce the copper oxide present in the electroplated copper and at the same time anneal it at a higher temperature to produce a larger grain size of Cu.[48] However, Refs. 49–51 report that at a higher temperature the diffusivity of hydrogen inside Cu is very high leading to hydrogen atom inclusion inside Cu voids. Therefore, it was decided to use a lower temperature. Reference 52 suggested a temperature of 400°C and an argon environment is to be kept in order to prevent hydrogen from

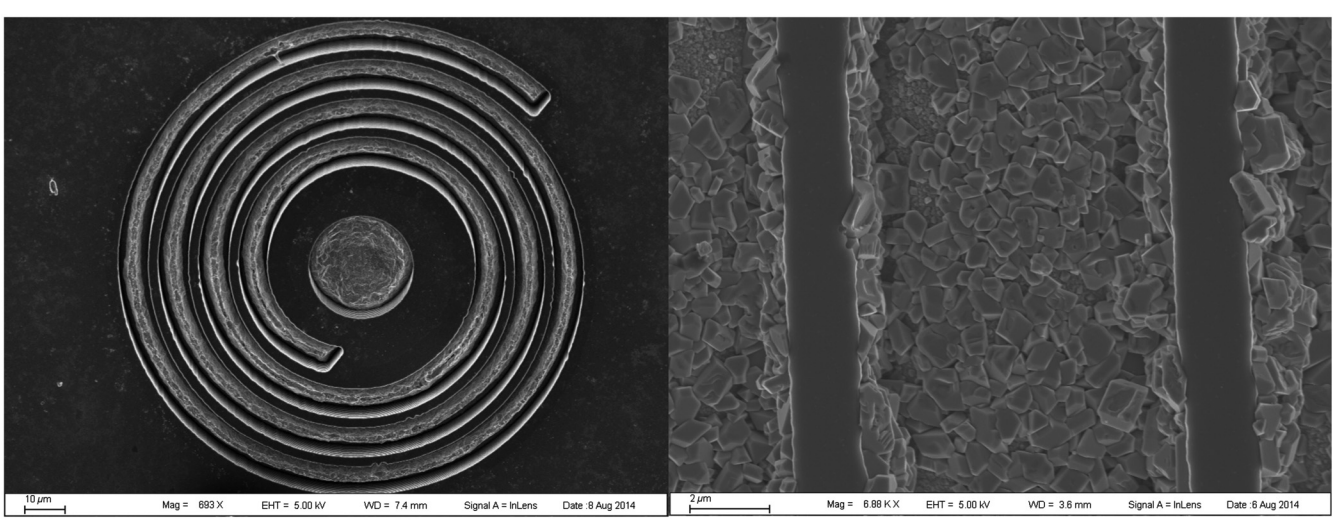

Fig. 13 Microcoils after successful wet etching removal of the copper overburden.

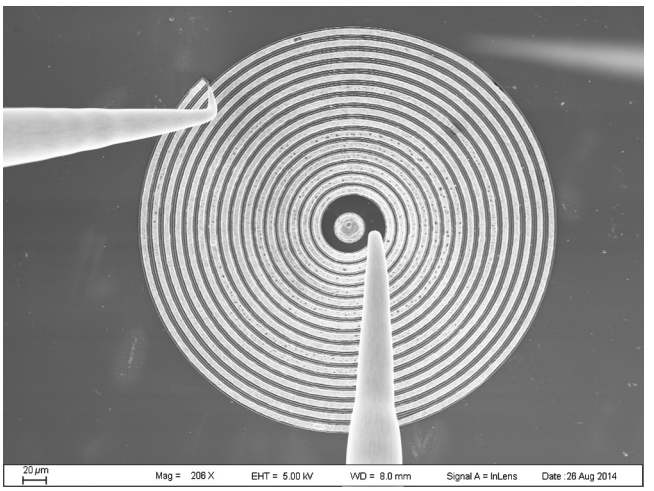

Fig. 15 Nanoprobing of a microcoil under SEM to measure the *I–V* characteristics.

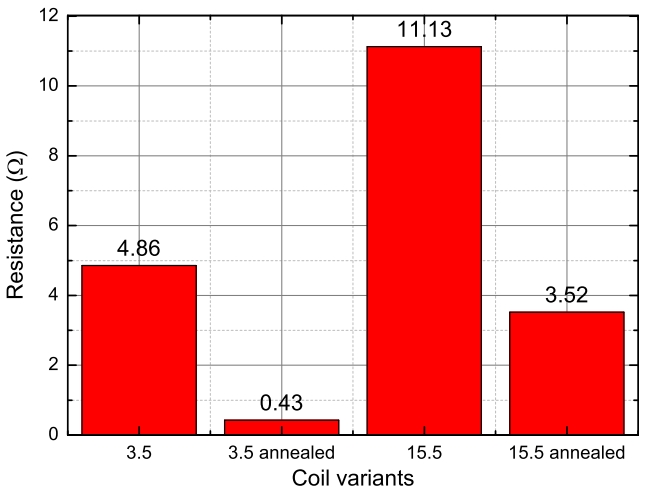

Fig. 16 Resistance values of microcoils with 3.5 and 15.5 turns before and after annealing at 400°C in Ar and H_2.

forming excess voids through formation of water vapor from the trapped oxygen which then escapes from the copper. Also, argon helps in keeping a passive environment in the presence of flammable hydrogen in the chamber. Hence, in the annealing, the hydrogen flow rate was kept low and linearly increased from 10 to 50 SCCM while the argon flow rate was kept constant at 100 SCCM and the temperature was ramped up to 400°C for 90 min. The plot in Fig. 16 shows the average resistance of each variant before and after annealing. As seen from the plot the lowest value of resistance we have obtained is 0.43 Ω which is pretty low compared to the reported values of blind via coils in Table 1. Only Refs. 14 and 15 have a lower resistance since their cross-sectional area is very large owing to the fact that the coil turns are obtained from TSV filling. But the disadvantage of these two microcoil structures obtained through TSV lies in the fact that the backside of the Si wafer cannot be anymore processed as described previously in Sec. 1. Q factors were measured to be 3×10^{-3} and 4.62×10^{-2} for 3.5 and 15.5 turn coil, respectively, at the very low frequency of only 5 MHz.

4 Conclusion

The work reported here carefully analyzes each step of fabricating a microcoil in a silicon substrate through electrodeposition of copper in blind HAR trenches, followed by controlled wet-etching removal of the excess copper. The ECD of copper were achieved inside continuous long blind HAR trenches etched by DRIE in a Si substrate, not in isolated trenches such as TSVs or TPVs. The challenges associated with filling with Cu such as long blind vias are reported and solved by modifying external nonchemical parameters. After successful copper deposition inside the trenches, a very efficiently controlled wet-etching procedure was developed to remove the Cu overburden. Finally, the obtained resistance was reduced after annealing at 400°C in the presence of a mixture of argon and hydrogen.

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