A Low-Jitter Polyphase-Filter-Based Frequency Multiplier With Phase Error Calibration

J. K. Yin and P. K. Chan

***Abstract*—A new low-jitter polyphase-filter-based frequency multiplier incorporating a phase error calibration circuit to reduce the phase errors is presented. Designing with a multiplication ratio of eight, it has been fabricated in a 0.13-μm CMOS process. For input frequency of 25 MHz, the measured jitter is 2.46 ps (rms) and $\pm$9.33 ps (pk–pk) at 200-MHz output frequency, while achievable maximum static phase error of the calibration circuit is 2.4 ps. The calibration leads to the normalized rms jitter of 0.049%.**

***Index Terms*—Calibration, delay-locked loop (DLL), frequency multiplier, phase-locked loop (PLL), polyphase filter (PPF).**

I. Introduction

TIMING jitter is an important parameter in design consideration for most of high-speed digital and communication systems. There are two common frequency multiplier architectures: 1) phase-locked loop (PLL) [1]; and 2) delay-locked loop (DLL) [12]. However, the PLL suffers from jitter accumulation effect due to narrow loop bandwidth [3]. Loop bandwidth maximization is limited by the stability requirement, which is at least ten times smaller than reference frequency [2]. Meanwhile, jitter in DLL does not accumulate from one cycle to another cycle of reference clock period, hence exhibiting better jitter result [4]. However, due to the cascade structure of delay chain in DLL, the jitter of delay cell caused by supply, substrate and device noise will accumulate in the chain. Moreover, mismatch of each delay cell and charge pump current will introduce static phase error for each clock edge defined from DLL, deteriorating the jitter performance of DLL. In this brief, a polyphase filter (PPF)-based frequency multiplier is proposed to achieve better jitter performance. First, cascade structure of delay chain is replaced with a passive RC PPF that defines the clock edges from crystal oscillator for frequency multiplication. Second, a phase error calibration (PEC) circuit, independent of delay sensing mismatch, is proposed to reduce the static phase errors contributed by the PPF and devices mismatch.

II. Proposed Frequency Multiplier

Fig. 1 shows the architecture of the proposed frequency multiplier. It consists of a PPF, eight units of voltage-controlled delay cell (VCDC), an edge combiner (EC), and a PEC. The reference frequency of the frequency multiplier is generated by a crystal oscillator. This is a low-jitter differential sine-wave source X_{o1} and X_{o2}. From this differential sine wave, PPF will generate four clock phases Ph_1 to Ph_4. Each clock phase is separated by 90° in phase. By applying the differential clock phases from PPF to VCDC, eight single-ended rail-to-rail clock edges ϕ_0 to ϕ_7, for frequency multiplication purpose will be generated. The functions of VCDC are: 1) to convert differential clock phases from PPF to single-ended rail-to-rail clock edges for EC; and 2) to provide delay variation for calibration purpose via control voltage V_{c1} to V_{c7}. Meanwhile, V_{c0} is biased by a fixed reference voltage V_{ref}. This is because the first clock edge ϕ_0 is selected as reference clock edge in calibration. Finally, the eight clock edges from VCDC will be combined by digital EC to generate multiplication frequency f_{out}.

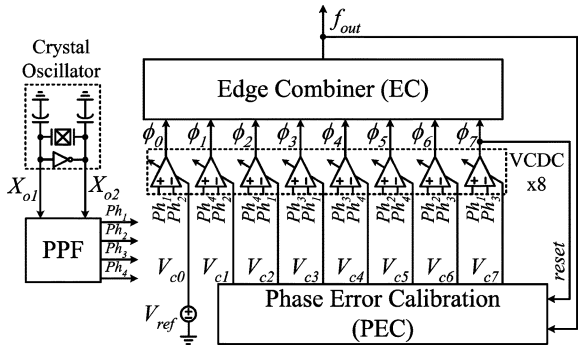

Fig. 1. Proposed architecture of PPF-based frequency multiplier.

However, the PPF and devices mismatch will cause unequal phase spacing between adjacent clock edges. The static phase error will induce deterministic jitter at multiplication frequency f_{out}. Therefore, a PEC circuit is employed. The details of the PEC circuit will be described in Section II-D.

The advantage of this architecture is that the clock edges, defined from a passive RC PPF and a VCDC, eliminates the use of cascade structure in delay chain. Therefore, the jitter of the clock edges is only contributed by the VCDC and thermal noise from resistors in PPF. Since VCDC provides delay variation for calibration, the delay of VCDC can be minimized just for covering the maximum phase error at clock edges. Therefore, the VCDC has better noise immunity to supply and substrate noise, which help to minimize jitter of clock edges. Meanwhile, the deterministic jitter caused by static phase error is minimized by PEC.

A. PPF

A passive RC PPF [5], [6] is used as clock phases generation circuit in this frequency multiplier. To achieve a functional PPF, the RC time constant of PPF must equal to $1/[2 \times \pi \times (\mathrm{input\ frequency})]$, where the targeted input frequency for this

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J. K. Yin is with Institute for Infocomm Research, Singapore 117674 (e-mail: yinjk@i2r.a-star.edu.sg).

P. K. Chan is with Nanyang Technological University, School of Electrical and Electronic Engineering, Singapore 639798 (e-mail: epkchan@ntu.edu.sg).

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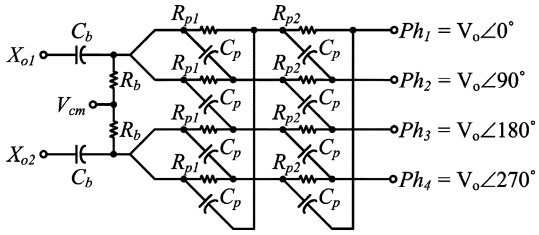

Fig. 2. Two-stage passive RC PPF.

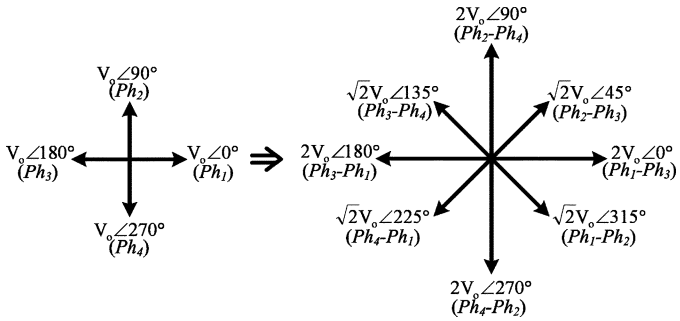

Fig. 3. Phasor diagram of the PPF output and eight differential clock phases.

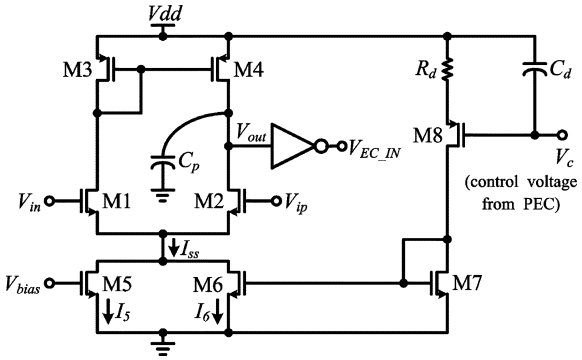

Fig. 4. Schematic circuit of VCDC.

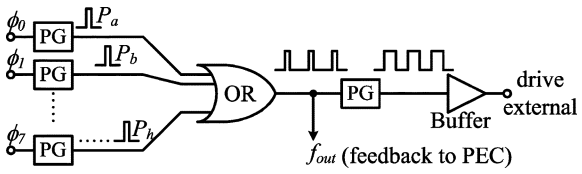

Fig. 5. EC.

design is 25 MHz. However, the RC time constant variation in CMOS process can be as large as $\pm 20\%$. This will cause the phase error of single-stage RC PPF as large as ± 609 ps. Therefore, two stages of passive RC PPF, as shown in Fig. 2, are needed to cover the process variation. The first stage and second stage of the PPF have RC time constant of $1/(2\times\pi\times 30\ \text{MHz})$ and $1/(2\times\pi\times 20\ \text{MHz})$, respectively. The two-stage PPF reduces the phase error to ± 65 ps. In this design, R_{p1}, R_{p2}, and C_p are 2.2 kΩ, 3.3 kΩ, and 2.4 pF, respectively.

The four clock phases generated by PPF are $\text{Ph}_1 = V_\text{o}\angle 0°$, $\text{Ph}_2 = V_\text{o}\angle 90°$, $\text{Ph}_3 = V_\text{o}\angle 180°$, and $\text{Ph}_4 = V_\text{o}\angle 270°$. Eight output clock edges can be generated by taking the differential of the clock phases. The phasor diagram of the PPF output clock phases and eight differential clock phases are shown in Fig. 3.

However, in practical implementation, there is a mismatch of the clock phases generated from PPF due to several reasons. First, the phase shift of reference signal from crystal oscillator, X_{o1} and X_{o2}, are more than 180° due to the delay of inverter in oscillator circuit. Second, the harmonic from the reference signal will also increase the mismatch of the clock phases. Third, the variation of RC time constant in PPF will also contribute to the clock phases mismatch although two stages of passive RC PPF are used. Forth, the crossing points of differential clock phases from PPF occur at different common voltage level. Therefore, the propagation delay of each VCDC is different, hence contributing to the clock edges mismatch. In this design, post layout simulation of crystal oscillator, PPF, VCDC, and EC shows the maximum phase error over the process corner at multiplication frequency, f_out, is ± 250 ps.

The only noise source from PPF is that of thermal noise of resistor. The total noise power is proportional to the resistor value. The details of the PPF noise analysis will be shown in Section III. The minimum value of resistor is limited by gain margin of crystal oscillator. To make sure the crystal oscillator can startup properly, the optimum resistor value has to be chosen carefully.

B. VCDC

The schematic of VCDC is shown in Fig. 4. Transistors M1-M6 form a differential amplifier with an active current mirror load. The differential amplifier will convert differential clock phase from PPF to a single-ended rail-to-rail output clock edge after passing through the inverter for edge combination. To optimize the noise performance, the gain of the differential amplifier is as high as possible to reduce the device noise contribution to the output jitter. A larger size of transistor M1 and M2 are used to minimize the flicker noise contribution. After optimization, noise contributed by VCDC is minimal.

Since each phase clock from PPF is a large signal, the differential amplifier exhibits slewing behavior. Thus, the delay of the differential amplifier can be approximated as $V_p(C_p/I_{ss})$, where I_{ss}/C_p is the slew rate, V_p is one half of the full output swing, and C_p is the effective capacitance associated at the output of the differential amplifier. I_{ss} is the total tail current contributed by the static biasing current I_5 and dynamic biasing current I_6. I_5 is fixed to avoid zero tail current when V_c is too high. Thus, the delay variation of VCDC for calibration can be achieved by storing the charge in MIM capacitor C_d, defining the V_c. In this design, the delay variation of the VCDC is ± 500 ps, in which ± 250 ps of the delay is allocated to cover the maximum phase error at multiplication frequency f_out and the remaining delay of ± 250 ps is treated as over-design margin.

C. EC

Fig. 5 shows the digital EC used in the frequency multiplier. Each of the eight clock edges, ϕ_0 to ϕ_7, generated from VCDC will pass through a digital pulse generator (PG) to generate a series of narrow pulsewidth signal, P_a to P_h, with the pulsewidth of around 1 ns. All this narrow pulsewidth signals will be combined by an OR-gate to generate multiplication frequency f_out.

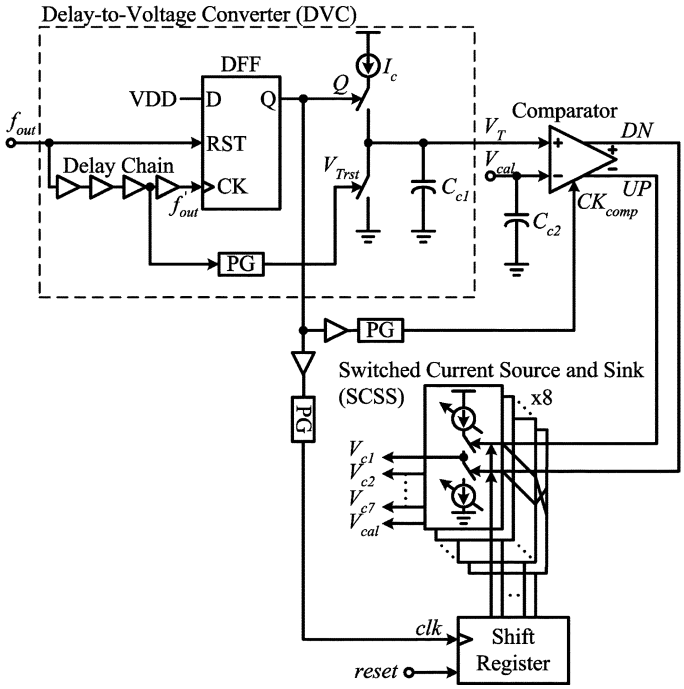

Fig. 6. Architecture of the PEC circuit.

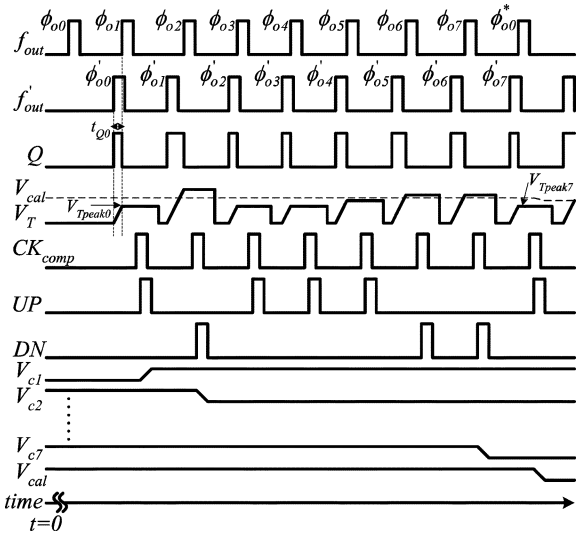

Fig. 7. Operation waveforms of the PEC circuit.

The $f_{\rm out}$ from OR-gate will be fed to PEC circuit for calibration. To achieve a multiplication frequency signal with duty cycle close to 50%, the $f_{\rm out}$ will pass through another PG, which will generate a signal with pulsewidth close to half period of $f_{\rm out}$. For measurement purpose, an output buffer with capability to drive a 50-Ω instrument load is used.

D. PEC

Fig. 6 shows the architecture of the PEC circuit. The PEC consists of one delay-to-voltage converter (DVC) and one comparator, which acts as delay sensing circuit to measure the delay of the adjacent clock edges from the multiplication frequency, $f_{\rm out}$. Furthermore, there are eight units of switched current source and sink (SCSS) to update the respective control voltage of VCDC ,V_{c1} to V_{c7}, and also the calibration voltage of comparator $V_{\rm cal}$.

The operation of PEC circuit is illustrated in Fig. 7. The multiplication frequency $f_{\rm out}$ consists of repeated eight clock edges ϕ_{o0} to ϕ_{o7}, which are generated by clock edges ϕ_0 to ϕ_7 from VCDC. First, clock edge of $f_{\rm out}$, ϕ_{o0}, will reset the D-flip-flop (DFF). Then, the 4-ns delay clock edge ϕ'_{o0} will clock the DFF and the output data Q will go high. Second clock edge of $f_{\rm out}$, ϕ_{o1}, will reset the DFF again. The signal Q will go low. t_{Q0} is the pulsewidth of Q that represents the delay between ϕ'_{o0} and ϕ_{o1}. Similarly, different clock phase pairs have their respective pulsewidth. The pulse signal Q will switch on the current source I_c to charge the C_{c1}. Therefore, the output of DVC, V_T, will be charged to a certain voltage level $V_{\rm Tpeak0}$. The $V_{\rm Tpeak0}$ can be expressed as t_{Q0} (I_c/C_{c1}).

By inserting a 4 ns delay chain, the delay between ϕ'_{o0} and ϕ_{o1} can be reduced from 5 to 1 ns. The t_{Q0} will be reduced by five times. Since the mean value of $V_{\rm Tpeak0}$ is designed at around 1 V, by reducing the t_{Q0}, more headroom is permitted to boost the I_c/C_{c1} and sensitivity of DVC.

The delay information is translated to voltage domain. This voltage level will be compared with a calibration voltage, $V_{\rm cal}$, when clock signal of comparator, $CK_{\rm comp}$, is high. If the delay of ϕ'_{o0} and ϕ_{o1} is shorter, the t_{Q0} is smaller. $V_{\rm Tpeak0}$ becomes lower than $V_{\rm cal}$, the comparator negative output will generate a pulse signal, UP, while signal DN will remain low. The UP signal will switch on the current source of SCSS to charge the capacitor in VCDC, hence increasing the V_{c1} to increase the delay of VCDC. After that, the signal V_T will reset to zero by V_{Trst} for next cycle of the delay sensing operation. This operation will continue until clock edge ϕ'_{o6} and ϕ_{o7}. Since all delay is calibrated according to arbitrary selected calibration voltage, $V_{\rm cal}$, therefore, all clock edges ϕ_{o1} to ϕ_{o7} have the same delay. However, the delay of last clock edge ϕ_{o7} and first clock edge of next cycle ϕ^*_{o0} is different with others. To make all the clock edges spaced equally, $V_{\rm cal}$ will be updated according to the delay sensed from clock edge ϕ_{o7} and ϕ^*_{o0}. If the $V_{\rm cal}$ is higher than the targeted $V_{\rm cal}$, the delay of each adjacent clock edge from ϕ_{o0} to ϕ_{o7} will be higher than 5 ns while the delay of clock edge ϕ_{o7} and ϕ^*_{o0} will be smaller than 5 ns. Therefore, the $V_{\rm Tpeak7}$ of this stage will be smaller than $V_{\rm cal}$. By reversing the UP and DN signal, the UP signal generated by comparator will switch on the current sink of SCSS to discharge the capacitor C_{c2} hence decreasing the $V_{\rm cal}$. This feedback operation will make all clock edges ϕ_{o0} to ϕ^*_{o0} spaced equally. There is no stability issue due to the first-order bang–bang feedback loop. This operation is synchronized by reset signal from ϕ_7.

PEC is a continuously calibration loop, so it will contribute noise to the frequency multiplier. However, due to the bang–bang feedback loop of the PEC, the noise contribution can be minimized by reducing the current source or sink in SCSS [7]. In initial stage, the current source or sink in SCSS is 250 μA to reduce the lock time. At steady state, the current will be reduced to 1 μA to minimize the PEC noise contribution.

The advantage of this PEC is only one delay sensing circuit being used to measure the delay mismatch of clock edge. Therefore, any mismatch of current source I_c, capacitor C_{c1}, and offset of comparator will be seen equally for every clock edge delay sensing. The calibration only involves in delay comparison, therefore, mismatch and offset will be cancelled by each

other. Furthermore, the calibration is sensing the output of frequency multiplier, so any mismatch due to circuit in EC and routing from VCDC to EC will be detected and calibrated.

III. PPF Noise Analysis and Comparison

By applying the Kirchoff's Laws on the PPF circuit, each transfer function of noise sources to the differential clock phase output can be found. The differential clock phase output noise contributed by all resistors in PPF, V_N, can be obtained as

$$V_N = 2 \cdot \sqrt{\frac{kT}{C_p}}. \tag{1}$$

The same technique can be used to find the output amplitude $|V_o|$, slew rate, and hence the jitter of the output. In the analysis, we assume $2\pi R_{p1} C_p \cong 2\pi R_{p2} C_p \cong 1/f_i$, where f_i is the input frequency.

Referring to Fig. 3, the first, third, fifth, and seventh differential clock phase has the same amplitude, so the jitter is Δt_{p1}. The remaining differential clock phase jitter is Δt_{p2}. Thus, the PPF-based frequency multiplier output jitter Δt_{po} contributed by eight differential clock phases can be expressed as

$$\begin{aligned}\Delta t_{po} &= \sqrt{\frac{(\Delta t_{p1})^2 + (\Delta t_{p2})^2 + (\Delta t_{p1})^2 + \cdots + (\Delta t_{p2})^2}{8}} \\ &= \sqrt{\frac{2kT}{\pi f_i |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{\rm rms}}} \cdot \left[\sqrt{\frac{4 \times 2^2 + 4 \times (\sqrt{2})^2}{8}}\right] \\ &= \sqrt{\frac{6}{\pi}} \cdot \sqrt{\frac{kT}{f_i |V_i|_{pp}}} \cdot \frac{1}{\sqrt{I_{\rm rms}}}\end{aligned} \tag{2}$$

where $|V_i|_{pp}$ and $I_{\rm rms}$ are input peak-to-peak amplitude and current consumption of PPF, respectively.

In conventional DLL, a delay cell jitter Δt_{d1} can be calculated from [8]. The variance of the clock edge jitter is proportional to the number of delay cell cascaded. Therefore, the DLL-based frequency multiplier output jitter Δt_{do} can be expressed as

$$\begin{aligned}\Delta t_{do} &= \sqrt{\frac{(\Delta t_{d1})^2 + 2 \cdot (\Delta t_{d1})^2 + \cdots + 8 \cdot (\Delta t_{d1})^2}{8}} \\ &= a_v \xi \cdot \sqrt{\frac{kT}{f_i V_{pp}}} \cdot \frac{1}{\sqrt{8 I_{ss}}} \\ &\quad \cdot \sqrt{\frac{1+2+3+4+5+6+7+8}{8}} \\ &= 3\sqrt{2} \cdot \sqrt{\frac{kT}{f_i V_{pp}}} \cdot \frac{1}{\sqrt{I_T}}\end{aligned} \tag{3}$$

where V_{pp}, I_{ss}, and $I_T = 8\, I_{ss}$ are one half of the full differential output swing, tail current of a delay cell and total tail current of eight delay cells respectively. Note that it is assumed the typical value of $a_v \xi \cong 2$, where $a_v = V_{pp}/(V_{GS} - V_T)$ and ξ are small-signal gain of delay cell and noise contribution factor respectively.

From (2) and (3), it is clear that the PPF-based frequency multiplier has better jitter performance under same current consumption and same V_{pp} and $|V_i|_{pp}$ value.

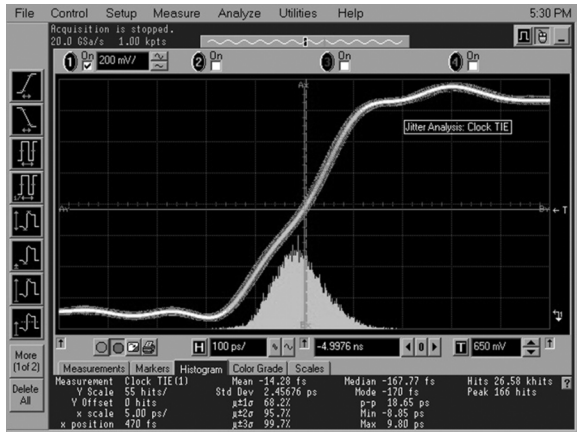

Fig. 8. Measured TIE jitter at 200 MHz.

TABLE I
STATIC PHASE ERROR BEFORE AND AFTER CALIBRATION

Delay Phase	Ideal Delay	Before Calibration		After Calibration	
		Measurement	Offset	Measurement	Offset
$\phi_{o0} - \phi_{o1}$	5.0000ns	4.8018ns	-198.2ps	4.9977ns	-2.3ps
$\phi_{o0} - \phi_{o2}$	10.0000ns	9.9610ns	-39.0ps	9.9978ns	-2.2ps
$\phi_{o0} - \phi_{o3}$	15.0000ns	14.8095ns	-190.5ps	14.9982ns	-1.8ps
$\phi_{o0} - \phi_{o4}$	20.0000ns	19.8872ns	-112.8ps	19.9988ns	-1.2ps
$\phi_{o0} - \phi_{o5}$	25.0000ns	24.9216ns	-78.4ps	25.0024ns	+2.4ps
$\phi_{o0} - \phi_{o6}$	30.0000ns	30.0254ns	+25.4ps	29.9982ns	-1.8ps
$\phi_{o0} - \phi_{o7}$	35.0000ns	34.8416ns	-158.4ps	34.9979ns	-2.1ps

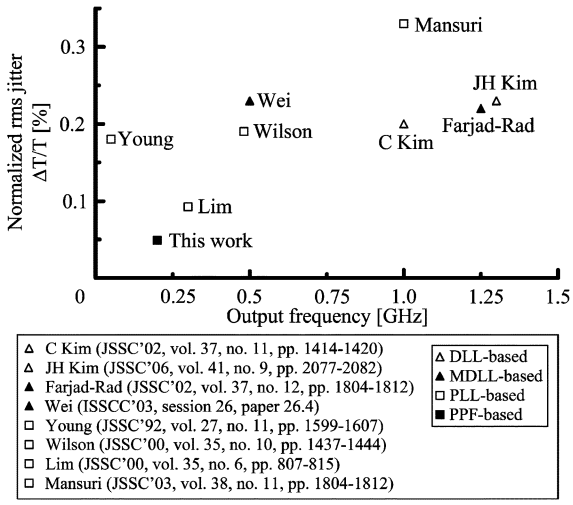

Fig. 9. Normalized jitter of frequency multipliers.

IV. Measurement Results

A 25-MHz sinusoidal reference frequency is generated from internal on-chip oscillator with an external crystal. Giving multiplication ratio of eight in design, the output frequency is 200 MHz. The prototype can generate output frequency range from 136 to 280 MHz with reference frequency of 17 to 35 MHz. The measured output time interval error (TIE) jitter histogram at 200 MHz is shown in Fig. 8. The rms and peak-to-peak TIE jitter are 2.46 and 18.65 ps, respectively. When using a 32-MHz reference crystal, the rms jitter at 256 MHz is 3.07 ps. The result is reasonably degraded due to the PEC circuit is optimized at 200 MHz in a lower power design constraint. Table I shows the static phase error of output clock phase before and after calibration. The maximum static

TABLE II
PERFORMANCE COMPARISON OF CALIBRATION CIRCUITS

Reference	[9]	[10]	[11]	[12]	This work
Process	0.25um	0.18um	0.18um	0.18um	0.13um
Supply	2.5V	1.8V	1.8V	1.8V	1.5V
Power	80mW	81mW	12mW	19.8mW	16.4mW
Area	1.6mm^2	1.03mm^2	0.05mm^2	0.07mm^2	0.49mm^2
Application	DLL-based Multi-phase clock @250MHz	DLL-based Multi-phase clock @2GHz	MDLL-based Frequency Multiplier @2GHz	DLL-based Frequency Multiplier @2GHz	PPF-based Frequency Multiplier @200MHz
Phase Error Reduction Method	Analog Calibration	Digital Calibration	Circuit Technique	Analog Calibration	Analog Calibration
Maximum Phase Error	7.1ps	3.5ps	5.0ps*	N. A.	2.4ps
Spurious Tones	N. A.	N. A.	-37dBc @2GHz	-46.5dBc @1.2GHz	-61dBc @200MHz

* Simulated result

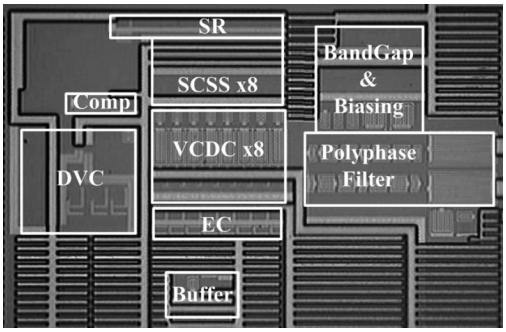

Fig. 10. Microphotograph of the proposed frequency multiplier.

phase error after calibration is 2.4 ps. Fig. 9 shows the normalized rms jitter of different type frequency multipliers having output frequency from 50 MHz to 1.3 GHz. The normalized rms jitter in this work is 0.049% at 200 MHz, which is the lowest among other frequency multiplier in nearby frequency. The performance of calibration circuit is also compared in Table II. Shown in Fig. 10, the fabricated frequency multiplier including bandgap and biasing circuit in 0.13-μm CMOS process occupies 0.49 mm^2 and consumes 16.4 mW at 1.5-V supply.

V. CONCLUSION

A new low-jitter frequency multiplier is proposed by using a passive RC PPF to define the coarse clock phase for random jitter reduction and a PEC circuit to minimize deterministic jitter arising from static phase error.

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