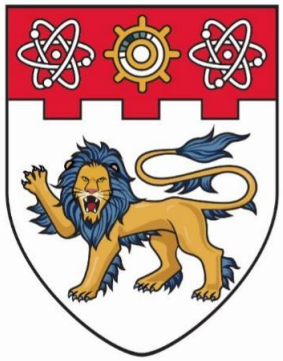

NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

A FAST-TRANSIENT DC-DC BUCK CONVERTER

DING XIANGBIN

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2018

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Summary

With the rapid development of system-on-chip integration and continuously scaling-down power supply, nowadays portable battery-powered devices have higher and sharper energy requirements. Switching converters are widely used as voltage regulators in those devices because of its high power-conversion efficiency. Due to the high-speed application and different modes operation requirements, the embedded microprocessors or digital systems operate at a higher frequency and the system need to switch between different modes more frequently. The frequently changing load induces significant undershoot/overshoot variation, which will deteriorate the overall system performance and stability. In this prospective, the fast-transient response becomes one of the key requirements for DC-DC converters in nowadays high-performance applications. Investigation of fast-transient techniques has been conducted to improve the transient response of DC-DC buck converters. A new pumping control scheme called Power-Driving-Tracked-Duration (PDTD) control is proposed to enhance the transient performance in the voltage-mode hysteretic DC-DC converters. It operates only when a large load current change is detected. Comparing with conventional counterparts, it simultaneously accelerates the transient response, reduces the undershoot/overshoot voltage and the effect of multiple undershoots/overshoots during the load current transitions. A theoretical analysis is also conducted to validate the circuit technique. The measured output voltage ripple is about $60mV_{pp}$. The obtained undershoot/overshoot settling time is 369ns/335ns in response to a 60-to-300mA/300-to-60mA load current step. The peak

efficiency is about 93%. The prototype is fabricated using TSMC 40nm CMOS process as a proof-of-concept.

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List of Glossary

PFM	Pulse Frequency Modulation
PDTD	Power-Driving-Tracked-Duration
APCA	Auxiliary Pump Current Assisted
PWM	Pulse Width Modulation
CCM	Continuous Current Mode
DCM	Discontinuous Current Mode
ECP	Error Correct Path
FFP	Feedforward Path
ESR	Equivalent Series Resistance
DASP	Digital Adaptive Slope Control
ZVD	Zero Voltage Detector
CS	Common Source
CG	Common Gate
FWS	Freewheel Switch

Chapter 1 Introduction

1.1 Motivation

In recent years, an explosive growth in portable devices, such as smartphones, tablets, laptops, digital cameras, are induced with the rapid development of system-on-chip (SoC) integration [1]–[8]. These devices combine millions of function blocks into one single chip, and the various sub-circuits in a SoC usually have different energy requirements [6], [9]. Concurrently, low power consumption has become one of the primary concerns for these portable battery-powered SoC applications [10]. Switching converters are widely used as voltage regulators in battery-powered portable devices due to its high power-conversion efficiency [1], [3], [6],[9]–[11]. Operating under different modes is an effective method of reducing the system power consumption [10], [14]–[16]. Battery-powered devices run in idle mode for most of time and work in active mode only in bursts to win high performance. Due to the high speed application requirements, the embedded microprocessors or digital systems operate at a higher frequency and the system need to switch between different modes more frequently [17]–[19]. During the dynamic loading change as well as the operation mode transfer, a massive load current change can be induced instantly [14]. A large undershoot/overshoot variation away from the designed output voltage can be generated for a significantly long period of setting time because of the transient regulation latency. The undershoot voltage may deteriorate the following sub-system performance seriously. This may cause memory loss in high speed

system. On the other hand, the overshoot voltage will heat up the chip, causing needless heat dissipation, thus extra power loss [4]. If the transient settling time is not fast enough, the high operating temperature can even damage the chip [4]. With the supply voltage decreasing and operation frequency increasing, it gives a more aggressive design requirement for the DC-DC converters with fast load regulations [20]. In this prospective, fast-transient response becomes one of the key requirements for DC-DC converters in nowadays high performance applications [11], [20]–[24].

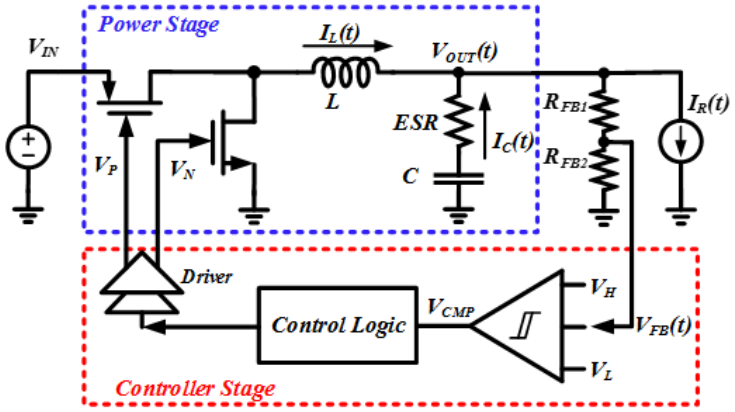

Figure 1.1. The Basic Block Diagram of a DC-DC Converter.

Figure 1.1 shows the basic block diagram of a DC-DC converter, consisting of the power stage and the controller stage. The load transient response is mainly constrained by the controller stage delay and power stage LC limitation. Various techniques have been developed to achieve fast-transient response and provide a reliable output voltage. Some of them focus on speeding up the controller stage response. Adaptive bandwidth compensation techniques [24], [25] and capacitor multiplier techniques [26], [27] are developed to extend the compensated bandwidth for voltage-mode and current-mode converters, thus speeding up the transient

response. V^2 converters introduce feedforward path to bypass the EA [14], [20], [28], but they suffer from the subharmonic oscillations. These techniques can improve the controller speed, but they also increase the system complexity. Their transient responses are limited by the OTA bandwidth through the frequency compensation to ensure stability. Hysteretic converters can offer faster transient response and better-guaranteed stability on the basis of compensation-free controller stage [11], [20], [22], [29]–[34]. Moreover, hysteretic converters can operate at PFM (Pulse Frequency Modulation) mode automatically under light load conditions to reduce the frequency-dependent switching loss, thus improving the light load efficiency [3], [5], [28], [35]. However, the ultimate transient speed of existing hysteretic converter is still constrained by the LC filter in the power stage, especially the inductor value. To overcome this limitation, an auxiliary pump current can be applied to bypass the inductor, compensating the load current change, thus enhancing the transient response [11], [12], [36]–[42]. Simple voltage-triggering pump current sources [37]–[39] are applied to guarantee a fast auxiliary current injection to enhance the transient speed. However, multiple undershoot/overshoot will be induced when the pump current sources are turned off instantly, deteriorating the expected transient performance as well as the system stability. Some control schemes such as Digital slope control schemes [40]–[43] give better turning-off control of pump current, but more complicated structures are required. Up until now, there has been very little work on the auxiliary current on-time duration to achieve the fast-transient response. This gives a design challenge to devise a simple and stable pump current control

scheme with well-controlled on-time duration.

In this work, a fast-transient hysteretic buck converter with a Power-Driving-Tracked-Duration (PDTD) control scheme for the auxiliary pump current source is proposed to improve the load transient response. In addition, a delayed-ramp is generated to prevent multiple undershoot/overshoot effect. This project is mainly designed for high-speed applications with a load current range up to 300mA [44], [45].

1.2 Objectives

The objectives of this project are given as follows:

1) To investigate the transient limitation of different buck converter topologies and existing fast-transient techniques
2) To conduct the transient analysis of the voltage-mode hysteretic buck converter and devise an improved fast-transient buck converter topology
3) To conduct the measurement of the test chips which are fabricated using TSMC 40nm CMOS technology

1.3 Contributions

The contributions of this research work are summarized as follows:

1) The investigation of an improved control scheme to obtain fast and smooth load transient performance without multiple undershoots/overshoots which are validated by the silicon prototype IC.
2) The theoretical analyses of transient response of the conventional and proposed voltage-mode hysteretic buck converters.

1.4 Organisation

This thesis is organized as follows:

Chapter one introduces the motivation as well as to state the objectives and the main contributions of this project. Chapter two describes the operating principle of DC-DC buck converters and reviews the previously-reported fast-transient converter topologies such as voltage-mode, current-mode, V^2 control, voltage-mode hysteretic control and auxiliary pump current assisted (APCA) architectures. Chapter three presents the transient analyses for the conventional voltage-mode hysteretic converters and the APCA buck converters, which are based on the representative reported scheme and the proposed PDTD control scheme. Detailed analysis is also conducted to illustrate the key advantages of the improved control scheme. Chapter four presents the building blocks of the fast-transient DC-DC buck converter together with the circuit implementations. Chapter five presents the measurement results and discusses the performance aspects of the proposed buck converter. Finally, the performance comparison is conducted with the recently-published state-of-art works to demonstrate the effectiveness of the proposed method. Chapter six gives the concluding remarks and recommendations for future work.

Chapter 2 Literature Review

In this Chapter, the fundamental operation principle of the DC-DC buck converter will be described. This is then followed by the review of other common topologies such as voltage-mode PWM converters, current-mode PWM converters, V^2 controlled converters, voltage-mode hysteretic converters and APCA converters. Their advantages and disadvantages are highlighted.

2.1 Operating Principle of DC-DC Switching Converter

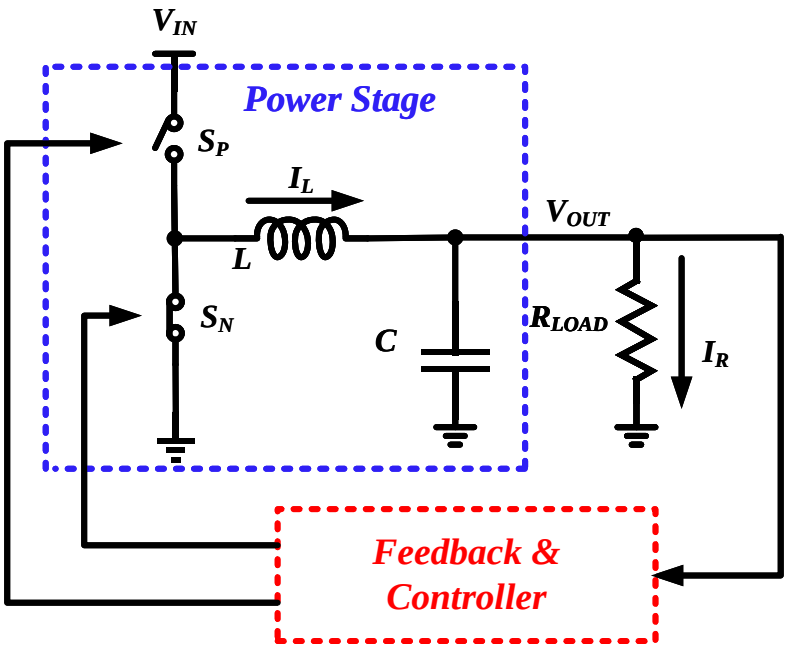

Figure 2.1. Block Diagram of a Buck Converter.

Figure 2.1 depicts the block diagram of a buck converter, which consists of the power stage and the controller stage. The power stage incorporates the PMOS/NMOS switching operation and converts the input voltage, V_{IN} to the desired stable output,

V_{OUT}. The controller regulates the output voltage through the switching operation of PMOS/NMOS. It is assumed that the power stage's components such as power switches (S_P, S_N), filter inductor (L) and output capacitor (C) are lossless. The supply voltage (V_{IN}) is modulated through the S_P and S_N switching operation to form square waveform pulse at the switching node (V_X). It will be converted to a nearly dc waveform if the LC filter is large enough [7], [8]. The voltage and current waveforms of a buck converter during steady state are illustrated in Figure 2.2.

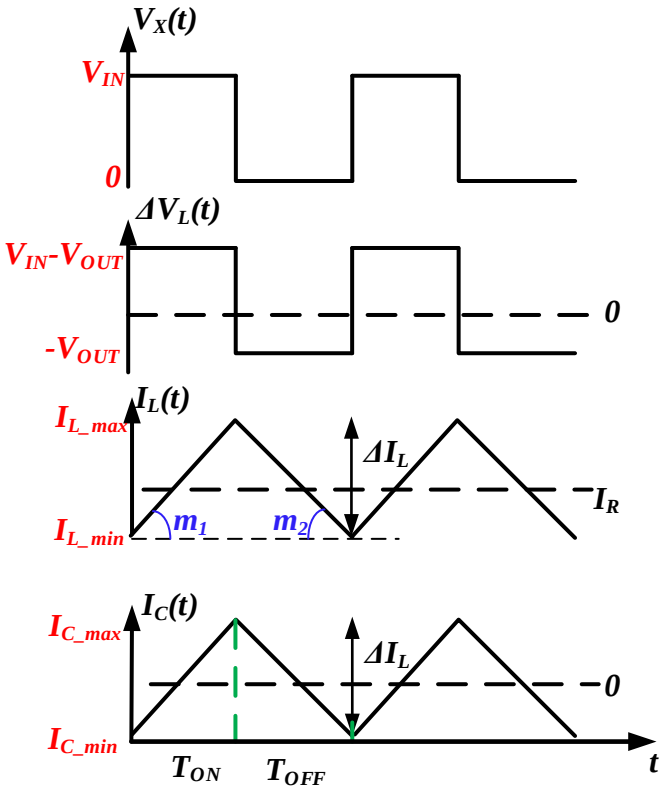

Figure 2.2. Voltage and Current Waveforms in Steady State.

Note that T_{ON}/T_{OFF} represents the turn-on/turn-off duration of S_P. V_X and ΔV_L is the switching node voltage and voltage over the inductor, respectively. I_L and I_C is the

current passing through the inductor and capacitor, respectively. $m_1/(-m_2)$ is the inductor current rising/falling slope.

During T_{ON} period, S_P/S_N is turned on/off, $V_X=V_{IN}$. The voltage across the inductor is $V_{IN}-V_{OUT}>0$, the current ramps up at a rate given by

$$m_1 = \frac{V_{IN} - V_{OUT}}{L} \tag{1}$$

During T_{OFF} period, S_P/S_N is turned off/on, $V_X=0$. The voltage across the inductor is $-V_{OUT}<0$, the current ramps down at a rate which is given by

$$m_2 = \frac{V_{OUT}}{L} \tag{2}$$

At steady state, the average inductor current should be equal to the load current. If $0.5I_L<I_R$, the converter works in Continuous Current Mode (CCM). If $0.5I_L>I_R$, the converter works in Discontinuous Current Mode (DCM).

When the load current change, the output voltage will deviate from the nominal value. The output voltage variation is fed back through the controller stage to regulate the power switch behavior, thus to stabilize the output voltage. The overall transient response is delayed by both controller stage and power stage.

2.2 Voltage-mode Control DC-DC Converter

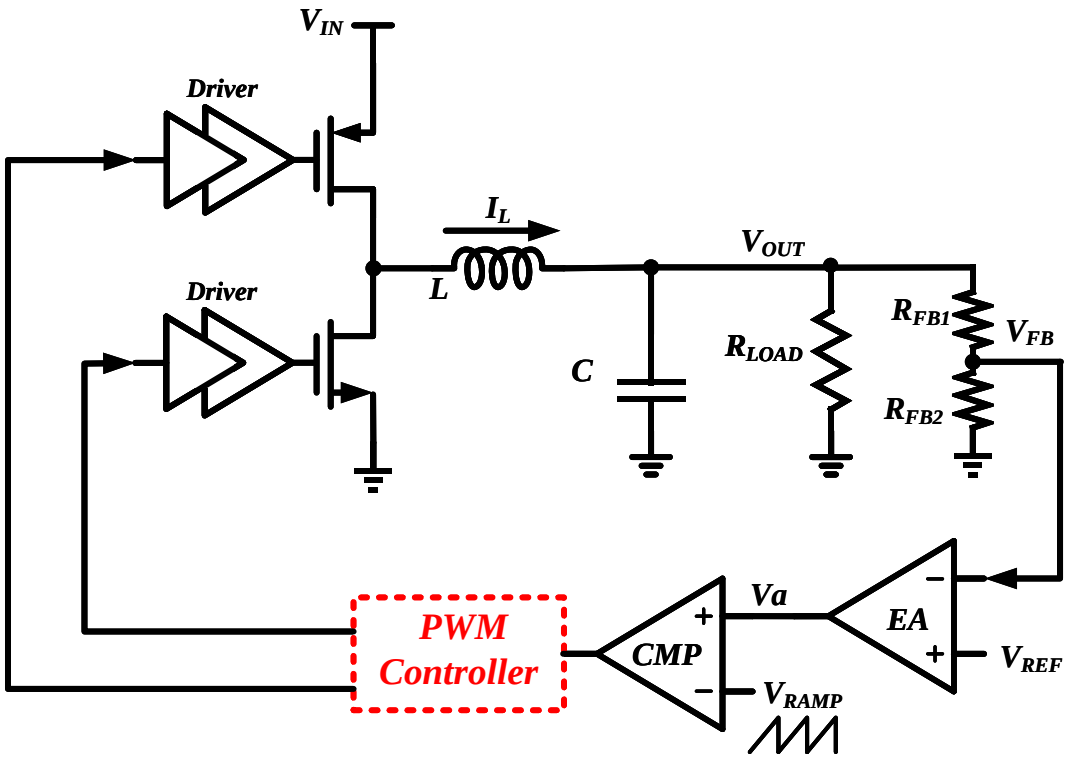

Figure 2.3. The Voltage-Mode Control DC-DC Converter.

Figure 2.3 depicts the generic topology of a voltage-mode PWM DC-DC converter, in which only one single voltage feedback path is employed. This feedback voltage V_{FB} is compared with the reference voltage V_{REF} by an error amplifier, generating the error voltage V_a. Then V_a is compared with a saw-tooth voltage waveform V_{RAMP} to generate the PWM control signal, V_c. As a result, the PWM performance is obtained and the pulse width of the PWM signal is determined to regulate the output voltage [7], [8], [46].

As discussed above, the voltage-mode regulation is achieved solely by voltage feedback path through the error amplifier. This gives a relative simple topology and high noise tolerance. However, a large compensation capacitor is usually required to stabilize the control loop system, which will slow down the load transient response. To improve the load transient response whilst maintaining the system stability, a complicated compensation network (e.g. Type III compensation network) is usually needed [7], [8], [21], [46]–[48].

2.3 Current-mode Control DC-DC Converter

Figure 2.3 shows the topology of the current-mode PWM DC-DC converters.

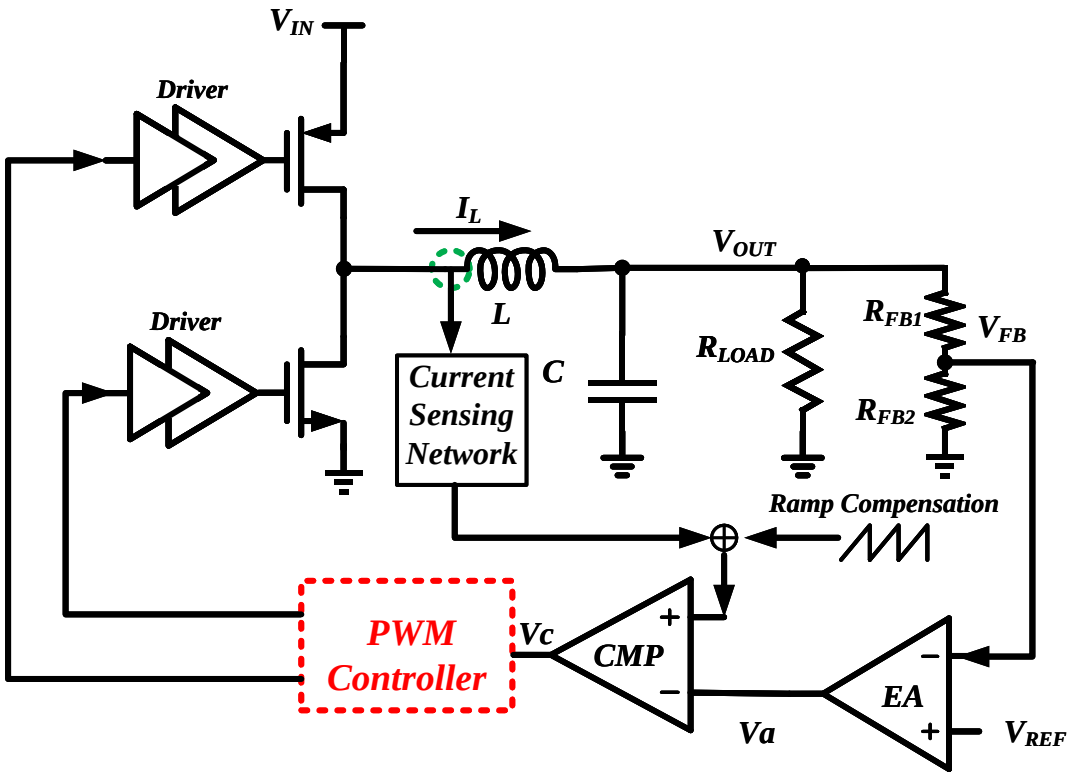

Figure 2.4. The Current-mode Control DC-DC Converter.

As depicted in Figure 2.4, the current-mode control DC-DC converter has two feedback paths: one is the output voltage feedback and the other is the sensed inductor current feedback. To implement the current feedback loop, an accurate current sense network is required. From (1) and (2), it can be seen that the inductor current rising/falling slope is determined by the V_{IN} and V_{OUT}. Thus, the inductor current loop can response faster to the output voltage variation [1], [8], [13], [15], [23], [27], [49]–[51].

However, this inner current feedback loop, which is sensitive to noise, requires more careful stability compensation technique so as to avoid sub-harmonic oscillation when D>0.5, a compensation ramp, V_{RAMP} is also essential [1], [8], [19]. As a result, the overall circuit design becomes more complicated. Furthermore, similar to voltage-mode control, the load transient response is also limited by the compensated OTA bandwidth as well as the charging/discharging the compensation capacitor.

2.4 V^2 Control DC-DC Converter

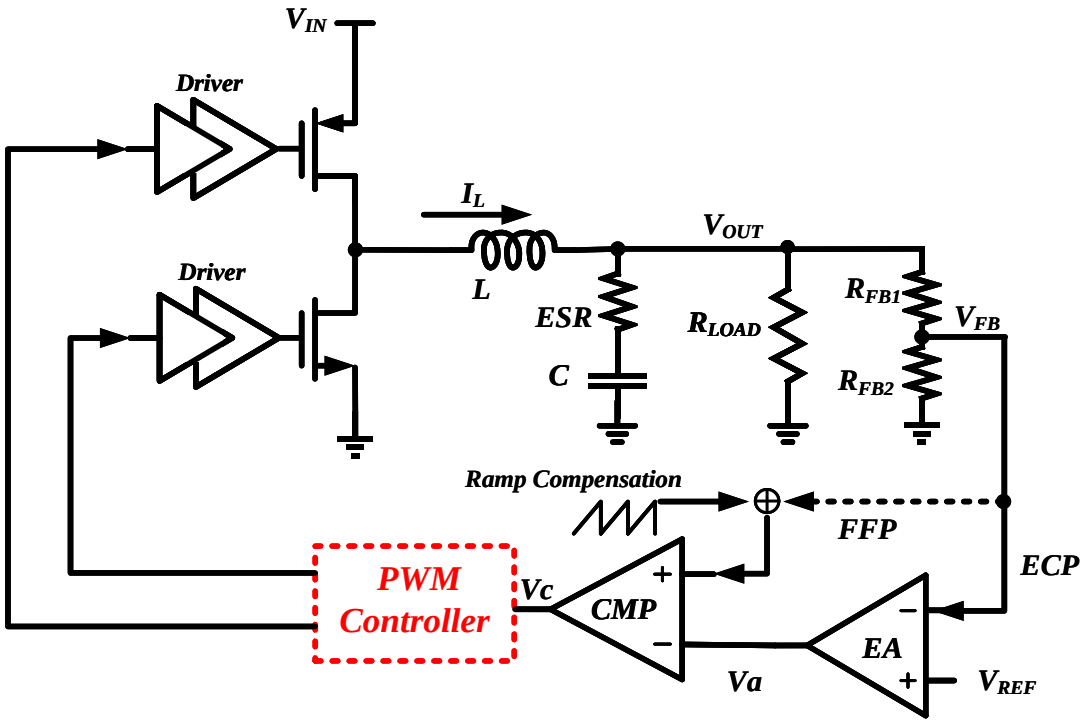

Figure 2.5. The Conventional V^2 Control DC-DC Converter.

Figure 2.5 illustrates the system architecture of the conventional V^2 control DC-DC converter. As referred by its name, the V^2 voltage regulation mechanism has two parallel feedback paths and both are derived from the output voltage. The error correct path (ECP) encompasses the compensated error amplifier to provide high DC accuracy while the feedforward path (FFP) bypasses the error amplifier to provide a fast-transient response. It is noted that the ramp signal is generated by the large equivalent series resistance (ESR) of the output capacitor, containing the DC portion of the output voltage [14], [20], [28], [32], [52]–[55].

When a load current change occurs, a large variation to V_{OUT} will be triggered

instantly. This FFP signal is able to fully turn on/off the power PMOS/NMOS immediately to compensate the current difference during load transient period. The load transient response is limited by the time delay contributed by the comparator and the power switch, which is not limited by the bandwidth of the ECP. Thus, the compensated ECP can have a low bandwidth and simple compensation network, whilst maintaining a higher loop gain to provide high static DC accuracy. Due to the low bandwidth of the error amplifier, the noise immunity can be significantly improved. Hence, by comparing with the conventional voltage-mode and current-mode control, V^2 control can achieve a fast-transient response with a relatively simple system architecture with better noise tolerance [2], [20], [28], [56].

Similar to the current-mode control, a ramp compensation is still required to avoid the subharmonic oscillation when D>0.5. The compensation network is still necessary for the high-gain ECP to ensure the stability [9], [22], [25].

2.5 Voltage-mode Hysteretic DC-DC Converter

Figure 2.6 depicts a basic topology of the voltage-mode hysteretic buck DC-DC converter.

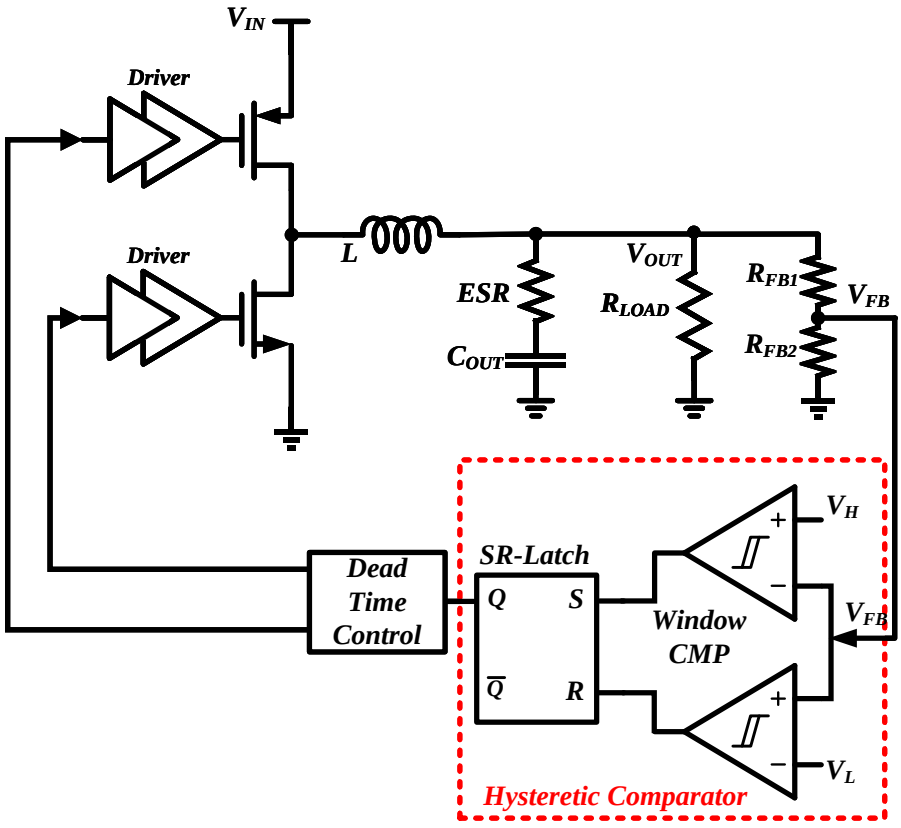

Figure 2.6. Voltage-mode Hysteretic Buck Converter.

As shown in Figure 2.6, there is only one voltage feedback path which is employed in the voltage-mode hysteretic buck converter. Instead of using error amplifier, the output voltage is directly fed back to and regulated by the hysteretic comparator. In particular, the hysteretic control is released from both the complicated stability compensation and sensitive slope compensation network. Thus, the system stability

is guaranteed in the hysteretic control. Since the output voltage is directly controlled by itself, the voltage-mode hysteretic converters can respond instantly to a step-up/step-down load current change [11], [22], [57]–[60].

The voltage regulation mechanism can be explained as follows. Initially, the feedback voltage, V_{FB} is lower than the lower threshold voltage V_L, thus the output of hysteretic comparator is low, turning on/off PMOS/NMOS. As a result, the inductor current i_L starts to increase and its ac component flows into the output capacitor, causing an increase in the output voltage, V_{OUT} as well as the feedback voltage, V_{FB}. When V_{FB} exceeds the upper threshold, V_H, of the comparator, the output of the window comparator will go high, turning off/on PMOS/NMOS. Thus, the V_{OUT} is pulled down until the V_{FB} becomes lower than lower threshold V_L again. Then the PMOS/NMOS will be turned on/off again. Hence, ideally the feedback voltage ripple will be locked by the hysteretic comparator within the hysteretic window, V_H-V_L. However, due to transient delay of the comparator and the controller loop, V_{FB} would be larger than V_H-V_L [28], [32].

Though the hysteretic control has a much faster transient response due to its op-amp free structure, the transient speed is still limited by the power stage elements, especially the inductor selection [41], [61] .This will be further discussed in Chapter 3.

2.6 APCA DC-DC Converters

Although various of topologies and methods have been developed to improve the load current transient response of DC-DC converters, it is still constrained by the physical limit proposed by the output LC filter [4], [37]–[41]. To push the transient response beyond the physical LC limit, various control techniques employing auxiliary current have been developed [37]–[41]. The common topologies of auxiliary pump current methods will be described. The main difference among the auxiliary pump current methods is that of the pump current control scheme.

2.6.1 Dual-Current Pump Module

One common scheme is to turn on and off the pump current by comparing the output voltage with defined the undershoot/overshoot threshold voltage [37]–[39]. The simplified schematic for this control scheme is depicted in Figure 2.7.

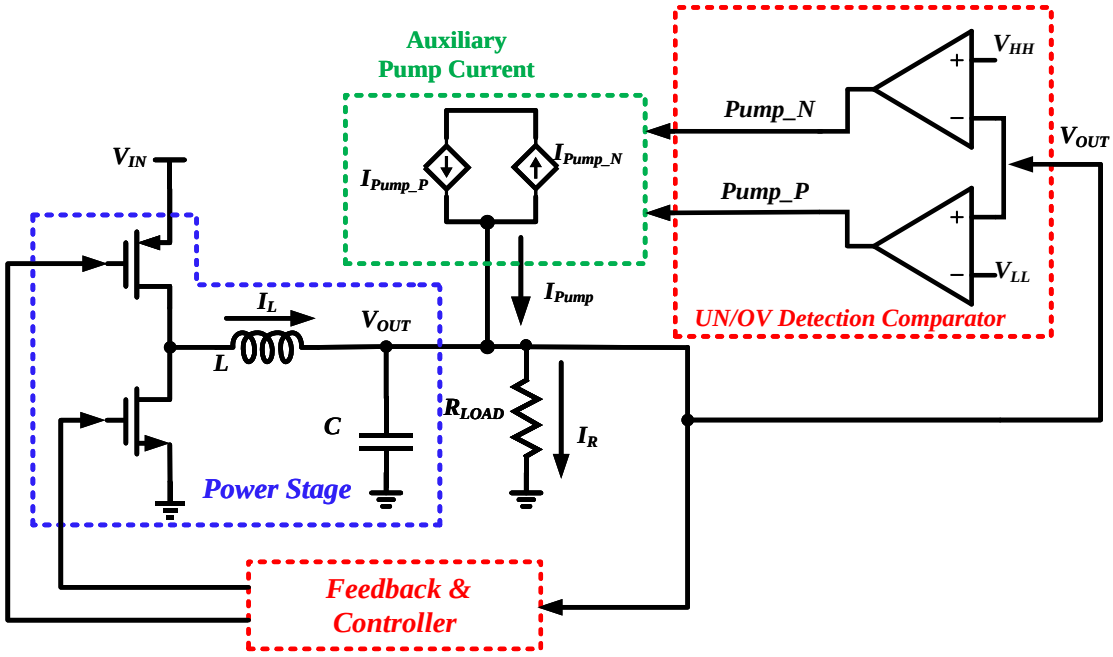

Figure 2.7. DC-DC Converter with Current Pump Technique.

In this control scheme, the auxiliary pump current is simply controlled by comparing V_{OUT} with the defined undershoot/overshoot detection threshold voltage, V_{HH}/V_{LL}.

- When a step-up load current change occurs, an undershoot is induced. If $V_{OUT}<V_{LL}$, the high side auxiliary current is triggered and pumped in; and once $V_{OUT}>V_{LL}$, the pump-in current will be turned off immediately.
- When a step-down load current change occurs, an overshoot is induced. If $V_{OUT}>V_{HH}$, the low side auxiliary current is triggered and pumped out. Once $V_{OUT}<V_{HH}$, the pump-out current will be turned off immediately.

This type of control scheme gives a simple structure and fast response. Unfortunately, the undershoot/overshoot is needed to be recovered once $V_{OUT}>V_{LL}/V_{OUT}<V_{HH}$. This

will cause insufficient auxiliary pump-in/out current duration and it will induce the multiple undershoot/overshoot effect. This will deteriorate the transient improvement [37]–[42], [61].

2.6.2 Digital Slope Control Scheme

Digital slope control schemes are developed to give better turning-off mechanism for the pump-in/pump-out current [40], [41]. The simplified schematic of the converter with digital adaptive slope control (DASP) [41] is shown in Figure 2.8.

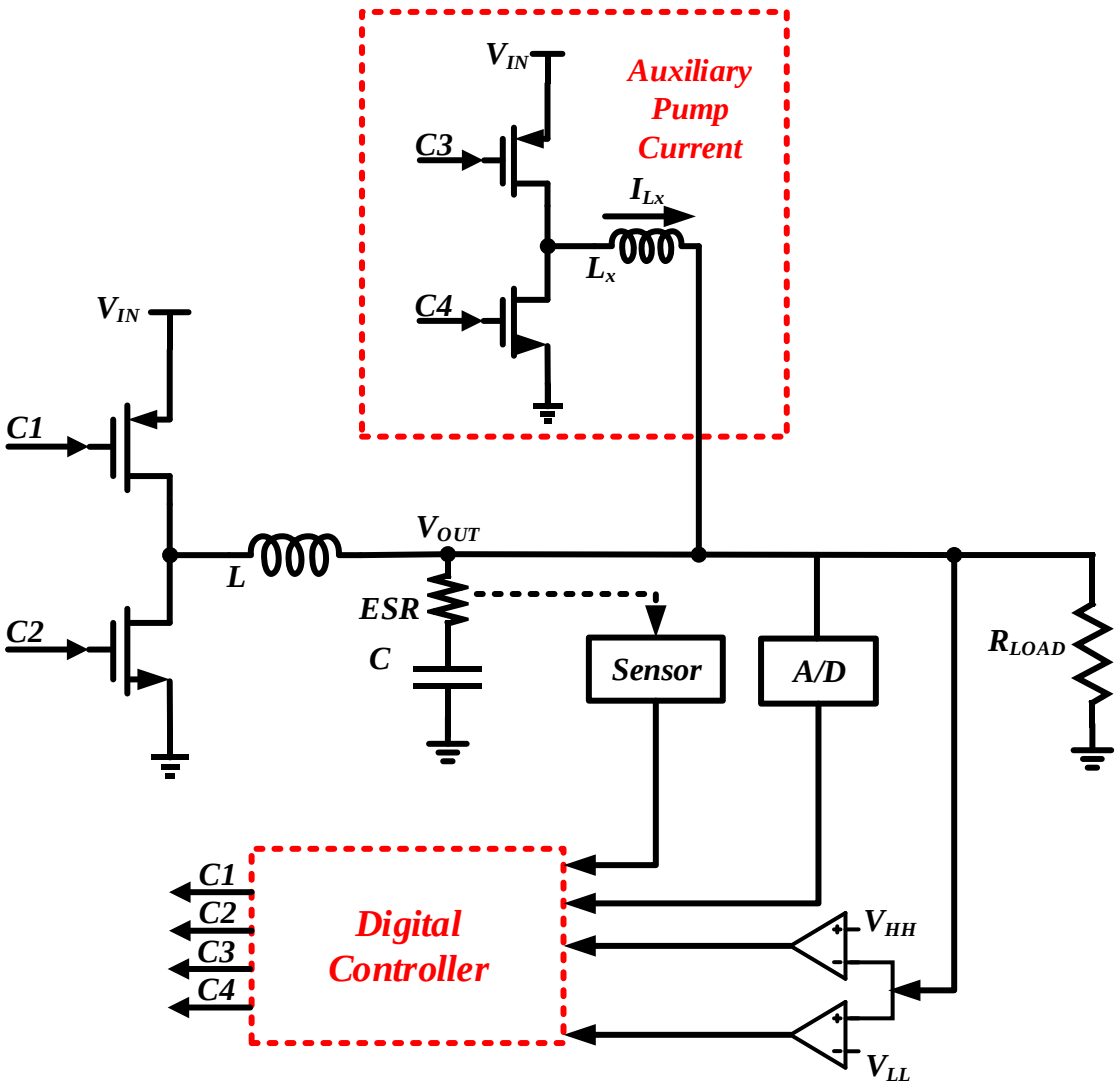

Figure 2.8. The DC-DC converter with DASC.

The control scheme adopts an extra power PMOS/NMOS transistor pair and inductor to release the auxiliary pump-in/pump-out current. The auxiliary current is turned on by comparing V_{OUT} with V_{HH}/V_{LL}, which is the undershoot/overshoot detection voltage. On the other hand, the pump current turning-off signal is generated through the current sensor which monitors the ESR current. When the sum of the inductor current and auxiliary current reaches the load current, the pump-in/pump-out current

is then turned off.

This control scheme achieves better control for the auxiliary current and improve the transient response. However, it requires more complicated circuit implementation and the transient settling time can still be reduced further.

Chapter 3 Transient Response Analyses for DC-DC Converters

Based on the review in Chapter 2, the transient response of a DC-DC converter is limited by the controller stage and the power stage. The voltage-mode hysteretic converter offers a fast-transient response by reducing the controller stage delay. However, its transient speed is still constrained by the power stage LC components. On the other hand, the auxiliary pump current sources can be added to overcome the LC limitation of the DC-DC converters. However, the auxiliary pump current control scheme should be carefully designed to give better transient improvement and system stability. At this juncture, a new topology that combines the voltage-mode hysteretic converter with an improved auxiliary pump current technique is proposed to further enhance the transient response.

Prior to the circuit implementation, the theoretical analysis of the transient response for the representative DC-DC converter is presented. They are based on the conventional voltage-mode hysteretic approach and the APCA approaches, which include the DASC and the proposed PDTD control schemes. In this Chapter, we take the undershoot settling as an example to analyze the transient response. The transient analyses for conventional voltage-mode hysteretic DC-DC converters are conducted first. The transient response limiting factors will be discussed. This is then followed

by the transient response analysis for the APCA converters with DASC and PDTD control scheme, respectively. To validate the effectiveness of the improved control scheme, a comparison between the two control schemes is performed.

3.1 Conventional Voltage-mode Hysteretic Converters

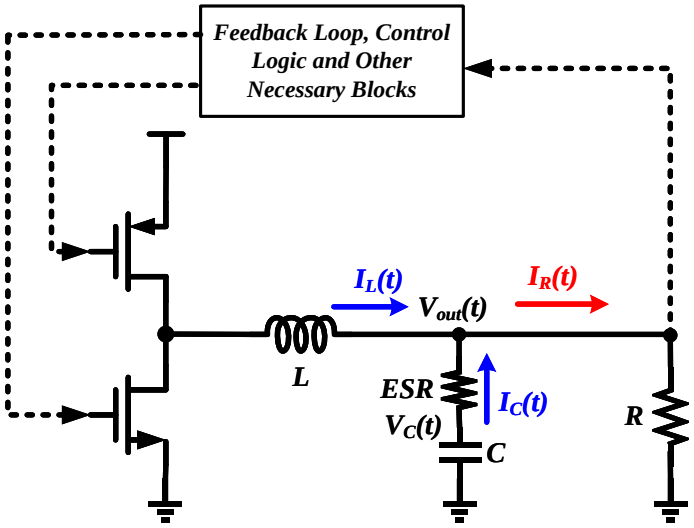

Figure 3.1. Simplified System Model for Conventional Hysteretic DC-DC Converters.

Figure 3.1 depicts the basic system model for the conventional voltage-mode hysteretic DC-DC converters. $I_L(t)$, $I_C(t)$ and $I_R(t)$ represents the inductor current, output capacitor current and load current, respectively. Due to the inductor limitation, the $I_L(t)$ usually ramps with a relatively slower speed than the $I_R(t)$.

In this Chapter, all the transient responses of DC-DC converter are analyzed by applying KCL and KVL at the output node, which are given as

$$I_R(t) = I_L(t) + I_C(t) \tag{3}$$

$$V_{out}(t) = V_C(t) - I_C(t)ESR \tag{4}$$

The transient analysis starts with the simplest case in which the $I_L(t)$ and $I_R(t)$ start to response simultaneously.

3.1.1 No Delay between $I_L(t)$ and $I_R(t)$

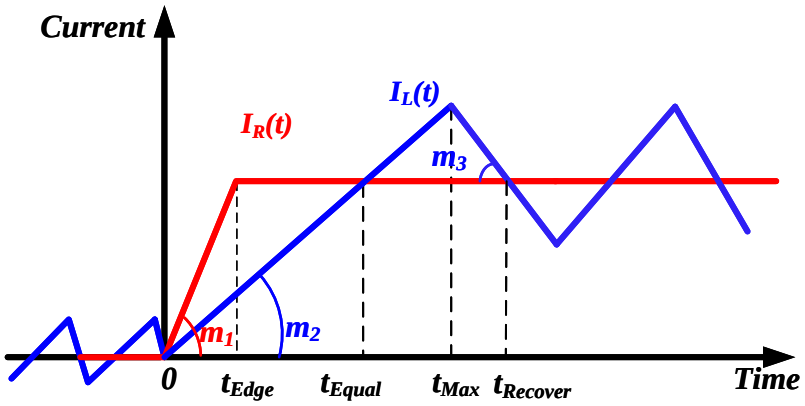

Figure 3.2. Ideal Transient Behaviors of $I_L(t)$ and $I_R(t)$.

There is no response delay between $I_R(t)$ and $I_L(t)$ in Figure 3.2 such that $I_L(t)$ can response to the $I_R(t)$ change instantaneously. To simplify the analyses, it is assumed that the initial current level of $I_R(t)$ is 0 and $I_R(t)$ reaches the new level I_R at t_{Edge}. $I_L(t)$ reaches I_R at t_{Equal} and hits its peak value at t_{Max}. The $I_L(t)$ drops back to the I_R again at $t_{Recover}$. m_1 and m_2 is the ramp-up slope of $I_R(t)$ and $I_L(t)$, respectively. $(-m_3)$ is the falling slope of $I_L(t)$. It is assumed that $I_L(t)$ responses to the $I_R(t)$ change instantaneously, and $m_1 >> m_2$, m_1 and m_2 are given by

$$m_1 = \frac{I_R}{t_{Edge}} \tag{5}$$

$$m_2 = \frac{V_{DD} - V_{OUT}}{L} \tag{6}$$

Thus, we have

$$I_R(t) = \begin{cases} m_1 t & 0 < t < t_{Edge} \\ I_R & t_{Edge} < t < t_{\mathrm{Recover}} \end{cases} \tag{7}$$

$$I_L(t) = \begin{cases} m_2 t & 0 < t < t_{Max} \\ -m_3 t + (m_2 + m_3) t_{Max} & t_{Max} < t < t_{\mathrm{Recover}} \end{cases} \tag{8}$$

$$I_C(t) = -C \frac{dV_C(t)}{dt} \tag{9}$$

$$I_R = \frac{V_{OUT}}{R} \tag{10}$$

where V_{OUT} is the nominal output voltage of the DC-DC converter and I_R is the corresponding load current at V_{OUT}.

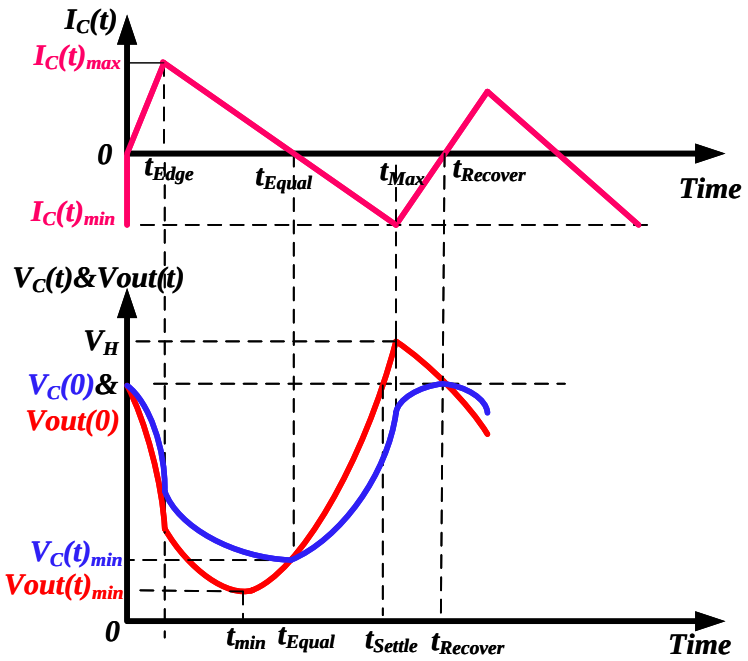

Figure 3.3. Transient Responses of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$.

3.1.1.1 0<t<t_{Edge}

In this region, both $I_R(t)$ and $I_L(t)$ ramps up and the current difference is given as

$$I_C(t) = I_R(t) - I_L(t) = (m_1 - m_2) \times t \tag{11}$$

Combining (9) and (11), we have

$$V_C(t) = -\frac{1}{C}\int I_C(t)dt = -\frac{1}{2C}(m_1 - m_2)t^2 + k_1 \tag{12}$$

$$V_{out}(t) = -\frac{1}{2C}(m_1 - m_2)t^2 - (m_1 - m_2)ESR \cdot t + k_1 \tag{13}$$

where k_1 is a constant. Assume at t=0, $V_C(0) = V_{out}(0) = V_{OUT}$, k_1 can be calculated from the initial value to yield

$$k_1 = V_{OUT} \tag{14}$$

In this region, the $I_R(t)$ rises much faster than the $I_L(t)$, thus $I_C(t)$ is positive and it discharges the output capacitor, thus inducing a voltage drop ΔV_{ESR} over the ESR. As a result, a large undershoot variation ΔV_{UN} is generated where $\Delta V_{UN} = V_{OUT} - V_{out}(t)$. The $I_C(t)$ increases linearly so that the output capacitor is discharged in an increasing speed on $[0, t_{Edge}]$. If the $I_R(t)$ rises rapidly such that $\frac{t_{Edge}}{2C} << ESR$ is fulfilled, the capacitor voltage variation $\Delta V_C(t)$ is much smaller than ΔV_{ESR}. This explains why ΔV_{UN} is dominant by ΔV_{ESR} and $V_{out}(t)$ almost decreases linearly.

$$V_{out}(t) \approx -(m_1 - m_2) ESR \cdot t + k_1 \tag{15}$$

The corresponding transient response of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ over $[0, t_{Edge}]$ is illustrated in Figure 3.3.

3.1.1.2 $t_{Edge} < t < t_{Max}$

In this region, the $I_R(t)$ finishes rising and becomes constant at I_R while the $I_L(t)$ keeps on ramping up. As a result, the corresponding $I_C(t)$ is given as follows:

$$I_C(t) = -m_2 t + I_R \tag{16}$$

$I_C(t)$ is a decreasing function and $I_C(t)=0$ when $I_L(t)= I_R$, thus $t_{Equal}=I_R/m_2$. For $I_C(t)>0$ over $[t_{Edge}, t_{Equal}]$, the output capacitor is discharged. For $I_C(t)<0$ over $[t_{Equal}, t_{Max}]$, the output capacitor is charged up. The corresponding time domain voltage response is given by the following relationships:

$$V_C(t) = \frac{1}{2C} m_2 t^2 - \frac{I_R}{C} t + k_2 \tag{17}$$

$$V_{out}(t) = \frac{1}{2C} m_2 t^2 + (m_2 ESR - \frac{I_R}{C})t - I_R ESR + k_2 \tag{18}$$

k_2 is a constant, which can be calculated through the $V_C(t_{Edge})$ value over both [0, t_{Edge}] and [t_{Edge}, t_{Max}]. $V_C(t_{Edge})$ is obtained from (12) and (17) to yield

$$V_C(t_{Edge}) = -\frac{1}{2C}(m_1 - m_2){t_{Edge}}^2 + k_1 = \frac{1}{2C} m_2 {t_{Edge}}^2 - \frac{I_R}{C} t_{Edge} + k_2 \tag{19}$$

Solving (19), we have

$$k_2 = -\frac{1}{2C} m_1 {t_{Edge}}^2 + \frac{I_R}{C} t_{Edge} + k_1 \tag{20}$$

Combining (5), (14) and (20), it gives

$$k_2 = \frac{{I_R}^2}{2m_1 C} + V_{OUT} \tag{21}$$

Solving $\frac{\delta V_C(t)}{\delta t} = \frac{1}{C} m_2 t - \frac{I_R}{C} = 0$ to give $t = t_{Equal} = \frac{I_R}{m_2}$ at $V_C(t)_{min}$, we have

$$V_C(t)_{\min} = -\frac{{I_R}^2}{2m_2 C} + k_2 \tag{22}$$

Similarly, solving $\frac{\delta V_{out}(t)}{\delta t} = \frac{1}{C} m_2 t + m_2 ESR - \frac{I_R}{C} = 0$ to give $t_{\min} = \frac{I_R}{m_2} - C \cdot ESR$ at $V_{out}(t)_{min}$, we have

$$V_{out}(t)_{\min} = -\left[\frac{m_2 C \cdot ESR^2}{2} + \frac{{I_R}^2}{2m_2 C}\right] + k_2 \tag{23}$$

As such, $V_C(t)$ decreases on [t_{Edge}, t_{Equal}], and it increases on [t_{Equal}, t_{Max}]. $V_{out}(t)$ decreases on [t_{Edge}, t_{min}], and it increases on [t_{min}, t_{Max}]. The undershoot variation ΔV_{UN} is defined as

$$\Delta V_{UN} = V_{OUT} - V_{out}(t)_{\min} = \frac{m_2 C \cdot ESR^2}{2} + \frac{I_R^{\,2}}{2C}\left(\frac{1}{m_2} - \frac{1}{m_1}\right) \tag{24}$$

Assume that the $V_{out}(t)$ settles down when $V_{out}(t) = \kappa V_{OUT}$ where κ is the settling accuracy. Then the corresponding settling time can be solved from (18) by setting $V_{out}(t_{Settle}) = \kappa V_{OUT}$ as

$$t_{Settle} = \sqrt{\frac{2C(\kappa V_{OUT} - k_2)}{m_2} + \left(\frac{I_R}{m_2}\right)^2 + (C \cdot ESR)^2} + \frac{I_R}{m_2} - C \cdot ESR \tag{25}$$

In the following analysis, the settling accuracy κ is set to be 100% for simplicity. This gives

$$t_{Settle} = \sqrt{\frac{2C(V_{OUT} - k_2)}{m_2} + \left(\frac{I_R}{m_2}\right)^2 + (C \cdot ESR)^2} + \frac{I_R}{m_2} - C \cdot ESR \tag{26}$$

For the voltage-mode hysteretic converters, the $V_{out}(t)$ is solely regulated by itself. During the transient period, the $V_{out}(t)$ keeps going up until $V_{out}(t) = V_H$ where $t = t_{Max}$.

$$t_{Max} = \sqrt{\frac{2C(V_H - k_2)}{m_2} + \left(\frac{I_R}{m_2}\right)^2 + (C \cdot ESR)^2} + \frac{I_R}{m_2} - C \cdot ESR \tag{27}$$

Since $V_H > V_{OUT}$, from (26) and (27), it can be seen that $t_{Settle} < t_{Max}$.

From (22)-(26), one can conclude that for a specific output voltage, V_{OUT}, the undershoot variation ΔV_{UN} and the transient settling time t_{Settle} are determined by the output current, I_R, and the inductor current slew rate, m_2. Note that I_R is assumed to be constant over $[t_{Edge}, t_{Max}]$. The corresponding transient response of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ over $[t_{Edge}, t_{Max}]$ is illustrated in Figure 3.3.

From Section 3.1.1.1 and Section 3.1.1.2, it can be deduced that both the ΔV_{UN} and t_{Settle} can be reduced by increasing m_2 or reducing I_R over $[t_{Edge}, t_{Max}]$.

3.1.1.3 t_{Max} <t< $t_{Recover}$

In this region, after $V_{out}(t)$ reaches V_H, the hysteretic comparator turns the power PMOS off and the power NMOS on. Thus, $I_L(t)$ starts to ramp down. At this juncture, the $I_C(t)$ becomes

$$I_C(t) = m_3 t + [I_R - (m_2 + m_3)t_{Max}] \tag{28}$$

For $I_C(t)<0$, it increases over $[t_{Max}, t_{Recover}]$, and the output capacitor is charged up. When $t=t_{Recover}$, it gives $I_C(t_{Recover})=0$. From the geometry relationships given by the $I_L(t)$ from t_{Max} to $t_{Recover}$, it is obtained as

$$\begin{aligned} t_{\text{Recover}} &= t_{Max} + \frac{m_2 t_{Max} - I_R}{m_3} \\ &= t_{Max} + \frac{m_2}{m_3}\left[\sqrt{\frac{2C(V_H - k_2)}{m_2} + (\frac{I_R}{m_2})^2 + (C \cdot ESR)^2} - C \cdot ESR\right] \end{aligned} \tag{29}$$

The voltage relationships are obtained as follows:

$$V_C(t) = -\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t_{Max}]}{C} t + k_3 \tag{30}$$

$$V_{out}(t) = -\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t_{Max}] + m_3 C \cdot ESR}{C} t + [(m_2 + m_3)t_{Max} - I_R]ESR + k_3$$

(31)

k_3 is a constant, which can be calculated through the $V_C(t_{Max})$ value over both $[t_{Edge}, t_{Max}]$ and $[t_{Max}, t_{Recover}]$. $V_C(t_{Max})$ is obtained from (17) and (30) to yield

$$V_C(t_{Max}) = \frac{1}{2C} m_2 {t_{Max}}^2 - \frac{I_R}{C} t_{Max} + k_2 = -\frac{1}{2C} m_3 {t_{Max}}^2 - \frac{[I_R - (m_2 + m_3)t_{Max}]}{C} t_{Max} + k_3 \tag{32}$$

Combining (21) and (32), it gives

$$k_3 = -\frac{1}{2C}(m_2 + m_3){t_{Max}}^2 + \frac{{I_R}^2}{2m_1 C} + V_{OUT} \tag{33}$$

Solving $\frac{\delta V_C(t)}{\delta t} = -\frac{1}{C} m_3 t - \frac{[I_R - (m_2 + m_3)t_{Max}]}{C} = 0$ to give $t=t_{Recover}$ at $V_C(t)_{max}$, and using $I_C(t)=0$ at $t=t_{Recover}$, the $V_C(t)$ can be treated to be recovered at $t=t_{Recover}$. Combining (29), (30) and (33) we have:

$$\begin{aligned} V_C(t)_{\max} &= -\frac{1}{2C} m_3 t_{\mathrm{Recover}}{}^2 - \frac{[I_R - (m_2 + m_3)t_{Max}]}{C} t_{\mathrm{Recover}} + k_3 \\ &= \frac{(m_2{}^2 + m_2 m_3)t_{Max}{}^2 - 2(m_2 + m_3)t_{Max} I_R + I_R{}^2}{2m_3 C} + \frac{I_R{}^2}{2m_1 C} + V_{OUT} \end{aligned} \tag{34}$$

Similarly, solving $\frac{\delta V_{out}(t)}{\delta t} = -\frac{1}{C} m_3 t - \frac{[I_R - (m_2 + m_3)t_{Max}] + m_3 C \cdot ESR}{C} = 0$ to give $t = t_{\mathrm{Recover}} - C \cdot ESR$, we have

$$V_{out}(t)_{\max} = V_{out}(t_{\mathrm{Recover}} - C \cdot ESR) \tag{35}$$

If the ESR is large enough such that $t_{\mathrm{Recover}} - C \cdot ESR < t_{Max}$, $V_{out}(t)_{max}=V_H$. In this case, $V_{out}(t)$ decreases over $[t_{Max}, t_{Recover}]$. Since $I_C(t_{Recover})=0$, we have $V_{out}(t_{Recover})=V_C(t_{Recover})$. The transient responses of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ over $[t_{Max}, t_{Recover}]$ are illustrated in Figure 3.3.

The time domain equations for key parameters are summarized in the Table 1. Combining (22), (23), (26) and (29), the undershoot voltage variations such as $V_C(t)_{min}$ and $V_{out}(t)_{min}$ can be improved, and the transient settling parameters such as t_{Settle} and $t_{Recover}$ can be reduced by increasing m_2 or reducing I_R. Note that in previous analysis, I_R is the output current magnitude over $[t_{Edge}, t_{Max}]$ and $[t_{Max}, t_{Recover}]$.

Table 1. Summary of Time Domain Equations from Sections 3.1.1.1, 3.1.1.2 and 3.1.1.3.

Region	Parameters	Time Domain Equations
$[0, t_{Edge}]$	$I_C(t)$	$(m_1-m_2)t$
	$V_C(t)$	$V_C(t) = -\frac{1}{2C}(m_1 - m_2)t^2 + V_{OUT}$
	$V_{out}(t)$	$V_{out}(t) = -\frac{1}{2C}(m_1 - m_2)t^2 - (m_1 - m_2)ESR \cdot t + k_1$ $\approx -(m_1 - m_2)ESR \cdot t + k_1$
$[t_{Edge}, t_{Max}]$	$I_C(t)$	$I_C(t) = -m_2 t + I_R$
	$V_C(t)$	$V_C(t) = \frac{1}{2C} m_2 t^2 - \frac{I_R}{C} t + k_2$
	$V_C(t)_{min}$	$V_C(t)_{\min} = -\frac{{I_R}^2}{2m_2 C} + k_2$
	$V_{out}(t)$	$V_{out}(t) = \frac{1}{2C} m_2 t^2 + (m_2 ESR - \frac{I_R}{C})t - I_R ESR + k_2$
	$V_{out}(t)_{min}$	$V_{out}(t)_{\min} = -\frac{(m_2 C \cdot ESR)^2 + {I_R}^2}{2m_2 C} + k_2$
	t_{Settle}	$t_{Settle} = \sqrt{\frac{2C(V_{OUT} - k_2)}{m_2} + (\frac{I_R}{m_2})^2 + (C \cdot ESR)^2} + \frac{I_R}{m_2} - C \cdot ESR$
	k_2	$k_2 = \frac{{I_R}^2}{2m_1 C} + V_{OUT}$
$[t_{Max}, t_{Recover}]$	$I_C(t)$	$I_C(t) = m_3 t + [I_R - (m_2 + m_3)t_{Max}]$
	$V_C(t)$	$V_C(t) = -\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t_{Max}]}{C} t + k_3$
	$V_{out}(t)$	$V_{out}(t) = -\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t_{Max}] + m_3 C \cdot ESR}{C} t$ $+[(m_2 + m_3)t_{Max} - I_R]ESR + k_3$
	$t_{Recover}$	$t_{Recover} = t_{Max} + \frac{m_2}{m_3}[\sqrt{\frac{2C(V_H - k_2)}{m_2} + (\frac{I_R}{m_2})^2 + (C \cdot ESR)^2} - C \cdot ESR]$
	k_3	$k_3 = -\frac{1}{2C}(m_2 + m_3){t_{Max}}^2 + \frac{{I_R}^2}{2m_1 C} + V_{OUT}$

3.1.2 With Delay between $I_L(t)$ and $I_R(t)$

Considering the reality where the $I_L(t)$ cannot response instantaneously after the $I_R(t)$ changes, the response delay t_D between the $I_L(t)$ and $I_R(t)$ is added. The modified transient diagram is shown in Figure 3.4. In this case, the transient response is mainly determined by three components: the response delay t_D, the $I_L(t)$ ramp-up rate m_2 and the load current $I_R(t)$.

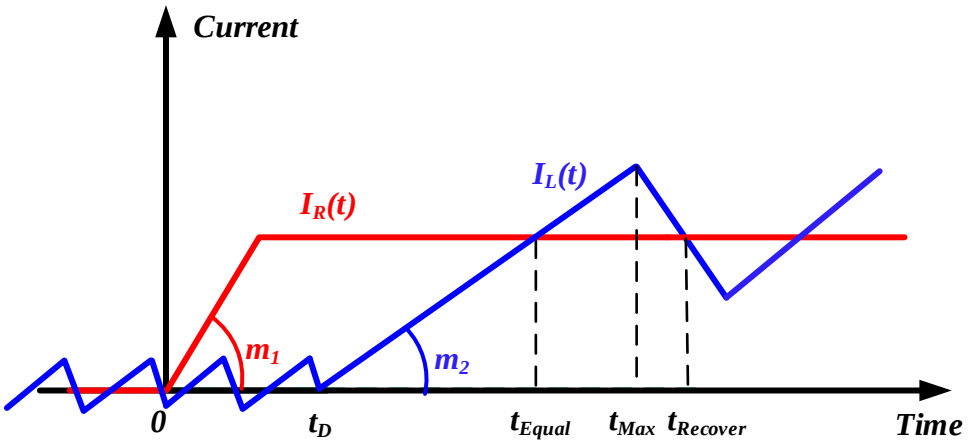

Figure 3.4. Transient Diagram of $I_R(t)$ and $I_L(t)$ with Response Delay.

To improve the transient response of DC-DC converters, one common method is to reduce t_D by speeding up the controller stage response. This technique is widely applied in the fast-transient PWM current/voltage-mode or V^2 control DC-DC converters by extending the limited bandwidth or bypass the compensation op-amp and so on [1],[3],[9],[46],[52]. In hysteretic DC-DC converters, the controller response is quite fast due to the op-amp free structure [11], [12], [20], [22], [29]–[34] and $I_L(t)$ can start to catch up the $I_R(t)$ change in a short time delay less than 100ns. Since the t_D is very small, improving the transient response by reducing t_D may not

be effective. Another method is to increase m_2 through a smaller inductance [4], [7], [8]. However, it will increase the inductor current ripple as well as the output voltage ripple, which is not preferred in most applications.

As discussed in Section 3.1.1, in voltage-mode hysteretic converters, when the load current changes, a large current difference $\Delta I(t)$ is induced between $I_R(t)$ and $I_L(t)$. The $\Delta I(t)$ is only compensated by the $I_C(t)$. The $I_C(t)$ discharges the output capacitor, hence causing the undershoot variation. To improve the transient response, an auxiliary pump current $I_P(t)$ can be added to compensate the $I_R(t)$ change. In this way, the $\Delta I(t)$ being compensated by $I_C(t)$ is reduced. This leads to the improvement of the transient response. The transient response of APCA voltage-mode hysteretic will be analyzed in the following part, which include the DASC and PDTD control schemes.

3.2 APCA Voltage-mode Hysteretic Converters

The simplified system model with auxiliary pump current is depicted in Figure 3.5.

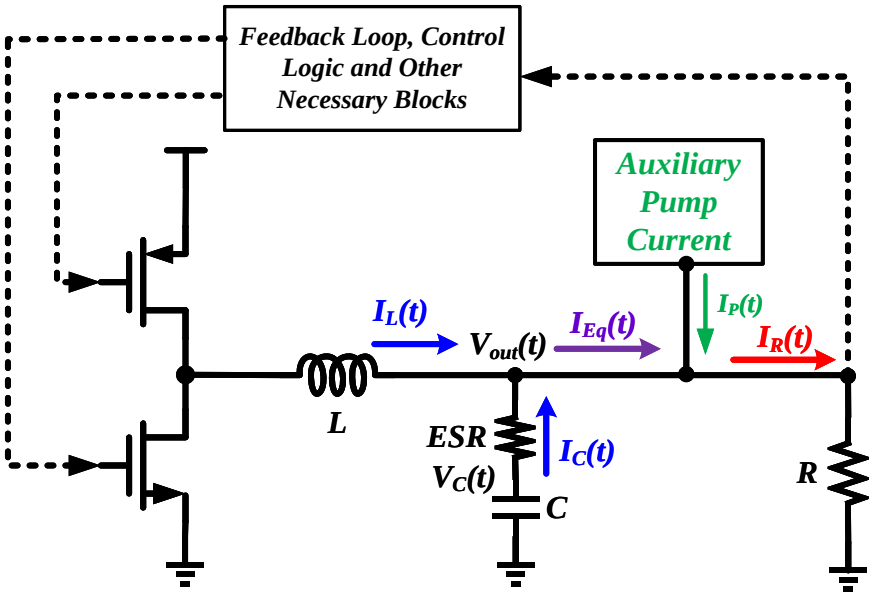

Figure 3.5. System Model for APCA DC-DC Converters.

$I_P(t)$ represents the equivalent pump current adding to the output node. $I_{Eq}(t)$ is the equivalent output current and $I_{Eq}(t)=I_R(t)-I_P(t)$. To simplify the transient analysis, the t_D effect is ignored due to the fast response of the voltage-mode hysteretic converters. This means that $I_L(t)$ and $I_R(t)$ start to rise simultaneously.

Various control schemes of the auxiliary current have been reported [37]–[41], [61]. However, little attention has been paid to the relationship between the transient improvement and the $I_P(t)$ on-time duration. Besides, the analysis for the transient improvement is not in detail. In this work, a comprehensive time-domain analyses for the transient improvement effect will be given. More importantly, the settling

time reduction of the proposed control scheme is compared with the representative conventional scheme.

3.2.1 Digital Adaptive Slope Control

This DASC control scheme is proposed in [41], [61], and the simplified architecture is depicted in Figure 3.6. In this control scheme, an extra pair of power PMOS/NMOS transistor with a smaller inductor L_x ($L_x << L$) are added to provide a rapid-rising current. This can be explained through the timing diagram shown in Figure 3.7.

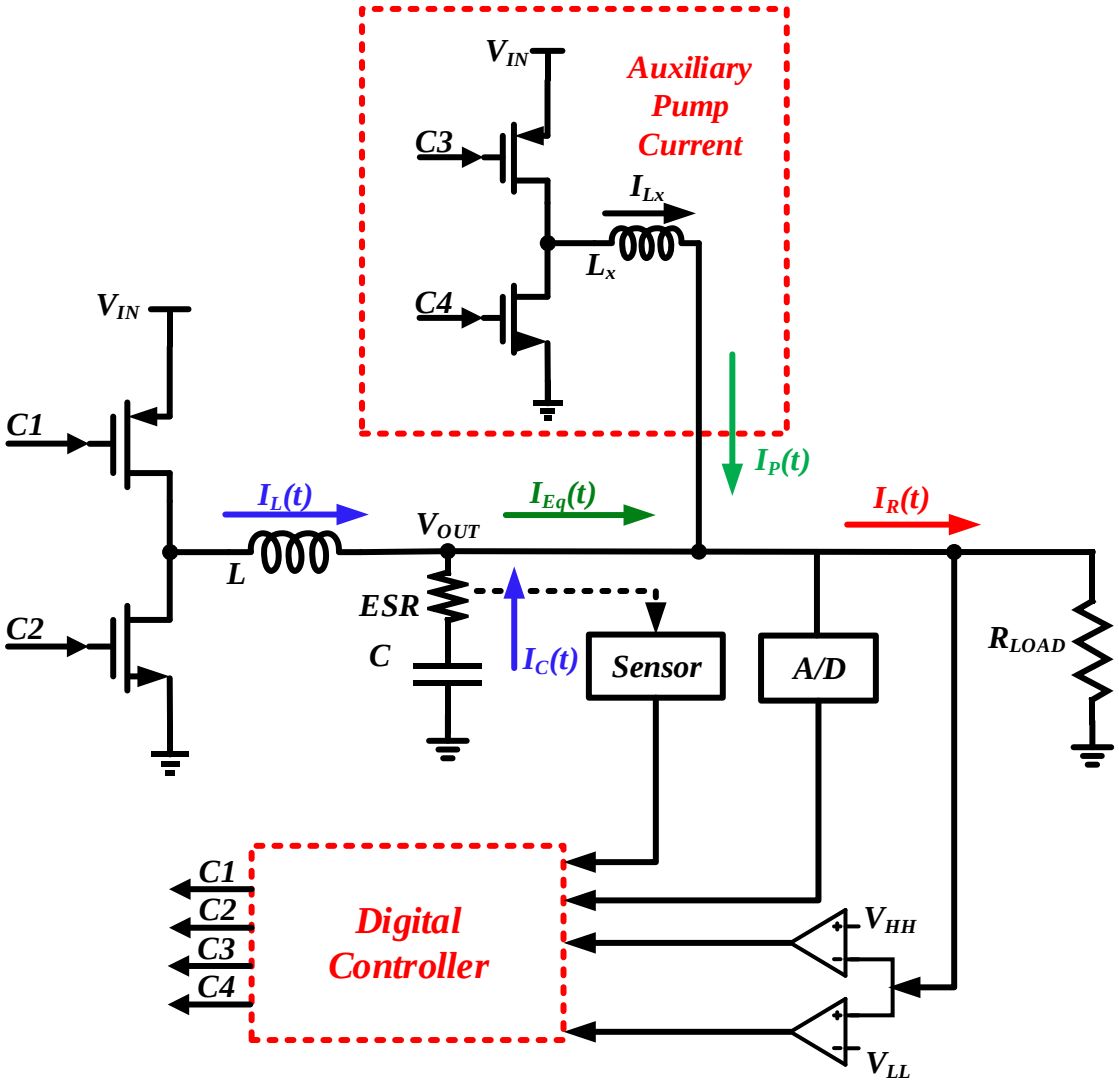

Figure 3.6. The DC-DC converter with DASC.

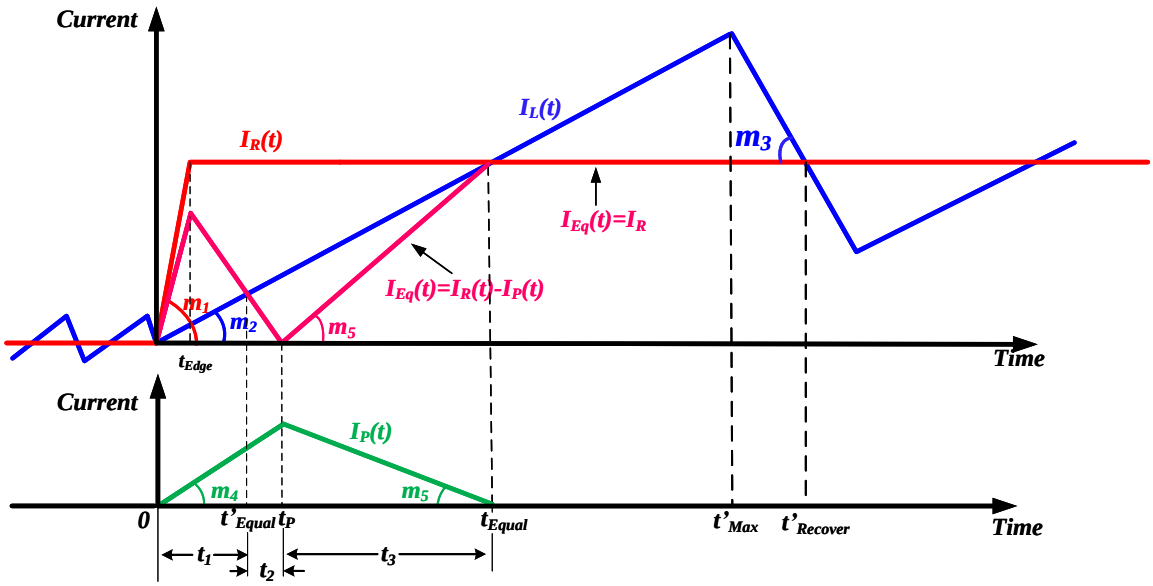

Figure 3.7. Timing Diagram of Digital Adaptive Slope Control.

The pump current $I_P(t)$ passes through the L_x to compensate the $I_R(t)$ change together with $I_L(t)$. The $I_L(t)$ reaches the equivalent output current $I_{Eq}(t)$ at t'_{Equal} (t_1) and the $I_P(t)$ keeps on rising for a duration of t_2. Then it is gradually turned off and falls to 0 at t_{Equal}. This gives

$$t_1 + t_2 + t_3 = t_{Equal} \tag{36}$$

t_{Equal} is the time instant when the $I_L(t)$ reaches $I_R(t)$. The $I_P(t)$ behavior is described as

$$I_P(t) = \begin{cases} m_4 t & 0 < t < t_P \\ -m_5(t - t_P) + I_P & t_P < t < t_{Equal} \end{cases} \tag{37}$$

$I_P(t)$ reaches its peak value I_P at t_P. m_4 is the ramp-up slope and ($-m_5$) is the falling slope. They are given as follows:

$$m_4 = \frac{V_{DD} - V_{OUT}}{L_x} \tag{38}$$

$$m_5 = \frac{V_{OUT}}{L_x} \tag{39}$$

At $t=t_1$, $I_L(t)$ reaches $I_{Eq}(t)$, we have

$$I_L(t_1) = I_{Eq}(t_1) = I_R - I_P(t_1) \tag{40}$$

Solving (40), it gives

$$t_1 = \frac{I_R}{m_2 + m_4} \tag{41}$$

After $I_L(t)$ reaches $I_{Eq}(t)$ at t_1, $I_P(t)$ keeps on rising, and the rise time duration is given by

$$t_2 = \frac{L_x}{L} t_1 = \frac{m_2}{m_4} t_1 \tag{42}$$

Combining (36), (41) and (42), it gives

$$t_3 = (\frac{L}{L_x} - \frac{L_x}{L}) t_1 = (\frac{m_4}{m_2} - \frac{m_2}{m_4}) t_1 \tag{43}$$

From the geometry relationships given by the $I_P(t)$ from 0 to t_{Equal}, it can be obtained that

$$m_5 t_3 = m_4 (t_1 + t_2) \tag{44}$$

$$t_P = t_1 + t_2 = (1 + \frac{m_2}{m_4}) t_1 = \frac{I_R}{m_4} \tag{45}$$

Combining (42), (43) and (44), we have

$$m_5 = \frac{m_2 m_4}{m_4 - m_2} \tag{46}$$

$$I_P = m_4 t_P = I_R \tag{47}$$

The transient response is analyzed in the following 5 regions: [0, t_{Edge}], [t_{Edge}, t_P], [t_P, t_{Equal}], [t_{Equal}, t'_{Max}] and [t'_{Max}, $t'_{Recover}$].

3.2.1.1 $0<t<t_{Edge}$

In this region, the $I_P(t)$ and $I_R(t)$ starts ramping up simultaneously. The transient responses for $I_C(t)$ and $V_C(t)$ can be obtained as follows:

$$I_C(t) = (m_1 - m_2 - m_4) \times t \tag{48}$$

$$V_C(t) = -\frac{1}{2C}(m_1 - m_2 - m_4)t^2 + k_4 \tag{49}$$

where k_4 is a constant. It can be calculated from the initial value of the $V_C(t)$ to yield $k_4 = V_{OUT}$. Note that $k_4 = k_1$. The output voltage can be obtained as

$$V_{out}(t) = -\frac{1}{2C}(m_1 - m_2 - m_4)t^2 - (m_1 - m_2 - m_4)ESR \cdot t + k_4 \tag{50}$$

If $\frac{t_{Edge}}{2C} << ESR$, we have

$$V_{out}(t) \approx -(m_1 - m_2 - m_4)ESR \cdot t + k_4 \tag{51}$$

Comparing (48)-(51) with (11)-(15), the $I_C(t)$ becomes smaller while the $V_C(t)$ and $V_{out}(t)$ become larger. This is because the $I_P(t)$ helps to compensate the $I_R(t)$ change, reducing the discharge current $I_C(t)$. Consequently, the $V_C(t)$ decreases with a smaller rate and the ΔV_{ESR} becomes smaller. Hence, the undershoot variation ΔV_{UN} is reduced.

3.2.1.2 $t_{Edge}<t<t_P$

In this region, the $I_R(t)$ becomes a constant I_R while $I_P(t)$ keeps on increasing. As a result, $I_{Eq}(t) = I_R - m_4 t$ is reducing, and the $I_C(t)$ is reducing. The corresponding transient behavior for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ can be obtained as follows:

$$I_C(t) = -(m_2 + m_4)t + I_R \tag{52}$$

$$V_C(t) = \frac{1}{2C}(m_2 + m_4)t^2 - \frac{I_R}{C}t + k_5 \tag{53}$$

$$V_{out}(t) = \frac{1}{2C}(m_2 + m_4)t^2 + [(m_2 + m_4)ESR - \frac{I_R}{C}]t - I_R ESR + k_5 \tag{54}$$

where k_5 is a constant. Since $k_4 = V_{OUT}$, we have

$$k_5 = \frac{m_1 t_{Edge}^{\ 2}}{2C} + V_{OUT} \tag{55}$$

Note that $k_5 = k_2$. Based on the $V_C(t)$ value over both $[0, t_{Edge}]$ and $[t_{Edge}, t_P]$, $V_C(t_{Edge})$ can be calculated from (49) and (53) to give

$$V_C(t_{Edge}) = -\frac{1}{2C}(m_1 - m_2 - m_4)t_{Edge}^{\ 2} + k_4 = \frac{1}{2C}(m_2 + m_4)t_{Edge}^{\ 2} - \frac{I_R}{C}t_{Edge} + k_5 \tag{56}$$

Solving $\frac{\delta V_C(t)}{\delta t} = \frac{m_2 + m_4}{C}t - \frac{I_R}{C} = 0$ to give $t'_{Equal} = \frac{I_R}{m_2 + m_4}$ at $V_C(t)_{min}$, we have

$$V_C(t)_{\min} = k_5 - \frac{I_R^{\ 2}}{2C(m_2 + m_4)} \tag{57}$$

Similarly, solving $\frac{\delta V_{out}(t)}{\delta t} = \frac{m_2 + m_4}{C}t + (m_2 + m_4)ESR - \frac{I_R}{C} = 0$ to give $t_{\min} = t'_{Equal} - C \cdot ESR$ at $V_{out}(t)_{min}$. Assume $t_{min} > t_{Edge}$, we have,

$$V_{out}(t)_{\min} = -\left[\frac{I_R^{\ 2}}{2C(m_2 + m_4)} + \frac{C(m_2 + m_4)ESR^2}{2}\right] + k_5 \tag{58}$$

t'_{Equal} is the time instant when the $I_L(t)$ reaches $I_{Eq}(t)$. From (52), the $I_C(t)$ drops to 0 at t'_{Equal}. After t'_{Equal}, $I_C(t)$ becomes negative and it reverses to charge up the output capacitor. Thus, $V_C(t)$ decreases on $[t_{Edge}, t'_{Equal}]$, and increases on $[t'_{Equal}, t_P]$. $V_{out}(t)$ decreases on $[t_{Edge}, t_{min}]$, and increases on $[t_{min}, t_P]$.

Comparing (16) and (22) with (53) and (57), the discharging current $I_C(t)$ decreases in a larger slope and becomes smaller in this region. As a result, $V_C(t)_{min}$ becomes larger.

Solving

$$\frac{\delta V_{out}(t)_{\min}}{\delta m_4} = -\frac{[C \cdot ESR(m_2 + m_4)]^2 - I_R{}^2}{C(m_2 + m_4)^2} = 0 \tag{59}$$

it yields

$$m_4 = \frac{I_R}{C \cdot ESR} - m_2 \tag{60}$$

It can be proved that $\frac{\delta V_{out}(t)_{\min}}{\delta m_4} > 0$ over $[0, \ \frac{I_R}{C \cdot ESR} - m_2]$. As a result, $V_{out}(t)_{min}$ increases with respect to m_4 over the region $0<m_4<\frac{I_R}{C \cdot ESR} - m_2$. From the assumption $t_{min}>t_{Edge}>0$, we have $m_4<\frac{I_R}{C \cdot ESR} - m_2$ in (58). It can be found that $m_4=0$ in (23). Comparing with (23) and (58), $V_{out}(t)_{min}$ becomes larger. The undershoot variation ΔV_{UN} is reduced through the auxiliary current $I_P(t)$.

3.2.1.3 $t_P<t<t_{Equal}$

In this region, the $I_P(t)$ is gradually turned off at the slope of m_5 and it is totally off at t_{Equal}. We have,

$$I_{Eq}(t) = m_5 t + I_R - I_P - m_5 t_P \tag{61}$$

$$I_C(t) = (m_5 - m_2)t + I_R - I_P - m_5 t_P \tag{62}$$

$$V_C(t) = \frac{1}{2C}(m_2 - m_5)t^2 - \frac{1}{C}(I_R - I_P - m_5 t_P)t + k_6 \tag{63}$$

$$\begin{aligned} V_{out}(t) = {} & \frac{1}{2C}(m_2 - m_5)t^2 - \frac{1}{C}(I_R - I_P - m_5 t_P)t + (m_2 - m_5)ESR \cdot t \\ & -(I_R - I_P - m_5 t_P)ESR + k_6 \end{aligned} \tag{64}$$

k_6 is a constant, which can be calculated through the $V_C(t)$ value over both [t_{Edge}, t_P] and [t_P, t_{Equal}]. $V_C(t_P)$ can is obtained from (53) and (62) to yield

$$\begin{aligned} V_C(t_P) &= \frac{1}{2C}(m_2 + m_4){t_P}^2 - \frac{I_R}{C}t_P + k_5 \\ &= \frac{1}{2C}(m_2 - m_5){t_P}^2 - \frac{1}{C}(I_R - I_P - m_5 t_P)t_P + k_6 \end{aligned} \tag{65}$$

Solving (65), it gives

$$k_6 = -\frac{m_4 + m_5}{2C}{t_P}^2 + k_5 \tag{66}$$

Since $m_2 < m_5$, solving $\frac{\delta V_C(t)}{\delta t} = \frac{m_2 - m_5}{C}t - \frac{I_R - I_P - m_5 t_P}{C} = 0$, it yields

$$t = \frac{I_R - I_P - m_5 t_P}{m_2 - m_5} \tag{67}$$

Substituting (46) and (47) into (67), we have $t = t_{Equal} = \frac{I_R}{m_2}$ at $V_C(t)_{max}$. $V_C(t)$ increases over [t_P, t_{Equal}]. This is because $I_L(t) > I_{Eq}(t)$ so that $I_C(t) < 0$. The $I_C(t)$ reverses to charge up the output capacitor.

Similarly, solving $\frac{\delta V_{out}(t)}{\delta t} = \frac{m_2 - m_5}{C}t - \frac{I_R - I_P - m_5 t_P}{C} + (m_2 - m_5)ESR = 0$ to give $t_{\max} = t_{Equal} - C \cdot ESR$ at $V_{out}(t)_{max}$, $V_{out}(t)$ increases on [t_P, t_{max}], and decreases on [t_{max}, t_{Equal}]. When $t = t_{Equal}$, $I_C(t) = 0$ and $V_C(t) = V_{out}(t)$, the undershoot settling time can be obtained as

$$t'_{settle} = \sqrt{\frac{2C(V_{OUT} - k_5)}{m_2 - m_5} + (\frac{I_R - I_P - m_5 t_P}{m_2 - m_5})^2 + (C \cdot ESR)^2} + \frac{I_R - I_P - m_5 t_P}{m_2 - m_5} - C \cdot ESR \quad (68)$$

In this region, $I_C(t)$<0 and it charges up the output capacitor. It also induces a positive voltage ΔV_{ESR} over ESR. $I_C(t)$ is minimum at t_P, charging up $V_C(t)$ at the fastest speed and generating the largest ΔV_{ESR}. Since $I_C(t)$ increases, the $V_C(t)$ ramps up in a decreasing slope and ΔV_{ESR} decreases as well. For this reason, the overall $V_{out}(t)$ recovery is slowed down, which is not desired for the fast-transient applications.

3.2.1.4 t_{Equal}<t<t'$_{Max}$

In this region, the $I_P(t)$ is fully turned off, and the $I_L(t)$ keeps on rising. The corresponding transient analysis for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ is the same as that in Section 3.1.1.2 with different initial conditions. The relationships are obtained as follows:

$$I_C(t) = -m_2 t + I_R \quad (69)$$

$$V_C(t) = \frac{1}{2C} m_2 t^2 - \frac{I_R}{C} t + k_7 \quad (70)$$

$$V_{out}(t) = \frac{1}{2C} m_2 t^2 + (m_2 ESR - \frac{I_R}{C}) t - I_R ESR + k_7 \quad (71)$$

k_7 is a constant, which can be calculated through the $V_C(t_{Equal})$ value over both [t_P, t_{Equal}] and [t_{Equal}, t'_{Max}]. $V_C(t_{Equal})$ is obtained from (63) and (70) to yield

$$\begin{aligned} V_C(t_{Equal}) &= \frac{1}{2C}(m_2 - m_5) t_{Equal}^2 - \frac{1}{C}(I_R - I_P - m_5 t_P) t_{Equal} + k_6 \\ &= \frac{1}{2C} m_2 t_{Equal}^2 - \frac{I_R}{C} t_{Equal} + k_7 \end{aligned} \quad (72)$$

Solving (72), we have

$$\begin{aligned} k_7 &= k_6 + \frac{m_4 {I_R}^2}{2m_2(m_4 - m_2)C} \\ &= k_2 + \frac{{I_R}^2}{2m_2 C} \end{aligned} \tag{73}$$

Since $I_R(t)<I_L(t)$, $I_C(t)<0$ over $[t_{Equal}, t'_{Max}]$, the output capacitor is charged up. Thus, $V_C(t)$ increases over $[t_{Equal}, t'_{Max}]$. The $V_{out}(t)$ keeps on going up until $V_{out}(t)=V_H$ when $t=t'_{Max}$, and we have

$$t'_{Max} = \sqrt{\frac{2C(V_H - k_7)}{m_2} + (\frac{I_R}{m_2})^2 + (C \cdot ESR)^2} + \frac{I_R}{m_2} - C \cdot ESR \tag{74}$$

From (73), we have $k_7>k_2$.Comparing (74) with (27), it can be proved that $t'_{Max}<t_{Max}$ .The improvement is only due to the larger initial condition k_7, which is not significant.

3.2.1.5 $t'_{Max}<t<t'_{Recover}$

In this region, the $I_L(t)$ decreases. The corresponding transient analysis for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ is the same as that in Section 3.1.1.3 with different initial conditions. The relationships are obtained as follows:

$$I_C(t) = m_3 t + [I_R - (m_2 + m_3)t_{Max}] \tag{75}$$

$$V_C(t) = -\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t'_{Max}]}{C} t + k_8 \tag{76}$$

$$\begin{aligned} V_{out}(t) = &-\frac{1}{2C} m_3 t^2 - \frac{[I_R - (m_2 + m_3)t'_{Max}] + m_3 C \cdot ESR}{C} t \\ &+[(m_2 + m_3)t'_{Max} - I_R]ESR + k_8 \end{aligned} \tag{77}$$

k_8 is a constant, which can be calculated through the $V_C(t'_{Max})$ value over both $[t_{Equal},$

t'_{Max}] and [t'_{Max}, $t'_{Recover}$]. $V_C(t'_{Max})$ is obtained from (70) and (76) to yield

$$\begin{aligned} V_C(t'_{Max}) &= \frac{1}{2C} m_2 t'^{2}_{Max} - \frac{I_R}{C} t'_{Max} + k_7 \\ &= -\frac{1}{2C} m_3 t'^{2}_{Max} - \frac{[I_R - (m_2 + m_3) t'_{Max}]}{C} t'_{Max} + k_8 \end{aligned} \tag{78}$$

Solving (78), it gives

$$k_8 = -\frac{1}{2C}(m_2 + m_3) t'^{2}_{Max} + k_7 \tag{79}$$

For $I_C(t)<0$, it increases over [t'_{Max}, $t'_{Recover}$]. The output capacitor is charged up. When $t=t'_{Recover}$, $I_C(t'_{Recover})=0$. From the geometry relationships, it is obtained as

$$m_3 = \frac{m_2 t'_{Max} - I_R}{t'_{Recover} - t'_{Max}} \tag{80}$$

$$t'_{Recover} = t'_{Max} + \frac{m_2}{m_3}\left[\sqrt{\frac{2C(V_H - k_7)}{m_2} + \left(\frac{I_R}{m_2}\right)^2 + (C \cdot ESR)^2} - C \cdot ESR\right] \tag{81}$$

Comparing (81) with (29), it can be proved that $t'_{Recover}<t_{Recover}$ and the improvement is only due to the larger initial condition k_7, which is not significant.

Combining Sections 3.2.1.1 to 3.2.1.5, the corresponding timing diagram of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ for the DASC is illustrated in Figure 3.8.

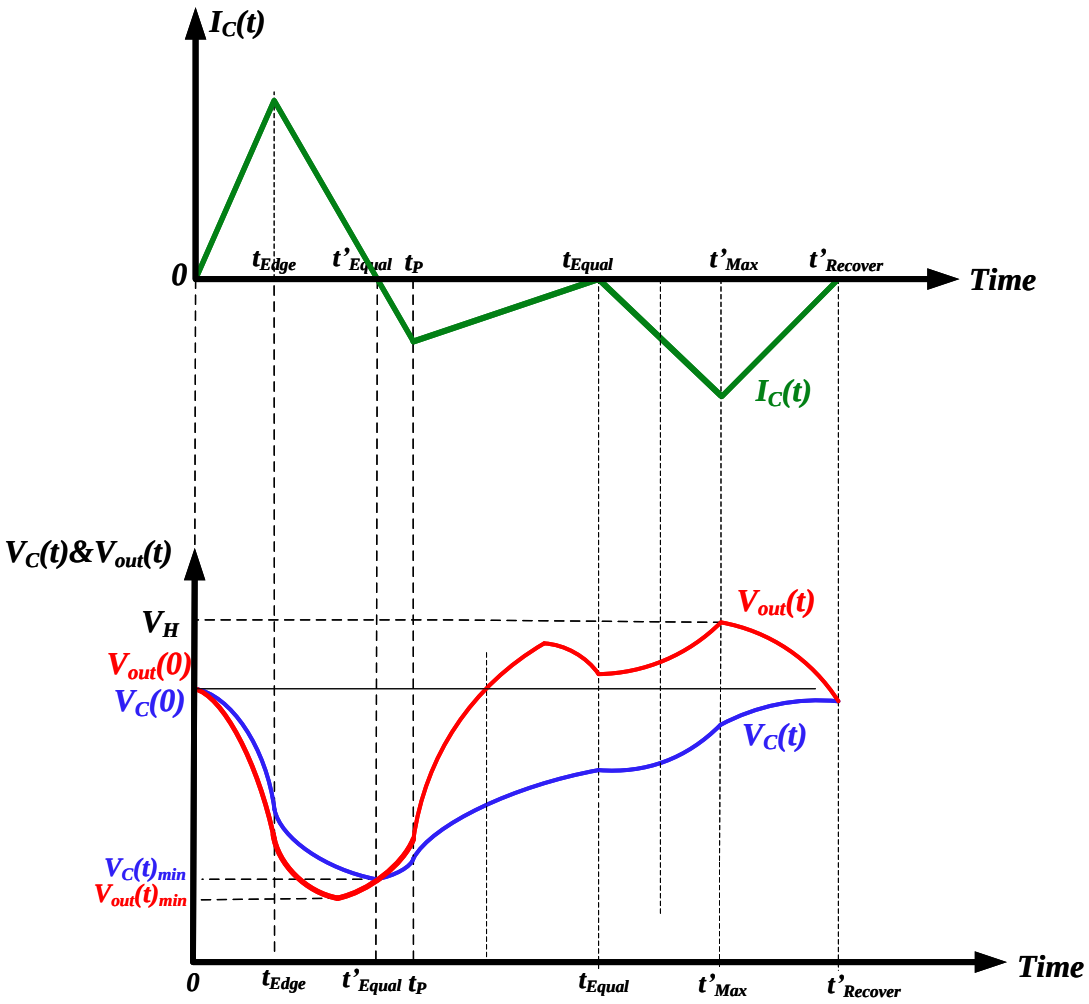

Figure 3.8. Timing diagram of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ for the DASC.

3.2.2 PDTD Control Scheme

The PDTD control scheme for the auxiliary pump current source is proposed in this project, and its simplified system model is depicted in Figure 3.9. In this control scheme, the $I_P(t)$ is designed to remain on until the $V_{out}(t)$ is fully settled down. The $I_C(t)$ is designed to charge up the output capacitor at an increasing slope to ensure the $V_C(t)$ and $V_{out}(t)$ are recovered as soon as possible.

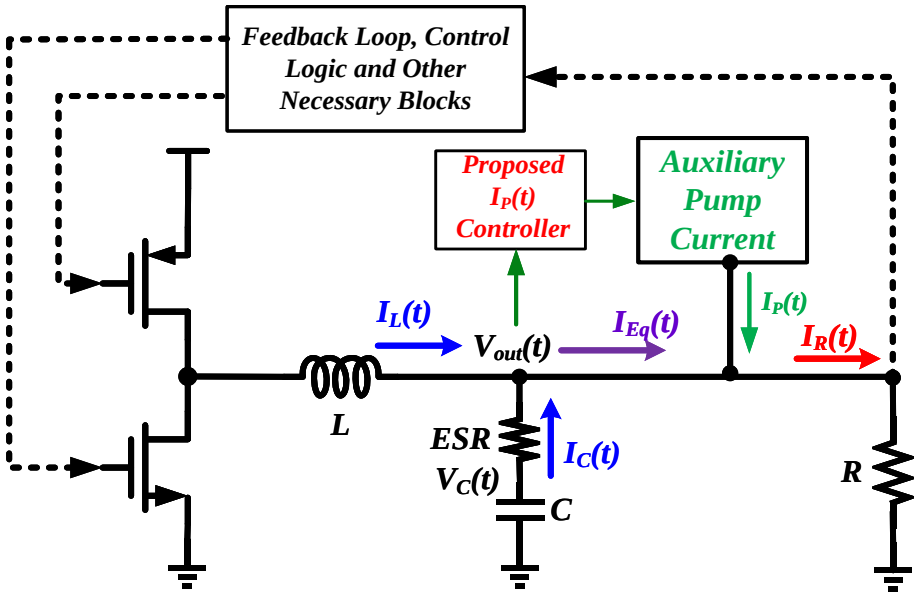

Figure 3.9. Simplified System Model with the PDTD Control Scheme.

The corresponding timing diagram for $I_R(t)$, $I_L(t)$, $I_P(t)$ and $I_{Eq}(t)$ is shown in Figure 3.10. The yellow shadow indicates the current difference of $I_P(t)$ with respect to DASP.

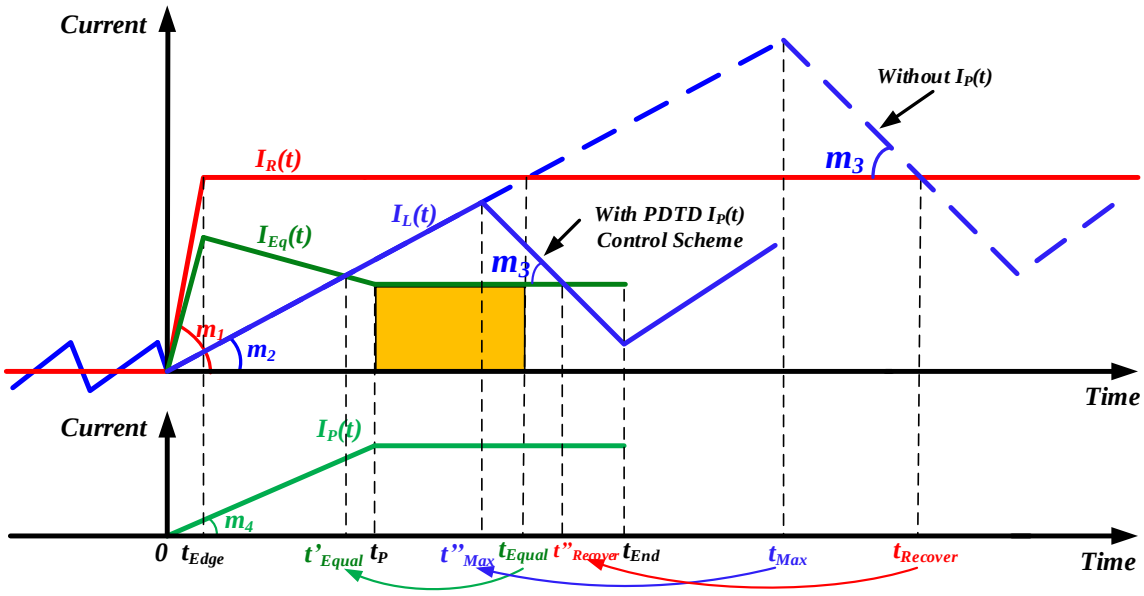

Figure 3.10. Timing Diagram of the PDTD Control Scheme.

Instead of turning off after it reaches the peak value, the $I_P(t)$ is designed to be hold at its peak value, I_P. The $I_P(t)$ behavior is described as

$$I_P(t) = \begin{cases} m_4 t & 0 < t < t_P \\ I_P & t_P < t < t''_{Recover} \end{cases} \quad (82)$$

In the proposed control scheme, the reduction of undershoot variation and the improvement of transient settling time are emphasized.

3.2.2.1 $0<t<t_{Edge}$ & $t_{Edge}<t<t_P$

To ensure the comparison between the PDTD control scheme and conventional DASC control scheme is fair, the transient analyses over $[0, t_{Edge}]$ and $[t_{Edge}, t_P]$ are assumed to be the same with that in the Section 3.2.1.1 and Section 3.2.1.2. This leads to the same undershoot reduction, thus having the same $V_C(t)_{min}$ and $V_{out}(t)_{min}$. The major difference is that of the control scheme over $[t_P, t_{Equal}]$.

3.2.2.2 $t_P<t<t''_{Max}$

In this region, the $I_P(t)=I_P$ and $I_{Eq}(t)= I_R-I_P$. The corresponding transient behaviors for $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ can be obtained as follows:

$$I_C(t) = -m_2 t + (I_R - I_P) \tag{83}$$

$$V_C(t) = \frac{1}{2C} m_2 t^2 - \frac{1}{C}(I_R - I_P)t + k_9 \tag{84}$$

$$V_{out}(t) = \frac{1}{2C} m_2 t^2 - \frac{1}{C}(I_R - I_P)t + m_2 ESR \cdot t - (I_R - I_P)ESR + k_9 \tag{85}$$

k_9 is a constant, which can be calculated through the $V_C(t_P)$ value over both $[t_{Edge}, t_P]$ and $[t_P, t'_{Max}]$. $V_C(t_P)$ is obtained from (53) and (84) to yield

$$\begin{aligned} V_C(t''_{Max}) &= \frac{1}{2C}(m_2 + m_4){t_P}^2 - \frac{I_R}{C} t_P + k_5 \\ &= \frac{1}{2C} m_2 {t_P}^2 - \frac{1}{C}(I_R - I_P)t_P + k_9 \end{aligned} \tag{86}$$

Solving (86), it gives

$$k_9 = -\frac{m_4}{2C}{t_P}^2 + k_5 = -\frac{m_4}{2C}{t_P}^2 + k_2 \tag{87}$$

In this region, $I_C(t)<0$, the output capacitor is charged up. Solving $\frac{\delta V_C(t)}{\delta t} = \frac{1}{C}[m_2 t - (I_R - I_P)] > 0$ and $\frac{\delta V_{out}(t)}{\delta t} = \frac{1}{C}[m_2 t + m_2 ESR - (I_R - I_P)] > 0$,both $V_C(t)$ and $V_{out}(t)$ rise with an increasing slope over $[t_P, t''_{Max}]$. As such, the transient settling time will be significantly reduced. This is given by

$$t''_{Settle} = \sqrt{\frac{2C(V_{OUT} - k_9)}{m_2} + (\frac{I_R - I_P}{m_2})^2 + (C \cdot ESR)^2} + \frac{I_R - I_P}{m_2} - C \cdot ESR \tag{88}$$

When $V_{out}(t)=V_H$, the time becomes

$$t''_{Max} = \sqrt{\frac{2C(V_H - k_9)}{m_2} + (\frac{I_R - I_P}{m_2})^2 + (C \cdot ESR)^2} + \frac{I_R - I_P}{m_2} - C \cdot ESR \quad (89)$$

Comparing (88) with (26), if $I_P < I_R$, we have $\frac{2C(V_{OUT} - k_9)}{m_2} + (\frac{I_R - I_P}{m_2})^2 < \frac{2C(V_{OUT} - k_2)}{m_2} + (\frac{I_R}{m_2})^2$ .Thus, $t''_{Settle} < t_{Settle}$. Comparing (88) with (68), it can be proved that $\frac{V_{OUT} - k_9}{m_2} < \frac{V_{OUT} - k_6}{m_2 - m_5}$ and $\frac{I_R - I_P}{m_2} < \frac{I_R - I_P - m_5 t_P}{m_2 - m_5}$, thus $t''_{Settle} < t'_{Settle}$. Similarly, it can be easily obtained that $t''_{Max} < t_{Max}$ and $t''_{Max} < t'_{Max}$.

3.2.2.3 $t''_{Max} < t < t''_{Recover}$

In this region, the $I_L(t)$ decreases. The corresponding relationships are obtained as follows:

$$I_C(t) = m_3 t + [(I_R - I_P) - (m_2 + m_3)t''_{Max}] \quad (90)$$

$$V_C(t) = -\frac{1}{2C} m_3 t^2 - \frac{[(I_R - I_P) - (m_2 + m_3)t''_{Max}]}{C} t + k_{10} \quad (91)$$

$$\begin{aligned} V_{out}(t) = & -\frac{1}{2C} m_3 t^2 - \frac{[(I_R - I_P) - (m_2 + m_3)t''_{Max}] + m_3 C \cdot ESR}{C} t \\ & + [(m_2 + m_3)t''_{Max} - (I_R - I_P)]ESR + k_{10} \end{aligned} \quad (92)$$

k_{10} is a constant, which can be calculated through the $V_C(t''_{Max})$ value over both $[t_{Edge}, t''_{Max}]$ and $[t''_{Max}, t''_{Recover}]$. $V_C(t''_{Max})$ can be calculated from (70) and (76) to yield

$$\begin{aligned} V_C(t''_{Max}) &= \frac{1}{2C} m_2 t''^2_{Max} - \frac{I_R - I_P}{C} t''_{Max} + k_9 \\ &= -\frac{1}{2C} m_3 t''^2_{Max} - \frac{[(I_R - I_P) - (m_2 + m_3)t''_{Max}]}{C} t''_{Max} + k_{10} \end{aligned} \quad (93)$$

Solving (93), it gives

$$k_{10} = -\frac{1}{2C}(m_2 + m_3)t''^2_{Max} + k_9 \quad (94)$$

For $I_C(t)<0$, it increases over [t''_{Max}, $t''_{Recover}$]. The output capacitor is charged up. When $t=t''_{Recover}$, $I_C(t''_{Recover})=0$. From the geometry relationships given by the $I_L(t)$ from t''_{Max} to $t''_{Recover}$, it is obtained as

$$m_3 = \frac{m_2 t''_{Max} - (I_R - I_P)}{t''_{Recover} - t''_{Max}} \tag{95}$$

$$t''_{Recover} = t''_{Max} + \frac{m_2}{m_3}\left[\sqrt{\frac{2C(V_H - k_9)}{m_2} + \left(\frac{I_R - I_P}{m_2}\right)^2 + (C \cdot ESR)^2} - C \cdot ESR\right] \tag{96}$$

Comparing (96) with (29) and (81), it can be proved that $t''_{Recover}<t_{Recover}$ and $t''_{Recover}<t'_{Recover}$, respectively.

Combining Sections 3.2.2.1 to 3.2.2.3, the corresponding timing diagram of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ for the improved control scheme is demonstrated in Figure 3.11.

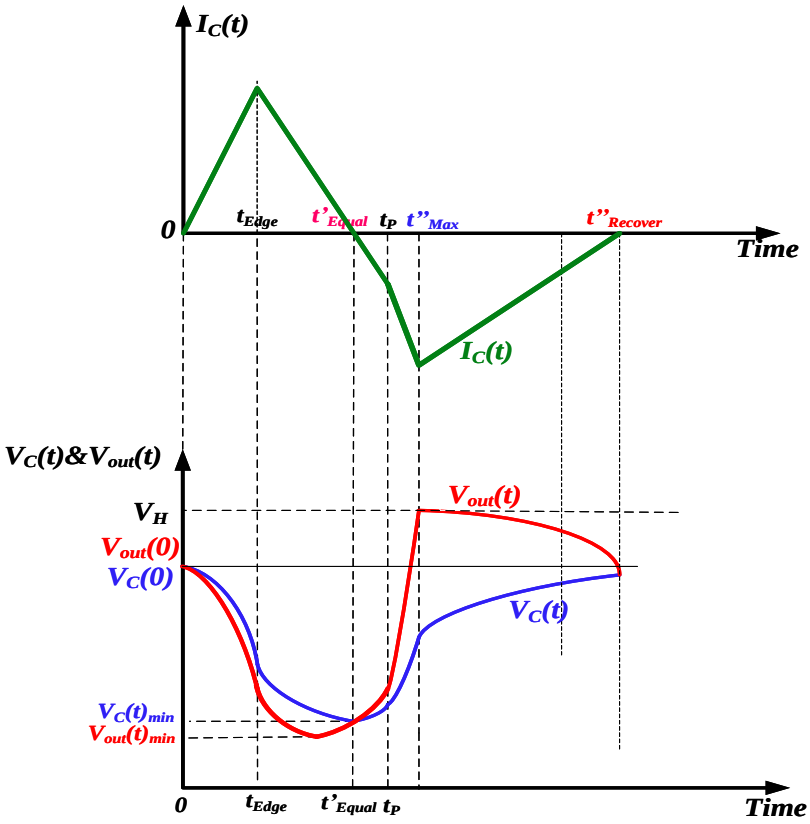

Figure 3.11. Timing Diagram of $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ for the PDTD Control Scheme.

The performance parameters of the transient response for DASC and the PDTD control schemes are listed in Table 2.

Table 2. Performance Parameters of Conventional, DASC and PDTD Control Schemes.

	Conventional	**DASC**	**PDTD**
$I_P(t)$	without $I_P(t)$	$\begin{matrix} m_4 t & 0 < t < t_P \\ -m_5(t-t_P)+I_P & t_P < t < t_{Equal} \end{matrix}$	$\begin{matrix} m_4 t & 0 < t < t_P \\ I_P & t_P < t < t''_{Recover} \end{matrix}$
$V_C(t)_{min}$	$-\frac{I_R^2}{2m_2C}+k_2$	$-\frac{I_R^2}{2C(m_2+m_4)}+k_5$	$-\frac{I_R^2}{2C(m_2+m_4)}+k_5$
$V_{out}(t)_{min}$	$-\left[\frac{m_2C\cdot ESR^2}{2}+\frac{I_R^2}{2m_2C}\right]+k_2$	$-\left[\frac{I_R^2}{2C(m_2+m_4)}+\frac{C(m_2+m_4)ESR^2}{2}\right]+k_5$	$-\left[\frac{I_R^2}{2C(m_2+m_4)}+\frac{C(m_2+m_4)ESR^2}{2}\right]+k_5$
t_{Settle} (t'_{Settle}/ t''_{Settle})	$\sqrt{\frac{2C(V_{OUT}-k_2)}{m_2}+(\frac{I_R}{m_2})^2+(C\cdot ESR)^2}+\frac{I_R}{m_2}-C\cdot ESR$	$\sqrt{\frac{2C(V_{OUT}-k_6)}{m_2-m_5}+(\frac{I_R-I_P-m_5t_P}{m_2-m_5})^2+(C\cdot ESR)^2}+\frac{I_R-I_P-m_5t_P}{m_2-m_5}-C\cdot ESR$	$\sqrt{\frac{2C(V_{OUT}-k_9)}{m_2}+(\frac{I_R-I_P}{m_2})^2+(C\cdot ESR)^2}+\frac{I_R-I_P}{m_2}-C\cdot ESR$
t_{Max} (t'_{Max}/ t''_{Max})	$\sqrt{\frac{2C(V_H-k_2)}{m_2}+(\frac{I_R}{m_2})^2+(C\cdot ESR)^2}+\frac{I_R}{m_2}-C\cdot ESR$	$\sqrt{\frac{2C(V_H-k_7)}{m_2}+(\frac{I_R}{m_2})^2+(C\cdot ESR)^2}+\frac{I_R}{m_2}-C\cdot ESR$	$\sqrt{\frac{2C(V_H-k_9)}{m_2}+(\frac{I_R-I_P}{m_2})^2+(C\cdot ESR)^2}+\frac{I_R-I_P}{m_2}-C\cdot ESR$
$t_{Recover}$ ($t'_{Recover}$/$t''_{Recover}$)	$\frac{m_2}{m_3}\sqrt{\frac{2C(V_H-k_2)}{m_2}+(\frac{I_R}{m_2})^2+(C\cdot ESR)^2}+t_{Max}-\frac{m_2C\cdot ESR}{m_3}$	$\frac{m_2}{m_3}\sqrt{\frac{2C(V_H-k_7)}{m_2}+(\frac{I_R}{m_2})^2+(C\cdot ESR)^2}+t'_{Max}-\frac{m_2C\cdot ESR}{m_3}$	$\frac{m_2}{m_3}\sqrt{\frac{2C(V_H-k_9)}{m_2}+(\frac{I_R-I_P}{m_2})^2+(C\cdot ESR)^2}+t''_{Max}-\frac{m_2C\cdot ESR}{m_3}$

Both the DASC and the PDTD control scheme use the auxiliary current $I_P(t)$ to reduce the discharging current $I_C(t)$, reducing the undershoot variation ΔV_{UN}. When the $V_{out}(t)$ and $V_C(t)$ start to recover, the reversed charging current $I_C(t)$ is increased. As such, the transient settling time is reduced. Comparing with the DASC, as discussed in Section 3.2.2.2 and Section 3.2.2.3, it has shown that $t''_{Settle}<t'_{Settle}$ and $t''_{Recover}<t'_{Recover}$. This has confirmed the PDTD control scheme can offer faster

transient response whilst maintaining similar undershoot reduction. The improvement comparison is illustrated in Figure 3.12.

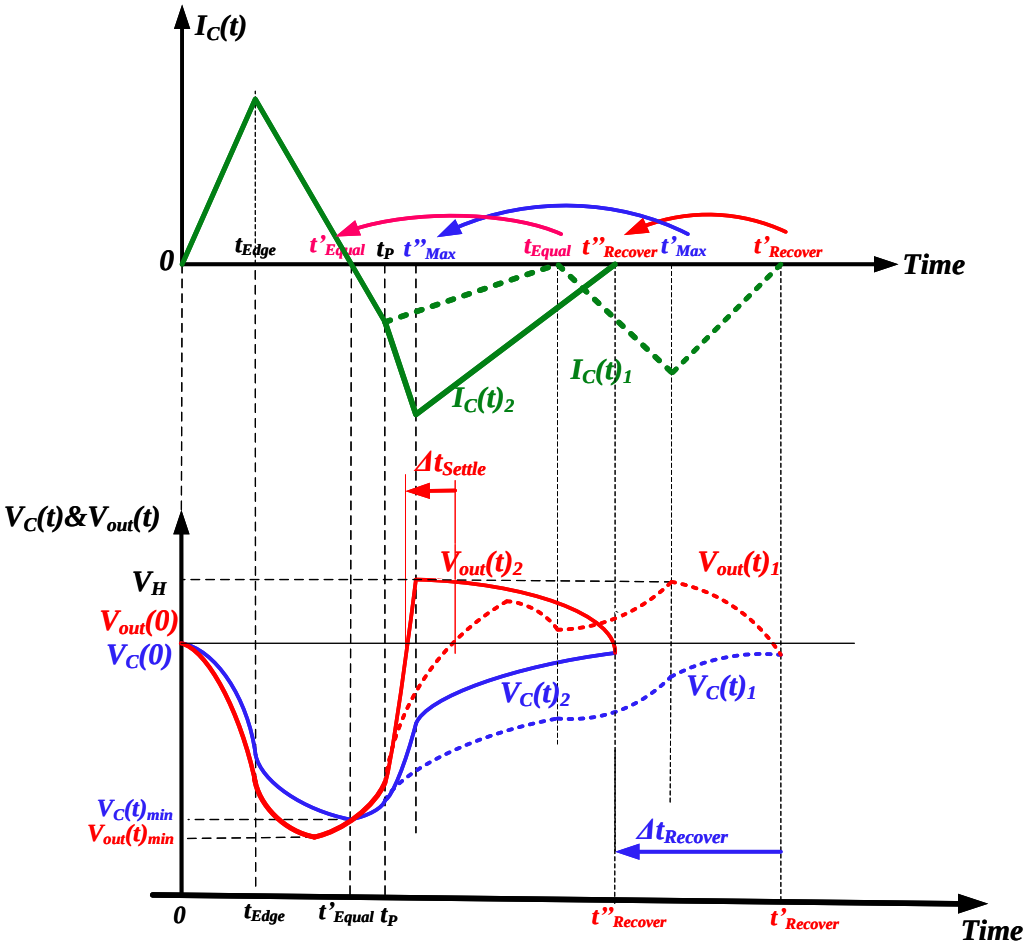

Figure 3.12. The $I_C(t)$, $V_C(t)$ and $V_{out}(t)$ for the DASC and the PDTD Control Scheme.

In Figure 3.12, $I_C(t)_1$, $V_C(t)_1$ and $V_{out}(t)_1$ represent the transient responses for the DASC while $I_C(t)_2$, $V_C(t)_2$ and $V_{out}(t)_2$ are the transient responses for the PDTD control scheme.

Similarly, the transient analyses in this Chapter can be applied to the step-down load

current change, and the conclusion is still valid.

Chapter 4 Circuit Implementations

In this Chapter, the implementation of the voltage-mode hysteretic converter with an improved auxiliary pump current technique is presented. The overall system is firstly described. This is followed by detailed implementation of necessary building blocks. The proposed DC-DC converter is designed and fabricated in TSMC 40nm CMOS process.

4.1 Overall System

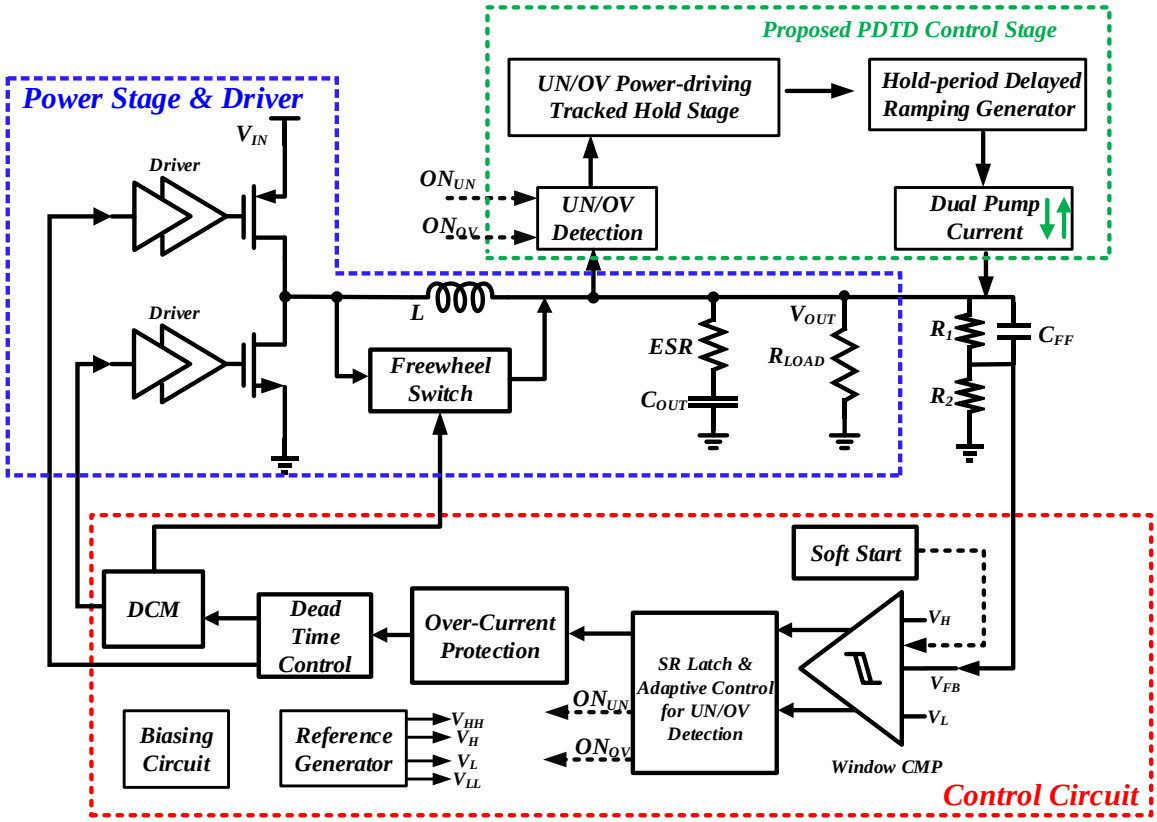

Figure 4.1. Overall System of Proposed Hysteretic DC-DC Buck Converter.

Figure 4.1 illustrates the whole system architecture of the voltage-mode hysteretic buck converter with the proposed PDTD control scheme of the pump current. The overall system consists of three schemes: (I) power stage and driver; (II) system control circuit; (III) proposed PDTD control stage. Of particular note, this project mainly focuses on improving the load current transient response whilst reducing multiple undershoot/overshoot effect and maintaining high efficiency during the steady state. In voltage-mode hysteretic converters, the output capacitor is required to have a large ESR to provide sufficient output voltage ripple $\Delta V_{out}(t)$. As suggested in [32], [62], the required minimum ESR value can be estimated by

$$ESR > \sqrt{\frac{L(V_H - V_L)}{C}\left(\frac{1}{V_{IN} - V_{OUT}} + \frac{1}{V_{OUT}}\right)} \tag{97}$$

With a sufficient ESR, $V_{out}(t)$ is dominant by the $V_{ESR}(t)$ and it is in phase with the $I_L(t)$. The $V_{out}(t)$ is fed to the hysteretic comparator, generating the voltage signal V_{WIN} as well as the adaptive control of undershoot/overshoot detection circuit ON_{UN} and ON_{OV}. V_{WIN} is used to regulate the $I_L(t)$ through the control of power transistors. Pulse-frequency modulation (PFM) control is added to improve the light load efficiency. Dual pump current sources are employed to compensate the large current difference between $I_R(t)$ and $I_L(t)$. They are triggered on by the undershoot/overshoot detection signal. The $I_P(t)$ turning on duration is modulated by the power-driving tracked hold stage whereas the turning-off mechanism is controlled by the hold-period delayed ramping generator. The detailed circuit implementation of the fast-transient DC-DC buck converter will be given in the following sub-sections.

4.2 Driver Stage

To drive the huge-sized power MOS transistor, a driver stage is required. The driver stage is employed by the inverter chain with an increasing transistor aspect ratio [63], [64]which are shown in Figure 4.2. The corresponding aspect ratio of the 4 inverters are designed as: 2,10,50,500.

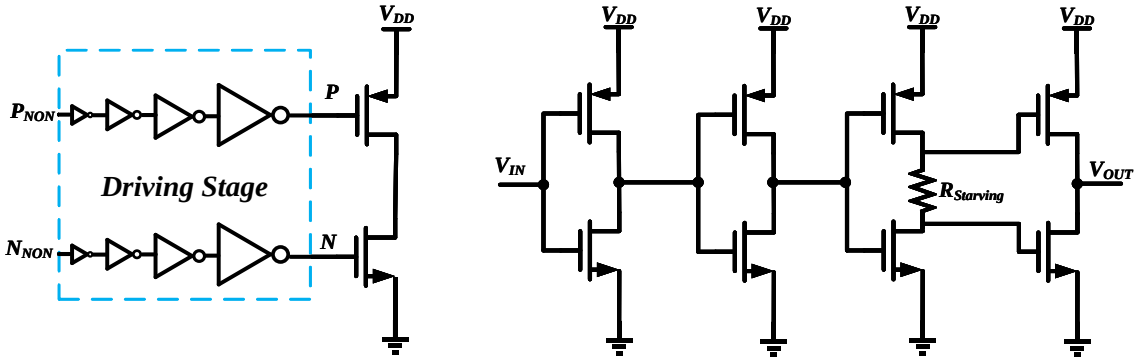

Figure 4.2. Inverter Chain Driver Stage.

In order to limit the short-through current in the last inverter stage, a starving resistor, $R_{starving}$, is inserted in the second last stage [63] to generate a time delay between the V_P and V_N. When V_{IN}rises from *0* to V_{DD}, V_N drops immediately, but V_P drops with a delay. Similarly, when V_{IN} drops from V_{DD} to *0*, V_P rises immediately while V_N rises with a delay. Thus, the short-through current will be reduced significantly due to non-overlapping of V_P and V_N. The corresponding signal of V_{IN}, V_P and V_N are shown in Figure 4.3.

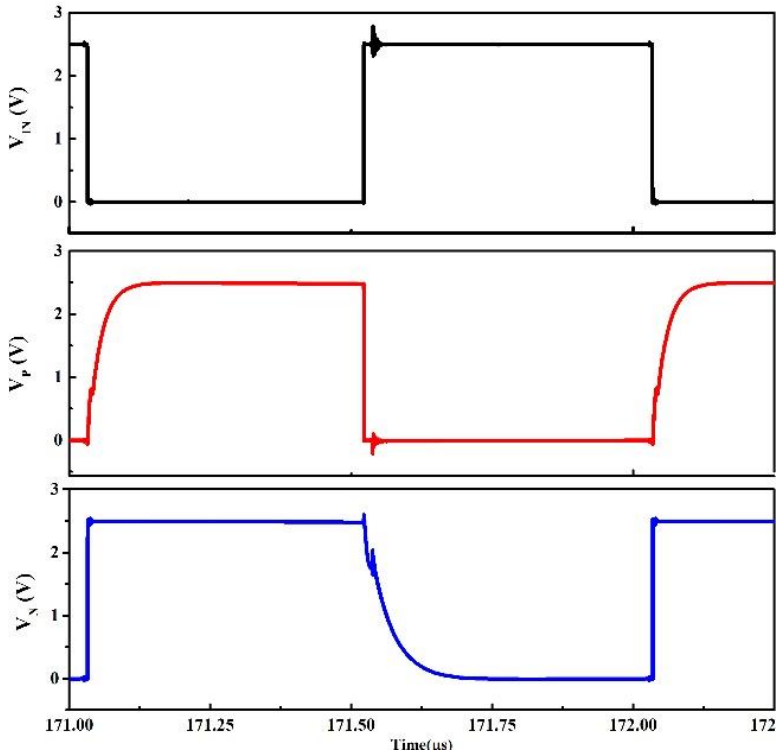

Figure 4.3. Driving Signals in the Last Driver Stage.

4.3 Hysteretic Comparator Stage

In this project, the hysteretic comparator is implemented by a pair of window comparator due to its simple structure and fast transient speed. Corresponding logic modulation is needed to realize the hysteretic control. The overall hysteresis comparator stage, which consists of a pair of window comparator and necessary logic gates, is shown in Figure 4.4.

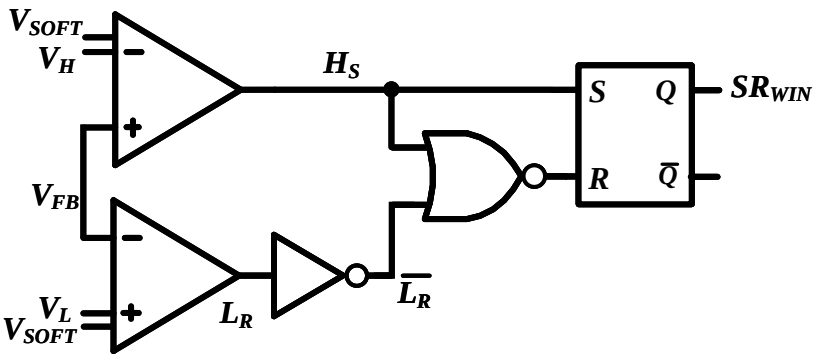

Figure 4.4. Hysteretic Comparator Stage.

V_{FB} and V_{SOFT} is the feedback voltage and the soft start reference, respectively. V_H/V_L is the high/low side boundary of the window comparator stage. SR_{WIN} is the output waveform to regulate the power PMOS and NMOS transistor. The required waveform of SR_{WIN} is illustrated in Figure 4.5.

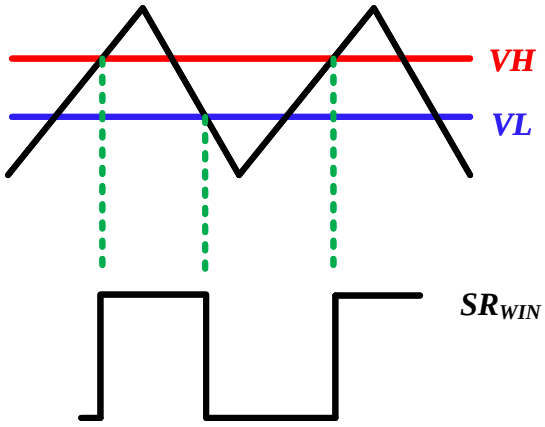

Figure 4.5. Output waveform of Comparator Stage.

The schematic of high-side and low-side window comparator is depicted in Figure 4.6 and Figure 4.7, respectively.

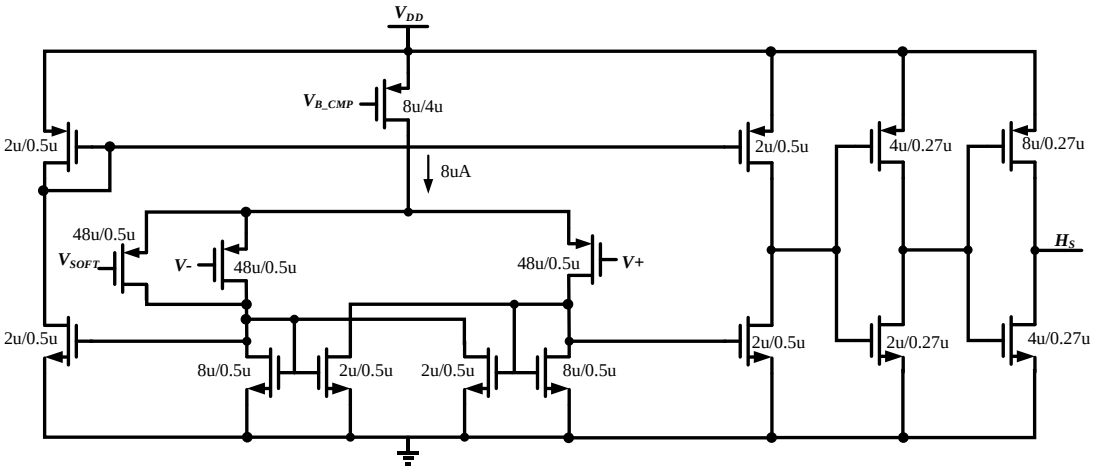

Figure 4.6. Simplified Schematic of the High-side Comparator.

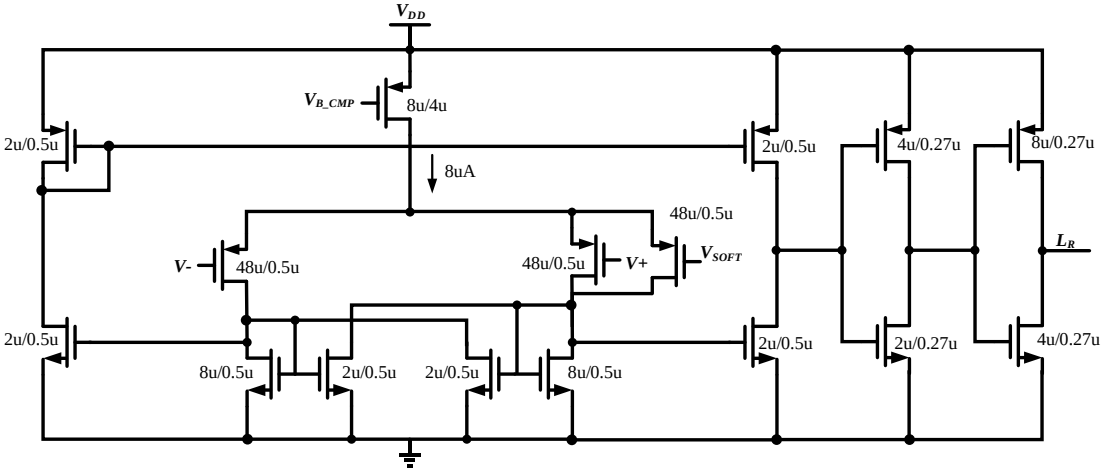

Figure 4.7. Simplified Schematic of the Low-side Comparator.

In ideal case, H_S and L_R cannot be high at the same time. However, due to the switching noise and time delay, both H_S and L_R may be high, which is forbidden for the SR latch input. This will cause the corruption of the switching regulation. To avoid both input of SR latch to be high at the same time, the inverter and NOR gate are added [1] to make sure that S=1 is dominant over R=1.

4.4 Dead Time Control Logic

Internal dead time is generated to avoid the short-through current from the input power supply to the ground, thus reducing the power losses in the converter and protecting the overall system [65]–[67]. It ensures that the power PMOS and NMOS transistor cannot be turned on at the same time. The schematic of dead time control circuit is shown in Figure 4.8.

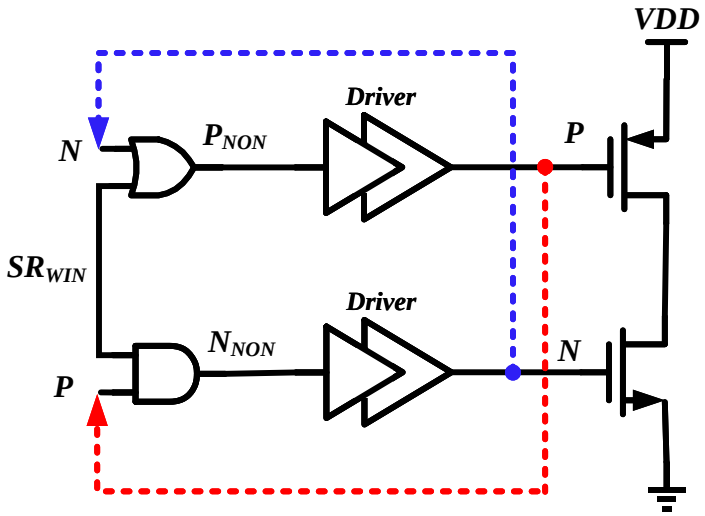

Figure 4.8. Dead Time Controller Circuit.

Note that *P/N* is the gate driving signal of power *PMOS/NMOS* transistor, SR_{WIN} is the control signal after the window comparator stage and P_{NON}/N_{NON} is the signal fed to the power transistor driver stage. When power PMOS transistor is on, that is $P=0$, the NMOS driving signal N_{NON} will be set to 0, thus the NMOS is kept off. On the other hand, when $N=0$, the PMOS driving signal P_{NON} is set to be 1, turning off the PMOS. Hence, the power PMOS/NMOS will be kept off until NMOS/PMOS is turned off. The asymmetrical transient delay for low-to-high/high-to-low signal is

generated to ensure that driving signals remain non-overlapping.

The transient behavior of low-to-high/high-to-low signal in the dead time control stage is shown in Figure 4.9 (a) and (b), respectively. Note that t_P and t_N represents the transient delay in the PMOS/NMOS driver stage, respectively. When $V_{OUT} > V_{REF}$, it requires the PMOS/NMOS to turn off/on to pull down the output voltage, and SR_{WIN} rises from *0* to V_{DD}. This rising signal will directly pass the PMOS side driver stage to pull up the PMOS gate, whilst it is latched before the NMOS side driver stage until the PMOS gate is fully pulled up to V_{DD}. Hence, the PMOS will be fully turned off before NMOS is turned on. Vice versa, the NMOS can be turned on only after the PMOS is fully turned off. The dead time for the low-to-high/high-to-low signal is t_N and t_P, respectively.

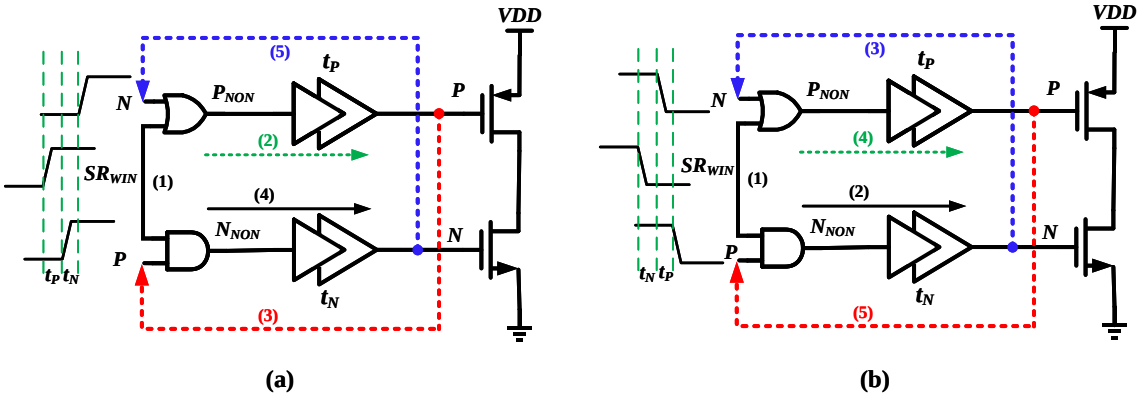

Figure 4.9. Dead Time Generation for (a) Low-to-High Logic; (b) High-to-Low Logic.

The corresponding power PMOS and NMOS driving signal is illustrated in Figure

4.10. The non-overlapping time between P and N is generated as expected.

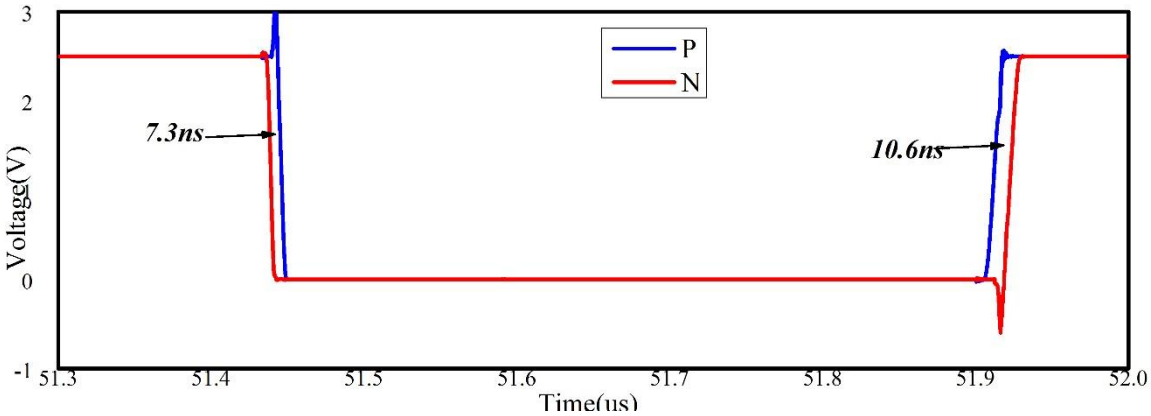

Figure 4.10. Driving voltage of PMOS and NMOS.

4.5 Undershoot/Overshoot Detection

In this section, the undershoot/overshoot variation is detected, and the corresponding output signal will be used to trigger the designed transient enhancement circuit, thus to improve the load current transient response. The undershoot and overshoot detection comparator is depicted in Figure 4.11and Figure 4.12, respectively.

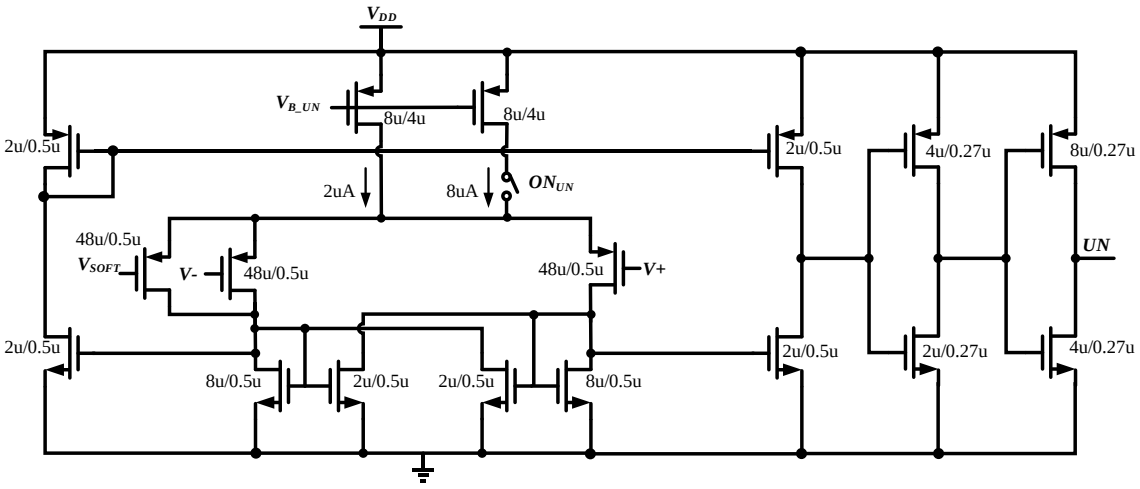

Figure 4.11. Undershoot Detection Comparator.

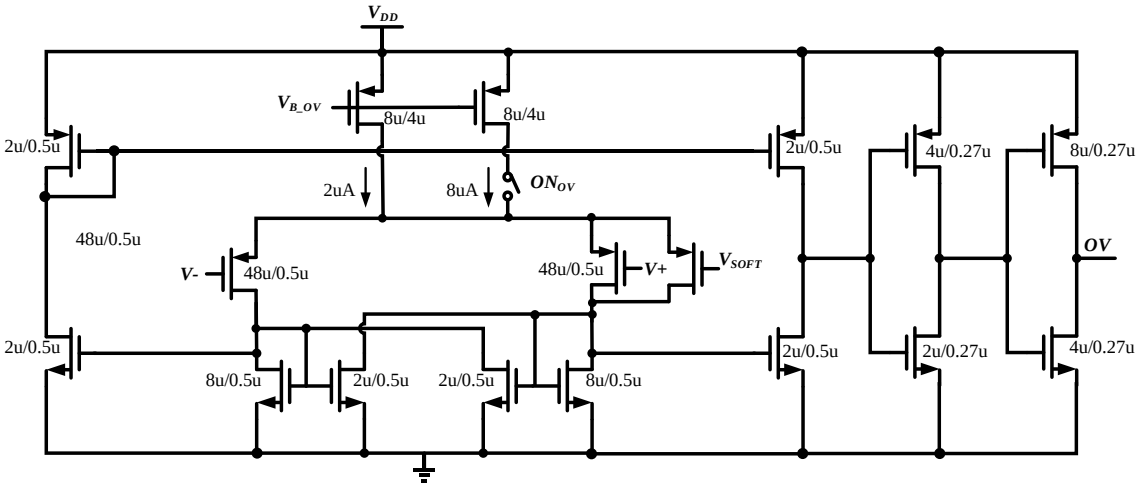

Figure 4.12. Overshoot Detection Comparator.

The feedback voltage V_{FB} is compared with a pair of reference voltages V_{LL} and V_{HH}, which is the undershoot and overshoot detection boundary, respectively. If $V_{FB}<V_{LL}$ or $V_{FB}>V_{HH}$, the undershoot or overshoot transient enhancement circuit will be triggered on, respectively.

The adaptive biasing control is added to reduce the power consumption. The control logic is shown in Figure 4.13.

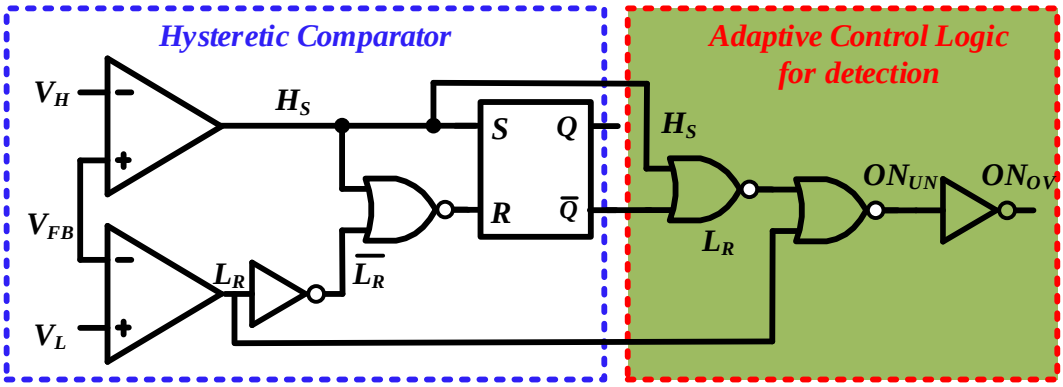

Figure 4.13. Adaptive Biasing Control Logic for Undershoot/Overshoot Detection.

The function behavior of the adaptive biasing logic and corresponding logic waveforms are demonstrated in Figure 4.14.

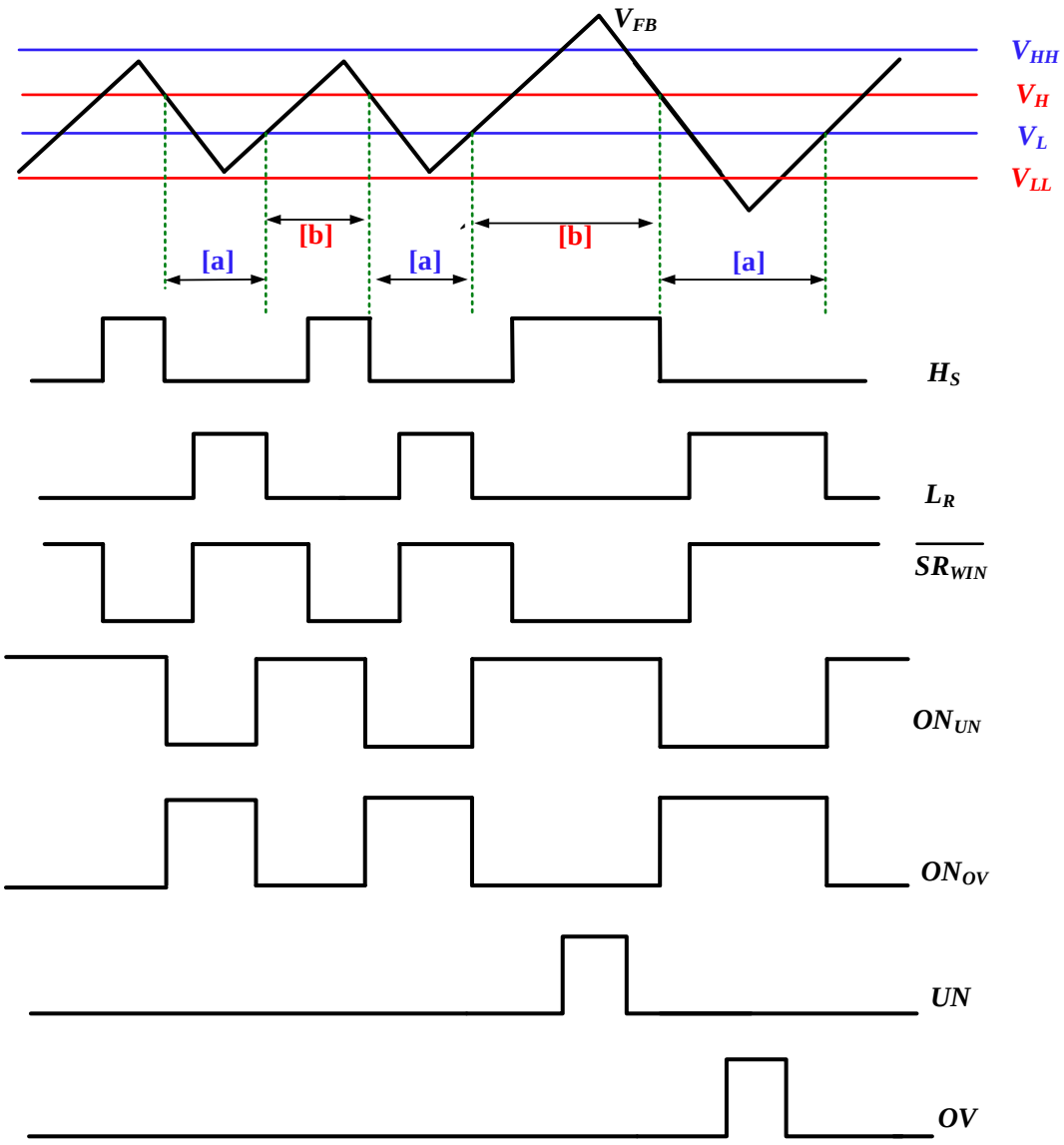

Figure 4.14. Adaptive Control Logic for Undershoot/Overshoot Detection.

V_H and V_L are the voltage boundaries of the window comparator stage, and V_{HH} and V_{LL} are the detection reference for the overshoot and undershoot detection comparator, respectively. ON_{UN}/ON_{OV} is the adaptive biasing control signal for undershoot/overshoot detection comparator, and UN/OV is the undershoot/overshoot

detection signal. Once $V_{FB} > V_{HH}$, OV is triggered to high. On the other hand, when $V_{FB} < V_{LL}$, the UN goes to high.

Period [a]/[b] is the designed as the adaptive biasing period for undershoot/overshoot detection comparator. Through this adaptive biasing control, the undershoot/overshoot detection comparator will be activated during only around half of the period, reducing the power consumption subsequently.

4.6 Power-Driving Tracked Hold Stage

As discussed in Chapter 3, the auxiliary current $I_P(t)$ can accelerate the transient response. The transient improvement is affected by the current magnitude I_P and hold-on duration of the $I_P(t)$. To achieve better transient enhancement, the pump current $I_P(t)$ should be hold on for a long enough time. On the other hand, the hold-on duration of $I_P(t)$ cannot be made too long because of the power loss. The optimal case is to hold on the $I_P(t)$ until the undershoot/overshoot is fully recovered. Once the $V_{out}(t)$ settles down, the $I_P(t)$ will be turned off to save power. Hence, the hold-on duration of $I_P(t)$ is required to be able to track the output voltage variation.

This is realized through the power-driving tracked hold stage, which is illustrated in Figure 4.15. It consists of three sub-stages: (1) wide pulse trigger stage, (2) pulse duration control stage and (3) exclude stage. *UN/OV* is the undershoot/overshoot detection signal. V_P/V_N is the power PMOS/NMOS driving voltage. WP_{UN}/WP_{OV} is the widened control signal triggered by *UN/OV* and $\overline{WP_{UN}}$ / $\overline{WP_{OV}}$ is their corresponding inverting signal. EN_{UN} and EN_{OV} is the pulse duration control signal for undershoot and overshoot wide pulse trigger stage, respectively. $\overline{HOLD_{UN}}$ /$\overline{HOLD_{OV}}$ is the output signal of the dual pulse hold stage for undershoot/overshoot.

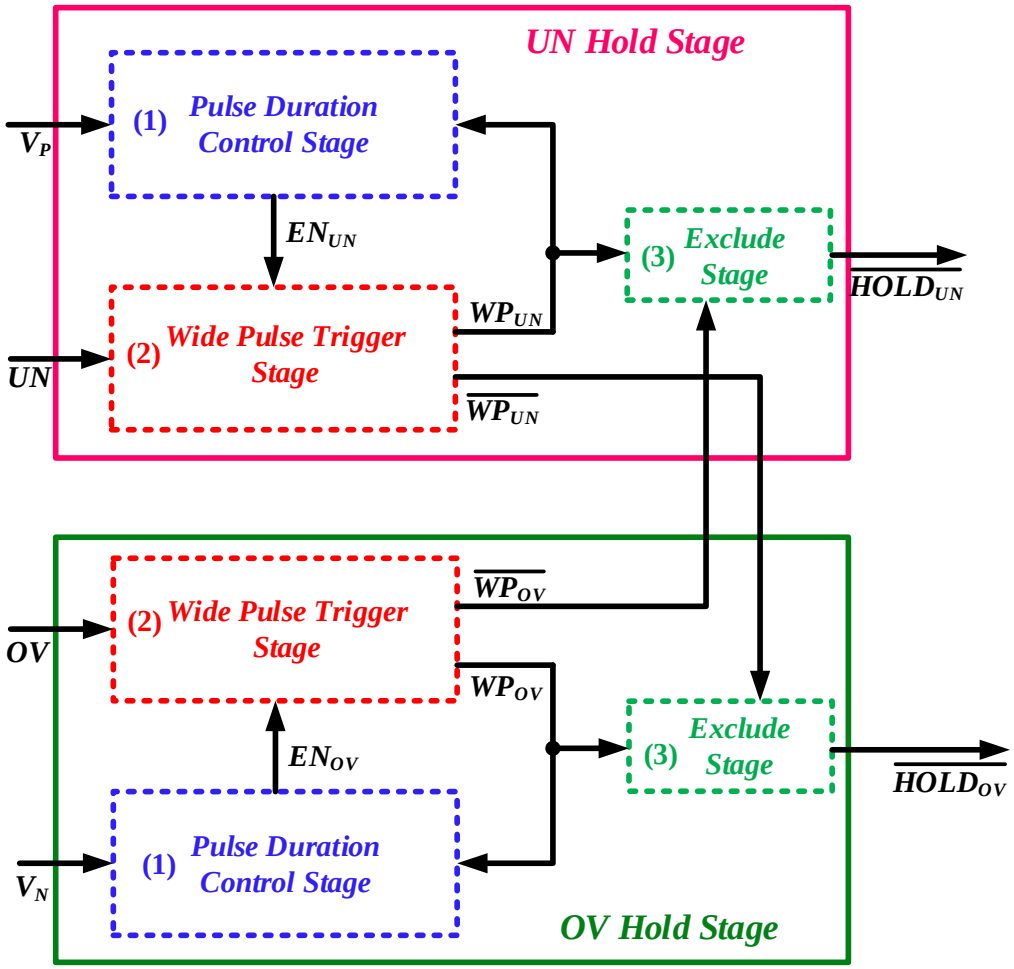

Figure 4.15. Dual Pulse Hold Stage.

The wide pulse trigger stage is to extend the short pulse undershoot/overshoot detection signal *UN*/*OV* such as to provide a long enough turn-on duration for $I_P(t)$. The endpoint of the wide pulse signal is determined by the pulse duration control stage, which detects the $V_{out}(t)$ by monitoring the power transistor driving voltage V_P and V_N. The exclude stage is to guarantee that *UN* and *OV* cannot be extended at the same time.

4.6.1 Wide Pulse Trigger Stage

As mentioned in Section 4.5, whenever undershoot/overshoot occurs, the *UN*/*OV* will be triggered by the window comparator pair. The *UN*/*OV* state changes whenever V_{FB} crosses V_{HH}/V_{LL}, giving a fast detection speed. This meets the requirement for the transient improvement. However, this narrow *UN*/*OV* causes insufficient turning-on duration for the $I_P(t)$, which will deteriorate the transient improvement as discussed in Section 3.2. To guarantee fast detection as well as sufficient turning-on duration, the turning-on and turning-off mechanism of the $I_P(t)$ is separated in this project. This is realized through the wide pulse trigger stage which is illustrated in Figure 4.16.

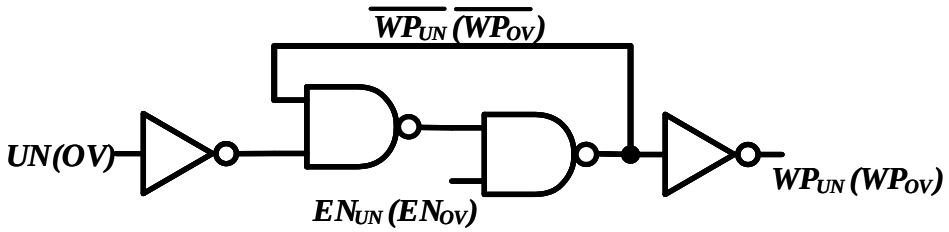

Figure 4.16. Wide Pulse Trigger Stage.

Use an undershoot detection as an example, this function can be explained as follows:

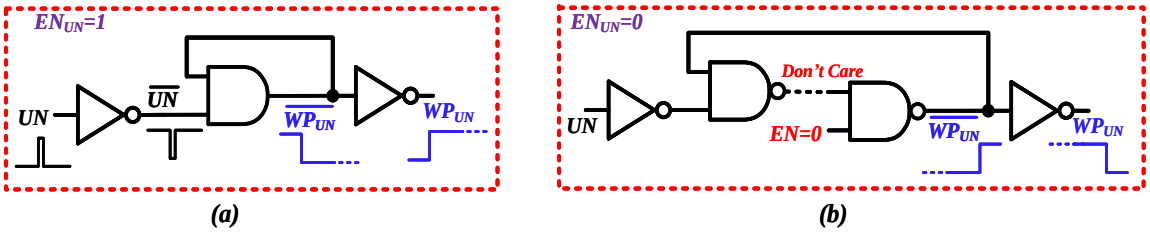

Figure 4.17. Equivalent Circuit for Wide Pulse Trigger Stage (a) EN_{UN}=1;(b) EN_{UN}=0.

When $EN_{UN}=1$, the equivalent wide pulse trigger stage is shown in Figure 4.17(a). When $V_{FB}<V_{LL}$, the narrow detection pulse UN goes to high, setting $\overline{WP}$ to 0 and WP to high. When $V_{FB}>V_{HH}$, UN drops to 0. Due to the feedback logic, $\overline{WP_{UN}}$ will be latched to 0 by itself and the WP_{UN} is kept at high. In this case, a wide pulse WP_{UN} can be triggered by the narrow UN pulse and the pulse duration of WP_{UN} is independent of UN. When $EN_{UN}=0$, the equivalent circuit is shown in Figure 4.17(b). In this case, the EN_{UN} will cut off the logic path and reset the wide pulse WP_{UN} to 0 regardless of the UN state.

It can be seen that the narrow trigger pulse UN is extended to a wide pulse WP_{UN} to provide sufficient hold-on duration for pump current $I_P(t)$. The rising edge of WP_{UN} is only triggered by UN when $EN_{UN}=1$. On the other hand, the falling edge of WP_{UN} is only controlled by the falling edge of EN_{UN}. As a result, the turning-on and turning-off mechanism of the $I_P(t)$ is separated. The falling edge of the EN_{UN} is realized through the pulse duration control stage.

4.6.2 Pulse Duration Control Stage

To improve the transient response of a voltage-mode hysteretic DC-DC converter, the $I_P(t)$ is required to be hold until the $V_C(t)$ recovery point $t"_{Recover}$ in Figure 3.10. After $V_C(t)$ recovers back, the $I_P(t)$ is required to be turned off to save power. In this project, the endpoint of the $I_P(t)$ duration is designed to be at t_{End} in Figure 3.10 and $t_{End}>t"_{Recover}$. In voltage-mode hysteretic buck converter, a large ESR value is required to keep $V_{out}(t)$ in phase with $I_L(t)$ and $I_L(t)$ is directly controlled by the power PMOS/NMOS transistor. Hence, the endpoint t_{End} can be determined by monitoring the power PMOS/NMOS transistor driving voltage V_P/V_N. This is realized through the circuit depicted in Figure 4.18.

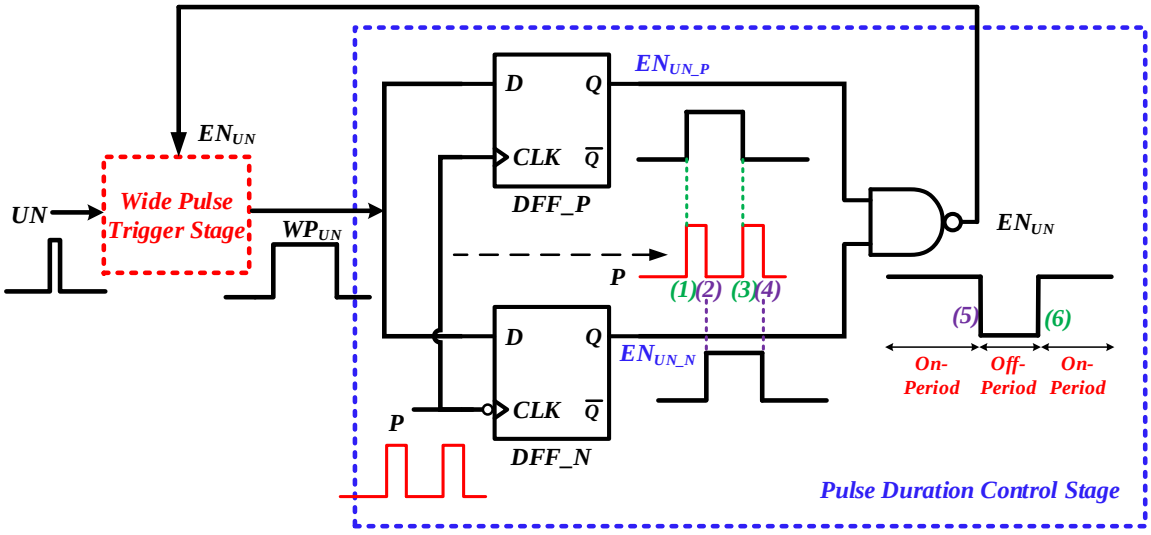

Figure 4.18: Pulse Duration Control Stage of Undershoot Detection.

DFF_P and DFF_N represents the positive and negative edge triggering D flip flop, respectively. WP_{UN} is the wide pulse triggered by the undershoot detection signal UN. V_P is the power PMOS transistor driving voltage, and edge (1) and (3) are the positive

edge while edge (2) and (4) are the negative edge. EN_{UN_P} and EN_{UN_N} are generated when the WP_{UN} goes through the flip flops DFF_P and DFF_N, respectively. EN_{UN} is the pulse duration control signal. When EN_{UN} is high, the wide pulse trigger stage is activated, and if UN is triggered, the wide pulse WP_{UN} will be generated. On the other hand, when EN_{UN} is low, the WP_{UN} will reset to 0 regardless of the state of UN. The corresponding waveform is illustrated in Figure 4.19.

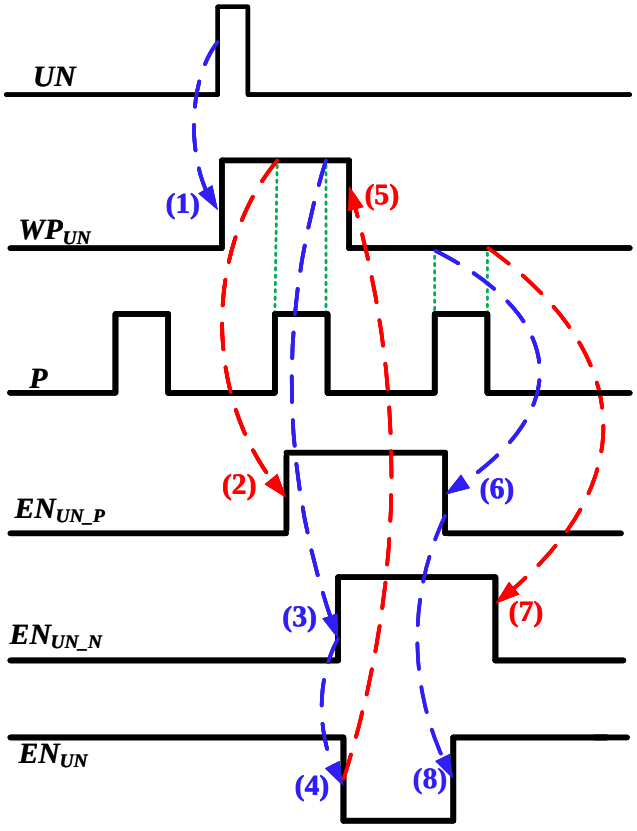

Figure 4.19: Timing Diagram of Pulse Duration Control Stage.

Initially, the wide EN_{UN} is high, activating the wide pulse trigger stage. When the undershoot occurs, UN goes to high, triggering the wide pulse WP_{UN} to be high at edge (1). This high WP_{UN} will be detected by the DFF_P and DFF_N to generate the

high EN_{UN_P}/ EN_{UN_N} at edge (2) and (3), respectively. When both EN_{UN_P} and EN_{UN_N} are high, EN_{UN} will be set to 0 at edge (4). The low level EN_{UN} will disable the wide pulse trigger stage and reset WP_{UN} to 0 at edge (5). As a result, the edge (5) determines hold-on duration of $I_P(t)$. The low level WP_{UN} will be continuously detected by the DFF_P and DFF_N to generate the low EN_{UN_P}/ EN_{UN_N} at edge (6) and (7), respectively. Once one of them is low, the EN_{UN} will be reset to high at edge (8), reactivating the wide pulse trigger stage again. This will ensure the power-driving tracked hold stage can work consecutively

The corresponding hold signal passing through the designed power-driving tracked stage for undershoot and overshoot is illustrated in the Figure 4.20 and Figure 4.21, respectively.

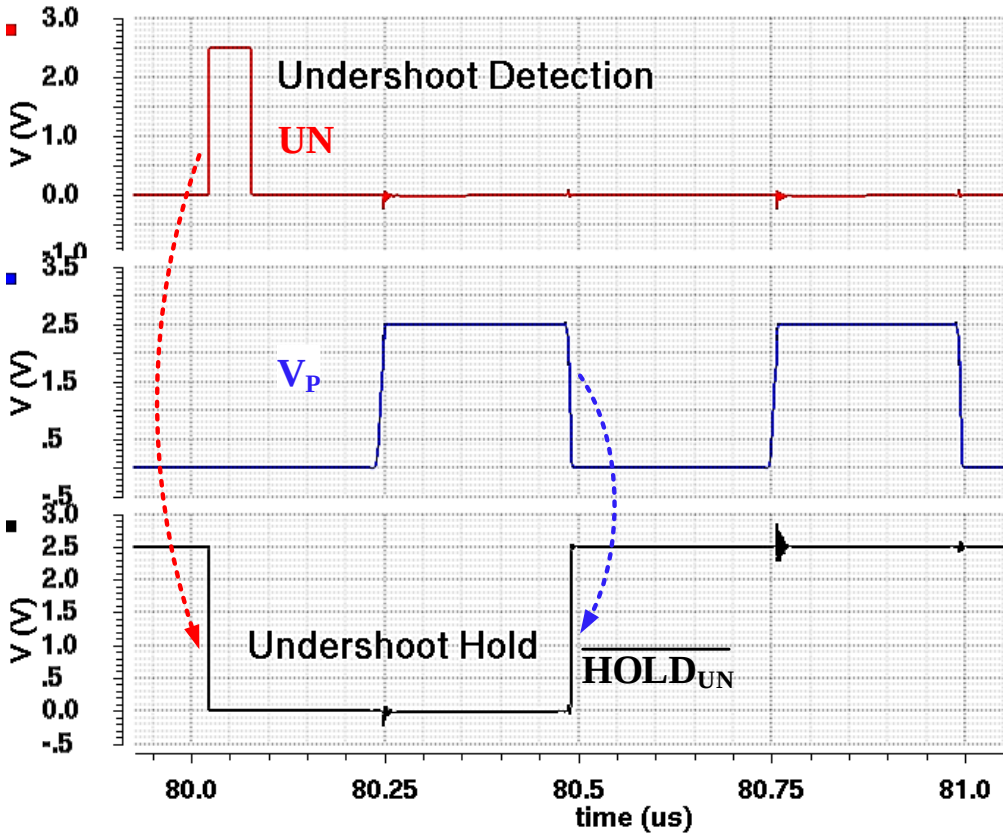

Figure 4.20: Pulse Extension Signals for Undershoot Detection.

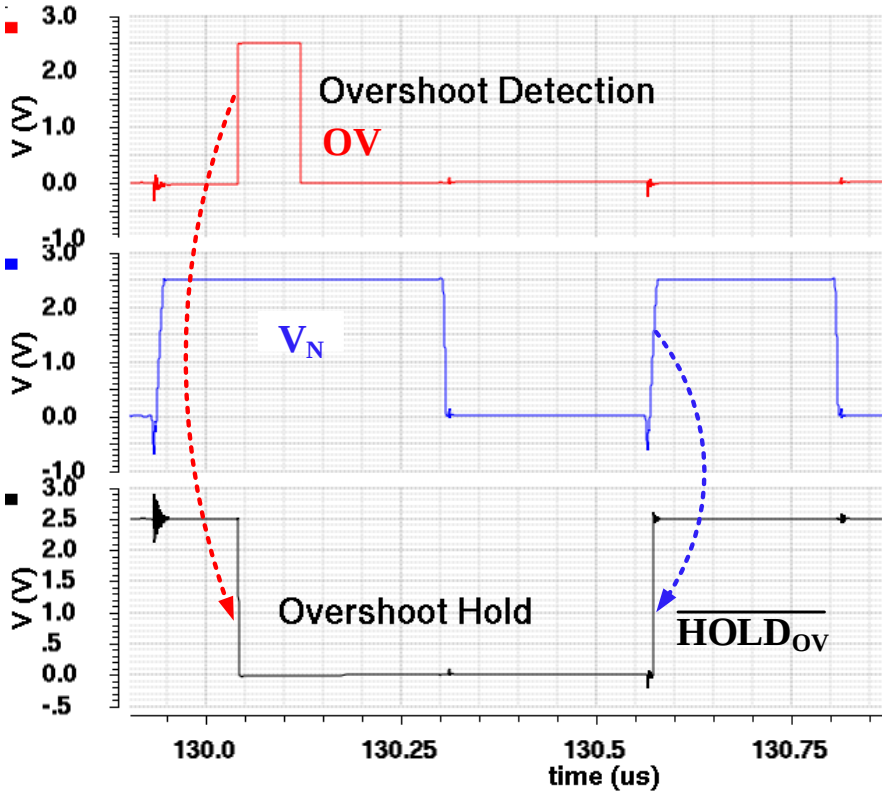

Figure 4.21: Pulse Extension Signals for Overshoot Detection.

Figure 4.20 and Figure 4.21 prove that the starting edge of the designed wide pulse signal is triggered by the undershoot/overshoot detection signal and the ending edge is determined by the second edge of V_P/V_N after the undershoot/overshoot detection as expected.

4.6.3 Exclusive Stage

To protect the overall system, the dual auxiliary pump current cannot be turned on at the same time. This can be achieved through the dual exclusive stage design shown in Figure 4.22. The WP_{UN}/WP_{OV} represents the wide pulse triggered by the detection

signal *UN*/*OV* and $\overline{WP_{UN}}$/$\overline{WP_{OV}}$ is the corresponding inverting signal. $\overline{HOLD_{UN}}$ /$\overline{HOLD_{OV}}$ is the final output signal after the power-driving tracked hold stage.

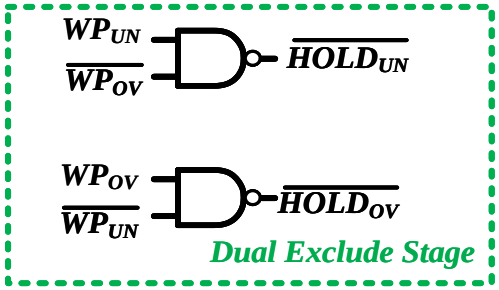

Figure 4.22: Dual Exclusive Control Stage.

This stage is to ensure the *UN*/*OV* cannot be passed at the same time. As a result, the auxiliary pump-in and pump-out current cannot be turned on at the same time. Hence no short-through occurs.

4.7 Hold-Period Delayed Ramping Generator

After the output voltage settles down, the $I_P(t)$ is turned off at t_{End}. However, if the $I_P(t)$ is turned off instantly, a large current difference between $I_L(t)$ and $I_P(t)$ will be generated, which has the same effect as the $I_R(t)$ change. As observed, multiple undershoot/overshoot effect will be induced [37], [38], deteriorating the transient response performance as well as the system stability. This problem can be solved by turning off $I_P(t)$ slowly such that the $I_P(t)$ change can be compensated by the $I_L(t)$. This is realized by generating a ramping period to slow down the ramping-up speed of the $I_P(t)$ control voltage $V_{GS}(t)$, which is illustrated in Figure 4.23.

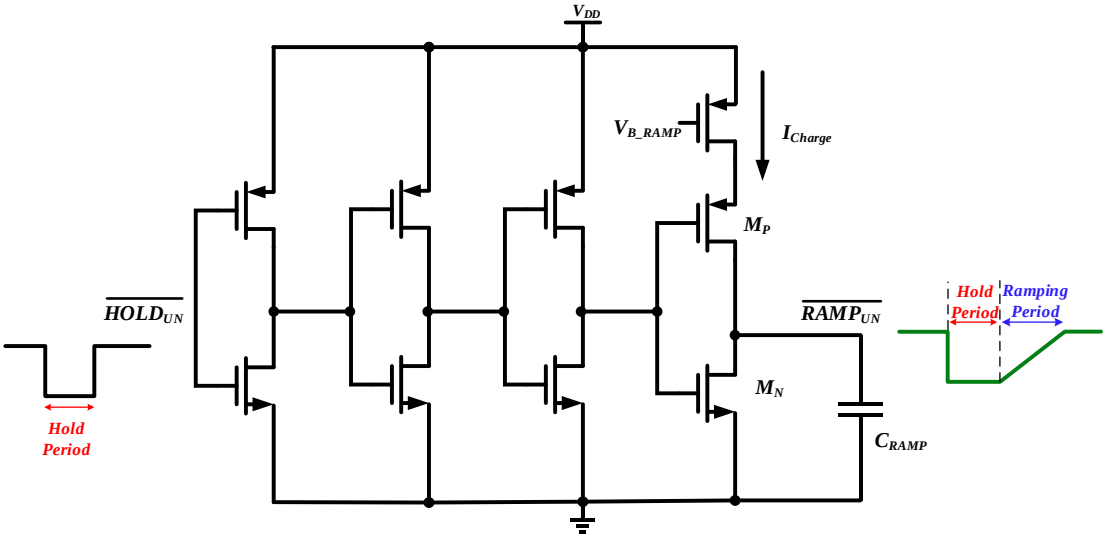

Figure 4.23: Hold-Period Delayed Ramping Generator.

$\overline{HOLD_{UN}}$ and $\overline{RAMP_{UN}}$ indicates the power-driving tracked hold signal and the $I_P(t)$ control voltage $V_{GS}(t)$, respectively. $\overline{RAMP_{UN}}$ is required to go down instantly to enhance the transient response. On the other hand, a relatively slow ramp-up slope is

essential to avoid multiple undershoot/overshoot effect. M_N has relatively larger aspect ratio than that of M_P. Once a large undershoot is detected, will goes to 0, discharging the capacitor C_{RAMP} rapidly through the large size M_N. As a result, $\overline{RAMP_{UN}}$ is pulled down instantly whereas the $I_P(t)$ is triggered on instantly to enhance the transient response. After the $V_{out}(t)$ recovers back, $\overline{HOLD_{UN}}$ is reset to high at t_{End} instantly to cut off the $I_P(t)$. Different from the $\overline{HOLD_{UN}}$, a ramping period is generated in $\overline{RAMP_{UN}}$ by a relatively small constant current I_{Charge} to slow down the $I_P(t)$ changing rate. If the $I_L(t)$ can compensate the $I_P(t)$ change, the multiple undershoots/overshoots will be significantly reduced or even eliminated. The ramp-up rate of $\overline{RAMP_{UN}}$ is given as

$$\frac{d\overline{RAMP_{UN}}(t)}{dt} = \frac{I_{charge}}{C_{RAMP}} \tag{98}$$

The simulation result for the input and output of the hold-period delayed ramping stage is shown in Figure 4.24.

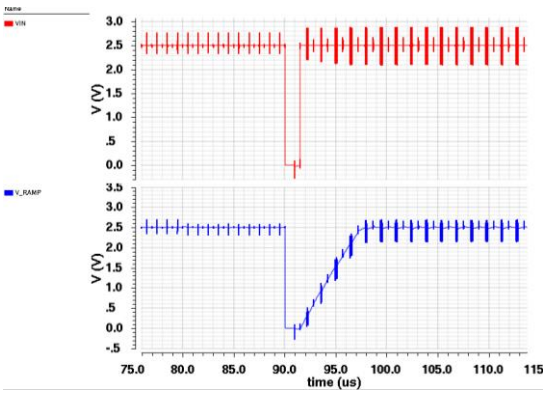

Figure 4.24: Simulation Result of Hold-Period Delayed Ramping Generator.

4.8 Dual Pump Current Stage

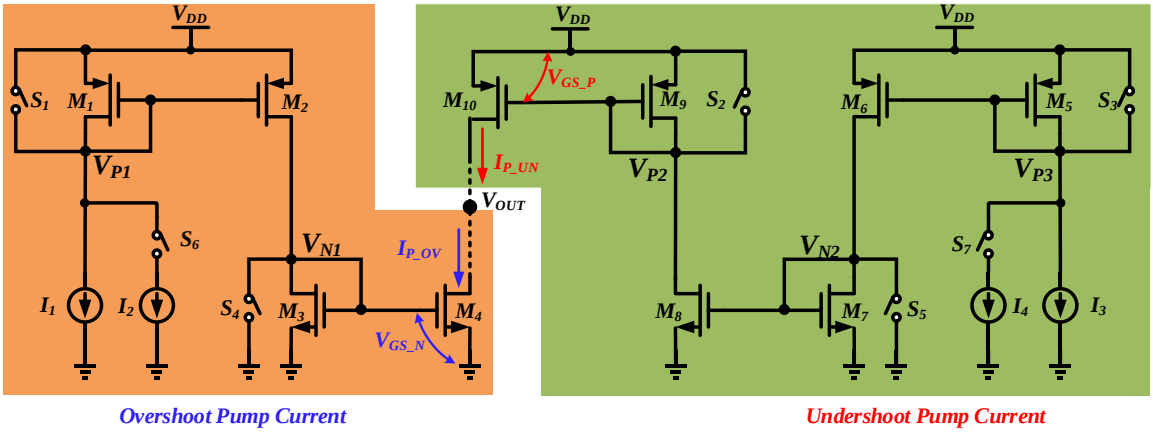

Figure 4.25: Dual Pump Current Stage.

As depicted in Figure 4.25, the undershoot and overshoot pump current (I_{P_UN} and I_{P_OV}) are added to the output node directly. The I_{P_UN} and I_{P_OV} are designed to be supply independent through the constant biasing current I_1-I_4. S_1-S_7 are controlled by the ramping voltage $\overline{RAMP_{UN}}$ or $\overline{RAMP_{OV}}$. Hence, I_{P_UN}/ I_{P_OV} can be instantly turned on to enhance the transient response and slowly turned off to reduce the multiple undershoot/overshoot. During the steady state, S_1-S_5 are turned on, pulling V_{P1}, V_{P2} and V_{P3} up to V_{DD} while pulling V_{N1} and V_{N2} down to ground. In this way, the I_{P_UN} and I_{P_OV} can be totally off to save power. I_1 and I_3 are always on to speed up the pump current start-up process. I_2 and I_4 are adaptively controlled by S_6 and S_7 to reduce the quiescent current.

The pump-in/pump-out current under a 200-mA step-up/step-down load current

change as well as the switch control voltages are illustrated in Figure 4.26.

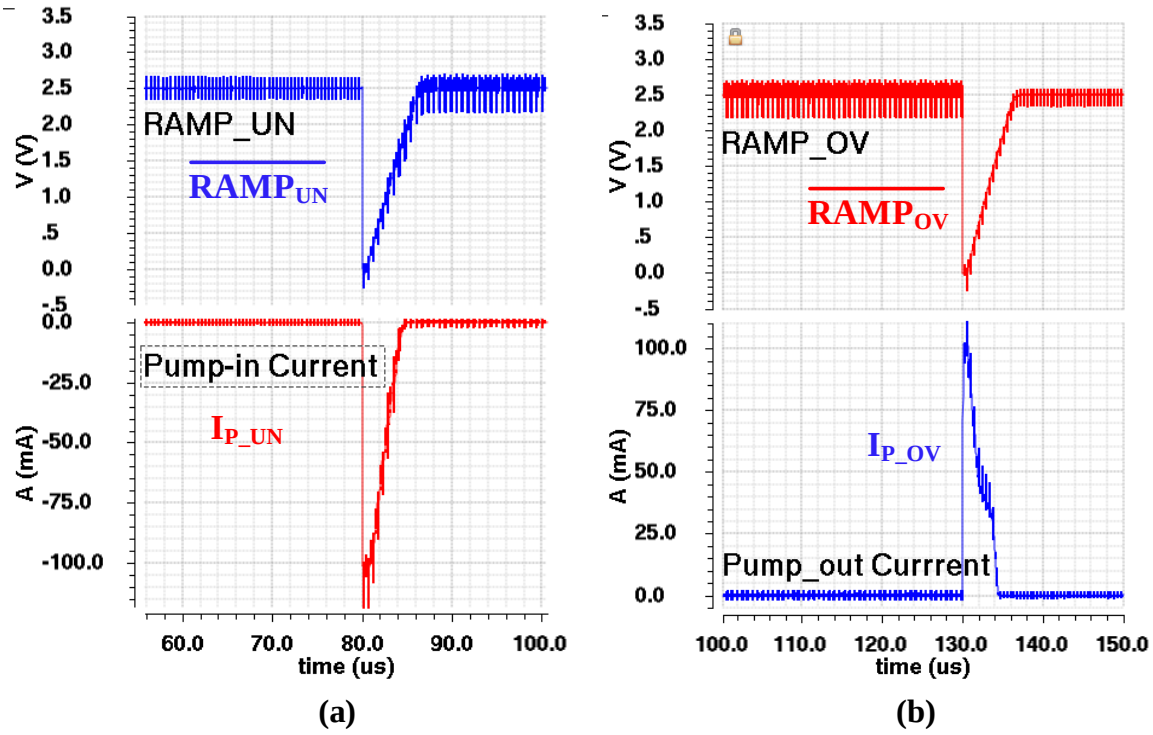

Figure 4.26. Switch Control Voltage and Pump Current for (a) Undershoot; (b) Overshoot.

Both switch control voltages are obtained after the ramping generator, and they are used to control the pump-in and pump-out current. Both pump-in and pump-out currents are instantly turned-on while slowly turned off as expected. The turning-off slope is approximately linear due to the linear ramping-up control voltage.

4.9 Discontinuous Mode Operation

As discussed previously, during the heavy load condition where $I_R>0.5I_L$, the inductor current always flows from the switching node L_X to the output node. No reverse current occurs. On the other hand, during the light load condition, if $I_R<0.5I_L$, the minimum inductor current, I_{Lmin} will be smaller than 0. In this case, the inductor current reverses back from the output node to ground through the turned-on NMOS path. This will induce a significant power loss in the light load condition. To improve the light load efficiency, the control algorithms are required to allow the DC-DC converters to switch between continuous conduction mode (CCM) and discontinuous conduction mode (DCM) [5], [35], [68].

When NMOS/PMOS power transistor is turned on/off, the switching node L_X is connected to ground and the inductor current starts to drop. Due to the inductor current continuity, there is a current flowing from ground to the inductor. The switching node voltage V_X is smaller than ground because of the voltage drop over the NMOS on-resistance. Since the inductor current falls gradually, V_X rises linearly but still lower than ground. The inductor current will reverse back after it continuously drops to be lower than 0, which creates a positive voltage drop over the NMOS on-resistance. As a result, V_X is larger than ground when NMOS is on. Hence, the reverse current can be detected by comparing V_X with ground during NMOS on period.

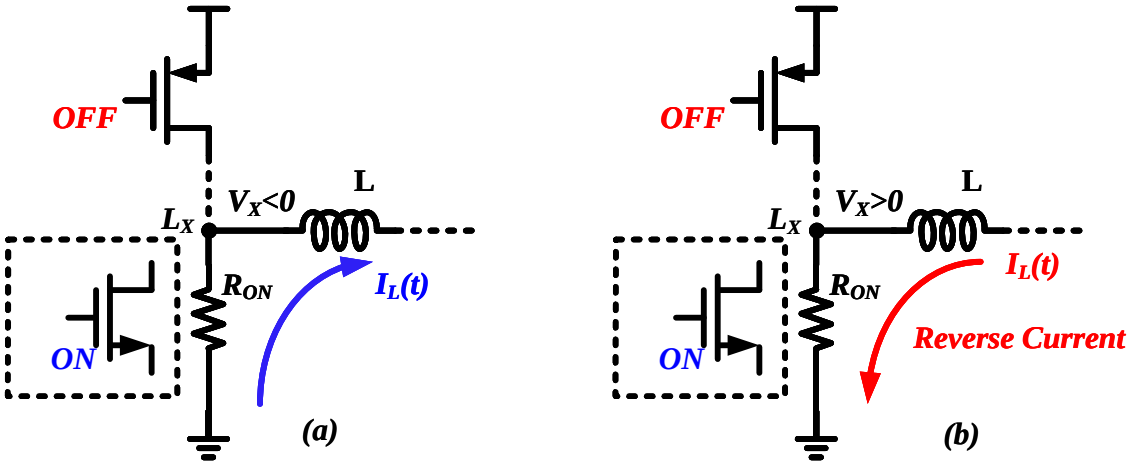

Figure 4.27. Inductor Current Diagram (a) without; (b) with Reverse Current.

4.9.1 Zero Voltage Detector(ZVD)

The basic principle for reverse current detection is to compare the V_X with ground, and to turn off NMOS immediately once $V_X>0$. For conventional DC-DC converters, reverse current detection is usually realized by either common-source (CS) comparator [5] or common-gate (CG) comparator [69]. Comparing with CS comparators, CG comparators have a simpler structure and faster response. However, most of the previous methods always operate during the full period of DC-DC converters. In fact, the inductor current is only possible to reverse back during the NMOS on period. Thus, the quiescent power consumption can be reduced by switching the ZVD into sleep mode when it is not necessarily active. In this project, the common gate ZVD with low power consumption is realized and the schematic is shown in Figure 4.28.

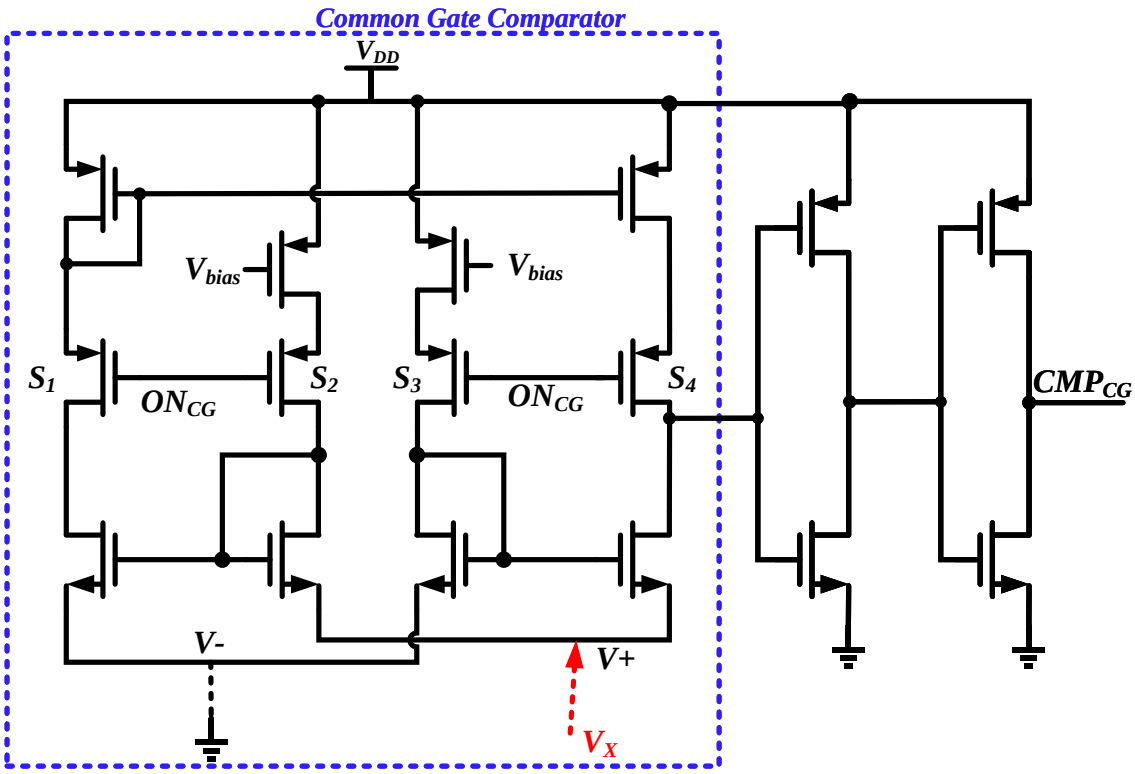

Figure 4.28. Zero Voltage Detector.

The ZVD consists of a common gate comparator input stage and a chain of inverters as the output stage. The non-inverting input ($V+$) of ZVD is connected to V_X and the inverting input ($V-$) is shorted to ground. CMP_{CG} and ON_{CG} is the output signal and the switch control signal, respectively. The ZVD can switch between the active mode and sleep mode controlled by the switch S_1~S_4. When ON_{CG} is high, ZVD goes into the sleep mode. When ON_{CG} is low, ZVD is active. Once V_X is larger than ground, ZVD will go to high, when the reverse current has been detected.

4.9.2 DCM Logic and Freewheel Switch Control

Once the reverse current is detected, the DC-DC converter should operate in the

DCM to improve the light load efficiency. The operation mode switch is realized by the DCM decision logic. The NMOS should be immediately turned off to cut off the reverse current path in order to reduce the power loss. In this case, V_X is close to zero after NMOS turns off. A large voltage gap is created between V_X and V_{OUT}. The inductor current will charge the large parasitic capacitor at L_X, which forms an LC tank with the output inductor. The energy is transferred back and forth, and the ringing effect appears. To solve this problem, a freewheel switch (FWS) transistor is added to release the energy stored in the inductor and parasitic capacitor when both NMOS and PMOS is turned off. To eliminate the ring effect and achieve a smooth inductor current waveform at DCM, FWS transistor should have a sufficiently large size to provide a low impedance path [35],[70]. The FWS connection is shown in Figure 4.29.

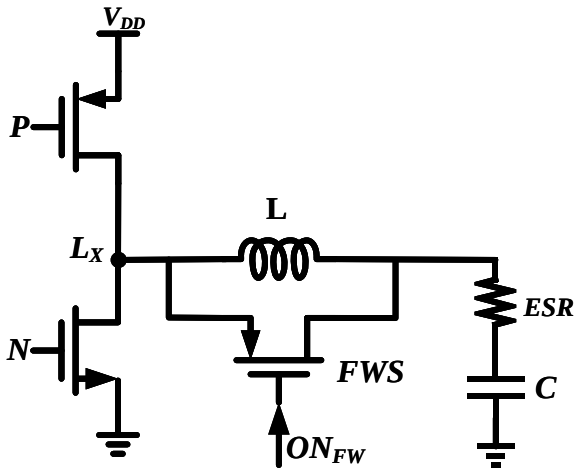

Figure 4.29. Freewheel Switch Connection.

The timing diagram of DCM, FWS logic and inductor current are illustrated in the Figure 4.30.

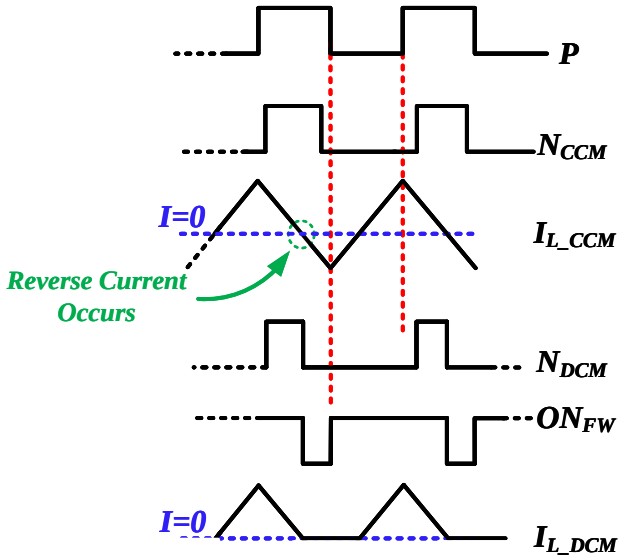

Figure 4.30. Time Diagram of DCM And FWS Control Logic and Inductor Current.

P and ON_{FW} is the control signal of PMOS and FWS, respectively. N_{CCM}/N_{DCM} represents the driving voltage of NMOS in CCM/DCM and I_{L_CCM}/I_{L_DCM} is the corresponding inductor current. Note that NMOS is required to be immediately cut off once the reverse current occurs in DCM. It should be kept off until being triggered on again in the following switch cycle. FWS should be turned and hold on when the reverse current occurs until PMOS is triggered on in the following switch cycle. As a result, no inductor current will reverse back to the ground and the ring effect at the switching node L_X is eliminated in the DCM. Finally, the light load efficiency of the designed DC-DC converter will be improved.

The corresponding control logic of DCM and FWS control logic is realized by the circuit in Figure 4.31. ON_{FW} and N_D represents the control logic of FWS and NMOS driving stage input signal, respectively. CMP_{CG} is the CG comparator output signal. *P/N* is the driving voltage of PMOS/NMOS power transistor. *ZVD* is the modified reverse current detection signal, which is wide pulse triggered by CMP_{CG} when *N* is high. Note that *ZVD* is less sensitive than CMP_{CG} and it is independent on the CMP_{CG} variation once the reverse current is detected until NMOS is turned off. P_{NON}/N_{NON} is the corresponding non-overlapped output signal for PMOS/NMOS driving after the dead time control stage. *P1* is the input signal feeding into the PMOS driving stage. *P1* and *P2* are leading and legging signal of P, respectively.

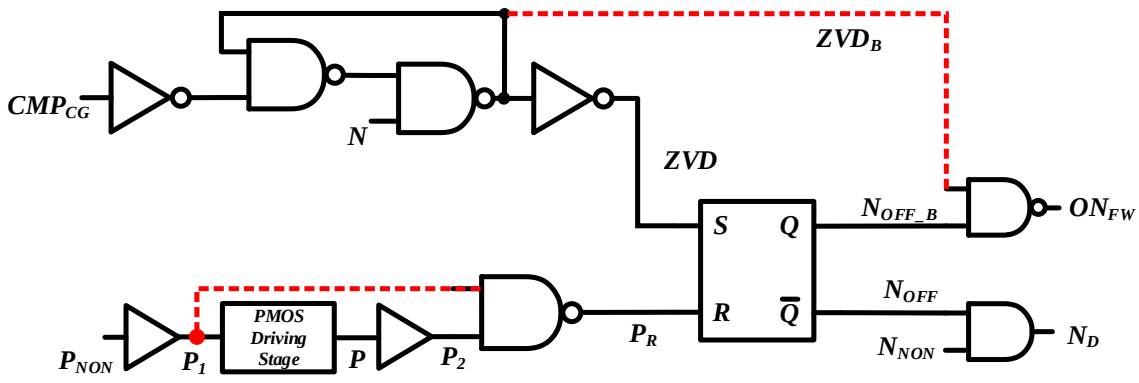

Figure 4.31. Schematic of DCM and FWS Control Logic Circuit.

When both *N* and *P* are high, the power NMOS/PMOS is on/off, the inductor current starts to fall and P_R goes to low. Once $I_L<0$, the reverse current occurs, $V_X>0$ and CMP_{CG} as well as ZVD goes to high. Thus, N_{OFF} is set to 0 to cut off the NMOS path and N_{OFF_B} is set to V_{DD} to turn on FWS. Note that it is necessary to ensure there is

no short path through the PMOS/NMOS and FWS. To achieve the required signal exclusion, to extra signal is added in, which is highlighted in red dot line.

- P_1 is added to ensure that FWS is off ahead of PMOS is on
- ZVD_B is to ensure that sure FWS is on after NMOS is totally off

4.9.3 ZVD Enable Logic

The quiescent power consumption can be reduced by switching ZVD into sleep mode when it is not necessary to be activated. This is controlled by the ZVD enable logic and its schematic is depicted in Figure 4.32.

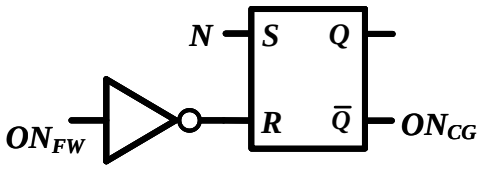

Figure 4.32. ZVD Enable Logic.

The ZVD is only necessary to be activated when NMOS is on. Once the DC-DC converter switches into the FWS period, ZVD can be released into the sleep mode to save power until the following NMOS on period.

4.10 Over-current Protection

Over-current protection is important in DC-DC converter design due to safety reason, especially for the hysteretic converters because of their clock free topology [1], [13], [15], [49]–[51], [71], [72]. The over-current protection stage is designed to prevent huge inrush current especially during the start-up period. It will also set the maximum allowable inductor current passing through the converter as well as the maximum load current limit. The common over-current protection circuit is shown in Figure 4.33.

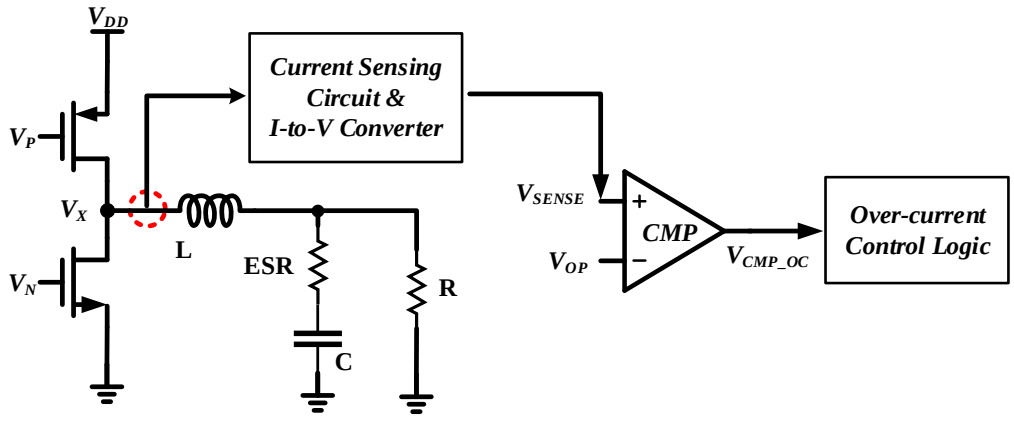

Figure 4.33. Over-current Protection Circuit.

The inductor current is sensed and converted into a corresponding voltage signal through the designed current sensing and current-to-voltage converter. The sensed current signal (in voltage) is compared with a reference voltage, V_{OP} to generate the over-current detection signal, V_{CMP_OC}. If $V_{SENSE} > V_{OP}$, it will turn off the PMOS through the over-current control logic, ramping down the inductor current.

4.10.1 Current Sensing Circuit

An on-chip current sensing circuit is applied for the over-current protection, which is shown in Figure 4.34 [1], [13], [71]–[73].

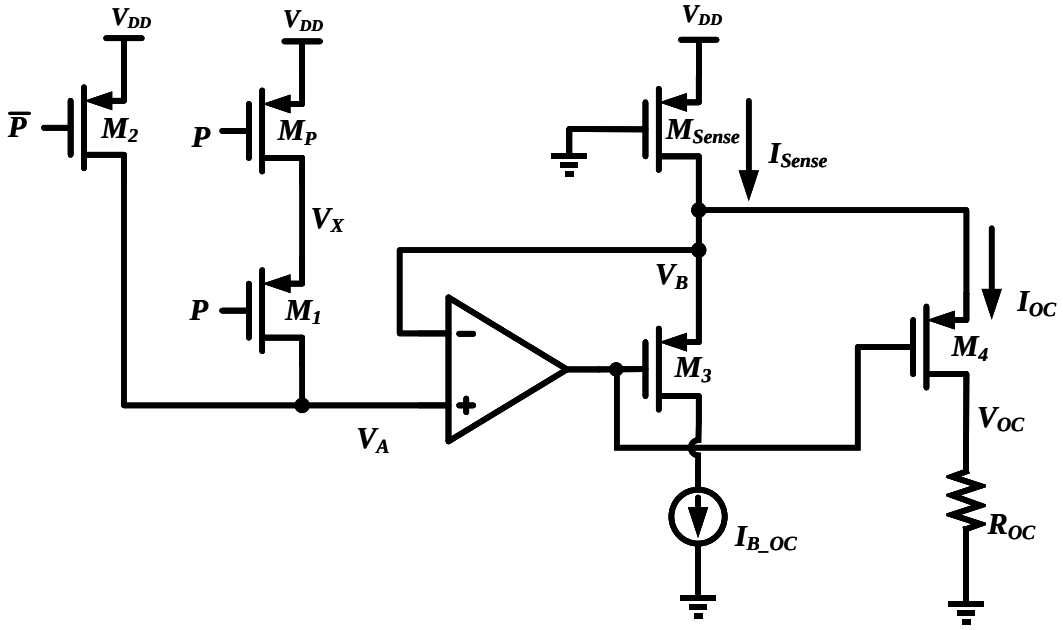

Figure 4.34. On-chip Current Sensing Circuit and I-to-V Converter.

The current sensing technique is achieved by a matched PMOS transistor M_{Sense} with a much smaller aspect ratio than that of the power PMOS transistor M_P. A high-gain op-amp forms a negative feedback with M_3 to make V_B track with V_A. During the power PMOS on period, P is low, turning on M_P and M_1. V_A is shorted to V_X, and V_B tracks with V_X. Thus, the PMOS current in the power stage can be copied to I_{Sense}. The switch transistors M_1 and M_2 are used to ensure that V_A will be tied to V_{DD} during the PMOS off period. As a result, only a small amount of current will flow through the sensing resistor R_{OC} in the PMOS off period. This will avoid wrong over-current

detection signal generation and reduce the current consumption. This will also guarantee fast track response of the current sensing [1].

Since V_X is a rail-to-rail signal, to provide high sensing accuracy, both V_A and V_B should be able to track V_X up to V_{DD}. A folded-cascode op-amp is applied to provide wide input tracking range up to V_{DD} and its circuit is shown in Figure 4.35 [74]–[79]. The biasing current I_{B_OC} is generated from the biasing circuit, it is added to provide the offset voltage to permit V_B to track with V_A up to around V_{DD}. The folded-cascode op-amp also provides high gain to improve the current sensing accuracy.

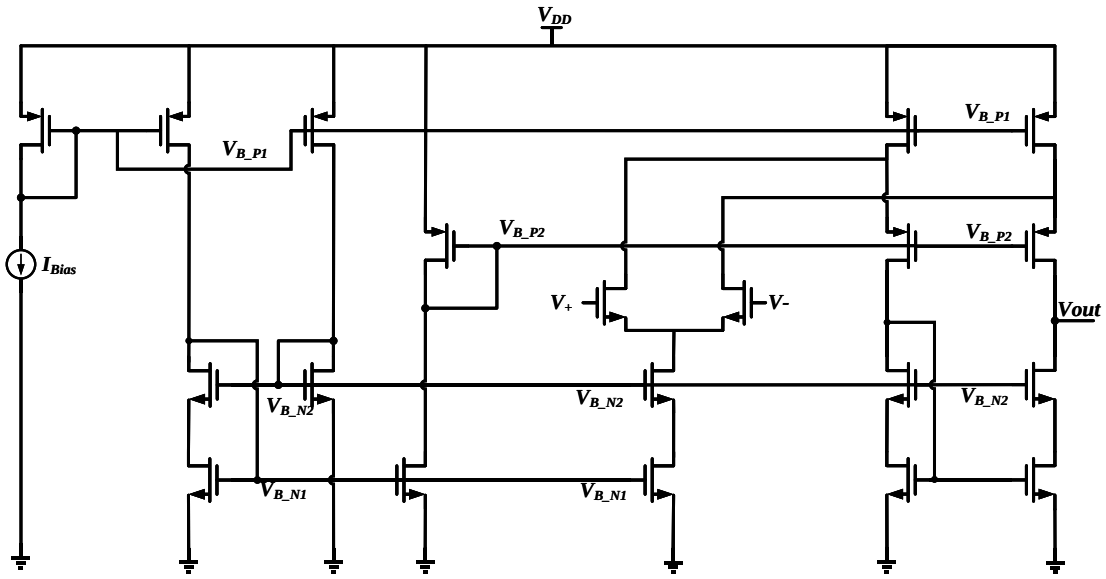

Figure 4.35. Designed Folded-cascode Op-Amp.

4.10.2 Over-current Control Logic

Whenever over-current occurs, the power PMOS/NMOS transistor should be turned off/on to ramp down the inductor current, thus protecting the overall system. The

over-current protect signal should also be able to release the inductor current to ramp up again. In this project, the over-current protect stage will force the power PMOS/NMOS to be off/on to reduce the inductor current to zero. Once the inductor current reaches zero, the PMOS/NMOS will be released to on/off again. These functions can be realized through the control logic depicted in Figure 4.36.

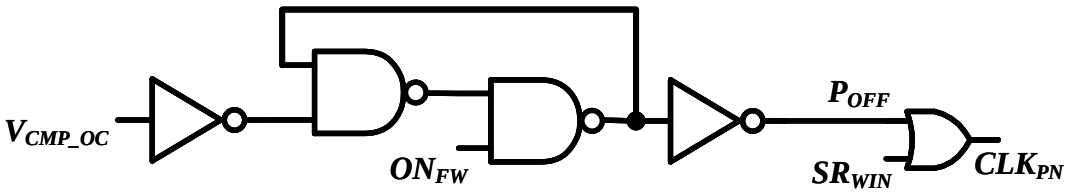

Figure 4.36. Over-current Control Logic.

V_{CMP_OC} is the over-current detection signal, and ON_{FW} is the control signal of FWS. P_{OFF} is the designed over-current protection signal to force the PMOS off. SR_{WIN} is the control logic after the window comparator stage, and CLK_{PN} is the new control signal feeding to the dead time control stage.

When over-current is detected, V_{CMP_OC} goes to high and ON_{FW} is high as well. V_{CMP_OC} is hold through the wide pulse trigger stage to generate P_{OFF}. P_{OFF} goes high and overwhelm SR_{WIN} to force PMOS/NMOS to be off/on. As a result, the inductor current starts to drop. Since P_{OFF} is latched at high, the inductor current continues to drop. Once I_L reaches zero, ON_{FW} will be triggered to ground. Hence, P_{OFF} will be reset to ground, releasing the DC-DC from the over-protection period. The inductor current will start to ramp up again.

4.11Soft Start Circuit

At the beginning of startup phase in DC-DC converters, the inductor current will rise very rapidly while dropping very slowly in each switching period due to the low initial output voltage. As a result, a massive inrush current will be generated in the first few switching periods. This large inrush current will charge up the output capacitor very rapidly, causing a severe overshoot voltage. On the other hand, the power supply may be pushed down too much that the function of other modules in the same power line may be deteriorated. To solve these problems, a soft-start circuit is required to smooth the inrush current and output overshoot voltage [15], [80]–[82] .

This conventional soft-start circuit is based on replacing the normal voltage reference with a slowly and linearly ramped-up reference. In this way, the output voltage can easily follow the reference to climb up, thus the inrush current and output overshoot can be reduced. A steadily rising voltage is usually accomplished by charging a capacitor with a constant current. The corresponding soft-start time can be calculated as:

$$V_{SOFT} = \frac{V_{REF} \times C_{SOFT}}{I_C} \tag{99}$$

Note that V_{REF} is the threshold voltage which determines the end of the soft-start period, C_{SOFT} is the capacitor value to be charged up and I_C is the charging current. However, to get a long soft-start time, a large capacitor size or extra pin-out is needed, increasing the cost and circuit size. On the other hand, to use a small on-chip

capacitor, a current of several *nA* is required, which is quite difficult to be precisely controlled [81].

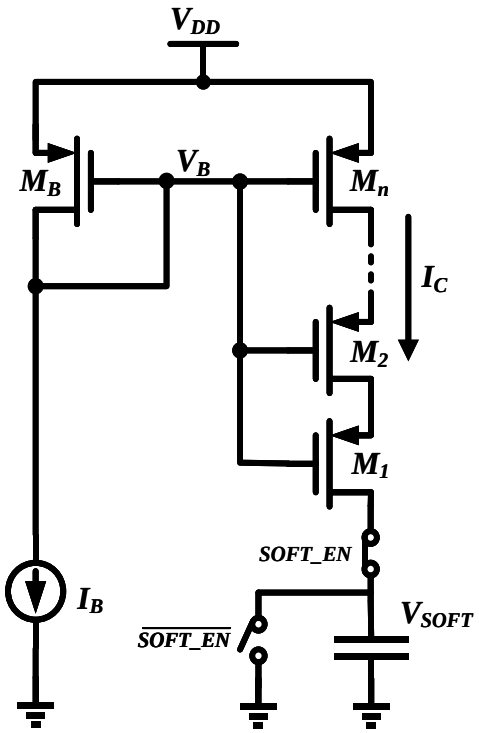

Figure 4.37. On-Chip Soft-start Ramp Generator.

In this project, a simple and effective soft-start circuit is employed as shown in Figure 4.37. The current source I_B is generated by the biasing circuit in the system. In this circuit, if V_{SOFT} is well below V_{DD}, only M_1 works in saturation region, while M_2-M_n works in triode region. As a result, the nA order charging current can be achieved easily, thus a long soft-start time can be achieved. This method can reduce the silicon area dramatically and this circuit does not need extra pin-out and discrete capacitor [15].

4.12Biasing Circuit

The self-biasing peak current source [63] is used in this project to provide supply independent biasing current to comparators, dual pump current stage and other necessary blocks. The biasing circuit is depicted in Figure 4.38 [63], [74], [75], [78], [83].

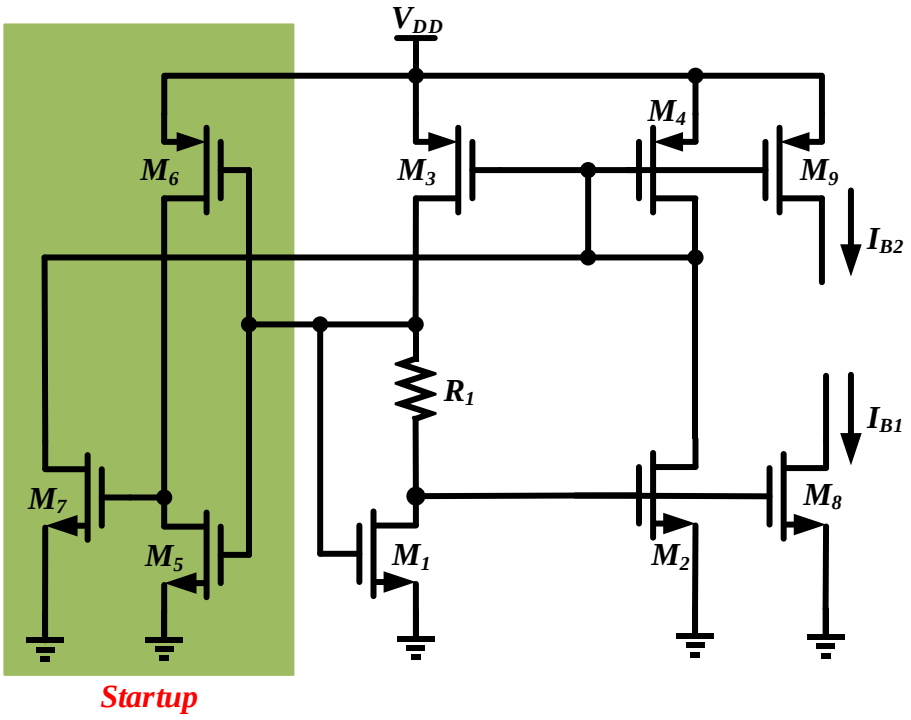

Figure 4.38. Self-Biasing Circuit.

To obtain good power supply rejection, $R_1=g_{m1}$ is required where g_{m1} is the transconductance of M_1. The startup circuit consists of M_5-M_7. M_5 has a wide channel width whilst M_6 requires a long channel length. I_{B1} and I_{B2} represent the sink and source biasing current for internal blocks, respectively.

4.13 Reference Generator

Due to the pad limitation, multiple internal reference voltages are generated through the reference generator shown in Figure 4.39.

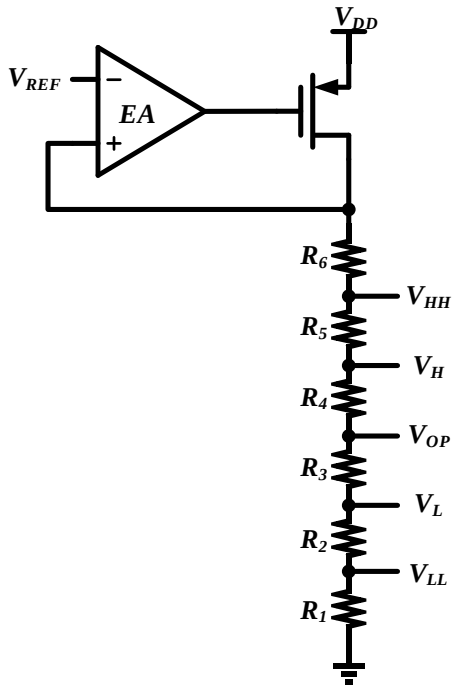

Figure 4.39. Schematic of Reference Generator.

V_{REF} is the external reference voltage. V_H/V_L is the hysteretic comparator high-side/low-side reference voltage. V_{LL} and V_{HH} is the undershoot and overshoot detection reference voltage, respectively. V_{OP} is the reference voltage for over-current protection, which is shown in Figure 4.33.

Chapter 5 Measurement Results and Discussions

The buck converter has been implemented using the TSMC 40nm CMOS process. The power transistors are placed such that the current path is short, hence reducing the power loss. The layout of power transistors layout is carefully drawn in such a way that the current density is made well-balanced. The layout and chip micrograph of the proposed buck converter is depicted in Figure 5.1 and Figure 5.2, respectively.

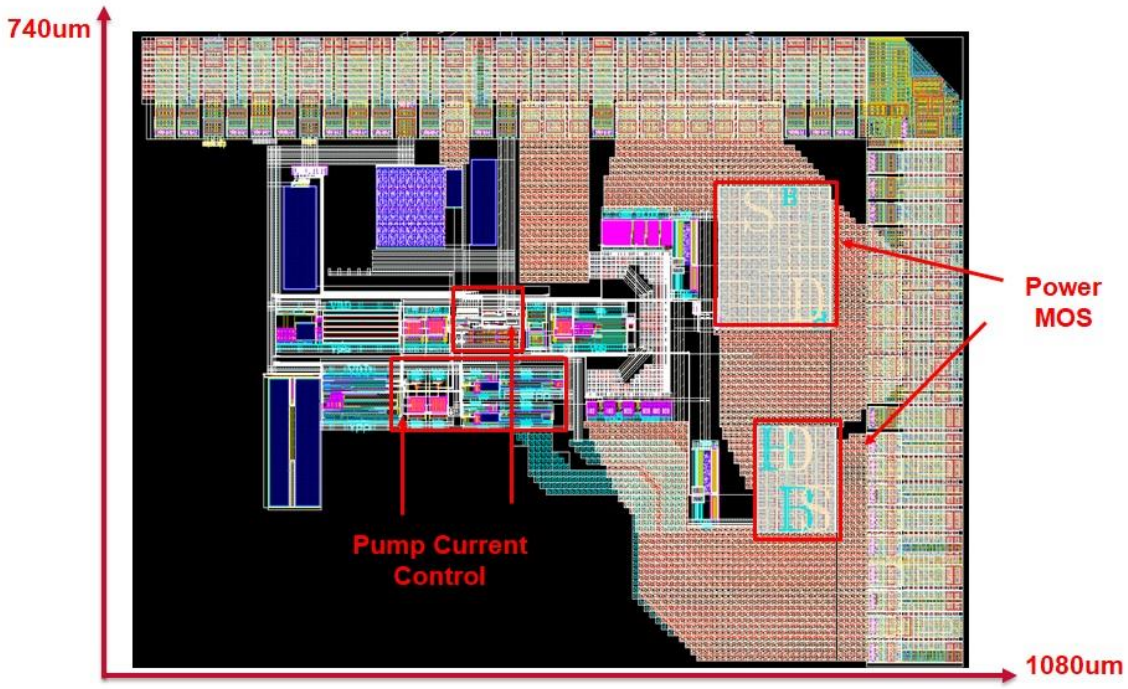

Figure 5.1. The Layout of Proposed Buck Converter.

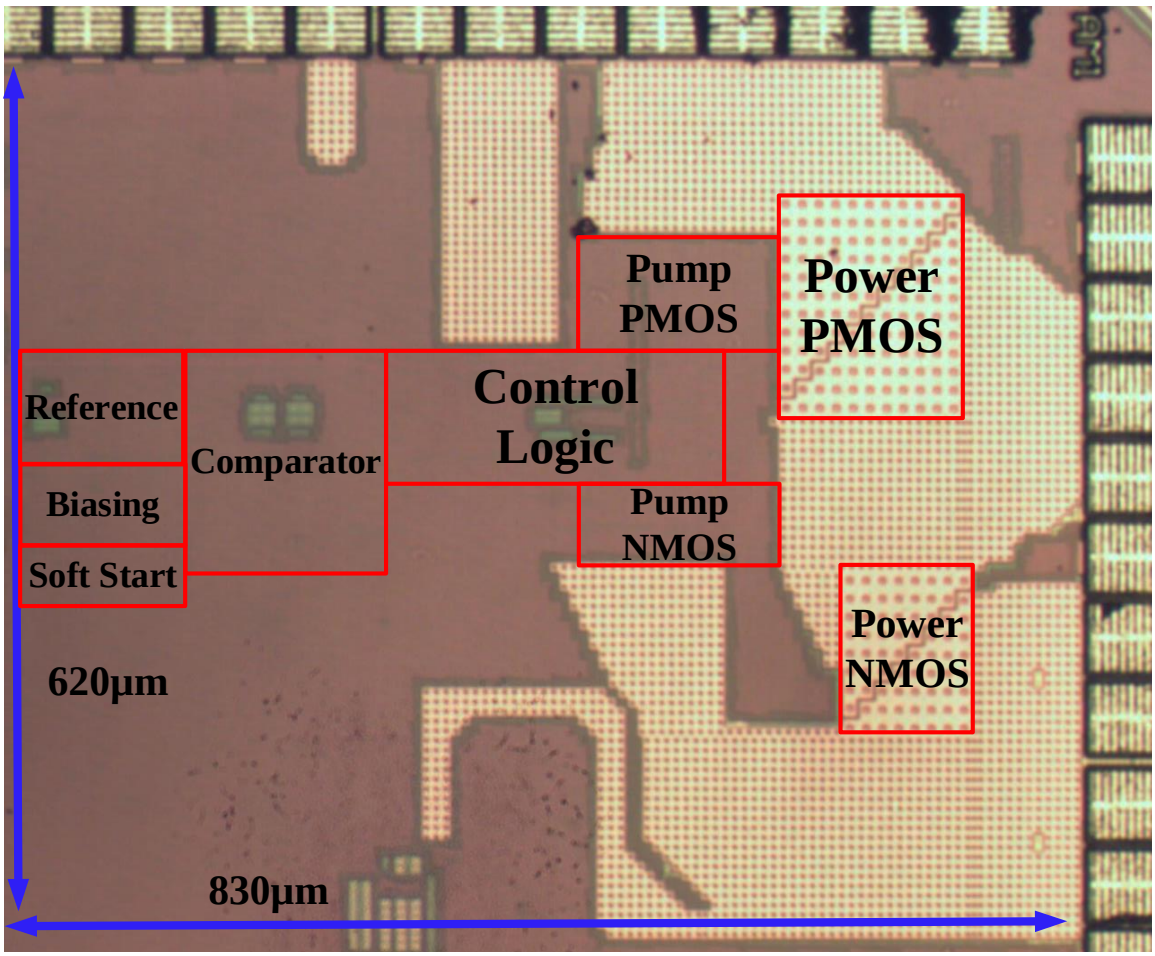

Figure 5.2. Chip Micrograph of the Proposed Buck Converter.

5.1.1 Steady-State Measurements

The buck converter is powered with an input of 2.5V and the nominal output voltage is 1.2V. The steady-state measurement results in CCM and DCM are illustrated in Figure 5.3 and Figure 5.4, respectively.

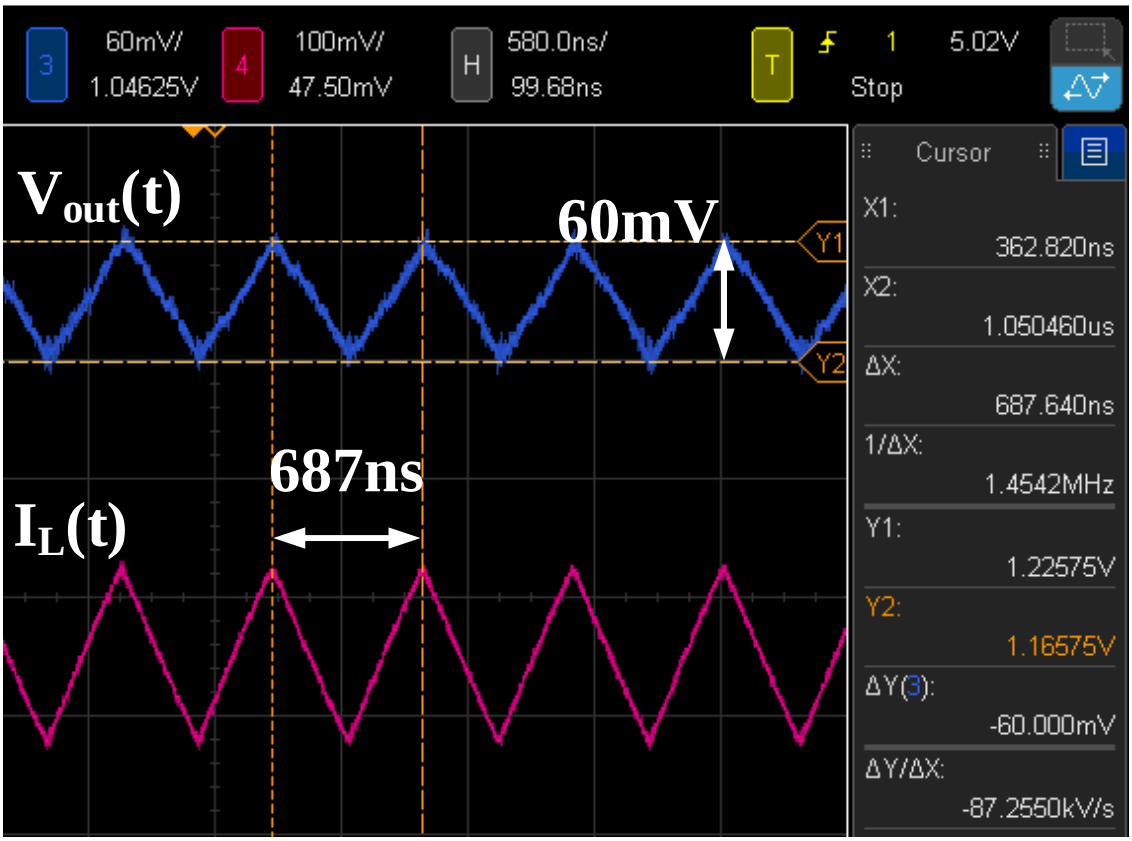

Figure 5.3. Steady State Waveforms (CCM).

Figure 5.3 shows the steady-state waveforms of the output voltage $V_{out}(t)$ and the inductor current $I_L(t)$ at the load current of 60mA. It has validated that the proposed converter can regulate properly in CCM. The output ripple is about $30mV_p$ whereas the switching frequency is about 1.45MHz. It also shows that the $V_{out}(t)$ is in phase

with the $I_L(t)$ because of the large ESR in the voltage-mode hysteretic converter as discussed in Section 4.1 and Section 4.6.2.

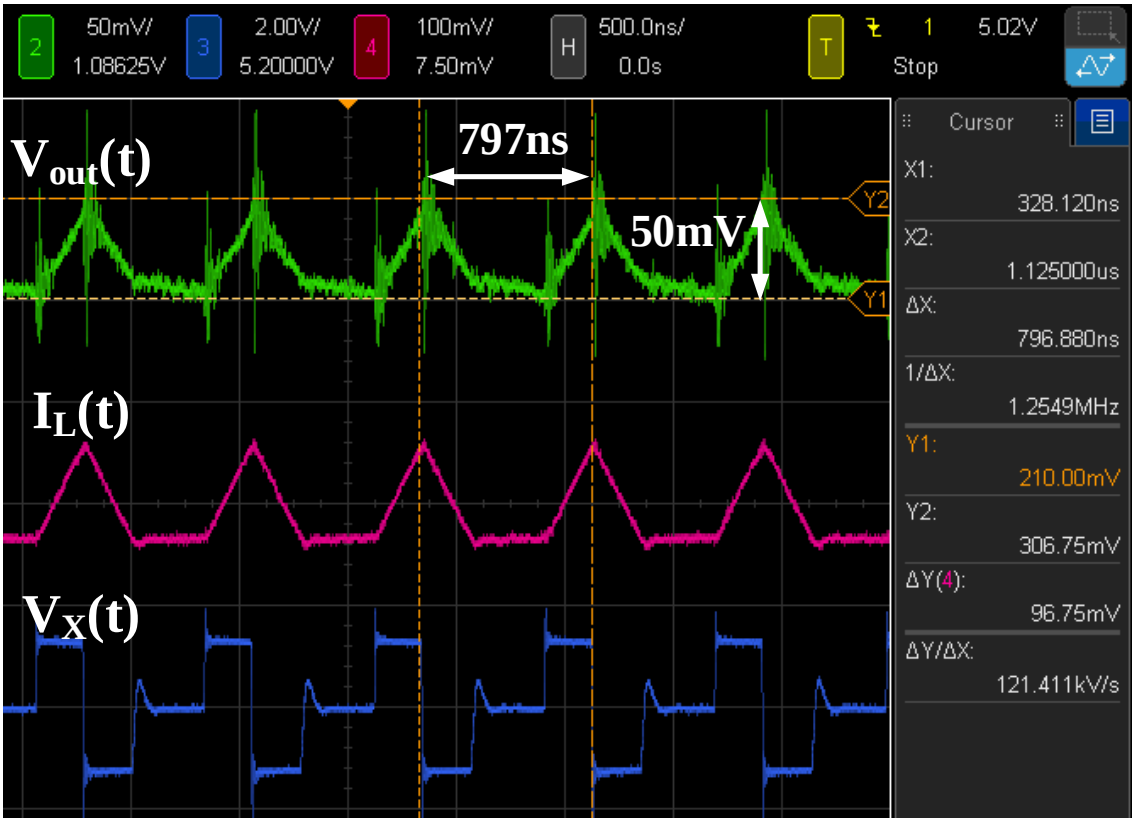

Figure 5.4. Steady State Waveforms (DCM).

Figure 5.4 shows the waveforms of the output voltage $V_{out}(t)$, the inductor current $I_L(t)$ and the switching node voltage $V_X(t)$ at the load current of 20mA. It has confirmed the design methodology of the DCM operation. During the light load condition, the reverse current can be detected and eliminated. The ring effect at the output node can be significantly reduced by applying the FSW control. As a result, the light load efficiency is improved.

The efficiency at different load currents is shown in Figure 5.5 with an input voltage

of 2.5V and an output voltage of 1.2 V. The output capacitor is 4.7μF and the output inductor is 4.7μH. The peak efficiency is about 93% at 60mA. Finally, due to the PFM control of hysteretic converters under DCM, the light load efficiency at 20mA is close to 90%.

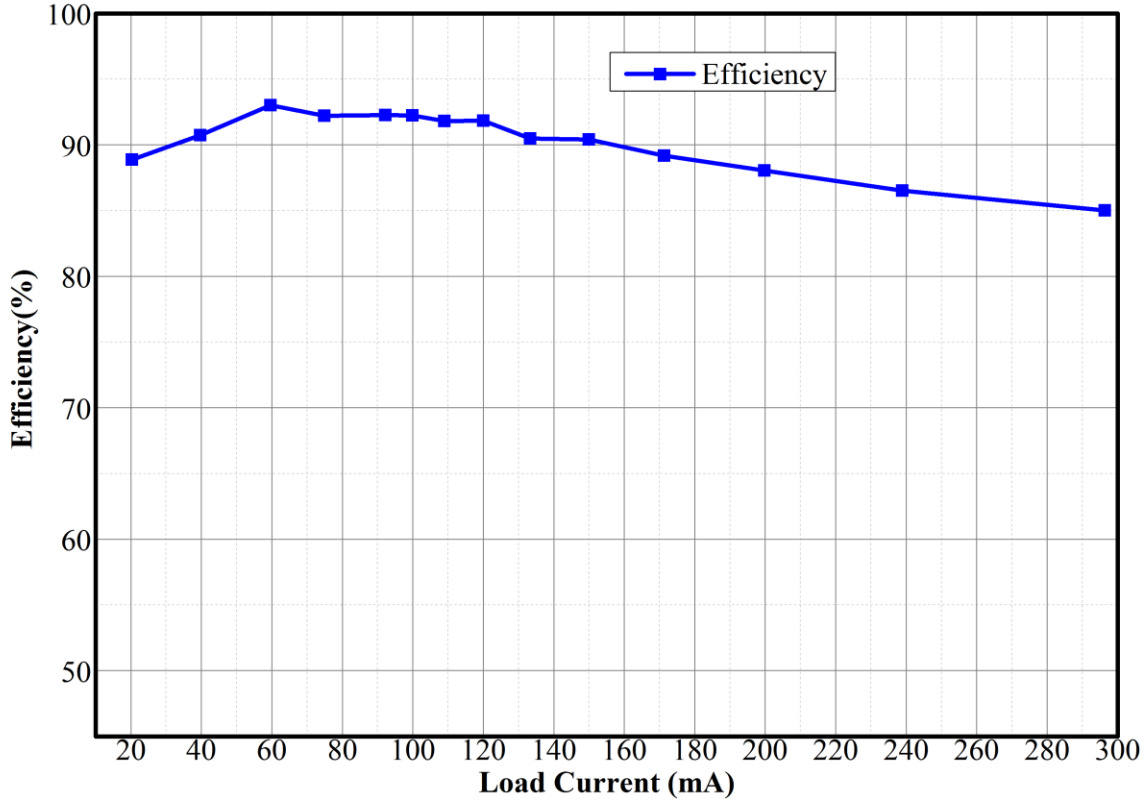

Figure 5.5. Power Efficiency at Different Load Currents.

5.1.2 Transient Response Measurement

The transient responses are measured with an input voltage of 2.5V and a dc output voltage of 1.2V. The output capacitor is 4.7μF and the output inductor is 4.7μH. The change of output load is realized through the circuit shown in Figure 5.6.

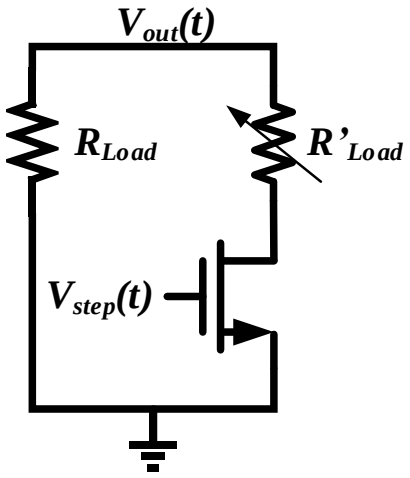

Figure 5.6. Output Load Resistance.

$V_{step}(t)$ is defined as the external load switch control signal. Initially, $V_{step}(t)$ remains low to turn off the MOS switch. When $V_{step}(t)$ goes to high, R_{Load} becomes in parallel with R'_{Load} and the MOS switch, causing the decrease of effective load resistance. This leads to a step-up load current change. When $V_{step}(t)$ goes back to low, the MOS switch turns off and the effective resistance is increased. As a result, a step-down load current change will be induced. Figure 5.7 depicts the measured transient waveforms for the external load switch control signal $V_{step}(t)$, the response of output voltage $V_{out}(t)$ and the change of inductor current $I_L(t)$ under a 60-to-300mA step-up current change and a 300-to-60mA step-down current change.

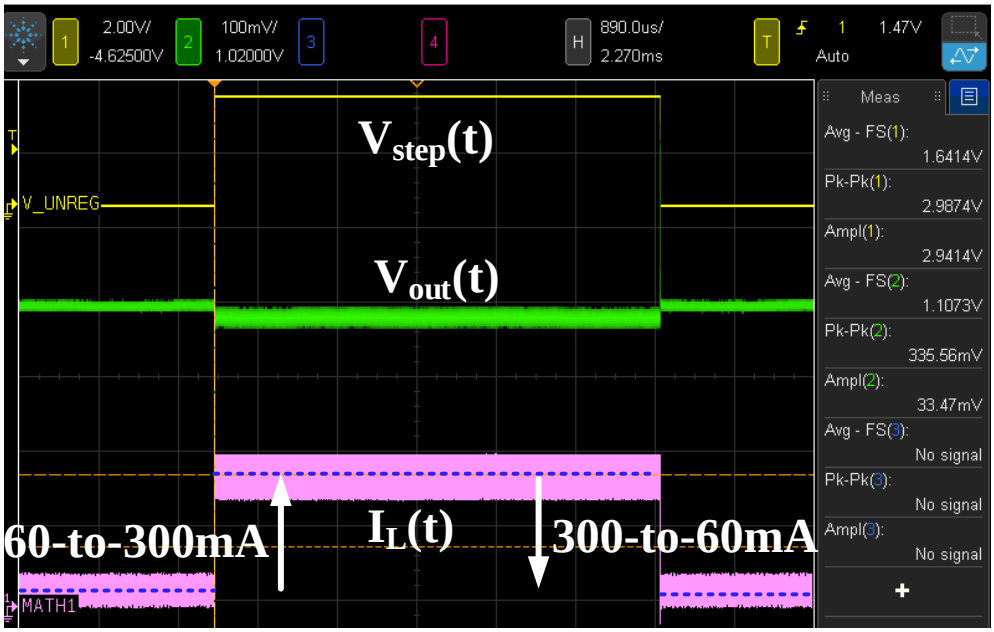

Figure 5.7. Transient Waveforms for the $V_{step}(t)$, $V_{out}(t)$ and $I_L(t)$.

For the conventional hysteretic buck converter without the $I_P(t)$, the undershoot and overshoot transient response for the 60-to-300mA and 300-to-60mA load current change is illustrated in Figure 5.8 and Figure 5.9, respectively. The undershoot/overshoot variation $\Delta V_{UN}/\Delta V_{OV}$ is about 128mV/127mV and the transient settling time t_{Settle} is about 1.31μs/1.185 μs.

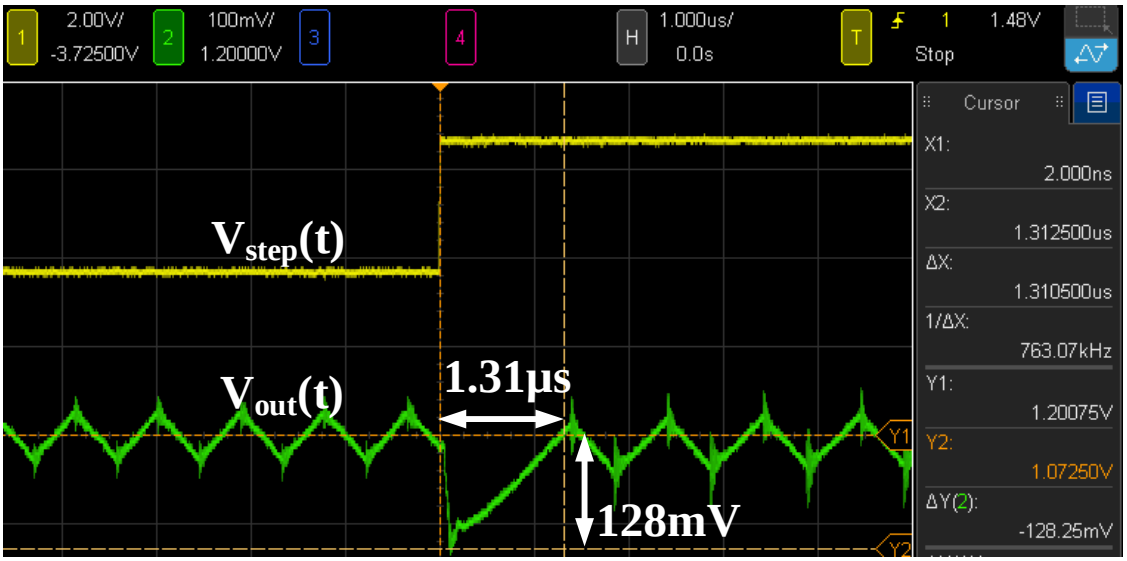

Figure 5.8. Undershoot Transient Response without $I_P(t)$ for 60-to-300mA Load Step.

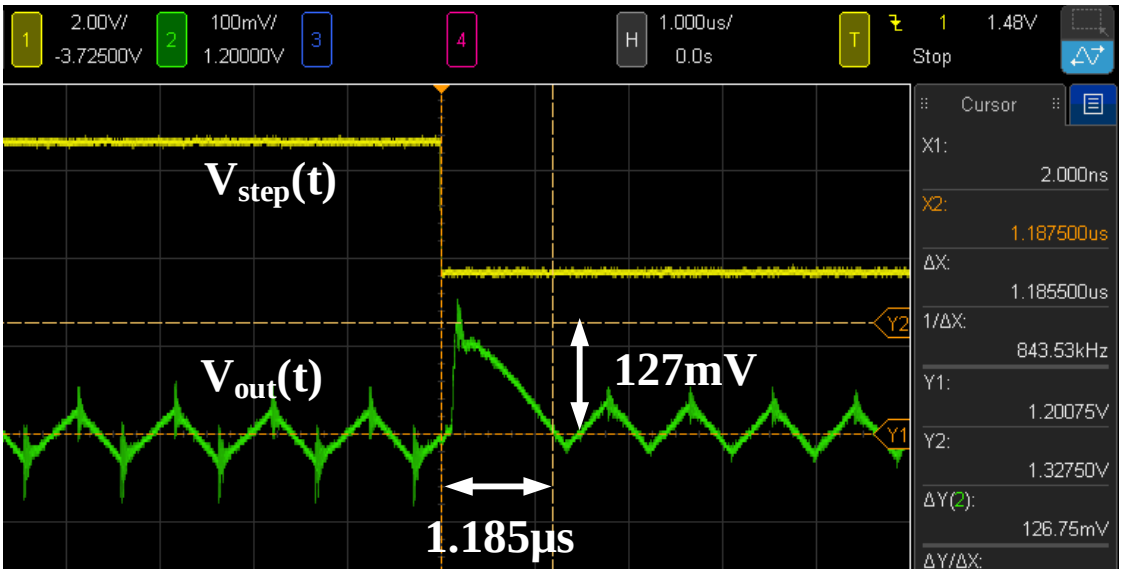

Figure 5.9. Overshoot Transient Response without $I_P(t)$ for 300-to-60mA Load Step.

For the APCA hysteretic buck converter with the PDTD $I_P(t)$, the

undershoot/overshoot transient response for the 60-to-300mA/300-to-60mA load current change is depicted in Figure 5.10 and Figure 5.11, respectively.

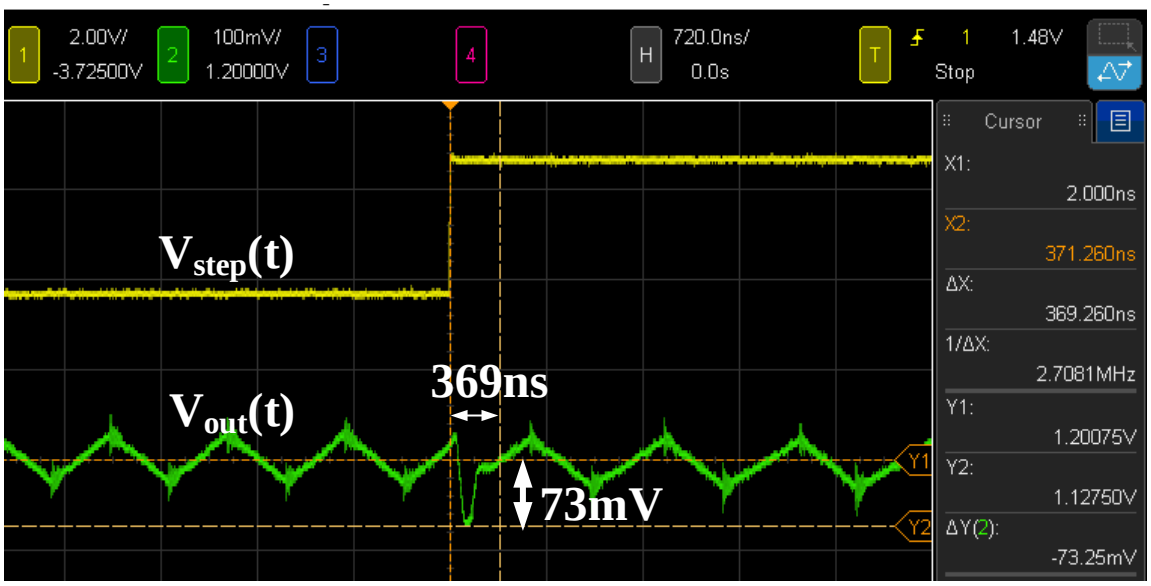

Figure 5.10. Undershoot Transient Response with the PDTD $I_P(t)$ for 60-to-300mA Load Step.

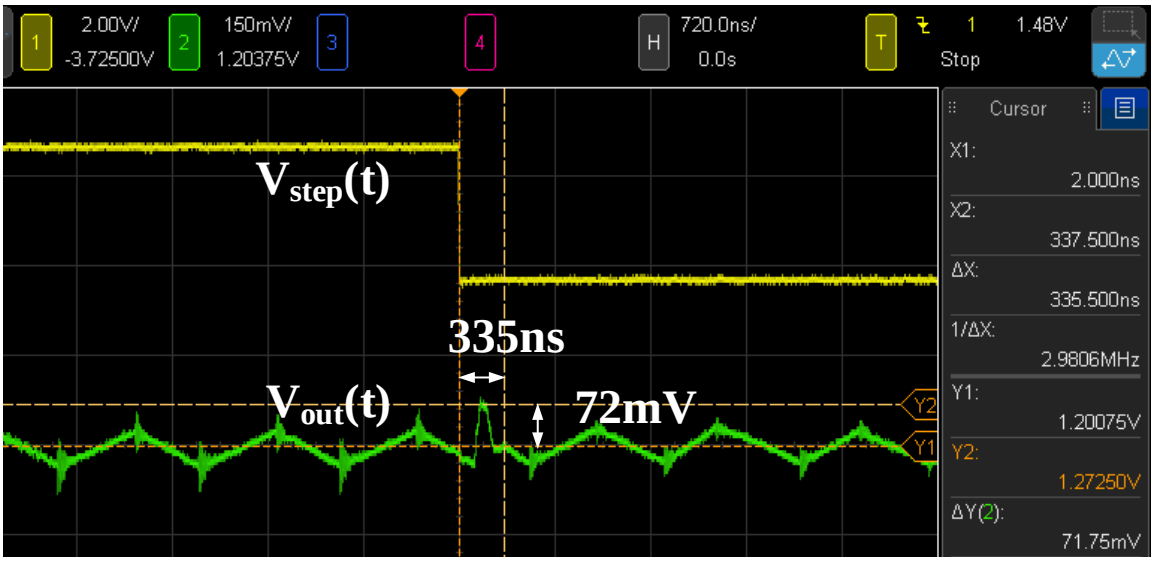

Figure 5.11. Overshoot Transient Response with the PDTD $I_P(t)$ for 300-to-60mA

Load Step.

Compared with the conventional counterpart, the undershoot/overshoot variation ΔV_{UN}/ ΔV_{OV} is reduced to 73mV/72mV and the transient settling time t_{Settle} is improved to 369ns/335ns. This has validated the effectiveness of the proposed PDTD scheme.

Table 3 shows performance comparison of the proposed converter with the reported works. It can be seen that the method has achieved faster transient response and comparable output ripple whilst keeping a reasonable high efficiency. Due to lack of the error amplifier in the design, the proposed topology has exhibited higher undershoot and overshoot voltage. Nevertheless, they are less than +/-10% of the nominal output voltage, which is acceptable in applications.

Table 3. Performance Comparison with the Reported Works.

Parameter	[20] ISSCC 2009	[50] JSSC 2011	[84] JSSC 2011	[33] TVLSI 2012	[11] JSSC 2015	[28] JSSC 2015	[34] ISSCC 2015	[6] JSSC 2015	[85] TVLSI 2016	This Work
Process (µm)	0.35	0.35	0.055	0.18	0.35	0.35	0.35	0.04	0.35	**0.04**
Input Voltage (V)	2.7-3.3	2.7-4.2	2.7-3.6	2.4-4.2	2.7-4.2	2.7-4.2	2.7-4.5	2.7-3.6	2.4-3.6	**1.2-2.5**
Output Voltage (V)	0.9-2.1	1	1.8/1.2	1.8	0.8-2.4	1.2	2	0.8-2.1	0.2-3.3	**0.6-2.1**
Load Current (mA)	50-500	<500	600	<500	<2000	18-700	NA	<900	600	**<450**
Output Ripple (mV_p)	NA	NA	30	NA	NA	NA	NA	<30	15	**30**
Inductor (µH)	2.2	1	4.7	4.7	1	2.2	4.7	4.7	4.7	**4.7**
Capacitor (µF)	4.4	4.7	4.7	4.7	4.7	10	10	4.7	10	**4.7**
Load Step (mA)	450	200	180	200	500	300	400	100	450	**240**
Tran. Time (L-H) (µs)	2.4	6	30	5	0.9	3	4.8	15	2.1	**0.369**
Undershoot (mV)	38	NA	100	40	25	48	35	30	>120	**73**
Tran. Time (H-L) (µs)	2.8	8	30	5	0.9	5	3	15	3.5	**0.335**
Overshoot (mV)	45	NA	100	40	35	30	38	30	>160	**72**
Peak Efficiency (%)	93	91	91	95	96	95.7	95.5	89	91	**93**
Freq. (MHz)	3	5	1	1	1.25	1	1	1	1	**1.45**

Conclusions and Future Works

5.2 Conclusions

In this project, the design of the voltage-mode hysteretic DC-DC buck converter with the PDTD control for the auxiliary pump current is proposed in conjunction with the theoretical analysis, circuit implementations and silicon prototype. The measurement results have shown that the proposed converter regulates properly in both CCM and DCM. With the proper freewheel switch control, the ring effect at the output node can be significantly reduced. In addition, other necessary function blocks such as: dead time control, over-current protection and soft start circuits are also implemented in the DC-DC converter in order to protect the overall system and maintain the power efficiency.

By applying the PDTD control scheme, the transient response of the voltage-mode hysteretic DC-DC buck converter can be further enhanced when compared with other reported topologies. Not only does it provide sufficient turning-on duration of the pump current to speed up the transient response, it also reduces the multiple undershoot/overshoot effect significantly. The time domain transient analysis, the simulation results and the measurement results have confirmed the effectiveness of the method. The performance comparison has demonstrated that the proposed work outperforms the reported state-of-art works on the transient performance metric

whilst displaying reduced multiple undershoot/overshoot effect, maintaining reasonable ripple voltage and power efficiency despite some increase of undershoot/overshoot voltage. Hence, the proposed PDTD pump current technique is very useful for realization of fast-transient voltage-mode hysteretic DC-DC buck converter.

5.3 Future Works

The future works of the project are summarized as follows:

The hysteretic converter with PDTD pump current proposed in this thesis has achieved fast-transient response. However, the voltage-mode hysteretic converter usually suffers from a relatively large output voltage ripple due to the large ESR of the output capacitor. This also produces a relatively large undershoot/overshoot variation when the load current change occurs. Future work will focus on the output voltage enhancement techniques to reduce the output voltage ripple as well as the undershoot/overshoot variation.

The proposed PDTD control scheme gives a sufficient turning-on duration of the $I_P(t)$ to accelerate the transient response. When the undershoot/overshoot recovers, the $I_P(t)$ will be turned off to save power. The $I_P(t)$ control scheme can be further explored to optimize the turning-on duration. In addition, the effectiveness of the proposed PDTD scheme should also be validated on other DC-DC buck converter topologies.

Finally, the switching frequency of the hysteretic DC-DC converter depends on many factors, such as output inductance and capacitance, ESR of the output capacitor, input and output voltage as so on. It will also be subject to the influence contributed by the hysteretic window and the circuit response delay. This uncertain switching frequency may induce wide EMI noise spectrum. Therefore, the constant frequency design techniques should be emphasized for low noise applications.

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