OPERATION AND PROTECTION OF DC SHIPBOARD POWER SYSTEM

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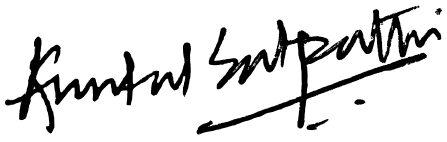
A thesis submitted to the Nanyang Technological University in partial fulfilment of the requirement for the degree of Doctor of Philosophy

2019

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.



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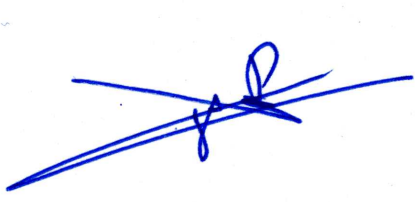
Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.



June 3, 2019

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Assoc. Prof. Josep Pou

Authorship Attribution Statement

This thesis contains material from **12** papers published in the following peer-reviewed journals and from papers accepted at conferences in which I am listed as an author.

- **Chapter 2** is published as:

  (i) **K. Satpathi**[1], A. Ukil[2], and J. Pou[3], "Short-circuit protection in DC electric ship propulsion system: Review of existing technologies and future research trends," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 272-291, Mar. 2018.

  The contributions of the co-authors are as follows:

  – Dr. A. Ukil[2] provided the initial project direction and edited the manuscript drafts.

  – I[1] prepared the manuscript drafts and carried out the literature review on fault detection, isolation and reconfiguration of dc shipboard power systems.

  – Assoc. Prof. J. Pou[3] suggested to include a section on proposing solutions and future works. He also helped in reviewing the manuscript for final submission.

- **Chapter 3** is published as:

  (i) **K. Satpathi**[1], A. Ukil[2], J. Pou[3] and M. A. Zagrodnik[4], "Design, analysis and comparison of automatic flux regulator with automatic voltage regulator based generation system for DC marine vessels," *IEEE Trans. Transport. Electrific.* vol. 4, no. 3, pp. 694-706, Sep. 2018.

  The contributions of the co-authors are as follows:

- I[1] developed the theory on automatic flux regulator for controlling the wound-rotor synchronous generator in dc marine vessels. I validated the findings with real-time simulation models at Electrical Power Systems Integration Lab@NTU.
- Dr. A. Ukil[2] provided initial project direction and suggested to include the comparison of automatic flux regulator with traditional automatic voltage regulator based control.
- Mr. M. A Zagrodnik[4] analyzed the performance of automatic flux regulator for variable speed generation systems.
- I[1] prepared the manuscript drafts which was initially reviewed by Dr. A. Ukil[2].
- Assoc. Prof. J. Pou[3] suggested to include case studies on marine applications. He helped me in analyzing the results, gave suggestions on organization of the manuscript and reviewed it for final submission.

(ii) **K. Satpathi**[1], N. Thukral[2], A. Ukil[3] and M. A. Zagrodnik[4], "Flux estimation based DC bus voltage control in marine DC power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016.

The contributions of the co-authors are as follows:

- I[1] developed the initial idea on controlling the synchronous generator which is interfaced with the voltage-source converter
- Mr. M. A. Zagrodnik[4] assisted in deriving the control system in rotor-reference system.
- I[1] prepared the manuscript drafts which were reviewed by Dr. A. Ukil[3].
- Ms. N. Thukral[2] helped me in developing the real-time simulation models and analyzing the results.
- Dr. A. Ukil[3] supervised the process and reviewed the manuscript for final submission.

- **Chapter 4** is published as:

(i) **K. Satpathi**[1], V. M. Balijepalli[2], and A. Ukil[3], "Modeling and real-time scheduling of DC platform supply vessel for fuel efficient operation," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 3, pp. 762-778, Sep. 2017.

The contributions of the co-authors are as follows:

- I[1] discussed the initial idea on operation of dc platform supply vessel with Dr. V. M. Balijepalli[2].
- Dr. V. M. Balijepalli[2] developed the generation scheduling algorithms using dc optimal power flow algorithms and the concept of minimizing specific fuel oil consumption at sub-optimal points.
- I[1] developed the real-time simulation models with integrated controllers of the full-fledged dc platform supply vessel at Electrical Power System Integration Lab@NTU.
- I[1] wrote the manuscript drafts which was initially reviewed by Dr. V. M. Balijepalli[2] and Dr. A. Ukil[3].
- Dr. A. Ukil[3] analyzed the results on minimization of fuel consumption and reviewed the manuscript for final submission.

(ii) **K. Satpathi**[1], A. Ukil[2], N. Thukral[3] and M. A. Zagrodnik[4], "Modeling of DC shipboard power system," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

The contributions of the co-authors are as follows:

- I[1] discussed the idea on the modelling and control of the complete dc shipboard power systems with Dr. A. Ukil[2] and Mr. M. A. Zagrodnik[4].
- Ms. N. Thukral[3] helped me with the development of real-time simulation model.
- I[1] prepared the manuscript drafts which was initially reviewed by Ms. N. Thukral[3] and Dr. A. Ukil[2].
- Mr. M. A. Zagrodnik[4] supervised on the real-time simulation system.
- Dr. A. Ukil[2] supervised on the modelling and control of the dc shipboard power systems and reviewed the manuscript for final submission.

- **Chapter 5** is published as:

  (i) **K. Satpathi**[1], A. Ukil[2], S. S. Nag[3], J. Pou[4] and M. A. Zagrodnik[5], "DC marine power system: Transient behaviour and fault management aspects," *IEEE Trans. Ind. Informat.*, vol. 15, no. 4, pp. 1911-1925, Apr. 2019.

  The contributions of the co-authors are as follows:

  – I[1] developed the concept of current-only directional protection for dc SPS using short-time Fourier transform and discussed with Dr. A. Ukil[2] and Assoc. Prof. J. Pou[4].

  – Dr. A. Ukil[2] gave suggestions on the current-only directional element and supervised the entire process.

  – Dr. S. S. Nag[3] helped me in developing the real-time simulation system and analyzing the results.

  – I[1] prepared the manuscript drafts which were initially reviewed by Assoc. Prof. J. Pou[4].

  – Assoc. Prof. J. Pou[4] suggested me to include the study on marine missions and their influence on the developed protection algorithms.

  – Mr. M. A. Zagrodnik[5] helped in studying the marine missions.

  – Assoc. Prof. J. Pou[4] gave suggestions with the organization of the manuscript and reviewed it for final submission.

  (ii) **K. Satpathi**[1], Y.M. Yeap[2], A. Ukil[3], and N. Geddada[4], "Short-time Fourier transform based transient analysis of VSC interfaced point-to-point DC system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 4080-4091, May 2018.

  The contributions of the co-authors are as follows:

  – I[1], Dr. Y. M. Yeap[2] and Dr. A. Ukil[3] developed the idea of detecting the fault condition using short-time Fourier transform.

  – I[1] validated the findings by detecting magnitude at zero-crossing frequency bins with the simulation models.

  – Dr. N. Geddada[4] developed the hardware test-bed for validation of short-time Fourier transform based dc protection. (These results are not included in this thesis).

- Dr. Y. M. Yeap[2] validated the short-time Fourier transform based protection with experimental test setup. (These results are not included in this thesis).
- I[1] prepared the manuscript drafts which were initially reviewed by Dr. Y. M. Yeap[2] and Dr. N. Geddada[4].
- Dr. A. Ukil[3] gave suggestions on the organization of the manuscript and reviewed it for final submission.

(iii) D. Francis[1], Q. Zhengting[2], **K. Satpathi**[3], N. Thukral[4] and A. Ukil[5], "Suitability of Rogowski coil for DC shipboard protection," in *Proc. IEEE TENCON Conf.*, Singapore, Nov. 2016.

The contributions of the co-authors are as follows:

- I[3] developed the idea of using Rogowski Coil for fault detection in dc shipboard power system.
- Ms. D. Francis[1] developed the Rogowski coil model to measure the transient dc current.
- Mr. Q. Zhengting[2] developed the integrator of Rogowski coil.
- I[1] developed the transient dc circuit and prepared the manuscript.
- Ms. N. Thukral[4] analyzed the fault results from the Rogowski coil.
- Dr. A. Ukil[5] reviewed the manuscript and supervised the whole process.

(iv) **K. Satpathi**[1] and A. Ukil[2], "Protection of MVDC shipboard power system using Rogowski coil," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

The contributions of the co-authors are as follows:

- I[1] developed the real-time simulation model for protection of dc shipboard power systems.
- I[1] prepared the manuscript drafts.
- Dr. A. Ukil[2] reviewed the protection system of dc shipboard power systems.
- Dr. A. Ukil[2] gave suggestions on the organization of the manuscript and reviewed it for the final submission.

(v) **K. Satpathi**[1] and A. Ukil[2], "Protection strategies for LVDC distribution system," in *Proc. IEEE PowerTech Conf.*, Eindhoven, Netherlands, Jun. 2015.

The contributions of the co-authors are as follows:

- Dr. A. Ukil[2] suggested me to study transient analysis for LVDC distribution system.
- I[1] did the transient analysis of LVDC distribution system.
- I[1] prepared the manuscript drafts. Dr. A. Ukil[2] gave suggestions on the organization of the manuscript and reviewed it for final submission.

- **Chapter 6** is published as:

(i) **K. Satpathi**[1], A. Ukil[2], S. S. Nag[3], J. Pou[4] and M. A. Zagrodnik[5], "DC marine power system: Transient behaviour and fault management aspects," *IEEE Trans. Ind. Informat.*, vol. 15, no. 4, pp. 1911-1925, Apr. 2019.

The contributions of the co-authors are as follows:

- I[1] developed the concept of current-only directional protection for dc SPS using short-time Fourier transform and discussed with Dr. A. Ukil[2] and Assoc. Prof. J. Pou[4].
- Dr. A. Ukil[2] gave suggestions on the current-only directional element and supervised the entire process.
- Dr. S. S. Nag[3] helped me in developing the real-time simulation system and analyzing the results.
- I[1] prepared the manuscript drafts which were initially reviewed by Assoc. Prof. J. Pou[4].
- Assoc. Prof. J. Pou[4] suggested me to include the study on marine missions and their influence on the developed protection algorithms.
- Mr. M. A. Zagrodnik[5] helped in studying the marine missions.
- Assoc. Prof. J. Pou[4] gave suggestions with the organization of the manuscript and reviewed it for final submission.

(ii) **K. Satpathi**[1], A. Ukil[2], S. S. Nag[3], J. Pou[4] and M. A. Zagrodnik[5], "Comparison of current-only directional protection in AC and DC power systems," in *Proc. Innovative Smart Grid Technologies (ISGT)*, Singapore, 2018.

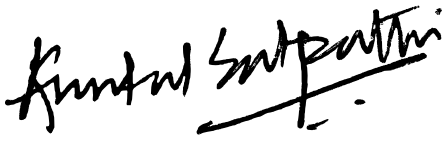
The contributions of the co-authors are as follows:

- I[1] developed the idea of comparing directional protection in ac and dc power systems.
- Dr. S. S. Nag[3] helped me in developing the real-time simulation system and analyzing the results.
- Dr. A. Ukil[2] gave suggestions on the current-only directional protection in ac power systems.
- I[1] prepared the manuscript drafts which were initially reviewed by Dr. A. Ukil[2].
- Assoc. Prof. J. Pou[4] gave suggestions with the comparison and organization of the manuscript for final submission.
- Mr. M. A. Zagrodnik[5] supervised the modelling of dc shipboard power system and reviewing the manuscript.

(iii) **K. Satpathi**[1], N. Thukral[2], A. Ukil[3] and M. A. Zagrodnik[4], "Directional protection scheme for MVDC shipboard power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016.

The contributions of the co-authors are as follows:

- I[1] developed the idea of directional protection for dc shipboard power system.
- Dr. A. Ukil[3] supervised the modelling of directional protection algorithm.
- Ms. N. Thukral[2] developed the real-time simulation model and assisted in analyzing the results.
- I[1] prepared the manuscript drafts.
- Dr. A. Ukil[3] reviewed the manuscripts for the final submission.
- Mr. M. A. Zagrodnik[4] supervised in the modelling of dc SPS and organization of the manuscript.



June 3, 2019

Date

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Acknowledgements

I would like to offer my sincerest gratitude to my advisor, Prof. Josep Pou. Thank you for the enriching discussions and constant guidance during my doctoral studies. Your words of encouragement have helped me sail through this journey with great motivation. I would like to offer my sincerest gratitude to my former advisor, Prof. Abhisek Ukil. Thank you for providing me with the wonderful opportunity to pursue research in the area of dc power system protection. Many thanks to you for always believing in me, and for your continuous support, patience, and motivation during my formative years.

I take this opportunity to extend special thanks to my program manager, Mr. Michael Adam Zagrodnik. Thank you for introducing to me insights of the marine industry. The learning from our late night technical discussions are fortunes that I will take back from this journey. Thank you for being my mentor and such a good friend. I express my sincere gratitude to Prof. Ali Iftekhar Maswood and Prof. Amit Gupta, the members of my thesis advisory committee. I am also thankful to the course coordinators during my teaching assistant duties for giving me an opportunity to conduct courses for the undergraduate students. This immensely helped to boost my confidence.

I am grateful to Dr. Soumya Shubhra Nag for all the enriching discussions on power electronics and on the dc grids in general. I sincerely thank Dr. Suvajit Mukherjee for his help and guidance in the research. I would like to thank my colleagues– Nishant, Dr. Murthy, Dr. Gabriel, Yicheng, Shicong, Deen, Sampath, Raghav, Tariq, Dr. Sukanta, Dr. Suman, Yeap, Dr. Nagesh, Ujjal and Navpreet for the conducive working environment and for being a great support. My sincere thanks go to Dr. Souvik Dasgupta, Dr. Sivakumar Nadarajan, Dr. Meng Yeong Lee, Ms Ruchika, Mr. Lim, Mr. Yap and Mr. Tarshan from Rolls-Royce@NTU Corp Lab for creating healthy and friendly working premises.

My stay in Singapore would not have been beautiful without the friendship of some wonderful people. Thank you Ankit and Bhrigu for your support and also for the memorable late night discussions. Special thanks go to Tanaya for being the constant source of encourage-

ment, love, and support. Thank you Shafquat, Sonia, Bhumika, Noopur, Mayank, Shreyashi, Naveen and Kalpesh for your friendship. A special thanks to my childhood friends, Narendra and Anjan, who encouraged me to pursue higher studies. I would also like to extend sincere regards to my colleagues from my previously associated organization, Jindal Power Ltd.– Mr. Ashish Gera, Mr. Sandeep Sahu, Mr. Tapas Sarangi and Mr. Manas Mahesh Das for being great mentors.

This thesis would not have been possible without the generous support from the Nanyang Technological University, Singapore. I would like to acknowledge and appreciate the financial, academic and technical support from the Rolls-Royce@NTU Corporate Lab[1]. I would like to take this opportunity to thank Mr. Mark Husband from Rolls-Royce, UK and all the anonymous reviewers around the world for providing invaluable comments to improve my journal manuscripts and conference proceedings.

Finally, I would like to thank my parents for their unconditional love and blessings. I dedicate this thesis to my parents, Mrs. Sarbajaya Satpathi and Mr. Asim Satpathi. Thank you, *Maa*, for all your sacrifices and for instilling in me a *never give up* attitude. I promise to deliver justice to your faith in me.

[1]This work is conducted within the Rolls-Royce@NTU Corporate Lab, supported by the National Research Foundation (NRF) Singapore, under the Corp Lab@University Scheme. The grant number for the project is RR-NTU-NRF: E-RT1.2.

Contents

Abstract

Marine vessels integrated with electrical propulsion have conventionally been based on fixed-voltage, fixed-frequency (50/60 Hz) ac generation and distribution system. In recent years, dc power system in the marine vessels has been proposed primarily to take advantage of the fuel-efficient operation, which is enabled through the integration of the variable frequency diesel generators. Such dc shipboard power system (SPS) also enables interconnection of the alternative power generation and energy storage technologies, which helps in peak shaving of the generators in the event of wide load variation. In spite of the advantages, one of the impediments to the widespread adoption of dc SPS is the lack of comprehensive short-circuit fault management strategies. These vessels are dominated by a significant number of active loads and a finite number of dc generation sources. As a result, the network configuration is expected to be dynamically altered to fulfil the required generation and load demands to cater for the desired marine mission. Such varying network configurations make the transient responses significantly different from the conventional ac grids and the prospective dc grids and hence making the fault management strategies more challenging. Thus, the modeling and control of dc generation sources, loading scenarios, and system operation become important aspects to effectively understand and analyze transient responses. The aim of this thesis is to address the modeling and control aspects of dc shipboard power systems and devising protection algorithms. This thesis considers the platform supply vessel (PSV) as the target dc marine vessel and covers detailed investigation on the challenges in the modeling and control and the solutions of the dc generation and load systems. PSV is taken as an example of the marine vessel due to its complex operating scenarios and wider applicability in the marine industry. Voltage source converter (VSC) based dc generation system is chosen owing to its improved operational benefits. The real-time transient framework and operation of the dc PSV are discussed along with the possible contingency scenarios, such as the outage of the generation systems, abrupt load changes, effect of the energy storage systems and so on. The disadvantage of the dc system is the lack of zero current crossing which worsens

the problem of arc quenching. In dc power system, the converters will be used as interfaces between the generators and the marine loads. During the fault, the dc-link capacitor will discharge rapidly, releasing high current. This capacitive discharge current represents a serious challenge in fault detection and protection as the current profile depends on the circuit parameters. Moreover, the time required to detect the dc fault current is very low. It is thus required to devise suitable protection algorithm for fault detection and isolation. Proper operation of the dc SPS calls for high fidelity control and modeling of the system components.

After the modeling and operation, this thesis also covers systematic transient studies to devise the short-circuit fault detection technique for the dc PSV. The transient response of the VSC-based dc generation system in the dc PSV is generally characterized by rapidly rising capacitive discharge current which is different from the ac counterpart. The limitations of the traditional time-domain based fault detection techniques for the varying network conditions of the dc PSV are also discussed. The rapidly rising fault current is expected to have high-frequency components which could be an effective indicator of the transient condition. With this regard, this thesis also covers a short-time Fourier transform (STFT) based quantitative analysis of the high-frequency components in the dc fault currents. Detailed operating principles, factors affecting the STFT operation and the sensitivity analysis are also discussed. For the enhanced selectivity in the dc PSV, a novel directional protection is also proposed which uses directional zonal interlocking as a directional element and STFT as fault detector. The efficacy of this proposed directional protection is also presented which is verified against a range of fault impedances initiated at the generator terminals, load terminals, lines and buses of the dc PSV. The thesis is concluded by discussing the future work and recommendations on the fault-tolerant architectures to external short-circuit faults.

Keywords: DC Power System, DC Power System Protection, DC Fault Analysis, DC Voltage Control, DC Shipboard Power System, Directional Protection, Platform Supply Vessel, Short-Time Fourier Transform.

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Acronyms

AC	Alternating Current
AFE	Active Front-End
AFR	Automatic Flux Regulator
AVR	Automatic Voltage Regulator
BESS	Battery Energy Storage System
CB	Circuit Breaker
CPL	Constant Power Loads
CSC	Current Source Converter
DC	Direct Current
DE	Diesel Engine
DG	Diesel Generator
DP	Dynamic Positioning
DZI	Directional Zonal Element
ESRDC	Electric Ship Research and Development Consortium
ESS	Energy Storage System
GT	Gas Turbine
HIL	Hardware-in-Loop
HVDC	High Voltage Direct Current
IED	Intelligent Electronic Device

IEEE	Institute of Electrical and Electronics Engineers
IG	Induction Generator
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
IPS	Integrated Power System
LVDC	Low Voltage Direct Current
MMC	Modular Multilevel Converter
MP	Main Propulsion
MTDC	Multi Terminal DC
MVDC	Medium Voltage Direct Current
OC	Over-Current
PLL	Phase Locked Loop
PMSG	Permanent Magnet Synchronous Generator
PSV	Platform Supply Vessel
PV	Photo-Voltaic
RRF	Rotor Reference Frame
RT	Retractable Thruster
RC	Rogowski Coil
SCR	Silicon Controlled Rectifier
SFOC	Specific Fuel Oil Consumption
SFRF	Stator Flux Reference Frame
SOC	State-of-Charge
SPS	Shipboard Power System
SSCB	Solid-State Circuit Breaker
STFT	Short-Time Fourier Transform
TT	Tunnel Thruster
VSC	Voltage-Source Converter
WT	Wavelet Transform
WRSG	Wound Rotor Synchronous Generator
ZCT	Zero-Crossing Time

Notations

e_T/E_T	Internal voltage of WRSG
v_T/V_T	Terminal voltage of WRSG
e_F/E_F	Field Excitation Voltage of WRSG
v_T^{SP}	Terminal voltage setpoint of WRSG
v_{dc}	DC-link voltage of AFE converter
v_{dc}^{SP}	DC-link voltage setpoint of AFE converter
X_s	Synchronous impedance
f	Frequency
C	DC-link capacitor
C_f	Filter Capacitance of the LC filter
f_{sw}	Switching frequency of the AFE rectifier
f_c	Cut-off frequency of LC Filter
f_L	Line frequency (of WRSG)
i_o	Output dc current of AFE rectifier
θ_p	Reference angle generated by PLL
i_{ds}^p, i_{qs}^p	d-q current of WRSG in PLL reference frame
v_{ds}^p, v_{qs}^p	d-q voltage of WRSG in PLL reference frame
i_{ds}^r, i_{qs}^r	d-q current of WRSG in RRF
v_{ds}^r, v_{qs}^r	d-q voltage of WRSG in RRF
θ_s	Reference angle at SFRF

i_{Ms}, i_{Ts}	M-T current of WRSG in SFRF
v_{Ms}, v_{Ts}	M-T voltage of WRSG in SFRF
δI_p	Peak ripple current of WRSG current
K_{exc}	Gain of Type-ST Exciter
L_s	WRSG stator inductance
L_f	Filter inductance of the LC filter
p	Number of poles of WRSG
R_s	WRSG stator resistance
R'_{fd}	Field winding resistance of WRSG (referred to stator)
R_d	Damping resistance of LC filter
v_{dc}	Output dc-link voltage
X_s/L_s	Synchronous Impedance/Inductance
X_{md}/X_{mq}	WRSG d-q axis reactance
X_{lf}	WRSG field circuit reactance
λ^r_{ds}, λ^r_{qs}	WRSG Flux linkage in RRF
λ_{Ms}, λ_{Ts}	WRSG Flux linkage in M-T axis
ψ_{Ms}, ψ_{Ts}	Flux linkage per second of WRSG in M-T axis
τ'_{do}	WRSG open circuit time constant
τ_{exc}	Time constant of Type-ST Exciter
ω_b, ω_r	Base speed and rotor speed of WRSG
P_{mech}	Mechanical power at diesel engine shaft
P_{load}	Load demand
P_G	Power produced by generator
$\mathscr{P}^{DG}/\mathscr{P}^{ESS}$	Power output of DG/ESS
$\mathbb{P}_{Gen}$	Total installed power in dc PSV
$\mathbb{L}^{CL}$, $\mathbb{L}^{DP}$	Constant/DP load
$\mathbb{L}^{HL}\mathbb{L}^{misc}$	Hotel loads/miscellaneous loads
u_F	Fuel injection input signal
k_{pm}	Fuel injection system gain
τ_{pm}	Fuel injection time constant
t_d	Dead-time of diesel engine
J	Diesel engine rotor inertia moment
ω_G	Diesel engine and generator angular speed

k_{loss}	Diesel engine rotational loss
T_G	Torque produced by the generator
p	Number of poles of generator
T_T	Thrust developed by the thrusters
τ_T	Torque developed by the thrusters
d_P	Propeller diameter
ω_P	Speed of the propeller
P_T	Power developed by the thrusters
C_T	Thrust co-efficient
C_τ	Torque coefficient
$\mathcal{S}_\mathcal{D}$	Short-time Fourier Transform in discrete domain
f_u	Update frequency or zero-crossing frequency bin
$\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}$	Magnitude of $\mathcal{S}_\mathcal{D}$ at f_u
RO_{IED_n}	Regenerative operation detected at n^{th} IED
RF_{IED_n}	Fault in reverse direction detected at n^{th} IED
NO_{IED_n}	Normal operation detected at n^{th} IED
FF_{IED_n}	Fault in forward direction detected at n^{th} IED
$\mathbb{D}$	Directional Element
$\mathbb{D}_{dc}$	Directional Element in dc power system
$\mathbb{D}_{ac}$	Directional Element in ac power system

Chapter 1

Introduction

1.1 Background and Motivation

The conventional power system in marine vessels with electric propulsion is based on fixed-voltage and fixed-frequency (50/60 Hz) ac generation and distribution system. With the stringent requirement of emission control as per the guidelines issued by the International Maritime Organization (IMO), it is pertinent to develop fuel efficient marine vessels hence limiting the exhaust gas emissions [1]. In conventional ac marine vessels, fuel efficiency is optimized by starting and stopping the interfaced diesel engines depending on the load conditions. Shaft electric machines have also been proposed to minimize the fuel consumption to a certain extent [2]. However in recent years, paradigm shift in the energy conversion technologies of the emerging marine vessels have witnessed a transition from ac to dc power systems. This transition to dc-based alternative power generation and distribution topologies is primarily strengthened by the fuel efficient operation of the interfaced diesel generator (DG) running at the optimized speed [3–9]. It is further supported by the availability of efficient ac/dc and dc/dc power electronic conversion devices. Such dc shipboard power systems (SPSs) could play a pivotal role in ensuring continuity of the electrical supply for vessels [10], which carry out critical marine missions such as dynamic positioning (DP) [11], ice-breaking [12], supporting the offshore supply vessels, etc. The advantages offered by the dc SPS have motivated the university and industrial research centers to focus on its research and development. One of the prominent research unit is USA based Electric Ship Research and Development Consortium (ESRDC) which comprises of eight university labs dedicated

to the development of feasibility of dc ships. Many industries such as ABB, Siemens, Rolls-Royce have started investing resources to develop the dc SPS. One of the major achievement in this area is the deployment of battery operated *MF Ampere* [13] passenger liner and DG based *ABB Dina Star* [9].

In spite of the advantages and opportunities, commercial deployment of dc SPS for longer voyages and marine missions (such as ice-breaking, DP, etc.) is difficult and complicated. One of the prime constraints encountered in the design of dc SPS is lack of standards and guidelines on implementation of comprehensive short-circuit fault management techniques within such systems. Short-circuit fault management of dc SPS essentially includes fault detection, fault isolation, and post-fault reconfiguration. Fault detection and isolation are required to identify and segregate the faulty part from the healthy section of the dc SPS. Reconfiguration of dc SPS is required to modify the system architecture to ensure that the power flow to critical loads is not unnecessarily interrupted.

Installed generation capacity in SPS is generally less than the number of connected loads. This is because specific set of loads are activated for a particular marine mission. As a result, magnitude of short-circuit fault current is dependent on the system configuration. In such condition, fault detection algorithms should be developed after systematic transient analysis of the complete dc SPS. Moreover, lack of set guidelines and standard design rules for such systems poses further difficulty in the system analysis. With this approach, modeling and control of all the system components and operation of dc SPS become important aspects before developing the protection algorithm. Fuel efficient operation of dc SPS should also be taken into account as this is the prime objective of choosing dc SPS over ac SPS. Analogous to land based multi-terminal dc (MTDC) systems, dc marine vessels are also envisaged to have multi-layer control system [14]. Primary controller regulates the dc bus voltage [15] and active power [16] along with suitable protection and fault management strategies [17]. Secondary control system comprises of load forecasting and power flow algorithms, which will be executed for a given state and requirements of the marine missions [18, 19]. The secondary control system also helps in optimizing power flow and load-shedding techniques to minimize the risk of blackout conditions.

Determining the protection system of SPS is further dependent on the class and nature of target marine vessel. Protection malfunction in the battery operated dc ferries covering short

distances [13] would result in loss of power and is expected to be tolerated as it would result in stalling of the vessel, and delay in operation with no major financial repercussions. Thus, low-complexity, low-cost fuse-based protection is expected to be suitable for such vessels. Conversely, continuity of power is of utmost importance for shipboard systems such as PSVs undertaking complex marine missions such as DP or supporting offshore supply vessels [11]. For such applications, delay in restoration of generation system due to inefficient protection algorithms resulting in inadvertent system blackout, might result in loss of position of the PSV. Further, for the PSV involved in critical activities such as oil exploration, etc., these events would lead to serious consequences causing a huge financial setback and environmental concerns such as spillage of oil. Moreover, as per IMO marine safety committee, DP vessel must be able to maintain its position for station keeping reliability even in case of the worst case failures. Thus, to harness the benefits of dc distribution with variable speed generation system in such marine vessels, a robust and comprehensive protection system is needed so that uninterrupted power flow is ensured under all contingencies.

With this regard, this thesis considers dc PSV as the target SPS and proposes a novel protection system design. PSV is chosen for its importance in the maritime industry, stringent operating conditions and protection requirements. The representative dc PSV is chosen to be in-line with the commercial Rolls-Royce UT-776 vessel which is based on ac power systems. Protection algorithm is designed after detailed modeling and control of the components of the dc PSV and understanding the protection requirements after performing systematic transient analysis with wide variety of fault impedances at various operating scenarios.

1.2 DC SPS vs Land-Based DC Microgrids

DC SPS is similar to the land-based dc microgrid in many aspects. Both are finite-inertia isolated power networks having high penetration of power electronic based generation systems and loads. Depending on the application areas, both land-based microgrids and SPS will have different distribution topologies. For instance, radial distribution is used for land based distribution systems requiring lower reliability while the one-and-half-breaker scheme used for systems requiring higher reliability. Similarly, the dc SPS can have different topologies depending on the operational requirements. For instance, passenger ferries have lower reliability requirements thus can have simpler topologies such as radial distribution systems [13]

while zonal distribution is used in naval vessels which have higher reliability and survivability requirements [20]. Generation systems for the land-based systems have significant renewable energy sources along with the conventional fossil based generation systems. However, due to space and weight constraints there are limited possibilities of including renewable energy sources in the marine vessels. Thus, variable speed based DGs are contemplated to be employed in dc SPS. The DG when operated at variable frequency is able to reduce the fuel consumption and emission. In most of the cases, land-based microgrids would have the opportunity to be connected with the stable utility grid. However for specialized applications such as military installations, stable utility grid might not be present. In such conditions, the power depends solely on the available distributed generation systems. SPS can only be connected through a 'ship-to-shore' interface [21] when it is in the dock. However, in dc SPS, the critical loads are the propulsion systems which also forms the major load of the system. Thus, loss of generation system will directly impact the marine missions.

As compared to the land based dc microgrids, dc SPSs are expected to be designed with more reliability to increase safety of the on-board passengers and crews. This demands faster fault detection algorithms for dc SPS applications. One of the prime difference between the land based dc microgrids and dc SPS are the significant differences in the loading

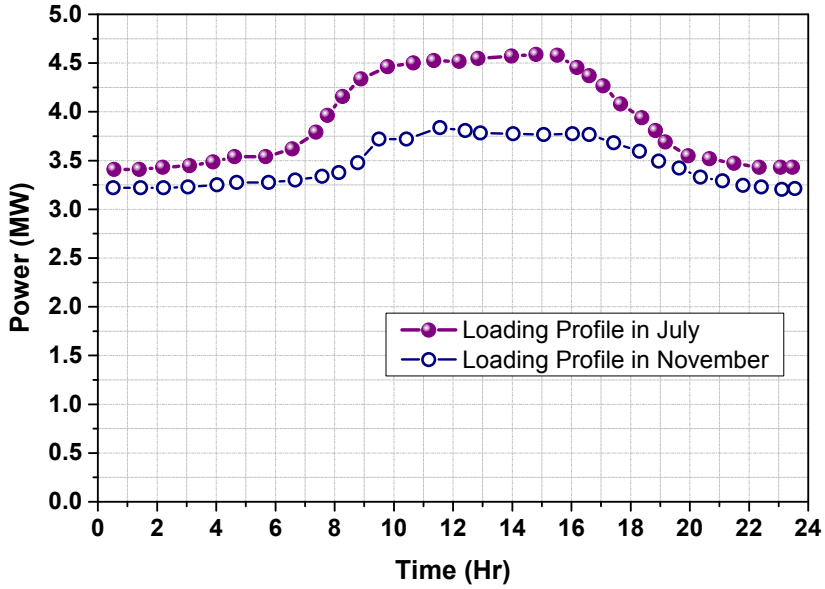
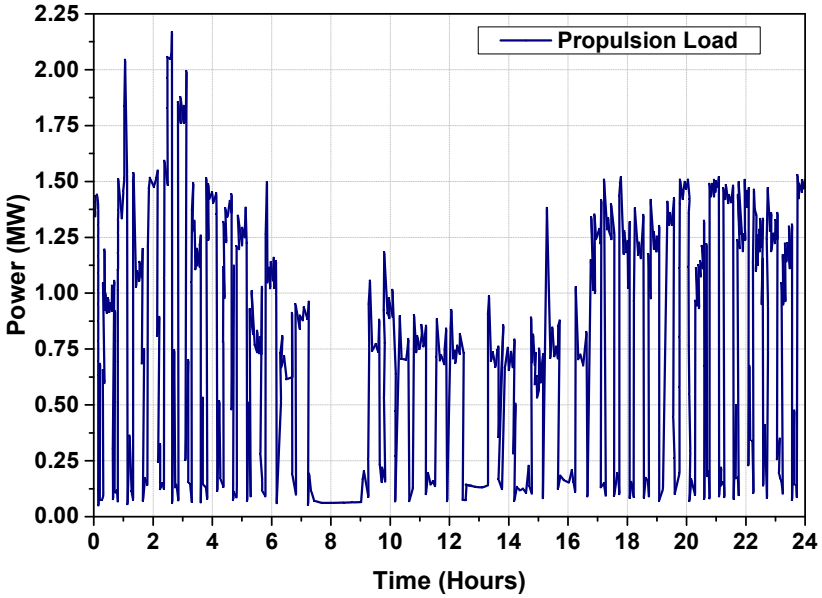
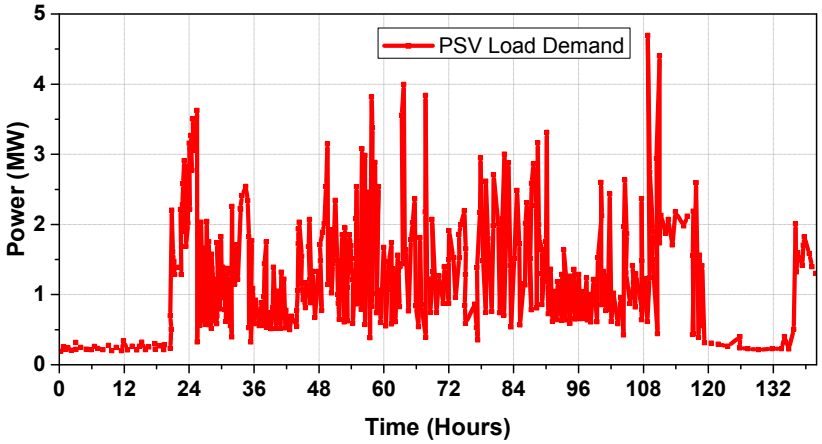


Fig. 1.1: Load demand of the land-based microgrid.

profiles [22]. DC microgrids and high voltage dc (HVDC) transmission systems have reasonably predictable load profiles as shown in Figs. 1.1 [23]. However, dc SPS is equipped with widely varying propulsion loads that may represent 80% of the total installed loads. For instance, the propulsion load demand of a ferry undergoing cruising operation and a PSV undergoing DP operation is shown in Figs. 1.2(a) and (b) respectively [24]. From the comparison between Fig. 1.1 and Fig. 1.2, it can be observed that loads in land-based systems



1.2(a)



1.2(b)

Fig. 1.2: Propulsion load demand of the SPS undergoing (a) cruising operation and (b) DP operation.

are conventional, continuous and generally predictable based on the past events and data. On the contrary, loads in dc SPS are unpredictable, which depends on the operating modes, weather conditions, etc. The loads in dc microgrids are slowly changing while the rate of change of DP load in dc SPS is very high indicating the prominent effect of the environmental and varying load demands. The difference in loading conditions becomes one of the important criteria of the fault detection algorithm. The fault detection method should not detect the fast changing marine loads with the fault conditions.

The other major difference between the land-based power system and SPS is the grounding requirements. Solid grounding is generally used in the land-based microgrids for faster earth fault detection, whereas in the SPS ungrounded or high resistance grounding is preferred as the marine vessels are expected to operate with single earth fault [25]. Thus, the pole-to-pole fault based transient analysis becomes important to develop the fault detection algorithms. A comparison between dc SPS and the land-based dc microgrid is shown in Fig. 1.1.

1.3 Scopes and Objectives

With the above-mentioned discussions, fault detection in dc SPS should fulfill the following functions:

(i) Fault detection algorithm should be independent of the system configuration thus be able to operate with varying magnitudes of fault currents.

(ii) Fault detection algorithm should be able to discriminate between the fault conditions and the fast changing load currents.

(iii) Pole-to-pole fault should be used for transient analysis in dc SPS due to ungrounded or high-impedance grounding conditions resulting in insignificant pole-to-ground fault currents.

The steps to design the protection system for the emerging dc SPS which will have varying system configuration is explained below:

Table 1.1: Comparison between dc SPS and land-based dc microgrid

Attributes	**DC SPS**	**Land based DC Microgrid**
System Inertia	Finite	Finite
Generation Systems*	Dominated by fossil fuel driven generation systems	Possibility of integrating large scale renewable energy sources
Grounding Requirements*	Ungrounded/Floating condition or high-impedance ground	Solid or low-impedance ground
Energy Storage Systems	Limited to 10%-20% of system generation	Depending on installed renewable energy sources such as PV
Rationale of Using dc Power Systems	Reduction of fuel consumption	Increased share of renewable energy sources and ability to work without stable grid
System Topology	Depending on application	Depending on application
Change in system configuration*	May vary widely depending on the marine missions	Known before hand depending on the availability of renewable energy sources
Ability to integrate with stable grid	Stable grid not available during marine operations	Stable grid not available for remote and specialized applications
Major Loads	Propulsion systems for most of the marine missions and hotel loads when in dock	Depending on applications. Hotel loads for building applications and motor loads for industrial applications
Load Demand*	Unpredictable and widely varying depending on marine missions and environmental conditions	Load demand generally known before-hand for target operating conditions
Rate-of-change of Load*	Total loads may exhibit faster transients	Total load demand is continuous

*Major difference between dc SPS and land-based dc microgrid.

(i) System modeling becomes the first important step before designing the protection algorithms. Selection of the generation systems, loads, bus-architectures and their tolerance to external dc faults are instrumental in deciding time required for the fault detection algorithms.

(ii) Following the system modeling, marine missions become an important aspect. It is essential to understand the loading profiles, changes in loads, variations in the network configurations and possible operational contingencies.

(iii) After modeling the dc marine systems with the required operating conditions, transient analysis would be the next step. A detailed short-circuit analysis by varying

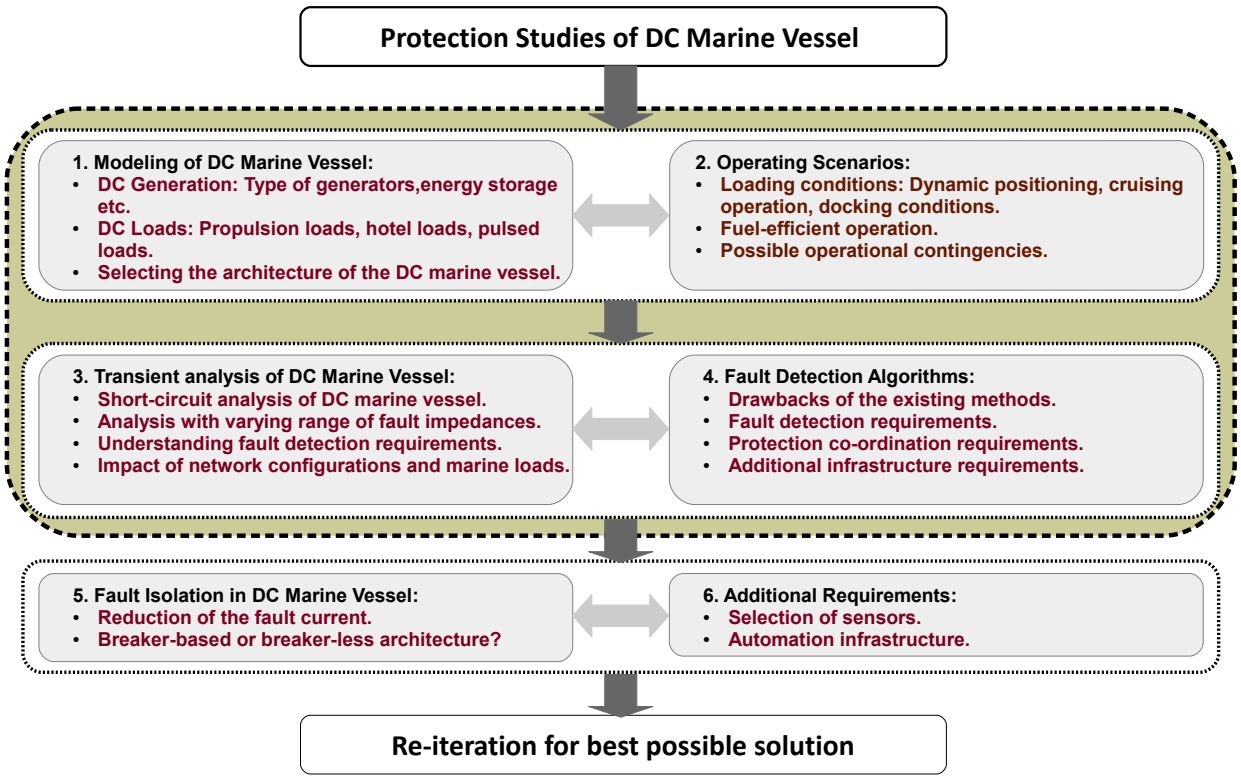


Fig. 1.3: Steps to design the protection system for dc marine vessel.

fault resistances from low-impedance to high-impedance at all the plausible locations would be useful to understand the variation of fault current contributions from various sources.

(iv) After such systematic transient studies, protection requirements of the target dc marine vessel could be determined. Subsequently, the fault detection and protection coordination algorithms can be designed depending on the requirements.

(v) Last step becomes the selection of fault isolation devices and need of any automation architecture to carry out such operation.

This thesis covers the first four steps required to design the protection algorithms which has been outlined by the dashed lines in Fig. 1.3. It has been assumed that the dc circuit breaker (DCCB) is available to isolate the faults. The contributions and organisation of thesis is described in Section 1.4.

1.4 Major Contributions and Organization of the Thesis

The major contributions of this thesis and organization of the chapters are given below:

Chapter 1 : This chapter provides the objectives and motivation of the thesis. The outline of the thesis and the major contributions are described.

Chapter 2 : In the existing literature, dc short-circuit fault management strategies are available for land-based dc microgrids and HVDC transmission systems. This chapter reviews the operation, advantages and limitations of these strategies for the applicability in dc SPS. It is seen that the different aspects of fault management such as fault detection, fault isolation, and reconfiguration are of equal importance and these are needed altogether to develop robust and comprehensive protection systems. The requirements of the protection system for dc SPS is dependent on various shipboard operating factors such as system configurations, marine missions and load conditions [6].

Chapter 3 : This chapter covers the selection, modeling and control of generation system for the dc SPS. This is important as the transient currents are dependent on the type of generation system. For high power dc PSVs, wound rotor synchronous generator (WRSG) fed two-level voltage source converter (2L-VSC) has been selected. The automatic flux regulator (AFR) based WRSG control has been proposed in this chapter and detailed comparison with the traditional automatic voltage regulator (AVR) based WRSG control is conducted. It is seen that the number of voltage sensor and field current requirements for this control is less than the conventional AVR based WRSG control [15, 26].

Chapter 4 : This chapter covers the detailed modeling of the system components such as generation systems, loads, energy storage systems, etc. and subsequently performs a fuel-efficient operational analysis of the dc SPS. Since the operation of dc SPS is different from the land based dc power systems, understanding the operation of the dc SPS would be essential in developing the protection algorithms. The detailed model of dc PSV is developed and fuel efficient operation has been described [4, 5]. Fuel reduction of 19% has been reported in this chapter.

Chapter 5 : After modeling the generation system and operational analysis of dc SPS in Chapter 3 and Chapter 4, respectively, this chapter covers the systematic time-domain transient analysis for varying fault impedances at various locations of dc PSV [27]. It is shown that the time-domain fault detection algorithms are ineffective for the dc PSVs with varying system configuration and the frequency-domain based fault detection techniques are more suitable for such application [17, 28]. A short-time Fourier transform (STFT) based fault detection technique has been presented in this chapter [27, 29–31]. The STFT based method is able to detect low-impedance faults in 1 ms and high-impedance faults in 2 ms. Apart from the fault detection algorithms, this chapter also discusses about sensor requirements for the fault detection algorithm. It is shown that the Rogowski coil is suitable for the fault detection application. A detailed modeling and operation of the Rogowski coil is also discussed in this chapter [30, 32].

Chapter 6 : This chapter proposes a protection solution for the full-fledged dc PSV. The STFT algorithm developed in Chapter 5 is taken for fault identification while a directional zonal interlocking (DZI) method has been developed for the fault localization [27]. This combination of DZI and STFT based novel directional protection is used for the fault detection in dc PSV at generator terminals, load terminals, lines and bus-bars. The fault impedances are valued from 0.001 Ω (low-impedance faults) to 100 Ω (very-high impedance faults). The proposed directional protection is found superior when compared with that of the existing directional protection approaches. The low-impedance faults are detected within 1 ms, the high-impedance faults are detected in 2 ms and the extremely high impedance faults have been set to 'ALARM' condition.

Chapter 7 : The main conclusions of this thesis are summarized in this chapter. Future work recommendations are also given.

Chapter 2

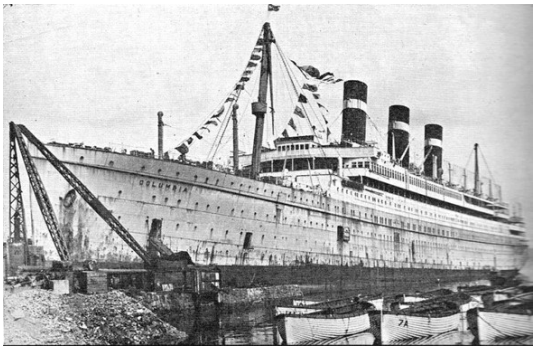
Literature Review

2.1 Evolution of Shipboard Systems

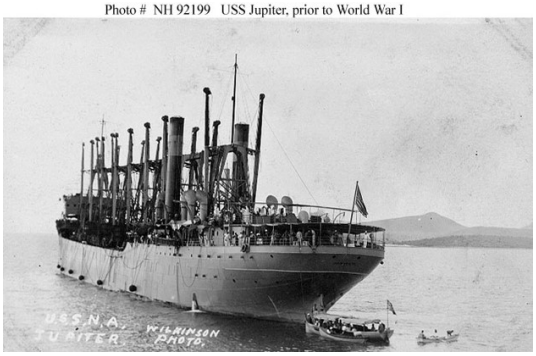
Architecture of shipboard systems depend on the available powering mechanisms of the propulsion systems. The earliest shipboard power system can be traced back to 1880s which is shown in Fig. 2.1. According to the records, *SS Columbia,* was the first commercial ship with on-board dc system [33]. In this vessel, steam turbines were used to drive the propeller while the dynamos were employed to harness the dc power output for the on-board lightning system as shown in Fig. 2.2(a) [33]. With the rising popularity of ac power systems and development of more rugged induction machines and synchronous generators; topologies and architectures of the marine vessels changed accordingly. High-powered propulsion systems were mostly based on turbo-electric machines where steam turbines were used to drive the individual propellers. These steam turbines were used to change to speed of the interfaced generators which in-turn altered the speed of the interfaced motors and hence the propellers. Schematic of this type of propulsion system is shown in Fig. 2.2(b) [33]. *SS Canberra* was the passenger vessel which used turbo-electric propulsion systems in the 1960s [33]. in addition to the turbo-electric propulsion systems, diesel engine (DE)/gas turbine (GT), based direct-propulsion systems were also developed where DE/GT is used to directly power up the propeller using gear-box (GB) of desired conversion ratio. A separate DE/GT was

The results of this chapter have been partially published in:

(i) **K. Satpathi**, A. Ukil, and J. Pou, "Short-circuit protection in DC electric ship propulsion system: Review of existing technologies and future research trends," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 272-291, Mar. 2018.



2.1(a)



2.1(b)

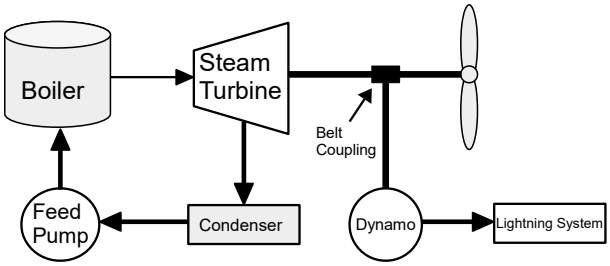
2.1(c)

2.1(d)

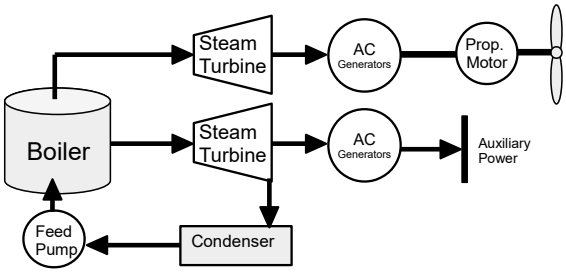
Fig. 2.1: Evolution of ships over time. (a) *SS Columbia* in 1880 (b) *USS Jupiter* in 1912 (c) *SS Canberra* in 1960 and (d) *ABB Dinastar* in 2013. [Source: PinInterest/Getty images]

used to drive the generators to fulfill the hotel and auxiliary load demands. Schematic of this type of arrangement is shown in Fig. 2.3(a). With such topology, *Vandal* became the first diesel-electric powered vessel developed in 1903 and *USS Jupiter* was the first naval ship constructed in 1912. In such vessels comprising of mechanical propulsion, speed of the propellers were adjusted by the operating speed of the prime-movers.

With the development of power electronic devices and conversion systems in the 1980s, variable speed control of the propulsion systems was introduced thus initiating electrical architectures for marine propulsion applications. Such architectures for shipboard power systems (SPS) can be of segregated- or integrated-type as shown in Fig. 2.3(b) and Fig. 2.3(c) respectively. In the segregated-type SPS, propulsion systems and hotel/auxiliary loads were powered from different diesel generators (DGs). However, in the integrated power system (IPS) type SPS, common generation systems were employed to power both propulsion system and hotel/auxiliary loads.



2.2(a)

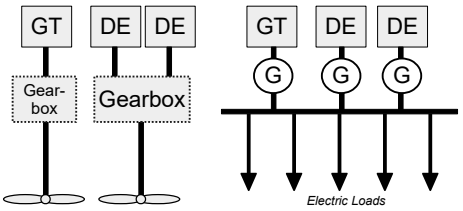


2.2(b)

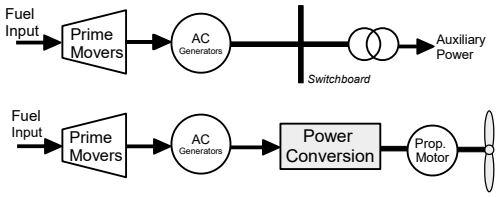
Fig. 2.2: (a) Steam-engine based propulsion system used in *SS Columbia* and (b) turbo-generator based propulsion system used in *USS New Mexico*.

Electric propulsion system is advantageous as compared to the mechanical based direct-propulsion systems. Power-electronics based variable-speed drive has higher efficiency of >95% when the loading is varied from 5% to 100% of the rated capacity. On the other-hand, engine based direct-propulsion system has efficiency of 85% – 90% for rated operating conditions and decreases significantly during low-loads. While employing the IPS architecture, dynamics of the generation and the propulsion systems could be segregated. Fuel consumption of the interfaced DG could further be optimized by turning them ON and OFF depending on the loading conditions. This is not possible in the electrical network in SPS with segregated architecture as shown in Fig. 2.3(b) where the engines powering the propulsion systems should be powered at all loading conditions. Thus, the IPS based architecture have additional advantage of fuel economy [18]. Moreover, the IPS based SPS with variable speed drives has the flexibility to place the components at desired locations for better maneuverability and enhanced fuel efficient operation resulting in significant emission control as compared to the engine based propulsion systems [34]. *Queen Elizabeth* was developed as the first ship, powered with diesel-electric integrated propulsion, inaugurated in 1987 [33]. However, this ship employed the drives to limit the speed control during the start-up and variable pitch propellers were utilized for power control. In later 1980s, fully functional variable speed propulsion systems were employed for cruising vessels. The development of advanced thruster systems such as azimuth and bow thrusters in 1990s resulted in better manoeuvring capability which was applicable for the offshore vessels [35].

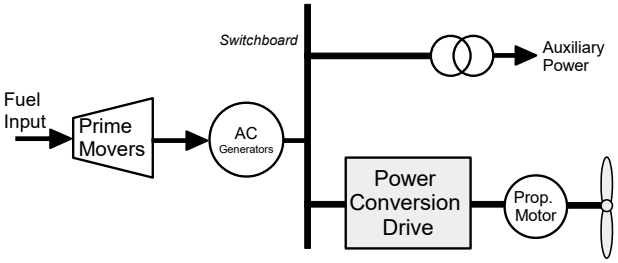
Selection of generators and propulsion motors are of prime importance for SPS which depends on various factors such as the type of vessel, installed capacity, power level and



2.3(a)



2.3(b)



2.3(c)

Fig. 2.3: A typical (a) diesel-engine based direct propulsion system. Integrating drives in the propulsion system by (b) segregated power generation for propulsion and auxiliary loads, and (b) integrated power system supplying power to both propulsion system and loads.

rated speed. The wound rotor synchronous generators, round rotor synchronous generators, permanent magnet synchronous generators are the possible generator types which could be used in the SPS. The selection, modeling and operation of the generation systems has been described in detail in Chapter 3. Asynchronous and synchronous motors have dominated the propulsion systems since the advent of electric propulsion architectures in the 1980s. As a general rule, synchronous motors have been employed for high power > 10 MW while the asynchronous motors have been prominent for power < 5 MW. Between 5–10 MW, rated speed was the decisive factor. In this power range, synchronous motors were used for low-speed propulsion applications while the asynchronous motors were used for medium speed propulsion architectures [36].

2.2 Towards DC SPS

2.2.1 Drawbacks of AC SPS

Architecture of ac SPS varies with the target applications as illustrated in Fig. 2.4 [36]. It can be seen that high-powered propulsion systems are dominant for the cruising and

liquefied natural gas carriers. On the contrary, increased number of propulsion systems and thruster loads are needed for offshore supply vessels and the vessels performing drilling operations. Loading of marine vessel is not fixed and varies over time which is dependent on the environmental conditions, marine missions etc. Fuel efficiency of such ac SPS driven by the DGs are better than the direct-propulsion based systems. However, the fuel efficiency reduces when the diesel engines are lightly loaded. This is illustrated in Fig. 2.5 which shows the fuel consumption of a 2-MW, 1000 rpm diesel engine for all operating speed when the loading of the engine is altered [9]. It is seen that the fuel consumption increases when the loading is reduced while speed being held to constant operating value. Thus for ac SPS which needs fixed frequency and hence constant operating speed, fuel efficiency decreases with decrease in loading. For such ac SPS, fuel efficiency can be improved by turning-OFF the lightly-loaded diesel engines and operating a fewer diesel engines in full-load condition.

2.2.2 Advantages of DC SPS

Fuel consumption of the diesel engines can be substantially improved when operated at variable speed. This operation can be illustrated with Fig. 2.5 where fuel consumption decreases substantially when the operating speed is optimized according to the loading conditions. Variation of operating speed is not possible in the fixed-frequency ac system. However, it is possible in the dc SPS where the variable speed DGs can be interfaced with dc bus using the power electronic interfaces. Apart from the fuel economy there are other advantages of dc SPS which are described below [4],[9]:

(i) *Regeneration:* As compared with the ac propulsion drives with diode front ends (shown in Fig. 2.4), the regenerative energy in dc power systems can be absorbed to other loads connected to the same dc-bus.

(ii) *Distribution Loss and Power Factor:* As compared to the ac systems, the absence of power factor and skin effect in the dc distribution results in reduction of cable size.

(iii) *Space and Weight Reduction:* DC SPS is expected to be more compact than the ac SPS because of the less number of transformers used. The reduced cable sizing in dc SPS also adds to weight reduction.

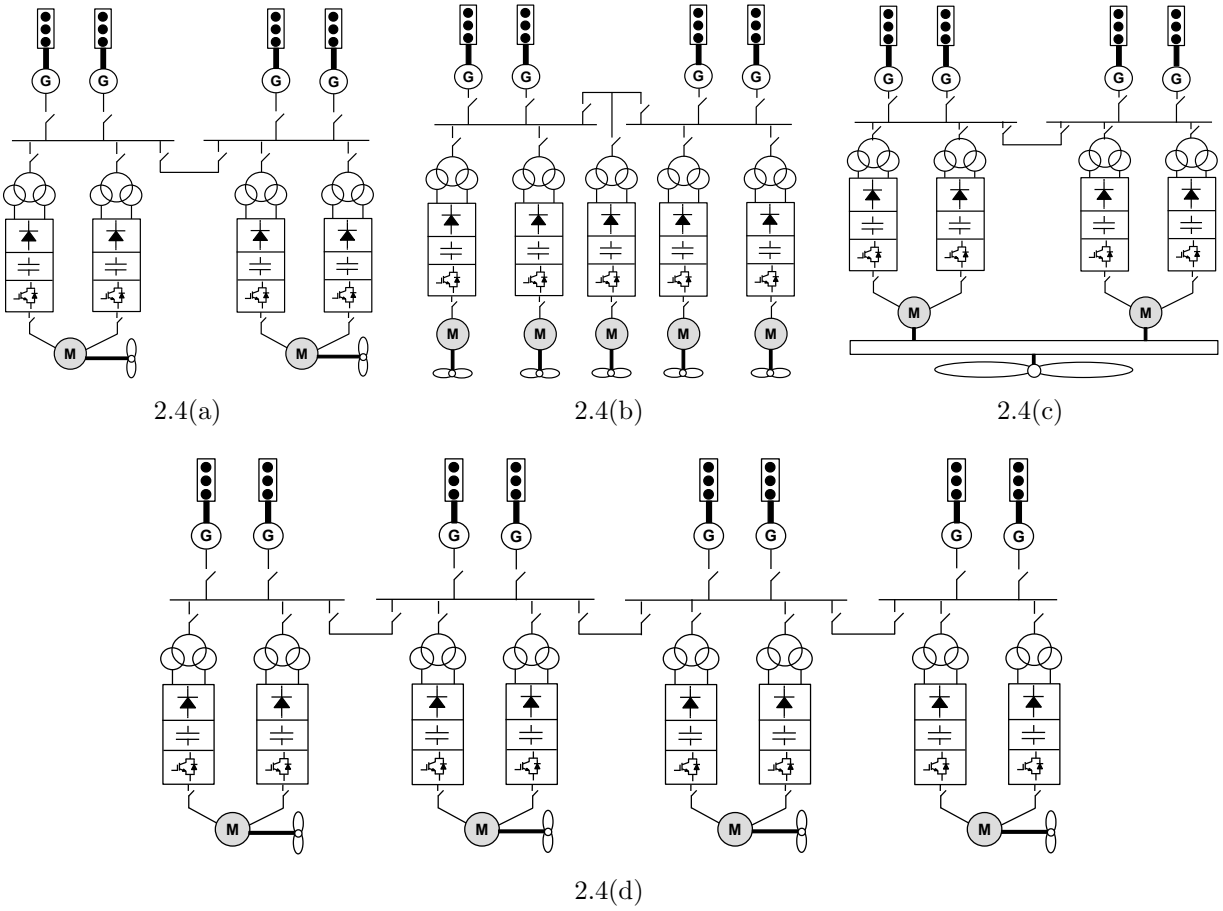


Fig. 2.4: Electrical architecture of (a) cruise propulsion system, (b) offshore supply vessels performing drilling operations, (c) liquefied natural gas carriers and (d) drill ship applications.

(iv) *Integration with Energy Storage System:* Various emerging energy storage systems [4, 7, 37] may be conveniently interfaced with the dc-bus using bi-directional dc-dc converters.

(v) *Quick Synchronization:* Critical phase and frequency synchronization are not required in dc SPS. Thus, in the event of "loss of generator", a reserve generator may be quickly brought on line and connected to the dc bus.

2.2.3 Standards Associated with DC SPS

The dc SPS is still in the research and development phase, hence, a few standards are available which should be referred to while designing and analyzing the dc SPS. IEEE Standard

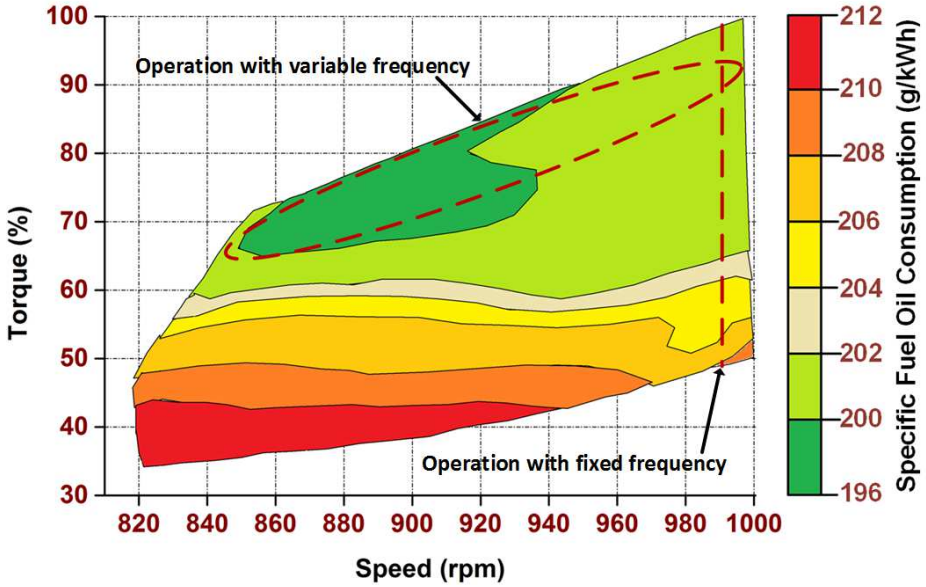


Fig. 2.5: Regions of SFOC in a diesel engine with variation of engine speed.

1709-2010 [25] deals with the design steps indicating the technical problem assessment. IEEE Std 1662-2008 [38] covers the guidelines and specifications of the power converters which are to be utilized in the dc SPS. If zonal distribution system is used in the system, then IEEE Std 1826-2012 [39] and MIL STD-1399 [40] section 300 and section 680 should be referred to. IEC/ISO/IEEE Std 80005-1 [21, 41] deals with the high voltage shore connections when the ship is at the dockyard.

2.2.4 Voltage Level of DC SPS

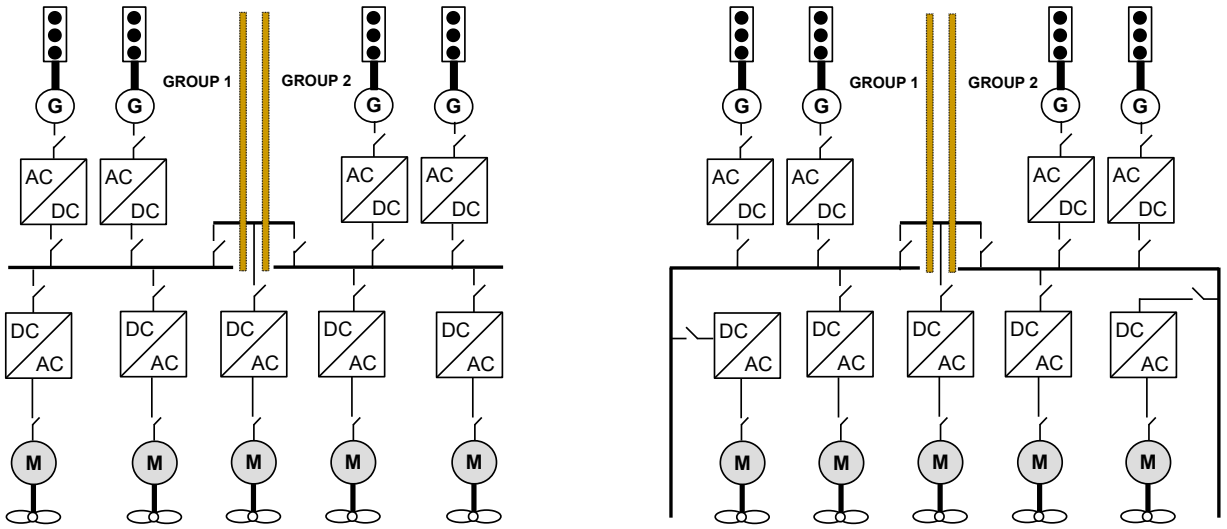
System voltage of the target dc SPS should be based on the desired generator voltage, propulsion motor drive voltage, converter design, load requirements, cable and bus-bar rating, and the fault energy [25]. According to the IEEE Std 1709-2010 [25], various medium voltage dc (MVDC) levels are listed in Table 2.1.

2.2.5 Architecture of the Target DC SPS: Platform Supply Vessel

In this thesis, target application of dc SPS has been considered as platform supply vessel (PSV) which will perform dynamic positioning (DP) and cruising operation and also support the offshore supply vessels. The electrical network of the PSV would look similar to Fig. 2.4(b) having multiple propulsion systems. Architecture of the PSV with dc

Table 2.1: Voltage Level of DC SPS

	MVDC Class kV	**Nominal MVDC Rated Voltage (kV)**
Established Classes	1.5	1.5 or ± 0.75
	3	3 or ± 1.5
Future Design Classes	6	6 or ± 3
	12	12 or ± 6
	18	18 or ± 9
	24	24 or ± 12
	30	30 or ± 15



2.6(a) 2.6(b)

Fig. 2.6: (a) Common bus and (b) distributed bus architecture of dc SPS.

power systems would resemble similar to Fig. 2.6. Architecture can be common-bus type or distributed-bus type as shown in Fig. 2.6(a) and (b) respectively [36]. Common-bus architecture enabled integration of all the converter and associated switchgear in a single cabinet. On the contrary, distributed architecture have flexibility in placing the generation and load systems and their interfacing converters at required location. This is helpful in space utilization and particularly for the podded propulsion architecture where the propulsion drive and propellers are integrated together. It is to be noted that other loads such as the fixed loads, hotel-loads etc. would also be connected to the dc bus.

The target marine vessel operating in DP mode needs higher reliability to ensure avail-

ability of power at all time. The DP operation is achieved by the thrust developed by the tunnel and rudder propellers which helps in maintaining the position of the vessel. Loading on the thrusters are generally low which vary with the environmental conditions. International maritime organization's safety committee circular 645 defines three DP equipment classes [11] which are intended for different levels of station keeping reliability. The classes are DP equipment class 1, 2 and 3 respectively. Generally the modern ships has to pass through DP equipment class 2 or 3 depending on applications. Both DP equipment class 2 and 3 mandates that the loss of position should not occur in the event of single fault in any active component or system. Such DP rules are important in designing the power systems. Some authorities want the vessel positioning system to be robust so that the vessel must be able to hold position even after the worst case failure. To achieve this level of redundancy, open bus-tie and closed bus-tie combination is proposed which are described below:

(i) *Open Bus-tie Systems :* In the open-tie configuration, dc SPS is divided into several groups which are electrically separate and independent of each other. This is shown in Fig. 2.6 when the tie-breakers of dc bus are in open condition. In case of failure of one group the other group takes over the DP operation thus improving the reliability. Prime drawback of this system is limited scope of fuel efficient operation as all the generators are required to operate continuously.

(ii) *Closed Bus-tie Systems :* In the closed-tie configuration, each group is electrically integrated with the other groups. This is shown in Fig. 2.6 when tie-breakers of the dc bus are in closed condition. Thus, fuel efficiency of the generators can be achieved by operating some of them at full load while keeping other standby generators. The prime drawback of this system is reduced redundancy. For such operations, the protection system should be robust to detect faults in every possible operation.

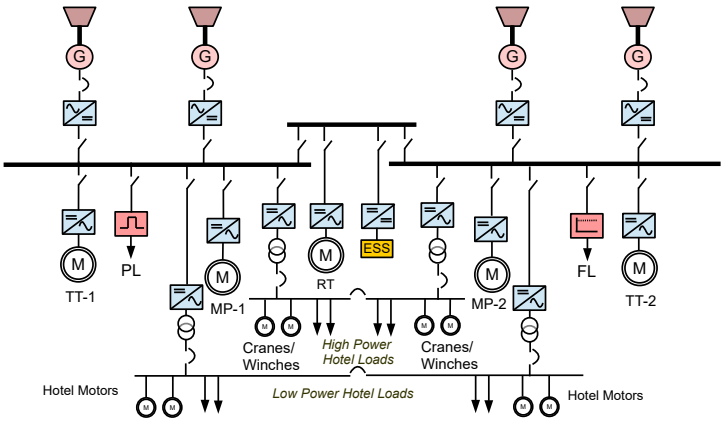
It is thus required to have closed bus-tie configuration with increased reliability to enable fuel efficient operation. Using the common dc bus with closed bus-tie systems shown in Fig. 2.7(a) results in lowest reliability. If the protection system is not carefully designed, faults in one of the main bus may trip all the generation and loads systems. Reliability of dc SPS can be enhanced by adopting breaker-and-half and zonal based distribution system

as shown in Fig. 2.7(b) and (c) respectively [42, 43]. As compared to the common dc-bus, breaker-and-half topology and zonal based distribution system require higher number of breakers which is suited for naval vessels requiring continuous power flow during the warfare.

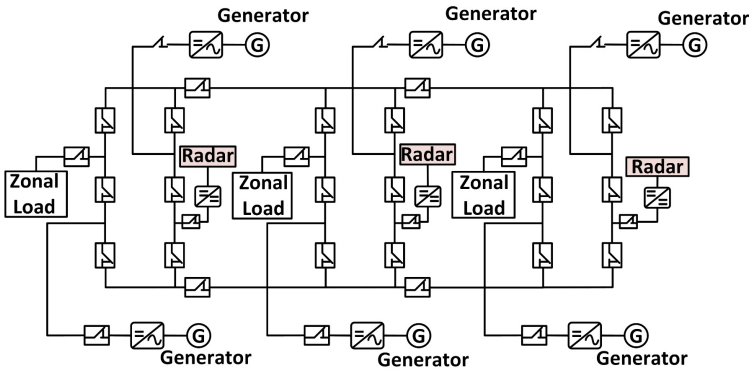
Thus for the proposed dc PSV undergoing cruising and DP operations, radial distribution system having multiple-bus is utilized to improve the reliability [4]. Rather than connecting on the common dc bus, loads are distributed among the buses as shown in Fig. 2.8. The generation system comprises of synchronous generators driven by a DE [4, 44] which could be operated in variable speed. The loads of the dc PSV comprises of main propulsion (MP) to perform the cruising operation and tunnel thrusters (TT) and retractable thrusters (RT) to accomplish the dynamic positioning operation. The high and low power hotel loads are also modeled, which comprise fixed frequency ac loads such as cranes/winches, air conditioning systems, lighting loads, small motors, etc. The detailed modeling of the components and the operation of the dc PSV are addressed in Chapters 3 and 4 of the thesis.

2.2.6 Existing Studies on SPS

System level studies and analysis of SPS is generally carried out using the transient simulation models. Traditionally offline simulation models have been used to for bigger and complex marine systems. They consume consume longer time to generate results which is quite cumbersome to analyze the multiple test conditions. Table 2.2 shows some of the existing simulation methods used to study SPS. It can be seen that most of the analysis has been done to study steady-state operations, development of the control strategies, load modeling and associate studies, control system design and modeling for interfacing additional converters etc. Hardware-in-loop based real-time simulation studies have been taken up in some of the studies in which the prime focus has been on development of the partitioning techniques, validation of the hierarchical control algorithms in the external controllers and so on. However, there have been limited studies on the transient analysis using the real-time simulation models and subsequent detection of the fault detection methods. It has been described in Section 1.3, that the operation of full-fledged marine vessel is required to determine the protection requirements and also for developing the protection algorithms. Thus, as described in Table 2.2, proposed study in this thesis uses the real-time transient simulation models



2.7(a)



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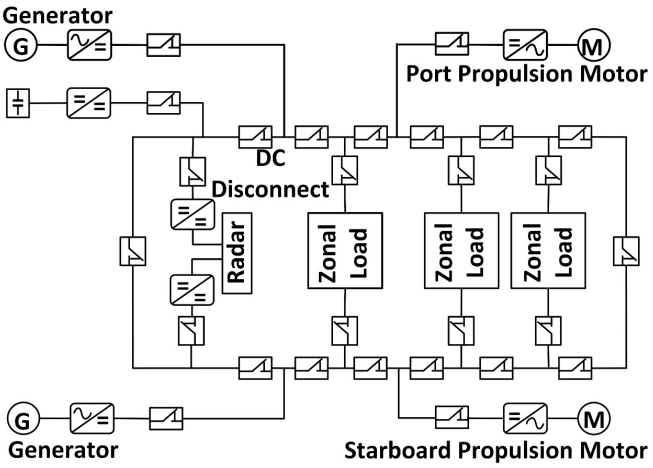


2.7(c)

Fig. 2.7: Typical schematic of dc SPS with (a) breaker-and-half topology, (b) ring bus topology.

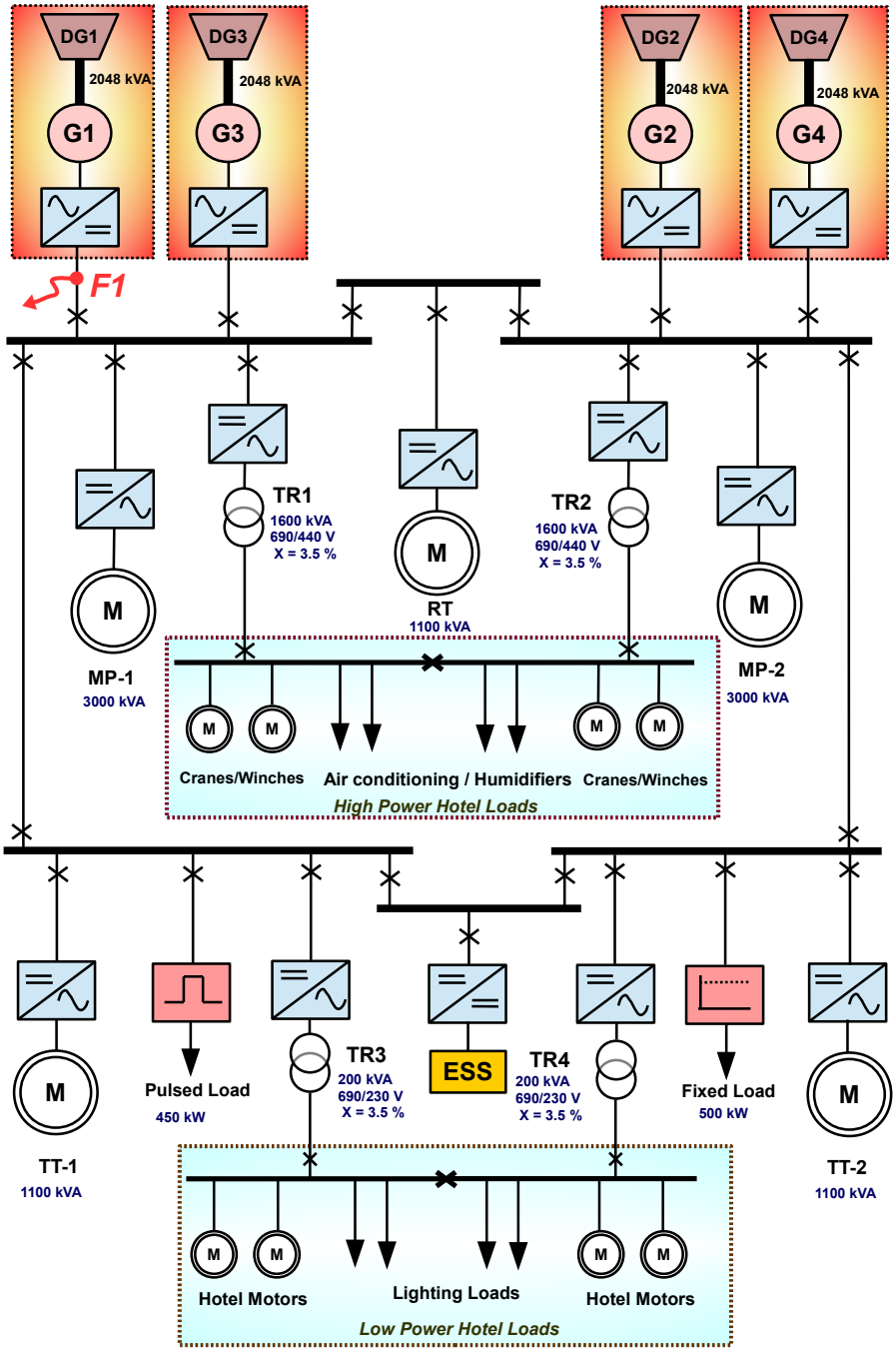


Fig. 2.8: Schematic of the representative dc PSV.

and performs subsequent fault studies. This type of study has not been taken up in earlier

Table 2.2: Earlier works on Modeling of SPS

Vessel Type	**Modeling Technique**	**Target Study**	**References**
AC SPS	Simulation using generalized V-I decoupling	Steady-state power systems analysis	[45]
MVDC SPS	RTDS based real-time simulation	Integration and operation of bi-directional dc/dc converter	[46]
AC SPS for drilling operation	MATLAB/Simulink based simulation	Vessel keeping with varying environmental conditions, electrical-bus reconfiguration	[47]
DC Zonal Distribution System	PSCAD based simulation	Transient analysis	[48]
AC Radial Shipboard System	Real-Time simulation in multicore computers	Developing new partitioning techniques	[49]
Low-Voltage DC All-Electric Ships	System level studies in MATLAB/Simulink by modeling the components in average value model, state-space average value model etc.	Loading profiles of SPS	[7]
MVDC Notional SPS	Average and detailed switching model	Stability analysis of SPS	[50]
DC Zonal electric Distribution System	Hardware-in-loop based real-time simulation	Hierarchical control of DC SPS	[51]
DC Ferry	MATLAB/Simulink based numerical models	Energy management system and study on minimization of fuel consumption	[52]
DC Platform Supply Vessel	Hardware-in-loop based real-time simulation	Modeling, control and operation of generation systems; transient studies and developing fault detection algorithms	Proposed in this Thesis

works.

2.3 Short-Circuit Protection Challenges of the DC SPS

The compact dc SPS is contemplated to be sharply impacted by short-circuit faults. Thus, in spite of the significant advantages offered by the dc SPS, lack of comprehensive fault management techniques to mitigate the short-circuit faults are the major set-backs to adopt

it for the critical marine missions. Prime challenges while designing the fault management strategies for dc SPS are:

(i) *Severe Transient Discharge:* In the dc SPS, current is limited by a very low ohmic resistance. During the short-circuit, entire grid is affected by almost same intensity of fault current [53] which challenges the selective operation of fault detection algorithm thus resulting in limited fault localization.

(ii) *Lack of Current Zero Crossing:* Arc extinguishing becomes a difficult task due to lack of zero current crossing in the dc system. As a result, traditional ac circuit breakers (ACCBs) cannot be used and new fault isolation techniques must be developed.

(iii) *Dependence on Converter Topology:* Short-circuit current is dependent on the interfaced converter topology [53]. For current controlled thyristor bridge topology, current can be reduced to zero, preventing the generator from feeding into the fault location [54]. In the case of IGBT-based VSC, generator continues to feed the fault through the freewheeling diodes till its own ac protection is activated [55].

(iv) *Effect of Output Filter:* The output filter connected with the converter (*'C-filter' for VSC* and *'L-filter' for CSC*) stores a considerable amount of energy during the fault which needs to be dissipated [53].

(v) *System Grounding:* The grounding considerations in the dc SPS is comparable with the ac system but the location of the grounding is different. Since the dc ship is expected to survive single earth faults, high resistance dc-link mid-point grounding is conceived to be utilized [25].

2.4 Practical Issues and Requirements for Protection of DC SPS

2.4.1 Current Sensor Requirements

Current sensor is one of the vital element for successful operation of the fault detection algorithm of the power system and converter controls [32, 56, 57]. An ideal current sensor

Table 2.3: Comparison of Different Current Sensors

Current Sensing Technology	**Low Resistance Current Shunt**	**Current Transformer**	**Hall Effect Sensor**	**Rogowski Coil**
Cost	Very Low	Medium	High	Low
Linearity over measurement range	Very Good	Fair	Poor	Very Good
High Current measuring capability	Very Poor	Good	Good	Very Good
Power Consumption	High	Low	Medium	Low
Current saturation problem	No	Yes	Yes	No
Output Variation with Temperature	Medium	Low	High	Very Low
DC Offset problem	Yes	No	Yes	No
Saturation and Hysteresis Problem	No	Yes	Yes	No

should be able to measure and track the fault current accurately. In traditional ac power systems, current transformers are used for measurement of currents during steady-state and transient conditions. Such current transformers have limited bandwidth which ranges till few kHz. Exceeding these limits results in non-linear operation with potential resonance problems [58, 59]. Further, the current transformer is prone to saturation while measuring high fault currents. Apart from traditional current transformer, there are a variety of current sensors available for the measurement of ac fault currents such as shunt resistors, hall-effect sensors, and Rogowski coils (RCs). Comparison of various current sensors typically used for ac current measurement and transient state detection are depicted in Table 2.3.

For the application in dc power systems, current sensors based on Hall-effect and low-resistance shunt-type can measure dc current. However, Table 2.3 shows that current sensors based on Hall-effect and low-resistance shunt-type have poor linearity and inability to measure high-dc currents (which will be the case during short-circuit faults) respectively. This demands for the use of a different type of current sensor to detect the transient conditions. It is similar to the ac protection where different classes of current transformers are used for measurement and protection purpose. The regular current transformers cannot be used due to magnetization while the RC has restriction in measuring the steady-state dc current. However, RC has been traditionally used to measure the fast changing high frequency ac currents and pulsed loads. Thus, it can be used to measure the rapidly rising transient dc

currents. Moreover, its lower cost, negligible dc offset and saturation problem along with its linear operation, low power consumption and capability to measure high current could make it suitable for fault detection application in the dc SPS where the dc fault current is expected to rise almost instantaneously due to discharge of dc-link capacitors. One of the major disadvantages of implementing RC is the requirement of integrator to translate the voltage induced across the coil into equivalent current value. The integrator requires additional power supply and its choice is dependent on the target application and required bandwidth. Saturation problem of RC is primarily mitigated by constructing the coil over non-ferrous thus having relative permeability $\mu_r \approx 1$. Sensitivity of output thus depends on the construction of the RC (number of turns, geometry of the coil etc.) along with the chosen integrator. Thus, a detailed study on the construction of RC with accurate modeling is required to address these hindrances and before deploying it for the dc fault detection application.

Advantages of RC

Some of the noted advantages of the RC are cited below [60]:

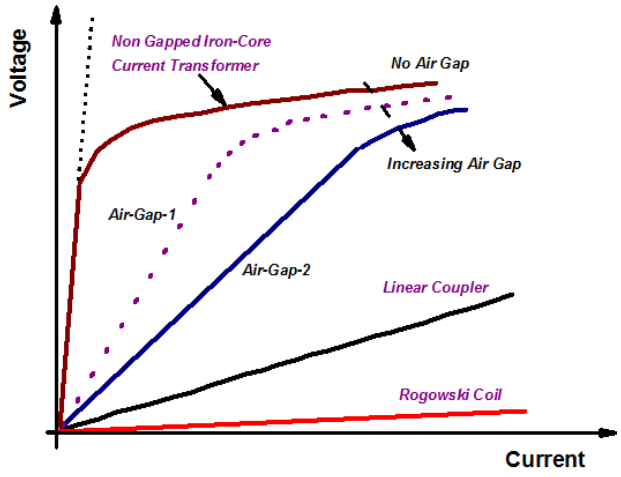
(i) *Linear Characteristics:* Compared with other devices for current measurement, RC has linear characteristic. When the current to be measured goes high, the voltage in the RC does not have saturation problem. This characteristic is shown in Fig. 2.9(a).

(ii) *Ease of Use:* The components of RC are robust, light in weight and easy to manipulate.

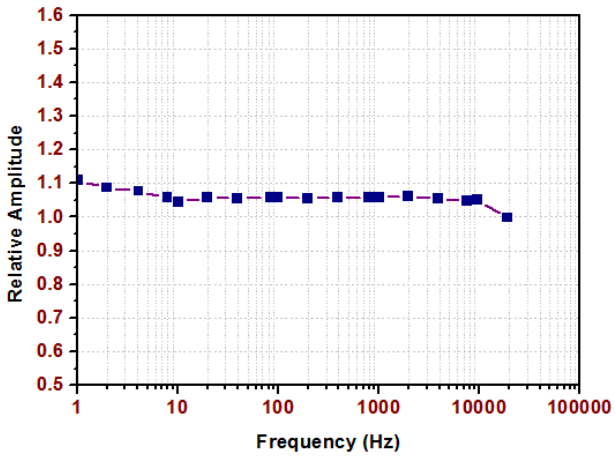
(iii) *Non-Intrusive Nature:* The RC acts as an independent measuring tool which needs to be placed around the current carrying conductor.

(iv) *Wide-Bandwidth:* The RC has larger bandwidth as compared to other current sensors such as LEM Flex II current probe [60] as shown in Fig. 2.9(b). For RC, the measurable frequency range is typically from 0.1 Hz to 1 GHz. This ensures that the transient state is correctly reflected by RC.

(v) *Excellent Transient Response:* The response time of the RC is very fast which is helpful particularly for the protection of dc SPS.



2.9(a)



2.9(b)

Fig. 2.9: (a) Characteristics of different current sensors depicting its linearity and saturation. (b) Bandwidth of LEM Flex II sensor.

(vi) *Safety:* RC is external current measurement device where the current path and measurement path are electrically isolated, hence it provides electrical safety to the operating personnel.

Operating Principle and Modeling of RC

One of the distinguishing features of RC is that the sensor coil is flexible and encircles the current carrying conductor. Thus, according to Ampere's law, current flowing through a conductor passing through the aperture of RC gives rise to a magnetic field surrounding this conductor where [61]:

$$I(t) = \frac{1}{\mu_o} \oint \vec{B}(t).\vec{ds}, \tag{2.1}$$

and according to Faraday's law [61]:

$$u(t) = \frac{d\phi}{dt} = \int B(t).dA = \frac{A}{s}.\mu_o.I(t) \tag{2.2}$$

where μ_o is the permittivity of free space, $u(t)$ is the induced voltage in the coil terminals, B is the magnetic field, I is the current, A is the cross-section of the coil and s is the number of turns per length unit. The voltage measured across the coil would be proportional to the rate of change of magnetic field, which is directly proportional to the rate of change of primary current.

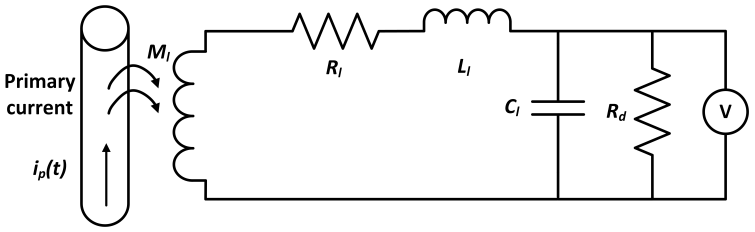


Fig. 2.10: Lumped model of Rogowski Coil.

It can be observed that the output of the coil varies instantaneously when the fault occurs. However, the ease of fault detection by the coil depends on the geometric configuration. The electrical parameters of a coil depend upon its geometrical structure [62]. The prime attributes of a RC are resistance (R_l), self-inductance (L_l), capacitance (C_l) and mutual resistance (M_l) [61, 62], which are expressed as following:

$$R_l = \rho_c \frac{l_w}{\pi d^2}, \tag{2.3}$$

$$L_l = \frac{\mu_o N^2 d_{rc}}{2\pi} ln \frac{b}{a}, \tag{2.4}$$

$$C_l = \frac{4\pi^2 \epsilon_0 (b+a)}{log(\frac{b+a}{b-a})}, \tag{2.5}$$

$$M_l = \mu_o N \frac{r_m - \sqrt{r_m^2 - r_{rc}^2}}{4\pi}, \tag{2.6}$$

where, ρ_c is the electrical resistivity of the coil wire, μ_o is the permittivity of free space, l_w is the length of coil wire, d is the radius of the wire, d_{rc} is the diameter of the loop of the coil, r_{rc} is the radius of each loop in the coil, r_m is the mean radius of the RC, N is the number of turns and a, b are the internal and external radius of the RC. Lumped model is utilized for the low-frequency analysis [61] which includes lumped inductor, resistor and capacitor as shown in Fig. 2.10. The transfer function of the lumped model can be given as [61]:

$$H(s) = \frac{V(s)}{I(s)} = \frac{s.M}{L_l C_l.s^2 + (R_l C_l + \frac{L_l}{Z}).s + 1 + \frac{R_l}{Z}} \tag{2.7}$$

Since the resistance of the coil is negligible, the transfer function can be reduced to:

$$H(s) = \frac{V(s)}{I(s)} = \frac{s.M}{L_l C_l.s^2 + (R_l C_l + \frac{L_l}{Z}).s + 1} \tag{2.8}$$

Accurate value of terminating resistor can be calculated using root locus analysis or bode plot, but for not so precise measurement the terminating resistor can be given as:

$$R_d = Z = \frac{1}{2\zeta}\sqrt{\frac{L_l}{C_l}}. \tag{2.9}$$

Terminating resistor is a determining factor of the coil output quality [61]. The coil has better performance for low values and the combined effect of small reflections and ohmic damping results in poor response with the higher termination resistance. $\zeta = 1$ is a good value for terminating resistor for critical damping. RC is modeled and integrated with the target dc SPS at point 'A' (in Fig. 2.8) under study to capture the profile of fault current. The pole-to-pole fault F_1 in Fig. 2.8 is intended to be detected by the RC at point 'A'. RC must be designed according to the dimensions of the dc bus bar is designed to carry the full load current. The bus-bar is designed with 15% margin above the rated current throughout its cross section. The bus bar design parameters are based on the copper development association [63] and are shown in Table 2.4.

Since the RC is intended to measure the fault current on the dc bus, the coil parameters are based on Table 2.4. From Table 2.4, the perimeter of the bus-bar cross section is $(0.2032\times 2) + (0.0127 \times 3 \times 2) = 0.4826\ m$. Hence, the RC of 0.5 m length is chosen for the given bus-bar. The parameters are shown in Table 2.5. The value of R_l is very small hence can be neglected. The L_l, C_l and M_l of the lumped parameter is calculated from (2.4), (2.5)

Table 2.4: Bus-Bar Parameters

Design Specifications	**Parameters**
Generation Capacity	8.192 MW
Bus Bar Voltage Level	1500 V
Bus Bar Current	5460 A
Conductivity of Copper	5.85 x 10^7 Siemens/m
Dielectric Constant	2
Generation Capacity	8 MW
Number of Conductors (N)	3
Length	18 m
Width	0.2032 m
Conductor Thickness	0.0127 m
Thickness of dielectric	2

Table 2.5: RC Parameters

RC Parameters	**Values**
μ_o	1.26 x 10^{-6} H/m
ϵ_o	8.854 x 10^{-12} F/m
Length of the coil is taken as l_{min}	0.5 m
Diameter of each loop of the coil, h	0.002 m
The inner diameter, d	0.078 m
The outer diameter, D	0.080 m
Number of turns, N	150

Table 2.6: Lumped Model Parameters

Case	**Number of Turns (N)**	**Length of Coil (l)** (m)	**Radius of the Coil (r)** (m)	**Diameter of each loop (h)** (m)	**Inner Diameter (d)** (m)	**Outer Diameter (D)** (m)	$\mathbf{L_l}(\mu\text{H})$	$\mathbf{C_l}$ (pF)	$\mathbf{R_d}$ (Ω)	$\mathbf{M_l}$ (μH)
1	60	0.5	0.079	0.002	0.078	0.080	1.251	29	49	0.436
2	90	0.5	0.079	0.002	0.078	0.080	2.814	29	49	0.654
3	120	0.5	0.079	0.002	0.078	0.080	5.003	29	49	0.873
4	150	0.5	0.079	0.002	0.078	0.080	7.817	29	49	1.0914

and (2.6), respectively, while R_d is calculated from (2.9). However, if N changes then the parameters of the coil L_l, M_l also change. These variations are shown in Table 2.6. The number of turns 'N' of the coil are varied and the parameters of the coil are calculated as per Table 2.5 and Table 2.6. The bolted short circuit is applied at point F_1 and the response of all the different RC cases of Table 2.6 are presented in Fig. 2.11. It can be seen that the induced voltage of the RC is highest for Case-4 which comprises of highest number of turns $N = 150$. The major factor behind this increased voltage is higher mutual inductance between the coil and current carrying conductor.

2.4.2 Timing and Fault Isolation Requirements

DC fault current rises rapidly as the system impedance is low compared to the ac system. In the ac systems, steady-state fault currents are used to detect the fault and determine the protection thresholds. However, for the dc power system, fault condition is determined by rapid discharge from the dc-link capacitors. During the fault conditions, IGBTs will be turned-off by their gate drivers once the current threshold is exceeded and the steady-state fault current will flow through the freewheeling diodes. This prolonged steady-state fault

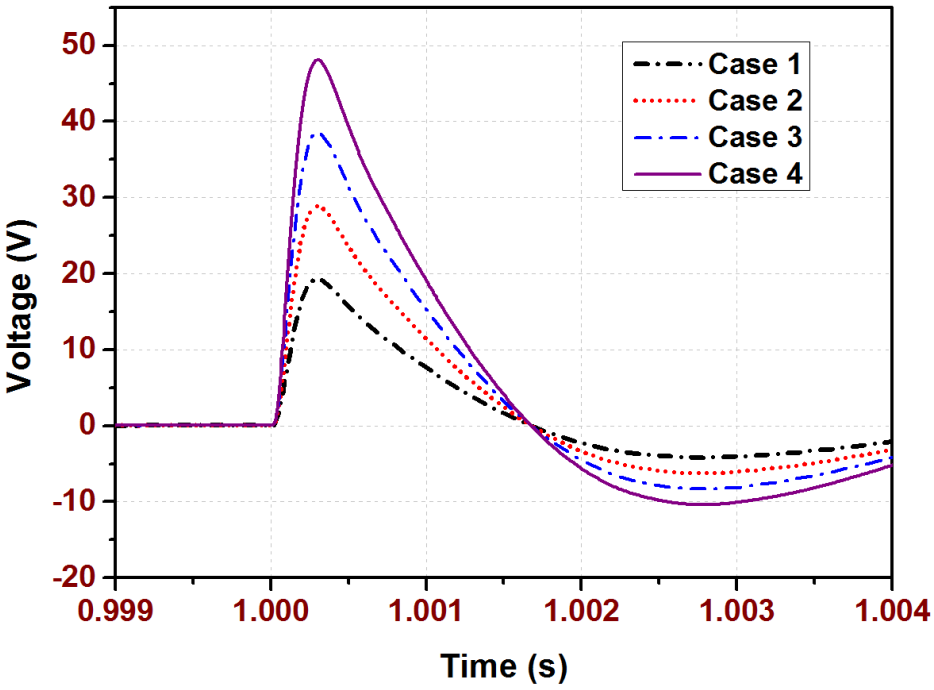


Fig. 2.11: RC output for various design cases as per Table 2.6.

currents will damage the freewheeling diodes once their thermal capability is exceeded [29]. Thus, the protection system should work before the thermal capability of the freewheeling diodes is reached. The converters can be over-designed to increase the thermal capability limits and thus allowing more time for the protection system. This condition will increase the cost of the interfaced converter. Apart from the rapidly rising fault currents, other detrimental effect of the fault condition is collapsing of the dc bus voltage. Such voltage collapse will result in tripping of the propulsion systems and other interfaced loads and hence aborting the critical marine missions. It is thus required that the fault detection and isolation must be completed within < 5 ms so that the thermal capabilities of the converters are not reached and the system voltage is restored quickly. With this regard, faster fault detection is needed to identify and isolate the faults. Algorithms detecting the transient conditions within 1 ms would be helpful for such applications.

In the traditional ac systems, circuit-breakers (CBs) are employed to isolate the faulty section. In such systems, the current and voltage waveforms have zero crossing which helps in extinguishing the arc while breaking the fault current. ACCBs have dedicated arc chutes which help in arc extinguishing and energy dissipation during breaking the fault current.

Time required for this operation depends on the type of CB employed in the system. The selection of arc quenching media is dependent on the power and voltage level. For higher power applications, vacuum and SF_6 based CBs are typically employed. The complete fault detection and isolation in a 50-Hz ac system usually takes around 80 ms.

Due to absence of natural current/voltage zero in dc systems, additional arrangements need to be done for arc extinguishing and subsequent fault current isolation. If CB-based fault isolation is employed, then additional resonance techniques can be used, which induce zero-crossing in the dc current. Further, an additional energy absorption circuit is needed to drive the dc current to zero whose rating depends on the speed of operation, rating of CB and inductance present in the system [64]. Apart from the CB-based fault isolation, breaker-less approach could be employed, which utilizes the interfaced converters as fault isolating devices. The detailed review and discussions of the various fault isolating techniques are covered in Section 2.5.2.

2.4.3 Selectivity Requirements and Challenges in Relay Co-ordination

In addition to successful fault detection, selective fault isolation by co-ordination among the intelligent electronic devices (IEDs) are important to remove the faulty section with minimum disruption to the system architecture. For the dc power systems, selectivity and coordination practices are expected to be adopted from the unit- and non-unit based protection co-ordination methods in the existing ac power systems [65].

Non-unit protection in the ac system is executed by the current or time grading operation where the selective operation is ensured by intentional time delays (in the order of hundreds of milliseconds) in the IEDs [65]. For the dc SPS, such gradings cannot be implemented due to fast-rising fault currents and stringent timing requirements [66]. Unit-based protection algorithm comprises of the differential protection and zone-based directional protection. Differential protection is the most popular unit-based protection technique where the decision (by IEDs) is taken by measuring the current and voltage at both sending and receiving end of the equipment under scrutiny [65]. The most important requirement of differential protection is the need of high-bandwidth communication network requiring the exchange of time-stamped current/voltage signals among the IEDs [65]. Since, dc SPS is of smaller size, differential protection can be easily implemented. However, the prime drawback is the lack of

standardized protocols for implementing the communication architectures for the protection of the dc power systems. On the contrary, protection of ac systems is implemented by using the established IEC 61850 standard. The zone-based directional protection is implemented by computing the fault condition and direction of fault at each local IEDs. The IEDs then exchange status signals with other IEDs or the central computer for fault identification and localization. With the zone-based protection, only status signals are transmitted thus will need low-bandwidth communication infrastructure [27].

It is thus needed to identify the type of protection coordination techniques based on the available resources and requirements. In this thesis the focus has been to develop protection algorithms which have minimal dependence on the communication systems.

2.4.4 Communication and Automation Infrastructure

It is pertinent to install communication and automation architecture to supplement the fault management strategies in dc SPS. In ac substations, data acquisition and transfer is carried out by adhering to the IEC 61850 standard. Data transfer is carried out between the merging units and the intelligent electronic devices (IEDs), while the tripping signals are transmitted by generic object oriented substation event (GOOSE) messages. The GOOSE messages in ac systems take 3 ms which is certainly not acceptable in dc networks where such delay should be limited to 1 ms. There have been significant advantages in the communication infrastructure of the ac substations by adopting the optical fibre communication hence reducing the propagation delay. This delay is further dependent on the packet size and bandwidth of the communication channel [64, 67].

2.4.5 Standardization and Interoperability Requirements

The requirements for the short-circuit fault management in dc ships are quite different from the ac counterpart. Unlike ac power systems, the dc SPS along with HVDC and dc microgrids are custom made mostly by a single manufacturer/vendor. On the contrary, multi-vendor system fosters innovation and enhances competitiveness which can be seen in the ac power systems where a variety of fault detection, isolation devices are available from different manufacturers. Although, there are standards for the development of dc SPS from the power electronics perspective (see Section 2.2.3); there have been lack of codes, fault detection

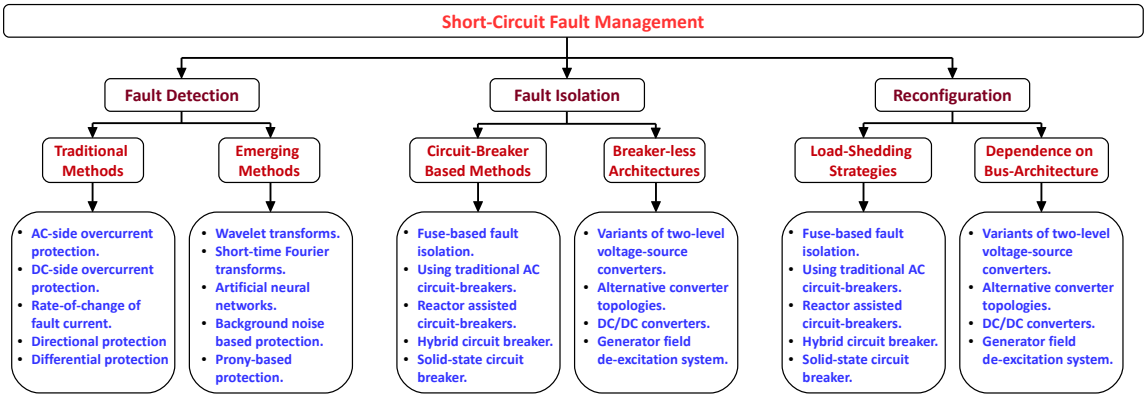


Fig. 2.12: Overview of fault management of dc SPS.

and isolation guidelines, and communication protocols. These gaps in the interoperability requirements if addressed would attract multiple vendors to venture in the area of dc fault management.

Such standardization would be possible with enhanced cooperation and successful implementation of the working groups. Cigré has been the front runner in the HVDC protection. Cigré B4-56 [68], Cigré B4/B5-59 and Cigré JWG A3-B4.34 are the working groups studying the grid codes for multi-terminal HVDC system, control and protection of HVDC grid and requirements for switching devices, respectively. Apart from Cigré, CENELEC TC8x WG6 has also been instrumental for working on dc grids. Communication protocols for the dc systems are expected to be modified version of the IEC 61869, IEC 60255, IEC 61850 and IEC 60834, which are widely implemented in ac systems. These advancements could facilitate the multi-vendor based dc grid protection solution.

2.5 Fault Management of DC SPS

Short-circuit fault management is comprised of three operations which are fault detection, fault isolation and reconfiguration as shown in Fig. 2.12.

2.5.1 Fault Detection and Localisation in DC SPS

Short-circuit fault detection and localisation in dc SPS is expected to be the modified version of that of land-based dc grid system. Due to compact nature of the dc SPS, the short-circuit

faults may severely impact the SPS operation. Hence extra precaution must be taken while designing the protection design for dc SPS. Researchers have been trying to devise suitable algorithms for quick fault detection and localisation in the land-based dc power system. Failure mode and effect analysis (FMEA) [69] and fault analysis have been carried out for low voltage dc (LVDC) and medium voltage dc power systems (MVDC) [70], [28], [71], and HVDC [55, 72]. This section briefly reviews a few notable advancements in the field of dc fault detection and localization methods developed for land-based power system and explores whether these methods would be suitable for the dc SPS.

Traditional Fault Isolation and Localisation Methods

i. **Protection From AC Side**

There are several fault detection algorithms available in the literature for the dc power systems. The simplest of all is the protection from the ac side [54], in which the circuit breaker isolates the ac generation system from feeding into the fault location. This method works well as the ac side protection is matured enough, but the main drawback is the time of operation. The ACCB takes 1-2 cycles to isolate the faulty section, which is excessively long for dc SPS. The handshaking technique can further be utilised for the fault localisation in ring type bus architecture using the direction of the flow of current. This operation results in power outage till the faulty section is isolated, thus making it inept for the vessels undergoing critical marine missions and requiring reliable and continuous power supply.

ii. **Protection Based on DC Side Overcurrent, Rate of Change of DC Current and Voltage**

Overcurrent (OC) based fault detection has been a popular choice for ac power systems [73]. Due to the compact nature of dc SPS, OCs cannot be preferably used because of similar fault current magnitudes across all the sections of dc ship for low-impedance faults. As a result, OC based primary protection is more suitable for point-to-point dc system and as a back-up protection in multi-terminal dc systems [74]. Instead of OC, rate of change of dc current or di/dt has been very popular for fault detection in dc grids [75]. The fault is identified by setting limits on the di/dt value which has also

been experimentally verified [76]. This di/dt can also be useful to determine the fault location as well. With the help of measured di/dt and the measured terminal voltage, the value of inductance of the protected section [76] can be estimated. During the fault condition, the estimated inductance differs from the original value thus localising the fault point. However, the prime drawback of this method is the requirement of high bandwidth sensor as it measures high di/dt and faster calculation with accurate knowledge of pre-fault line inductance. The di/dt works satisfactorily for point-to-point system but its effectiveness for meshed dc power systems is questionable and thus would be an interesting study to make.

In the multi-terminal dc systems, the rate of rise of the fault current can be restricted by adding extra line inductances which alters the di/dt profiles across the dc grid [77]. Inclusion of such protective inductors have been widely used for the HVDC applications where the voltage and power level are significantly higher ($500\times$ or more) than the dc SPS [78]. It is thus needed to place such inductors to limit the rise of current which can be isolated by the dc breakers. However, using the inductors for dc SPS will increase the space of the generation system and also may change the operating conditions.

During the fault conditions, bus-voltage also reduces thus in addition to the di/dt based protection, rate of change of voltage or dv/dt based protection can also be used for the dc SPS. It measures the change in voltage during the faults in the system [79]. The prime disadvantage is that the change in voltage is not significant during the high-impedance faults which would be detailed in Chapter 6. Moreover, the voltage sensor is much expensive than the current sensor and may increase the cost of the protection device.

iii. **Differential and Directional Based Protection**

Fault detection and localisation is generally possible with the differential and directional based unit-protection schemes. The directional protection where the change in current direction indicates the fault condition is most likely to be adopted from the experience in ac power systems [73, 80]. The requirement of this type of protection is to have suitable DCCB to isolate the faulty section. The differential protection used in the ac system can also be applied to the dc system. The basic philosophy remains

same in which the current entering the node equals the current leaving the node [73]. Since the rate of rise of fault current is too high, implementation of differential protection requires extremely fast and high fidelity current sensors [56] and communication requirements [66, 81].

Emerging Fault Isolation and Localisation Methods

i. **Signal Processing Based Methods**

Signal processing tools such as wavelet transform [82–86] and short-time fourier transform [29, 30, 87] based fault detection algorithms have also been applied to dc power systems. Along with the wavelet transform, high precision fault classification method using artificial neural networks (ANNs) have been proposed by researchers [85]. Although these methods provide sufficiently accurate results they are not devoid of challenges. The selection of suitable wavelets and training of the ANN algorithm sometimes might be difficult. Moreover, these methods introduce significant computational burden. Data mining [88] approach is also used by the researchers to determine the threshold values of the relays which are useful for relay coordination. This is applied in multiple distributed generation systems. The suitability of such signal processing techniques while mitigating the practical challenges (Section 2.4) and considering the operating profile of dc SPS would be an interesting area to venture in.

ii. **Protection Based on Converter Operation**

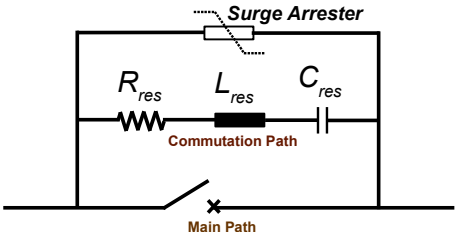
Converter based fault detection has also been suggested by researchers. Capacitor dc circuit breaker (CDCCB) have been proposed, which limits the capacitive discharge current during the fault [89]. Freewheeling diodes of the IGBT based VSC might be replaced with suitable turn-off devices (such as thyristors) which can limit the fault current from ac side [89]. Although the method seems viable if implemented, it would result in bulkier converter design. The solid state defender has been proposed which is designed to operate during the bus faults, load fault and power system transients [90]. Moreover, the solid state defender can also act as an impedance transformer to cope up with the negative impedance instability. However, the requirement of high input capacitor is the major drawback of this method. Moreover, the equivalent series resistance of the capacitor might affect the operation.

iii. **Other Miscellaneous Techniques**

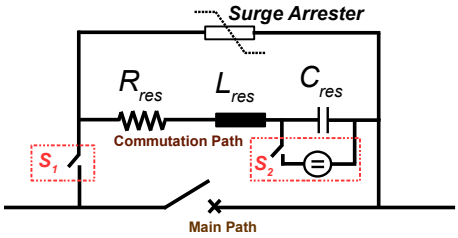
Apart from the above-mentioned methods, some other interesting methods have been proposed for dc fault detection and localisation. For instance, the travelling wave based fault detection is becoming increasingly popular for fault detection in HVDC systems. It measures the time difference between the incident and reflected wave and is suitable for dc power systems with longer lines and cables. However, for dc SPS having short distance, applying this method would rely on stringent communication requirements which is the prime drawback [91], [92]. Similarly, electromagnetic time reversal techniques have been proposed for the fault localisation of HVDC systems [93]. Both methods might not be suitable for dc SPS for its compact size as compared to the HVDC system. Other interesting fault detection techniques include prony based fault detection algorithm [94], and algorithm based on background noise of the converter [95]. Although the methods provide better results, they are still in the development phase and need substantial investigation. The transient impedance based methods are also proposed for the protection of dc power system [96], while the active impedance based methods have been popular for determining the fault location in the zonal distribution systems [97].

Several signal injection based offline methods have also been proposed for the fault location where an external signal is injected and from the return response the fault location is identified [98], [99]. Communication assisted centralised protection has also been proposed where the entire dc microgrid is divided into sub-microgrids. The fault localisation is performed by isolating these entire sub-microgrid once the relay detect the fault. This method needs high-bandwidth communication networks and it has the drawback of power outage during the process [100]. The fault localisation based on the steady state fault current and voltage consisting of sixth harmonic components are also suggested [101].

Distance protection is more suitable for the transmission networks, which essentially monitors line impedance changes during fault conditions. It is more suitable for long-distance HVDC systems where the change in impedance is substantial during the faults. However, the dc SPS is smaller in size where the length between generation systems

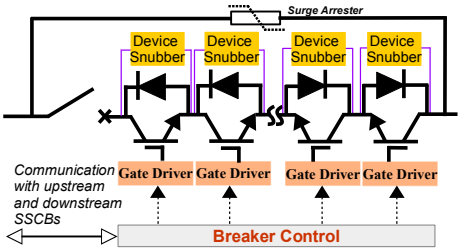


2.13(a)

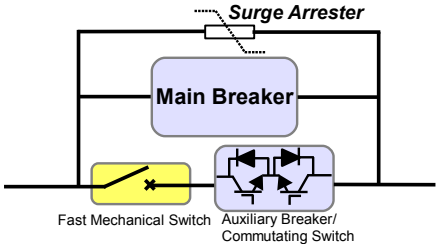


2.13(b)

Fig. 2.13: Schematic of dc circuit breaker with (a) passive and (b) active damping.



2.14(a)



2.14(b)

Fig. 2.14: Schematic of (a) SSCB and (b) HCB.

and loads of maximum 100 m. During the fault conditions, the change in impedance will not be substantial and thus may not be an effective solution.

The existing fault detection methodologies along with suitable references have been indicated in Table 2.7. From the above discussion, it can be inferred that fault detection technique helps in locating the fault. However, fault isolating techniques are required for quick fault isolation, which is described in the subsequent sections.

2.5.2 Fault Isolation of DC SPS

After fault detection and localization, fault isolation is an important aspect of the dc fault management strategy [103], [104]. The dc fault isolation technique must be established, which can work in conjunction with the dc fault detection and localization algorithms thus ensuring selective tripping operation. Tripping of the ACCB to isolate dc fault results in power outage for a significant amount of time. Thus, protection of dc SPS can be broadly classified into breaker-based and breaker-less protection. Conventional ACCB uses the natural zero

Table 2.7: Review of Fault Detection and Localisation Methods

Method	Operation	Limitation	Ref.
Protection from ac side*	(i) During the faults, the ACCB trips. (ii) The faulty section is isolated by no load isolating switches.	(i) Time consuming as the ac circuit breaker takes 1-2 cycles to operate. (ii) Power outage during isolation of faulty section.	[54]
Current Differential Protection*	(i) Matured technology in ac systems. (ii) Measures the current difference of the input and the output.	(i) Stringent communication requirements. (ii) High bandwidth sensor requirements.	[66, 81]
Directional Protection*	(i) Based on magnitude and direction of current/voltage. (ii) Intelligent electronic devices (IEDs) used for monitoring, control and communication functions. (iii) Solid state circuit breakers (SSCBs) used for fault isolation.	(i) High bandwidth sensor requirements. (ii) Low bandwidth communication requirement.	[17, 102]
VSC as current limiter	(i) Capacitive dc circuit breaker (CDCCB) proposed to limit the current discharge from the capacitor. (ii) Anti-parallel freewheeling diodes replaced by turn-off devices.	(i) The CDCCB should be of higher rating and should be fast. (ii) Bulky converter set with complicated control.	[89]
Converter based Protection	(i) Solid state defender developed to operate during bus fault, load fault and power transients. (ii) Also operates as impedance transformer to avoid negative incremental instabilities.	(i) Requirement of high input capacitance. (ii) Equivalent series resistance of the capacitor poses problems during operation.	[90]
Protection using initial di/dt*	(i) Uses rate of current discharge from dc-link capacitor to detect and estimate the fault location. (ii) Simpler concept to implement.	(i) High bandwidth, non-saturable sensor requirements. (ii) Presence of high frequency noise in the capacitive discharge current.	[76]

Method	Operation	Limitation	Ref.
Fault detection by master-slave control§	(i) Slave controller monitors the current flow and master controller monitors the current difference in the slave controllers.	(i) Assumes the passive type loads. (ii) Stringent communication requirements between master and slave controller.	[98, 99]
Using Wavelet Transform and Artificial Neural Networks (ANN)	(i) Wavelet transform for fault detection and ANN for fault classification. (ii) Independent of fault duration and no requirement of injecting external signal.	(i) Choice of wavelet function and decomposition level is important and crucial. (ii) Consumption of large memory and increased computational time.	[85, 86]
Using Background Noise	(i) Switching transients of the converters are used for fault location estimation.	(i) Complicated control algorithms. (ii) Might be difficult to localise fault for multiple paralle generation system.	[95]
Travelling wave based approach*	(i) Measure small difference between incident and reflected wave arrivals. (ii) Have high accuracy.	(i) Might not be useful for compact dc SPS. (ii) Dependent on the topology of the distribution system.	[91, 92]
Prony based method	(i) Faulty section identified and isolated by comparing the fault current direction. (ii) Prony algorithms applied to extract the characteristic frequency.	(i) Immature technology.	[94]
Co-ordination of Converters and Bus-Tie switches*	(i) The converter setpoint is set to zero for fault current mitigation. (ii) System is suitably reconfigured when the converter output is set to zero.	(i) Power outage during the reconfiguration might affect the marine loads and marine operation.	[54]
Sixth-harmonic based method§	(i) Simple concept and easier to implement. (ii) Limited to VSC based dc distribution system.	(i) Requires higher number of steady-state fault current data for better performance.	[101]

∗: Can do fault localisation as well. §: For fault localisation.

crossing in the current and voltage to extinguish the arc generated while breaking the ac fault current. In the breaker-based protection of dc SPS, dc circuit breakers (DCCBs) would be utilized to segregate the faulty section from the healthy section. Due to the absence of natural zero crossing in dc systems, additional arrangements need to be done while extinguishing the dc fault current. For such applications, DCCBs with passive/active resonating circuit[105] shown in Fig. 2.13, solid-state circuit-breakers (SSCBs) [106, 107] or hybrid circuit breakers (HCB) [108, 109] shown in Fig. 2.14 could be employed to extinguish the fault current. It should be ensured that the isolation of the faulty section would result in minimum power interruptions to as many loads as possible. In addition to these, dc/dc converters [110] and Z-source converters [111] could also be used as breakers to isolate the fault sections. Various fault isolation techniques have been listed in Table 2.8.

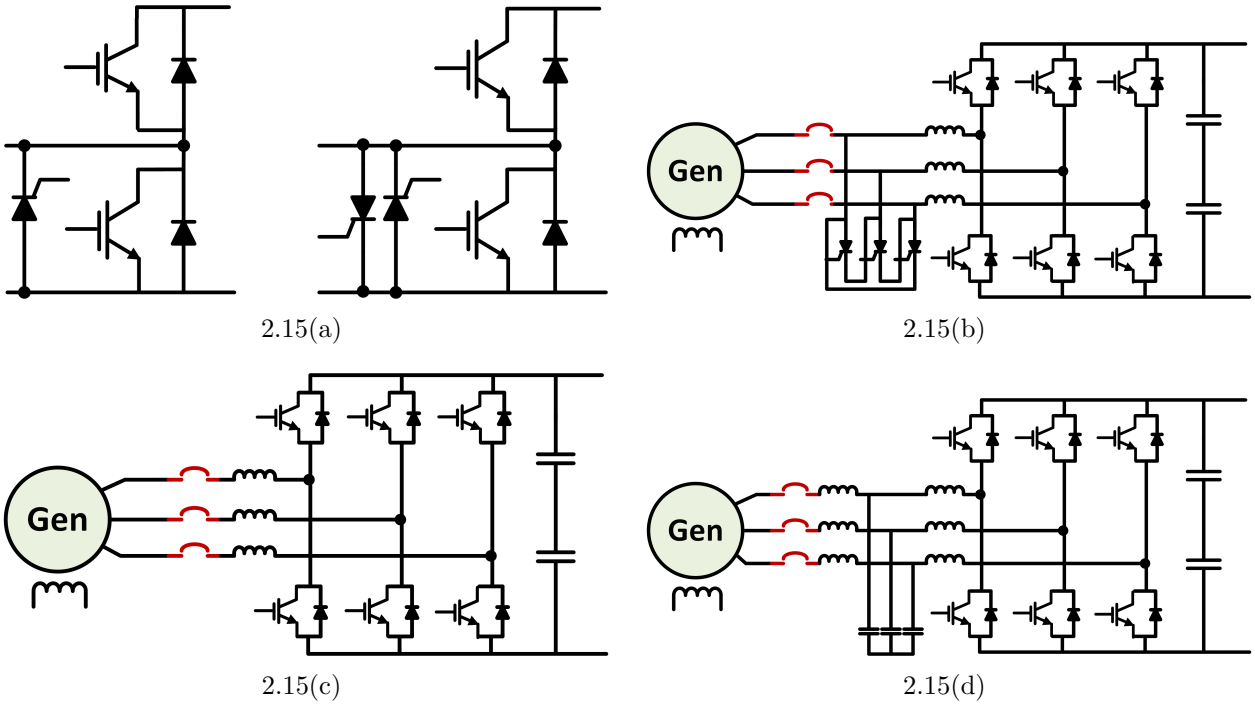


Fig. 2.15: Variants of 2L-VSC: (a) Parallel connection of freewheeling diodes, (b) crowbar circuit in the ac side, (c) high inductance choke in the ac side and (d) LCL filter in the ac side.

Breaker-less protection or the converter based protection of the dc SPS is essentially achieved by interfacing the fault tolerant (FT) converter across the generation system. The FT converter obstructs the fault current contribution from the generation side to the fault

Table 2.8: Review of Fault Isolation Techniques

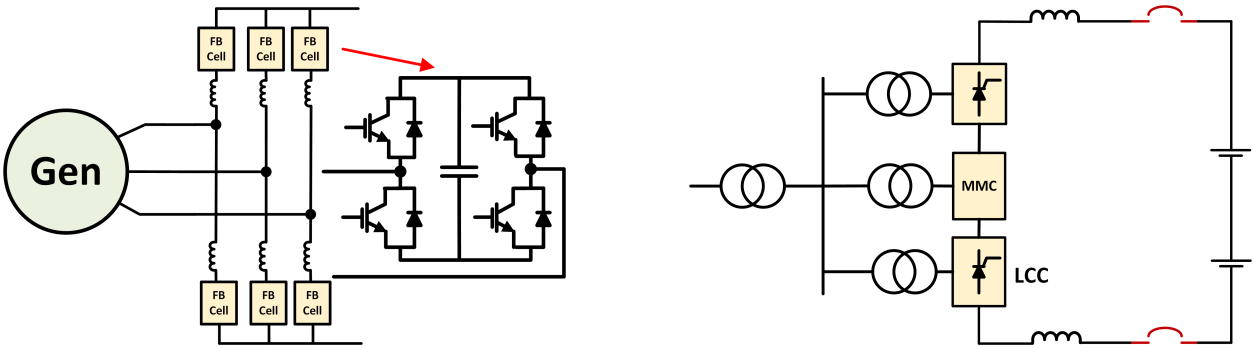
	Method	Technology	Advantages	Disadvantages	Ref.
Modification of AC CB	Conventional ACCB	Arc Quenching Methods using Chutes	(i) Already commercially available.	(i) Might be larger in size. (ii) Might not work properly for larger fault currents.	[105]
	Fuses	Melting when current limit is exceeded	(i) Simple operation and well known technology.	(i) After operation fuse must be replaced. (ii) Cannot be used for protection coordination purpose.	[112]
	Reactor Assisted AC CB	Inducing artificial zero-crossing	(i) Provides galvanic isolation.	(i) Initial current surge cannot be prevented. (ii) Operation dependent on ACCB operating time.	[113]
	Hybrid CB	Arc Quenching + Induced zero crossing	(i) Current commutation is done using the power electronic switches.	(i) In research and development stage.	[114]
DC/DC Converter based Fault Isolation System	Dual Active Bridge	DC/DC converter as breaker	(i) Limits the discharge from the dc-link capacitor. (ii) Offers galvanic isolation.	(i) Cooling arrangements for transformer. (ii) Requires control of two units of 2L-VSC.	[115]
	DC/DC Bridge with LCL filter	DC/DC converter as breaker	(i) Fault current reduction is readily achieved at specified level. (ii) Operation at higher frequency allows for reduction in inductor sizing.	(i) The size of the passive components is concern. (ii) Definitive selection of passive components for particular operating voltage and frequency.	[116]
	Bi-directional Buck Boost Converter	Converter based fault isolation	(i) Low harmonic distortion on phase currents. (ii) Low switching frequency of 2L-VSC resulting in high efficiency.	(i) Capacitor current control. (ii) Requires communication for control purpose.	[117]

	Method	Technology	Advantages	Disadvantages	Ref.
Solid State Circuit Breaker	Solid State Fault Current limiter (SSFCL)		(i) Self triggered interruption capability. (ii) Handles large amount of energy dissipation.	(i) Not suitable for higher voltages. (ii) One shot operation like fuses.	[114]
	SCR based ACCB	Solid-State Circuit Breaker	(i) Anti-parallel connection of SCR used for ac systems. (ii) Performance improvement to overall power distribution system.	(i) Significant thermal losses. (ii) Not suitable for dc application.	[114]
	IGBT/IGCT based ACCB	Solid-State Circuit Breaker	(i) Series connection of the IGBTs/IGCTs. (ii) Ability to detect the fault and turn-off in micro-seconds. (iii) Limiting the fault energy.	(i) More losses than the SCR based breaker. (ii) Contacts must be opened as fast as possible.	[103]

location thus safeguarding the semiconductor switches of the converter and also the interfaced ac generator. The faulty section can be subsequently isolated using no-load isolating switches or low speed mechanical circuit-breakers [104]. The FT converter is majorly divided into two categories which are the variants of 2L-VSC and using emerging converters. In the variants of 2L-VSC, prime motive is to save the freewheeling diodes which can be achieved by several practices shown in Fig. 2.15. However, in the emerging converters, the new generation topologies are used to restrict the flow of fault current as shown in Fig. 2.16. The flow of fault current can also be restricted by choosing wound rotor synchronous generator (WRSG) over permanent magnet synchronous generators (PMSG). WRSG has field circuit which can be de-excited during the faults in the system. Various available techniques for field circuit de-excitation is shown in Fig. 2.17. The breaker-less protection has been listed in Table 2.9.

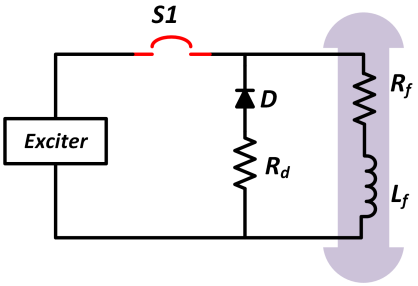
2.5.3 Reconfiguration of DC SPS

After the fault detection and isolation the reconfiguration becomes another important aspect of the fault management of dc SPS. Reconfiguration ensures continuity of power supply for the vessels undertaking complicated marine missions such as cruising [35], dynamic positioning [11], ice-breaking [12], naval warfare etc. During these marine missions, loss of power

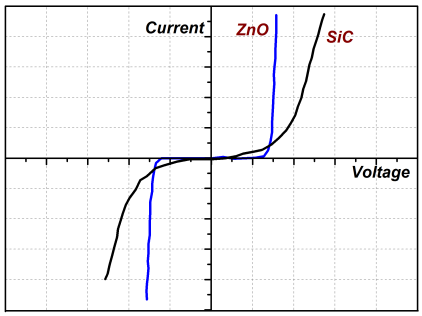


2.16(a) 2.16(b)

Fig. 2.16: Emerging converter topologies (a) 4Q-MMC circuit and (b) series VSC-LCC circuit.



2.17(a)



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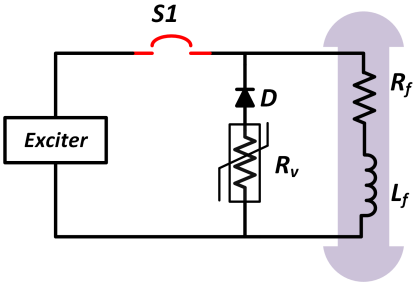

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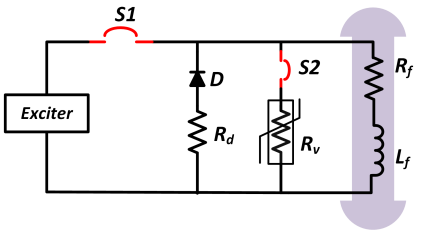


2.17(d)

Fig. 2.17: De-excitation of generator using (a) fixed resistance, (c) voltage dependent resistance; and (d) combination of fixed resistance and VDR. (b) V-I characteristic of SiC and ZnO based VDRs.

due to power system faults is not affordable. The reconfiguration of dc ship is governed primarily by selection of highly reliable bus architecture and load shedding techniques. The reconfiguration methods are described in the subsequent sections.

Table 2.9: Review of Fault Tolerant Generation Systems

	Method	Advantages	Disadvantages	Ref.
Variants of 2L-VSC	Single/Double Thyristor Switches	(i) Fault current is divided hence saving the freewheeling diodes. (ii) Easy to operate.	(i) IGBT module becomes bulky. (ii) The dv/dt remains same as before.	[118]
	Thyristor Activated Crowbar Circuit	(i) Smaller size and lower weight. (ii) Inexpensive thyristors. (iii) Mature technology, used in industry.	(i) Devices to be cooled down before re-starting. (ii) Dependent on operation of GCB. (iii) Susceptible to dv/dt.	[119]
	High choke in ac side	(i) Mature technology. (ii) Reliable component and easy to maintain. (iii) Also reduces current ripple of the machine.	(i) Possibly heavy and larger in size. (ii) Increased cooling requirements. (iii) Increased reactive power exchange and core losses.	[78]
	LCL in ac side	(i) Limit fault current at specified value while maintaining unity power factor. (ii) Reduction of harmonics.	(i) Substantial size of L and C. (ii) Complicated control.	[120]
	Protective Inductor in dc side	(i) Limits the discharge from the dc-link capacitor. (ii) Limits the fault current contribution from the generation side.	(i) Difficult to determine exact value. (ii) Possibly larger size.	[78]
Emerging Converter Topologies	2Q/4Q MMC	(i) Less weight, transformerless design with high efficiency. (ii) Capacitors do not discharge in case of 4Q-MMC. (iii) Modular design thus minimising cost.	(i) Complicated control circuit for voltage balancing. (ii) Inductors required which adds weight and cooling burden. (iii) High speed communication requirement for control purpose.	[121]
	Cascaded H-Bridge Configuration	(i) Modular design minimising production cost. (ii) Capacitor does not discharge during faults. (iii) Mature technology, used in industry.	(i) Difficult to control and requires communication. (ii) Higher initial cost due to additional components.	[122, 123]

	Method	Advantages	Disadvantages	Ref.
Emerging Converter Topologies	H-Bridge cells in ac side	(i) Low harmonic distortion on phase currents. (ii) Low switching frequency of 2L-VSC resulting in high efficiency.	(i) Capacitor current control. (ii) Requires communication for control purpose.	[122]
	Series VSC-LCC converter	(i) Combines the advantage of VSC and LCC. (ii) Reliable component and easy to maintain. (iii) Also reduces current ripple of the machine.	(i) Complicated control algorithms. (ii) Useful for point to point HVDC systems.	[124]
	Bipolar dc/dc Converter	(i) Able to provide very high gain. (ii) Able to restrict the fault current.	(i) More suitable to integrate battery energy storage systems. (ii) Increased number of circuit components.	[125]
Generator de-excitation System	Fixed Resistance based De-excitation System	(i) Faster decay of generator current. (ii) Limits the overcurrent contribution of the connected generators. (iii) Mature technology and is used in the industry for rapid field de-excitation.	(i) Higher de-excitation resistance might cause overvoltages across field windings. (ii) Field circuit breaker also experiences over-voltage for higher de-excitation resistance.	[126]
	Voltage dependent resistance (VDR) based de-excitation System	(i) Limits the induced voltage across the field windings and field circuit breaker.	(i) New technology hence immature. (ii) Choice of type of VDR is a concern. (iii) Difficult to operate in parallel operation.	[127]
	Fixed Resistance + VDR based de-excitation System	(i) Better field de-exciting capability than fixed resistance and VDR based system.	(i) Needs one additional switch. (ii) The voltage setpoint at switch the switch connecting the fixed resistance needs to decided.	

Load Shedding Methods

The reliable bus architecture of dc SPS ensures continuous power supply from the generator to the loads. One way to protect the system from collapsing is by implementing real-time load shedding algorithms [128]. Unlike the land-based dc power systems, the loads in SPS are prioritized according to the marine missions [129]. Generally, the loads are classified in

three groups namely vital; semi-vital and nonvital loads which are dependent on the ship mission.

2.6 Summary

This chapter reviews the operation, advantages, and limitations of these strategies for the applicability in the dc SPS. It is seen that the different aspects of fault management, such as fault detection, fault isolation, and reconfiguration, are of equal importance and these are needed altogether to develop robust and comprehensive protection systems. The dc SPS being different from land-based dc systems, the requirements of the protection system would be dependent on various shipboard operating factors such as system configurations, marine missions, and load conditions.

Part I

Architecture Development of DC SPS

Chapter 3

Generation System in DC Marine Vessels

3.1 Introduction

Generation system in the conventional ac marine vessel i.e. "*ac generation system*" comprises of the fixed frequency diesel generator (DG) to comply with the strict frequency and phase synchronization requirements [8, 130]. However, DG in dc marine vessel is expected to be interfaced with an active front-end (AFE) rectifier, enabling it to run asynchronously and operate in variable speed according to the load demand. As discussed in Chapter 1, this particular operation of "*dc generation system*" (DG + AFE) leads to lower specific fuel oil consumption (SFOC) resulting in increased fuel efficiency [4, 131]. It is to be noted that the common control requirements for ac and dc generation systems is to maintain the terminal voltage of the generation system while operating the interfaced ac generator (of the DG) within the prescribed flux limits. This operation largely depends on the selection of generator and the AFE converter (for dc marine vessel).

Selection of the generators in the marine system depends on the prime-mover, its operating speed as well as on the power level. Fig. 3.1 shows the installed capacity of the generator

The results of this chapter have been partially published in:

(i) **K. Satpathi**, A. Ukil, J. Pou and M. A. Zagrodnik, "Design, analysis and comparison of automatic flux regulator with automatic voltage regulator based generation system for DC marine vessels," *IEEE Trans. Transport. Electrific.* vol. 4, no. 3, pp. 694-706, Sep. 2018.

(ii) **K. Satpathi**, N. Thukral, A. Ukil and M. A. Zagrodnik, "Flux estimation based DC bus voltage control in marine DC power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016. [Best Session Presentation]

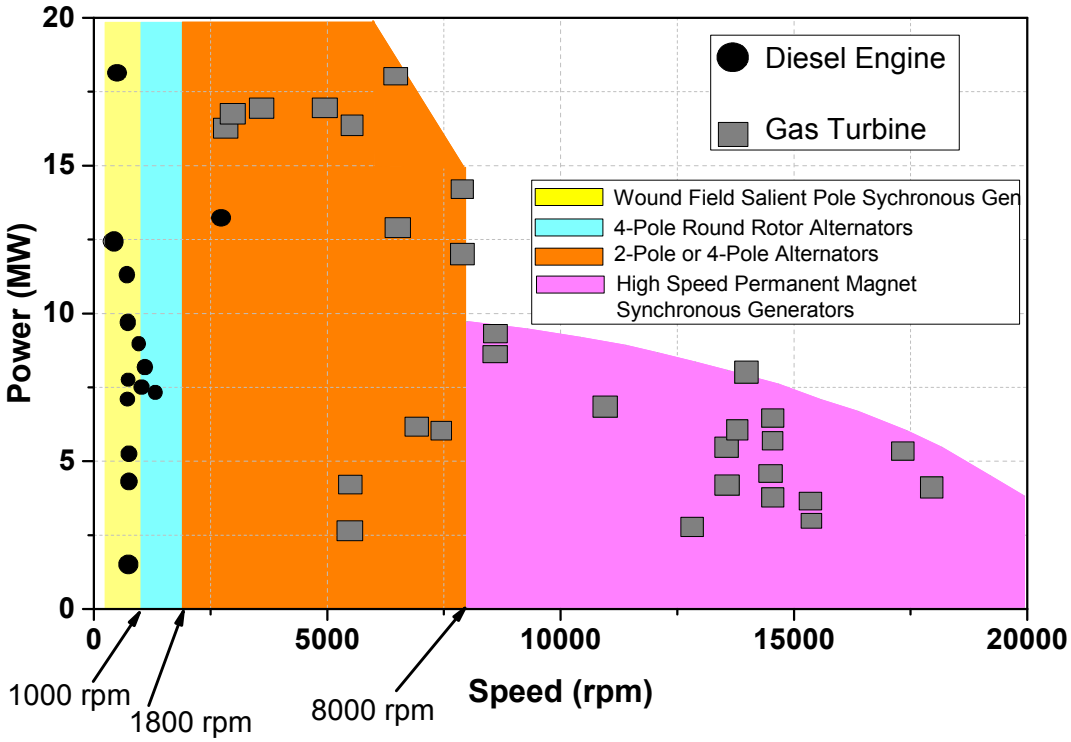


Fig. 3.1: Selection of generators with varying prime-movers and their operating speed.

and the prime-mover which should be used at desired operating speed. It can be observed that diesel engines (DE) should be used as prime-mover at low speed ($<$ 1800 rpm) while gas turbines are used for high speed prime-movers ($>$ 1800 rpm). Correspondingly, different types of generators can be used with such prime-movers which are [132]:

(i) *Wound-Rotor Synchronous Generators (WRSG) :* WRSG based generation systems are used for low-speed ($\leq$ 1000 rpm), high-power generation systems. The pole pairs in the WRSG is mostly ≥ 4. The prime advantage of such system is lower cost and simpler construction. Prime-mover of these generators are the low-speed diesel engines.

(ii) *Wound-Field Round-Rotor Synchronous Generators (RRSG) :* RRSG is the cheapest alternative when compared with turbo-alternators. Pole pairs in RRSG is mostly limited to 4. The operating speed is between 1000 rpm to 1800 rpm. Operation at the lower operating speed results in simpler rotor construction.

Table 3.1: Parameters of the WRSG

Rating	2048 kVA, 690 V, 60 Hz, 8 pole, 1800 rpm
Armature Circuit	$R_s = 0.002591$ pu, $X_{ls} = 0.007$ pu , $X_d = 1.87$ pu, $X'_d = 0.219$ pu $X''_d = 0.116$ pu $X_q = 1.05$ pu $X''_q = 0.121$ pu
Field Circuit	$R'_f = 0.002$ pu $X'_f = 0.5$ pu

(iii) *Turbo-Alternators :* Turbo-alternators are the two-pole synchronous generators typically used in power plants and utilities where the generator is driven by steam or gas turbines. The steel rotor is manufactured by an expensive forging and milling process. The operating speed of these turbo-alternators varies from 1800 rpm to 8000 rpm.

(iv) *High Speed Permanent Magnet Synchronous Generators (PMSGs) :* For very high operating speed (> 8000 rpm), WRSG and RRSG are not suitable owing to the excitation windings, rotating exciters etc. For such applications, PMSGs are found to be a suitable alternative. The absence of rotating exciters and other auxiliaries help the usage of PMSGs for such conditions. However, PMSGs have some disadvantages such as requirements of rare-earth materials for the rotor construction and the inability to control the rotor-flux during transient events such as power system faults.

In this thesis, DE based prime-mover is chosen whose rating is 2048 kVA and operates at 1800 rpm. This particular prime-mover is chosen as similar type of prime-mover has been used in the Rolls-Royce UT 776 PSV and this thesis studies on the equivalent PSV with onboard dc power system. With this prime-mover, WRSG becomes the suitable choice as per Fig. 3.1. In addition to lower cost and robust design, WRSG has superior fault current limiting capability, which is partially achieved through a field de-excitation system [126].

3.1.1 AC Generation System

In ac marine vessels, WRSG is generally interfaced with the ac bus [130]. Such cases emulate the control requirements for ac grid conditions where WRSG terminal voltage, i.e., ac bus voltage, is measured and maintained at the desired set-point by a closed-loop voltage regulator based field excitation system which is conventionally known as the 'automatic voltage regulator' (AVR). Availability and measurement of the sinusoidal voltage at the WRSG terminals have supported the widespread utilization of AVR in ac power systems, and also in

the traditional ac marine vessels [133, 134]. The field current is controlled by a dc voltage source which is generally an SCR based phase controlled rectifier [134]. Apart from the time delay introduced by the SCR based phase controlled rectifier, a dominant factor in determining the synchronous generator excitation system is the field winding time constant. A typical open-loop frequency response of excitation control system is shown in Fig. 3.2 [134]. This response is generally determined when the synchronous machine under study is in open-circuit condition. The Bode plot of the open loop transfer function determines the relative stability criteria such as gain margin and phase margin. For stable operation, gain margin $>$ 6 dB and phase margin of $>40^o$ are recommended for the field excitation system. According to IEEE Std 421.2, cross-over frequency is chosen within 5 Hz. The functional block diagram of the AVR is depicted in Fig. 3.3 and comprises of three basic blocks (a, b and c) for voltage regulation and three advanced blocks (d, e and f) for load compensation and stability of the multi-machine system [134]. AVR compares the terminal voltage of the WRSG against a defined set-point and subsequently varies the field current/field voltage to maintain the desired terminal voltage for different loading conditions. In other words, AVR indirectly controls the flux of the WRSG by directly maintaining the terminal voltage to a speed dependent set-point.

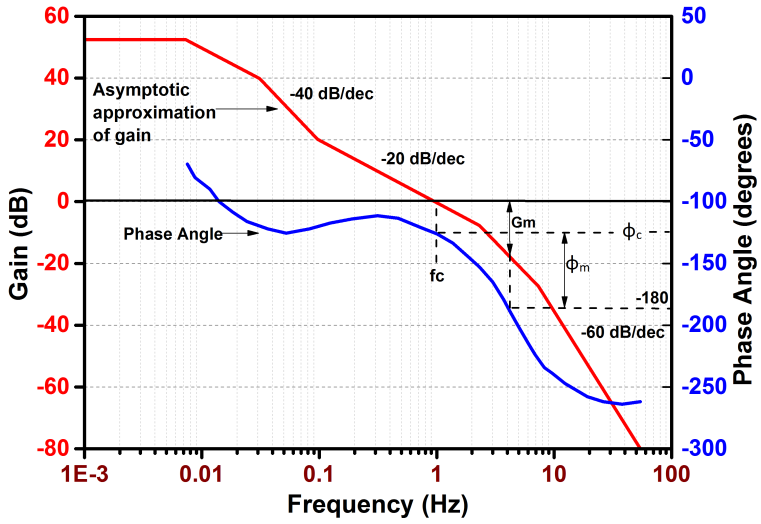


Fig. 3.2: Typical open-loop frequency response of an excitation control system with the generator terminals open circuited.

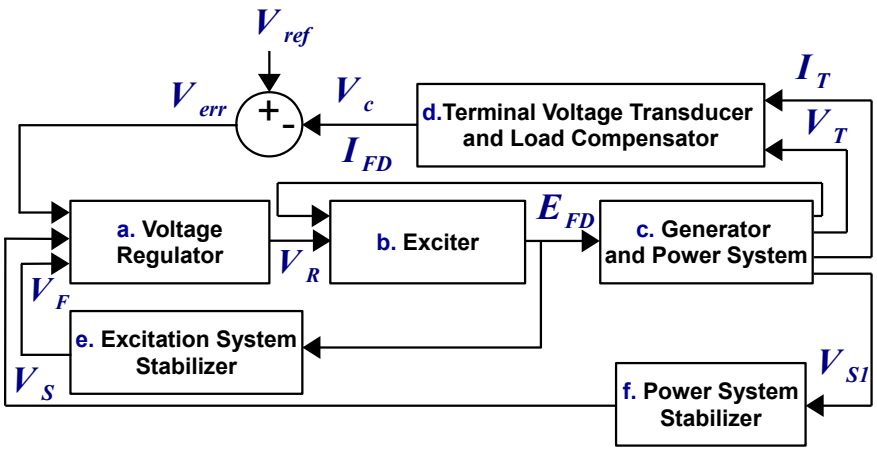
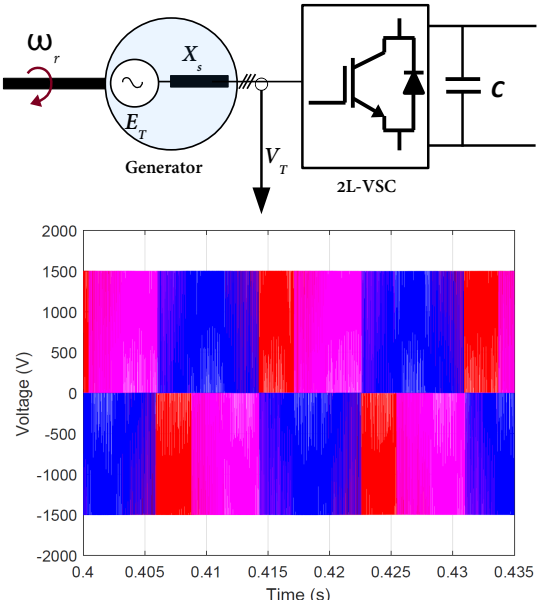


Fig. 3.3: Functional block diagram of AVR based field excitation control system of WRSG.

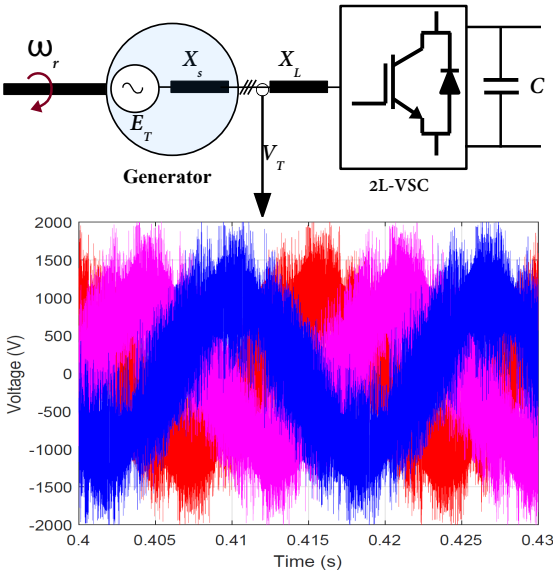
3.1.2 DC Generation System: Problem Statement

Control objective of dc generation system is to regulate the dc bus voltage at the AFE rectifier output while independently operating the WRSG within the prescribed flux limits. In this thesis two-level voltage source converter (2L-VSC) based AFE rectifier has been taken to interface the generation system. Since WRSG is interfaced directly with the 2L-VSC, its terminal voltage is influenced by the switching voltages of VSC which is shown in Fig. 3.4(a). Although the internal voltage of the generator (e_T) is sinusoidal, the terminal voltage (v_T) after the synchronous impedance (X_s) is of switching voltage type. Hence, the measurement of the voltage directly at the WRSG terminal would not reflect its performance thus limiting the applicability of AVR for WRSG terminal voltage and flux control. However, AVR can be suitably integrated by filtering out the switching voltage across the WRSG terminal thus enabling sinusoidal measurement of v_T. To regulate the dc-link voltage, vector control of the 2L-VSC rectifier would be done considering the WRSG (with AVR control) as weak grid network [16].

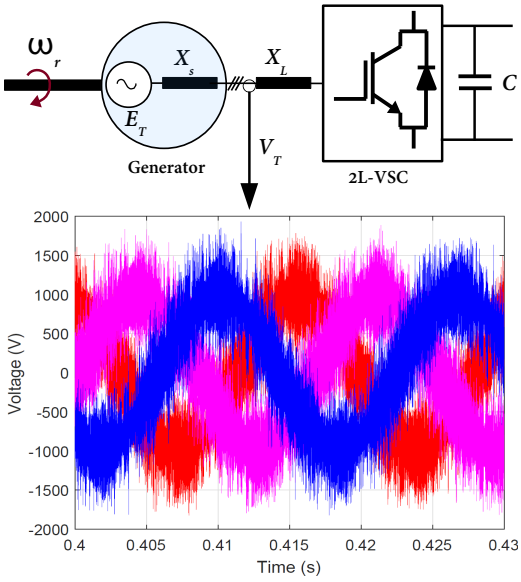
Hence, the type of interfaced filter plays a significant role in devising control framework for AVR based dc generation system. For instance, v_T while using the first order L filter is shown in Fig. 3.4(b) and Fig. 3.4(c). It can be seen that higher value of L is required to get the sinusoidal voltage at v_T. For example in Fig. 3.4(b), L is taken to be 308 μH while in Fig. 3.4(c), the value of L is taken to be 616 μH. However, inclusion of such high L will create



3.4(a)



3.4(b)



3.4(c)

Fig. 3.4: Generator terminal voltage when (a) interfaced directly with the converter and (b) interfaced with the filter inductor ($L = 308$ μH) and (c) interfaced with the filter inductor ($L = 616$ μH).

huge voltage drop across the filter and reduce the converter input voltage. This will limit the maximum dc voltage at the AFE converter output when the loading is increased thus,

slowing down the dynamic response of the system [135]. Thus, higher-order filters such as LCL filter might be an alternative choice to the first-order L filter [135]. LCL filter can be emulated by installing an LC filter at the generator terminal where X_s along with external LC would thus act as LCL filter.

Such interfaced filters for the applicability in AVR based dc generation system increases the space and weight along with increased cooling requirements at higher loads. Moreover, during variable speed operation, the voltage reference set-point to the AVR must be changed continuously to regulate terminal voltage/frequency (v_T/f) ratio hence maintaining the flux of the WRSG.

3.1.3 Automatic Flux Regulator Based DC Generation System

To avoid interfacing of the filter for the integration of AVR, this chapter proposes flux regulation based field excitation system of WRSG and is termed as Automatic Flux Regulator (AFR). Instead of regulating the terminal voltage, AFR directly regulates the machine flux of the WRSG thus indirectly regulating the terminal voltage at the operating speed. Unlike AVR, AFR is independent of the measurement of the WRSG terminal voltage and is an integral part of the flux estimation control routine of the vector control of WRSG [136]. Further, it is independent of the dc bus voltage control at AFE rectifier output which is maintained by controlling torque producing current of the WRSG. This control might be perceived to be derived from the field oriented control of the synchronous machine drive which has received limited attention [136–138] due to the dominance of permanent magnet synchronous generator (PMSG) drives [139–141] and induction generator drives [142–145]. The vector control should be done at the reference frame rotating at synchronous speed to make the control parameters dc quantities. However, it is shown later in Section 3.4.1 that the control in the rotor reference frame (RRF) would lead to installation problems such as the requirement of higher voltage rating of WRSG and interfaced AFE rectifier at full load. Hence, vector control operation at the stator flux reference frame (SFRF) is selected in this thesis, which proves to be advantageous as the torque and flux producing current components are suitably decoupled. Further, there is no need of detailed flux equations in M-T axis of SFRF as the aim is to maintain the total flux of the WRSG using AFR.

3.2 Contributions of the Chapter

As detailed before, AVR based field excitation system directly regulates the WRSG terminal voltage while indirectly controlling the WRSG flux. On the contrary, AFR based field excitation system directly regulates the WRSG flux thus indirectly controlling the WRSG terminal voltage. In spite of the advances in the control paradigm of the AFE rectifier; there has been no study on the design, control and subsequent comparison of these two field excitation control methods intended for the dc generation system of emerging marine vessels. With this regard, the following contributions have been reported in this chapter:

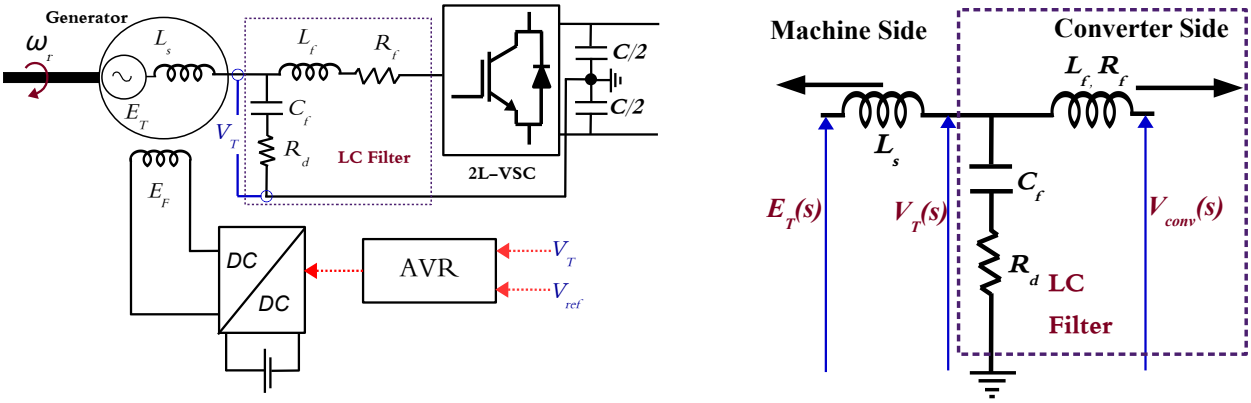
(i) Vector control of AFE rectifier has been devised considering AVR controlled WRSG as weak grid. AVR operation is supported by filter designed at the desired cut-off frequency. Type-ST based AVR [134] has been chosen for its lower footprint and is expected to be suitable for marine applications where space and weight reduction is prime concern [146]. This is a minor contribution which has been included in Section 3.3.

(ii) Vector control of WRSG drive has been devised with the AFR based field excitation system. The control system of AFR based field excitation system is developed by detailed small-signal analysis of the variation of the WRSG flux. The derivation of AFR is done analogously with the AVR based field excitation system for easier and fair comparison. This is major contribution which was missing in the existing literature and has been reported in Section 3.4.

(iii) Control loop design of AVR and AFR based field excitation system of WRSG for dc generation has been made compliant with IEEE Std.421.2 [134]. Subsequently, the comparative analysis based on time and frequency domain analysis has been performed and described in Section 3.5. Such comparatively analysis is a major contribution which has not been previously discussed in the literature.

(iv) Operation of AVR and AFR based dc generation system for various marine operating conditions have been compared and reported in Section 3.6. The operation such as load change, step change, fault conditions have been validated with a real-time hardware-in-loop (HIL) based simulation environment.

The discussions on the findings of this chapter are summarised in Section 3.7.



3.5(a) 3.5(b)

Fig. 3.5: (a) Schematic of LC filter interfaced with WRSG and (b) single phase representation of LC filter.

3.3 AVR Based DC Generation System

To integrate the AVR, sinusoidal voltage is required at the WRSG terminals. It has been discussed earlier in Section 3.1.2 that if WRSG is directly interfaced with the VSC, terminal voltage of WRSG will be dominated by the converter switching components. This prohibits the installation of AVR based field excitation control. Thus, an additional filter is required at the WRSG terminals for the AVR based dc generation system as shown in Fig. 3.5(a). Filter is designed in such a way that the three-phase sinusoidal voltage at fundamental frequency is available at the terminal of WRSG and is denoted by v_{Ta}, v_{Tb}, v_{Tc}. This voltage is measured by AVR and maintained at desired setpoint by regulating the field excitation voltage. Thus, the interfaced 2L-VSC perceives this source as weak grid and controls the dc bus voltage and line current by vector control operation [16] at the reference frame dictated by the phase-locked loop (PLL). PLL uses the phase voltage measured at the WRSG terminals as input and generates reference angle (θ_p) for control. In this rotational reference frame, v^p_{ds} and v^p_{qs} are decoupled from each other. The current at PLL reference frame i.e. i^p_{ds} controls the active power. Current i^p_{qs} is set to zero to enable unity power factor operation. A phasor representation of such operation is shown in Fig. 3.6. With this method, operation of AVR (to maintain the terminal voltage of WRSG and thus the operating flux) becomes independent of the operation of 2L-VSC which maintains the dc-link voltage.

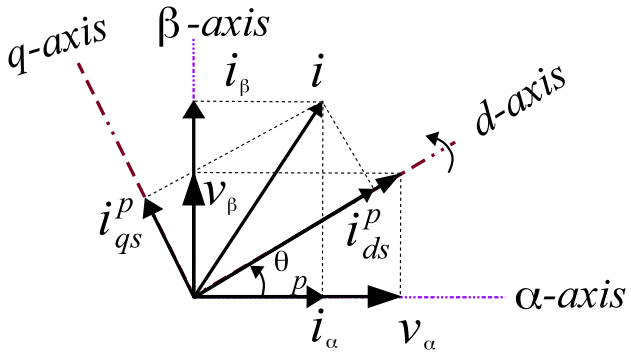


Fig. 3.6: Phasor diagram for vector control of AFE rectifier interfaced with the WRSG regulated by the AVR at PLL reference frame.

3.3.1 Filter Design for AVR Based DC Generation System

Designing the filter becomes an important aspect of the AVR based dc generation system shown in Fig. 3.5(a). A two-level VSC has been used to integrate the variable speed diesel generator. Single phase diagram of the LC filter is shown in Fig. 3.5(b), where $E_T(s)$ is the internal voltage of the WRSG, $V_T(s)$ is the terminal voltage and $V_{conv}(s)$ is the converter input voltage, which is the source of the switching voltages and harmonics. This is a case of LCL filter design where machine side inductance (L_s) and resistance (R_s) are already fixed. However, the relationship between v_T and v_{conv} is dependent on the selected filter parameters L_f, C_f and R_d which are consistent with Fig. 3.5(b) and is given by:

$$\frac{V_T(s)}{V_{conv}(s)} = \frac{1/L_fC_f + s(R_d + R_f)/L_f}{s^2 + s(R_d + R_f)/L_f + 1/L_fC_f}. \tag{3.1}$$

In such a design, selection of L_f and C_f are important to determine the sinusoidal voltage at the WRSG output. To calculate L_f and R_f, base impedance is needed, which is calculated from Table 3.1 using line-to-line voltage, V_{L-L}, and rated power, P, and is given by:

$$Z_{Base} = \frac{V^2_{L-L}}{P} = \frac{690^2}{2048 \times 10^3} = 0.2324\ \Omega \tag{3.2}$$

WRSG is designed to give f_s =60 Hz output, thus the base rotational speed (ω_{Base}) is given by:

$$\omega_{Base} = 2\pi f_s = 2\pi 60 = 376.99\ \text{rad/s} \tag{3.3}$$

From Z_{Base} and ω_{Base} the base inductance L_{Base} is calculated as:

$$L_{Base} = \frac{Z_{Base}}{\omega_{Base}} = \frac{0.2324}{376.99} = 6.16 \times 10^{-4} \text{ H} \tag{3.4}$$

It is now required to calculate the value of filter inductance L_s which will reduce the ripple of line current and is given by [135]:

$$L_f = \frac{V_{dc}}{8 f_{sw}\ \delta I_p} \tag{3.5}$$

where, δ_{is-max} is the maximum ripple allowed in the line current and f_{sw} is the switching frequency. The total inductance should be 10% of L_s to limit the voltage drop across the filter. Thus, the constraint for selection of L_f becomes:

$$L_f \leq 0.1 L_{Base} \tag{3.6}$$

The filter capacitance C_f is selected so as not to increase the reactive power output from WRSG, thus the constraint in selecting C_f is given by [135]:

$$C_f \leq 5\% \frac{P}{2\pi f_s V_{l-l}^2} = \frac{0.05 \times 2048 \times 10^3}{2\pi \times 60 \times 690^2} = 570.5\ \mu\text{F} \tag{3.7}$$

However, C_f can also be calculated by the cut-off frequency (f_{res}) of (3.1) which can be calculated as:

$$C_f = \frac{1}{4\pi^2 f_{res}^2 L_f} \tag{3.8}$$

Selection of f_{res} is dependent on the cut-off frequency (f_c) of (3.1) whose constraint is:

$$10\ f_L < f_c < \frac{f_{sw}}{2}, \tag{3.9}$$

Passive damping with damping resistor R_d has been considered in this thesis to mitigate potential resonant problems. R_d is added in series with C_f and is given by:

$$R_d = 2\zeta \sqrt{\frac{L_f}{C_f}} - R_f, \tag{3.10}$$

where, ζ is the required damping ratio and R_f is assumed to be 1 mΩ.

Filter parameters are computed for two conditions, Case-1 and Case-2 illustrated in Table 3.2. It shows the two conditions with $L_f = 6.16 \times 10^{-5}$ H which is $10\% L_{Base}$ and

Table 3.2: Selection of Filter Parameters for ζ=0.707

Parameters	**Criteria**	**Case:1** ($L_f = 0.1L_{Base}$)	**Case:2** ($L_f = 0.15L_{Base}$)
f_s	–	60 Hz	60 Hz
f_{sw}	–	10 kHz	10 kHz
L_f	(3.6)	6.16×10^{-5} H	9.24×10^{-5} H
C_f	(3.7)	570.5 μF	570.5 μF
ζ	–	0.707	0.707
R_d	(3.10)	0.465 Ω	0.569 Ω
f_{res}	–	878.7 Hz	693.2 Hz

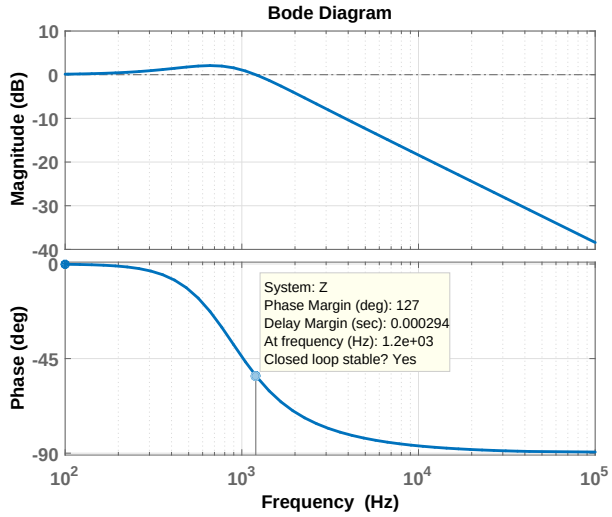
$L_f = 9.24 \times 10^{-5}$ H which is $15\%L_{Base}$ respectively. Fig. 3.7(a) and Fig. 3.7(b) shows the Bode plot of (3.1) for Case-1 of Table 3.2 and terminal voltage of WRSG respectively. Whereas, Fig. 3.7(c) and Fig. 3.7(d) shows the Bode plot of (3.1) for Case-1 of Table 3.2 and terminal voltage of WRSG respectively. It can be seen that THD improves with the increase in L_f. This is because the f_{res} decreases and subsequently f_c also reduces as shown from the bode plots.

3.3.2 Control of AVR Based DC Generation System

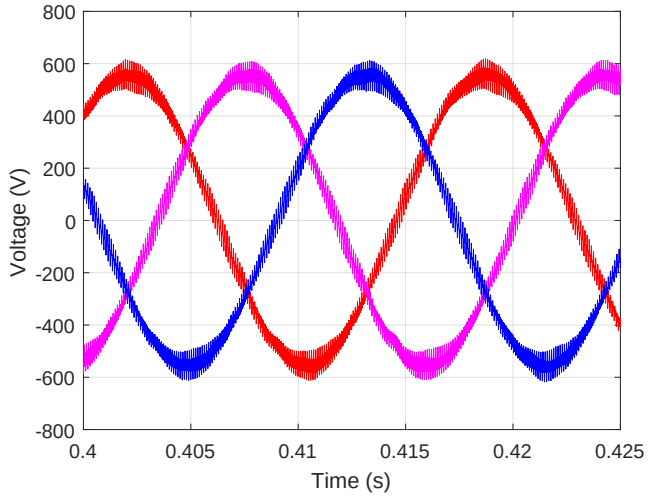
The schematic of the control of the AVR based generation system as shown in Fig. 3.8. The interfaced LC filter described in Section 3.3.1 enables the sinusoidal WRSG terminal voltage (v_{Ta}, v_{Tb} and v_{Tc}). The AVR based field excitation circuit measures this terminal voltage and maintains at the speed dependent set-point. The 2L-VSC perceives WRSG as a weak-grid and controls the voltage at the dc-link output and current through the L_f and R_f of the filter by the vector control operation. The vector control is done by the angle decided by the PLL at the WRSG terminal. The switching frequency of the VSC is set at 10 kHz Hz, the bandwidth of current control loop is set at 1000 Hz, voltage control loop is set at 100 Hz and the bandwidth of AVR control is set at 5 Hz [134].

Controlling Terminal Voltage of WRSG: Selection of AVR

In comparison with Fig. 3.3, basic blocks (a, b and c) have been considered for the AVR control. The control loop schematic of the Type-ST based AVR for regulation of v_T is shown in Fig. 3.9. The parameters of the WRSG are indicated in Table 3.1. Type I generator



3.7(a)



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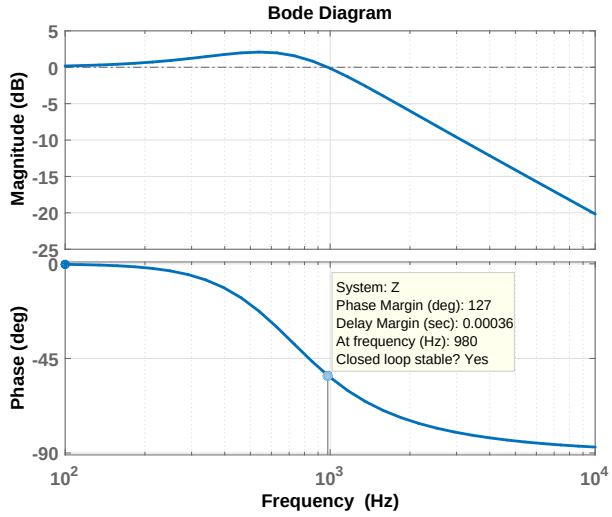

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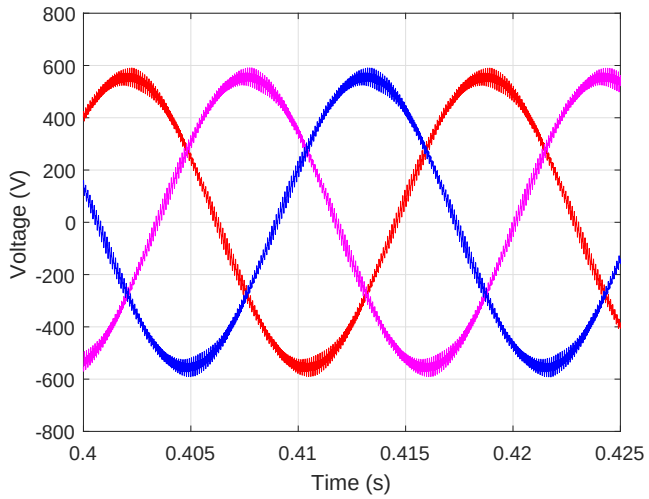


3.7(d)

Fig. 3.7: (a) Bode plot of filter transfer function (3.1) and (b) terminal voltage of WRSG for ζ =0.707, L_f =10%L_{Base} [THD = 6.25%]. (c) Bode plot of filter transfer function (3.1) and (d) terminal voltage of WRSG for ζ =0.707, L_f =15%L_{Base} [THD=5.09%]. (v_{Ta}: Red, v_{Tb}: Magenta and v_{Tc}: Blue).

transfer function is considered as shown in Fig. 3.9 where τ'_{do} is calculated from (3.11) [126]. Using the generator parameters in Table 3.1, τ'_{do} comes to be 3.75 s.

$$\tau'_{do} = \frac{1}{R'_f}\frac{X_{md} + X_{lf}}{\omega_b}. \tag{3.11}$$

First order transfer function has been considered for the exciter with τ_{exc} = 0.01 s and

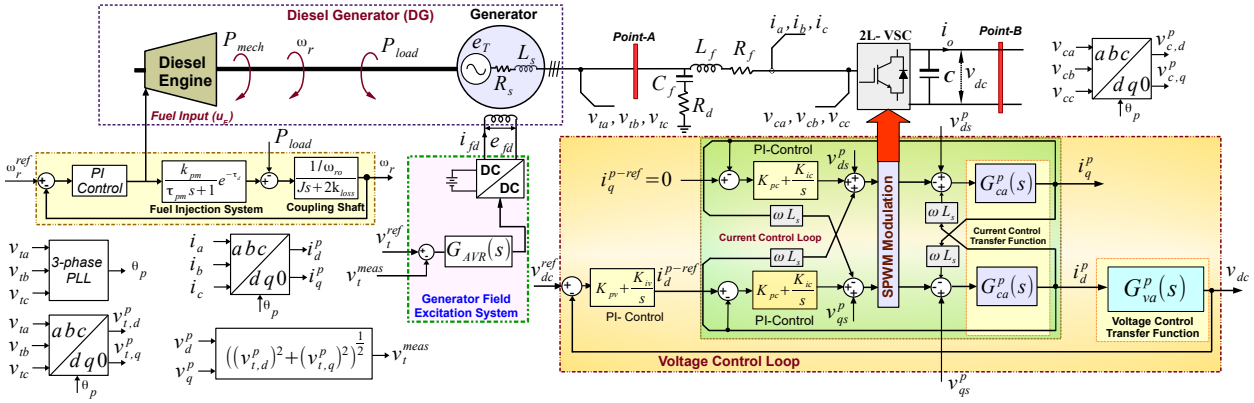


Fig. 3.8: Overview of the functional block diagram of AVR based dc generation.

$K_{exc} = 1$. The AVR is designed for the bandwidth of 5 Hz as per IEEE Std 421.2 [134]. $G_{AVR}(s)$ is the controller of the AVR which is used to regulate the terminal voltage v_T of WRSG to the desired setpoint v_T^{SP}. A detailed analysis to determine the $G_{AVR}(s)$ is done in Section 3.5.

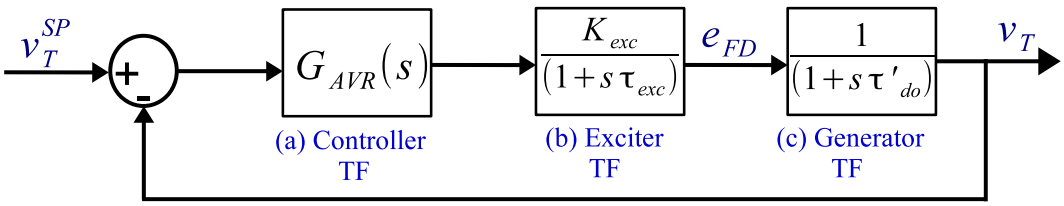


Fig. 3.9: Control system diagram of the Type-ST based AVR for WRSG terminal voltage control.

Voltage Control Loop

By neglecting the power losses across the filter in Fig. 3.8, it is assumed that the power generated at Point-A equals to the power output of the converter (Point-B). This can be illustrated by:

$$\frac{3}{2}(v_{t,d}^p i_d^p + v_{t,q}^p i_q^p) = C\frac{dv_{dc}}{dt}v_{dc} + v_{dc}i_o, \tag{3.12}$$

where, $v_{t,d}^p$, $v_{t,q}^p$ and i_d^p, i_q^p are measured at point-A of Fig. 3.8. At point B, v_{dc} and i_o are measured. C is the dc-link capacitor which is determined by the hold-up time $t_{hold-up}$ and is calculated as:

$$\frac{C({V_1}^2 - {V_2}^2)}{2} = P.\ t_{\text{hold up}} \tag{3.13}$$

where, $t_{hold\ up}$ is set to be 5 ms, $V_1 = 1500\ V$, $V_2 = 0.8V_1$ and $P = 2048$ kVA. Selection of $t_{hold-up}$ has been detailed in Chapter 5 of the revised thesis. The value of C comes to ≈ 25 mF. In the proposed control technique at PLL reference frame, $i_q^p = 0$ for unity power factor operation. Thus the power equation becomes:

$$\frac{3}{2}v_{t,d}^p i_d^p = C\frac{dv_{dc}}{dt}v_{dc} + v_{dc}i_o. \tag{3.14}$$

By perturbation of (3.14), the following equation is received:

$$\frac{3}{2}(V_{t,d}^p + \hat{v}_{t,d}^p)(I_d^p + \hat{i}_d^p) = C(V_{dc} + \hat{v}_{dc})\frac{d}{dt}(V_{dc} + \hat{v}_{dc}) + (V_{dc} + \hat{v}_{dc})(I_o + \hat{i}_o). \tag{3.15}$$

Expanding the perturbed equation looks as:

$$\begin{aligned}\frac{3}{2}(V_{t,d}^p I_{ds}^p + V_{t,d}^p\hat{i}_d^p + \hat{v}_{t,d}^p I_d^p + \hat{v}_{t,d}^p\hat{i}_d^p) = {} & CV_{dc}\frac{d}{dt}V_{dc} + CV_{dc}\frac{d}{dt}\hat{v}_{dc} + C\hat{v}_{dc}\frac{d}{dt}V_{dc} + C\hat{v}_{dc}\frac{d}{dt}\hat{v}_{dc} \\ & + V_{dc}I_o + V_{dc}\hat{i}_o + \hat{v}_{dc}I_o + \hat{v}_{dc}\hat{i}_o.\end{aligned} \tag{3.16}$$

By separating the constant terms, linearizing the perturbed equation and neglecting the higher-order terms, the equation becomes:

$$\frac{3}{2}(V_{t,d}^p\hat{i}_d^p + \hat{v}_{t,d}^p I_d^p) = CV_{dc}\frac{d}{dt}\hat{v}_{dc} + V_{dc}\hat{i}_o + \hat{v}_{dc}I_o. \tag{3.17}$$

Taking Laplace transform, we get:

$$\frac{3}{2}(V_{t,d}^p\hat{i}_d^p(s) + \hat{v}_{t,d}^p(s)I_d^p) = (sCV_{dc} + I_o)\hat{v}_{dc}(s) + V_{dc}\hat{i}_o(s). \tag{3.18}$$

By re-arranging the terms, the following equation is generated:

$$(sCV_{dc} + I_o)\hat{v}_{dc}(s) + V_{dc}\hat{i}_o(s) = \frac{3}{2}(V_{ds}^p\hat{i}_{ds}^p(s) + \hat{v}_{ds}^p(s)I_{ds}^p). \tag{3.19}$$

The plant transfer function for the voltage control loop ($G_{va}^p(s)$) is given by $\hat{v}_{dc}(s)/\hat{i}_{ds}^p(s)$ (shown in (3.20)) which is obtained by defining the disturbance inputs $\hat{i}_o$ and $\hat{v}_{ds}^p$ to be zero.

$$G_{va}^p(s) = \frac{\hat{v}_{dc}(s)}{\hat{i}_{ds}^p(s)} = \frac{3}{2}\frac{V_{ds}^p}{sCV_{dc} + I_o}\Big|_{\hat{i}_o(s)=0,\hat{v}_{ds}^p=0}. \tag{3.20}$$

Fig. 3.10 shows the voltage control loop at PLL reference frame, reference voltage of dc-link (v_{dc}^{ref}) is compared with the measure value v_{dc}. The error signal is passed through the PI control block which gives the $d-$axis reference current ($i_d^{p,ref}$). This is fed to the current control loop which is much faster than the voltage control loop. Thus, to determine the values of the PI controller, the effect of current control loop is neglected.

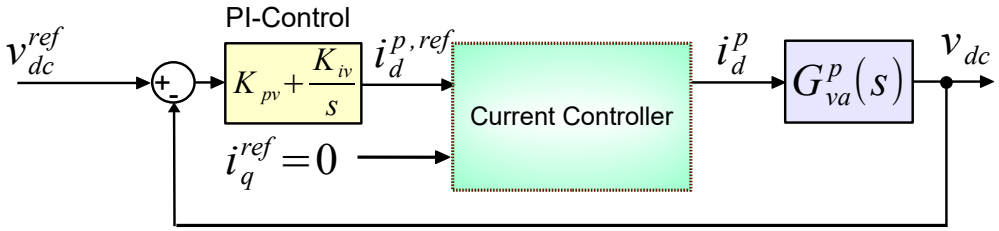


Fig. 3.10: Voltage control loop at PLL reference frame.

Current Control Loop

In the current control loop, line currents i_a, i_b, and i_c are controlled. They flow from point A to point B through the filter inductor L_f having winding resistance R_f. Voltage at the source is represented by (v_t^p) and the voltage at converter input terminal is denoted by (v_c^p), which is shown in Fig. 3.8. Regulating the magnitude and phase of v_c^p with respect to v_t^p results in the required current flow. In the $d-q$ reference frame, the voltage balance equations at the steady-state operating condition are given by:

$$v_{t,d} - v_{c,d} = i_d^p R_f + L_f \frac{d}{dt} i_d^p - \omega_r L_f i_q^p \tag{3.21a}$$

$$v_{t,q} - v_{c,q} = i_q^p R_f + L_f \frac{d}{dt} i_q^p + \omega_r L_f i_d^p \tag{3.21b}$$

where, the variables are consistent with Fig. 3.8. Voltage at the converter terminal $v_{c,d}^p$ and $v_{c,q}^p$ (in $d-q$ axes) is given by:

$$v_{c,d}^p = m_d \frac{V_{dc}}{2} \tag{3.22a}$$

$$v_{c,q}^p = m_q \frac{V_{dc}}{2} \tag{3.22b}$$

where m_d and m_q are the modulation signals in $d-q$ axes. It is seen from (3.21), that both equations are not independent and have decoupling terms of $\omega_r L_f i_q^p$ and $\omega_r L_f i_d^p$ respectively for $d-$ and $q-$ axes voltage balance equations. For decoupling, we derive m_d and m_q using new control variables u_d and u_q which is given by:

$$m_d = \frac{2}{V_{dc}}(u_d + v_{t,d}^p - \omega_r L i_q^p) \tag{3.23a}$$

$$m_q = \frac{2}{V_{dc}}(u_q + v_{t,q}^p + \omega_r L i_d^p) \tag{3.23b}$$

Substituting (3.23) in (3.22), $v^p_{c,d}$ and $v^p_{c,q}$ is given by:

$$v^p_{c,d} = (u_d + v^p_{t,d} - \omega_r L i^p_q) \tag{3.24a}$$

$$v^p_{c,q} = (u_q + v^p_{t,q} + \omega_r L i^p_d) \tag{3.24b}$$

Substituting (3.24) in (3.21), relationship between $u_{d,q}$ and $i^p_{d,q}$ is given by (3.25) which is independent of any coupled terms as per (3.21). This will be used to derive the current control loop.

$$u_d = -(i^p_d R_f + L_f \frac{d}{dt} i^p_d) \tag{3.25a}$$

$$u_q = -(i^p_q R_f + L_f \frac{d}{dt} i^p_q) \tag{3.25b}$$

By perturbation of (3.25), the following equation is received:

$$U_d + \hat{u}_d = -(I_d + \hat{i}_d) R_f - L_f \frac{d}{dt}(I_d + \hat{i}_d) \tag{3.26a}$$

$$U_q + \hat{u}_q = -(I_q + \hat{i}_q) R_f - L_f \frac{d}{dt}(I_q + \hat{i}_q) \tag{3.26b}$$

By linearizing the perturbed equations and neglecting the constant and higher-order terms, a small-signal is developed which is given by:

$$\hat{u}_d = -\hat{i}_d R_f - L_f \frac{d}{dt} \hat{i}_d \tag{3.27a}$$

$$\hat{u}_q = -\hat{i}_q R_f - L_f \frac{d}{dt} \hat{i}_q \tag{3.27b}$$

Taking Laplace transform of this perturbed equation, plant transfer function of the current-control loop is given by:

$$G^p_{ca}(s) = \frac{\hat{i}_{d,q}(s)}{\hat{u}_{d,q}(s)} = -\frac{1}{R_f + sL_f}. \tag{3.28}$$

PI controller is used to implement the current controller. The complete block diagram of the current controller is shown in Fig. 3.11.

Controller Design Parameters

Voltage and current control loops are designed for 2048 kVA generation system. The switching frequency of the interfaced VSC is 10 kHz. The required parameters to compute the plant transfer functions of the voltage and current controller are shown in Table 3.3. The plant transfer function, derived controllers are listed in Table 3.4. Bode plot of the voltage control loop and the current control loop is shown in Fig 3.12.

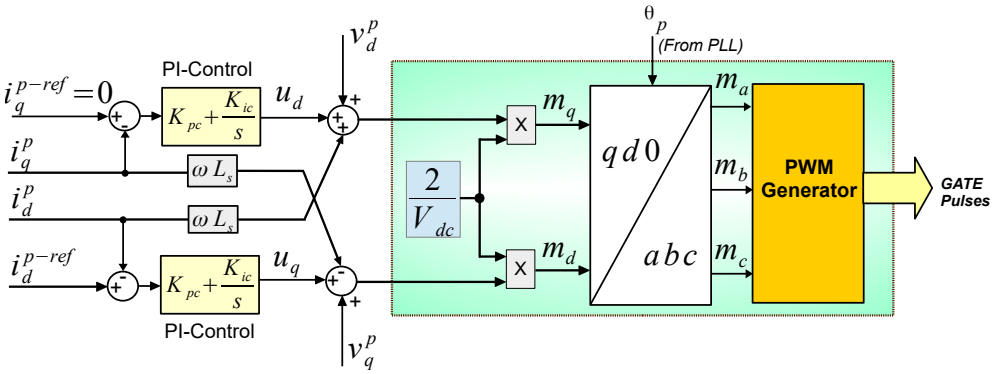


Fig. 3.11: Current control loop at PLL reference frame.

Table 3.3: Parameters to Compute Voltage and Current Control Plant Transfer Functions

f_{sw}	L_f	R_f	C	I_O	V_{dc}
10 kHz	6.16 x 10^{-5} H	1 mΩ	25 mF	1365 A	1500 V

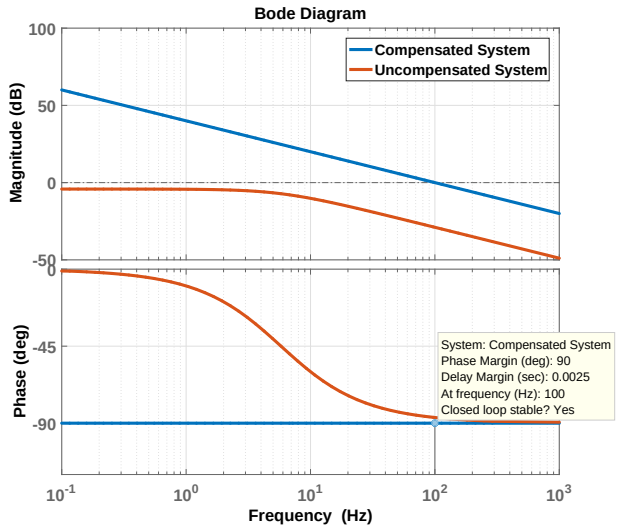
Table 3.4: Controller Design for PLL based Generation System

Parameters	**Voltage Control Loop**	**Current Control Loop**
Plant Transfer Function	$G_{pv} = \frac{22.52}{s + 36.4}$	$G_{pc} = \frac{17391}{s + 17.39}$
Bandwidth	100 Hz	1000 Hz
Proportional Constant	$k_{pv} = 27.9$	$k_{pc} = -0.387$
Integral Constant	$k_{iv} = 1015.56$	$k_{ic} = -6.283$
Controller Transfer Function	$27.9 + \frac{1015.56}{s}$	$-\left(0.387 + \frac{6.283}{s}\right)$

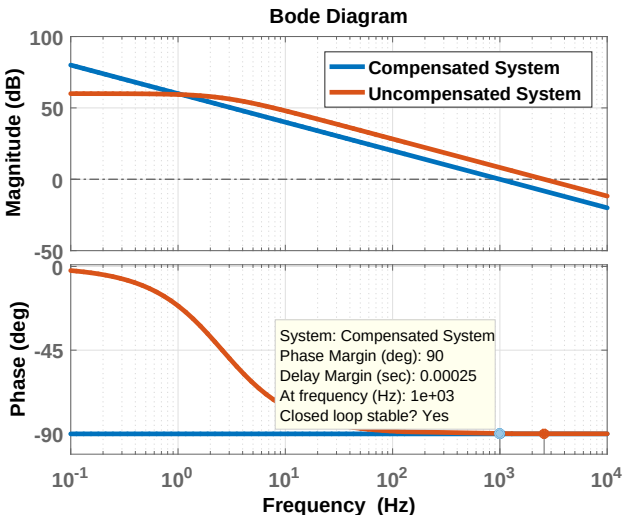
3.4 AFR Based DC Generation System

3.4.1 Selection of Reference Frame

Selection of reference frame is important to implement the AFR based dc generation system. The reference frame should be synchronously rotating to make the control parameters dc quantities in the steady-state, thus enabling easier controllability. As a result, RRF or SFRF might be the feasible reference frames.



3.12(a)



3.12(b)

Fig. 3.12: Bode plot of the uncompensated and compensated system of (a) voltage control loop and (b) current control loop.

Operation at RRF

At RRF, the torque (T) is given by:

$$T = 3p\frac{i^r_{qs}\lambda^r_{ds} - i^r_{ds}\lambda^r_{qs}}{4}. \tag{3.29}$$

The flux equation along d- and q- axis of RRF is given by:

$$\lambda^r_{ds} = -L_{ls}i^r_{ds} + L_{md}(-i^r_{ds} + i'^r_{fd} + i'^r_{kd}), \tag{3.30}$$

$$\lambda^r_{qs} = -L_{ls}i^r_{qs} + L_{mq}(-i^r_{qs} + i'^r_{kq1} + i'^r_{kq2}). \tag{3.31}$$

At no-load condition $i^r_{qs} = 0$, hence $\lambda^r_{qs} = 0$ and $v_T = e_T = 690$ V (Table 3.1). The λ^r_{ds} is given by:

$$|e_T| = \omega_r\lambda^r_{ds} \implies \lambda^r_{ds} = \frac{|e_T|}{\omega_r}, \tag{3.32a}$$

$$\lambda^r_{ds} = \frac{690.\sqrt{2}}{\sqrt{3}.377} \implies \lambda^r_{ds} = 1.49\ Wb. \tag{3.32b}$$

By neglecting the damper winding currents (i'^r_{kd}, i'^r_{kq1}, i'^r_{kq2}) and setting $i^r_{ds} = 0$, λ^r_{ds} can be regulated by the field current, i'^r_{fd}, while the torque can be controlled by varying i^r_{qs}. In

such a case, the torque equation becomes:

$$T = 3p\frac{i^r_{qs}\lambda^r_{ds}}{4} = 3p\frac{i^r_{qs}L_{md}i^{'r}_{fd}}{4}. \tag{3.33}$$

The power equation at RRF becomes:

$$P = 3p\frac{i^r_{qs}\lambda^r_{ds}}{4}\omega_r. \tag{3.34}$$

As per the proposed control strategy, at steady state $i^r_{ds} = i^{r*}_{ds} = 0$. Hence, the stator flux is given as:

$$\lambda^r_{qs} = -(L_{ls} + L_{mq})i^r_{qs}, \tag{3.35a}$$

$$\lambda^r_{ds} = L_{md}.i^{'r}_{fd}. \tag{3.35b}$$

Hence λ^r_{ds} $(= L_{md}.i^{'r}_{fd})$ can be maintained constant by adjusting field current $i^{'r}_{fd}$ which is controlled by field voltage e_F. Hence, estimation of λ^r_{ds} is required for proper flux control. Estimation of machine flux, λ^s_{ds} and λ^s_{qs} is computed in stationary reference frame (SRF) which is carried out by:

$$\lambda^s_{ds} = \int (v^s_{ds} + i^s_{ds}r_s)\ dt, \tag{3.36a}$$

$$\lambda^s_{qs} = \int (v^s_{qs} + i^s_{qs}r_s)\ dt, \tag{3.36b}$$

the machine flux, λ_s is given by:

$$|\lambda_s|^2 = {\lambda^s_{ds}}^2 + {\lambda^s_{qs}}^2. \tag{3.36c}$$

In the RRF, the λ^r_{ds} $(= i^r_{fds}.L_{md})$ can be estimated by:

$$(\lambda^r_{ds})_{est} = \sqrt{|\lambda_s|^2 - ((L_{ls} + L_{mq}).i^r_{qs})^2}. \tag{3.37}$$

In this control at RRF, λ^r_{ds} is maintained at nominal value i.e. 1.49 Wb for all the loading conditions.

Limitations of Operation at RRF

(i) **Ineffective Decoupling of Flux Components:** Although the $d-$ axis flux and $q-$ axis current could be controlled independently, the flux along $d-$ and $q-$ axes are not decoupled completely. This is because, the $d-$ axis flux is controlled by the field current while the $q-$axis flux is dependent on the $q-$axis current, which is illustrated below:

$$\lambda_{ds}^{r} = L_{md} i_{fd}^{'r}, \tag{3.38}$$

$$\lambda_{qs}^{r} = L_{mq} i_{qs}^{r}. \tag{3.39}$$

At RRF, $i_{fd}^{'r}$ will try to keep λ_{ds}^{r} constant. However, an increase in load will increase i_{qs}^{r} which will further increase λ_{qs}^{r} as per (3.39). Thus, the total machine flux, $\lambda_s = \sqrt{\lambda_{ds}^{r} + \lambda_{qs}^{r}}$, also increases with increase in load.

(ii) **Selection of Terminal DC Voltage:** In RRF, output terminal voltage (v_t) at steady-state is given by:

$$v_t^2 = (v_{ds}^{r})^2 + (v_{qs}^{r})^2, \tag{3.40}$$

Using (3.40) and neglecting resistance and leakage inductance, the voltage equation becomes

$$\begin{aligned} {v_t}^2 &= \omega_r^2 {\lambda_{ds}^{r}}^2 + \omega_r^2 {\lambda_{qs}^{r}}^2, \\ &= (\omega_r L_{md} i_{fd}^{'r})^2 + (\omega_r L_{mq} i_{qs}^{r})^2, \\ &= (\omega_r L_{md} i_{fd}^{'r})^2 \left(1 + \frac{L_{mq}^2 {i_{qs}^{r}}^2}{L_{md}^2 {i_{fd}^{'r}}^2}\right). \end{aligned} \tag{3.41a}$$

The no-load voltage e_T is given by $e_T = \omega_r \lambda_{ds}^{r} = \omega_r L_{md} i_{fd}^{'r}$, the expression of v_T becomes

$${v_T}^2 = {e_T}^2 \left(1 + \frac{L_{mq}^2 {i_{qs}^{r}}^2}{L_{md}^2 {i_{fd}^{'r}}^2}\right). \tag{3.41b}$$

The terminal voltage equation in p.u. becomes:

$$|v_{t(p.u.)}| = \sqrt{1 + \frac{L_{mq_{p.u.}}^2 {i_{qs_{p.u.}}^{r}}^2}{L_{md_{p.u.}}^2 {i_{fd_{p.u.}}^{r}}^2}}. \tag{3.42}$$

From the specification of the machine in Table 3.1, the base current is calculated as $I_{base} = 1713\ A$. From (3.34), $i_{qs_{p.u.}}^{r} = 1.42\ p.u.$. From the flux control strategy, the

field current is maintained at nominal value, hence $i^r_{fd_{p.u.}} = 1.0\ p.u.$ Due to the saliency of the synchronous machine, the ratio of $\frac{L_{mq}}{L_{md}}$ lies between 0.5 to 0.8. From Table I, $\frac{L_{mq}}{L_{md}} = 0.56$, thus taking the value of 0.56, the terminal voltage becomes:

$$|v_{T(p.u.)}| = \sqrt{1 + 0.56^2 1.42^2} = 1.278\ p.u. \tag{3.43}$$

Hence, if the no load voltage (e_T) is 690 V, then the output dc-link voltage at full load should be greater than:

$$|V_{t(p.u.)}| > 1.278.\sqrt{2}.690 > 1246\ V. \tag{3.44}$$

Considering the fact that the dc bus voltage should be more than 1246 V and by considering a voltage droop of 4%, the nominal dc bus voltage (V_{dc-nom}) should be at least 1500 V.

Thus, operating at RRF will result in increased operating flux and terminal voltage at higher loads thus requiring increased ratings of the interfaced AFE rectifier [15].

Operation at SFRF

It is thus inferred that selection of reference frame is crucial to implement the AFR based dc generation system. The flux is required to be decoupled at all operating scenarios and should preferably be controlled by the field exciter circuit. On the other hand, the torque output of WRSG could be controlled by the vector control operation of the AFE rectifier. As opposed to the operation at RRF, this is possible if the control is done at SFRF. The phasor diagram representing the various reference frames of WRSG is shown in Fig. 3.13. The torque equation of WRSG when the vector control is carried out at SFRF is shown as [147]:

$$T = 3p\frac{i_{Ts}\lambda_{Ms} - i_{Ms}\lambda_{Ts}}{4}. \tag{3.45}$$

The detailed operation is described in Section 3.4.2 and Section 3.4.3.

3.4.2 System Description of the Vector Control of WRSG at SFRF

The proposed AFR based dc generation system is illustrated in Fig. 3.14 where by theory, $\lambda_{Ts} = 0$ and $\lambda_{Ms} = |\lambda_s|$ (WRSG flux) when the control is done at SFRF ($M - T$ axis).

Further, the WRSG is operated at unity power factor by setting $i_{Ms} = 0$. Thus, with the mentioned objectives, the torque equation reduces to:

$$T = 3p\frac{i_{Ts}\lambda_{Ms}}{4}. \tag{3.46}$$

The output power or equivalently the output dc bus voltage is maintained by varying i_{Ts} according to varying load demand. λ_{Ms} or equivalently λ_s of WRSG is independently controlled by AFR based field excitation. The whole control framework can be divided into five major control blocks, as shown in Fig. 3.14, and are discussed below:

B1. Estimation of the phase voltages (v_{abc}) of WRSG is done by the dc-link voltage and the switching combination (S_{abc}) of the AFE rectifier [148].

B2. After v_{abc} is estimated, the angle to convert the control parameters into SFRF is computed. This angle (θ_s) is calculated by $\tan^{-1}(\lambda_\beta/\sqrt{\lambda_\alpha^2 + \lambda_\beta^2})$ where λ_α and λ_β are flux components in the α and β axes which are in stator reference frame (Fig. 3.13).

B3. The flux linkages per second in M-T axis (SFRF), i.e. ψ_{Ms} and ψ_{Ts}, are estimated utilizing θ_s computed in Step B2. By theory, $\psi_{Ts} = 0$, and the ψ_{Ms} ($= \psi_s$, WRSG flux linkages per second) is fed to the AFR based excitation control.

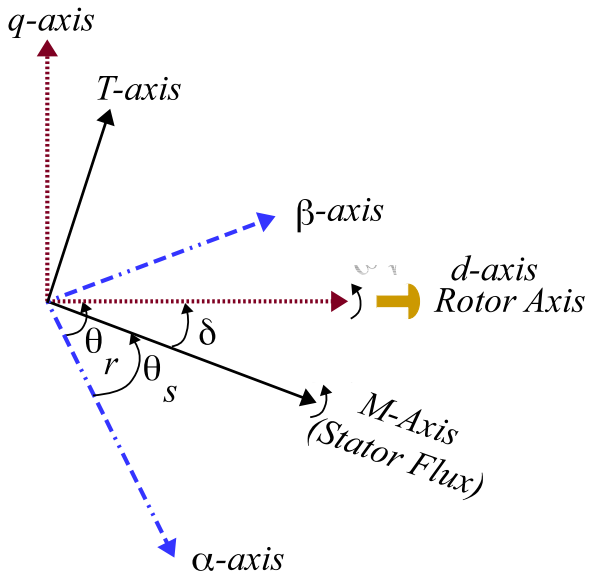


Fig. 3.13: Phasor diagram showing the relative orientation of $d-q$ and $M-T$ axes for WRSG.

B4. The AFR based excitation control maintains ψ_{Ms} or (equivalently λ_s) to a specified set-point defined by the user. This is maintained by varying the field current and field voltage in accordance with changing load angle (δ).

B5. The power control loop consists of voltage and current control loops. The design of these loops and the selected bandwidth are similar to the design presented in Section 3.3.2 with the only difference that the present control is done in $M-T$ axis. This loop is independent of the flux control by AFR in Step B4. The voltage loop (G_{vf}) is computed from the small signal analysis of the power balance equation in (3.47) and is illustrated in (3.48). The current loop transfer function is also shown in (3.48).

$$3p\frac{i_{Ts}\lambda_{Ms}}{4}\omega_r = C\frac{dv_{dc}}{dt}v_{dc} + v_{dc}i_o. \tag{3.47}$$

$$G_{vf}(s) = \frac{3}{4}\frac{p\lambda_{Ms}\omega_r}{sCV_{dc}+I_o}; \qquad G_{cf}(s) = \frac{1}{R_s+sL_s}. \tag{3.48}$$

3.4.3 Control Loop Derivation of AFR Based WRSG Field Excitation System

One of the objective of AFR is to control the stator flux (λ_s) by a field excitation circuit, which can equivalently be achieved by regulating the stator flux linkage per second, $\psi_s(=\psi_{Ms})$, to the desired value. The voltage equations of WRSG in terms of flux linkages/second in $M-T$ frame is illustrated as [147]:.

$$v_{Ms} = -r_s i_{Ms} - \frac{\omega_r}{\omega_b}\psi_{Ts} + \frac{1}{\omega_b}\frac{d}{dt}\psi_{Ms}, \tag{3.49a}$$

$$v_{Ts} = -r_s i_{Ts} + \frac{\omega_r}{\omega_b}\psi_{Ms} + \frac{1}{\omega_b}\frac{d}{dt}\psi_{Ts}, \tag{3.49b}$$

and the WRSG terminal voltage v_t is given by:

$$v_t^2 = v_{Ms}^2 + v_{Ts}^2, \tag{3.49c}$$

where, v_{Ms} and v_{Ts} are phase voltages, i_{Ms} and i_{Ts} are line currents, ψ_{Ms} and ψ_{Ts} are flux linkages per second in M-T axis. r_s is WRSG stator resistance, ω_b and ω_r are base speed and

generator speed respectively. As ψ_{Ms} = constant and $\psi_{Ts} = 0$ in M-T axis, by neglecting r_s, the equation of terminal voltage becomes:

$$v_t^2 = v_{Ms}^2 + v_{Ts}^2, \tag{3.50a}$$

$$v_t^2 = \left(\frac{1}{\omega_b}\frac{d}{dt}\psi_{Ms}\right)^2 + \left(\frac{\omega_r}{\omega_b}\psi_{Ms}\right)^2, \tag{3.50b}$$

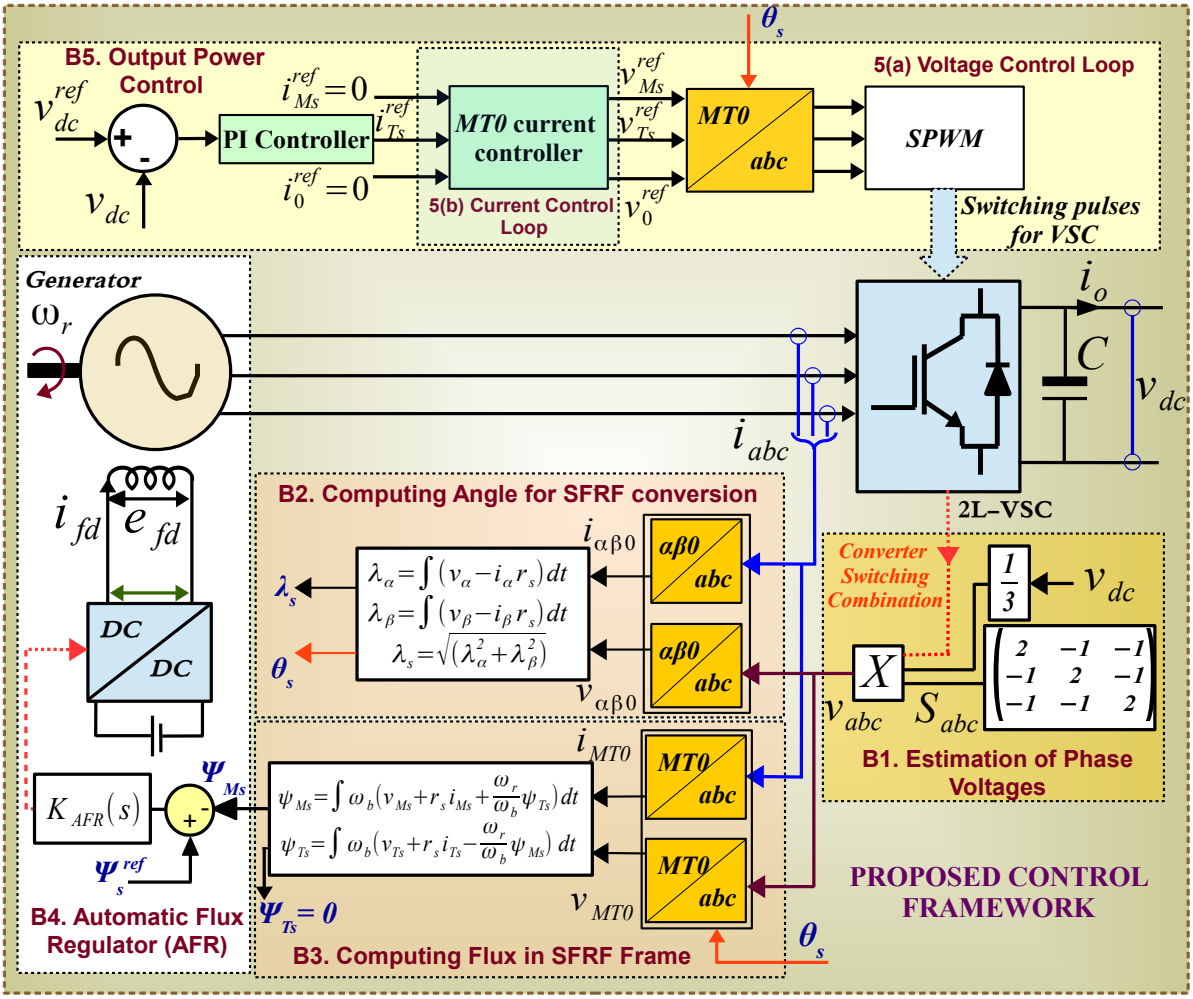


Fig. 3.14: Overview of the vector control of WRSG drive for dc bus voltage control and AFR for WRSG control.

where, $\psi_{Ms} = \psi_s$. Thus, by applying small signal analysis to (3.50b), the relation between ψ_{Ms} and v_t can be found out.

$$(V_t + \hat{v}_t)^2 = \Big(\frac{1}{\omega_b}\frac{d}{dt}(\Psi_{Ms} + \hat{\psi}_{Ms})\Big)^2 + \Big(\frac{\omega_r}{\omega_b}(\Psi_{Ms} + \hat{\psi}_{Ms})\Big)^2, \tag{3.51a}$$

$$\frac{d}{dt}(\Psi_{Ms} + \hat{\psi}_{Ms}\Big) = \omega_b(V_t + \hat{v}_t)\sqrt{1 - \left(\frac{\omega_r(\Psi_{Ms} + \hat{\psi}_{Ms})}{\omega_b(V_t + \hat{v}_t)}\right)^2}. \tag{3.51b}$$

The RHS of (3.51b) is of the form $A_k(1-x)^{1/2}$ which can be expanded binomially and linearised by neglecting higher order terms to obtain:

$$\frac{d}{dt}(\Psi_{Ms} + \hat{\psi}_{Ms}\Big) \approx \omega_b(V_t + \hat{v}_t)\left(1 - \frac{1}{2}\left(\frac{\omega_r(\Psi_{Ms} + \hat{\psi}_{Ms})}{\omega_b(V_t + \hat{v}_t)}\right)^2\right). \tag{3.51c}$$

Expanding (3.51c) and neglecting higher order terms:

$$\frac{d}{dt}\hat{\psi}_{Ms} \approx 2\omega_b\hat{v}_t - \frac{\omega_r^2}{\omega_b}\frac{\Psi_{Ms}}{V_t}\hat{\psi}_{Ms}. \tag{3.52a}$$

Applying Laplace transform:

$$s\psi_{Ms}(s) \approx 2\omega_b v_t(s) - \frac{\omega_r^2}{\omega_b}\frac{\Psi_{Ms}}{V_t}\psi_{Ms}(s). \tag{3.52b}$$

Re-arranging the terms, the relation between $\psi_{Ms}(s)$ $(= \psi_s(s))$ and $v_t(s)$ is shown as:

$$\frac{\psi_s(s)}{v_t(s)} \approx \frac{\omega_b}{\frac{1}{2}s + \frac{1}{2}\frac{\omega_r^2}{\omega_b}\frac{\Psi_s}{V_t}}. \tag{3.52c}$$

This relation between $\psi_s(s)$ and $v_t(s)$ will be used to determine the plant transfer function and to design the controller of the AFR based field excitation system. The AFR based controller is implemented as shown in B4 block of Fig. 3.14. The schematic for the AFR based WRSG control is depicted in Fig. 3.15 where the Ψ_s is maintained at the desired setpoint Ψ_s^{SP} dependent on the $G_{AFR}(s)$. $G_{AFR}(s)$ is determined by the plant transfer function of generator, exciter and $D(s)$ as analyzed in Section 3.5.

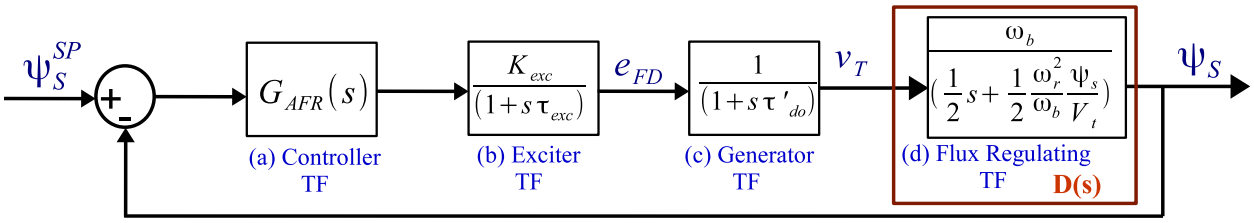


Fig. 3.15: Functional block diagram of the field excitation circuit in the proposed AFR based control.

3.5 Controller Response Analysis

In the dc generation system, the aim of both AVR and AFR based field excitation system is to regulate the operating flux of the WRSG within the prescribed operating limits. AVR does this by maintaining the terminal voltage of WRSG against speed dependent setpoint whereas the AFR does this by regulating the WRSG flux to its rated value, which is described in Section 3.3 and Section 3.4, respectively. In this section, a comparative analysis of the AFR with AVR based field excitation is carried out to support its effectiveness and highlight its potential benefits.

3.5.1 Controller Design and Frequency Response Analysis

One of the prime difference between the control structure of the AVR and AFR based excitation system is the need of additional transfer function $D(s)$ (in (3.53)) in the AFR based system as marked in Fig. 3.15.

$$D(s) = \frac{\omega_b}{\frac{1}{2}s + \frac{1}{2}\frac{\omega_r^2}{\omega_b}\frac{\Psi_s}{V_t}} \tag{3.53}$$

$G_{AVR}(s)$ and $G_{AFR}(s)$ shown in Fig. 3.9 and 3.15 are the controllers of the AVR and AFR which are used to maintain the terminal voltage and machine flux, respectively, at defined setpoints and within the required bandwidth. As per, IEEE Std 421.2, bandwidth of 5 Hz is chosen for the field regulating applications. Conventionally, $G_{AVR}(s)$ and $G_{AFR}(s)$ are modeled by proportional controllers (P-controllers) to maintain the desired bandwidth, which will have persistent steady-state errors. Thus, in addition to the P-controller, the K-factor based controller is also considered which is based on the pole-zero placement technique [149].

Table 3.5: Controller Transfer Functions for AVR and AFR System

Control	**AVR** $\left(G_{AVR}(s)\right)$	**AFR** $\left(G_{AFR}(s)\right)$
Proportional Control	$\dfrac{124}{1+0.001s}$	$\dfrac{63}{1+0.001s}$
K-factor Control	$\dfrac{77.18}{s}\left(\dfrac{1+s/31.42}{1+s/161.97}\right)$	$\dfrac{28.38}{s}\left(\dfrac{1+s/0.45}{1+s/217.96}\right)$

In this way, steady-state and transient responses could be studied when the type of controllers are altered. The general structure of the P-controller is:

$$G_{AVR_P}(s) = \frac{K_P}{1+s\tau_P}, \tag{3.54}$$

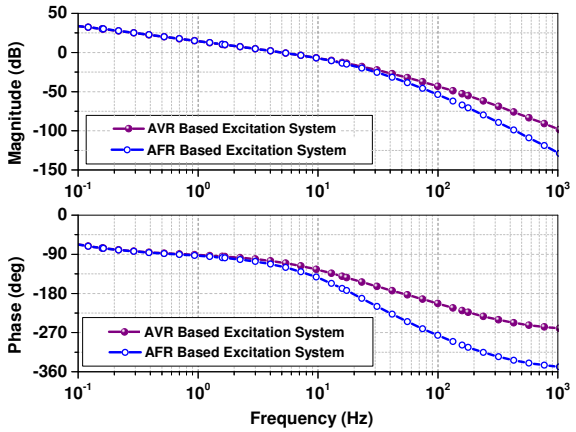
where, K_P is the gain and τ_P is the time-constant of the amplifier. Generally, τ_P is very small constant value while K_P is adjusted to obtain the desired bandwidth. On the other hand, the general structure for the K-factor based controller is:

$$G_{AVR_K}(s) = \frac{K_K}{s}\left(\frac{1+s/\omega_z}{1+s/\omega_p}\right). \tag{3.55}$$

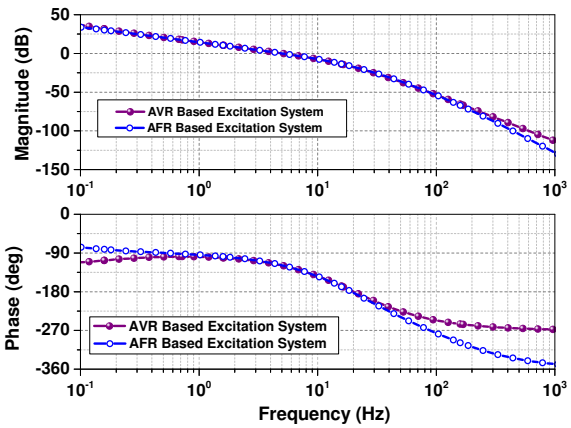
In such controllers the gain K_K, pole ω_p and zero ω_z could be adjusted to obtain the desired bandwidth and phase margin. For a fair comparison, bandwidth of both AVR and AFR have been fixed at 5 Hz. The controller transfer functions for AVR and AFR are shown in Table 3.5. Bode plots of both systems are compared in Fig. 3.16. It can be observed that the responses of both AVR and AFR are similar in the low frequency region. Due to the presence of $D(s)$, the gain and phase margin of AFR are lesser than AVR but within permissible limits. The frequency-domain metrics for such normal operating conditions are presented in Table 3.6.

3.5.2 Step Response Analysis

Fig. 3.17 compares the step response of the closed-loop voltage control for AVR and closed-loop flux control for AFR based field excitation system. As the bandwidth of both systems is kept same, the rise times are reasonably comparable. Although other parameters such as peak amplitude of AFR is different from AVR but are within permissible limits as prescribed by IEEE Std 421.2 [134]. The time-domain metrics for such normal operation are depicted in Table 3.6.

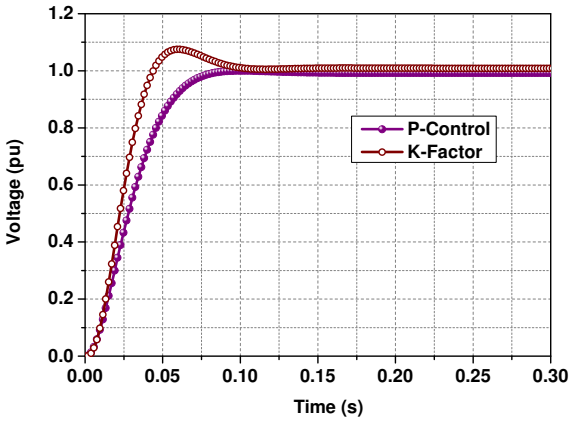


3.16(a)

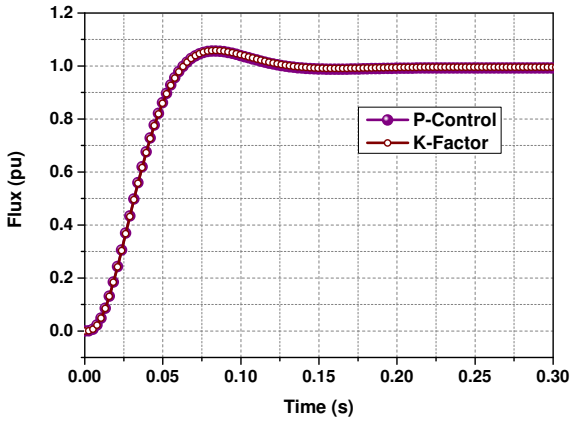


3.16(b)

Fig. 3.16: Comparison of the bode plot of AVR and AFR based excitation system for (a) P-control and (b) K-factor based control.



3.17(a)



3.17(b)

Fig. 3.17: Comparison of the step response of (a) AVR and (b) AFR based field excitation system using both P-control and K-factor based control.

3.5.3 Response to Change in Parameters and Operating Limits

$G_{AVR}(s)$ and $G_{AFR}(s)$ are designed considering the plant transfer functions of exciter and WRSG. Inaccurate determination of the plant transfer functions might adversely effect the field regulating operation. To test robustness and operating capabilities of the AVR and AFR based field excitation system, system parameters such as K_{exc} and τ_{exc} of the exciter and τ'_{do} of WRSG are varied [150]. Time-domain, frequency-domain and stability performance metrics are monitored, which are shown in Table 3.6. It is observed that the AFR based

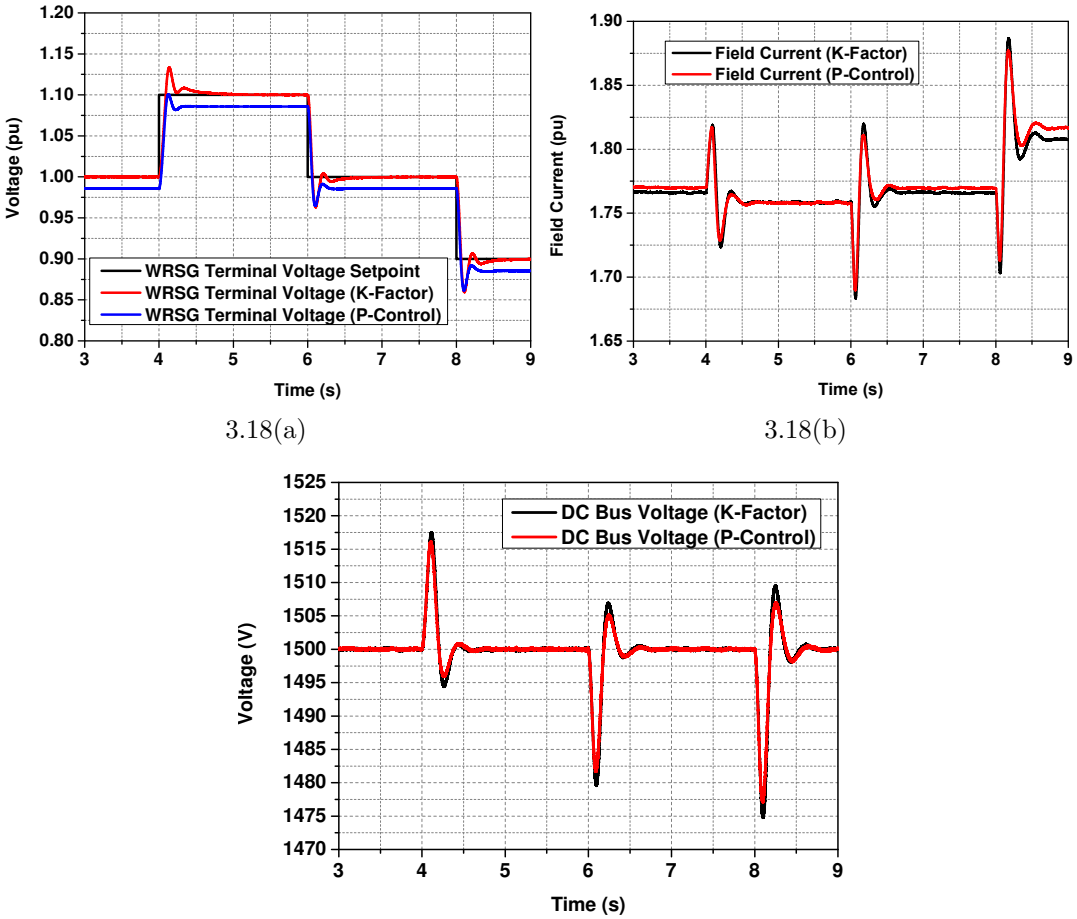
Table 3.6: Performance Metrics of AVR and AFR based Field Excitation System to Varying System Parameters

Conditions	**Parameters**		**AVR Based System**		**AFR Based System**	
			P-Control	K-Factor	P-Control	K-Factor
Normal Operating Conditions	Time Domain Parameters	Rise Time (s)	0.0455	0.0385	0.0403	0.0372
		Settling Time (s)	0.0718	0.1271	0.1054	0.1233
		Overshoot (%)	0.7973	7.5146	2.99	8.45
		Undershoot (%)	0	0	0	0
	Frequency-Domain Parameters	Gain Margin (dB)	33.3637	7.7131	9.91	5.58
		Phase Margin (deg)	71.1844	60.7919	66.17	59.26
		Bandwidth (Hz)	5.01	5.03	5.06	5.00
	Stability Limits	Gain (K)	4137	595	624	158
50% Increase in both Exciter Time Constant and Gain	Time Domain Parameters	Rise Time (s)	0.0443	0.0395	0.0281	0.0284
		Settling Time (s)	0.1284	0.1403	0.1492	0.1524
		Overshoot (%)	5.174	13.936	18.99	18.48
		Undershoot (%)	0	0.77	3.63	3.61
	Frequency-Domain Parameters	Gain Margin (dB)	32.39	6.72	6.25	6.26
		Phase Margin (deg)	64.46	54.37	49.21	49.21
		Bandwidth (Hz)	4.79	4.81	6.72	6.69
	Stability Limits	Gain (K)	4017	571	393	118
50% Reduction of both Exciter Time Constant and Gainn	Time Domain Parameters	Rise Time (s)	0.0527	0.0407	0.1093	0.1152
		Settling Time (s)	0.0962	0.0652	0.2018	0.2018
		Overshoot (%)	0	1.6129	0	0
		Undershoot (%)	0	0	0	0
	Frequency-Domain Parameters	Gain Margin (dB)	36.35	10.6746	22.91	23
		Phase Margin (deg)	79.34	68.71	82.65	82.35
		Bandwidth (Hz)	5.19	5.2	2.65	2.64
	Stability Limits	Gain (K)	4507	647	1443	240
50% Increase in τ'_{do}	Time Domain Parameters	Rise Time (s)	0.0754	0.0611	0.0676	0.0691
		Settling Time (s)	0.1339	0.1892	0.1178	0.1232
		Overshoot (%)	0	2.2518	0	0
		Undershoot (%)	0	0	0	0
	Frequency-Domain Parameters	Gain Margin (dB)	49.99	11.55	14.85	14.90
		Phase Margin (deg)	77.08	68.89	73.61	73.43
		Bandwidth (Hz)	3.42	3.47	3.47	3.45
	Stability Limits	Gain (K)	6200	894	935	239
50% Reduction in τ'_{do}	Time Domain Parameters	Rise Time (s)	0.0221	0.021	0.0203	0.0205
		Settling Time (s)	0.0734	0.1552	0.109	0.1128
		Overshoot (%)	11.05	27.74	19.83	18.92
		Undershoot (%)	1.2	8.1	4.72	4.7
	Frequency-Domain Parameters	Gain Margin (dB)	16.73	3.87	4.97	4.99
		Phase Margin (deg)	57.44	41.76	48.73	48.76
		Bandwidth (Hz)	9.1	8.87	9.1	9.1
	Stability Limits	Gain (K)	2074	296	313	78

system offers similar characteristics than the AVR based system.

3.6 Operational Analysis

With reference to the modeling and control framework developed in Sections 3.3, 3.4 and 3.5; this section presents the operation of both AVR and AFR based dc generation system. This



3.18(a) 3.18(b)

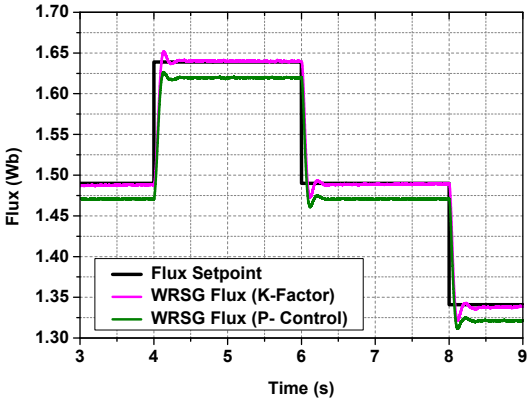
3.18(c)

Fig. 3.18: (a) WRSG terminal voltage, (b) WRSG field current and (c) dc-link voltage for P-control and K-factor based $G_{AVR}(s)$ with step change in WRSG terminal voltage setpoint.

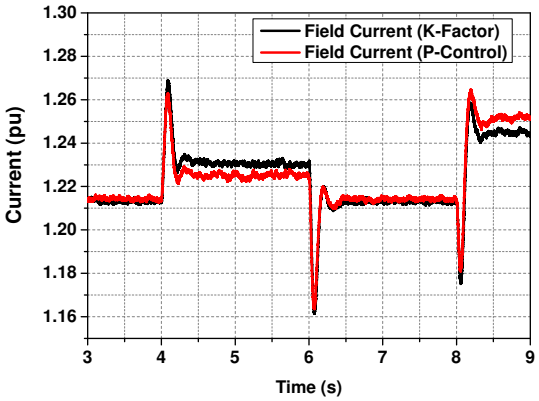
operation has been validated with the OPAL-RT OP5600 based HIL real-time simulation platform [4, 151]. The marine loads and contingencies have been tested for both types of generation systems for detailed one-to-one comparison.

3.6.1 Output with Step Change in Set-point of Control Parameter

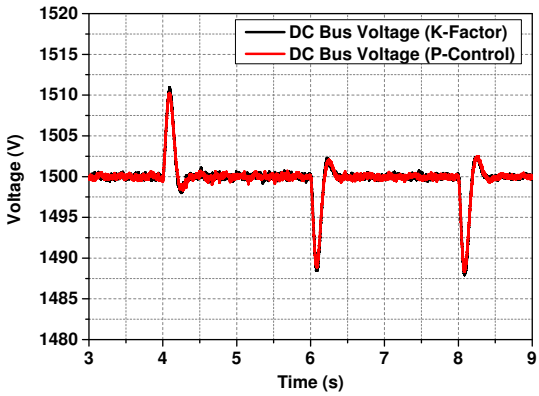
Step change in the terminal voltage (for AVR) and flux set-points (for AFR) are changed from 1.0 pu to 1.1 pu at 4 s and to 0.9 pu at 8 s to study its impact on the field current requirements and output dc bus voltage. The results are shown in Fig. 3.18 and 3.19 respectively. Both P-control and K-factor based controllers are implemented and compared. As expected, it is seen that there is a persistent steady-state error for proportional control while the control



3.19(a)



3.19(b)



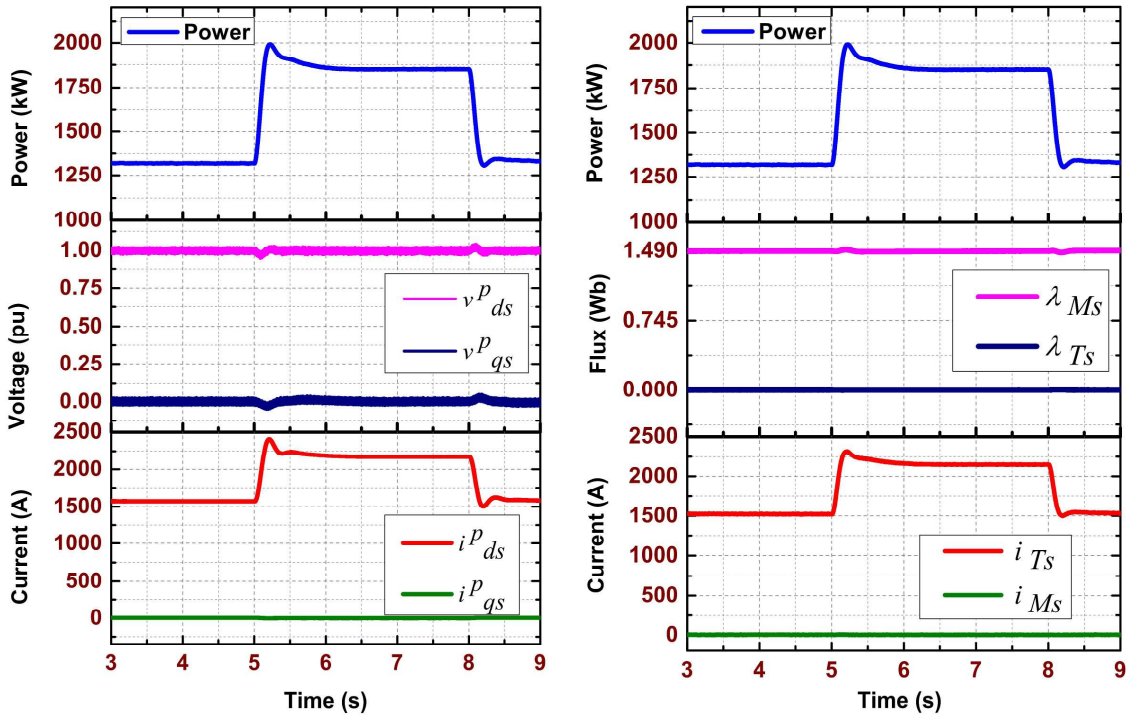
3.19(c)

Fig. 3.19: (a) WRSG flux, (b) WRSG field current and (c) dc-link voltage for P-control and K-factor based $G_{AVR}(s)$ with step change in WRSG flux setpoint.

variable closely follows the set-point for the K-factor based method. It can further be seen that the dc bus voltage is more sensitive to the step change in AVR control. The overshoot in the dc bus voltage for AVR is 1.17% while with AFR is 0.73%. In both cases the overshoot is within permissible limits according to the IEEE Std 421.2 [134].

3.6.2 Decoupling of the Control Parameters

For the AFR based control, ψ_{Ms} (or equivalently λ_{Ms}) should be decoupled from ψ_{Ts} (or λ_{Ts}). Similarly, decoupling of v_{ds}^{p} from v_{qs}^{p} is required for the AVR based control. For unity power factor i_M (in AFR) and i_q^p (in AVR) is maintained at zero. The control parameters must be de-coupled at all load condition and also during load change transients. This is shown by the load change operation as shown in Fig. 3.20. The generator output is varied



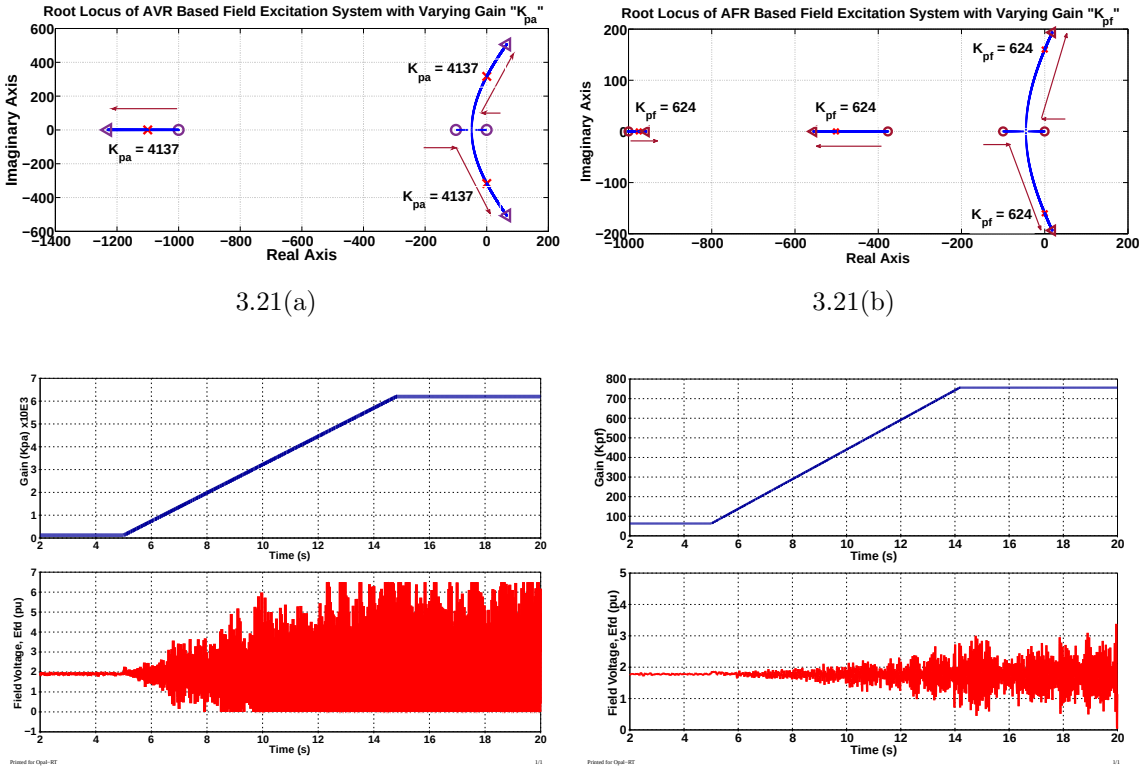
3.20(a) 3.20(b)

Fig. 3.20: (a) Decoupling of v^p_{ds} and v^p_{qs}; i^p_{ds} and i^p_{qs} for AVR based system and (b) decoupling of λ_{Ms} and λ_{Ts}; i_{Ms} and i_{Ts} for AFR based system when generator output is altered.

from 1300 kW to 1850 kW at 5 s and again restored to 1300 kW at 8 s. Fig. 3.20 shows the decoupled control parameters during this operation. The K-factor based control is used for both AVR and AFR based dc generation system.

3.6.3 Verifying the Stability Limits

The stability limits of both the AVR and AFR operating with P-control are primarily dominated by the selection of gains K_{pa} (for AVR) and K_{pf} (for AFR). Analysis of the root locus diagram in Fig. 3.21(a) shows that the gain K_{pa} increasing beyond 4137 leads to instability in the AVR control. This is evident from the study of the corresponding change in field voltage E_{fd} is shown in Fig. 3.21(c). The E_{fd} fluctuates from 0 pu to 6 pu when $K_{pa} > 4137$ making the AVR based control inoperable. Similarly, root locus diagram in Fig. 3.21(b) infers that the gain K_{pf} increasing beyond 624 would lead to instability in the AFR system. This is supported by the corresponding change in field voltage E_{fd} shown in Fig. 3.21(d). It can be



3.21(a) 3.21(b)

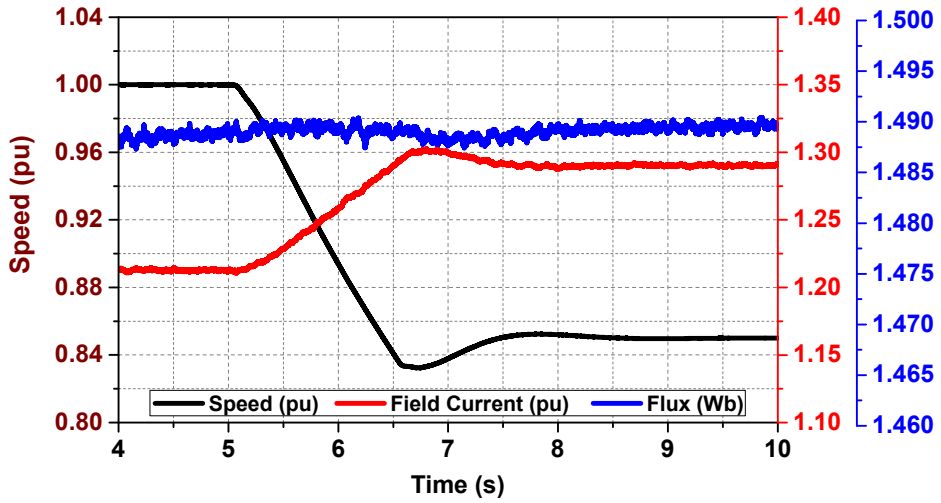
3.21(c) 3.21(d)

Fig. 3.21: Stability limits of the AVR and AFR based control with the variation of (a) K_{pa} and (b) K_{pf}; the variation of output field voltage while changing (c) K_{pa} for AVR and (d) K_{pf} for AFR.

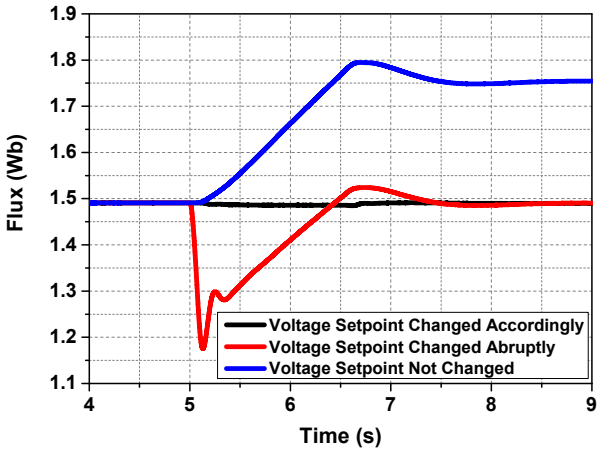
observed that for higher gains (K_{pf}> 624), E_{fd} fluctuates from 0.5 pu to 3.5 pu making the AFR based excitation control inoperable.

3.6.4 Operation during Variable Speed

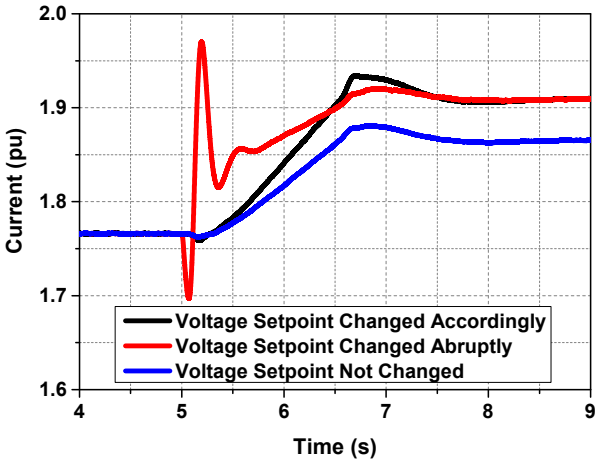
The dc marine vessels are expected to integrate the variable speed DGs. During such operation, the operating parameter such as the machine flux of the interfaced WRSG should be maintained at nominal values. For AVR based system, the terminal voltage set-point of WRSG should be altered continuously with the operating speed so that constant v_t/f ratio is maintained and machine flux does not reach the saturation region. On the other hand, in the AFR based WRSG, machine flux is directly regulated at the desired setpoint without the need of any set-point variation as compared to the AVR based system. This is a major



3.22(a)



3.22(b)



3.22(c)

Fig. 3.22: (a) WRSG flux and field current when the operating speed of DG is reduced from 1 pu to 0.85 pu at 5 s for AFR based dc generation system. Variation of (b) WRSG flux and (c) field current requirement when operating speed is reduced from 1 pu to 0.85 pu at 5 s for AVR based dc generation system and when terminal voltage setpoint is unchanged, abruptly changed and varied in according to the WRSG speed.

advantage of the AFR based generation system. This operation is shown in Fig. 3.22 when the speed is changed from 1 pu to 0.85 pu at 5 s.

For AFR based system in Fig. 3.22(a), WRSG flux is maintained at desired setpoint (1.49 Wb) while the field current increases to regulate the flux at lower speed. For the AVR based system the WRSG terminal voltage setpoint is changed according to the WRSG operating

speed. With the changing speed, the WRSG terminal voltage setpoint is changed from 1 pu to 0.85 pu as shown in Fig. 3.22(b) and 3.22(c). When the setpoint is changed abruptly from 1 pu to 0.85 pu, there is a transient effect in the field current and the machine flux. However, if the voltage setpoint is altered for every operating speed, the transient effect in WRSG field current and flux is minimized.

3.6.5 Operation during Fault Conditions

A fault resistance of 0.01 Ω is introduced at the terminals of AFE rectifier for both AFR and AVR based dc generation systems when they were delivering 2000 kW power to study the response of the field excitation circuit and the output fault current. For both cases, the field voltage E_{fd} rises to the maximum upper limit (Fig. 3.23) which is set as per IEEE Std 421.2 [6, 134]. The initial fault current due to capacitor discharge is equal at 12 kA for both cases. The ac fault current delivered by the WRSG in case of AVR based system is limited by the filter inductor, hence it is lower than the AFR based system which can be seen from Fig. 3.23(b, d).

3.7 Summary

This chapter investigates the suitability of AFR based excitation control of the WRSG for the application in the dc generation system for emerging marine vessels. The efficacy of the proposed method is supplemented by the comparative analysis with the conventional AVR based field excitation control. This study would be helpful in the development and selection of the type of field excitation system to control the WRSG for such applications. Detailed modeling for both systems is performed which substantiates the suitability of the AFR based dc generation system in the emerging dc marine vessels. Based on the operation and control of the AVR and AFR based dc generation system, the following discussions are remarked:

(i) Conventionally, the generation system in traditional ac marine vessels is based on AVR based field excitation system, which is dependent on the measurement of the terminal voltage of WRSG. However, in the 2L-VSC based dc generation system, the terminal voltage can only be measured by employing a tuned LC filter, which increases the space and weight requirements and further increases the cost. Contrarily, the proposed AFR

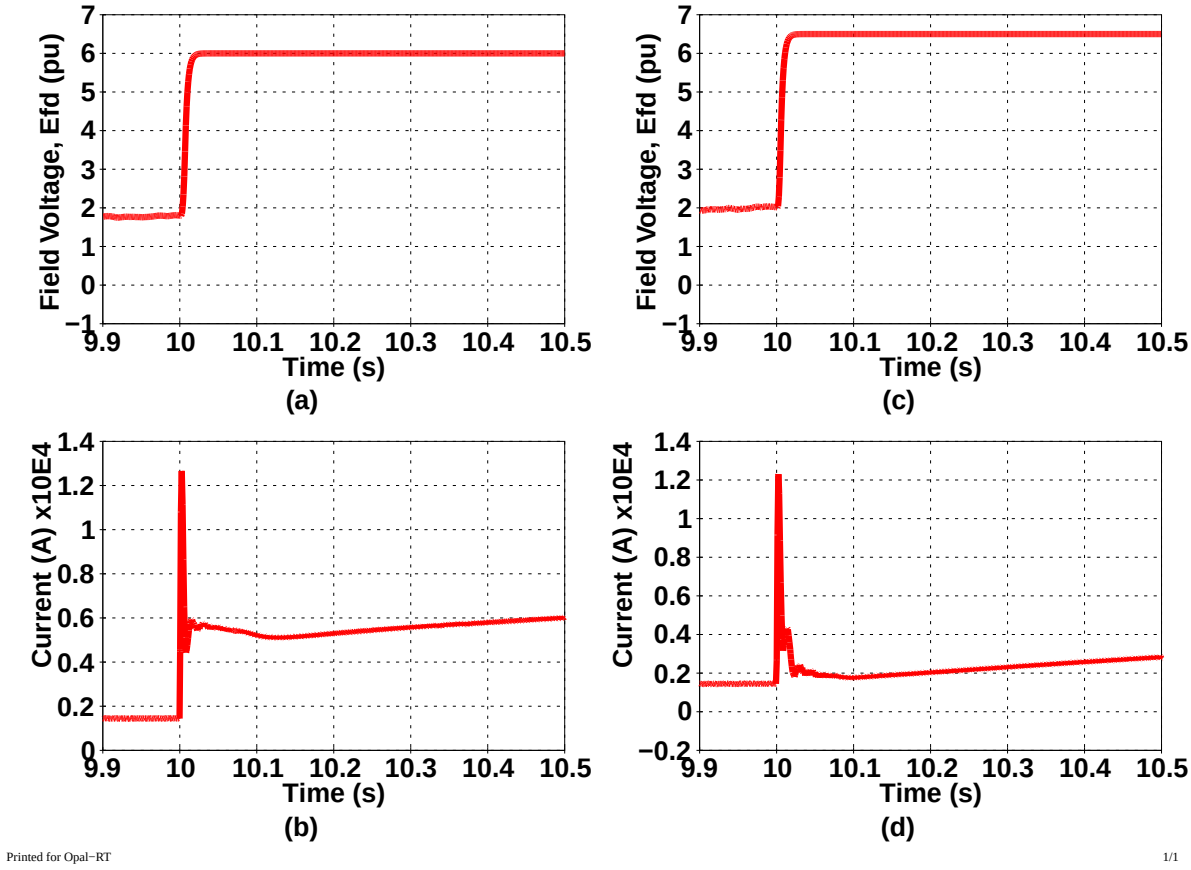


Fig. 3.23: (a) Field voltage & (b) dc fault current for the AFR based system and (c) field voltage & (d) dc fault current for AVR based system.

based control does not require the measurement of terminal voltage thus not requiring an additional LC filter. This is the principal advantage of the AFR based dc generation system as compared to the AVR one. This reduces the complexity of the control, helps in restricting the size and space requirements and avoids the need of additional cooling requirements for the filter during full load conditions.

(ii) AVR regulates the terminal voltage while AFR maintains the WRSG flux. Thus, the modeling and derivation of the required '*terminal voltage to flux*' transfer function and control loop design for the field excitation circuit have been derived for the AFR based dc generation system. This was the prime research gap in the existing literature. This design has been done analogously to the AVR based field excitation system.

(iii) DC-link voltage control for the AVR based dc generation system is carried out by the vector control operation of the interfaced AFE rectifier at PLL reference frame. This is done by considering the WRSG and interfaced LC filter as weak grid network. It serves as a base model and is used for comparison with the AFR based dc generation system. The dc-link voltage control for AFR system is done by vector control operation of the WRSG fed AFE rectifier at SFRF.

(iv) Controller response analysis with the emphasis on the variation of system parameters in both AVR and AFR yields similar results. This makes AFR a suitable alternative to the AVR based dc generation system. The AFR based dc generation system is evidently promising, which is supported by the stability analysis and the detailed comparative analysis with AVR based dc generation in both time- and frequency- domain.

Table 3.7: AVR vs AFR based dc Generation System

Parameter	**AVR based dc Generation System**	**AFR based dc Generation System**
WRSG Excitation Control Parameter	Terminal Voltage (v_T)	Flux Linkage per second (ψ_s) / Flux (λ_s)
Reference Frame for WRSG & AFE converter control	As per PLL	Stator Flux Reference Frame
De-coupling Parameters	i^p_{ds} and i^p_{qs}; v^p_{ds} and v^p_{qs}	i_{Ms} and i_{Ts} ; ψ_{Ms} and ψ_{Ts}
Additional Requirements	Need of LC filter	Need of converter switching combinations
Footprint	More due to LC filter	Expected to be less
Losses	More for passive damping based LC filter	Expected to be less
Variable Speed Operation	Manual change of voltage set-point	No change of set-point
Voltage Sensors	3 (ac) + 1 (dc)	1 (dc)
Cost	More due to additional voltage sensors, LC filters and cooling requirements	Lesser than AVR due to direct connection of WRSG with VSC resulting in less number of voltage sensors and LC filters

(v) AFR directly regulates the WRSG flux, thus changing the speed of WRSG would not effect the operating parameters. However, AVR requires the v_T^{SP} to be varied in according to the changing speed. It is seen that the abrupt change of v_T^{SP} results in transient variation of the WRSG flux and field current. As a result, it is required that v_T^{SP} has to be altered at every operating speed for smoother operation. Thus, additional arrangements are needed to provide the speed dependent v_T^{SP}.

(vi) It is observed that for similar loading condition field current requirement for AFR based dc generation system is more than that of AVR based dc generation system. This is because the AVR based control is done at PLL reference frame and AFR based control is done at SFRF. When converted into RRF, the d-axis current (in RRF) is higher in the case of the AVR based control. Thus higher field current is needed to counter this d-axis current and also to establish the WRSG flux. Therefore, the AFR based system would require lower rated field circuit as compared to the AVR based system. This becomes an additional advantage of using AFR based dc generation system.

With regards to the discussion, the comparison of both types of dc generation system is illustrated in Table 3.7.

Chapter 4

Modeling, Control and Fuel-Efficient Operation of DC PSV

4.1 Introduction

Development of integrated power system (IPS) for shipboard applications has enabled the marine loads such as the propulsion systems to be powered from the common generation units which has been discussed in detail in Chapter 2. This has resulted in reduction of the number of installed prime-movers and offered designers flexibility to place the generation system at any suitable location. In Chapter 3, AFR based modeling and control framework of the WRSG based dc generation system was presented. This dc generation system is compact in size and will be used to develop the dc PSV in this chapter. This chapter focuses on the modeling and control of the components of the dc PSV and reduction of the specific fuel oil consumption (SFOC) of the generation system for various operating conditions. This is primarily achieved by operating the interfaced diesel generator (DG) at the optimized speed according to the load demand. Fuel efficient operation of the generation systems in marine vessel is a relatively new topic with limited number of research attempts made in

The results of this chapter have been partially published in:

(i) **K. Satpathi**, V. M. Balijepalli, and A. Ukil, "Modeling and real-time scheduling of DC platform supply vessel for fuel efficient operation," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 3, pp. 762-778, Sep. 2017.

(ii) **K. Satpathi**, A. Ukil, N. Thukral and M. A. Zagrodnik, "Modeling of DC shipboard power system," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

this area. Most of the work has been reported in the domain of ac marine vessels, such as application of the shaft generator system (SHG) integrated with the DGs [2], agent based real-time load management to control the loads [152], and stochastic approaches [14].

4.2 Contributions of the Chapter

The main contribution of this chapter is to provide a conceptual basis for implementing a real-time simulation model with generation scheduling for different operating conditions. The major contributions are:

- Real-time simulation framework for the entire dc shipboard system has been developed in this chapter. Modeling and control of the various components of marine vessels such as the DG based generation systems, energy storage systems (ESS), propulsion loads, hotel loads, pulsed loads etc. are incorporated in a real-time simulator. The loading conditions have been simulated considering the realistic marine missions. Such real-time simulation framework is useful to analyze multiple test study scenarios.

- Real-time scheduling of the generation systems have been carried out for various operating conditions and different contingencies such as availability of generation systems, sudden load changes and network faults. Scheduling of the generation system is determined by the dc optimal power flow (OPF) algorithms utilizing reduced bus-bar model. SFOC of the DGs are minimized by operating them at optimized speed which is determined by the cost function.

- Dynamics of the full dc SPS have been studied during contingencies. Moreover, trajectory of SFOC of the DGs during various contingencies have been studied, which has been effectively realized by the real-time simulation platform.

The minor contributions of this chapter are:

- This chapter also considers the charging ESS by the onboard photovoltaic (PV) system. Design of PV for the target dc PSV is also described.

- This chapter also describes the possibility of SFOC minimization with an option of scheduling ESS at the sub-optimal points. It has been described with a case study.

4.3 Modeling of DC PSV

The bus-breaker model of the representative dc PSV is shown in Fig. 4.1. Such two-bus architecture has been chosen to improve the reliability and survivability of the vessel. This has been discussed in Chapter 2 and is coherent with the commercially available PSVs [153, 154]. The representative dc PSV comprises of four diesel engines (DEs) which are coupled with the WRSG ($\mathscr{P}^{DG}$) thus forming the DGs. It also comprises of one PV based ESS ($\mathscr{P}^{ESS}$). The total generation capacity can be illustrated by:

$$\mathbb{P}_{Gen} = \{\mathscr{P}^{DG\ n},\ \mathscr{P}^{ESS}\ ||\ n\ =\ 1:4\}. \tag{4.1}$$

DGs are interfaced with the dc bus by the two-level voltage source converter (2L-VSC) acting as an AFE rectifier. The PV based ESS is integrated with the dc bus via dc/dc converter. The nominal bus voltage of dc PSV is set at 1500 V which according to IEEE Std 1709-2010 falls under MVDC shipboard architecture [25]. As compared to the land based power systems, marine vessels have loads pertaining to different marine missions. Variable frequency propulsion system ($L_{propulsion}$) comprises of main propulsion (MP) systems to cater for the cruising loads ($\mathbb{L}^{CL}$); tunnel thrusters (TT) and retractable thrusters (RT) to cater for the DP load ($\mathbb{L}^{DP}$) [8]. The total connected propulsion load is illustrated as $L_{propulsion} = \{\mathbb{L}^{CL},\ \mathbb{L}^{DP}\}$. The fixed frequency hotel loads are required for air conditioning/lighting systems, cranes/winches, small hotel motors etc. The hotel loads are classified into high power ($\mathbb{L}^{HL_{high}}$) and low power ($\mathbb{L}^{HL_{low}}$) loads. The miscellaneous loads ($\mathbb{L}^{misc}$) for radar and pulsed load operation are also considered as it may form the integral part of modern PSVs. The hotel loads can be illustrated as $L_{hotel}\ =\ \{\mathbb{L}^{HL_{high}},\ \mathbb{L}^{HL_{low}},\ \mathbb{L}^{misc}\}$ and the total load L_{total} can be expressed as follows:

$$L_{total} = \{\mathbb{L}^{CL},\ \mathbb{L}^{DP},\ \mathbb{L}^{HL_{high}},\ \mathbb{L}^{HL_{low}},\ \mathbb{L}^{misc}\}. \tag{4.2}$$

The power rating of the components and converter systems are shown in Fig. 4.1. De-rating factor of 125% has been used for the selection of the converters, cables and bus-bars to cater for the short time overload demands. Modeling and control of various components are discussed in the subsequent subsections.

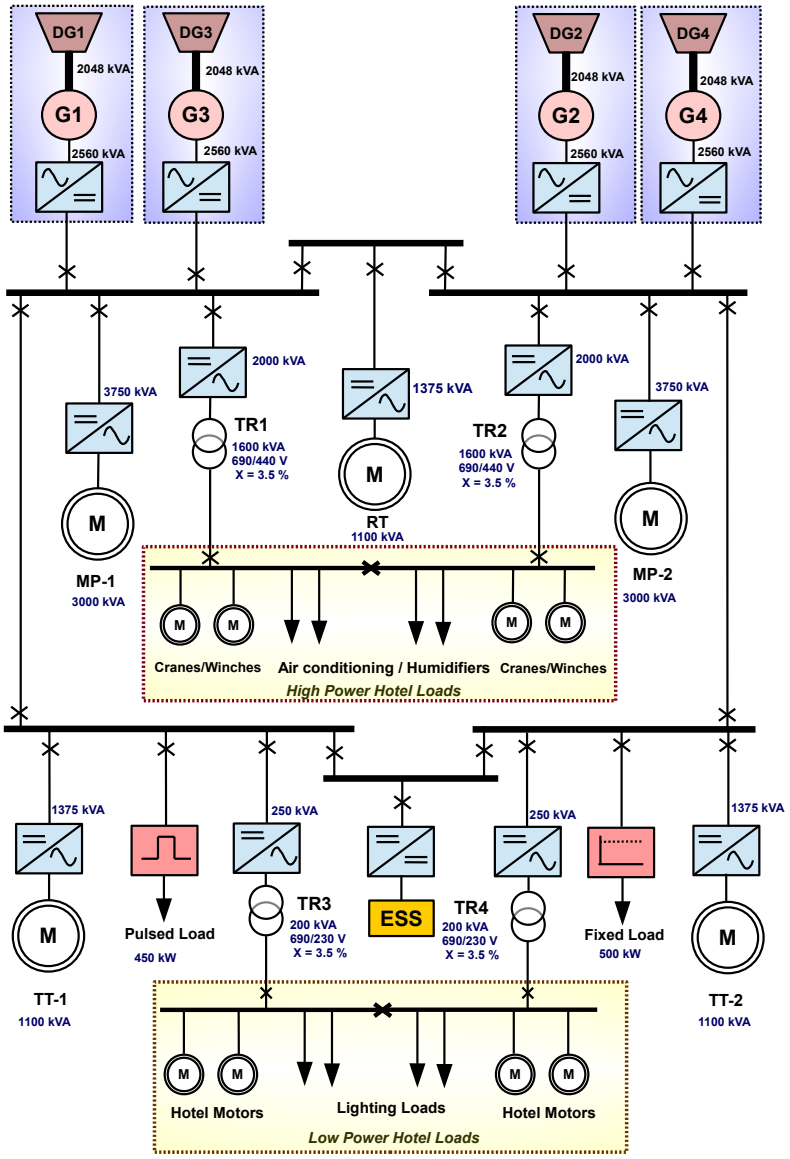


Fig. 4.1: Bus Breaker model of representative dc PSV.

4.3.1 Generation System Modeling

Diesel Engine

DEs are used as prime-movers for the WRSG in dc PSV [155]. The prime-mover model comprises of fuel injection system, dead time (t_d) representing elapsed time until a cylinder produces torque and inertia of the rotating parts. The dead-time approximation of the prime-

mover is realised by exponential delay and the transfer function is given by (4.3) [156].

$$h_{pm}(s) = \frac{P_{mech}(s)}{u_F(s)} = \frac{k_{pm}}{\tau_{pm}s + 1} e^{-t_d s}. \tag{4.3}$$

The differential equation governing the active power flow through the DE is illustrated by (4.4) and is used to determine the speed control loop of DE.

$$J\frac{d\omega_G}{dt} + k_{loss}\omega_G = \frac{P_{mech} - P_{load}}{\omega_G}. \tag{4.4}$$

The speed control loop of the DE is derived by linearizing (4.4) around the operating point $\omega_G = \omega_{Go}$. Under such conditions, the transfer function is determined as:

$$h_r(s) = \frac{\omega_G(s)}{\sum P} = \frac{1/\omega_{Go}}{Js + 2k_{loss}} \tag{4.5}$$

where $\sum P = P_{mech} - P_{load}$. The complete block diagram for DE speed control is shown in Fig. 4.2.

In the dc PSV, DE should be able to operate with minimum fuel consumption which is enabled by operating it at the optimized speed according to the load demand. Fig. 4.3(a) represents the brake specific fuel consumption (BSFC) of the representative DE operating at different power for different operating speed [44]. The cost function to determine the optimum operating speed of the DE ($C(\omega)$) in terms of the power output of the DG ($\mathscr{P}^{DG}$) is calculated to determine the operating points of the DE. This is achieved with the help of curve-fitting techniques and the cost function C(ω), is derived as following:

$$C(\omega) = A_0 + A_1\mathscr{P}^{DG} + A_2(\mathscr{P}^{DG})^2 + A_3(\mathscr{P}^{DG})^3 + A_4(\mathscr{P}^{DG})^4 + A_5(\mathscr{P}^{DG})^5, \tag{4.6}$$

where $A_0 = 720.93$, $A_1 = 1.2591$, $A_2 = -0.00292$, $A_3 = 3.8104 \text{ x } 10^{-6}$, $A_4 = -2.1716 \text{ x } 10^{-9}$, $A_5 = 4.5206 \text{ x } 10^{-13}$. The actual DE speed for various power requirements and the curve-fit version is shown in Fig. 4.3(b).

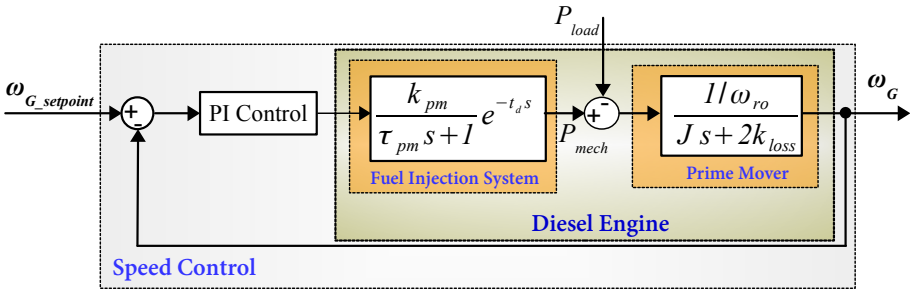
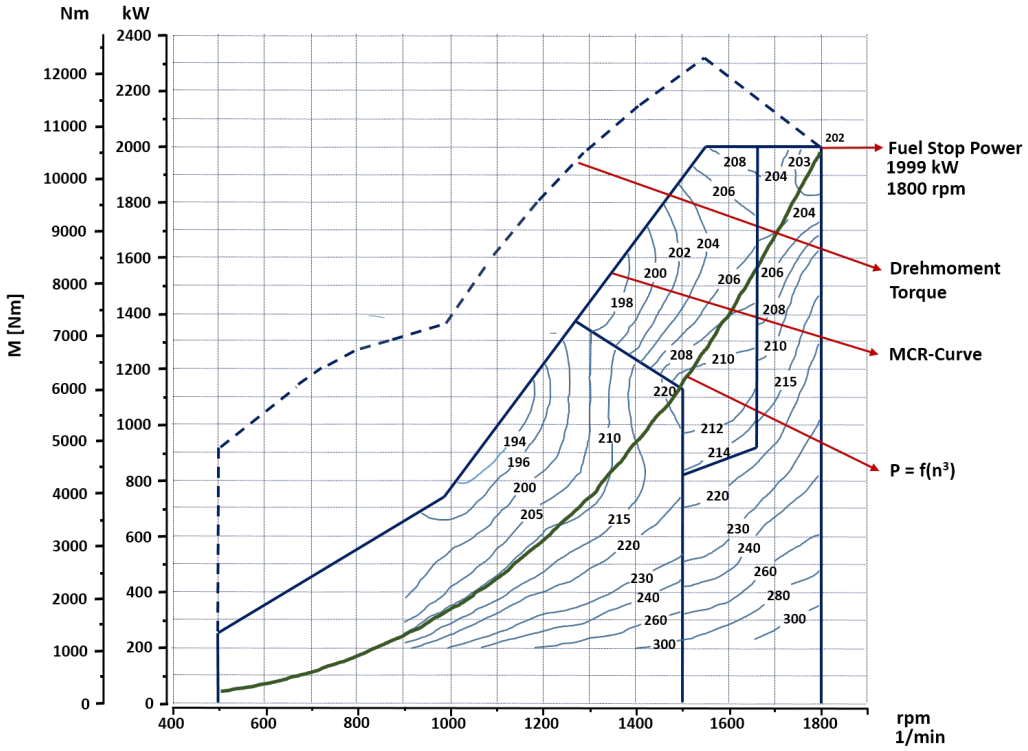
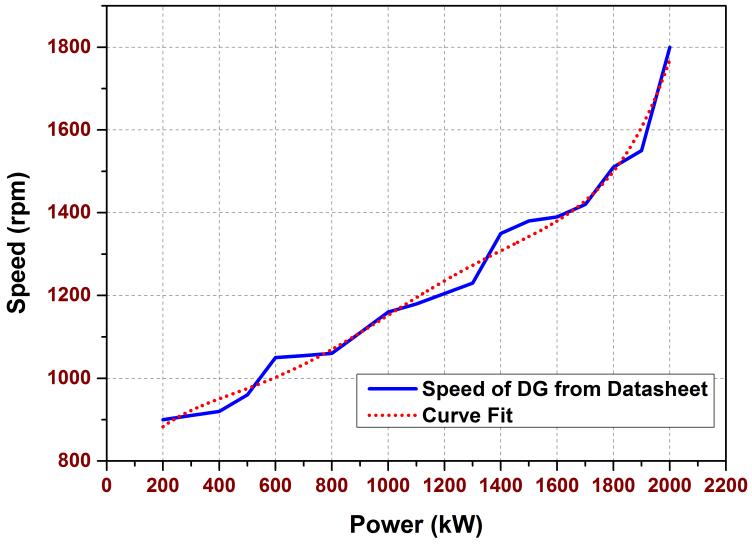


Fig. 4.2: Control loop diagram for the speed regulation of the DE.



4.3(a)



4.3(b)

Fig. 4.3: (a) BSFC chart for representative 2000 kW DE and (b) the corresponding curve-fit of diesel engine speed for optimized SFOC for various loading conditions .

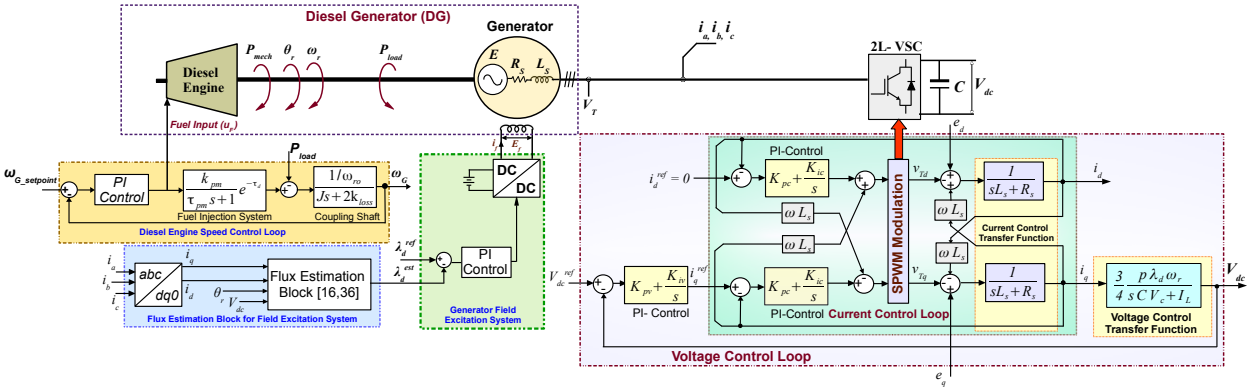


Fig. 4.4: Complete control loop of the DG interfaced with 2L-VSC.

Control of the DG-AFE Rectifier

DG includes full $M-T$ model of WRSG at stator flux reference frame (SFRF) with both the field and damper windings [147]. Control is done in $M-T$ reference frame by independently regulating the torque producing current in $T-$ axis, i_{Ts}, and machine flux in $M-$ axis, λ_{Ms} respectively. This decoupling is achieved by maintaining $i_{Ms} = 0$ [26]. Switching frequency of the VSC is chosen to be 10 kHz and the VSC is modelled in both average and detailed switching models for comparative studies in the real-time simulation environment. The detailed modeling and control of the DG interfaced with 2L-VSC has been addressed in Chapter 3. The combined control loop representation of the DG system interfaced with 2L-VSC is shown in Fig. 4.4.

4.3.2 Marine Loads

DC PSV comprises of propulsion systems, thruster systems, hotel loads and miscellaneous loads such as pulsed load to undertake different marine missions. Prioritization of the operation of these loads is dependent on the marine missions undertaken by the vessel [157] and a sample priority table considered in this thesis, as shown in Table 4.1. Modeling of these loads is required to understand the power consumption pattern which would eventually be necessary for scheduling of generation sources. The modeling and control of different loads are discussed in the subsequent sections.

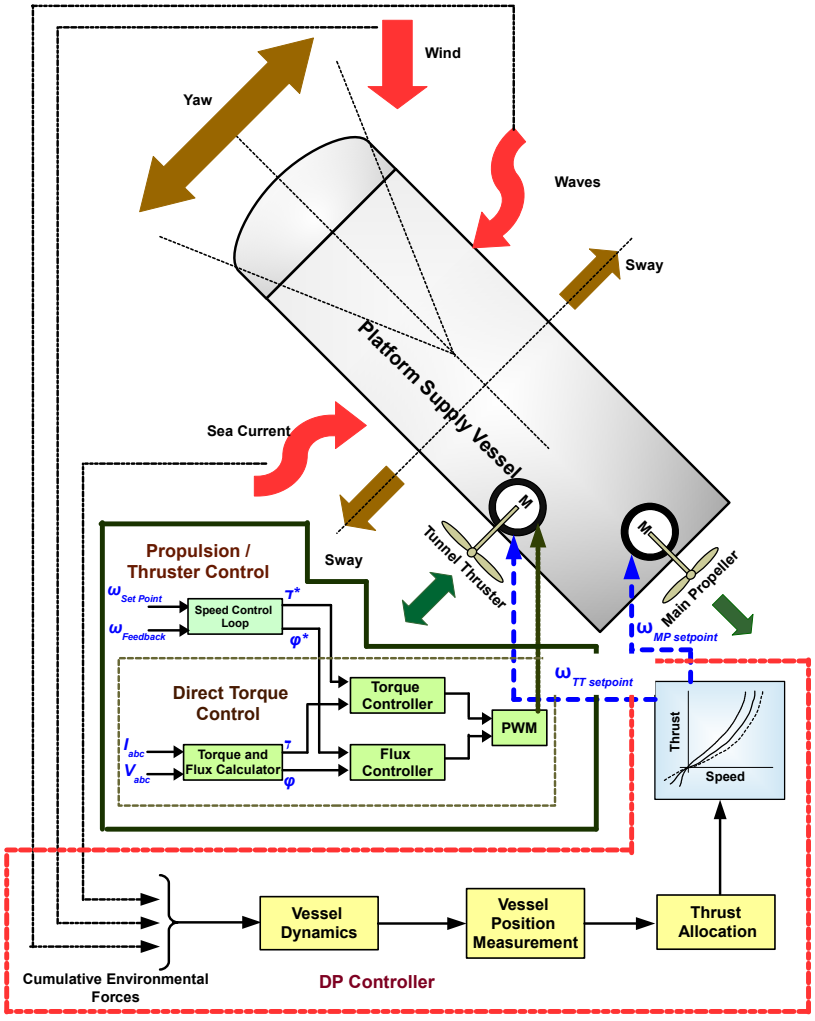


Fig. 4.5: Schematic of DP of PSV.

Propulsion Systems

In the PSVs, the propulsion systems ($L_{propulsion}$) are the main consumers of energy which undertake cruising and DP operation. The power requirement during the cruising operation

Table 4.1: Load Priorities for Different Marine Missions

Marine Mission	Main Propulsion System	Tunnel Thrusters	Hotel Loads	Pulsed Loads
Cruising	HP	MP	MP	LP
Dynamic Positioning	HP	HP	MP	LP
Naval Warfare	HP	LP	LP	HP
At Port	LP	LP	HP	LP

HP: High Priority, MP: Medium Priority, LP: Low Priority

($\mathbb{L}^{CL}$) is dependent on the operating speed of the PSV (ω_P) as shown as following:

$$\mathbb{L}^{CL} \propto \omega_P^3 \tag{4.7}$$

Power requirement during DP operation ($\mathbb{L}^{DP}$) carried out by the PSVs is primarily dependent on the environmental forces and desired co-ordinate locations [158]. The sea current, wind velocity, surge and sway of the vessels have to be balanced by the thrust produced by the thruster systems in order to maintain the desired co-ordinates. The generalised schematic of the DP system is shown in Fig. 4.5. The thrust production of the propeller is dependent on the speed (ω_P), propeller geometry (α) and hydro-dynamic quantities (β). The thrust (T_T) and torque (τ_T) developed by the thrusters for speed (ω_P), diameter of the propeller (d_P) are given as follows [158]:

$$T_T = g_T(n, \alpha, \beta) = C_T \rho d_P^4 \omega_P^2, \tag{4.8a}$$

$$\tau_T = g_\tau(n, \alpha, \beta) = C_\tau \rho d_P^5 \omega_P^2, \tag{4.8b}$$

where, C_T and C_τ are determined by open-water tests for submerged vessels and is dependent on propeller advance velocity. In this chapter, $C_\tau = 0.56$, density of water $\rho = 997 kg/m^3$ and $d_P = 3.5m$ are considered. The power consumed by the thrusters of DP system is shown in the following:

$$\mathbb{L}^{DP} = 2\pi n \tau = C_\tau \rho d_P^5 \omega_P^3. \tag{4.9}$$

For the worst weather conditions, the power demanded by the DP system to maintain desired co-ordinates would be significantly higher than that of the power demand during the calm weather condition. Direct torque control (DTC) is chosen over field oriented control (FOC) for propulsion motors and DP thrusters for its fast and superior performance and limited dependence on the machine parameters [159].

Hotel Loads

House-loads represent lighting, ventilation, accommodation loads and auxiliary systems such as small pumps. Their contribution to the total loads is usually quite small for PSV, except for vessels such as passenger cruise carriers and survey vessels. As shown in Fig. 4.1, two types of house loads are considered in this thesis. The high power hotel loads ($\mathbb{L}^{HL_{high}}$) supplying

power to cranes/winches and air-conditioning/humidifiers have cumulative rating of 3200 kVA, 440 Vac and operates as 60 Hz frequency. The low power hotel loads ($\mathbb{L}^{HL_{low}}$) have cumulative rating of 400 kVA, 230 Vac and operates at 60 Hz frequency and are responsible for small hotel motors and lighting loads. Two level voltage source inverter (2L-VSI) with constant output of 690 Vac, 60Hz is utilised for the house loads.

Miscellaneous Loads

Miscellaneous loads ($\mathbb{L}^{misc}$) comprise of the pulsed and radar loads. Pulsed loads have presence in the modern naval vessels which are used as electromagnetic guns, free electron lasers, radars and high energy lasers, which draw huge amount of current lasting for a short period of time. This intermittent nature of the loads has effect on the stability of the generation sources [160]. The pulsed load duration may vary from few microseconds to milliseconds. In this work, the pulsed load duration is selected to be 20 ms. The pulsed power load can be illustrated by the following:

$$\mathbb{L}^{pulse} = \frac{1}{T}\int_{t_1}^{t_2} P_o.\ dt \tag{4.10}$$

where, P_o is the rated power of the pulsed load, T is the time period of the pulsed load. t_1 and t_2 are the start and stop time of the pulsed load.

4.3.3 Energy Storage System

Future autonomous vessels are expected to be operated with different forms of renewables. Here, in this work it is assumed that battery based ESS (BESS) units are supplied from the PV based renewable source, which are interfaced with the dc PSV to cater for the short time load requirement and power fluctuations of the shipboard system. Such energy storage system also acts as reserve generation supply during the contingencies or sudden change of load. Unlike land based power systems where energy is stored in the ESS when its cost is low and releases when the grid electricity cost is high [19], here, there is no such variations in the cost. Electricity stored in the BESS is based on the marginal cost of the power supplied from the DGs. Cost function considered for the BESS is a constant price with the maximum power transfer based on the state of charge (SOC) as depicted in the following:

$$C_{ess} = f_p/kwh \tag{4.11}$$

The operational capacity of the ESS is restricted to 10% of the total installed generation capacity as illustrated in the following:

$$\mathscr{P}^{ESS} = 0.1 * \mathbb{P}_{Gen} \tag{4.12}$$

The PV-BESS is set to operate by limiting the battery usage between 20% and 100% of total storage capacity, further the scheduling constraints are imposed accordingly. The selection, sizing and schematic of the PV-BESS is described below.

PV Energy Sources in Marine Vessels

As per the green ship initiative, combination of photovoltaic(PV)-DG based generation systems are expected to be part of future marine vessels [161]. The rating and capacity of the PV panel is dependent on the available space in the target marine vessel [162]. For marine vessels undertaking longer voyages, e.g., liquefied natural gas carriers carriers having easier accessibility to roof top terrace; proliferation of PV based generation system with 20% capacity of the total generation system has been suggested [161–163]. This thesis considers the PSV with size and power rating comparable with the commercial available PSVs such as Rolls-Royce UT776 [153] and Viking Queen [154]. These two PSVs are equal in size and rating according to the description provided in the whitepaper [153, 154]. The deck area of the PSV is of commercial interest and cannot be utilised for PV installation [162]. Thus, the PSV has limited available space for PV array installation. It has been assumed that 600 m^2 of the total area of 1800 m^2 [153, 154] is available for installing PV arrays. Considering the parameters of the commercially available Sunpower 305 Solar Panel [164] with the available installation area of 600 m^2, the rating of total installed PV capacity is described in Table 4.2. The economic analysis of the PV panel is dependent on several market parameter and specifications but is expected to be consistent with the method provided in [163].

Sizing of PV-BESS System

According to the IEEE Std 1562-2007 [165] and IEEE Std 1013-2007 [166], sizing of the BESS connected to the PV is determined while assuming that there is no power available from the PV system. BESS is installed in the dc SPS with the intention of fulfilling the intermittent loads and supporting the generation system during various contingencies [18].

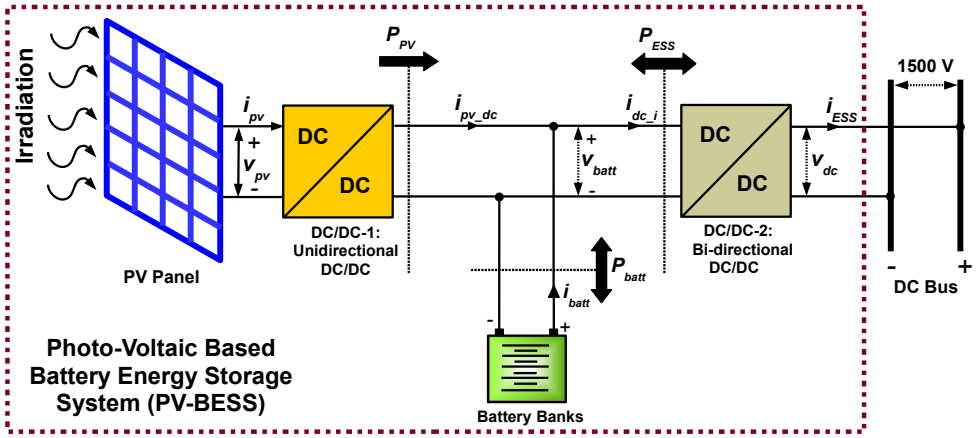
Table 4.2: Total PV Installed Capacity Using Sunpower 305 Solar Panel

Parameters	**Values**
Irradiance	1000 W/m^2
Power	305 W
Maximum Power Voltage (V_{pm})	54.7 V
Maximum Power Current (I_{pm})	5.58 A
Module Area	1.63 m^2
Total Available Area	600 m^2
Total Available PV Installation	112 kW $\approx$ 110 kW
Number of Modules	360
Modules in Series (N_s)	6
Modules in Parallel (N_p)	60
Rated Terminal Voltage (V_{tm})	330 V

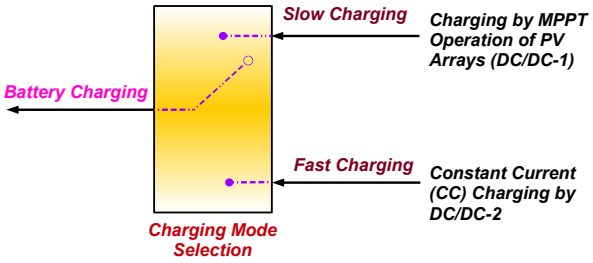
Table 4.3: Parameters of the Interfaced BESS

	Parameters	**Values**
Battery Module	Model Name	SAFT Seanergy Modules
	Nominal Voltage	46.2 V
	Nominal Capacity	60 Ah
Battery Pack	Nominal Voltage	650 V
	Nominal Capacity	1200 Ah
	Modules in Series (N_s)	14
	Modules in Parallel (N_p)	20

The PV power is primarily used to charge the BESS and maintain its SOC at maximum possible level. The selection of the BESS has been done to minimize the weight and size constraints of the dc marine vessels [18]. Further, the 10% power level of BESS is chosen to make it consistent with the trends of BESS selection in commercially available marine vessels [167]. The parameters of the BESS are chosen according to the commercially available *SAFT Seanergy* modules, which are suitable for hybrid propulsion applications [168]. The parameters of the battery module and the battery pack considering 10% of power demand are shown in Table 4.3.



4.6(a)



4.6(b)

Fig. 4.6: (a) Schematic of PV based Battery Energy Storage System (PV-BESS) and (b) representation of the battery charging schemes.

Schematic of PV interfaced BESS

The schematic of the PV and BESS interfaced with the dc bus is shown as per Fig. 4.6(a) [169]. To extract the maximum power, the PV panel is interfaced with an unidirectional DC/DC-1 converter, which works on perturb and observe (P&O) based maximum power point tracking (MPPT) algorithm [170] for the proposed real-time transient simulation scheme. The modeling of the PV generator and the MPPT algorithm is consistent with the strategy discussed in [170]. The DC/DC-2 converter is a bi-directional converter used to interface the PV-BESS to the dc bus. The modeling and control of DC/DC-2 is consistent with the approach provided in [7]. During normal operation when the SOC of the battery is above threshold limit (SOC_{max}), the converter DC/DC-2 operates at boost conversion mode supplying the power to the dc ship as fulfilling scheduled generation requirements and complying with (4.13a)–(4.13h). The variables in (4.13a)–(4.13h) is consistent with annotations

shown in Fig. 4.6(a).

$$P_{PV} > 0, \tag{4.13a}$$

$$P_{Batt} > 0, \tag{4.13b}$$

$$P_{ESS} > 0, \tag{4.13c}$$

$$i_{PV\_DC} > 0, \tag{4.13d}$$

$$i_{batt} > 0, \tag{4.13e}$$

$$i_{dc\_i} = i_{batt} + i_{PV\_DC} > 0, \tag{4.13f}$$

$$i_{ESS} > 0, \tag{4.13g}$$

$$P_{ESS} = P_{batt} + P_{PV}. \tag{4.13h}$$

When the SOC of the BESS is below the lower threshold (SOC_{min}), it could either be charged exclusively by the PV system or by the combination of PV system and DC/DC-2 converter. Since the power output of the PV array has limitation owing to dependence on available irradiation, charging with PV panel would result in slow charging as depicted in Fig. 4.6(b). Constant current (CC) based fast charging of the BESS can be carried out by maintaining the output current of DC/DC-2 at desired charging rate suggested by the manufacturers. During the charging operation supported by both PV panels and DC/DC-2 the (4.14a)–(4.14h) are satisfied.

$$P_{PV} > 0, \tag{4.14a}$$

$$P_{Batt} < 0, \tag{4.14b}$$

$$P_{ESS} < 0, \tag{4.14c}$$

$$i_{PV\_DC} > 0, \tag{4.14d}$$

$$i_{batt} < 0, \tag{4.14e}$$

$$i_{dc\_i} = i_{batt} - i_{PV\_DC} < 0, \tag{4.14f}$$

$$i_{ESS} < 0, \tag{4.14g}$$

$$P_{batt} = P_{ESS} + P_{PV}. \tag{4.14h}$$

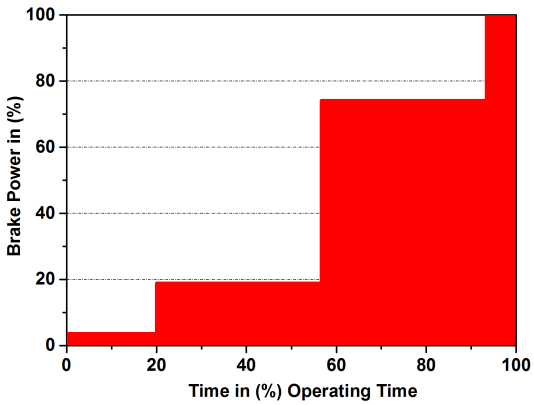


Fig. 4.7: Brake power of PSV for DP operation.

4.4 Operation of DC Platform Supply Vessel

Installed generation capacity of the PSV is generally lower than the total loads connected to the system. This is because a defined set of loads are activated for particular marine mission as indicated in Table 4.1. For cruising operation, PSV operates mostly in fixed speed condition and for DP mode, the operating speed may change depending on the load and environmental conditions. Hence, the brake power of PSV for DP operation is not constant as shown in Fig. 4.7 where the vessel mostly operates between 20%–80% of the total installed brake power [44]. Thus, incorporating dc OPF algorithm and operating the vessel at minimum SFOC can be implemented to increase the fuel efficiency. For dc OPF, reduced bus-branch model segregating the ac and dc subsystems with AC/DC–DC/AC boundary node is shown in Fig. 4.8. Generators Gen-1 and Gen-3 are clubbed together and are connected to bus B1. Similarly the Gen-2 and Gen-4 are clubbed together and connected to bus B2. The total generation capacity ($\mathbb{P}_{Gen}$) of the DGs and the ESS with the bus they are interfaced to is illustrated in the following:

$$\mathbb{P}_{Gen} = \{\mathscr{P}_{B1}^{Gen13},\ \mathscr{P}_{B2}^{Gen24},\ \mathscr{P}_{B14}^{ESS}\} \tag{4.15}$$

The loads $\mathbb{L}_{CL}$, $\mathbb{L}_{DP}$, $\mathbb{L}_{HL_{high}}$, $\mathbb{L}_{HL_{high}}$, $\mathbb{L}_{misc}$ interfaced with respective bus are depicted in

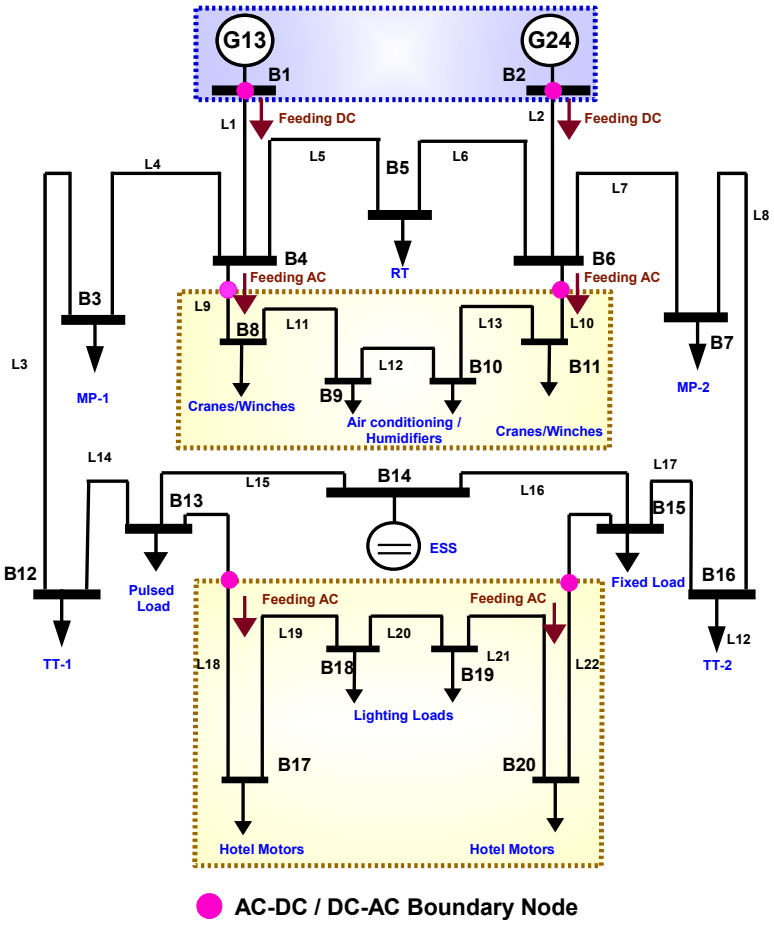


Fig. 4.8: Reduced Bus-Branch Model of representative dc PSV.

the following:

$$\mathbb{L}_{CL} = \{\mathscr{L}_{B3}^{MP1}, \mathscr{L}_{B7}^{MP2}\}, \tag{4.16a}$$

$$\mathbb{L}_{DP} = \{\mathscr{L}_{B12}^{TT1}, \mathscr{L}_{B16}^{TT2}, \mathscr{L}_{B5}^{RT}\}, \tag{4.16b}$$

$$\mathbb{L}_{HL_{high}} = \{\mathscr{L}_{n}^{HL1} || \; n = B8 \; to \; B11\}, \tag{4.16c}$$

$$\mathbb{L}_{HL_{low}} = \{\mathscr{L}_{m}^{HL2} || \; m = B17 \; to \; B20\}, \tag{4.16d}$$

$$\mathbb{L}_{misc} = \{\mathscr{L}_{B13}^{PL}, \mathscr{L}_{B15}^{FL}\} \tag{4.16e}$$

Table 4.4: Line Parameters of dc PSV

To Bus	From Bus	Line	R (mΩ)	X (mΩ)	P (kVA)	V (pu)
4	1	L1	0.48	-na-	2x2048	1.0
6	2	L2	0.48	-na-	2x2048	1.0
12	3	L3	0.092	-na-	2x1750	1.0
4	3	L4	0.092	-na-	2x1750	1.0
5	4	L5	1.5	-na-	3000	1.0
6	5	L6	1.2	-na-	3000	1.0
7	6	L7	0.64	0.75	1600	1.0
16	7	L8	0.64	0.75	1600	1.0
9	4	L9	3.2	-na-	1100	1.0
11	6	L10	3.2	-na-	1100	1.0
9	8	L11	2.56	-na-	450	1.0
10	9	L12	2.56	-na-	450	1.0
11	10	L13	2.56	2.31	2x200	1.0
13	12	L14	2.56	2.31	2x200	1.0
14	13	L15	3.2	-na-	1100	1.0
15	14	L16	0.03	-na-	2x2048	1.0
16	15	L17	0.03	-na-	2x2048	1.0
17	13	L18	0.03	-na-	2x2048	1.0
18	17	L19	0.03	-na-	2x2048	1.0
19	18	L20	0.03	-na-	2x2048	1.0
20	19	L21	0.03	-na-	2x2048	1.0
15	20	L22	0.03	-na-	2x2048	1.0

4.5 Real-Time DC PSV Power Management System

4.5.1 Problem Statement

As explained in the previous sections, operation of dc PSV requires real-time scheduling mechanisms to fulfill load demands in various operating conditions. The real-time transient simulation scheme with dc OPF is more suitable for such conditions which determines the power injections of the DGs and ESS subjected to physical and operational constraints (relevant data in Table 4.4 and Table 4.5). SFOC of the DGs can be minimized by operating the DGs in optimized speed. Equality constraints include power balance at each node and inequality constraints include the network operating limits, DG limits, ESS limits and limits on the other control variables. These control variables include active power output of the generators, power electronic controls, amount of load disconnected, and the status of storage devices.

4.5.2 Problem Formulation

Scheduling of the generation systems is governed in such a way to effectively utilize the available resources and minimize the SFOC by operating the DGs in optimized speed. In

Table 4.5: Bus Data of dc PSV

Bus	$\mathbf{P_{max}}\uparrow$**(kW)**	$\mathbf{P_{min}}\downarrow$**(kW)**	**Q(kVAr)**	**V(pu)**
B1	+4096	0	-na-	1.05
B2	+4096	0	-na-	1.05
B3	-3000	0	-na-	1
B4	-640	0	-480	1
B5	-1100	0	-na-	1
B6	-640	0	-480	1
B7	-3000	0	-na-	1
B8	-240	0	-180	1
B9	-400	0	-300	1
B10	-400	0	-300	1
B11	-240	0	-180	1
B12	-1100	0	-na-	0.95
B13	-450	0	-na-	0.95
B14	+820	0	-na-	1
B15	-450	0	-na-	0.95
B16	-1100	0	-na-	0.95
B17	-80	0	-60	1
B18	-80	0	-60	1
B19	-80	0	-60	1
B20	-80	0	-60	1

this process, the optimization framework considers the set constraints as follows:
Minimize SFOC

$$F(\{\mathscr{P}_{B1}^{Gen13},\ \mathscr{P}_{B2}^{Gen24},\ \mathscr{P}_{B14}^{ESS}\}) = f(x,u) \tag{4.17}$$

subject to

$$w(x,u) = 0 \tag{4.18}$$

$$q(x,u) \leq 0 \tag{4.19}$$

where the cost function referring to the active power of the energy resources is minimized while respecting the equality constraints $w(x,u)$ and inequality constraints $q(x,u)$. These constraints can be viewed as linear and nonlinear constraints:

$$w(x,u) = \begin{bmatrix} w_{nl}(x,u) \\ J_e(x,u) + o_e \end{bmatrix} \tag{4.20}$$

$$q(x,u) = \begin{bmatrix} q_{nl}(x,u) \\ J_i(x,u) + o_i \end{bmatrix} \tag{4.21}$$

where, J_e and J_i are the state variables of converter and dc network. Energy storage and dc side converter power feed-in are mapped to the corresponding ac buses to satisfy the Kirchhoff Law.

Vector x consists of dependent variables such as: fixed parameters such as non-controlled generator or ESS outputs, non-controlled loads, and line parameters. Vector u consists control variables including: real power generation, PSV load shedding parameters/priorities, ESS charging and discharging limits, ramp rates of the DG, dc line flows, and converter control settings. The equality and inequality constraints are namely, power flow equations, limits on all control variables, generation/load balance, branch flow limits and SOC limits. Considering Fig. 4.8 which represents reduced bus-bar model of dc PSV (having DGs, ESS, and different types of loads); for an anticipated group of loads, total system generation should be scheduled in such a way to minimize the SFOC of DG. In such cases, network equality constraints are represented by the standard load flow equations [171]. In the real-time operation, PSV load balance equation neglecting the line losses is given by:

$$\sum_{i=1}^{B}(\mathscr{P}_{Bi}^{Gen} + \mathscr{P}_{Bi}^{ESS}) - \sum_{i=1}^{D}(\mathscr{P}_{Di}^{L} + \mathscr{P}_{Di}^{ESS}) = 0. \tag{4.22}$$

Inequality constraints limits are set accordingly, for example, generator limits are set as :

$$\mathscr{P}_{Bi_{min}}^{Gen} \leq \mathscr{P}_{Bi}^{Gen} \leq \mathscr{P}_{Bi_{max}}^{Gen}, \tag{4.23}$$

$$Q_{Bi_{min}}^{Gen} \leq Q_{Bi}^{Gen} \leq Q_{Bi_{max}}^{Gen}. \tag{4.24}$$

Load shedding or load balancing limits has been set as:

$$0 \leq \mathscr{L}_{Bi}^{shed} \leq \mathscr{L}_{Bi}^{D_{total}}. \tag{4.25}$$

Energy storage limits set as:

$$\mathscr{P}_{Bi_{min}}^{ESS} \leq \mathscr{P}_{Bi}^{ESS} \leq \mathscr{P}_{Bi_{max}}^{ESS}. \tag{4.26}$$

Converter voltage limits on the ac side are non-linear in nature and can be set as:

$$\mathscr{V}_{conv_{min}}^{2} \leq \mathscr{V}_{\mathscr{R}conv}^{2} + \mathscr{V}_{\mathscr{I}conv}^{2} \leq \mathscr{V}_{conv_{max}}^{2}. \tag{4.27}$$

Converter filter side constraints are as follows, where V_R and V_I are real and imaginary parts of the voltage:

$$\mathscr{V}_{filter_{min}}^{2} \leq V_{Rfilter}^{2} + V_{Ifilter}^{2} \leq \mathscr{V}_{filter_{max}}^{2}, \tag{4.28}$$

and the limits on the dc voltages and converter currents are as follows

$$\mathscr{V}_{min}^{dc} \leq \mathscr{V}^{dc} \leq \mathscr{V}_{max}^{dc}, \tag{4.29}$$

$$I_{min}^{conv} \leq I^{conv} \leq I_{max}^{conv}. \tag{4.30}$$

The current flow limits through the line is given by:

$$I_{L_x\ min} \leq I_{L_x} \leq I_{L_x\ max}; x = [1:22]. \tag{4.31}$$

The $q(x,u)$ in (4.21) is formed by the (4.23)–(4.31) as stated above. It is to be noted that the voltage and branch flow limits are the only non-linear limits on the ac side. Options of setting branch limits, and other operational limits in the dc PSV are implemented as well.

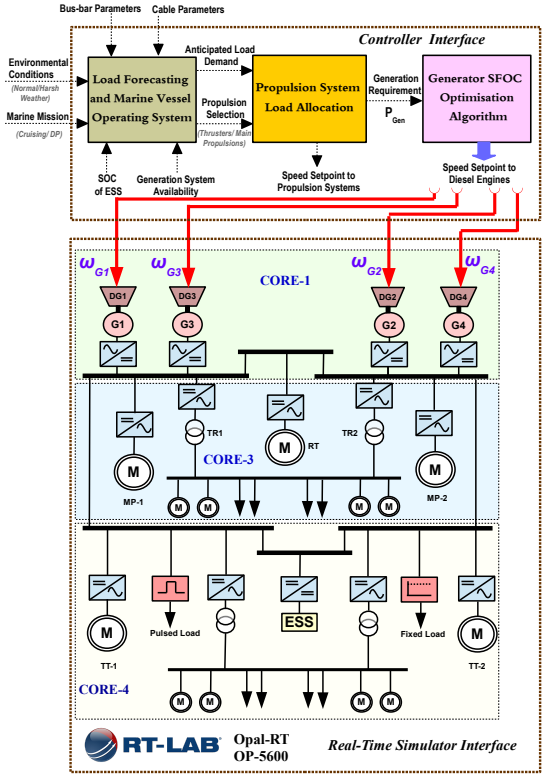
Power generation schedules obtained from the optimization framework have been fed to the SFOC calculation block to calculate the speed ($C(\omega)$) based on (4.6) derived in Section 4.3, where speed is derived as a function of generator schedules:

$$C(\omega) = f(\mathscr{P}^{DG}). \tag{4.32}$$

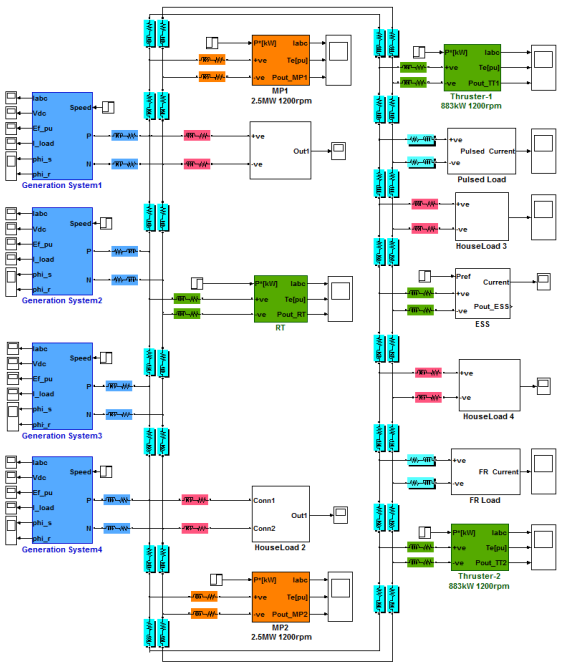
SFOC at each optimized speed point corresponding to the power schedules has been calculated using the *'SFOC lookup table'* available in the SFOC calculation block.

4.5.3 Real-Time Transient Simulation of DC PSV

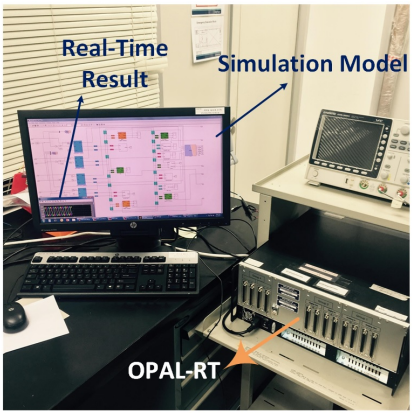
The architecture of the real-time transient simulation setup comprising of generator scheduling scheme based on dc OPF is shown in Fig. 4.9(a). Depending on the operating mode, the scheduling block takes the input from the operating personnel. The available generation is also fed to calculate the reserve generation capacity and setting the upper limits of the generation system. Line parameters (Table 4.4) and bus-bar parameters (Table 4.5) are fed to ensure that the loading in each line/bus stays within prescribed limits. The scheduled generation is calculated and fed to the SFOC optimization block to calculate the power demand and corresponding speed set point of each of the in-line DGs. The scheduling block and the SFOC algorithm is the part of the controller while the rest of the system of dc PSV system is divided into master/slave computational subsystems and loaded into computing cores of OPAL-RT OP5600 based real-time simulator. The segregation of cores of the real-time simulation model has been realized with the help of gyrators and the partitioning contours of the divided subsystems are shown in Fig. 4.9(a). The description of the real-time simulation system is described below.



4.9(a)



4.9(b)



4.9(c)

Fig. 4.9: (a) Architecture of the Real-Time Load Scheduling of dc PSV (b) schematic in MATLAB/SIMULINK environment and (b) representative OPAL-RT setup for real-time simulation.

Overview of Real-Time Simulation System

The real-time simulation is conducted on the OPAL-RT based OP5600 real-time simulator, which operates on RedHat Linux based operating system and is interfaced with the host

PC by TCP/IP cable. The setup of the real-time simulation system is shown in Fig. 4.9(c). OPAL-RT uses RT-LAB based real-time platform which facilitates the conversion of MATLAB/Simulink models into real-time executable models [151]. It has dedicated toolboxes such as RT-Events, RTE-drive, ARTEMiS®to support the real-time simulation system. Execution of the model is achieved by ARTEMiS®solver which is a high-order time-step integration algorithm and is not prone to numerical oscillations. The minimum time step available for real-time simulation in the dc transient real-time simulation model is 10 μs. All the results obtained with the switching models are compared with the averaged models to analyse the performance of VSCs under such time step limitations as well. The partitioning of system using gyrators helps in avoiding numerical inaccuracies by ensuring parallel computation of the partitioned subsystems.

Gyrator Based Partitioning of System

Gyrator is an ideal energy transducer used for bond graph representation of a physical system [172]. This method has been used for partitioning of the bigger marine dc power system into smaller subsystems for parallel computation in real-time transient simulation framework. With reference to Fig. 4.10(a), 4.10(b) the bigger system is divided into Subsystem-1 and Subsystem-2 with the help of gyrator, G_rY while satisfying the following:

$$V_1 = f(I_2) \tag{4.33a}$$

$$V_2 = f(I_1), \tag{4.33b}$$

From (4.33a) and (4.33b), it can be implied that current I_2 in Subsystem-2 is dependent on the voltage V_1 of Subsystem-1 or vice versa. This approach can be realised by implementing dependent current and voltage sources. The partitioning of subsystems for 'n' number of elements utilising gyrator based partitioning approach is shown in Fig. 4.11. In both Fig. 4.10(a) and Fig. 4.11, a very high value resistance (R_T) is placed to ensure numerical consistency of the simulation and memory block is used to avoid algebraic loop errors. The measured current and voltage between the computational subsystems is transferred using `OpComm` block [151, 173]. With the gyrator based approach the entire dc marine

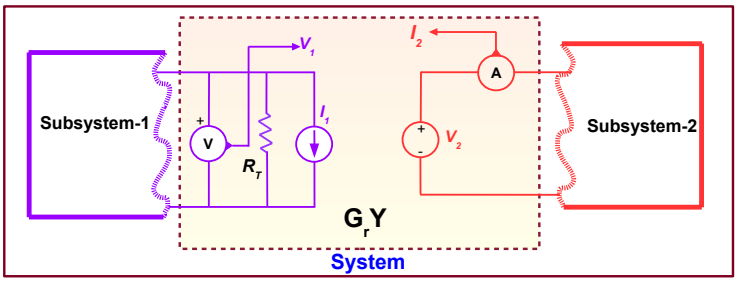
system is divided into four subsystems (three computational subsystems and one console subsystem). The computational subsystems comprise of one master (`SM_Generator`) and two slave subsystems (`SM_Bus1Load`, `SM_Bus2Load`). The console subsystem (`SC_Console`) is the user interface for data logging. The final partitioned executable file for transient real-time simulation is shown in Fig. 4.12.

Obtaining Results

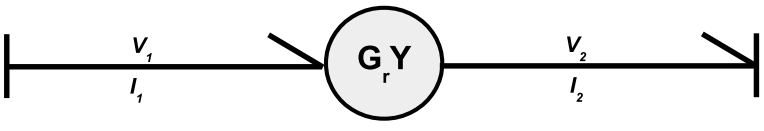
The output results from the real-time simulator have been obtained by: (i) monitoring scopes in the console subsystem (`SC_Scope`), (ii) by viewing the results in the monitoring oscilloscope and (iii) by saving the data in `.mat` file by `OpWrite` block [151, 173] for offline analysis. All the results presented in this chapter are obtained by processing `.mat` files. The results obtained from the oscilloscope are also presented for comparison with the offline analyzed results.

4.5.4 Algorithm for Real-Time Transient Simulation

Pseudo-code for real-time generation scheduling of dc PSV for minimized SFOC is shown as Algorithm 1. Algorithm 1 is located in the external controller whose primary function is to generate the power schedule for each generation systems according to the loading conditions.



4.10(a)



4.10(b)

Fig. 4.10: (a) Representation of gyrators for partioning between Subsystem-1 and subsystem-2 and (b) Bond graph structure of a gyrator.

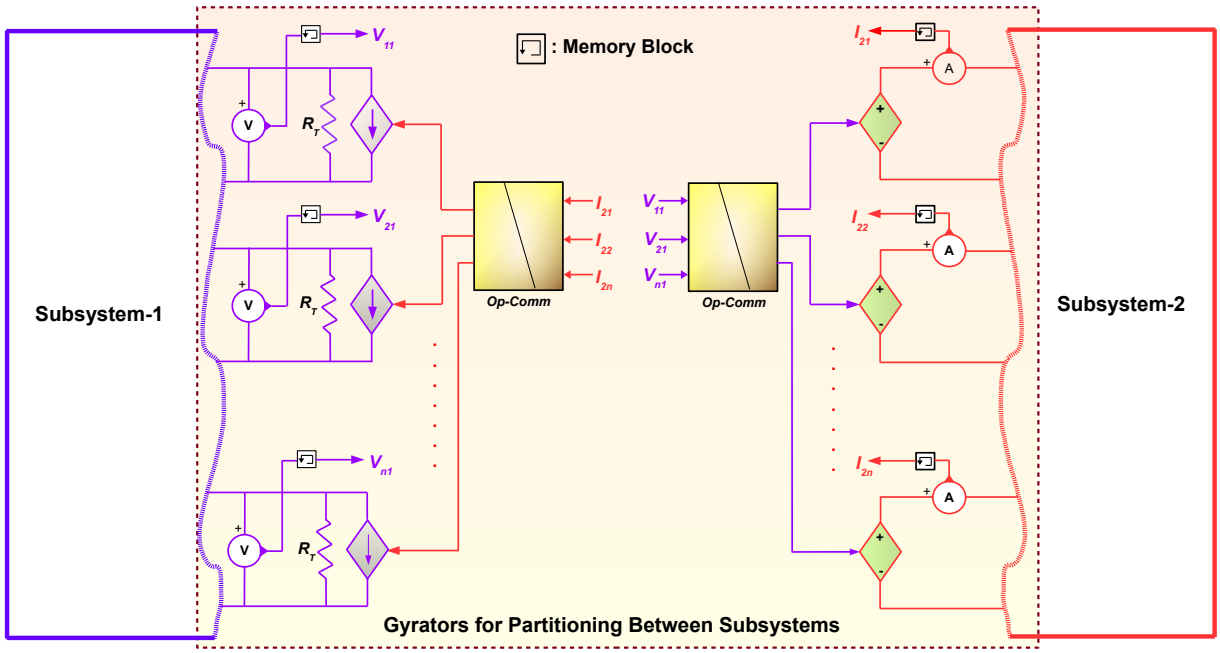


Fig. 4.11: Gyrator based system partitioning for 'n' number of elements.

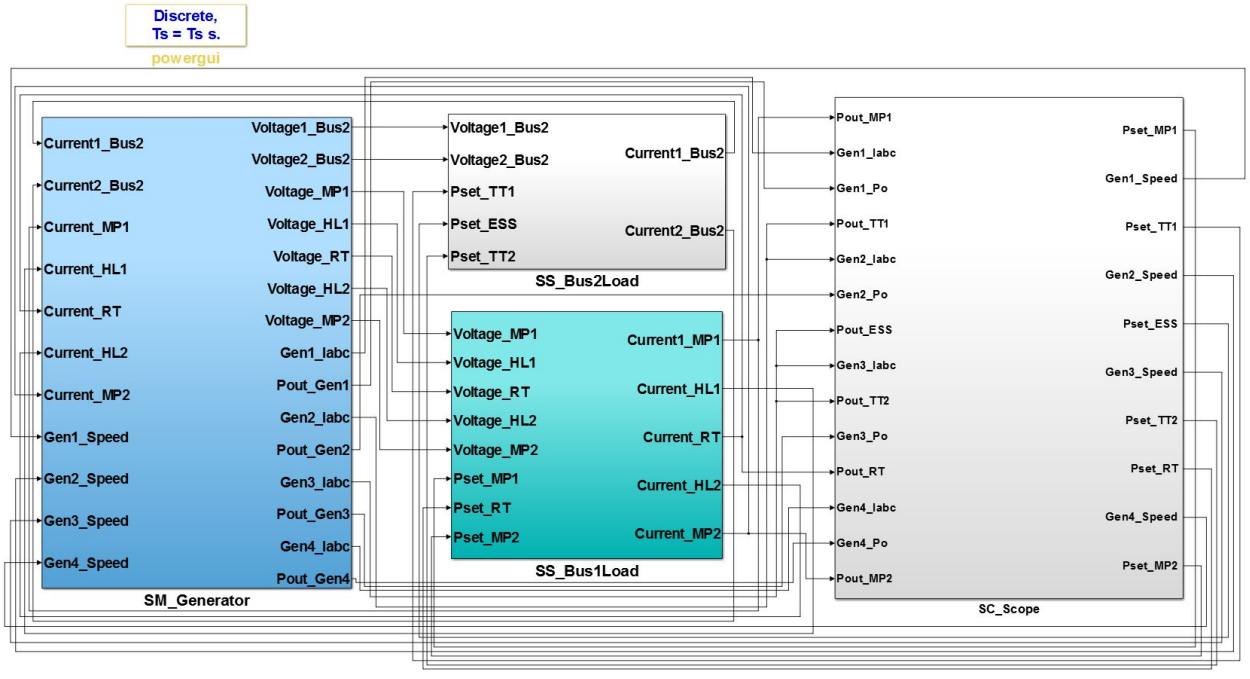


Fig. 4.12: Representative MATLAB/Simulink model into partitioned subsystems for real-time simulation in OPAL-RT.

First step is to collect the information of the dc PSV regarding the availability/unavailability of generation systems, type of marine missions, load demands etc. Based on such information, the dc OPF generates the schedule for all the generation systems utilizing the reduced bus-bar model. The speed of the DE is set to the desired speed as determined by the cost function which is (4.6). Speed and power set-points are fed to the dc PSV which is located in the real-time simulator. This process is repeated for the defined time instants.

Algorithm 1 Pseudo-code of Scheduling for dc PSV

– Read generation data, network data, load estimation data, static load data, SOC of ESS, and other PSV parameters.
– Define operating limits based on the shipboard real-time marine missions. ▷ (4.19)–(4.32).
– Build initial Z-bus by handling isolated nodes, if any. ▷ Table 4.4, Table 4.5
– Create incidence matrix for the existing shipboard network.
- Initialize the proposed Optimization Suite. ▷ (4.23)-(4.30)
while ((Error tolerance for power) < Set limit) **do**
    while (All options are not processed) **do**
        - Find $\triangle X_{bus}$ with power injection matrices
        - Calculate power flow, line outage conditions (if any), SOC of ESS
        while (All scheduling options are not processed) **do**
        end while
        - Store the scheduling options
        - Evaluate objective function f ▷ (4.6), (4.13)
    end while
    for (Each generated schedule P_i i = 1,2,...,no. of generators:P **do**
    (a) Create speed vector from scheduled generations P_i;
    (b) Evaluate the schedules for minimized SFOC.
    Check the error criterion to met. Otherwise, the appropriate speed is chosen from the corresponding generator speed vector.
    end for
end while
- Dispatch the scheduling plans to generation systems.

4.6 Real-Time Simulation Results

With reference to the operational aspects of the proposed dc PSV power management system, this section presents the simulation results of various cases of operating modes and associated contingencies in the real-time operation. The various contingencies associated

Table 4.6: Contingency List

CASE	CONTINGENCY CONDITION	CONNECTED LOADS					Gen-1		Gen-2		Gen-2		Gen-4		ESS
		$TT1$	$TT2$	RT	$MP1$	$MP2$	P_{G1}	ω_{G1}	P_{G2}	ω_{G2}	P_{G3}	ω_{G3}	P_{G4}	ω_{G4}	
1A	Sudden gain of DP load	-300	-300	-300	0	0	+949	1130	+949	1130	+949	1130	+949	1130	+4
		-800	-800	-800	0	0	+1324.88	1280	+1324.88	1280	+1324.88	1280	+1324.88	1280	+0.49
1B	Sudden gain of DP load with inadequate SOC	-300	-300	-300	0	0	+950	1130	+950	1130	+950	1130	+950	1130	-
		-800	-800	-800	0	0	+1325	1280	+1325	1280	+1325	1280	+1325	1280	-
2A	Sudden loss of DP load	-800	-800	-800	0	0	+1324.88	1280	+1324.88	1130	+1324.88	1130	+1324.88	1130	+4
		-200	-200	-200	0	0	+899.37	1108	+899.37	1108	+899.37	1108	+899.37	1108	+2.5
2B	Sudden loss of DP load with inadequate SOC	-800	-800	-800	0	0	+1325.88	1280	+1325.88	1130	+1325.88	1130	+1325.88	1130	-
		-200	-200	-200	0	0	+900	1109	+900	1109	+900	1109	+900	1109	-
3A	Bus-2 isolated at low DP load	-300	-300	-300	0	0	+949	1130	+949	1130	+949	1130	+949	1130	+4
		-300	-300	-300	0	0	+1701	1425	+1701	1425	0	0	0	0	+398
3B	Bus-2 isolated at low DP load with inadequate SOC	-300	-300	-300	0	0	+950	1130	+950	1130	+950	1130	+950	1130	-
		-300	-300	-300	0	0	**+2100**	n/a	**+2100**	n/a	0	0	0	0	-
4	Inadequate SOC at low DP load	-300	-300	-300	0	0	+949	1130	+949	1130	+949	1130	+949	1130	+4
		-300	-300	-300	0	0	+950	1130	+950	1130	+950	1130	+950	1130	-
5A	Bus-2 isolated at high DP load	-800	-800	-800	0	0	+1324.88	1280	+1324.88	1280	+1324.88	1280	+1324.88	1280	+0.49
		-800	-800	-800	0	0	+1934.60	1650	+1934.60	1650	0	0	0	0	**+1430.8**
5B	Bus-2 isolated at high DP load with inadequate SOC	-800	-800	-800	0	0	+1325	1280	+1325	1280	+1325	1280	+1325	1280	0
		-800	-800	-800	0	0	**+2650**	n/a	**+2650**	n/a	0	0	0	0	0
6	Inadequate SOC at high DP load	-800	-800	-800	0	0	+949	1130	+949	1130	+949	1130	+949	1130	+ 0.49
		-800	-800	-800	0	0	+948.8	1130	+948.8	1300	+948.8	1300	+948.8	1300	-
7A	Sudden Gain in Cruising Load	0	0	0	-1000	-1000	+1224.86	1243	+1224.86	1243	+1224.86	1243	+1224.86	1243	+0.55
		0	0	0	-2500	-2500	+1875.17	1570	+1875.14	1570	+1875.14	1570	+1875.14	1570	**+399.32**
7B	Sudden Gain in Cruising Load with inadequate SOC	0	0	0	-1000	-1000	+1225	1243	+1225	1243	+1225	1243	+1225	1243	-
		0	0	0	-2500	-2500	+1975	1716	+1975	1716	+1975	1716	+1975	1716	-
8A	Sudden Loss in Cruising Load	0	0	0	-2500	-2500	+1875.17	1570	+1875.17	1570	+1875.17	1570	+1875.17	1570	**+399.32**
		0	0	0	-1000	-1000	+1224.86	1243	+1224.86	1243	+1224.86	1243	+1224.86	1243	+0.55
8B	Sudden Loss in Cruising Load with inadequate SOC	0	0	0	-2500	-2500	+1975	1716	+1975	1716	+1975	1716	+1975	1716	-
		0	0	0	-1000	-1000	+1225	1243	+1225	1243	+1225	1243	+1225	1243	-
9	Bus-2 isolated at low Cruising Load	0	0	0	-1000	-1000	+1224.86	1243	+1224.86	1243	+1224.86	1243	+1224.86	1243	0.55
		0	0	0	-1000	-1000	+1879.62	1575	+1879.62	1575	0	0	0	0	**+1140.76**
10A	Bus-2 isolated at high Cruising Load	0	0	0	-2500	-2500	+1875.17	1570	+1875.17	1570	+1875.17	1570	+1875.17	1570	+399.32
		0	0	0	-2500	-2500	**+2750.25**	n/a	**+2750.25**	n/a	0	0	0	0	**+2399.5**
10B	Bus-2 isolated at high Cruising Load (partial load shedding)	0	0	0	-2500	-2500	+1875.14	1570	+1875.14	1570	+1875.2	1570	+1875.2	1570	+399.5
		0	0	0	-2500	-2500	**+2384.5**	n/a	**+2384.5**	n/a	0	0	0	0	**3130.96**
10C	Bus-2 isolated at high Cruising Load(maximum load shedding)	0	0	0	-2500	-2500	+1875.17	1570	+1875.17	1570	+1875.17	1570	+1875.17	1570	+399.32
		0	0	0	-2500	-2500	+1652.5	1400	+1652.5	1400	0	0	0	0	**+2014.85**

TT: tunnel thruster; RT: retractable thruster; MP: main propulsion; Gen: Generator
Output of the generator, ESS and load consumption in kilo watts (kW). Generator shaft speed in *rpm*.

with dc PSV are listed in Table 4.6 which has been prepared considering both availability and unavailability of 10% ESS described in Section 4.3. From Table 4.6, it can be observed that the generator and ESS output are marked in red color for some specific contingencies. This indicates the overload conditions of the generation system for supplying high power output. In the proposed framework, such relaxation has been set for the PSV generation systems to emulate real-time characteristics.

4.6.1 PSV Operating Modes and Associated Contingencies

Dynamic Positioning Operation

For the DP operation, $\mathbb{L}_{CL}$ is set to zero while $\mathbb{L}_{HL_{high}}$, $\mathbb{L}_{HL_{low}}$ are set at 1000 kVA and 270 kVA, respectively, and $\mathbb{L}_{misc}$ is set to the rated value. As described previously, the value of $\mathbb{L}_{DP}$ is dependent on the weather conditions, propeller design and characteristics. Under normal weather condition $\mathbb{L}_{DP}$ is set at lower value with all the thrusters operating at lower loading conditions as shown in (4.34a). On the contrary at harsh weather conditions, the

thrusters are set to be operating at higher loading conditions as shown in (4.34b).

$$\mathbb{L}_{DP\ low} = \{\mathscr{L}_{B12}^{TT1}, \mathscr{L}_{B16}^{TT2}, \mathscr{L}_{B5}^{RT}\} = \{-300kW, -300kW, -300kW\}, \tag{4.34a}$$

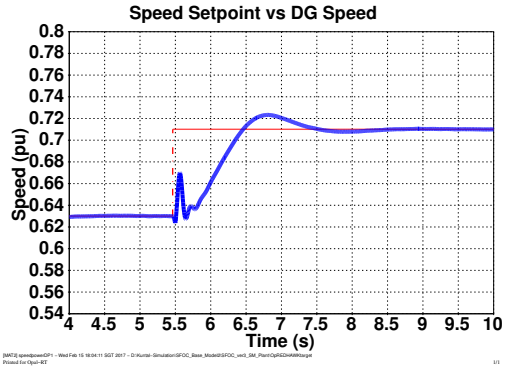
$$\mathbb{L}_{DP\ high} = \{\mathscr{L}_{B12}^{TT1}, \mathscr{L}_{B16}^{TT2}, \mathscr{L}_{B5}^{RT}\} = \{-800kW, -800kW, -800kW\}. \tag{4.34b}$$

Various contingency cases have been prepared such as loss of generation system and unavailability of ESS (inadequate SOC) at low DP load and high DP load conditions. Utilizing the transient simulation framework formulated in Section 4.5, the desired power and corresponding operating speed set point of the generation systems $\mathbb{P}_{Gen}$ for all the contingency cases have been listed in Table 4.6. During the fault at bus-2 ($\mathscr{P}_{B2}^{Gen24} = 0$) with harsh weather conditions, power demand to the ESS ($\mathscr{P}^{ESS}$) exceeds its rated capacity which cannot be suitably fulfilled. This inadequate generation availability can be mitigated by load shedding operation by referring to Table 4.1. However, the ESS helps in generation scheduling when the Bus-2 is isolated during low load DP operation and also during sudden gain/loss of DP loads, which is indicated in blue color in Table 4.6. The results pertaining to sudden gain in DP load as per Case 1A of Table 4.6 are shown in Fig. 4.13.

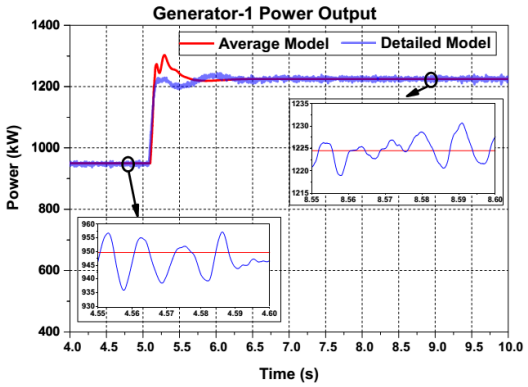
The path of transition of the operating point of the optimized SFOC from initial set-point to the final set-point has been traced in Fig. 4.13(d). The trajectory of the SFOC for fixed speed operation is also plotted for comparison with the proposed operation methodology. From Fig. 4.13(d) it can be inferred that there is substantial reduction of SFOC with the proposed method. The reduction in SFOC is 19% when the DGs are allowed to operate in optimized speed rather than fixed speed during low load DP mode. The operating regime of the DG exceeds the prescribed contour of operation because of the abrupt increase in the load. However, in the real-system the load transition is expected to be smoother rather than sudden abrupt changes. Nevertheless, the initial and final SFOC is optimized and lies within stable region. The output from the monitoring oscilloscope is presented in Fig. 4.13(e) for comparison with the offline results.

Cruising Mode Operation

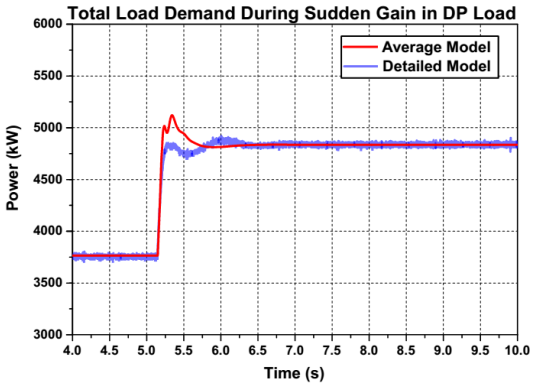
For the cruising operation, $\mathbb{L}_{DP}$ is set to zero while $\mathbb{L}_{HL_{high}}$, $\mathbb{L}_{HL_{low}}$ and $\mathbb{L}_{misc}$ are set to similar value that of DP operation. The $\mathbb{L}_{CL}$ primarily depends on the operating speed of the vessel. For low cruising speed the loading of the main propulsion systems are given in



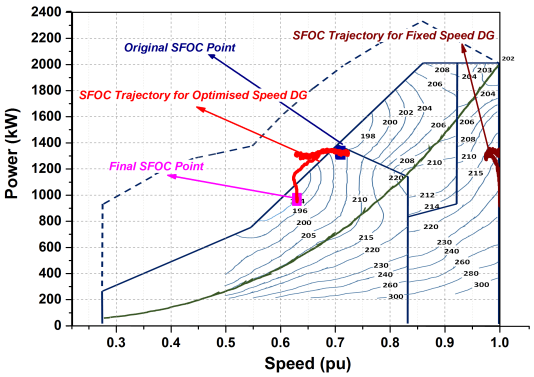
4.13(a)



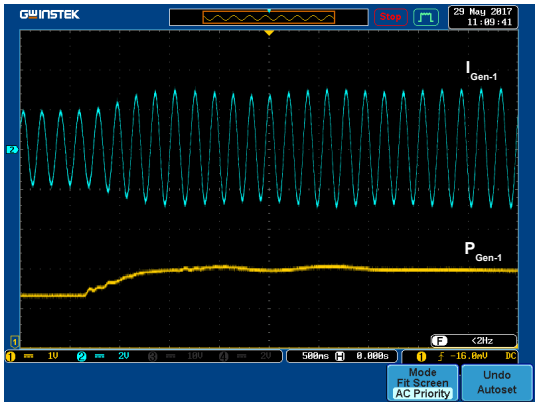
4.13(b)



4.13(c)



4.13(d)



4.13(e)

Fig. 4.13: (a) Speed set point vs DG speed, (b) power variation of DG-1, (c) change in total load demand and (d) transition of SFOC to optimized point in real-time and (e) output in monitoring oscilloscope during sudden gain in DP load as per Case 1A of Table 4.6.

(4.35a) while for higher speeds, the loading of the main propulsion systems are given by (4.35b).

$$\mathbb{L}_{CL\ low} = \{\mathscr{L}_{B3}^{MP1}, \mathscr{L}_{B7}^{MP2}\} = \{-1000kW, -1000kW\}, \tag{4.35a}$$

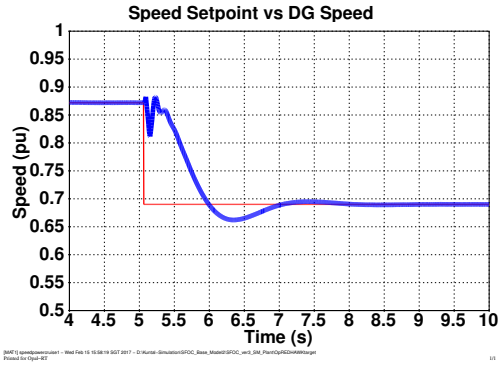
$$\mathbb{L}_{CL\ high} = \{\mathscr{L}_{B3}^{MP1}, \mathscr{L}_{B7}^{MP2}\} = \{-2500kW, -2500kW\}. \tag{4.35b}$$

Similar to the DP operation, various contingency conditions have been prepared for the cruising loads which are described in Table 4.6. In the contingencies associated with fault at Bus-2, the $\mathscr{P}_{B14}^{ESS}$ exceeds its rated capacity thus implementation of load shedding algorithm becomes impertinent. However, when the Bus-2 is isolated and by setting maximum load shedding by employing $\mathbb{L}_{HL_{high}} == 0$ and $\mathbb{L}_{misc} == 0$ the $\mathscr{P}_{B14}^{ESS}$ still exceeds the rated limits as highlighted in Case 10C of Table 4.6. Thus, during this contingency, higher cruising load cannot be supported, thus the speed of the PSV needs to be slowed down to prevent inadvertent black-out condition. However, scheduling of ESS is helpful for the sudden gain/loss of the cruising loads indicated with blue color in Table 4.6. The real-time simulation results during sudden loss of cruising load are shown in Fig. 4.14.

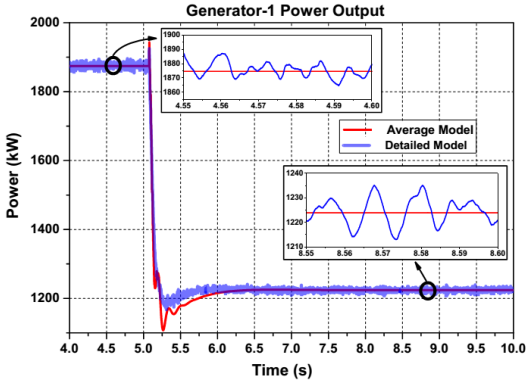
The transition of SFOC operating point from initial to final set point value is shown in Fig. 4.14(d). The same operation is repeated when the vessel operates with fixed speed generation system and the SFOC is compared in Fig. 4.14(d). It can be established that the SFOC is minimized with the proposed method. Although the power is abruptly decreased, the operating point lies within the contours of the operating limits of the DG. As discussed earlier, the change in load would not be abrupt in real scenario hence the DG would operate with minimum SFOC in the stable region. Output from the monitoring oscilloscope is presented in Fig. 4.14(e) for comparison with the offline results.

4.6.2 Dynamics of the PV based BESS System

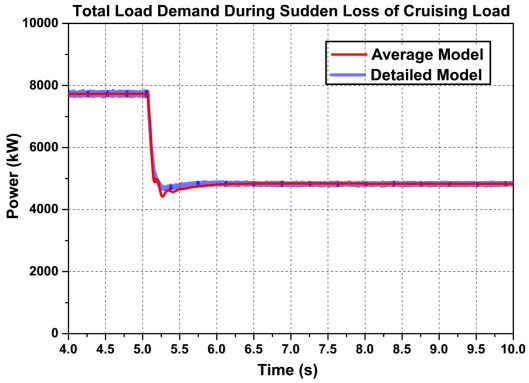
(i) **Charging of BESS:** As discussed in Section 4.3.3, the charging of the BESS could be carried out either by slow charging or fast charging schemes. Fig. 4.15 shows the variation of irradiance and the output power of the DC/DC-1 while operating at MPPT mode of operation. The PV current (i_{pv}) for charging the BESS is shown



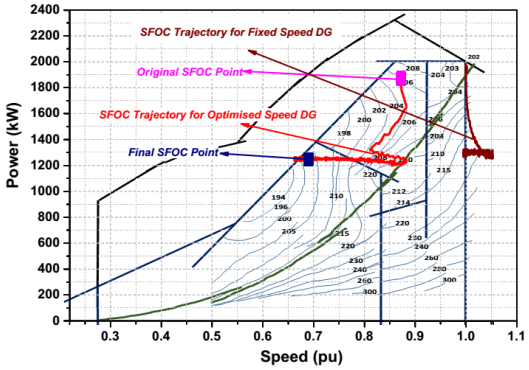
4.14(a)



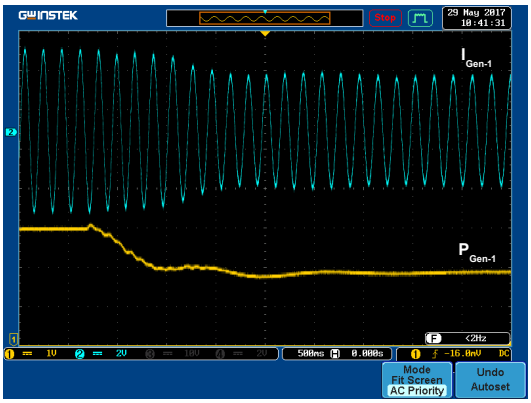
4.14(b)



4.14(c)



4.14(d)



4.14(e)

Fig. 4.14: (a) Speed set point vs DG speed, (b) power variation of DG-1, (c) change in total load demand and (d) transition of SFOC to optimized point in real-time and (e) output in monitoring oscilloscope during sudden loss in cruising load as per Case 8A of Table 4.6.

in Fig. 4.15(b). For fast charging the DC/DC-2 maintains battery charging current determined by the set point ($i_{batt-SP}$) as shown in Fig. 4.15(c). With the DC/DC-1 current i_{pv} the variation of i_{dc_i} and i_{batt} with change of irradiation and battery charging current set point is shown in Fig. 4.15(c). Fig. 4.15(d) shows the variation of SOC of the BESS when it is subjected to slow charging and fast charging respectively. The slow charging of the BESS can be employed while the PSV is in dockyard. Alternatively, the fast charging schemes might be employed by forecasting the nature of job to be done by the PSV and if the job requires intermitted power requirements.

(ii) **Discharging of BESS:** The discharging of the BESS is explained with reference to Case 8A of Table 4.6. During sudden change of the DP operation, the power demand off the BESS decreases from 399.32 kW to 0.55 kW. The power delivered by the PV-BESS system is shown in Fig. 4.15(e).

4.6.3 Possibility of Treatment of Sub-Optimal Points

With the contingency scenario 8A of Table 4.6, initial derived generation of 1875.17 kW and ESS of 399.32 kW are the points-1 in Fig. 4.16(a). Table 4.7 shows the calculated SFOC at this operating point. Such a SFOC is dependent on the operating speed of the DG and the ESS output. However, it has been observed that the scheduling constraints are also satisfied at the sub-optimal locations with certain generation schedules and the corresponding SFOC values associated with it. These points are termed as *local-optimum* points. To illustrate this, $\mathscr{P}_G^n$ is considered as generator schedule and & f as the objective function used in Algorithm 1. The conditions for *minima* is represented by [174]:

$$\mathscr{P}_G^n \in \mathbb{R} \implies f'(P_G^n) = 0, \tag{4.36a}$$

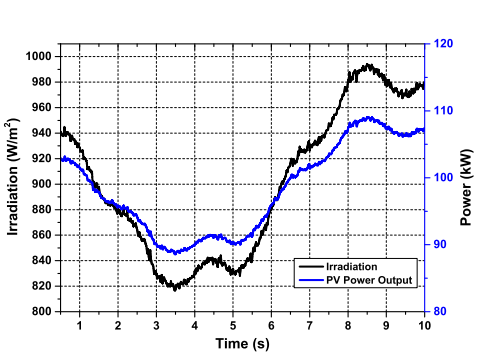
$$f'(\mathscr{P}_G^n) > 0. \tag{4.36b}$$

Conditions for local minima (sub-optimal point) is given in the following:

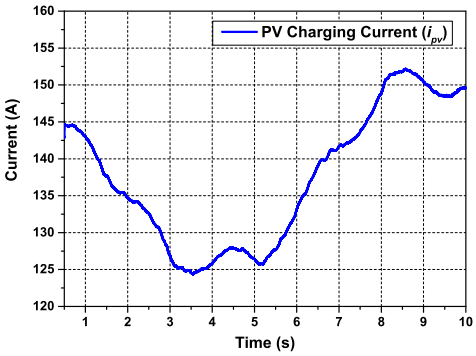
$$f^* = f(\mathscr{P}_G^{n*}), \tag{4.37}$$

for local minimizer $\mathscr{P}_G^{n*}$. This is the smallest function value in some feasible neighbourhood defined by the following:

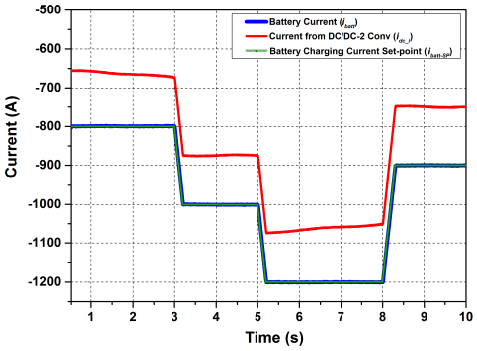
$$\mathscr{P}_G^{n*} \in \Omega. \tag{4.38}$$



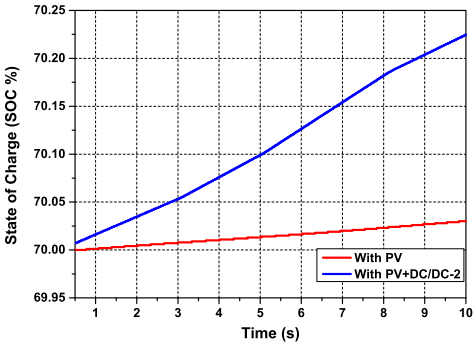
4.15(a)



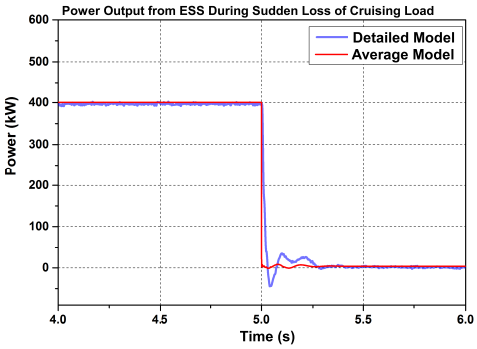
4.15(b)



4.15(c)



4.15(d)



4.15(e)

Fig. 4.15: (a) Change in power availability from PV panels with change in irradiation, (b) variation of current output of PV panel while operating it in MPPT mode, (c) charging current characteristic from DC/DC-2 (d) change in SOC of BESS when it is charged from PV panel and both with PV panel and DC/DC-2 and (e) DC/DC-2 output for contingency 8A in Table 4.6.

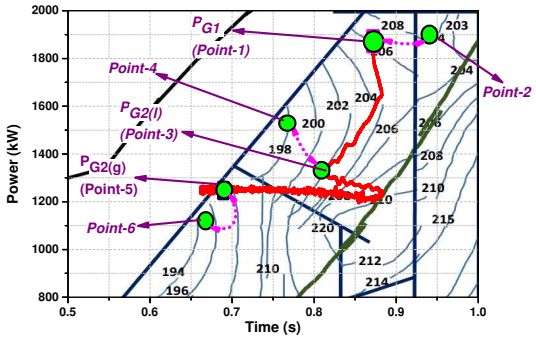
There exists a $\delta > 0$ such that

$$f^* \leqslant f(\mathscr{P}_G^{n*}) \;\forall\; P_G^n, \quad \text{in } \{\mathscr{P}_G^{n*} \in \Omega : |\mathscr{P}_G^n - \mathscr{P}_G^{n*}|\} \leqslant \delta. \tag{4.39}$$

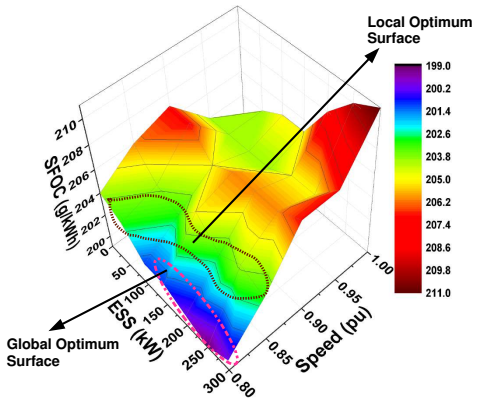
Thus, there can be many local minima, i.e., multiple sub-optimal points which are not global minima. It has been observed that during real-time simulations such sub-optimal (local optimum points), which satisfy the given constraints, have the potential to speed up the calculations of the scheduling process while diligently treating the associated ESS to arrive at better SFOC values than the corresponding SFOC at global optima. This has been demonstrated using Table 4.7 corresponding to Fig. 4.16(a), where the ESS is varied at all sub-optimal locations to study the impact on the SFOC. Absence of ESS during the initial state at P_{G1} would improve the SFOC operating scenario (*Point-2*), however the limits of generator capacity (2048 kW) are enforced to consider the ESS as an option (*Point-1*). Here, ESS is delivering at 399.32 kW and the corresponding SFOC is 207 (*Point-1*). Now, with sudden loss of the cruising load it can be noticed that before arriving to the global optimum point $P_{G2(g)}$ (*Point-5*), it has been passing through a local optima $P_{G2(l)}$ (*Point-3*) where the corresponding SFOC is 205 against the global optimum SFOC of 197 ($P_{G2(g)}$, *Point-5*). During such a phase, it is evident that ESS is no longer required to contribute to the load, and accordingly scheduling algorithm suggested the output of ESS at +0.55kW. However, considering enforced operation of ESS at this instant shall make the corresponding SFOCs of P_{G2} and $P_{G2(l)}$ at 195 (*Point-6*) and 200 (*Point-4*), respectively. Hence, instead of abrupt suspension of ESS supply, slowly adjusting the ESS in such as way to yield the best scenario of SFOC is a possibility and where the sub-optimal points can be diligently treated.

Table 4.7 shows the variation of SFOC corresponding to these sub-optimal points considering ESS in operation even after the sudden loss of load and at optimized speed of generators. However, it may not be prudent to consider such points in all the contingency cases owing to operational constraints such as availability and SOC of the interfaced ESS. Hence, it is evident that the sub-optimal point can yield better SFOC at optimized speed and, further, it also has an advantage in reducing the time propagation of schedules for feeding to the shipboard controllers. It is also noticed that the sub-optimal points can accommodate ESS for better performance of DGs. To speed up the calculation in scheduling process and to treat the consideration of ESS; sub-optimal schedules can yield a feasible solution.

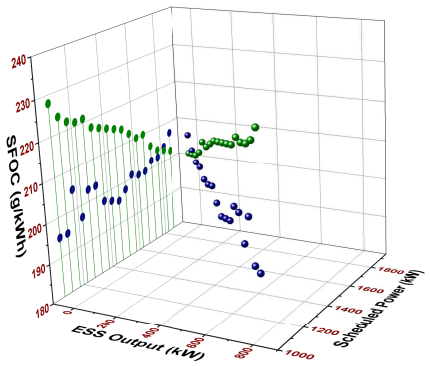
Dependence of ESS output on sub-optimal locations is further demonstrated with the help of Fig. 4.16(b), 4.16(c), 4.16(a)(d). In Fig. 4.16(b), power extraction from ESS is varied from 0 kW to 300 kW to visualise the changing operating points of the SFOC of DG while



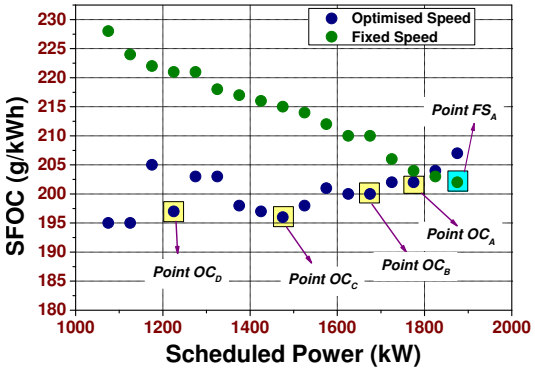
4.16(a)



4.16(b)



4.16(c)



4.16(d)

Fig. 4.16: (a) Trajectory of the SFOC during sudden loss of cruising load with locations of various sub-optimal points, (b) surface plot of SFOC variation for varying ESS and DG speed, (c) comparison of the changing operating points and (d) location of suboptimal points for DGs operating at optimised speed and fixed speed.

fulfilling constant load demand of 1875 kW. The location of the global optima with minimized SFOC and local optima is highlighted in Fig. 4.16(b). In Fig. 4.16(c), 4.16(a)(d) it is further

Table 4.7: Variation of SFOC at Sub-Optimal Points during Sudden Loss of Cruising Load

Points	**ESS Output** (kW)	**Generation Output** (kW)	**Optimised Speed** (p.u.)	**SFOC** (g/kWh)
1	400	1875	0.872	207
2	0	1975	0.953	204
3	0	1330	0.72	205
4	400	1230	0.70	200
5	0.55	1225	0.69	197
6	400	1125	0.66	195

compared with the DG operating at constant speed. With reference to the Fig. 4.16(a) the following observations can be cited below:

(i) Fig. 4.16(b) depicts the surface plot of the SFOC variation with ESS and DG speed in the aforesaid treatment of suboptimal points. The sub-optimal scheduled points are also marked in the figure.

(ii) Fig. 4.16(c), 4.16(d) shows the comparative analysis of the location of sub-optimal points for fixed speed and optimised speed operation of the DGs. It can be observed that the minimum SFOC for the corresponding sub-optimal points for fixed speed DGs are achieved while operating at rated conditions denoted by *Point* FS_A in Fig. 4.16(d).

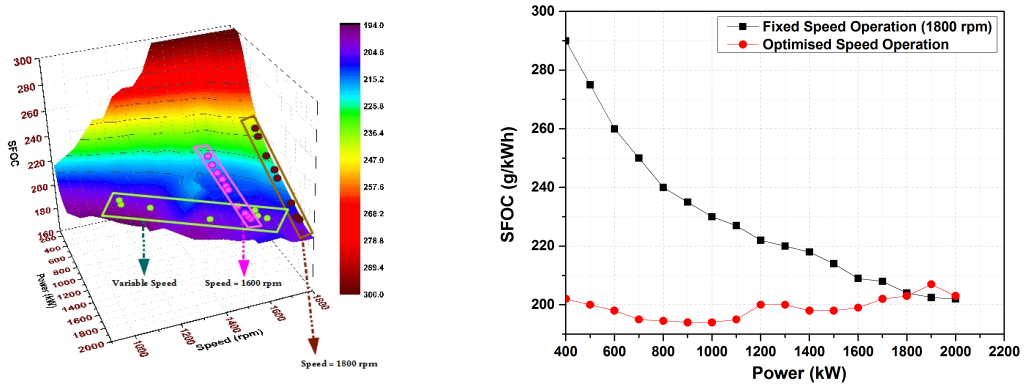
(iii) For the DGs operating at optimised speed, there are multiple sub-optimal points depending on ESS output and operating speed of DG. These sub-optimal points the variable speed DGs the sub-optimal locations are dependent on the injected power from ESS and DG operating speed as shown in Fig. 4.16(d). The location of the sub-optimal points are shown as *Point* OS_A, *Point* OS_B, *Point* OS_C and *Point* OS_D, in Fig. 4.16(d).

4.6.4 Comparison with the Operation at Different Speeds

For all the operating cases in Table 4.6, SFOC is compared when the generator is running at 1800 rpm, 1600 rpm and at the calculated optimized speed. Variation of the operating points are plotted in Fig. 4.17. It can be seen that SFOC is significantly reduced when running at optimized speed, thus highlighting the advantages of the proposed real-time transient simulation scheme.

4.7 Summary

This chapter investigates the modeling and control approaches of dc PSV with real-time transient simulation framework to minimize the fuel consumption in terms of SFOC while considering treatment of sub-optimal points along with an option of utilizing onboard PV based energy storage facility. This sort of real-time operation is expected to be key ingredient of the future autonomous marine vehicles. The following discussions are cited:



4.17(a) 4.17(b)

Fig. 4.17: (a) Variation of operating point of SFOC for generator running at 1800 rpm, 1600 rpm and variable speed (optimised speed) and (b) comparison of SFOC for generator running at 1800 rpm and optimised speed.

(i) DC OPF based algorithms have been applied for real-time scheduling of generation resources with an objective to minimize the fuel consumption. This operation is within the framework of the proposed real-time transient simulation setup and has been successfully demonstrated in this chapter. Results obtained are promising and strengthens the ability of the future dc marine vessels to comply with the upcoming stringent laws on pollution control. It has been shown that the output of ESS can influence the generator set points particularly during sudden load changes for DP and cruising missions.

(ii) Traditionally, the power sharing happens according to generator ratings through droop control rather than optimal generation scheduling as per load demand for a particular marine mission. Hence, an optimal scheduling system based on dc OPF for tackling any specific nature of marine missions has been demonstrated in this work and the results indicated such an approach will enable the PSV to operate in fuel efficient regime with improved transient responses.

(iii) Responses of the DGs to various contingencies are studied and it has been found that unavailability of the generation system due to fault at bus bar demands higher requirement of ESS to satisfy the load demands. In such cases, it is pertinent to have load shedding routines which are dependent on the marine missions to prevent power blackout of the vessel. This highlights the necessity for considering such routines in

future autonomous dc PSVs. Some cases have been highlighted using the proposed real-time transient simulation framework.

(iv) Higher fuel savings are noticed while the generators are operated at optimised speed for low power demand. In comparison to fixed speed operation, reduction in SFOC of 19% has been reported when the PSV was operating at low power DP operation.

This operating real-time transient model of the dc PSV will be utilized in the subsequent chapters for systematic fault studies and devising fault detection algorithms.

Part II

Design of Protection System for DC SPS

Chapter 5

Short-Circuit Transient Analysis and Protection Requirements of DC SPS

5.1 Introduction

It has been described in Chapter 1 and Chapter 2 that dc power systems offer numerous advantages when applied to shipboard applications. The major advantages are improved fuel efficiency, easier integration of emerging generation sources and no requirement of phase and frequency synchronisation of the ac generators. However, the dc power systems in SPS face challenges with regards to lack of comprehensive fault detection and protection techniques. Without effective and stable measures to detect and counter the electrical faults in the system, the SPS may not be able to carry out its intended mission and may jeopardize the

The results of this chapter have been partially published in:

(i) **K. Satpathi**, A. Ukil, S. S. Nag, J. Pou and M. A. Zagrodnik, "DC marine power system: Transient behaviour and fault management aspects," *IEEE Trans. Ind. Informat.*, vol. 15, no. 4, pp. 1911-1925, Apr. 2019.

(ii) **K. Satpathi**, Y.M. Yeap, A. Ukil, and N. Geddada, "Short-time Fourier transform based transient analysis of VSC interfaced point-to-point DC system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 4080-4091, May 2018.

(iii) D. Francis, Q. Zhengting, **K. Satpathi**, N. Thukral and A. Ukil, "Suitability of Rogowski coil for DC shipboard protection," in *Proc. IEEE TENCON Conf.*, Singapore, Nov. 2016.

(iv) **K. Satpathi** and A. Ukil, "Protection of MVDC shipboard power system using Rogowski coil," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

(v) **K. Satpathi** and A. Ukil, "Protection strategies for LVDC distribution system," in *Proc. IEEE PowerTech Conf.*, Eindhoven, Netherlands, Jun. 2015.

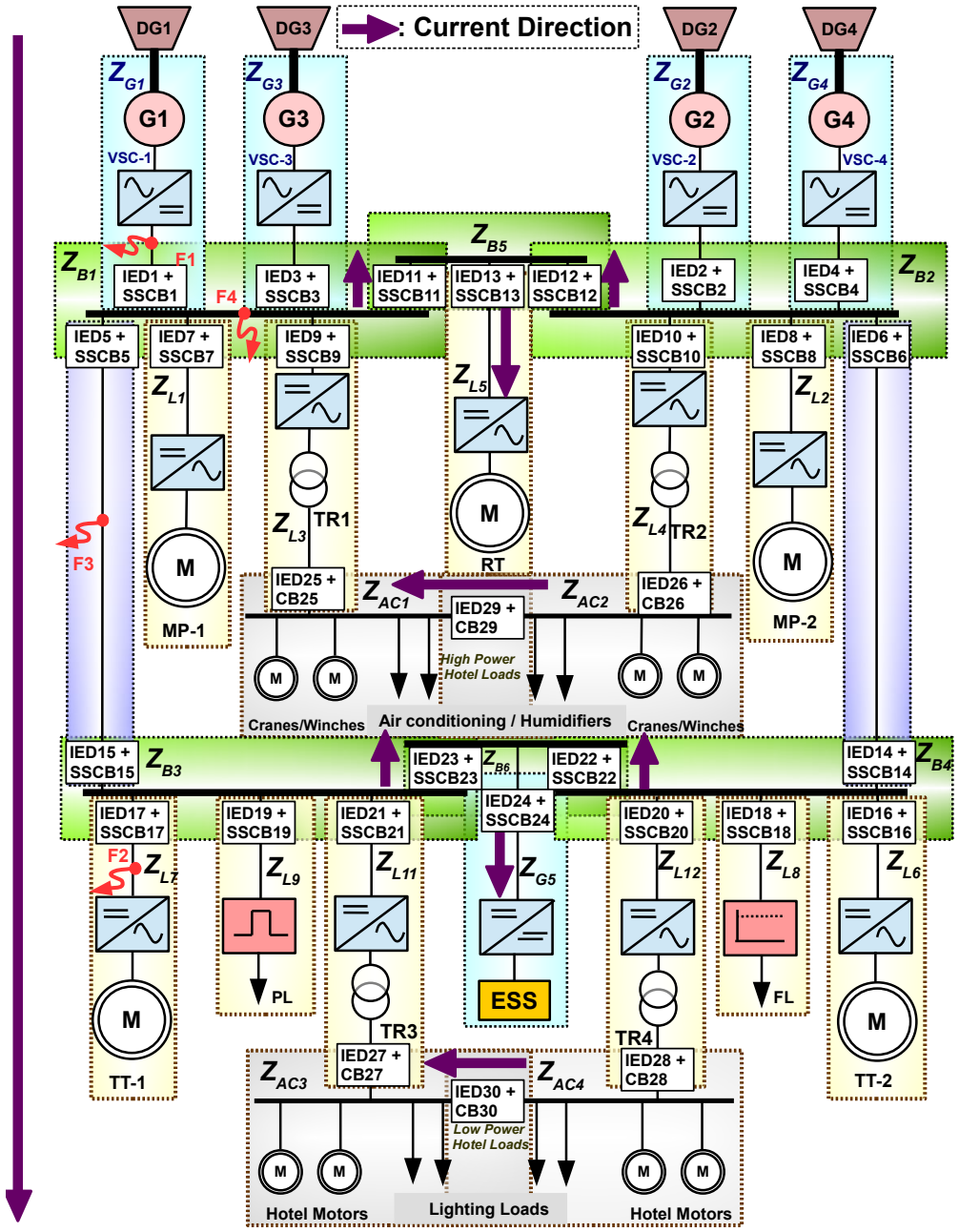


Fig. 5.1: Representative dc PSV for dc fault studies.

safety of vessel and crew. It is thus required to perform in-depth fault studies in systematic manner to understand the protection requirements in the target dc SPS, which is considered as the PSV in this thesis. Fig. 5.1 depicts the real-time simulation schematic of the dc PSV intended for the short-circuit fault analysis and understanding the protection system design.

It comprises of four 2-MW variable speed DGs interfaced with the 1.5 kV dc bus using 2L-VSC. MP is the 2.5-MW main propulsion drive responsible for cruising operation. TT and RT are 883-kW tunnel thruster and retractable thruster drive, respectively, to undertake DP operation. ESS is the energy storage system interfaced with the dc bus using a bi-directional dc/dc converter. Detailed modeling, control of the interfaced components along with the operation of dc PSV have been already described in detail in Chapter 3 and Chapter 4. Computation of the real-time simulation system is carried out by state-space-nodal analysis in an RT-Lab platform based on OPAL-RT [151, 173]. The generators and loads of dc PSV are interfaced with the dc bus using intelligent electronic device (IED) and solid state circuit breaker (SSCB). Since the prime components of dc PSV are generators, loads, bus-bars and cables, for network protection in such dc SPS, possible fault locations would be at these components. Thus, the faults F_1, F_2, F_3 and F_4 have been chosen, which correspond to the faults at the generator terminals, load terminals, buses, and cables. This is shown in Fig. 5.1. Time- and frequency domain analysis of the fault currents are carried out at these locations to understand the protection requirements.

5.2 Contribution of the Chapter

The following major contributions are included in this chapter:

(i) A detailed short-circuit analysis has been done at the generator and load terminals, lines and bus-bars. Time-domain based fault analysis has been carried out for the fault resistances varying from very low-impedance (0.001 Ω) to very high impedance (100 Ω) faults.

(ii) Selectivity requirements for the dc PSV are elaborately discussed. The requirements are compared with those of ac power systems.

(iii) Protection requirements for the dc SPS are identified. It is shown that the time-domain based fault detection techniques might not be suitable for application in the dc SPS. On the contrary, the frequency-domain analysis is found to be suitable for fault detection in such application. Short-Time Fourier Transform (STFT) based fault detection has been proposed for such applications.

(iv) This chapter also develops and describes the step-by-step procedure of STFT-based fault detection for the dc SPS. A mathematical analysis of the STFT algorithm has been developed for the normal pre-fault current, stepped change in dc current and for the fault conditions. Detailed understanding of the STFT for dc protection and the threshold setting for the fault detection is supported by such analysis.

The minor contributions of this chapter are:

(i) Effect of the fault on the propulsion loads and the changing system configuration are also studied.

(ii) It is shown that the Rogowski coil (RC) can be suitable for the fault detection process in the dc power system. Application of RC for fault detection process is also discussed.

5.3 Time-Domain Analysis of DC Short-Circuit Faults

Short-circuit faults and sudden changes in the load demand are the most common transients associated with dc power systems. However, the dc SPS is expected to be high-impedance grounded (at the mid-point of the dc-link capacitor) or ungrounded to operate for single earth fault thus improving the survivability of the vessel [4]. In such scenarios pole-to-pole short-circuit fault becomes the most severe kind of fault, which might critically impact the operation of dc SPS, and has been considered in this chapter. Analysis of the short-circuit fault is essential to investigate the nature of the fault transients. This is needed to understand the protection requirements and to find proper solutions. The plausible short-circuit faults F_1, F_2, F_3 and F_4 are initiated at the generator terminals, load terminals, lines and the busbar, respectively, as shown in Fig. 5.1.

5.3.1 Short-Circuit Fault in DC SPS

Stages of DC Fault Current

Pole-to-pole short-circuit fault is considered in this chapter which occurs when the positive and negative poles are short-circuited through a fault impedance. It has been discussed earlier in Chapter 3 that the generation system of the target dc PSV would comprise of

WRSG interfaced with the 2L-VSC, as shown in Fig. 5.1. It is thus expected that the dc-link capacitor of 2L-VSC will discharge immediately and will form the dominant part of the dc short-circuit current at low-impedance faults. This is followed by the fault current contribution from the interfaced ac generation system. For the generation system comprising of WRSG interfaced with the 2L-VSC, fault currents can be divided into discharge from the dc-link capacitor, generator sub-transient, transient discharge and the steady-state fault current. This is shown in Fig. 5.2. The response of 2L-VSC based dc generation system to an external fault condition is shown in Fig. 5.3 and is explained below.

Stage 1: Before the fault inception, dc-link voltage exceeds the line-to-line voltage of the ac source. The dc-link capacitor discharges almost instantaneously during the fault hence reducing the dc-link voltage. This process is shown in Fig. 5.3(a). The transient dc-link capacitive discharge current becomes a significant portion of the dc fault current (Fig. 5.2), which alone may cause thermal damage to the components in the fault path (especially the dc-link capacitor itself), mechanical damage caused by magnetic forces exerted on conductors and overvoltage damage.

Stage 2: As the dc-link voltage reduces below the line-to-line voltage of the ac source, the generator starts contributing toward the fault current. At this point of time, the

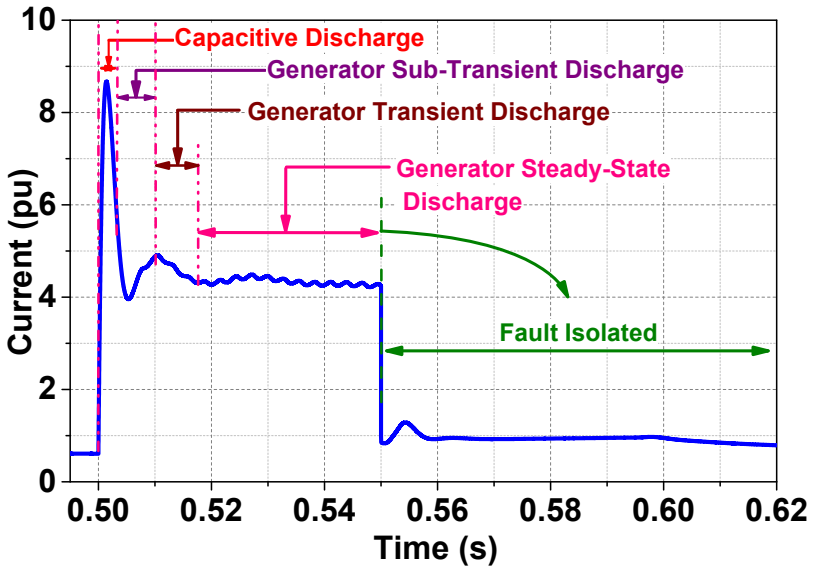
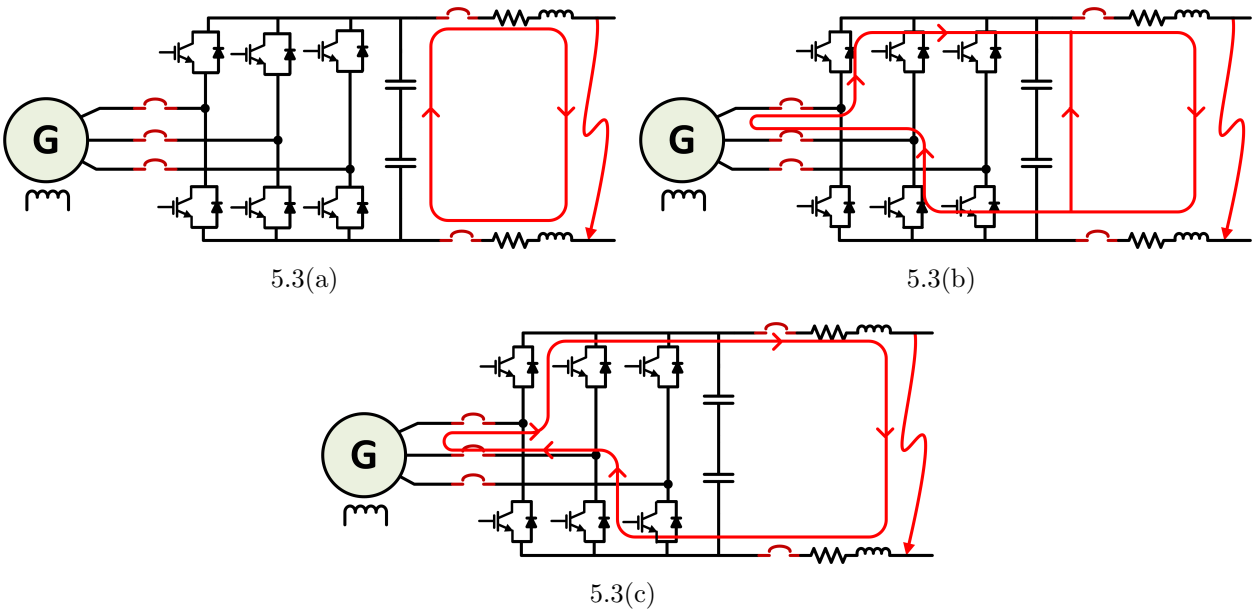


Fig. 5.2: DC fault current contributing sources for low-impedance 0.15Ω fault. (Base current = 1300 A)



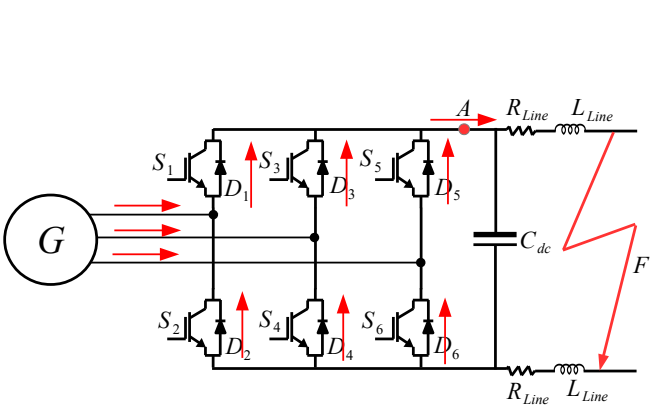
5.3(a) 5.3(b) 5.3(c)

Fig. 5.3: Different stages of fault current, (a) Stage 1, (b) Stage 2, (c) Stage 3.

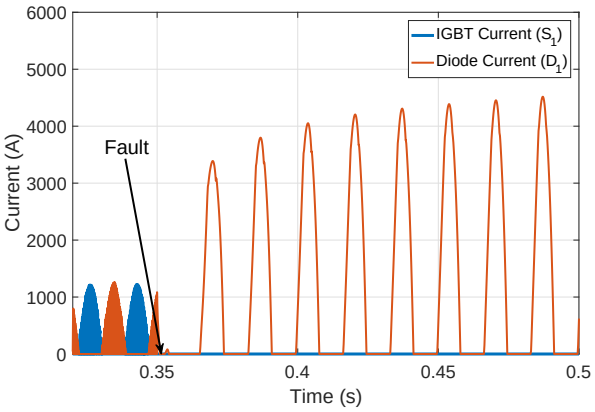
freewheeling diodes are no longer reverse biased, and they start conducting alternatively. The IGBTs will be blocked owing to the overcurrent protection by the gate driver protection circuits. This operation is shown in Fig. 5.3(b).

Stage 3: All the freewheeling diodes are conducting and the generator is essentially in short-circuit condition. The freewheeling diodes start conducting after the IGBTs are suitably blocked. Steady-state fault current flows from the ac generator to the line resistance, leakage inductance and the stray capacitance. The fault current is sustained by the ac source, with the diode bridge in operation. The load in this case is the dc-link capacitor in parallel with the stray inductance, equivalent resistance of the system and fault resistance. This is shown in Fig. 5.3(c).

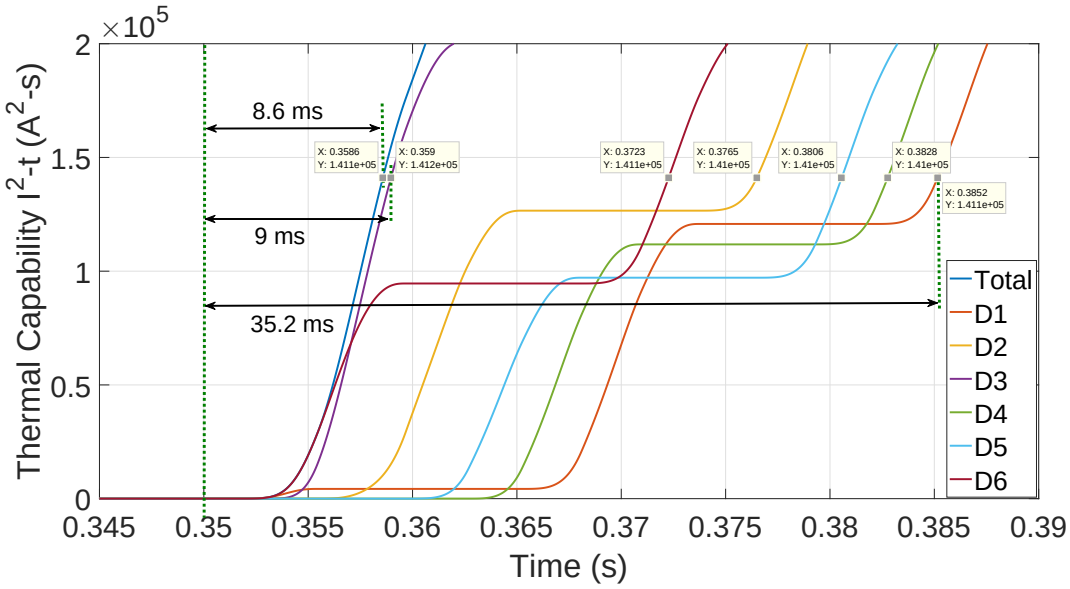
During the dc fault, IGBTs are turned-OFF and freewheeling diodes conduct the steady-state fault current. These freewheeling diodes are damaged when their thermal capability i.e. I^2t exceed the rated value. In this thesis, IGBTs of the interfaced VSC in Fig 5.1 is chosen to be similar to FF1000R17IE4 module [175] whose I^2-t of the freewheeling diode is $1.4\times10^5 A^2$-s. The fault detection algorithm should be able to isolate the fault before thermal limit of $1.4\times10^5 A^2$-s is achieved in any of the freewheeling diodes. During steady-state fault



5.4(a)



5.4(b)



5.4(c)

Fig. 5.4: (a) 2L-VSC during fault condition, (b) current through IGBT (S_1) and diode (D_1) during prefault and fault condition and (c) I^2-t of various freewheeling diodes when fault is initiated at 0.35s. 'Total' represents I^2-t calculated at point-A. [It is assumed that IGBTs are turned-OFF instantaneously after fault inception and fault resistance is 0.1 Ω.]

conditions as shown in Fig. 5.4(a), IGBTs will be turned-OFF and VSC will behave as a three phase diode bridge rectifier with each diode conducting for 180^o depending on the source voltage polarity. The diodes will have discontinuous currents with zero current for brief period of time when it is not forward biased as shown in Fig. 5.4(b).

The thermal capability i.e. I^2-t of the diode is calculated by integrating the square of

current flowing through it and is given by:

$$I^2t_{D_n} = \int I_{Dn}^2 dt \tag{5.1}$$

where, I_{Dn} is the current flowing through the diode under consideration. Different diodes will have different rate-of-rise of fault current as it depends on the fault inception timing and also on the conduction state in the pre-fault condition. During the conduction state, I^2-t will be dependent on the current flowing through the diode. However, when a particular diode does not conduct, the I^2-t will be the previous attained value. Thus, at some points the I^2-t is rising and at some point it is flat as illustrated in Fig. 5.4. However, for the cumulative I^2-t of all the diodes (which is measured before dc-link capacitor at point 'A' shown in Fig. 5.4(a)), current value is generally continuous and hence the I^2-t computed at this point will not have flat regions. Monitoring I^2-t of individual diodes requires additional hardware components which would not be possible for every conditions, thus the cumulative I^2-t at point 'A' can be also used as a requirement for the fault detection algorithms.

Effect of Generation System on Fault Currents

The type of generation system plays an important role in determining the protection requirements. It has been discussed in Chapter 3 that WRSG based generation system would be preferred choice for the diesel engine based prime-movers which is typically used in the PSVs. It has been discussed in Chapter 3 that either automatic flux regulator (AFR) based control or automatic voltage regulator (AVR) based control can be implemented to integrate WRSG with the dc bus. In either of the methods, dc- fault detection and isolation should be done before thermal capability, I^2-t of the freewheeling diodes exceed the rated value. This depends on the in-feed ac fault current supplied by the generation system. In the AFR based method, WRSG is directly interfaced with 2L-VSC whereas for AVR based method, WRSG is interfaced with VSC using additional LC filter. Thus, for dc fault, rate of increase of in-feed ac fault current for AFR based generation system will be higher than the AVR based generation system. In other words, short-circuit current from WRSG is able to damage the freewheeling diodes within very small time duration for AFR based generation system. This is shown in Fig. 5.4(c) where the diode D_6 reaches its thermal capability within 9 ms during low impedance fault (0.1 Ω) at location F_1 of Fig. 5.1 while the cumulative I^2t is reached in

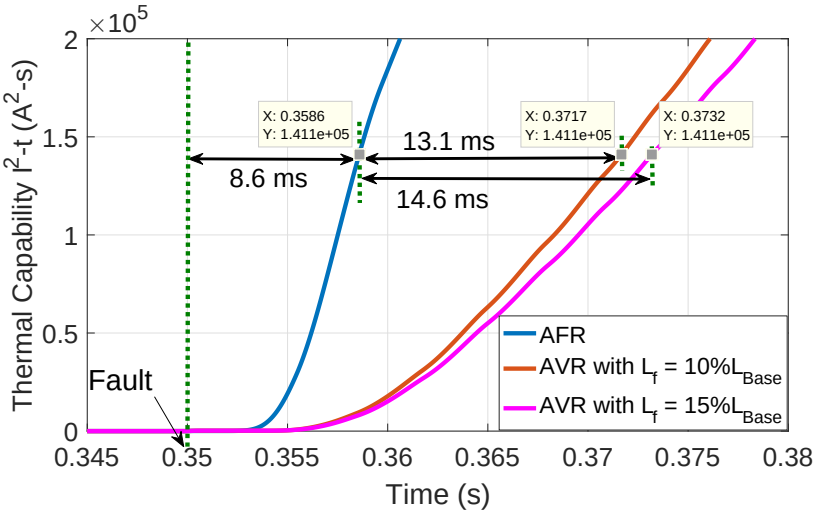


Fig. 5.5: Comparison of the thermal capability (I^2-t) for AFR and AVR based generation system for 0.1Ω fault resistance.

8.6 ms. Cumulative thermal capability of the AFR based system is compared with the AVR based system in Fig. 5.5. For fault impedance of 0.1 Ω at F_1, thermal capability of AFR based system is reached earlier than the AVR based generation system as shown in Fig. 5.5. Thus, a faster protection system is required when AFR based generation is used. For such dc faults, ac side protection is not useful in limiting the I^2-t of the freewheeling diodes. This is because, implementing the ac side protection and isolating the generation system is slow process and takes between 40-60 ms. However, thermal capability of the freewheeling diodes can be limited by modifying the ac side protection which can be implemented by the following methods:

- Simplest way of implementing the ac protection is by oversizing the components (especially the freewheeling diodes) of the interfaced converters. Oversizing is done in such a way that the operation of ac side protection will be faster than the time required to reach the thermal limits of the freewheeling diodes. This will make the converters quite expensive as we need to design the converter for worst transient conditions.

- Protective inductors can be integrated with the ac or dc side to limit the rate of rise of the fault current. In such way, the time required to achieve the thermal limits can be delayed. However, introducing the additional inductors may change the operational dynamics of the converters and also increase the converter size.

- Another way of achieving the ac side protection is by application of thyristor-based crowbar circuits as discussed in Section 2.8.2. The thyristors are turned-ON when the dc fault condition is detected. Thus, the dc fault is transformed into ac fault which is isolated by the ac breakers. For such operation, the thyristors should be adequately thermally-rated to accommodate the three-phase short-circuit currents.

It is seen that the protection from ac side is not a convenient solution for dc SPS. It requires certain modifications which will increase the cost and space of the generation systems. Moreover, isolating the generation systems for faults in the networks of dc PSV will result in complete power loss and blackout which will not be a favourable choice for the dc SPS undergoing marine missions. In Chapter 3 it was concluded that the AFR based generation system would be favourable choice for the dc SPS and thus is considered in this thesis. From Fig. 5.5, it can be concluded that faster protection algorithms are needed to detect the dc faults. Thus, the time needed to detect the fault should be within $\leq$ 5ms to satisfactorily detect the low-impedance faults.

5.3.2 Fault Current Calculations

The components in the ac systems such as transformers, generators, motors etc. are more rugged and can withstand short-time overcurrent transients. As a result, the steady-state fault currents are used to detect the fault condition and also to develop the protection coordination algorithms. On the other hand, in a dc system, transient discharge from the dc-link capacitor is dominant for low-impedance faults. Such transient responses can be utilized for fault detection and protection settings. Further, in the dc system, power electronic interfaces are prone to damage by the overcurrents from ac side. Thus, fault condition must be detected during dc-link capacitor discharge in *Stage 1* of the fault current, as discussed in Section 5.3.1.

Discharge through the dc-link capacitor is illustrated using the transient dc circuit of a single generation system as shown in Fig. 5.6. In Laplace-domain, fault current contribution from the dc-link capacitor can be given as:

$$I_f(s) = \frac{\frac{V(0+)}{s} + LI(0+)}{sL + \frac{2R + R_f}{2} + \frac{1}{sC}}. \tag{5.2}$$

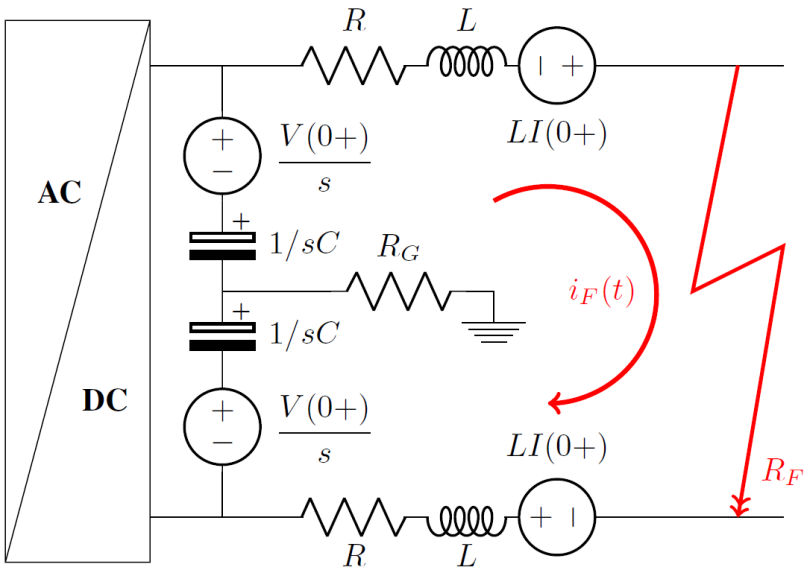


Fig. 5.6: Transient dc circuit of a dc generation system to analyse the capacitive discharge in the dc fault current.

where, $V(0+)$ is the initial voltage of the dc-link capacitor (C) and $I(0+)$ is the initial current flowing through line inductance (L). This fault current equation can be reduced to:

$$I_f(s) = \frac{\frac{V(0+)}{L} + sI(0+)}{s^2 + \frac{2R + R_f}{2L} + \frac{1}{LC}}. \tag{5.3}$$

Depending on the fault resistance and fault location, the nature of fault current may be overdamped or underdamped. From (5.3), overdamped (o.d.) condition is reached when $(2R + R_f)/4L > 1/\sqrt{LC}$. Underdamped (u.d.) condition is reached when $(2R + R_f)/4L < 1/\sqrt{LC}$. The fault current for the *o.d.* and *u.d.* fault currents are shown below.

Overdamped Fault Currents:

The fault current in (5.3) can be written as:

$$I_f(s) = \frac{\frac{V(0+)}{L}}{s^2 + \frac{2R + R_f}{2L} + \frac{1}{LC}} + \frac{sI(0+)}{s^2 + \frac{2R + R_f}{2L} + \frac{1}{LC}} \tag{5.4}$$

As discussed overdamped fault condition occurs when $(2R + R_f)/4L > 1/\sqrt{LC}$ and thus results in positive roots $m_{1,2}$ of denominator of (5.3) and is given by:

$$m_{1,2} = \frac{2R + R_f}{4L} \mp \sqrt{\left(\frac{2R + R_f}{4L}\right)^2 - \frac{1}{LC}} \tag{5.5}$$
$$= \alpha \mp \beta$$

where, $\alpha = \dfrac{2R + R_f}{4L}$, $\beta = \sqrt{\alpha^2 - \dfrac{1}{LC}}$

Thus, (5.4) can be expressed as:

$$I_f(s) = \frac{\dfrac{V(0+)}{L}}{(s + m_1)(s + m_2)} + \frac{sI(0+)}{(s + m_1)(s + m_2)} \tag{5.6}$$

This can be re-arranged as:

$$I_f(s) = \frac{V(0+)}{L}\frac{1}{(m_2 - m_1)}\left(\frac{1}{(s + m_1)} - \frac{1}{(s + m_2)}\right) + \frac{I(0+)}{(m_2 - m_1)}\left(\frac{m_2}{s + m_2} - \frac{m_1}{s + m_1}\right) \tag{5.7}$$

Taking inverse Laplace of $I_f(s)$, $\mathscr{L}^{-1}\{I_f(s)\}$, $i_f(t)$ is calculated as:

$$i_f(t) = \frac{V(0+)}{L}\frac{1}{(m_2 - m_1)}\left(e^{-m_1 t} - e^{-m_2 t}\right) + \frac{I(0+)}{(m_2 - m_1)}\left(m_2 e^{-m_2 t} - m_1 e^{-m_1 t}\right) \tag{5.8}$$

Replacing $m_{1,2}$ using (5.5), $i_f(t)$ is given as:

$$i_f(t) = \frac{V(0+)}{2\beta L}\left(e^{-(\alpha-\beta)t} - e^{-(\alpha+\beta)t}\right) + \frac{I(0+)}{2\beta}\left((\alpha + \beta)e^{-(\alpha+\beta)t} - (\alpha - \beta)e^{-(\alpha-\beta)t}\right) \tag{5.9}$$

$$i_f(t) = \frac{e^{-\alpha t}}{2\beta}\left[\frac{V(0+)}{L}\left(e^{\beta t} - e^{-\beta t}\right) + I(0+)\left((\alpha + \beta)e^{-\beta t} - (\alpha - \beta)e^{\beta t}\right)\right] \tag{5.10}$$

Underdamped Fault Currents:

Underdamped fault condition occurs when $(2R + R_f)/4L < 1/\sqrt{LC}$ and thus results in imaginary roots $m_{1,2}$ of denominator of (5.3) and is given by:

$$m_{1,2} = \frac{2R + R_f}{4L} \mp j\sqrt{\frac{1}{LC} - \left(\frac{2R + R_f}{4L}\right)^2} \tag{5.11}$$
$$= \alpha \mp j\omega_d$$

where, $\alpha = \dfrac{2R + R_f}{4L}$, and $\omega_d = \sqrt{\dfrac{1}{LC} - \alpha^2}$. Fault current is (5.3) is written as:

$$I_f(s) = \frac{\dfrac{V(0+)}{L} + sI(0+)}{(s + m_1)(s + m_2)} \tag{5.12}$$

Replacing $m_{1,2}$ using (5.11), $I_f(s)$ is given as:

$$I_f(s) = \frac{\dfrac{V(0+)}{L} + sI(0+)}{(s + \alpha - j\omega_d)(s + \alpha + j\omega_d)} \tag{5.13}$$

$$I_f(s) = \frac{\dfrac{V(0+)}{L} + sI(0+)}{(s + \alpha)^2 + \omega_d^2} \tag{5.14}$$

$$I_f(s) = \frac{\dfrac{V(0+)}{L}}{(s + \alpha)^2 + \omega_d^2} + \frac{(s + \alpha)I(0+)}{(s + \alpha)^2 + \omega_d^2} - \frac{\alpha I(0+)}{(s + \alpha)^2 + \omega_d^2} \tag{5.15}$$

Taking inverse Laplace transform $\mathscr{L}^{-1}$ of $I_f(s)$, $\mathscr{L}^{-1}\{I_f(s)\}$, $i_f(t)$ is given as:

$$i_f(t) = \mathscr{L}^{-1}\left\{ \frac{\dfrac{V(0+)}{L}}{(s + \alpha)^2 + \omega_d^2} + \frac{(s + \alpha)I(0+)}{(s + \alpha)^2 + \omega_d^2} - \frac{\alpha I(0+)}{(s + \alpha)^2 + \omega_d^2} \right\} \tag{5.16}$$

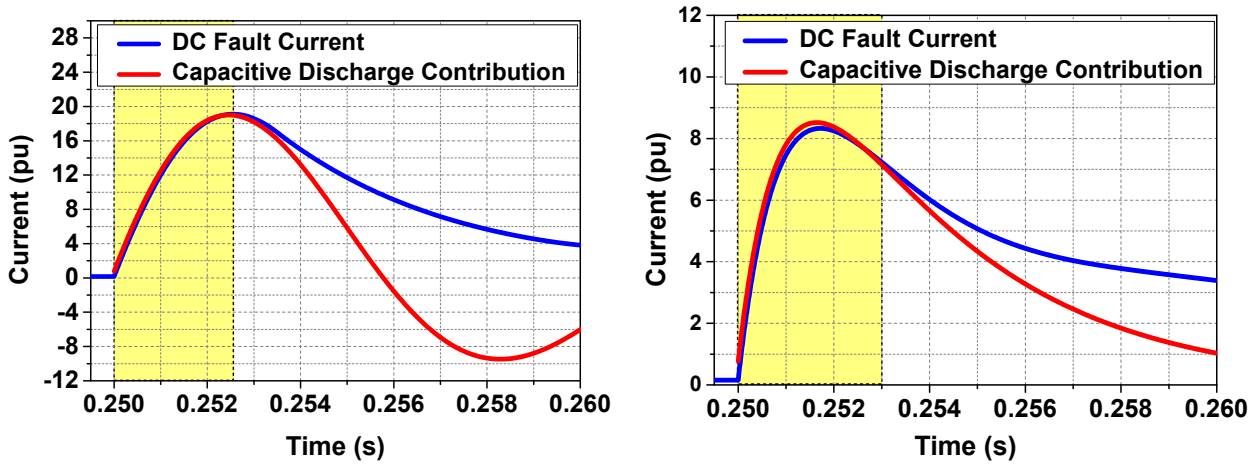
This can be reduced to:

$$i_f(t) = e^{-\alpha t}\left\{ \left(\frac{V(0+)}{\omega_d L} - \frac{I(0+)\alpha}{\omega_d} \right) \sin \omega_d t + I(0+) \cos \omega_d t \right\} \tag{5.17}$$

Contribution of the capacitive discharge as per (5.10) and (5.17) to the dc fault current is shown in Fig. 5.7. It shows a good agreement between the simulation and analytical results confirming the dominance of capacitive discharge at low-impedance faults.

5.3.3 Influence of Fault Resistance and Location

A low-impedance fault is characterized by the dc-link capacitor discharge; however, the dc generation system may see a high-impedance fault as load change with no significant contribution from the dc-link capacitor. Thus, the study on the effect of the fault current due to varying fault resistance and location is imperative to formulate the fault detection algorithms



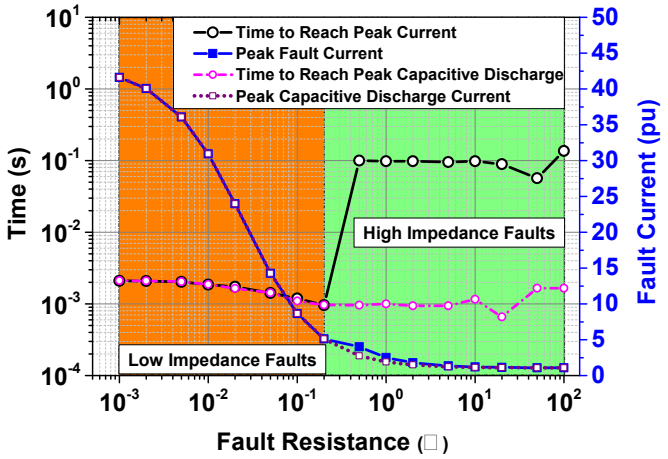
5.7(a) 5.7(b)

Fig. 5.7: DC fault current and contribution of the capacitive discharge in dc fault current for (a) underdamped fault condition (0.01 Ω fault resistance) and (b) overdamped fault condition (0.15 Ω fault resistance). The highlighted area shows the time till which the capacitive discharge current is dominant in the dc fault current.

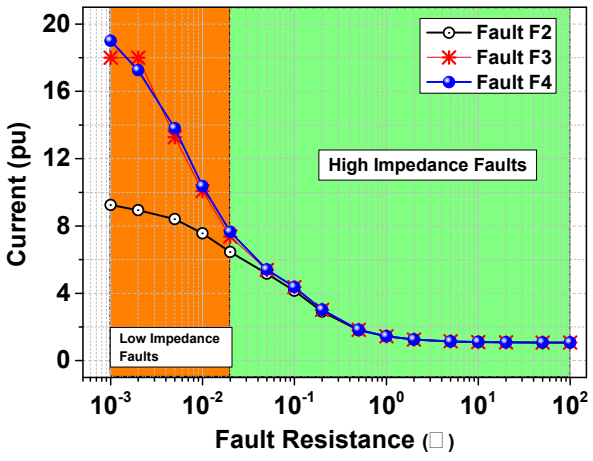
while identifying their limitations at the same time. This approach has not been widely used in the existing literature, as the bolted short-circuit fault study has predominantly been the prime focus. In this chapter, the full fledged dc PSV model has been taken into account and the faults of varying resistances are initiated at locations the plausible fault locations F_1, F_2, F_3 and F_4, as shown in Fig. 5.1.

For the fault F_1, the peak current and time to reach the peak current for various fault resistances observed by VSC-1 are shown in Fig. 5.8(a). The fault currents for low-impedance faults are dominated by the transient discharge of the dc-link capacitor, thus taking less time to reach the peak as shown in Fig. 5.8(a). As the fault resistance is increased, the magnitude of the capacitive discharge is lower than the fault current supplied from the ac side (G1) and thus it takes longer time to reach the peak fault current. Although the time required to reach the peak capacitor discharge is similar to that of low-impedance faults; it is the time to reach the peak fault current that increases. As seen from Fig 5.8(a), the transition from the low-impedance to high-impedance fault is observed by the increased time required to reach the peak fault current. Compared to low-impedance faults, there is a jump in peak fault current detection of magnitude of 10 for high-impedance fault currents.

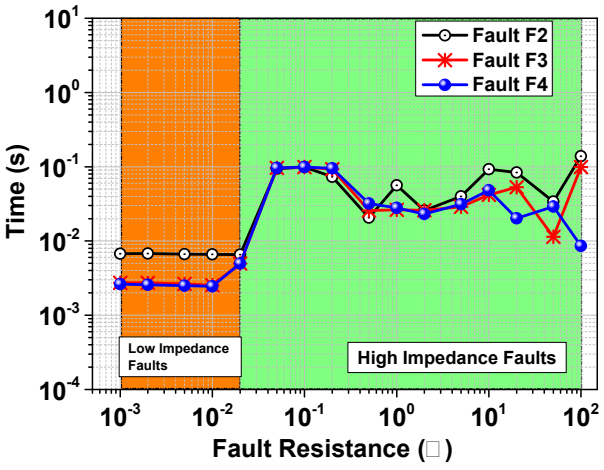
The variations of the magnitude and time to reach the peak fault current, as observed by VSC-1 for various fault resistances at different fault locations F_2, F_3 and F_4, are depicted in Figs. 5.8(b) and 5.8(c), respectively. The magnitude of the peak fault current decreases as the fault location is further from the G1 generating source. As compared to the characteristic of fault F_1 in Fig. 5.8(a), the transition from low- to high-impedance fault is reached earlier at lower fault resistance values due to the impact of the line lengths. As expected, the faults at generator terminals are more detrimental as compared to the faults elsewhere in



5.8(a)



5.8(b)



5.8(c)

Fig. 5.8: (a) Peak fault current and time required to reach the peak current for fault F_1, as seen from VSC-1. (b) Peak current and (c) time required to reach the peak current for various fault resistances for fault locations F_2, F_3 and F_4.

the system due to lower line lengths and higher fault current magnitudes.

5.3.4 Effect of the Loads and System Configuration

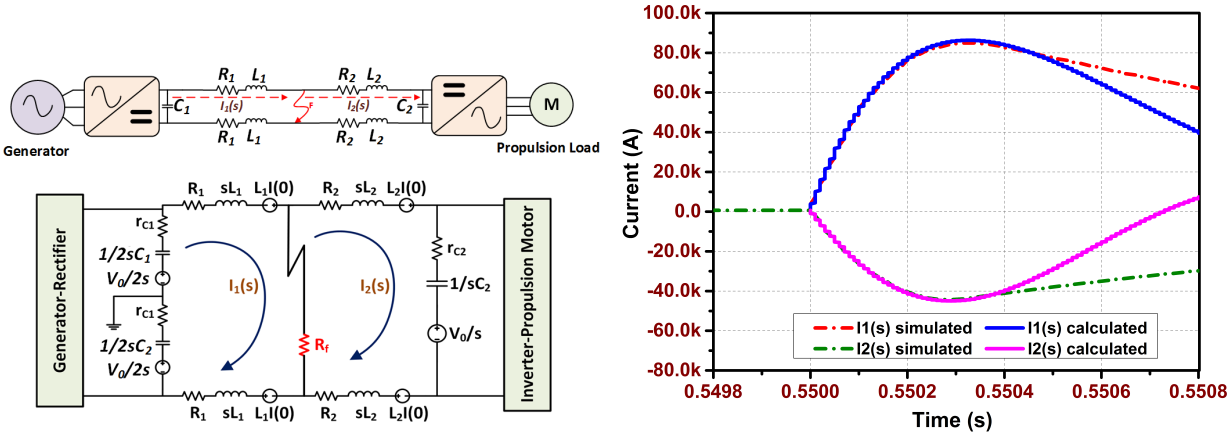
It has been discussed in Chapter 3 and Chapter 4 that the dc-link capacitor is an important design parameter as it is the dc-link voltage that is regulated by the generator facing converters. The loads of the dc PSV comprise of the inverter-fed propulsion and hotel loads which also have input dc-link capacitors. During the faults, the dc-link discharge from the dc generation and loads will become the dominant part of the dc short-circuit current. The intensity of the dc fault current varies with the number of interconnected generators and loads, which is dependent on the marine mission and associated system configuration which is further detailed in Section 5.3.4. In this thesis, the dc-link capacitor of the converters are designed according to the power hold-up time ($t_{\text{hold up}}$) [77]. It has already been discussed in Section 5.3.1 that 5 ms is the available time within which the I^2t of the freewheeling diode will be exceeded during bolted short-circuit faults. To support the availability of power in such condition, the $t_{\text{hold up}}$ is set to 5 ms. The expression to derive the dc-link capacitor according to $t_{\text{hold up}}$ is given by the following:

$$\frac{C({V_1}^2 - {V_2}^2)}{2} = P.\ t_{\text{hold up}} \tag{5.18}$$

where, $t_{hold\ up}$ is set to be 5 ms, $V_1 = 1500\ V$ and $V_2 = 0.8V_1$, which is in-line with the performance of commercial drives. For propulsion systems, the dc-link capacitor is calculated to be 10 mF, and for generation systems, the dc-link capacitor is calculated to be ≈25 mF.

To illustrate the effect of faults on the loads of the marine vessels, transient analysis has been done with the system comprising of one generator interfaced converter connected with an inverter fed propulsion load, as shown in Fig. 5.9. Referring to Fig. 5.9(a), the Laplace transform of the bolted short-circuit fault current $I_1(s)$ and $I_2(s)$ resulting from capacitive discharge of the generation system and propulsion load, respectively, can be expressed as:

$$I_1(s) = \frac{\dfrac{V(0+)}{2L_1} + s\ I(0+)}{s^2 + s\dfrac{R_1 + r_{c1}}{L_1} + \dfrac{1}{2L_1C_1}}, \tag{5.19}$$



5.9(a) 5.9(b)

Fig. 5.9: (a) DC SPS comprising of one generation and one load unit with its equivalent circuit during capacitive discharge, (b) comparison of simulated and calculated values of $I_1(s)$ and $I_2(s)$ during bolted short-circuit fault.

$$I_2(s) = \frac{\dfrac{-V(0+)}{2L_2} + s\ I(0+)}{s^2 + s\dfrac{2R_2 + r_{c2}}{2L_2} + \dfrac{1}{2L_2C_2}}. \tag{5.20}$$

The dc-link capacitor of the 2L-VSC is denoted by 'C', the line resistance and inductance are indicated by 'R' and 'L', 'R_f' is the fault resistance, '$V(0+)$' and '$I(0+)$' are the initial voltages and currents through the dc-link capacitor and the line inductor. The nature of the fault current from the dc-link can be under-damped or over-damped depending on the fault resistance, fault location and circuit configurations. For $i_1(t)$, the overdamped condition is achieved when $\left(\dfrac{R_1 + r_{c1}}{L_1}\right)^2 > \dfrac{2}{L_1C_1}$ and the fault current discharge from the dc-link capacitor can be calculated as per Section 5.3.2 and is given by:

$$i_1(t) = \frac{e^{-\alpha_1 t}}{2\beta_1}\left[\frac{V(0+)}{L_1}\left(e^{\beta_1 t} - e^{-\beta_1 t}\right) + I(0+).\left((\alpha_1+\beta_1)e^{-\beta_1 t} - (\alpha_1-\beta_1)e^{\beta_1 t}\right)\right], \tag{5.21}$$

For $i_1(t)$, the underdamped condition is achieved when $\left(\dfrac{R_1 + r_{c1}}{L_1}\right)^2 < \dfrac{2}{L_1C_1}$ and the fault current is given by:

$$i_1(t) = e^{-\alpha_1 t}\left[\left(\frac{V(0+)}{\omega_{d1}L_1} - \frac{I(0+)\alpha_1}{\omega_d}\right)\sin\omega_{d1}t + I(0+).\cos\omega_{d1}t\right], \tag{5.22}$$

where, $\alpha_1 = \dfrac{R_1 + r_{c1}}{2L_1}$, $\beta_1 = \sqrt{\Big(\dfrac{R_1 + r_{c1}}{2L_1}\Big)^2 - \dfrac{1}{2L_1C_1}}$ and $\omega_{d1} = \sqrt{\dfrac{1}{2L_1C_1} - \Big(\dfrac{R_1 + r_{c1}}{2L_1}\Big)^2}$.

Similarly, for $i_2(t)$, the overdamped current is given by the following:

$$i_2(t) = \frac{e^{-\alpha_2 t}}{2\beta_2}\left[- \frac{V(0+)}{L_2}\left(e^{\beta_2 t} - e^{-\beta_2 t}\right) + I(0+).\left((\alpha_2 + \beta_2)e^{-\beta_2 t} + (\alpha_2 - \beta_2)e^{\beta_2 t}\right)\right]. \quad (5.23)$$

And for $i_2(t)$, the underdamped condition is given as following:

$$i_2(t) = e^{-\alpha_1 t}\left[- \left(\frac{V(0+)}{\omega_{d2}L_2} + \frac{I(0+)\alpha_1}{\omega_d}\right)\sin\omega_{d2}t + I(0+)\cos\omega_{d2}t\right], \quad (5.24)$$

where, $\alpha_2 = \dfrac{2R_2 + r_{c2}}{4L_2}$, $\beta_2 = \sqrt{\Big(\dfrac{2R_2 + r_{c2}}{4L_2}\Big)^2 - \dfrac{1}{2L_2C_2}}$ and $\omega_{d2} = \sqrt{\dfrac{1}{2L_2C_2} - \Big(\dfrac{2R_2 + r_{c2}}{4L_2}\Big)^2}$.

There is a good agreement between the analytical and simulated dc-link discharge, as shown in Fig. 5.9(b), till the dc-link discharge is dominant.

It is further seen that the fault current is dependent on the magnitude of dc-link capacitor as seen from the expressions of β and ω for over-damped and under-damped fault conditions respectively. Thus, although the $t_{hold-up}$ could be set to a higher value (5.18), it will increase the value of dc-link capacitor which in-turn increase the fault current as shown in Fig. 5.10. In other words, $t_{hold-up}$ directly influences the fault current during low-impedance faults. Increasing the dc-link capacitor will not significantly alter the cost or size of the high power converter in dc SPS, it will increase the fault current contributions from it. To accommodate such increased fault currents, sizing of the network components such as bus-bars, cables should be improved accordingly. Thus, the cost of the dc SPS will increase in indirect way.

During the low-impedance faults, current from the propulsion load reverses owing to low-impedance fault, which is inferred by the negative magnitude of $i_2(t)$. To further understand the influence of the low-impedance pole-to-pole faults, Fig. 5.11(a) is taken into consideration which depicts a smaller part of the dc PSV (in Fig. 5.1). A pole-pole fault is initiated at $t = 0.25\ s$ at point F_1, which is the dc power cable connecting Gen-1 with the dc bus. Fig. 5.11(b) shows the direction of current during fault F_1 when simulated without any protection algorithm. It can be observed that during the fault F_1, the dc-link capacitors

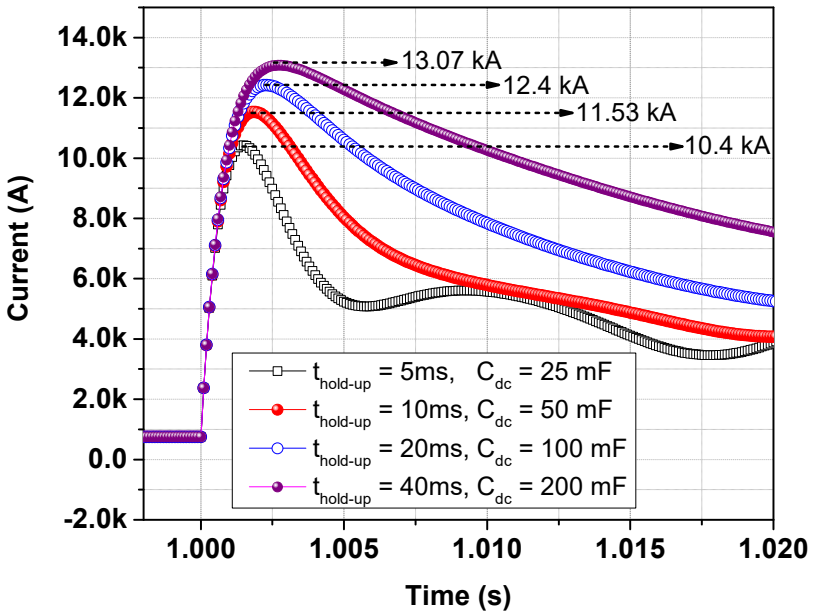
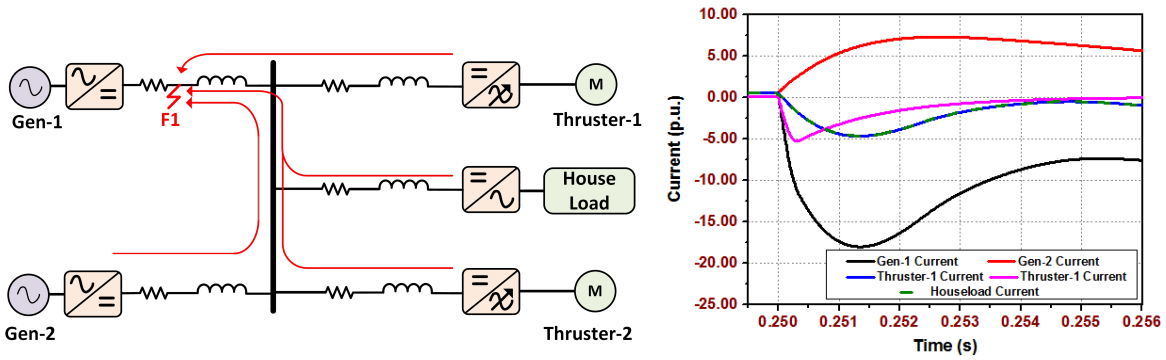


Fig. 5.10: Fault currents indicating the peak magnitudes when $t_{hold-up}$ is increased by increasing the value of dc-link capacitor (C_{dc}).



5.11(a) 5.11(b)

Fig. 5.11: Direction of flow of faulted current during fault F1.

of the motor loads (Thruster 1& 2), Gen-2 and the house-load discharge at the fault point. The current direction of the motor loads and house-load change from its normal path to the opposite direction. This change in the fault current direction becomes the basis of the directional protection scheme in the dc SPS.

The change in current direction or current reversal during the fault severely impacts the operation of the propulsion system. The effect on the operation of Thruster-1 is shown in Fig. 5.12(a). It can be seen that during the fault F_1, the dc-link voltage collapses, the torque

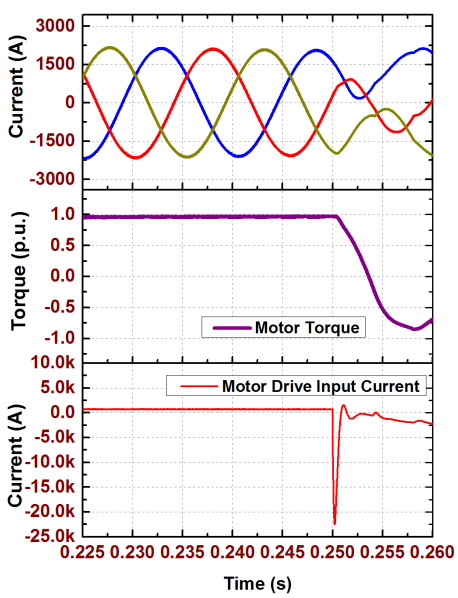
becomes negative and the motor regenerates into the bus. If the negative fault current were blocked, then the motor would work quite normally for a short period of time depending on the hold-up time of the dc-link capacitor which is shown in Fig. 5.12(b). From the Fig. 5.12(c), it can be seen that the negative current is blocked at 0.25 s and the motor runs normally till 0.2627 s, where effective control is lost and the motor current and torque collapses. This is because the dc-link capacitor is completely discharged in 12.74 ms (5.18). Blocking the dc-link discharge from such active loads is advantageous as the severity of fault current at F_1 is further reduced when the reverse current is blocked as seen from Fig. 5.12(d).

The intensity of the fault current is dependent on the system configurations as well. An example of different cases of marine missions such as DP, cruising and dock conditions are shown in Table 5.1, which have different combinations of generators and loads. Fault F_3 of fault resistance 0.1 Ω is initiated and the magnitude and time to reach the peak fault current flowing through IED5 and IED15 are listed in Table 5.2. The peak fault current for Case 4 (Table 5.2) is higher than that of Case 1, as it has a higher number of connected generation and load systems. The time required to reach the peak fault current is dependent on the number of capacitors being discharged along with their rise time. The adverse impacts of the fault current can be reduced, provided the fault current contributions from the active loads are blocked, which is seen by a significant reduction in the peak fault current, as shown previously in Fig. 5.12(d) and also in Table 5.2. To block the fault currents, the fault isolating devices for the load systems is expected to have a different architecture as compared to the generation, lines and bus-bar ones.

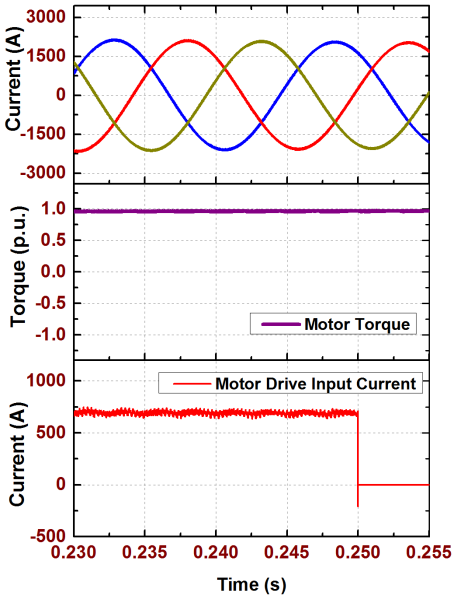
It can be deduced from Table 5.2 that the fault current is dependent on the system configuration. The OC protection with adaptive tripping setpoints would be suitable for

Table 5.1: System Configuration for Different Marine Missions

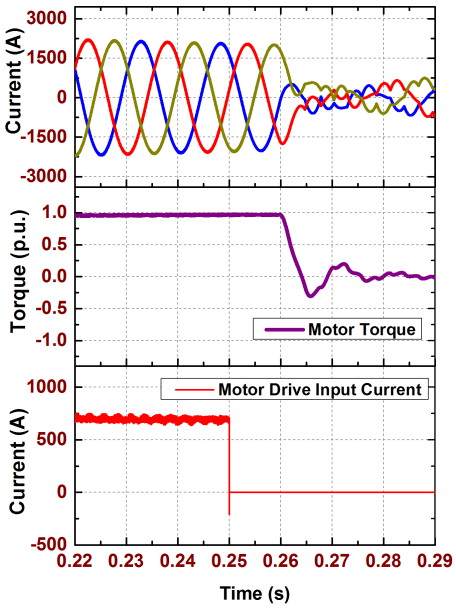
Case	**Operating Mode & Load**	**Generator Combination**	**Load Combination**
1	DP: 1500 kW	G1	RT,HL1,HL2
2	DP: 2500 kW	G1,G2	TT1,TT2,RT, HL1, HL3
3	Cruising: 5000 kW	G1,G2,G3	MP1,MP2,HL1,HL2
4	Cruising: 6000 kW	G1,G2,G3,G4	MP1, MP2,HL1,HL3
5	At Dock: 100 kW	G1	HL1, HL2
6	At Dock: 500 kW	G1	HL1, HL2, HL3



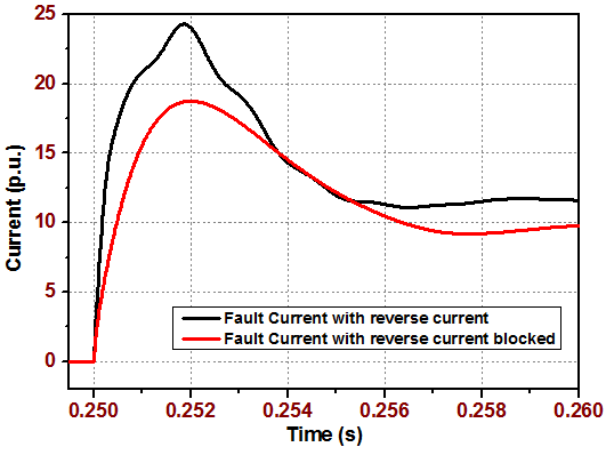
5.12(a)



5.12(b)



5.12(c)



5.12(d)

Fig. 5.12: Thruster-1 (a) motor current, motor torque and motor drive input current during fault F_1, (b) motor current, motor torque and motor drive input current when negative current is blocked during fault F_1, (c) motor current, motor torque and motor drive input current for sustained fault F_1 with negative current blocked and (d) severity of fault current with and without blocking reverse current.

Table 5.2: Fault Current Flowing Through IED5 and IED15 before and after the Active Loads are Blocked

Case	Mode	IED5		IED15	
		i_{peak} (kA)	t_{peak} (ms)	i_{peak} (kA) **	t_{peak} (ms)
1(a)	Before Blocking	35.57	0.59	-11.78	0.59
1(b)	After Blocking	17.56	3.00	-5.34	2.90
2(a)	Before Blocking	39.72	3.20	-27.74	3.40
2(b)	After Blocking	30.23	2.80	-9.78	2.80
3(a)	Before Blocking	62.79	3.00	-20.54	3.00
3(b)	After Blocking	40.60	2.70	-13.13	2.70
4(a)	Before Blocking	63.31	2.90	-24.97	0.59
4(b)	After Blocking	48.12	2.60	-16.04	2.60
5(a)	Before Blocking	33.90	0.59	-11.24	0.59
5(b)	After Blocking	17.45	3.00	-5.30	2.90
6(a)	Before Blocking	34.62	0.59	-23.59	0.49
6(b)	After Blocking	17.33	3.10	-8.15	0.09

**: Current direction through IED15 changes during fault.

such scenarios. However, this approach is limited by the optimisation requirements of the tripping setpoints for each marine missions. It is thus necessary to implement a protection system with preferably a fixed setpoint.

5.3.5 Choosing the Selectivity for Protection Coordination

Selectivity in AC systems

In ac power systems, the protection set-points are determined using the steady-state fault currents. Traditionally, the IEDs are chronometrically coordinated, i.e., time-current based selectivity is employed. This is in accordance with the IEC 60255-3 [176] and is prevalent for longer inductive lines where the close-in and far-end faults have significantly different magnitudes. On the other hand, fixed current and time set-point based 'definite mean time' tripping of IEDs are implemented for smaller ac systems having shorter line lengths. Additionally, directional element has been popularly integrated for enhanced selective operation in such smaller systems comprised of multiple generation units and loads [177]. This combination of directional element working in conjunction with the OC scheme is popularly termed as directional protection. During the fault, directional relay determines the fault direction

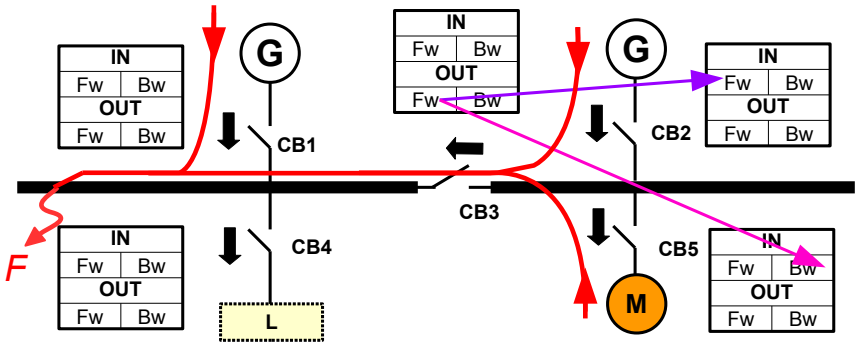


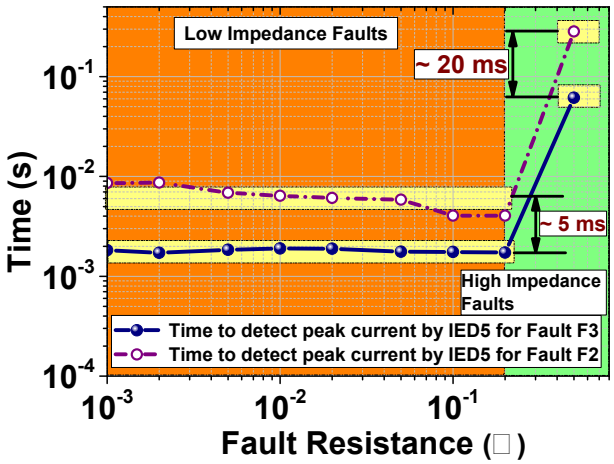
Fig. 5.13: Diagram of directional selectivity in ac system.

while the fixed set-point OC relay issues the trip command either in the forward or reverse direction. For illustration, the ac system with the direction of prefault current is depicted in Fig. 5.13. When the fault (F) is at busbar, the IED of CB3 detects forward fault and blocks the CB2 and CB5 in forward and reverse direction, respectively. Thus, the CB3 trips in the time set by its forward time delay. The directional selectivity prevents from false-tripping of the CBs but rather dictates the CBs to operate within its time settings defined by forward or reverse operation mode.

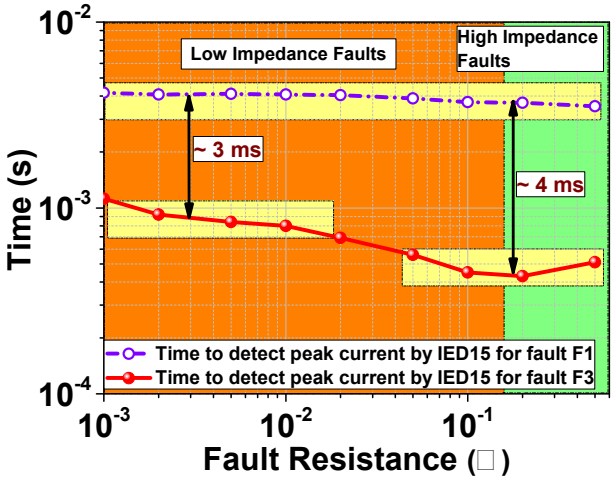
Selectivity in DC systems

For the dc PSV with shorter line lengths and inductances, the time to reach the peak fault current is expected to be in the similar range for both close-in and far-end faults resulting in similar tripping times. Thus, it becomes difficult to coordinate the multiple IEDs considering such time constraints. This is illustrated by the operation of IED5 and IED15 (of Fig. 5.1) in Fig. 5.14. IED5 should be able to discriminate between the faults F_2 and F_3, while the IED15 should be able to discriminate between the faults F_1 and F_3. The time required to reach the peak fault current by IED5 and IED15 (Fig. 5.1) is shown in Figs. 5.14(a) and 5.14(b), respectively. It is noted that the IEDs must be able to discriminate the faults in the range of few milliseconds, which is almost in the same time range. Thus, a directional based selectivity could be suitable choice for the selective protection and for the protection co-ordination in the dc PSV.

Differential protection based selective operation can also be used for dc SPS. It requires communication infrastructure which can be implemented in smaller sized dc SPS. However,



5.14(a)



5.14(b)

Fig. 5.14: Fault impedance of 0.1 Ω for F2 and F3. Time required by (a) IED5 and (b) IED15.

differential protection needs to exchange the time-stamped current signals between the IEDs. This requires communication protocol and infrastructure which is not yet standardized for dc protection. As the time required for fault detection is set to 5 ms, the communication system should be very fast which is another challenge. On the contrary in the directional protection, the direction status signals are exchanged as compared to the time-stamped signals in differential protection.

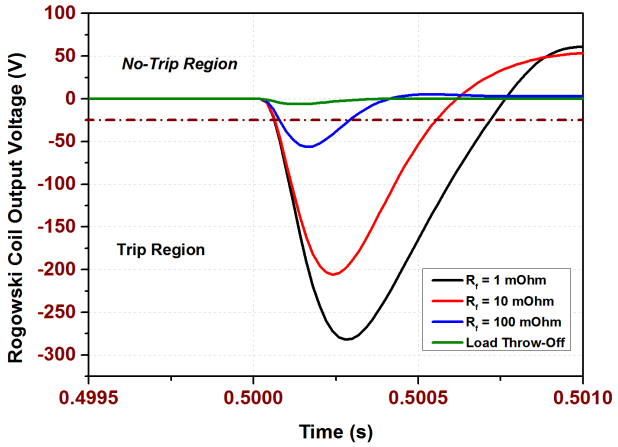
5.3.6 Rogowski Coil as Current Sensing Element for Fault Current Detection

For ac power systems, there are a variety of current sensors available which can be utilized for transient state detection. The sensors include the shunt resistors, current transformers (CTs), hall effect sensors, Rogowski coils (RCs) etc. For dc systems, hall-effect based sensors are predominantly used as other magnetic core-based current sensors are prone to saturation during the dc faults. However, RC can be used in dc system to measure the transient currents due to absence of magnetic materials which results in lack of saturation problem and linear operation. It has been mostly used to measure ac currents and high-speed impulse currents. RC is however, not suitable to measure the steady-state dc current or slow changing dc load currents. Thus, for steady-state operation different current sensors (preferably Hall-effect based sensors) would be used while RCs will only be used to detect the transient conditions. This protection operation will be similar to the protection of ac systems where different types and classes of sensors are used for measurement and protection purpose.

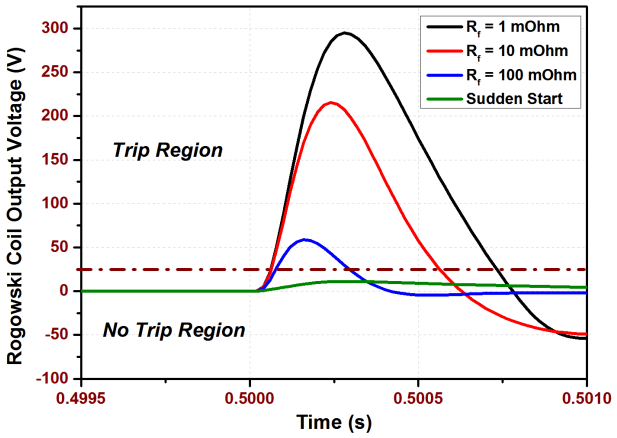
Different types of RCs, their construction and operating principles along with the modeling techniques have been described in detail in Chapter 2. To understand the effectiveness of the RC for fault detection, its lumped model with maximum number of turns (= 150) has been used in this chapter. RC is integrated with IED1 shown in Fig. 5.1 to detect the current flow during pole-pole fault '$F1$' and $F2$. The output of RC at IED1 for various transient conditions at '$F1$' and '$F2$' are shown in Fig. 5.15(a) and Fig. 5.15(b) respectively. The output voltage of the RC increases for low-impedance faults while is insignificant for sudden load change. Thus, set-points are needed to discriminate between '*Trip Region*' and '*No-Trip Region*'. In this chapter, the setpoint is considered as 25 V. It would be dependent on the maximum load switching such as the pulsed loads which are expected in the system.

5.4 Protection Requirements for DC PSV and Motivation for Frequency-Domain Based Fault Detection Techniques

In Section 5.3, time-domain based fault analysis of dc PSV is carried out for a range of fault impedances when incepted at different plausible locations. Based on the fault analysis the following observations are cited:



5.15(a)



5.15(b)

Fig. 5.15: Comparison of RC output for different type of fault and transient conditions at (a) point $F1$ and (b) $F2$.

(i) For the low-impedance faults, the intensities of the fault currents are similar at all locations. This is due to the compact power system architecture of the dc SPS. As a result, all the IED will detect similar overcurrent (OC) magnitudes.

(ii) When compared to the dc power systems for transmission applications such as the high-voltage dc (HVDC) systems, protective inductors have been traditionally used to restrict the amount of fault current. However, dc SPS is quite smaller in size as compared to the HVDC systems, and the voltage levels in dc SPS can be 500× lower than the HVDC system. As a result, the magnitude of fault currents in dc SPS would be very less when compared to the HVDC applications. For these reasons, protective inductors are found suitable to limit the higher magnitude of fault current in the HVDC systems and subsequently applying OC based protection. Being a transmission system, HVDC systems have fixed system topology for normal operating conditions. The peak transient currents are expected to be constant which is used to design and select the protective inductors. On the contrary, dc SPS is a distribution network where the system topology changes with the marine missions. As a result, magnitude of fault current also changes with the system configuration as described in Section 5.3.4. This sets up difficulty in choosing the protective inductors for dc marine applications. If the protective inductors are chosen as per the worst transient condition, its working may

be prohibitive in the system configuration comprising of less number of generators and load systems.

(iii) If there are no protective inductors, OC based protection is challenging to implement. The changing system configuration depending on the marine mission changes the fault current intensities. Thus, a particular IED will have different current magnitudes for similar fault impedances when incepted for different marine missions. This difference in current further enhanced when the loads are blocked to restrict the fault current. This is discussed in Table 5.2. Thus, for successful operation of the OC protection (with or without the protective inductors), the tripping set-points should be optimized for each marine mission.

(iv) It is thus required to design a fault detection algorithm which would not require optimised set-points but rather a fixed tripping threshold. With such requirements, the frequency-domain analysis of the rapidly rising fault currents is expected to have high-frequency components, which might be effective indicators of the fault condition. With this regard, the Wavelet Transform (WT) or STFT could be applied for such conditions. However, the interest is the quantitative analysis of the high-frequencies present in the fault current. Thus, the STFT is chosen for such applications which should operate within 1-2 ms to comply with the fault detection requirements described in Section 5.3.1.

(v) Time-graded selectivity is not suitable for the dc SPS, which is evident from Fig. 5.14. The time difference between the operation of the two successive IEDs is around 3 ms which is very less for the protection coordination. Thus, utilizing the directional element will be useful in the dc PSV. For enhanced selective operation directional zonal interlocking (DZI) based selectivity could be implemented. Unlike in ac systems where the directional element triggers the forward or backward operation of multiple IEDs, DZI in dc systems triggers the IEDs of a particular zone.

(vi) Another aim of the protection algorithm is minimal dependence on the communication infrastructure as the standards and protocols are still not available for dc system protection as discussed in Section 5.3.5. Thus, the differential protection will not be

a feasible solution. Directional protection does not require stringent communication requirements as it exchanges only the status signals between the IEDs. It will be shown in Chapter 6 that the generator and load protection is independent of communication infrastructure while the protection of lines and buses need low-bandwidth communication infrastructure.

Thus, the DZI and STFT based fault detection algorithm would be suitable for the application in dc SPS.

5.5 STFT based Analysis of DC Short-Circuit Faults

There have been limited research attempts toward the study of frequency-domain analysis of dc fault conditions. The WT has been applied for analyzing non-periodic and non-stationary dc fault/transient current and voltage signals [84, 178]. With variable window size, it allows for simultaneous time and frequency-domain analysis of the transient signal. However, the frequency-domain analysis in the WT is illustrated by detailed coefficients, which cannot provide precise frequency content information. Moreover, the selection of suitable mother wavelet is crucial for the operation of the WT. On the other hand, the presence of high-frequency components could be determined by the STFT. Unlike WT, STFT operates over a fixed window length which can provide precise frequency content information for a specified window size [30]. This has been previously utilized for the diagnostic applications of induction motors [179] and transformers [180], and for power quality analysis in ac power systems [181].

5.5.1 STFT Operation

As described earlier, STFT is a frequency-domain analysis that helps in the quantitative analysis of the frequency components present in the input signal. The dc current signal is passed through predefined fixed size window function, and the discrete Fourier transform (DFT) is computed to determine the available frequency components. To continuously analyze the dc current, the successive windows are overlapped with each other, determined by the hop size, which is less than the window size while the DFT is being successively computed. This operation of STFT based fault detection algorithm is illustrated in Fig. 5.16.

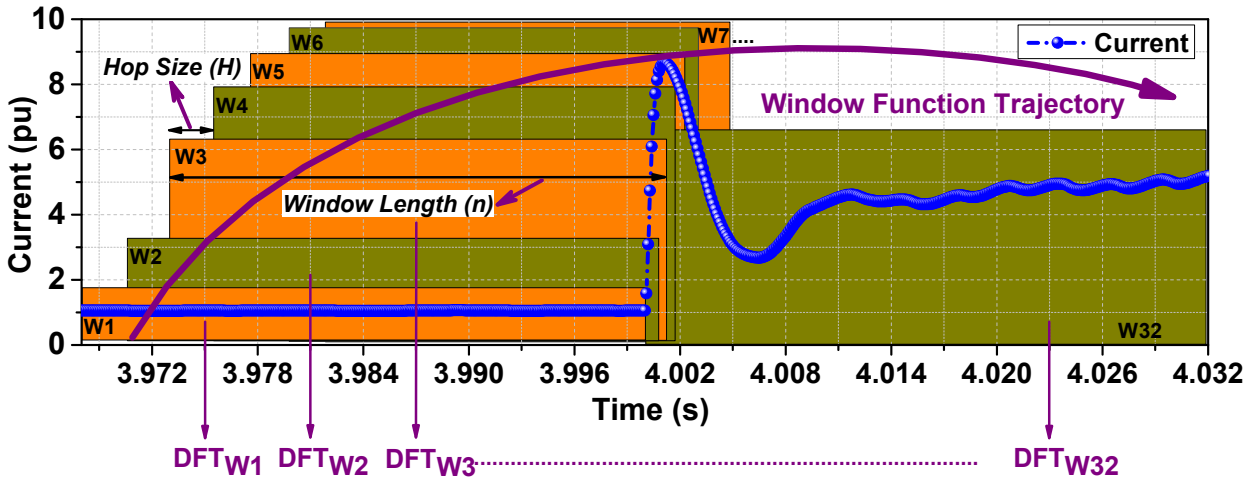


Fig. 5.16: STFT operation to detect the high frequency components in the fault current.

Table 5.3: Parameters Used in STFT Algorithm

Sampling Frequency (f_s)	$\boldsymbol{H}$	$\boldsymbol{n}$	**Time Res.** ($=H/f_s$)	**Freq. Res.** ($=f_s/n$)
10 kHz	2	32	0.2 ms	312.5 Hz

$W1$, $W2$, $W3$,... are the fixed size window function applied to the dc current signal under investigation. The DFT is then computed for each window (DFT_{Wn}). This process is repeated by moving the window determined by the hop size and again computing the DFT. In the discrete-domain, STFT ($\mathcal{S}_{\mathcal{D}}$) is expressed as:

$$\mathcal{S}_{\mathcal{D}[m,k]}\{i[n]\} = \sum_{n=0}^{n=N-1} i[n]w[n-mH]e^{-j\frac{2\pi nk}{N}}, \tag{5.25}$$

where, $i[n]$ is the input signal, $w[n]$ is the window function, N is the number of FFT points, n is the time-domain index of $i[n]$, m is the position of $w[n]$ around which it is real and symmetric, H is the hop size between the successive windows and k is the frequency index. n is decided by the length of $w[n]$. Hanning window function is chosen as it is neither too sluggish nor is sensitive to smaller load changes [29]. The parameters used for computing $\mathcal{S}_{\mathcal{D}}$ are listed in Table 5.3 [29, 182].

The frequency resolution of the computed DFT is governed by f_s and n which is given by f_s/n Hz. The frequency resolution improves with larger window size and vice versa. This property of the STFT makes it suitable for quantitative analysis of the frequency components

in non-stationary signals like fault/transients. For application to dc fault detection, where the time resolution is an important parameter, it could be improved by reducing H without affecting the frequency resolution. Thus, with the improved time resolution, STFT-based definitive quantitative analysis of frequency components for a particular window length could be a robust fault indicator in the dc SPS. The STFT operation is dependent on a number of parameters which are described below:

(i) **Sampling Frequency (f_s) :** It directly affects the time and frequency resolution of the STFT output. Higher f_s results in improved time and frequency resolution and vice versa. In this chapter f_s of the STFT based algorithm is limited to 10 kHz, which is consistent with the sampling frequency used for practical relaying applications.

(ii) **Number of Input Sample (n) :** It is the non-zero input samples of the input current/voltage on which the windowing function is applied. Increase in n would increase the window size, hence improving the spectral resolution among the present signals of different frequencies.

(iii) **Total number of FFT points (N) :** Increase of N helps in better approximation of the continuous Fourier transform (CFT) of the input signal. Zero padding of the input signal is done if the number of input samples (n) is lower than the number of FFT points (N). However, the computation time increases with increase in 'N'.

(iv) **Type of Window Function ($w[n]$) :** Rectangular, Triangular, Hanning, Hamming and Bartlett are some of the popular window functions available to perform STFT. In this chapter, Hanning window function is used for the transient state detection.

(v) **Hop Size (H) :** It is responsible for the time resolution of the STFT output. The lower the hop size, the better the time resolution becomes. In this chapter, H is chosen to be 2 samples which is equivalent to a time resolution of 0.2 ms.

To understand the operation and characteristics of the STFT algorithm during load change and fault conditions, an analogous expression of (5.25) in the continuous domain will be evaluated which is given by:

$$\mathcal{S}_{\mathcal{C}}\{i(t)\} = \int_0^{\tau} i(t)w(t-t_1)e^{-j\omega t}dt. \tag{5.26}$$

In the continuous domain, a 32-sample window function is represented by a window function of 3.2 ms length. And equivalently H in continuous domain is 0.2 ms. The expression of the window function in continuous-domain $w(t)$ for a rectangular window function is given by:

$$w(t) = 1 \tag{5.27}$$

whereas for the Hanning window, $w(t)$ is given by:

$$w(t) = \begin{cases} \int_{\tau_1}^{\tau_2} 0.5(1 + \cos\omega_\tau t)dt, & \text{for } \tau_1 < 0 \ \& \ \tau_2 > 0 \\ \int_{\tau_1}^{\tau_2} 0.5(1 - \cos\omega_\tau t)dt, & \text{for } \tau_1, \tau_2 > 0 \end{cases} \tag{5.28}$$

5.5.2 Application of STFT to Prefault Constant DC Current

The STFT of the dc current depends on the chosen window function. If the rectangular window is chosen, generalized representation of the STFT of the pre-fault constant dc current operating over time τ_1 to τ_2 is given as:

$$\begin{aligned} \mathcal{S}_\mathcal{C}\{I_o\} &= \int_{\tau_1}^{\tau_2} I_o.w(t).e^{-j\omega t}dt \\ &= I_o(\tau_2 - \tau_1)\Big(e^{-j\omega(\tau_1+\tau_2)/2}\,\text{sinc}\,\frac{\omega}{2\pi}(\tau_2 - \tau_1)\Big) \end{aligned} \tag{5.29}$$

For Hanning window function, the generalised representation of the constant dc current operating over time τ_1 to τ_2 is given as:

$$\begin{aligned} \mathcal{S}_\mathcal{C}\{I_o\} &= \int_{\tau_1}^{\tau_2} I_o.w(t).e^{-j\omega t}dt \\ &= I_o(\tau_2 - \tau_1)\Big(0.5e^{-j\omega(\tau_1+\tau_2)/2}\,\text{sinc}\,\frac{\omega}{2\pi}(\tau_2 - \tau_1) \\ &- 0.25e^{-j(\omega+\omega_\tau)(\tau_2+\tau_1)/2}\,\text{sinc}\,\frac{\omega+\omega_\tau}{2\pi}(\tau_2 - \tau_1) \\ &- 0.25e^{-j(\omega-\omega_\tau)(\tau_2+\tau_1)/2}\,\text{sinc}\,\frac{\omega-\omega_\tau}{2\pi}(\tau_2 - \tau_1)\Big) \end{aligned} \tag{5.30}$$

where ω is the frequency when varied from $0 : f_s/2$, having a resolution of f_s/n (Table 5.3). The ω_τ in (5.30) is $2\pi/\tau$ where τ is the window length (3.2 ms).

Under normal operating conditions, STFT of the dc current under investigation would result in sinc function which will have a frequency response similar to that shown in Fig. 5.17 and would comprise of main-lobes and side-lobes decaying with roll-off rate depending on the choice of window functions. The magnitude will be less at the frequencies known as update

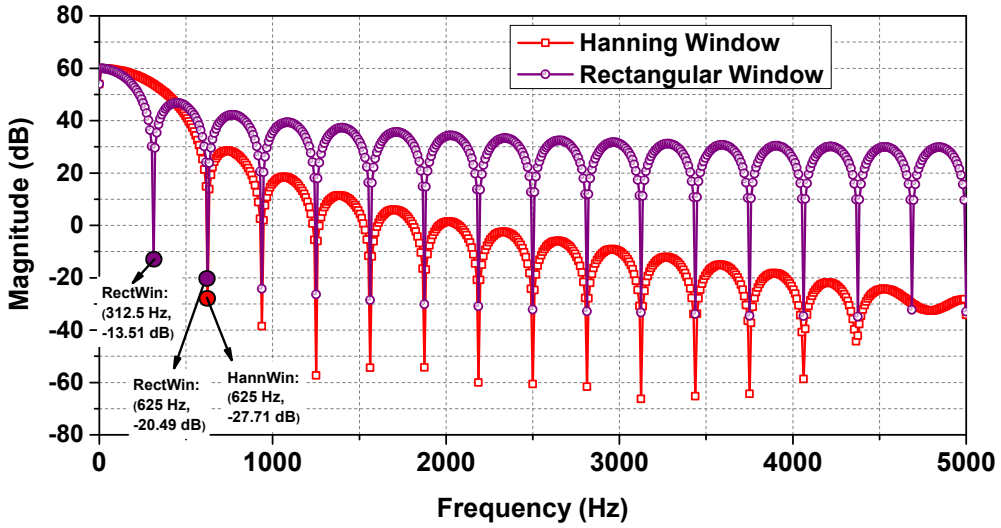


Fig. 5.17: Comparison of the Hanning and Rectangular Window Function.

frequency bins or zero-crossing frequency bins and is denoted by f_u. In discrete domain, having 32-sample window and 10 kHz sampling frequency which is considered in this chapter (Table 5.3), f_u will be the multiple of $k.f_s/N$ i.e. 312.5 k Hz. The starting frequency of f_u depends on the selected window function. For the rectangular window function f_u starts from $1.f_s/N$ i.e. 312.5 Hz and extends till $f_s/2$ i.e. 5000 Hz. However, for Hanning window, the frequency f_u starts from $2.f_s/N$ i.e. 625 Hz and extends till 5000 Hz. For the given parameters in Table 5.3, the locations of f_u for Rectangular and Hanning window function for given parameters are shown in Table 5.4 and Table 5.5 respectively.

During the faults in dc PSV, the rapid discharge from the dc-link capacitor is expected to be comprised of high frequency components. This ingression of the high frequency components in the fault current is expected to be identified by the magnitude at f_u, i.e. $|\mathcal{S}_\mathcal{D}|_{f_u}$ or $|\mathcal{S}_\mathcal{C}|_{f_u}$. Thus, the STFT algorithm can detect the fault condition as following:

$$\mathcal{S}_{\mathcal{D}fault} = \begin{cases} 1, & \text{if } |\mathcal{S}_\mathcal{D}|_{f_u} \geqslant \sigma \text{ dB} \\ 0, & \text{otherwise} \end{cases} \tag{5.31}$$

where, σ is the fixed setpoint (in dB).

5.5.3 Application of STFT to Step Change in DC Current

The STFT is applied to the step change in current as shown in Fig 5.18. The dc current

Table 5.4: Update-Frequency Bins for 32 Sample Rectangular Window

Window Type	**Win. Length** [n]	**Update Frequency Bins** (f_u)		
		$2f_s/n$	$3f_s/n$	$4f_s/n$
Rectangular Window	32	312.5 Hz	625 Hz	937.5 Hz

Table 5.5: Update-Frequency Bins for 32 Sample Hanning Window

Window Type	**Win. Length** [n]	**Update Frequency Bins** (f_u)		
		$2f_s/n$	$3f_s/n$	$4f_s/n$
Hanning Window	32	625 Hz	937.5 Hz	1250 Hz

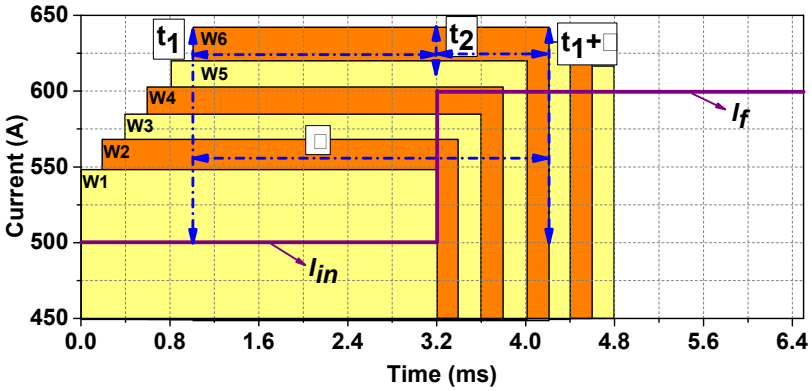


Fig. 5.18: Step change in dc current and moving window for STFT operation.

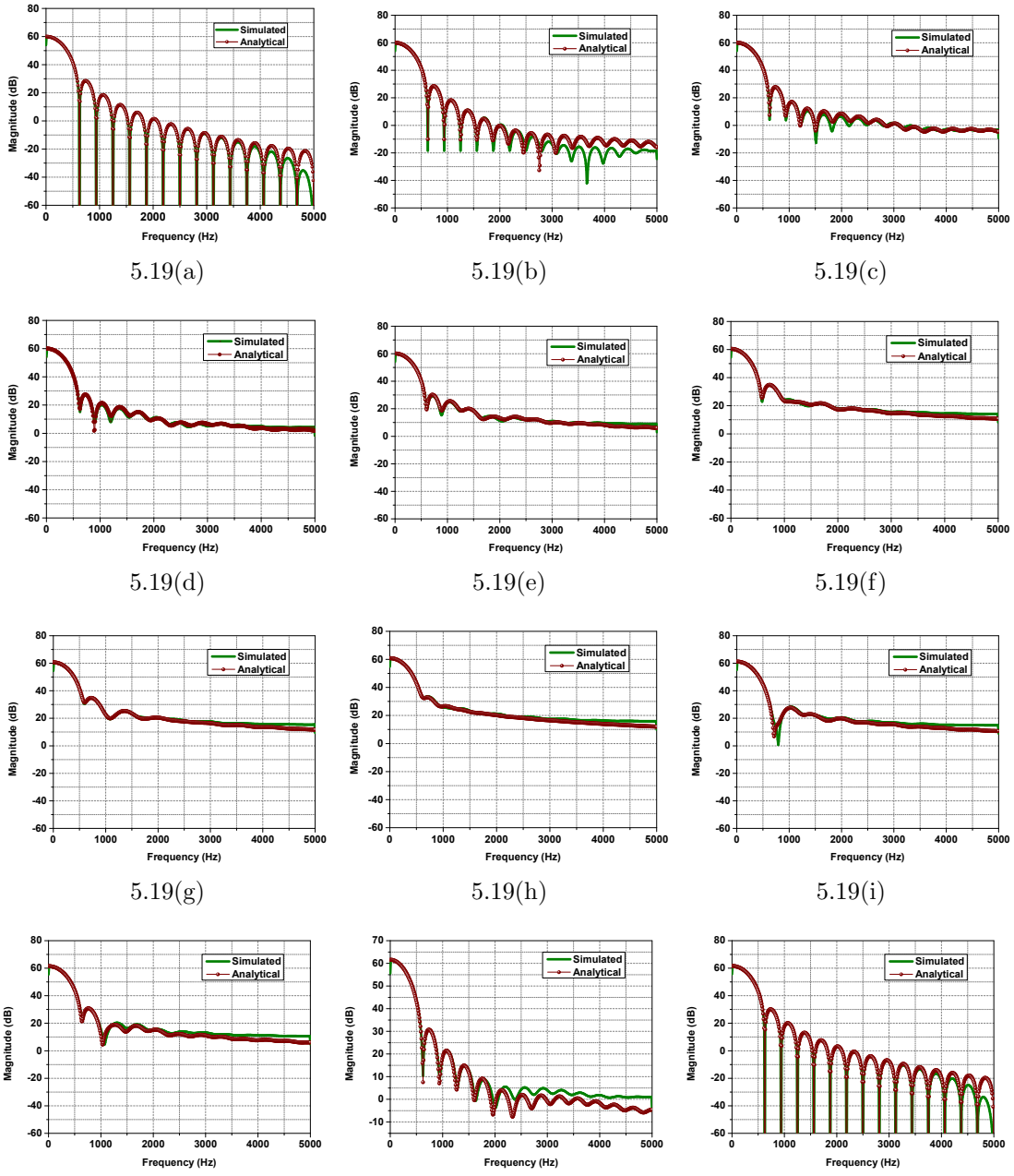
changes from I_{in} to I_f which in this case is 500 A and 600 A, respectively. The expression of current becomes important while applying STFT for the window at any time instant. For instance, in $W5$ the equivalent dc current can be represented by the following:

$$I_{dc} = A(\text{for}: \ t_1 < t < t_1 + \tau) - B(\text{for}: \ t_1 < t < t_2) + C(\text{for}: \ t_2 < t < t_1 + \tau) \qquad (5.32)$$

where, $A = [(t_2 - t_1)I_{in} + (t_1 + \tau - t_2)I_f]/\tau$, $B = [A - I_{in}]$ and $C = [I_f - A]$. The $\mathcal{S}_\mathcal{C}$ of the step change in current is given by:

$$\mathcal{S}_\mathcal{C}\{I_{dc}\}\Big|_{t_1}^{t_1+\tau} = \mathcal{S}_\mathcal{C}\{A\}\Big|_{t_1}^{t_1+\tau} + \mathcal{S}_\mathcal{C}\{B\}\Big|_{t_1}^{t_2} + \mathcal{S}_\mathcal{C}\{C\}\Big|_{t_2}^{t_1+\tau} \qquad (5.33)$$

The $\mathcal{S}_\mathcal{C}\{A\}$, $\mathcal{S}_\mathcal{C}\{B\}$ and $\mathcal{S}_\mathcal{C}\{C\}$ are calculated as per (5.30). The comparison of the $\mathcal{S}_\mathcal{D}\{I_{dc}\}$ and $\mathcal{S}_\mathcal{C}\{I_{dc}\}$ is shown in Fig. 5.19. For the prefault condition, the magnitude at f_u (Table 5.5)



5.19(a) 5.19(b) 5.19(c)

5.19(d) 5.19(e) 5.19(f)

5.19(g) 5.19(h) 5.19(i)

5.19(j) 5.19(k) 5.19(l)

Fig. 5.19: STFT of the stepped current signal of Fig. 5.18; (a) before load step change. STFT of the stepped current signal after: (b) 0.2 ms (c) 0.4 ms (d) 0.6 ms, (e) 0.8 ms, (f) 1.2 ms, (g) 1.4 ms, (h) 1.6 ms, (i) 2.0 ms, (j) 2.4 ms, (k) 2.8 ms and (l) 3.2 ms of load change.[$\mathcal{S}_{\mathcal{D}f_u}$: Simulated; $\mathcal{S}_{\mathcal{C}f_u}$: Calculated.]

is very less as discussed in Section 5.5.1. This is because the $\mathcal{S}_{\mathcal{C}}\{B\}$ and $\mathcal{S}_{\mathcal{C}}\{C\}$ is zero. As a result the output of $\mathcal{S}_{\mathcal{C}}\{I_{dc}\}$ is sinc function, which is only dependent on τ. When the

window is moved by H, the stepped up signal will also be encompassed by it. Thus, the output will be the sinc function depending on τ, $(t_2 - t_1)$ and $(t_1 + \tau - t_2)$ as per (5.33). This results in relatively higher magnitude at the defined f_u. This variation in the $\mathcal{S}_{\mathcal{C}}\{I_{dc}\}$ and $\mathcal{S}_{\mathcal{D}}\{I_{dc}\}$ for the window functions with various degree of overlapping between the I_{in} and I_f is shown in Fig. 5.19. The magnitude of $\mathcal{S}_{\mathcal{C}}\{I_{dc}\}$ and $\mathcal{S}_{\mathcal{D}}\{I_{dc}\}$ at f_u is highest when the window encompasses 50% of I_{in} and 50% of I_f (Fig. 5.19(h)). The $\mathcal{S}_{\mathcal{C}}\{I_{dc}\}$ and $\mathcal{S}_{\mathcal{D}}\{I_{dc}\}$ comes to normal condition when the window encompasses the I_f completely as shown in Fig. 5.19(l). It is further observed that the higher order f_u are distorted even for smaller overlapping between I_f and I_{in} where as the first order f_u, i.e., 625 Hz is relatively robust and distorts for maximum overlapping condition. As a result, $f_u = 625$ Hz is taken in this chapter for the setpoint to detect the transient conditions.

5.5.4 Selection of Window Length for STFT based Fault Detection

For the pre-fault DC signal with negligible ripple component such as analytical expressions in Section 5.5.2, the magnitude at the update-frequencies are significantly negative (in dBs). However, in the dc SPS formed by interfacing 2L-VSC, the dc current would have ripples, affecting the frequency-domain response. The ripples in the pre-fault current might increase the magnitude at the update-frequency bins, causing a false identification of the transient condition. Thus, the window length must be chosen for which the update-frequency bins do not lie within the vicinity of ripple frequencies of the pre-fault DC current. The dominant ripple frequency of the dc pre-fault current is expected to be six times the ac side frequency (360 Hz; AC side frequency = 60 Hz). This is primarily caused by the conduction pattern of the semiconductor switches of the 3-ϕ 2L-VSC. To illustrate this, the load was changed at 1 s and ripple current components were observed in the real-time simulation system of dc PSV. A ripple current of 5 A is present before the load change, and 7 A after the load change. In the time-domain, the magnitude of the ripple component is significantly less as compared to the line current. However, in frequency-domain, the ripple content would result in 14 dB_A (for 5A ripple content) and 17 dB_A (for 7 A ripple content) change in the magnitude. This would result in shifting of the frequency response magnitude toward more positive region. Thus, on the contrary of highly negative magnitude at the zero frequency bins for ideal dc current, the actual magnitude would move toward more positive side.

Table 5.6: First Three Update-Frequency Bins of Hanning Window for Various Window Lengths

Window Length [n]	**Update Frequency Bins** (f_u)		
	$2f_s/n$	$3f_s/n$	$4f_s/n$
16	1250 Hz	1875 Hz	2500 Hz
32	625 Hz	937.5 Hz	1250 Hz
64	312.5 Hz	468.75 Hz	625 Hz
128	156.25 Hz	234.375 Hz	312.5 Hz
256	78.125 Hz	117.1875 Hz	156.25 Hz
512	39.0625 Hz	58.59375 Hz	78.125 Hz

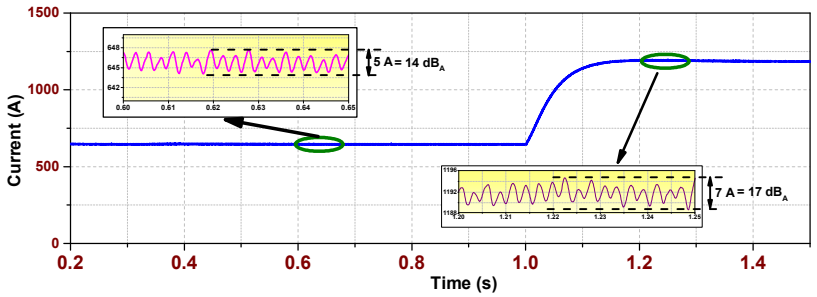


Fig. 5.20: Simulated dc current with load change at 1 s.

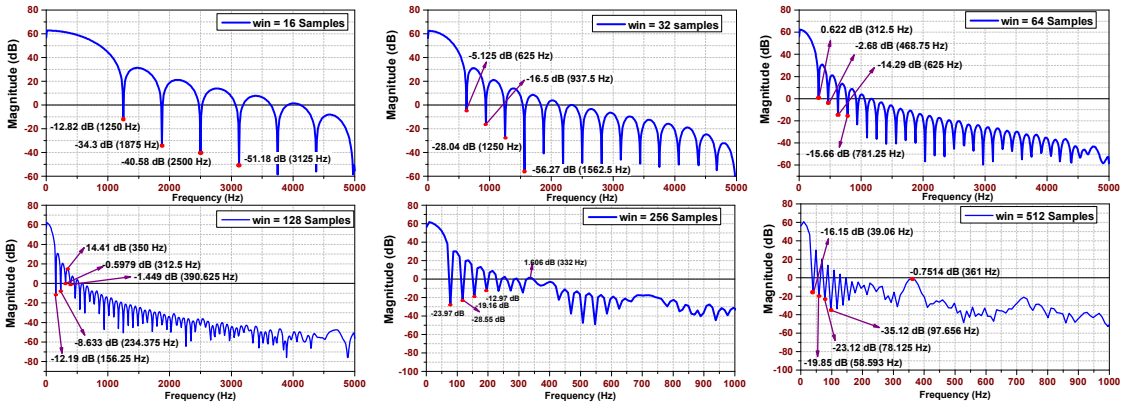


Fig. 5.21: Frequency spectrum of simulated pre-fault current for various window lengths.

The frequency response of the simulated dc signal for various window lengths and corresponding update-frequency bins consistent with Table 5.6 are shown in Fig. 5.21. The window lengths must be chosen carefully considering the 360 Hz ripple component. Priority

of the selection of the 'n' should be given to the update-frequency bins, which do not lie within the range of 360 Hz. By comparing Table 5.6 and Fig. 5.21, the window length of 16, 32, 256 and 512 samples might be chosen. By choosing $w[n]$ of 64 samples, the magnitude at first update-frequency bin has positive magnitude, which is caused by the presence 360 Hz ripple component. This is confirmed by performing STFT with increased window lengths (128, 256, 512), where the magnitude at the vicinity of $\approx$ 360 Hz has higher magnitudes. This is also indicated in Table 5.6.

5.5.5 Determining Threshold for STFT based Fault Detection

It has been described in (6.16) that the STFT algorithm is dependent on σ for effective fault identification. The variation of this σ is described in Fig. 5.19 when step change of dc current is initiated. Since, the STFT quantifies the frequency components present in the input signal; the magnitude at f_u i.e. σ is expected to be modified by the ripple content of the dc current under investigation. As a result, the STFT of the dc current would not resemble to the sinc function as described in Section 5.5.3 and Fig. 5.19(a), 5.19(l). Since ripples are present in the current of dc PSV, the current can be represented by:

$$I_{dc} = I_o + \sum_{n=1,2,3...} I_n \sin \omega_n t. \tag{5.34}$$

The current I_{dc} comprises of the dc component, I_o and very small contributions from the ripples $I_n \sin \omega_n t$. In such case, the STFT computation will be modified to:

$$\mathcal{S}_{\mathcal{C}}\{I_{dc}\} = \int_0^{\tau} \Big(I_o + \sum_{n=1,2,3...} I_n \sin \omega_n t\Big) w(t) e^{-j\omega t}.dt \tag{5.35}$$

$\mathcal{S}_\mathcal{C}$ of I_o will take form of (5.30) and, to obtain the essence of the ripple components, $\mathcal{S}_\mathcal{C}$ of the ripples can be expressed as:

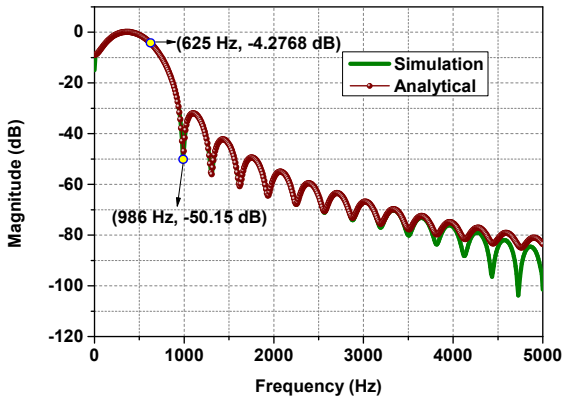
$$\begin{aligned}
\mathcal{S}_\mathcal{C}\{I_n\} &= \int_0^\tau \sum_{n=1,2,3\ldots} I_n \sin\omega_n t \; w(t) e^{-j\omega t}.dt \\
&= \sum_{n=2,3,4\ldots} \Bigg[\Bigg\{ \frac{I_n\tau}{2j} \Big[(e^{-j(\omega-\omega_n)\tau/2} \operatorname{sinc} \frac{\omega-\omega_n}{2\pi}\tau) \\
&- 0.5\Big(e^{-j(\omega-\omega_n-\omega_\tau)\tau/2} \operatorname{sinc} \frac{\omega-\omega_n-\omega_\tau}{2\pi}\tau\Big) \\
&- 0.5\Big(e^{-j(\omega-\omega_n+\omega_\tau)\tau/2} \operatorname{sinc} \frac{\omega-\omega_n+\omega_\tau}{2\pi}\tau\Big)\Big] \Bigg\} \\
&- \Bigg\{ \frac{I_n\tau}{2i} \Big[(e^{-j(\omega+\omega_n)\tau/2} \operatorname{sinc} \frac{\omega+\omega_n}{2\pi}\tau) \\
&- 0.5\Big(e^{-j(\omega+\omega_n-\omega_\tau)\tau/2} \operatorname{sinc} \frac{\omega+\omega_n-\omega_\tau}{2\pi}\tau\Big) \\
&- 0.5\Big(e^{-j(\omega+\omega_n+\omega_\tau)\tau/2} \operatorname{sinc} \frac{\omega+\omega_n+\omega_\tau}{2\pi}\tau\Big)\Big] \Bigg\} \Bigg]
\end{aligned} \tag{5.36}$$

The magnitude of the $\mathcal{S}_{\mathcal{C}I_n}$ is given as following:

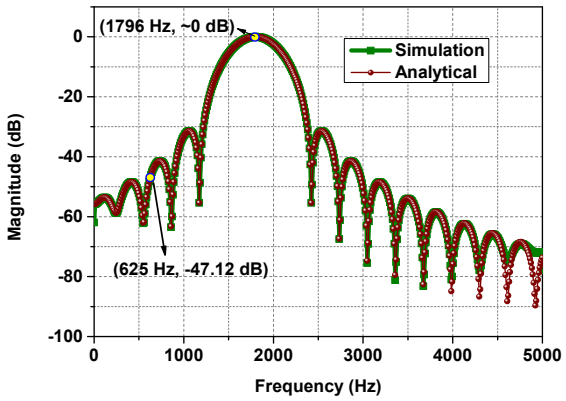
$$|\mathcal{S}_{\mathcal{C}I_{dc}}|_{\omega=0:f_s/2} = 20\log_{10}\left|\frac{\mathcal{S}_\mathcal{C}\{I_o\}+\mathcal{S}_\mathcal{C}\{I_n\}}{0.5\;\tau}\right| \text{ dB} \tag{5.37}$$

To illustrate the effect of the ripples, $n = 6$ and $n = 30$ is considered as per (5.36) and is shown in Fig. 5.22(a) and Fig. 5.22(b), respectively. To understand the effect of ripples, the magnitude of I_6 and I_{30} has been set to 1. It is seen from Fig. 5.22(a) that the lower order harmonic (360 Hz) severely influences the magnitude at f_u= 625 Hz. The magnitude at 360 Hz increases to -4.27 dB while it is expected to be very less. For the higher order harmonics in Fig. 5.22(b), the magnitude is higher in the vicinity of the corresponding higher order frequencies. As a result, the magnitude at f_u= 625 Hz is quite low. This is further illustrated in Fig. 5.22(c), which depicts the impact of 2^{nd}, 6^{th} and 12^{th} harmonic on the STFT magnitude of I_{dc} at 625 Hz when I_n/I_o is varied in (5.35). There is increasing trend in the magnitude at 625 Hz when I_n/I_o is increased. I_o is the base current which depends on the power level of the system. In this chapter, I_o is taken to be 1300 A thus additional $20\log_{10} I_o$ would be added to the magnitude at desired ripple content (Fig. 5.22(c)). Following this procedure, σ for tripping has been chosen to be 20 dB.

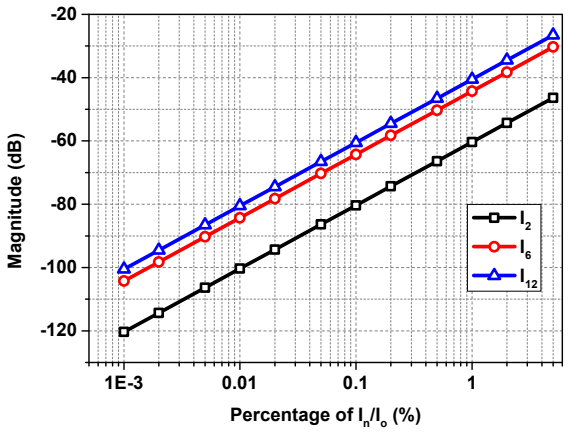
$$\mathcal{S}_{\mathcal{C}I_{dc}}|_{f=625Hz} = I_o\Big[(0 + 2.5967 \times 10^{-32}i) + \frac{I_2}{I_0}(0.0518 - 0.0612i) + \frac{I_3}{I_0}(0.1344 - 0.0116i) + \frac{I_4}{I_0}(0.2090 + 0.1139i) + \frac{I_5}{I_0}(0.2025 + 0.2946i) + \frac{I_6}{I_0}(0.0587 + 0.4681i) + \frac{I_7}{I_0}(-0.2189 + 0.5448i) + \frac{I_8}{I_0}(-0.5509 + 0.4460i) + \frac{I_9}{I_0}(-0.8073 + 0.1509i) + \frac{I_{10}}{I_0}(-0.8636 - 0.2762i) + \frac{I_{11}}{I_0}(-0.6625 - 0.6991i) + \frac{I_{12}}{I_0}(-0.2480 - 0.9632i) + ...\Big] \tag{5.38}$$



5.22(a)



5.22(b)



5.22(c)

Fig. 5.22: STFT of (a) 360 Hz, (b) 1800 Hz signal. (c) Normalised magnitude of $\mathcal{S}_{\mathcal{C}I_{dc}}$ at 625 Hz for various I_n/I_o.

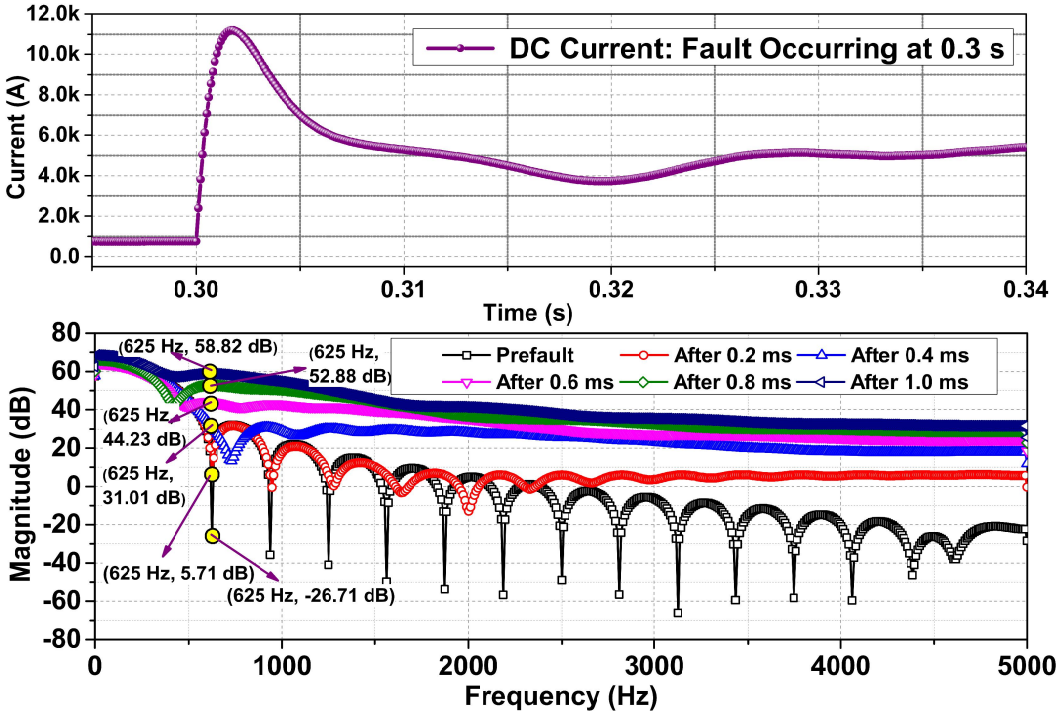


Fig. 5.23: Variation of the STFT magnitude at f_u= 625 Hz as the Hanning window progressively captures the fault current signal.

5.5.6 Detecting Fault Condition by STFT

As per (5.10) and (5.17), the fault current signals comprises of exponential component for overdamped conditions and sinusoidal component for the underdamped conditions, respectively. The STFT of the overdamped fault takes the form of :

$$\begin{aligned}\mathcal{S}_{\mathcal{C}}\{I_{od}\} &= \int_0^{\tau} i_{od}\; w(t)\; e^{-j\omega t} dt \\ &= \mathcal{X}\Big[\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j\omega)\tau}}{\mathcal{A}-\mathcal{B}+j\omega} - 0.5\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j(\omega-\omega_\tau))\tau}}{\mathcal{A}-\mathcal{B}+j(\omega-\omega_\tau)} \\ &- 0.5\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j(\omega+\omega_\tau))\tau}}{\mathcal{A}-\mathcal{B}+j(\omega+\omega_\tau)}\Big] - \mathcal{Y}\Big[\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j\omega)\tau}}{\mathcal{A}-\mathcal{B}+j\omega} \\ &- 0.5\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j(\omega-\omega_\tau))\tau}}{\mathcal{A}-\mathcal{B}+j(\omega-\omega_\tau)} - 0.5\frac{1-e^{-(\mathcal{A}-\mathcal{B}+j(\omega+\omega_\tau))\tau}}{\mathcal{A}-\mathcal{B}+j(\omega+\omega_\tau)}\Big]\end{aligned} \tag{5.39}$$

where $\mathcal{X} = \Big[\frac{V(0+)}{2.\mathcal{B}.L} + \frac{I(0+)}{2}\Big]$ and $\mathcal{Y} = \Big[\frac{V(0+)}{2.\mathcal{B}.L} - \frac{I(0+)}{2}\Big]$. $\mathcal{A}$ and $\mathcal{B}$ are according to (5.10). The STFT of the underdamped fault current signal takes the form of (5.36). The STFT analysis of the fault currents would follow a similar procedure as described in Section 5.5.3. In both

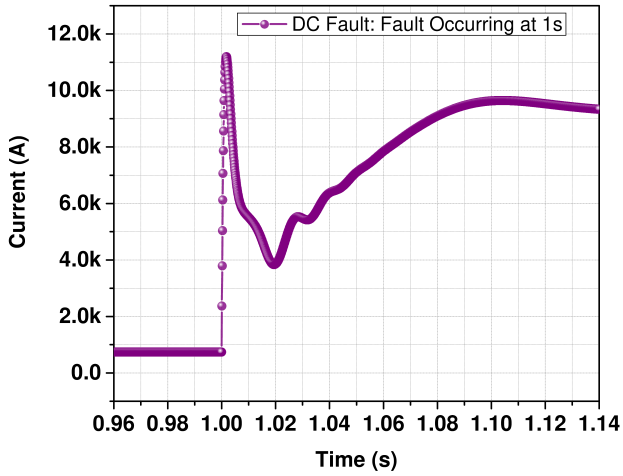
Table 5.7: Magnitude at Update Frequency Bins of 625 Hz for the STFT of i_{IED5} and i_{IED15} and Time to Reach

Case	Mode	IED5		IED15	
		$\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}$ (dB)	$t_{\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}}$ (ms)	$\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}\rvert$ (dB)	$t_{\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}}$ (ms)
1	Before Blocking	22.2567	0.2	37.866	0.4
	After Blocking	22.2567	0.2	32.6968	0.4
2	Before Blocking	45.6311	0.4	21.2959	0.2
	After Blocking	22.5083	0.2	39.6161	0.4
3	Before Blocking	24.7209	0.2	40.2659	0.4
	After Blocking	24.6852	0.2	36.293	0.4
4	Before Blocking	24.2759	0.2	44.8228	0.4
	After Blocking	24.2759	0.2	40.4097	0.4
5	Before Blocking	21.9615	0.2	37.5648	0.4
	After Blocking	21.9615	0.2	32.3493	0.4
6	Before Blocking	23.234	0.2	44.804	0.4
	After Blocking	23.234	0.2	39.0298	0.4

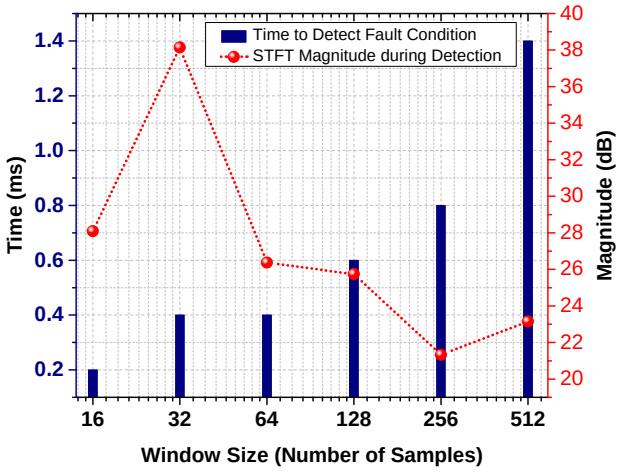
$\sigma = 20$ dB, $f_u = 625$ Hz

cases, the magnitude at f_u= 625 Hz is altered by $(\omega + \omega_\tau)$ and $(\omega - \omega_\tau)$ for overdamped signal and $(\omega + \omega_d + \omega_\tau)$, $(\omega + \omega_d - \omega_\tau)$, $(\omega - \omega_d + \omega_\tau)$, and $(\omega - \omega_d - \omega_\tau)$ for underdamped fault current signal. The variation of STFT magnitude of dc fault current at 625 Hz for 0.1 Ω fault resistance is shown in Fig. 5.23. It can be observed that the STFT magnitude at 625 Hz is very less for prefault dc current. As the Hanning window encompasses the fault current, the STFT magnitude at 625 Hz rises as shown in Fig. 5.23. STFT is applied for the fault currents with different system configurations, as listed in Table 5.2, where the OC protection would be challenging to implement. In spite of the changing system configuration and blocking/unblocking of the loads, STFT is able to detect the fault condition as per the threshold described in Section 5.5.5 and is illustrated in Table 5.7.

The pseudo code of the STFT based fault detection is included in Appendix A. Selection of window length (n) is crucial for STFT-based fault detection which has been explained in Section 5.5.4. Considering ideal condition with no ripple content, influence of n on fault detection timing is shown in Fig. 5.24. Fig. 5.24(a) shows the fault current generated with 0.1 Ω fault resistance. Fig. 5.24(b) shows the fault detection time when n is changed, and also shows the magnitude of STFT when fault is detected. It is seen that the fault detection timing increases with the increase in n. As n is increased, the frequency resolution



5.24(a)



5.24(b)

Fig. 5.24: (a) DC fault current at 1 s for fault impedance of 0.1Ω and, (b) time required to detect dc fault when window size is varied. Tripping setpoint, σ is taken to be 20 dB and the figure also shows the magnitude of $\mathcal{S}_{\mathcal{D}}$ when the fault is detected.

improves. Thus, for higher value of n, first zero-crossing frequency bin (f_{u1}) is the low-frequency component however for lower value of n, f_{u1} is the high-frequency component. STFT-based fault detection works by detecting the high-frequency components which is done by measuring the increased magnitude at f_{u1}. Thus, for lower n, fault condition is detected easily as compared to higher n. Thus in this thesis, n is selected to be 32 samples. The accuracy in frequency-resolution is not very important as we are concerned with the presence of the high-frequency components and not on the accurate magnitude of the high-frequency component. Thus, only the time-resolution is important which is decided by the hop-size and sampling frequency.

5.6 Summary

This chapter covers time and frequency-domain based fault analysis in the dc SPS. With such fault analysis, the protection requirements are identified which are found to be different from the conventional dc power systems. The results of this chapter can be summarized as follows:

(i) The compact nature of dc SPS results in fault currents of similar intensities at all the fault locations. Moreover, the system configuration of dc SPS is changing owing to

demands of the marine missions. This results in changing fault current intensities. Thus, the time-domain based OC protection would require optimized tripping set-points to develop the fault detection strategies for every marine missions.

(ii) It has been discussed that blocking the fault currents from propulsion loads are useful to restrict the magnitudes of fault currents which could be useful in de-rating the fault isolation devices.

(iii) It is found that the time-graded selectivity is not sufficient for dc SPS which is mitigated by the DZI based selectivity.

(iv) A step-by-step guide to implement the STFT based fault detection is proposed in this chapter which is supported by the detailed mathematical analysis. It is seen that proper selection of the window length is an important parameter which should be chosen while considering the ripple content of the dc current. The algorithm provides reliable fault detection with 100% accuracy, for window size of 16 or 32 samples in the simulation test system.

(v) Analytical evaluation for the pre-fault condition, stepped change in the dc current and for fault conditions are also presented. Through such analysis, it is easier to comprehend the present high-frequency components in the dc current under various transient conditions.

(vi) A method for the selection of the protection threshold for the STFT based fault detection is deduced from the mathematical analysis. This is dependent on the harmonic content of the pre-fault dc current.

(vii) As the STFT uses standard windowed based FFT, it could be conveniently configured in the embedded system domain as opposed to the other fault detection methods such as wavelet transform.

Chapter 6

Current-Only Directional Protection Scheme for DC SPS

6.1 Introduction

The dc PSV is taken as an example of the target dc SPS in this thesis. The detailed modeling, control and operation is covered in Chapter 3 and Chapter 4, respectively. It has been discussed that the dc PSV is compact in size with lower cable lengths and has higher penetration of active loads as compared to the land based dc microgrids. The shorter line lengths in dc PSV results in severe short-circuit fault currents of similar magnitude at almost all locations occurring at the same time instant. Such surge in the fault currents can damage the interfacing converters as well. In addition to the generation sources, the active propulsion loads of the dc PSV will also discharge to the fault point further aggravating the fault conditions. The short-circuit transient analysis along with investigation on the protection requirements covered in the Chapter 5 reveals that the dc PSV would require

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The results of this chapter have been partially published in:

(i) **K. Satpathi**, A. Ukil, S. S. Nag, J. Pou and M. A. Zagrodnik, "DC marine power system: Transient behaviour and fault management aspects," *IEEE Trans. Ind. Informat.*, vol. 15, no. 4, pp. 1911-1925, Apr. 2019.

(ii) **K. Satpathi**, A. Ukil, S. S. Nag, J. Pou and M. A. Zagrodnik, "Comparison of current-only directional protection in AC and DC power systems," in *Proc. Innovative Smart Grid Technologies (ISGT)*, Singapore, 2018.

(iii) **K. Satpathi**, N. Thukral, A. Ukil and M. A. Zagrodnik, "Directional protection scheme for MVDC shipboard power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016.

unit protection techniques where the faulty section would be identified and isolated. The protection system of the dc PSV is anticipated to be inspired from system-level protection studies of MTDC microgrids [31, 183]. The existing dc fault detection strategies that could be applicable to dc SPS are discussed in Chapter 2. Monadi *et al.* [100] proposed a centralized differential protection scheme where the entire MTDC microgrid is divided into several sub-microgrids. During the fault, the affected sub-microgrid is disconnected from the rest of the dc system which is later restored after the fault has been isolated. Although this scheme works satisfactorily for MTDC microgrids, this would not be suitable for dc PSVs undergoing DP operation where the power outage for the sub-microgrid section could not be tolerated. Moreover, the differential based unit protection would demand accurate measurement and transmission of the time-stamped current/voltage signals requiring high-bandwidth communication infrastructure thus adding cost to the system [74, 100, 184]. Instead, a zone-based directional protection could be implemented which relies on a low-bandwidth communication infrastructure.

Directional protection has been a popular choice in ac systems where it is a combination of directional element ($\mathbb{D}$) (for fault localisation) and time-domain based over-current (OC) relay to detect the faulty section [73, 177]. In land-based ac systems, the amount of generation systems and loads are known beforehand, thus the OC tripping thresholds are selected accordingly [185]. There have been limited but increasing number of attempts in the directional protection for application in the land-based dc microgrids [102, 186]. In such scenarios, the directional protection is achieved by the $\mathbb{D}$, while the fault condition is identified when the bus voltage crosses the undervoltage (UV) threshold and the fault isolation devices are activated when the OC threshold is exceeded. The directional protection could be further modified by implementing only the $\mathbb{D}$ and UV threshold. It is found that such time-domain based directional protection works satisfactorily for low-impedance faults and requires fixed OC and UV thresholds. The loading in dc SPSs, such as PSVs is constantly changing and is dependent on the type of mission profiles. The DGs are expected to operate at optimized speeds and some of them might be taken out of service depending on the load demand [187]. Thus, the application of the OC relay in directional protection will require optimized protection settings which might prove to be restrictive for such changeable system configurations in the dc PSVs. This has been described in Chapter 5 where it is found that

the STFT based fault detection technique could be suitable for such applications. Thus, appropriate modeling of $\mathbb{D}$ and STFT based fault detection can be used to devise a novel current-only directional protection for the dc SPS. The proposed current-only directional protection is based on the time-domain based $\mathbb{D}$ and frequency-domain based fault detection algorithm. This is significantly different from the existing directional protection approaches which have both the $\mathbb{D}$ and fault detection criteria in time-domain.

6.2 Contributions of the Chapter

The contents and main contributions of this chapter are:

(i) Following the existing trend of the time-domain based directional protection techniques, this chapter starts with the directional protection based on $\mathbb{D}$ and UV and is termed as the '*Traditional Directional Protection*'.

(ii) The drawbacks of the existing $\mathbb{D}$ is identified, which is modified by the directional zonal interlocking (DZI) based fault localization technique. It is seen that the DZI has higher degree of operation as compared to the conventional $\mathbb{D}$.

(iii) This chapter proposes a modified directional protection for dc PSVs that works by synergistic operation of the DZI and STFT. Both DZI and STFT are computed with the current signals thus making it low-cost and less complex. Such *'current-only'* algorithms have been developed for the protection of generation and load systems, lines and buses. The protection method is validated by inspecting its operation against the fault currents of varying intensities at all locations. This is obtained by increasing fault resistances from low to high-impedance. The generation and load systems are protected independently, whereas protection of lines and buses is achieved by a low-bandwidth communication infrastructure.

(iv) The efficacy of the proposed current only directional protection is supported by the comparative analysis with the existing approaches.

6.3 Directional Protection Algorithm: Traditional Approach

As discussed in Chapter 5, the low impedance pole-to-pole short-circuit fault is indicated by the rapid discharge from the dc-link capacitors. The magnitude and direction of the dc-link capacitor discharge is dependent on the fault resistance and fault location, respectively. Since the current direction may reverse during regenerative operation of the propulsion loads; a combination of branch current and bus-bar voltage could be taken for fault identification to enhance higher reliability. This is because the bus-bar voltage is expected to collapse in case of low-impedance faults.

The traditional directional protection utilises current direction along with time-domain analysis of the current and voltage elements to identify the fault condition and fault location. The fault condition is validated when overcurrent (OC) and undervoltage (UV) thresholds are exceeded. Fault localisation is achieved by comparison of the direction element ($\mathbb{D}$) outputs of the various branches. The directional protection is carried out by the operation of the intelligent electronic devices (IEDs) installed at every branch of the dc power system. To understand this protection method, Fig. 6.1 has been taken into consideration which is a subset of the full-fledged dc PSV introduced in Chapter 4. Fig. 6.1 shows a representative dc SPS comprising of generator side connected with the load side via bus-bar. The generator side comprises of 2×2048 kVA dc generation system while the load side comprises of $2{\times}883$ kW tunnel thrusters and $1{\times}300$ kVA houseload. The sectionalising of the bus-bar using IED6 is done to increase the reliability of the system. The detailed modeling and operation of the generation systems and loads have been covered in the Chapter 3 and Chapter 4. The IED detects and SSCB isolates the respective section when fault 'F_j' (for $j-$th segment of the line) happens. The dc PSV is divided into several zones 'Z_k' (for $k-$th zone) based on their common functionalities. Under normal conditions, the steady-state current or the prefault current direction is fixed, which flows from the generator side to the load side and is considered as positive direction. For the traditional approach, the directional element, $\mathbb{D}$ is determined by (6.1) [30, 102, 186].

$$\mathbb{D} = \begin{cases} 1, & \text{if } i[n] \geqslant 0 \\ 0, & \text{if } i[n] < 0 \end{cases} \tag{6.1}$$

F_1, F_2 and F_3 mark the location of pole-pole short-circuit fault at the generator side, load side and bus-bar side, respectively, as indicated in Fig. 6.1 and the following protection algorithms are used.

6.3.1 Case Studies with Traditional Directional Protection

Faults at the Generator Terminal

The direction of the fault current during the fault at the generator terminal is shown in Fig. 6.1(a). This is identified by the increased current magnitude in the reverse direction and reduction in the dc bus voltage beyond permissible limit at the generator IED (IED_{Gen}). As the current direction always reverses during the low-impedance faults at the generator, the current magnitude is not necessary for the fault detection. Thus, the fault detection logic by the IED_{Gen} is shown in (6.2) and the result is shown in Fig. 6.2(a).

$$\text{IED}_{Gen_{Fault}} \implies \mathbb{D}_{\text{IED}_{Gen}} = 0 \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.2}$$

Faults at the Load Terminal

For the fault at load side as shown in Fig. 6.1(b), the fault condition is identified by the OC in the forward direction and reduction of the dc bus voltage beyond prescribed limit at the load side IED (IED_{Load}). Thus, the fault condition is given by (6.3) and the result is shown in Fig. 6.2(a).

$$\text{IED}_{Load_{Fault}} \implies \mathbb{D}_{\text{IED}_{Load}} = 1 \;\; \&\& \;\; I_{Load} > I_{Threshold} \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.3}$$

As explained in Section 5.3.4 of Chapter 5, the IED_{Load} has additional responsibility of blocking the reverse current when the fault happens outside the load systems. This condition will happen when (6.4) is achieved.

$$\text{IED}_{Load_{Block}} \implies \mathbb{D}_{\text{IED}_{Load}} = 0 \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.4}$$

Faults at the Bus-bar

During the fault at the bus-bar (Fig. 6.1(c)), the current direction detected by the IED_{Gen} is positive whereas the current direction of all the IED_{Load} is negative. Thus, the fault at the bus-bar is characterised by the following:

$$\text{IED}_{Bus_{Fault}} \implies \mathbb{D}_{\text{IED}_{Gen}} = 1 \;\; \&\& \;\; \mathbb{D}_{\text{IED}_{Load}} = 0 \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.5}$$

After sectionalising into Section I and Section II, the current direction of IED6 becomes an important aspect of the bus-bar protection. It would be possible to identify the fault location, by comparing the current direction at IED6 along with current direction of IEDs of the generators and loads with the required current/voltage thresholds. Under normal condition, current direction of IED6 is set to be positive when the current flows from Section I to Section II. The fault at Section I is identified by IED6 by the following logic:

$$\text{IED}_6 \implies \mathbb{D}_{\text{IED}\,1} = 1 \;\; \&\& \;\; \mathbb{D}_{\text{IED}\,3} = 0 \;\; \&\& \;\; \&\& \;\; \mathbb{D}_{\text{IED}\,6} = 0 \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.6}$$

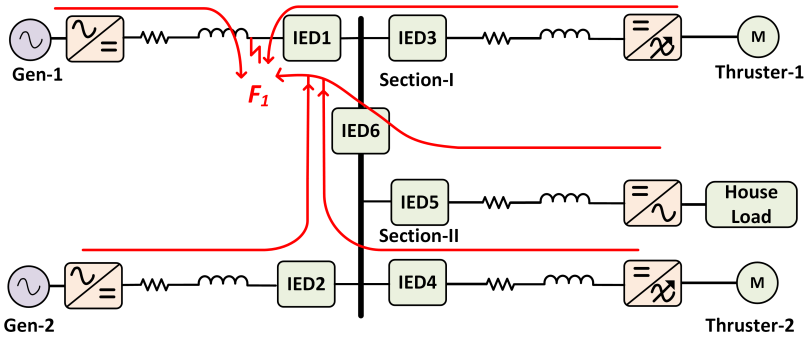
The fault at Section II is identified by IED6 by the following logic:

$$\text{IED}_6 \implies \mathbb{D}_{\text{IED}\,2} = 1 \;\; \&\& \;\; \mathbb{D}_{\text{IED}\,4,5} = 0 \;\; \&\& \;\; \&\& \;\; \mathbb{D}_{\text{IED}\,6} = 1 \;\; \&\& \;\; V_{Bus} < V_{Threshold}. \tag{6.7}$$

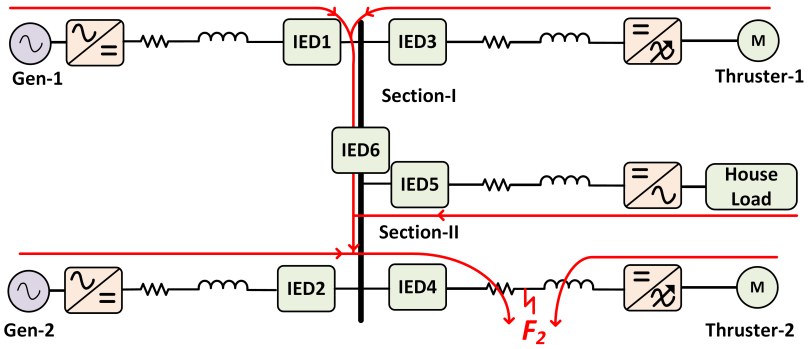
The generalised primary protection algorithm for the generator, load and bus-bar protection ((6.2)–(6.7)) has been included in the Appendix B.

6.3.2 Fault Isolation Requirements and Architecture of IEDs

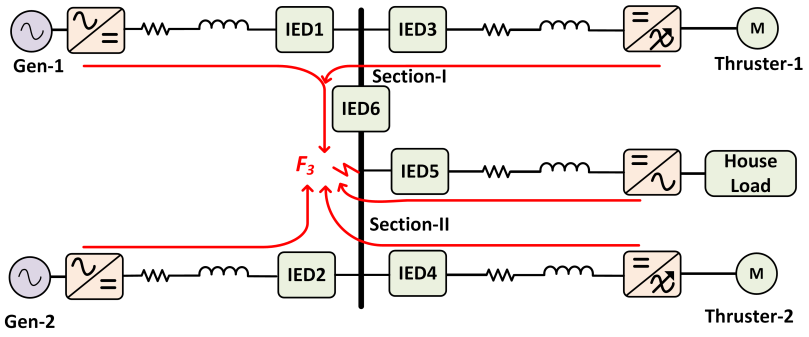
The generator side and the load side are connected with the bus-bar with their respective IEDs. Since the traditional directional protection utilises current and voltage signals, the IED would comprise of digital relay, current transducer (CT), voltage transducer (VT) and breakers (S) to isolate the fault current as shown in Fig. 6.3. The information from CT and VT is sent to the digital relay to determine the fault condition. After necessary computation, the relay gives decision output to breakers S1 and S2. The suffix *'p'* and *'n'* in S1 and S2 represent the breakers associated with *'positive dc rail'* and *'negative dc rail'*, respectively. Since the fault isolation in the dc SPS is primarily challenged by the absence of current



6.1(a)



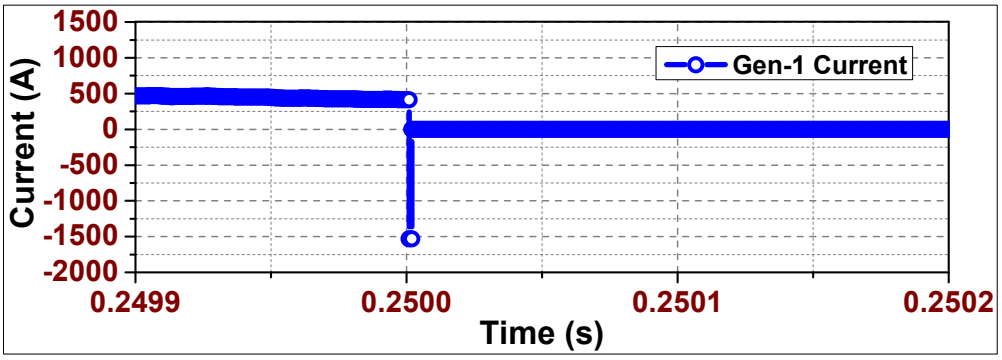
6.1(b)



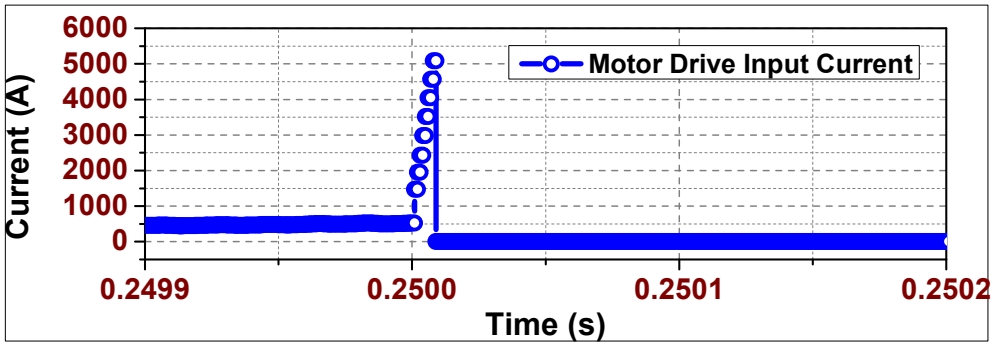
6.1(c)

Fig. 6.1: Fault current direction during fault at (a) Gen-1 terminal (b) Thruster-2 terminal (c) Section II of the bus-bar.

zero crossing; solid state circuit breakers (SSCBs) are conceived to be advantageous for such applications, which have additional advantages of lack of arcing process and well-defined pre-existing control techniques [114]. The relatively higher on-state resistance of SSCBs and the requirement of isolator for galvanic isolation are some of the issues that need to be mitigated. The on-state resistance could be reduced by connecting the SSCB blocks in optimized series-



6.2(a)



6.2(b)

Fig. 6.2: Variation of (a) Gen-1 current and (b) Thruster-2 current during fault F_1 and F_2, respectively. The variation in current are shown when the traditional directional protection is applied.

parallel combination [106]. An IGBT/IGCT based SSCB is considered in this chapter as it has lower turn-off time < 400 μs and higher current interrupting capability [106]. Apart from the fault isolation, a modified topology of SSCB should be used to block the load side dc-link capacitor discharge, as discussed in Subsection 5.3.4. Hence, the load side SSCBs would have different structure as compared with those at the generator, line or busbar sides. Based on the decision of IED, the TRIP/BLOCK command is issued to the respective load side SSCBs. The structure of the IED and SSCB is shown in Fig. 6.8. The load side IED is different from the IED of the generator and the bus-bar as the load side IED has additional responsibility of blocking the fault current.

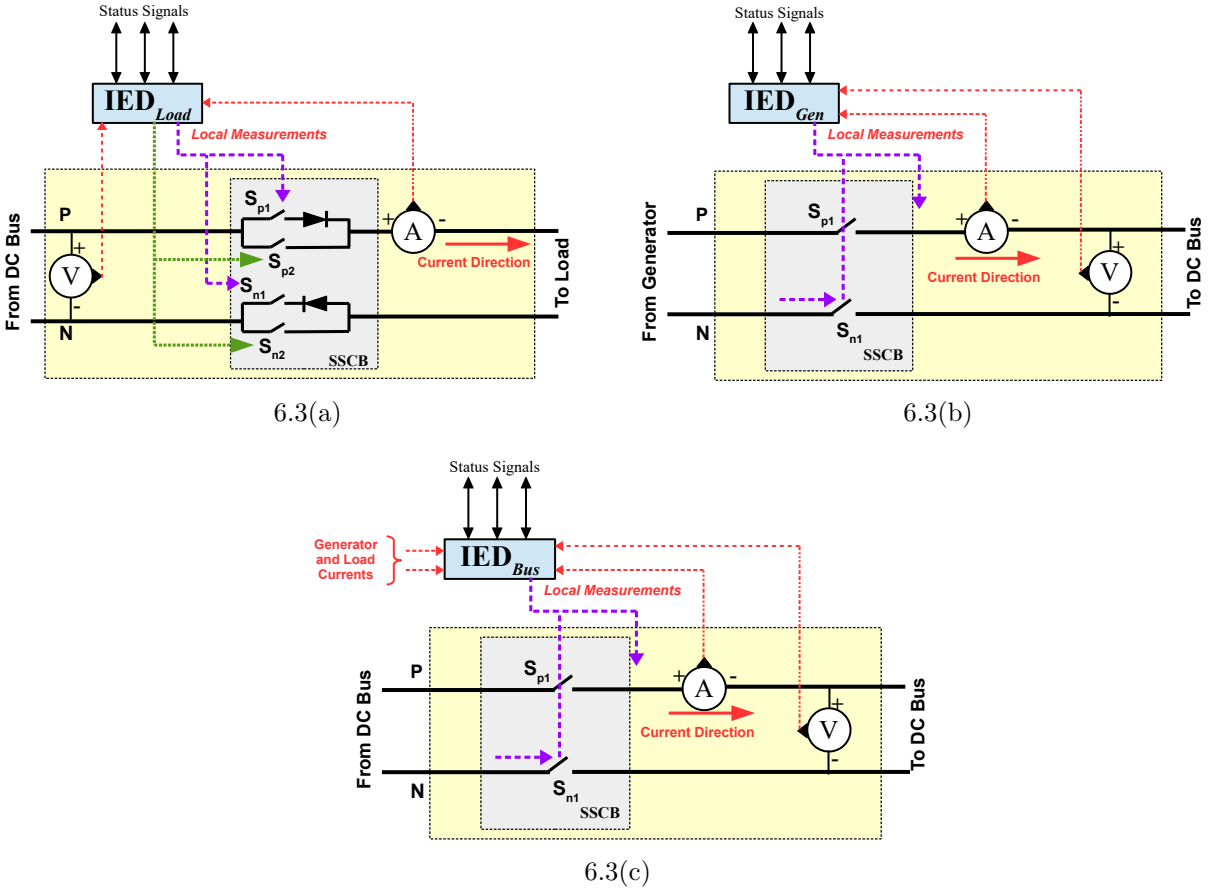


Fig. 6.3: Detailed diagram of (a) load side IED (b) generator side IED and (c) bus-bar side IED.

6.3.3 Back-up Protection for the Traditional Directional Protection

Back-up protection comes into action when the primary directional protection fails. With reference to Fig. 6.1, the following back-up protection logic is developed for faults F_1, F_2 and F_3.

Back-up Protection for IED_{Gen}

If the IED_{Gen} fails to operate during the faults at the generator terminals, the Bus_{IED} should TRIP on directional OC and the $Load_{IED}$ should remain in the BLOCKED condition. Thus, for fault F_1, if IED1 fails to act, IED 6 should trip on directional OC while the IED 3 should remain in the blocked condition, which is shown in (6.8).

$$\text{IED}\,1_{Back\ Up} \implies \text{IED}\,6_{Backup\ Trip}\ \&\&\ \text{IED}\,3_{Block} \tag{6.8a}$$

$$\text{IED}\,6_{Backup\ Trip} \implies \mathbb{D}_{\text{IED}\,6} = 0\ \&\&\ i_{\text{IED}\,6} < -i_{BackUp\ Bus}\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.8b}$$

$$\text{IED}\,3_{Block} \implies \mathbb{D}_{\text{IED}\,3} = 0\ \&\&\ V_{Bus} < V_{Threshold}. \tag{6.8c}$$

Back-up Protection for IED_{Load}

If the IED_{Load} fails to operate during the faults at the load terminals, the IED_{Bus} and IED_{Gen} should TRIP on directional OC. If some other loads are present their IEDs should block the dc-link discharge from them. Thus, for fault F_2 (Fig. 6.1(b)) if IED 4 fails to TRIP then IED 2 and IED 6 TRIPs on directional OC while IED 5 becomes BLOCKED which is shown in (6.9).

$$\text{IED}\,4_{Back\ Up} \implies \text{IED}\,2_{Backup\ Trip}\ \&\&\ \text{IED}\,6_{Backup\ Trip}\ \&\&\ \text{IED}\,5_{Block} \tag{6.9a}$$

$$\text{IED}\,6_{Backup\ Trip} \implies \mathbb{D}_{\text{IED}\,6} = 1\ \&\&\ i_{\text{IED}\,6} > i_{BackUp\ Bus}\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.9b}$$

$$\text{IED}\,2_{Backup\ Trip} \implies \mathbb{D}_{\text{IED}\,2} = 1\ \&\&\ i_{\text{IED}\,2} > i_{BackUp\ Gen}\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.9c}$$

$$\text{IED}\,3_{Block} \implies \mathbb{D}_{\text{IED}\,3} = 0\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.9d}$$

Back-up Protection for IED_{Bus}

If the IED_{Bus} fails to operate for either faults in the Section I or Section II, all the IED_{Load} should be under BLOCKED condition. Thus, for fault $F3$, if IED 6 fails to trip, then IED 1 & IED 2 TRIPs on directional OC while the IED 3, IED 4 and IED 5 becomes BLOCKED as shown in (6.10) .

$$\text{IED}\,6_{Back\ Up} \implies \text{IED}\,1,2_{Backup\ Trip}\ \&\&\ \text{IED}\,2_{Backup\ Trip}\ \&\&\ \text{IED}\,3,4,5_{Block} \tag{6.10a}$$

$$\text{IED}\,1,2_{Backup\ Trip} \implies \mathbb{D}_{\text{IED}\,1,2} = 1\ \&\&\ i_{\text{IED}\,1,2} > i_{BackUp\ Gen}\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.10b}$$

$$\text{IED}\,3,4,5_{Block} \implies \mathbb{D}_{\text{IED}\,3,4,5} = 0\ \&\&\ V_{Bus} < V_{Threshold} \tag{6.10c}$$

Load Back-up Tripping

The IED_{Load} is blocked to restrict the negative current which is a part of the backup protection strategy. As described in Section 5.3.4, the dc-link capacitor is designed as per the capacitor hold-up time ($t_{hold\ up}$). Thus, if the IED_{Load} is BLOCKED for more than $t_{hold\ up}$, IED_{Load} should initiate the TRIP command as per (6.11). The BLOCK condition is initiated to increase the availability of the propulsion systems.

$$\text{IED}_{Load-TRIP} \implies \text{IED}_{Load-BLOCK}\,|_{t>t_{hold\ up}} \tag{6.11}$$

6.3.4 Current/Voltage Thresholds and Protection Settings

The current and voltage thresholds are important for the operation of the traditional directional protection approach. Moreover, for the backup protection, the OC settings of IED_{Gen}, IED_{Load} and IED_{Bus} should be different from each other to enhance selective tripping operation.

Current Threshold

(i) IED_{Gen} **Settings:** For the primary protection, fault detection by the IED_{Gen} is only dependent on the directional element output and UV threshold and is independent of the current magnitude. Thus, for primary protection i_{Gen} is irrelevant. However, IED_{Gen} also supports the backup protection for IED_{Load} and $\text{IED}_{Bus-bar}$ where i_{Gen} is selected to be 2 $\times$ rated dc generator current.

(ii) IED_{Load} **Settings:** For the primary protection, fault detection by the IED_{Load} is dependent on the directional element output, OC magnitude and the UV threshold. Thus, for primary protection i_{Load} is chosen to be 3 $\times$ the nominal propulsion current. The IED_{Load} also supports for the backup protection for IED_{Gen} and $\text{IED}_{Bus-bar}$ where it is BLOCKED initially and is TRIPPED on Load backup TRIPPING (6.11).

(iii) IED_{Bus} **Settings:** For the primary protection, fault detection by the IED_{Bus} is only dependent on the directional element output and UV threshold and is independent of the current magnitude. Thus, for primary protection i_{Bus} is irrelevant. However, the

IED_{Bus} also supports for the backup protection for IED_{Gen} and IED_{Load} where i_{Bus} is selected to be 1.5 × rated dc generator current.

The consolidated current threshold settings for all the IEDs are shown in Table 6.1. The base current is taken as the dc generator output full load current (1365 A). For the back-up protection the IED_{Bus} is set to trip at 1.5 *p.u.* and IED_{Gen} is set to 2 *p.u.* This differentiation in the current setting is done to avoid protection malfunction.

Table 6.1: Current Threshold Settings

Fault Location	**IED No.**	**Main Protection**	**Back-up Protection**
Gen-1	IED1	$i_{\text{IED}\,1} < 0$	$i_{\text{IED}\,6}$< -2048A (1.5 pu)
Gen-2	IED2	$i_{\text{IED}\,2}$<0	$i_{\text{IED}\,6}$> 2048A (1.5 pu)
Motor-1	IED3	$i_{\text{IED}\,3}$>1800A (1.32 pu)	$i_{\text{IED}\,6}$< -2048 (1.5 pu); $i_{\text{IED}\,1}$> 2730A (2 pu)
Houseload	IED4	$i_{\text{IED}\,4}$>600A (0.44pu)	$i_{\text{IED}\,6}$> 2048A(1.5 pu); $i_{\text{IED}\,1}$> 2730A (2 pu)
Motor-2	IED5	$i_{\text{IED}\,5}$>1800A (1.32 pu)	$i_{\text{IED}\,6}$> 2048A (1.5 pu); $i_{\text{IED}\,1}$> 2730A (2 pu)
Bus-bar Upstream	IED6	$i_{\text{IED}\,1}$> 0 && $i_{\text{IED}\,6}$< 0 && $i_{\text{IED}\,4}$< 0	$i_{\text{IED}\,4}$> 2730A (2 pu); $i_{\text{IED}\,2}$> 2730A (2 pu)
Bus-bar Downstream	IED6	$i_{\text{IED}\,2}$> 0 && $i_{\text{IED}\,6}$> 0 && $i_{\text{IED}\,4}$> 0 && $i_{\text{IED}\,5}$> 0	$i_{\text{IED}\,1}$> 2048A (1.5 pu); $i_{\text{IED}\,2}$> 2730A (2 pu)

Voltage Threshold

The UV threshold ($V_{Threshold}$) is an indicator of the fault condition. Thus, the $V_{Threshold}$ becomes an important parameter for the traditional directional protection. As the loads in dc SPS is mostly the constant power loads (CPLs), selecting very less voltage will increase the current consumption, which can lead to instability. With this regards, $V_{Threshold}$ has been set to 80% of the rated voltage (V_{Rated}).

$$V_{Threshold} = 0.8 \times V_{Rated} \tag{6.12}$$

Since the V_{rated} is 1500 V, the $V_{Threshold}$ comes out to be 1200 V.

The Algorithm of the Back-Up protection has been included in Appendix B.

6.3.5 Back-Up Protection Example: Faults at Propulsion Load

The backup protection with the current and voltage settings are tested for fault $F2$ as shown in Fig. 6.1(b) when IED 4 fails to generate the TRIP command. From Fig. 6.1(b), it can be

seen that the fault current for $F2$ is contributed by Gen-1 and Gen-2. Since the fault is at Section II, IED 6 and IED 2 is tripped as back-up protection as per the defined current and voltage protection setting and is shown in Fig. 6.4. It can be seen that IED 6 TRIPs as soon as the bus-bar current reached 1.5 p.u. The IED 2 is tripped when Gen-2 current reached 2 p.u. It can be seen that IED 1 and Gen-1 current is not effected as the current threshold setting of IED 6 is lower than IED 1 & IED 2.

6.4 Overcoming Limitations of Traditional Directional Protection

6.4.1 Limitations of the Traditional Directional Protection

It is seen in the earlier sections that $\mathbb{D}$ is instrumental for fault detection and localisation in dc SPS. However, it is to be noted that $\mathbb{D}$ is merely an indicator of current flow direction which might also change during load switching, regenerative actions, generator/load outage and so on. To identify the fault conditions, the traditional directional protection uses the bus UV and line OC. This method is applied to the full-fledged dc PSV (in Fig. 6.5). The fault detection time for a range of fault impedances are shown in Table 6.2 for the faults F_1, F_2, F_3 and F_4 in Fig. 6.5. Since the traditional directional protection is dependent on a number of parameters such as the bus voltage, direction of multiple IEDs along with current and voltage thresholds; the time required in such cases for fault detection is quite higher ($>$ 10 ms) than the required time which is $\approx$ 5ms (as explained in Section 5.3 of Chapter 5). Moreover, modeling $\mathbb{D}$ as per (6.1) results in satisfactory operation for low-impedance faults and might not work well for the high-impedance faults. For instance in Fig. 6.5, the current magnitude is negative for the fault F_1 and thus $\mathbb{D} = 0$. Variation of $\mathbb{D}$ (as per (6.1)) is illustrated in Fig. 6.6(a) where the change in current direction of IED 1 is monitored while increasing fault resistance at F_1. For high-impedance faults, it is seen that the limit of the $\mathbb{D}$ is reached at 0.05 Ω. Thus, the current will not reverse making $\mathbb{D} = 1$ for the high-impedance fault at F_1. This makes the traditional directional protection inoperable for high-impedance faults. Similar studies have been conducted for faults F_2, F_3 and F_4. The time required (in ms) to detect the fault and the limit of fault resistance is illustrated in Table 6.2.

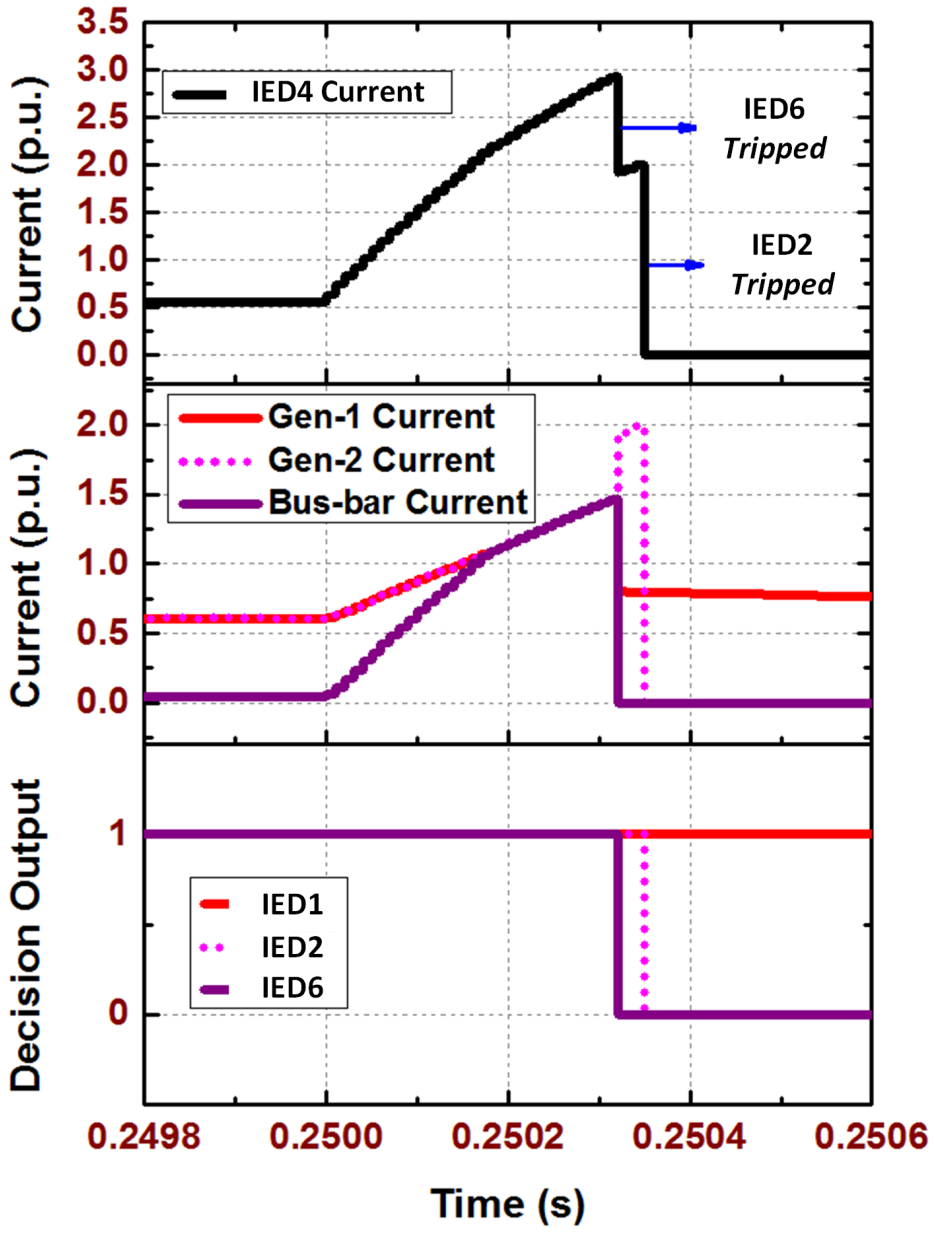


Fig. 6.4: Back-up protection for fault F_2 at IED 4.

6.4.2 Proposed Directional Protection

To mitigate the drawbacks of the traditional $\mathbb{D}$ in (6.1), the $\mathbb{D}$ could be alternatively be modeled as:

$$\mathbb{D} = \begin{cases} 1, & \text{if} \quad i[n] - i[n-1] \geqslant +\delta \quad (\textit{Forward Direction}) \\ 0, & \text{if} \quad i[n] - i[n-1] \leqslant -\delta \quad (\textit{Reverse Direction}) \\ X, & \text{if} \quad i[n] - i[n-1] < |\delta| \quad (\textit{No Change}) \end{cases} \tag{6.13}$$

The new $\mathbb{D}$ compares the present current sample ($i[n]$) and past current sample values ($i[n-1]$) to determine the direction of the fault current. Here, δ is a non-zero constant while $\mathbb{D}$ retains the previous operating value ($X = \{0, 1\}$) when the current difference lies between $\pm\ \delta$. The conventional method, i.e. (6.1), is ineffective in the high-impedance fault region while the modified method (6.13) is dependent on the selection of δ. δ should be higher than the ripple content of the dc current otherwise $\mathbb{D}$ might give erroneous outputs. Comparison of (6.13) is done with (6.1) to illustrate its effectiveness and is shown in Fig. 6.6(b) and

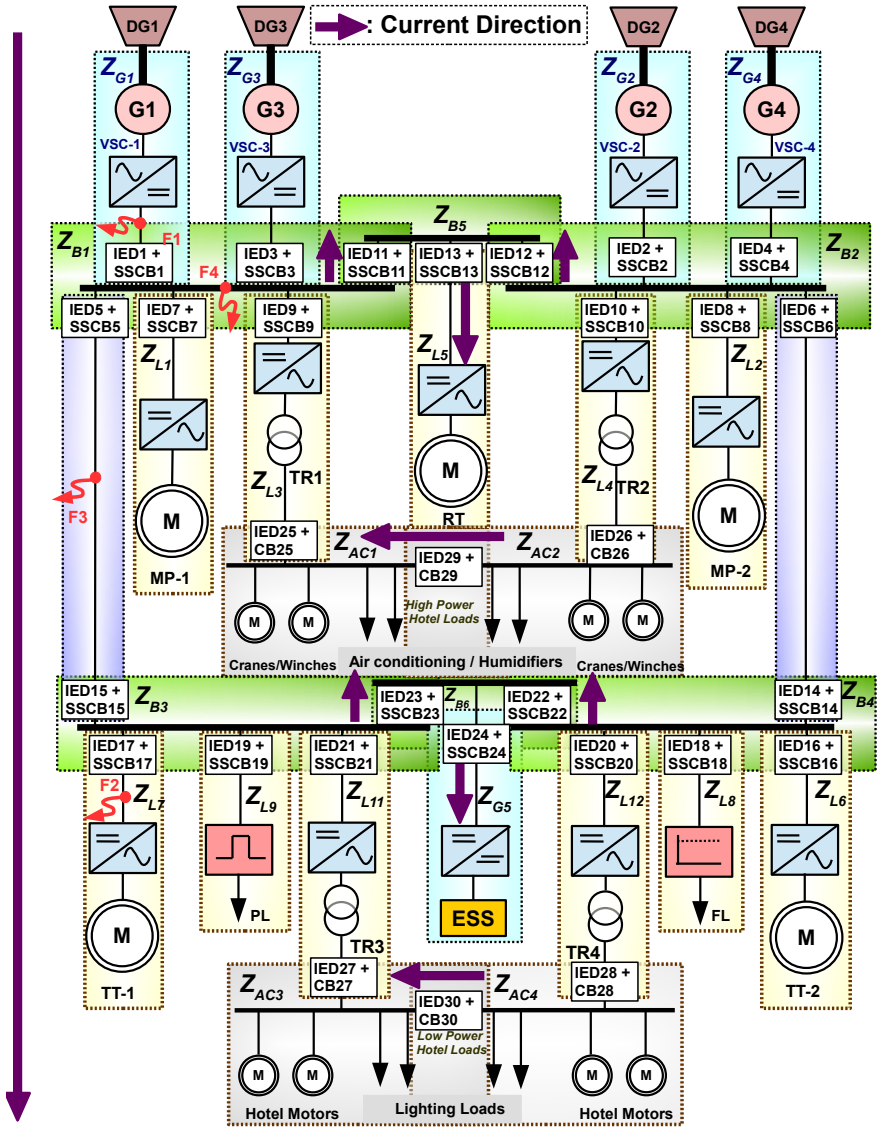


Fig. 6.5: Representative dc PSV for dc fault studies.

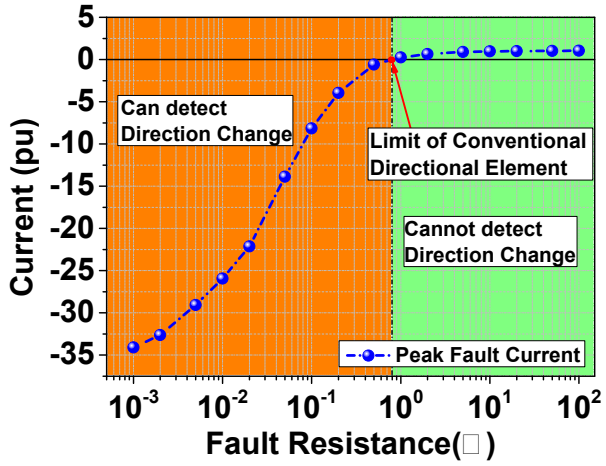
Fig. 6.6(c). It can be inferred that reducing δ will increase the operational limit of $\mathbb{D}$ (as per (6.13)) for higher fault impedances.

In addition to the $\mathbb{D}$ as per (6.1), the traditional directional protection is dependent on the OC and UV thresholds. Setting the thresholds will be difficult for the dc SPS which has varying fault current levels with changing system configuration as discussed in Subsection 5.3.4. Further the thresholds are not fixed and need to be optimized depending on the system configuration. Even if some threshold values are selected, they would be difficult to achieve for the medium to high-impedance faults owing to the lower fault currents. The generator system may see the high-impedance as a load change operation with no substantial increase in the fault current and reduction in the bus voltage. Hence, for the application in the dc SPS, the directional protection is required to be independent of the voltage and current magnitudes. Instead of time-domain based OC and UV detection, Short-Time Fourier Transform (STFT) based fault detection as discussed in Chapter 5 can be embedded in the directional protection for the application in dc PSVs. It detects the fault conditions by analyzing the presence of high frequency components in the current signals and does not require optimized tripping set-points. With this method, the UV detection

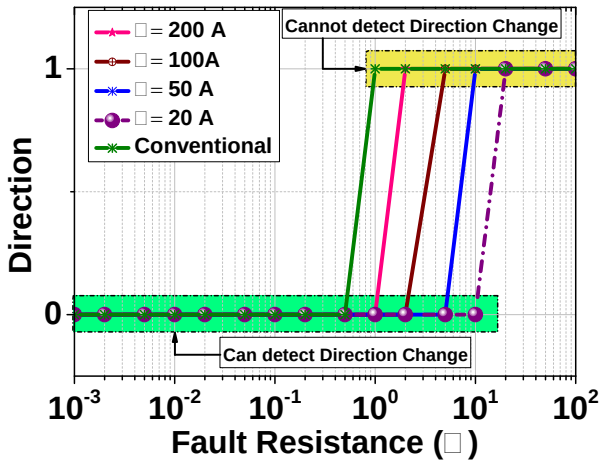
Table 6.2: Time Taken (ms) to Detect Fault Using Traditional Directional Protection

Fault Resistance	**Fault F1**	**Fault F2**	**Fault F3**	**Fault F4**
0.001 Ω	13.2	17.6	12.0	12.1
0.002 Ω	13.1	16.6	21.1	12.2
0.005 Ω	13.4	21.2	12.2	13.4
0.01 Ω	13.2	23.4	13.3	12.9
0.02 Ω	14.9	24.0	12.2	12.8
0.05 Ω	13.2	24.2	13.9	13.5
0.1 Ω	ND	ND	13.9	12.9
0.2 Ω	ND	ND	ND	ND
0.5 Ω	ND	ND	ND	ND
1 Ω	ND	ND	ND	ND
2 Ω	ND	ND	ND	ND
5 Ω	ND	ND	ND	ND
10 Ω	ND	ND	ND	ND
20 Ω	ND	ND	ND	ND
50 Ω	ND	ND	ND	ND
100 Ω	ND	ND	ND	ND

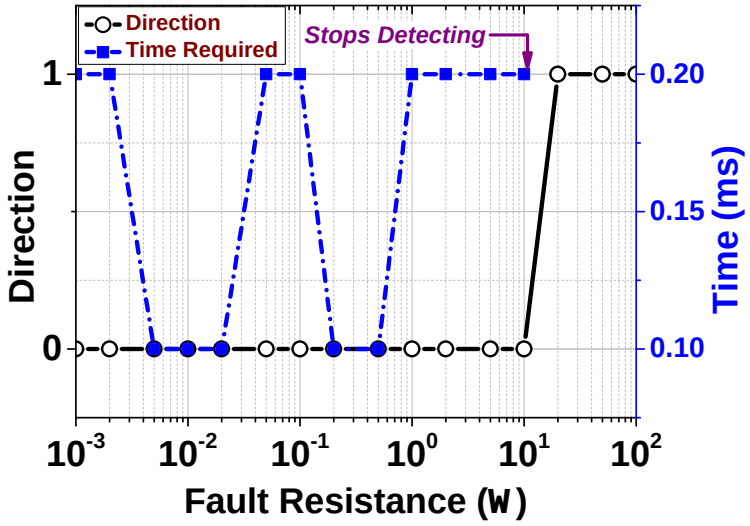
ND- No Detection, $V_{thresh} = 0.8$ pu; $I_{Threshold} = 2$ pu.



6.6(a)



6.6(b)



6.6(c)

Fig. 6.6: (a) Peak current through IED1 when fault F_1 resistance is varied from 0.001 Ω to 100 Ω. (b) Comparison of the proposed $\mathbb{D}$ (with various δ in (6.13) against conventional $\mathbb{D}$ in (6.1). (c) Time required and $\mathbb{D}$ output for IED1 when δ=10 A (in (6.13)) is employed.

will not be required thus omitting the need of expensive voltage transducers. This becomes another major advantage of the modified directional protection algorithm which is based on the STFT based fault detection algorithm.

For enhanced selective fault detection, the entire dc PSV is divided into several zones ($f(\mathcal{Z})$) with the coordinated operation of the IEDs. $\mathbb{D}$ is computed in the IEDs of a specific zone and is termed as directional zonal interlocking (DZI). Thus, DZI is the operation of $\mathbb{D}$

within a defined ($f(\mathcal{Z})$). Hence, $\mathbb{D}$ would be useful to determine the location of zone ($\mathcal{Z}$) when a change in current direction has occurred. Based on the common functionalities $f(\mathcal{Z})$ is defined as per (6.14) and is marked in Fig. 6.5.

$$f(\mathcal{Z}) = \begin{cases} \mathcal{Z}_{Gi},\ i = 1:5 & : \text{generation systems} \\ \mathcal{Z}_{Lj},\ j = 1:11 & : \text{loads} \\ \mathcal{Z}_{Bk},\ k = 1:6 & : \text{buses} \\ \mathcal{Z}_{ACm},\ m = 1:4 & : \text{ac systems} \\ \mathcal{Z}_{Cn},\ n = 1:2 & : \text{lines / cables} \end{cases} \tag{6.14}$$

After identifying the ($f(\mathcal{Z})$), fault condition is confirmed by the STFT algorithm and thus issuing the TRIP command. With this regard, Section 6.5 introduces a novel current-only directional protection method which uses modified directional protection as per (6.13) and the STFT based fault detection.

6.5 Protection Algorithm Design of the Proposed Current-Only Directional Protection

From the earlier discussions, it is inferred that the DZI and STFT based protection is suitable for dc SPS. The directional element in DZI should only determine the direction of the fault current while the tripping decision is initiated by the STFT based fault detection algorithm. As discussed in Chapter 5, STFT is a frequency-domain analysis that helps in the quantitative analysis of the frequency components present in the input signal. This is determined by computing the discrete Fourier transform of the signal over a pre-defined window function. In the discrete domain, it is expressed as follows:

$$\mathcal{S}_{\mathcal{D}}[m,k] = \sum_{n=0}^{n=N-1} i[n]w[n-mH]e^{-j\frac{2\pi nk}{N}}, \tag{6.15}$$

where, $i[n]$ is the input signal, $w[n]$ is the window function, N is the number of FFT points, n is the time-domain index of $i[n]$, m is the position of $w[n]$ around which it is real and symmetric, H is the hop size between the successive windows and k is the frequency index. n is decided by the length of $w[n]$. The parameters used for computing $\mathcal{S}_{\mathcal{D}}$ are listed in Table 6.3 [29, 182]. The fault detection by $\mathcal{S}_{\mathcal{D}}$ has been explained in detail in Chapter 5,

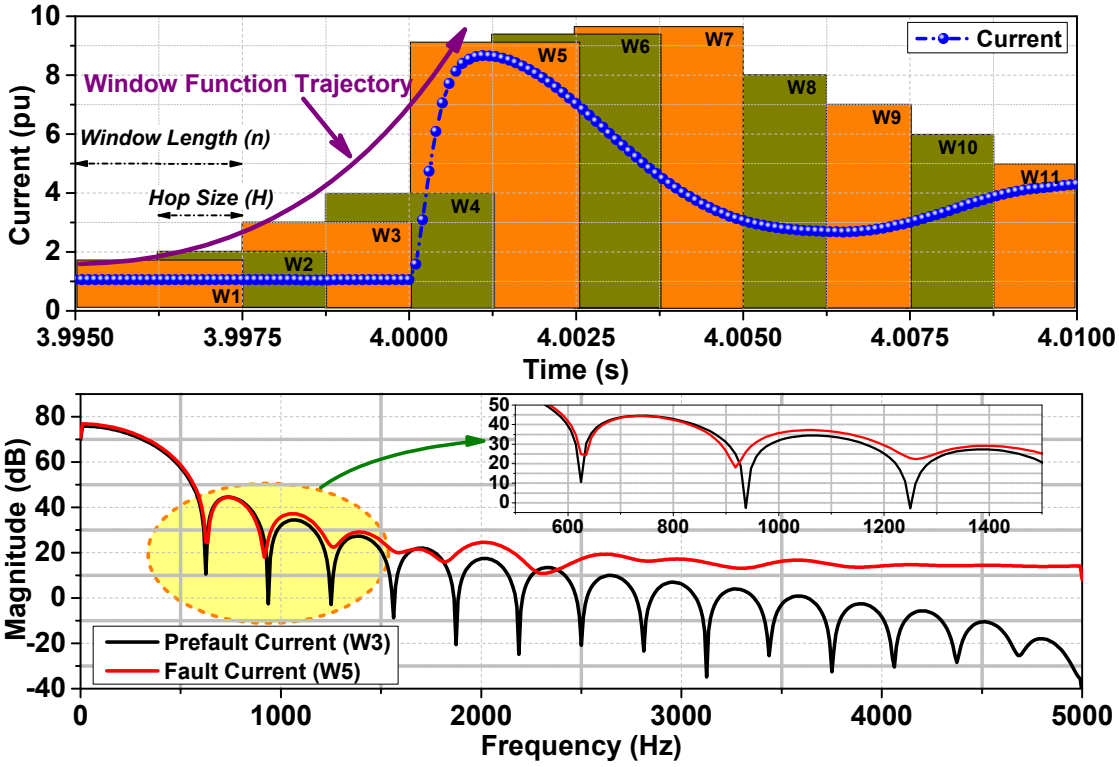


Fig. 6.7: STFT operation to detect the high frequency components in the fault current.

and is illustrated in Fig. 6.7 where $w[n]$ is applied to $i[n]$. For the prefault current, the frequency spectrum has nearly zero magnitude at update frequency bins (f_u), which is shown in Fig 6.7. The locations of f_u for given parameters are shown in Table 6.4. During the faults in dc PSV, the rapid discharge from the dc-link capacitor is expected to be comprised of high frequency components. This ingression of the high frequency components in the fault current is identified by the increased magnitude at f_u, i.e. $|\mathcal{S}_{\mathcal{D}}|_{f_u}$, and is illustrated in the inset of Fig. 6.7. Thus, along with DZI, this STFT algorithm will be embedded in the IED and will operate according to:

$$\mathcal{S}_{\mathcal{D}fault} = \begin{cases} 1, & \text{if } |\mathcal{S}_{\mathcal{D}}|_{f_u} \geqslant \sigma \ dB \\ 0, & \text{otherwise} \end{cases} \tag{6.16}$$

where, σ is the fixed setpoint (in dB). STFT is applied for the fault currents with different system configurations, as listed in Table 5.2, where the OC protection would be challenging to implement. In spite of the changing system configuration and blocking/unblocking of the loads, the STFT is able to detect the fault condition as shown in Table 6.5.

Table 6.3: Parameters Used in STFT Algorithm

Sampling Frequency (f_s)	$\boldsymbol{H}$	$\boldsymbol{N}$	**Time Res.** ($=H/f_s$)	**Freq. Res.** ($=f_s/n$)
10 kHz	1	32	0.1 ms	312.5 Hz

Table 6.4: Update-Frequency Bins for 32 Sample Hanning Window

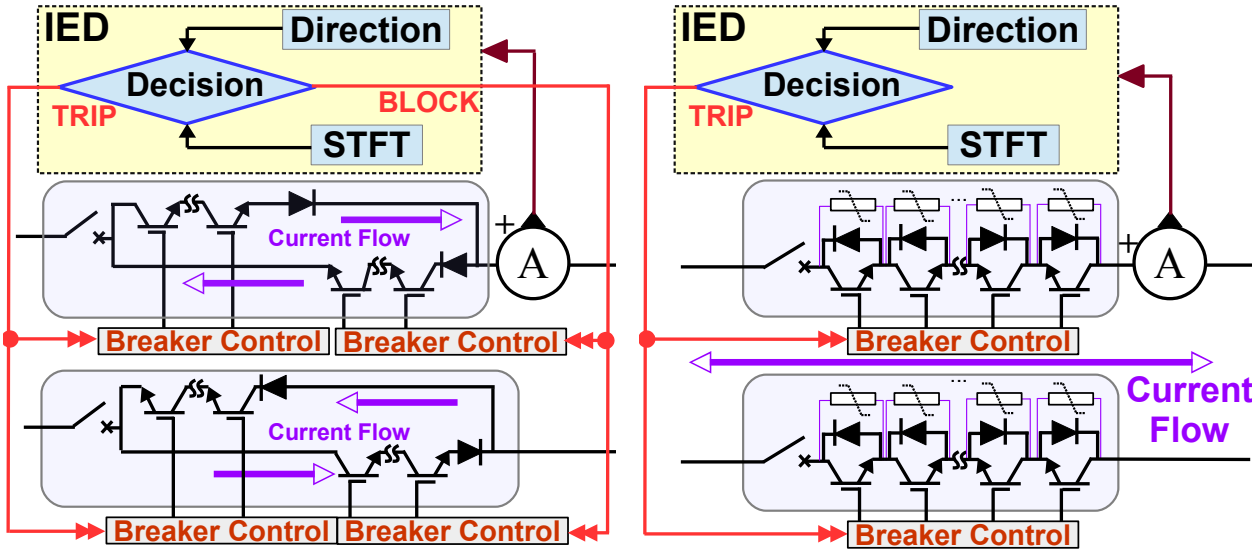
Window Type	**Win. Length** [n]	**Update Frequency Bins** (f_u)		
		$2f_s/n$	$3f_s/n$	$4f_s/n$
Hanning Window	32	625 Hz	937.5 Hz	1250 Hz

Table 6.5: Magnitude at Update Frequency Bins of 625 Hz for the STFT of i_{IED5} and i_{IED15} and Time to Reach

Case	**Mode**	**IED5**		**IED15**	
		$\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}$ (dB)	$t_{\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}}$ (ms)	$\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}\rvert$ (dB)	$t_{\lvert\mathcal{S}_\mathcal{D}\rvert_{f_u}}$ (ms)
1	Before Blocking	22.2567	0.2	37.866	0.4
	After Blocking	22.2567	0.2	32.6968	0.4
2	Before Blocking	45.6311	0.4	21.2959	0.2
	After Blocking	22.5083	0.2	39.6161	0.4
3	Before Blocking	24.7209	0.2	40.2659	0.4
	After Blocking	24.6852	0.2	36.293	0.4
4	Before Blocking	24.2759	0.2	44.8228	0.4
	After Blocking	24.2759	0.2	40.4097	0.4
5	Before Blocking	21.9615	0.2	37.5648	0.4
	After Blocking	21.9615	0.2	32.3493	0.4
6	Before Blocking	23.234	0.2	44.804	0.4
	After Blocking	23.234	0.2	39.0298	0.4

$\sigma = 20$ dB, $f_u = 625$ Hz

The direction of prefault current in the dc PSV is predetermined as indicated by thick arrows in Fig. 6.5. The STFT is combined with $\mathbb{D}$ to devise the protection logic of the dc PSV. The logical output of the STFT, i.e. $\mathcal{S}_\mathcal{D}$ (based on (6.16)) and $\mathbb{D}$ (based on (6.13)), are calculated in the IEDs. Based on such outputs, the various possible outcomes of the IEDs are listed in Table 6.6. This information has been used for devising protection logic for faults at locations F_1, F_2, F_3 and F_4 (Fig. 5.1) is discussed in the next section. Since the DZI and STFT based directional protection is only dependent on the current sensing, the schematic of the IED and SSCB would be bit different from Fig. 6.3.



6.8(a) 6.8(b)

Fig. 6.8: Diagram of the IED along with the SSCBs for interfacing (a) loads and (b) generator, lines and bus-bar.

Table 6.6: Truth Table of IED Depicting Various Possibilities

$\mathbb{D}$	$\mathcal{S}_{\mathcal{D}fault}$	**State**	**Notation**
0	0	Regenerative Operation	*RO*
0	1	Faults at Reverse Direction	*RF*
1	0	Normal Operation	*NO*
1	1	Faults in Forward Direction	*FF*

6.6 Case Studies With Proposed Current-Only Directional Protection

The prime components of the dc shipboard power systems are the generators, loads, lines and bus-bars. Thus for network protection in dc ships, the possible fault locations (F_1, F_2, F_3 and F_4) are chosen at these locations which correspond to the faults at the generator terminals, load terminals, buses, and cables. The faults are never perfect and are complex in nature, where the fault impedance changes from very high-impedance to low-impedance. To study the response of the proposed current-only directional protection, fault impedance is varied from low-impedance i.e. 0.001 Ω to very high impedance i.e. 100 Ω at all the

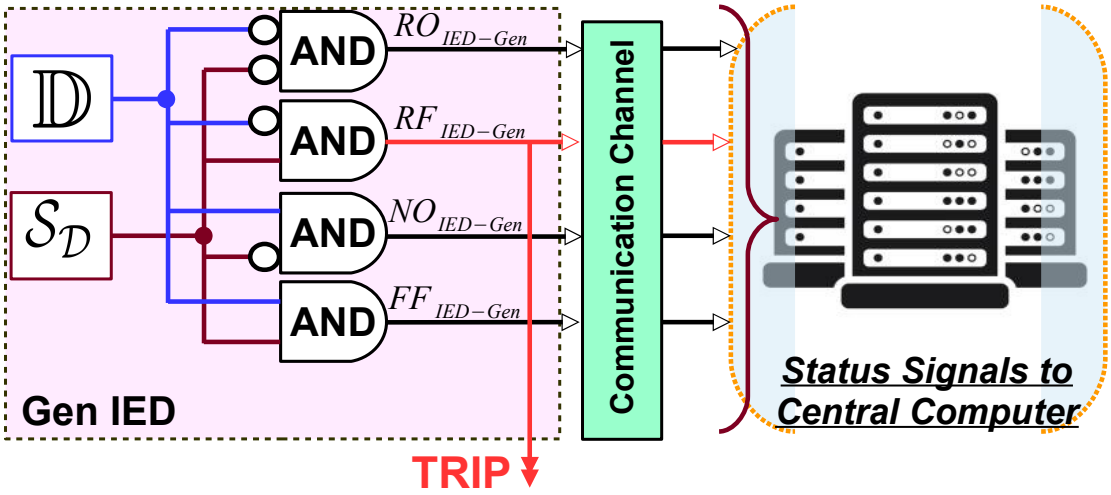


Fig. 6.9: Logic diagram for generator protection.

designated fault locations.

6.6.1 Faults at Generator Terminal

The faults at generator zone $\mathcal{Z}_G$ is identified by RF, i.e. the reversal of current through the respective IED with the presence of high frequency components in it. For illustration, fault F_1 at Gen-1 terminal (Fig. 6.5) is detected by RF_{IED1}, which is given by:

$$RF_{\text{IED}_{Gen}} \implies \mathbb{D} = 0 \;\; \&\& \;\; |\mathcal{S}_{\mathcal{D}}|_{f_u} \; > \; \sigma_{gen} \; dB. \tag{6.17}$$

The relay diagram for generator IED incorporating (6.17) with notations consistent with Table 6.6 is shown in Fig. 6.9. Operation of the IED1 for fault F_1 with increasing fault resistances is shown in Table 6.7. For low-impedance faults, IED1 is able to detect the fault condition and initiate TRIP command. However, for extremely high-impedance faults, STFT is high but since $\mathbb{D}$ is not able to detect the change in current direction, IED is set to ALARM output.

6.6.2 Faults at Load Terminal

The faults at load zone $\mathcal{Z}_L$ is identified by FF through the respective load IEDs. Such cases are identified by:

$$FF_{\text{IED}_{Load}} \implies \mathbb{D} = 1 \;\; \&\& \;\; |\mathcal{S}_{\mathcal{D}}|_{f_u} \; > \; \sigma_{load} \; dB. \tag{6.18}$$

Table 6.7: Decision Time of IED1 as per Fig. 6.9 for Different Values of Fault Resistance F_1

Fault Resistance (Ω)	$\mathbb{D}$	$t_{\mathbb{D}}$ (ms)	$\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}$ (dB)	$t_{\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}}$ (ms)	**Trip/Alarm**	**Decision Time** (ms)
0.001	0	0.2	27.41	0.4	TRIP	0.4
0.002	0	0.2	35.73	0.4	TRIP	0.4
0.005	0	0.2	30.54	0.4	TRIP	0.4
0.01	0	0.2	32.33	0.4	TRIP	0.4
0.02	0	0.2	21.27	0.2	TRIP	0.2
0.05	0	0.2	28.33	0.4	TRIP	0.4
0.1	0	0.2	25.01	0.4	TRIP	0.4
0.2	0	0.2	28.73	0.4	TRIP	0.4
0.5	0	0.2	23.54	0.4	TRIP	0.4
1	0	0.2	21.58	0.4	TRIP	0.4
2	0	0.2	23.32	0.6	TRIP	0.6
5	0	0.2	22.29	0.8	TRIP	0.8
10	0	0.2	17.44	0.8	TRIP	0.8
20	1	NaN*	16.32	0.8	ALARM	0.8
50	1	NaN*	15.60	43	ALARM	43
100	1	NaN*	15.88	543	ALARM	543

NaN*- Current direction not changing. $\sigma_{gen} = 15$ dB, $f_u = 625$ Hz.

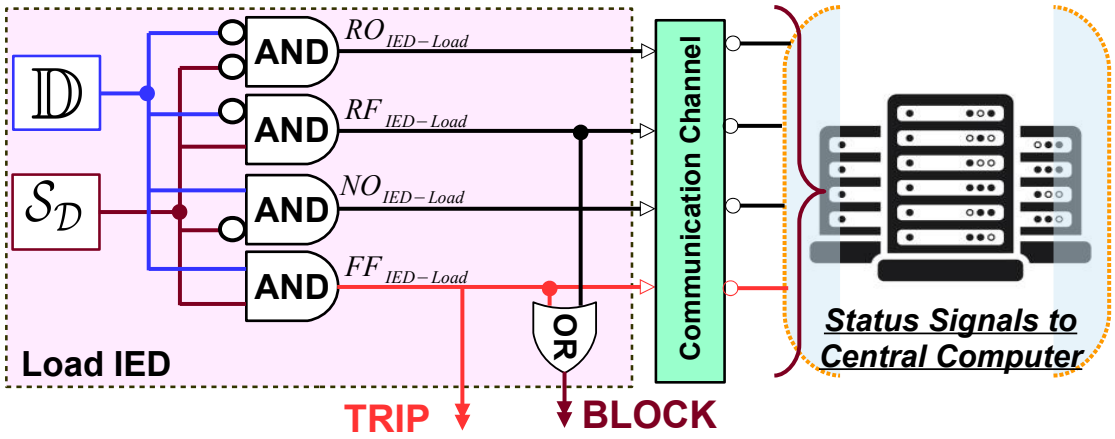


Fig. 6.10: Logic diagram for load protection.

where the current direction is similar to that of the prefault current along with the presence of high frequency components. The faults outside $\mathcal{Z}_L$ is characterized by RF as:

$$RF_{\text{IED}_{Load}} \implies \mathbb{D} = 0 \;\; \&\& \;\; |\mathcal{S}_{\mathcal{D}}|_{f_u} > \sigma_{load}\, dB. \tag{6.19}$$

In such conditions, the IEDs might block the SSCBs as discussed in Section 5.3.4.

The relay diagram for load IED is shown in Fig. 6.10 and the operation of IED17 for fault F_2 with increasing fault resistances is shown in Table 6.8. As the current direction remains

the same, the protection algorithm is dependent on the STFT output for fault detection. In such cases, the IED is unable to detect the extremely high-impedance faults.

6.6.3 Protection of Lines and Buses

Compared to the generator and load systems; protection of the lines and buses would require operation of multiple IEDs. For instance, fault F_3 in Fig. 6.5 would be detected and isolated by the operation of IED5 and IED15, while the fault F_2 will be decided by the outcome of IED1, IED3, IED11, IED5, IED7 and IED9. Hence, there is a need of communication interface among the IEDs for fault detection in the lines and buses. Centralized protection using a common protection interface could be implemented, which is expected to be adopted from the IEC 61850 based centralized ac protection systems [67]. However, the centralized protection has certain disadvantages such as single point failures, data-loss, additional communication delays etc. However, in the proposed directional protection, all the computations are done at the local IEDs whereas the status signals are exchanged with the central computer which can be transmitted at very high rate. The status signals helps

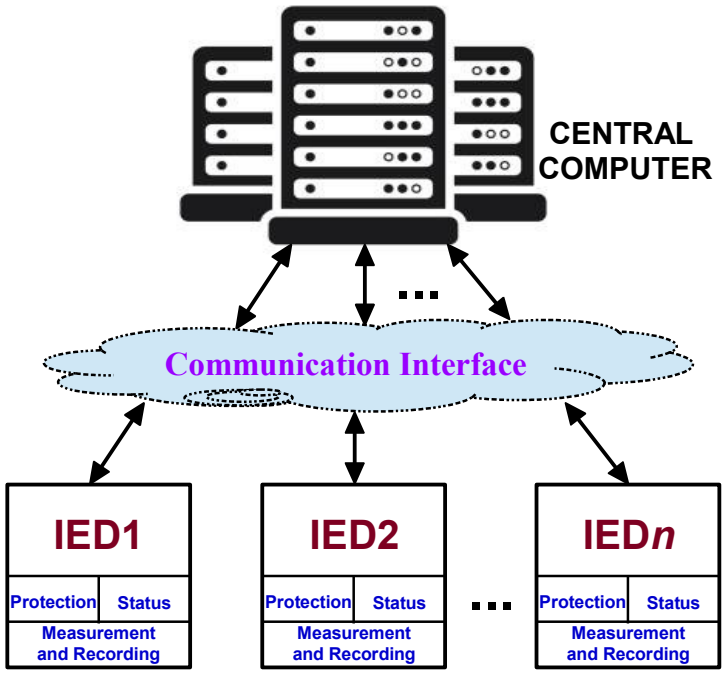


Fig. 6.11: Interface of the IEDs with the central computer for centralized protection of dc PSV.

Table 6.8: Decision Time of IED17 as per Fig. 6.10 for Different Values of Fault Resistance F_2

Fault Resistance (Ω)	$\lvert\boldsymbol{\mathcal{S}_{\mathcal{D}}}\rvert_{f_u}$ (dB)	$\boldsymbol{t}_{\lvert\boldsymbol{\mathcal{S}_{\mathcal{D}}}\rvert_{f_u}}$ (ms)	**Trip/Alarm**	**Decision Time** (ms)
0.001	20.05	0.4	TRIP	0.4
0.002	28.84	0.4	TRIP	0.4
0.005	29.87	0.4	TRIP	0.4
0.01	26.35	0.4	TRIP	0.4
0.02	28.9	0.4	TRIP	0.4
0.05	20.2	0.4	TRIP	0.4
0.1	24.58	0.4	TRIP	0.4
0.2	27.51	0.4	TRIP	0.4
0.5	29.9	0.4	TRIP	0.4
1	21.17	0.4	TRIP	0.4
2	26.86	0.6	TRIP	0.6
5	24.19	0.8	TRIP	0.8
10	21.17	0.8	TRIP	0.8
20	22.02	1.4	TRIP	1.4
50	21.01	1.4	TRIP	1.4
100	21.71	43	ALARM	43

σ_{load} = 20 dB; f_u = 625 Hz.

in determining the faults at lines and bus-bars. However, due to stringent time requirements in dc systems (Subsection 5.3.3), direct adoption of the communication infrastructure from the ac system would not be suitable for such applications. Hence, high speed optical fibre based communication could be selected for faster exchange of data. Further, adopting low-bandwidth communication would limit the hardware requirements [64]. Thus, instead of the time-stamped current samples, the IED decisions (i.e. the binary outputs) could be exchanged to compute the decision. With these considerations, the architecture of the IEDs communicating with the central computer is shown in Fig. 6.11. This topology is similar to the 5^{th} generation architecture for the centralized protection of the ac substation in [67], which has high reliability and thus making it suitable for the protection of dc PSV.

Faults at Lines

For the low-impedance fault at F_3 (Fig. 6.5), TRIP command is issued by the central computer when FF_{IED5} and RF_{IED15} are activated. For very high-impedance faults, the current through IED15 might not reverse thus it might indicate *NO* instead of *RF*. This condition can be accommodated by the ALARM output. These conditions are shown in the relay diagram in Fig. 6.12. Table 6.9 shows the outcome of IED5 and IED15 for increasing fault

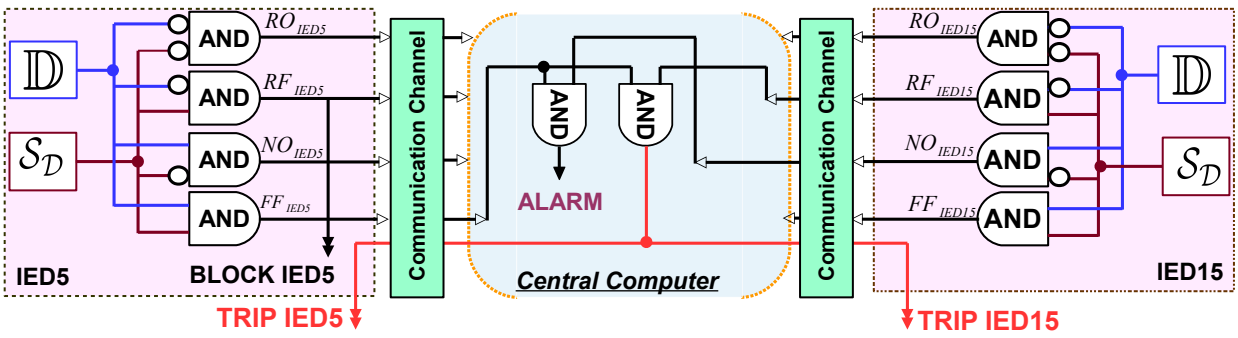


Fig. 6.12: Logic diagram for protection of fault F_3 in line of Zone-3.

Table 6.9: Decision Time of IED5 and IED15 as per Fig. 6.12 for Different Values of Fault Resistance F_3

Fault Resistance (Ω)	**IED5**	**IED15**		**Trip/Alarm**	**Decision Time** (ms)
	$t_{\lvert \mathcal{S}_{\mathcal{D}} \rvert_{f_u}}(ms)$	$t_{\mathbb{D}}$ (ms)	$t_{\lvert \mathcal{S}_{\mathcal{D}} \rvert_{f_u}}(ms)$		
0.001	0.2	0.1	0.2	TRIP	0.2
0.002	0.4	0.1	0.4	TRIP	0.4
0.005	0.2	0.1	0.2	TRIP	0.2
0.01	0.2	0.2	0.2	TRIP	0.2
0.02	0.2	0.2	0.2	TRIP	0.2
0.05	0.2	0.1	0.2	TRIP	0.2
0.1	0.2	0.1	0.2	TRIP	0.2
0.2	0.4	0.1	0.2	TRIP	0.4
0.5	0.4	0.2	0.4	TRIP	0.4
1	0.6	0.1	0.4	TRIP	0.6
2	0.6	0.2	0.6	TRIP	0.6
5	0.8	0.2	0.8	TRIP	0.8
10	1	0.1	0.8	TRIP	1.0
20	1.4	NaN	1	ALARM	1.4
50	393	NaN	393	ALARM	393
100	413	NaN	413	ALARM	413

σ_{line} = 20 dB; f_u = 625 Hz.

resistances. It is seen that the proposed method is able to fairly identify faults and initiate TRIP command. For very high-impedance faults, the method gives ALARM output.

Faults at Bus-Bar

As per Fig. 6.5, the bus-bar fault F_4 would result in tripping of all the SSCBs associated with IED1, IED3, IED7, IED9, IED5 and IED11. The outputs of all the IEDs would be sent to the central computer for computation before the TRIP signals are initiated. The

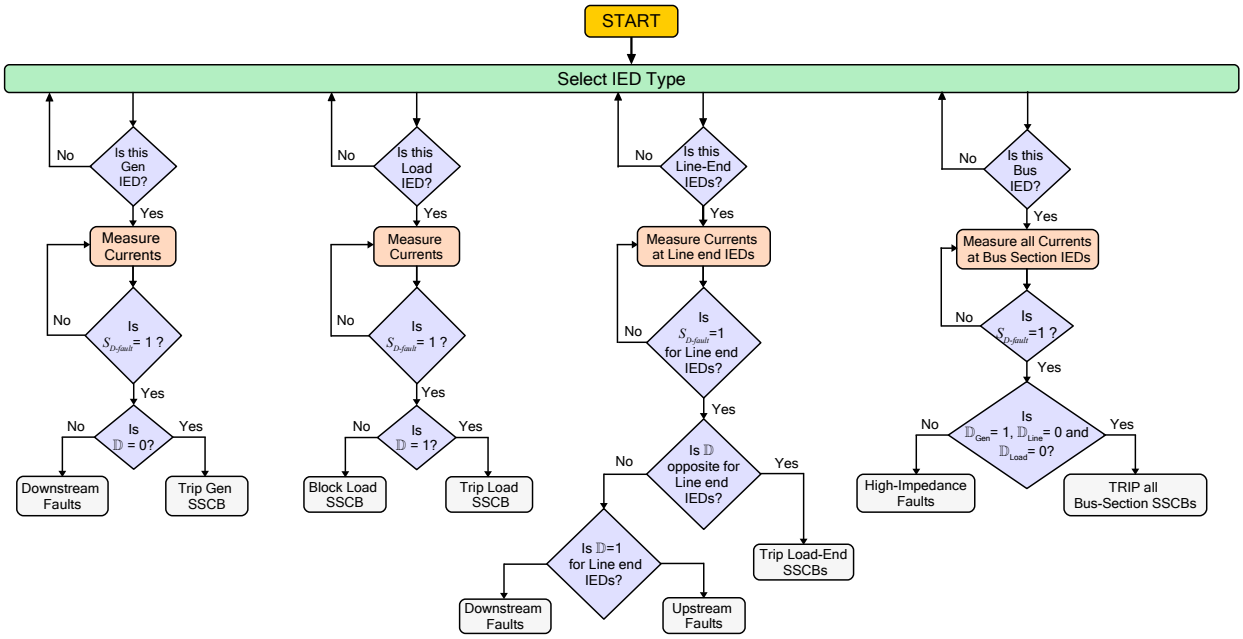


Fig. 6.13: Generalised flowchart of the proposed protection of generator, load, line and bus-bar of dc PSV.

low-impedance fault at F_4 would be characterised by $FF_{\text{IED}\,1}$, $FF_{\text{IED}\,3}$, $RF_{\text{IED}\,7}$, $RF_{\text{IED}\,9}$, $RF_{\text{IED}\,5}$ and $RF_{\text{IED}\,11}$. Current direction and STFT of IED11 is of prime importance for protection of IED11. Similar to Subsection 6.6.3, ALARM is initiated for fault F_4 when IED11 is able to detect the fault while the rest of the IEDs cannot. The detailed operation of the various associated IEDs for fault F_4 is listed in Table 6.10.

The decisions whether the IED is a GEN, LOAD, LINE or BUS IED are likely input parameters to the devices.

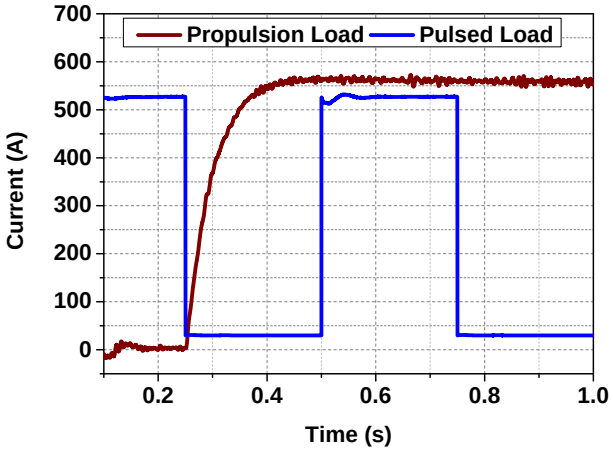
6.6.4 Generalized Flowchart for Current-Only DC Protection

The description and operation of the current-only directional protection for the application in dc PSV for the faults in generator terminals, load terminals, lines and bus-bars have been described in previous sections. Required protection logic is activated in the IEDs after making the decision whether the IED is for generator, load, line or bus-bar. Thus the type of IED is likely to be the input parameter. With this regard, the consolidated flow chart of the proposed dc protection algorithm for dc PSV is depicted in Fig 6.13.

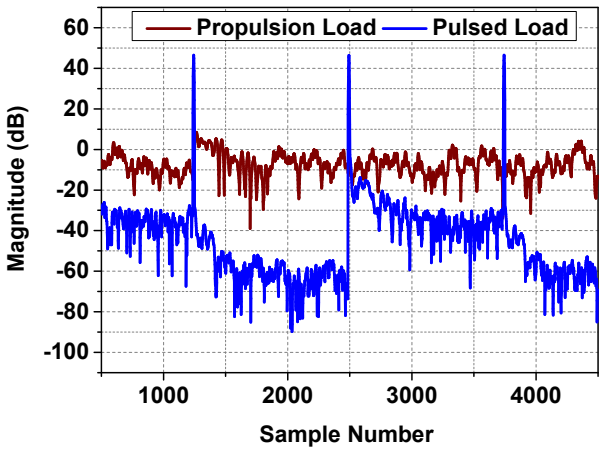
Table 6.10: Status of the IEDs in Zone $\mathcal{Z}_{B1}$ for Fault F_4

Fault Resistance (Ω)	**IED1**	**IED3**	**IED7**		**IED9**		**IED5**		**IED11**		**Trip/Alarm**	**Decision Time** (ms)
	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$	$t_{\mathbb{D}}(ms)$	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$	$t_{\mathbb{D}}(ms)$	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$	$t_{\mathbb{D}}(ms)$	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$	$t_{\mathbb{D}}(ms)$	$t_{\|\boldsymbol{S_D}\|f_u}(ms)$		
0.001	0.4	0.4	0.1	0.4	0.2	0.4	0.1	0.2	0.1	0.2	TRIP	0.4
0.002	0.4	0.4	0.2	0.4	0.2	0.4	0.2	0.2	0.2	0.2	TRIP	0.4
0.005	0.4	0.4	0.2	0.4	0.2	0.4	0.2	0.2	0.2	0.2	TRIP	0.4
0.01	0.4	0.4	0.2	0.4	0.2	0.4	0.1	0.4	0.1	0.2	TRIP	0.4
0.02	0.4	0.4	0.2	0.6	0.2	0.6	0.1	0.2	0.1	0.2	TRIP	0.6
0.05	0.4	0.4	0.1	0.4	0.1	0.4	0.1	0.4	0.1	0.4	TRIP	0.4
0.1	0.6	0.6	0.2	0.4	0.2	0.4	0.1	0.2	0.1	0.2	TRIP	0.6
0.2	0.6	0.6	0.2	0.6	0.2	0.6	0.1	0.4	0.1	0.4	TRIP	0.6
0.5	0.8	0.8	0.2	0.6	0.2	0.8	0.1	0.6	0.1	0.4	TRIP	0.8
1	0.8	0.8	NaN	1	NaN	1	0.2	0.4	0.2	0.4	TRIP	1
2	1.2	1.2	NaN	1	NaN	1.2	0.2	0.6	0.2	0.4	TRIP	1.2
5	NaN	NaN	NaN	NaN	NaN	NaN	NaN	1	0.2	0.6	ALARM	1
10	NaN	NaN	NaN	NaN	NaN	NaN	NaN	0.8	NaN	1	ALARM	1
20	NaN	NaN	NaN	NaN	NaN	NaN	NaN	31	NaN	1	ALARM	31
50	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	-	-
100	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	-	-

$\sigma_{gen}, \sigma_{load}, \sigma_{line} = 20$ dB; $f_u = 625$ Hz.



6.14(a)



6.14(b)

Fig. 6.14: (a) Time-domain characteristics of propulsion and pulsed load. (b) STFT magnitude at f_u= 625 Hz for propulsion and pulsed load.

6.6.5 Effect on the Load Change Operation

The current-only directional protection should be able to reliably detect the fault condition without spuriously tripping for the transient load changes in the dc PSV. Majority of the loads interfaced with the dc PSV are CPLs whose rise time of the load current depends on the bandwidth of the current controller and also the nature of the load. For the dominant inductive loads such as propulsion systems, ac hotel loads etc., the rise time of the current due to sudden load demand is more than the rise time of the fault current. These loads are termed as Low Bandwidth CPLs. However, with the emerging power electronic loads having high bandwidth of the current control loop and lower load inductance such as pulsed loads, the rise time of the current due to sudden load change might be comparable with the rise time of the fault current. These loads are termed as High Bandwidth CPLs. The proposed current-only directional protection algorithm should be immune to the sudden change in the Low Bandwidth and High Bandwidth CPL in the dc PSV. As per Fig. 6.5, sudden change in the propulsion load and operating the pulsed load at regular intervals are taken into consideration, which are low-bandwidth and high-bandwidth CPLs and is shown in Fig. 6.14(a). According to the STFT based protection logic as per (6.16), the magnitude of STFT at f_u= 625 Hz is shown in Fig. 6.14(a) which is for the loads described in Fig. 6.14(b). Due to higher inductance of the propulsion system, the rate of rise of current is slower which

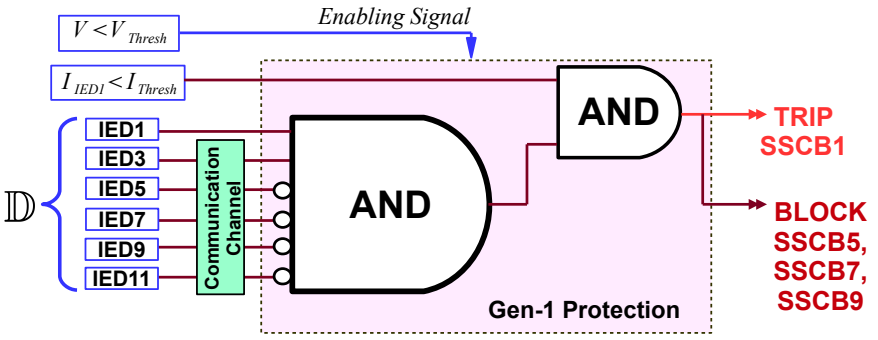
as a result does not significantly alter the magnitude at 625 Hz. On the contrary, the pulsed load resembles a sequential step change operation as described in Section 5.5.3 (of Chapter 5) results in increased magnitude at 625 Hz for every transition of dc current, which is shown in Fig. 6.14(b). According to (6.18), the fault detection logic for such system would be given by the following:

$$\text{IED}_{Fault-CPL} \implies \mathbb{D} = 1 \;\; \&\& \;\; |\mathcal{S}_{\mathcal{D}}|_{f_u} \; > \; \sigma_{CPL} \text{ dB}\,. \tag{6.20}$$

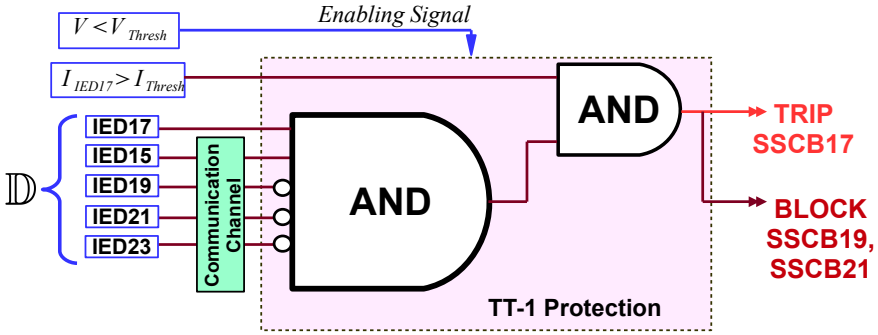
If $\sigma_{CPL} = 20\,\text{dB}$ (according Chapter 5), then for the propulsion loads, $|\mathcal{S}_{\mathcal{D}}|_{f_u}$ will be less than the σ_{CPL}, which do not indicate the fault conditions. However, for the pulsed load based CPLs, the $\sigma_{CPL} > 20\,\text{dB}$ as shown in Fig. 6.14(b). While designing the protection logic for such pulsed loads, the $\mathbb{D}$ is initially set to 0, and the δ would be set above the rated switching range so that the condition $\mathbb{D} = 1$ is not achieved during the normal pulsed load operations as per (6.20). This small change in the protection logic is required to provide selectivity between the high-bandwidth loading transients and the fault conditions.

6.7 Comparison of Current-Only Directional Protection With Existing Directional Protection Approaches

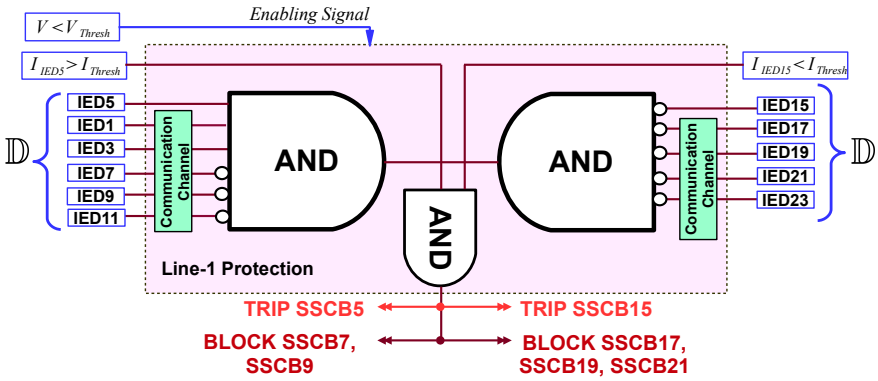
These existing approaches are mostly dependent on the communication among the IEDs. During the short-circuit faults, the IEDs are activated and exchange signals when the voltage falls below $V_{Threshold}$, i.e., when the UV condition is achieved. In the existing approaches $\mathbb{D}$ is modeled as per (6.1), which are then compared for all the IEDs. The fault location is confirmed when there is a contrasting difference of $\mathbb{D}$ between the successive IEDs. Tripping command to the respective fault isolating device (typically a SSCB) is executed when the $I_{Threshold}$ is exceeded. The operation of the existing methods is termed as Method-1 and is dependent on stringent OC and UV setpoints [186]. The logical diagram of the IEDs for protection of the generators, loads and lines using the existing methods is shown in Fig. 6.15. The modified version of existing method is termed as the traditional directional protection, which was described in Section 6.3 where the generator and load protection are independent of the communication infrastructure and the protection of lines and buses are carried out by the low-bandwidth communication infrastructure [17, 30]. However, the



6.15(a)



6.15(b)



6.15(c)

Fig. 6.15: Logical diagram of IED for protection of (a) Generator (fault F_1), (b) Load (fault F_2) and (c) Line (fault F_3) using the existing directional protection algorithm.

traditional directional protection is also dependent on the UV threshold and OC thresholds (for the protection of loads, lines and bus-bar). Thus, both methods require stringent OC and UV setpoints which might not operate for high-impedance faults and the thresholds are difficult to set for the dc SPS with varying system configuration and changing fault current

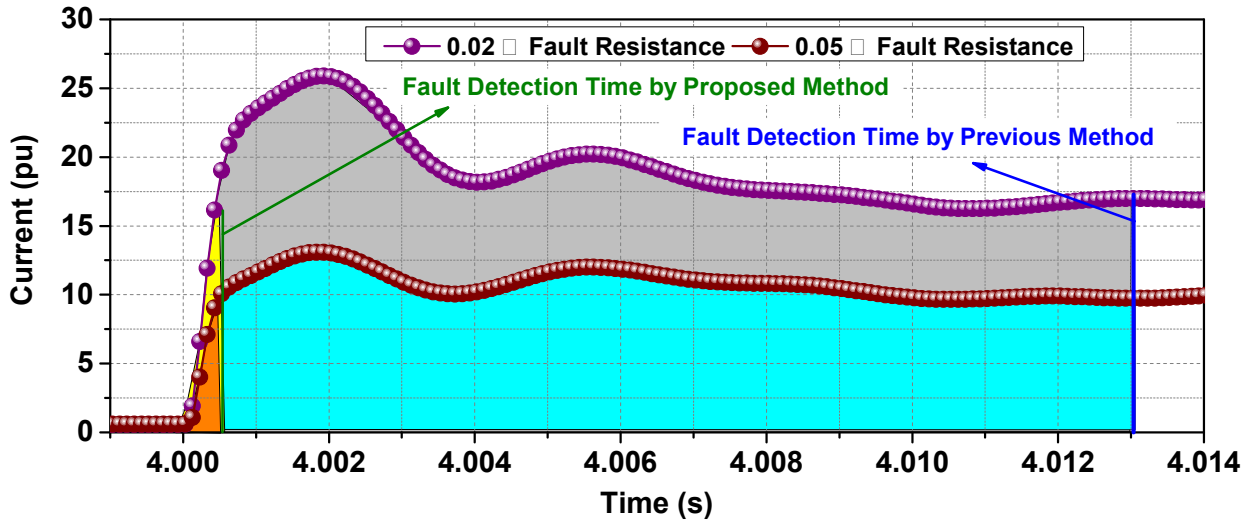


Fig. 6.16: Current of IED5 for 0.02 Ω and 0.05 Ω fault at F_3. Fault detection time by the existing and proposed dc protection methods are also highlighted.

levels, which has been described previously in Section 5.3.4.

The comparison of the Method-1, traditional directional protection and the proposed current-only directional protection is shown in Table 6.11 and Table 6.12. For comparison purpose, $I_{Threshold}$ value for Method-1 based directional protection is set at 2 pu while the $I_{Threshold}$ for traditional directional protection is consistent with Table 6.1. The fault resistances are varied from very low-impedance faults (0.001 Ω) to very high-impedance fault (100 Ω) and the operating times of the directional protection algorithms are compared. As the fault impedance rises, the $I_{Threshold}$ and $V_{Threshold}$ (for Method-1) are difficult to satisfy thus limiting its operation, which can be seen in Table 6.11 and Table 6.12 where Method-1 cannot work after 0.1 Ω fault impedance. Method-2 is able to detect the fault till $\mathbb{D}$ and $V_{Threshold}$ criteria are satisfied. It seems to work better than Method-1 but has limitations which has been described earlier in Fig. 6.6(b) and cannot work 0.2 Ω onwards. The advantage of the proposed current-only directional protection method is further illustrated in Fig. 6.16 where both protection algorithms are compared at IED5 for fault F_3 (Fig. 6.5) with fault impedances 0.02 Ω and 0.05 Ω. From the current measured at IED5 (Fig. 6.16), it can be seen that the proposed protection is much faster than the existing approaches. Thus the required energy to be dissipated by the fault isolation devices would be much less.

Table 6.11: Time Taken (ms) to Detect Fault Using Conventional and Proposed Fault Detection Methods

Fault Resistance	**Fault F1**			**Fault F2**		
	Method-1	Method-2	Proposed Method	Method-1	Method-2	Proposed Method
0.001 Ω	13.2	1.7	0.4	17.6	4.3	0.4
0.002 Ω	13.1	1.8	0.4	16.6	6.7	0.4
0.005 Ω	13.4	2.2	0.4	21.2	10.3	0.4
0.01 Ω	13.2	3.3	0.4	23.4	10.4	0.4
0.02 Ω	14.9	4.0	0.2	24.0	10.3	0.4
0.05 Ω	13.2	7.0	0.4	24.2	10.4	0.4
0.1 Ω	ND	16.3	0.4	ND	10.3	0.4
0.2 Ω	ND	ND	0.4	ND	ND	0.4
0.5 Ω	ND	ND	0.4	ND	ND	0.4
1 Ω	ND	ND	0.4	ND	ND	0.4
2 Ω	ND	ND	0.6	ND	ND	0.6
5 Ω	ND	ND	0.8	ND	ND	0.8
10 Ω	ND	ND	0.8	ND	ND	0.8
20 Ω	ND	ND	0.8	ND	ND	1.4
50 Ω	ND	ND	43	ND	ND	1.4
100 Ω	ND	ND	543	ND	ND	43

ND- No Detection, V_{thresh} = 0.8 pu; I_{thresh} (Method-1) = 2 pu.

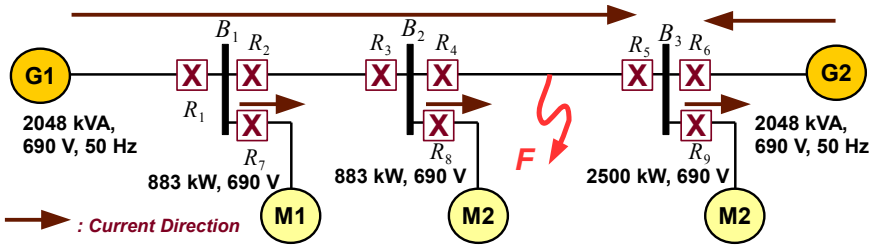
Table 6.12: Time Taken (ms) to Detect Fault Using Conventional and Proposed Fault Detection Methods

Fault Resistance	**Fault F3**			**Fault F4**		
	Method-1	Method-2	Proposed Method	Method-1	Method-2	Proposed Method
0.001 Ω	12.0	12.0	0.2	12.2	12.1	0.4
0.002 Ω	21.1	21.1	0.4	12.2	12.1	0.4
0.005 Ω	12.2	12.2	0.2	13.5	13.4	0.4
0.01 Ω	13.4	13.3	0.2	13.0	12.9	0.4
0.02 Ω	12.3	12.2	0.2	12.8	12.8	0.6
0.05 Ω	14.0	13.9	0.2	ND	13.5	0.4
0.1 Ω	ND	13.9	0.2	ND	12.9	0.6
0.2 Ω	ND	ND	0.4	ND	ND	0.6
0.5 Ω	ND	ND	0.4	ND	ND	0.8
1 Ω	ND	ND	0.6	ND	ND	1.0
2 Ω	ND	ND	0.6	ND	ND	1.2
5 Ω	ND	ND	0.8	ND	ND	1.0
10 Ω	ND	ND	1.0	ND	ND	1.0
20 Ω	ND	ND	1.4	ND	ND	31
50 Ω	ND	ND	393	ND	ND	ND
100 Ω	ND	ND	413	ND	ND	ND

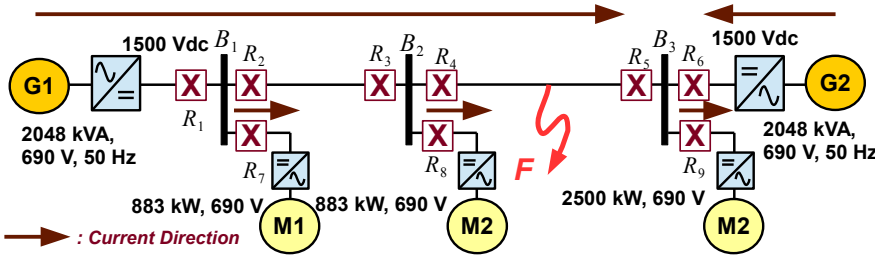
ND- No Detection, V_{thresh} = 0.8 pu; I_{thresh} (Method-1) = 2 pu.

6.8 Comparison of Current-Only Directional Protection in DC and AC Power Systems

The emerging power system architecture is expected to be comprised of hybrid ac/dc clusters taking advantages of both ac and dc power systems. For the protection solutions, current-



6.17(a)



6.17(b)

Fig. 6.17: SLD of (a) representative ac system and (b) representative dc system with radial distribution system.

only directional protection can be used as it is a popular choice in the ac systems and is effective for the dc power systems as discussed in this chapter. Due to differences in the transient responses between the ac and dc power systems, application of the directional protection would be significantly different. This section briefly compares the current-only directional protection in ac and dc power systems which could be useful for the hybrid ac/dc power networks. It is seen that the current-only directional protection developed for the dc SPS described in this chapter can also be used for the fault detection in other dc grid applications.

This one-to-one comparison of the directional protection in ac and dc power system is done by using the ac and dc power systems bearing similar topology as shown in Fig. 6.17(a) and Fig. 6.17(b) respectively. In both Fig. 6.17(a) and Fig. 6.17(b), 'G' denotes the generator while 'M' denotes the motor. 'R' comprises of the IED and the circuit breaker. The IED detects the abnormal condition and gives tripping signal to the circuit breaker.

Table 6.13: Relay Directions for Low-Impedance Fault 'F' in Fig. 6.17(b)

Case	R1	R2	R3	R4	R5	R6
Pre-Fault Current	1	1	1	1	1	0
Fault Current	1	1	1	1	0	0

6.8.1 Current-Only Directional Protection in DC System

Determining Direction ($\mathbb{D}_{dc}$)

Direction of current in dc system i.e. $\mathbb{D}_{dc}$ can be computed as per (6.13) which is used to identify the faulty segment. For instance, $\mathbb{D}_{dc}$ for pre-fault and fault F in Fig. 6.17(b), gives the current direction in various R's as shown in Table 6.13. It is seen that during the fault, the current through R_5 changes indicating a transient condition.

Fault Detection

$\mathbb{D}_{dc}$ only determines the change in current direction, which apart from a faulty condition, might also change during sudden load change, regenerative operation, change in system configuration etc. Thus, to confirm the fault condition, time-domain based OC protection or STFT based protection could be integrated with $\mathbb{D}_{dc}$.

a. $\mathbb{D}_{dc}$ + OC Based Fault Detection

To illustrate this $\mathbb{D}_{dc}$ + OC based dc directional protection, fault F is initiated in Fig. 6.17(b). The peak fault current and $\mathbb{D}$ as per (6.13) is shown in Table 6.14. For low-impedance faults, the high-magnitude peak current is dominated by the dc-link capacitive discharge. Moreover, the current through R_5 reverses, which can be seen by the negative peak current during such conditions. However, for high impedance faults, the magnitude of peak current reduces. The current through R_5 stops reversing for high-impedance faults as inferred from Case 12 onwards. However, with the proposed directional element, the directional change can be detected until case-14 which is for very high-impedance fault. The OC based protection depends on the fixed operating set-points. The peak current for high impedance faults has lower magnitude, hence this protection may not operate for high-impedance faults. This is a major limitation of the $\mathbb{D}_{dc}$+ OC based dc directional protection.

Table 6.14: Peak Fault Current and $\mathbb{D}_{dc}$ in R_4 and R_5 for a Range of Fault Impedances at 'F' in Fig. 6.17(b)

Case	**Fault Resistance**(Ω)	**Current Through** R_4 (i_{R_4})		**Current Through** R_5 (i_{R_5})	
		i_{peak} (kA)	$\mathbb{D}_{dc}$	i_{peak} (kA)	$\mathbb{D}_{dc}$
1	0.001	18.30	1	-20.74	0
2	0.002	17.75	1	-20.14	0
3	0.005	16.31	1	-18.48	0
4	0.01	14.38	1	-16.27	0
5	0.02	11.61	1	-13.09	0
6	0.05	7.35	1	-8.15	0
7	0.1	4.55	1	-4.89	0
8	0.2	2.71	1	-2.61	0
9	0.5	1.47	1	-0.95	0
10	1	0.88	1	-0.35	0
11	2	0.58	1	-0.04	0
12	5	0.40	1	0.14	0
13	10	0.33	1	0.21	0
14	20	0.30	1	0.24	0
15	50	0.28	1	0.26	1

Base current: 1300 A. $\delta = 20$ A.

b. $\mathbb{D}_{dc}$ + STFT Based Fault Detection

Rise time of the dc fault current is much faster than the rise time of the ac fault current due to lower inductance, and time constant of the system. Thus, the frequency-domain based approach could be used to compute the high-frequency components and hence confirming the fault condition. Operation of the STFT based dc directional protection for a range of fault impedances is shown in Table 6.15. It can be seen that the STFT algorithm can identify the high-frequency components for very high-impedance faults, which was difficult by using only OC relay[29–31, 182]. Thus the proposed $\mathbb{D}_{dc}$ + STFT based dc directional protection could be a preferred choice over the conventional $\mathbb{D}_{dc}$ + OC based dc directional protection.

6.8.2 Current-Only Directional Protection in AC System

Determining Direction $\mathbb{D}_{ac}$

Zero-crossing time (ZCT) based method has been popular to determine the direction of fault current in current-only directional protection in ac power systems [188]. This time-domain operation is depicted in Fig. 6.18. During normal operation (pre-fault current), the ZCT remains constant which is dependent on the system frequency. In this chapter, the

system frequency is chosen to be 50 Hz which makes the ZCT to be 10 ms. However, during the faults, the ZCT will change depending on the fault location in the forward or reverse direction. It is observed that the ZCT increases for the forward faults, while it reduces under reverse fault conditions which is shown in Fig. 6.18.

Fault Detection

To implement the current-only directional protection for ac systems, ZCT based directional element $\mathbb{D}_{ac}$ is combined with OC based fault detection algorithm [73, 177]. For selective fault identification in distribution systems, definite-mean time based time-current coordination in the OC relays is implemented. To study this current-only directional protection, a range of fault impedances are initiated at point F of Fig. 6.17(a) and the peak rms fault current and maximum ZCT through R_4 and R_5 are indicated in Table 6.16. For fault F, R_4 will detect the forward fault while R_5 will detect the reverse fault condition. Thus, the ZCT width for R_4 will be larger than 10 ms while ZCT width for R_5 will be less than 10 ms. This can be seen in Table 6.16 for low-impedance faults from Case 1 to Case 8. For medium- to high-impedance faults, the ZCT for R_4 and R_5 is closer to 10 ms thus becoming difficult to

Table 6.15: Decision Time of STFT Algorithm at R_4 and R_5 for a Range of Fault Impedances at 'F' in Fig. 6.17(b)

Case	**Fault Resistance** (Ω)	**Current Through** R_4 (i_{R_4})		**Current Through** R_5 (i_{R_5})	
		$\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}$ (dB)	$t_{\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}}$ (ms)	$\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}$ (dB)	$t_{\lvert\mathcal{S}_{\mathcal{D}}\rvert_{f_u}}$ (ms)
1	0.001	28.8605	0.20	30.8125	0.20
2	0.002	28.8462	0.20	30.7981	0.20
3	0.005	28.8035	0.20	30.7552	0.20
4	0.01	28.7326	0.20	30.684	0.20
5	0.02	28.5918	0.20	30.5427	0.20
6	0.05	28.1779	0.20	30.127	0.20
7	0.1	27.5149	0.20	29.461	0.20
8	0.2	26.2807	0.20	28.2212	0.20
9	0.5	23.1728	0.20	25.0951	0.20
10	1	30.7181	0.40	21.2195	0.20
11	2	25.3774	0.40	27.3136	0.40
12	5	24.5924	0.80	26.4906	0.80
13	10	23.3233	1.00	20.4584	0.80
14	20	20.5049	1.20	22.0975	1.20
15	50	15.5	–	16.4	–

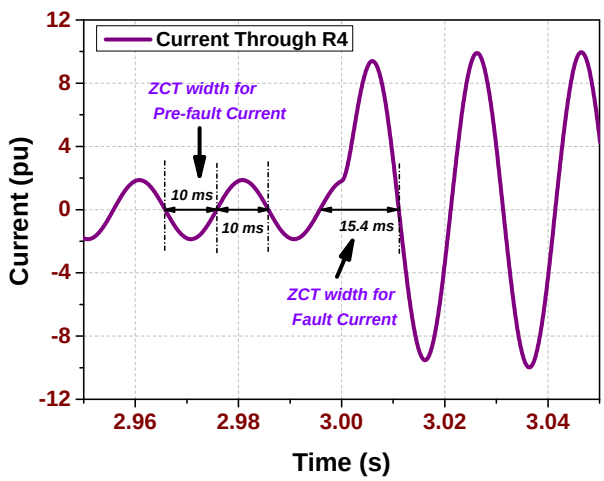
$\sigma = 20$ dB, $f_u = 625$ Hz.

Table 6.16: ZCT and Peak Fault Current Flowing Through R4 and R5 for a Range of Fault Impedances at 'F' in Fig. 6.17(a)

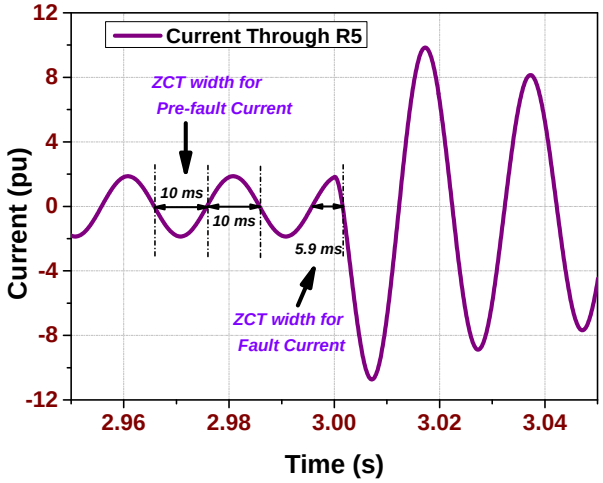
Case	**Fault Resistance**(Ω)	R_4		R_5	
		ZCT_{R_4} (ms)	$i_{R_{4-rms}}$ (pu)	ZCT_{R_5} (ms)	$i_{R_{5-rms}}$ (pu)
1	0.001	18.1	13.73	5.7	15.61
2	0.002	17.5	12.48	5.7	14.11
3	0.005	16.4	9.63	5.8	10.70
4	0.01	15.4	7.09	5.9	7.37
5	0.02	14.3	4.70	6.1	4.43
6	0.05	12.9	2.56	6.8	2.15
7	0.1	11.9	1.82	7.9	1.57
8	0.2	11.1	1.57	8.9	1.57
9	0.5	10.5	1.57	10	1.57
10	1	10.3	1.57	10	1.57
11	2	10.2	1.57	10	1.57
12	5	10.1	1.57	10	1.57
13	10	10	1.57	10	1.57
14	20	10	1.57	10	1.57
15	50	10	1.57	10	1.57

Base current: 1673 A, Normal current flow: 1.57 pu

detect the fault current direction. Moreover, the there is not so significant rise in the peak current of R_4 and R_5. Thus, the $\mathbb{D}_{ac}$ + OC based directional protection works satisfactorily for low-impedance faults and is unable to detect the fault conditions for high-impedance faults.



6.18(a)



6.18(b)

Fig. 6.18: ZCT for (a) fault in forward direction and (b) fault in reverse direction.

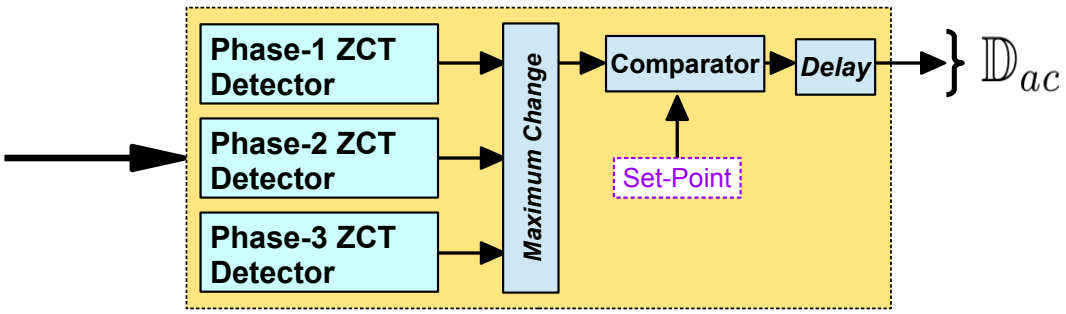


Fig. 6.19: Illustration of ZCT algorithm.

With regards to the above discussions, comparison of the various aspects of the directional protection in the ac and dc power systems is depicted in Table 6.17.

6.9 Summary

Directional protection is the combined operation of the directional element and the fault detection algorithm. The existing directional protection methodologies requires synergistic operation of the directional element, OC threshold and UV threshold, which requires relatively longer time and is restrictive for medium to high impedance faults. This chapter proposes proposes two directional protection techniques. The first one is termed as the '*traditional directional protection*' and is mostly based on $\mathbb{D}$ and UV while the second one is the current-only directional protection which uses DZI and STFT based fault detection algorithm which is based only with the current inputs. This chapter also discusses and compares the proposed methods with the variants of directional protection available in the existing literature along with their advantages and limitations. The results of this chapter can be summarized as follows:

(i) The traditional directional protection is based on the $\mathbb{D}$ and UV, which becomes restrictive for the high-impedance faults. Further, the backup protection will require strict thresholds which will not be feasible for the shipboard applications.

(ii) DZI based directional element has been proposed in this chapter, which is modeled by dividing the dc PSV into several zones. Its efficacy is supported by the comparative studies with the existing $\mathbb{D}$.

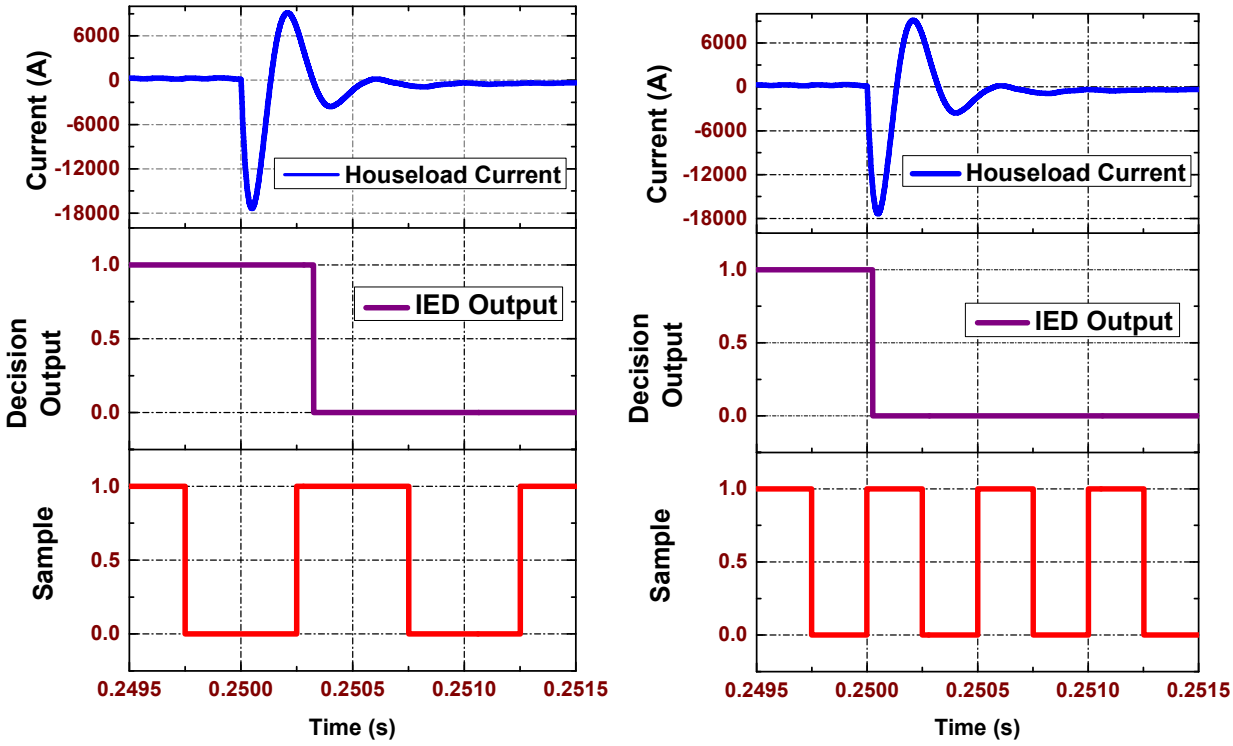
Table 6.17: AC Directional Protection v/s DC Directional Protection

Comparison Metrics	**AC Directional Protection**	**DC Directional Protection**
Protection Philosophy	Directional Element + OC Relay [73, 177]	(i) Directional element + OC tripping [6, 29, 30]. (ii) Directional element + STFT tripping.*
Modeling Directional Element	(i) Voltage polarising techniques [73]. (ii) Current-only methods. (a) ZCT based time-domain methods [188]. (b) Phase estimation based frequency-domain methods [189].	(i) Sign of the fault current [6, 28, 186]. (ii) Comparison with pre-fault current.*
Polarising element for current-only protection	(i) Polarising with pre-fault current [188]. (ii) Polarising with post-fault current [190].	(i) Polarising with pre-fault current.*
Fault Tripping Criteria	(i) Fixed time and OC settings [177]. (ii) Time-current characteristics [73].	(i) Comparison with the sign of the pre-fault current [30, 186]. (ii) OC protection. (iii) Detection of high frequency components [29, 30, 87].
Tripping Setpoint Optimisation	Required if OC is used with variable system configuration [6].	(i) Required if OC is used with variable system configuration [6]. (ii) Not required if frequency-domain based protection such as STFT is used.*

∗: Proposed in this thesis.

(iii) The current-only directional protection is based on the operation of the DZI based fault localization and STFT based fault detection. Fault condition is confirmed when both DZI and STFT are activated. This method can detect the fault condition with the impedance of very high values.

(iv) For both traditional and current-only directional protection, fault identification for the generators and loads are done independently while the protection of lines and buses would require low-bandwidth communication. The IEDs (along with SSCBs) and the communication requirements to realise this protection systems have also been



6.20(a) 6.20(b)

Fig. 6.20: Dependence of fault identification on sampling frequency. It is seen that the IED takes longer time to respond for (a) lower sampling frequency than (b) higher sampling frequency.

discussed.

(v) The rate of change of fault current is dependent on the nature of the fault circuit (underdamped or damped) and the resonant frequency. It is thus possible that circuits with very different time constants may appear within the same system. In such scenarios, the sampling time will be crucial parameter to identify the transient conditions. For instance, Fig. 6.20 shows the underdamped current from the dc-link discharge of the houseloads to which directional protection is applied. It is seen that if the sampling frequency is less then the IED may take longer time to operate.

(vi) DC-link is the key element for the directional protection as it indicates the probable fault location known by the direction of its discharge. In case of the resistive load this direction cannot be determined as it is not connected across dc-link capacitor. Thus, the protection logic should be modified accordingly.

(vii) It is seen that the $\mathbb{D}_{ac} + OC$ based directional protection in time-domain is suitable for low-impedance faults in ac systems. For high-impedance faults, the $\mathbb{D}_{ac}$ is unable to detect the current direction. For dc systems, a new directional element $\mathbb{D}$ termed as DZI along with STFT based fault identification are proposed. This $\mathbb{D}$ + STFT based dc directional protection is further compared with the $\mathbb{D}$+OC based dc directional protection. As compared to $\mathbb{D}_{dc} + OC$, $\mathbb{D}_{dc}$ + STFT based dc directional protection is able to identify the high-impedance faults due to rapidly rising fault currents.

(viii) This chapter has also presented a comparative analysis of dc and ac directional protection. In ac systems, time- or frequency-domain based $\mathbb{D}_{ac}$ and time-domain based fault detection (OC relay) constitute the directional protection. However, for dc systems, time-domain based $\mathbb{D}_{dc}$ (based on magnitude) and frequency-domain based fault detection (STFT) are more preferable. This is the major difference between directional protection in ac and dc systems.

(ix) The proposed protection method has not been tested in hardware-in-the-loop based system due to unavailability of the industrial hardware. The dSPACE based controller was available, however its performance was not suitable to verify the protection logics. Thus, the complete dc PSV was simulated with all the controllers inline in the real-time simulation platform and the fault conditions were simulated. The fault currents were analyzed offline in MATLAB. With the availability of commercial controllers such as NI-CRiO, B&R automation etc., the proposed protection would be verified in future.

Chapter 7

Conclusion and Recommendations

7.1 Conclusion

This thesis presents a wide range of contributions towards the short-circuit fault management strategies of dc SPS. PSV was taken as the target marine vessel owing to its complex operational profile and widespread demand in the marine industry. Unlike the ac power system, there are limited number of available standards for the dc power systems when applied to the marine vessels. The dc SPS is different from land-based dc systems, as a result the requirements of the protection system would be dependent on various shipboard operating factors such as system configurations, marine missions and load conditions. Thus, the modeling, control and operation of the dc SPS is also discussed in this thesis. The findings of this work have been published in the international conference proceedings and journal publications. Based on this, conclusions of the thesis can be summarised as follows:

(i) Chapter 1 and Chapter 2 attempt to discuss the objective of the thesis and a detailed literature review. Suitability of the existing dc fault management strategies for dc SPS are investigated in detail. Comparative analysis of the existing methods have also been included.

(ii) Operation of the dc SPS is different from the land-based dc power systems such as dc microgrids and HVDC transmission system. Thus, before devising the required short-circuit fault management techniques, detailed modeling of the dc SPS is important to study its various operating modes and requirements. This has been included in Chapter 3 and Chapter 4.

(iii) A novel AFR based dc generation system has been proposed in Chapter 3, which is supported by detailed mathematical analysis. It is found to be advantageous than the traditional AVR based dc generation system as it does not require expensive voltage sensors. As compared to the AVR based dc generation, the AFR based dc generation system operates smoothly during the variable speed operation. One-to-one comparison between the AVR and AFR based dc generation system is also done which supports the suitability of AFR over AVR for SPS. Apart from the dc SPS, this AFR based generation can be implemented in the more-electric aircraft and dc microgrids which employ variable frequency generation systems.

(iv) Modeling, control of the components of dc PSV and various marine operation modes are discussed in Chapter 4. A method to minimize specific fuel consumption (SFOC) of the variable frequency DGs have been discussed. Fuel savings of 19% has been reported with such operation.

(v) After modeling of the dc SPS, fault study would be the next step to understand the transient responses. Due to rapid discharge of dc-link capacitors during the short-circuit, fault response in dc system is significantly different from the ac counterpart. In ac systems, steady-state fault currents are used for protective relaying. However, for dc systems, transient discharge current is used for fault detection. Hence, a fault study is important before developing the fault detection techniques.

(vi) Similar to the protection of ac power systems, protection algorithms developed for the dc SPS should have selective operation as well. Although the ac protection algorithms cannot be directly applied to the dc SPS due to different fault current responses and timing requirements, some of the basic time-domain based ac protection systems such as directional and differential protection could be implemented in dc SPS. Differential protection requires time-stamped current signals for their operation, thus requiring high-bandwidth communication infrastructure. The directional protection requires fixed overcurrent settings for its reliable operation. As the network configuration is constantly changing to satisfy the marine missions, overcurrent settings will be different for every operation. In such conditions, frequency-domain based methods can be used to identify the transient conditions by detecting the presence of high-frequency components [29]. These analysis are covered in Chapter 5.

(vii) A novel current-only directional protection is proposed in Chapter 6. A time-domain based zonal interlocking is used to identify the fault localization and has STFT based algorithm to confirm the fault condition. This method can successfully detect the very high-impedance faults at the generator terminals, loads, lines and bus-bars. In ac systems, the directional element and fault detection algorithm are based in time-domain while in the proposed method, the directional element is based on time-domain while the fault detection is based on the frequency-domain. This is the major difference.

(viii) The proposed current-only directional protection is suitable for the compact dc power systems with varying loading conditions such as marine vessels where the fault currents widely vary with changing system configurations. However, this method can also be employed to the systems with fixed system configurations and loading conditions such as more-electric aircraft and dc microgrids.

7.2 Recommendations for Further Research

This thesis explores various aspects short-circuit protection strategies focussed on the dc SPS. While it has addressed the important fundamental problems, it has also generated some future research proposals which is expected to be interesting and essential.

(i) There is a need of communication protocols for the monitoring of the IEDs and also for protection purpose. In ac systems, there have been significant advances in the communication and automation infrastructure as shown in Fig. 7.1 [67]. However, there are no available protocols and standardised communication interfaces for the application in the dc SPS [64]. Thus, the future research could be focused on the cross-disciplinary research and development of these communication protocols with enhanced interoperability.

(ii) The fault isolating devices pose another biggest challenge in implementing fault management systems in dc SPS. The modified ACCB with additional resonating branch takes longer time to operate whereas the SSCB has more conduction losses. As a result, the hybrid circuit breaker could be a feasible option. However, these DCCBs are conceived to be bigger in size with significant cooling arrangements. Since the dc

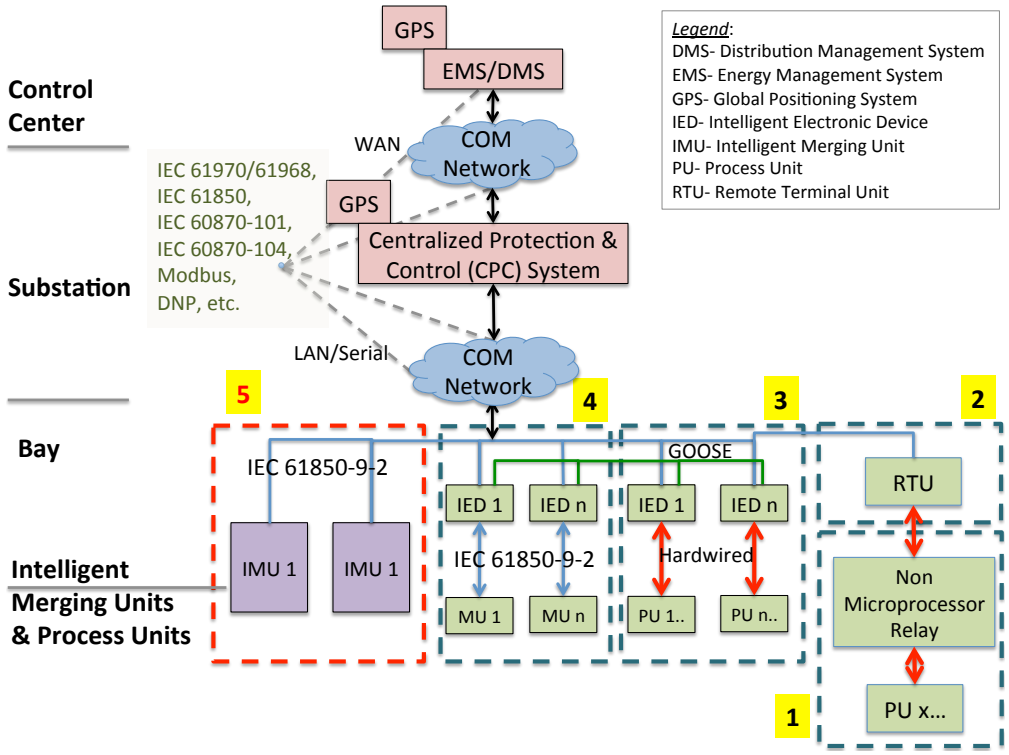


Fig. 7.1: Centralised protection architecture in ac power systems.

SPS has space and weight limitations, breaker-less topologies might be preferred. In recent years, battery operated dc ferries have emerged. Such class of dc SPS could be integrated with the fault tolerant topologies to integrate the battery. The additional advantages of being able to restrict the fault current becomes another reason to adopt the breaker-less topology. The future fault isolating devices could be a combination of the circuit-breakers and the breaker-less topology.

(iii) The dc power system for marine vessel is primarily selected for its fuel-efficient operation. However, in recent years the dynamic ac technology has been proposed by ABB resulting in fuel efficient operation [191]. Although the fuel efficiency of dc SPS is far better than the dynamic ac technology, the investment on the dynamic ac technology is much less than the dc SPS. It is expected that the future power systems would comprise of the hybrid ac/dc power sytems. Thus, future research could be aligned to select the fuel efficient topologies for the dc SPS. Real-time testing of such architectures along with the operation of the fault management strategies would be required

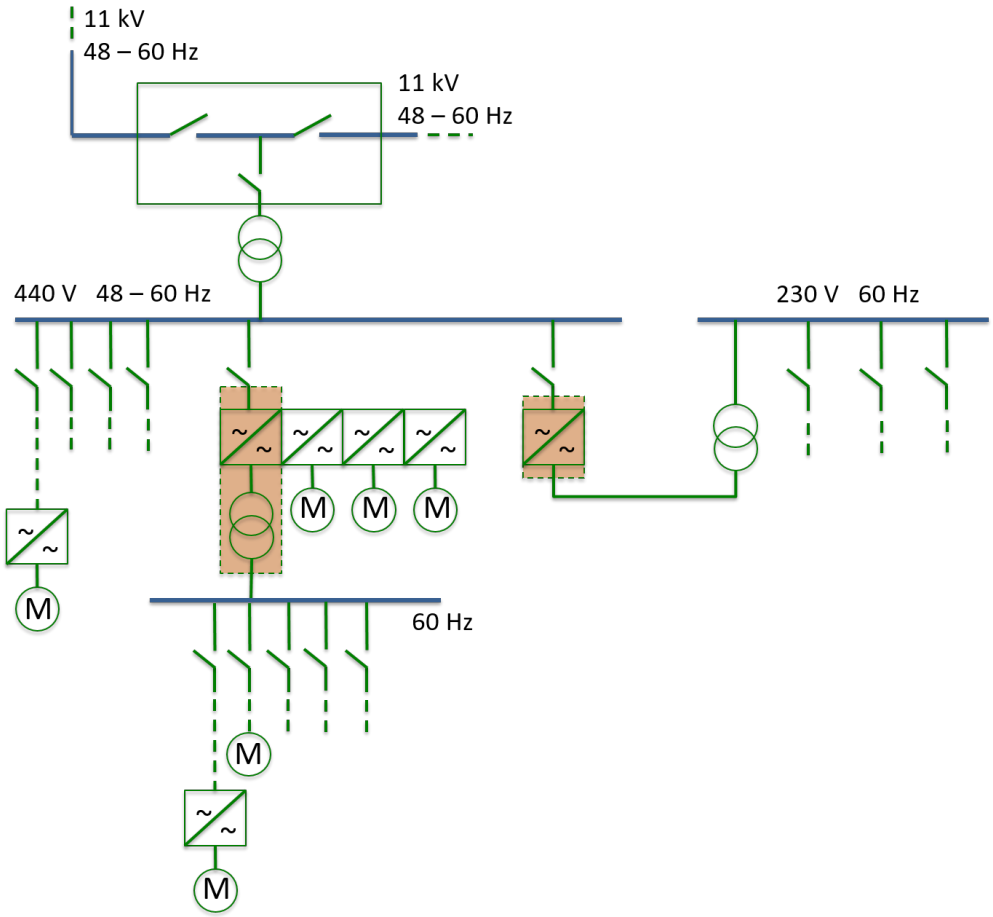


Fig. 7.2: Dynamic ac topology proposed by ABB.

to develop the comprehensive fault management strategies.

Author's Publications

- **ACCEPTED/PUBLISHED :**
  - **As First Author**
    - ***Refereed Journal Publications:***

J5. **K. Satpathi**, A. Ukil, S. S. Nag, J. Pou and M. A. Zagrodnik, "DC marine power system: Transient behaviour and fault management aspects," *IEEE Trans. Ind. Informat.*, vol. 15, no. 4, pp. 1911-1925, Apr. 2019.

J4. **K. Satpathi**, A. Ukil, J. Pou and M. A. Zagrodnik, "Design, analysis and comparison of automatic flux regulator with automatic voltage regulator based generation system for DC marine vessels," *IEEE Trans. Transport. Electrific.* vol. 4, no. 3, pp. 694-706, Sept. 2018.

J3. **K. Satpathi**, Y.M. Yeap, A. Ukil, and N. Geddada, "Short-time Fourier transform based transient analysis of VSC interfaced point-to-point DC system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 4080-4091, May 2018.

J2. **K. Satpathi**, A. Ukil, and J. Pou, "Short-circuit protection in DC electric ship propulsion system: Review of existing technologies and future research trends," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 272-291, Mar. 2018.

J1. **K. Satpathi**, V. M. Balijepalli, and A. Ukil, "Modeling and real-time scheduling of DC platform supply vessel for fuel efficient operation," *IEEE Trans. Transport. Electrific.*, vol. 3, no. 3, pp. 762-778, Sep. 2017.

∗ ***Refereed Conference Publications:***

C6. **K. Satpathi**, A. Ukil, S. S. Nag, and J. Pou, "Comparison of current-only directional protection in AC and DC power systems," in *Proc. Innovative Smart Grid Technologies (ISGT)*, Singapore, 2018.

C5. **K. Satpathi**, A. Ukil, N. Thukral and M. A. Zagrodnik, "Modeling of DC shipboard power system," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

C4. **K. Satpathi** and A. Ukil, "Protection of MVDC shipboard power system using Rogowski coil," in *Proc. IEEE Int. Conf. on Power Electronics, Drives and Energy Systems (PEDES)*, Trivandrum, India, Dec. 2016.

C3. **K. Satpathi**, N. Thukral, A. Ukil and M. A. Zagrodnik, "Flux estimation based DC bus voltage control in marine DC power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016. [Best Session Presentation]

C2. **K. Satpathi**, N. Thukral, A. Ukil and M. A. Zagrodnik, "Directional protection scheme for MVDC shipboard power system," in *Proc. Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Florence, Italy, Oct. 2016.

C1. **K. Satpathi** and A. Ukil, "Protection strategies for LVDC distribution system," in *Proc. IEEE PowerTech Conf.*, Eindhoven, Netherlands, Jun. 2015.

– **As Co-Author**

– ***Refereed Journal Publications:***

J2. A. Ukil, Y.M. Yeap, K. Satpathi, "Power systems frequency estimation using amplitude tracking square wave for low-end protective relays," *Measurement*, 2019. (*In press*)

J1. Y. M. Yeap, N. Geddada, **K. Satpathi**, and A. Ukil, "Time and frequency domain fault detection in VSC interfaced experimental DC test system," *IEEE Trans. Ind. Informat.*, vol. 14, no. 10, pp. 4353-4364,

Oct. 2018.

∗ ***Refereed Conference Publications:***

C4. A. Ukil, Y. M. Yeap, and **K. Satpathi**, "Low-complex frequency estimation method using amplitude tracking square wave," in *Int. Conf. Electronics, Information, Communication (ICEIC)*, Auckland, New Zealand, Jan. 2019.

C3. A. Ukil, Y. M. Yeap, **K. Satpathi** and N. Geddada, "Fault identification in AC and DC systems Using STFT analysis of high frequency components," in *Proc. Innovative Smart Grid Technologies (ISGT)*, Auckland, New Zealand, 2017.

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C1. D. Francis, Q. Zhengting, **K. Satpathi**, N. Thukral and A. Ukil, "Suitability of rogowski coil for DC shipboard protection," in *Proc. IEEE TENCON Conf.*, Singapore, Nov. 2016.

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Appendix A

Pseudo Code for STFT Based DC Fault Detection

The prime-identification for the fault condition is the non-zero magnitude at the update-frequency bins for the given window size. Due to the presence of ripples in the output DC current, the magnitude at the first update-frequency could be positive. Hence, relying on the magnitude of the first update-frequency bin would not be a robust solution. Instead, the fact that magnitudes of first few update-frequencies increases beyond a certain set-point, may be used for fault detection algorithm. From the results, the set-point for simulation system can be set at 20 dB. Algorithm 2 depicts a generic pseudo-code for STFT based fault detection. The algorithm uses FFT with slight modification for fault detection which could be easily implemented in embedded hardware system proving its practicability in real system.

Algorithm 2 Pseudo-code of STFT Based DC Fault Detection

1: – Read input current signals ($\mathtt{x_{cur}}$) and sample at sampling frequency of $\mathtt{f_s}$.
2: – Define operating parameters of STFT such as window size (`n`), window type (`w[n]`), number of FFT points (`N`), hopping size (`H`).
3: –Frequency resolution: $\mathtt{f_s/N}$; Time resolution: $\mathtt{H/f_s}$
4: –Define tripping set-point $\mathtt{X_{trip}}$.
5: **while** ((`H` + `n`) $<$ total input samples of $\mathtt{x_{sig}}$) **do**
6: – `x = x_cur[1:n].*w[n]` ▷ Windowing the signal.
7: – `X = FFT(x,N)` ▷ FFT on windowed signal.
8: – Store `X`.
9: – Calculate Magnitude ($|X|$ dB.)
10: **for** `f=1:fs/N:fs/2` **do**
11: Plot `f` vs `|X|`
12: **if** `|X|>` $\mathtt{X_{trip}}$ `dB` at `m.fs/n` **then**
▷ first three update-frequencies i.e. `m=2` & `3` & `4` for improved reliability.
13: –Fault in the System
14: –Trip the CB/Fault Isolating Device.
15: **else**
16: –No Fault in the System.
17: –Go Back to Step 10.
18: **end if**
19: **end for**
20: – `x = x_cur[1+H:n+H]`
21: – Go to Step 5.
22: **end while**
23: Print Results.

Appendix B

Algorithms for Directional Protection

1. Generalised Directional Protection

Algorithm 3 Generalised Directional Protection

—Set $V_{Threshold}$ and $I_{Threshold}$.
—Read dc bus voltage and current at all IEDs.
if current at IED_{Load} <0 **then**
    BLOCK reverse current
end if
while dc bus voltage <$V_{threshold}$ **do**
    if current at IED_{Gen} <0 **then**
        TRIP IED_{Gen} ▷ Generator Protection
    end if
    if current at IED_{Load} >$I_{threshold}$ **then**
        TRIP IED_{Load} ▷ Load Protection
    end if
end while
while all Gen currents>0 && all Load currents<0 **do**
    if current at bus-bar ID <0 **then**
        TRIP IED_{Bus} && IED_{Gen} && IED_{Load} in upper section ▷ Bus-bar Section-1 Protection
    else
        TRIP IED_{Bus} && IED_{Gen} && IED_{Load} in lower section ▷ Bus-bar Section-2 Protection
    end if
end while
—Goto Step 2

2. Directional Protection Algorithm with Back-up

Algorithm 4 Directional Protection with Backup

—Set $V_{Threshold}$, $I_{Threshold,Gen}$, $I_{Threshold,Load}$ $I_{Threshold-Backup,Gen}$, $I_{Threshold-Backup,Bus}$, t_{holdup}.
—Read dc bus voltage and current at all IEDs.
if current at IED$_{Load}$ <0 **then**
    BLOCK reverse current
end if
while V_{bus} <$V_{threshold}$ **do**
    if $i_{\text{IED}\,1}$ <0 **then** ▷ F1 Detected
        TRIP IED 1 ▷ F1 Isolated
    end if
    if $i_{\text{IED}\,6}$ >I_{backup} **then**
        TRIP IED 6 ▷ F1 Back-up Bus-bar Trip
    end if
    wait $t = t_{holdup}$
    if $i_{\text{IED}\,3}$ == 0 && $V_{bus} < V_{Threshold}$ **then**
        TRIP IED 3 ▷ F1 Back-up Motor Trip
    end if
end while
while V_{bus} <$V_{threshold}$ **do**
    if $i_{\text{IED}\,4}$ >$I_{threshold}$ **then** ▷ F2 Detected
        Trip IED 4 ▷ F2 Isolated
    end if
    if $i_{\text{IED}\,6}$ >I_{backup} **then**
        TRIP $i_{\text{IED}\,6}$ ▷ F2 Back-up Bus-bar Trip
    end if
    if $i_{\text{IED}\,2}$>$I_{backup,gen}$ **then**
        TRIP IED 2 ▷ F2 Back-up Gen-2 Trip
    end if
    Wait $t = t_{holdup}$
    if $i_{\text{IED}\,5}$ == 0 **then**
        TRIP IED 5 ▷ F2 Back-up Load Trip
    end if
end while

33: **while** V_{bus} <$V_{threshold}$ **do**
34: **if** $i_{\text{IED}\,1}$ >0 && $i_{\text{IED}\,2}$ >0 && $i_{\text{IED}\,3}$ <0 && $i_{\text{IED}\,4}$ <0 && $i_{\text{IED}\,5}$ <0 **then**
35: **if** $i_{\text{IED}\,6}$ >0 **then** ▷ F3 Detected
36: TRIP IED 1, IED 3, IED 6 ▷ F3 isolated
37: **end if**
38: **if** $i_{\text{IED}\,1}$ >$I_{Threshold-backup,gen}$ **then**
39: TRIP IED 1 ▷ F3 Back-up Gen-1 Trip
40: **end if**
41: **if** $i_{\text{IED}\,2}$ >$I_{Threshold-backup,gen}$ **then**
42: TRIP IED 2 ▷ F3 Back-up Gen-2 Trip
43: **end if**
44: wait $t = t_{holdup}$
45: **if** $i_{\text{IED}\,3}$ == 0 **then**
46: TRIP IED 3 ▷ F3 Back-up Thruster-1 Trip
47: **end if**
48: **if** $i_{\text{IED}\,4}$ == 0 **then**
49: TRIP IED 4 ▷ F3 Back-up Thruster-2 Trip
50: **end if**
51: **if** $i_{\text{IED}\,5}$ == 0 **then**
52: TRIP IED 5 ▷ F3 Back-up HouseLoad Trip
53: **end if**
54: **end if**
55: **end while**
56: —Go to Step 2.