A 6bit 1.2GS/s Symmetric Successive Approximation Energy-Efficient Time-to-Digital Converter in 40nm CMOS

Qian Chen[1], Yuan Liang[1,2], Chirn Chye Boon[1*]
[1] Nanyang Technological University, Singapore 639798
[2] IHP, Innovations for High Performance Microelectronics, Germany 15236
[*]Contact author: eccboon@ntu.edu.sg

***Abstract*—This work presents a 6bit 1.2GS/s symmetric successive approximation (SSA) energy-efficient time-to-digital converter (TDC). The delay offset of the successive approximation (SA) TDC has been alleviated by employing the balanced architecture and optimizing the phase detector (PD). Size-optimized inverter chain is deployed as the delay unit with good linearity to increase the conversion rate and reduce the power consumption. In addition, dynamic logic is implemented to further improve the speed and energy efficiency. As a proof-of-concept design, the TDC is verified by post-layout simulation (Transient noise + Monte Carlo (MC)) in 40nm low power CMOS technology, achieving 0.98LSB /1.03LSB worst case differential nonlinearity (DNL)/integral nonlinearity (INL) and 0.014pJ/conversion-step figure-of-merit (FOM). The simulated single-shot precision (SSP) of the proposed TDC is 0.71 LSB.**

Keywords—ADC-based wireline, time-based ADC (TBADC), CMOS ADC, successive approximation (SA), symmetric successive approximation (SSA), energy-efficient, time-to-digital converter (TDC), dynamic logic

I. INTRODUCTION

The continuously scaling CMOS technology has facilitated the use of digital circuits in mixed-signal processing. However, the negative aspects resulted from CMOS miniaturization, such as, drop of intrinsic gain, lower supply voltage and worse threshold voltage variation, increase the difficulty of analog-to-digital conversion (ADC) design and impede the digitization progress for ultra-deep micron circuits. Recently, time-based ADC (TBADC) has gained more attention due to its digital-friendly features [1]. The signal in time domain is independent of the supply voltage (Fig. 1), thus TBADC is immune to the worse SNR resulting from the CMOS scaling which makes TBADC a promising low-power solution for data conversion. On the other hand, high-speed ADC-based wireline for the next generation optical communication has put the urgent need for the low-power high-speed ADC with small area and medium resolution. Fortunately, the TBADC featuring friendly digital-orientation exactly meets the power and speed requirements of the ADC-based wireline system [2]. In fact, several high-speed medium resolution TBADC have been reported these days. Ref. [2] proposed a 2GS/s 8-bit TBADC based on the remainder number system (RNS). It reduces the power consumption by reducing the comparator numbers. Ref. [3] reported a two-step 950MS/s 8-bit TBADC with 2.3mW power dissipation. It achieves excellent power efficiency by employing fully time signal processing. However, the energy efficiency of these TBADCs still needs to be further improved for the implementation in high-speed wireline system, especially when time-interleave (TI) architecture is employed.

Noticeably, time-to-digital converter (TDC) is the key building block of TBADC which translates the time interval into digital output code. Since most of the power consumption comes from the TDC block of TBADC, it's crucial to reduce the power consumption of the TDC in order to improve the energy efficiency of the whole system. However, designing a high-speed low-power TDC is non-trivial. It is widely known that the delay-line based flash architecture is welcomed to be implemented in the high-speed TDC. The regular structure of the flash TDC is shown in Fig. 2. The complexity of the flash architecture is exponentially dependent on the number of bits. A conventional *N*-bit delay-chain flash TDC requires 2*N*-1 delay elements and 2*N*-1 D-flip-flops (DFFs), leading to high power and area consumption even for low-to-medium resolution application. To reduce the number of delay units of the flash TDC, time amplifier (TA) based coarse–fine TDC has been proposed in [4], allowing lower power consumption compared with the basic flash TDC by amplifying the time residue and reducing the number of delay units and comparators. However, the TA-based TDC requires precise TA gain control and the conversion rate needs to be lowered (due to the TA latency). The benefits from the TA-based structure will be further reduced for low-to-medium resolution TDC. On the other hand, successive approximation (SA) architecture has been proposed in [5] in order to achieve medium-resolution low-power TDC. It halves the number of delay units through binary searched time comparison. Since the decision select blocks are deployed in the heading direction of the signal in [5], the loop of the conventional SA architecture is also un-rolled and the extra digital-to-time converter (DTC) and control logic have been eliminated, increasing the conversion rate and reducing the power consumption.

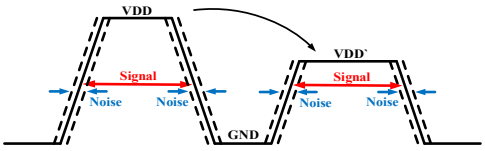

Fig. 1 Signal in time domain.

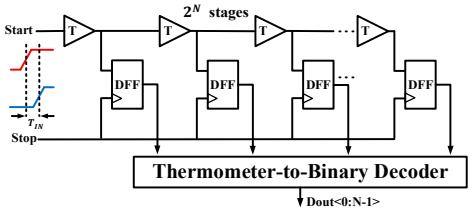

Fig. 2 Conventional delay-line based flash TDC.

Unfortunately, the structure of the SA TDC reported in [5] is asymmetric and it produces large offset between the

reference and input signal. Foreground calibration algorithm and corresponding circuits such as DTC and timing generator have been proposed and implemented on-chip while the calibration control logic is implemented off-chip. This calibration method increases the complexity of the TDC and sacrifices the energy efficiency of the whole system. In addition, the traditional unbalanced DFF is implemented as the phase detector (PD) which aggravates the intrinsic offset. The unbalanced PD also reduces the conversion rate because of its serious metastability issue.

To further explore the advantages of the SA architecture, we propose a novel symmetric SA (SSA) TDC targeting at 6bit resolution and gigahertz sampling for high-speed ADC-based wireline application. We implement size-optimized inverter chain as the delay unit to increase the speed and reduce the power consumption. The number of PD has been reduced to N-1 (N-bit) the same as [5], although the delay unit number needs to be increased to guarantee the balanced structure. Moreover, the dynamic logic has been utilized to further improve the conversion speed and energy efficiency. The post-layout simulation shows that the TDC achieves 1.2GS/s sample rate with only 0.52mW power consumption at typical corner implemented in 40nm low power CMOS technology.

The rest of this paper is organized as follows. Section II introduces the architecture and circuit blocks of the proposed TDC. Section III presents the post-layout simulation results and discusses the calibration implementation. Finally, the conclusion is drawn in Section IV.

II. Architecture and Circuits

The overall architecture of the proposed 6bit SSA TDC is shown in Fig. 3. Since differential structure is implemented, only 5 delay stages are needed to realize the 6bit resolution, while the last stage is made of one PD. The time difference of the input signals at stage n is detected by the PD and then the signals will be delayed by a fixed delay T_{PD} or $T_{FS}/2^n$ respectively depending on the decision result of the PD (T_{FS} is the full range of the TDC). If the signal in one path is ahead of the other one, it will be delayed by $T_{FS}/2^n$ while the other will be delayed by T_{PD} and vice versa. Hence, the TDC achieves digital quantization through successive approximation. The decision signal 0/1 made by the PD represents the bit number of the stage and a sample clock will be generated to synchronize the output code.

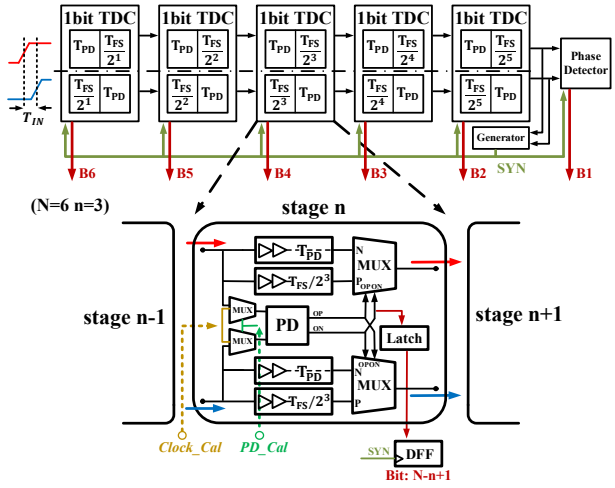

Fig. 3 Architecture of the proposed SSA TDC.

The diagram of the 1bit stage is shown below the architecture in Fig. 3. There exist two delay chains for each signal path with a 2:1 multiplexer (MUX) cascaded behind them. Ideally, T_{PD} is 0 which means no added delay. However, the decision signal of PD should be setup before the signal arrives at the input of the MUX, thus, extra reference delay should be added at both delay chains to cover the setup time (depends on the metastability of PD). It is different with the voltage-based SA structure since the timing information can't be stored or held. Then, a SR latch is implemented to sense the output of the PD and a DFF is utilized to synchronize the final digital codes.

The timing diagram of the input signals of each stage is shown in Fig. 4. The synchronized sample clock is also shown in the bottom of the figure. The time difference is shortened gradually which will be smaller than one delay unit time (one LSB) at the input of final stage (PD) (assuming the input time signal is close to full scale of the TDC). The synchronized sample clock is generated from the input of the last stage. It should be setup before the next rising edge of the input signal coming to the TDC. Therefore, the maximum frequency of the SA TDC can be derived with this limit.

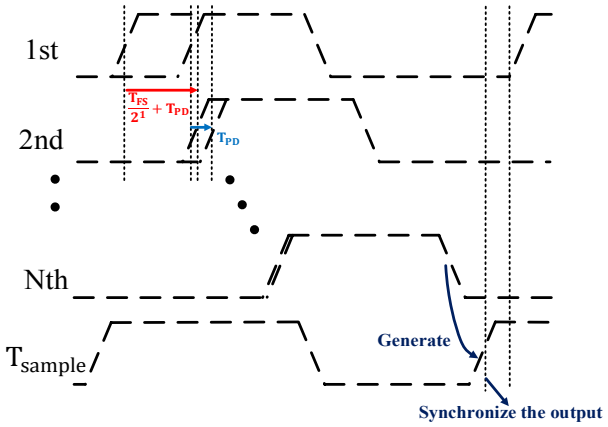

Fig. 4 Timing diagrams of the input signals of the 1bit TDCs.

Assume that the delay of the MUX is T_{mux}, the setup time of DFF is T_{DFF} and the time of delay unit is T_{UNIT}, the minimum time for the TDC to finish one comparison is shown as below:

$$T_{PERIOD} = \left(2^4 + 2^3 + 2^2 + 2^1 + 2^0\right) \times T_{UNIT} + 6 \times T_{PD} + 5 \times T_{MUX} + T_{DFF} \quad (1)$$

The maximum working frequency of the TDC is the reciprocal of T_{PERIOD}. We can improve the conversion speed of the TDC by reducing T_{PD}, T_{mux} and T_{UNIT}. Compared with the phase detector in [6], the SR latch is move outside the PD to reduce the T_{PD}. Dynamic logic circuits have been implemented to reduce the T_{MUX}. In addition, the corresponding pull-up/dull-down transistors of the delay unit are enlarged to reduce T_{UNIT}, since only one edge of the signal (rising or falling) is concerned (make sure the pulse change of the MSB delay chain is smaller enough than 50% duty cycle).

The circuit diagram of the PD is shown in Fig. 5 (a). It is a modified version of arbiter from [6] with the latch removed to reduce the metastability time. When both IP/IN return to 0, the output OP/ON of the PD will be reset to 0. Two additional charging paths composed of cascaded PMOS controlled by the input signals are added to reset both drain

nodes of the input transistors. It removes the offset induced by the charge stored at these nodes from the last comparison. The 2:1 dynamic MUX is shown in Fig. 5(c). 4 Cascaded PMOS pairs are deployed to reset the output nodes and the drain nodes of the input transistors, setting the proper initial state before the selection signal comes. The input transistor is located below the selection transistor to avoid the offset caused by the selection signal. Otherwise, part of the charge stored at the drain node of the selection transistor during reset period will flow to ground when the selection transistor turns on. Since the time interval between the input and selection signal is uncertain, the amount of the charge flowing to ground varies. It causes different initial status when the selected signal starts to output resulting in offset. Since no static current path exits for both PD and MUX, the power consumption of the TDC has been reduced a lot. Moreover, the dynamic logic helps to improve the conversion speed. The SR latch is shown in Fig. 5(d). The latch will reverse its status only when OP/ON from the PD changes its polarity which enables the sampling of the comparison result. The transistors in the delay unit (the n-MOS of the first inverter and the p-MOS of the second inverter) have been scaled up to reduce the unit time delay as shown in Fig. 5(b) (only rising edge is concerned). The post-layout simulation shows the time of one delay unit has been reduced from 10.7ps to 8.1ps in the 40nm low power CMOS.

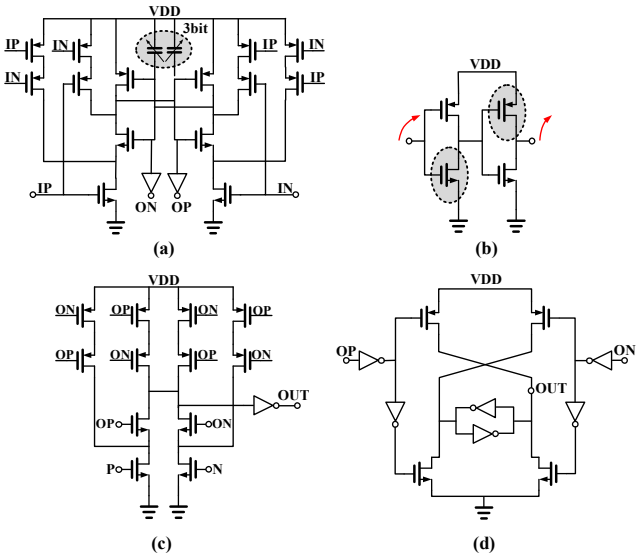

Fig. 5 Proposed circuit blocks (a) PD, (b) size-optimized delay unit, (c) dynamic MUX and (d) SR-latch.

Note that all the structures of the circuit blocks are perfect symmetrical which improves the linearity of the TDC. In addition, common-centroid layout techniques have been adopted to reduce the mismatches from layout and process. The layout of the PD core is shown in Fig. 6.

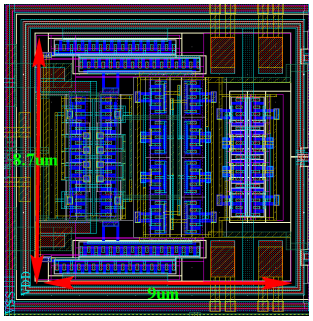

Fig. 6 The layout of the PD core.

III. Simulation Verification

A. Simulation Results

The static performance of the TDC has been verified by simulating the DNL/INL. A slow-ramp voltage signal is input to the ideal VTC (implemented by Verilog-A) to generate the input time signal of the TDC. Fig. 7(a) shows the DNL/INL at typical corner. It shows that the layout has little influence of the linearity of the TDC. To check the effects of process mismatch, Monte Carlo (MC) simulation has been employed and the results are shown in Fig. 7(b). The worst-case differential nonlinearity (DNL)/integral nonlinearity (INL) is 0.98 LSB/1.03LSB respectively.

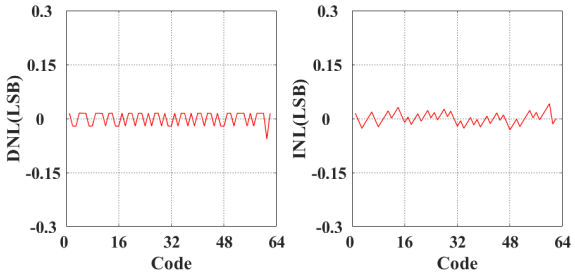

Fig. 7(a) DNL/INL at typical corner.

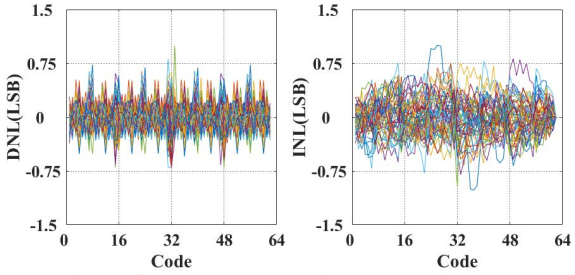

Fig. 7(b) DNL/INL from Monte Carlo (MC) simulation (100 runs).

Dynamic performance also has been verified with the ideal VTC. Fig. 8(a) shows SFDR/THD/ENOB results near Nyquist with clock frequency sweeps from 100k to 1.2G. Since the clock jitter and power noise will deteriorate the TDC performance, the transient noise simulation with jitter clock (~1ps edge-to-edge jitter) and noisy supply (~100mV peak-to-peak noise amplitude) has been implemented. The results are shown in Fig. 8(b). It shows that ENOB keeps stable and the TDC is immune to the effects of noise from different source.

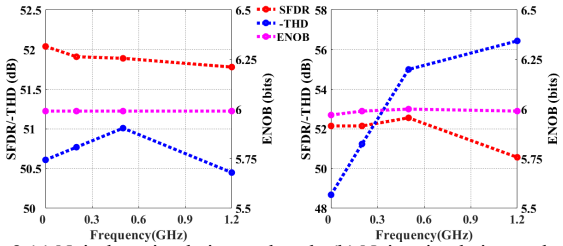

Fig. 8 (a) Noiseless simulation testbench. (b) Noisy simulation testbench.

A major performance metric for TDC is the single-shot precision (SSP) [7]. To simulate the SSP, we conduct transient noise simulation as described before (with MC: global variation + local variation) in order to emulate the real measurement environment more closely. The simulation results with different PVT condition are shown in Fig. 9. While the results with noiseless simulation environment are shown in Fig. 9 (a-c) for comparison. The input time difference is set to 1ps (code 31) for both noisy and

noiseless setups. It shows that the worst case SSP is 0.71 LSB at SS corner.

The TDC consumes 0.47mA average current from 1.1V power supply with 1.2GHz clock at typical corner. The simulation results are summarized in Table I and compared to several state-of-the-art high-speed TDC works.

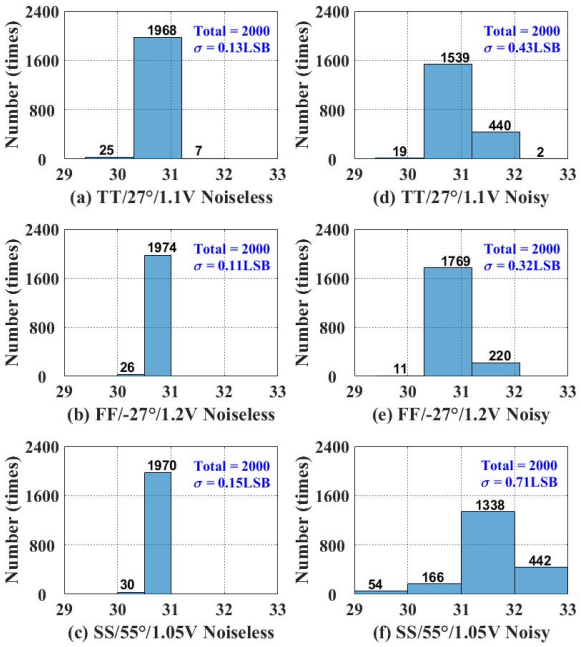

Fig. 9 Single-shot code histograms (MC simulation) (a-c) with noiseless simulation testbench (d-f) with noisy simulation testbench.

B. *Offset Calibration*

Since the LSB of the proposed 6bit TDC is about 8ps, it's large enough to cover the offset caused by layout and process mismatch which is verified by the simulation. However, alternative calibration scheme is still a necessity for practical measurement.

As shown in the 1bit TDC diagram of Fig. 4, two MUXs are added before each PD. When *PD_Cal* is enabled, the signal *Clock_Cal* will input to both IP/IN of the PD. 3bit digital controlled capacitor array are loaded to the PD as shown in Fig. 6(a). The PD offset can be calibrated by tuning the loaded capacitor then, the probability of one/zero of the PD's output is near 50% when calibration is finished. Note that external sample clock of DFF will be utilized for PD offset calibration.

The calibration of the delay offset is realized by adding extra tuneable delay units in MSB and MSB-1 stages, since only the offset from MSB stages matters (introduced by the long delay chain). Apply zero input (make sure all PD offset are calibrated) and tune the delay units until code "100000" and "011111" are almost 50% (other codes appeared should be reduced as much as possible).

The aforementioned offset calibration ideas are verified using behavioural model in MATLAB platform. Further research can be focused on the PVT-insensitive delay unit [8], fine delay unit and PD metastability issues in order to apply the proposed architecture to the high resolution TDC implementation.

IV. Conclusion

An energy-efficient 6bit 1.2GS/s symmetrical successive approximation (SSA) TDC has been reported in this paper. By employing a balanced architecture, the delay offset of the SA TDC has been alleviated leading to better linearity performance. Size-optimized inverter chain and dynamic logic circuits have been implemented to improve the sample rate and reduce power consumption. The proposed TDC achieves an excellent 0.014pJ/conversion-step figure-of-merit (FOM) based on the post-layout simulation, providing an effective time quantization solution for low-power high-speed TBADC with low-to-medium resolution applying to ADC-based wireline.

TABLE I. Performance Comparison of High-Speed TDC.

	JSSC 2012[5]	JSSC 2014[9]	ISSCC 2015[10]	JSSC 2018[7]	[a]This work
Tech. (nm)	CMOS 65	CMOS 65	FinFET 14	CMOS 45	CMOS 40
Arch.	SA	Cyclic	Stochastic	RNS	SSA
Resolution (bits)	10	12	10	9	6
Speed (GS/s)	0.08	0.25	0.1	0.215	1.2
DNL (LSB)	1.35	0.6	0.8	0.57	0.98
INL (LSB)	2	1.7	2.3	1.1	1.03
SSP(LSB)	0.59	0.69	N.A.	0.74	0.71
Power (mW)	9.6	15.4	0.78	24.2	0.52
[b] FOM (pJ/conv.-step)	0.23	0.32	0.025	0.48	0.014

[a] Post-layout simulation.

[b] $\mathrm{FOM} = \mathrm{Power} / (2^{\mathrm{Nlinear}} f_s)$.
$\mathrm{N_{linear}} = \mathrm{N_{bits}} - \log_2(\mathrm{INL}+1)$.

Acknowledgment

This work was supported by the Singapore Ministry of Education Academic Research Fund Tier 2 (MOE2019-T2-1-114).

References

[1] Kenichi Ohhata, "A 2.3-mW, 1-GHz, 8-Bit fully time-based two-step ADC using a high-linearity dynamic VTC CMOS," *IEEE J. Solid-State Circuits*, vol. 54, no. 7, pp. 2038–2048, July 2019.

[2] Shuang Zhu, Bo Wu, Yongda Cai and Yun Chiu, "A 2-GS/s 8-bit non-interleaved time-Domain flash ADC based on remainder number system in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1172–1183, April 2018.

[3] Kenichi Ohhata, "A 2.3-MW, 950-MHz, 8-Bit Fully-Time-Based Subranging ADC Using Highly-Linear Dynamic VTC," *IEEE Symposium on VLSI Circuits*, June 2018, pp. 95-96.

[4] KwangSeok Kim, Young-Hwa Kim, Wonsik Yu and SeongHwan Cho, "A 7 bit, 3.75 ps Resolution Two-Step Time-to-Digital Converter in 65 nm CMOS Using Pulse-Train Time Amplifier," *IEEE J. Solid-State Circuits*, vol. 48, no. 4, pp. 1009–1017, February 2013.

[5] Hayun Chung, Hiroki Ishikuro and Tadahiro Kuroda, "A 10-Bit 80-MS/s Decision-Select Successive Approximation TDC in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1232–1241, May 2012.

[6] Bongjin Kim, Hoonki Kim and Chris H. Kim, "An 8bit, 2.6ps two-step TDC in 65nm CMOS employing a switched ring-oscillator based time amplifier," *IEEE Custom Integrated Circuits Conference (CICC)*,September 2015, pp. 1-4.

[7] Bo Wu, Shuang Zhu, Yuan Zhou and Yun Chiu, "A 9-bit 215 MS/s Folding-Flash Time-to-Digital Converter Based on Redundant

Remainder Number System in 45-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 53, no. 3, pp. 839–849, March 2018.

[8] Zhe Liu *et al.*, "A DLL-based Configurable Multi-Phase Clock Generator for True-Time-Delay Wideband FMCW Phased-Array in 40nm CMOS," *IEEE International Symposium on Circuits and Systems (ISCAS)*, May 2018, pp. 1-4.

[9] KwangSeok Kim, WonSikYu and SeongHwan Cho, "A 9 bit, 1.12 ps Resolution 2.5 b/Stage Pipelined Time-to-Digital Converter in 65 nm CMOS Using Time-Register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, April 2014.

[10] Sung-Jin Kim *et al.*, "A 0.6V 1.17ps PVT-Tolerant and Synthesizable Time-to-Digital Converter Using Stochastic Phase Interpolation with 16× Spatial Redundancy in 14nm FinFET Technology," *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, February 2015, pp. 280-281.