

a402224

# **Design of Bandpass Delta-Sigma Modulators**

**Chen Yuan**



**School of Electrical & Electronic Engineering**

A thesis submitted to the Nanyang Technological University  
in fulfillment of the requirement for the degree of  
Master of Engineering

2005

TK  
7872  
.M6  
C518  
2005

## **Acknowledgement**

I would like to express my sincere appreciation to my supervisor, Ast./Prof. Tiew Kei Tee, for his invaluable advice and encouragement throughout my two-years research. Ast/Prof Tiew has, through many times of good discussions, taught me not only on how to deal with research problems, but also on how to develop a positive attitude toward solving difficult and challenging problems. This has certainly benefited me greatly. I also wish to thank Ms Du Yuan Yuan, all other research students and the technicians in Center for Integrated Circuits and Systems for their help and encouragement towards my research.

## Abstract

This thesis is focused on the design of high-speed bandpass continuous-time delta-sigma modulators for analog-to-digital conversion. First, a sixth-order bandpass delta-sigma modulator that uses subsampling relative to the radio frequency (RF) or intermediate frequency (IF) of a receiver, while oversampling the signal bandwidth is described in this thesis. The continuous-time filter that works at RF/IF frequency together with the discrete-time filter operating at lower frequency provide both noise shaping to quantization noise and subsampling noise. The transfer function derivation with finite Q factor bandpass filter is analyzed, and two different modulator structures are compared based on the derived transfer function to achieve better noise shaping for both quantization noise and subsampling noise. Because the sampling frequency is much lower than the RF/IF frequency, the complexity and power consumption of the digital signal processing stage is greatly reduced. The subsampling delta-sigma modulator is simulated in AMIS 0.5 $\mu$ m CMOS process; the peak SNDR is 51dB with 70MHz input frequency, 18.667MHz sampling frequency and 200kHz bandwidth. Second, a novel compensation technique that compensates for the intersymbol interference and excess loop delay in the 1-bit NRZ feedback DAC of continuous-time delta-sigma modulators is presented. The technique does not require a prior knowledge of the NRZ DAC output pulse in response to the input transition. As such, it could potentially compensate for most of the NRZ DAC nonidealities at high sampling frequency. A second-order bandpass continuous-time delta-sigma modulator is simulated to verify the effectiveness of the proposed DAC compensation technique..

# Table of Contents

Acknowledgement .....	i
Abstract .....	ii
Table of Contents .....	iii
List of Figures .....	v
List of Tables .....	viii
Chapter 1 Introduction .....	1
1.1 Motivation .....	1
1.2 Objective & Contributions .....	4
1.3 Thesis Organization .....	5
Chapter 2 Background of Delta-Sigma Modulator .....	6
2.1 Analog to Digital Conversion .....	6
2.2 Basic Theory of Delta-Sigma Modulator .....	8
2.2.1 Quantization .....	8
2.2.2 Noise Shaping .....	10
2.2.3 Bandpass Delta-Sigma Modulators .....	11
2.2.4 Discrete-Time vs. Continuous-Time .....	14
2.2.5 Performance Metrics .....	15
References .....	17
Chapter 3 Continuous-Time Bandpass Delta-Sigma Modulators .....	18
3.1 Design of Continuous-Time Delta-Sigma Modulator .....	18
3.1.1 Design Consideration and Challenges .....	18
3.1.2 Continuous-Time to Discrete-Time Transformation .....	20
3.1.3 Design Methodology .....	24
3.2 Clock Jitter .....	26
3.2.1 Clock Jitter in Continuous-Time Delta-Sigma Modulators .....	27
3.2.2 Techniques to Reduce the Clock Jitter in CT $\Delta\Sigma$ .....	29
3.3 Excess Loop Delay .....	36
3.3.1 Excess Loop Delay in Continuous-Time $\Delta\Sigma$ s .....	36
3.3.2 Compensation for Excess Loop Delay .....	37
3.4 Subsampling in Continuous-Time $\Delta\Sigma$ .....	40
3.5 Architectures with Mixers/Subsampling in $\Sigma\Delta$ Loop .....	44
References .....	50
Chapter 4 Subsampling Bandpass Delta-Sigma Modulators .....	55
4.1 Transfer Function Derivation with Finite Q Bandpass Filter .....	55
4.1.1 Z-domain Loop Transfer function .....	55
4.1.2 Matching the Z-Domain Loop Transfer Function to DT Bandpass $\Delta\Sigma$ Loop Transfer Function .....	58
4.2 The Proposed Subsampling Bandpass $\Delta\Sigma$ .....	60
4.2.1 Architecture of the Proposed Subsampling $\Delta\Sigma$ .....	62
4.2.2 Local-Oscillator Signal & Clock Jitter .....	67
4.2.3 The Proposed Sixth Order Subsampling Bandpass $\Delta\Sigma$ .....	69
References .....	73
Chapter 5 Simulation Results of the Proposed Subsampling $\Delta\Sigma$ .....	75
5.1 System Level Simulation Results .....	75
5.2 Circuit Level Implementation .....	79
5.3 Circuit Level Simulation Results .....	93

*Table of Contents*

---

Reference: .....	95
Chapter 6 DAC Compensation for Continuous-Time Delta-Sigma Modulators.....	97
6.1 Effects of NRZ DAC Nonidealities .....	97
6.2 DAC Nonidealities Compensation.....	99
6.3 Simulation Results .....	103
References .....	109
Chapter 7 Conclusions and Future Works .....	111
7.1 Conclusions.....	111
7.2 Recommendations for Future Works .....	113
Author's publications.....	115

## List of Figures

Figure 1. 1 Conventional super-heterodyne dual-conversion radio receiver architecture .....	2
Figure 1. 2 The receiver architecture with bandpass A/D .....	2
Figure 2. 1 Quantization noise power spectral density for Nyquist rate conversion and oversampling conversion .....	9
Figure 2. 2 LP $\Delta\Sigma$ and its discrete-time equivalent model .....	10
Figure 2. 3 BP $\Delta\Sigma$ and its discrete-time equivalent model .....	12
Figure 2. 4 NTF zeros and signal band locations in LP and BP $\Delta\Sigma$ .....	13
Figure 2. 5 The principle of quantization noise shaping in $\Delta\Sigma$ .....	13
Figure 2. 6 A model for DT and CT $\Delta\Sigma$ s .....	15
Figure 3. 1 Multi-stage bandpass $\Delta\Sigma$ .....	19
Figure 3. 2 Open-loop CT $\Delta\Sigma$ and its DT equivalent .....	21
Figure 3. 3 Clock jitter effect in DT versus CT design .....	26
Figure 3. 4 Equivalent representations of a jittered bit stream .....	27
Figure 3. 5 Error sequence energy in different types of modulator .....	29
Figure 3. 6 Input filter and SC feedback DAC in [13] .....	30
Figure 3. 7 Circuit diagram of second-order delta-sigma modulator based on transmission lines in [14] .....	31
Figure 3. 8 Second-order continuous-time modulator with FIR filters in its feedback path in [15] .....	32
Figure 3. 9 Shaped DAC pulse in [17] .....	33
Figure 3. 10 Static locking error in shaped DAC pulse .....	35
Figure 3. 11 Illustration of excess loop delay on NRZ DAC pulse .....	37
Figure 3. 12 Block diagram of multi-feedback $\Delta\Sigma$ in [5] .....	39
Figure 3. 13 Block diagram of continuous-time multibit $\Delta\Sigma$ architecture in [20] ..	39
Figure 3. 14 Block diagram of Subsampling CT $\Delta\Sigma$ .....	40
Figure 3. 15 Signal spectra in a subsampling CT $\Delta\Sigma$ .....	42
Figure 3. 16 Block diagram of the subsampling CT $\Delta\Sigma$ in [24] .....	43
Figure 3. 17 Block diagram of the 81MHz receiver in [26] .....	45
Figure 3. 18 Block diagram of the $\Delta\Sigma$ using a down-conversion mixer in the forward path together with a reconstruction filter in the feedback path [28] .....	46
Figure 3. 19 Block diagram of the $\Delta\Sigma$ using a down-conversion mixer in the forward path and frequency up-conversion in the feedback path [29] .....	47
Figure 3. 20 Diagram of the CT, frequency-translation bandpass $\Delta\Sigma$ in [31] .....	49
Figure 3. 21 Block diagram of the CT bandpass $\Delta\Sigma$ in [32] .....	49
Figure 3. 22 Frequency plots of NRZ/RZ with different pulse width .....	50
Figure 4. 1 Open Loop subsampling $\Delta\Sigma$ .....	56
Figure 4. 2 Block diagram of the proposed subsampling $\Delta\Sigma$ .....	61
Figure 4. 3 Equivalent DT subsampling $\Delta\Sigma$ .....	63
Figure 4. 4 Equivalent DT subsampling CRFB $\Delta\Sigma$ .....	64
Figure 4. 5 Equivalent DT subsampling CRFF $\Delta\Sigma$ .....	64
Figure 4. 6 CRFB&CRFF $NTF_q$ magnitude response .....	65

## List of Figures

Figure 4. 7 CRFB $NTF_s$ magnitude response.....	66
Figure 4. 8 CRFF $NTF_s$ magnitude response .....	66
Figure 4. 9 DAC jitter effect with different local-oscillator signal.....	68
Figure 4. 10 The proposed 6th order subsampling bandpass $\Delta\Sigma$ .....	69
Figure 4. 11 The DT filter in the proposed $\Delta\Sigma$ .....	71
Figure 4. 12 $NTF_q$ magnitude response of the proposed $\Delta\Sigma$ .....	72
Figure 4. 13 $NTF_s$ magnitude response of the proposed $\Delta\Sigma$ .....	73
Figure 5. 1 Output spectra of the ideal proposed subsampling $\Delta\Sigma$ with 200 kHz bandwidth (65536 points) .....	75
Figure 5. 2 Equivalent DT $\Delta\Sigma$ of the proposed subsampling $\Delta\Sigma$ .....	76
Figure 5. 3 Dynamic range plot of the ideal proposed subsampling $\Delta\Sigma$ & its equivalent DT $\Delta\Sigma$ .....	76
Figure 5. 4 Inband output spectra of the proposed subsampling $\Delta\Sigma$ and its equivalent DT $\Delta\Sigma$ with subsampling noise (65536 points).....	77
Figure 5. 5 Inband output spectra of the 1% DAC jittered proposed subsampling $\Delta\Sigma$ with different local-oscillator (65536 points) .....	78
Figure 5. 6 Peak SNDR vs. Q factor of continuous-time filter.....	79
Figure 5. 7 Circuit blocks of the proposed subsampling $\Delta\Sigma$ .....	79
Figure 5. 8 Second-order Gm-C bandpass filter .....	80
Figure 5. 9 Schematic of linearized OTA with common-mode detection .....	81
Figure 5. 10 Schematic of common-mode feedback circuit .....	82
Figure 5. 11 Schematic of $g_{mr}$ for Q-enhancement.....	82
Figure 5. 12 Schematic of the buffer .....	83
Figure 5. 13 Simulated frequency response of the continuous-time filter .....	83
Figure 5. 14 Schematic of the analog delay block .....	84
Figure 5. 15 Schematic of the folded cascode OpAmp .....	85
Figure 5. 16 Schematic of the switched capacitor common mode feedback .....	86
Figure 5. 17 Schematic of the biasing circuit .....	87
Figure 5. 18 Simulated frequency response of the OpAmp when driving a 2pF load on each output .....	87
Figure 5. 19 Schematic for the latch-based comparator .....	88
Figure 5. 20 Schematic for the TSPC D flip-flop .....	90
Figure 5. 21 Raise cosine shaped DAC .....	91
Figure 5. 22 Schematic of the switch driver .....	91
Figure 5. 23 Timing diagram .....	92
Figure 5. 24 Two phase clock generator .....	93
Figure 5. 25 Cadence simulation result of the proposed subsampling $\Delta\Sigma$ with ideal DT filter (2048 points) .....	93
Figure 5. 26 Cadence simulation result of the full circuit level implementation of proposed subsampling $\Delta\Sigma$ (2048 points).....	94
Figure 5. 27 Dynamic range plot of the proposed subsampling $\Delta\Sigma$ with full circuit level implementation.....	94
Figure 6. 1 Distortion due to limited rise and fall times of a DAC using NRZ pulse .	97
Figure 6. 2 Modeling of NRZ DAC nonideal output.....	98
Figure 6. 3 Block diagram of the proposed $\Delta\Sigma$ with DAC nonidealities compensation .....	99

*List of Figures*

---

Figure 6. 4 Illustration of the NRZ DAC nonidealities compensation scheme .....	100
Figure 6. 5 Block diagram of control logic .....	102
Figure 6. 6 Circuit blocks of the second-order bandpass $\Delta\Sigma$ M with DAC compensation .....	103
Figure 6. 7 Circuit blocks of the control logic .....	104
Figure 6. 8 Schematic of the reference/compensation DAC cells .....	105
Figure 6. 9 Schematic of the combined reference DAC cell connected to node 1,2 .	106
Figure 6. 10 Output spectra of the second-order $\Delta\Sigma$ M without compensation.....	107
Figure 6. 11 Output spectra of the second-order $\Delta\Sigma$ M with compensation.....	107
Figure 6. 12 Histogram of SNR with DAC mismatch of 0.01 variance. ....	109

## List of Tables

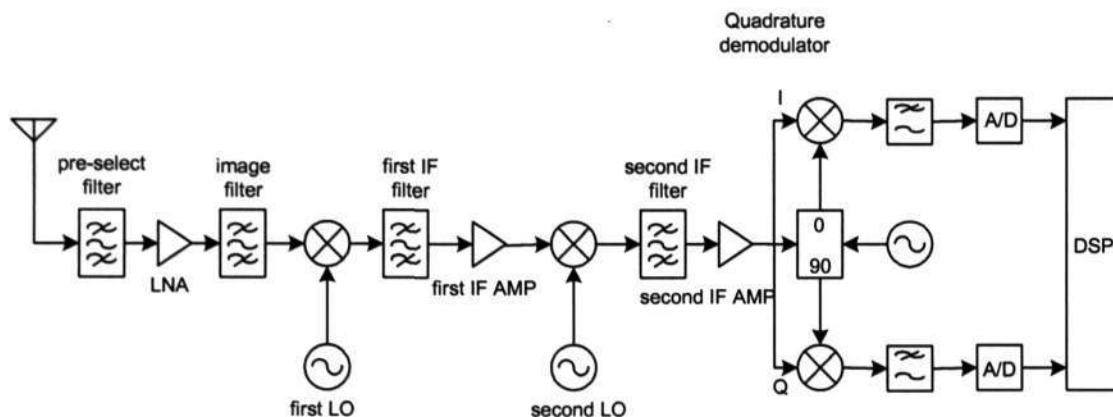
Table 5. 1 SNDR vs. center frequency shift of the CT bandpass filter with subsampling noise.....	77
Table 5. 2 Transistor sizes of $g_{m1}$ , $g_{m2}$ , $g_{m3}$ , $g_{m4}$ .....	81
Table 5. 3 Transistor sizes of the common-mode feedback.....	82
Table 5. 4 Transistor sizes of $g_{mr}$ .....	83
Table 5. 5 Transistor sizes of the buffer .....	83
Table 5. 6 Transistor sizes and bias voltages of NMOS input OpAmp.....	85
Table 5. 7 Transistor sizes of the bias circuit.....	88
Table 5. 8 Transistor sizes of the comparator .....	89
Table 5. 9 Transistor sizes of the TSPC D flip-flop .....	89
Table 6. 1 Cadence/MATLAB simulation results of the second-order $\Delta\Sigma$ M.....	108

# Chapter 1

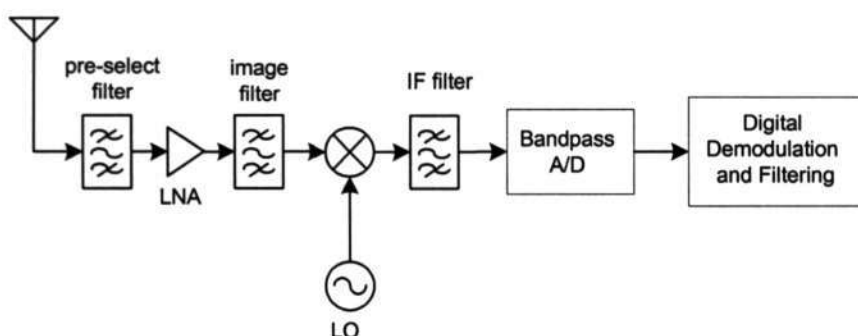
## Introduction

### 1.1 Motivation

The increasing demand for mobile communications has introduced numerous challenges in the design of cellular and cordless systems. One way to improve these systems is to reduce the cost and power consumption of the radio transceiver. Since bandpass delta-sigma analog-to-digital converters (A/Ds) can digitize high-frequency signals with a narrow bandwidth, they enable the RF IC designer to consider novel system architectures. In a typical radio receiver design, the baseband conversion scheme requires demodulation of the message using two matched mixers fed by in-phase (I) and quadrature (Q) carriers. The output of each mixer is then low-pass filtered and subsequently converted to digital form with separate A/D converters as shown in Fig. 1.1. In this case, analog quadrature demodulation which suffers from component variation, temperature sensitivities, noise, nonlinearities, and dc offset is used. If the A/D conversion is used at the intermediate frequency (IF) stage, as shown in Fig. 1.2, demodulation and IF filtering can be done digitally which avoids I and Q mismatch and other limitations of analog circuits. The robustness of the digital circuitry gives manufacturing advantages and allows the use of sophisticated algorithms, which are especially useful with digitally coded transmission. Furthermore, the digital filtering makes possible greater flexibility and programmability, which is a preferred property in multi-mode mobile phones.



**Figure 1.1 Conventional super-heterodyne dual-conversion radio receiver architecture**



**Figure 1.2 The receiver architecture with bandpass A/D**

Delta-sigma A/D converters are often preferable to conventional Nyquist rate A/D converters since they use oversampling which relaxes the requirement for an analog anti-aliasing pre-filter, they are robust against circuit imperfections, have inherent linearity due to the use of single-bit quantizer, and can achieve high resolution with reduced complexity. Bandpass delta-sigma A/D converters provide a means of performing high-resolution conversion on narrowband signals at high frequencies which is well suited for use in front-end or early IF stages of radio receivers.

Bandpass delta-sigma modulator is usually realized either by a discrete time (DT) circuit such as switched-capacitor (SC) or switched-current (SI) circuits, or by continuous time (CT) circuit that uses Gm-C techniques or LC filter. Continuous time

bandpass delta-sigma modulators are much faster than discrete time bandpass delta-sigma modulators in the same process which makes them suitable for such high-frequency applications. The main problem of continuous time delta-sigma modulators is the clock jitter and other DAC nonidealities such as excess loop delay.

In this thesis, a new compensation technique to compensate for the NRZ DAC nonidealities is presented. This compensation is based on acquiring the error signal by using additional DACs which are matched to the feedback DAC. The major advantage of this compensation technique is that it does not require any prior knowledge of the DAC nonidealities.

Normally for bandpass delta-sigma modulators, the sampling frequency is four times the center frequency, resulting in a very high sampling frequency. Sampling at such high frequencies requires expensive process and increases the complexity and power consumption of the digital signal processing stage. This problem can be solved by using an architecture employing subsampling with respect to the IF signal. This enables sampling at a frequency much lower than the center frequency and realizing the frequency down-conversion.

Despite these features subsampling suffers from some drawbacks. One drawback is that the subsampling operation will introduce more noise than conventional sampling operation. Another drawback is the performance of continuous-time filter will degrade that a controllable moderate  $Q$  factor continuous-time bandpass filter cannot adequately suppress quantization noise. So a subsampling bandpass delta-sigma modulator is proposed; a discrete-time filter is placed after the continuous-time filter to give additional noise shaping. The continuous-time bandpass filter operates at high

frequency and after subsampling the discrete-time filter operates at low frequency. These two filters working together provide noise shaping both to the quantization noise and the noise introduced by the subsampling operation.

## 1.2 Objective & Contributions

1. Review the published techniques that reduce the clock jitter in continuous-time  $\Delta\Sigma$ M s
2. Review the published techniques that compensate excess loop delay in continuous-time  $\Delta\Sigma$ M s
3. Review the published architectures with mixers/subsampling in  $\Sigma\Delta$ M loop
4. Analysis the transfer function derivation with finite Q-factor bandpass filter with subsampling
5. A subsampling bandpass  $\Delta\Sigma$ M for digitizing signals close to the front-end of a radio receiver with the following characteristics is proposed:
  - Subsampling of IF signal which results in a sampling frequency lower than the IF.
  - A moderate Q-factor continuous-time filter and a discrete-time filter are used together to provide noise shaping both to quantization noise and sampling noise.
  - A jitter insensitive pulse shaped DAC is used with the function of frequency translation.

6. A novel compensation technique that compensates for the intersymbol interference and excess loop delay in the 1-bit NRZ feedback DAC of continuous-time  $\Delta\Sigma$ Ms is proposed

### 1.3 Thesis Organization

This chapter introduces the motivation and objectives of this report and the application of the bandpass delta-sigma modulator. In Chapter 2, the background of the delta-sigma modulators is presented. Chapter 3 reviews some important properties of continuous time delta-sigma modulators and architectures with mixers/subsampling in modulator loop. The proposed subsampling bandpass delta-sigma modulator is analyzed in Chapter 4 and the associated system level and circuit level simulation results are given in Chapter 5. Chapter 6 presents the novel DAC compensation scheme for continuous time delta-sigma modulators. Chapter 7 is the conclusion and future works.

## Chapter 2

# Background of Delta-Sigma Modulator

### 2.1 Analog to Digital Conversion

The exploitation of digital signal processing is increasing all the time. Its benefits are flexibility, programmability and insensitivity to nonidealities. However, information is usually transferred, collected, and/or used in analog form. The imperfections of analog circuitry and different noise sources limit the achievable conversion resolution and dynamic range. Technology scaling does not improve the situation and the demand for lower supply voltages actually makes the design more difficult and calls for new analog circuit structures. Several well-know ADC architectures are:

#### 1. Flash and Folding Converters

Due to large area flash and folding converters are best suited for resolutions  $< 10$  bits at high sampling rates. The power consumption of flash converters is also very large. These types of ADCs do not always have an input S/H circuit since this would limit the conversion speed. Without a S/H circuit at the input the dynamic performance at high input frequencies is poor. Some two-stage folding converters suitable for high resolutions at high sampling rates have been reported. They are however usually implemented in bipolar or BiCMOS processes.

## 2. Pipelined Converters

For higher resolutions pipelined converters are better suited than flash or folding converters. The requirements on the comparators can be relaxed by using digital correction. However, inaccuracies in the DACs necessitate calibration techniques for high resolutions..

## 3. Time-Interleaved Converters

In the time-interleaved converter several ADCs operating at a lower speed are connected in parallel. Mismatch in the channels will cause distortion but can be reduced by calibration techniques and the dynamic performance at high input frequencies is limited by phase-skew errors between the channel. These errors are reduced by an input S/H. However, the input S/H must operate at the full speed of the ADC. Therefore it is difficult to design.

## 4. Oversampling Delta-Sigma Converters ( $\Delta\Sigma$ )

Oversampling ADCs are relatively insensitive to imperfections in the analog components, which make them suitable for high resolutions. The main drawback is that the oversampling limits the signal bandwidth. The oversampling delta-sigma converter is normally used for signal bandwidths up to a few MHz.

Depending on the sampling frequency, ADCs can be separated into two categories. The first category is Nyquist ADC such as the architectures 1,2 and 3 described above. The second category is the architecture 4, oversampling delta-sigma converters.

## 2.2 Basic Theory of Delta-Sigma Modulator

$\Delta\Sigma$  have become a popular alternative to conventional Nyquist A/D converters. The basic principle behind  $\Delta\Sigma$  is to trade signal bandwidth for resolution. Moreover, the feedback loop with filter can shape the spectra of the modulation noise. The traditional ADC requires a very sharp roll-off analog lowpass (LP) filter before the signal sampling occurs. In the case of LP  $\Delta\Sigma$  a low order LP filter, for example an RC filter, is usually adequate, because of the higher sampling frequency. The  $\Delta\Sigma$  is a simple circuit structure and, compared to Nyquist rate converters, is insensitive to analog circuit nonidealities, despite the higher clock rate. However, the required digital filter and decimation stage have to be considered in the total power budget when an A/D topology is selected.

### 2.2.1 Quantization

If the quantization step of a B bit ADC is  $\Delta$  and the quantization error is evenly distributed in the range  $\pm \Delta/2$ , with  $\Delta=2V_{ref}/(2^B-1)$ . We obtain the average quantization noise power as

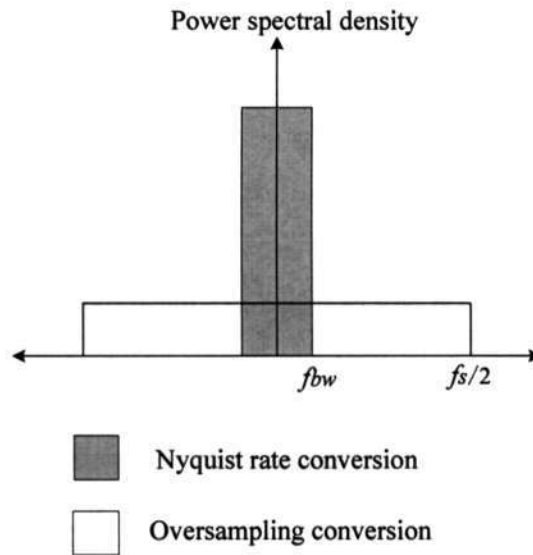
$$\sigma_e^2 = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \cong \left( \frac{2V_{ref}}{2^B} \right)^2 / 12 \quad (2.1)$$

If the signal is treated as a zero mean random process and its power is  $\sigma_x^2$ , then the signal to noise ratio is :

$$SNR = 10 \log \left( \frac{\sigma_x^2}{\sigma_e^2} \right) = 10 \log \left( \frac{\sigma_x^2}{V_{ref}^2} \right) + 4.77 + 6.02B \text{ [dB]} \quad (2.2)$$

The SNR can be improved by using oversampling technique. Due to the sampling operation, the quantization noise power folds in the frequency range  $[0, f_s/2]$  as shown in Fig.2.1. Assuming that quantization noise is white, we may write the single-sided quantization noise power spectral density as

$$N_q = \frac{2}{f_s} \cdot \sigma_e^2. \quad (2.3)$$



**Figure 2. 1 Quantization noise power spectral density for Nyquist rate conversion and oversampling conversion**

If the desired signal band  $f_{bw}$  is filtered by an ideal brickwall digital filter ( $H_d$ ) then the in-band noise power is

$$\sigma_{ey}^2 = \int_{-f_{bw}}^{f_{bw}} |H_d(f)|^2 N_q df = 2 \int_0^{f_{bw}} |H_d(f)|^2 N_q df = \frac{\sigma_e^2}{f_s} 2f_{bw} = \frac{\sigma_e^2}{OSR}, \quad (2.4)$$

where the oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{2f_{bw}} = \frac{f_s}{f_{Nyq}}. \quad (2.5)$$

The achievable SNR in dB is then:

$$SNR = 10 \log \left( \frac{\sigma_x^2}{\sigma_{ey}^2} \right) = 10 \log(\sigma_x^2) - 10 \log(\sigma_e^2) + 10 \log(OSR) \quad [dB] \quad (2.6)$$

We see that by doubling the sampling frequency the quantization noise power can be reduced by 3dB or that the resolution is improved by half a bit. This is valid for all ADCs but further noise reduction is possible by quantization noise shaping, which is utilized in  $\Delta\Sigma$ Ms.

### 2.2.2 Noise Shaping

The effectiveness of oversampling can be improved by a  $\Delta\Sigma$ M, in which the feedback signal is used to shape the quantization noise spectra. In LP  $\Delta\Sigma$ Ms (Fig.2.2) the basic building blocks are an integrator and a quantizer and D/A converter. By linearizing the loop the output signal of a first order LP  $\Delta\Sigma$ M can be written in the z-domain as

$$Y_{LP}(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \quad (2.7)$$

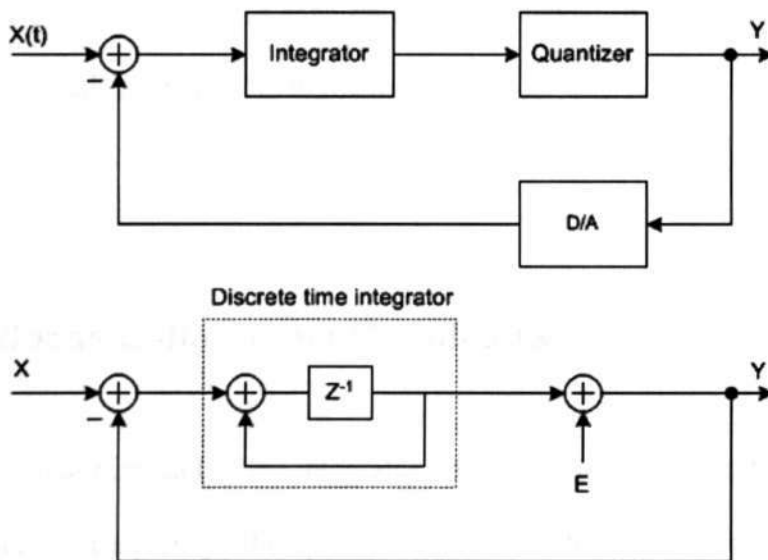


Figure 2. 2 LP  $\Delta\Sigma$ M and its discrete-time equivalent model

We see that the noise transfer function (NTF) has a zero at DC and hence the quantization noise is high-pass filtered. The signal transfer function (STF) causes only one clock period delay between input and output.

The inband noise power at the output of a first order LP  $\Delta\Sigma$  is:

$$\sigma_{ey}^2 = \sigma_e^2 \frac{\pi^2}{3} \left( \frac{2f_{bw}}{f_s} \right)^3 = \sigma_e^2 \frac{\pi^2}{3} \left( \frac{1}{OSR} \right)^3 \quad (2.8)$$

The SNR in dB is then:

$$SNR = 10 \log \left( \frac{\sigma_x^2}{\sigma_{ey}^2} \right) = 10 \log(\sigma_x^2) - 10 \log(\sigma_e^2) + 10 \log \left( \frac{\pi^2}{3} \right) + 30 \log(OSR) \quad [dB] \quad (2.9)$$

For every doubling of the sampling frequency, the SNR improves by 9dB, or equivalently, the resolution improves by 1.5bits.

This is a significant improvement compared to eq. (2.6) and it enables the use of a low resolution internal quantizer (even 1-bit) in the loop if the OSR is high enough. A more effective quantization noise shaping can be achieved by increasing the order of the loop filter or adding resonators to the loop.

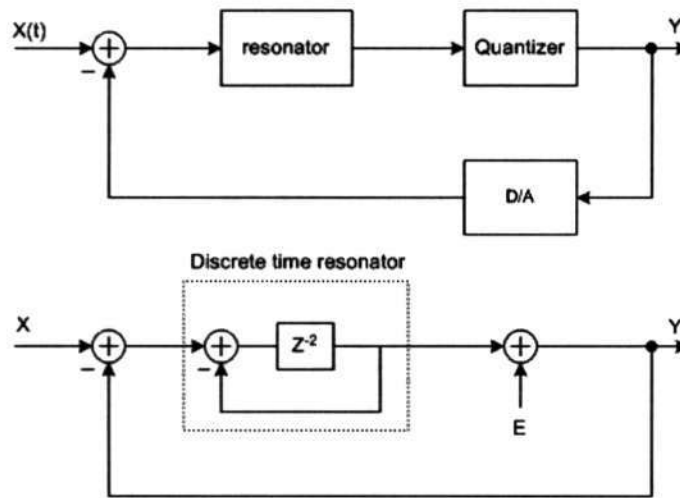
### 2.2.3 Bandpass Delta-Sigma Modulators

If we use a resonator instead of the integrator, the noise would tend to be shaped away from the resonate frequency, the quantization noise then has a band reject shape

because the loop filter is bandpass, and the resulting  $\Delta\Sigma$  is called bandpass (BP)  $\Delta\Sigma$  [1].

This can be done by replacing the integrators in the LP  $\Delta\Sigma$  by resonators, which is equivalent to  $z^{-1} \rightarrow -z^{-2}$  transformation. This leads to the second order BP  $\Delta\Sigma$  structure as shown in Fig. 2.3 and we obtain

$$Y_{BP}(z) = z^{-2}X(z) + (1 + z^{-2})E(z). \quad (2.10)$$



**Figure 2. 3 BP  $\Delta\Sigma$ M and its discrete-time equivalent model**

Now the NTF has zeros at the frequencies  $\pm fs/4$  instead of DC and the quantization noise is shaped away from the frequencies around  $fs/4$ . The differences between LP and BP  $\Delta\Sigma$ M are further clarified in Fig. 2.4 and 2.5.

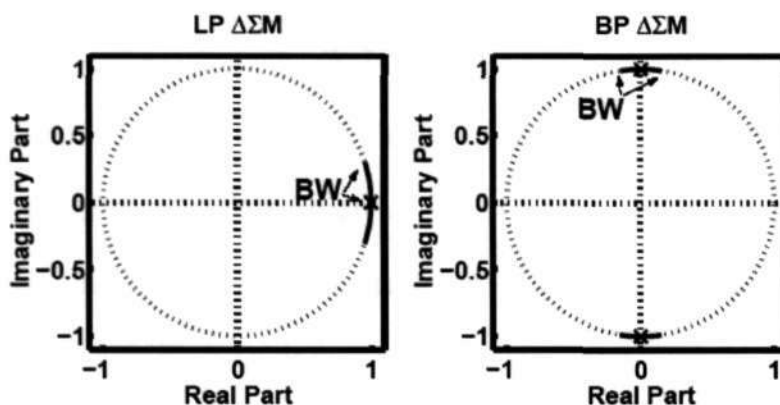


Figure 2. 4 NTF zeros and signal band locations in LP and BP  $\Delta\Sigma$ M

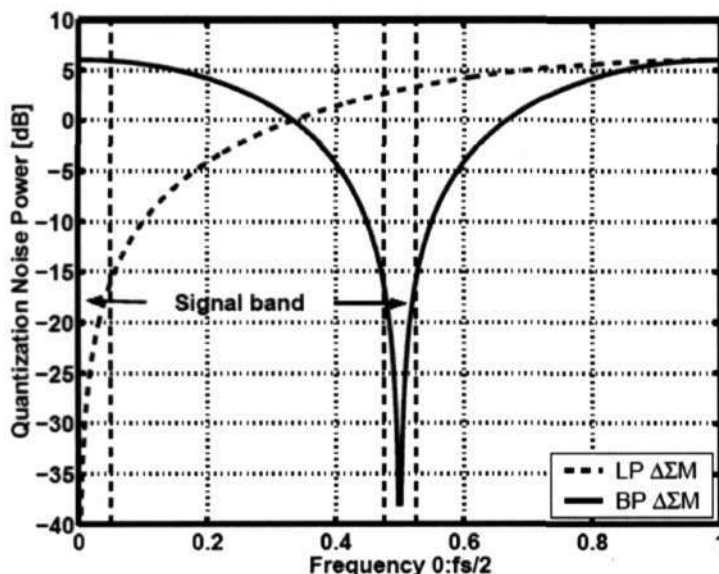


Figure 2. 5 The principle of quantization noise shaping in  $\Delta\Sigma$ M

The LP  $\Delta\Sigma$ M and their properties are well-known and therefore the easiest way to design BP  $\Delta\Sigma$ M is to select a suitable LP  $\Delta\Sigma$ M prototype and perform the LP to BP transformation. The preceding  $z^{-1} \rightarrow -z^{-2}$  transformation is attractive because the properties of the LP prototype, such as stability and dynamics, are preserved. The disadvantage is that the notch of the NTF is fixed at the  $\pm fs/4$ . The general discrete-time LP-to-BP transformation is

$$z \rightarrow -z \frac{z+a}{az+1}, -1 < a < 1. \quad (2.11)$$

and it enables full control of the notch frequency through the parameter  $a$ . However, the dynamic properties of the LP prototype are not preserved [2]. The third possibility is to use a filter optimizer to design a suitable NTF for the specific purpose.

The LP-to-BP transformation doubles the order of the loop filter and hence, in principle, the number of required active components is also doubled. However, one should take note that, one BP  $\Delta\Sigma$ M replaces two LP  $\Delta\Sigma$ Ms in both  $I$  and  $Q$  signal paths and hence no extra active components are needed.

#### 2.2.4 Discrete-Time vs. Continuous-Time

$\Delta\Sigma$ M can be designed as discrete-time (DT) or continuous-time (CT) circuits as shown in Fig. 2.6. With DT circuits an S/H stage is required at the input of the  $\Delta\Sigma$ M to convert a CT analog signal to a discrete-time signal. This block can limit the linearity and noise floor of the whole  $\Delta\Sigma$ M and, furthermore, an anti-alias filter is needed prior to the sampler. With CT circuits the sampling occurs only in the ADC and the sampling errors are attenuated by the loop. The loop filter also operates as an anti-alias filter and therefore the analog pre-filter may be eliminated. The power dissipation of CT  $\Delta\Sigma$ Ms is usually lower than that of DT switched-capacitor (SC) circuits and they are suitable for high-speed and low-power applications. However,

the linearity requirements are harder to achieve, for example with the RC or Gm-C techniques, than with the SC technique. The main problem of the CT  $\Delta\Sigma$ Ms is the clock jitter [3], which will be discussed in Chapter 3.

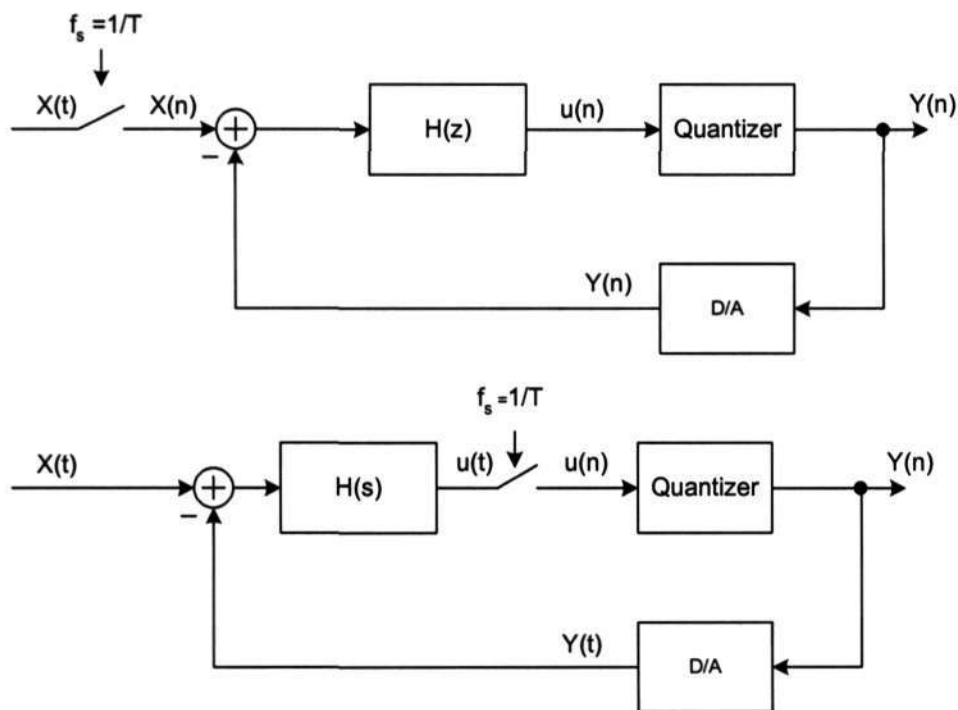


Figure 2. 6 A model for DT and CT  $\Delta\Sigma$ Ms

## 2.2.5 Performance Metrics

The *signal-to-noise ratio (SNR)* is the ratio between signal power and noise power within a specified frequency band. The SNR is usually shown as a function of the input signal level and the measured peak.

The signal-to-quantization noise ratio (SQNR) is the ratio between signal power and quantization noise power within a specified band. The SQNR is a useful figure in the design phase and for a  $2\bar{N}$ -order BP  $\Delta\Sigma\text{M}$ , we have [4]

$$SQNR_{\max} \approx 10 \log_{10} \left( \frac{3(2\bar{N}+1)OSR^{(2N+1)}}{2\pi^{2N}} \right) + 6.02(B-1) \quad (2.12)$$

where B is the number of bits in the internal ADC. One should be very cautious about using eq. (2.12) for high order ( $N>2$ ) or multi-bit ( $B>2$ )  $\Delta\Sigma\text{M}$ s because the selected circuit structure and different nonidealities affect the achievable SQNR quite considerably. Therefore system level simulation with specific circuit architecture has to be performed to obtain more realistic results.

*Dymanic Range (DR)* has a similar definition as described for the conventional converters. It is defined as the range of input amplitude (assuming single sinusoid at some specific frequency) that gives positive SNR at the output. Since DR is usually expressed in dB, it can be regarded as the power of sinusoid with maximum stable amplitude, to the power of the sinusoid that gives 0 dB SNR. A DR plot is obtained by plotting SNR vs. input amplitude. Dynamic range can also be defined in terms of bits:

$$DR_{bit} = \frac{DR_{dB} - 1.761}{6.021} \quad (2.13)$$

*Speed, Power Dissipation and Area.* Both the sampling frequency and OSR have to be known in order to define the real conversion speed of the  $\Delta\Sigma\text{M}$  which, in the case of Nyquist ADCs, is usually expressed as the number of samples per second. When different circuits are compared the input signal frequency has to be taken into account

because high linearity is harder to achieve at high frequencies and clock jitter may reduce the circuit dynamic range.

Power dissipation is a very important issue in battery-operated devices, and also because of heating problems, has to be considered in other applications too. The technology scaling, together with low power supplies, helps to reduce the power dissipation of digital circuits, but low power consumption and a low power supply in analog circuits are challenges that need to be solved.

The circuit area can be an important figure of merits in some applications, but usually the area of  $\Delta\Sigma$ M is considered to be small compared to other ADC topologies. However, in multi-bit  $\Delta\Sigma$ M the circuit area may be a significant issue.

## References

- [1] R. Schreier and M. Snelgrove, "Bandpass Sigma-Delta Modulation," IEE Electronics Letters, Vol. 25, No. 23, Nov. 1989, pp.1560-1561.
- [2] S. Norsworthy, R. Schreier and G. Temes , "Delta-Sigma Data Converters," New York, IEEE PRESS, 1997.
- [3] H. Tao and J.M. Khoury, "Analysis of Timing Jitter in Bandpass Sigma-Delta Modulators," IEEE Trans. Circuits and System II, Vol. 46, No. 8, Aug. 1999, pp. 991 – 1001.
- [4] J. Candy and G. Temes, "Oversampling Delta-Sigma Data Converters," New York, IEEE PRESS, 1992.

# Chapter 3

## Continuous-Time Bandpass Delta-Sigma Modulators

### 3.1 Design of Continuous-Time Delta-Sigma Modulator

Bandpass delta-sigma modulator is well suited for A/D conversion of narrow band signals modulated on a carrier signal. Due to relaxed settling time requirement, and sampling within the loop, continuous-time delta-sigma modulator can operate at higher sampling frequency with moderate dynamic range.

#### 3.1.1 Design Consideration and Challenges

As in the case of the design of many other analog circuits, the design of delta-sigma modulator is governed by several performance goals such as SNR and power consumption.

A brief overview of the most important design considerations and challenges will be given here:

- *Architecture:* The two most commonly used architectures are the single loop  $\Delta\Sigma$  and multi stage (MASH)  $\Delta\Sigma$  [1]. A multi stage  $\Delta\Sigma$ , depicted in Fig. 3.1, uses a second-order  $\Delta\Sigma$  to shape the quantization noise of the previous

modulator and accomplish noise cancellation in the digital filter, thereby avoiding stability problems. The disadvantage of the MASH structure is its sensitivity to mismatch of quantizer level and filter functions. However, current CMOS technology usually has large process variation, which could result up to 50% variation in the RC time constant. It will result in incomplete cancellation, which causes the cancellation to fail, and the SNR will not be improved.

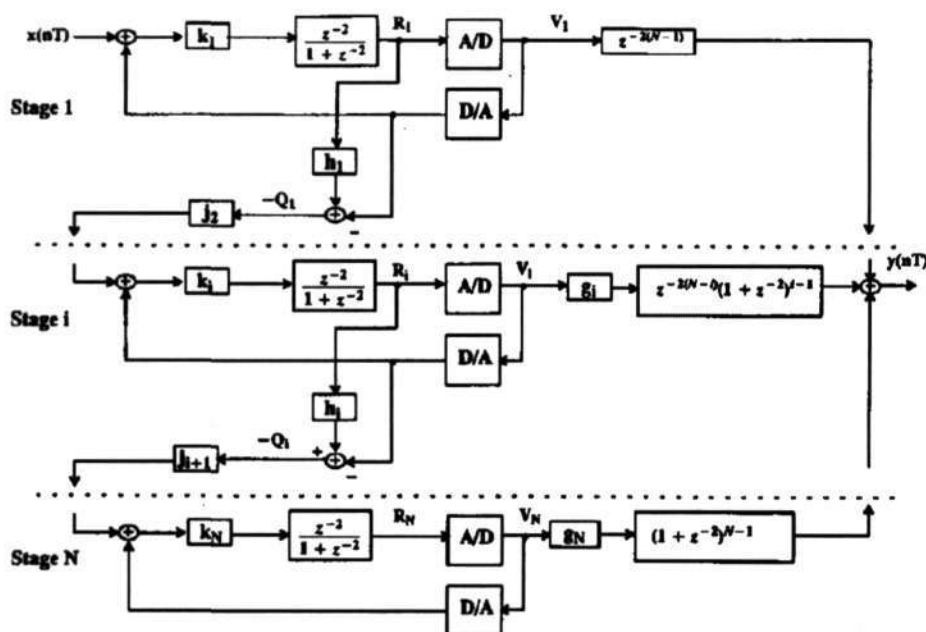


Figure 3. 1 Multi-stage bandpass  $\Delta\Sigma\text{M}$

- Quantizer Resolution:* Increasing the resolution of the quantizer in a  $\Delta\Sigma\text{M}$  increases the theoretically achievable SNR of the modulator considerably. Unfortunately, the required accuracy of the implementation increases proportionally. The linearity of the DAC directly affects the performance of  $\Delta\Sigma\text{M}$ . A one bit DAC can achieve higher degree of linearity than that of a

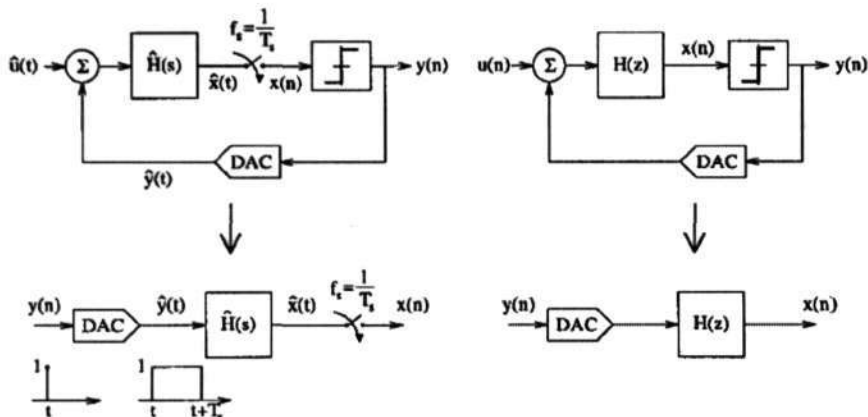
multi-bit DAC. For a multi-bit DAC, some calibration [2] and mismatch shaping techniques are needed such as dynamic element matching (DEM) [3].

- *Order of the Loop Filter:* A high order loop filter results in a high theoretical SNR, even at low oversampling ratio. For a loop filter with an order larger than two, the stability of the  $\Delta\Sigma$  depends on the input signal and will be more affected by the excess loop delay [4] [5].
- *Oversampling Ratio:* Increasing the oversampling ratio is the easiest way for increasing the theoretical SNR of a  $\Delta\Sigma$ . Generally, changing the OSR does not affect the stability of the modulator nor does it require a more accurate implementation. The major obstacle for very high sampling frequency is the bandwidth requirement on the  $\Delta\Sigma$  circuitry itself and signal processing circuitry following the modulator.

### 3.1.2 Continuous-Time to Discrete-Time Transformation

A Continuous-time  $\Sigma\Delta$  is internally a discrete-time system [5]. Because the quantizer in a CT  $\Sigma\Delta$  is clocked, which means there is an implicit sampling action inside the modulator, and sampled circuits are DT circuits. We can make the sampling explicit by placing the S/H immediately prior to the quantizer, as depicted in the upper left diagram of Fig. 3.2; this does not change the behavior of the modulator. If we want to know how this is equivalent to a DT modulator, shown in the upper right of

Fig. 3.2, then it is illustrative to make both inputs zero and open both loops just before the quantizer. This leads to the bottom two diagrams of Fig. 3.2.



**Figure 3. 2 Open-loop CT ΔΣM and its DT equivalent**

In the CT open-loop diagram, the quantizer output  $y(n)$  is a DT quantity, and we may think of the DAC as a “discrete-to-continuous converter.” It generates a CT pulse  $\hat{y}(t)$  from the output sampled  $y(n)$ . This pulse is filtered by  $\hat{H}(s)$  (the CT loop filter) to provide  $\hat{x}(t)$  at the quantizer input, which is then sampled to produce the DT quantizer input  $x(n)$ . The input and output of both CT and DT open-loop diagrams are thus DT quantities. A CT  $\Sigma\Delta M$  would produce the same sequence of output bits  $y(n)$  as DT  $\Delta\Sigma M$  if the outputs to the quantizer in both were identical at the following sampling instants [6]:

$$x(n) = x(t) \Big|_{t=nT_s} \cdot \tag{3.1}$$

This would be satisfied if the impulse responses of the open loops in Fig. 3.2 were equal at sampling times, leading to the condition [7]

$$Z^{-1}\{H(z)\} = L^{-1}\{\hat{R}_D(s)\hat{H}(s)\} \cdot \left(\sum_{k=0}^{\infty} \delta(t - nT_s)\right), \tag{3.2}$$

or, in the time domain [8]

$$h(n) = [\hat{r}_D(t) * \hat{h}(t)] \Big|_{t=nT_s} = \int_{-\infty}^{\infty} \hat{r}_D(\tau) \hat{h}(t - \tau) d\tau \Big|_{t=nT_s}, \quad (3.3)$$

where  $\hat{r}_D(t)$  is the impulse response of the DAC. Since we require the CT and DT impulse responses to be the same, the transformation between the two is called the *impulse-invariant transformation* [7]. Using the impulse-invariant transformation eq. (3.2) can be written as [4]:

$$H(z) = Z \{ L^{-1} \{ \hat{R}_D(s) \hat{H}(s) * \frac{1}{1 - e^{-sT_s}} \} \}. \quad (3.4)$$

Using the Cauchy residue theorem, the equivalent DT transfer function can be solved:

$$H(z) = \sum_{n=1}^N \operatorname{Res}_{s=s_n} \frac{\hat{R}_D(s) \hat{H}(s)}{1 - e^{-sT_s} z^{-1}}. \quad (3.5)$$

In which  $s_n$  are the poles of  $\hat{R}_D(s)$  and  $\hat{H}(s)$ . The residue  $\operatorname{Res} f(x)$  for an  $m$ -th order pole at  $x = x_0$  is given by

$$\operatorname{Res}_{x=x_0} f(x) = \frac{1}{(m-1)!} \lim_{x \rightarrow x_0} \left\{ \frac{d^{m-1}}{dx^{m-1}} [(x - x_0)^m f(x)] \right\}. \quad (3.6)$$

As an example, the equivalent DT transfer function of a second order resonator will be calculated. The CT transfer function of a resonator is:

$$\hat{H}(s) = \frac{\omega_g (s + \omega_z)}{s^2 + s\omega_0/Q + \omega_0^2}. \quad (3.7)$$

If the DAC uses a Return-to-Zero (RZ) pulse shape with duration of  $0.5T_s$ . The impulse response  $\hat{r}_D(t)$  of the DAC pulse shape is given by:

$$\hat{r}_D(t) = u(t - T_s/4) - u(t - 3T_s/4). \quad (3.8)$$

In which  $u(t)$  is the unit step function. The Laplace transform of the DAC pulse shape equals to:

$$\hat{R}_D(s) = L\{\hat{r}_D(t)\} = \frac{e^{-s\frac{T_s}{4}} - e^{-s\frac{3T_s}{4}}}{s} \quad (3.9)$$

The  $H(z)$  can be calculated by residues, giving :

$$H(z) = z^{-1} \left( \frac{(e^{s\frac{3T_s}{4}} - e^{s\frac{T_s}{4}})\omega_g(s + \omega_g)}{s(s - s_1^*)(1 - e^{sT_s}z^{-1})} \Big|_{s \rightarrow s_1} + \frac{(e^{s\frac{3T_s}{4}} - e^{s\frac{T_s}{4}})\omega_g(s + \omega_g)}{s(s - s_1)(1 - e^{sT_s}z^{-1})} \Big|_{s \rightarrow s_1^*} \right), \quad (3.10)$$

with  $s_1 = -\omega_0/2Q + j\omega_0\sqrt{1-1/4Q^2}$  and  $s_1^*$  being the complex conjugated of  $s_1$ .

Because of the terms  $e^{-s\frac{3T_s}{4}}$  and  $e^{-s\frac{T_s}{4}}$  in eq. (3.9), the impulse-invariant transformation does not converge in the left half of the complex plane. This problem is overcome by recognizing that  $e^{-sT_s}$  equals a delay of full sample period and results in a term  $z^{-1}$  in the equivalent DT transfer function, as a result, we replace  $e^{-s\frac{T_s}{4}}$  and  $e^{-s\frac{4T_s}{4}}$  by  $e^{s\frac{3T_s}{4}}$  and  $e^{s\frac{T_s}{4}}$  in eq. (3.10), respectively.

Combining the two terms in eq. (3.10) gives:

$$H(z) = k_g \frac{z^{-1}(a_1 + a_2 z^{-1})}{1 - 2b \cos(\theta_0)z^{-1} + b^2 z^{-2}} \quad (3.11)$$

For  $Q \geq 1$ :

$$\theta_0 \approx \omega_0 T_s \quad (3.12)$$

$$k_g \approx (\omega_g / \omega_0) \sin(\omega_0 T_s / 4) \quad (3.13)$$

$$b = e^{-\theta_0/2Q} \quad (3.14)$$

$$a_1 \approx (\omega_z / \omega_0) \sin(\theta_0 / 2) - \cos(\theta_0 / 2) \quad (3.15)$$

$$a_2 \approx \cos(3\theta_0 / 2) - (\omega_z / \omega_0) \sin(3\theta_0 / 2) \quad (3.16)$$

Clearly, the poles of the equivalent DT transfer function are fully determined by the poles of the CT transfer function. The relationship between the CT poles  $s_1$  and the DT poles  $z_1$  is given by:

$$z_1 = e^{s_1 T} \quad (3.17)$$

The zeros of the DT transfer function depend on both the poles and zeros of the CT transfer function. When the equivalent DT transfer function  $H(z)$  of the CT resonator has been determined, the coefficient  $\omega_0$ ,  $Q$ ,  $\omega_g$  and  $\omega_z$  of the CT resonator can be found using eqs. (3.12)-(3.16). Note that the CT loop filter structure should have sufficient degrees of freedom to allow for the implementation of the desired DT loop filter transfer function.

### 3.1.3 Design Methodology

So the design of a  $\Delta\Sigma\text{M}$  with a continuous time loop filter can be done in discrete time domain. The sampled response of the CT loop filter to the pulse of the quantizer DAC can be replaced by an equivalent DT loop filter. The stability of the  $\Delta\Sigma\text{M}$  is also analyzed in the discrete time domain. Once the DT loop filter is designed, the CT loop transfer function can be determined from the DT loop filter and the pulse shape of the DAC. The direct transformation of DT transfer function is possible using the above techniques or *Schreier's* method in the time domain [33]. The latter uses a state-space

representation. Although *Schreier's* transformation is more general, the heavy use of matrix notation, singularity problem make the use of this transformation technique rather difficult. For the resulting CT transfer function a suitable filter structure should be found. Starting from a known CT filter structure the coefficient can be determined easily from the CT to DT transformation. For this method to succeed, the CT filter structure should have sufficient degrees of freedom to implement the required DT transfer function. When the coefficients of the CT are found, a suitable implementation of CT loop filter can be designed [4].

The method above only deals with loop filter equivalence, which affects the noise transfer function in the linearized delta sigma model. There are some subtleties concerning the signal transfer function [8], where signal transfer function is simply assumed to be equal to a gain of one in the signal band. Actually the assumption is approximate for most design. And the difference between the signal transfer function of CT loop and DT loop can be compensated by another filter.

A rough design methodology for single loop, one bit (bandpass) delta sigma modulator with a continuous time loop filter can be extracted [4]:

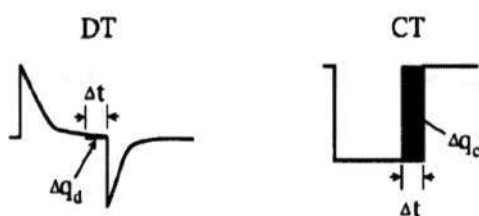
1. Define the design goal (such as tuning frequency) and performance target (i.e. SNR, power consumption and bandwidth).
2. Determine the oversampling ratio and order of loop filter using theoretical estimates of the achievable dynamic range and possible power consumption limitations on the sampling frequency.
3. Design the DT loop filter such that the  $\Delta\Sigma\text{M}$  is small-signal stable. The poles of the loop filter determine the in-band gain and tuning frequency. The zeros of the

loop filters determine the stability of the modulator.

4. Determine the equivalent DT loop filter of a CT loop filter structure having sufficient degrees of freedom, Note that the pulse shape of the DAC can have a considerable influence on the equivalent DT loop filter transfer function.
5. Match the designed DT filter transfer function with the equivalent DT loop filter transfer function and solve the CT loop filter coefficients.
6. Determine a suitable implementation of the CT loop filter.

### 3.2 Clock Jitter

CT  $\Delta\Sigma$ Ms generally suffer more degradation from clock jitter than that of DT  $\Delta\Sigma$ Ms. As sampling frequency increases, clock jitter becomes an even more important consideration for the design of high-resolution converters. [9]



**Figure 3. 3 Clock jitter effect in DT versus CT design**

Suppose there is timing jitter in the quantizer clock (clock jitter). On the left-hand side of Fig. 3.3, a typical feedback current waveform for a switched-capacitor DT  $\Delta\Sigma$ M is depicted. Most of the charge transfer occurs at the start of the clock period, so that the amount of charge lost  $\Delta q_d$  due to a timing error is relatively small. By contrast, the right-hand side of Fig. 3.3 shows the Non-Return-to-Zero (NRZ)/ Return-to-Zero

(RZ) DAC output current in a CT  $\Delta\Sigma$ M; here, charge is transferred at a constant rate over a clock period, and so charge loss  $\Delta q_c$  from the same timing error is a larger proportion of the total charge. Moreover, in a DT design, jitter in the input sample-and-hold (S/H) clock means only the input waveform is affected. In a CT design, the sampling occurs at the quantizer rather than the input, which means the jitter affects the sum of the input plus quantization noise—a signal with considerably more power than the input alone. Hence, CT  $\Delta\Sigma$ Ms are more sensitive to clock jitter than DT designs [10].

Clock jitter causes a slight random variation in the amount of charge fed back per clock cycle. Put another way, it is akin to adding a random phase modulation to the output bit stream. In an oversampling converter, the spectra of the output stream is very noisy outside the (narrow) signal band; a random phase modulation causes the noise outside the signal band to fold into the signal band, raising the converter noise floor and degrading its resolution.

### 3.2.1 Clock Jitter in Continuous-Time Delta-Sigma Modulators

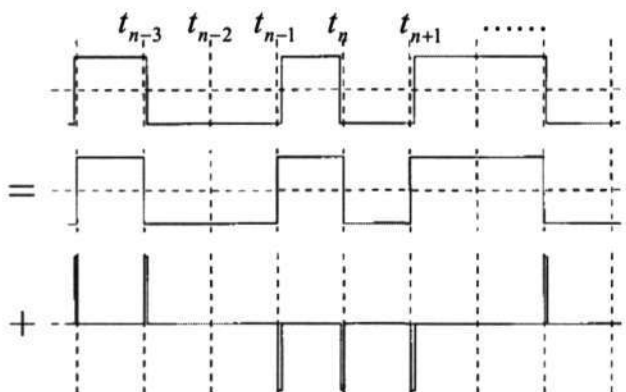


Figure 3. 4 Equivalent representations of a jittered bit stream

This problem has been studied in [9][10]. Suppose the sampling times for  $N$  output bits are given by

$$t_n = nT_s + \beta_n, \quad n = 0, 1, \dots, N-1, \quad (3.18)$$

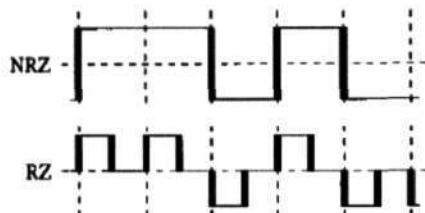
and for the moment, let  $\beta_n$  be variables with variance  $\sigma_t^2$ . The effect of jitter in an NRZ modulator can be explained by considering Fig. 3.4. The output bit stream with jitter shown in the top diagram is equivalent to the sum of an unjittered bit stream (the middle diagram) and a stream of pulses, which we call the error sequence, resulting from the jitter (the bottom diagram). By the linearity of the Fourier transform, the output spectrum for the top signal must be equal to the sum of the spectra of the bottom two signals. The error sequence can be represented by

$$e_{NRZ}(n) = [y(n) - y(n-1)] \frac{\beta_n}{T_s}. \quad (3.19)$$

The theoretical SNR limit due to sampling a signal at an intermediate frequency  $f_{IF}$  with a NRZ jittered DAC is [9]:

$$SNR_{NRZ} = 10 \log_{10} \frac{\sqrt{OSR}}{2\pi\sigma_t f_{IF}}. \quad (3.20)$$

Some  $\Delta\Sigma$ Ms eschew NRZ DAC pulses for RZ pulses to reduce problems caused by unequal DAC edge rise and fall times; although a differential architecture gets around these problems because differential signals are inherently symmetric [11]. Error sequence energy in different types of modulator is different and shown in Fig. 3.5.



**Figure 3. 5 Error sequence energy in different types of modulator**

We may distinguish the two cases as follows:

- 1) In an NRZ modulator, jitter only matters when the output changes sign; the error sequence  $e_{NRZ}$  is nonzero only at those times.
- 2) In an RZ modulator, both the rising and the falling edge of the pulse occur every clock cycle, so jitter affects a total of  $2N$  edges. The energy is being transferred over only half a cycle;  $\sigma_j^2$  is therefore twice as large relative to the energy transfer period in an NRZ modulator

Generally, clock jitter affects RZ modulators more severely than modulators employing just NRZ feedback. A good rule of thumb is: jitter noise will be 6 dB (1 bit) worse in the band of interest [10].

### 3.2.2 Techniques to Reduce the Clock Jitter in CT $\Delta\Sigma$ M

Besides using a precise clock and PLL to achieve low clock jitter, there are also several published techniques used to reduce the clock jitter sensitivity in CT  $\Delta\Sigma$ Ms.

### 1. Reduced Timing Jitter Sensitivity Based On SC DAC Feedback

A modified switched capacitor feedback structure was proposed by *Ortmanns* [12] in 2001 and implemented by *Veldhoven* in 2003 [13] to reduce the sensitivity to time jitter.

As mentioned before, the DT  $\Delta\Sigma$ Ms are less sensitive to the clock jitter than the CT  $\Delta\Sigma$ Ms. So a SC DAC feedback is used instead of the switched-current DAC feedback; the feedback current is similar to the waveform on the left-hand side of Fig.3.3, and the CT modulator still implies the intrinsic anti-aliasing filter.

The SC DAC circuit used in [13] is illustrated in detail in Fig.3.6. On the other hand the required bandwidth and slew-rate (SR) of the filter integrators have to be much higher due to the very fast SC-signal pulse, canceling some of the advantage of the CT modulator.

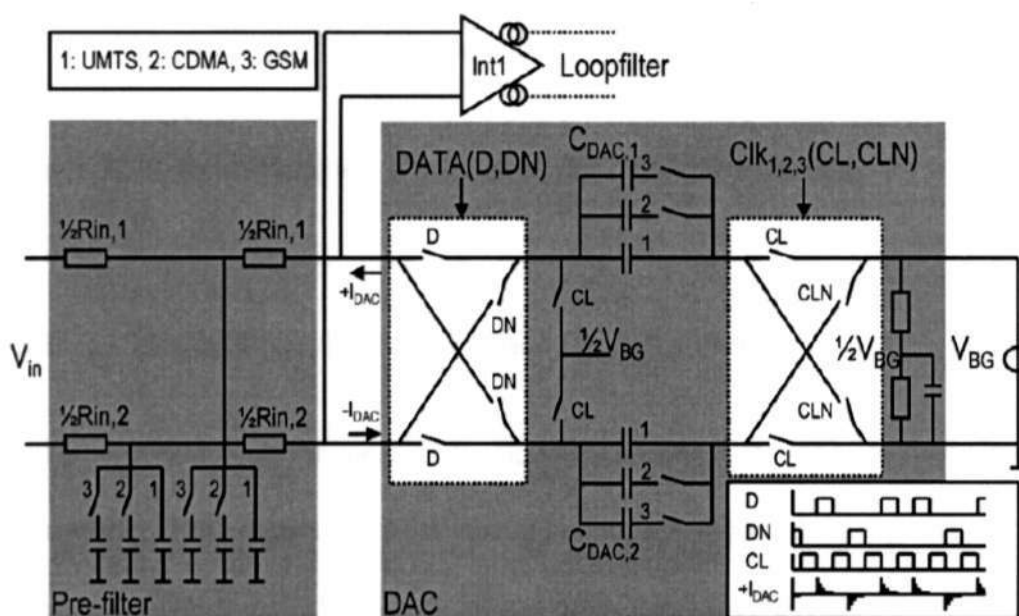
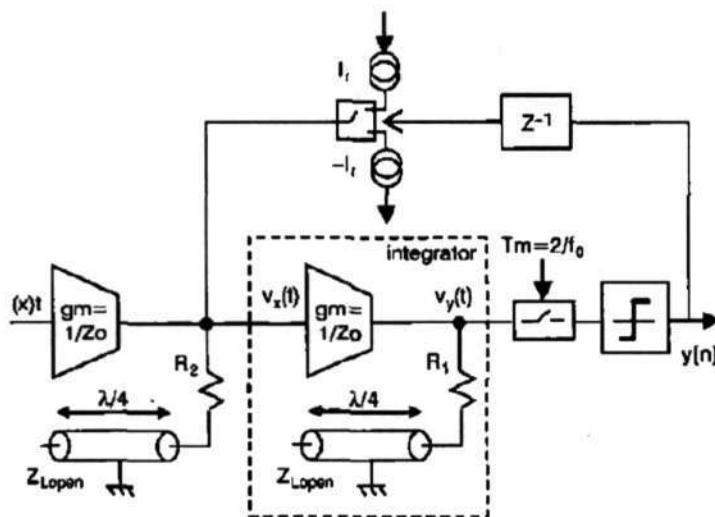


Figure 3. 6 Input filter and SC feedback DAC in [13]

## 2. Reduced Timing Jitter Sensitivity Based On Time Delays

[14] proposed an alternative to integrated capacitors employing passive resonators implemented with transmission lines as depicted in Fig. 3.7. This architecture employs a noise-shaping filter for the clock jitter based on the *continuous time delay*. For signals well below its cutoff frequency, a properly loaded transmission line behaves as a linear-phase four pole with nearly constant attenuation. The error introduced by the time jitter is shaped by the NTF of the modulator. However, due to low operational frequency, the passive-element has to be implement *off-chip*.

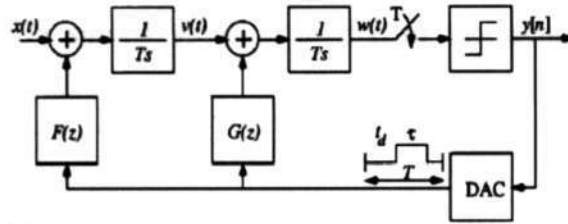


**Figure 3. 7 Circuit diagram of second-order delta-sigma modulator based on transmission lines in [14]**

## 3. Reduced Timing Jitter Sensitivity Based On FIR Filter

A  $\Delta\Sigma$ M with spectrally shaped feedback was discussed in [15]. A finite-impulse response filter (FIR) is used in the feedback path of a low-pass delta-sigma modulator in order to combat the clock jitter. A second-order  $\Delta\Sigma$ M incorporation two FIR filters in its feedback is depicted in Fig.3.8. The FIR filter are defined in terms of their  $(L+1)$

coefficients as  $F(Z) = \sum_{l=0}^L f_l z^{-l}$  and  $G(Z) = \sum_{l=0}^L g_l z^{-l}$ . The filter corresponding to the first integrator is a lowpass filter which smoothes out the feedback waveform by attenuating the high frequency quantization and reduces the sensitivity to the clock jitter.



**Figure 3. 8 Second-order continuous-time modulator with FIR filters in its feedback path in [15]**

The improvement in reducing the jitter sensitivity is offered by  $F(z)$  and the other filters are required to ensure the stability of the system.

The magnitude of  $F(z)$ 's frequency response is :

$$F(e^{j\omega}) = \frac{1}{L+1} \frac{\sin\left(\frac{(L+1)\omega}{2}\right)}{\sin\left(\frac{\omega}{2}\right)}. \quad (3.21)$$

For a continuous-time modulator without FIR filter, the power spectral density of noise is [16]:  $S_e(e^{j\omega}) = (\sigma_\tau^2 / \tau^2)$ . Where  $(\tau \rightarrow \tau + \delta_\tau)$  is the duration of the feedback DAC. Therefore,  $F(z)$  makes the noise spectrum signal-depend. If the input signal is a sine-wave  $x(t) = A \cos(2\pi f_0 t)$ , then with the  $F(z)$ , the spectral density of noise is:

$$S_e(e^{j\omega}) = \left( \frac{\sigma_\tau^2}{\tau^2} \right) \left\{ \frac{A^2}{2} \left( \frac{1}{L+1} \right) \frac{\sin\left(\frac{(L+1)\omega_0}{2}\right)}{\sin\left(\frac{\omega_0}{2}\right)} + \theta \right\}, \quad (3.22)$$

Where  $\Theta$  is a function of  $L$  and input signal and can be negligible compared with  $\frac{A^2}{2} \left( \frac{1}{L+1} \right) \frac{\sin\left(\frac{(L+1)\omega_0}{2}\right)}{\sin\left(\frac{\omega_0}{2}\right)}$ . Therefore, the comb filter attenuates the noise by a factor of  $\frac{A^2}{2} \left( \frac{1}{L+1} \right) \frac{\sin\left(\frac{(L+1)\omega_0}{2}\right)}{\sin\left(\frac{\omega_0}{2}\right)}$ . This FIR filter feedback is implemented in switched-capacitor circuit. Hence some of the advantages of CT modulators are offset by the use of SC FIR filter, a similar situation as that of the technique using SC DAC feedback.

#### 4. Reduced Timing Jitter Sensitivity Based On Pulse Shaped DAC

A pulse shaped DAC is proposed which decreases clock jitter sensitivity [17]. The DAC pulse is depicted in Fig.3.9 for a single bit DAC. The pulse is at the same frequency as the sampling clock ( $\omega_s=2\pi/T$ ) and is given by (3.23)

$$I_{DAC} = A_I (1 - \cos(\omega_s t)) \tag{3.23}$$

If the raised cosine wave is ideal and locked to the clock, the clock will act on the feedback pulse when it has a zero value. First and second-order insensitivity to clock jitter are expected since the pulse has both zero value and zero slope at the sampling instants of  $\pm kT$ .

In [17], the author analyzes the error source of pulse shaped DAC:

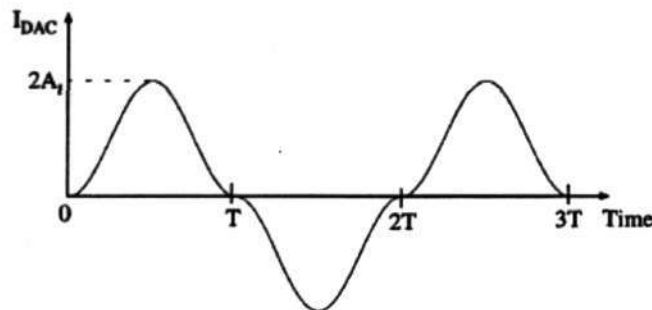


Figure 3. 9 Shaped DAC pulse in [17]

*A: Ideal locking*

Suppose the raised cosine feedback pulse is ideal and perfectly locked to the DAC clock. The only source of error is then jitter in the feedback DAC clock. Integrating  $I_{DAC}$  over a period gives the amount of charge fed back in one cycle

$$q_f = A_I \int_{t_0}^{T+\tau(t_T)} (1 - \cos(\omega_s t)) dt . \quad (3.24)$$

Where  $\tau(t_0)$  and  $\tau(t_T)$  are the values of the clock jitter at  $t = 0$  and  $T$ , respectively, and  $A_I$  is the amplitude of the raised cosine feedback pulse. The nominal value of the integral in eq. (3.24) is  $A_I T$  when  $\tau(t_0)$  and  $\tau(t_T)$  are zero. Assume  $\tau(t_0)$  and  $\tau(t_T)$  are zero-mean Gaussian uncorrelated random variables with variance  $\sigma_t^2$ . The SNR limit can be computed by approximating the input charge as half the value of the nominal feedback pulse  $A_I T / 2$  to avoid overloading the modulator. So the SNR is limited by the DAC clock jittering according to:

$$SNR = 20 \log_{10} \frac{\sqrt{OSR}}{7.3 \pi^2 f_s^3 \sigma_t^3} \quad (3.25)$$

*B. Locking Error*

A locking error of  $t_0$  between the sampling clock edge and  $I_{DAC}$  is depicted in Fig.3.10. The feedback waveform is sampled at an offset  $t_0$  from the zero crossings of the  $I_{DAC}$  waveform. This creates two sources of error that could degrade SNR. The first is the static offset, or “excess loop delay”. The second is the clock jitter acting on the nonzero waveform.

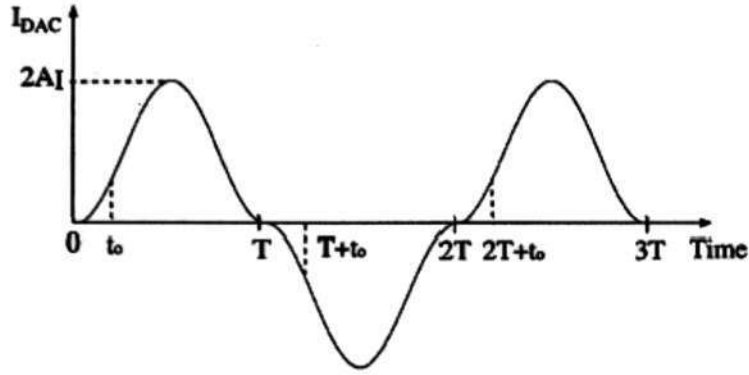


Figure 3. 10 Static locking error in shaped DAC pulse

Suppose the clock is offset from the feedback pulse by a constant value of  $t_0$  as shown in Fig.3.10. The fed-back charge is given by

$$q_f = A_I \int_{t_0 + \tau(t_0)}^{T + t_0 + \tau(t_f)} (1 - \cos(\omega_s t)) dt . \quad (3.26)$$

The SNR limit is:

$$SNR \approx 20 \log_{10} \frac{\sqrt{OSR}}{56 \sigma_t f_s \left(\frac{t_0}{T}\right)^2} . \quad (3.27)$$

### C. Phase Noise

Phase noise is the nonideality in the raised cosine feedback pulse itself. The feedback charge  $q_f$  with only phase noise in the raised cosine feedback pulse is given by

$$q_f = A_I \int_0^T (1 - \cos(\omega_s t + \phi(t))) dt . \quad (3.28)$$

The error in  $q_f$  due to phase noise is then

$$E_q = A_I \int_0^T -\cos(\omega_s t + \phi(t)) dt . \quad (3.29)$$

Assuming that the phase noise spectrum is flat with an amplitude of  $A$  at frequencies near an offset of  $\omega_s$  away from the carrier. It can be shown that the SNR limit due to phase noise in the feedback pulse is not dependent on  $f_{IF}$  or  $f_s$ . It is only dependent on the amplitude of the phase noise and the bandwidth of the signal  $f_b$ .

$$SNR \approx 20 \log_{10} \frac{1}{2\sqrt{Af_b}}. \quad (3.30)$$

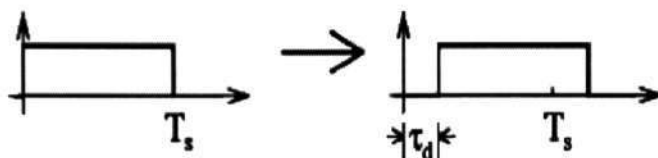
The effects of jitter in a conventional CT  $\Delta\Sigma$ M with a square NRZ feedback pulse, and a CT  $\Delta\Sigma$ M with the raised cosine-shaped feedback pulse were compared in [17]. The SNR was compared for a  $f_{IF} = f_s / 4$  BP converter with a bandwidth 40 MHz. The phase noise amplitude,  $A$ , was 150 dBm with a 7 dBm carrier, and the standard deviation of the jitter was 0.7 ps<sub>rms</sub>. These values were chosen as typical numbers from current state-of-the-art. For these typical clock jitter and oscillator phase noise numbers, the raised cosine feedback pulse had a better performance than the conventional CT  $\Delta\Sigma$ M above  $f_{IF} = 20\text{MHz}$ .

### 3.3 Excess Loop Delay

#### 3.3.1 Excess Loop Delay in Continuous-Time $\Delta\Sigma$ Ms

A real quantizer does not make a decision instantaneously [6]: the quantizer is a regenerative circuit with finite regeneration gain. A quantizer input close to zero volt, will therefore take longer to resolve. Furthermore, DAC has a nonzero switching

time. The important quantity in a CT  $\Delta\Sigma$ M is the excess loop delay, which is defined as the total delay between the sampling clock edges of the DAC output.



**Figure 3. 11 Illustration of excess loop delay on NRZ DAC pulse**

As shown in Fig.3.11, loop delay has the effect of shifting the DAC pulse in time such that an NRZ pulse is delayed by  $\tau_d$ . This changes the mapping between continuous and discrete domains.

In general, if the loop delay causes the DAC pulse to extend beyond  $T_s$ , then the modulator order increase by one [18]. It was proved that one pole of the noise transfer function will move out of the unit cycle after a certain excess loop delay for the second-order lowpass (38%), second order bandpass (58%) and fourth-order bandpass (22%) modulators. This means that excess loop delay may eventually make a CT  $\Delta\Sigma$ M unstable [5].

### 3.3.2 Compensation for Excess Loop Delay

#### A. DAC Pulse Selection [6]

Assume that a perfect rectangle DAC pulse has a magnitude of 1 and lasts from  $\alpha$  to  $\beta$ , ie.,

$$r_{(\alpha,\beta)}(t) = \begin{cases} 1, & \alpha \leq t \leq \beta, 0 \leq \alpha \leq \beta \leq 1 \\ 0, & \text{otherwise.} \end{cases} \quad (3.31)$$

If we were to use DAC pulses with  $\beta < 1$ , then the pulses would extend past only if the condition

$$\tau_d > 1 - \beta. \quad (3.32)$$

This suggests that if we used an RZ DAC instead of an NRZ DAC, the modulator remain stable for  $\tau_d \leq 0.5$  for a lowpass modulator.

Thus, for a given  $\tau_d \leq 0.5$  and RZ DAC pulse, we can make the  $H(s)$  match exactly the desired  $H(z)$  by tuning the parameter in  $H(s)$  for a known excess loop delay.

### B. Feedback Coefficient Tuning [5]

To obtain the correct equivalent discrete-time loop transfer functions with some excess loop delay. A topology that adds an extra feedback as shown in Fig.3.12 provides a full degree of freedom to approach this. Tuning the pulse-shaping coefficients would result in a match between the desired prototype transfer function and the actually realized loop transfer function. With an amount of excess loop delay  $\tau_d$  added in the delta-sigma feedback loop, the resultant equivalent discrete-time transfer function using the modified Z-transform is

$$H_l(z, m) = \sum_{i=1}^l k_{ai} Z_m \left[ L^{-1} \left[ DAC_a(s) \cdot \hat{H}^i(s) \right]_{t=nT} \right] + k_{ai} Z_m \left[ L^{-1} \left[ DAC_b(s) \cdot \hat{H}^i(s) \right]_{t=nT} \right], \quad (3.33)$$

where  $m = 1 - \tau_d$ .

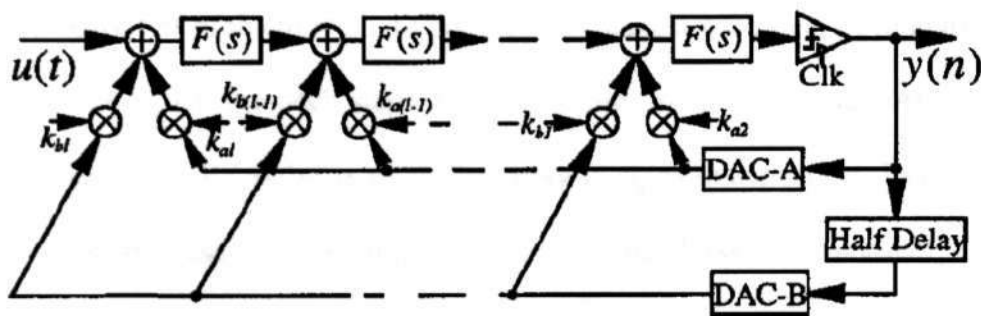


Figure 3. 12 Block diagram of multi-feedback  $\Delta\Sigma M$  in [5]

C. Additional Latch Stage

A third method we can try is to use additional latching stage after the internal ADC as shown in Fig 3.13 [19], [20]. This architectural solution eliminates performance degradation due to the nonzero excess loop delay and signal-dependent delay of the internal ADC (quantizer). Or, in other words, the nonzero excess loop delay is accommodated in the architecture level design.

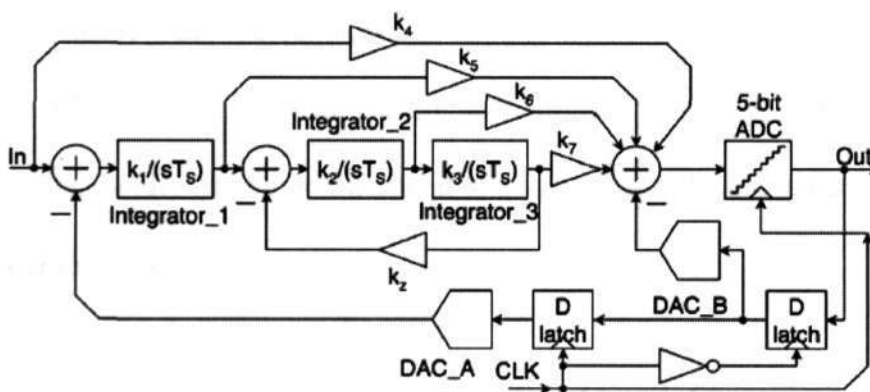


Figure 3. 13 Block diagram of continuous-time multibit  $\Delta\Sigma M$  architecture in [20]

The compensations using RZ DAC or feedback coefficient tuning are all based on the well-estimated excess loop delay. However, because the delay in the quantizer is signal dependent. So it is difficult to estimate a very accurate loop delay. The additional

latch can solve this problem well, giving previous stage a good deal of time to settle. The drawback is that the latch stage does not absorb the delay in the DAC. For the delay in DAC, if a RZ pulse is used, the delay is signal-independent. Even a NRZ pulse is used, because the sampling frequency of a bandpass  $\Delta\Sigma$  normally is only four times of the IF and the output will almost always be switching. The delay is close to a signal-independent delay and an accurate delay can be estimated. Hence using RZ DAC or feedback coefficient tuning mentioned above can solve this drawback and compensate for the predictable delay in DAC.

### 3.4 Subsampling in Continuous-Time $\Delta\Sigma$

Normally for bandpass  $\Delta\Sigma$ , the sampling frequency is four times the center frequency, resulting in a very high sampling frequency. Actually the IF input can be sampled at a much lower rate because narrowband signal exhibits only a small change from one carrier cycle to the next. Called “subsampling”, the idea is that a bandpass signal with bandwidth  $\Delta f$  can be translated to a lower band if sampled at a rate equal to or greater than  $2\Delta f$  [21].

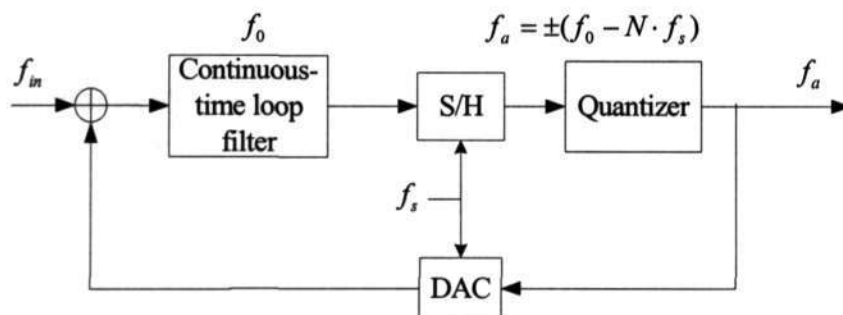


Figure 3. 14 Block diagram of Subsampling CT  $\Delta\Sigma$

The concept of subsampling a CT bandpass  $\Delta\Sigma\text{M}$  was introduced by *Gourgue* [24]. The basic idea of subsampling a CT bandpass  $\Delta\Sigma\text{M}$  is to subsample with respect to the center frequency of a narrow-band input signal and to oversample with respect to the bandwidth of the input signal. Fig. 3.14 depicts the basic scheme of a subsampling CT modulator.

The operation of the subsampling CT  $\Delta\Sigma\text{M}$  can be explained by constructing the resulting spectra of the signals inside the  $\Delta\Sigma\text{M}$  (see Fig. 3.15) with no aliasing. The  $\Delta\Sigma\text{M}$  is sampled at a rate  $f_s$ . The loop filter of the bandpass  $\Delta\Sigma\text{M}$  is tuned to a frequency of  $f_0 > f_s/2$ . When an input signal with frequency  $f_{in}$  close to  $f_0$  is applied to the modulator, it will pass through the loop filter and will be sampled by the coarse ADC (quantizer). As a result, the input signal will be aliased to a frequency  $f_a$ :

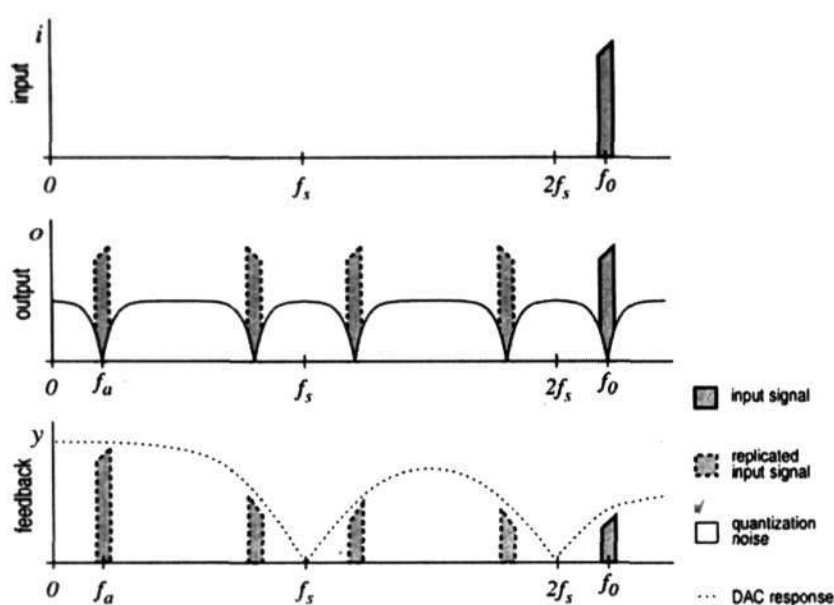
$$f_a = \pm(f_{in} - N \cdot f_s), \quad (3.34)$$

with  $N$  an integer such that  $f_a \in [0, f_s/2]$ . The factor  $N$  will be called the subsampling factor. The output spectra will contain replicated versions of the input signal spectra and the shaped quantization noise of the coarse quantizer. The output signal is filtered by the hold-function of the DAC, resulting in the feedback signal. In Fig.3.15 an NRZ pulse shape is assumed for the DAC. In that case the feedback signal is equal to the output signal filtered by:

$$R(f) = T_s \frac{\sin(\pi f T_s)}{\pi f T_s}. \quad (3.35)$$

The key to the operation of the subsampled CT  $\Delta\Sigma\text{M}$  is that the DAC output spectra repeats at multiples of the sample frequency. Unfortunately, the filtering operation by

the hold function of the DAC severely affects the efficiency of the feedback loop. This is particularly true for high subsampling factors. Theoretically, the loop filter can compensate the loss of gain caused by the hold function. However, the reduced output power of the DAC at  $f_0$  causes a reduction of the maximum possible input signal amplitude. In the case that the (in-band) system noise exceeds the (in-band) quantization noise, the performance of the modulator depends on the absolute maximum input signal amplitude. A reduction of the maximum input amplitude will result in a reduction of the maximum SNR, of the modulator.

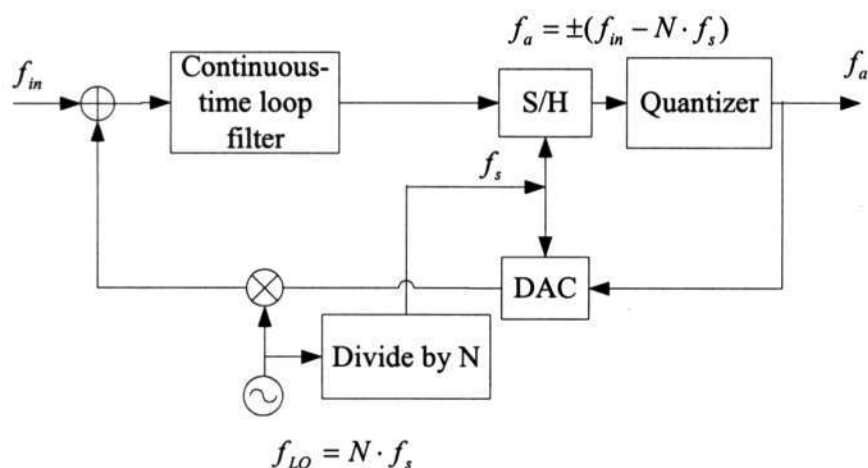


**Figure 3. 15 Signal spectra in a subsampling CT  $\Delta\Sigma$ M**

*Gourgue* suggested a solution to the loss of gain of the DAC at high frequencies by modulating (mixing) the feedback signal  $f_a$  with a carrier as depicted in Fig. 3.16. By modulating the feedback signal, the large amplitude replica of the input signal at  $f_a$ , is upconverted to  $f_{in}$ , thereby increasing the efficiency of the DAC at the frequency  $f_{in}$  and increasing the maximum possible input amplitude. As the mixer is placed within the feedback loop after the DAC, any additional distortion introduced

by the mixer will add directly to the distortion in the output of the  $\Delta\Sigma$ . A  $\Delta\Sigma$  employing subsampling and on-chip Q-enhanced LC filter was implemented by *Hussein* in 2000 with this structure [22].

Owing to the large reduction in the downconversion rate, the use of subsampling can simplify the design of analog-to-digital converter. Despite these features subsampling suffers from an important drawback: aliasing of noise. It can be proved that subsampling by a factor of  $N$  multiplies the downconverted noise power of the sampling circuit by a factor  $2N$  [21] and multiplies the clock phase noise power by  $N^2$  [23].



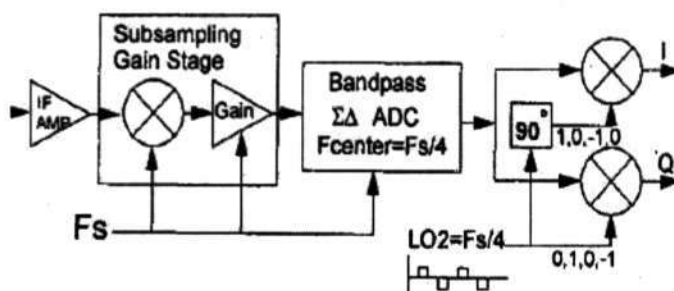
**Figure 3. 16** Block diagram of the subsampling CT  $\Delta\Sigma$ M in [24]

### 3.5 Architectures with Mixers/Subsampling in $\Sigma\Delta$ Loop

Most of these conventional bandpass  $\Delta\Sigma$  architecture is that the sampling frequency is four times the IF and very little architecture is 1.25 times the IF [25]. This results in a very high sampling rate. The process used on those  $\Delta\Sigma$ s are expensive and sampling at these high frequencies increase the complexity and power consumption of the digital signal processing stage. Thus, in an attempt to address these problems, the subsampling  $\Delta\Sigma$  proposed by Gourgue [24] presented a theoretical study of a useful architecture which downconverts the IF signal by subsampling. The described design operates at a 10.7MHz IF with a sampling frequency of 4.71MHz, converting the IF to discrete time bandpass signal centered at 1.28MHz. The DAC feedback path incorporates a mixer and a local oscillator at 9.42MHz to upconvert the discrete-time bandpass signal back into the loop filter's passband. A block diagram of the modulator is shown in Fig.3.16. As discussed in section 3.4, the distortion introduced by the mixer in the feedback path will add directly to the distortion in the output of the  $\Delta\Sigma$ . However, the noise introduced in the subsampling S/H is suppressed by the loop transfer function.

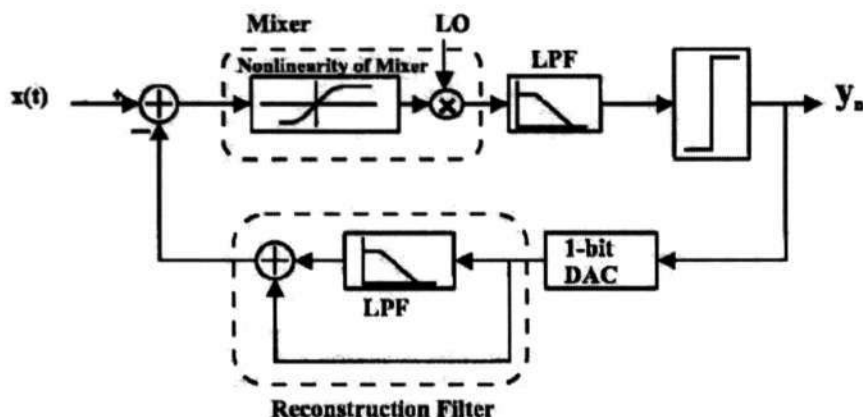
In order to downconvert the IF signal and reduce the sampling frequency. Some  $\Delta\Sigma$ s with built-in mixer or subsampling S/H before the input of the loop were proposed. An 81-MHz IF receiver was proposed by *Hairapetian* in 1996 [26]. Due to the IF sampling nature, the receiver is immune to DC offset, flicker noise and errors due to mismatches between  $I$  and  $Q$ . As depicted in Fig.3.17, the receiver contains an IF amplifier, downconversion subsampling stage and a bandpass  $\Delta\Sigma$ , the 81MHz IF is downconverted to 3.25MHz by a sampling frequency 13MHz with 62dB SNR. In

1997 [27] reported an extremely low-power, lowpass  $\Delta\Sigma$  in which the input could operate at a 10MHz IF. This architecture used a subsampling S/H circuit as a mixer and passive switched-capacitor filter for the loop filter of  $\Delta\Sigma$  to lower the power consumption. Because the subsampling S/H will introduce more noise than conventional S/H, circuit noise is dominated by the sum of the noise generated in the subsampling stage for these two  $\Delta\Sigma$ s.



**Figure 3. 17 Block diagram of the 81MHz receiver in [26]**

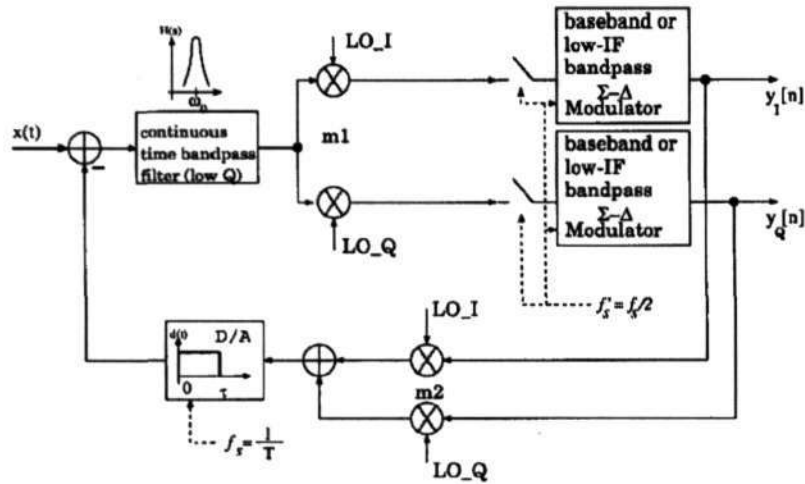
In 1999 [28], a 400MHz IF digitizer based on embedding a down-conversion mixer in the forward path of  $\Delta\Sigma$  together with a reconstruction filter in the feedback path was developed (Fig. 3.18). In order to downconvert the IF frequency and suppress the distortions introduced by the subsampling S/H or mixer, the mixer is placed inside the loop, and a reconstruction filter is used in the feedback path to suppress the distortions in the mixer. The modulator was implemented in a  $0.8\mu\text{m}$  BiCMOS and achieved a measured resolution of 12 bits for a 40kHz bandwidth with sampling frequency of 20MHz. The problem of this design is that the replica having a frequency equal to the input frequency is severely attenuated by the DAC in the feedback loop, as we have discussed before.



**Figure 3. 18 Block diagram of the  $\Delta\Sigma$  using a down-conversion mixer in the forward path together with a reconstruction filter in the feedback path [28]**

Continuous-time bandpass  $\Delta\Sigma$  modulator using frequency down-conversion in the forward path of the loop and frequency up-conversion in the feedback path was given in 1999 [29]. A block diagram of this modulator is given in Fig.3.19. The motivations for such a design described by the authors are:

- To avoid the front-end S/H as in a DT modulator, the sampling operation is placed inside the feedback loop, and it is preceded by a CT bandpass filter in a conventional CT modulator to suppress the S/H distortion.
- If such a filter has high  $Q$  ( $>100$ ), as in conventional designs, it will be difficult to control the  $Q$ , and the center frequency errors will be problematic. Thus a relatively low- $Q$  filter is chosen.
- Since the aforementioned CT loop filter has low  $Q$ , it does not adequately suppress quantization noise; so another discrete-time filter at low center frequency is used.



**Figure 3. 19 Block diagram of the  $\Delta\Sigma$ M using a down-conversion mixer in the forward path and frequency up-conversion in the feedback path [29]**

The modulator was implemented in 0.35 $\mu$ m CMOS process to convert a 200kHz bandwidth signal at a 100MHz IF frequency with a sampling frequency of 400MHz. The achieved peak SNR is 54dB which falls far from the 98dB prediction based on simulations of the ideal behavioral model. The disadvantage of this design is the complexity of the hardware. It required two baseband or low-IF  $\Delta\Sigma$ M inside the modulator and four mixers.

A detail analysis of the CT bandpass  $\Delta\Sigma$ M based on subsampling of the IF signal was given by *Hussein* [22] in 2000. Transfer functions with infinite Q bandpass filter were derived for the mixed signal system. The analysis shows that the loop transfer function can be made equivalent to the typical DT bandpass  $\Delta\Sigma$ M by changing the phase of the local-oscillator signal. The modulator operates at a 195MHz IF with a bandwidth of 150kHz and a sampling frequency of 20MHz. The CT loop filter is implemented using an on-chip LC resonator with Q enhanced circuit in a 1.2 $\mu$ m

CMOS process. Because an  $N=10$  subsampling factor is used, the requirement for the CT loop filter is very high which will be discussed in next chapter.

An 80MHz bandpass  $\Delta\Sigma$ M for 100MHz IF receiver was proposed in 2003 [30]. The circuit was targeted for a 100MHz IF and operates at a sampling frequency of 80MHz. It combines frequency downconversion with analog-to-digital conversion by directly subsampling an input signal from the IF of 100MHz to a digital IF of 20MHz. The measured peak SNRs are 80dB and 42dB for a bandwidth of 270 kHz and 3.84 MHz respectively. The circuit is implemented with 0.35 $\mu$ m CMOS process. The subsampling factor  $N$  is only one, so the sampling frequency is still close to the IF. But the noise aliasing in the subsampling S/H is minimized.

In 2003 [31], a pure continuous-time  $\Delta\Sigma$ M using frequency down-conversion in the forward path of the loop and frequency up-conversion in the feedback path was reported. The architecture is depicted in Fig. 3.20 (only one path of  $I/Q$  is depicted). The IF signal, after passing through a low  $Q$ , wideband bandpass filter, is downconverted to baseband. The downconverted IF signal is fed to a CT, second-order, low pass  $\Delta\Sigma$ M. The output of the lowpass  $\Delta\Sigma$ M is upconverted and feedback to the low  $Q$  filter. However, due to the structure of the modulator and low  $Q$  wideband bandpass filter, the noise shaping for noise introduced by the mixer in the forward path is very low. This means this modulator suffers both the noise introduced in the mixer in forward path and mixer in the feedback path. The more analysis will be given in Chapter 4.

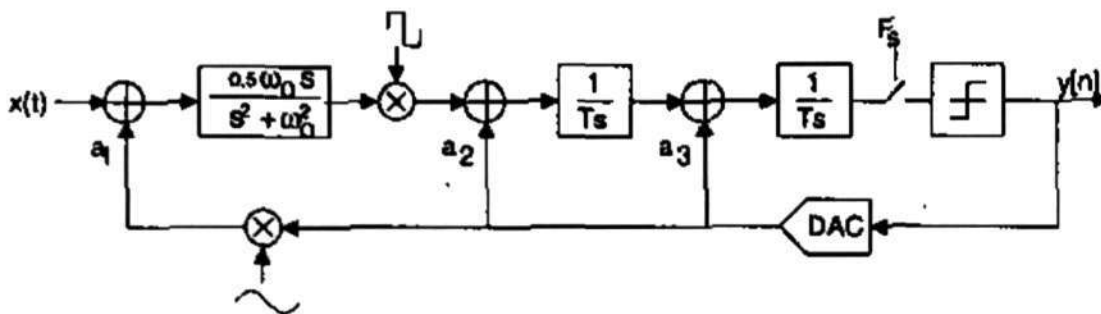


Figure 3. 20 Diagram of the CT, frequency-translation bandpass  $\Delta\Sigma M$  in [31]

A behavioral simulation of a fourth-order multi-bit continuous-time bandpass  $\Delta\Sigma M$  for direct RF conversion was proposed in 2004 [32]. Fig. 3.21 shows the structure of this  $\Delta\Sigma M$ . The 2.1GHz carrier frequency is down converted to 0.7GHz after subsampled by 2.8GHz.

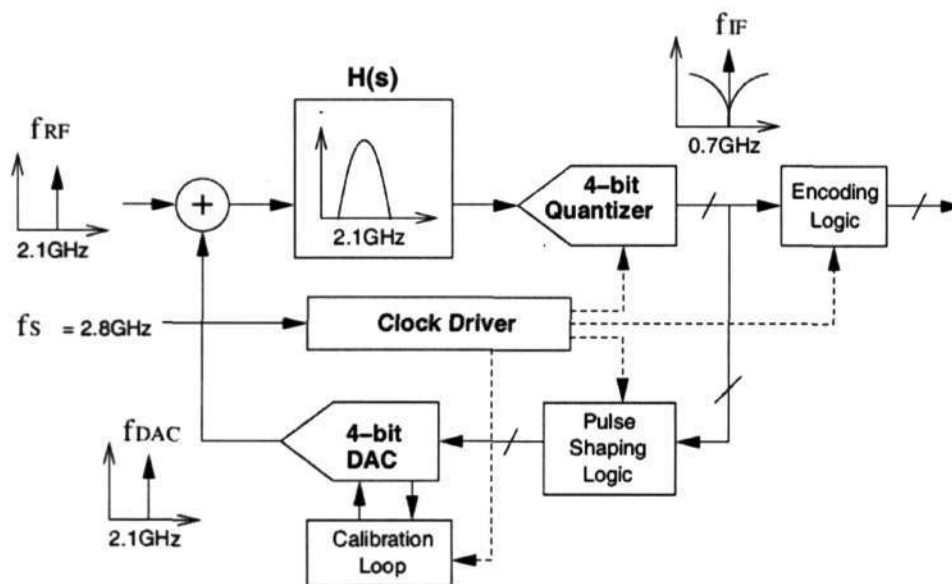
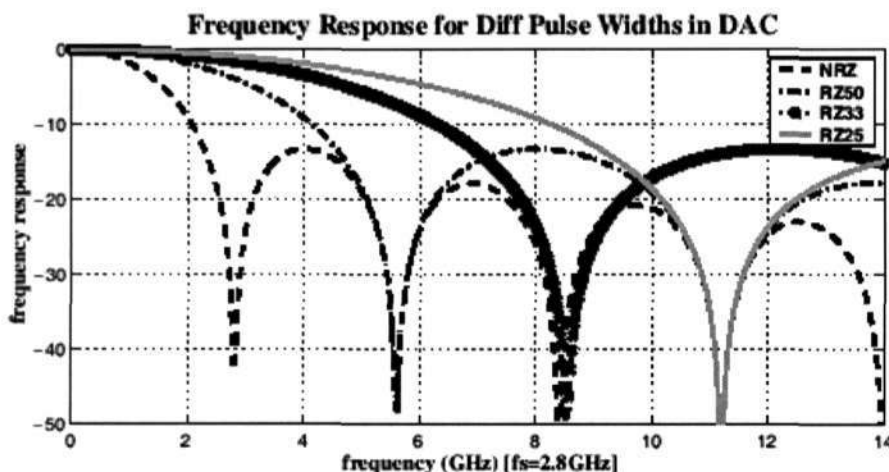


Figure 3. 21 Block diagram of the CT bandpass  $\Delta\Sigma M$  in [32]

A RZ-33% (33% pulse width) DAC is used in the feedback to increase the DAC output power in 2.8GHz as depicted in Fig. 3.22. This solution is only effective when

the subsampling factor is very small; such as in this  $\Delta\Sigma$ M, the subsampling factor is one.



**Figure 3.22** Frequency plots of NRZ/RZ with different pulse width

As mentioned in [32], the continuous-time filter is implemented with a Gm-Opamp-C biquad structure. Actually it is difficult to build a Gm-Opamp-C biquad structure filter centered at 2.1GHz and the performance of this filter will be further degraded by the effect of subsampling which will be discussed in Chapter 4.

## References

- [1] D.B. Ribner, "Multistage Bandpass Delta Sigma Modulators," IEEE Trans. Circuit and System II, Vol. 41, No. 6, Jun. 1994, pp. 402 – 405.
- [2] D.W. Groeneveld, "A Self-Calibration Technique for Monolithic High-Resolution D/A Converters," IEEE Journal of Solid-State Circuits, Vol.24, No. 6, Dec. 1999, pp. 1517 – 1522.
- [3] S. Tao, "Mismatch Shaping for a Current-Mode Multibit Delta-Sigma DAC," IEEE Journal of Solid-State Circuits, Vol. 34, No. 3, Mar. 1999, pp. 331 –338 .

- [4] J.V. Engelen, "Bandpass Sigma Delta Modulators," Kluwer Academic Publishers, 1999.
- [5] W. Gao and O. Shoaie, "Excess Loop Delay Effects in Continuous-Time Delta-Sigma Modulators and Compensation Solution," IEEE International Symposium on Circuits and Systems, Vol. 1, Jun. 1997, pp. 65-68.
- [6] J.A. Cherry and W.M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," IEEE Trans. Circuits and Systems II, Vol. 46, No. 4, Apr. 1999, pp. 376-389.
- [7] F. M. Gardner, "A Transformation for Digital Simulation of Analog Filters," IEEE Trans. Communications, Vol. 44, No. 7, Jul. 1986, pp. 676-680.
- [8] O. Shoaie and W.M. Snelgrove, "Design and Implementation of a Tunable 40 MHz-70MHz Gm-C Bandpass  $\Delta\Sigma$  Modulator," IEEE Trans. Circuits and Systems II, Vol. 44, No. 7, Jul. 1997, pp. 521-530.
- [9] H. Tao and J.M. Khoury, "Analysis of Timing Jitter in Bandpass Sigma-Delta Modulators," IEEE Trans. Circuits and Systems II, Vol. 46, No. 8, Aug. 1999, pp. 991 - 1001.
- [10] J.A. Cherry and W.M. Snelgrove, "Clock Jitter and Quantizer Metastability in Continuous-Time Delta-Sigma Modulators," IEEE Trans. Circuits and Systems II, Vol. 46, No. 6, Jun. 1999, pp. 661-676.
- [11] J.F. Jensen, G. Raghavan and A.E. Cosand, "A 3.2-GHz Second-Order Delta-Sigma Modulator Implemented in InP HBT Technology," IEEE

- Journal of Solid-State Circuits, Vol. 30, No. 10, Oct. 1995, pp. 1119–1127.
- [12] M. Ortmanns and F. Gerfers, “Clock Jitter Insensitive Continuous-Time  $\Sigma\Delta$  Modulators,” IEEE International Conference on Electronics, Circuits and Systems, Vol. 2, Sep. 2001, pp. 1049-1052.
- [13] R.H.M. Veldhoven, “A Trip-Mode Continuous-Time  $\Sigma\Delta$  Modulator With Switched-Capacitor Feedback DAC for a GSM-EDGE/CDMA2000/UMTS Receiver,” IEEE Journal of Solid-State Circuits, Vol. 38, No. 12, Dec. 2003, pp. 2096-2076.
- [14] L. Hernandez, “Continuous-time Sigma-Delta Modulators with Reduced Timing Jitter Sensitivity Based On Time Delays,” IEE Electronics Letters, Vol. 39, No. 14, Jul. 2003, pp. 1039-1041.
- [15] O. Oliaei, “Sigma-Delta Modulator with Spectrally Shaped Feedback,” IEEE Trans. Circuits and System II, Vol. 50, No. 9, Sep. 2003, pp. 518-530.
- [16] O. Oliaei, “State-Space Analysis of Clock Jitter in Continuous-Time Oversampling Data Converters,” IEEE Trans. Circuits and System II, Vol. 50, No. 1, Jan. 2003, pp. 31-37.
- [17] S. Luschas and H.S. Lee, “High-Speed Sigma Delta Modulators with Reduced Timing Jitter Sensitivity,” IEEE Trans. Circuits and Systems II, Vol. 49, No. 11, Nov. 2002, pp. 712-720.
- [18] O. Oliaei, “Continuous-Time Delta-Sigma A/D Converters for High Speed Applications,” PhD These, Carleton University, 1995.

- [19] M.S. Kappes, "A 2.2-mW CMOS Bandpass Continuous-Time Multibit Delta Sigma ADC with 68 dB of Dynamic Range and 1-MHz Bandwidth for Wireless Applications," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 7, Jul. 2003, pp. 1089-1104.
- [20] S. Yan, "A Continuous-Time Sigma Delta Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE Journal of Solid-State Circuits*, Vol. 39, No. 1, Jan. 2004, pp. 75-86.
- [21] B. Razavi, "RF Microelectronics," Prentice Hall PTR, 1998,
- [22] A.I. Hussein and W.B. Kuhn, "Bandpass  $\Delta\Sigma$  Employing Undersampling of RF Signals for Wireless Communication," *IEEE Trans. Circuit and System II*, Vol. 47, No. 7, Jul. 2000, pp. 614-620.
- [23] D.H. Shen, "A 900-MHz RF Front End With Integrated Discrete-Time Filters," *IEEE Journal of Solid-State Circuits*, Vol.31, No. 12, Dec. 1999, pp. 1945-1954.
- [24] F.Gourgue and Mbellanger, "A Bandpass Subsampled Delta-Sigma Modulator for Narrowband Cellular Mobile Communications," *IEEE International Symposium on Circuits and Systems*, Vol. 5, Jun. 1997, pp. 353-356.
- [25] P. Cusinato and D. Tonietto, "A 3.3-V CMOS 10.7-MHz Sixth-Order Bandpass  $\Sigma\Delta$  Modulator with 74-dB Dynamic Range," *IEEE Journal of Solid-State Circuits*, Vol.36, No. 4, Apr. 1999, pp. 629-638.
- [26] A. Hairapetian, "An 81-MHz IF Receiver in CMOS," *IEEE International Symposium on Circuits and Systems*, Vol. 31, Dec. 1996, pp. 1981-1986.

- [27] F. Chen and B. Leung, "A 0.25-mW Low-pass Passive Sigma-Delta Modulator with Built-in Mixer for a 10-MHz IF Input," *IEEE Journal of Solid-State Circuits*, Vol.32, No. 6, Jun. 1997, pp. 774-782.
- [28] A.Namdar and B.H.Leung, "A 400MHz, 12-bit, 18-mw, IF Digital with Mixer Inside a Sigma-Delta Modulator Loop," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 12, Dec. 1999, pp. 1765-1776.
- [29] H. Tao and J.M. Khoury, "A 400-Ms/s Frequency Translating Bandpass Sigma-Delta Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 34, No. 12, Dec. 1999, pp. 1741-1752.
- [30] T. Salo and S. Lindfors, "A 80-MHz Bandpass  $\Delta\Sigma$  Modulator for a 100-MHz IF Receiver," *IEEE Journal of Solid-State Circuits*, Vol.38, No. 7, Mar. 2003, pp. 464-474.
- [31] A. Pulincherry and M. Hufford, "Continuous-Time, Frequency Translating, Bandpass Delta-Sigma Modulator," *IEEE International Symposium on Circuits and Systems*, Vol. 1, May. 2003, pp. 1013-1016.
- [32] U.V. Koc and J. Lee, "Direct RF Sampling Continuous-Time Bandpass Delta Sigma A/D Converter Design for 3G Wireless Applications," *IEEE International Symposium on Circuits and Systems*, Vol. 1, May. 2004, pp. 409-412.
- [33] R. Schreier and B. Zhang, "Delta-Sigma Modulators Employing Continuous-Time Circuitry," *IEEE Trans. Circuits and Systems I*, Vol. 43, No. 4, Apr. 1996, pp. 324-332.

# Chapter 4

## Subsampling Bandpass Delta-Sigma Modulators

### 4.1 Transfer Function Derivation with Finite Q Bandpass Filter

The transfer function derivation with infinite Q bandpass filter for subsampling bandpass  $\Delta\Sigma$ M was analyzed in [1]. However, infinite Q bandpass filter is impractical and the effect of the finite Q will be more pronounced due to the subsampling operation. Hence the analysis of the transfer function derivation with finite Q bandpass filter is important.

#### 4.1.1 Z-domain Loop Transfer function

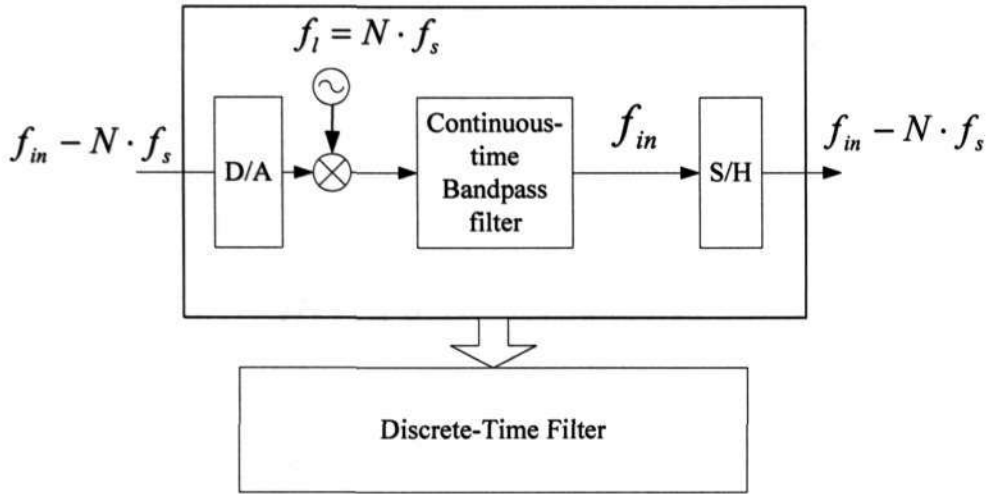
For the subsampling  $\Delta\Sigma$ M depicted in Fig.3.16, from the DAC in the feedback to the S/H is internally a discrete-time system as shown in Fig.4.1.

The relationship between the sampling frequency  $f_s$ , local oscillator frequency  $f_l$  and the centre frequency of the continuous-time bandpass filter (IF)  $f_0$  are:

$$f_l = N \cdot f_s \quad (4.1)$$

$$f_0 = (N - 0.25) \cdot f_s \quad (4.2)$$

Where  $N$  is the subsampling factor.



**Figure 4. 1 Open Loop subsampling  $\Delta\Sigma$ M**

A general continuous-time bandpass is given as :

$$\hat{H}(s) = \frac{A(s-B)}{s^2 + s\omega_0/Q + \omega_0^2}, \quad (4.3)$$

where A is a constant gain factor and AB is the coefficient for  $s^0$  in the numerator. For each output of the S/H which is discrete in nature, the output of the NRZ DAC is a rectangular pulse of width  $T_s$ , which can be described by the difference of two unit step functions

$$DAC(t) = u(t) - u(t - T_s) \quad (4.4)$$

The local oscillator signal is  $\sin \omega_l t$  and the mixer output is the multiplication of the NRZ DAC output and the local oscillator signal

$$M(t) = \sin \omega_l t [u(t) - u(t - T_s)] \quad (4.5)$$

This can be transformed to the s-domain as

$$M(s) = \frac{\omega_l}{s^2 + \omega_l^2} \cdot (1 - e^{-sT_s}). \quad (4.6)$$

Using eq. (3.2), the equivalent DT transfer function from the DAC to S/H is then

Chapter 4 Subsampling Bandpass  $\Delta\Sigma$  Modulators

$$H(z) = ZL^{-1}\left[\frac{A(s-B)}{s^2+s\omega_0/Q+\omega_0^2} \cdot \frac{\omega_1}{s^2+\omega_1^2} \cdot (1-e^{-sT_s})\right]. \quad (4.7)$$

Solving eq.(4.7), when  $Q \gg 1$

$$H(z) \approx g_t \cdot \frac{-k_1 z^{-1} - k_2 z^{-2}}{1 + a^2 z^{-2}}. \quad (4.8)$$

Where

$$g_t = A \frac{\omega_1}{\omega_1^2 - \omega_0^2} \quad (4.9)$$

$$a = e^{-\frac{\omega_0 \cdot T_s}{2Q}} \quad (4.10)$$

$$k_1 \approx 1 - \frac{aB}{\omega_0} \quad (4.11)$$

$$k_2 \approx \frac{aB}{\omega_0} + a^2 \quad (4.12)$$

For the conventional CT bandpass  $\Delta\Sigma$ M without subsampling,  $f_0 = 0.25 f_s$ , then

$$a = a_1 = e^{-\frac{2\pi f_s}{8Q} \frac{1}{f_s}} = e^{-\frac{\pi}{4Q}}. \quad (4.13)$$

For the subsampling bandpass  $\Delta\Sigma$ M, substituting eq. (4.2) into eq. (4.10) yields:

$$a = a_2 = e^{-\frac{2\pi f_s (N-0.25)}{2Q} \frac{1}{f_s}} = e^{-\frac{\pi(N-0.25)}{Q}} \quad (4.14)$$

Rewriting eq. (4.14)

$$a_2 = e^{-\frac{\pi(N-0.25)}{Q}} = e^{-\frac{\pi}{4Q^*}} \quad (4.15)$$

Where

$$Q^* = \frac{Q}{4(N-0.25)}. \quad (4.16)$$

The relationship between  $Q^*$  and  $Q$  shows that after subsampling, the effect of the continuous-time bandpass filter with a Q-factor of  $Q$  working at an IF of  $f_0$  is equal to the effect of a continuous-time bandpass filter working at a frequency of  $f_s/4$  with an effective Q-factor of  $Q^*$ , and the Q-factor is reduced by a factor of  $\frac{1}{4(N-0.25)}$ . The filter with a Q factor of  $Q^*$  is the effective filter providing the zeros for the noise transfer function of quantization noise and subsampling noise.

In [1], a subsampling factor of  $N=10$  is used, this implies that the Q factor of the equivalent bandpass filter working at an IF= $f_s/4$  will be scaled by a factor of  $1/39$ . *Hussein* analyzes the z-domain transfer function when the CT bandpass filter having an infinite Q. When the Q is infinite, the effect of the subsampling is not obvious, so the simulation result appears acceptable. However, the assumption of infinite Q is impractical, and no measured result was reported in [1].

#### 4.1.2 Matching the Z-Domain Loop Transfer Function to DT Bandpass $\Delta\Sigma$ Loop Transfer Function

Using the design methodology discussed in section 3.1.3. We want the  $H(z)$  in eq. (4.8) to approach the particular DT bandpass  $\Delta\Sigma$ , for a second-order bandpass  $\Delta\Sigma$ , which is :

$$H(z) = \frac{-gz^{-2}}{1+gz^{-2}}. \quad (4.17)$$

$g=1$ , when the Q of the loop filter is infinite.

*A. Changing the Z-domain loop transfer function by changing the local-oscillator signal*

[1] introduced a way of changing the z-domain loop transfer function by changing the local-oscillator signal. In the previous analysis, the local-oscillator signal was represented by  $\sin \omega_l t$ . In general, it can be considered  $\sin(\omega_l t + \theta)$  and eq. (4.5) becomes

$$M(t) = \sin(\omega_l t + \theta)[u(t) - u(t - T_s)] \quad (4.18)$$

$$M(s) = \left[ \cos \theta \frac{\omega_l}{s^2 + \omega_l^2} + \sin \theta \frac{\omega_l}{s^2 + \omega_l^2} \right] \cdot (1 - e^{-sT_s}) \quad (4.19)$$

Assuming that CT bandpass filter is the ideal LC bandpass filter used in [1]:

$$\hat{H}(s) = \frac{As}{s^2 + \omega_0^2} \quad (4.20)$$

Using eq. (3.2), the new equivalent DT transfer function from the DAC to S/H is then

$$H(z) = ZL^1 \left[ \left( \frac{As}{s^2 + \omega_0^2} \right) \left( \cos \theta \frac{\omega_l}{s^2 + \omega_l^2} + \sin \theta \frac{\omega_l}{s^2 + \omega_l^2} \right) (1 - e^{-sT_s}) \right] \quad (4.21)$$

From eq. (4.21) and by using the relationship given by eq. (4.1) and (4.2), the z-domain loop transfer function in this case is

$$H(z) \approx g_1 \cdot \frac{-g_1 z^{-1} - g_2 z^{-2}}{1 + z^{-2}} \quad (4.22)$$

where

$$g_1 \approx -\cos(\theta) + c \sin(\theta) \quad (4.23)$$

$$g_2 \approx \cos(\theta) + c \sin(\theta) \quad (4.24)$$

and  $c = \omega_l / \omega_0$ .

When  $\theta = \pi / 4$ , since  $c = \omega_1 / \omega_0$  is very close to 1,  $g_1$  is very small with respect to  $g_2$ , and z-transfer function in eq. (4.22) approaches the particular DT bandpass  $\Delta\Sigma$  loop transfer function, when  $g_1 \cdot g_2 = -1$ .

### *B. Changing the Z-domain loop transfer function by choosing bandpass filter structure*

Another way to change the z-domain loop transfer function is choosing a bandpass filter that has sufficient freedom to match the typical DT bandpass  $\Delta\Sigma$  transfer function such as a Gm-C filter with proper structure [2] [3]. For the general CT bandpass filter in eq.(4.3), from the eqs. (4.8)-(4.12), it can be seen that when  $B = \omega_0 / a$ , (4.8) equals to:

$$H(z) \approx g_t \cdot \frac{-(1+a^2)z^{-2}}{1+a^2z^{-2}} \quad (4.25)$$

By scaling the gain of  $H(z)$ ,  $H(z)$  can match the particular DT bandpass  $\Delta\Sigma$  transfer function.

## **4.2 The Proposed Subsampling Bandpass $\Delta\Sigma$**

The noise shaping performance is degraded drastically for effective Q less than 20 [4]. The low Q of the filter causes the noise transfer function to flatten out in the center of the passband, resulting in poorer noise shaping.

As discussed in section 4.1.1, the effective Q of the CT bandpass filter reduces to  $Q^*$  because of subsampling. So for the subsampling  $\Delta\Sigma$  in [1], using eq.(4.16), if the effective CT bandpass filter working at an IF frequency of  $f_s/4$  has a Q-factor  $Q^*$  equal to 20, then the Q of CT bandpass filter working at 195MHz IF should have  $Q = Q^* \cdot 4(N - 0.25) = 20 \cdot 4(10 - 0.25) = 740$ . Such a high Q is not practical for an on-chip bandpass filter. Another way to get a  $Q^*$  greater than 20 with a reasonable Q CT bandpass filter center at 195MHz is to choose a small N. If  $N=1$  and  $Q^* = 20$ , then the Q should be 60. By using eq. (4.2), the sampling frequency  $f_s$  will be 267MHz, still a very high frequency for  $N=1$ . For small N, the advantage of subsampling is decreasing.

For these reasons, the subsampling  $\Delta\Sigma$  using a structure in [1] is not so suitable when the modulator is tuned to IF signals at high frequency such as 70MHz. It is difficult to design a low noise, linear, high Q ( $Q>100$ ) CT bandpass filter. When the Q is not very high, the effective equivalent CT bandpass filter working at an IF frequency  $f_s/4$  with a much lower  $Q^*$  cannot suppress quantizer noise adequately.

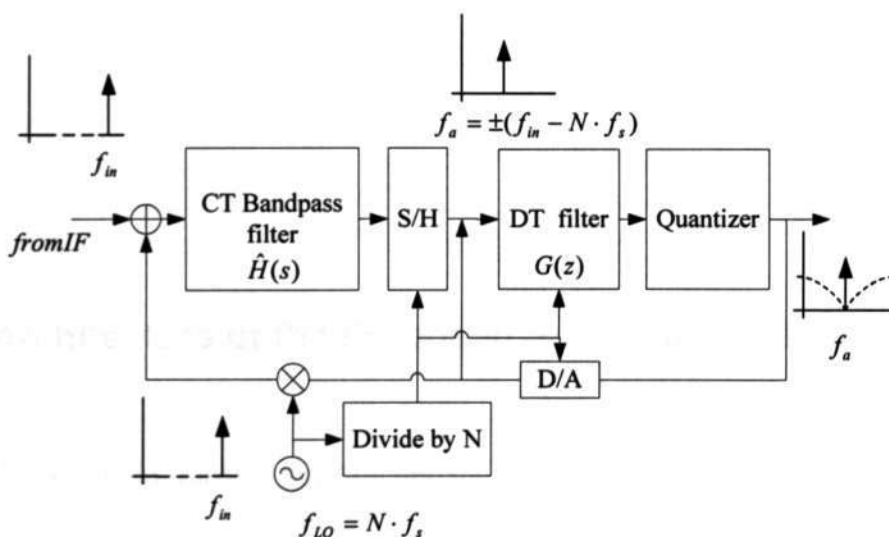
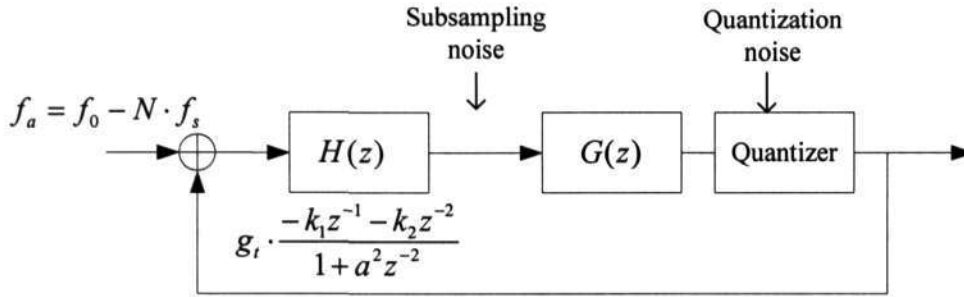


Figure 4. 2 Block diagram of the proposed subsampling  $\Delta\Sigma$ M

To solve this problem, a new subsampling  $\Delta\Sigma$ M is proposed. The modulator is operating at 70MHz IF under 18.667MHz sampling frequency (subsampling factor  $N=4$ ) with 200kHz bandwidth. The 70MHz IF was down-converted to 4.667MHz by subsampling. The block diagram is depicted in Fig.4.2. A DT filter follows a relatively moderate-Q (e.g.  $Q=60$ ) CT bandpass filter to give additional noise shaping for the quantization noise. As discussed in section 3.5, if the subsampling S/H is in front of the  $\Delta\Sigma$ M, because the subsampling S/H will introduce more noise than conventional S/H, circuit noise is dominated by the sum of the noise generated in the subsampling stage. In the proposed  $\Delta\Sigma$ M, the subsampling operation is inside the loop, after the CT bandpass filter. Although the relatively moderate-Q CT bandpass filter cannot provide enough noise shaping for the quantization noise, it can suppress the noise introduced by subsampling under the quantization noise with a suitable  $Q$  and subsampling factor  $N$ . Different from the modulator in [5], after subsampling, the IF signal was down-converted to a lower IF instead of down-converting to baseband by mixer. So it does not need  $I$  and  $Q$  signals processing paths, thus reducing the circuit complexity and avoiding the  $I/Q$  mismatch problem.

### 4.2.1 Architecture of the Proposed Subsampling $\Delta\Sigma$ M

Using the Z-domain transfer function derived in section 4.1.1 the equivalent DT  $\Delta\Sigma$ M that operates at  $f_s/4$  is depicted in Fig.4.3:



**Figure 4. 3 Equivalent DT subsampling  $\Delta\Sigma$ M**

The transfer function can be derived as:

$$Y(z) = STF(z)X(z) + NTF_q(z)N_q(z) + NTF_s(z)N_s(z), \quad (4.26)$$

where  $X(z)$  is the input signal;  $Y(z)$  is the output signal;  $N_q(z)$  is quantization noise and  $N_s(z)$  is the subsampling noise;  $STF(z)$  is the signal transfer function ;  $NTF_q(z)$  is the quantitation noise transfer function and  $NTF_s(z)$  is subsampling noise transfer function.

### 4.2.1.1 The order of the Subsampling bandpass $\Delta\Sigma$ M

The order of the proposed  $\Delta\Sigma$ M is the order of the equivalent DT transfer function from the DAC in the feedback to the S/H  $H(z)$  as shown in Fig.4.1 plus the order of the following DT filter  $G(z)$ . The order of the  $H(z)$  is two and it introduces one zero fixed at  $z = j(1/a)$  to  $NTF_q$ . Because the Q factor of the CT bandpass filter is finite, then  $a > 1$  and this zero is inside the unit circle. Hence the noise shaping of the  $NTF_q$  is mainly determined by the zeros on the unit circle introduced by  $G(z)$ . In order to achieve high SNR and at the same time keep the modulator stable, a fourth-order  $G(z)$  is chosen. Thus the CT and DT filter work together to achieve a sixth-order bandpass loop filter.

### 4.2.1.2 Bandpass $\Delta\Sigma$ Ms structures

Many different single-stage structures are available for bandpass  $\Delta\Sigma$ Ms, the conventional structures include cascade-of-resonator in feedback (CRFB) and cascade-of-resonator in feedforward (CRFF).

For the subsampling  $\Delta\Sigma$ Ms, the noise shaping for both quantization noise and subsampling noise are important. To achieve a better noise shaping in both the S/H and quantizer noises, two different  $\Delta\Sigma$ Ms are compared. Their equivalent DT  $\Delta\Sigma$ Ms are depicted in Fig.4.4 (CRFB) and Fig.4.5 (CRFF); the CT bandpass filter is supposed to be ideal and all the zeros of  $NTF_q$  are at  $z=0+lj$  to simplify the analysis.

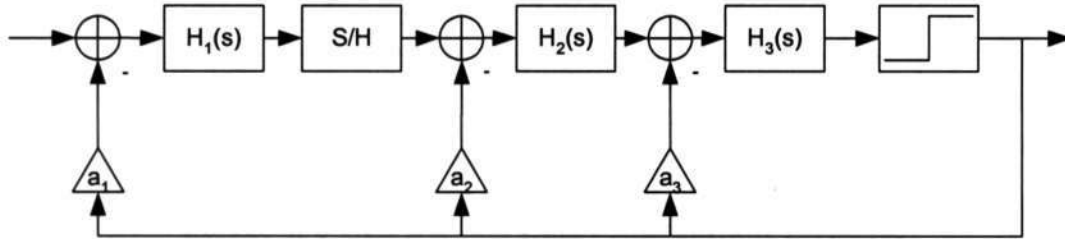


Figure 4. 4 Equivalent DT subsampling CRFB  $\Delta\Sigma$ M

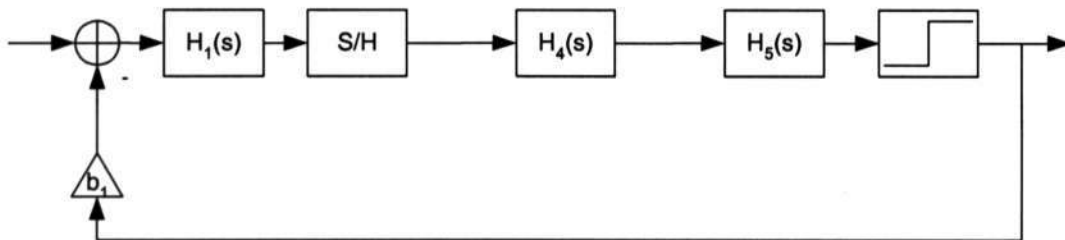


Figure 4. 5 Equivalent DT subsampling CRFF  $\Delta\Sigma$ M

Chapter 4 Subsampling Bandpass  $\Delta\Sigma$  Modulators

Both the  $NTF_q$  of these two modulators with CRFB and CRFF structures are the same, matching the optimized sixth-order  $NTF_q$  [6]. The inband rms gain of the  $NTF_q$  is -53dB as shown in Fig.4.6.

$$NTF_q = \frac{(1 + z^{-2})^3}{(1 + 0.7532z^{-2})(1 - 0.4385z^{-1} + 0.8988z^{-2})(1 + 0.4385z^{-1} + 0.8988z^{-2})} \quad (4.27)$$

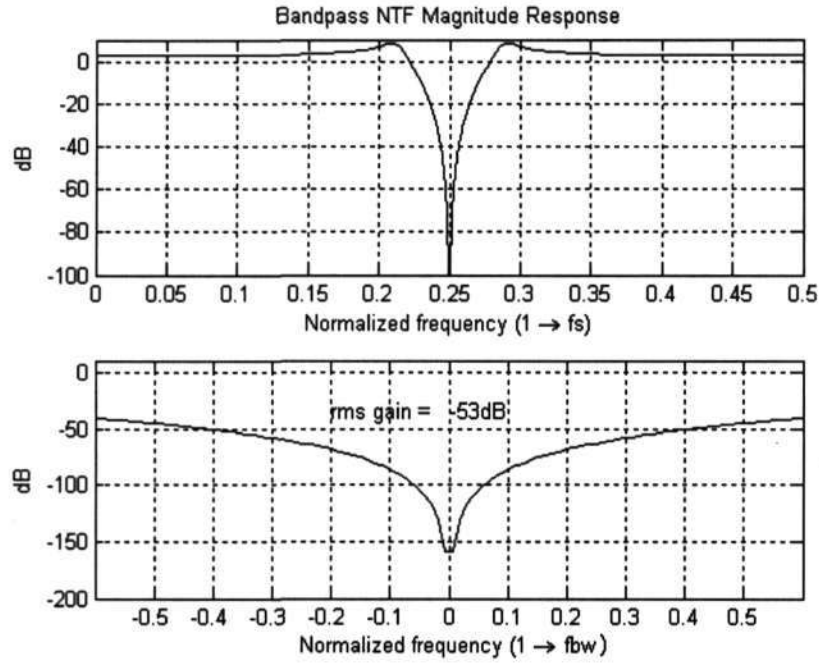


Figure 4. 6 CRFB&CRFF  $NTF_q$  magnitude response

Although the  $NTF_q$  of these two modulators are the same, their  $NTF_s$  are different due to the different structure.

The  $NTF_s$  of the CRFB modulator is:

$$NTF_s(CRFB) = \frac{(1 + z^{-2})}{(1 + 0.7532z^{-2})(1 - 0.4385z^{-1} + 0.8988z^{-2})(1 + 0.4385z^{-1} + 0.8988z^{-2})} \quad (4.28)$$

The  $NTF_s$  of the CRFF modulator is:

$$NTF_s(CRFF) = \frac{0.6416(1 + 0.1734z^{-1} + 0.7812z^{-2})(1 - 0.1734z^{-1} + 0.7812z^{-2})(1 + z^{-2})}{(1 + 0.7532z^{-2})(1 - 0.4385z^{-1} + 0.8988z^{-2})(1 + 0.4385z^{-1} + 0.8988z^{-2})} \quad (4.29)$$

Chapter 4 Subsampling Bandpass  $\Delta\Sigma$  Modulators

The inband rms gains of the  $NTF_s(\text{CRFB})$  and  $NTF_s(\text{CRFF})$  are  $-2\text{dB}$  and  $-28\text{dB}$ , respectively, as depicted in Fig.4.7 & Fig.4.8.

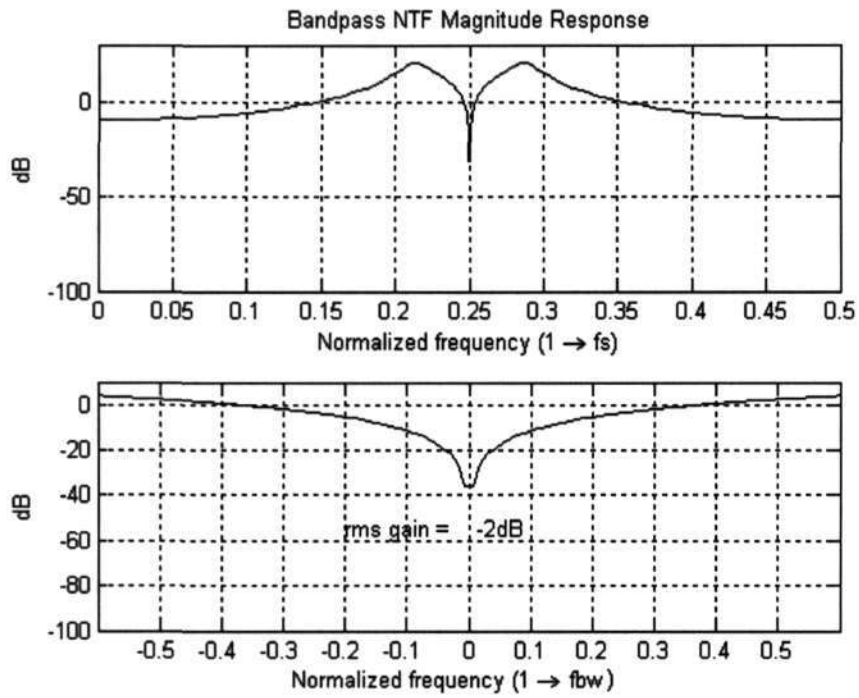


Figure 4. 7 CRFB  $NTF_s$  magnitude response

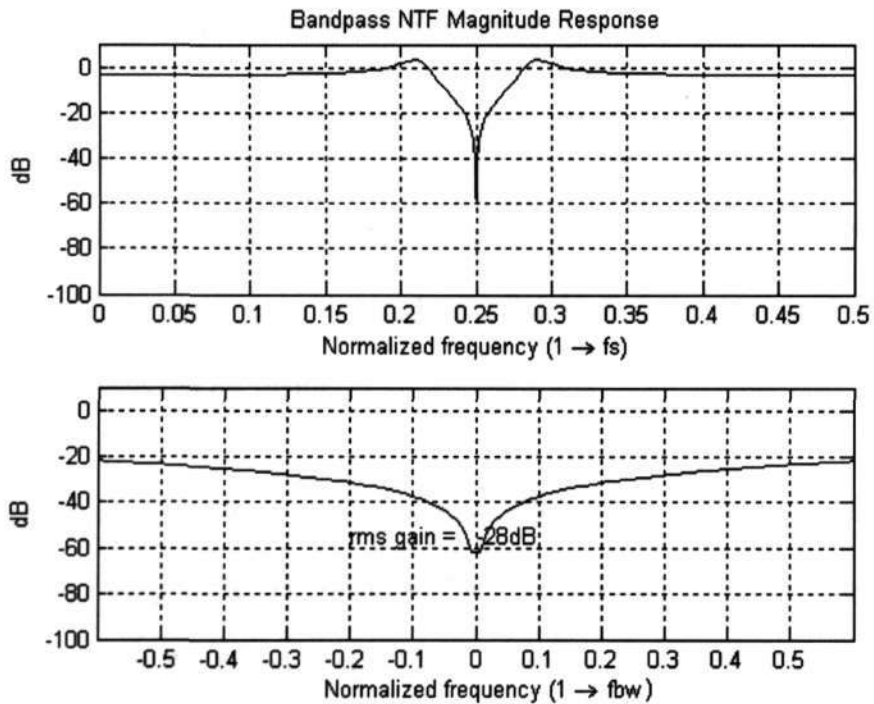


Figure 4. 8 CRFF  $NTF_s$  magnitude response

The modulator using CRFF structure provides much more noise shaping for the subsampling noise than the modulator using CRFB structure. It is because the  $NTF_s(\text{CRFB})$  only has one zero at the DC and  $NTF_s(\text{CRFF})$  has another two zeros inside the unit circle besides the zero at the DC. The effect of these two zeros become more important when the Q factor of the CT filter is finite. Because when the Q factor is finite, the zero provide by the CT filter will also be inside the unit circle.

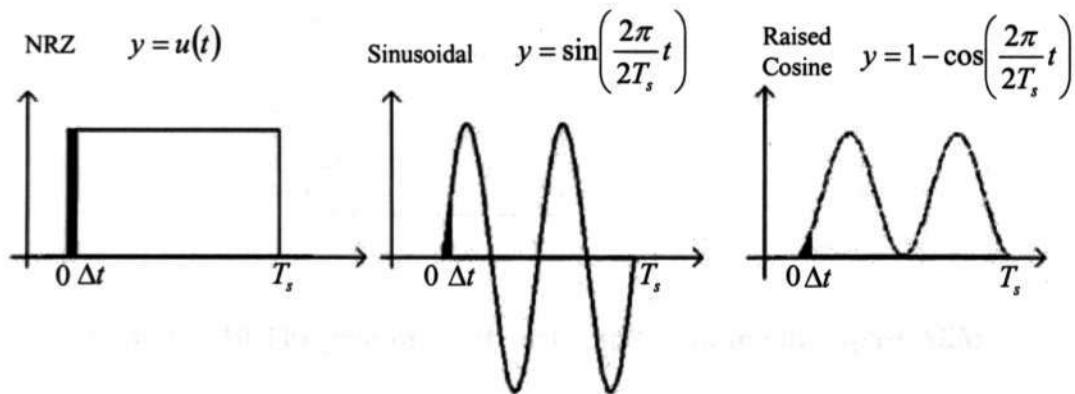
So the subsampling  $\Delta\Sigma\text{M}$  using CRFF structure is more suitable for the subsampling application. It provides more noise shaping for the subsampling noise than the  $\Delta\Sigma\text{M}$  using CRFB structure when the noise shaping for the quantization noise of these two  $\Delta\Sigma\text{M}$ s are the same.

### 4.2.2 Local-Oscillator Signal & Clock Jitter

As the mixer is placed within the feedback loop after the DAC, any additional distortion introduced by the mixer will add directly to the distortion at the output of the  $\Delta\Sigma\text{M}$ . But at the same time, the modulator can be less sensitive to the DAC jitter by mixing with selected oscillator.

The mixer is used in the proposed subsampling  $\Delta\Sigma\text{M}$  to up-convert the signal frequency. By using different local-oscillator signal, the mixer can form a pulse shaped DAC [7] as the raised cosine DAC discussed in section 3.2.2 to reduce the clock jitter sensitivity.

The jitter effect with different local-oscillator signal is shown in Fig.4.9. It has been proved that the raised cosine DAC is less sensitive to clock jitter than the conventional DAC having a rectangle pulse like the NRZ DAC [8]. If a sinusoidal oscillator is used in the mixer, the DAC pulse is shaped to a sinusoidal wave. Because the sinusoidal pulse is chopped at the zero crossings, depending on the quantizer output, to generate the feedback pulse at the sampling instants. The feedback pulse has less amplitude than the conventional NRZ pulse as shown in Fig 4.9. However, sinusoidal signal has the highest slope at the zero crossing. Hence any loss of synchronization between the sinusoidal signal and clock signal will greatly increase the amplitude of the pulse at the sampling instants. A raised cosine DAC pulse has both zero value and zero slope at the sampling instants, so the raised cosine pulse DAC is the most clock jitter insensitive one among these three DACs.



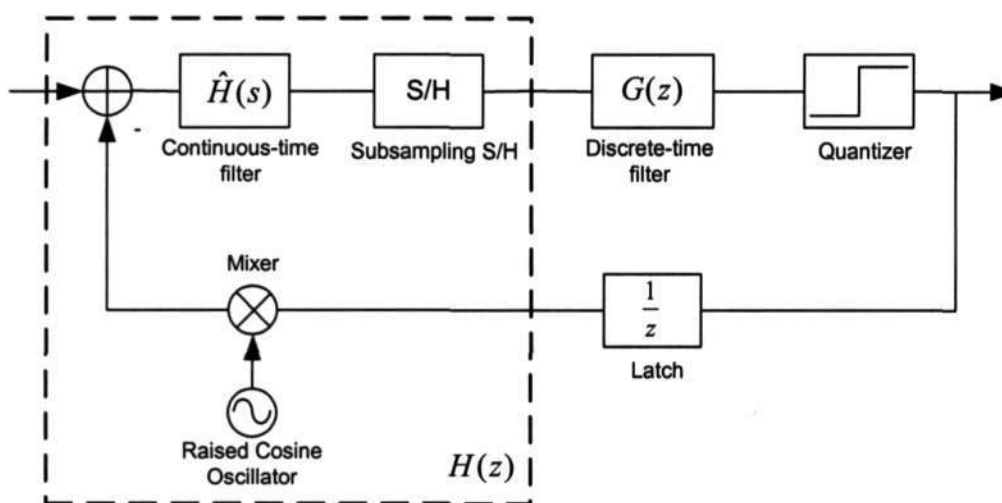
**Figure 4. 9 DAC jitter effect with different local-oscillator signal**

A raised cosine oscillator is used in the proposed  $\Delta\Sigma$ M to reduce the clock jitter sensitivity. To realize the frequency up-conversion, the frequency of the local-oscillator is  $f_l = N \cdot f_s$ . In the proposed  $\Delta\Sigma$ M,  $f_l = 4 \cdot f_s$  for a subsampling factor  $N=4$ . There are four raised cosine pulses in one sampling period. The phase noise is expected to improve due to the averaging effect [8]. So with a well-designed mixer, a

better SNR can be achieved compared to the conventional continuous-time  $\Delta\Sigma$  without mixer in the feedback path.

### 4.2.3 The Proposed Sixth Order Subsampling Bandpass $\Delta\Sigma$

The complete proposed subsampling sixth-order CT bandpass  $\Delta\Sigma$  is depicted in Fig.4.10.



**Figure 4. 10 The proposed 6th order subsampling bandpass  $\Delta\Sigma$**

The modulator is operating at an IF of 70MHz with a 18.667MHz sampling frequency (subsampling factor  $N=4$ ) with 200kHz bandwidth. The 70MHz IF is down-converted to 4.667MHz by subsampling. The Q factor of the CT filter is 60, and the DT filter  $G(z)$  is in the form of IIR block [9]. A raised cosine oscillator is used in the mixer to reduce the clock jitter sensitivity. One clock delay is purposely introduced in front of the DAC in the feedback loop [10]. The effect of nonzero excess loop delay and signal-dependent delay of the internal ADC is eliminated by the latch.

A Gm-C filter is chosen that has enough freedom to match the particular DT filter.  $Q=60$  was selected for the simulation. Of course, a better performance can be achieved when a higher  $Q$  can be obtained.

LC filter could be another choice. The typical transfer function of a second order LC bandpass filter is:

$$G(s) = \frac{As}{s^2 + s\omega_0/Q + \omega_0^2} \quad (4.30)$$

Because eq. (4.30) does not contain  $s^0$  in the numerator, the CT filter does not have enough freedom to match to the DT filter. The equivalent DT filter of eq. (4.30) is:

$$G(z) \approx \frac{-K(z^{-1} + z^{-2})}{1 + a^2 z^{-2}} \quad (4.31)$$

It results in the  $NTF_q$  having a pole at  $z=1+0j$  and the NTF asymmetric. The asymmetry of the NTF can be solved by changing the phase of the raised cosine oscillator as discussed in section 4.1.2. When

$$I_{DAC} \approx A_I(1 - \cos(\omega_1 t + \pi/4)) \quad (4.32)$$

But the phase shift of the DAC will cause the DAC to have higher amplitude at sampling instants, and hence more sensitive to the clock jitter. So the Gm-C filter is the better choice.

The raised cosine oscillator can be given by:  $I_{DAC} = A_I(1 - \cos(\omega_1 t))$ . By solving eq.(3.2), when

$$\hat{H}(s) = \frac{A(s-B)}{s^2 + s\omega_0/Q + \omega_0^2}, B = \omega_0 \frac{Q + e^{-\frac{\omega_0}{2Q}T_s}}{Q \cdot e^{-\frac{\omega_0}{2Q}T_s}} \quad (4.33)$$

$$H(z) \approx g_t \cdot \frac{-z^{-1}}{1 + a^2 z^{-2}} \quad (4.34)$$

Compared with the particular DT loop filter of a second-order bandpass  $\Delta\Sigma$ M in eq. (4.17). One clock delay is realized by the latches in the front of the DAC in the feedback loop.

The block diagram of the IIR block is shown in Fig.4.11. When the input signals are bounded, the output signals of the IIR block are also bounded. This is the major difference between the delay-based IIR blocks and integrator-based. The output swing of the integrator-based blocks is usually very high. The coefficients spread of the DT filter is low at around 3.5.

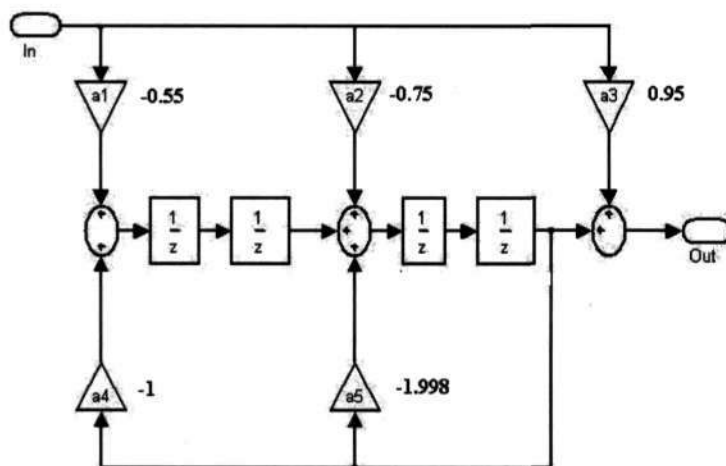


Figure 4. 11 The DT filter in the proposed  $\Delta\Sigma$ M

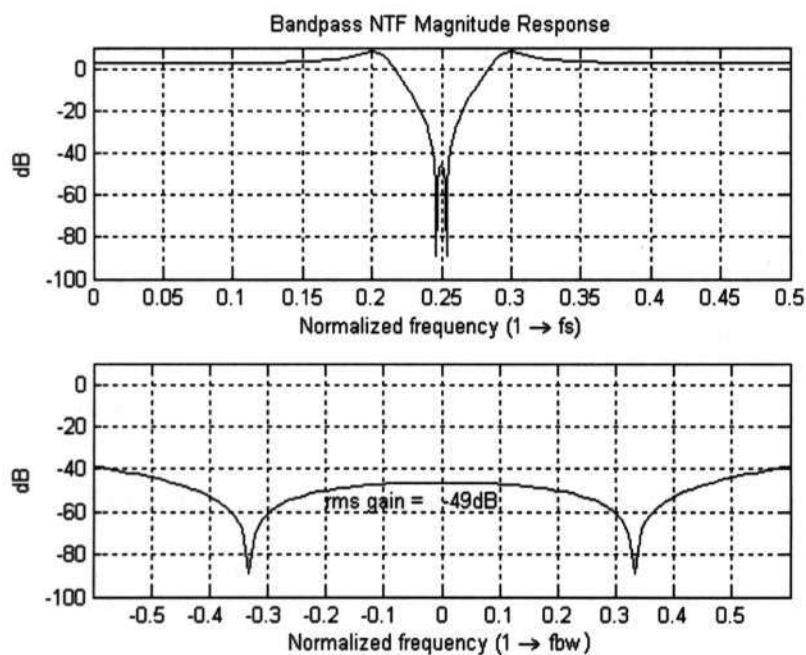
The  $NTF_q$  and  $NTF_s$  can be written as:

$$NTF_q = \frac{1}{1 + H(z)G(z)z^{-1}} = \frac{(1 + 0.675z^{-2})(1 + 0.045z^{-1} + z^{-2})(1 - 0.045z^{-1} + z^{-2})}{(1 + 0.523z^{-2})(1 + 0.513z^{-1} + 0.8884z^{-2})(1 - 0.513z^{-1} + 0.8884z^{-2})} \quad (4.35)$$

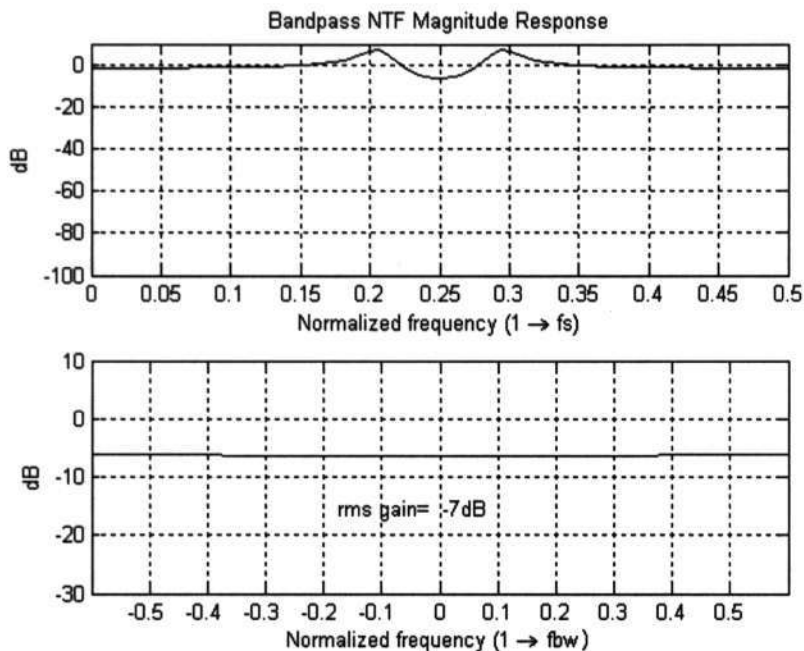
$$NTF_s = \frac{G(z)}{1 + H(z)G(z)z^{-1}} = \frac{0.95(1 + 0.276z^{-1} + 0.642z^{-2})(1 - 0.276z^{-1} + 0.642z^{-2})(1 + 0.675z^{-2})}{(1 + 0.523z^{-2})(1 + 0.513z^{-1} + 0.886z^{-2})(1 - 0.513z^{-1} + 0.886z^{-2})} \quad (4.36)$$

The inband rms gains of the  $NTF_q$  and  $NTF_s$  are  $-49\text{dB}$  and  $-7\text{dB}$ , respectively, as shown in Fig.4.12, Fig.4.13.

The noise shaping for the subsampling noise is much lower than the noise shaping for the quantization noise, because it is mainly decided by the CT filter. However, as the subsampling noise is at a much lower level compared with the quantization noise [11] when the bandwidth is narrow, the limited noise shaping may suppress the subsampling noise under the quantization noise.



**Figure 4.12**  $NTF_q$  magnitude response of the proposed  $\Delta\Sigma\text{M}$



**Figure 4.13** *NTF*, magnitude response of the proposed  $\Delta\Sigma$ M

## References

- [1] A.I. Hussein and W.B. Kuhn, "Bandpass  $\Delta\Sigma$ M Employing Undersampling of RF Signals for Wireless Communication," *IEEE Trans. Circuits and System II*, Vol. 47, No. 7, Jul. 2000, pp. 614-620.
- [2] J.V. Engelen, "Bandpass Sigma Delta Modulators," Kluwer Academic Publishers, 1999.
- [3] I. Hus, "A 70-MHz Continuous-Time CMOS Band-pass SD Modulator for GSM Receivers," *IEEE International Symposium on Circuits and Systems*, Vol. 3, May. 2000, pp. 750-753.

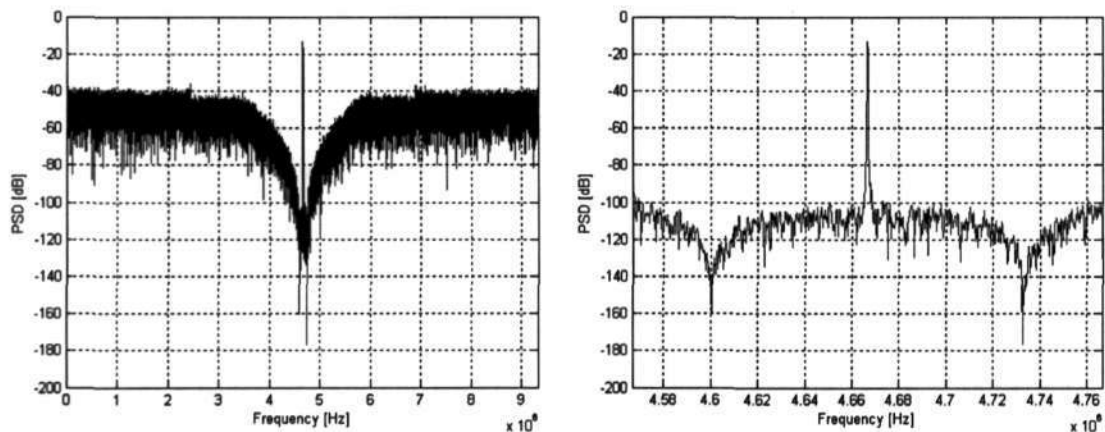
- [4] W.Gao and W.M. Snelgove, "A 950-MHz IF Second-Order Integrated LC Bandpass Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 5, May. 1998, pp. 723-732.
- [5] H. Tao and J.M. Khoury, "A 400-Ms/s Frequency Translating Bandpass Sigma-Delta Modulator," *IEEE Journal of Solid-State Circuits*, Vol.34, No. 12, Dec. 1999, pp. 1741-1752.
- [6] F. Gerfers, M. Ortmanns and Y. Manoli, "A 1.5-V 12-bit Power-Efficient Continuous-Time Third-Order Sigma Delta Modulator," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 8, Aug.2003, pp. 1343-1352.
- [7] S. Luschas, R.Schreier and H.S. Lee, "A 942 MHz Output, 17.5 MHz Bandwidth, -70dBc IMD3 Sigma Delta DAC," *IEEE Custom Integrated Circuit Conference 2003*, Sep. 2003, pp. 131-134.
- [8] S. Luschas and H.S. Lee, "High-Speed Sigma Delta Modulators with Reduced Timing Jitter Sensitivity," *IEEE Trans. Circuits and Systems II*, Vol. 49, No. 11, Nov. 2002, pp. 712-720.
- [9] R. Jiang and T.S. Fiez, "A 14-bit  $\Delta\Sigma$  ADC with 8OSR and 4-MHz Conversion Bandwidth in a 0.18- $\mu\text{m}$  CMOS Process," *IEEE Journal of Solid-State Circuits*, Vol.31, No.1, Jan. 2004, pp. 63-74.
- [10] S. Yan, "A Continuous-Time Sigma Delta Modulator with 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE Journal of Solid-State Circuits*, Vol.39, No. 1, Jan. 2004, pp. 75-86.
- [11] A. Hairapetian, "An 81-MHz IF Receiver in CMOS," *IEEE International Symposium on Circuits and Systems*, Vol. 31, Dec 1996, pp. 1981-1986.

## Chapter 5

# Simulation Results of the Proposed Subsampling $\Delta\Sigma$

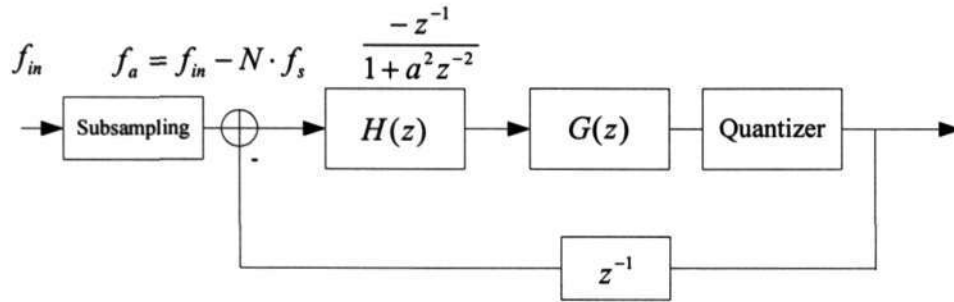
### 5.1 System Level Simulation Results

The system level simulation of the proposed subsampling bandpass  $\Delta\Sigma$  was simulated in MATLAB/SIMULINK, the peak SNDR is 65dB with a signal bandwidth of 200 kHz, 18.667 MHz sampling frequency when all the models are ideal and the input amplitude is  $-9$ dBFS. The 70MHz IF signal is down converted to 4.667MHz and the band-reject noise shaping is centered at 4.667MHz as shown in Fig.5.1.



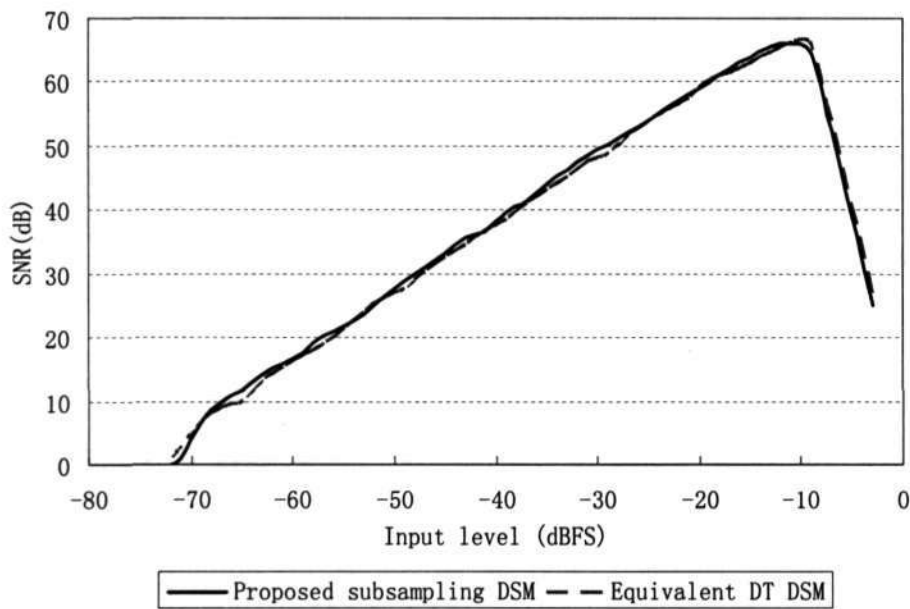
**Figure 5. 1 Output spectra of the ideal proposed subsampling  $\Delta\Sigma$ M with 200 kHz bandwidth (65536 points)**

The equivalent DT  $\Delta\Sigma$ M of the proposed subsampling  $\Delta\Sigma$ M that the subsampling operation is assumed in front of the modulator loop is shown in Fig.5.2.



**Figure 5. 2 Equivalent DT  $\Delta\Sigma\text{M}$  of the proposed subsampling  $\Delta\Sigma\text{M}$**

The dynamic range plot of the ideal proposed subsampling  $\Delta\Sigma\text{M}$  and its equivalent DT  $\Delta\Sigma\text{M}$  is depicted in Fig.5.3. It shows that the simulation results of these two  $\Delta\Sigma\text{M}$ s are very close and the modeling is effective.

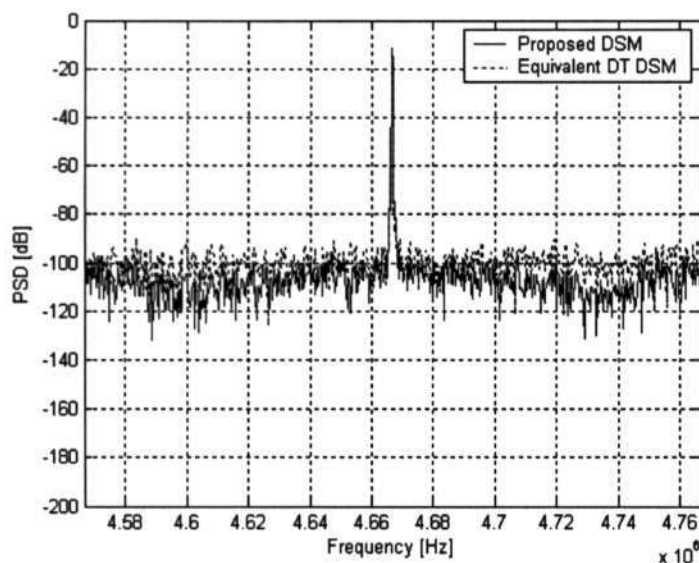


**Figure 5. 3 Dynamic range plot of the ideal proposed subsampling  $\Delta\Sigma\text{M}$  & its equivalent DT  $\Delta\Sigma\text{M}$**

Because the subsampling stage is quite noisy, when there is  $240 \text{ nV} / \sqrt{\text{Hz}}$  white noise introduced to the S/H, the peak SNDR of the proposed subsampling  $\Delta\Sigma\text{M}$  will drop 1dB to 64dB. With the same subsampling noise, the peak SNDR of the equivalent DT

$\Delta\Sigma\text{M}$  will drop to 57dB. The 7dB difference is due to the -7dB subsampling noise shaping.

The inband output spectra of the proposed subsampling  $\Delta\Sigma\text{M}$  and its equivalent DT  $\Delta\Sigma\text{M}$  with subsampling noise is depicted in Fig.5.4.



**Figure 5. 4 Inband output spectra of the proposed subsampling  $\Delta\Sigma\text{M}$  and its equivalent DT  $\Delta\Sigma\text{M}$  with subsampling noise (65536 points)**

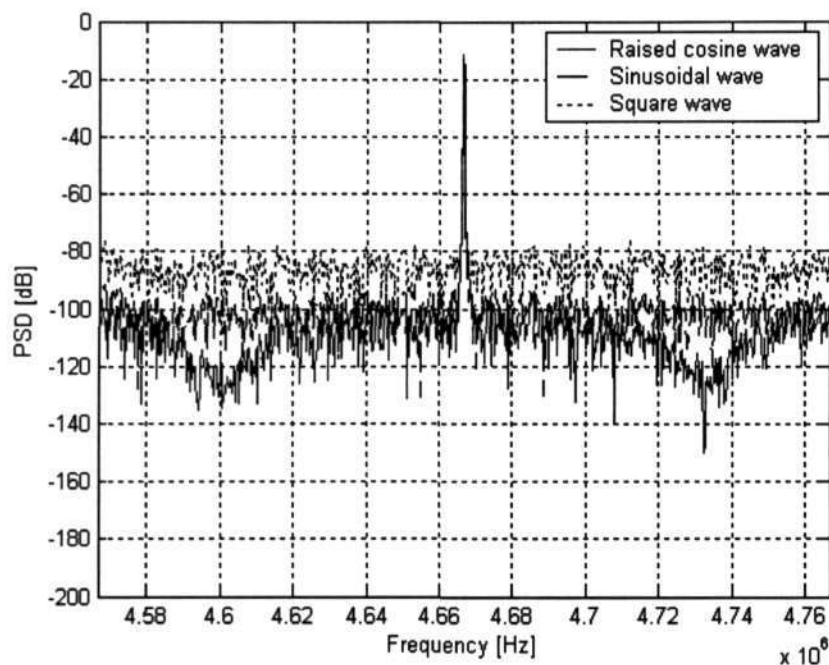
Because of the subsampling noise shaping provided by the CT filter; almost all the subsampling noise is suppressed. However, the matching of the CT filter is important. The performance degradation for the center frequency shift of the CT filter is shown in Table 5.1.

**Table 5. 1 SNDR vs. center frequency shift of the CT bandpass filter with subsampling noise**

0 Mismatch	64dB
0.5% Mismatch	62dB
1% Mismatch	61dB

Thanks to the raised cosine oscillator [1] [2], the proposed modulator is very insensitive to the DAC clock jitter. The SNDR performance is almost the same with 1% DAC clock jitter. With the same clock jitter in DAC, the SNDR of the  $\Delta\Sigma\text{M}$  with

sinusoidal oscillator drops 9dB, compared to that of 20dB drop in the SNDR of the  $\Delta\Sigma M$  with rectangle oscillator! The simulation results are shown in Fig.5.5. The subsampling noise is not introduced in this DAC jitter simulations.



**Figure 5. 5 Inband output spectra of the 1% DAC jittered proposed subsampling  $\Delta\Sigma M$  with different local-oscillator (65536 points)**

Higher SNDR can be achieved by increasing the Q factor of the CT filter; it will increase both the noise shaping for quantization noise and subsampling noise. The plot of peak SNDR of the ideal subsampling  $\Delta\Sigma M$  with/without the DT filter versus Q factor of the CT filter is depicted in Fig.5.6. The subsampling noise is not included in this simulation. It can be seen from Fig.5.6 that when the Q-factor is not very high, the noise shaping provided by the CT filter cannot suppress the quantization noise adequately. So the additional noise shaping provided by the DT filter is very necessary. The main function of the relatively moderate Q CT filter is to suppress the noise introduced by the S/H which is much lower than the quantization noise, due to the fact that the S/H is placed after the CT filter in the proposed  $\Delta\Sigma M$ .

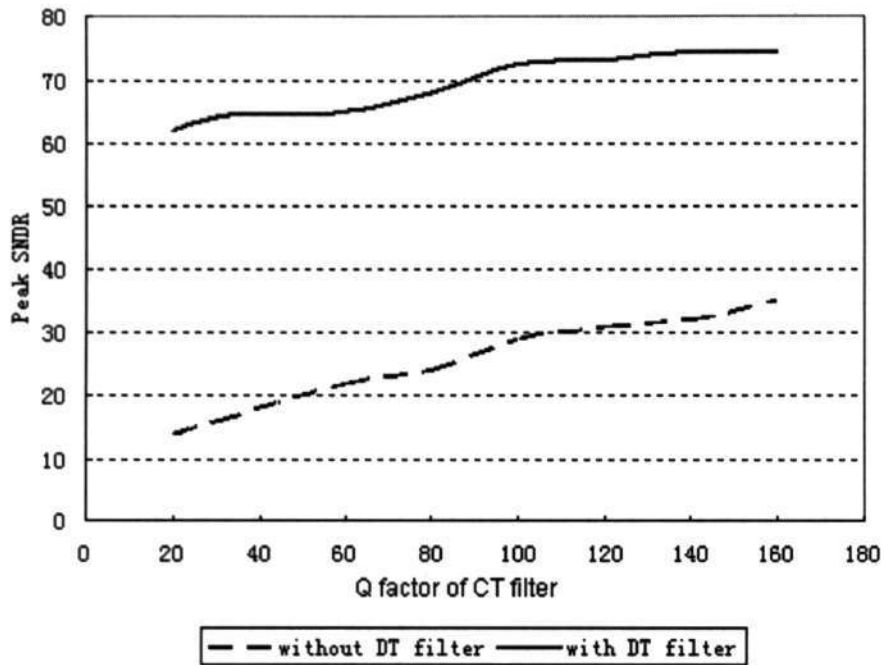


Figure 5. 6 Peak SNDR vs. Q factor of continuous-time filter

## 5.2 Circuit Level Implementation

The proposed subsampling  $\Delta\Sigma$  will be implemented in 0.5 $\mu$ m AMIS CMOS process with 3V power supply. Fig.5.7 depicts the circuit blocks of the proposed subsampling  $\Delta\Sigma$ .

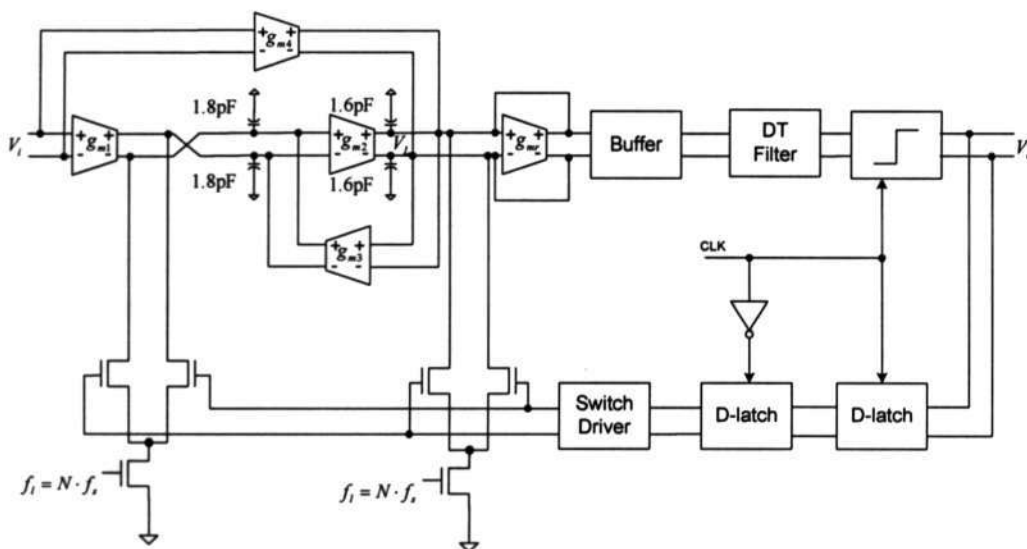


Figure 5. 7 Circuit blocks of the proposed subsampling  $\Delta\Sigma$

A. Continuous-Time filter & Buffer

A CT filter with Q-enhancement technique is shown in Fig.5.8 which has enough degree of freedom to match the wanted DT transfer function [3].

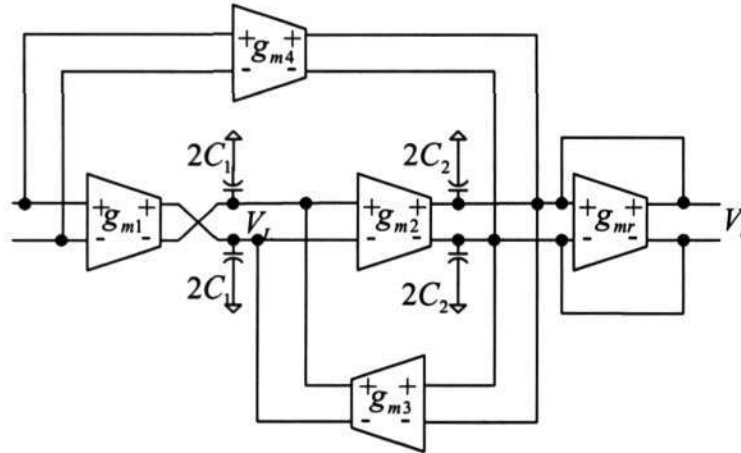


Figure 5. 8 Second-order Gm-C bandpass filter

The operational transconductance amplifier (OTA) labeled  $g_{mr}$  forms a positive feedback loop to compensate for the Q-factor loss of the filter due to the finite output impedance of the OTA, therefore increasing the Q value [3]. The center frequency can be tuned by changing  $g_{m2}$  and  $g_{m3}$  while the Q factor can be tuned by adjusting  $g_{mr}$ . The transfer function is

$$\hat{H}(s) = \frac{s \frac{g_{m1}}{C+C_0} - \frac{g_{m1}g_L + g_{m2}g_{m3}}{(C+C_0)(C+C_L)}}{s^2 + s \left[ \frac{g_L - g_{mr}}{C+C_0} + \frac{g_0}{C+C_L} \right] + \frac{g_{m2}g_{m3}}{(C+C_0)(C+C_L)} + \frac{g_0(g_L - g_{mr})}{(C+C_0)(C+C_L)}}, \quad (5.1)$$

Where  $g_0$  and  $g_L$  are the sum of the output conductance,  $C_1 = C_2 = C$ ,  $C_0$  and  $C_L$  are the sum of the parasitic capacitances at the  $V_o$  and  $V_L$  nodes respectively. Compared to

eq.(4.33), this structure ensures sufficient degree of freedom to realize the desired DT transfer function.

The OTA  $g_{m1}$  to  $g_{m4}$  used in this work is shown in Fig.5.9 [3]. The transconductance can be adjusted by  $V_c$ . In order to increase the input amplitude,  $g_{m1}$ ,  $g_{m4}$  is designed much smaller than  $g_{m2}$  and  $g_{m3}$ . The transistor sizes are given in the Table 5.2.

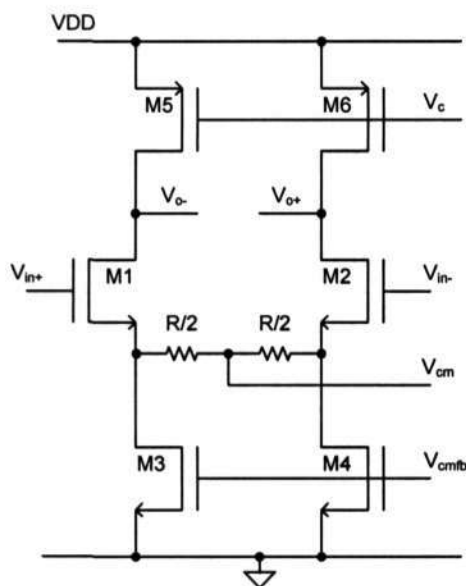


Figure 5. 9 Schematic of linearized OTA with common-mode detection

Table 5. 2 Transistor sizes of gm1, gm2, gm3, gm4

	gm1	gm2	gm3	gm4
M1-M2	9um/0.9um	120um/0.9um	120um/0.9um	9um/0.9um
M3-M4	9um/0.6um	108um/0.6um	108um/0.6um	9um/0.6um
M5-M6	6um/1.2um	72um/1.2um	72um/1.2um	6um/1.2um
R	2k	1k	1k	2k

The source degeneration resistor is split into two to sense the common-mode voltage of previous stage. As shown in the Fig.5.10, the detected voltage is compared with the reference voltage, and the error is fed back to the control node. The transistor sizes of the common-mode feedback circuit are shown in Table 5.3.

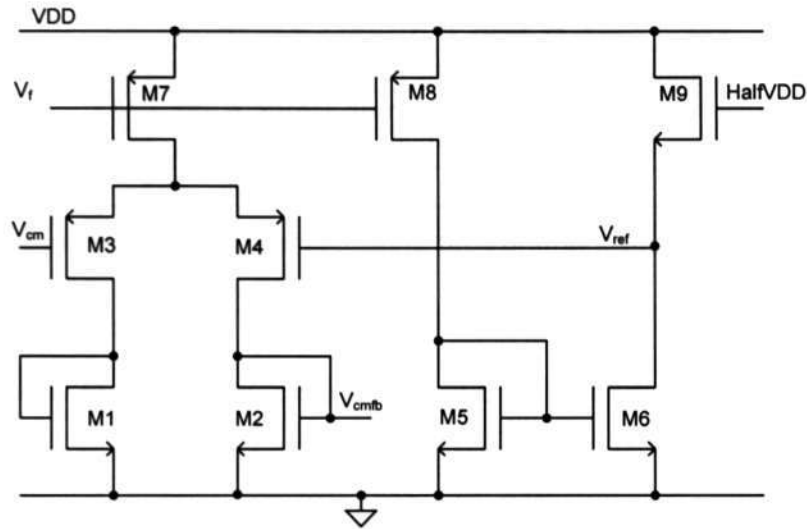


Figure 5. 10 Schematic of common-mode feedback circuit

Table 5. 3 Transistor sizes of the common-mode feedback

M1-M2	108um/0.9um	M7	144um/1.2um
M3-M4	108um/0.6um	M8	72um/1.2um
M5-M6	72um/1.2um	M9	60um/0.9um

The transconductor  $g_{mr}$  shown in Fig.5.11 is designed for Q-enhancement. The small transconductance value avoids over-enhancing the Q-factor; therefore ensuring the filter's stability. The Q-factor can be adjusted by Vq. Table 5.4 shows its transistor sizes.

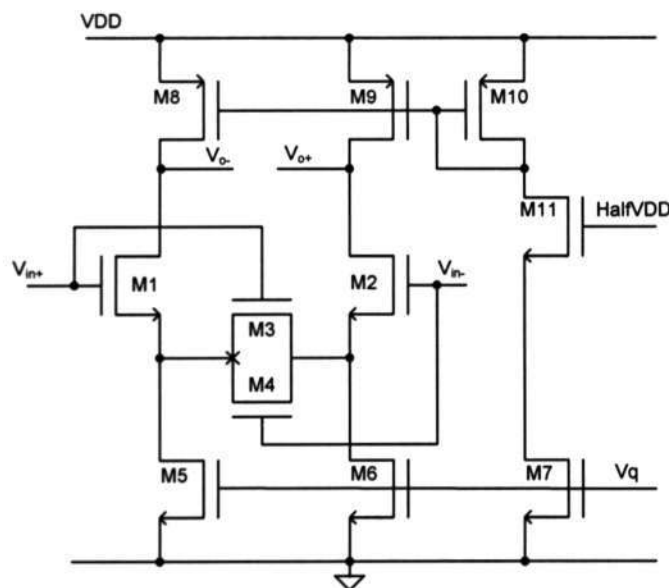
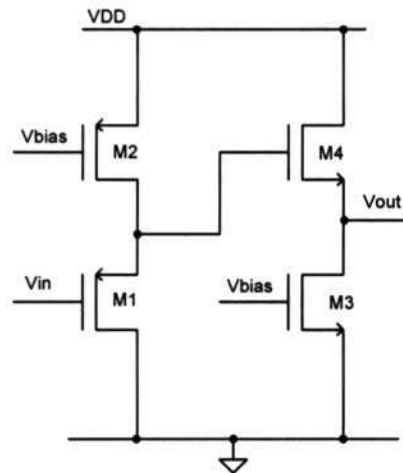


Figure 5. 11 Schematic of  $g_{mr}$  for Q-enhancement

**Table 5. 4 Transistor sizes of  $g_{mr}$**

M1-M2	1.8um/1.2um	M8-M9	18um/1.5um
M3-M4	4.5um/1.8um	M10	18um/1.5um
M5-M6	24um/0.9um	M11	18um/1.5um
M7	24um/1.2um		

To prevent sample transients from disturbing the continuous-time filter state, a buffer stage implemented by two source followers is used as depicted in Fig.5.12. The output of the buffer is set to 1.5V to drive the following DT filters adequately.

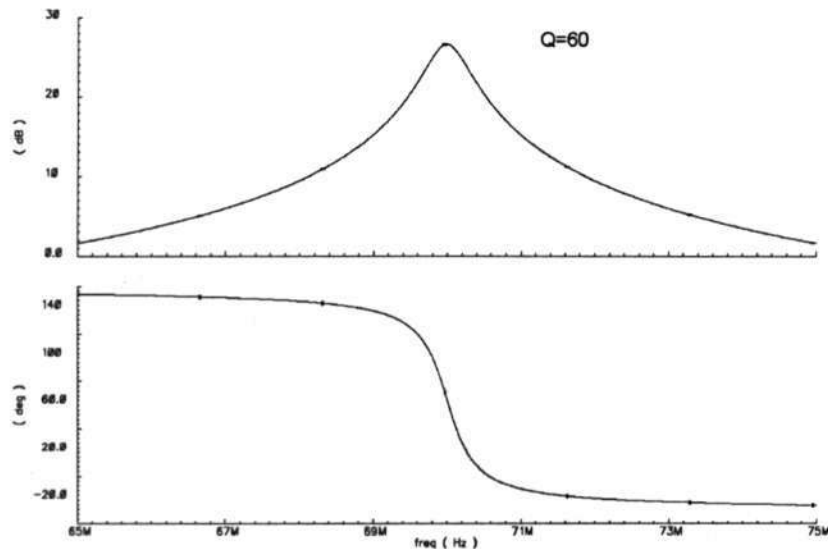


**Figure 5. 12 Schematic of the buffer**

**Table 5. 5 Transistor sizes of the buffer**

M1	30um/0.6um	M3	15um/0.6um
M2	30um/0.6um	M4	100um/0.6um

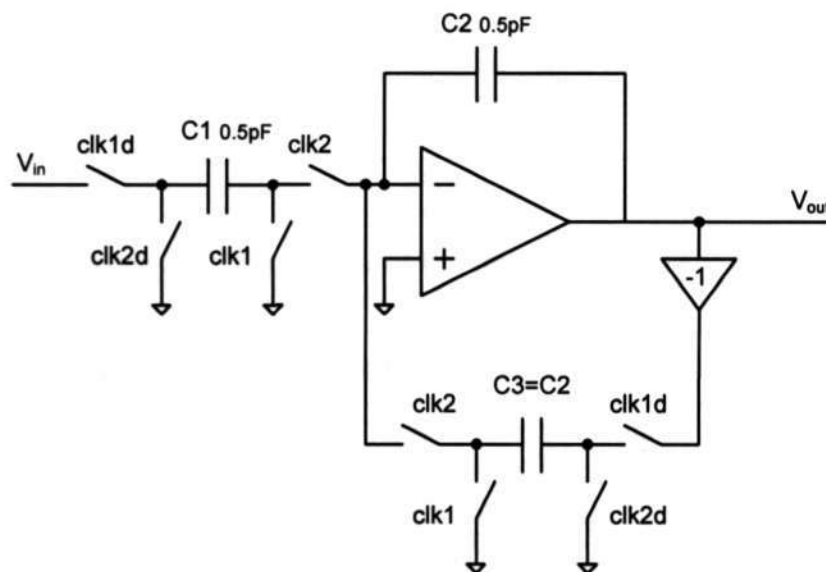
The simulated frequency response of the continuous-time filter is shown in Fig.5.13.



**Figure 5. 13 Simulated frequency response of the continuous-time filter**

### B. DT filter

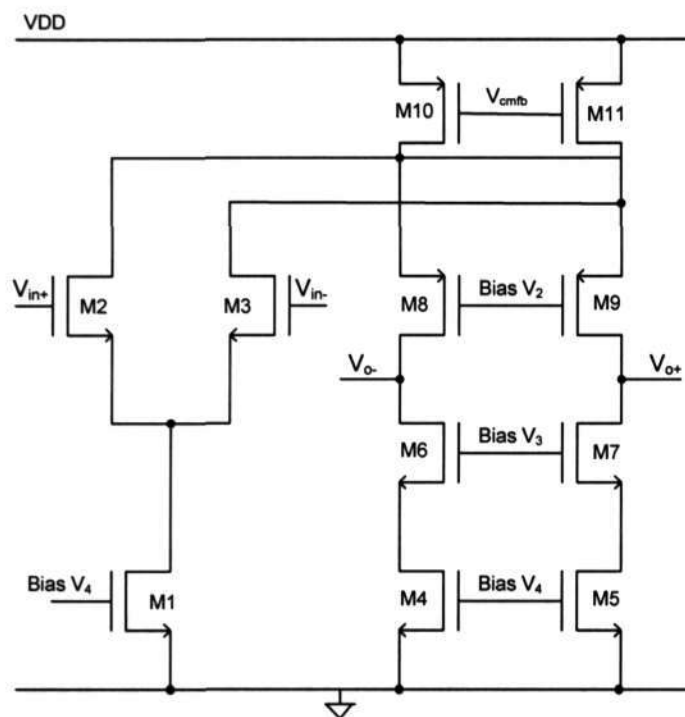
A delay-based structure is derived in [4] for the DT filter. Fig.5.14 depicts the schematic of the analog delay block which is an integrator with an additional switched-capacitor feedback. During  $\phi_2$ , the charge on  $C_3$  is transferred to the integrating capacitor  $C_2$  and the previous output is cancelled. The output of the analog delay block is sampled on  $\phi_1$  by the next stage. The advantage of this structure is that it can provide valid outputs for a whole clock period. Conventional switched-capacitor gain circuit can only provide valid outputs for half a clock period.



**Figure 5. 14 Schematic of the analog delay block**

NMOS input folded-cascode OpAmp is used to implement the analog delay as shown in Fig.5.15 [5]. The NMOS input folded-cascode OpAmp provides a higher gain than the PMOS input one because of the greater mobility of NMOS devices, but at the cost of the lowering the pole at the folding point. The M10/M11 must be wide enough to carry the drain currents of both M2/M3 and M8/M9. The total capacitance at the

folding points is larger than that of PMOS input OpAmp. The transistor sizes of the OpAmp and the bias voltages are shown in Table 5.6.



**Figure 5. 15 Schematic of the folded cascode OpAmp**

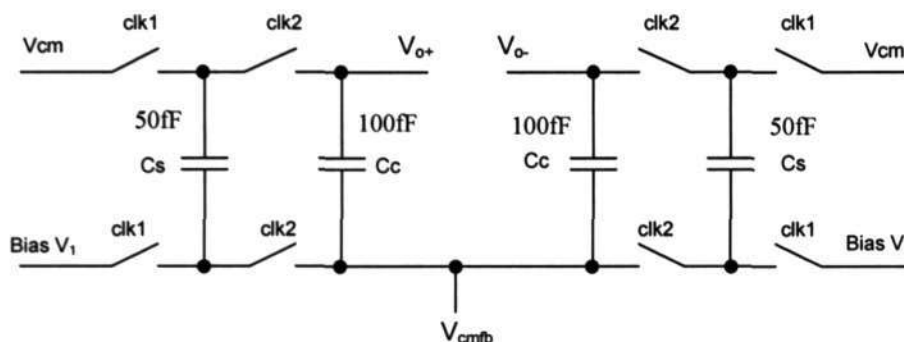
**Table 5. 6 Transistor sizes and bias voltages of NMOS input OpAmp**

M1	150um/0.6um	Bias V1	1.6V
M2/M3	300um/0.6um	Bias V2	1.3V
M4/M5	75um/0.6um	Bias V3	1.3V
M6/M7	150um/0.6um	Bias V4	1V
M8/M9	564um/0.6um		
M10/M11	400um/1um		

A switched-capacitor common mode feedback (CMFB) circuit shown in Fig.5.16 is used to keep the OpAmp output common mode potential stable [6].

Capacitors  $C_c$  generate the average of the output voltage  $V_{o+}$  and  $V_{o-}$  of the OpAmp. The generated  $V_{cmfb}$  is used to control the current sources in the OpAmp. The DC voltage across  $C_c$  is determined by capacitor  $C_s$  which is switched between a bias

voltage  $V_1$  and the desired common mode level  $V_{cm}$ . This circuit acts as a simple SC low-pass filter having a DC output signal.



**Figure 5. 16 Schematic of the switched capacitor common mode feedback**

The use of SC CMFB only results in a little bit more capacitive load for the OpAmp. If continuous-time CMFB circuits are used, the extra poles introduced in the current mirrors may decrease the bandwidth and increase the setting time.

Fig 5.17. shows the wide swing constant-transconductance bias circuit that generates bias voltage  $V_1$ - $V_4$  for the folded-cascode OpAmp [6]. The NMOS current mirror consists of transistors M1-M4. The gate voltages of cascode transistor M3 and M4 are derived by M5. The current for this biasing transistor is actually derived from the bias loop via M10 and M11. Similarly, the PMOS current mirror consists M6-M9, along with the diode-connected biasing transistor M14. The bias current derived via M12 and M13. To prevent zero current in all transistors at the start up, a start-up circuit consists M15-M18 is included. The transistor sizes of the bias circuits are shown in Table 5.7.

Chapter 5 Simulation Results of the Proposed Subsampling  $\Delta\Sigma M$

As seen in the Fig.5.18, the simulated unity gain frequency of the OpAmp when driving a 2pF load on each output is approximately 400MHz, and the phase margin is 59 degree.

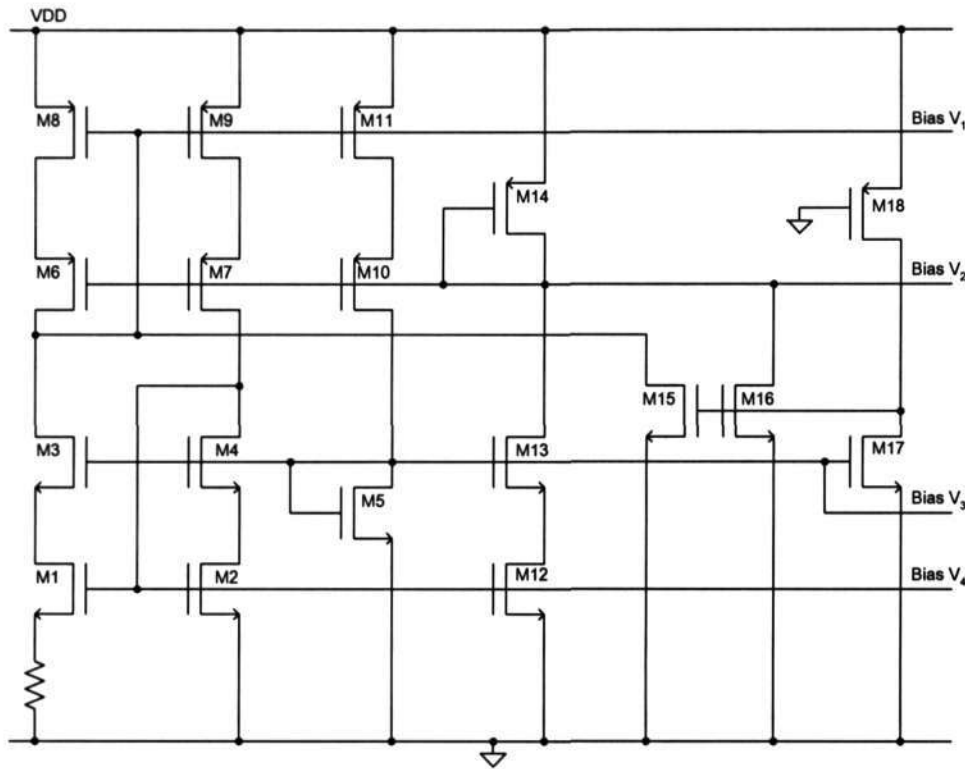


Figure 5. 17 Schematic of the biasing circuit

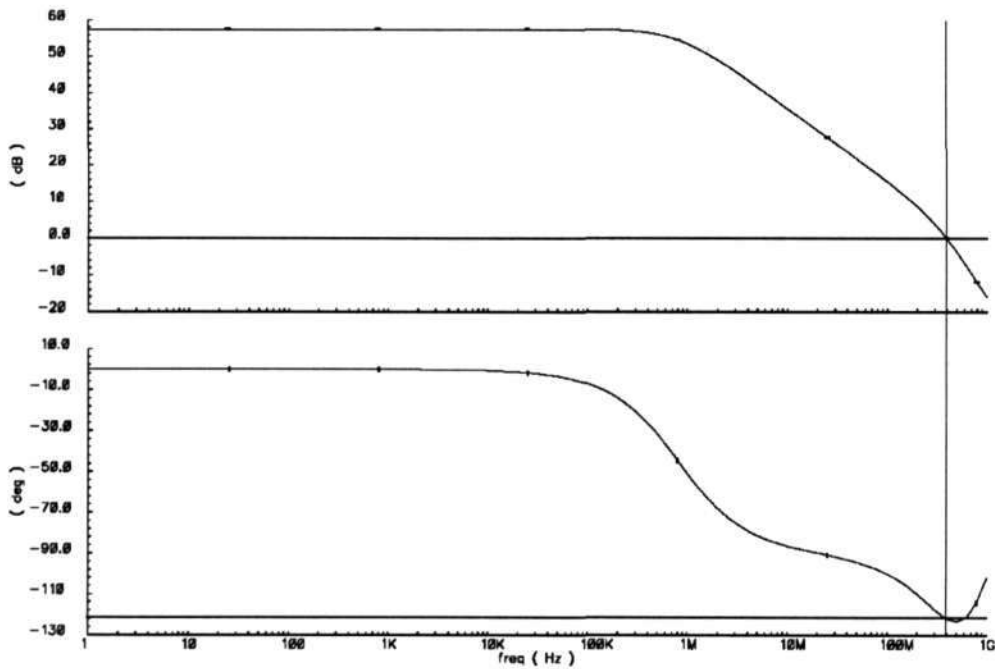


Figure 5. 18 Simulated frequency response of the OpAmp when driving a 2pF load on each output

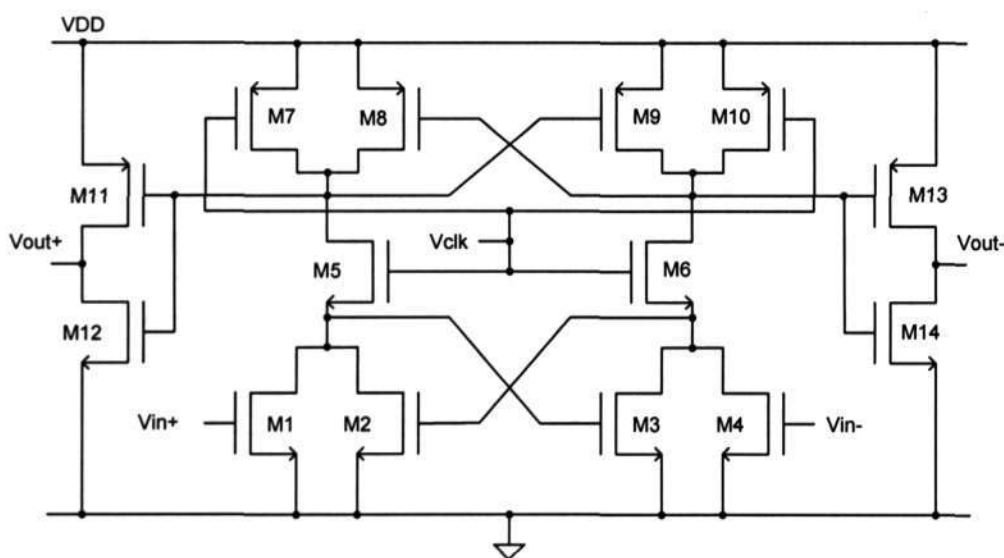
**Table 5. 7 Transistor sizes of the bias circuit**

M1	40um/1um	M7	20um/1.6um	M13	10um/1.6um
M2	10um/1um	M8	20um/1um	M14	5um/1.6um
M3	10um/1.6um	M9	20um/1um	M15	10um/1um
M4	10um/1.6um	M10	20um/1.6um	M16	10um/1um
M5	2.5um/1.6um	M11	20um/1um	M17	10um/1um
M6	20um/1.6um	M12	10um/1um	M18	20um/2um
R	5k				

*C. Comparator & Latch*

The 1-bit quantizer is realized using a latched-typed comparator [7] as depicted in Fig. 5.19. Pre-amplifier is not required because the noise will be suppressed by the loop.

When the clock signal is low, the comparator is in the pre-charge phase, transistor M5 and M6 are cut off and the comparator does not respond to any input signal. The drain voltage of M7/M10 will be pulled to VDD, and the output of the two inverters M11-M12, M13-M14 will be pulled to ground. Here M11-M14 act as buffers to isolate the latch from the output load.



**Figure 5. 19 Schematic for the latch-based comparator**

During the evaluation phase, when the clock signal goes high, both the drain voltage of M7/M10 drop from the VDD and both the drain voltage of M1/M4 increase. If  $V_{in+}$  is higher than  $V_{in-}$ , M1 draws more current than M4. Thus the drain voltage of M7 drops faster than the drain voltage of M10. As the drain voltage of M7 drops threshold voltage below VDD, M9 turns on and charge the drain voltage of M10 to high level and  $V_{out-}$  will be pulled to ground. The regenerative action of M8 and M9 together with that of M2 and M3 pull the drain voltage of M7 to ground and  $V_{out+}$  will be pulled to VDD.

The transistor sizes of the comparator are shown in the Table 5.8.

**Table 5. 8 Transistor sizes of the comparator**

M1	7.2um/0.6um	M8	33.6um/0.6um
M2	30um/0.6um	M9	33.6um/0.6um
M3	30um/0.6um	M10	44.4um/0.6um
M4	7.2um/0.6mu	M11	44.4um/0.6um
M5	24um/0.6um	M12	14.4um/0.6um
M6	24um/0.6um	M13	44.4um/0.6um
M7	44.4um/0.6um	M14	14.4um/0.6um

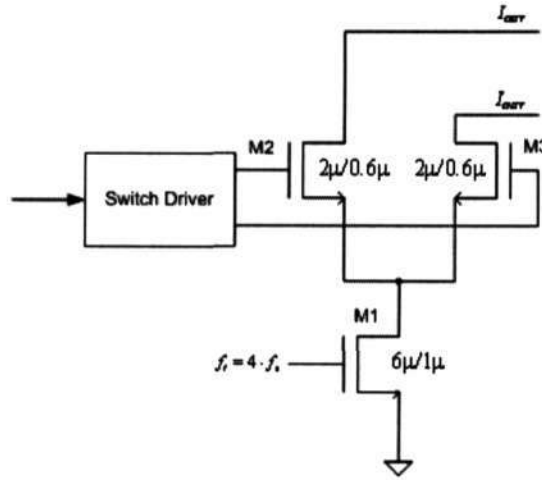
The comparator output will be pulled to ground during the pre-charge phase. To convert the RZ comparator output to NRZ output and realize the one clock delay, two TSPC D flip-flop are used [8]. The schematic of the TSPC D flip-flop is shown in Fig.5.20. The transistor sizes of the TSPC D flip-flop are shown in the Table 5.9

**Table 5. 9 Transistor sizes of the TSPC D flip-flop**

M1	3.6um/0.6um	M6	60um/0.6um
M2	15um/0.6um	M7	54um/0.6um
M3	30um/0.6um	M8	40um/0.6um
M4	15um/0.6um	M9	40um/0.6um

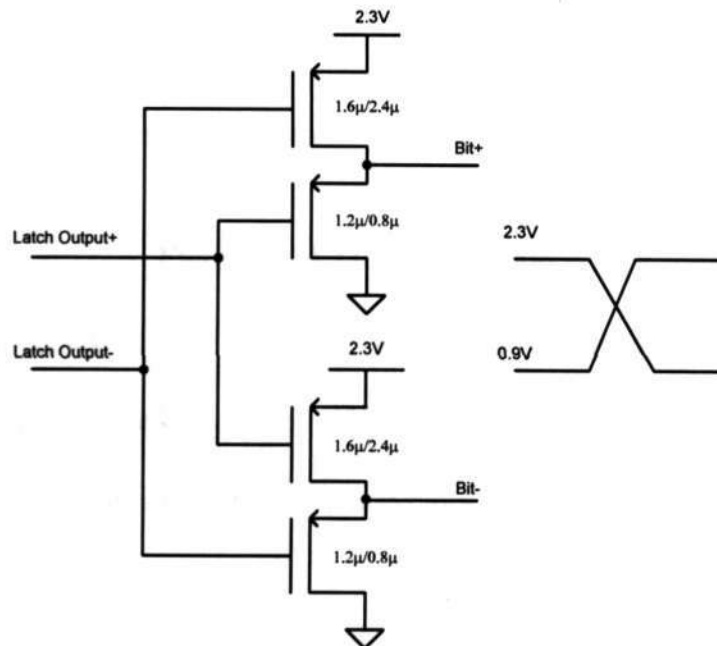


upconversion [9]. Switches M2 and M3 are designed to be in saturation and steer M1's current depending on the input data.



**Figure 5. 21 Raise cosine shaped DAC**

A switch driver is placed between the D flip-flop and the DAC cell. The switch driver design shown in Fig.5.22 has a high crossing point, so M2 and M3 are never simultaneously in the off state and the  $V_{ds}$  of M1 is constant [10]. Another function of the switch driver is to reduce the D flip-flop swing from 0V-3V to 0.9V-2.3V and keep the M2/M3 in saturation region.



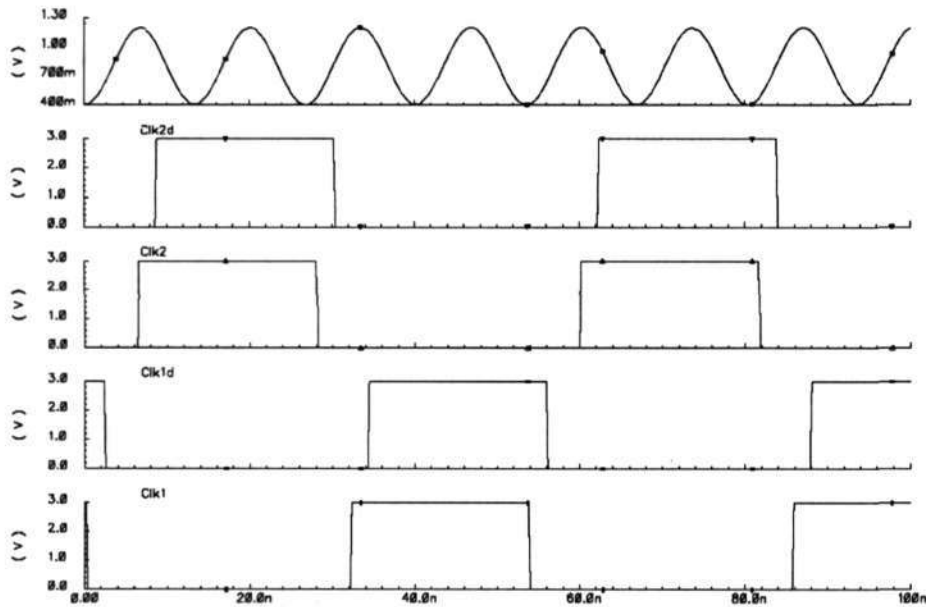
**Figure 5. 22 Schematic of the switch driver**

### E. Clock Arrangement & Clock Generator

The timing between the clock signal and raise cosine oscillating signal is important. If the oscillating signal is

$$V_{LO} = V_1 - V_2 \cdot \cos(\omega_1 t) \quad (5.2)$$

And the second D flip-flop gives the output at  $k \cdot T_s$ . Then the S/H should also sample the signal at  $k \cdot T_s$ . This means  $\phi_1$  (clk1) should end exactly at  $k \cdot T_s$  as shown in the Fig 5.23.



**Figure 5. 23 Timing diagram**

The non-overlap clock clk1, clk1d, clk2 and clk2d are generated using a fully-differential, two phase clock generator [11]. The external source  $\phi_R$  drives the clock generator. The block diagram of the two phase clock generator is depicted in Fig.5.24.

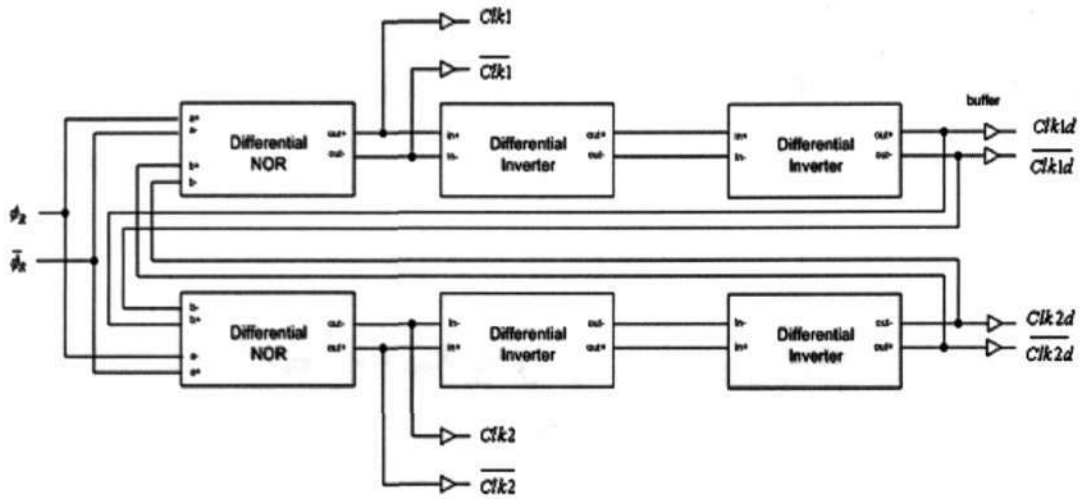


Figure 5. 24 Two phase clock generator

### 5.3 Circuit Level Simulation Results

Fig.5.25 shows the Cadence simulation of the proposed subsampling bandpass  $\Delta\Sigma M$  with real circuit blocks except the DT filter which is implemented by voltage control voltage source (VCVS) and ideal switches. The input frequency is 70.003MHz, the sampling frequency is 18.6667MHz and the frequency of the local oscillating signal is four times of the sampling frequency, 74.6667MHz. When the input signal is -12dBFS, the peak SNDR is 57dB.

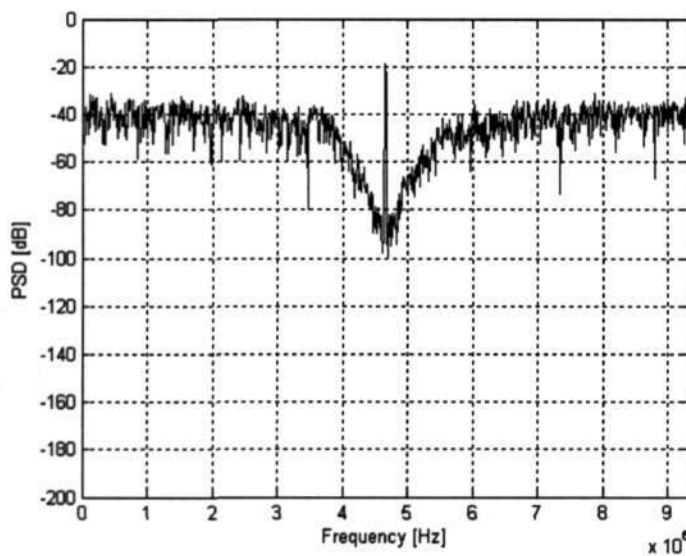
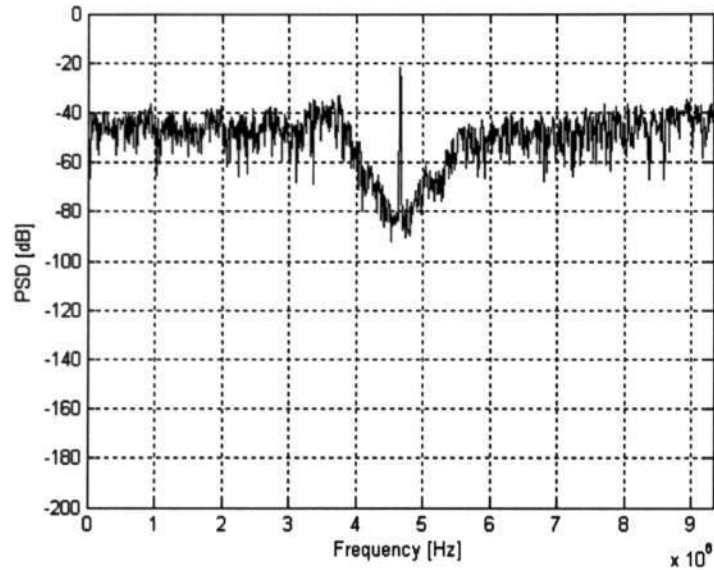


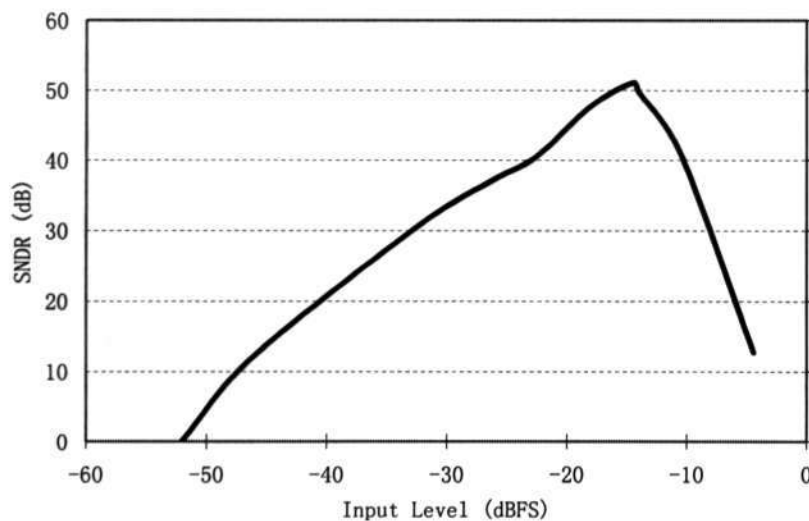
Figure 5. 25 Cadence simulation result of the proposed subsampling  $\Delta\Sigma M$  with ideal DT filter (2048 points)

Fig.5.26 shows the Cadence simulation of the full circuit level implementation of the proposed subsampling bandpass  $\Delta\Sigma$ . The peak SNDR is 51dB when the input signal is  $-13$ dBFS.



**Figure 5. 26** Cadence simulation result of the full circuit level implementation of proposed subsampling  $\Delta\Sigma$  (2048 points)

The dynamic range plot of the proposed subsampling  $\Delta\Sigma$  with full circuit level implementation is depicted in Fig.5.27.



**Figure 5. 27** Dynamic range plot of the proposed subsampling  $\Delta\Sigma$  with full circuit level implementation

The Cadence simulation result using all circuit is 6dB less than that of the Cadence simulation with ideal DT filter. The 6dB difference may come from the nonidealities of the OpAmp and MOS switches. There are another 8dB difference between the Cadence simulation using ideal DT filter and MATLAB ideal building block simulation. This 8dB difference may come from the nonidealities of CT filter, comparator, latch and the DACs. Because of the complexity of the modulator, the extensive full circuit level simulation is really needed. But the very long simulation time is a constraint.

**Reference:**

- [1] S. Luschas and H.S. Lee, "High-Speed Sigma Delta Modulators with Reduced Timing Jitter Sensitivity," *IEEE Trans. Circuits and Systems II*, Vol. 49, No. 11, Nov. 2002, pp. 712-720.
- [2] S. Luschas, R. Schreier and H.S. Lee, "A 942 MHz Output, 17.5 MHz Bandwidth, -70dBc IMD3 Sigma Delta DAC," *IEEE Custom Integrated Circuit Conference 2003*, Sep. 2003, pp. 131-134.
- [3] H. Liu and A.I. Karsilayan, "An Accurate Automatic Tuning Scheme for High-Q Continuous-Time Bandpass Filters Based on Amplitude Comparison," *IEEE Trans. Circuits and Systems II*, Vol. 50, No. 8, Aug. 2003, pp. 415-423.

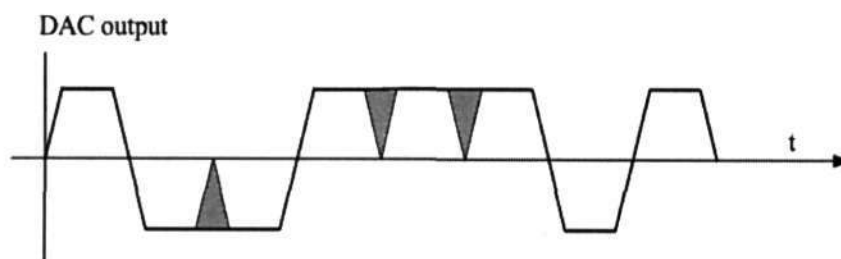
- [4] R. Jiang and T.S. Fiez, "A 14-bit  $\Delta\Sigma$  ADC with 8OSR and 4-MHz Conversion Bandwidth in a 0.18- $\mu\text{m}$  CMOS Process," *IEEE Journal of Solid-State Circuits*, Vol.31, No.1, Jan. 2004, pp. 63-74.
- [5] B. Razavi, "Design of Analog CMOS Integrated Circuit," McGraw-Hill, 2001.
- [6] D.A. Johns and K. Martin, "Analog Integrated Circuit Design," John Wiley & Son, Inc.
- [7] A. Yukawa, "A CMOS 8-bit High-Speed A/D Converter IC," *IEEE Journal of Solid-State Circuits*, Vol. 20, No. 3, Jun. 1985, pp. 775-779.
- [8] B. Chang, J. Park and W. Kin, "A 1.2GHz CMOS Dual-Modulus Prescaler Using New Dynamic D-Type Flip-Flop," *IEEE Journal of Solid-State Circuits*, Vol.31, No. 5, May. 1996, pp. 749-752.
- [9] E. Klumperink, "Reduce MosFET 1/f Noise and Power Consumption by Switched Biasing," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 7, Jul. 2000, pp. 994-1001.
- [10] T.Y. Wu, C.T. Jih and J.C. Chen, "A Low Glitch 10-bit 75-MHz CMOS Video D/A Converter," *IEEE Journal of Solid-State Circuits*, Vol.30, No.1, Jan. 1995, pp.68-72.
- [11] A.K. Ong, "Bandpass Analog-to-Digital Conversion for Wireless Application," PhD Thesis 1998.

## Chapter 6

# DAC Compensation for Continuous-Time Delta-Sigma Modulators

### 6.1 Effects of NRZ DAC Nonidealities

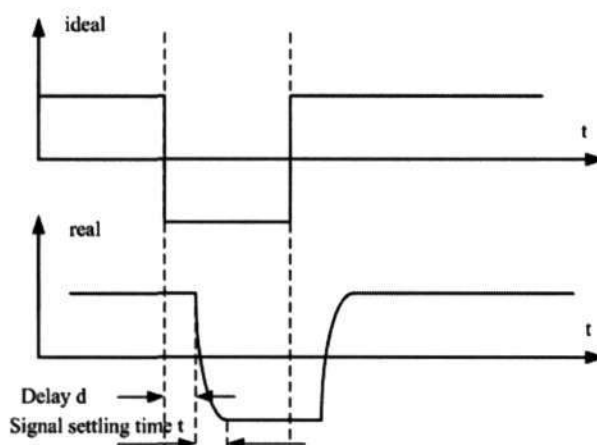
Beside the excess loop delay we mentioned in Chapter 3. There are some other nonidealities in NRZ DAC. One distortion in a 1-bit NRZ DAC is caused by intersymbol interference. Because the NRZ pulse transition in practice will have a limited rise and fall time, the effective DAC feedback level will depend on whether or not there is an output transition from one level to the opposite level. In case of a transition, the effective DAC feedback level will be less than that without transition. This is depicted in Fig.6.1 where the output of a 1-bit DAC with limited rise and fall times is shown. The errors caused by the absence of rising and falling edges are indicated by the shaded regions. Because the distortion depends on the preceding symbol, it is signal dependent and will result in harmonic distortion components and intermodulation products [1].



**Figure 6. 1 Distortion due to limited rise and fall times of a DAC using NRZ pulse**

One approach to reduce the effects of limited rise and fall times is to use RZ pulses. However, clock jitter affects RZ more severely than CT modulators employing just NRZ DAC feedback. A general rule of thumb is that jitter noise in a RZ DAC will have 6dB higher noise level in the signal band [2].

Combining the intersymbol interference and the excess loop delay, the nonidealities of DAC can be modeled by a delay and first order linear system as shown in Fig.6.2 where the finite rise and fall time and delay are shown.



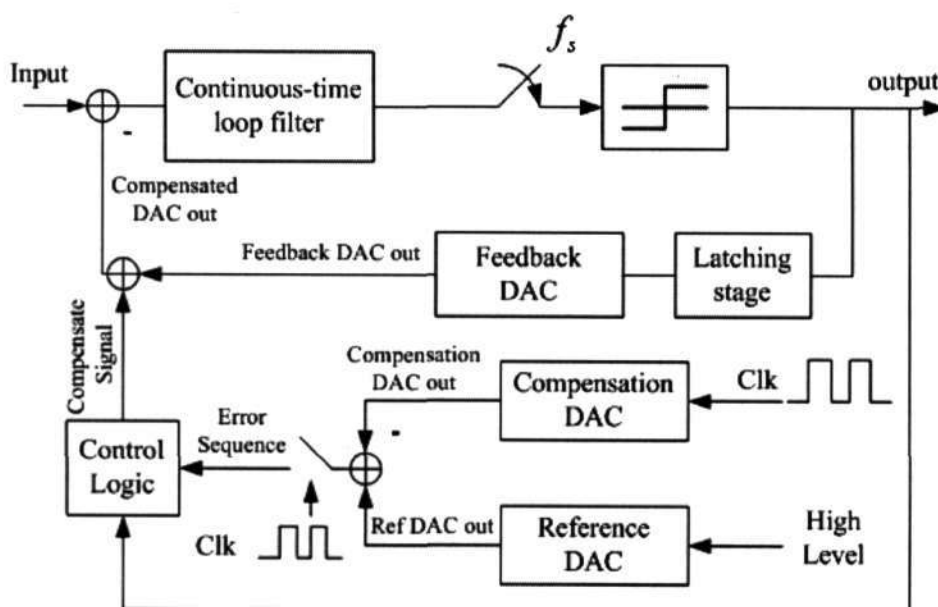
**Figure 6. 2 Modeling of NRZ DAC nonideal output**

As we discussed in Chapter 3, the signal dependent delay in the quantizer can be absorbed by using an additional latching stage after the quantizer. However, this latching stage does not absorb the delay in the feedback DAC and when the sampling frequency is very high; the delay introduced by the DAC will contribute more loop delay and degrade the performance of the CT  $\Delta\Sigma$ M.

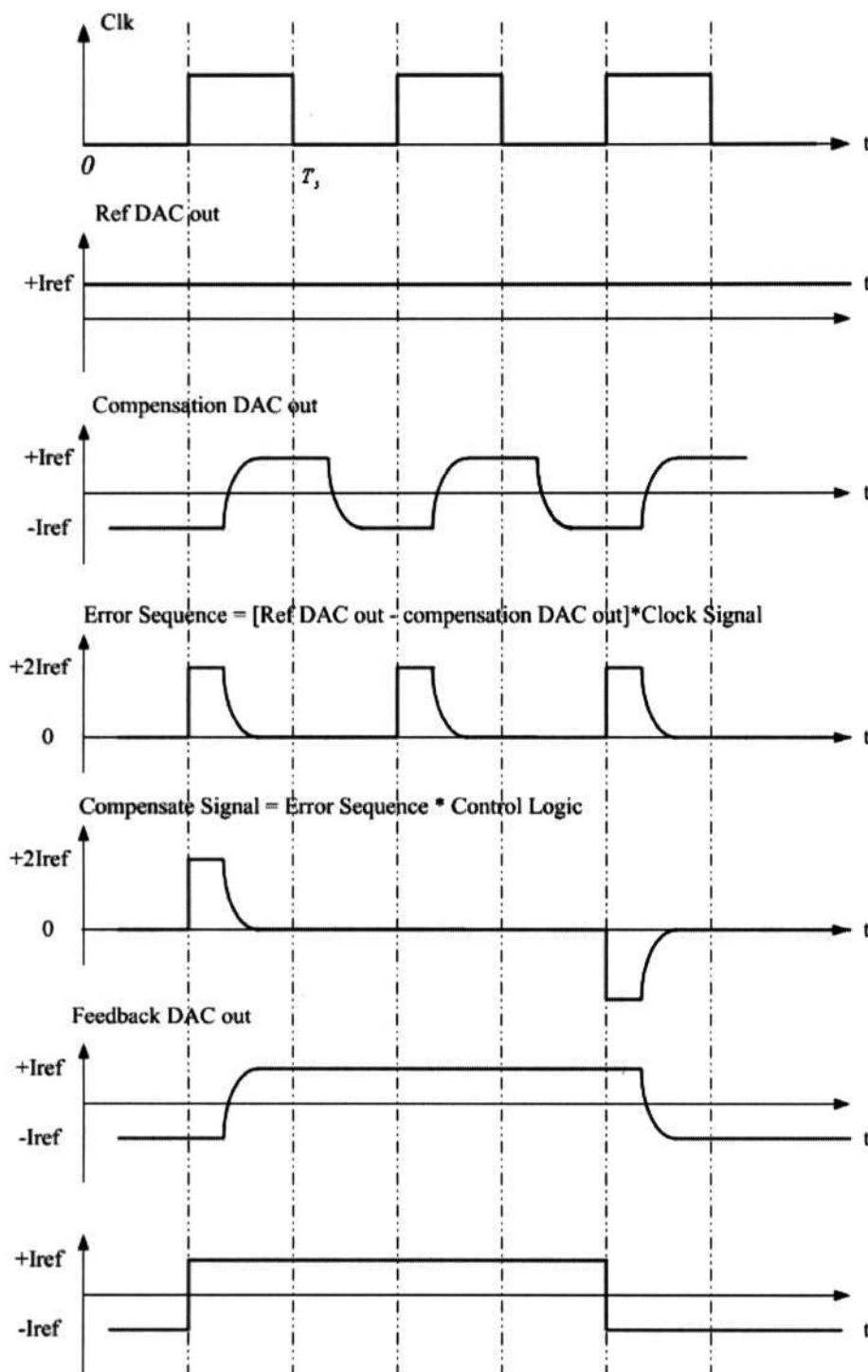
## 6.2 DAC Nonidealities Compensation

The design of continuous-time  $\Delta\Sigma$  without consideration of these NRZ DAC nonidealities would result in poor noise shaping performance and might even result in an unstable system, especially for high speed continuous-time  $\Delta\Sigma$ . Most existing methods like feedback coefficient tuning [3] are based on the accurate nonidealities estimation, which may be difficult to achieve. To overcome these DAC nonidealities without any prior knowledge of the nonidealities, a novel continuous-time  $\Delta\Sigma$  with NRZ DAC nonidealities compensation is proposed as shown in Fig. 6.3 [4].

The proposed CT  $\Delta\Sigma$  employs some extra 1-bit DACs and a control logic circuit. The illustration of this compensation scheme is depicted in Fig.6.4. The only assumption here is that all these DACs are relatively well-matched and for ease of illustration their nonidealities are modeled by a delay and first order linear system, as depicted in Fig. 6.2.



**Figure 6. 3 Block diagram of the proposed  $\Delta\Sigma$ M with DAC nonidealities compensation**



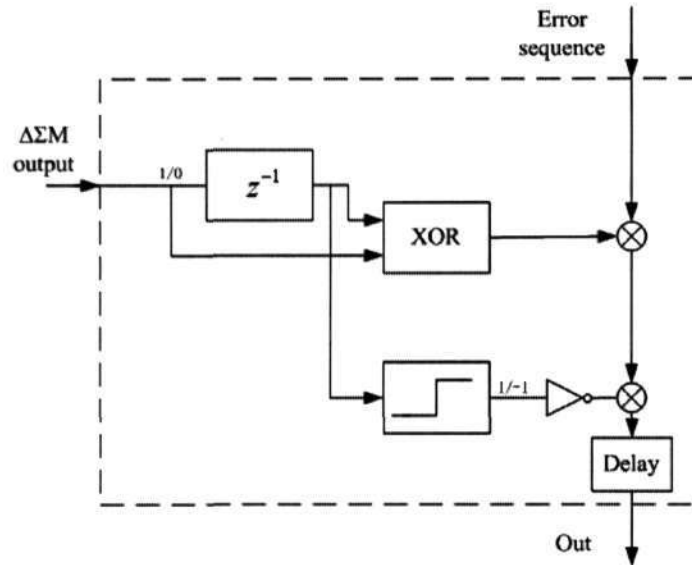
**Figure 6. 4 Illustration of the NRZ DAC nonidealities compensation scheme**

Assuming the two extra DACs, reference DAC, compensation DAC, and the feedback DAC in the feedback path are well-matched, the nonidealities of these three DACs will be very similar. As shown in Fig.6.3 and Fig.6.4, the input of the reference DAC is always high or “1” and it outputs a constant high DAC output level for reference.

The input of the compensation DAC is a clock signal whose frequency is the same as the sampling frequency  $f_s$  and the output is this clock signal with the associated DAC nonidealities discussed earlier. By enabling the difference between the reference DAC output and the compensation DAC output when the clock signal is high, an error sequence can be obtained. The error sequence is controlled by a control logic circuit. When the output of the  $\Delta\Sigma$  has a “0” to “1” transition, the error signal will be added to the feedback DAC output; when the  $\Delta\Sigma$  output has a “1” to “0” transition, the error signal which is negative will be added to the feedback DAC output as shown in Fig.6.4. Hence the nonidealities of the feedback DAC will be compensated to produce an ideal NRZ DAC pulse. Noting that the frequency of the error sequence is  $f_s$ , and the output of the feedback DAC only changes once in one clock cycle, the error sequence could provide the required compensating signal in all cases.

One latching stage is inserted in front of the feedback DAC to eliminate the performance degradation due to the non-zero excess loop delay and signal-dependent delay of the quantizer as well as allow sufficient time for the compensation block of the proposed  $\Delta\Sigma$  to settle to its final value.

The control logic block is depicted in Fig.6.5. When the  $\Delta\Sigma$  output has a “0” to “1” transition, the error sequence pass the control logic; when the  $\Delta\Sigma$  output has a “1” to “0” transition, the inverted error sequence pass the control logic. The delay block in the logic maintains synchronization between the compensation signal and the feedback DAC output.

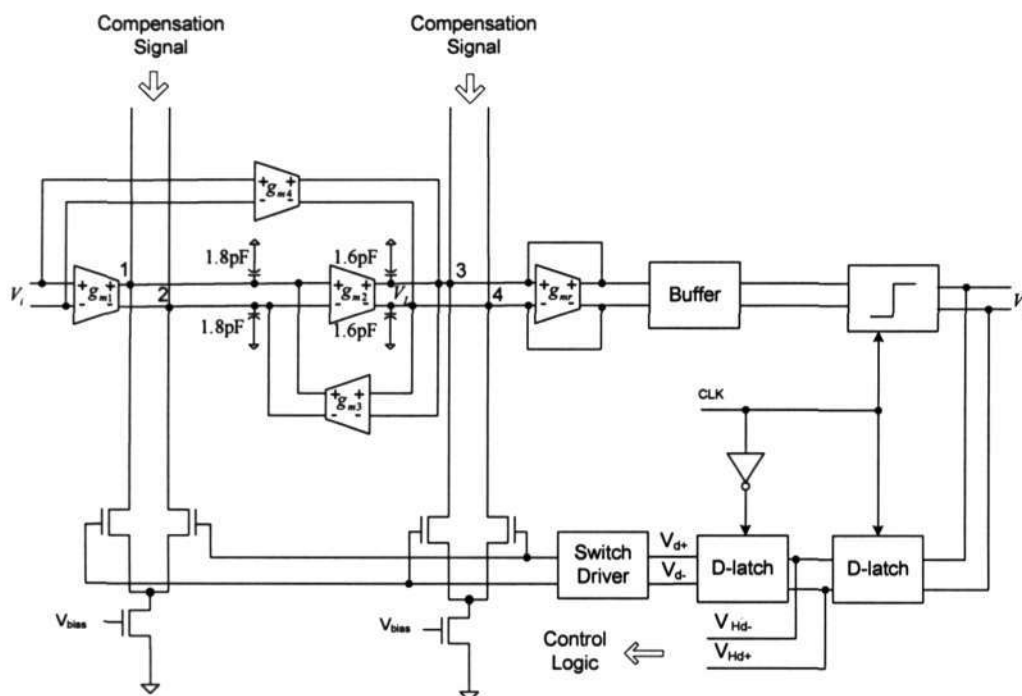


**Figure 6. 5 Block diagram of control logic**

One major advantage of this compensation technique is that the compensation signal is obtained from the error signal generated by using additional DACs which are matched to the feedback DAC. The knowledge of the actual DAC nonidealities such as the extent of loop delay and the manner in which the DAC settles to the final value is not required for the proposed compensation scheme to function properly. As long as all the DACs are relatively well-matched, this technique should be able to compensate for any NRZ DAC pulse shapes. The extra components used in the proposed compensation techniques are quite minimal as compared to techniques using digital compensation and calibration technique.

### 6.3 Simulation Results

A second-order bandpass continuous-time  $\Delta\Sigma$  with the proposed DAC nonidealities compensation is shown in Fig 6.6. The sampling frequency is 280MHz and the input signal is centered at 70MHz with a signal bandwidth of 1MHz. The continuous-time filter, buffer, comparator, D-latch and switch driver have same structures with these circuits used in the subsampling  $\Delta\Sigma$  discussed in Chapter 5.

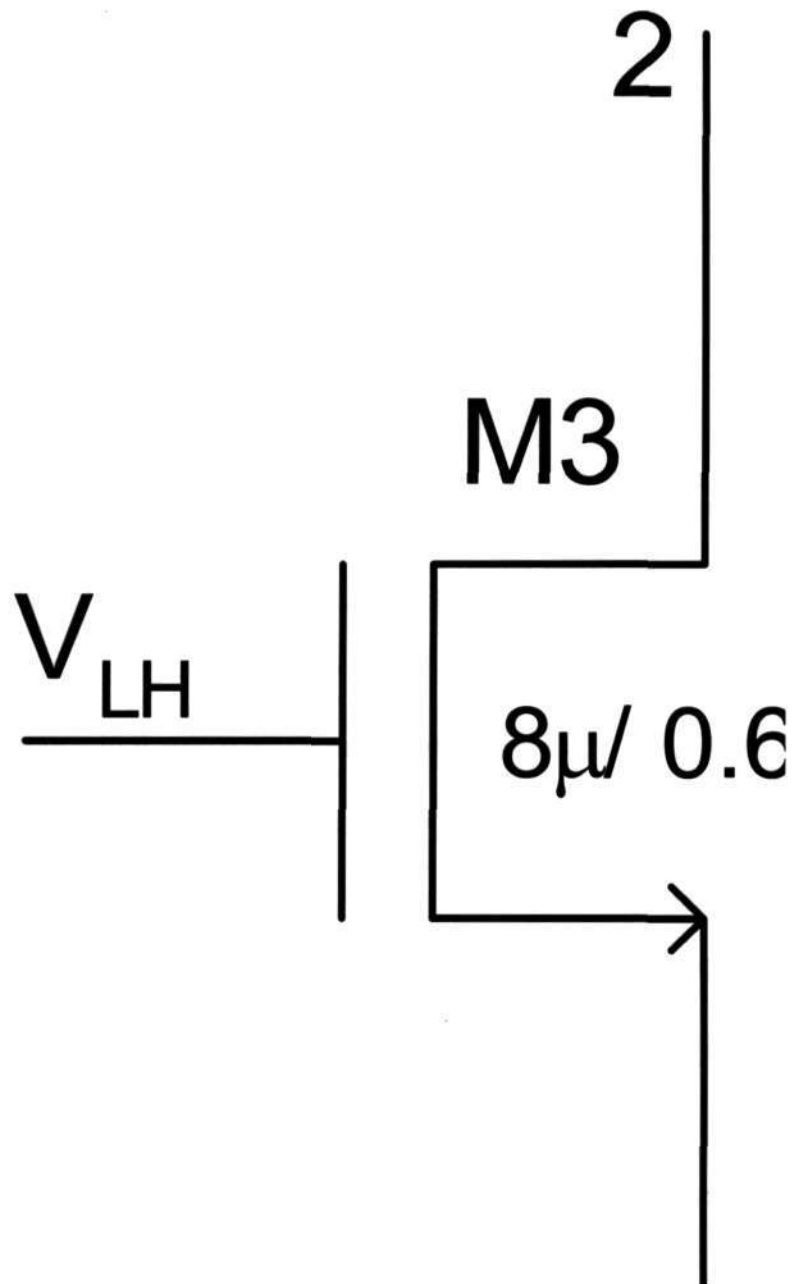


**Figure 6. 6 Circuit blocks of the second-order bandpass  $\Delta\Sigma$  with DAC compensation**

The first D-latch output  $V_{Hd+}$  and  $V_{Hd-}$  which are half clock delayed compared with the modulator output are sent to the control logic circuit. The compensation signals are connected to the node 1-4 together with the DAC feedback signals.

The control logic circuit is shown in Fig 6.7. The transistors of the inverters marked “s” have smaller sizes than the transistors of other inverters to synchronize the input signals of XOR/OR gates. The total delay in the control logic circuit is exactly half clock period that synchronizes the control logic output and the second D-latch output





**Figure 6. 8 Schematic of the reference/compensation DAC cells**

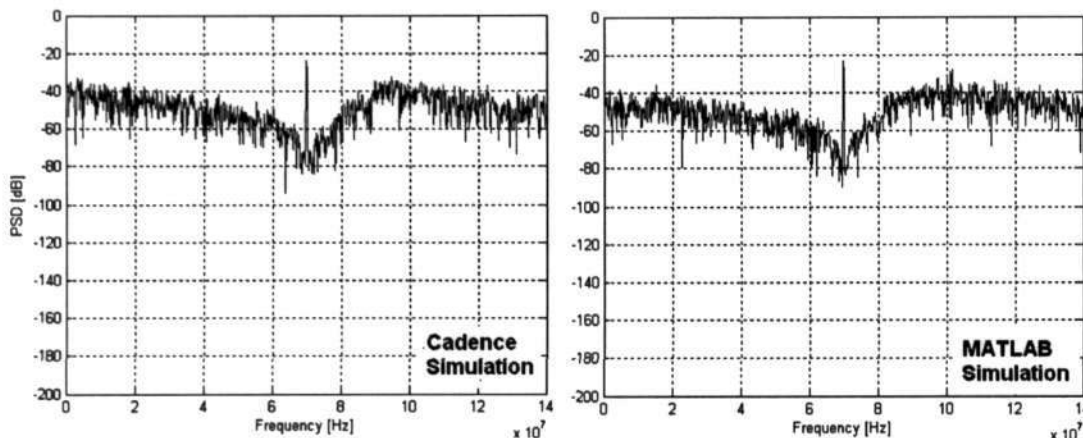
When  $V_{LH}$  is high, the output difference between the reference DAC cell and the compensation DAC cell will be added to the feedback DAC output signal; when  $V_{HL}$  is high, the output difference between the reference DAC cell and the compensation DAC cell will be subtracted from the feedback DAC output signal; as illustrated in Fig.6.4.

**Figure 6. 9 Schematic of the combined reference DAC cell connected to node 1,2**

All the DAC cells used for reference and compensation are the same. In one cell, the transistor sizes of M1 and M2 are twice the transistor sizes of M1<sub>0</sub> and M2<sub>0</sub> that used in the feedback DAC cell due to the differential operation. Transistor M3 and M4 are used as switches to steer the current. In Fig 6.8, there are two DAC cells used for reference/compensation. If these two DAC cells are combined into one DAC cell as shown in Fig 6.9, the function is still the same, but the transistor M3, M4 will both be in off states when V<sub>LH</sub> and V<sub>HL</sub> are both low. The source voltage of M3/M4 will drop close to zero and the big glitches will degrade the performance. So the reference/compensation DAC cell is split into two DAC cells and the complementary signal of V<sub>LH</sub> and V<sub>HL</sub> are used to reduce the glitches.

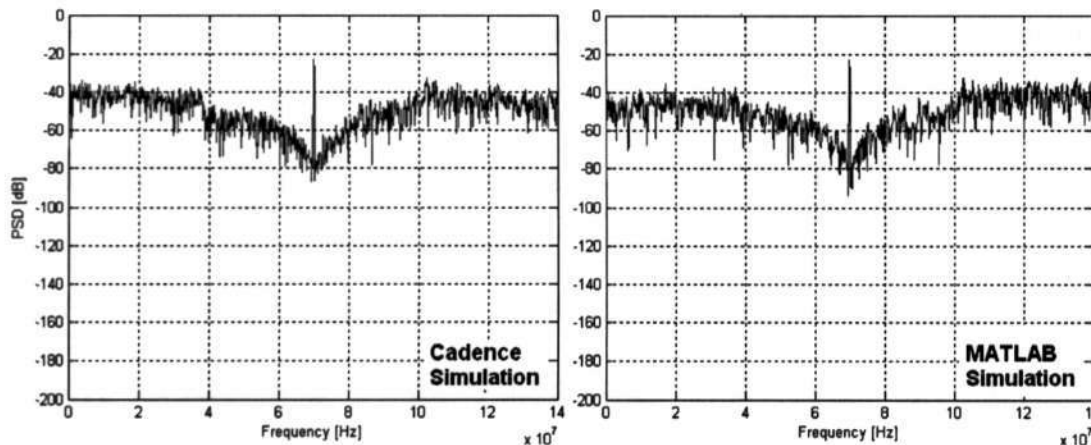
The second-order bandpass  $\Delta\Sigma$ M with/without DAC compensation are both simulated in Cadence and MATLAB. The output spectra of the second-order  $\Delta\Sigma$ M without DAC compensation is shown in the Fig 6.10. Because of the delay in the switch driver and feedback DAC itself, the output spectra become asymmetrical and the SNDR from Cadence simulation and MATLAB simulation are 43dB and 50.5dB respectively,

with  $-6\text{dBFS}$  input level. In MATLAB simulation, the total 790ps excess loop delay and 640ps rise time are modeled as a delay and first order linear system as shown in Fig.6.2.



**Figure 6. 10 Output spectra of the second-order  $\Delta\Sigma$ M without compensation**

The output spectra of the second-order  $\Delta\Sigma$ M with DAC compensation is shown in the Fig 6.11. The output spectra return to symmetrical because of the compensation. The SNDR from Cadence simulation and MATLAB simulation are 49dB and 56.3dB respectively, with  $-6\text{dBFS}$  input.



**Figure 6. 11 Output spectra of the second-order  $\Delta\Sigma$ M with compensation**

The MATLAB simulation results with ideal NRZ DAC are almost the same with the MATLAB simulation results with DAC compensation. The Cadence/MATLAB simulation results when the input level is -6dBFS are summarized in Table 6.1.

**Table 6. 1 Cadence/MATLAB simulation results of the second-order  $\Delta\Sigma$**

Bandwidth	Cadence simulation		MATLAB simulation		
	Without Compensation	With Compensation	Without Compensation	With Compensation	Ideal NRZ DAC
1MHz	43dB	49dB	50.5dB	56.3dB	56.7dB
2MHz	40.1dB	43.8dB	42.4dB	46.3dB	47dB

The SNDR of the second-order  $\Delta\Sigma$  with/without DAC compensation from Cadence simulation are both lower than that from MATLAB simulation because of the circuits nonidealities. But the SNDR improvements come from the DAC compensation are very close; the SNDR was improved by 3.7dB when the bandwidth is 2MHz and the SNDR was improved by 6dB when the bandwidth is 1MHz. The effectiveness of this compensation scheme is verified both from the output spectra waveform and the SNDR improvement.

The mismatch among three DACs is also investigated. The Monte Carlo simulation is done in MATLAB to determine the DAC magnitude mismatch effect. The simulation result is shown in Fig.6.12. It shows that in most cases the SNDR shift is less than 2dB when the variance of the DAC magnitude mismatch is 0.01.

Finally, as we discussed in chapter 3, the higher the order of the  $\Delta\Sigma$ , the more sensitive the  $\Delta\Sigma$  is to the excess loop delay. So the compensation scheme is potentially more effective when used in higher order  $\Delta\Sigma$ s.

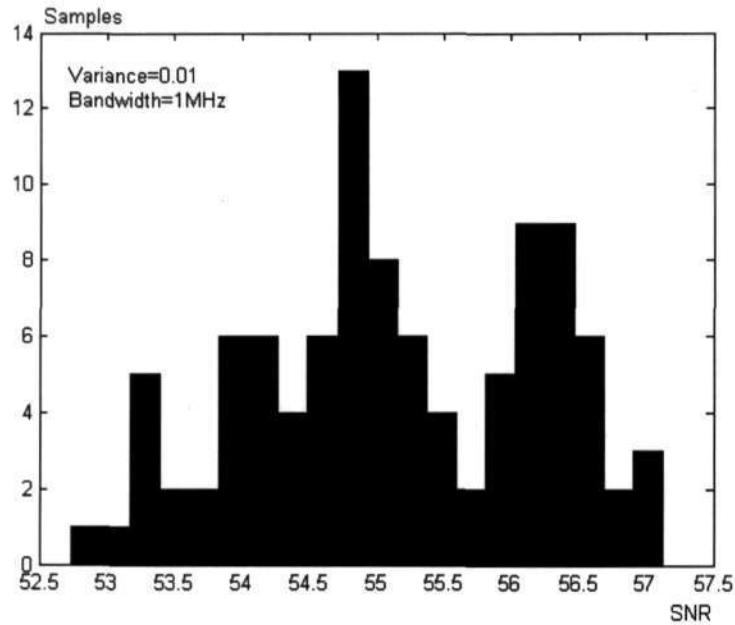


Figure 6. 12 Histogram of SNR with DAC mismatch of 0.01 variance.

## References

- [1] J.V. Engelen, "Bandpass Sigma Delta Modulators," Kluwer Academic Publishers, 1999.
- [2] J.A. Cherry and W.M. Snelgrove, "Excess Loop Delay in Continuous-Time Delta-Sigma Modulators," IEEE Trans. Circuits and Systems II, Vol. 46, No. 4, Apr. 1999, pp. 376-389.
- [3] W. Gao and O. Shoaie, "Excess Loop Delay Effects in Continuous-Time Delta-Sigma Modulators and Compensation Solution," IEEE International Symposium on Circuits and Systems, Vol. 1, Jun. 1997, pp. 65-68.

*Chapter 6 DAC Compensation for Continuous-Time  $\Delta\Sigma$ s*

---

- [4] K.T. Tiew and Y. Chen, "DAC Compensation for Continuous-Time Delta-Sigma Modulator," IEEE International Symposium on Circuits and Systems, May 2005.

# Chapter 7

## Conclusions and Future Works

### 7.1 Conclusions

#### *A. Subsampling bandpass delta-sigma modulator*

Normally for bandpass delta-sigma modulators, the sampling frequency is four times the center frequency, resulting in a very high sampling frequency. Sampling at such high frequencies requires expensive processes and increases the complexity and power consumption of the following digital signal processing stage. This problem can be solved by using an architecture employing subsampling with respect to the IF signal. This enables sampling at a frequency much lower than the center frequency and realizing the frequency down-conversion.

In this thesis, the transfer function derivation with finite  $Q$  factor bandpass filter is analyzed. The effectiveness of the continuous-time filter will degrade because of the subsampling operation that a controllable moderate  $Q$  factor continuous-time bandpass filter cannot adequately suppress quantization noise. Thus a subsampling bandpass delta-sigma modulator is proposed; a discrete-time filter is placed after the continuous-time filter to give additional noise shaping. The continuous-time bandpass filter operates at high frequency and after subsampling the discrete-time filter operates at low frequency. These two filters working together provide noise shaping both to

the quantization noise and the noise introduced by the subsampling operation. Two different modulator structures are compared based on the derived transfer function to achieve better noise shaping for both quantization noise and subsampling noise. Pulse-shaped DAC is used to reduce the clock jitter sensitivity and realize the frequency translation. The associated system level and circuit level simulation results are given in the thesis.

#### *B. DAC compensation for continuous-time delta-sigma modulators*

In the continuous-time delta-sigma modulator, the NRZ DAC is widely used because it is less sensitive to clock jitter compared with the RZ DAC. But the nonidealities of NRZ DAC such as intersymbol interference and excess loop delay will degrade the modulator performance.

In this thesis, a novel compensation technique to compensate for the NRZ DAC nonidealities is proposed. This compensation is based on acquiring the error signal by using additional DACs which are matched to the feedback DAC. The major advantage of this compensation technique is that it does not require any prior knowledge of the DAC nonidealities. A second-order bandpass continuous-time delta-sigma modulator employing the proposed compensation scheme is simulated and it is found from the circuit/system level simulation that in the presence of DAC nonidealities, the peak SNR could be enhanced by about 6dB by using the proposed compensation scheme.

## 7.2 Recommendations for Future Works

### *A. Subsampling bandpass delta-sigma modulator*

Future works for the subsampling bandpass  $\Delta\Sigma$  can be focused in the following areas:

#### 1. Analysis and improvement on the continuous-time filter.

A low noise, linear continuous-time filter is one of the most important blocks in the proposed subsampling  $\Delta\Sigma$ . Increasing the Q factor of the continuous-time filter increases noise shaping for both subsampling noise and the quantization noise, thus higher SNR can be achieved or bigger subsampling factor can be used. The research on the filter tuning and calibration is also essential.

#### 2. Optimization of the DT filter

The effects of OpAmp nonidealities used in the DT filter can be studied further and alternative SC implementation techniques such as two-path, double-sampling could be considered.

#### 3. Push the modulator closer to the front end of the receiver

It would be more insightful that the modulator can work at higher IF frequencies where the settling time and speed of the OpAmp and comparator become a big issue.

### *B. DAC compensation for continuous-time delta-sigma modulators*

Future works for the DAC compensation scheme can be focused in the following areas:

1. Use the DAC compensation scheme in high order  $\Delta\Sigma$ Ms

High order  $\Delta\Sigma$ M are more suffered from the DAC nonidealities. The effect of this DAC compensation scheme will be more obviously when used in higher order  $\Delta\Sigma$ Ms.

2. Extend the compensation scheme to multi-bit DACs

With the help of DEM, the multi-bit DACs are often used in the continuous-time  $\Delta\Sigma$ Ms. The compensation scheme can be further investigated for multi-bit DAC applications.

## **Author's publications**

Y. Chen and K.T. Tiew, "Sixth-order Subsampling Continuous-Time Bandpass Delta-Sigma Modulator," IEEE International Symposium on Circuits and Systems, May 2005.

K.T. Tiew and Y. Chen, "DAC Compensation for Continuous-Time Delta-Sigma Modulator," IEEE International Symposium on Circuits and Systems, May 2005.

Y. Chen and K. T. Tiew, "Fourth-order Subsampling Continuous-Time/Discrete-Time Bandpass Delta-Sigma Modulator," Proceedings of 10th International Symposium on ICs, Devices and Systems, ISIC-2004, Singapore, Sep. 2004.