

**NANYANG**  
**TECHNOLOGICAL**  
**UNIVERSITY**

**THROUGH-SILICON-VIA (TSV) DESIGN, FABRICATION  
AND CHARACTERIZATION FOR 3D IC APPLICATIONS**

**ZHANG LIN**

**SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING**

**2014**

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AND CHARACTERIZATION FOR 3D IC APPLICATIONS**

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**A thesis submitted to the Nanyang Technological University  
in partial fulfilment of the requirement for the degree of  
Doctor of Philosophy of Electrical and Electronic Engineering**

**2014**

# Acknowledgements

I would like to express my deepest gratitude to my supervisor, Nanyang Assistant Professor Tan Chuan Seng for giving me the opportunity to study and research in the field of three-dimensional integrated circuit (3D IC). He continuously inspired me along my PhD journey with his knowledge and passion in R&D. Without his guidance, support and all the valuable discussions during my PhD study, I could not accomplish the research goal. It is truly my great honour to work with him for the past four years.

I also would like to thank Dr. Li Hong Yu who is my co-supervisor at the Institute of Microelectronics (IME), for the invaluable guidance and support to help me whenever I encountered problems. With all her careful supports and suggestions along the PhD journey, I accomplished the project smoothly and efficiently.

Many thanks to Prof. Ang Diing Shenp, Prof. Chen Tupei, Prof. Liu Ai Qun, Prof. Tan Cher Ming, Prof. Wong Kin Shun Terence, Prof. Wang Hong, for their great lectures which help me not only to understand more deeply in the semiconductor related field, but also to build up the skills required in research field.

Thanks to my teammates, Dr Peng Lan, Dr Riko I Made, Dr Lim Dau Fatt, Mr Donny Lai, Mr Lu Weijie, Ms Ang Wan Chia, Dr Kaushik Ghosh, Mr Zhang Jiye and Dr Fan Ji, for all the supports and discussions to make our team successful and interesting. Not forgetting my friends at IME, Mr Li Yida, Dr Tao Jifang, Dr Fang Zheng and Dr Wang Jian, and all the technical staffs for their accompanies and valuable supports through the journey.

Last but not least, my warmest thanks to my parents and all my close friends, for being around and supporting me whenever happiness and sadness happened. We shared the joys and tears together. With your love, I feel happy, confident and encourage for my PhD project and for my future work and life.

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# Executive Summary

Three-dimensional (3D) integration is identified as a key and promising path, not only to facilitate the continuation of the conventional scaling, but also to enable the “More-than-Moore” heterogeneous integration of a vast different functionalities into a system in a single chip form. By using 3D integration in integrated circuits, potential benefit gains such as density, performance, heterogeneous integration, and lower cost can be achieved. Through-Silicon-Via (TSV) technology can provide shorter interconnection lengths; this translates to a lower inductance and conductance loss. In addition, TSV can also be designed and embedded in a 3D integrated circuit (IC) stack to assist in heat removal, which is a critical challenge facing 3D IC. Moreover, thermo-mechanical stress due to the mismatch of the coefficient of thermal expansion (CTE) between Si and TSV Cu core has critical effects on the active device performances in the vicinity of the TSV.

In this thesis, fabrication processes and results of TSVs with 5  $\mu\text{m}$  of diameter and aspect ratio of 1:2 to 1:3 are discussed. The results show that super-conformal filling TSVs with plasma enhanced tetraethylorthosilicate (PETEOS) oxide, black diamond low- $\kappa$ , bi-layer of  $\text{Al}_2\text{O}_3$  and PETEOS oxide and bi-layer of  $\text{Al}_2\text{O}_3$  and low- $\kappa$  liners are successfully fabricated.

In our electrical  $C$ - $V$  measurements, we show that through careful process tuning, we are able to shift the  $C$ - $V$  curve to achieve accumulation capacitance within the operating voltage of interests ( $\sim 0$ -5 V). This was due to the PETEOS oxide liner deposition process which introduces beneficial negative fixed charges, and is estimated to have a density of charge of  $\sim -8.43 \times 10^{11} \text{ cm}^{-2}$  corresponding to a shift of +7.5 V in the positive flat-band voltage ( $V_{FB}$ ). In comparison to the inversion capacitance which changes rapidly with

substrate dopant concentration, small signal frequency and temperature fluctuation, the accumulation capacitance is stable and independent on the substrate temperature for better prediction and control of signal transmission in TSV in the presence of non-uniform hotspot heating. At the same time, in order to further reduce the accumulation capacitance, TSVs with black diamond low- $\kappa$  material as the liner were also successfully fabricated and the  $C$ - $V$  results show that the capacitance is reduced by  $\sim 28\%$  compared with the TSVs with conventional PETEOS oxide liner. In addition, novel material selection of a thin  $\text{Al}_2\text{O}_3$  ( $\sim 10$  nm) has been integrated between the Si substrate and the dielectric liner successfully by utilizing atomic layer deposition (ALD) process. The  $\text{Al}_2\text{O}_3$ -induced negative fixed charge, which has the density on the order of  $\sim -7.44 \times 10^{11} \text{ cm}^{-2}$ , could be effectively utilized to shift the  $C$ - $V$  curve so that stable accumulation capacitance was obtained. The corresponding flat-band voltage ( $V_{FB}$ ) shift is  $+7.1 \text{ V}$ .

Electrical  $I$ - $V$  measurements are carried out to monitor the leakage current of the dielectric liners from the TSV Cu core to the Si substrate. The results show that no catastrophic breakdown within the desired operating voltage range for all the liners, but the low- $\kappa$  liner was expected to introduce higher leakage current than the oxide liner due to its porosity. After annealing in forming gas ( $\text{H}_2/\text{N}_2$ ) at  $350^\circ\text{C}$  for 30 min, the leakage current density of the low- $\kappa$  liner reduced from  $\sim 6.8 \times 10^{-6} \text{ A/cm}^2$  to a comparable level of oxide liner which is  $\sim 1.2 \times 10^{-6} \text{ A/cm}^2$ .

In order to study the thermal properties of TSV, a doped polysilicon line as a heat generator surrounded by rows of TSVs of different dimensions and densities were fabricated. It was found that the use of appropriate TSV arrays which surround and are placed beneath a temperature sensor have an effective cooling capability of as much as  $\sim 40^\circ\text{C}$ .

Finite element analysis (FEA) modelling and high resolution micro-Raman analysis are carried out to monitor and compare the thermo-mechanical stress exerted on the Si substrate of TSV structures with different TSV diameters and liners. Results show that scaling down the TSV size could improve the stress, since the Cu core volume is decreased. Also it is shown that the low- $\kappa$  liner, due to its smaller elastic modulus ( $\sim 4.2$  GPa), acts as a compliant layer to cushion the Cu-TSV stress on the Si compared with PETEOS oxide ( $\sim 75$  GPa). This relaxes the keep-out-zone (KOZ) requirement. KOZ is imposed around a TSV where no other devices can be placed within a KOZ to minimize the performance degradation due to the stress induced by the TSVs. The higher the KOZ is, the lower the silicon area utilization is.

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# List of Abbreviations

2D	Two-Dimensional
3D	Three-Dimensional
3D IC	Three-Dimensional Integrated Circuit
AC	Alternating Electric Current
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
C2C	Chip to Chip
C2W	Chip to Wafer
CD	Critical Dimension
CMOS	Complementary Metal-Oxide-Semiconductor
CMP	Chemical-Mechanical Polishing
$C_{ox}$	Accumulation Capacitance
CTE	Coefficient of Thermal Expansion
CV	Capacitance-Voltage
DC	Direct Electric Current
DRIE	Deep Reactive-Ion Etching
ECP	Electro-Chemical Plating
EDA	Electronic Design Automation
EDX	Energy-dispersive X-ray Spectroscopy
eG	Electro-Grafting
EM	Electromigration

F2F	Face to Face
FA	Failure Analysis
FEA	Finite Element Analysis
FIB	Focused Ion Beam
HF	High Frequency
IC	Integrated Circuit
I/O	Input/Output
ITRS	International Technology Roadmap for Semiconductors
IV	Current-Voltage
KOZ	Keep-Out-Zone
MOS	Metal-Oxide-Semiconductor
PETEOS	Plasma Enhance Tetraethylorthosilicate
PEVCD	Plasma-Enhanced Chemical Vapor Deposition
PoP	Package-on-Package
PVD	Physical Vapor Deposition
$Q_f$	Fixed Charge
RC	Resistance-Capacitance
RF	Radio Frequency
SACVD	Sub-Atmospheric Chemical Vapor Deposition
SEM	Scanning Electron Microscope
SoC	System-on-Chip
TaN	Tantalum Nitride
TCV	Through-Chip-Via
TEM	Transmission Electron Microscope
TEOS	Tetraethylorthosilicate

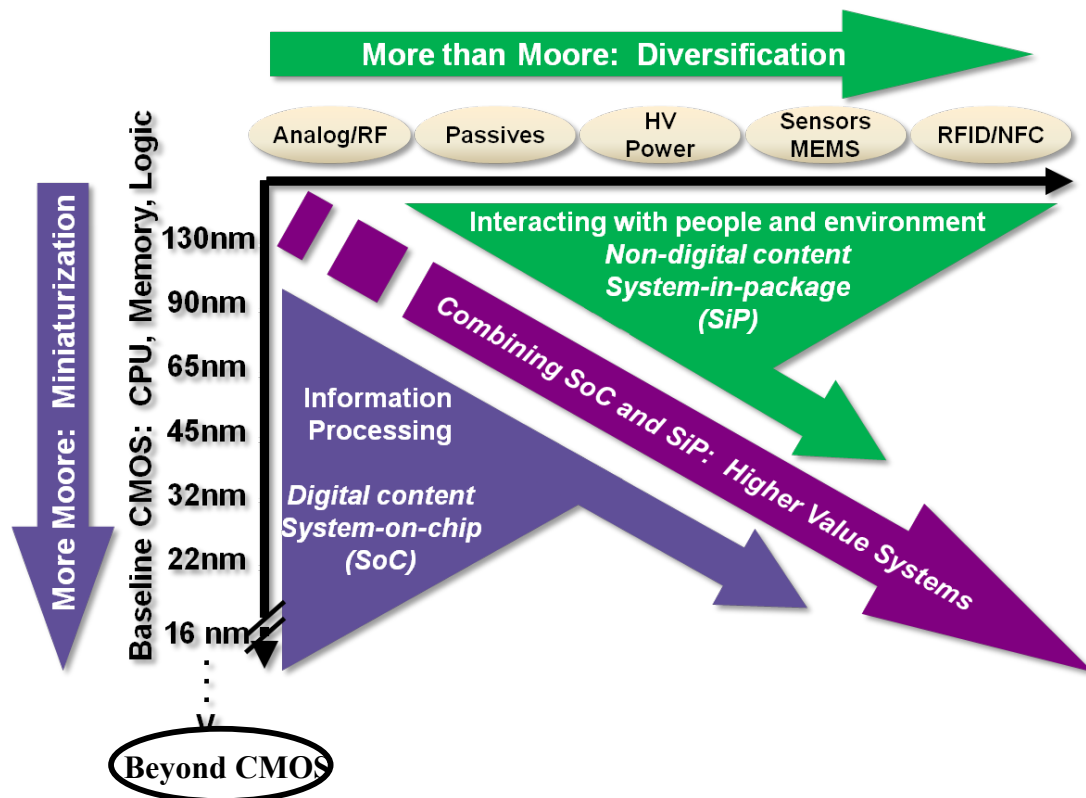
TMA	Tri-Methylaluminum
TSV	Through-Silicon-Via
$V_{FB}$	Flat-Band Voltage
W2W	Wafer to Wafer

# Chapter 1: Introduction

## 1.1 Background

Over the past few decades, technology advancement of electronic devices has been dramatically developed and progressed. Nowadays, people are becoming fans of portable iPad/iPhone with thousands of applications catering to entertainment and business. It is hard to imagine that just twenty years ago, people were using bulky desktops and the idea of portable devices was a fantasy.

Moore's law provides the guidance for the device dimension scaling. However, the conventional device scaling has become challenging due to fundamental and economic limits. Hence, people are looking for solutions beyond the 20 nm technology node. In addition, besides the size scaling limitations, the resistance-capacitance ( $RC$ ) delay issue in interconnects is of concern as well when the total interconnection length has become longer due to larger chip sizes and a constant increase in the number of transistors. Therefore, instead of conventional geometrical scaling, people are exploring the possibility to use the vertical dimension, which is popularly known as the three-dimensional integrated circuit (3D IC). The 3D IC enables vertical access between ICs, and by vertically stacking multiple ICs significantly increases system integration in order to meet the increasing demands of system performance growth ("More Moore") and functionality diversification ("More than Moore") [1.1]. Figure 1.1 illustrates the contents and relationships between "More Moore" and "More than Moore". Instead of planar wiring for different functional blocks, vertical interconnections between adjacent stacking layers will significantly decrease the global interconnect length which in turn reduces the  $RC$  delay.



**Figure 1.1: Illustration of "More Moore" and "More than Moore". "More Moore" focuses on the device miniaturization, "More than Moore" focuses on the device functional diversification [1.1].**

3D IC have gained widespread recognition due to the advantages it provides beyond conventional scaling limits. It provides advantages in the form factor, density, heterogeneous integration, low cost and performance enhancement (reducing signal propagation delay and power consumption) [1.2]. The practical exploitation of the third dimension is usually accomplished with a combination of wire bonding [1.3] and through-silicon-via (TSV) [1.4]. The high aspect ratio TSV is usually fabricated by deep silicon etching, dielectric layer deposition as the lining for electrical isolation, and super-conformal filling with copper; this forms a metal-oxide-semiconductor (MOS) structure [1.5]. Despite its advantages, the

integration of TSVs poses challenges in mechanical stress [1.6] and electrical parasitic [1.7]. Although TSVs provide vertical interconnections between different layers, it differs from the conventional planar interconnects that are embedded in the dielectric layer. The TSV is instead embedded in the Si substrate and isolated using a dielectric liner, which makes it electrically coupled with the Si substrate. Hence, a MOS structure is formed where the metal core (copper) of TSV acts as the gate in an MOS capacitor, and results in the accumulation, depletion and inversion regions in a typical TSV's capacitance-voltage ( $C-V$ ) curve.

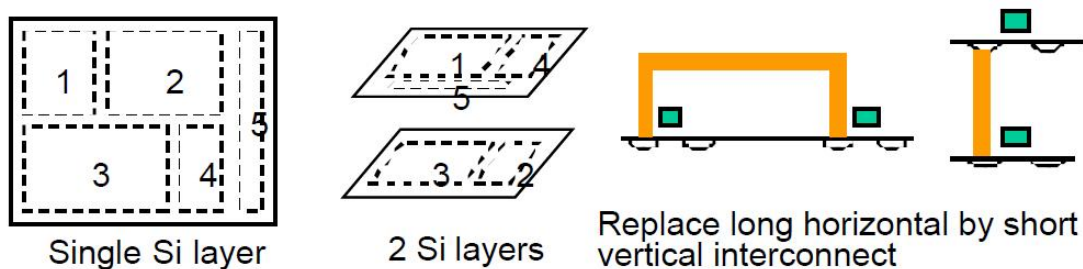
The TSV parasitic capacitance has the most predominant impact on circuit operation [1.7]. It is essential to keep the TSV capacitance as small as possible, and for this purpose the usage of a low- $\kappa$  dielectric for the liner could provide significant reduction in complimentary metal-oxide-semiconductor (CMOS) backend capacitance and offer many circuit performance advantages [1.8]. In principle, integration of a low- $\kappa$  dielectric into the TSV as the liner can definitely reduce down the TSV capacitance. At the same time, a stable TSV parasitic capacitance is desired when there's non-uniform heating which causes hotspots across the chip. Process tuning and material selection can introduce beneficial negative fixed charge in the TSV liner to shift the TSV CV curve so that during operating voltage of interests ( $\sim 0-5V$ ), the TSV exhibits only an accumulation capacitance which is stable and independent on the substrate dopant concentration, small signal frequency or temperature fluctuation.

Furthermore, thermal management is another challenge facing 3D IC. Hence, TSVs can also be designed as passive heat removal elements embedded in the 3D IC stacks owing to the good heat conduction properties of the Cu core and Si substrate. However, the thermo-mechanical stress induced in the Si substrate due to coefficient of thermal expansion (CTE) mismatch of Cu and Si is another potential reliability issue. In addition, it can also lead to a shift in the electron/hole mobility of silicon in the vicinity of TSVs [1.9, 1.10].

## 1.2 Motivation for the Development of Three-Dimensional Integrated Circuit (3D IC)

### 1.2.1 RC Delay Improvement

Moore's law was formulated implicitly considering only two-dimensional (2D) lithography scaling and integration of all functions on a single chip, perhaps through system-on-chip (SoC). When the area is scaled down, this leads to a decrease in the interconnecting lines width which causes the line resistance to increase. On the other hand, when the interconnect pitch is scaled down, the length will increase; therefore, when combined together, both effects of scaling down will lead to a higher  $RC$  delay. Figure 1.2 illustrates how a vertical interconnection can provide for a much shorter global interconnect between vertically stacked ICs, hence reducing the  $RC$  delay.



**Figure 1.2:** Illustration of going 3D by replacing conventional 2D shows  $RC$  improvement due to shorter vertical interconnect length [1.11].

### 1.2.2 Higher Circuit Density

Another crucial advantage offered by 3D IC is that it enables to increase the circuit density but without any necessary 2D lithography down scaling effort. Figure 1.3 shows how Samsung has applied 3D integration to realize a 16 Gbit memory device that consisted of eight vertically stacked NAND flash dies, with each die 50  $\mu\text{m}$  thick and with a capacity of 2 Gbit [1.12]. The stacking was achieved and realized by utilizing TSVs and microbumps as shown in Figure 1.3. The density of this stacked device is, therefore, 8 times larger than that of the single die, yet resulting in a final stack thickness of only  $\sim 560 \mu\text{m}$ ; this is even thinner than the thickness of wafer before back grinding. The total length of the equivalent global interconnects is obviously significantly reduced due to replacing the conventional planar interconnecting wires with the vertical interconnects. This results in an approximately 30% increase in the performance due to the reduced electrical resistance.

More active IC layers could be stacked using the existing technology node. Figure 1.4 shows schematically a comparison between conventional wire bonding and vertical interconnect using TSV.

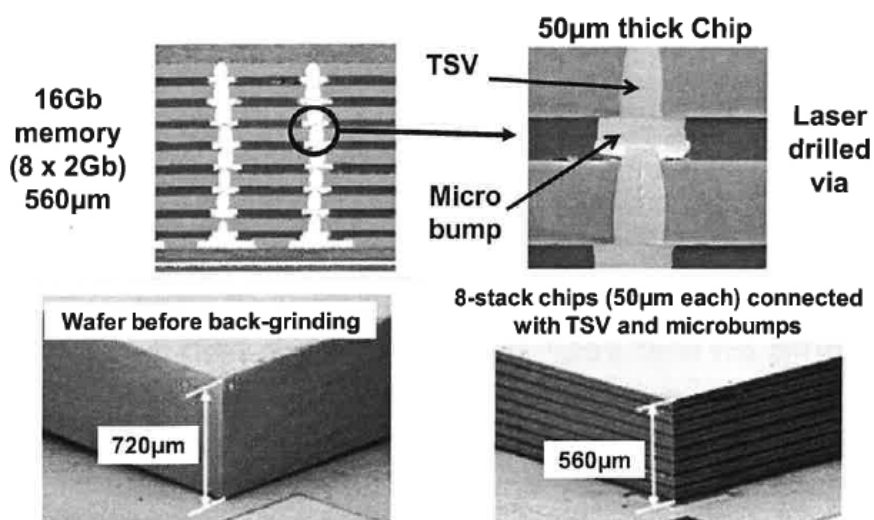


Figure 1.3: 3D IC application: 8 stacked NAND flash memory by Samsung [1.12].



**Figure 1.4: Schematic of wiring bonding and vertical interconnect using TSV. It is evident that the vertical interconnect provides a much shorter interconnect length [1.12].**

### ***1.2.3 Other Advantages of 3D ICs***

Beside the *RC* delay and circuit density enhancement, 3D ICs can also provide several other advantages, such as:

- a) Bandwidth enhancement with wide input/output (I/O) interfaces: 3D interconnects implementation provides the opportunity to place the memory chip on top of the logic device, in this way the number of I/O channels extend to the whole chip area;
- b) Smaller form factor: reduction in chip footprint without sacrificing the packing density;
- c) Performance enhancement: the 3D architecture offers flexibility in system design, functional placement and wire routing, and it also significantly reduces interconnect delay and power consumption;
- d) High volume low cost production: reduction of processing complexity and integration costs; and
- e) Heterogeneous integration: it enables multifunctional devices to be implemented with low cost and small footprint.

Even with the benefits listed above, just like any other new technology, 3D ICs also face challenges such as: TSV formation, thermal management, thermo-mechanical stress, thin wafer handling, bonding environment, wafer to wafer (W2W) bonding alignment, contact performance, testing as well as electronic design automation (EDA) needs. All these issues should be well addressed and solved in order to achieve mass production for 3D IC to be adapted by the semiconductor industry.

### 1.3 Scope of Research

This project entails a comprehensive study on the TSV design, fabrication and its integration in 3D IC process flow, in the context of electrical characterization (such as capacitance-voltage ( $C-V$ ) and current-voltage ( $I-V$ ) measurements to control and improve the TSV performance in terms of capacitance stabilization and reduction, leakage current improvement; thermal property study to demonstrate that TSV arrays can be used as passive heat removers; reliability study (such as thermo-mechanical stress modelling and measurement by micro-Raman analysis) to control and mitigate the Cu-TSV induced stress.

The detailed scopes and objectives of the project are listed below:

1) Advanced TSV process development:

The main TSV process consists of deep reactive-ion etching (DRIE) Si etch, liner plasma enhance chemical vapor deposition (PECVD) deposition, Ta barrier/Cu seed layer physical vapor deposition (PVD) and Cu electroplating (ECP) filling. The following requirements should be met for a robust TSV structure:

- a. Minimized scalloping roughness resulted after the BOSCH DRIE process;
- b. Conformal liner deposition;
- c. Full Cu filling without voids or delaminations.

2) Electrical characterization of TSV liners:

The electrical characterization of fabricated TSVs is carefully carried out, particularly with respect to parasitic capacitance and leakage current, since the primary role of TSV is to provide inter-layer connectivity.

3) Thermal property of TSV:

Formation and placement as well as characterization of thermal TSV in a 3D IC stack to demonstrate TSV arrays as an effective heat removal element.

4) Cu-TSV induced thermo-mechanical stress study:

Modeling of and measurement on the fabricated TSV samples to study and mitigate the stress induced in the Si substrate.

## 1.4 Organization of Thesis

The organization of this thesis is as follows. Chapter 2 presents the literature review study about 3D IC technology which includes a discussion on 3D packaging and 3D integration. The TSV process and its related issues are then presented in detail. In addition, the properties of low- $\kappa$  dielectrics which can be used in TSV are briefly discussed. Finally, TSV electrical modelling and characterization as well as Cu-TSV induced thermo-mechanical stress are presented.

In Chapter 3, we describe the wafer layout and mask design prior of the TSV device designs. Subsequently, the fabrication process flows for electrical characterization and thermal property study are presented, which also include the TSV fabrication and process related results.

In Chapter 4, we present the electrical characterization of the TSV, which includes the electrical measurement setup and testing methodology. The electrical characterization comprised of  $C$ - $V$  and leakage current measurements of TSV with PETEOS oxide liner, low- $\kappa$  liner, novel bi-layer of  $\text{Al}_2\text{O}_3$  and oxide liner, and novel bi-layer of  $\text{Al}_2\text{O}_3$  and low- $\kappa$  liner are presented.

In Chapter 5, the thermal properties of TSV are discussed. We then show the modelling and measurement results by micro-Raman analysis of Cu-TSV induced thermo-mechanical stress. Stress control and mitigation is achieved by utilizing a low- $\kappa$  material as the TSV dielectric liner.

Chapter 6 summarizes the doctoral project, concludes the contributions and recommends future work.

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# Chapter 2: Literature Review

## 2.1 Three-Dimensional Integrated Circuit (3D IC) Technology

Ever since the invention of the transistor by Bardeen, Brattain and Shockley in 1947, and the invention of the silicon (Si) integrated circuit (IC) by Jack Kilby of Texas Instruments in 1958, an explosion in the development of electronic devices occurred. In 1965, Gordon Moore proposed the doubling of the number of transistors in an IC every 18 months. This proposal became widely known as the famous Moore's Law, and has been the most powerful driver for the microelectronic industry over the past 50 years. The significance of this law implied that development has to focus on the scaling of two-dimensional (2D) lithography, and the integration of all functions, such as memory and processor, on a single chip, an approach known as system-on-chip (SoC). Aggressive scaling has been done via the lithography approach over the years but recently it seemed that this approach is slowly reaching its limits [2.1]. Hence, the following of Moore's Law has shifted gradually to using 3D integration. 3D integration allows the vertical stacking of active devices to increase the transistors density as opposed to the conventional method of packing transistors in a 2D form. Besides the improved density, there are also other advantages which include the lower  $RC$  delay, lower power consumption and the feasibility of heterogeneous integration.

Yole Development released the roadmap of 3D IC applications shown in Figure 2.1. It shows various 3D IC applications with more different functionalities integrated together from 2006 to 2016. This will require the use of more complex and higher density of 3D interconnects to realize the projection. It is worth pointing out that in order to achieve the final "full 3D IC" plan and the implementation of heterogeneous integration, the development of interconnects with minimum pitch of  $< 10 \mu\text{m}$  is essential [2.3].

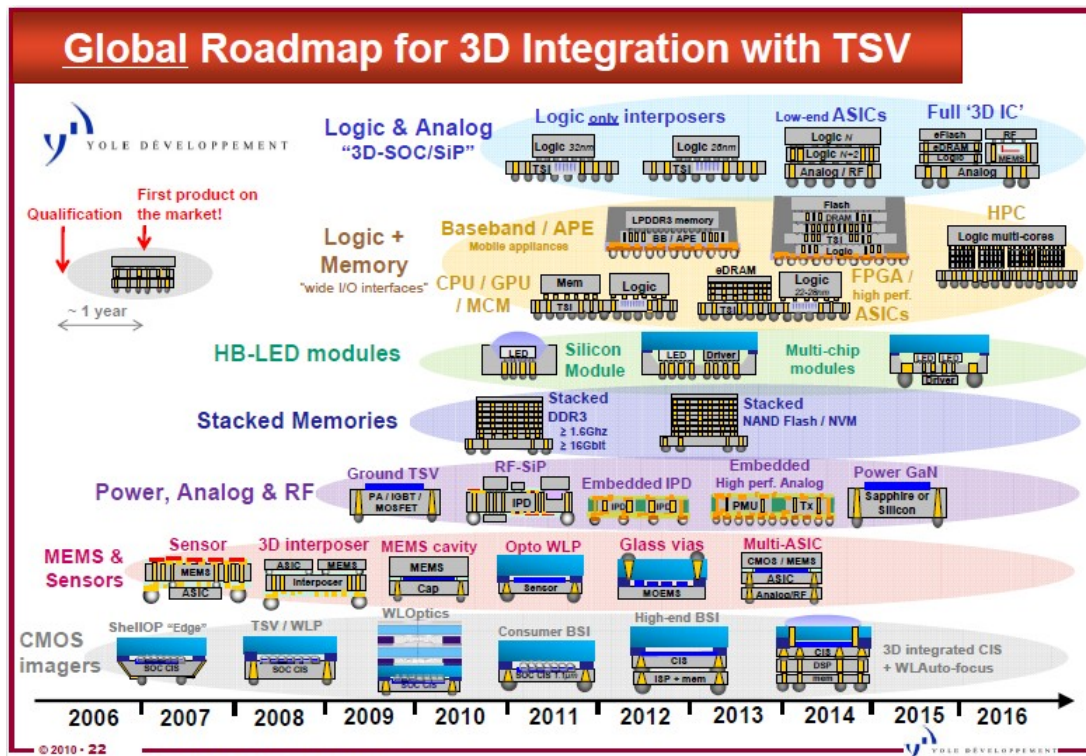


Figure 2.1: Roadmap of 3D IC applications released by Yole Development [2.2].

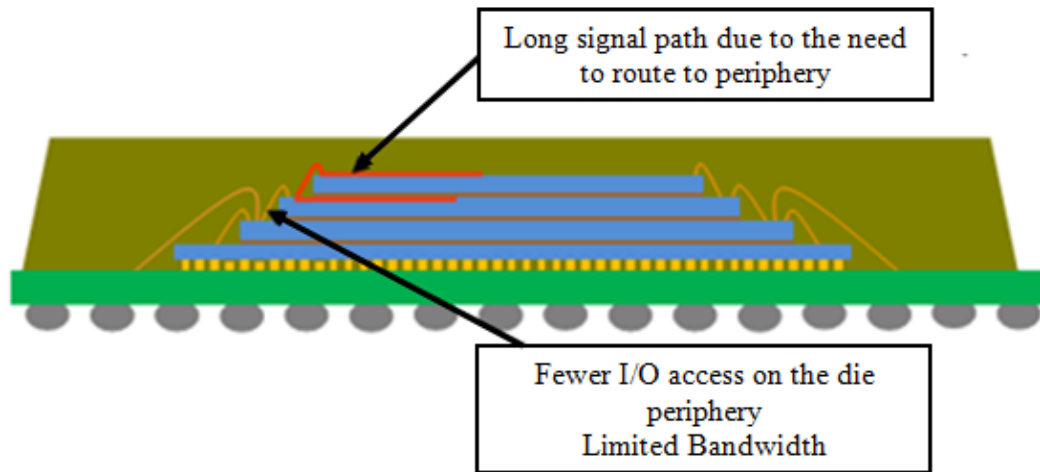
## 2.2 3D Packaging and 3D Integration

3D implementation is classified into two major categories: 3D packaging and 3D integration. 3D integration is further divided into two subcategories, namely 3D IC integration and 3D Si integration [2.4]. Nowadays, industry has adopted 3D packaging for mass production due to the demand of devices with a small form factor. Figure 2.2 shows an example of 3D packaging - 3D stacking of IC chips using wirebonds. In this packaging scheme, Au/Cu wires are normally utilized to connect the input/output (I/O) from the periphery of chip to the substrate. Although this is a very cost effective way of size shrinkage, this method is limited due to small boundary area of the chip [2.5, 2.6].

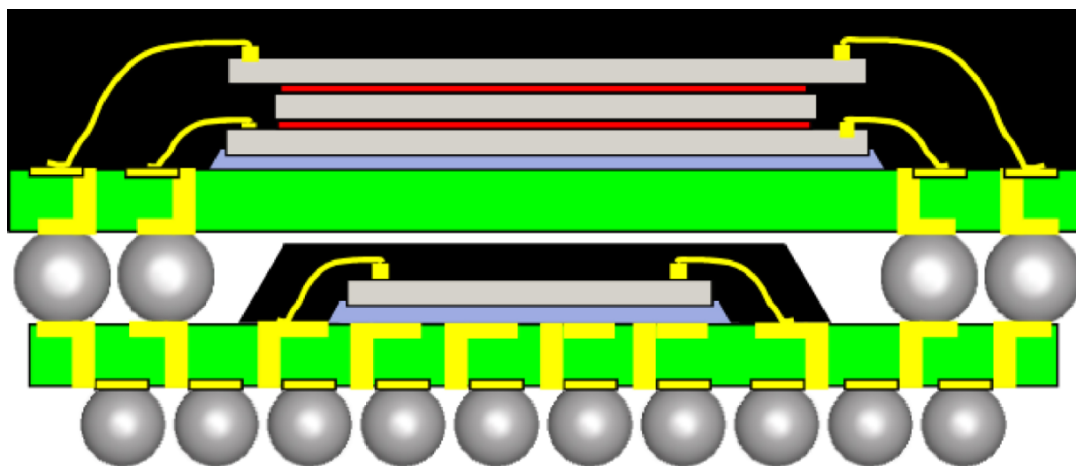
Another example of 3D packaging is the Package on package (PoP) technology shown in Figure 2.3. This packaging scheme is considered the second most important development of 3D packaging technology, and was developed to address the need for an alternate method as well as a more efficient packaging technology. In this scheme, individual packages are integrated in a vertical fashion with flexible fan-outs to the substrate. PoP has a prominent advantage, namely it enables the integration of logic and memory chips on the same package form factor. This can be achieved without the logistics and business-related issues involved with a logic-memory stacked die package. Both methods introduced represent 3D packaging implementations with no through-silicon-via (TSV) used for vertical interconnections.

On the other hand, different from 3D packaging, 3D integration utilizes the TSV as the interconnectors whereas 3D packaging does not involve TSV. 3D integration can be further subcategorized into two groups, namely 3D IC integration and 3D Si integration. 3D IC integration is also known as a More-than-Moore technology where a stack of active

devices are formed using local on-chip interconnects in the vertical direction with TSV and micro-bumps. By doing so, a higher density is achieved without further transistor shrinkage.

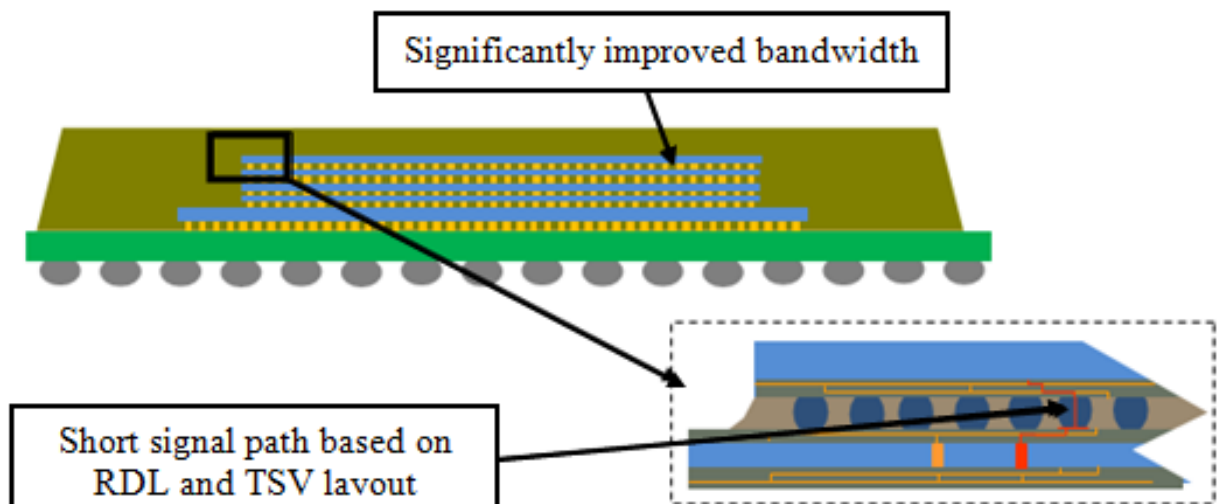


**Figure 2.2: 3D packaging: chips are vertically stacked through wire bonding to connect with the substrate schematic; Long signal path, limited bandwidth and fewer I/O access on the die periphery [2.7].**



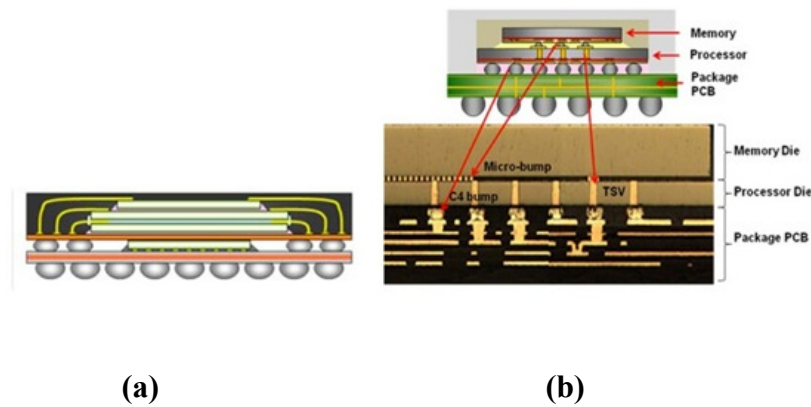
**Figure 2.3: 3D packaging: package on package (PoP) schematic shows that two completed packages are vertically stacked [2.8].**

Figure 2.4 illustrates the use of TSV in the adjacent layer for interconnection, where stacked ICs can be processed separately for different applications, such as a system-on-chip design, which will benefit from a bandwidth enhancement and heterogeneous integration [2.9]. This is supported by the fact that the performance of electronic devices is becoming more interconnect-dominated, and traditional transistor down-scaling and chip size increase result in much longer global interconnects and thus a significantly increased  $RC$  product [2.10]; To counteract the influence of the  $RC$  product, several measures can be taken. First, signals of increased power can be used to compensate the resistance-capacitance coupled effect. Secondly and more efficiently, 3D ICs can be used to separate different functional blocks into different vertical layers to reduce the total interconnect length. As a result, lower  $RC$  delay and power consumption can be expected to improve the overall device performance.

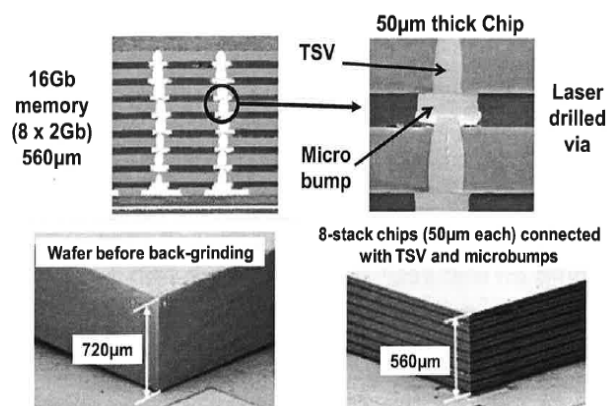


**Figure 2.4: 3D IC integration by utilizing TSV and micro-bumps for interconnections; short signal path and improved bandwidth [2.7].**

In 2006, Samsung has demonstrated 3D stacking of memory using TSV [2.11]. Figure 2.5 (a) and (b) are the comparison between a conventional 3D wirebond packaging method and interchip connection using TSV and micro-bumps respectively. More I/O connections are expected from TSV memory and a much smaller device can be obtained without the use of wirebonds. Figure 2.6 shows scanning electron microscope (SEM) and focus ion beam (FIB) images to confirm the TSV and micro-bumps interconnections. It can also be seen that the overall thickness of the stacked chip is comparable with that of a conventional single memory die.

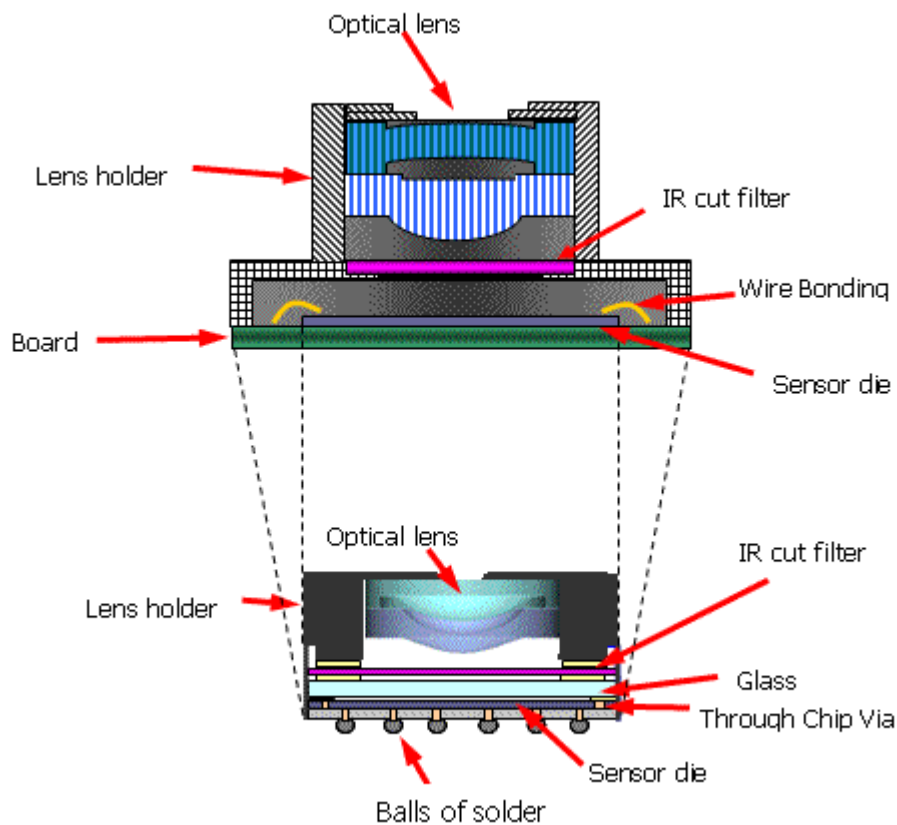


**Figure 2.5: (a) Conventional 3D packaging with wirebond; (b) 3D stacking with TSV memory [2.11].**



**Figure 2.6: SEM/FIB images of a single memory wafer and 8 stacked thin chips with TSV and micro-bumps [2.11].**

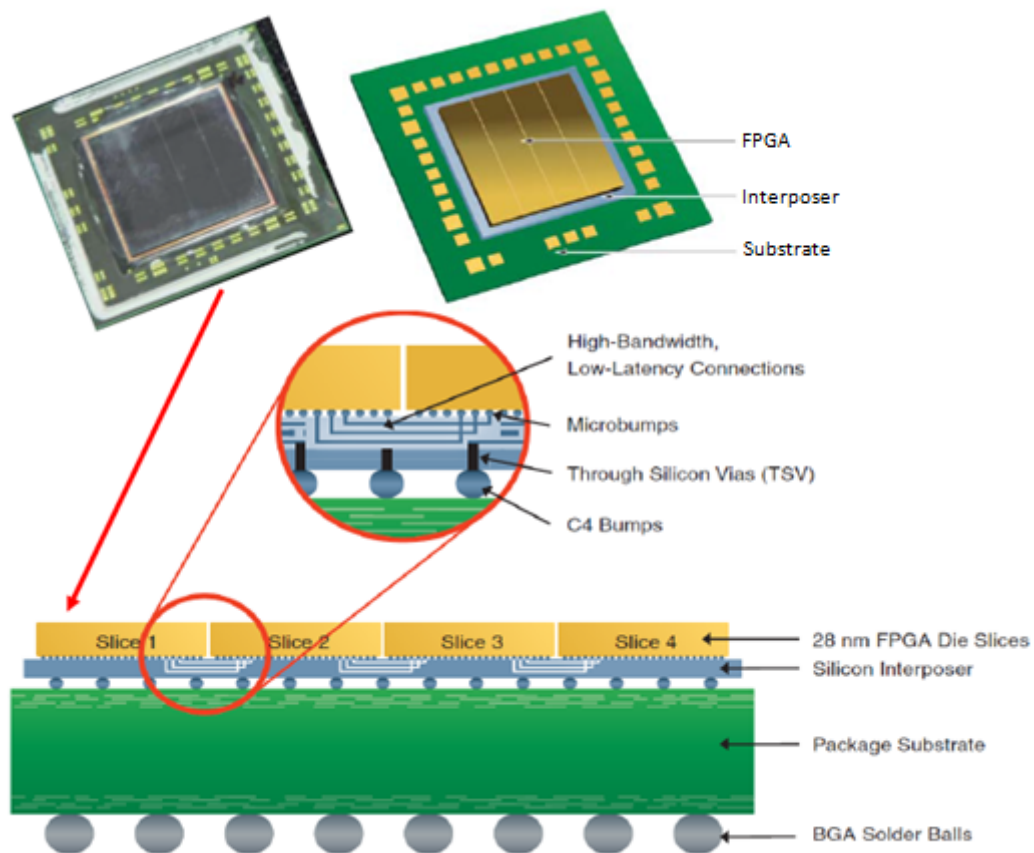
In 2008, Toshiba initiated the world's first mass manufacturing of the CMOS image sensor using 3D integration [2.12]. Through-chip-via (TCV) which is now known as TSV, was used to replace the conventional wirebonding to achieve a much smaller module size. The reduced area was previously required for wirebonding the module to a substrate. Furthermore, through pixel size reduction, it contributed to a module size up to 64% smaller than previous camera modules manufactured (with the same sensors). Figure 2.7 shows the sensor die being interconnected with the upper optical device to form a heterogeneous integration.



**Figure 2.7: 3D TSV integrated CMOS image sensor by replacing wirebonds with through-chip-via [2.12].**

In the midst of developing the area of 3D IC integration, another technology, called TSV interposer, was also developed in parallel and is also known as carrier or substrate 2.5D integration [2.13]. It is worth pointing out that the TSV interposer is not regarded as a transitional technology to 3D integration, but rather as a separate entity. 2.5D TSV interposers can enable packaging of chips in the 32-22 nm nodes where the fragile mechanical stability of the low- $\kappa$  dielectrics used in these products will require their bonding to an intermediate silicon interposer before final placement in a standard package. Figure 2.8 shows Xilinx's 4 FPGAs on a passive TSV interposer [2.14].

3D Si integration, which is popularly considered the right way to go in order to answer Moore's Law, emphasized that there should be no gap between the active layers, and does not involve micro-bumps. Figure 2.9 shows the schematic of a 3D Si integration which



**Figure 2.8: Xilinx's 4 FPGAs on a passive TSV interposer [2.14].**

consists of TSVs, bonding interfaces and four different layers. Unlike 3D IC integration which utilizes chip to chip (C2C), chip to wafer (C2W) or wafer to wafer (W2W) bonding methods, W2W is the only bonding method for 3D Si integration. As shown in Figure 2.10, W2W bonding can be achieved by implementing a SiO<sub>2</sub>-SiO<sub>2</sub> direct bonding or a Cu-Cu direct bonding. Since the TSV fabrication yield loss is higher due to a smaller TSV size (diameter < 1.5µm) and the requirement of a stricter bonding condition, the 3D Si integration is still in upstream research development stage.

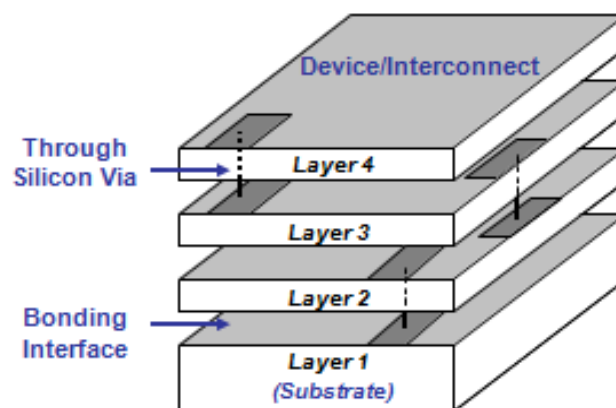


Figure 2.9: Schematic of 3D Si integration [2.10].

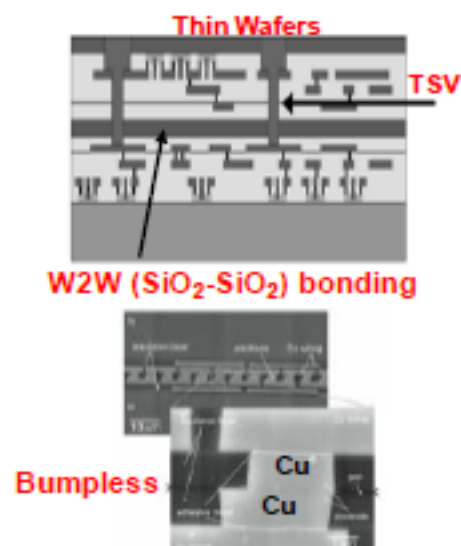


Figure 2.10: 3D Si integration by utilizing W2W bonding (SiO<sub>2</sub>-SiO<sub>2</sub> or Cu-Cu direct bonding) which is bumpless [2.15][2.16].

### 2.3 Through-Silicon-Via (TSV) Fabrication Process

Through-Silicon-Via is considered the key enabler for 3D integration. Figure 2.11 shows the three different types of TSV fabrication integration technologies, with each of them possessing its own individual advantages as well as integration problems [2.17-2.20]. The fabrication process of TSV mainly consists of a deep reactive ion etch (DRIE) for via formation, followed by a dielectric liner deposition using either plasma enhanced chemical vapor deposition (PECVD) or thermal oxidation for oxide liner, barrier and seed layer deposition by physical vapor deposition (PVD) or electro-grafting (eG), via filling by Cu electroplating (ECP), and finally a chemical mechanical polishing (CMP) process for Cu plating overburden removal [2.21]. Figure 2.12 shows a basic TSV process consisting of the 5 steps listed above [2.22].

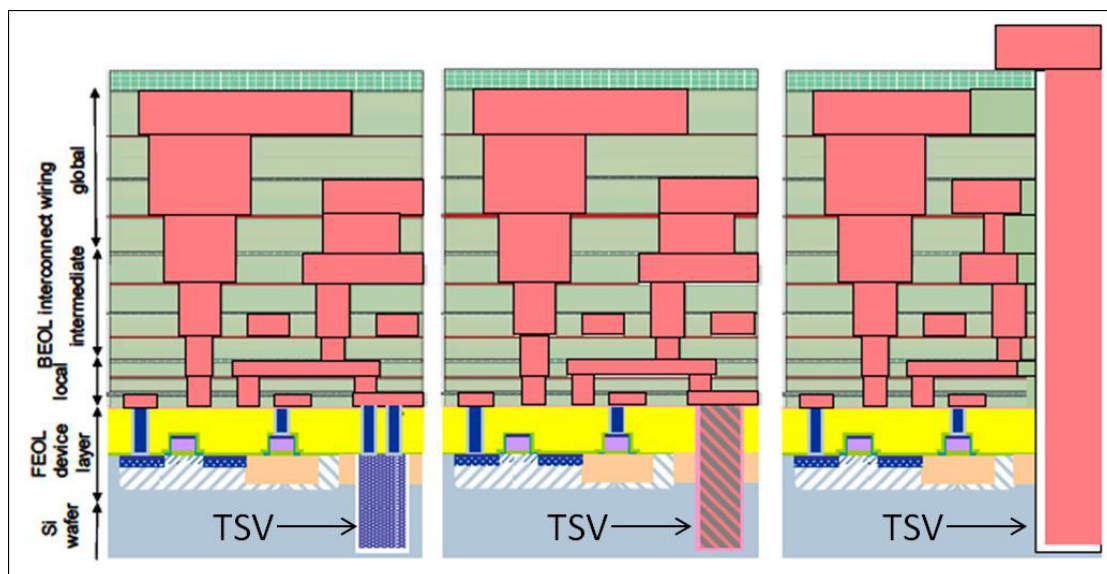
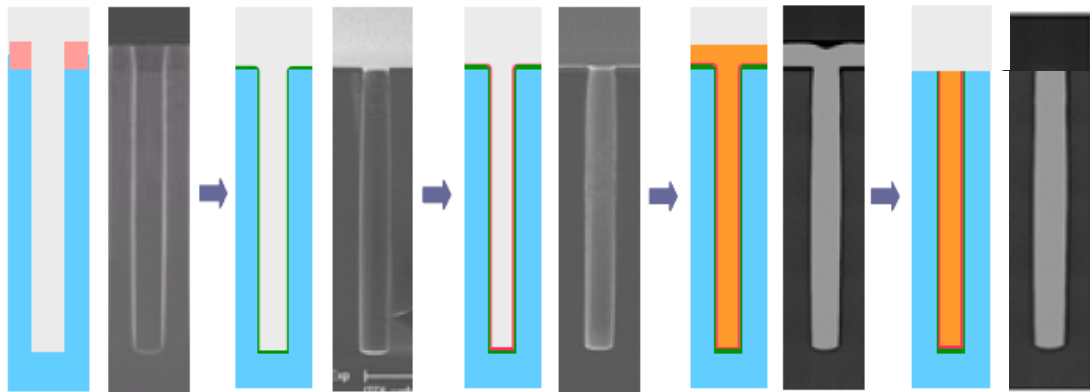


Figure 2.11: Schematics of via-first, via-middle and via-last 3D integration [2.17].



**Figure 2.12: TSV basic 5 process steps [2.22]: DRIE Si etching, dielectric liner deposition, barrier and seed layer deposition, Cu ECP and Cu CMP.**

### ***2.3.1 Deep Reactive Ion Etching (DRIE) Si Via Etch***

The most often used Si DRIE processes are those developed by BOSCH and Surface Technology Systems (STS), who also sell the equipments. Si DRIE is the key process that is used for via formation. Figure 2.13 shows the photo image and schematic of a STS ICP (inductive charged plasma) machine consisting of a single chamber and manual loadlock system platform.

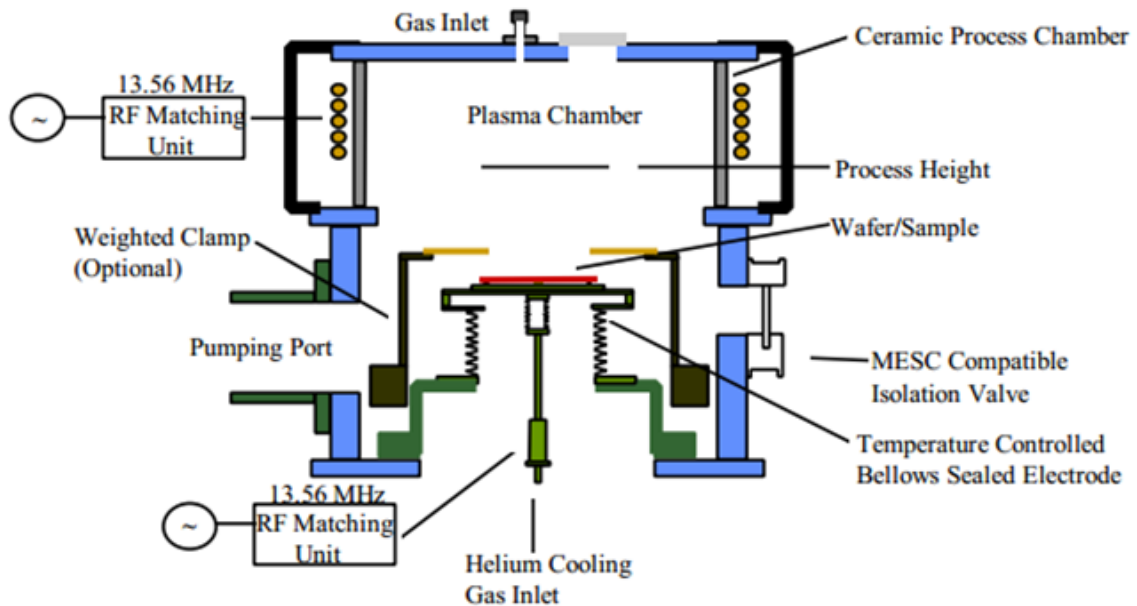


Figure 2.13: Photo image and schematic of STS ICP machine for DRIE Si etch [2.23][2.24].

The BOSCH process is commonly used for deep Si etching while reducing the slope of the side wall. It is a room temperature process which uses photoresist or silicon dioxide as etch mask. The process involves alternating etch and passivation steps - during the etch step,

SF<sub>6</sub> plasma is used to etch quickly and isotropically the Si; during the passivation step, C<sub>4</sub>F<sub>8</sub> plasma is used to form a protective polymer coating on the trench's sidewalls, and before the next round of etching step, C<sub>4</sub>F<sub>8</sub> is removed (Figure 2.14). However, the drawback of this process to achieve a vertical sidewall is the effect of scalloping. In order to have a robust TSV, the sidewall scalloping effect should be kept as small as possible. If the scalloping is too significant, it would be a challenge for the subsequent dielectric liner deposition process to be conformal and may lead to high leakage during operation. Similarly, it would also be a challenge for a conformal barrier and copper seed layer deposition which may lead to incomplete Cu filling in the via hole. Hence, a good DRIE etch process has the following requirements:

- 1) Sidewall scalloping roughness as small as possible;
- 2) Via should be formed vertical or slightly tapered;
- 3) Via uniformity should have less than 5% variation across the whole wafer;
- 4) Via forming speed should be reasonable.

Figure 2.15 shows vias formed by using a DRIE process with a diameter of 5 μm and a depth of 50 μm. The TSV has an 89° tapered wall which is reported to be better for subsequent Cu seed layer deposition as well as Cu ECP filling [2.22].

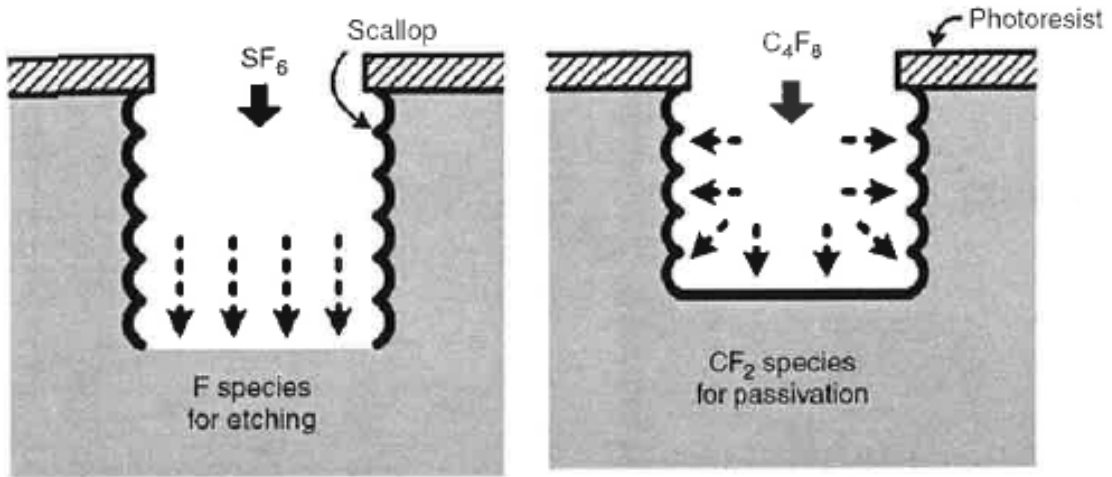


Figure 2.14: BOSCH DRIE process alternates a Si etching cycle and a sidewall passivation cycle [2.22].

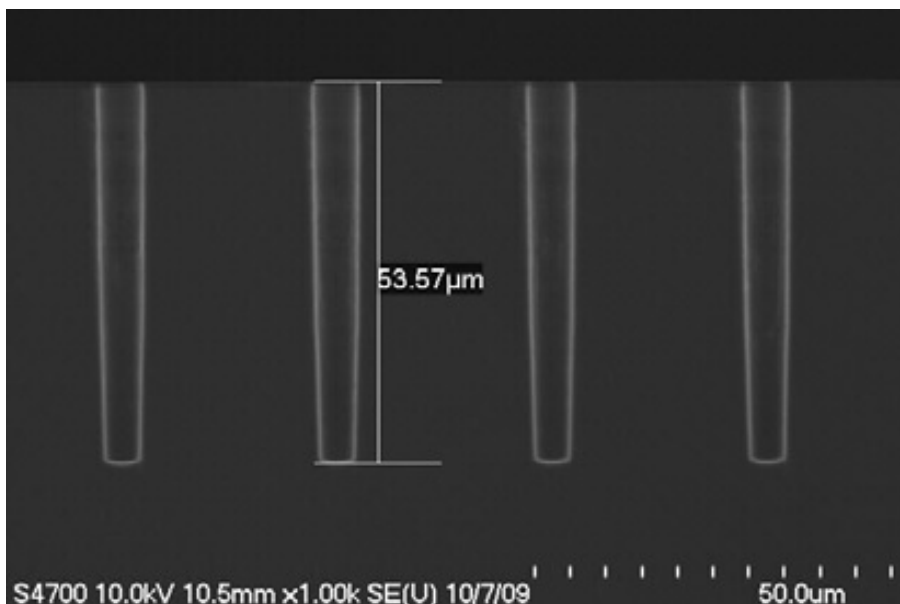
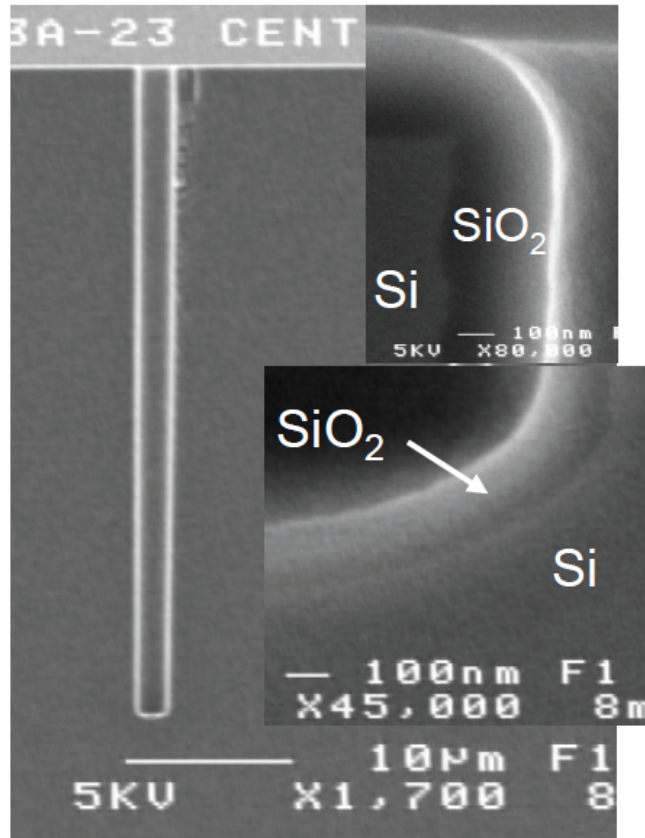


Figure 2.15: Via formation after BOSCH DRIE process with a diameter of 5  $\mu\text{m}$  and a depth of 50  $\mu\text{m}$  [2.22].

### 2.3.2 Dielectric Liner Deposition

SiO<sub>2</sub> is commonly used as the dielectric liner in TSV to isolate the metal core of TSV from the silicon substrate. A good dielectric liner is desired for ensuring a small leakage current between TSV and the substrate, hence conformality is a critical consideration. There are two methodologies for forming the via, namely the via-first and via-middle approach. In both approaches, thermal oxidation or sub-atmospheric chemical vapor deposition (SACVD) O<sub>3</sub>-TEOS (Tetra-Ethyl-Ortho-Silicate) oxide can be used to achieve a very conformal dielectric layer. However, as the operating temperature is relatively high, such deposition methods are not compatible with backend processing. For the via-last process, using plasma enhanced chemical vapor deposition (PECVD) for depositing the SiO<sub>2</sub> dielectric is a better choice due to its lower thermal budget (250°C to 400°C). However, using this method, non-conformal filling of sidewall is an issue. In order to be compatible with the backend process, a lower temperature < 350°C is desired. Other possible dielectric candidates such as thermal CVD of Si<sub>3</sub>N<sub>4</sub> and atomic layer deposition (ALD) Al<sub>2</sub>O<sub>3</sub> are also discussed in literature [2.25]. Thermal CVD of Si<sub>3</sub>N<sub>4</sub> is attractive owing to excellent deposition conformality and dielectric performance, but the film is highly tensile and the integrity of the film in the via hole may cause a problem. ALD can provide excellent conformal dielectric deposition, however, Al<sub>2</sub>O<sub>3</sub> is not readily integrated into front end of line (FEOL) IC processing. Figure 2.16 shows that the SACVD O<sub>3</sub>-TEOS oxide liner has a step coverage of 50% at the bottom of the TSV. Positive fixed charge induced in PECVD oxide liner is commonly observed from the deposition process. This can cause a shift in the TSV capacitance as observed in the *C-V* curve, and should be controlled. At the same time, the controlled fixed charge in the liner material can be used to achieve the desired TSV capacitance performances [2.26].

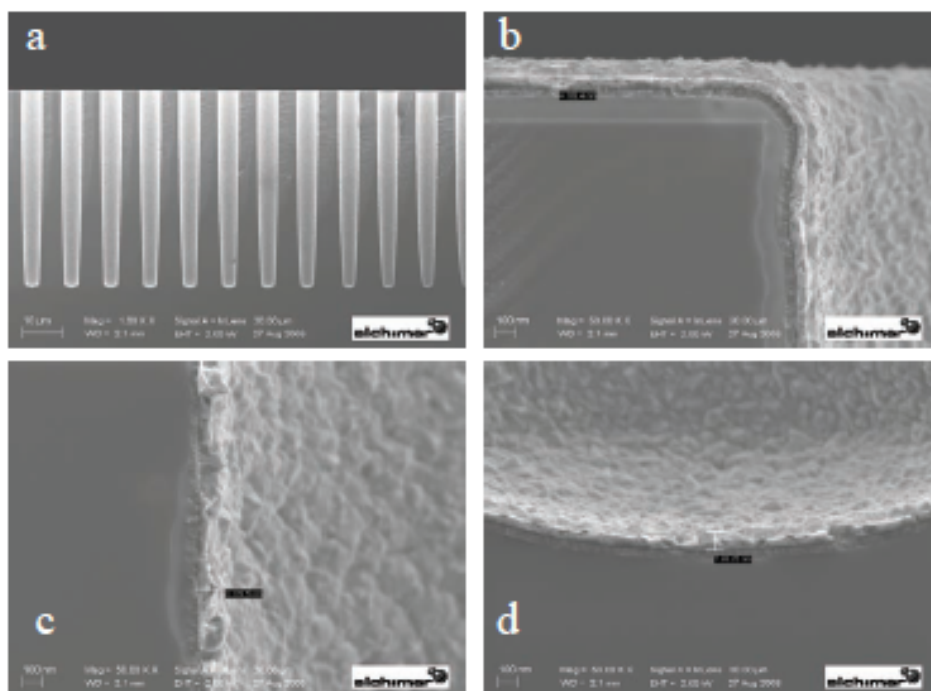


**Figure 2.16: SACVD O<sub>3</sub>-TEOS oxide process shows 50% step coverage at the TSV bottom [2.25].**

### ***2.3.3 Barrier and Seed Layer Deposition***

The barrier/adhesion layer and Cu seed layer can be deposited by physical vapor deposition (PVD) sputtering. Usually higher supply power can increase the adhesion and provide better sidewall coverage. Conformality and continuity of the deposited metal are critical for the subsequent Cu electroplating process. Prior to the PVD sputtering of the metal, a pre-cleaning process using Ar plasma to bombard the wafer surface is critical to clear the surface of any contaminants. However, due to the fundamental limitations of copper PVD seed coverage in high aspect ratio TSVs, the use of another method – the electrografting (eG) process is a potentially better candidate due to its inherent ability to produce surface-initiated conformal

films on any conducting or semiconducting materials. It was further reported by Alchimer that copper seed layers formed using eG in a TSV trench meet all key unit process requirements such as conformality, resistivity, adhesion and low contaminant levels [2.27]. Figure 2.17 shows the example of eG Cu seed deposited in  $5\mu\text{m}\times 50\mu\text{m}$  TSVs coated with CVD TiN, which has a step coverage of eG copper seed close to 90% [2.27].



**Figure 2.17: SEM cross section of eG copper deposited in  $5\mu\text{m}\times 50\mu\text{m}$  TSVs coated with CVD TiN: a) overview; b) top (109 nm of eG copper); c) sidewalls (129 nm of eG copper); d) bottom (98 nm of eG copper); a step coverage of eG copper seed close to 90% [2.27].**

#### **2.3.4 Cu Electroplating (ECP)**

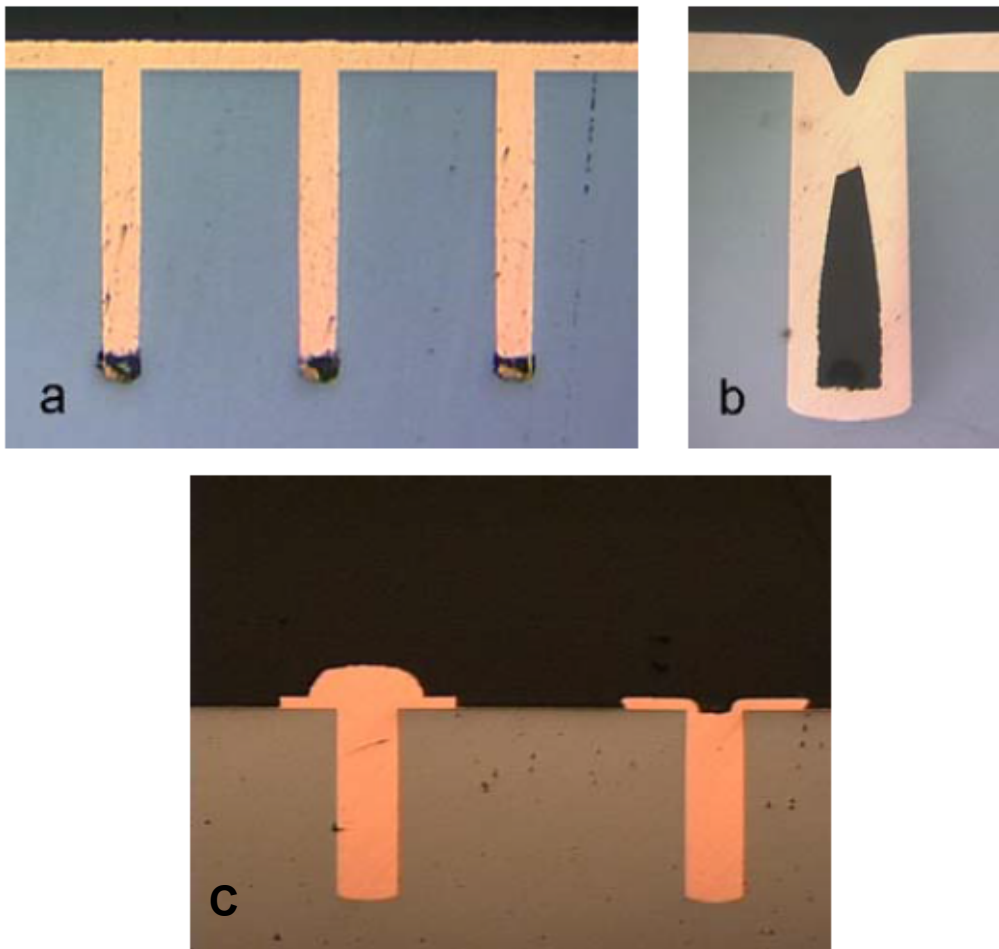
Next in the TSV formation is the filling of the via hole with Cu. Cu is commonly used as the core of the TSV in 3D integration due to its electrical properties, such as low resistivity and reduced electromigration (EM). In order to have a void-free TSV filled with Cu, bottom-up electroplating is commonly used. The plating current is the most important parameter in ECP. While a small current (e.g., 0.1 A) will help to achieve a better via filling especially for high aspect ratio vias, the trade off lies in the slower plating speed. In addition, other plating solution components, such as the suppressor, the leveler and the accelerator are all critical control factors for a good process. The suppressors are typically polyalkylene glycol type polymers which are used to improve the morphology and profile of the via filling. Secondly, the levelers are typically alkane surfactants containing sulfonic acids and amine or amide functionalities; these are also used to improve the morphology. Lastly, the accelerators are typically sulfur derivatives of propane sulfonic acid which are used to brighten the plated Cu color and to preventing it from oxidation under ambient conditions. Besides the plating current and its chemistry, pre-treatments (such as wetting, DI rinsing) and the addition of a pre-absorbing accelerator are also essential in achieving a void-free filling. Furthermore, the uniformity of the plating can also be improved by solution agitation and rotating the wafer during the process.

Figure 2.18 shows various Cu filling defects which include bottom void, pinch off, and Cu mound [2.28]. All these defects can have a serious effects on TSV interconnect properties and the subsequent processes. Voids in TSV may cause higher TSV resistance or even open vias. In addition, voids may also trap chemicals during the ECP process, and thus may be a reliability hazard. Cu mounds and thick Cu overburden may lead to lengthy chemical mechanical polishing (CMP) process, which will increase the cost and potentially

increase the nonuniformity of the final result. Hence an optimal worthy ECP process should have the following traits [2.28]:

- 1) Void free Cu filling of the vias;
- 2) Fast plating time;
- 3) Minimal overburden; and
- 4) No Cu mound defects on surface.

In the case of 3D Si integration, due to the smaller via size (diameter  $< 1.5 \mu\text{m}$ ), tungsten (W) is usually used and is deposited by a CVD process using  $\text{WF}_6$  and  $\text{H}_2$  gases [2.25].



**Figure 2.18: Various TSV Cu ECP defects: a) voids at bottom; b) via pinch off; c) Cu mound [2.28].**

### 2.3.5 Cu Chemical and Mechanical Polishing (CMP)

The excess Cu layer on top of the TSVs from the previous Cu electroplating process is known as the Cu overburden and it is removed by the chemical and mechanical polishing (CMP) process. Figure 2.19 shows the schematic of the typical CMP tools, which consists of a rotating and extremely flat platen covered by the polish pad. The wafer that is being polished is mounted upside-down in a wafer carrier on a backing carrier film. The process uses an abrasive and corrosive chemical slurry in conjunction with the polishing pad. The pad and wafer are pressed together by a dynamic polishing head. The dynamic polishing head is rotated with different axes of rotation to even out any irregular topography. The slurry flow rate and down force should be optimized to achieve high removal rate, better uniformity and less stress. The head speed should be 1 to 2 times the table speed.

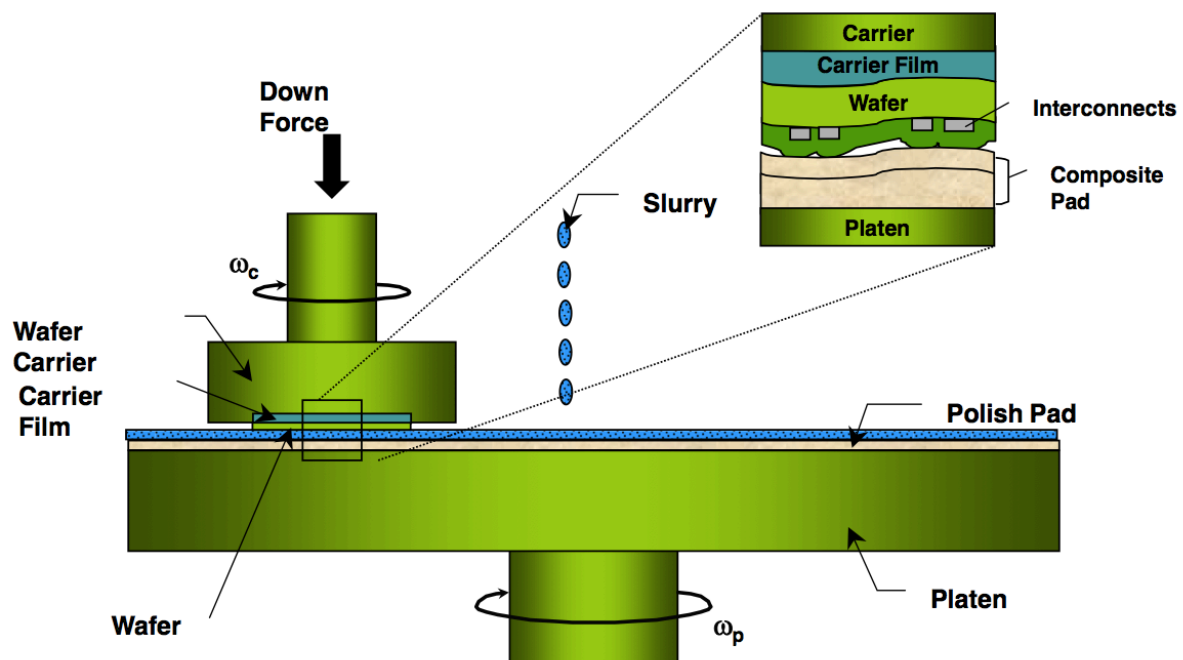


Figure 2.19: Schematic of the typical CMP tools [2.29].

The CMP process for TSV has its own challenges [2.30]. Due to the dimensions of the TSV, its Cu filling normally results in more overburden than that occurring for standard Cu interconnects and this may result in a longer CMP process time. When Cu filling defects are present, such as Cu mounds, the CMP process may be even more complicated. Annealing is usually performed to reduce the wafer warpage [2.28].

## 2.4 Low- $\kappa$ Dielectric Property

Large signal delay and high power consumption are the two important issues industry is facing as we move on to the nanometer regime. Presently, Cu has become the common metallization material which reduces the resistance. In order to also decrease the capacitance and thus reduce the  $RC$  delay, low- $\kappa$  materials which can impact the interconnect capacitance are hence being intensively studied. The usage of a low- $\kappa$  dielectric can significantly reduce the complementary metal-oxide-semiconductor (CMOS) backend interconnect capacitance and provide many advantages in circuit performances in deep submicron technology nodes [2.31]. Since low- $\kappa$  dielectric deposition process is compatible with the TSV process, it can be used in principle to reduce the TSV capacitance. On the other hand, power consumption is contributed by two components. Firstly, the dynamic power dissipated in the interconnects which depends on the capacitance of the interconnects, and secondly, the static power dissipation, which is related to the leakage current between interconnects. Hence, in order to have a robust dielectric, a low- $\kappa$  dielectric with low leakage is desired and required.

### 2.4.1 $RC$ Time Constant of Interconnects

The signal delay associated with the interconnects is determined by the  $RC$  time constant. Figure 2.20 shows a capacitor formed by two metal lines and a dielectric layer in between. The capacitance can be calculated as

$$C = \kappa\epsilon_0 LW/d \quad (1),$$

where  $\kappa$  is the dielectric constant of the inter-metal dielectric layer,  $\epsilon_0$  is the permittivity in the vacuum,  $L$  is the length of the metal line,  $W$  is the width of the metal line, and  $d$  is the distance between the two metal lines. The resistance of the metal line is given by

$$R = \rho L/Wt \quad (2)$$

where  $\rho$  is the resistivity of metal line, and  $t$  is the thickness of the metal line. Therefore, the  $RC$  time constant is estimated as

$$RC = \varepsilon_0 \kappa \rho L^2 / dt \quad (3)$$

Hence, it can be seen that a low- $\kappa$  material can be used to reduce the  $RC$  delay since it is proportional to the dielectric constant  $\kappa$  value.



**Figure 2.20: Capacitor formed by two metal lines and a dielectric layer in between.**

#### 2.4.2 Fundamental Low- $\kappa$ Dielectric Physics

Different methods could be used to get a low- $\kappa$  dielectric film based on the Clausius Mossotti's relation, which is simplified as below for a dielectric material

$$\frac{\kappa-1}{\kappa+2} = \frac{N\alpha}{3\varepsilon_0} \quad (4)$$

where  $\kappa$  is the dielectric constant,  $N$  is the number density of molecules (number of molecules per volume), and  $\alpha$  is the molecular polarization. From equation (4), it can be seen that the dielectric constant  $\kappa$  depends on both number density of molecules of the material ( $N$ ) and polarization of molecules ( $\alpha$ ) [2.32]. Hence, in order to reduce the  $\kappa$  value of the dielectric, we can either select a material with a smaller molecular polarization ( $\alpha$ ), or a smaller number

density ( $N$ ). Molecular polarization consists of electronic polarization ( $\alpha_e$ ), distortion polarization ( $\alpha_i$ ) which is related to the ionic bonds in the dielectric and permanent dipole moment polarization ( $\alpha_d$ ) [2.33]. Hence, in order to reduce the molecular polarization, the electronic polarization can be reduced by using an element with a smaller electron density so that  $\alpha_e$  is decreased, and/or reducing distortion polarization ( $\alpha_i$ ) either by reducing the number of ionic bonds, or by using a material whose molecules are not polar so as to minimize  $\alpha_d$ . Another method to reduce the  $\kappa$  value is to introduce pores into the dielectric film, so that the number density of molecules of the material ( $N$ ) is reduced. In a nutshell, it is practical to reduce the  $\kappa$  value of the dielectric film by making the dielectric film porous.

### **2.4.3 Classification of Porous Low- $\kappa$ Dielectrics**

Porous low- $\kappa$  dielectrics are classified according to their basic compositions and structures, and mainly consist of two categories: constitutive and subtractive. Final porous structures of constitutive porous dielectrics mainly depend on the first layer deposited. The constitutive porous dielectrics can be of 3 types: silsesquioxane (SSQ)-based, silica-based and organic polymer, all of which can be applied on using both spin-on process and chemical vapor deposition (CVD) process. Subtractive porous dielectrics are created by thermal desorption or chemical etching by using constitutive porous films deposited by CVD or PECVD as the starting film. During the process, certain parts of original structures are selectively removed, and pores are hence created.

In July 2005, Applied Materials – market leader in low- $\kappa$  dielectric film technology introduced an “Applied Producer Black Diamond II” system for the purpose of depositing the semiconductor industry’s most advanced low- $\kappa$  film, with a  $\kappa$  value of less than 2.5 [2.34]. The low- $\kappa$  value is achieved by its tightly distributed small sized pores which provide excellent integration stability and high mechanical integrity at the same time.

## 2.5 TSV Electrical Modeling and Characterization

TSV is typically used for electrical connection between two stacked IC layers, and the TSV parasitic capacitance has the most predominant impact on the circuit operation [2.35]. Hence the electrical characterization should be well understood.

### 2.5.1 Analytical Modeling

**Capacitance Modeling:** Planar MOS capacitor structures are well known and have been studied extensively in literature [2.36-2.38]. The capacitance of a MOS capacitor varies with the gate voltage as shown in Figure 2.21. A TSV effectively forms a circular MOS structure as shown in Figure 2.22. The MOS effect in TSV is analytically modeled by solving Poisson's equation in cylindrical coordinates with a full depletion approximation which assumes no mobile charge carriers (holes or electrons) in the depletion region [2.39].

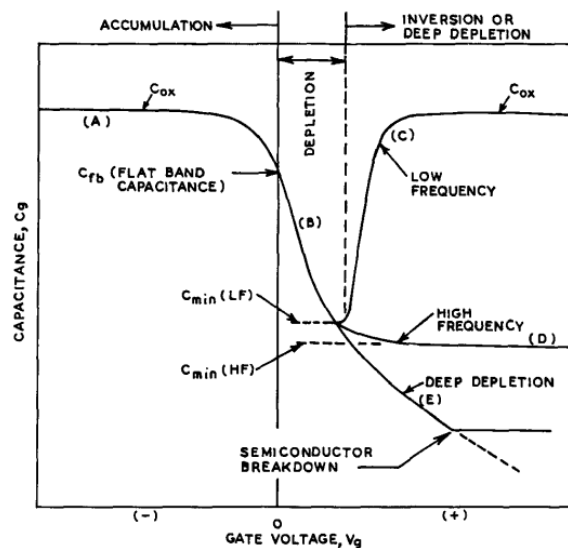
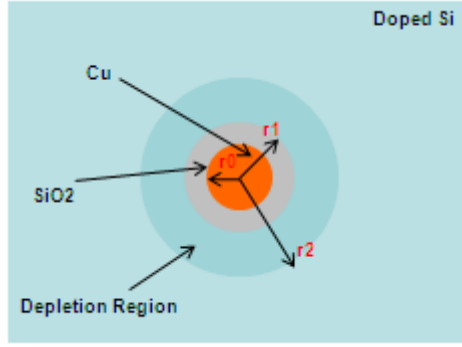


Figure 2.21: Typical capacitance vs. gate voltage plot for planar MOS capacitance [2.38].



**Figure 2.22: Top view of a TSV, illustrating how it forms a circular MOS structure.**

Neglecting all defect charges in the oxide liner and Si/SiO<sub>2</sub> interface, the gate voltage is

$$V_G = V_{FB} + \phi_s + \frac{Q_M}{C_{ox}} \quad (5),$$

where  $V_{FB}$ = flatband voltage;  $Q_M$ = charge on the metal;  $C_{ox}$ = capacitance per unit area of the SiO<sub>2</sub> liner.

The flatband voltage equals to the work function difference between the gate metal ( $\phi_M$ ) and the semiconductor ( $\phi_{Si}$ ):

$$V_{FB} = \phi_M - \phi_{Si} \quad (6)$$

$$\phi_M - \phi_S = \phi_M - \chi - \frac{E_g}{2q} - V_t \ln \frac{N_a}{n_i} \quad (7)$$

where  $\chi$ = electron affinity of Si (in V);  $E_g$ = band gap energy of Si (in eV);  $q$ = electronic charge;  $V_t=0.026V$  (at 300K);  $T$ =absolute temperature;  $N_a$ =Doping concentration of the surrounding Si substrate (presumed to be of  $p$ -type);  $n_i$ =intrinsic carrier concentration of Si.

The Poisson's equation in cylindrical co-ordinates can be expressed as

$$\frac{d^2\phi}{dr^2} + \frac{1}{r} \frac{d\phi}{dr} = - \frac{\rho}{\epsilon_s} \quad (8),$$

where  $\phi$ =potential;  $\rho$ =charge density;  $\epsilon_s$ =dielectric constant of Si.

Assume that the electric charge distribution does not vary with the angle around the TSV or the axial distance due to symmetry. In the full depletion approximation, the depletion layer charge is completely due to the ionized doping atoms, and hence the Poisson's equation can be simplified as in equation (9)

$$\frac{1}{r} \frac{d}{dr} \left( r \frac{d\phi}{dr} \right) = \frac{qN_a}{\epsilon_s} \quad (9)$$

with boundary conditions: at  $r = r_2$  shown in Figure 2.21, the electric field and potential is zero. By integrating the above equation from  $r$  to  $r_2$

$$-r \frac{d\phi}{dr} = \frac{qN_a}{2\epsilon_s} (r_2^2 - r^2) \quad (10)$$

integrating from  $r_1$  to  $r_2$ ,

$$\phi_s = \frac{qN_a}{2\epsilon_s} \left( r_2^2 \ln \frac{r_2}{r_1} - \frac{r_2^2 - r_1^2}{2} \right) \quad (11)$$

where  $\phi_s$  = surface potential at the Si/SiO<sub>2</sub> interface.

The charge on the metal,  $Q_M$  is equal to the charge in the depletion region,

$$Q_M = qN_a \pi (r_2^2 - r_1^2) L \quad (12),$$

and the oxide liner capacitance can be calculated as

$$C_{ox} = \frac{2\pi\epsilon_{ox}L}{\ln \frac{r_1}{r_0}} \quad (13).$$

By combining the above equations, it results that

$$V_G = \phi_M - \chi - \frac{E_g}{2q} - V_t \ln \frac{N_a}{n_i} + \frac{qN_a}{2\varepsilon_s} \left( r_2^2 \ln \frac{r_2}{r_1} - \frac{r_2^2 - r_1^2}{2} \right) + \frac{qN_a(r_2^2 - r_1^2)}{2\varepsilon_{ox}} \ln \frac{r_1}{r_0} \quad (14)$$

When the radius of the depletion region edge at threshold  $r = r_T$ , and  $\phi_s = 2\phi_F = 2V_t \ln \frac{N_a}{n_i}$ , the threshold voltage of inversion is given as

$$V_T = \phi_M - \chi - \frac{E_g}{2q} + V_t \ln \frac{N_a}{n_i} + \frac{qN_a(r_T^2 - r_1^2)}{2\varepsilon_{ox}} \ln \frac{r_1}{r_0} \quad (15).$$

The depletion region capacitance is

$$C_{di} = \frac{2\pi\varepsilon_s L}{\ln \frac{r_2}{r_1}} \quad (16),$$

and hence the total TSV capacitance  $C$  is given by

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_{di}} \quad (17).$$

**Resistance Modeling:** The DC resistance of a TSV can be estimated as

$$R = \rho \times L/A = \rho \times L/(\pi r_0^2) \quad (18).$$

There is a resistance increase due to the skin effect, and is significant for higher diameter TSV structures. The skin effect is the tendency of an alternating electric current (AC) to distribute itself within a conductor so that the current density near the surface of the conductor is greater than that at its core. In other words, the electric current tends to flow at the "skin" of the conductor, at an average depth called the skin depth. The skin effect causes the effective resistance of the conductor to increase with increasing current frequency

because much of the conductor carries little current [2.40]. The total effective area of the TSV is given

$$A = \sigma \times \pi \times (2r_0) \quad (19),$$

where  $\sigma$  is the skin depth, given by  $\sigma = \sqrt{\frac{2\rho}{\omega\mu}} = \sqrt{\frac{\rho}{\pi f\mu}}$ , hence the TSV resistance due to skin effect is

$$R_{ac} = \frac{\rho \times L}{2\pi\sigma r_0} \quad (20).$$

**Inductance Modeling:** The partial self-inductance of the TSV depends upon the diameter and length of the TSV and is given by the following empirical expression [2.41]:

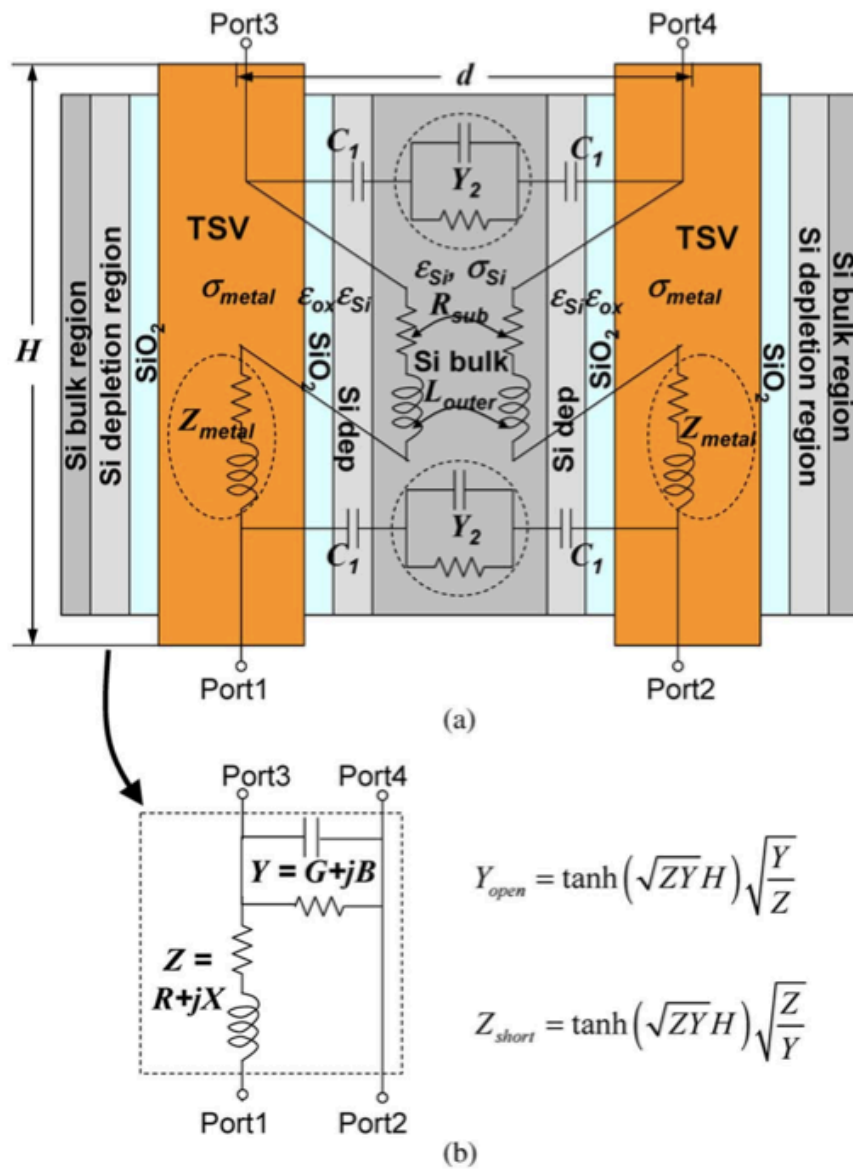
$$L_{TSV} = \frac{\mu_0}{4\pi} \left[ 2l_{TSV} \ln \left( \frac{2l_{TSV} + \sqrt{r_{TSV}^2 + (2l_{TSV})^2}}{r_{TSV}} \right) + \left( r_{TSV} - \sqrt{r_{TSV}^2 + (2l_{TSV})^2} \right) \right] \quad (21).$$

However, the TSV's inductance can be ignored for clock frequencies below 3 GHz.

### 2.5.2 Compact Resistance-Inductance-Capacitance-Conductance (RLCG) Model for TSV

In 45 nm technology, the highest frequency of concern or significant frequency ( $f_B$ ) of the signals on interconnects can be as high as 62 GHz [2.42]. Hence, the simple modeling of TSV interconnects as  $RC$  elements presented in the previous section is insufficient at high frequencies. In [2.43], a compact RLCG model for TSVs is derived to model the AC conduction in the silicon substrate (from  $Re(Y_2)$ ), the skin effect in the TSV metal (from

$Z_{metal}$ ), and eddy current (from  $R_{sub}$ ) in silicon for high frequency analysis. The equivalent circuit is shown in Figure 2.23 (a).



**Figure 2.23: (a) Equivalent distributed circuit (RLCG) model for a pair of TSVs, which can be reduced to (b) a distributed transmission line model [2.43].**

The equivalent circuit in Figure 2.23 (a) can further be reduced to a simplified transmission line model (Figure 2.23 (b)). In the Figure,  $d$  is the center to center distance;  $\sigma_{metal}$  and  $\sigma_{Si}$  are the conductivity of TSV metal and Si, respectively;  $C_l$  is the capacitance per unit TSV

height due to the dielectric and the Si depletion region;  $Y_2$  is the admittance per unit TSV height due to bulk Si;  $Z_{metal}$  is the inner impedance per unit TSV height due to the TSV metal;  $L_{outer}$  is the outer inductance per unit TSV height between two TSVs;  $R_{sub}$  is the resistance per unit TSV height due to eddy currents in the substrate;  $Y$  and  $Z$  are the effective admittance and the impedance per unit TSV height, respectively;  $H$  is the TSV height; and  $Y_{open}$  is the input admittance between ports 1 and 2 if ports 3 and 4 are open circuit; similarly,  $Z_{short}$  is the input impedance between ports 1 and 2 if ports 3 and 4 are short circuited. The reduced equivalent circuit contains two components: parallel admittance per unit TSV height ( $\mathbf{Y} = \mathbf{G} + \mathbf{jB}$ , where  $G$  and  $B$  are the equivalent conductance and susceptance, respectively) and serial impedance per unit TSV height ( $\mathbf{Z} = \mathbf{R} + \mathbf{jX}$ , where  $R$  and  $X$  are the equivalent resistance and reactance, respectively). Furthermore, as being defined in Figure 2.23 (b), the open circuit total admittance  $Y_{open}$  and short circuit total impedance  $Z_{short}$  can be reduced to  $Y_{open} \approx \mathbf{YH}$  and  $Z_{short} \approx \mathbf{ZH}$  since  $\sqrt{|\mathbf{ZY}|}H \ll 1$  at reasonably high frequencies ( $\leq 100$  GHz).

**CG Model-Parallel Admittance per TSV Height:** The parallel admittance per unit TSV height ( $Y$ ) can be treated as a series of capacitance of the dielectric and Si depletion region ( $C_1$ ) and the coupling admittance due to bulk Si ( $Y_2$ )

$$Y = [2(j\omega C_1)^{-1} + Y_2^{-1}]^{-1} = G + j\omega C = G + jB \quad (22)$$

where  $\omega$  is the radial frequency; the factor of 2 arises from the fact that there are two TSVs and the  $C_1$  of both of them are in series with  $Y_2$ , where,

$$C_1 = \left[ \frac{1}{2\pi\epsilon_{ox}} \ln \left( 1 + \frac{t_{ox}}{r_{via}} \right) + \frac{1}{2\pi\epsilon_{Si}} \ln \left( 1 + \frac{w_{dep}}{r_{via} + t_{ox}} \right) \right]^{-1} \quad (23)$$

in equation (23),  $\epsilon_{ox}$  and  $\epsilon_{Si}$  are the permittivity of oxide and Si, respectively. The geometrical parameters  $r_{via}$ ,  $t_{ox}$  and  $w_{dep}$  are the radius of the via, the thickness of the isolation dielectric, and the Si depletion width. Using the method of images, one can write

$$Y_2 = \pi(\sigma_{Si} + j\omega\epsilon_{Si})/\cos^{-1}\left[\frac{d}{2}/(r_{via} + t_{ox} + w_{dep})\right]. \quad (24)$$

**RL Model-Serial Impedance per TSV Height:** The serial impedance per unit height ( $Z$ ) can be expressed as

$$Z = \left(-\frac{d\phi_1}{dz} + \frac{d\phi_2}{dz}\right)/I \quad (25)$$

where  $\phi_1$  and  $\phi_2$  are the scalar potential in TSV 1 and 2, respectively;  $I$  is the total current in the two TSVs. In quasi-magnetostatic field

$$-\frac{d\phi}{dz} = E_z + j\omega A_z = \frac{J_z}{\sigma_{eff}} + j\omega A_z \quad (26)$$

where  $E_z$  is the  $z$ -direction component vertical to the substrate of the electric field in either the TSV metal or the Si substrate;  $A_z$  is the corresponding magnetic vector potential;  $J_z$  is the corresponding current density; and  $\sigma_{eff}$  is the effective conductivity in either the TSV metal or the Si substrate.

The general differential equation for  $J_z$  for a single TSV azimuthal system can be obtained from Maxwell's equations, i.e.,

$$j\omega\mu J_z(r) = \frac{1}{r} \frac{d}{dr} \left( r \frac{d}{dr} E_z(r) \right) = \frac{1}{\sigma_{eff}} \frac{1}{r} \frac{d}{dr} \left( r \frac{d}{dr} J_z(r) \right) \quad (27)$$

where  $\mu$  is the permeability in either the TSV metal or Si; and  $r$  is the radial direction coordinate of TSV.

In the case of a single TSV, the boundary conditions require that  $J_z(\infty) = 0$ . Consequently, the expression for  $J_z(r)$  can be written as

$$J_z(r) = \begin{cases} c_1 J_0((1-j)r/\delta_{metal}), & r < r_{via} \\ c_2 H_0^{(2)}((1-j)r/\delta_{Si}), & r > r_{via} + t_{ox} + w_{dep} \end{cases} \quad (28)$$

where  $c_1$  and  $c_2$  are constants;  $J_0$  is the 0<sup>th</sup> order Bessel function of the first type;  $H_0^{(2)}$  is the 0<sup>th</sup> order Hankel function of the second type; and  $\delta_{metal}$  and  $\delta_{Si}$  are the damping parameters, i.e.,

$$\delta_{metal} = \sqrt{2/\omega\mu\sigma_{metal}} \quad \delta_{Si} = \sqrt{2/\omega\mu(\sigma_{Si} + j\omega\epsilon_{Si})} \quad (29)$$

$c_1$  and  $c_2$  can be normalized as

$$\begin{aligned} \frac{c_1}{I} &= \left[ \int_0^{r_{via}} J_0((1-j)r/\delta_{metal}) \cdot 2\pi r dr \right]^{-1} \\ &= (1-j)[2\pi r_{via} \delta_{metal} J_1((1-j)r_{via}/\delta_{metal})]^{-1} \end{aligned} \quad (30a)$$

$$\begin{aligned} \frac{c_2}{I} &= - \left[ \int_{r_{via}+t_{ox}+w_{dep}}^{\infty} H_0^{(2)}((1-j)r/\delta_{Si}) \cdot 2\pi r dr \right]^{-1} \\ &= \frac{[(1+j)\pi\delta_{Si}(r_{via}+t_{ox}+w_{dep})]^{-1}}{H_1^{(2)}((1-j)(r_{via}+t_{ox}+w_{dep})/\delta_{Si})} \approx -\frac{1}{2\delta_{Si}^2} \end{aligned} \quad (30b)$$

where  $I$  is the total current;  $J_1$  is the 1<sup>st</sup> order Bessel function of the first type;  $H_1^{(2)}$  is the 1<sup>st</sup> order Hankel function of the second type; the equivalent sign is valid since  $r_{via} + t_{ox} + w_{dep} \ll \delta_{Si}$ .

From (25), (26), and the superposition of two TSVs,  $d\phi/dz$  in the two TSVs can be expressed as

$$\begin{aligned}
& -\frac{1}{I} \cdot \frac{d\phi_1}{dz} = \frac{1}{I} \cdot \frac{d\phi_2}{dz} \approx \frac{J_z(r_{via} - \Delta r)}{\sigma_{metal} I} + \frac{j\omega}{I} [A_z(r_{via}) - A_z(d)] \\
& = J_z(r_{via} - \Delta r)/(\sigma_{metal} I) + (j\omega/I)[A_z(r_{via}) - A_z(r_{via} + t_{ox} + w_{dep})] \\
& \quad + (j\omega/I)[A_z(r_{via} + t_{ox} + w_{dep}) - A_z(d)] \quad (31)
\end{aligned}$$

where  $\Delta r$  is an infinitesimal value; and  $J_z(r_{via} - \Delta r)$  indicates the current density at the surface of the TSV metal. According to (28) and (30a), the first term on the right-hand side of (31), called the inner impedance ( $Z_{metal}$ ), can be expressed as

$$\begin{aligned}
Z_{metal} &= \frac{J_z(r_{via} - \Delta r)}{\sigma_{metal} I} \\
&= \frac{(1-j) \cdot J_0((1-j)r_{via}/\sigma_{metal})}{\sigma_{metal} \cdot 2\pi r_{via} \delta_{metal} \cdot J_1((1-j)r_{via}/\delta_{metal})}. \quad (32)
\end{aligned}$$

The second term on the right-hand side of (31) is purely imaginary, which can be obtained from the vector potential Green's function as:

$$\frac{j\omega}{I} [A_z(r_{via}) - A_z(r_{via} + t_{ox} + w_{dep})] = \frac{j\omega\mu}{2\pi} \cdot \ln\left(\frac{r_{via} + t_{ox} + w_{dep}}{r_{via}}\right). \quad (33)$$

Since the  $d\phi/dz$  outside the two TSVs is zero, the third term on the right-hand side of (31) can be derived from (28)-(30b), i.e.,

$$\begin{aligned}
\frac{j\omega[A_z(r_{via} + t_{ox} + w_{dep}) - A_z(d)]}{I} &= \frac{-J_z(r_{via} + t_{ox} + w_{dep} + \Delta r) + J_z(d)}{(\sigma_{Si} + j\omega\epsilon_{Si})I} \approx \frac{\omega\mu}{4} \left[ H_0^{(2)}\left(\frac{1-j}{\delta_{Si}}(r_{via} + t_{ox} + \right. \right. \\
& \quad \left. \left. w_{dep})\right) - H_0^{(2)}\left(\frac{(1-j)d}{\delta_{Si}}\right) \right]. \quad (34)
\end{aligned}$$

The real part of this term is physically due to the eddy current. Multiplying by 2 (due to two TSVs),

$$R_{sub} \approx \frac{\omega\mu}{2} \cdot Re \left[ H_0^{(2)} \left( \frac{1-j}{\delta_{Si}} (r_{via} + t_{ox} + w_{dep}) \right) - H_0^{(2)} \left( \frac{(1-j)d}{\delta_{Si}} \right) \right]. \quad (35)$$

Multiplying the sum of the right-hand side of (33) and the imaginary part of the right-hand side of (34) by 2 gives  $\omega L_{outer}$  (where  $L_{outer}$  is the outer inductance):

$$L_{outer} \approx \frac{\mu}{\pi} \ln \left( \frac{r_{via} + t_{ox} + w_{dep}}{r_{via}} \right) + \frac{\mu}{2} \cdot Im \left[ H_0^{(2)} \left( \frac{1-j}{\delta_{Si}} (r_{via} + t_{ox} + w_{dep}) \right) - H_0^{(2)} \left( \frac{(1-j)d}{\delta_{Si}} \right) \right]. \quad (36)$$

Therefore, the serial impedance per unit TSV height ( $Z$ ) can be treated as the sum of three components, i.e., the inner impedance of the TSV ( $Z_{metal}$ ), the outer inductance ( $L_{outer}$ ), and the resistance due to eddy current in the substrate ( $R_{sub}$ ), i.e.,

$$Z = 2Z_{metal} + j\omega L_{outer} + R_{sub}. \quad (37)$$

In the case of a TSV pair where one TSV serves as the return path of the other,  $L_{outer}$  is approximately the reciprocal of the "capacitance" between two TSVs as if the "medium permittivity" between the TSVs is  $1/\mu$ . This is valid as long as  $|\delta_{Si}| \gg d$ . Similar to (24),  $L_{outer}$  can also be expressed as

$$L_{outer} \approx \frac{\mu}{\pi} \cos^{-1} \left( \frac{d}{2r_{via}} \right). \quad (38)$$

### 2.5.3 TSV Capacitance Reduction Techniques

A typical TSV  $C$ - $V$  curve has accumulation, inversion and depletion regions. When the TSV gate voltage is smaller than the flatband voltage, the TSV capacitance is the dielectric layer capacitance. For high frequency signals, the TSV capacitance is the minimum in the maximum depletion region when the TSV gate voltage is greater than the threshold voltage. Furthermore, when the TSV gate voltage is between the flatband voltage and the threshold

voltage, the TSV capacitance is not constant. Hence, the minimum TSV capacitance at the maximum depletion region is desired for the circuit performance. Saito *et al.* [2.44] describes two potential approaches to operate the TSV in the maximum depletion region as follows:

- 1) A reverse bias voltage is applied to the substrate, or the TSV signals are modulated to cause depletion extending from the Si/SiO<sub>2</sub> interface into the substrate. However, it requires additional area consumption for additional circuit, which is not desirable.
- 2) Counter-doping the substrate for achieving depletion of the TSV in the operating voltage range. In the case, an *n*-type semiconductor layer is formed within the *p*-type silicon substrate surrounding the insulating SiO<sub>2</sub> film. However, this process requires a high temperature annealing which is likely to violate the thermal constraints imposed on TSV processing.

Katti, G., *et al.* proposed to induce more fixed positive oxide charge during the liner deposition step so as to shift the *C-V* curve towards more negative values along the X-axis, and to thus achieve maximum depletion capacitance at the operating voltage [2.45]. This can be done using the CVD oxide deposition process, and is a much more preferred method as compared to others. The value of the fixed oxide charge depends on several factors, namely the oxidizing ambient, oxidizing temperature, silicon orientation, cooling rate from elevated temperature, cooling ambient, and subsequent anneal cycles. The decrease in the atomic concentration of oxygen increases the carbon incorporation. This results in an increase in the fixed oxide charges [2.46].

## 2.6 Cu-TSV Induced Thermo-mechanical Stress

One of the challenges in TSV development is to reduce its stress impact on neighbouring device functionality. A thermo-mechanical stress is induced during the copper electroplating and annealing processes due to the mismatch in the thermal coefficients (CTEs) of Cu and Si. Beside the Cu protrusion which can be a potential reliability problem, the thermo-mechanical stress will cause a shift in the electron/hole mobility of silicon in the vicinity of TSVs. A maximum 14% shift in the mobility has been reported in several publications [2.47-2.49]. Therefore, electrical evaluation of devices in the vicinity of TSVs is essentially required for successful 3D integration design: 1) To derive layout design rules to provide a keep-out zone (KOZ), and 2) To exploit TSV-induced stress effect to improve the device performance [2.50]. Several studies have reported and evaluated the TVS proximity influence on active devices, such as MOSFET. Micro-Raman spectroscopy is commonly used to evaluate the TSV induced stress near the Si surface. Methods proposed to effectively reduce the stress so that a smaller KOZ could be obtained include reducing Cu volume with smaller TSV CD [2.51] and the metallization improvement [2.52]. Figure 2.23 compares of micro-Raman analysis results before and after the metallization improvement. Table 2.1 below summaries the KOZ for specific technology nodes as well as  $I_{on}$  changes defined and evaluated by different organizations.

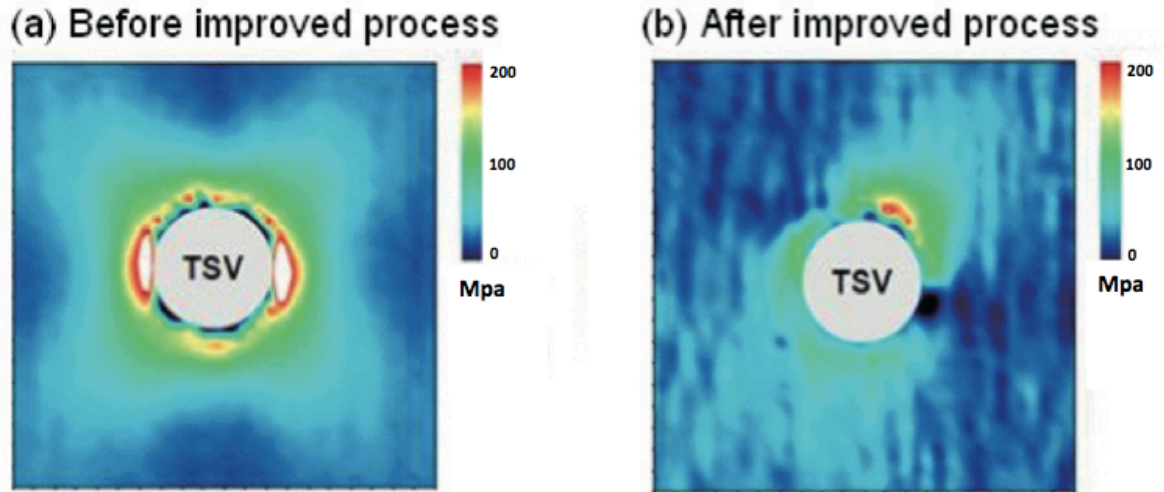


Figure 2.24: TSV-induced stress micro-Raman measurement results: a) Before improvement and b) After improvement. A smaller KOZ is expected after improvement [2.52].

Reference	Technology node [nm]	TSV Ø [μm]	KOZ [μm]	% ΔI <sub>on</sub> /I <sub>on</sub>	
				NMOS	PMOS
Yang <i>et. al.</i> [2.47]	130	5.2	1.1	0.0	0.0
Weerasekera <i>et. al.</i> [2.50]	65	8	1.2	4.0	4.0
Beyne [2.53]	65	5	1.7	0.6	4.0
Cho <i>et. al.</i> [2.54]	45	6	2	2.0	2.0
West <i>et. al.</i> [2.55]	28	10	4	2.3	2.3

Table 2.1: Summary of KOZ due to TSV induced stress and I<sub>on</sub> change for specific technology nodes.

## 2.7 Summary

In this chapter, 3D IC technology was first overviewed and a global road map of 3D integration was presented. Eventually, a heterogeneous integration as full "3D IC" would be desired for industry.

Secondly, we gave a comparison between 3D packaging and 3D integration. The difference between the two approaches of 3D implementations is the TSV involvement which is one of the key enablers for 3D integration.

Thirdly, as the key enabler of 3D integration, TSV processes were then discussed in detail. The main TSV processes can be summarized in five steps namely, DRIE Si etch for via formation, dielectric liner deposition to isolate the TSV core from the Si substrate, barrier and seed layer sputtering, Cu ECP to have a void free Cu filling, and Cu CMP to remove the Cu overburden. Each of the above process steps has its own challenges, modifications and optimizations are required to have a robust TSV structure.

Low- $\kappa$  dielectric properties and physics were then presented. A low leakage low- $\kappa$  dielectric is always desired and required for interconnects. Due to its requirement of compatibility with the standard TSV process, the low- $\kappa$  material's integration with the TSV structure as the dielectric liner is interesting for further studies. Since the TSV is used for signal transmission between the stacked chips, its electrical characteristics are also very important. Electrical modeling of the TSV's key parameters such as the resistance, capacitance and inductance modeling, were proposed. In addition, we reviewed several techniques proposed by other research groups which were found to be useful in reducing the parasitic capacitance of the TSV, as a lower capacitance is desired for faster signal or data transmissions. Last but not least, the TSV's Cu-induced thermo-mechanical stress and its related reliability issues were also presented. These stress-induced reliability issues have to

be studied and solved since they are critical for the performance of the active devices situated in the vicinity of TSVs.

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# Chapter 3: TSV Structure Design and Fabrication

## 3.1 Introduction

In this chapter, the fabrication process flows of TSV structures for electrical characterization and thermal property studies are presented. The fabrication process of TSV mainly consists of a deep reactive ion etch (DRIE) for via formation, followed by a dielectric liner deposition using PECVD or thermal oxidation for oxide liner. Thereafter, the barrier and seed layer deposition can be deposited by physical vapor deposition (PVD) or electrografting (eG) process, via filling by Cu ECP, and finally a CMP process for Cu plating overburden removal [3.1].

We evaluated TSV structures of different sizes, pitches and densities in this project. In order to have a robust TSV structure for the subsequent characterization purposes, each of the TSV process steps must be fully understood and optimized. In addition, the process observations and optimizations done to mitigate the encountered issues are presented. After fabrication, direct current (*DC*) tests such as capacitance-voltage (*C-V*) and current-voltage (*I-V*), and thermal measurements performed on these structures will be presented in the subsequent chapters.

Some of the results in this chapter have been published in our publications as follows:

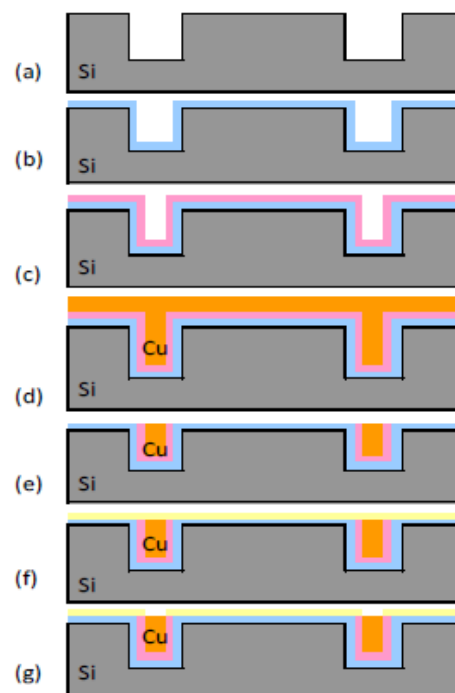
1. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, “Design, Fabrication and Electrical Characterization of TSV”, *12th Electronics Packaging Technology Conference (EPTC)*, December, 2010.

2. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, "Through Silicon Via (TSV) Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current", *International Conference on Solid State Devices and Materials (SSDM)*, September, 2011.
3. **L. Zhang**, R. I Made, H. Y. Li, S. Gao, G. Q. Lo, D. L. Kwong, and C. S. Tan, "Spatial Variation of TSV Capacitance and Method of Stabilization with Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge at the Silicon-Liner Interface", *IEEE International Electron Devices Meeting (IEDM)*, December, 2011.
4. **L. Zhang**, H. Y. Li, G. Q. Lo, and C. S. Tan, "Thermal Characterization of TSV Array as Heat Removal Element in 3D IC Stacking," *Electronic Packaging Technology Conference (EPTC)*, Singapore, December 5-7, 2012.
5. **L. Zhang**, D. F. Lim, H. Y. Li, S. Gao, and C. S. Tan, "Through Silicon Via Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current", *Japanese Journal of Applied Physics*, 51 (4), 2012.

## 3.2 TSV Structure Design

### 3.2.1 Wafer Layout and Mask Design

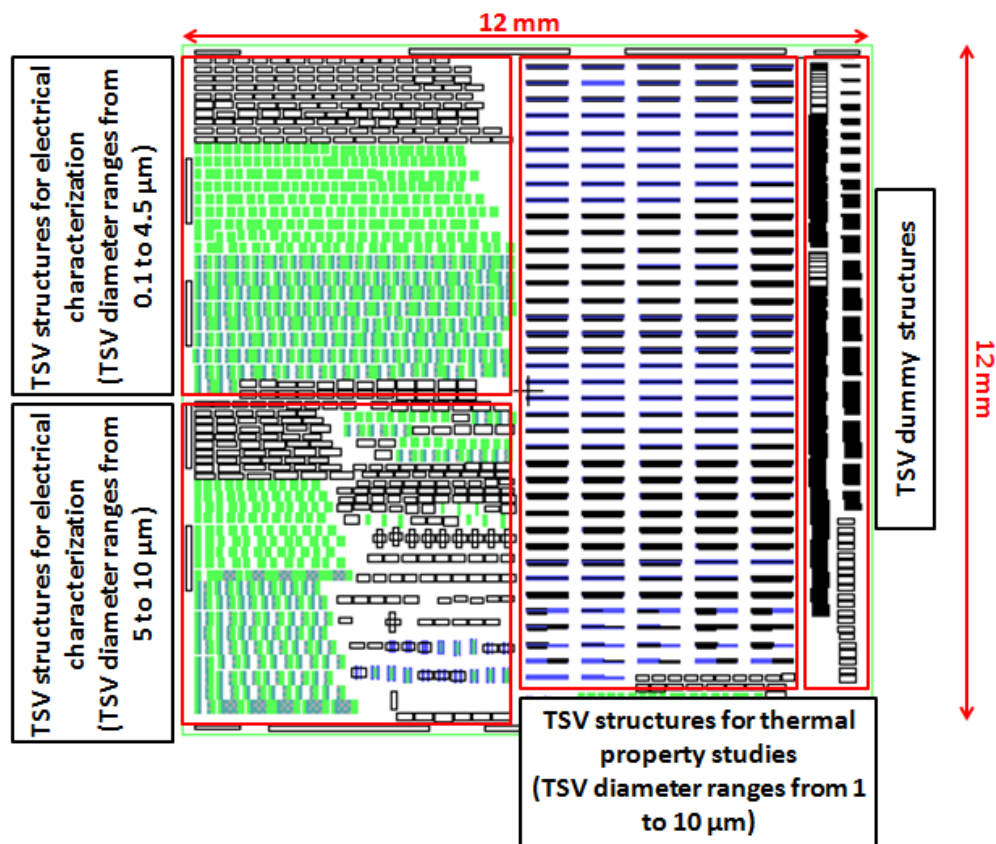
The fabrication of a high aspect ratio (aspect ratio refers to the ratio of TSV height to TSV diameter) TSV is required to meet the demand for high density input/output (I/O). Therefore, in order to fabricate a void free TSV, the process conditions and steps in achieving a super-conformal filling of TSV is desired. In this work, we are targeting a TSV diameter of 5  $\mu\text{m}$  with an aspect ratio of 2 to 3. We chose this aspect ratio for ease of fabrication, and although a higher aspect ratio is always desired, this aspect ratio is sufficient for the study of the liner properties. Figure 3.1 shows the process flow of the TSV fabrication on an 8" *p*-type Si wafer which has a resistivity ranges from 6 to 9  $\Omega\text{cm}$ . A deep trench in the Si wafer is first etched



**Figure 3.1: TSV fabrication process flow: a) DRIE Si etch; b) dielectric liner deposition; c) Ta barrier/Cu seed layer sputtering; d) Cu ECP; e) Cu CMP; f) passivation; g) TSV opening [3.2].**

using the BOSCH DRIE process, followed by a dielectric isolation ( $\text{SiO}_2$ ) layer deposition. Thereafter, PVD of Ta barrier & Cu seed layer is done before filling the trench using a Cu ECP process and finally Cu CMP to remove the Cu overburden [3.2].

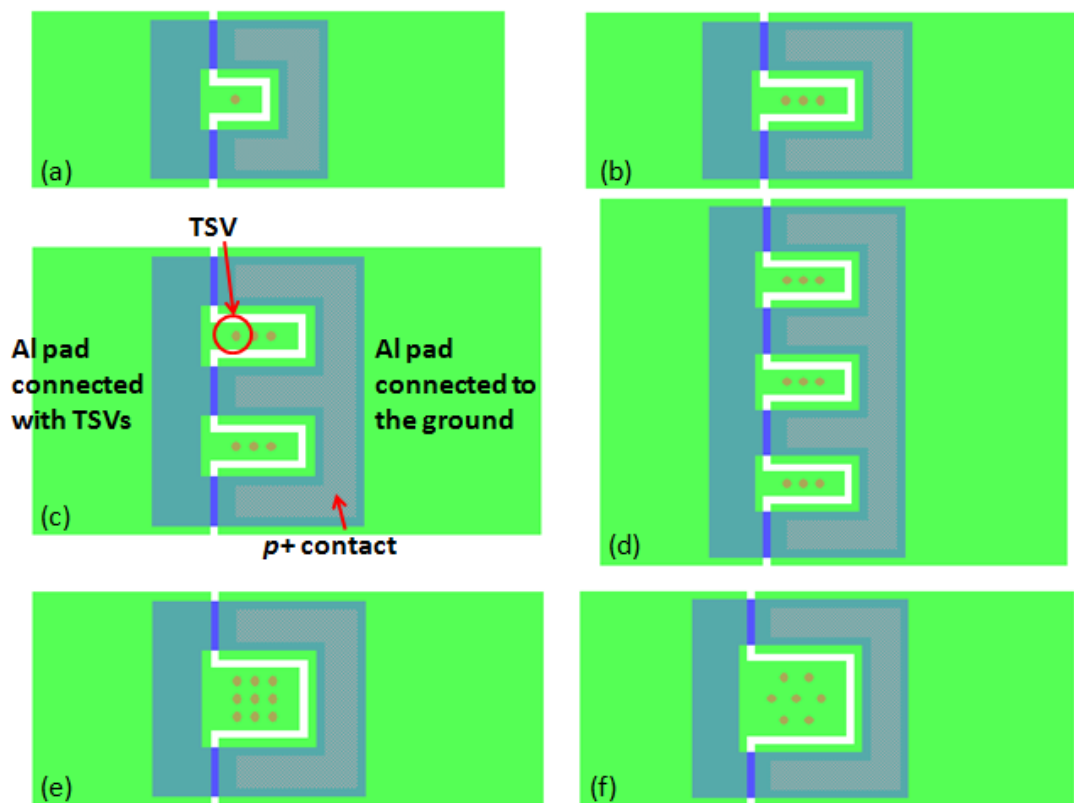
The wafer was fully patterned with a number of 121 reticles, and each reticle has the size of  $12\text{ mm} \times 12\text{ mm}$  while Figure 3.2 shows the magnified layout of the reticle. The reticle contains five mask layers and it consists of all the major components or structures to be characterized – TSV structures for electrical characterization, TSV structures for thermal property studies, dummy TSV structures for process optimization and failure analysis. As shown in Figure 3.2, different TSV structures are grouped in different areas of the reticle, it is designed systematically so that each TSV structure can be located easily while performing the testing.



**Figure 3.2:** Zoom in view of the reticle shows die level mask design; different structures are grouped in different locations of the die.

### 3.2.2 Electrical Structure Design

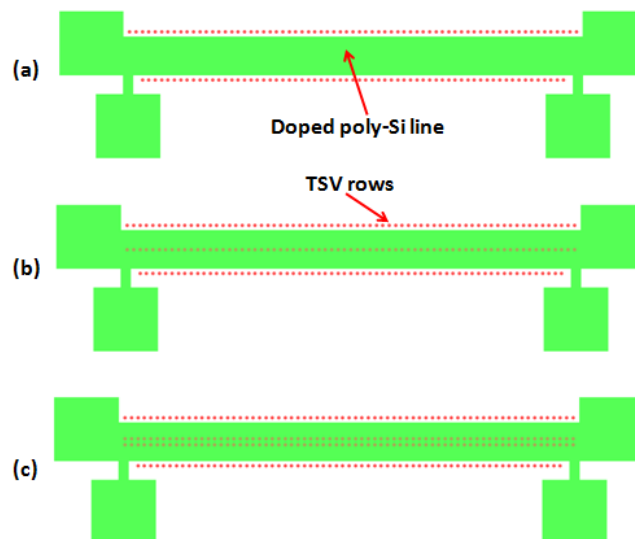
The TSV structures studied in this work – single TSV, single TSV row, double TSV rows, TSV arrays with different TSV sizes, TSV pitches and densities are designed to characterize the electrical properties, such as parasitic capacitance and leakage current of TSV as a function of size, pitch and arrangement. Figure 3.3 shows some of the designed TSV structures which incorporate the variations as described. Typically, the TSVs are surrounded by  $p^+$  boron doped substrate, with one of the Al pads connected to the TSV arrays while the other Al pad is connected to the  $p^+$  implant area to provide a stable ground to the Si substrate.



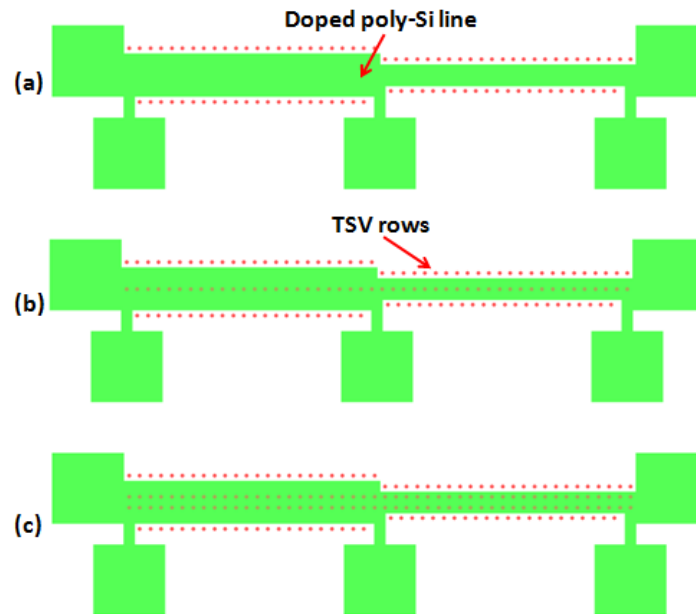
**Figure 3.3: Schematic top view of designed TSV structure for electrical characterizations: (a) single TSV; (b) single TSV row; (c) double TSV rows; (d) triple TSV rows; (e) square TSV array; (f) hexagonal TSV array.**

### 3.2.3 Thermal Structure Design

The purpose of fabricating TSV structures for thermal characterization is to demonstrate that TSV arrays can be used as an effective heat removal element, as well as to elucidate how the density and placement of TSV arrays can affect the heat conduction. Figure 3.4 shows the test structures fabricated and evaluated in this work. To study the heat dissipation capability, a temperature sensor comprising a Kelvin structure was fabricated in the vicinity of the TSV array. Other types of temperature sensors, such as  $p-n$  diode and gate poly, have been reported [3.3, 3.4]. In this work, a doped poly-silicon resistor realized on top of the oxide layer is used as the temperature sensor. Since the resistance value of the doped poly-silicon lines changes with temperature, one can calculate the temperature by measuring the resistance of the lines. The test structures shown in Figure 3.5 have non-uniform poly-Si lines to simulate the hotspot in the circuit. The purpose of this design is to see how effectively the TSV can remove the heat when the heating power is varied across the entire chip.



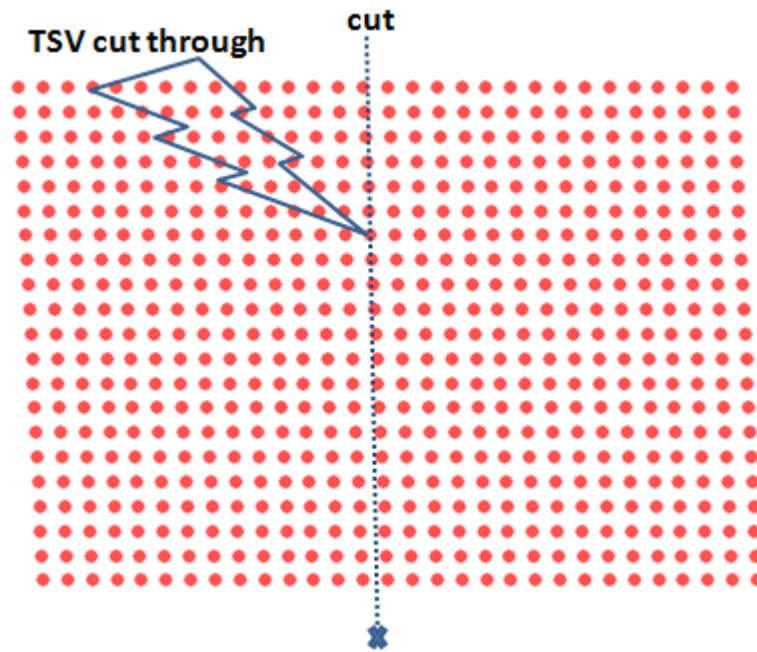
**Figure 3.4: Schematic of the uniform temperature sensor in the form of Kelvin structure for TSV thermal property studies: (a) only TSV rows surrounded the poly-Si line; (b) TSV rows surrounded and one TSV row beneath the poly-Si line; (c) TSV rows surrounded and two TSV rows beneath the poly-Si line.**



**Figure 3.5: Schematic of the thermal structure with non-uniform temperature sensor.**

### **3.2.4 Dummy TSV Blocks**

In order to have a robust TSV and to optimize the TSV process, failure analysis (FA) tools such as scanning electron microscope (SEM), focus ion beam (FIB) and transmission electron microscope (TEM) have to be used along the way to monitor the process outcome. Since a single alone TSV is very difficult to be located for FA purposes, the dummy TSV blocks are designed for ease of finding the TSV locations. Figure 3.6 shows one example of a TSV block used for FA. A random cut will definitely hit a TSV, hence it reduces the time and work effort to search for a TSV.



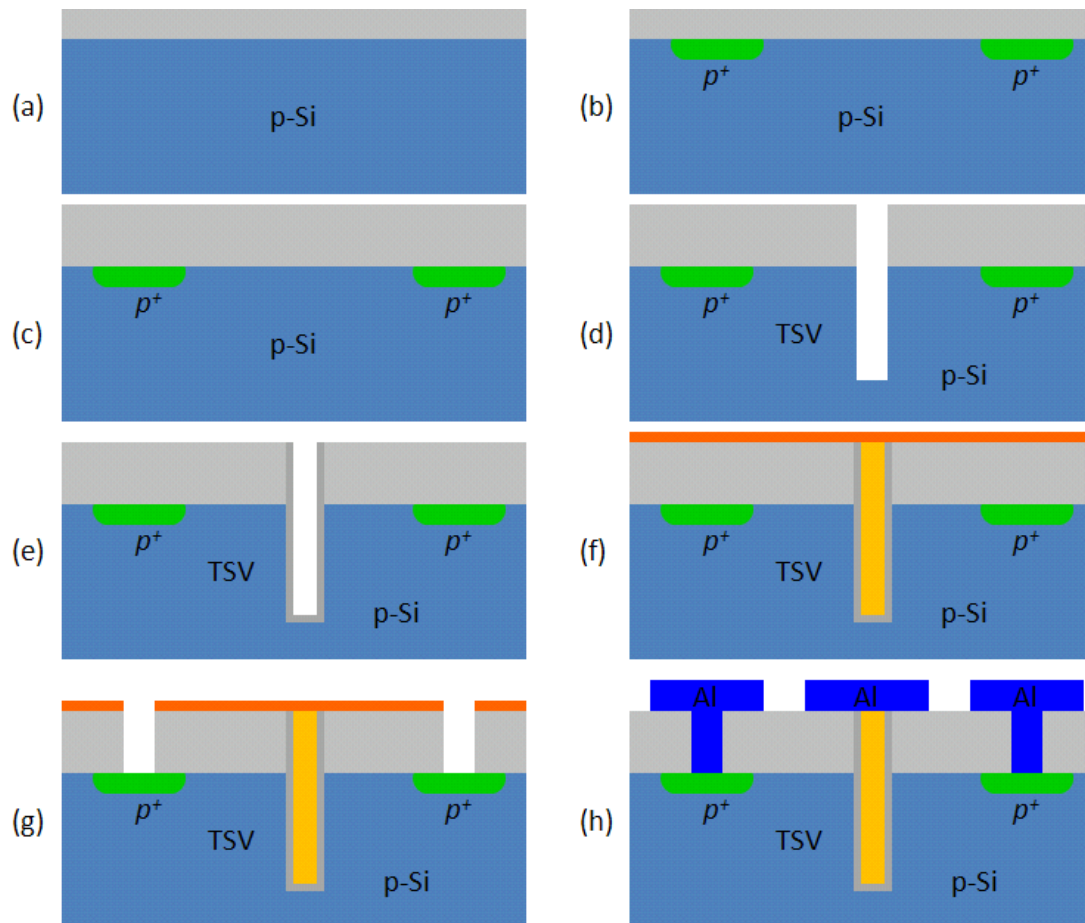
**Figure 3.6: Dummy TSV block for the ease of locating a TSV for failure analysis. A random cut will definitely cut through a TSV.**

### 3.3 Fabrication Processes

#### 3.3.1 Electrical Structure Fabrication Process

Figure 3.7 shows schematically the process flow of the TSV structure for electrical characterization. The TSV structures are fabricated on a *p*-type 8" Si wafer with a resistivity in the range of 6 - 9  $\Omega\text{cm}$ . Firstly, a 100 Å thermal oxide layer is grown on top of the Si wafer to protect the wafer from the subsequent *p*<sup>+</sup> doping implantation, then boron implantation is done to act as an electrical ground. The implant condition used is  $2 \times 10^{16} \text{ cm}^{-2}$  at 150 keV and activation is performed at 1050°C for 60 min. Next, a 8000 Å CVD oxide is deposited, as shown in Figure 3.7 (a), (b) and (c). To form the via, the oxide is patterned using photolithography and etched away to be used as the hard mask for the via formation by DRIE Si etch using a cyclic etching-passivation BOSCH process (Figure 3.7 (d)). Subsequently, the isolation liner is deposited in a plasma-enhanced CVD (PECVD) chamber at temperature < 400°C using tetraethylorthosilicate (TEOS) and Black Diamond precursors for oxide and low- $\kappa$  liner respectively, as shown in Figure 3.7 (e). The Black Diamond used is one of the common low- $\kappa$  dielectrics in industry for the 90/65 nm nodes (Applied Materials). Prior to the TSV Cu filling, a Ta barrier and a Cu seed layer are sputtered using a PVD process in the ENDURA deposition chamber. Subsequently, Cu electroplating (ECP) is carried out till the via hole is fully filled and the TSV is formed. We used the RENA system and Enthone or Shanghai XinYang chemical solution for the ECP process. It is worth pointing out that the acid Cu plating process was specially developed for filling blind micro-vias and plating through-holes simultaneously. The excess Cu overburden is then removed by a CMP process which uses Rohm and Haas high polish rate slurry which is a colloidal silica-based used in Cu CMP for bulk Cu removal. After the CMP process, a low temperature nitride deposition as well as a Cu annealing are carried out (Figure 3.7 (f)) to stabilize the Cu grain size. Finally,

the contact holes are opened by etching away the silicon nitride and the oxide, then Al is deposited and patterned to form the probing pad for electrical probing (Figure 3.7 (g) and (h)). Alternatively, one can also deposit blanket Al at the backside of the wafers for grounding.



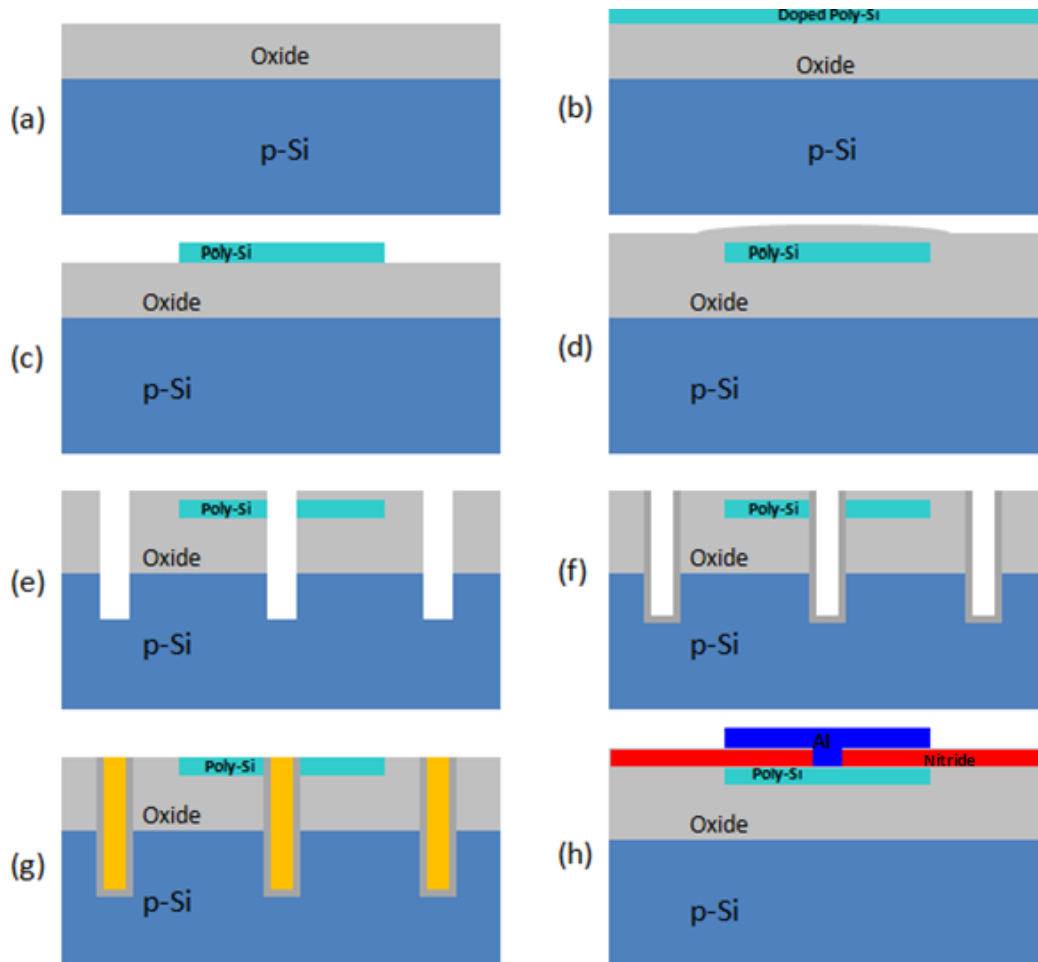
**Figure 3.7: Schematic process flow of a TSV structure for electrical characterization: (a) 100 Å thermal oxide deposition; (b) boron implantation; (c) 8000 Å CVD oxide; (d) via formation by DRIE Si etch and using oxide as the hard mask; (e) liner deposition; (f) Ta barrier/Cu seed deposition followed by Cu ECP, Cu CMP to remove the Cu overburden and nitride passivation deposition; (g) contact open; (h) Al metallization and patterning.**

### 3.3.2 Thermal Structure Fabrication Process

Figure 3.8 shows the schematic process flow of the TSV structure for thermal dissipation characterization. The TSV structures are fabricated on a *p*-type 8" Si wafer with a resistivity range of 6-9  $\Omega\text{cm}$ , same as the wafer used for fabrication of TSV structure for electrical characterization. Firstly, 2000 Å of thermal oxide are grown on top of the Si wafer, and after that 5000 Å of poly-Si are deposited at 580°C. In the poly-Si deposition process,  $\text{PoCl}_3$  is used as the doping precursors and the annealing process after deposition is carried out at 900°C for 30 min. Subsequently, the doped poly-Si is patterned and etched to form the resistor liner as a heat generator (Figure 3.8 (a), (b) and (c)) in the form of a Kelvin structure. Then a 1  $\mu\text{m}$  CVD oxide is deposited using PECVD at 350°C. Oxide CMP is then carried out to achieve a surface with no topography. Subsequently, all the standard TSV fabrication process is carried out as described earlier. Vias are firstly formed by etching away the oxide and doped poly-Si layers followed by the DRIE BOSCH process for deep Si etch (Figure 3.8 (d) and (e)). Subsequently, the TSV liner is deposited by PECVD at 400°C and 350°C using TEOS and Black Diamond as precursors for oxide and the low- $\kappa$  liner, respectively, which is identical with what was used in the fabrication of the TSVs for electrical characterization. Ta barrier and Cu seed layer sputtering are then carried out in an ENDURA deposition chamber, then the Cu ECP is carried out till all the TSVs are fully filled, and CMP is carried out by using the same process of the electrical structures (Figure 3.8 (f) and (g)). After Cu annealing is carried out at 200°C in  $\text{N}_2$  for 30 min, finally the passivation nitride is opened and Al is deposited and patterned to form the probing pad for testing, completing the process (Figure 3.8 (h)).

The thermal structure basically consists of a doped poly-Si line as a heat generator surrounded by or beneath with the TSVs. It was used to study how the heat can be conducted

away through TSVs to the Si substrate, and how the TSV density and size can affect the heat conduction.



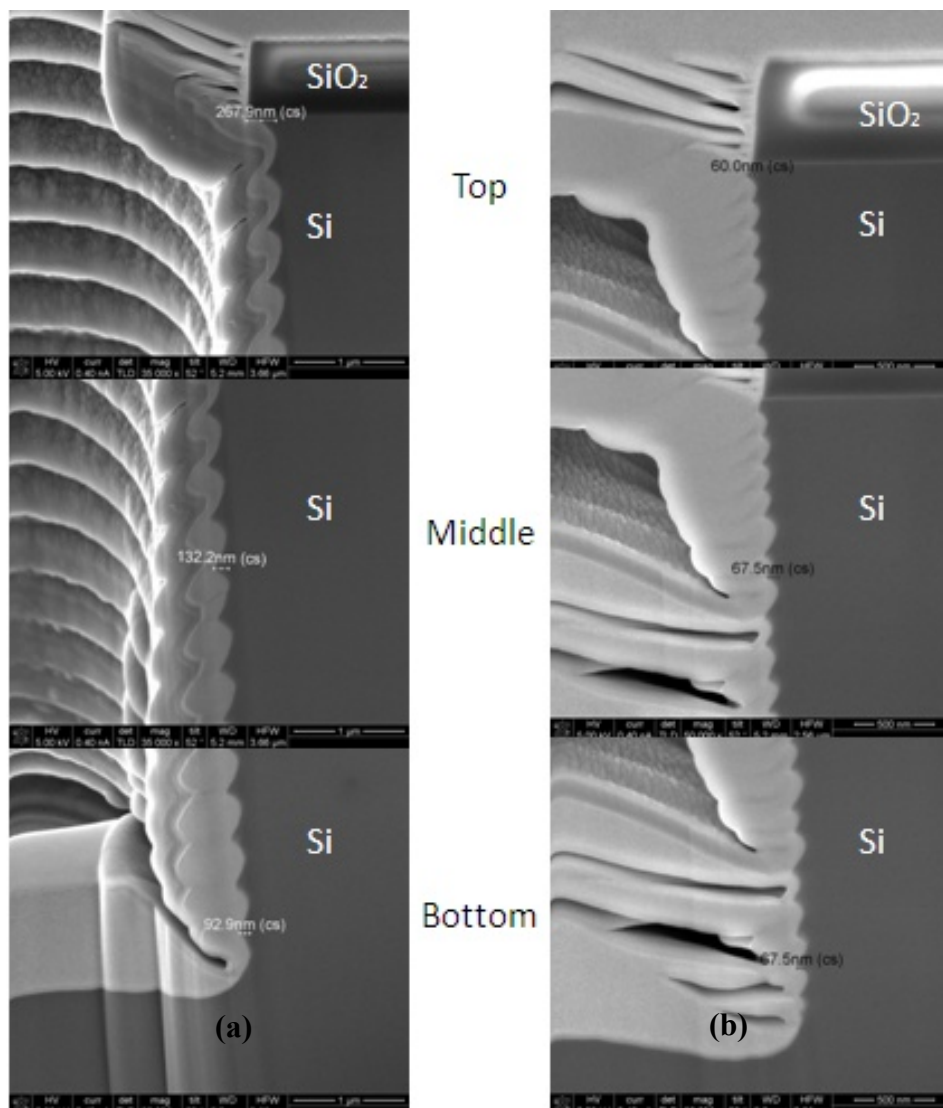
**Figure 3.8: Schematic process flow of TSV structure for thermal property study: (a) 2000 Å thermal oxide deposition; (b) 5000 Å poly-Si deposition,  $\text{PoCl}_3$  doping and annealing; (c) doped poly-Si etch; (d) 1  $\mu\text{m}$  CVD oxide deposition; (e) oxide CMP to flatten the surface and via formation by DRIE Si etch; (f) liner deposition and Ta barrier/Cu seed layer sputtering; (g) Cu ECP followed by Cu CMP to remove Cu overburden; (h) nitride passivation, contact open and Al metallization and patterning.**

### 3.4 Process Control and Optimization

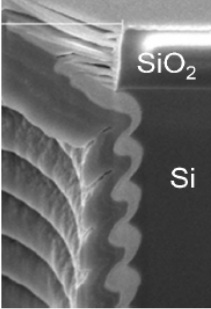
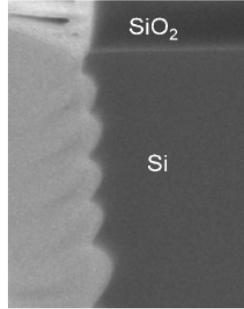
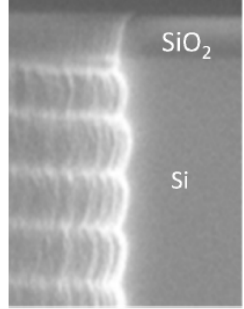
In summary, the major fabrication steps of TSV include DRIE Si etch, dielectric liner deposition, barrier/Cu seed layer deposition, Cu filling by Cu ECP, and Cu overburden removal by Cu CMP [3.5]. All the process steps are critical in forming a stable and robust TSV and optimization of the process to achieve this will be essential.

#### 3.4.1 DRIE Si Etch

The sidewall roughness from the scalloping effect by the cyclic etching and passivation of the BOSCH process and oxide hard-mask undercut (also known as over-hang) must be kept as small as possible. If the sidewall roughness or the undercut is too significant, it would be a challenge for the subsequent dielectric liner to form in a conformal liner which will induce a higher leakage current. The same reason applies for achieving a conformal Ta barrier and Cu seed layer as well which will lead to incomplete Cu filling or voids inside the TSV, and thus reduced TSV yield and reliability. After the initial DRIE run (the value of gas flows are 130 sccm, 13 sccm and 110 sccm for SF<sub>6</sub>, O<sub>2</sub> and C<sub>4</sub>F<sub>8</sub> respectively), the resulting average sidewall scalloping was ~120 nm and the undercut was ~240 nm, as shown in Figure 3.9 (a). By adding 20 sccm of C<sub>4</sub>F<sub>8</sub> during the etching cycle, the sidewall scalloping and undercut are both improved: the sidewall roughness is reduced to ~70 nm and the undercut is ~60 nm, as shown in Figure 3.9 (b). In order to eliminate the undercut completely, a double-mask step can be used to etch the oxide hard-mask and Si separately (Process C). In this process, the opening in the second mask layer is designed to be smaller than the first one. Table 3.1 presents a summary of the etching results of the TSV [3.6].



**Figure 3.9: Unfilled TSV after DRIE Si etch; (a) Initial results obtained with the standard recipe show sidewall scalloping of ~120 nm and undercut of ~240 nm; (b) Improved results show sidewall scalloping of ~70 nm and undercut of ~60 nm [3.2].**

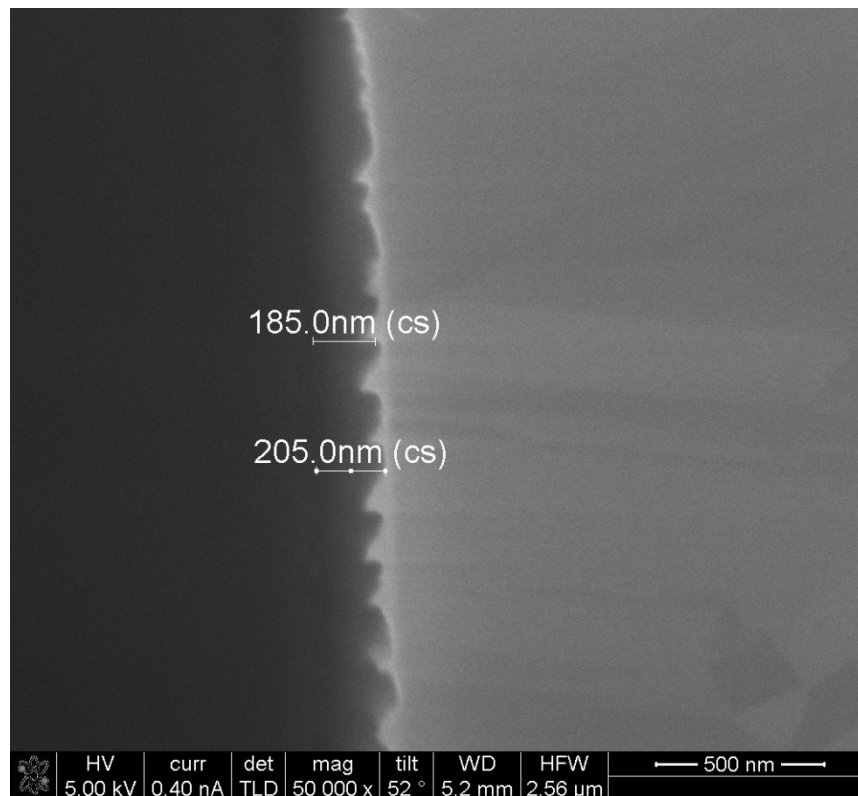
Process	A	B	C
Mask	Single	Single	Double
Etching Gas	SF <sub>6</sub> , O <sub>2</sub>	C <sub>4</sub> F <sub>8</sub> , SF <sub>6</sub> , O <sub>2</sub>	C <sub>4</sub> F <sub>8</sub> , SF <sub>6</sub> , O <sub>2</sub>
Passivation Gas	C <sub>4</sub> F <sub>8</sub>	C <sub>4</sub> F <sub>8</sub>	C <sub>4</sub> F <sub>8</sub>
Etch Profile <i>(SEM image of unfilled TSV)</i>			
Roughness (nm)	107-129	68-75	50-75
Undercut (nm)	239	60	~0

**Table 3.1: Comparison of TSV etching processes and profiles. When a single mask step is used, the addition of C<sub>4</sub>F<sub>8</sub> during the etch cycle improves the scallop sidewall roughness as well as oxide hard-mask undercut. The undercut is negligible of a double-mask etching step is used to etch the SiO<sub>2</sub> hard-mask and Si separately [3.6].**

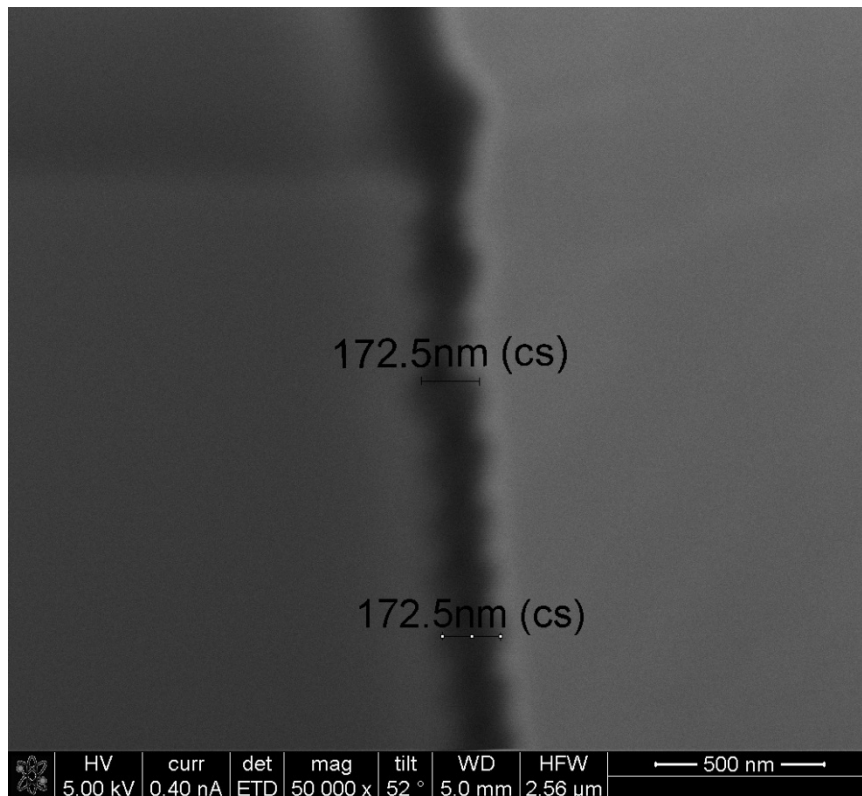
### 3.4.2 Dielectric Liner Deposition

In this work, several materials and material combinations are utilized and integrated as the dielectric liner of the TSV structure. Oxide is the commonly used material as the dielectric liner of TSV due to its good dielectric properties and complementary metal–oxide–semiconductor (CMOS) process compatibility. Figure 3.10 shows the FIB image of an oxide liner deposited at 400°C in a PECVD chamber. The step coverage, which is defined as the ratio of the thickness of a film over a step edge to the thickness in a flat area, of the oxide liner is continuous and is around 35% and the average thickness is ~ 200 nm.

When the TSV is used for signal transmission, its parasitic capacitance has the most predominant impact on the circuit operation [3.7] and must be addressed carefully. A large capacitance can result in large signal latency and power consumption. It is therefore imperative to reduce the TSV capacitance either by selecting the optimum dimension or appropriate material. The usage of a low- $\kappa$  dielectric can significantly reduce the CMOS backend interconnect capacitance and provide many advantages in circuit performance for deep submicron technology nodes [3.8]. Since the low- $\kappa$  dielectric and its deposition process are compatible with the TSV process, it can be used in principle to reduce the TSV capacitance. In this work, a low- $\kappa$  material is successfully integrated in the TSV structure as the dielectric liner with an average thickness of  $\sim 200\text{nm}$ , as shown in Figure 3.11. It is carried out at  $350^\circ\text{C}$  in a PECVD chamber using black diamond as the precursor.



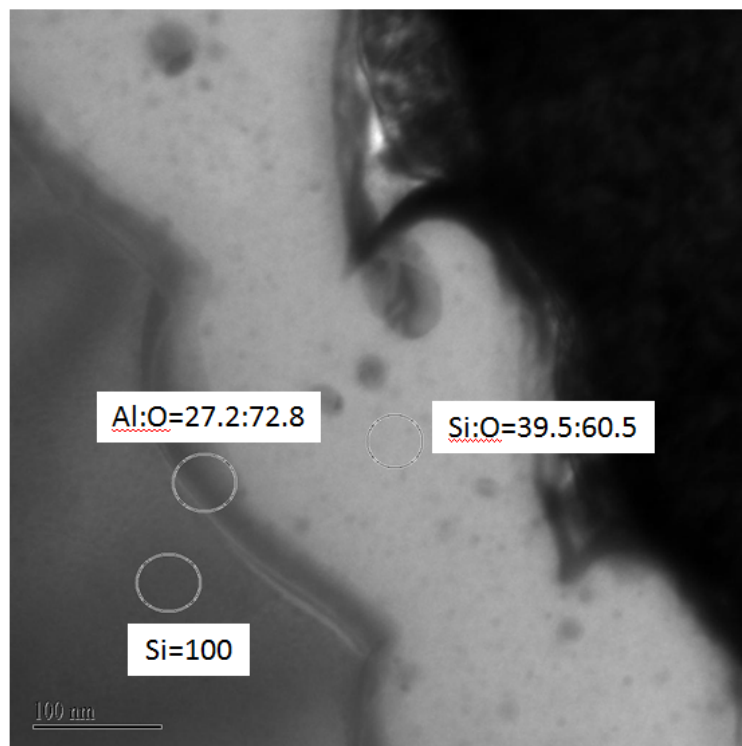
**Figure 3.10: FIB image of TSV structure shows conformal oxide liner deposition. The average thickness of the oxide liner is  $\sim 200\text{ nm}$ .**



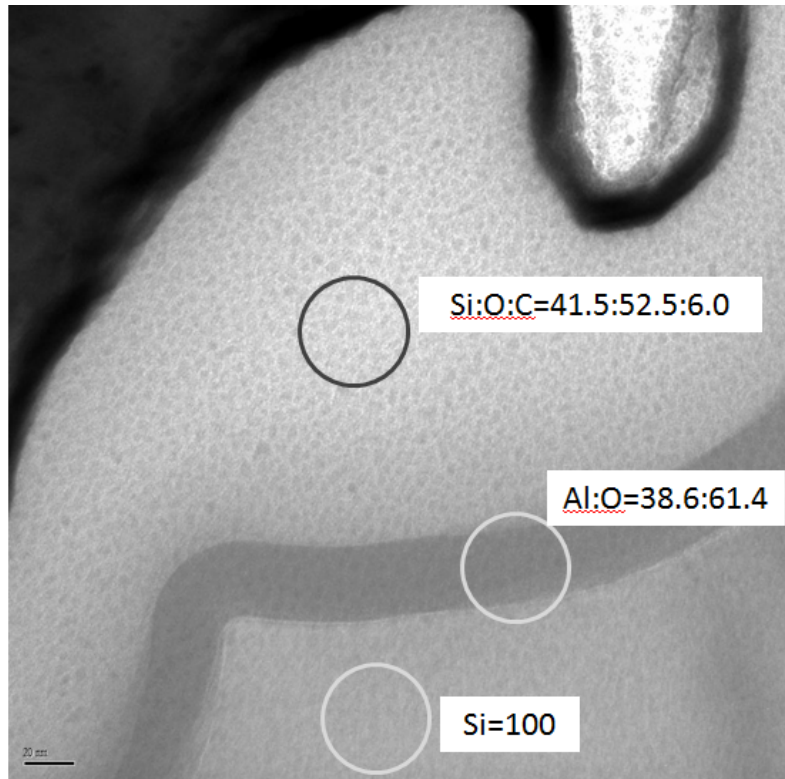
**Figure 3.11: FIB image of TSV structure shows conformal low- $\kappa$  liner deposition. The average thickness of the oxide liner is ~200 nm.**

On the other hand, capacitance stability is also an important consideration in an integrated circuit (IC) design. In order to prevent instabilities which can appear in the case of non-uniform hotspot heating across an area, a temperature-independent TSV capacitance is ideally desired. Negative fixed charge in the oxide liner can be utilized to effectively shift the TSV's  $C$ - $V$  curve so that the stable accumulation capacitance is maintained within the ranges of voltages and temperatures of interests. The density of the fixed charge depends on several factors such as the oxidizing ambient, deposition temperature, silicon orientation, cooling rate, and subsequent annealing cycle. It is worth noting that the negative fixed charge in CVD

oxide has also been reported previously [3.9, 3.10]. By process tuning, i.e. by changing the ratio of gas flows and deposition RF power, the desired amount of negative fixed charges can be obtained. Other than the process tuning, the desired  $C-V$  shift can also be achieved by  $\text{Al}_2\text{O}_3$ -induced negative fixed charge. A very thin layer of  $\text{Al}_2\text{O}_3$  is successfully integrated in between the Si substrate and the dielectric liner by utilizing atomic-layer-deposition (ALD) process. As shown in Figure 3.12, an  $\text{Al}_2\text{O}_3$  layer  $\sim 100 \text{ \AA}$  thick was inserted in-between the Si and oxide liner. An energy dispersive X-ray spectroscopy (EDX) performed on the different material layers confirmed that the atomic ratio of Al to O was 27.2 to 72.8. Figure 3.13 shows that the integration of a  $\sim 100 \text{ \AA}$   $\text{Al}_2\text{O}_3$  layer was extended in-between the Si and a low- $\kappa$  liner. EDX results show that the atomic ratio of Al to O was 38.6 to 61.4.



**Figure 3.12: HRTEM image of liner. Conformal deposition of an  $\text{Al}_2\text{O}_3$ /oxide dielectric liner was achieved with ALD and PECVD. An atomic ratio of Al:O=27.2:72.8 of the  $\text{Al}_2\text{O}_3$  layer was obtained from EDX measurements.**

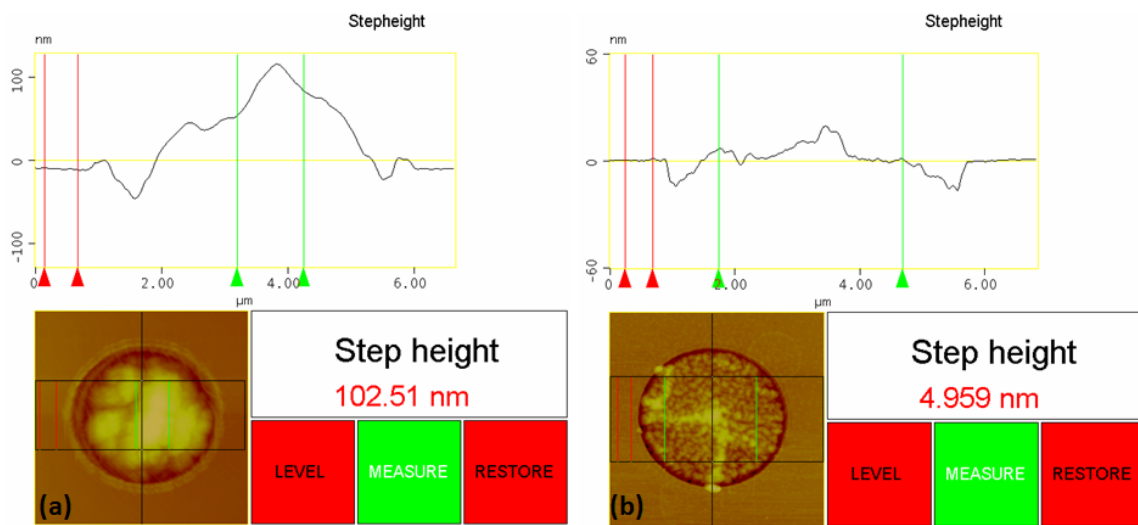


**Figure 3.13: HRTEM image of the liner stack. The  $\text{Al}_2\text{O}_3$  layer was deposited by ALD and the low- $\kappa$  dielectric (SiOC) liner was PECVD deposited conformally at a temperature of  $350^\circ\text{C}$ .**

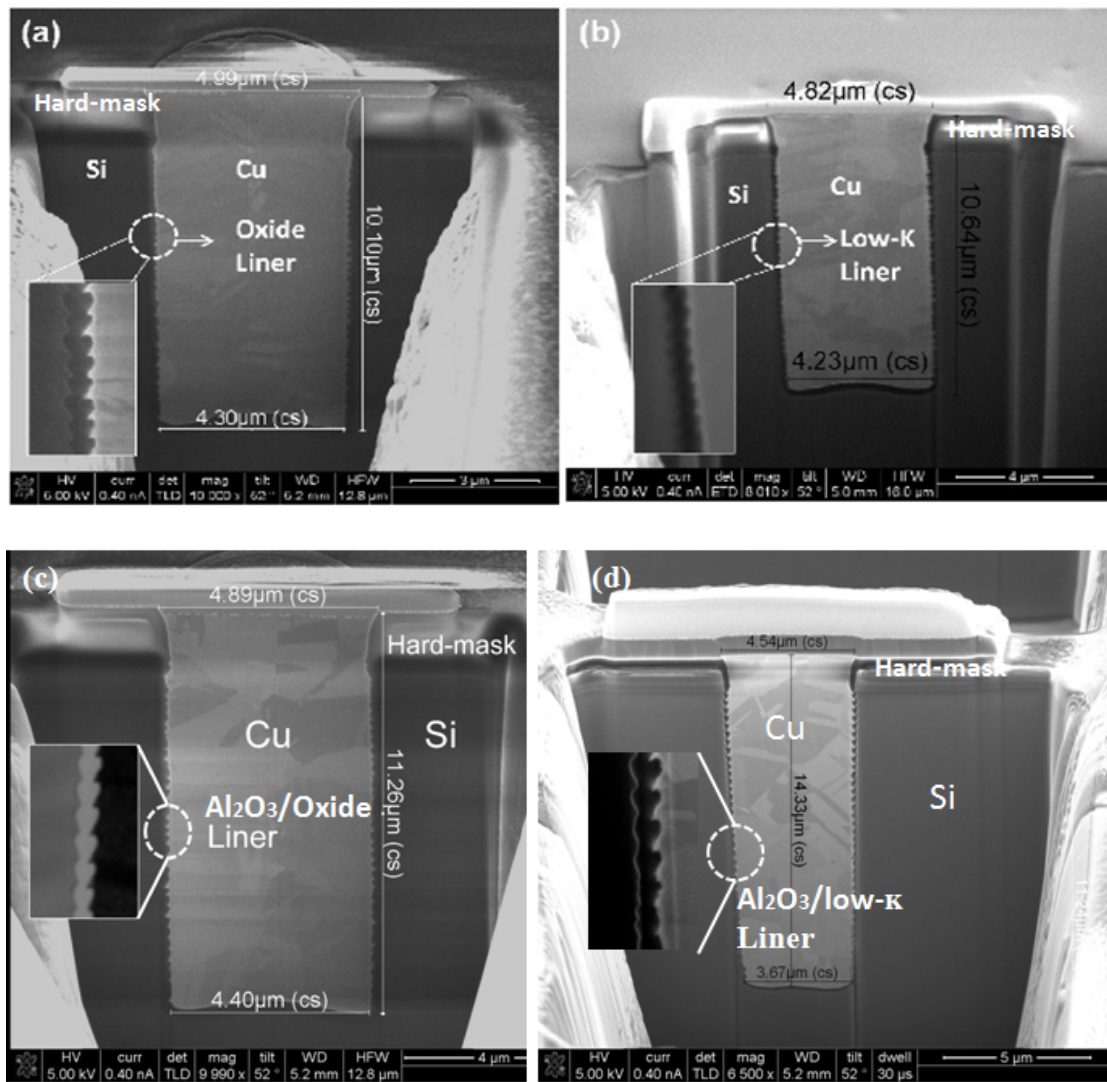
### ***3.4.3 Ta Barrier/Cu Seed Layer Deposition and Cu ECP***

Ta barrier/Cu seed layer deposition and Cu ECP are very critical for the TSV structure fabrication. Non-conformal Ta barrier and Cu seed layer deposition may lead to incomplete Cu filling of the via hole. Additionally, Cu ECP related issues are very commonly seen during the process, which includes bottom voids, pinch off and Cu protrusion [3.11]. In this work, the Ta barrier and Cu seed were sputtered using PVD in an ENDURA deposition

chamber. Subsequently, Cu electroplating (ECP) was carried out to fully fill the TSV. For this purpose we use a RENA system and Enthone chemical solution. The acid copper plating process was specially developed for filling blind micro-vias and plating through-holes simultaneously in this work. In order to control the Cu protrusion, a combination of annealing and CMP touch up is used. In Figure 3.14, AFM surface profiles show that Cu protrusion is reduced from 102.5 nm (Figure 3.14 (a)) to 5.0 nm (Figure 3.14 (b)) with this optimization [3.6]. Figure 3.15 shows the FIB images of Cu filled TSV with different material selections as the dielectric liner. Excellent step coverage was achieved and all the TSVs were filled with Cu without any voids or delaminations.



**Figure 3.14: Cu protrusion is controlled with proper annealing to allow optimum Cu grain growth, the Cu protrusion is reduced from (a) 102.5 nm to (b) 5.0 nm [3.6].**

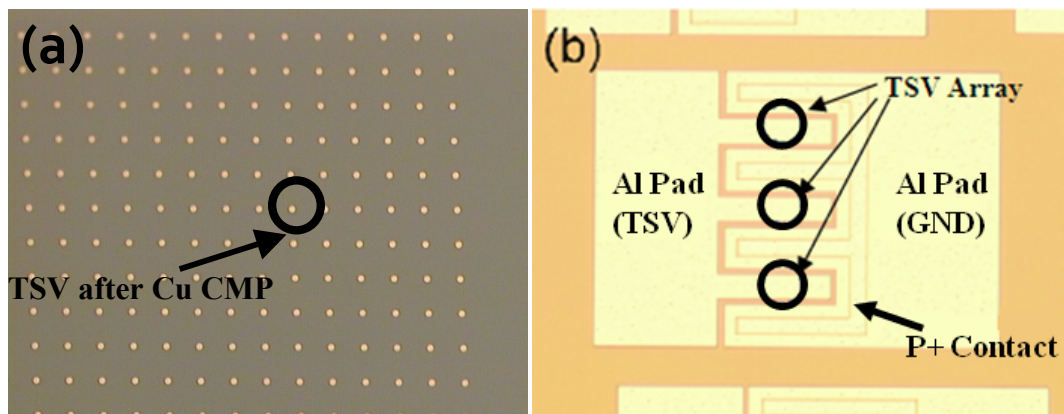


**Figure 3.15: FIB images of TSVs with  $\sim 5 \mu\text{m}$  diameter and  $\sim 10\text{-}15 \mu\text{m}$  depth, filled with Cu and lined with: (a) PETEOS oxide; (b) Black diamond low- $\kappa$  material; (c) Bi-layer of  $\text{Al}_2\text{O}_3$  and oxide; (d) Bi-layer of  $\text{Al}_2\text{O}_3$  and low- $\kappa$ , as the isolation liners, respectively. Conformal deposition was achieved and no voids or delaminations can be observed.**

### 3.4.4 Cu CMP

The Cu overburden from previous Cu ECP process was subsequently polished by a Cu CMP process. In this work, a Rohm and Haas high polish rate slurry was used. This is a colloidal silica-based slurry used in Cu CMP for bulk Cu removal.

Figure 3.16(a) is the plan view of an array of TSVs, each with diameter of 5  $\mu\text{m}$  after removing the Cu overburden by CMP from microscope. It shows that the Cu overburden was completely removed. Figure 3.16(b) shows the final electrical MOS structure formed by TSV for electrical probing testing. From the microscope image, it can be seen that the Si substrate is grounded by using a  $p^+$  contact. The probe pad capacitance which is a source of secondary parasitics during the  $C$ - $V$  measurement of the TSV, was kept low by using thicker oxide below the Al probe pad and formation of TSV array to increase the effective TSV area. The oxide below the Al probe pad is much thicker ( $\sim 1600$  nm) than the TSV liner ( $\sim 200$  nm). It is also possible to de-embed the probe pad capacitance by forming dummy pads without TSVs.



**Figure 3.16: (a) Optical microscope photo of a plan view of a TSV array (each TSV has  $\text{Ø}=5 \mu\text{m}$ ) after CMP, clearly showing no sign of residual Cu debris; (b) Electrical MOS structure formed by TSV for probing. The Si substrate is grounded using the  $P^+$  contact. The probe pad capacitance is kept low by using thicker oxide below the Al probe pad and formation of TSV array to increase the effective TSV area [3.6].**

### 3.5 Summary

In this chapter, a wafer level design of the TSV structures was first discussed. TSV structures designed for electrical characterization and thermal properties as well as dummy TSV blocks were introduced. The detailed fabrication process flows of these TSV structures using CMOS process were then presented. Subsequently, process observations and related issues were also highlighted. It was found that the TSV scalloping effect and undercut have been significantly improved for better leakage control and better Cu filling by optimizing the DRIE BOSCH process conditions. In addition, a low- $\kappa$  material (Black diamond) has been integrated successfully and conformally as the TSV dielectric liner. In order to stabilize the CV characteristics of the TSV to the operating voltage, a thin layer of  $\text{Al}_2\text{O}_3$  has been integrated in-between the Si substrate and the dielectric liner for both oxide and low- $\kappa$  black diamond. This design is critical to induce negative fixed charge in the  $\text{Al}_2\text{O}_3$  layer in order to control and optimize the TSV capacitance performance. We also showed that the fabricated TSV structures can be achieved with no void or delaminations. Cu protrusion was improved by proper annealing and CMP touch-up. Finally, all Cu overburdens were fully polished away by our optimized Cu CMP process.

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# Chapter 4: Electrical Characterization Results and Discussions

## 4.1 Introduction

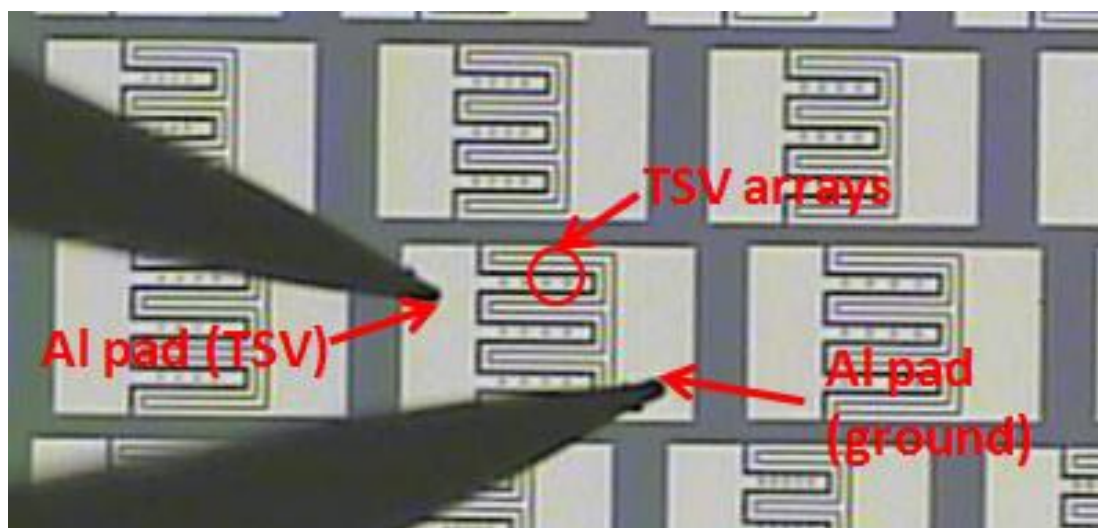
Through-silicon-via (TSV) provides the electrical connection between adjacently stacked integrated circuits (ICs). This is different from the conventional planar interconnects which are embedded in dielectric. As TSV is embedded in the Si substrate, its electrical coupling effect with the Si substrate through the circular metal-oxide-semiconductor (MOS) structure formed has to be considered. In analogy with a typical MOS capacitor, the metal core (Cu) is the gate, while the surrounding dielectric and the Si substrate in which it is embedded represent the oxide and semiconductor, respectively. Hence, the TSV's capacitance-voltage ( $C-V$ ) curve will exhibit the same accumulation, depletion and inversion regions. The  $C-V$  curve of a power TSV follows the high-frequency curve in the inversion region due to the presence and influence of the switching noise typical to power distribution lines. On the other hand, due to the fast digital signal change in a signal TSV, its  $C-V$  curve follows the deep depletion characteristic in the inversion region [4.1]. The TSV parasitic capacitance plays a very important role in the circuit operation, hence the TSV capacitance behavior must be fully understood and controlled. In addition, a good TSV used for signal transmission should possess the ability to retain the signal. This signifies that a signal leakage as small as possible is desired. Hence, current-voltage ( $I-V$ ) measurements should be carried out as well in order to monitor the leakage of the various dielectric materials integrated as the TSV liner.

Some of the results in this chapter have been published in our publications as follows:

1. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, “Design, Fabrication and Electrical Characterization of TSV”, *12th Electronics Packaging Technology Conference (EPTC)*, December, 2010.
2. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, “Through Silicon Via (TSV) Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current”, *International Conference on Solid State Devices and Materials (SSDM)*, September, 2011.
3. **L. Zhang**, R. I Made, H. Y. Li, S. Gao, G. Q. Lo, D. L. Kwong, and C. S. Tan, “Spatial Variation of TSV Capacitance and Method of Stabilization with Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge at the Silicon-Liner Interface”, *IEEE International Electron Devices Meeting (IEDM)*, December, 2011.
4. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, “Achieving Stable Through-Silicon-Via (TSV) Capacitance with Oxide Fixed Charge”, *IEEE Electron Device Letters*, 32 (5), 2011.
5. **L. Zhang**, D. F. Lim, H. Y. Li, S. Gao, and C. S. Tan, “Through Silicon Via Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current”, *Japanese Journal of Applied Physics*, 51 (4), 2012.
6. **L. Zhang**, L. Peng, H. Y. Li, D. L. Kwong, and C. S. Tan, “Operating TSV in Stable Accumulation Capacitance Region by Utilizing Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge”, *IEEE Electron Device Letters*, 33 (6), 2012.

## 4.2 Measurement Setup

The measurement setup image for electrical  $C-V$  measurements using an Agilent  $CV$  meter is shown in Figure 4.1. For characterization, the input voltage applied was swept from -25 V to 25 V on the Al pad connected to the TSV arrays while the other Al pad was connected to the Si substrate utilizing the  $p+$  contact. The probe pad capacitance, which is a source of secondary parasitic during the  $C-V$  measurement on the TSV, is kept low by using a layer of thicker oxide below the Al probe pad and the formation of TSV array to increase the effective TSV area. It is also possible to de-embed the probe pad capacitance by forming dummy pads without TSVs. Moreover, the electrical field is stressed up to 3 MV/cm for the electrical  $I-V$  measurements.



**Figure 4.1:** Microscope image of the electrical measurement setup. One Al pad is connected to the TSVs, while the other Al pad is connected to the  $p+$  ground. The input voltage was swept from -25 V to 25 V.

### 4.3 Conventional Plasma Enhanced Tetraethylorthosilicate (PETEOS) Oxide Liner

Plasma Enhanced Tetraethylorthosilicate (PETEOS) oxide is the conventional material to be utilized as the dielectric liner of TSV. This is because of several advantages such as good dielectric properties, conformality, and complementary metal–oxide–semiconductor (CMOS) process compatibility. In our experiments, TSV structures with PETEOS oxide as the dielectric liner will be the baseline structures.

#### 4.3.1 Electrical $C$ - $V$ Measurement

Figure 4.2 shows the measured  $C$ - $V$  curve at 1 MHz for two different deposition conditions of the PETEOS oxide liner. The temperature of the two deposition processes are the same ( $\sim 180^\circ\text{C}$ ), but other parameters such as ratio of gas flow and power are adjusted to achieve the desired  $C$ - $V$  characteristics. From Figure 4.2 we can see that the TSV capacitance changes from accumulation to depletion to inversion region as the voltage applied was swept from -30 V to 30 V. This  $C$ - $V$  characteristic demonstrates the behaviour of a MOS capacitor on a  $p$ -type Si substrate. In comparison with process A, the  $C$ - $V$  curve of process B shifts more towards the positive values along the X-axis so that the accumulation capacitance region is obtained within the operating voltage of interests ( $\sim 0$ -5 V). The shift of the  $C$ - $V$  curve in this later case was caused by the fixed charges induced during the PETEOS oxide deposition process. Such negative fixed charge in plasma enhanced chemical vapour deposition (PECVD) oxide has also been reported previously [4.2, 4.3]. In order to calculate the fixed charge density induced during the deposition process, knowledge of the flat-band voltage in

the  $C$ - $V$  curve is required. From a  $C_{ox}$  of  $\sim 1.8 \times 10^{-8}$  F/cm<sup>2</sup> obtained from the measurements, the effective oxide liner thickness is calculated to be  $\sim 192$ nm, by using the equation

$$C_{ox} = \frac{2\pi\epsilon_{ox}L}{\ln\frac{r_1}{r_0}} \quad (1),$$

where  $L$  is the TSV depth,  $r_0$  is the radius of the Cu core and  $r_1$  is the TSV radius (as etched).

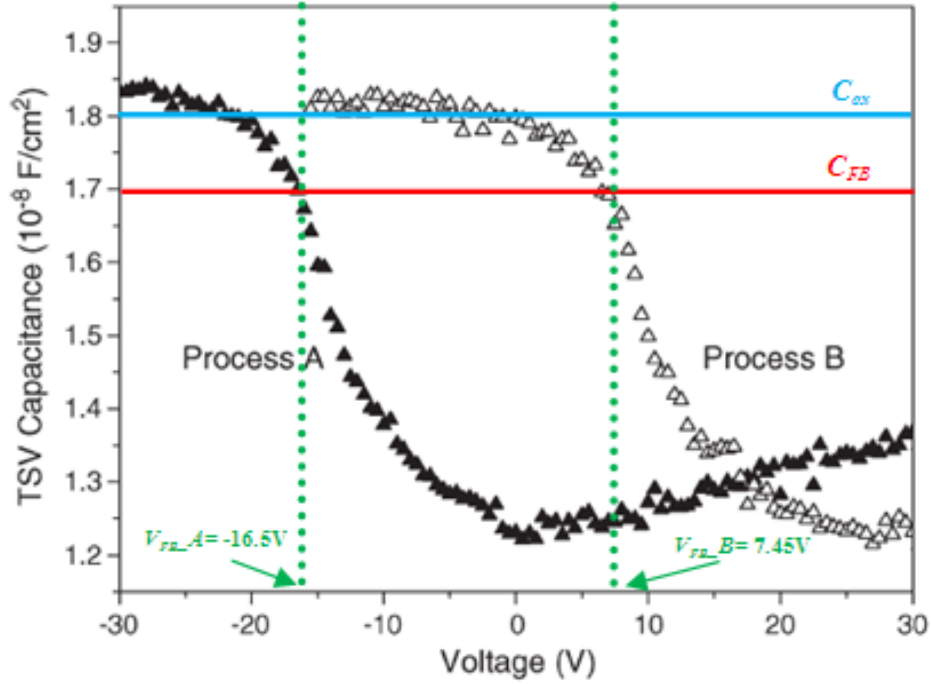
Next, the flat-band capacitance ( $C_{FB}$ ) can be estimated using the equation [4.4]

$$\frac{C_{FB}}{C_{ox}} = \frac{1}{1 + \frac{136\sqrt{T/300}}{t_{ox}\sqrt{N}}} \quad (2),$$

where  $T$  is the temperature in Kelvin,  $N$  is the silicon substrate doping concentration  $\approx 1 \times 10^{16}$  cm<sup>-3</sup>, and  $t_{ox}$  is the oxide liner thickness. By using this equation, we can estimate that  $C_{FB} \approx 0.963C_{ox} \approx 1.7 \times 10^{-8}$  F/cm<sup>2</sup>. Hence the locations of the flat-band voltage ( $V_{FB}$ ) on the  $CV$  plots are  $\sim -16.5$  V and  $\sim 7.3$  V for process A and B, respectively, as shown in Figure 4.2. In the presence of the fixed charge ( $Q_f$ ) in the oxide liner, the relation between  $V_{FB}$  and  $Q_f$  becomes

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} \quad (3),$$

where  $\phi_{ms}$  is the difference in the work function between the gate and the Si. In the case of Cu as the gate,  $\phi_{ms} = -0.22$ V. Hence we can calculate that the fixed charge induced during the oxide liner deposition is  $\sim 1.8 \times 10^{12}$  cm<sup>-2</sup> and  $\sim -8.43 \times 10^{11}$  cm<sup>-2</sup> for process A and process B, respectively.



**Figure 4.2:  $C$ - $V$  characteristic of TSV MOS structure showing clear regions of accumulation, depletion, and inversion. With proper process tuning, negative fixed charge within the oxide liner can cause a flatband voltage shift that stabilizes the TSV capacitance in the accumulation region within the operating voltage region of interest ( $\sim 0$ - $5$  V). The accumulation capacitance of a single TSV with a  $5\ \mu\text{m}$  diameter and  $10\ \mu\text{m}$  depth is  $\sim 28.3$  fF [4.5].**

For baseline process A, the TSV capacitance within the operating voltage ( $\sim 0$ - $5$  V) is the depletion capacitance. Although this capacitance value is lower, its value is not stable as it depends on the substrate doping concentration, small signal frequency and the temperature. The accumulation and depletion capacitances of TSV-MOS embedded in the  $p$ -Si are plotted as a function of substrate temperature in Figure 4.3. The depletion capacitance is susceptible to and increases with temperature while the accumulation capacitance is independent on the

temperature. Figure 4.4 (a) and (b) show the measured  $C-V$  curves at 100 kHz and 2 MHz, respectively, on a planar MOS structure (dielectric thickness is  $\sim 200$  nm). These  $C-V$  curves show that at a smaller frequency signal (100 kHz) when the temperature is higher ( $> 175^\circ\text{C}$ ), the minority carriers (electrons) with enough energy can respond fast enough to form an inversion layer, so that the capacitance is prevented from decreasing further. But at a higher frequency signal (2 MHz), the electrons cannot respond fast enough to form the inversion layer, so that the depletion continues and capacitance continues decreasing as the voltage is swept. In a 3D circuit with TSV distribution across the entire chip, it is essential to ensure that the TSV capacitance is stable. This is because the emergence of hot spots due to non-uniform heating will lead to undesired TSV performance variation across the entire chip and thus complicate the circuit design, if the TSV capacitance varies with the temperature. Therefore, process B satisfies this requirement by inducing enough negative fixed charge during the liner deposition process and hence causing a positive shift in the  $V_{FB}$  so as to ensure that the accumulation capacitance is kept constant within the operating voltage range. The negative fixed charge successfully results in a  $+7.5\text{V}$  shift in  $V_{FB}$  in this experiment.

Operating the TSV in a stable but higher capacitance will not increase the overall parasitic capacitance significantly when the TSV length is only a small fraction of the on-chip interconnects length. However, in high-end multicore processor application, the TSV density is estimated to occupy  $\sim 3\%$  of the silicon area [4.6], and hence the total TSV capacitance is much smaller as compared with the on-chip interconnect capacitance. Thus, the operation of the TSV in the accumulation region for applications that require a stable TSV capacitance at the expense of a slightly higher value, is an important tradeoff. This is required to stabilize the TSV parasitic capacitance as well as to avoid a spatial performance variation of the TSV. It is worth pointing out that the TSV capacitance can still be kept small by proper design so as to meet the parasitic capacitance requirement. In actual applications, in order to minimize

the potential process variation and to have a more stable oxide apacitance, the process tuning can be further optimized to shift the  $V_{FB}$  toward higher voltages.

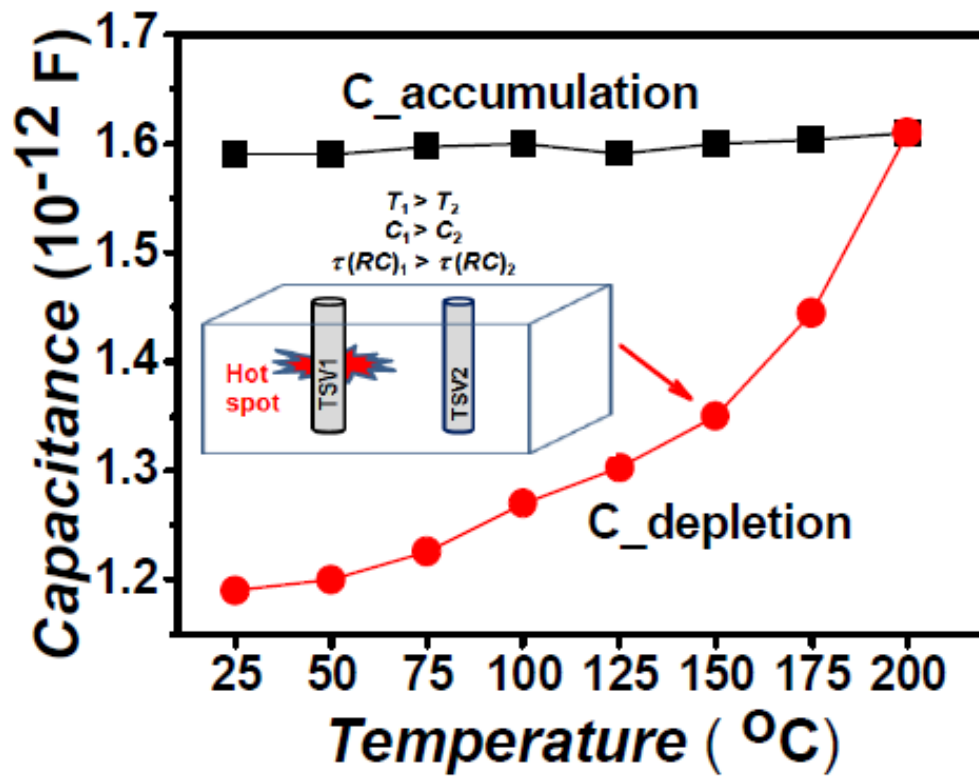
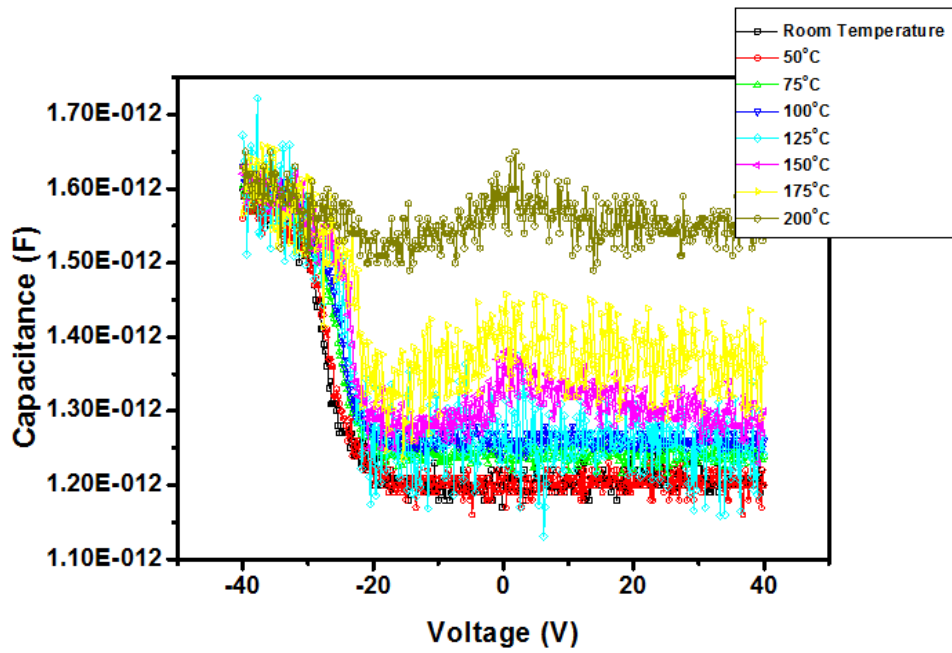
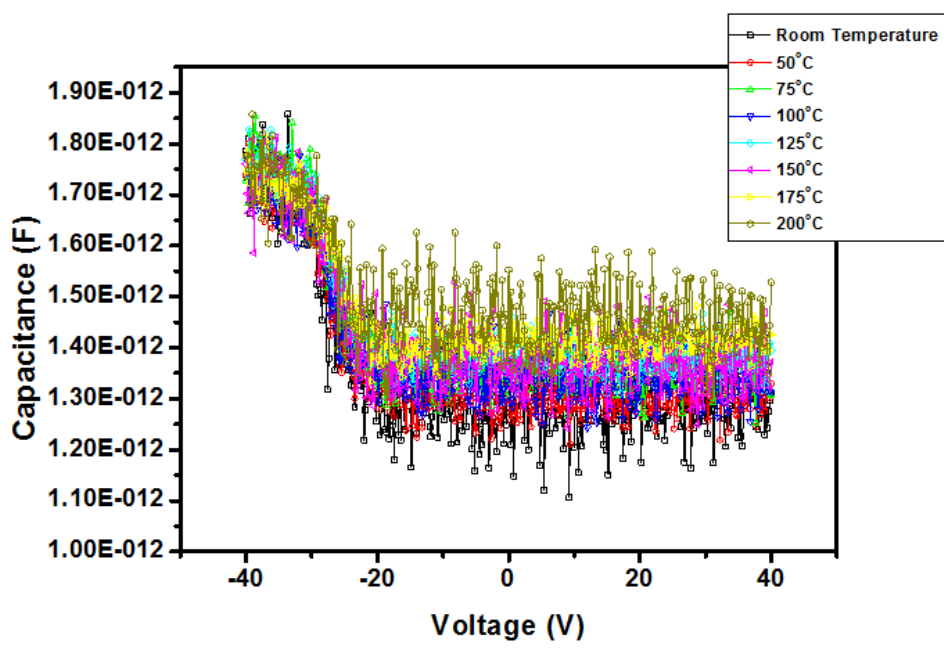


Figure 4.3: While a TSV's accumulation capacitance is stable, its depletion capacitance increases rapidly with substrate temperature [4.7].



(a)

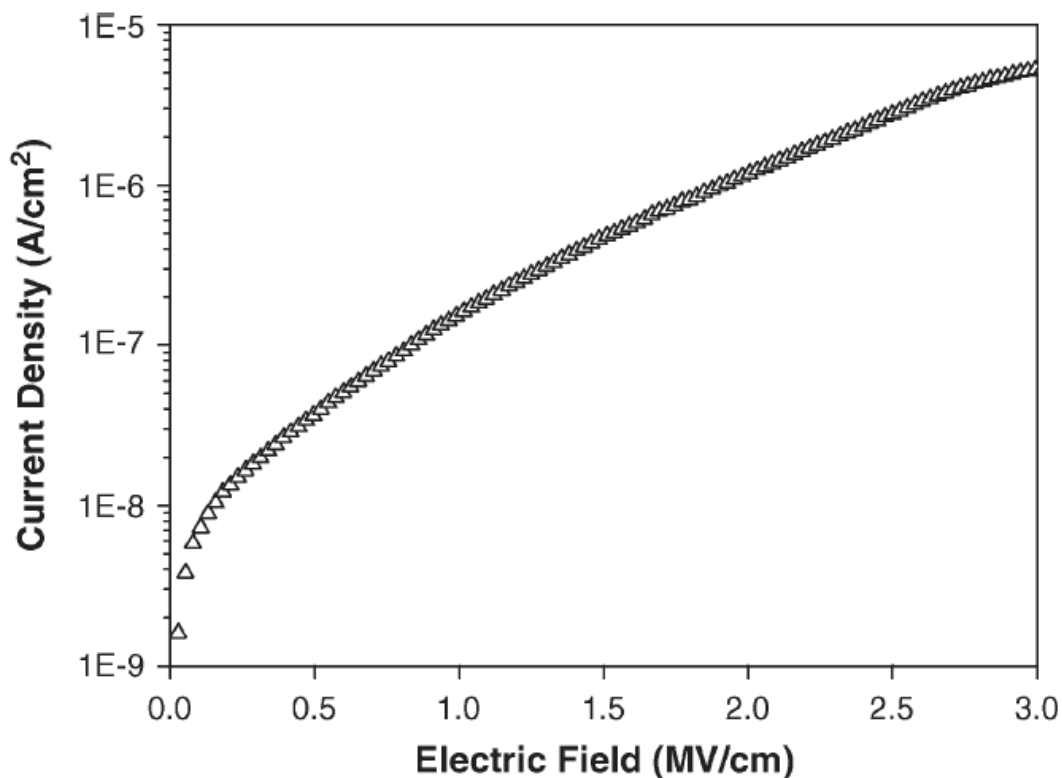


(b)

Figure 4.4: Measured  $C-V$  characteristics of a planar MOS at a small signal frequency of (a) 100 kHz and (b) 2 MHz. It shows that the depletion capacitance varies when the substrate temperature changes and compensating for this change will complicate the circuit design.

### 4.3.2 Electrical $I$ - $V$ Measurements

The  $I$ - $V$  characteristic is used to monitor the leakage of the PETEOS oxide liner using the same samples used for  $C$ - $V$  measurement. From Figure 4.5, the TSV's leakage current is  $\sim 1.2 \times 10^{-6}$  A/cm<sup>2</sup> at an electric field of 2 MV/cm; this value is comparable with the value reported in literature of  $1 \times 10^{-6}$  A/cm<sup>2</sup> [4.8]. In an actual on-chip TSV application, the voltage is of the order of 5 V ( $\sim 0.25$  MV/cm), and therefore, the leakage current is about two orders of magnitude smaller, at  $\sim 10^{-8}$  A/cm<sup>2</sup>. The results of the  $I$ - $V$  measurement also show that at least up to an electric field of 3 MV/cm, there is no abrupt breakdown observed for the PETEOS oxide liner.



**Figure 4.5: Leakage current through the oxide liner from  $I$ - $V$  measurement. No hard breakdown is observed. The leakage current density at an electric field of 2 MV/cm is  $\sim 1.2 \times 10^{-6}$  A/cm<sup>2</sup> which is comparable with the reported value of  $1 \times 10^{-6}$  A/cm<sup>2</sup> [4.5, 4.8].**

#### 4.4 Black Diamond Low- $\kappa$ Liner

In order to enhance the 3D IC performance, TSV should introduce a small parasitic capacitance. More specifically, in the previous section, we have introduced and demonstrated the use of the accumulation capacitance within the operating voltage of interests ( $\sim 0-5$  V) since it offers independence on the substrate temperature fluctuations but at the expense of a slightly higher capacitance value. The simulated  $C-V$  characteristics of an MOS structure at high frequency as a function of the dielectric constant ( $\kappa$ ) are shown in Figure 4.6. In this simulation, the liner thickness is taken as 200 nm while the substrate doping ( $N_a$ ) is  $1 \times 10^{16}$   $\text{cm}^{-3}$ . In principle, the TSV's capacitance can be lowered by using a liner with a small  $\kappa$  value, as predicted by the simulation result in Figure 4.6.

In this work, the results of this simulation are confirmed and implemented in practice by having the low- $\kappa$  liner successfully integrated as the TSV dielectric liner by using the Applied Material's Black Diamond Plasma-Enhanced Chemical Vapor Deposition (PECVD) technology to lower down the TSV accumulation capacitance. The low- $\kappa$  liner deposition process includes two major steps: a) The deposition step is carried out at  $350^\circ\text{C}$  for 49.5 seconds with a pressure of 4 torr, a 600 W radio-frequency (RF) power and 100 sccm  $\text{O}_2$  and 600 sccm TMS gases flow; then, b) A helium treatment step is performed for 20 seconds at  $350^\circ\text{C}$  with a pressure of 8.7 torr and a 750 W RF power, at a helium gas flow of 1300 sccm.

The low- $\kappa$  liner is thus successfully integrated in the TSV structures as previously shown in Chapter 3, with excellent step coverage and no void or delamination filling with Cu.

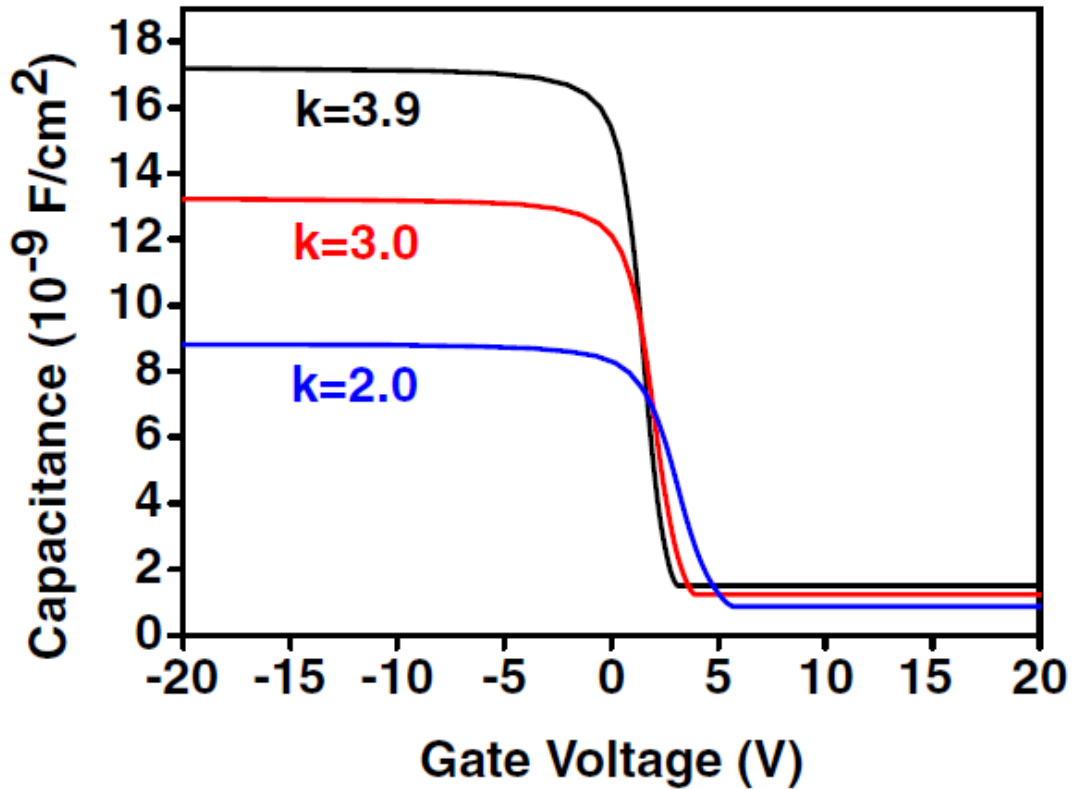


Figure 4.6: Capacitance reduction in a TSV's MOS structure using a low- $\kappa$  dielectric 200 nm thick and a substrate doping,  $N_a$ , of  $1 \times 10^{16} \text{ cm}^{-3}$ [4.9, 4.10].

#### 4.4.1 Electrical $C$ - $V$ Measurements

Figure 4.7 shows the comparison between the measured  $C$ - $V$  characteristics at 100 KHz for both PETEOS oxide and low- $\kappa$  liners at an average liner thickness of  $\sim 200$  nm. From these measurements, the effective low- $\kappa$  value is estimated to be  $\sim 2.88$  by using the equation (1) in previous section. The low- $\kappa$  liner dielectric capacitance value is lowered down by  $\sim 27.6\%$  when compared with that of the PETEOS oxide liner. We can also observe that the  $C$ - $V$  curve of the PETEOS oxide liner TSV shifted negatively in the  $V_{FB}$  due to the positive fixed charge induced during the liner deposition step, which is reported to be  $\sim 1.8 \times 10^{12} \text{ cm}^{-2}$  in the previous section, while the low- $\kappa$  liner deposition process is observed to have much less

induced fixed charges. In Table 4.1, the measured capacitance values are compared with the analytical data calculated based on the MOS model [4.11]. A small discrepancy is seen and this is attributed to the non-uniformity in the liner thickness in the actual TSV structure arising from process-induced sidewall roughness.

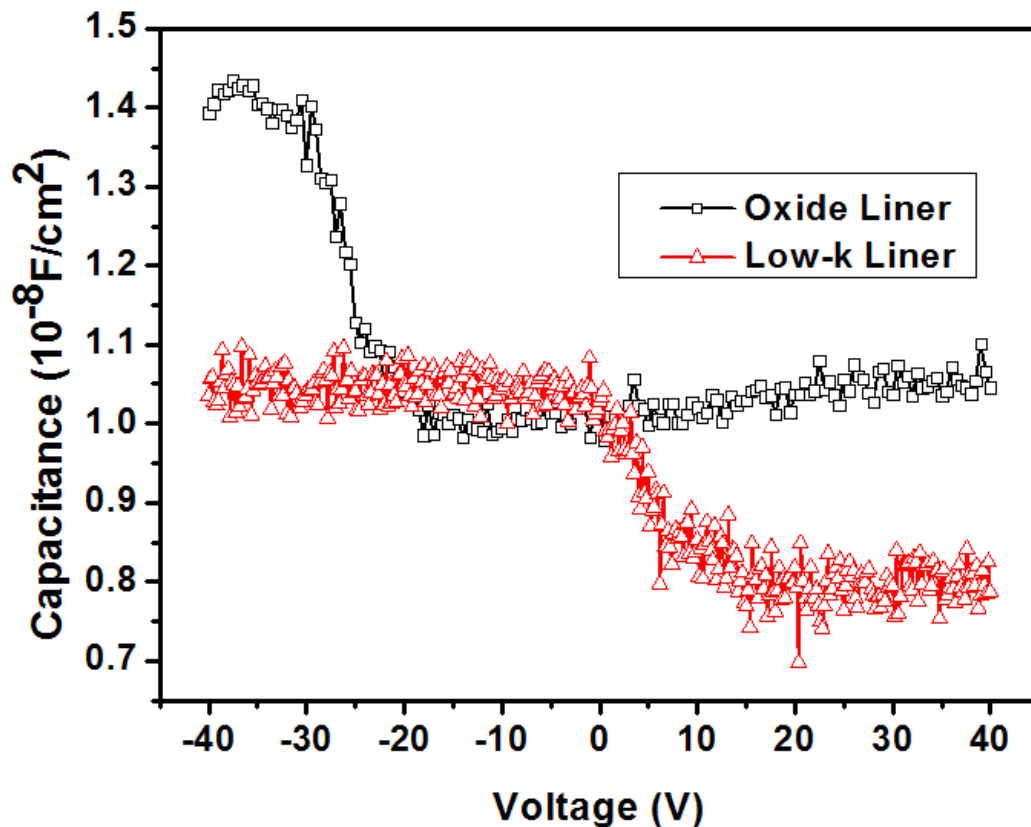


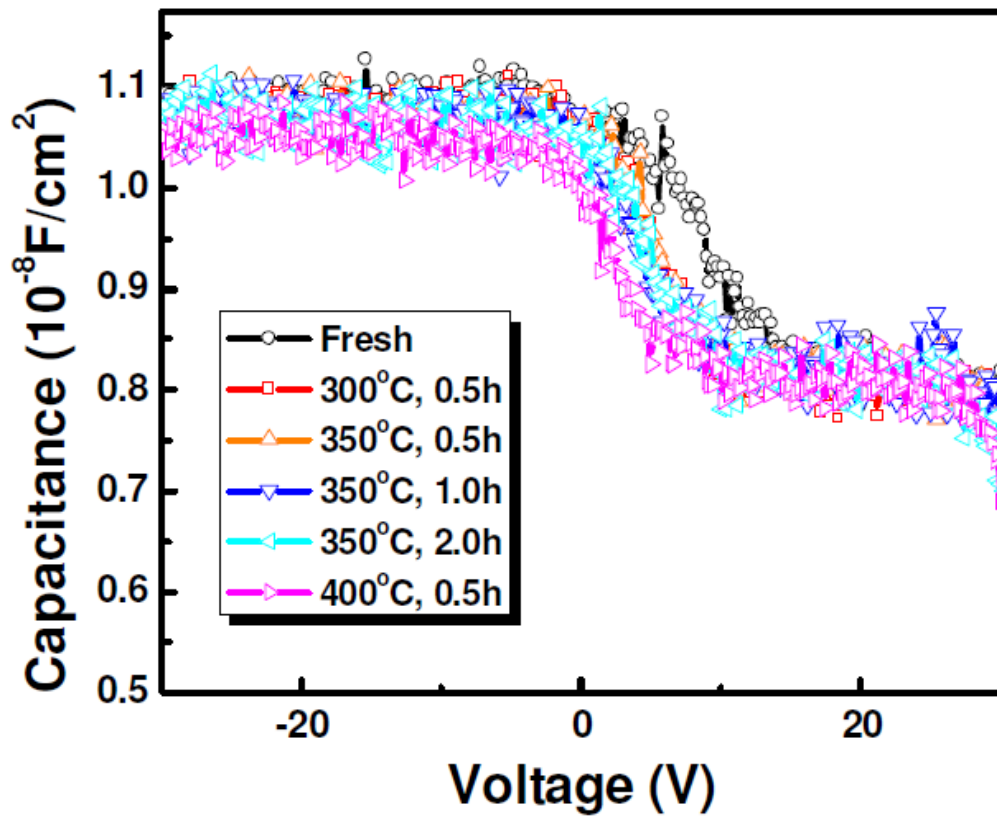
Figure 4.7:  $C$ - $V$  measurements (100 kHz) of TSV structures formed using PETEOS oxide liner and low- $\kappa$  liner. A  $\sim 27.6\%$  reduction in accumulation capacitance is obtained by replacing the PETEOS oxide liner with a low- $\kappa$  liner [4.9, 4.10].

	PETEOS (/cm)	Low-k (/cm)
<b>Liner Capacitance</b> $C_{ox} = \frac{2\pi\epsilon_{ox}}{\ln(r_0/r_1)}$	22.4 pF 22.1 pF (CV)	17.5 pF 15.9 pF (CV)
<b>Si Depletion Radius (<math>r_2</math>)</b> $\frac{qNa}{2\epsilon_s} \left( r_2^2 \ln \frac{r_2}{r_1} - \frac{r_2^2 - r_1^2}{2} \right) = 2\phi_F$	$r_2 - r_1 = 265$ nm	$r_2 - r_1 = 265$ nm
<b>Si Depletion Capacitance</b> $C_{dep} = \frac{2\pi\epsilon_s}{\ln(r_2/r_1)}$	62.4 pF	62.4 pF
<b><math>C_{min}</math></b> $C_{min} = \left( 1/C_{dep} + 1/C_{ox} \right)^{-1}$	17.5 pF 15.6 pF (CV)	13.7 pF 12.1 pF (CV)

**Table 4.1: Comparison between liner and minimum MOS capacitance value (per unit length) based on analytical calculation and  $C$ - $V$  measurement (for  $r_0=2.205 \mu\text{m}$  and  $r_1=2.410 \mu\text{m}$ ). Dielectric thickness is set at 200 nm and the substrate doping,  $N_a$ , is  $10^{16} \text{cm}^{-3}$ .**

It is thus evident that the usage of a low- $\kappa$  material for the liner can significantly reduce the TSV accumulation capacitance. However, due to its inherent porosity, several reliability issues, such as mechanical reliability as well as dielectric reliability, are becoming more important as devices scale down [4.12]. The leakage current is one of the important dielectric reliability issues that must be considered. In the next section, improving the leakage current by annealing will be presented. Therefore, it is important to monitor the possible change in the permittivity value of the low- $\kappa$  liner when annealing is used in order to retain

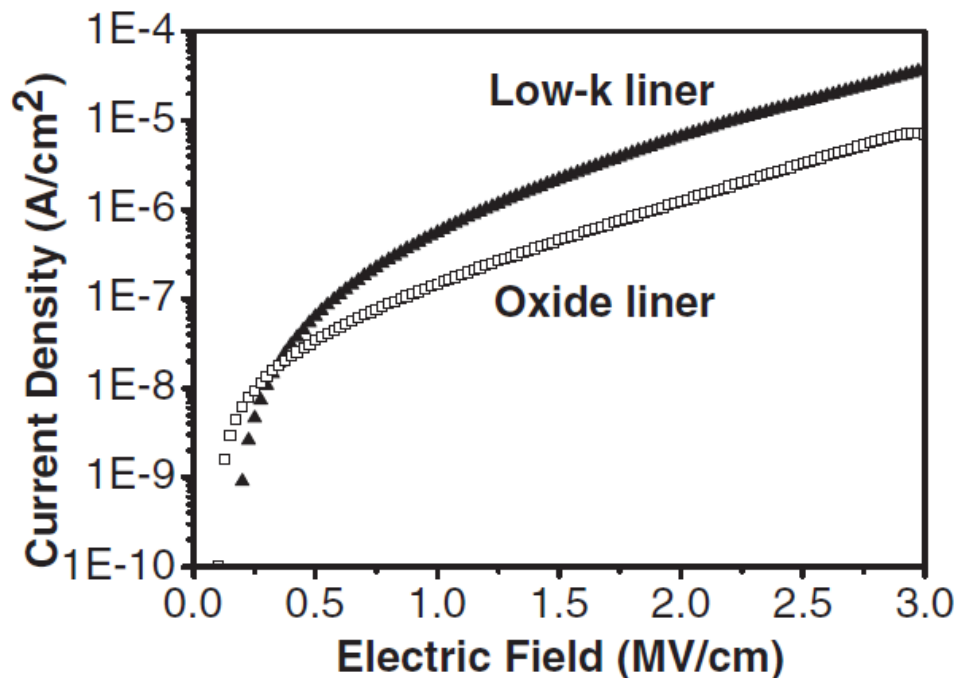
its role in capacitance reduction. However, Figure 4.8 shows that only a small reduction in the effective  $\kappa$  value occurs after various annealing treatments which were applied to control the leakage current. In addition, annealing was also effective in reducing the density of fixed charge as seen from the negative shift in the flat-band voltage to the ideal value of -0.27 V.



**Figure 4.8:** *C-V* characteristics before or after various annealing treatments. The flatband voltage is shifted to the left signifying a reduction in negative fixed charge density. The  $\kappa$  value changes slightly from 2.88 to 2.85 (300°C and 350°C annealing) and then to 2.80 (400°C annealing).

#### 4.4.2 Electrical $I$ - $V$ Measurements

While it is encouraging that the TSV capacitance can be reduced by the incorporation of low- $\kappa$  material as the liner, its implication on the leakage current to the Si substrate needs to be investigated for a complete assessment. Electrical  $I$ - $V$  measurements were performed to monitor the leakage of the TSV dielectric liner. Isolation property of the dielectric liner must be preserved during the TSV operation, and a good dielectric liner should have a leakage as small as possible. Figure 4.9 shows the leakage current density vs. the electric field. The results show that for an electric field up to 3 MV/cm (corresponding to 60 V), there's no abrupt breakdown observed for both PETEOS oxide and low- $\kappa$  liners. This shows that the liner thickness is sufficient to prevent dielectric breakdown for the usual operating voltage below 60 V. However, Figure 4.9 also reveals that the low- $\kappa$  liner obviously suffers from a higher leakage current as compared to the PETEOS oxide liner due to its structural porosity.



**Figure 4.9:**  $I$ - $V$  measurements on TSV structures. The low- $\kappa$  liner is found to exhibit a higher leakage current as compared with the PETEOS oxide liner [4.9, 4.10].

A careful study on the leakage current was then carried out and the result is presented in the cumulative plot in Figure 4.10. From Figure 4.10, it can be seen that a low- $\kappa$  liner suffers from a higher leakage current (at an electric field of 2 MV/cm) as compared with PETEOS oxide liner by as much as  $2.5 \times$  at mid-distribution. It was found that annealing the TSV in forming gas ( $N_2/H_2$ ) at  $350^\circ\text{C}$  for 30 min can improve the leakage current for both the PETEOS oxide and low- $\kappa$  liners. For post annealing, the leakage current at mid-distribution is  $\sim 1.2 \times 10^{-6}$  and  $\sim 6.8 \times 10^{-6}$  A/cm<sup>2</sup> for the PETEOS oxide and the low- $\kappa$  liner, respectively, at an electric field of 2 MV/cm. The leakage current value for the PETEOS oxide liner is comparable with the value of  $1 \times 10^{-6}$  A/cm<sup>2</sup> reported by Archard *et al* [4.8]. A higher leakage current is measured for the low- $\kappa$  liner in comparison with the PETEOS oxide liner due to a higher porosity in the low- $\kappa$  film, but it could be caused by other imperfections, such as the scalloping roughness (as a result of the BOSCH deep DRIE etching) which makes it difficult to deposit a conformal low- $\kappa$  liner on the TSV sidewall. Therefore, for the low- $\kappa$  liner to be effectively used in TSV application, further process optimization is required to further reduce the leakage current. Possible solutions include modified annealing (with higher temperature or longer duration), reducing the TSV's wall scalloping roughness, and the usage of a slightly thicker low- $\kappa$  liner.

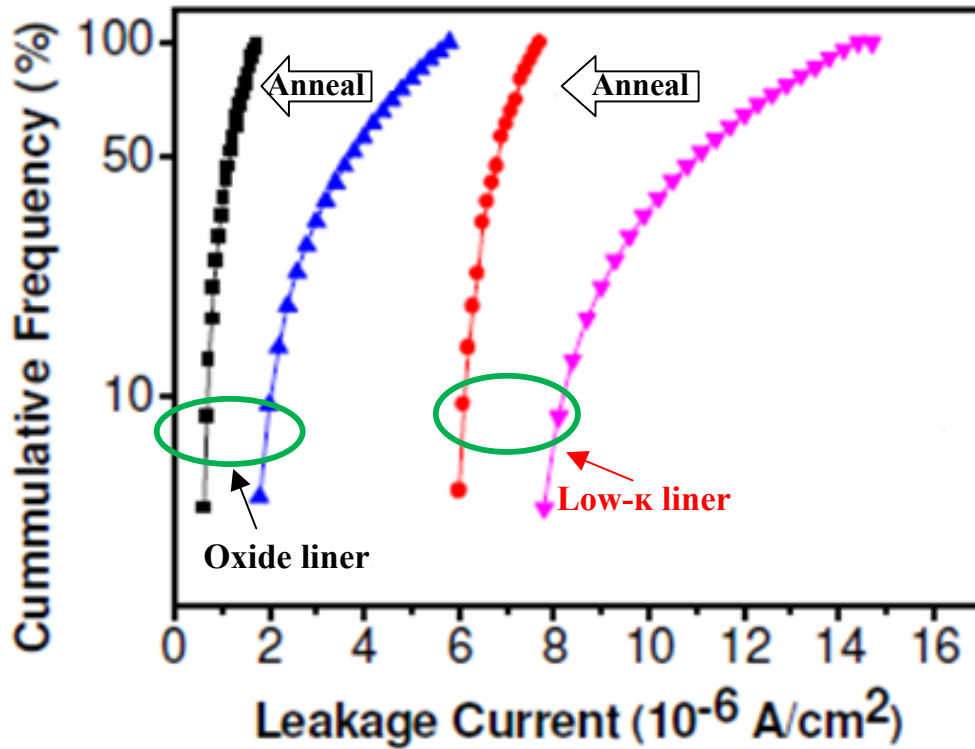


Figure 4.10: Leakage current measurements at an electric field of 2 MV/cm. The low- $\kappa$  liner experiences a much higher leakage than the PETEOS oxide liner. However, for both low- $\kappa$  and PETEOS oxide liners, the leakage current is reduced after annealing at 350°C for 30 min in forming gas [4.9, 4.10].

## 4.5 Al<sub>2</sub>O<sub>3</sub>/Oxide Bi-layer Liner

In the previous section, we have discussed the operation of the TSV in the stable accumulation capacitance region to overcome the spatial TSV performance variations caused by non-uniform hotspot heating. The depletion capacitance is susceptible to thermal-induced variations and our measurements showed it increased with temperature. The impact of the depletion capacitance fluctuation on TSV signal delay is calculated using a predictive technology model (PTM) in Figure 4.11. The TSV signal delay is compared for technology node and  $n$ -MOS width ( $W_n$ ) in Figure 4.12. When the TSV is operated in the depletion region ( $\sim 0$ -5 V), depletion capacitance dependence on temperature results in spatial TSV latency variation and clock skew in H-tree network in the event of non-uniform hotspot heating, which is shown in Figure 4.13. Therefore, TSV with tolerance to spatial variation is desirable and successfully achieved previously by PETEOS oxide liner deposition process tuning. This resulted in the induced negative fixed charge to effectively shift the flatband voltage and the accumulation capacitance is obtained within the operating voltage of interests ( $\sim 0$ -5 V).

In this section, a novel material selection of thin Al<sub>2</sub>O<sub>3</sub> ( $\sim 100$  Å) is successfully integrated and inserted between the Si substrate and the dielectric liner. The flat-band voltage shift is achieved by the negative fixed charge in the thin Al<sub>2</sub>O<sub>3</sub> layer at the  $p$ -Si/liner interface. Al<sub>2</sub>O<sub>3</sub> is known to induce negative fixed charge and routinely used to passivate  $p$ -Si in Si solar cells [4.13, 4.14]. The Al<sub>2</sub>O<sub>3</sub> was deposited using atomic layer deposition (ALD) process at 300°C. The deposition process involves sequential surface reactions of Al(CH<sub>3</sub>)<sub>3</sub> (tri-methylaluminum(TMA)) and H<sub>2</sub>O. An advantage of using ALD in the deposition of Al<sub>2</sub>O<sub>3</sub> is the ability to attain perfect step-coverage on high aspect ratio vias and it has been discussed that ALD has the capability of filling high aspect ratios via till the extent of 40:1

[4.15]. Due to the higher  $\kappa$  value of the  $\text{Al}_2\text{O}_3$ , if we assume a constant total liner thickness, a larger thickness of  $\text{Al}_2\text{O}_3$  will result in an increase of the final TSV capacitance which is undesirable. Therefore, a thin layer of  $\text{Al}_2\text{O}_3$  is preferred. In view of our PETEOS liner thickness of 200 nm, we then decided to adopt an  $\text{Al}_2\text{O}_3$  thickness of 100 Å which is 5% of total dielectric thickness as a start.

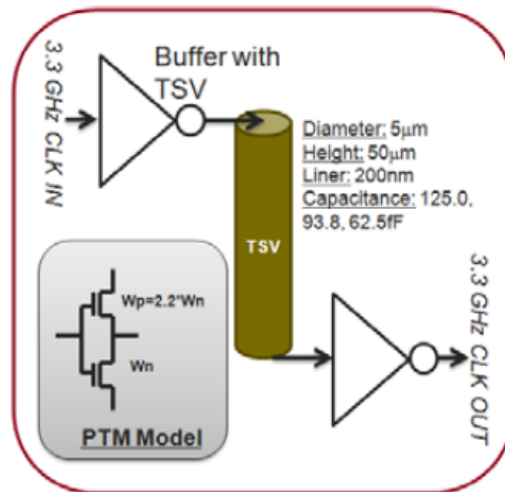


Figure 4.11: TSV signal delay estimation using predictive technology model (PTM) for different capacitance.

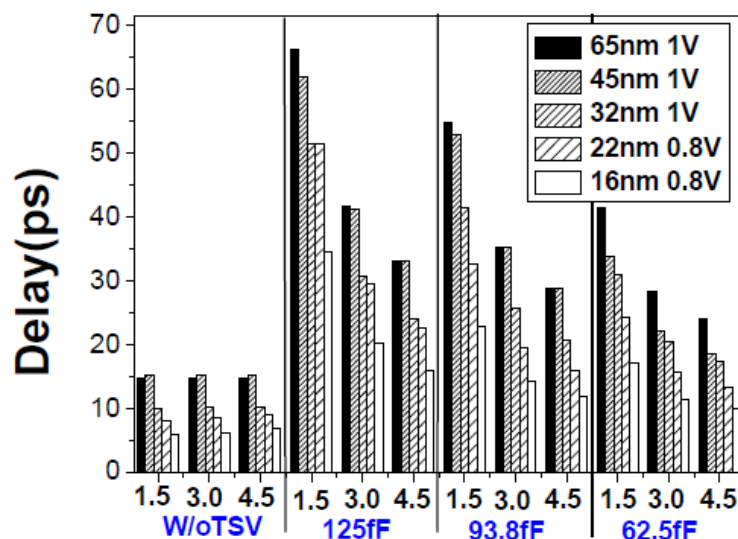
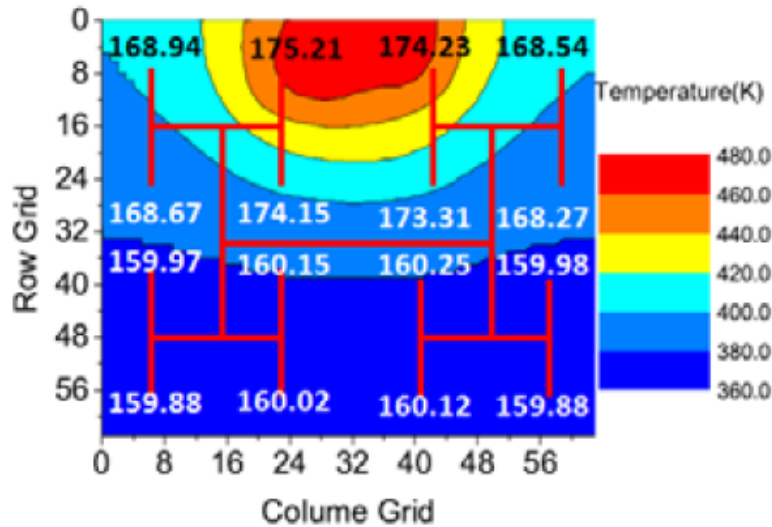


Figure 4.12: Comparison of TSV signal delay for different technology nodes,  $n$ -MOSFET widths ( $W_n$  in  $\mu\text{m}$ ) and TSV capacitances (fF).



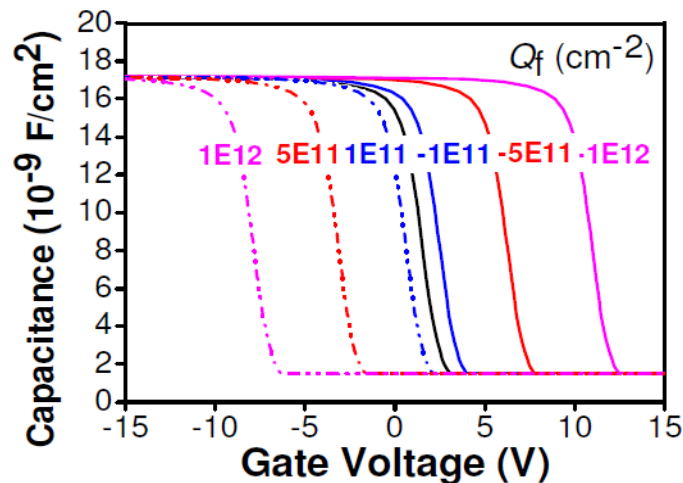
**Figure 4.13: H-tree clock skew (ps) due to non-uniform hotspot heating and the corresponding spatial variation in TSV capacitance.**

#### 4.5.1 Electrical C-V Measurements

The simulated  $C$ - $V$  characteristics of MOS structures at high frequency on  $p$ -Si are shown in Figure 4.14. In principle, the presence of a negative fixed charge ( $Q_f$ ) within the insulator results in a positive flat-band voltage  $V_{FB}$  shift. We can take advantage of this characteristic to operate the TSV-MOS in the accumulation region within the operating voltage of interests ( $\sim 0$ -5 V). This is achieved experimentally by inserting a thin layer of  $\text{Al}_2\text{O}_3$  between the Si substrate and the PETEOS oxide liner. A positive shift in  $V_{FB}$  is obtained as shown in Figure 4.15-4.17 under various annealing conditions which can be applied to control and improve the leakage current. A smaller accumulation capacitance ( $C_{ox}$ ) was measured for an  $\text{Al}_2\text{O}_3$ /PETEOS oxide bi-layer liner due to a larger effective liner thickness, such as 16.1 vs. 17.0 nF/cm<sup>2</sup> with  $\text{N}_2/\text{H}_2$  annealing in Figure 4.16.

Without the presence of the oxide fixed charge,  $V_{FB}$  is just the difference in the work functions between the gate and Si and is approximately -0.27 V. It can be shown that the fixed charge ( $Q_f$ ) in the liner can effectively shift the  $V_{FB}$  as predicted by equation (3)

discussed in the previous section. The effects of annealing in forming gas  $N_2/H_2$  and inert gas  $N_2$  on both the PETEOS oxide liner and  $Al_2O_3$ /PETEOS oxide bi-layer liner are presented in Figure 4.18 and 4.19. The PETEOS oxide liner contains a large number of positive fixed charges. The charge density is on the order of  $\sim 9.70 \times 10^{11} \text{ cm}^{-2}$  based on the calculations shown in the previous section. This results in a negative shift in  $V_{FB}$  ( $V_{FB} = -9.60 \text{ V}$  for the sample annealed in  $N_2/H_2$ ). Therefore, TSV is operated in the depletion region and is unstable within the operating voltage range of interests ( $\sim 0\text{-}5 \text{ V}$ ). With the insertion of  $Al_2O_3$  layer, a large amount of negative fixed charge is induced. The charge density calculated is on the order of  $\sim -7.44 \times 10^{11} \text{ cm}^{-2}$ , which causes a positive shift in  $V_{FB}$  ( $V_{FB} = 7.10\text{V}$  for the sample annealed in  $N_2/H_2$ ). As a result, the TSV is in the stable accumulation region when operated between  $\sim 0\text{-}5 \text{ V}$  and its capacitance in this region does not fluctuate with temperature. Figure 4.20 summarizes the  $C\text{-}V$  characteristics of TSV structures with PETEOS oxide liner and  $Al_2O_3$ /PETEOS oxide bi-layer liner after annealing in forming gas ( $N_2/H_2$ ) and inert  $N_2$  gas at  $300^\circ\text{C}$  for 30 min at 100 kHz.



**Figure 4.14:** The effects of fixed charges in shifting the flatband voltage of MOS structure, as resulted from simulations. (Dielectric thickness is 200 nm and the substrate doping,  $N_a$ , is  $10^{16} \text{ cm}^{-3}$ ) [4.7].

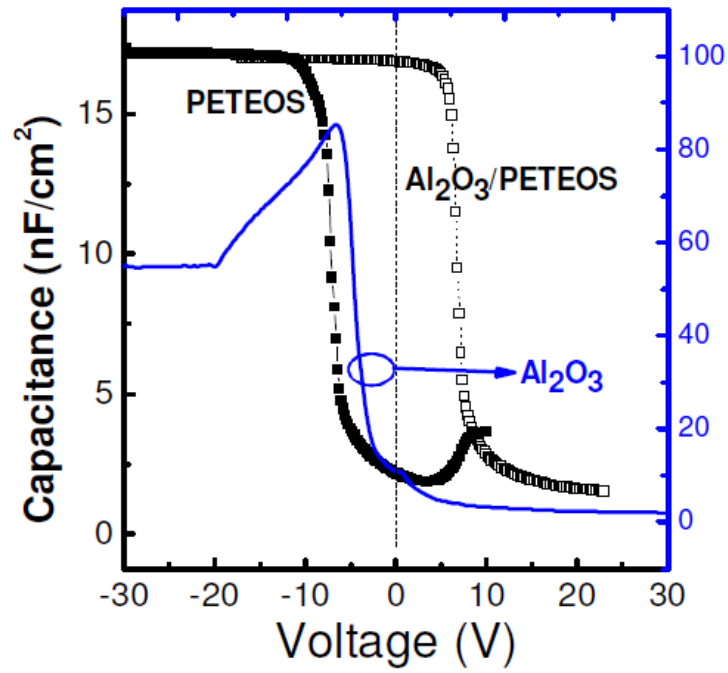


Figure 4.15:  $C$ - $V$  characteristics of the TSV-MOS before annealing [4.7].

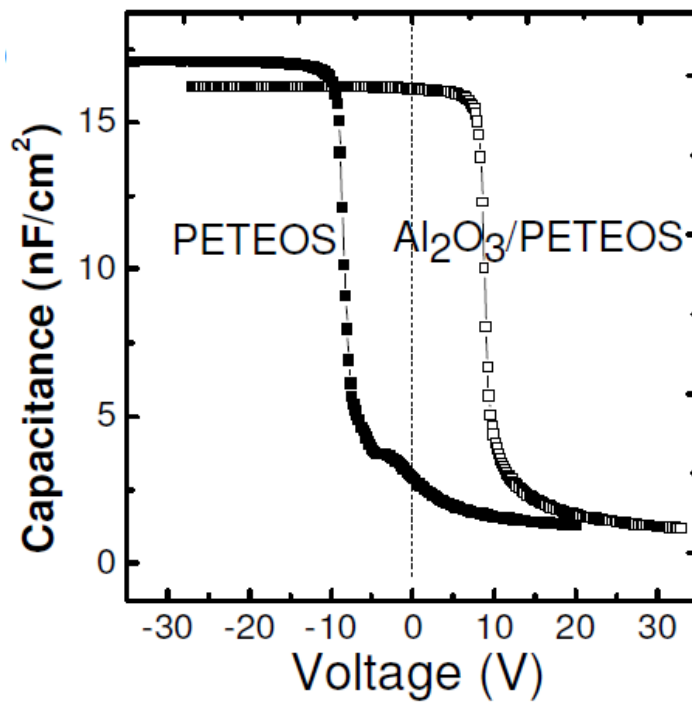


Figure 4.16:  $C$ - $V$  characteristics of the TSV-MOS after annealing in forming gas ( $N_2/H_2$ ) at 300°C for 30 min [4.7].

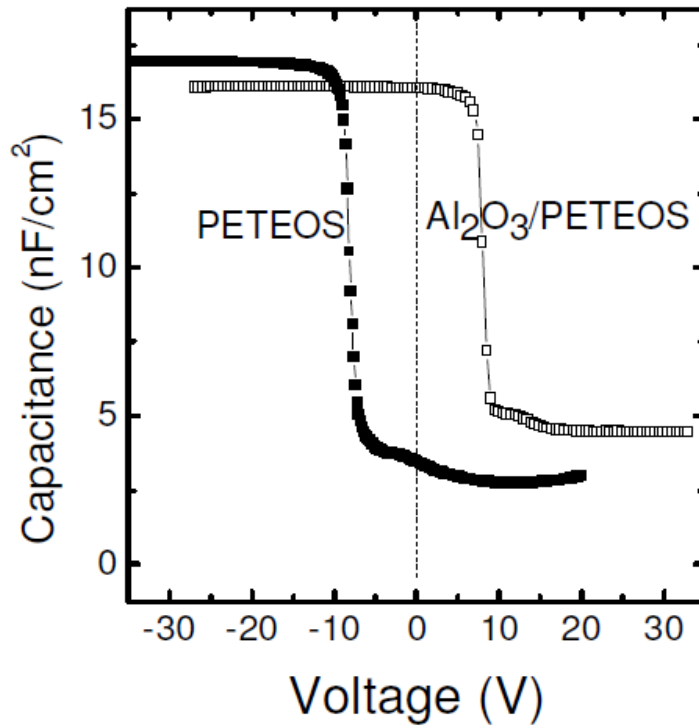


Figure 4.17:  $C$ - $V$  characteristics of the TSV-MOS after annealing in inert  $N_2$  at  $300^\circ\text{C}$  for 30 min [4.7].

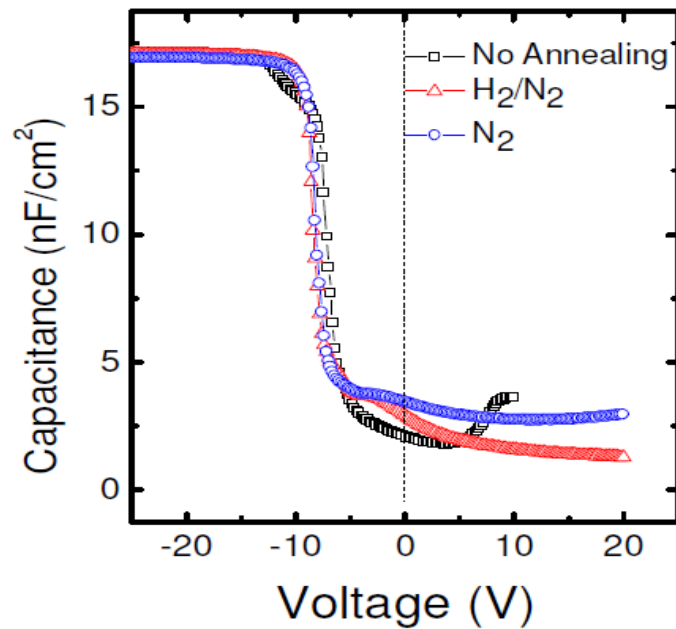


Figure 4.18: Summary of  $C$ - $V$  characteristics of the PETEOS oxide liner after annealing in various ambients. The fixed charge density  $Q_f$  is  $\sim 9.7 \times 10^{11} \text{ cm}^{-2}$  and the flatband voltage  $V_{FB}$  is  $-9.6 \text{ V}$  (after annealing in  $N_2/H_2$ ) [4.7].

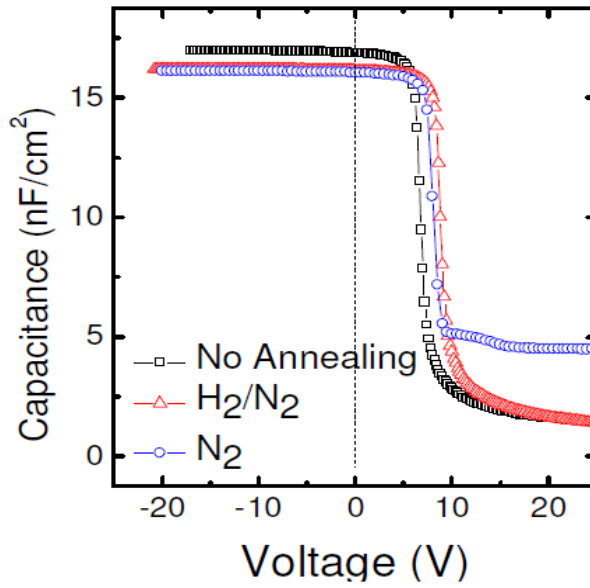


Figure 4.19: Summary of  $C$ - $V$  characteristics of the  $\text{Al}_2\text{O}_3/\text{PETEOS}$  oxide bi-layer liner after annealing in various ambients. The fixed charge density  $Q_f$  is  $\sim -7.44 \times 10^{11} \text{ cm}^{-2}$  and the flatband voltage  $V_{FB}$  is 7.1 V (after annealing in  $\text{N}_2/\text{H}_2$ ) [4.7].

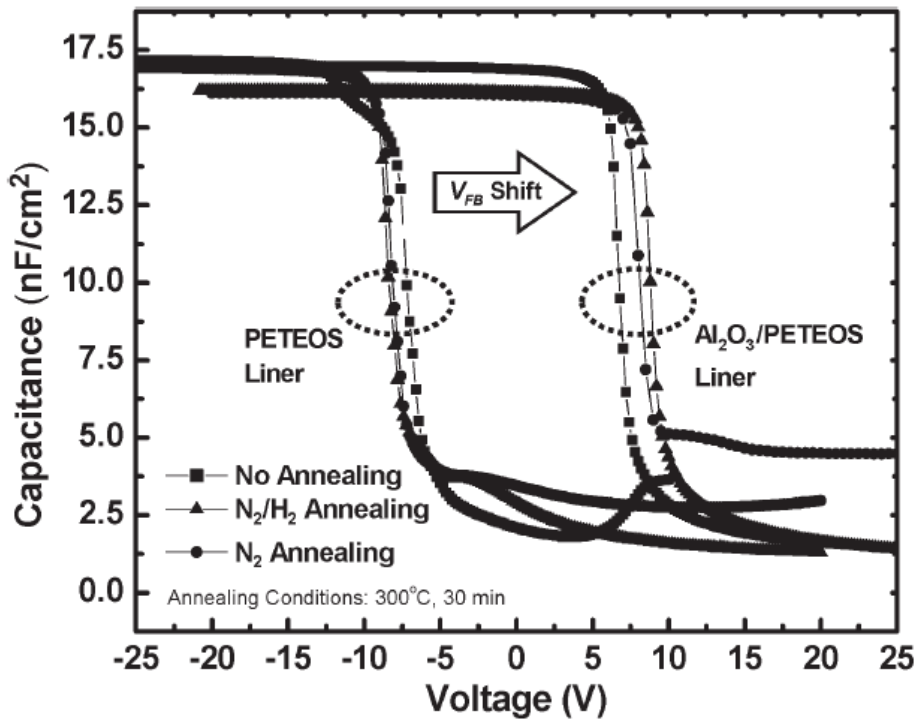
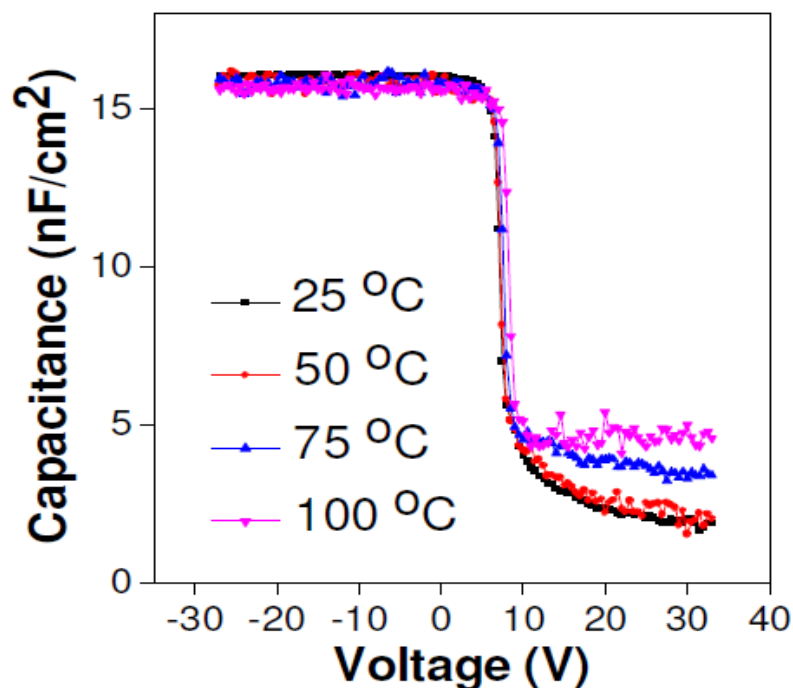


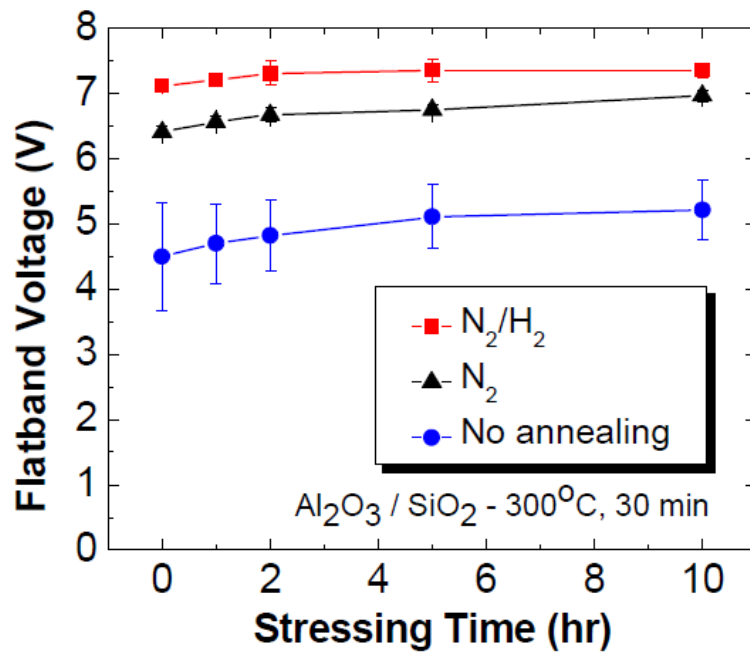
Figure 4.20: Summary of  $C$ - $V$  characteristics of TSV structures with  $\text{Al}_2\text{O}_3/\text{PETEOS}$  oxide bi-layer liner and only PETEOS oxide liner after annealing in inert  $\text{N}_2$  gas or forming gas ( $\text{N}_2/\text{H}_2$ ) at  $300^\circ\text{C}$  for 30 min [4.16].

As demonstrated in Figure 4.21 for Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer liner after the forming gas annealing, the  $C_{ox}$  value is stable when the measurement temperature is changed between 25 to 100°C. However, the depletion capacitance increases with temperature. The accumulation capacitance is estimated to be ~25.3 fF, and is higher than the depletion capacitance of ~6.5 fF. However, this value is still below the requirement of < 100 fF proposed in [4.17]. Even with an increased TSV depth up to 25 μm, as reported [4.18] with an aspect ratio of ~1:5, the estimated accumulation capacitance of ~63.3 fF is still well within the requirement.

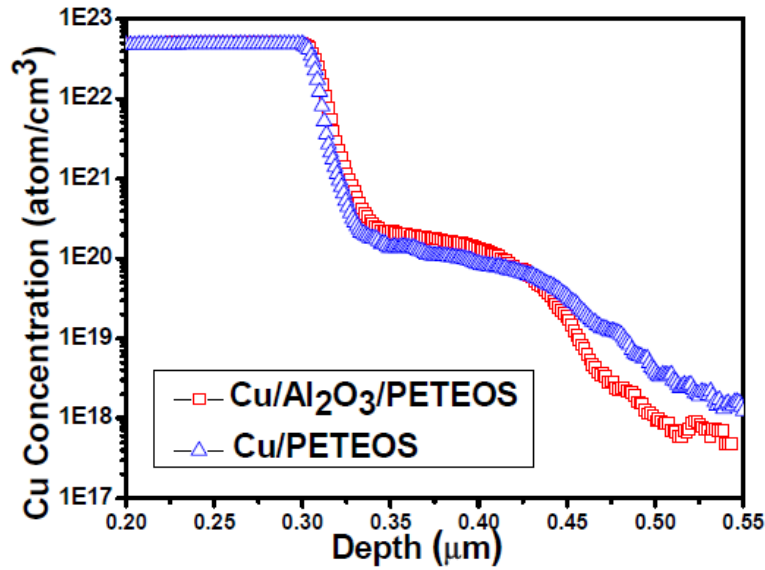


**Figure 4.21: Stable accumulation capacitance within the range of interest for the operating voltage (~0-5 V) is achieved with the Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer liner. Depletion capacitance does not provide similar performance as it increases with temperature [4.7].**

The stability of the negative fixed charge density is important since the positive shift in  $V_{FB}$  is achieved by the  $Al_2O_3$ -induced negative fixed charge. Figure 4.22 shows the stability of the negative fixed charge as seen from the  $V_{FB}$  change. After an accumulated constant biasing (2 MV/cm) for 10 hours, it was observed that the negative fixed charge density increases initially and plateau after  $\sim 5$  hours. This confirms that the stable accumulation capacitance is maintained within the range of interest for the operating voltage ( $\sim 0-5$  V). In addition,  $Al_2O_3$  can effectively act as an extra barrier against Cu diffusion in TSV, as confirmed with secondary ions mass spectroscopy (SIMS) analysis on blanket wafers in Figure 4.23.



**Figure 4.22:  $Al_2O_3$ -induced negative fixed charge density increases initially and becomes stable after  $\sim 5$  hours of accumulated biasing at 2 MV/cm [4.7, 4.16].**

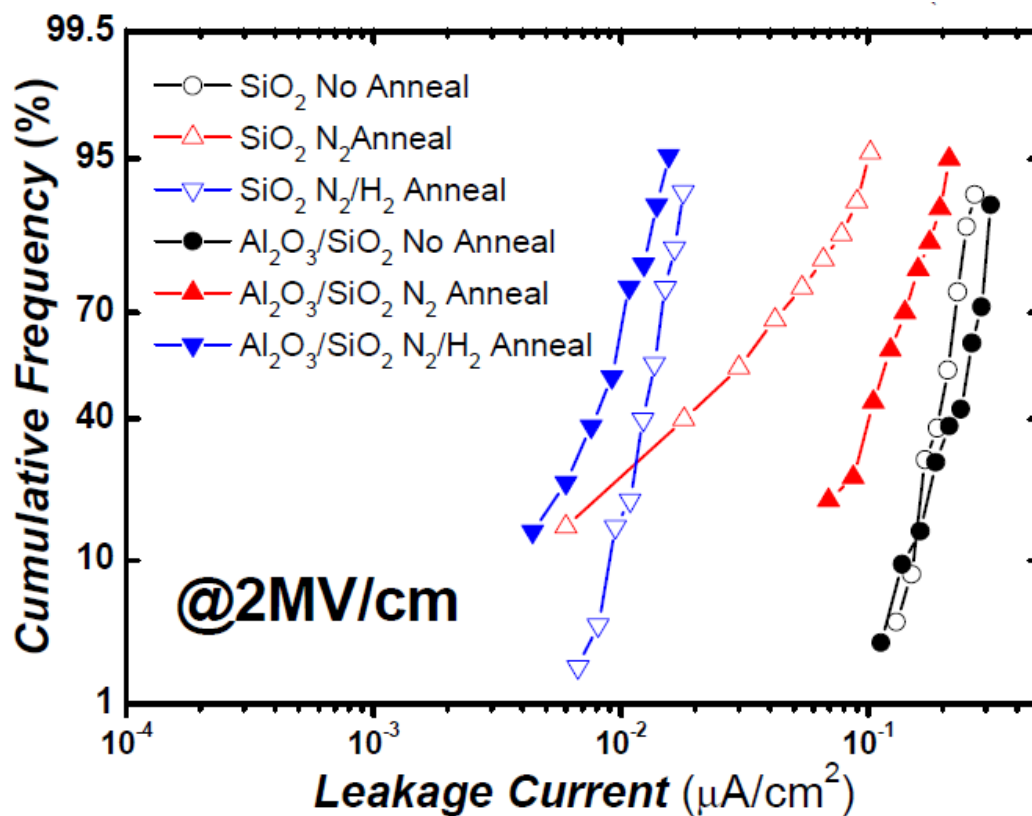


**Figure 4.23:** SIMS analysis shows that Al<sub>2</sub>O<sub>3</sub> (100 Å) is effective in suppressing Cu diffusion [4.7].

#### 4.5.2 Electrical *I-V* Measurements

Another important electrical property of the dielectric liner is the leakage current from the Cu core through the liner to the Si substrate. *I-V* measurements were performed to evaluate the leakage performance of the liner. Figure 4.24 shows the leakage current density of the Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer liner and PETEOS oxide liner after annealing in inert N<sub>2</sub> gas or forming gas (N<sub>2</sub>/H<sub>2</sub>) at 300°C for 30 min under an electric field of 2 MV/cm. The result shows that annealing at 300°C for 30 min can significantly improve the leakage current, and it can be noted that annealing in forming gas (N<sub>2</sub>/H<sub>2</sub>) provides the largest improvement, due to the reduction of defect states of the Si-dielectric interface by hydrogen. Owing to the small atomic size of the hydrogen, it can effectively diffuse into the Si-dielectric interface and complete the Si dangling bonds. In contrast, N<sub>2</sub> molecules have much larger atomic size, and therefore are not able to diffuse and to link to dangling bonds as effectively as the H<sub>2</sub> used in

the forming gas. Hence, the use of forming gas during annealing provides the best improvement of the leakage current. By post-annealing in forming gas, at mid-distribution, the leakage current density of the Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer liner is on the order of 10<sup>-8</sup> A/cm<sup>2</sup>; i.e. a reduction of ~ 10× as compared to the leakage current of the unannealed samples. It is worth pointing out that this leakage current density level is suitable for actual TSV applications [4.8].



**Figure 4.24:** Leakage current measurement results of Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer liner and only PETEOS oxide liner. Leakage current density is improved by ~10× after annealing in forming gas (N<sub>2</sub>/H<sub>2</sub>) at 300°C for 30 min [4.7, 4.16].

## 4.6 Al<sub>2</sub>O<sub>3</sub>/Low-κ Bi-layer Liner

In the previous section, it was shown how the integration of a low-κ material as the TSV dielectric liner has successfully reduced the accumulation capacitance. Moreover, the insertion of a thin Al<sub>2</sub>O<sub>3</sub> layer between the Si substrate and the PETEOS oxide liner successfully shifted the flat-band voltage of the TSV MOS capacitor so that temperature independent accumulation capacitance is obtained within the range of interest for the operating voltage (~0-5 V). In this section, we demonstrate the novel integration of a thin Al<sub>2</sub>O<sub>3</sub> layer with a low-κ bi-layer liner which allows us to achieve both smaller and stable capacitance at the same time.

### 4.6.1 Electrical C-V Measurements

The measured C-V curves at 100 kHz on TSV structures with PETEOS oxide liner, low-κ liner and Al<sub>2</sub>O<sub>3</sub>/low-κ bi-layer liner after annealing in forming gas (N<sub>2</sub>/H<sub>2</sub>) at 350°C for 30 min are shown in the Figure 4.25. The C-V curves show very clear accumulation and depletion regions which depend on the voltage applied on the Cu. It is shown that by replacing the PETEOS oxide liner with the low-κ liner which has an estimated dielectric constant of ~2.8, the accumulation capacitance is reduced by ~26%. This was discussed and verified in the previous section and this improvement further guarantees that the requirements listed in [4.17] and [4.18] can be fulfilled.

As discussed in the previous section,  $V_{FB}$  is the difference in the work functions between Si substrate and the Cu core without the presence of fixed charge and it is estimated to be -0.268 V, and the presence of a fixed charge can effectively shift the  $V_{FB}$ . Due to the insertion of a ~100 Å thin Al<sub>2</sub>O<sub>3</sub> layer between Si and the low-κ liner, a large amount of

negative fixed charge is induced, with a charge density on the order of  $\sim -1.3 \times 10^{12} \text{ cm}^{-2}$ . The negative fixed charge causes a positive shift in  $V_{FB}$  ( $\Delta V_{FB} = +19\text{V}$ ). As a result, the TSV is operated in the stable accumulation capacitance region within the voltage range of interest ( $\sim 0\text{-}5 \text{ V}$ ) to overcome the spatial performance variation caused by non-uniform hotspot heating. Figure 4.26 further shows that the accumulation capacitance does not fluctuate with the substrate temperature while depletion capacitance rapidly increases with the temperature.

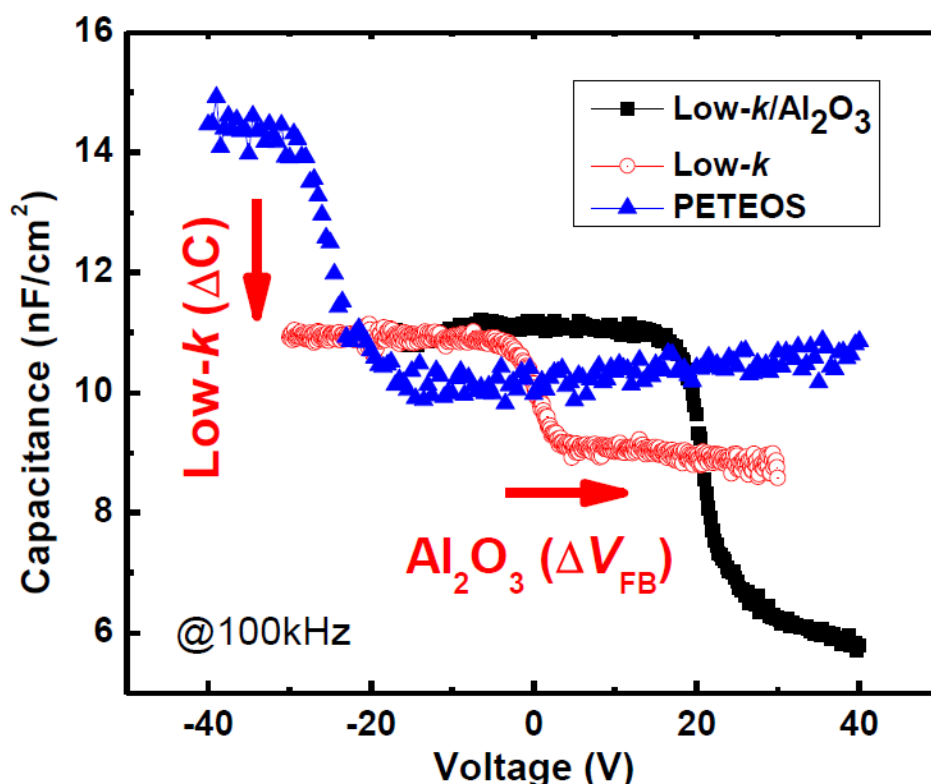
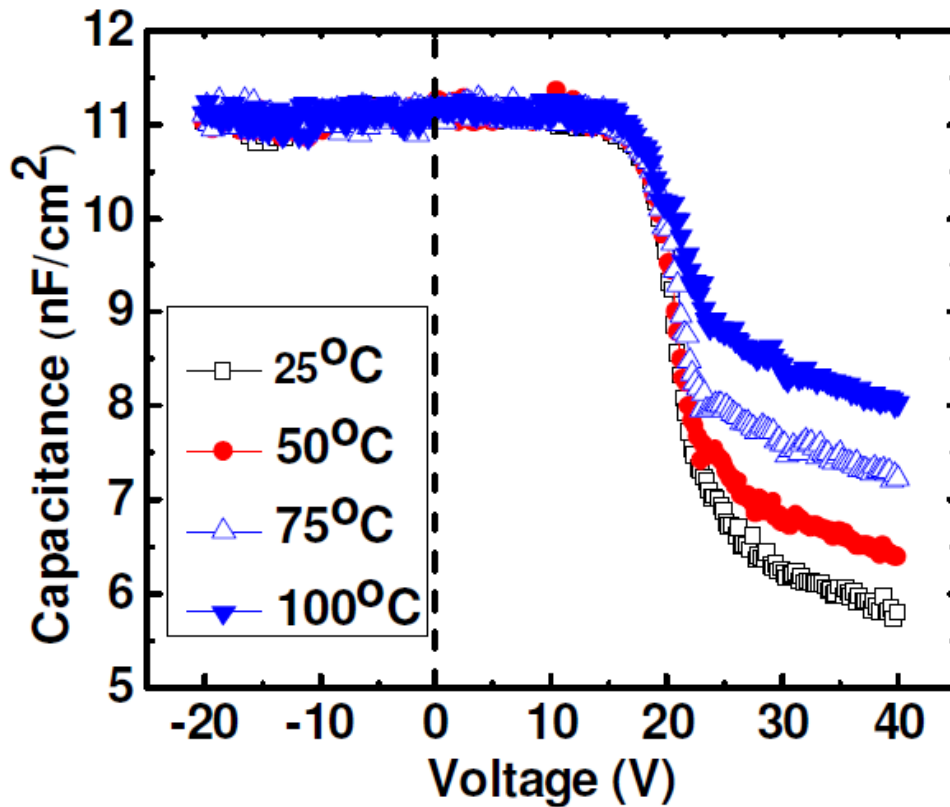


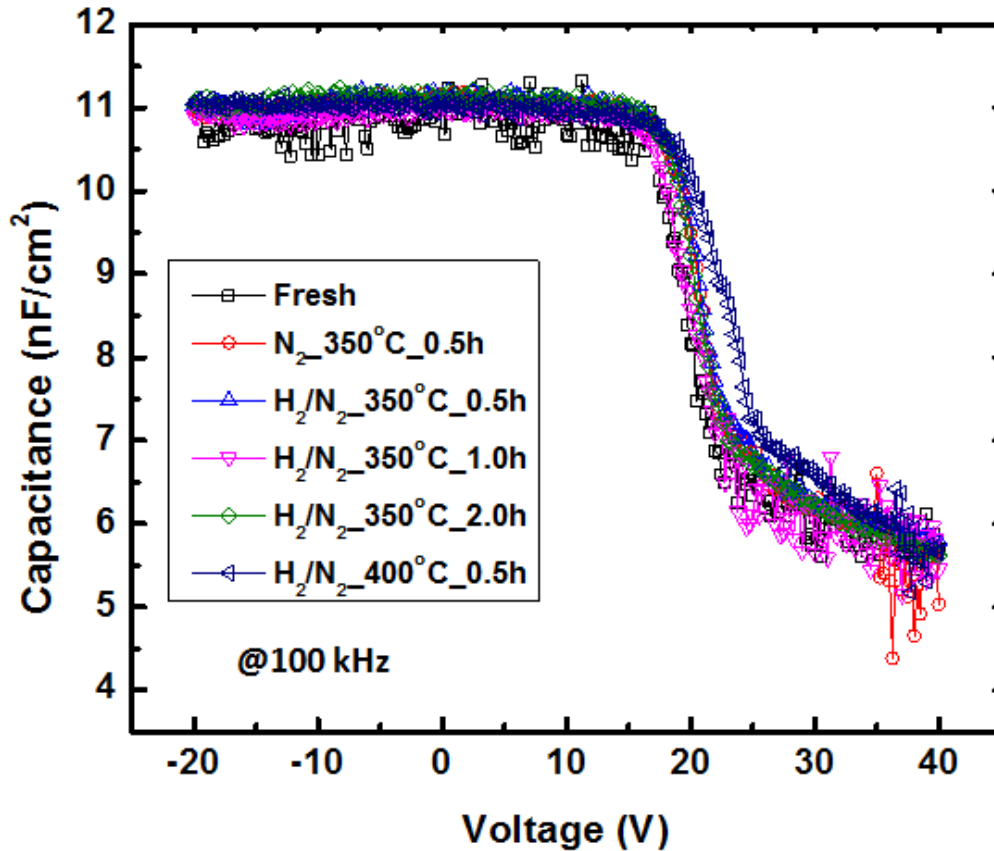
Figure 4.25:  $C$ - $V$  characteristics of TSV structures with different liners after annealing in forming gas ( $\text{N}_2/\text{H}_2$ ) at  $350^\circ\text{C}$  for 30 min. It shows the transformation from PETEOS oxide to low- $\kappa$  (capacitance reduction) and to  $\text{Al}_2\text{O}_3$ /low- $\kappa$  bi-layer liner (stable capacitance) such that the TSV is operated, within the operating voltage range of interest ( $\sim 0\text{-}5 \text{ V}$ ), at lower and stable accumulation region hence immune to substrate temperature.



**Figure 4.26: Stable accumulation capacitance within operating voltage range of interest (~0-5 V) is achieved with the Al<sub>2</sub>O<sub>3</sub>/low-κ bi-layer liner. Depletion capacitance increases with temperature. Sample has been annealed in forming gas (N<sub>2</sub>/H<sub>2</sub>) at 350°C for 30 min.**

Since the reduction in the accumulation capacitance is achieved with a smaller dielectric constant of the low-κ material and various annealing treatments were carried out for leakage current control and improvement, the stability of the dielectric constant after annealing has to be examined. Figure 4.27 shows the  $C-V$  measurement of TSVs with Al<sub>2</sub>O<sub>3</sub>/low-κ bi-layer liner after annealing at various conditions. It shows that there is a slight positive shift in the flatband voltage and the accumulation capacitance remains unchanged which indicates the dielectric constant  $\kappa$  value remains constant. Once again, the stability of Al<sub>2</sub>O<sub>3</sub>-induced negative fixed charge is also studied under prolonged biasing with a high electric field of 2 MV/cm. The negative fixed charge density is again found to increase

initially and plateau after  $\sim 5$  hours of accumulated biasing time as seen from the  $V_{FB}$  change in Figure 4.28. This confirms that sufficient negative fixed charge is maintained even under electric biasing of the TSV.



**Figure 4.27:  $C$ - $V$  characteristics of TSVs with  $\text{Al}_2\text{O}_3/\text{low-}\kappa$  bi-layer liner after annealing at various conditions. It confirms that the dielectric constant  $\kappa$  value of low- $\kappa$  dielectric remains unchanged after annealing.**

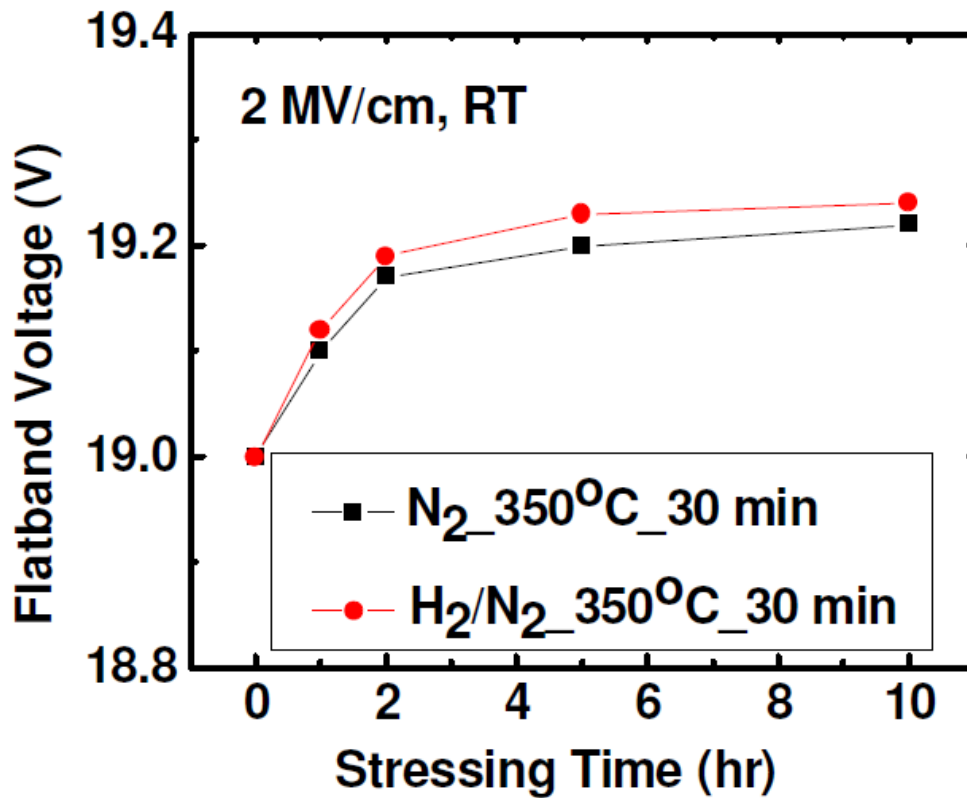
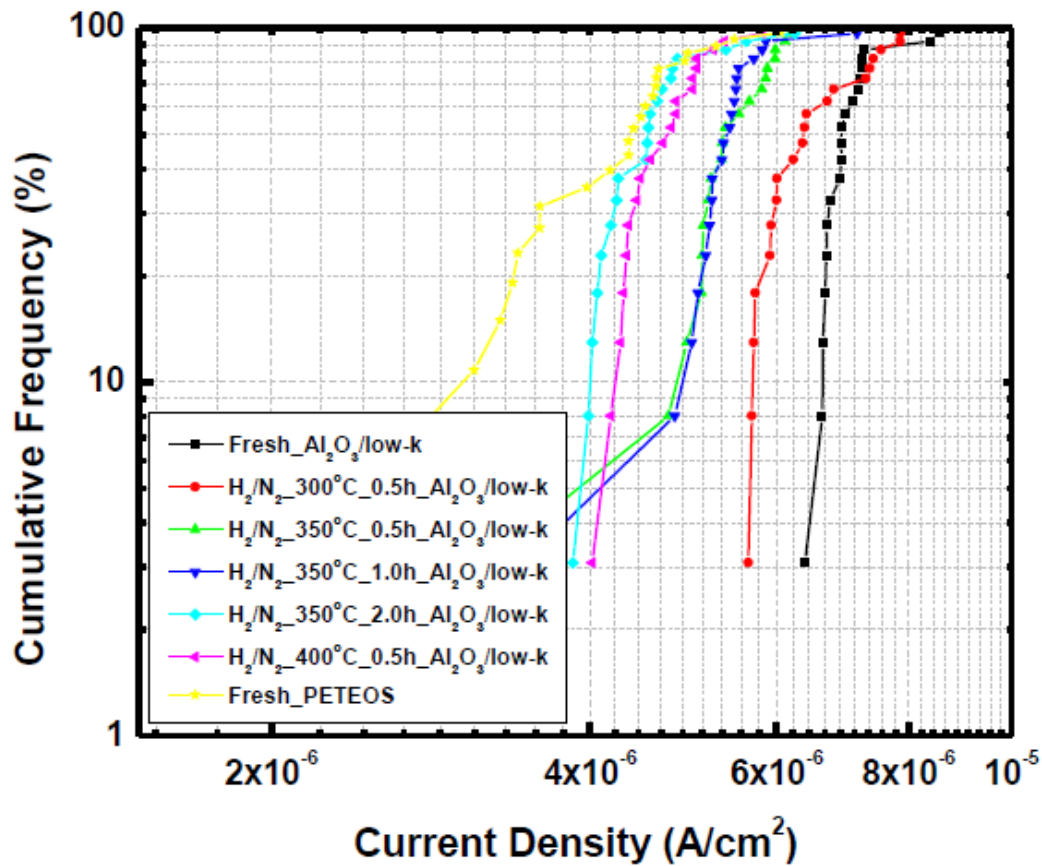


Figure 4.28: The stability of the negative fixed charge under 2 MV/cm biasing. The  $V_{FB}$  increases initially and then stabilizes after 5 hours. The increment and stabilization in  $V_{FB}$  during constant field biasing does not present a concern as the accumulation capacitance remains constant within the operating voltage range of interest ( $\sim 0$ -5 V).

#### 4.6.2 Electrical I-V Measurements

Electrical  $I$ - $V$  measurements were performed as usual to monitor the leakage current of the Al<sub>2</sub>O<sub>3</sub>/low- $\kappa$  bi-layer liner. Figure 4.29 presents the leakage current density of Al<sub>2</sub>O<sub>3</sub>/low- $\kappa$  bi-layer liner at an electric field of 2 MV/cm after annealing at various conditions. The result shows that annealing in forming gas (N<sub>2</sub>/H<sub>2</sub>) at 350°C for 2 hours or at 400°C for 0.5 hours

can significantly improve the leakage current density and effectively reduce it to a level of  $\sim 4 \times 10^{-6} \text{ A/cm}^2$  at mid-distribution comparable to that of the PETEOS oxide liner.



**Figure 4.29: Leakage current measurements of  $\text{Al}_2\text{O}_3/\text{low-}\kappa$  bi-layer liner after annealing. The leakage current density improved to a level comparable with that for the PETEOS oxide liner after annealing in forming gas ( $\text{N}_2/\text{H}_2$ ) at  $350^\circ\text{C}$  for 2 hours or  $400^\circ\text{C}$  for 0.5 hours.**

## 4.7 Summary

This chapter presents the results of electrical characterization using *CV* and *IV* measurements which were performed for various TSV liners, such as PETEOS oxide, low- $\kappa$ , Al<sub>2</sub>O<sub>3</sub>/PETEOS oxide bi-layer, and Al<sub>2</sub>O<sub>3</sub>/low- $\kappa$  bi-layer. The novel material integration of thin Al<sub>2</sub>O<sub>3</sub> with low- $\kappa$  dielectric bi-layer in the TSV structure as the liner has been successfully achieved. The TSV parasitic capacitance was further optimized in terms of capacitance stability and capacitance reduction. A 26% reduction of the accumulation capacitance was achieved due to the smaller dielectric constant  $\kappa$  value of the low- $\kappa$  material. Moreover, at the same time stable accumulation capacitance was maintained within the range of interest for the operating voltage ( $\sim 0-5$  V) by utilizing the negative fixed charge ( $|Q_f| = 1.3 \times 10^{12} \text{ cm}^{-2}$ ) induced in the thin Al<sub>2</sub>O<sub>3</sub> layer between the Si and the low- $\kappa$  layer. Finally, annealing the TSV in forming gas (N<sub>2</sub>/H<sub>2</sub>) can significantly improve the leakage current density of the dielectric liners.

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# Chapter 5: Cu-TSV Thermal Property Study and Stress Mitigation

## 5.1 Introduction

The idea of three-dimensional (3D) integration emerges in order to overcome the two-dimensional (2D) conventional scaling limits and to provide lower signal latency, lower power consumption, smaller form factor, higher bandwidth, higher density and heterogeneous integration [5.1]. 3D integration employs TSV which replaces the conventional interconnectors to provide high density and short vertical interconnection between stacked layers. However, high power density can affect adversely the performance of 3D integrated circuits (ICs), and in such cases thermal management becomes critically important [5.2]. TSV is embedded in the silicon substrate and commonly fabricated by utilizing high aspect ratio silicon deep reactive ion etching (DRIE), lining with dielectric layer and copper super conformal filing, respectively [5.3]. By taking advantage of the excellent thermal conduction properties of silicon, in this work we experimentally demonstrate that the use of TSV arrays in circuits can provide an additional heat conduction path through the Cu core to the silicon substrate; this has the benefits of enhanced heat dissipation which helps in the thermal management of 3D integration.

Although the integration of TSV in Si has great benefits, it also has the drawback of generating significant thermo-mechanical stress levels in the device during operation [5.4]. A Cu-TSV exerts this thermo-mechanical stress onto the surrounding Si in the immediate vicinity of the TSV due to the mismatch in the coefficients of thermal expansion (CTE) of Cu and Si. During the Cu-TSV annealing process and subsequent cooling, a strong compressive

stress developed in the close vicinity of the TSV. It was shown that this stress level decreases exponentially and becomes constant as a function of the radial distance from the TSV edge. Similar observations have also been reported by Trigg *et al* recently [5.5]. The reason for this phenomenon is that the high temperature annealing step initiates grain growth inside the Cu pillar [5.6]. The thermo-mechanical stress leads to detrimental effects such as cracking, delamination and malfunctioning of the individual transistors. Furthermore, it can also result in mobility variation and interconnect distortion [5.7]; the carrier mobility can be varied by more than 7% with every 100 MPa of stress [5.8]. The International Technology Roadmap for Semiconductors (ITRS) has invariably proposed the scaling of TSV diameter to a value as low as 2  $\mu\text{m}$  in the future. Lowering the TSV diameter could minimize the overall thermal stress due to a smaller Cu volume [5.5, 5.9]. However, rigorous scaling of the TSV diameter results in an extremely stringent aspect ratio that is technically challenging for void-free Cu filling during the electroplating process. In the following sections, we will discuss the use of a dielectric material with a lower elastic modulus, such as low- $\kappa$  [5.10] which can act as a compliant layer to cushion the thermo-mechanical stress induced by the TSV.

Some of the results in this chapter have been published in our publications as follows:

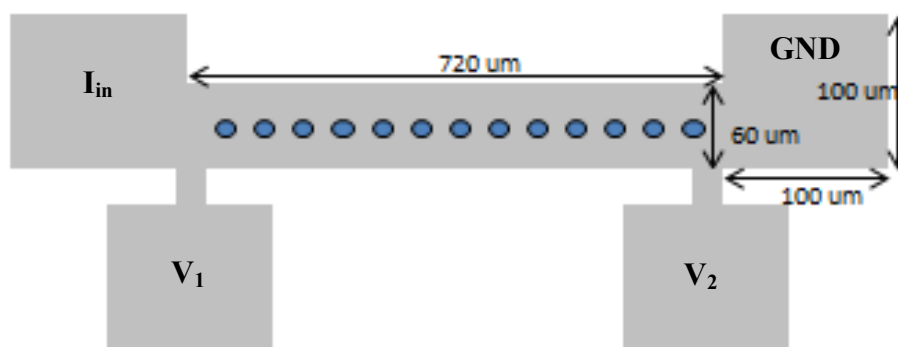
1. K. Ghosh, J. Zhang, **L. Zhang**, Y. Dong, H. Y. Li, C. M. Tan, G. Xia, and C. S. Tan, “Integration of Low-k Dielectric Liner in Through Silicon Via and Thermo-mechanical Stress Relief,” *Applied Physics Express, JSAP*, 5(12), 2012.
2. **L. Zhang**, K. Ghosh, J. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, “TSV Scaling with Constant Liner Thickness and the Related Implications on Thermo-mechanical Stress, Capacitance, and Leakage Current,” *International Conference on Solid State Devices and Materials (SSDM)*, Kyoto, Japan, September 25-27, 2012.
3. **L. Zhang**, K. Ghosh, J. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, “Strategy for TSV Scaling with Consideration on Thermo-mechanical Stress and

Acceptable Delay," *International Microsystems, Packaging, Assembly Circuits Technology Conference (IMPACT)*, Taipei, Taiwan, October 24-26, 2012.

4. **L. Zhang**, H. Y. Li, G. Q. Lo, and C. S. Tan, " Thermal Characterization of TSV Array as Heat Removal Element in 3D IC Stacking," *Electronic Packaging Technology Conference (EPTC)*, Singapore, December 5-7, 2012.
5. **L. Zhang**, H. Y. Li, G. Q. Lo, and C. S. Tan, "Low- $\kappa$  Material as Cu-TSV Dielectric Liner for Stress and Capacitance Control," *International Conference on Materials for Advanced Technologies (ICMAT)*, July, 2013.

## 5.2 Thermal Characterization Results and Discussions

The purpose of this experiment is to demonstrate that TSV arrays can be used as an effective heat removal element, and to show how the density and placement of TSV arrays could affect the heat conduction. The Kelvin structure fabricated for electrical measurements is made of polysilicon 5000 Å thick patterned on top of an oxide layer 2000 Å thick, and it has a length of 720 μm and a width of 60 μm, as shown schematically in Figure 5.1.



**Figure 5.1: Schematic of the Kelvin structure fabricated for electrical measurements. The length is 720 μm and width is 60 μm. Four probe pins are needed for the testing: current is injected to pad “I<sub>in</sub>”, pad “GND” is connected to ground pin, pads “V<sub>1</sub>” and “V<sub>2</sub>” are connected to other two pins to measure the voltage difference across the polysilicon line. The circles represent the vias realized in the substrate, underlying the oxide layer on which the polysilicon Kelvin line is fabricated [5.11].**

In our design, the TSV arrays are placed such that they surround and are beneath the doped polysilicon line. The resistance of the doped polysilicon line is measured in a temperature range of 25 to 200°C by placing the wafers on a heated probe chuck. By applying a test current (1 mA), the resistance can be estimated from:

$$R = (V_1 - V_2) / I \quad (1)$$

where  $R$  is the resistance of the line,  $I$  is the injected current,  $V$  is the voltage. Measurements were performed at steady state to eliminate the inaccuracy, and the test current was chosen to be small enough to avoid unwanted heating that might cause the temperature of the doped poly-line to increase. The relationships between the line resistance and the line temperature for the different TSV placements and densities (in terms of TSV pitches) summarized in Table 5.1, are plotted in Figures 5.2-5.8. It is observed that very good linear fits can be established for the measured data points in all cases.

	<b>TSV Placement</b>	<b>TSV Density (Pitch)</b>
1	No TSV	N. A.
2	1 row of TSV beneath	15 $\mu\text{m}$
3	2 rows of TSV beneath	15 $\mu\text{m}$
4	1 row of TSV beneath and 2 rows of TSV surround	15 $\mu\text{m}$
5	2 rows of TSV beneath and 2 rows of TSV surround	15 $\mu\text{m}$
6	1 row of TSV beneath	10 $\mu\text{m}$
7	1 row of TSV beneath	20 $\mu\text{m}$

**Table 5.1: Summary of the placement and density of the TSV structures used for thermal characterization measurements.**

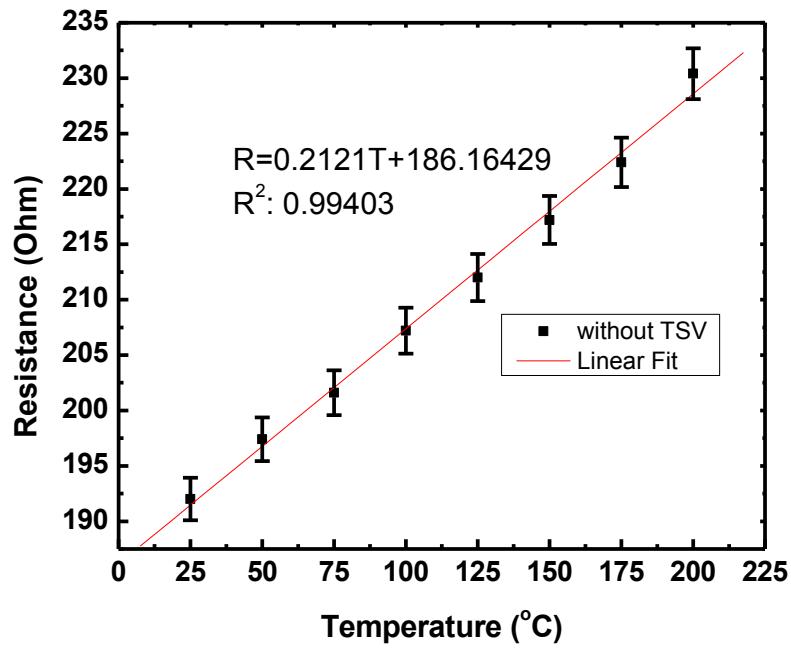


Figure 5.2: Polysilicon line resistance vs. line temperature: structure without TSV [5.11].

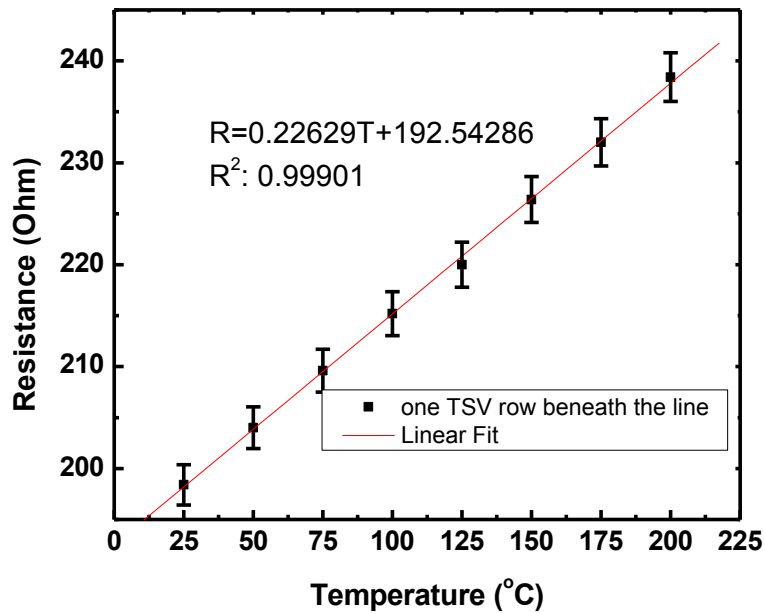


Figure 5.3: Polysilicon line resistance vs. line temperature: structure with one TSV row beneath the line (TSV pitch = 3 times TSV diameter) [5.11].

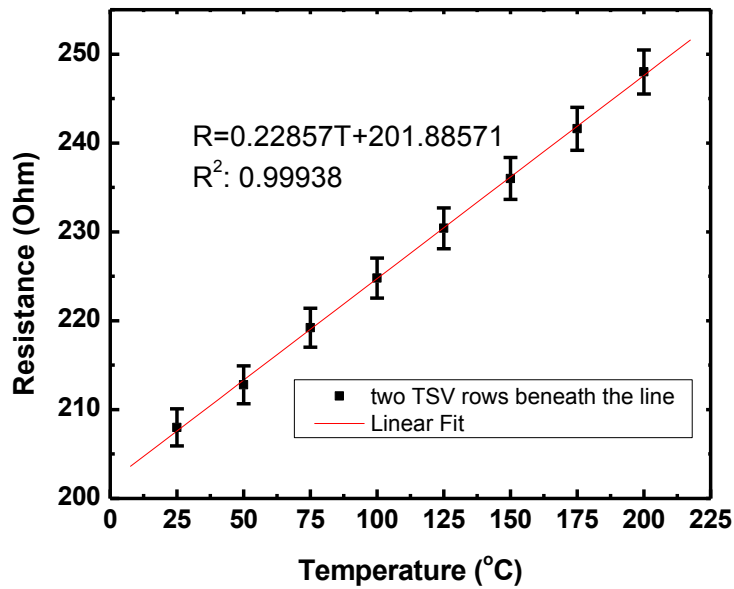


Figure 5.4: Polysilicon line resistance vs. line temperature: structure with two TSV rows beneath the line (TSV pitch = 3 times TSV diameter) [5.11].

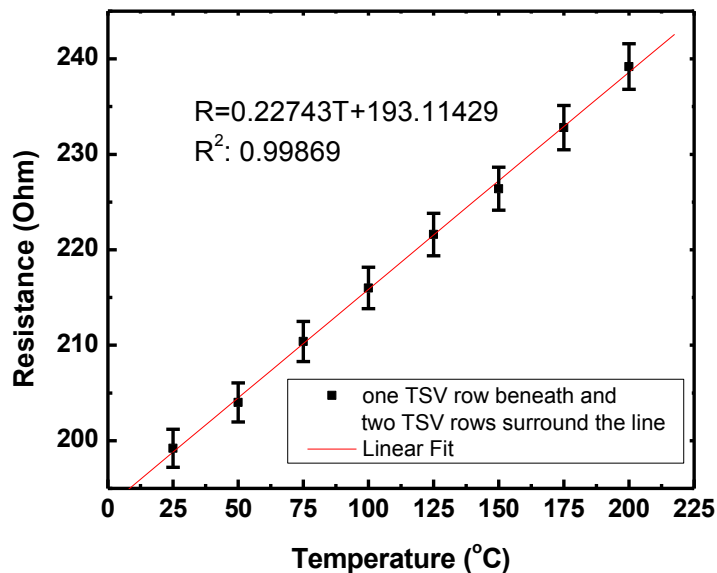


Figure 5.5: Polysilicon line resistance vs. line temperature: structure with one TSV row beneath and two TSV rows surround the line (TSV pitch = 3 times TSV diameter) [5.11].

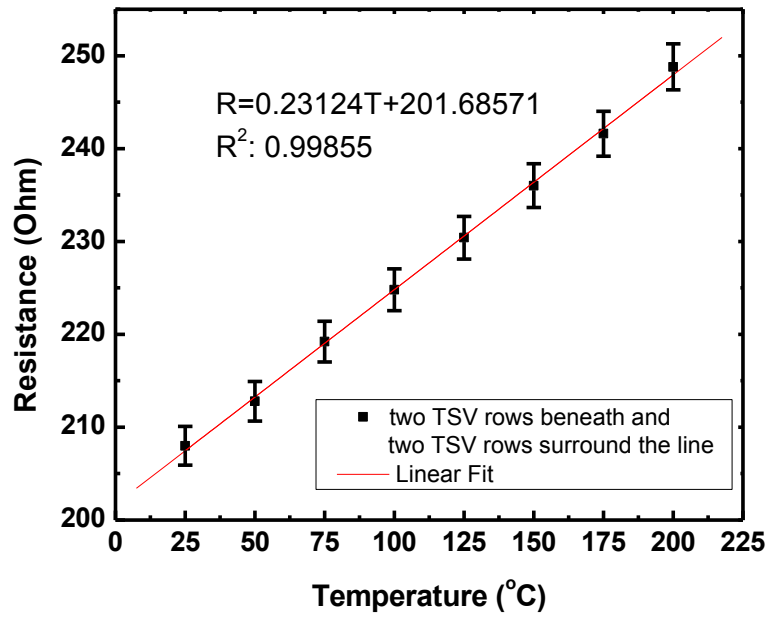


Figure 5.6: Polysilicon line resistance vs. line temperature: structure with two TSV rows beneath and two TSV rows surround the line (TSV pitch = 3 times TSV diameter) [5.11].

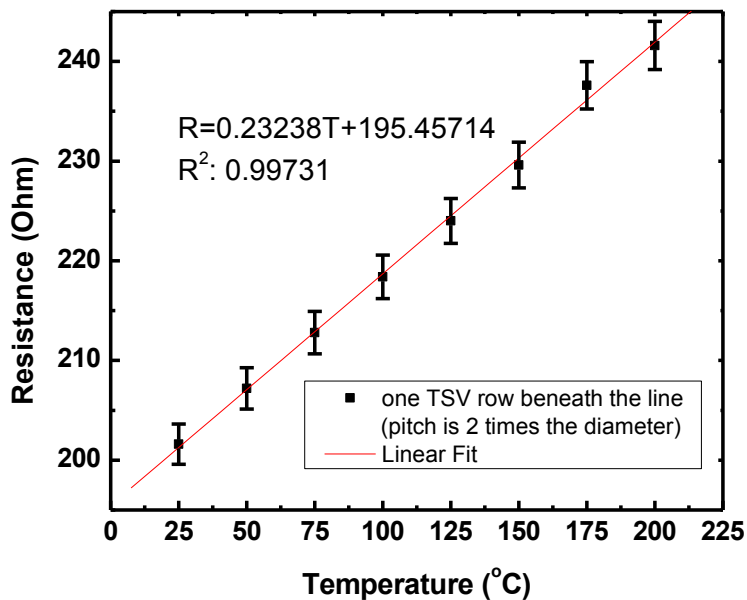
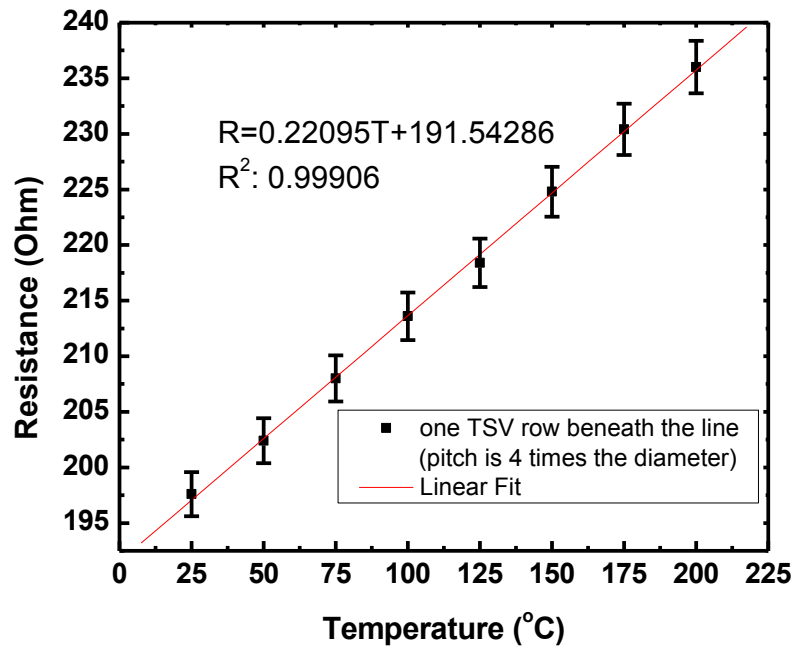


Figure 5.7: Polysilicon line resistance vs. line temperature: structure with one TSV row beneath the line (TSV pitch = 2 times TSV diameter) [5.11].



**Figure 5.8: Polysilicon line resistance vs. line temperature: structure with one TSV row beneath the line (TSV pitch = 4 times TSV diameter) [5.11].**

During the second step of the characterization, the doped polysilicon line temperature was maintained constant at 25°C, while a stressing current ranging from 1 mA to 112.5 mA (corresponding power density ranges from ~0 to  $8 \times 10^7$  W/m<sup>2</sup>) was injected in the polysilicon line. By calibrating the resistance value to the temperature value based on the linear relationships established in Figures 5.2-5.8, it is easy to estimate the doped polysilicon line temperature under various stressing currents. The results in Figure 5.9 show that the temperature of the doped polysilicon line is significantly reduced when there are TSV arrays placed beneath the line. When there is one TSV row and two TSV rows beneath the doped polysilicon line (TSV pitch is 3 times the diameter), we measured a temperature reduction of ~32 °C and ~44 °C respectively at a power density of  $8 \times 10^7$  W/m<sup>2</sup>. It is worth pointing out,

however, that the TSV arrays surrounding the line do not help significantly in the temperature reduction. Figure 5.10 shows the effect of TSV pitch on the temperature reduction. It shows that when the pitch is smaller, the temperature reduction is more significant. This observation is expected given that when the TSV pitch is smaller, the TSV densities will be higher and hence more Cu cores can be used to conduct the heat away through the Cu core to the silicon substrate.

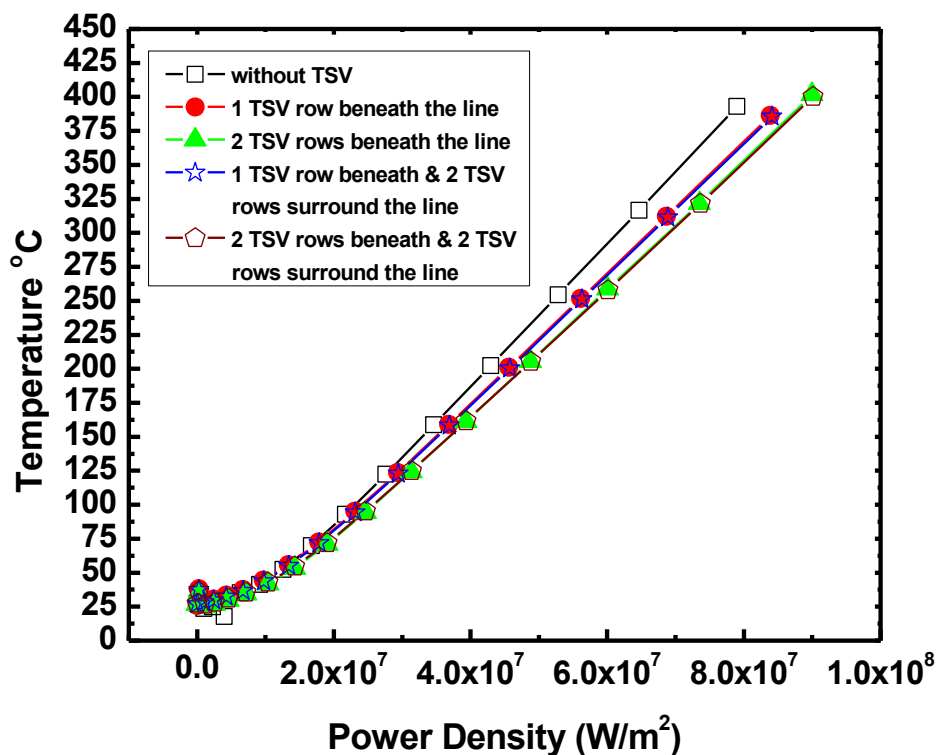


Figure 5.9: Line temperature at different power density. It shows that TSV arrays beneath the line can significantly reduce down the temperature. The temperature reduction as high as  $\sim 44^{\circ}\text{C}$  at a power density of  $8 \times 10^7 \text{ W/m}^2$  can be achieved when there are two TSV rows beneath the doped poly-silicon line (TSV pitch is 3 times the diameter) [5.11].

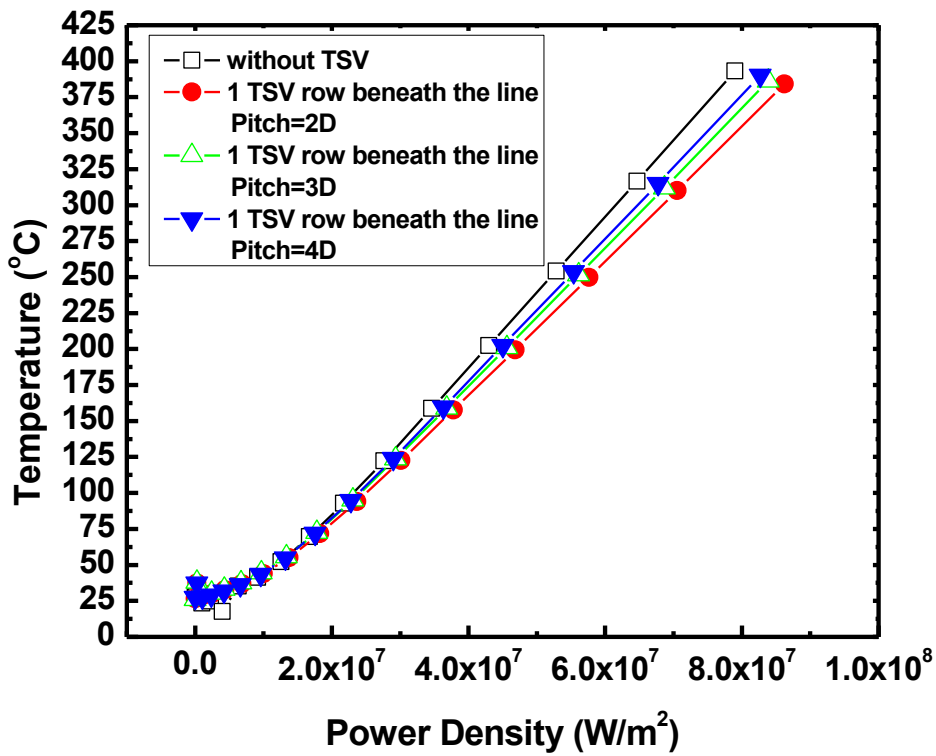


Figure 5.10: Line temperature at different power density. It shows that TSV arrays with smaller pitch have more significant effect on the temperature reduction since the TSV density under the polysilicon is higher [5.11].

### 5.3 Cu-TSV Induced Stress Modeling

A 3D finite element analysis (FEA) model was constructed to determine the thermal stress distribution in the TSV samples, with the material physical properties used summarized in Table 5.2. The model consists of TSV with diameter ranges from 4 to 10  $\mu\text{m}$ , and depth of 10  $\mu\text{m}$  on the Si (100) surface. The conformal 200 nm dielectric liner, Ta diffusion barrier and Cu filling in the TSVs were also taken into account. A thermal load from the reference temperature (200°C, assumed to be stress-free) to room temperature (25°C) of  $\Delta T = 175$  °C was considered. For simplicity, a linear elastic and isotropic model was assumed to obtain a first-order understanding of the phenomenon. As a result of the thermal load during cooling, the Cu core tended to contract at a higher rate than that of Si due to the larger CTE of Cu. Since Cu was confined in the TSV, a thermo-mechanical stress was induced on the surrounding Si. In reality, such near-surface stresses could possibly be estimated via  $\mu$ -Raman analysis using a 442 nm laser line with an approximate penetration depth of 0.16  $\mu\text{m}$  into the Si surface. The stress state in the Si surface was considered to be nearly biaxial at this depth. Thus, the biaxial stress ( $\sigma_r + \sigma_\theta$ ) profile was extracted at a depth of 0.16  $\mu\text{m}$  from the above simulation. The stress profile is presented in the next section.

At the very beginning of this chapter, we have discussed that scaling down the TSV size could improve on the thermo-mechanical stress exerted on the Si substrate due to the smaller volume of the Cu core. Our simulation study FEA on single Cu-TSV which is shown in Figure 5.11 has clearly revealed that the larger the TSV diameter, the larger the compressive stress in the Si substrate in the close vicinity of the TSV row.

Material	Young's modulus (GPa)	Poisson ratio	Density (kg/m <sup>3</sup> )	CTE (ppm/K)
Silicon	170	0.28	2329	2.6
Copper	120	0.34	8960	16.5
Low- $\kappa$	4.2	0.30	1500	12.0
PETEOS	70	0.17	2200	0.5

Table 5.2: Physical properties of materials used in the structure of a TSV [5.12].

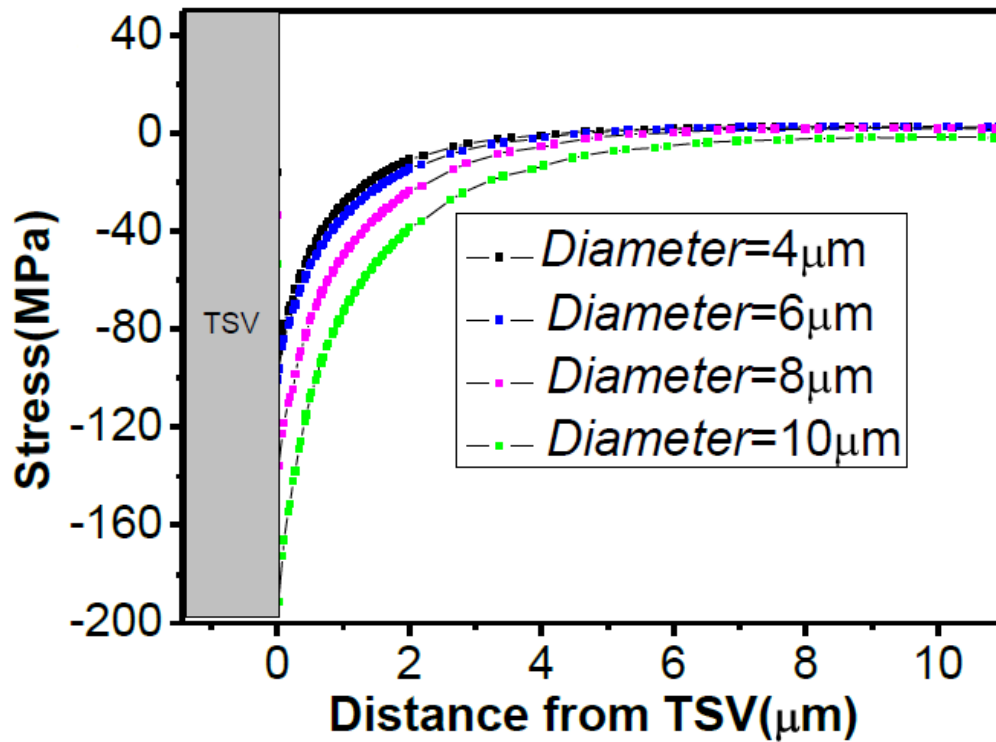


Figure 5.11: FEA simulation curves of the thermo-mechanical stress exerted by a single Cu-TSV on Si substrate as a function of distance from the edge of TSV. Larger TSV has exerted higher compressive stress on the Si substrate [5.13].

Two-dimensional (2D) finite element analyses on Cu and dielectric liner interconnect structures have shown that the triaxial tensile stress in Cu significantly arises due to stiff barrier layers surrounding the Cu line [5.14, 5.15]. This stress is transmitted to the peripheral Si crossing through the liner barrier. Thus, the use of a softer liner with a higher compliance in principle imparts a lower stress on the Si. Simulation on a poly (p-xylylene)-type organo polymeric compound [5.16] (commonly known as parylene, with Young's modulus of  $\sim 4$  GPa) as a liner material in a TSV interconnect shows that it could relieve the thermal stress distribution in Si by 75 MPa. Theoretically, the incorporation of a low- $\kappa$  dielectric carbon-doped oxide, SiOC in place of a traditional oxide-based dielectric can significantly reduce the triaxial tensile stresses in Cu; however, it also enhances plastic deformation particularly in the via and its vicinity [5.17]. SiOC is commonly known as carbon-doped porous silica where the average porosity is in the range of 1–3 nm [5.18, 5.19]. Therefore, the application of SiOC as a liner material for TSV could potentially alleviate the thermal stress. There is limited experimental evidence of the buffering of the thermo-mechanical stress effect on Si by using low- $\kappa$  SiOC as the liner material in TSV. Owing to a low Young's modulus of  $\sim 4.2$  GPa for the low- $\kappa$  dielectric as compared to 70 GPa for conventional plasma-enhanced tetraethyl orthosilicate (PETEOS) dielectric, a significantly lower transmission of thermal stress to the Si bulk at the close vicinity of Cu-TSV is expected.

Our FEA simulation results shown in Figure 5.12 indicate that the low- $\kappa$  liner with a smaller elastic modulus acts as a compliant layer to cushion the Cu-TSV induced stress on the Si as compared with the PETEOS oxide liner. The stress-free temperature is set at 200°C and the system is cooled down to 25°C for this simulation.

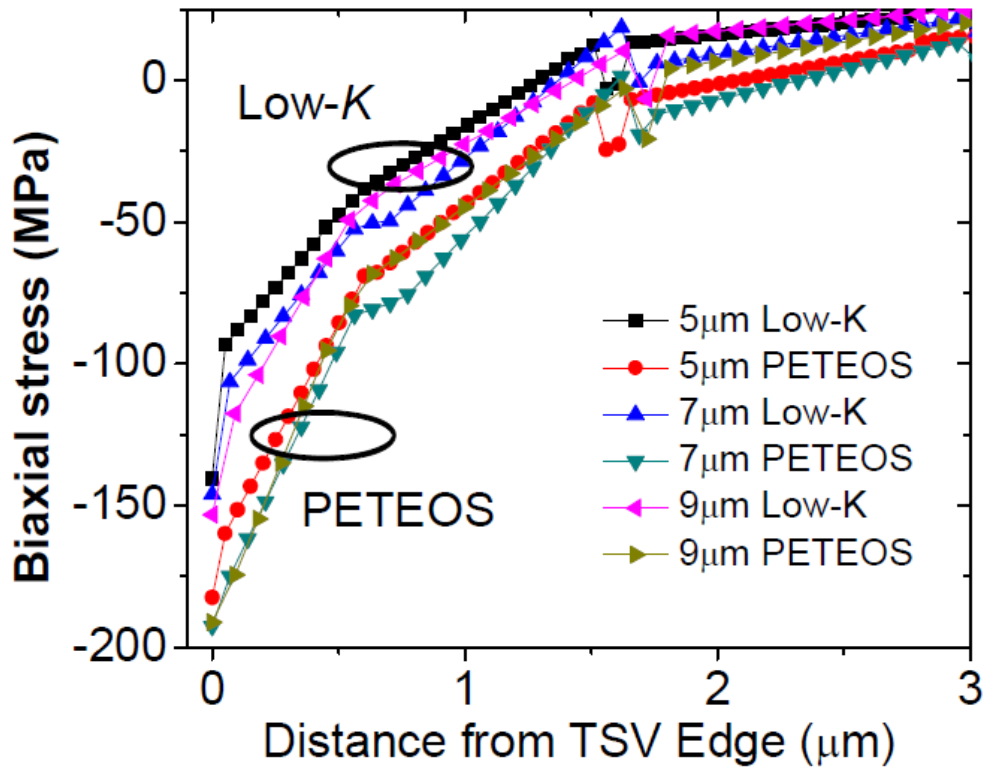


Figure 5.12: FEA simulation results of the thermo-mechanical stress exerted by a single Cu-TSV on the Si substrate as a function of distance from the edge of the TSV. It can be seen that for a TSV structure with a similar diameter, the near-surface stress in the Si surrounding the Cu-TSV decreased substantially when a low- $\kappa$  liner is used rather than the PETEOS oxide liner [5.20].

## 5.4 Cu-TSV Induced Stress Measurement by micro-Raman Analysis

Various techniques have been adopted to investigate the thermo-mechanical stress in the Cu interconnect structures. They include

1. Synchrotron radiation X-ray diffraction [5.21],
2. The bending beam technique [5.22] (i.e., the measurement of curvature change under thermal annealing),
3. Cross-sectional transmission electron microscopy (TEM) with convergent beam electron diffraction [5.23] and
4.  $\mu$ -Raman analysis which is the most effective method [5.9, 5.24].

The high-resolution TEM accompanied by electron diffraction could accurately extract the localized stress information. However, the TEM sample preparation is a destructive process that invariably causes partial stress relaxation that leads to a less accurate measurement. In contrast, the  $\mu$ -Raman analysis is non-destructive and the measurement accuracy level can reach a spectral resolution of  $0.05 \text{ cm}^{-1}$ , which corresponds to 21.7 MPa in the stress variation [5.24]. In addition, changing the Raman laser spectral line could possibly extract the stress depth profile [5.9]. In this work,  $\mu$ -Raman spectroscopy with high-groove-density (2400 gr/mm) diffraction grating was used and resulted in a high spectral resolution of  $0.3 \text{ cm}^{-1}$  per pixel for the 442 nm laser source. Lorentzian peak fitting was then used to further refine the resolution to  $0.03 \text{ cm}^{-1}$  which corresponds to the stress sensitivity level of 15 MPa.

$\mu$ -Raman spectroscopy with a 442 nm laser, a  $100\times$  objective lens (NA = 0.90), and a focused spot size of  $0.8 \text{ }\mu\text{m}$  was used to estimate the stress level in Si surrounding the Cu-TSV. Raman measurement was obtained with a line scan along the [011] direction on the Si (100) wafer with a step of 250 nm as shown schematically in Figure 5.13. To extract this biaxial stress from the Raman shift, the effective proportionality relation was applied as



**Figure 5.13: Schematic of high resolution Raman scanning along a TSV row prior to metallization.**

$$\sigma_r + \sigma_\theta \text{ (MPa)} = -470\Delta\omega \text{ (cm}^{-1}\text{)}, \quad (2)$$

where  $\Delta\omega$  (i.e.,  $\omega_i - \omega_0$ ) is the deviation of the Si–Si Raman vibration peak due to stress,  $\omega_i$  is the Si–Si peak position under stress condition, and  $\omega_0$  is the reference wave-number position for stress-free bulk Si. The measured Raman curves were fitted by Lorentzian fitting for better resolution, similar to the approach reported in [5.25]. A resolution of  $0.03 \text{ cm}^{-1}$  was obtained by fitting. Based on this approach, the stress level in the Si area along the scan line can be calculated.

First of all, the  $\mu$ -Raman analysis was carried out on single TSVs with various diameters to examine and confirm the scaling effect on the thermo-mechanical stress. The measurement result matches well with the simulation result presented in the previous section (Figure 5.11). It shows that the larger the TSV diameter, the higher will be the compressive stress in the Si in the close vicinity of the TSV row. For the PETEOS oxide liner TSV with diameter of  $10 \text{ }\mu\text{m}$ , the maximum stress experienced is  $220 \text{ MPa}$ , whereas that for diameters of  $8 \text{ }\mu\text{m}$ ,  $6 \text{ }\mu\text{m}$  and  $4 \text{ }\mu\text{m}$  is  $123$ ,  $105$  and  $85 \text{ MPa}$ , respectively (shown in Figure 5.14). For the low- $\kappa$  liner TSV, the same dependence is observed. When the diameter is  $10 \text{ }\mu\text{m}$  for the

low- $\kappa$  liner TSV, the maximum stress is only 123 MPa, whereas the stress for diameters of 8  $\mu\text{m}$ , 6  $\mu\text{m}$  and 4  $\mu\text{m}$  is 94, 59 and 42 Mpa, respectively (shown in Figure 5.15). This observed trend is due to the low Cu volume in smaller diameter TSVs, which results in lower stress in the Si surrounding the lower diameter TSV; the stress originates from the large difference in the CTE value for Cu and Si. Similar results have recently been reported in [5.22]. By taking into account the laser intensity attenuation, the measured value of stress is a weighted volume average of the near-surface stress up to the laser penetration depth. In our simulation we consider the overall average resultant stress at a depth of 160 nm from the Si surface, which is the penetration depth of the 442 nm laser. Thus, for the increasing emphasis on miniaturization of modern packaging technology with 3D TSV array interconnect, it is desirable to scale down the TSV diameter below 5  $\mu\text{m}$  in order to minimize the thermo-mechanical stress issue. Table 5.3 summarizes the  $\mu$ -Raman analysis results of the single TSV with various diameters and different liner materials.

<b>TSV Diameter (<math>\mu\text{m}</math>)</b>	<b>TSV with PETEOS Oxide Liner Stress (MPa)</b>	<b>TSV with Low-<math>\kappa</math> Liner Stress (MPa)</b>
10	220	123
8	123	94
6	105	59
4	85	42

**Table 5.3: Summary of  $\mu$ -Raman analysis results of TSVs with various diameters and liner materials.**

Furthermore, the effect of a dielectric liner (PETEOS oxide vs. low- $\kappa$ ) on the Si stress distribution at the close vicinity of TSV interconnects was then carefully studied by  $\mu$ -Raman spectroscopy and is shown in Figure 5.16. The measurement results again match well with the simulation results (in Figure 5.12). It was observed that for a TSV structure with the same diameter, the near-surface stress in Si surrounding the Cu-TSV decreased substantially when a low- $\kappa$  liner is used rather than the PETEOS oxide liner. At the immediate vicinity of the Si/TSV interface, the compressive stress decreased from  $\sim 221$  MPa (PETEOS oxide liner) to  $\sim 122$  MPa (low- $\kappa$  liner) for the TSV with a diameter of  $10\ \mu\text{m}$ . A similar trend was also observed for the  $8\ \mu\text{m}$  TSV (stress decreased from  $\sim 123$  to  $\sim 92$  MPa) and the  $6\ \mu\text{m}$  TSV (stress decreased from  $\sim 106$  to  $\sim 59$  MPa) samples. Hence, it can be concluded that the use of a low- $\kappa$  liner can reduce the compressive stress near the TSV surrounding by 29% to 45%, as compared with the PETEOS oxide counterpart for the TSV diameter presented above. Under our experimental conditions, the observed thermo-mechanical stress relief with a low- $\kappa$  liner could be attributed to the lower Young's modulus of 4.2 GPa (shown in Table 5.2) and higher porosity than those of the PETEOS oxide liner. The lower Young's modulus and higher porosity of the low- $\kappa$  liner make it more compliant as a buffer layer to cushion the stress exerted by Cu-TSV on the surrounding Si.

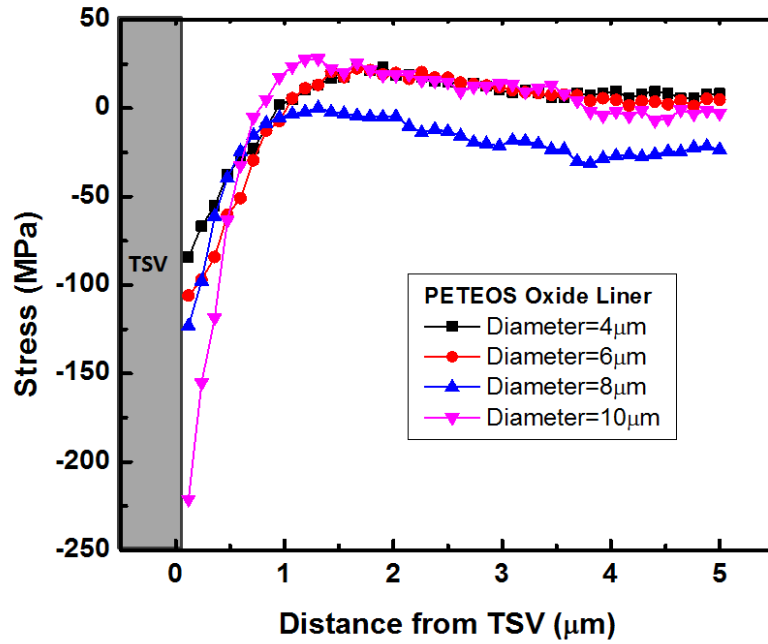


Figure 5.14:  $\mu$ -Raman analysis results of the thermo-mechanical stress exerted by a single Cu-TSV with PETEOS oxide liner on Si substrate as a function of distance from the edge of TSV [5.13].

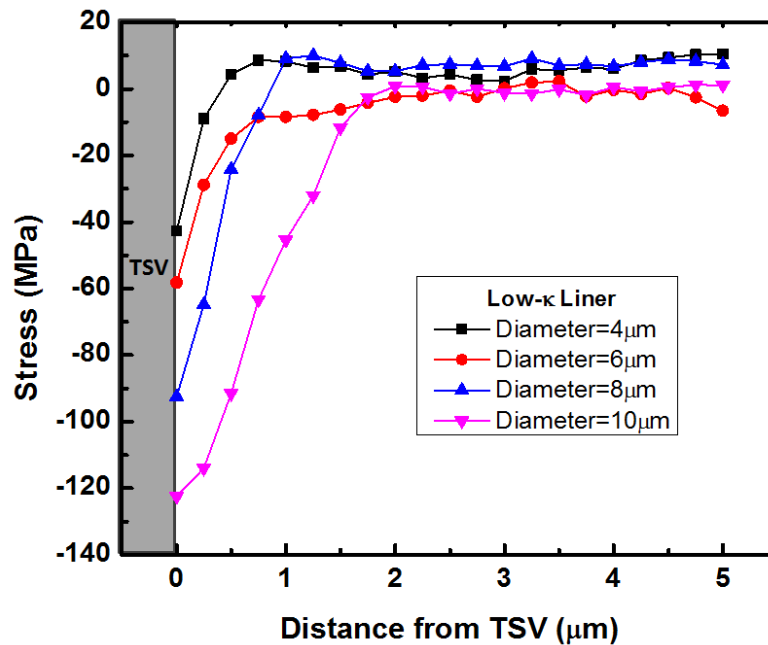
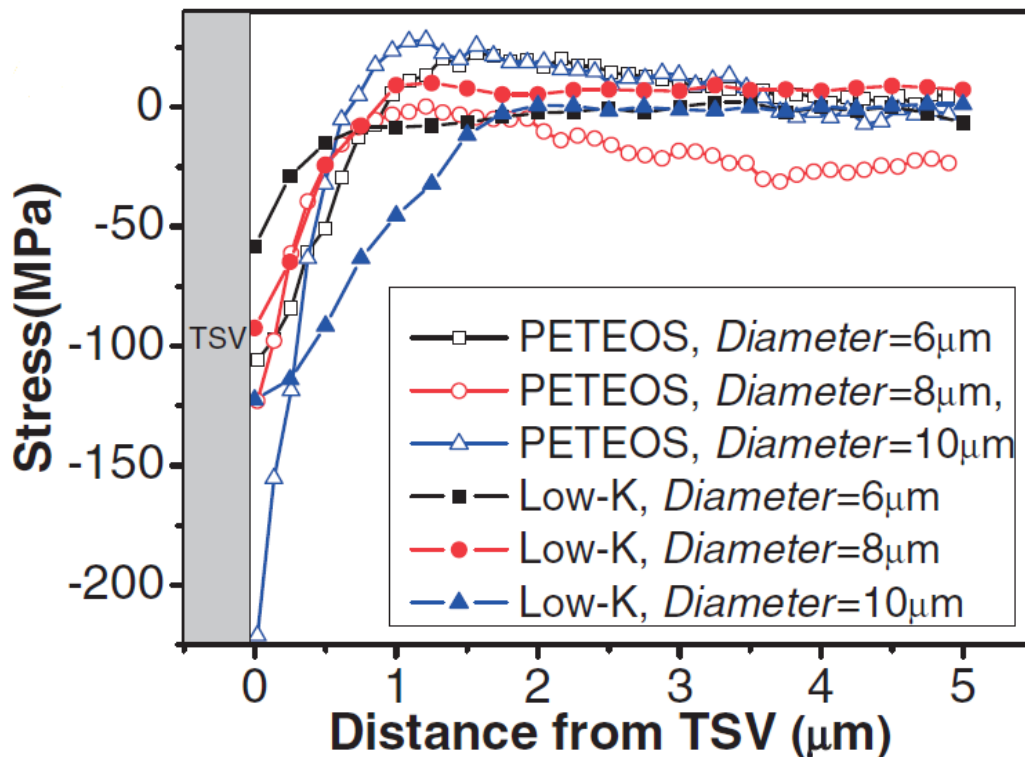


Figure 5.15:  $\mu$ -Raman analysis results of the thermo-mechanical stress exerted by a single Cu-TSV with low- $\kappa$  liner on Si substrate as a function of distance from the edge of TSV.



**Figure 5.16:  $\mu$ -Raman analysis results of the thermo-mechanical stress exerted by a single Cu-TSV on Si substrate as a function of distance from the edge of TSV with PETEOS oxide and low- $\kappa$  dielectric liners. The TSV diameter ranges from 6 to 10  $\mu\text{m}$ . The measurement results match well with the simulation results and show that the low- $\kappa$  liner can act as a compliant layer to reduce the stress on the Si substrate [5.12].**

In order to verify the biaxial stress exerted on Si substrate by Cu-TSV, high resolution  $\mu$ -Raman spectroscopy is also performed on a row of 3 TSVs prior to metallization. In Figure 5.17, it is verified that with a low- $\kappa$  liner lower compressive stress is exerted by the Cu-TSV on the Si between the TSV. This has positive implications on the variability, reliability and keep-out zone (KOZ). The 2D stress map is also presented in Figure 5.18. It is also worthy to

point out that the stress on Si outside of TSV row is due to the liner thin film residual stress on Si which is thickness dependent and could be eliminated with chemical mechanical polishing (CMP).

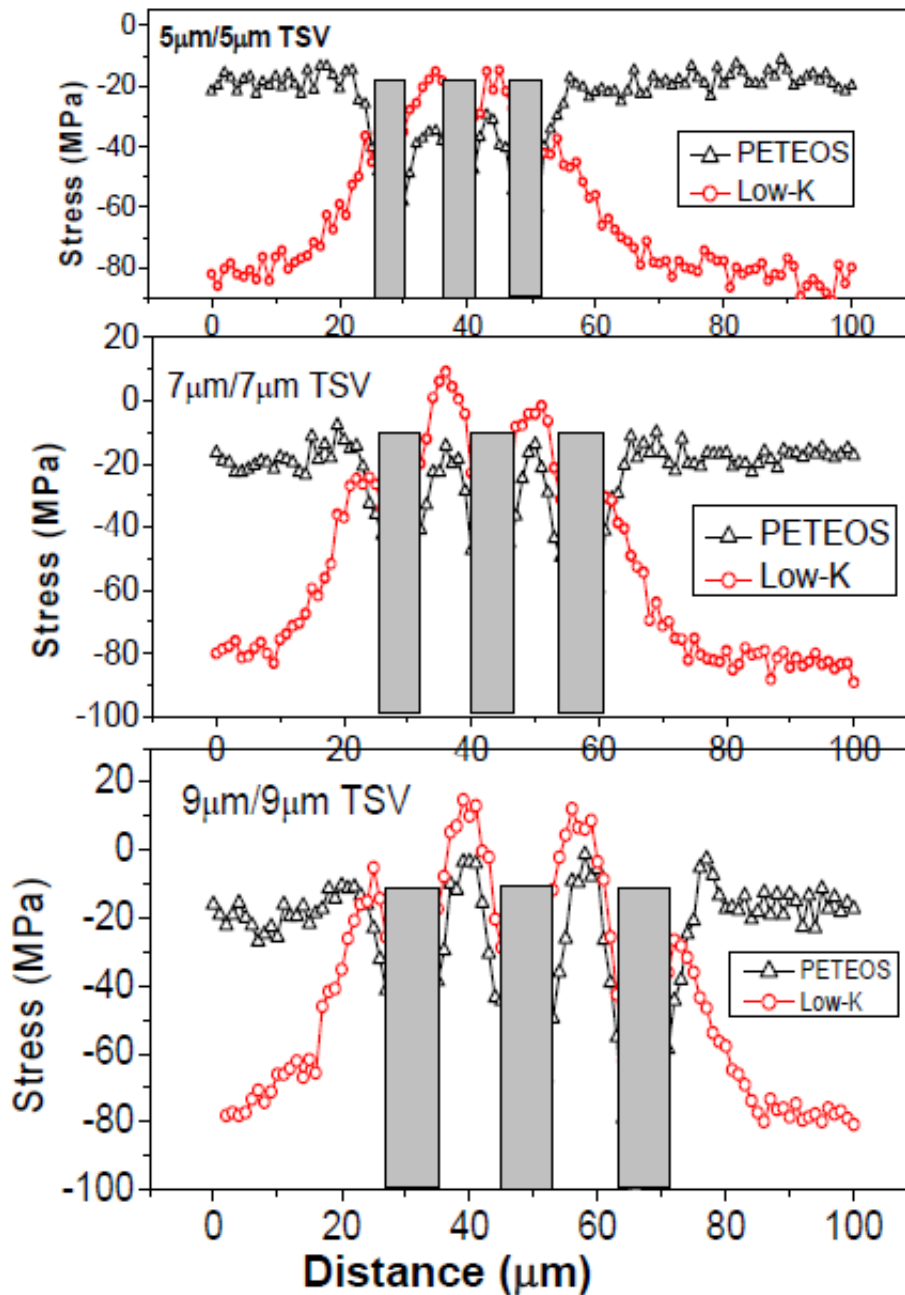


Figure 5.17: Si Stress profile (biaxial) along TSV rows from  $\mu$ -Raman analysis. Each row contains 3 TSVs with similar TSV pitch and diameter (5, 7, 9  $\mu\text{m}$ ). The stress

profiles show the low- $\kappa$  liner is more compliant and can cushion the stress exerted by Cu-TSV on the Si between TSVs more effectively than the PETEOS oxide liner [5.20].

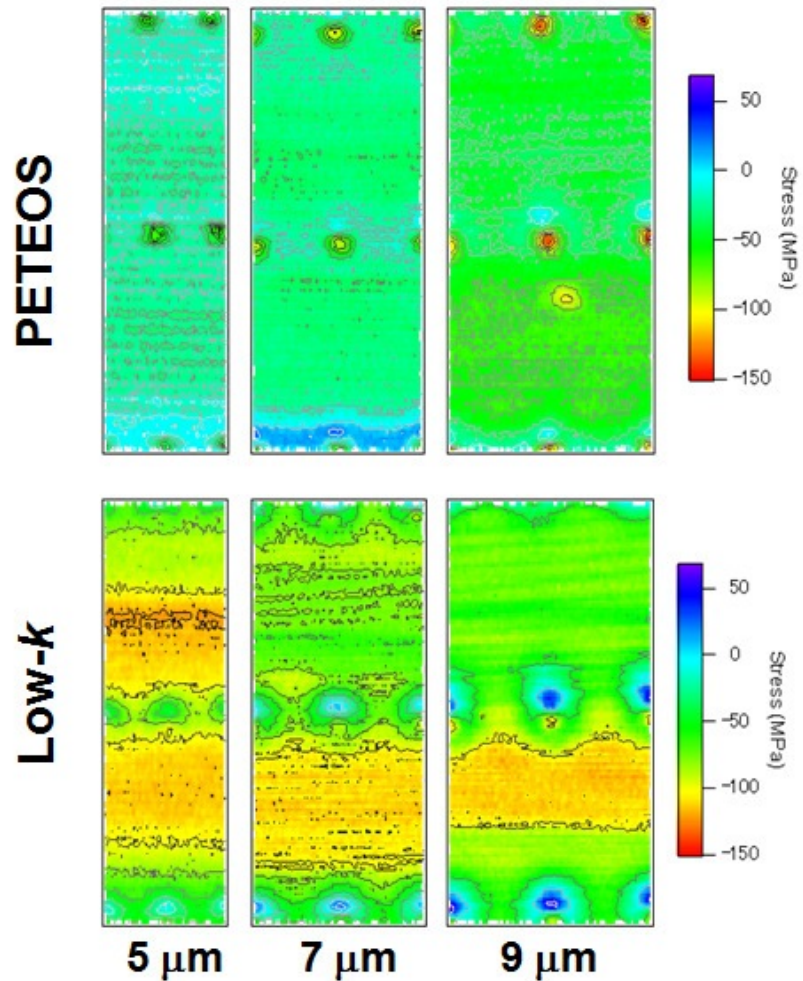


Figure 5.18: Biaxial stress mapping of the Si based on high resolution  $\mu$ -Raman spectroscopy. Each scanning area consists of 3 TSVs in a row with varying diameter and pitch [5.20].

## 5.5 Summary

In this chapter, the thermal characterization of TSV as a heat removal element is firstly examined and the results show that TSV arrays can effectively conduct the heat away through the Cu core to the silicon substrate. Significant temperature reduction of up to  $\sim 44$  °C was experimentally achieved by placing two rows of TSV with a diameter of 5  $\mu\text{m}$ , a depth of 10  $\mu\text{m}$ , and a pitch of 15  $\mu\text{m}$  beneath the doped polysilicon line. Moreover, both the simulation and  $\mu$ -Raman analysis results demonstrated that the miniaturization of the TSV dimension is one way to reduce the thermo-mechanical stress in Si surrounding the TSV structure due to the lower Cu volume. It is also possible to control the stress level via the selection of a suitable liner material with a lower elastic modulus. The interesting findings in this work can be attributed to the fact that the choice of a lower Young's modulus and a porous dielectric liner material could effectively reduce the compressive near-surface stress in Si by 29%–45% as compared with the conventional liner such as PETEOS oxide which is more rigid. This work has provided evidence of the technical merits of a low- $\kappa$  material to mitigate an undesired Cu-TSV induced stress in the surrounding Si.

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# Chapter 6: Conclusion and Future Work

## 6.1 Summary and Contributions

Through-silicon-vias (TSV) with diameters of 5  $\mu\text{m}$  and depths between 10-15  $\mu\text{m}$  have been successfully fabricated. Sidewall scalloping roughness and undercut were improved significantly by adding passivating  $\text{C}_4\text{F}_8$  gas in the etching cycle of BOSCH process and using double mask step. This optimization resulted in a final sidewall roughness and undercut in the range of 50-75 nm. PETEOS oxide liner as well as Black Diamond low- $\kappa$  liner were then integrated with the TSV structures with excellent step coverage. In addition, novel bi-layer liners which consists of either  $\text{Al}_2\text{O}_3$  and PETEOS oxide or  $\text{Al}_2\text{O}_3$  and low- $\kappa$  have also been successfully integrated in the TSV structure. The TSV structures were then fully filled with Cu without any voids or delaminations.

Electrical  $C$ - $V$  measurement results show that through careful process tuning, a negative fixed charged can be induced during the PETEOS oxide liner deposition to cause a positive flat-band voltage ( $V_{FB}$ ) shift so that the TSV capacitance is kept in the stable accumulation capacitance region within the range of interest for the operating voltage ( $\sim 0$ -5 V). Furthermore, the utilization of  $\text{Al}_2\text{O}_3$ -induced negative fixed charge was also successfully demonstrated to shift the  $C$ - $V$  curve effectively so that the stable accumulation capacitance was maintained. This is essential for applications which require a stable TSV capacitance and is desirable for circuit prediction when there are hotspots caused by non-uniform heating during operation. The  $C$ - $V$  measurement results of the TSVs with low- $\kappa$  material as the liner show that a  $\sim 28\%$  reduction in capacitance is achieved as compared to the TSVs with PETEOS oxide liner. Electrical  $I$ - $V$  measurements were also carried out to monitor the dielectric leakage. Results show that no abrupt breakdown is observed for both oxide and

low- $\kappa$  liner until an electric field of at least 3 MV/cm is applied. By annealing in forming gas ( $N_2/H_2$ ) at 350°C for 30 min, the leakage current density of the low- $\kappa$  liner is improved to the level comparable with that of oxide liner.

TSV array as a passive heat removal element was successfully demonstrated. Significant temperature reduction of up to  $\sim 44$  °C is experimentally achieved by placing two rows of TSV with a diameter of 5  $\mu\text{m}$ , a depth of 10  $\mu\text{m}$ , and a pitch of 15  $\mu\text{m}$  beneath a doped polysilicon line through which a power density of  $8 \times 10^7$  W/m<sup>2</sup> was injected. In addition, through thermo-mechanical modelling and measurement results by micro-Raman analysis, we show that TSV dimension scaling is one possible method to reduce the thermo-mechanical stress in Si surrounding the TSV structure due to the lower Cu volume. Another possible method to control the stress level is to select a suitable liner material with a lower elastic modulus, such as a low- $\kappa$  material which can act as a compliant layer to cushion the stress.

## 6.2 Future Work

In this project, the fabrication process of TSV with diameter of 5  $\mu\text{m}$ , and depth of 10-15  $\mu\text{m}$  have robustly demonstrated. Novel material selections, such as low- $\kappa$ , bi-layer liner which incorporates  $\text{Al}_2\text{O}_3$ , as the TSV liner material have been systematically studied in terms of electrical characterizations, and thermo-mechanical stress study. Significant capacitance reduction, capacitance stabilization and stress mitigation are achieved for 3D IC applications. Beyond the work presented in this thesis, the following recommendations are worthy for future work:

- 1) The fabrication of TSVs with smaller dimensions, such as diameter  $< 5 \mu\text{m}$  and higher aspect ratios  $> 5$  needs to be investigated and fabricated for higher density requirement. Characterization to study the effects of further downscaling the TSV dimensions would be useful.

- 2) For the low- $\kappa$  liner to be effectively used in TSV applications, further optimization in the leakage current is required. Possible solutions include optimization in annealing, such as annealing with higher temperature or longer duration; optimization in scalloping roughness, and to use a slightly thicker low- $\kappa$  liner.

- 3) A low- $\kappa$  liner should also be integrated in the TSV structure for thermal property study, so that the comparison of the thermal conduction properties between low- $\kappa$  and PETEOS oxide liners can be studied.

- 4) The TSV structures can be incorporated with Cu-Cu bonding to demonstrate the 3D integration. The transistor fabrication FEOL process can be involved so that comprehensive test structures could be included in the future study to evaluate the effects of TSV, such as the thermo-mechanical stress, on transistor operations.

# List of Achievement and Publications

## Achievement:

1. Commendation Award of the 6<sup>th</sup> Taiwan Semiconductor Manufacturing Co (TSMC) Outstanding Student Research Award in Hsinchu, Taiwan, September, 2012.

## Journal Publications:

1. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, "Achieving Stable Through-Silicon-Via (TSV) Capacitance with Oxide Fixed Charge", *IEEE Electron Device Letters*, 32 (5), 2011.
2. **L. Zhang**, D. F. Lim, H. Y. Li, S. Gao, and C. S. Tan, "Through Silicon Via Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current", *Japanese Journal of Applied Physics*, 51 (4), 2012.
3. **L. Zhang**, L. Peng, H. Y. Li, D. L. Kwong, and C. S. Tan, "Operating TSV in Stable Accumulation Capacitance Region by Utilizing Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge", *IEEE Electron Device Letters*, 33 (6), 2012.
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5. L. Peng, **L. Zhang**, J. Fan, H. Y. Li, D. F. Lim, and C. S. Tan, "Ultrafine Pitch (6-um) of Recessed and Bonded Cu-Cu Interconnects by Three-Dimensional Wafer Stacking," *IEEE Electron Device Letters*, 33 (12), 2012.

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### **Conference Publications:**

1. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, "Design, Fabrication and Electrical Characterization of TSV", *12th Electronics Packaging Technology Conference (EPTC)*, December, 2010.
2. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, "Techniques to Stabilize Through-Silicon-Via (TSV) Capacitance within the Operating Voltage Region", *International Conference on Materials for Advanced Technologies (ICMAT)*, June, 2011.
3. **L. Zhang**, H. Y. Li, S. Gao, and C. S. Tan, "Through Silicon Via (TSV) Fabrication with Low-k Dielectric Liner and Its Implications on Parasitic Capacitance and Leakage Current", *International Conference on Solid State Devices and Materials (SSDM)*, September, 2011.
4. **L. Zhang**, R. I Made, H. Y. Li, S. Gao, G. Q. Lo, D. L. Kwong, and C. S. Tan, "Spatial Variation of TSV Capacitance and Method of Stabilization with Al<sub>2</sub>O<sub>3</sub>-Induced Negative Fixed Charge at the Silicon-Liner Interface", *IEEE International Electron Devices Meeting (IEDM)*, December, 2011.
5. L. Peng, J. Fan, **L. Zhang**, H. Y. Li, D. F. Lim, and C. S. Tan, "Ultrafine pitch (6-um) evolution of Cu-Cu bonded interconnects in 3D wafer-on-wafer stacking," *International Interconnect Technology Conference (IITC)*, June 4-6, 2012.
6. **L. Zhang**, K. Ghosh, J. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "TSV Scaling with Constant Liner Thickness and the Related Implications on Thermo-mechanical Stress, Capacitance, and Leakage Current," *International*

*Conference on Solid State Devices and Materials (SSDM)*, Kyoto, Japan, September 25-27, 2012.

7. **L. Zhang**, K. Ghosh, J. Zhang, Y. Dong, H.Y. Li, C. M. Tan, G. Xia, and C. S. Tan, "Strategy for TSV Scaling with Consideration on Thermo-mechanical Stress and Acceptable Delay," *International Microsystems, Packaging, Assembly Circuits Technology Conference (IMPACT)*, Taipei, Taiwan, October 24-26, 2012.
8. **L. Zhang**, H. Y. Li, G. Q. Lo, and C. S. Tan, " Thermal Characterization of TSV Array as Heat Removal Element in 3D IC Stacking," *Electronic Packaging Technology Conference (EPTC)*, Singapore, December 5-7, 2012.
9. L. Peng, **L. Zhang**, H. Y. Li, G. Q. Lo, and C. S. Tan, "Mechanical Characterization of Wafer Level Bump-less Cu-Cu Bonding," *Electronic Packaging Technology Conference (EPTC)*, Singapore, December 5-7, 2012.
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