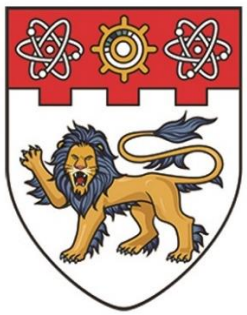


NANYANG TECHNOLOGICAL UNIVERSITY
SINGAPORE

TOPOLOGIES AND CONTROL METHODS FOR PROTECTION OF DC ELECTRICAL SYSTEM IN AIRCRAFT

MRIDUL MARWAHA

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

2023

TOPOLOGIES AND CONTROL METHODS FOR PROTECTION OF DC ELECTRICAL SYSTEM IN AIRCRAFT

MRIDUL MARWAHA

School of Electrical & Electronic Engineering

A thesis submitted to the Nanyang Technological University
in partial fulfilment of the requirement for the degree of
Doctor of Philosophy

2023

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarised materials, and has not been submitted for a higher degree to any other University or Institution.

16/01/2023

. . . . . .
Date

. . . . . .
Mridul Marwaha

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

16/01/2023

of. Josep Pou

Authorship Attribution Statement

This thesis contains material from 2 to be submitted and 3 papers published in the following peer-reviewed journal(s) / from papers accepted at conferences in which I am listed as an author.

A part of Chapter 2 is published as M. Marwaha, M.H.M. Sathik, K. Satpathi, Y. Yu, F. Sasongko, J. Pou, C. Gajanayake, and A. K. Gupta, "Comparative Analysis of Si, SiC and GaN Field-Effect Transistors for DC Solid-State Power Controllers in More Electric Aircraft," in *Proc. IEEE Energy Convers. Congr. Expo. - Asia (ECCE-Asia)*, pp. 592-597, May 2021. DOI: 10.1109/ECCE-Asia49820.2021.9479031.

The contributions of the co-authors are as follows:

- This work was carried out under the supervision of Prof. J. Pou.
- Prof. J. Pou and Dr. C. Gajanayake provided the initial project direction, provided several valuable advice, provided guidance, and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I co-designed the hardware with Dr. M.H.M. Sathik and performed the laboratory work at the Rolls-Royce@NTU corporate lab. I also analyzed the data.
- Dr. K. Satpathi, Dr. Y. Yu, and Dr. F. Sasongko, assisted in improving the manuscript and also in hardware setup design and experiments.
- Dr. A. K. Gupta provided guidance to improve the works and manuscript.

Chapter 5 is published as

M. Marwaha, K. Satpathi, J. Pou, D. A. Molligoda, C. Gajanayake, and A. K. Gupta, "Coupled-Inductor-Based Bidirectional Z-Source Breaker for DC System Protection," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, pp. 3433-3438, Oct. 2020. DOI: 10.1109/IECON43393.2020.

9255389.

The contributions of the co-authors are as follows:

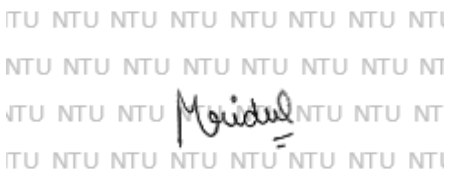
- This work was carried out under the supervision of Prof. J. Pou.
- Dr. K. Satpathi, Prof. J. Pou, and Dr. C. Gajanayake, provided the initial project direction, provided several valuable advice, provided guidance, and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I performed the simulation work at the Rolls-Royce@NTU corporate lab. I also analyzed the data.
- Dr. D. A. Molligoda assisted in improving the works and manuscript.
- Dr. A. K. Gupta provided guidance to improve the works and manuscript.

M. Marwaha, K. Satpathi, M. H. M. Sathik, J. Pou, C. J. Gajanayake, A. K. Gupta, D. Molligoda, and R. K. Surapaneni, "SCR-Based Bidirectional Circuit Breaker for DC System Protection with Soft Reclosing Capability," *IEEE Trans. Ind. Electron. [Early Access].* DOI: 10.1109/TIE.2022.3187585.

The contributions of the co-authors are as follows:

- This work was carried out under the supervision of Prof. J. Pou.
- Dr. K. Satpathi, Prof. J. Pou, and Dr. C. J. Gajanayake, provided the initial project direction, provided several valuable advice, provided guidance, and edited the manuscript drafts.
- I prepared the manuscript drafts.
- I designed the hardware and performed the laboratory work at the Rolls-Royce@NTU corporate lab. I also analyzed the data.
- Dr. M. H. M. Sathik provided some components for hardware setup.
- Dr. D. Molligoda assisted in improving the works, and also in the analysis of the results.

- Dr. M. H. M. Sathik, Dr. D. Molligoda, and Dr. R. K. Surapaneni, assisted in improving the manuscript and also in hardware setup design and experiments.
- Dr. A. K. Gupta provided guidance to improve the works and manuscript.



16/01/2023

. . . . . .

Date

. . . . . .

Mridul Marwaha

Acknowledgements

I would like to express my sincere gratitude to my supervisor, Prof. Josep Pou, for his guidance, valuable advice, and unparalleled support, throughout the study. His teachings, have helped me develop understanding of this subject, as well as, have helped me grow personally. I would also like to thank him for his enthusiastic encouragement.

I would like to extend my sincere thanks to my Rolls-Royce manager, Dr. Chandana Gajanayake, for guidance and technical discussions. I would also like to thank him for motivating me. I am extremely grateful to my Thesis Advisory Committee members, Adjunct Assoc. Prof. Amit Gupta and Assoc. Prof. Xu Yan, for their helpful advice.

I thankfully acknowledge the financial assistance provided by Nanyang Technological University, Rolls-Royce Singapore Pte. Ltd, and National Research Foundation (NRF) of Singapore.

Special thanks to researchers, Dr. Kuntal Satpathi, Dr. Devinda Molligoda, Dr. Mohamed Halick Mohamed Sathik, Dr. Neha Beniwal, Dr. Liang Gaowen, Dr. Yu Yang, Dr. Ravi Kiran Surapaneni, Dr. Firman Sasongko, Dr. Anh Vu Ho, Dr. Ezequiel Rodriguez Ramos, Dr. Hossein Dehghani Tafti, Dr. Glen Ghias Farivar, Dr. Naga Brahmendra Yadav Gorla, Dr. Suvajit Mukherjee, Dr. Suman Mondal, Dr. Wang Shuai, Dr. Sun Changjiang, Dr. Sarbani Mukherjee, Dr. Shafquat Ullah Khan, for valuable advice and encouragement. Many thanks to Mr. Zeng Yu, Mr. Xia Yang, Ms. Aditi Narang, Mr. Jiang Zhuolin, Mr. Gaurav Mani Gupta, Mr. Liu Qingxiang, Mr. Hein Wai Yan, Ms. Anusha Kumaresan, Ms. Radhika Sarda, Mr. Enrique Alejandro, Mr. Xie Dunjian, Mr. Jie Huamin, Mr. Dong Jiaxin, Mr. Dai Jiahong, for insightful discussions and encouragement. I would like to thank Mr. Herbert Ratemo, Mr. Ramash Manoharan, Mr. Lim Kim Peow, Ms. Lakshmi Pathiyil, for their kind help in lab related documents.

I am thankful to all my friends in Singapore. Many thanks to Avalpreet, for his help since first day in this university. I would also like to thank him for all the talks and motivating me during the journey. Thanks also to Tauquir, Vijesh, Anshuman, Parikshit, Juhi, Sankaran, Apoorva, for all the discussions that we had.

I am extremely thankful to my parents and my brother, for love and unwavering support.

Abstract

Conventional aircraft are evolving towards more-electric aircraft, replacing the mechanical, pneumatic, and hydraulic subsystems with their electrical counterparts. More-electric aircraft provide many advantages such as high efficiency, extended control, less maintenance requirement, and fuel saving. Recent studies have shown that the adoption of a dc grid in these electrical systems further improves the overall efficiency and performance. However, fault currents in dc grids have no zero crossings, making fault isolation highly challenging. In ac grids, mechanical circuit breakers (MeCBs) are the most commonly used fault isolation devices. However, there are several limitations of MeCBs in dc grids such as slow response time, additional auxiliary circuit requirement, and limited dc fault current breaking capability. To overcome these limitations, solid-state power controllers/ solid-state circuit breakers (SSPCs/ SSCBs) are emerging as a promising technology for protection of dc electrical systems in aircraft. This thesis is mainly focused on these SSPCs/ SSCBs.

The capacitors associated with the power electronic converters are initially at zero potential. Direct connection of a dc source and these capacitors, results in very high peak current and voltage overshoot, which can cause high stress on the semiconductor devices, capacitors, and current feeding components. One of the main challenges of SSPCs/ SSCBs is to smoothen the inrush current. The first part of the contribution of the thesis is focused on precharging.

Constant current precharging control strategy is proposed in this thesis, which regulates the semiconductor device current by varying the gate-source voltage. The main objective of this method is to ensure that the device current follows a constant reference. The proposed algorithm has improved adaptability and applicability. In this method, the operating temperature is assumed to be constant. However, the value of this parameter varies. In order to address this point, a constant temperature precharging algorithm is proposed in this thesis. The proposed control strategy regulates the junction temperature of the semiconductor device. This parameter is

controlled in such a way that the thermal stress on the semiconductor device is low. The proposed precharging algorithms are verified on a laboratory prototype. The experimental results obtained using this setup, are presented in this thesis.

Another important consideration is that SSPCs/ SSCBs have high on state power loss. This is because semiconductor devices are in the load current path. To overcome this limitation, silicon controlled rectifier (SCR) based SSPCs/ SSCBs are considered as one of the promising solutions. The second part of the contribution of the thesis is focused on SCR based SSPCs/ SSCBs.

Z Source Breakers (ZSBs) are one class of SCR based SSPCs/ SSCBs. A coupled inductor based bidirectional ZSB topology is proposed in this thesis. The proposed topology has lower on state power loss, and simple structure. However, ZSBs imposes an upper limit on the step-load change, and this complicates the design of protection coordination. In order to address these points, an SCR-based bidirectional SSPC/ SSCB (SCR-BCB) topology is proposed in this thesis. Additionally, the proposed SCR-BCB topology has soft reclosing capability. The proposed SCR-BCB topology is verified using simulation and hardware experiments.

Table of Contents

List of Figures

List of Tables

List of Acronyms and Notations

A. List of Acronyms

ac	Alternating Current
APU	Auxiliary Power Unit
ATRU	Auto Transformer Rectifier Unit
CI-BZSB	Coupled-Inductor-Based Bidirectional Z-Source-Breaker
DAC	Digital-to-Analog Converter
dc	Direct Current
ETO	Emitter Turn-off Thyristor
FCLI	Fault Current Limiter and Interrupter
FCS	Fully Controlled Semiconductor
FETs	Field Effect Transistors
GaN	Gallium Nitride
GCT	Gate Commutated Thyristor
GTO	Gate Turn-off Thyristor
HCB	Hybrid Circuit Breaker
HVac	High Voltage Alternating Current
HVdc	High Voltage Direct Current
IATA	International Air Transport Association
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
LCS	Load Commutation Switch
MEA	More Electric Aircraft
MeCB	Mechanical Circuit Breaker
MOV	Metal Oxide Varistor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
PWM	Pulse Width Modulation
SCR	Silicon Controlled Rectifier
SCR-BCB	SCR-based bidirectional SSPC/ SSCB

SiC	Silicon Carbide
SOA	Safe Operating Area
SPI	Serial Peripheral Communication
SSPC/ SSCB	Solid State Power Controller/ Solid State Circuit Breaker
SW	Switching Element
TRU	Transformer Rectifier Unit
UFD	Ultra-Fast Disconnector
WBG	Wide Bandgap
ZSB	Z-Source Breaker

B. List of Notations

C_{case}	Thermal capacitance of the case
C_L	Load capacitor
i_c	Capacitor current
I_{cmax}	Maximum value of capacitor current
i_d	Drain current
i_s	Source current
I_{ref}	Current reference
I_{rm}	Maximum value of current reference
L_{pc}	Precharging inductor
p_d	Power dissipated by semiconductor device
R_{CE}	Collector-emitter resistance
R_{DS}	Drain-source resistance
R_{pc}	Precharging resistance
$R_{th(j-c)}$	Thermal resistance junction-case
T_s	Step/ sampling time
t_{step}	Interrupt service routine time
$t_{junc.}$	Junction temperature
t_{case}	Case temperature
V_{CE}	Collector-emitter voltage
V_{Cexp}	Expected value of capacitor voltage
v_{gs}	Gate-source voltage
V_s	Source voltage

Chapter 1

Introduction

1.1 Background and Motivations

Global warming due to carbon emissions, has a severe impact on planet Earth. In order to limit the global temperature increase, many countries have introduced net zero policies, these aim to drastically reduce emissions in the coming few decades. Fig. 1.1 shows percentage of total global emissions covered under net zero targets and its distribution. Aviation sector contributes towards these emissions and is also included in net zero targets. Fig. 1.2 shows the contribution of the aviation sector towards global carbon dioxide emissions as a function of time. This sector contributes $\approx$ 2.5 % of global carbon dioxide emissions. The absolute value of carbon dioxide emissions has an increasing trend year by year, as depicted by the red line in Fig. 1.2. According to the 'Jet Zero Strategy: Delivering net zero aviation by 2050' report [19],

"At current rates, aviation is expected to become one of the largest emitting sectors by 2050. We have to break the link between air travel and rising global temperatures. Aviation's success must no longer damage the planet. That is why we have developed the Jet Zero Strategy – not only securing a more sustainable future for our climate, but also for our aviation industry, and the critical role it plays in boosting trade, tourism and travel"

Therefore, net zero targets are important, and these facilitate to limit the rising global temperature and avoid extreme climatic behaviors.

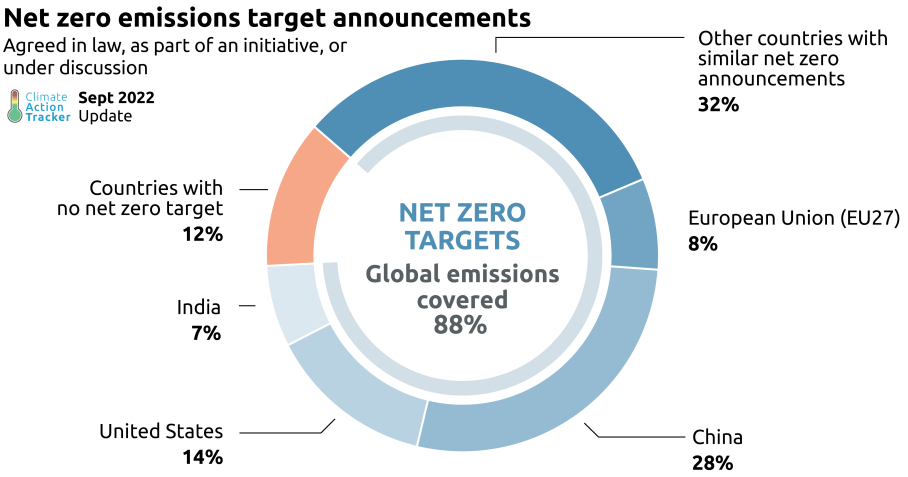


Figure 1.1: Percentage of total global emissions covered under net zero targets [1].

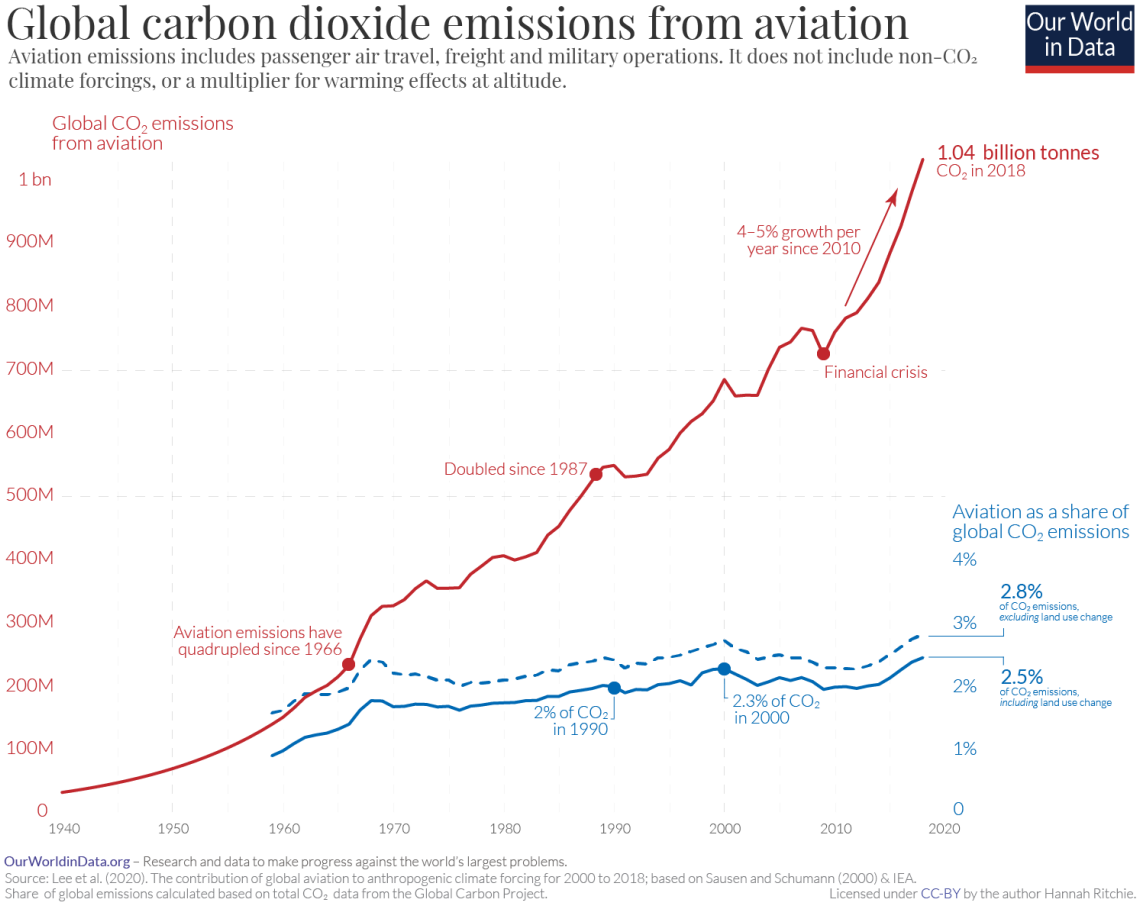


Figure 1.2: Contribution of aviation sector towards global carbon dioxide emissions [2].

In order to achieve these targets, it is essential to explore and develop new technologies, and at the same time, improve existing technologies. According to the International Air Transport Association (IATA), Press Release No. 66 [20],

“The strategy is to abate as much CO2 as possible from in-sector solutions such as sustainable aviation fuels, new aircraft technology, more efficient operations and infrastructure, and the development of new zero-emissions energy sources such as electric and hydrogen power. Any emissions that cannot be eliminated at source will be eliminated through out-of-sector options such as carbon capture and storage and credible offsetting schemes.

“We have a plan. The scale of the industry in 2050 will require the mitigation of 1.8 gigatons of carbon. A potential scenario is that 65% of this will be abated through sustainable aviation fuels. We would expect new propulsion technology, such as hydrogen, to take care of another 13%. And efficiency improvements will account for a further 3%. The remainder could be dealt with through carbon capture and storage (11%) and offsets (8%). The actual split, and the trajectory to get there, will depend on what solutions are the most cost-effective at any particular time. Whatever the ultimate path to net zero will be, it is absolutely true that the only way to get there will be with the value chain and governments playing their role,” said Walsh.”

More efficient operations can be achieved by electrification, thus, it is considered as one of the promising solutions for reducing emissions, enabling the way towards more sustainable aviation. Some of the additional advantages of electrification are less maintenance requirement, fuel saving, and extended control [4, 21–23]. These benefits lead to increased revenue of aircraft manufacturers and operators.

In more-electric aircraft (MEA), mechanical, pneumatic, and hydraulic subsystems of conventional aircraft are replaced with their electrical counterparts [24–26]. Adoption of dc grids into electrical systems can further improve the operational efficiency [27–29]. Some of the prominent advantages are absence of reactive power flow, no skin and proximity effect, and reduced power conversion steps. There are several differences between onboard dc grids and ground-based dc grids [24]. The power requirement in case of onboard dc grids is dependent on the mission profile, and thus, varies drastically with time. In addition, in the case of onboard dc grids, power density and reliability are considered as very important factors. Moreover, subsystems in onboard dc grids have different voltage level requirements. Sensitive electronic components require a low voltage source, and power electronics components require a high voltage source. However, special consideration is required for fault isolation devices due to the absence of current zero-crossing in dc grids [27, 30].

In ac grids, MeCBs are the most commonly used fault isolation devices. However, there are many limitations of these MeCBs in dc grids such as frequent welding of contacts, slow response time, and limited dc fault current breaking capability [5, 12, 13]. In order to address these issues of MeCBs, semiconductor-based SSPCs/ SSCBs have recently gained popularity as a promising alternative [8, 12–16]. SSPCs usually provide more functions that SSCBs. These functions are related to the supervision and diagnostics of the circuit. However, the main task of both SSPCs and SSCBs is to protect the components of an electrical network, and both of them are semiconductor-based protection devices, due to which, these terms are used interchangeably. Some of the key advantages of SSPCs/ SSCBs are discussed as follows,

- Semiconductor devices are the main switching element due to which fault isolation is fast. Consequently, fault current magnitude is less.
- No arc is formed during the fault isolation process.
- It is easy to remotely control SSPCs/ SSCBs because the gating signals are of low voltage value. Therefore, the system level controllability is improved. In addition, this feature enables distributed protection panels, and these are closer to the source and load centers. Consequently, wire length is reduced.
- In addition to the on and off states, SSPCs/ SSCBs are able to produce pulsed output voltage. The duty-ratio of the pulse-width modulation (PWM) signal, affects the average value of the output voltage. Therefore, SSPCs/ SSCBs have advanced load management capability.
- MeCBs have some sort of mechanism to separate the contacts, and this mechanism is noisy. SSPCs/ SSCBs are less noisy because semiconductor devices are the main switching element.
- SSPCs/ SSCBs have a micro-controller unit, which executes the control algorithm. The input pins of these controllers are connected to the sensors. Thus, SSPCs/ SSCBs have sensing and processing capabilities, due to which these can also be employed for predictive maintenance of various subsystems.

In spite of the above mentioned advantages, there are limitations of SSPCs/ SSCBs. These limitations are discussed as follows,

- Initially, the capacitors associated with the capacitive loads have no charge. Direct connection of source and uncharged capacitor causes high peak current and voltage transient, which has a severe impact on the semiconductor devices, capacitors, and current feeding components. SSPC/ SSCB's job is to suppress the inrush current and charge the capacitor in a controlled manner. In order to accomplish this task, SSPCs/ SSCBs have some sort of precharging mechanism. Most of the precharging methods in the literature make use of an additional circuit. This circuit adds to the weight of the overall system, which is a critical factor in aerospace applications.

- On state power loss is dependent on the type of element in the load current path. SSPCs/ SSCBs have high power loss because load current flows through the semiconductor devices.

The advantages of SSPCs/ SSCBs clearly highlight that it is a promising technology for protection of dc grids. However, there are limitations of this technology and these are addressed in this thesis.

1.2 Research Objectives

SSPC/ SSCB technology is a key-enabler for wide-spread adoption of dc grids. Thus, it is important to address issues associated with this technology and these are considered in this research. The main objectives of this thesis are as follows,

- Analysis of various switchgear devices, power semiconductor devices, SSPC/ SSCB topologies, and precharging methods under different operating conditions. This objective is addressed in Chapter 2.

- Suggest novel precharging methods, which do not require additional precharge circuit, are easy to implement, and are usable for a wide range of semiconductor devices. This objective is addressed in Chapter 3 and 4.

- Suggest a novel Z-Source breaker (ZSB) topology, which has low on state power loss, simple structure, and is bidirectionally symmetric. Investigate the limitations of ZSBs, and examine alternate solutions. This objective is addressed in Chapter 5.

- Suggest a novel silicon controlled rectifier (SCR)-based SSPC/ SSCB topology, which overcomes the limitations of ZSBs and has soft reclosing capability. This objective is addressed in Chapter 5.

1.3 Major Contributions of the Thesis

The research work has been carried out to fulfill the research objectives. The major contributions of this thesis are as follows,

- A constant current precharging algorithm is proposed. The main novelty is that the proposed algorithm has a higher adaptability to the change of source parameters. In addition, it is easily implementable to a wide range of semiconductor devices. Moreover, the main semiconductor device is utilized for precharging instead of adding an auxiliary circuit, thus reducing the required number of components. The flowchart of the proposed algorithm, analytical evaluations, and experimental results, are presented in this thesis.

- An active thermal precharging algorithm for control of SSPCs/ SSCBs is developed. The main novelty is that the thermal stress on the semiconductor device is regulated. In addition, it has high adaptability to the change of source parameters as well as ambient temperature. The proposed algorithm is verified using hardware experiments and the results demonstrate that good regulation of junction temperature is achieved.

- A coupled-inductor-based bidirectional ZSB topology is proposed. The main novelty is that the number of power semiconductor devices in the load current path are less. Therefore, the on state power loss is lower. In addition, even with unequal values of inductors, the proposed topology is symmetric. The mathematical analysis and simulation results are presented in this thesis.

- A novel SCR-based bidirectional dc SSPC/ SSCB topology is proposed. The main novelty is that the proposed topology has soft reclosing capability. This capability helps in reducing repetitive voltage and current stress on the breaker and current feeding components. Additionally, the heat loss by the surge suppression devices during reclosing is negligible. In order to analyse the effect of component values on various circuit-level considerations, mathematical expressions are derived in this thesis. Simulation and scaled-down experimental

results are also presented to verify the operation of the breaker under various operating conditions.

1.4 Organization of the Thesis

This thesis has six chapters. The main contents of the rest of the chapters are summarized as follows,

Chapter 2 presents an overview of existing studies in the field of research. MEA architecture and challenges associated with fault protection of dc subsystem, are discussed. Various switchgear and protection devices are reviewed in this chapter. Operation modes, advantages, and limitations of SSPC/ SSCB technology are explained.

Chapter 3 proposes a constant current precharging algorithm for SSPCs/ SSCBs. The details of the proposed algorithm and derivation of various key parameters, are presented in this chapter. The proposed algorithm is verified using hardware setup. Experimental results obtained using this setup are illustrated and discussed.

Chapter 4 proposes a constant temperature precharging algorithm for SSPCs/ SSCBs. The flowchart of the proposed algorithm is presented and explained in this chapter. Experimental results for verification of the proposed control strategy are also presented.

Chapter 5 proposes two SCR-based SSPC/ SSCB topologies. Operation modes of these topologies, mathematical analysis and derivations, and simulation and experimental results are presented in this chapter.

Chapter 6 is the final chapter of this thesis. Conclusion of the research work and recommendations for future research are presented in this chapter.

Chapter 2

Literature Review

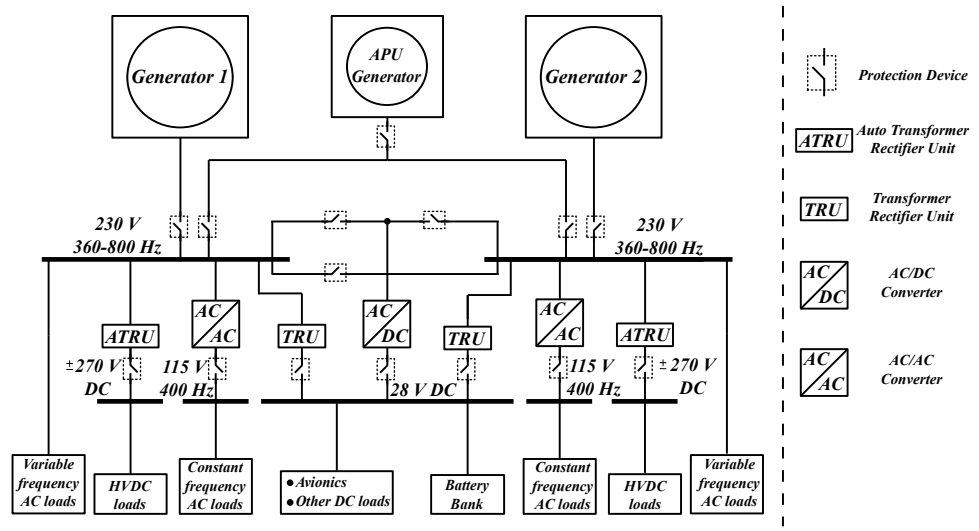
This chapter presents a review of emerging and existing technologies in this field. The architecture of MEA is discussed, followed by an overview of switchgear and protection devices. Thereafter, power semiconductor devices and associated SSPC/ SSCB topologies are presented. Subsequently, precharging methods for SSPCs/ SSCBs are explained. Advantages and limitations of these technologies and topologies are also discussed in this chapter.

2.1 More Electric Aircraft Technology

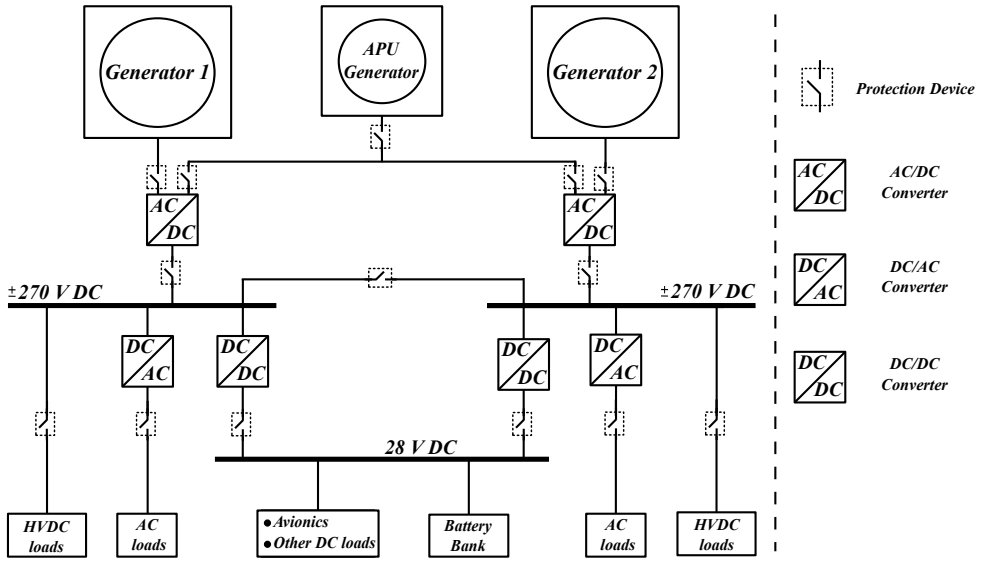
Conventional aircraft are evolving towards MEA. There are two main reasons behind this trend. The first reason is that MEA emits less greenhouse gases, thus, these are less polluting. The second reason is the financial benefit associated with the MEA. These have high efficiency, reduced weight, extended control, and less maintenance requirements [3, 4, 25, 31–34]. Bleedless architecture of MEA enable reduction in fuel consumption by up to 2% [4]. These advantages results in monetary benefit for stakeholders.

In MEA, electrical systems are utilized for various tasks which are fulfilled by mechanical, pneumatic, and hydraulic systems in conventional aircraft. Thus, the electrical power generation capacity is increased by two to four times compared to conventional aircraft [35]. This increase in power generation capacity necessitates modification of the conventional architecture, in order to efficiently utilize the generated electric power. Several MEA architectures are studied in the literature [3]. The two promising MEA architectures are shown in Fig. 2.1(a) and (b). Compared to the

Hybrid HVac/ HVdc architecture (Fig. 2.1(a)), the HVdc architecture (Fig. 2.1(b)) has a wider region of stable operation [3]. In aerospace applications, voltage range of HV category is different from other applications, and lower limit of the range is 135 V. These architectures have a 270-V dc bus, which is not available in conventional aircraft. This change is driven by the advantages offered by dc grids [9, 10, 36–41]. The dc architectures require a lower number of conductors compared to ac grids, thus, the wiring-system weight is reduced. Due to the absence of reactive power flow, and no skin effect, conductor cross-sectional area is less. It is easier to integrate asynchronous systems, battery energy storage systems, and fuel cells. Despite the above-mentioned advantages, fault isolation in dc grids is highly challenging due to the absence of current zero-crossing [36].



(a)



(b)

Figure 2.1: (a) Hybrid HVac/ HVdc and (b) HVdc MEA architectures [3, 4].

In ac grids, MeCBs contribute towards the major portion of switchgear. During fault condition, metal contacts of MeCB are separated after a tripping command is initiated by the controller. The arc formed across the metal contacts is automatically extinguished owing to the periodic current zero-crossing in ac systems. Such MeCBs cannot be directly used for protection of dc grids in MEA. These require additional bulky auxiliary circuits [9]. Moreover, MeCBs have slow response time [10], which can lead to catastrophic failure due to very high fault current ramp rate in dc systems. In addition, MeCBs have limited dc fault current breaking capability [42]. Hence, semiconductor-based SSPCs/ SSCBs and hybrid circuit breakers (HCBs) are a promising solution to realize fault isolation in dc grids [9, 10, 34]. HCBs are designed using a combination of MeCBs and SSPCs/ SSCBs to achieve operational advantages of both, i.e., low conduction loss and fast fault isolation. However, response time of HCBs is limited to the range of few ms due to moving contacts [9]. Hence, SSPCs/ SSCBs are preferred in applications requiring submillisecond operating speed range [8–10,12–16]. SSPCs/ SSCBs are controlled using low voltage signals, and require no moving parts, thus, the response time of these protection devices is fast. Moreover, no arc is formed during the fault isolation process. These protection devices are thoroughly discussed in the next section. The modes of operation of these devices, are also explained in detail.

2.2 Switchgear and Protection Devices

In this section, operating principle, advantages, and disadvantages of four main types of switchgear and protection devices (fuses, MeCBs, SSPCs/ SSCBs, and HCBs), are discussed.

Switchgear and protection devices/ fault isolation devices are broadly classified into four categories, fuses, MeCBs, SSPCs/ SSCBs, and HCBs, as shown in Fig. 2.2. The main job of these devices is to protect the system by isolating the fault and, in some cases, by suppressing the current and voltage transients.

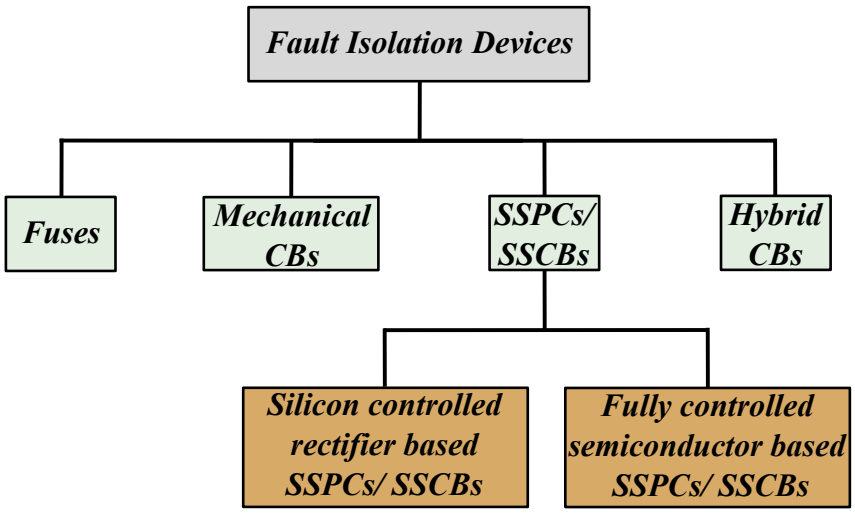
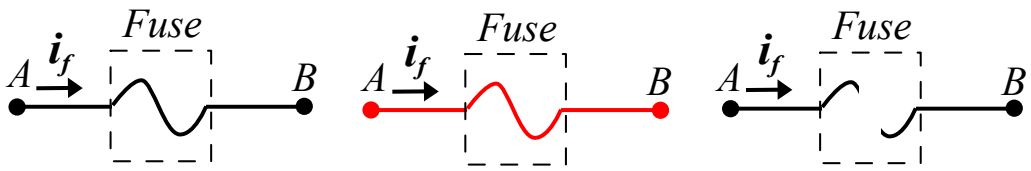


Figure 2.2: Classification of fault isolation devices.

Fuses are simple, low cost, and easy-to-use protection device. A fuse is made up of a wire and is connected in series in the circuit, as shown in Fig. 2.3(a). It has a rated value of current specified in the datasheet, beyond this value the fuse-wire starts melting. In case of steady state condition, it carries the full load current, as shown in Fig. 2.3(b). It is selected in such a way that its current rating is more than the full load current. In case of overcurrent/ fault condition, fuse-wire melts to isolate the faulty section, as shown in Fig. 2.3(c). The time required for the fuse-wire to completely melt is dependent on the overload value. There are two main limitations of fuses. The first limitation is that their characteristics varies with temperature. The second limitation is that the melted fuse-wire is replaced manually due to which the system downtime is large. In order to address these issues, fuses are used in conjunction with other protection devices.



(a) (b) (c)

Figure 2.3: Modes of operation of fuse: (a) off state, (b) steady state, and (c) fault state.

MeCBs are used in almost all ac power distribution architectures. There are various types of MeCBs available in the market such as thermal switches, molded case CBs, insulated case CBs, and power CBs [43]. CB panel in Boeing 737 (conventional

aircraft) is shown in Fig. 2.4, MeCBs are the main protection devices in this aircraft. MeCBs have two metal contacts, moving and fixed contact. During the off state, these contacts have physical separation between them, as shown in Fig. 2.5(a). In order to connect the source and load side, these metal contacts are joined together using force, shown in Fig. 2.5(b). During fault condition, these contacts are separated to isolate the faulty section from the healthy system, as shown in Fig. 2.5(c). Arc is formed across the contacts due to the inductance in the current path. This arc is naturally extinguished owing to periodic current zero-crossings in ac system. However, there are many limitations of MeCBs in dc grids [5, 9, 10, 12, 13]. Response time is slow due to moving contacts, which can cause very high fault current magnitudes. In addition, an auxiliary circuit is required for arc quenching. Moreover, maintenance requirements are high due to oxidization of contacts. In order to address these issues, semiconductor-based SSPCs/ SSCBs and HCBs have recently gained attention and are considered as a promising solution for protection of dc grids.

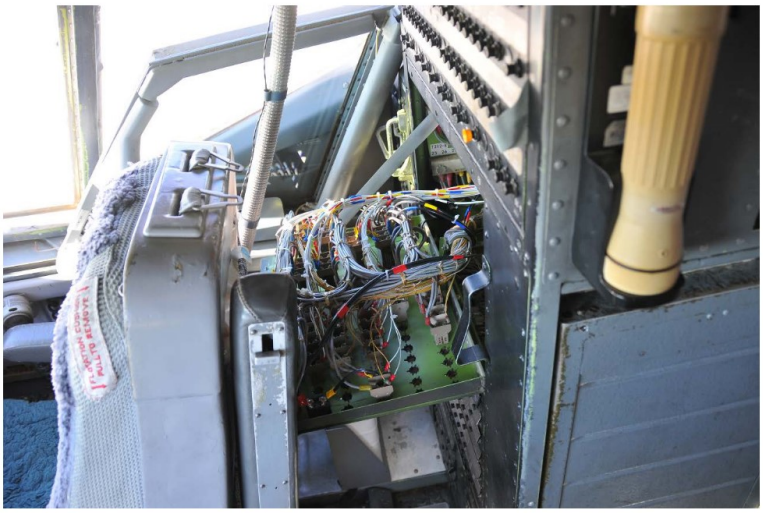
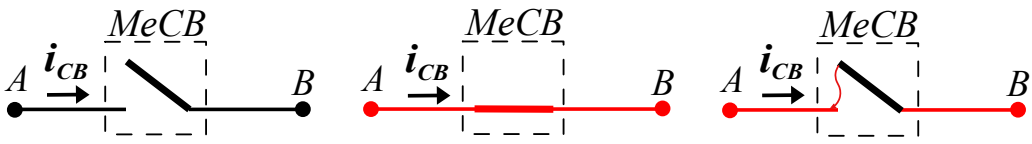


Figure 2.4: CB panel in Boeing 737 [5].



(a) (b) (c)

Figure 2.5: Modes of operation of MeCB: (a) off state, (b) steady state, and (c) fault state.

Structure of HCB is illustrated in Fig. 2.6(a) [11]. It consists of an ultra-fast

disconnector (UFD), load commutation switch (LCS), main breaker branch, and clamping circuit. UFD and main breaker are designed to sustain the maximum voltage across the CB. LCS is a low voltage switch, which is designed in such a way that it is able to carry the fault current. During off state, UFD is open circuit and semiconductor devices gated low. During steady state, UFD and LCS carry the full load current, as shown in Fig. 2.6(b). In case of fault condition, main breaker is gated high and thereafter, LCS is gated low. Consequently, fault current flows through the main breaker, as shown in Fig. 2.6(c). The contacts of the UFD are separated to regain voltage withstand capability, illustrated in Fig. 2.6(d). Once the contacts are fully apart, the main breaker is gated low and thus, the current is diverted to the clamping circuit, shown in Fig. 2.6(e). The clamping circuit opposes the flow of current, as a result, the current drops to zero. Hence, the faulty section is electrically isolated from the healthy system. HCBs are faster than MeCBs, however, HCBs have higher power loss due to the presence of LCS in the load current path. Due to moving contacts, the operating speed of an HCB is in the range of few millisecond. Sub-millisecond response time is achievable by making use of SSPCs/ SSCBs. Structure of SSPC/ SSCB is similar to HCB. It has main breaker and clamping circuit, however, it does not have UFD and LCS. Semiconductor devices in the main breaker branch are utilized for both the main tasks, carrying the load current as well as for fault current breaking. However, losses of SSPCs/ SSCBs are more than HCBs due to the presence of high voltage semiconductor devices in the load current conduction path.

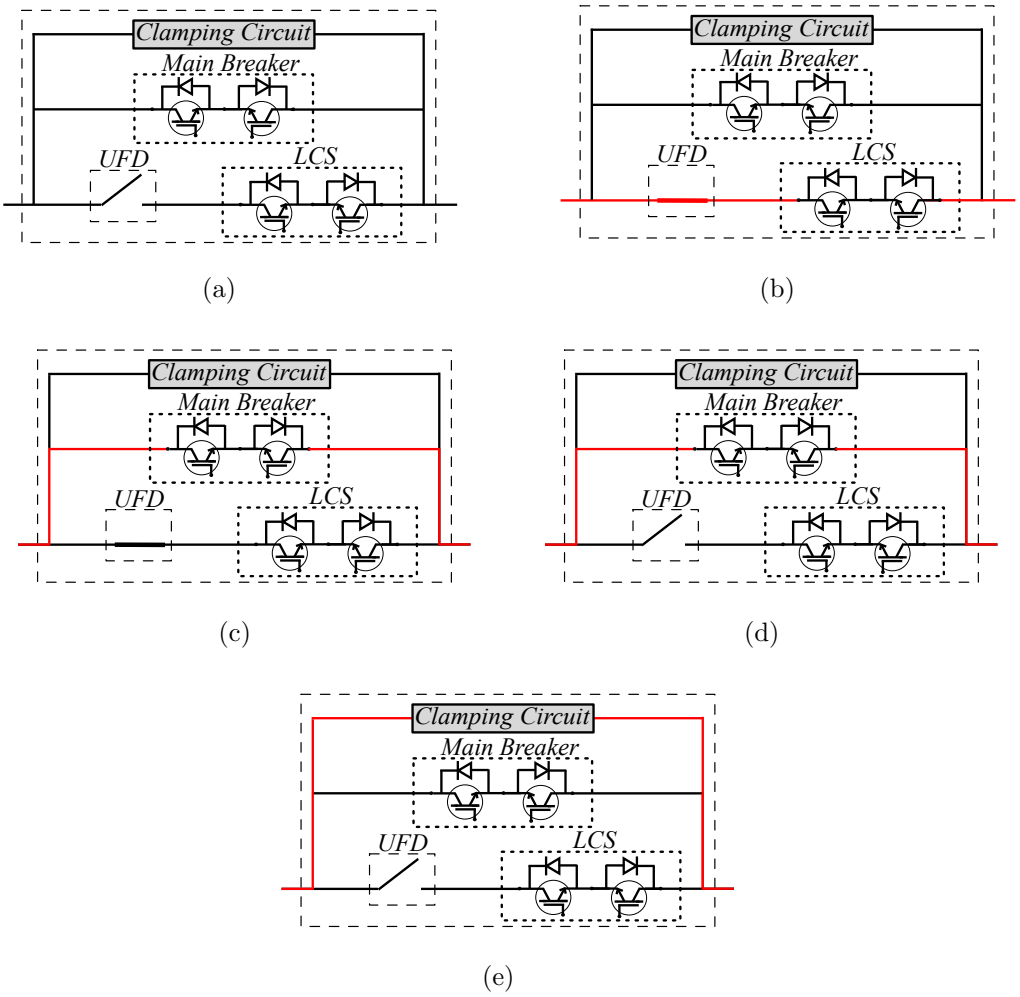


Figure 2.6: Modes of operation of HCB: (a) off state, (b) steady state, (c) transfer of current from LCS branch to main breaker branch, (d) contacts separation of UFD, and (e) clamping state.

A detailed comparison of MeCBs, SSPCs/ SSCBs, and HCBs, is illustrated in Table 2.1. The key points are discussed as follows,

- The response times of SSPCs/ SSCBs are fastest because semiconductor devices are the main switching elements. HCBs and MeCBs have relatively slow response time due to the presence of moving contacts.

- On state power loss is higher in the case of HCBs and SSPCs/ SSCBs, than MeCBs, due to the presence of semiconductor devices in the load current path. HCBs have low voltage semiconductor devices in the load current path. Low voltage semiconductor devices have lower on state voltage drop than high voltage semiconductor devices, thus, HCBs have lower on state power loss than SSPCs/ SSCBs.

- MeCBs and UFDs generate high audible-noise while switching from off state to on state and vice-versa. SSPCs/ SSCBs generate low audible-switching-noise because semiconductor devices do not require physical isolation for changing state.

- Semiconductor devices are controlled using low voltage gating signals, these signals are easily corrupted by noise in the system. On the other side, mechanical switches have high noise margins because these are controlled using relatively high voltage. Hence, MeCBs have higher noise tolerance compared to SSPCs/ SSCBs and HCBs.

- MeCBs and UFDs are affected by external vibrations. Large amplitude vibration can lead to sudden disconnection of load, and consequently, arcing in between the contacts. SSPCs/ SSCBs are not vibration sensitive.

- MeCBs are utilized for opening the load circuit as well as for fault current isolation. An arc is formed across the contacts at each of these switching instants. This arc has a detrimental impact on the breaker as well as on the system components. UFDs do not break the current flow, and are operated only after the current is completely transferred to the main breaker branch. Thus, HCBs produce no or minimal arc during fault isolation. In case of SSPCs/ SSCBs, fault isolation is carried out by semiconductor devices because of which no arc is formed during the process.

- MeCBs have a limited number of cycles of operation because of the arcing phenomena. The arc causes the metal contacts to degrade and hot-spots are formed on the surface. The contact resistance also increases with the increase in the number of completed cycles. The impact of current breaking on semiconductor devices is not as significant as in case of metal contacts. Thus, SSPCs/ SSCBs have higher number of cycles of operation compared to MeCBs.

- MeCBs have been used in industry for many years, their standards and manufacturing capabilities are well established. HCBs and SSPCs/ SSCBs are relatively new technologies and their standards are currently under development.

Table 2.1: Comparison of MeCBs, SSPCs/ SSCBs, and HCBs [5, 8–18]

	MeCBs	SSPCs/ SSCBs	HCBs
Response time	Slow	Fast	Medium
Power loss	Low	High	Medium
Acoustic switching noise	High	Low	High
Noise tolerance	High	Low	Low
Cost	Low	High	Very high
Thermal conductivity	High	Low	Low
Reliability	Low	High	Low
Moving parts	Yes	No	Yes
Vibration sensitive	Yes	No	Yes
Arcing during fault isolation	Yes	No	No
Well established industry standards	Yes	No	No

The points discussed above clearly indicate that SSPC/ SSCB technology is an attractive solution for protection of dc grids. This is the main motivation for conducting research in this area. The contributions of this thesis are in the field of SSPC/ SSCB technology.

2.3 Solid-State Power Controllers/ Solid-State Circuit Breakers

A general structure of SSPC/ SSCB is shown in Fig. 2.7(a). It has semiconductor devices, which conducts the load current and in addition, breaks the fault current. These semiconductor devices are switched using gate driver and controller. The controller measures the voltage and current of various nodes and branches, and depending on these inputs, takes the appropriate action. The main role of clamping circuit is to prevent the voltage across the device from reaching unsafe levels by clipping high voltage transient [9, 10, 16–18, 44]. A precharging circuit is used for controlled charging of load capacitor [8, 14–16].

Different modes of operation of SSPCs/ SSCBs are illustrated in Fig. 2.7. These modes are explained as follows,

- During the off state, the semiconductor devices are electrically non-conductive. Thus, the source and load sides are electrically isolated from each other.

- In the case of capacitive loads, an intermediate precharging state is required because the capacitors associated with the load are initially at zero voltage potential. Direct connection of source and uncharged capacitor causes high peak current and voltage transient, which has detrimental impact on the breaker as well as on the system components. One of the main tasks of SSPC/ SSCB is to charge the capacitor in a controlled manner. Several precharging methods for SSPCs/ SSCBs have been proposed in the literature. Some of these methods require an additional circuit, which is connected in parallel with the semiconductor devices, as shown in Fig. 2.7(b). While the other remaining methods utilize the main semiconductor device for precharging. These precharging methods are discussed in detail in Section 2.3.3. In case of resistive and inductive loads, and for tie SSPC/ SSCB, this intermediate state is not required.

- Once the capacitor is completely charged, the semiconductor devices are switched from the off state to the on state, by applying appropriate gate-source voltage. During steady state, the semiconductor devices conduct the full load current, as shown in Fig. 2.7(c).

- In case of fault condition, the current and voltage values deviate from their steady state values. The controller detects the fault by using these current and voltage measurements, and initiates a tripping command. An appropriate voltage is applied across the gate & source terminals of the semiconductor device to change its state from the on state to the off state. The current is diverted to the clamping circuit, as shown in Fig. 2.7(d). This circuit forces the current to zero and, at the same time, ensures that the voltage across the semiconductor device is within safe limits. Consequently, isolating the faulty section from the healthy system.

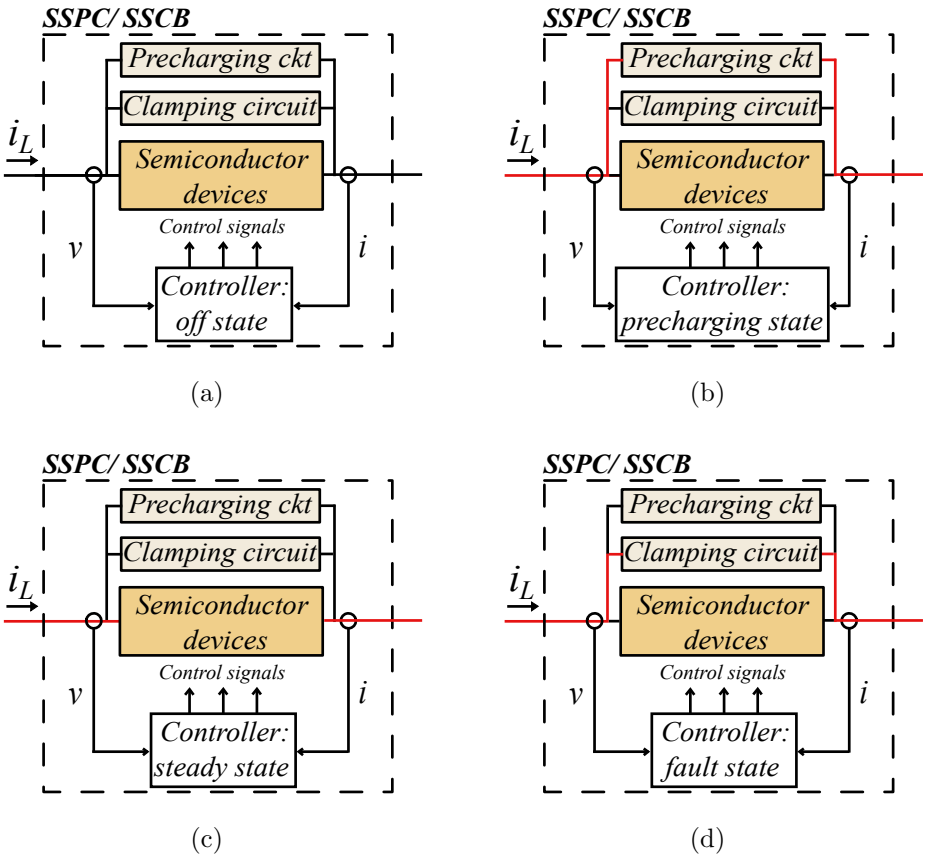


Figure 2.7: Modes of operation of SSPC/ SSCB: (a) off state, (b) precharging state[1], (c) steady state, and (d) fault state.

[1] This state is required only for capacitive loads.

2.3.1 Power Semiconductor Devices

In this section, some of the most commonly used power semiconductor devices for SSPC/ SSCB technology are discussed. Principle of operation, advantages, and limitations of these devices, are briefly explained.

A broad classification of power semiconductor devices is shown in Fig. 2.8. The most commonly used power semiconductor devices are field effect transistors (FETs), insulated gate bipolar transistors (IGBTs), and thyristors [8–10,16,45]. FETs, as the name suggests, are voltage controlled unipolar devices. The FET's channel width is dependent on the gate voltage. These are further divided into Si, SiC, and GaN FETs, based on material properties. In on-state, these are represented as a resistor ($R_{DS(on)}$). They are widely used for low current applications due to the absence of PN junction knee voltage. The $R_{DS(on)}$ value increases very drastically with the increase in device voltage, because of which, Si FETs are suitable for low voltage and current applications [10]. Wide bandgap (WBG) semiconductor based FETs have benefits

over Si FETs [9, 10]. Compared to Si FETs, SiC FETs of similar ratings have lower value of $R_{DS(on)}$. GaN FETs have lower $R_{DS(on)}$ than SiC FETs.

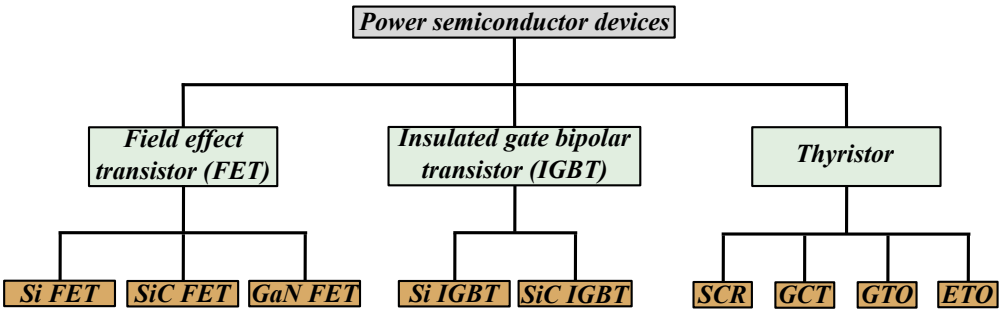


Figure 2.8: Classification of power semiconductor devices.

IGBTs, as the name suggests, are bipolar transistors, implying that the current conduction path is composed of majority as well as minority carriers. Due to this property, IGBTs offers low resistance to current flow. They are represented as a voltage source (V_{CE}) in series with a resistor (R_{CE}). The power dissipated by the IGBT follows the expression, $p_d = i_d^2 R_{CE} + i_d V_{CE}$. Due to V_{CE}, the power dissipated by the IGBT is more than the FET for low values of current. However, for high values of current, the IGBT has lower power loss. Compared to FETs, IGBTs have higher short-circuit current handling and breaking capability. SiC IGBTs have pushed the limits of Si IGBTs, as these have lower power loss and are available in the market for higher voltage ratings.

Thyristors are being used in industry for a very long time. Silicon controller rectifier (SCR) belongs to thyristor family and these are being used for converter applications. SCR-based SSPCs/ SSCBs have recently gained popularity in the research community and industry [10]. The SCR is a unidirectional and half-controlled semiconductor device, implying that only the turn on of the SCR is gate-controlled. In order to turn off the SCR, the current is forced to zero and a negative voltage is imposed across the device for a time interval greater than the turn-off time specified in the datasheet. During this time interval, the SCR undergoes the reverse recovery of charge carriers. Compared to IGBTs, SCRs have lower on-state losses [9], superior current handling capability [9, 10, 46], and lower cost [9, 10]. Unlike the SCR, gate commutated thyristor (GCT), gate turn-off thyristor (GTO), and emitter turn-off thyristor (ETO) are fully-controlled, implying that both the turn-on and turn-off of these devices are gate-controlled. However, the on-state power loss of these devices is more than SCRs [9]. A summary of the features and limitations of FETs, IGBTs,

and SCRs, is presented in Table 2.2.

Table 2.2: Key Features and Limitations of FETs, IGBTs, and SCRs

	Key Features	**Limitations**
FETs	• FETs are unipolar devices. • Due to the absence of PN junction knee voltage, the power loss in the case of low value of current is lower than other semiconductor devices.	• On state resistance value increases very drastically with the increase in device breakdown voltage.
IGBTs	• IGBTs are bipolar transistors. • In the case of high value of current, power loss is lower than FETs, and higher than SCRs. • Short-circuit current handling and breaking capability is higher than FETs, and lower than SCRs.	• Power dissipated by the IGBTs is more than FETs for low value of current. This is because of the PN junction knee voltage.
SCRs	• SCRs are bipolar devices. • Compared to IGBTs, SCRs have lower on-state losses, superior current handling capability, and lower cost.	• SCR is a half-controlled semiconductor device. In order to turn off the SCR, an auxiliary circuit is required.

In Chapters 3 and 4, the FET is considered because it is widely used for MEA application due to the absence of PN junction knee voltage [8–10, 12, 13, 15, 16, 45]. However, the algorithms proposed in these chapters, are applicable to any semiconductor device with similar operating characteristics in the saturation region.

The SCR has recently gained attention in the research community [6, 7, 47–55]. SCR-based SSPCs/ SSCBs are considered a promising technology for protection of high current loads [9, 10]. In Chapter 5, SCR-based SSPC/ SSCB topologies are proposed for the interconnection and protection of two electrical buses in MEA. This

type of SSPC/ SSCB is referred to as tie SSPC/ SSCB.

2.3.2 SSPC/ SSCB Topologies

SSPC/ SSCB topologies are broadly divided into two categories based on the nature of power semiconductor device, as shown in Fig. 2.9. As discussed in the previous section, the SCR is a half-controlled semiconductor device. Thus, in case SCR-based SSPCs/ SSCBs, the on state is achieved by using gating signals. However, these have special configurations to enable forced commutation of SCRs. SSPCs/ SSCBs based on other power semiconductor devices fall under the category of fully controlled semiconductor (FCS)-based SSPCs/ SSCBs. In case of FCS-based SSPCs/ SSCBs, both on and off states of the semiconductor devices are achieved by using gating signals. A summary of the features and limitations of FCS-based SSPCs/ SSCBs and SCR-based SSPCs/ SSCBs, is presented in Table 2.3. In aircraft applications, weight, size, and volume are very important parameters. Heat sink is one of the main contributors towards these parameters [56]. Heat sink weight and size is dependent on the power loss. Thus, low on-state power loss is one of the desirable properties of SSPCs/ SSCBs.

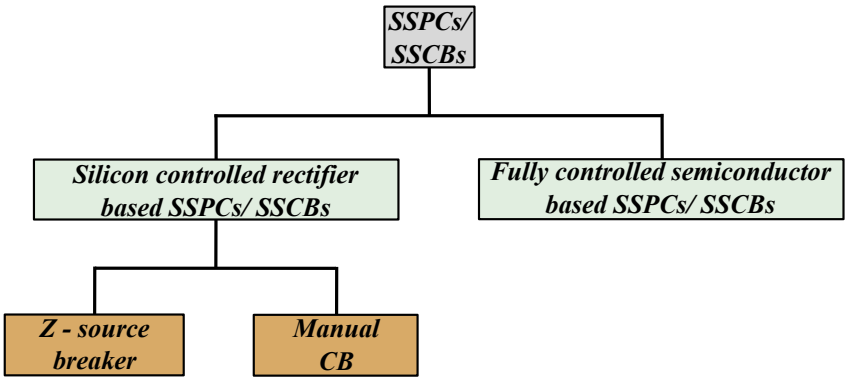


Figure 2.9: Classification of SSPCs/ SSCBs.

Table 2.3: Key Features and Limitations of FCS-Based SSPCs/ SSCBs and SCR-Based SSPCs/ SSCBs

	Key Features	**Limitations**
FCS-based SSPCs/ SSCBs	• On and off states of the SSPCs/ SSCBs are achieved by regulating the gate voltage. • Fast response time.	• High on-state power loss.
SCR-based SSPCs/ SSCBs	• In the case of high current value, on-state power loss is lower than FCS-based SSPCs/ SSCBs.	• Turn-off of the SCRs requires special consideration.

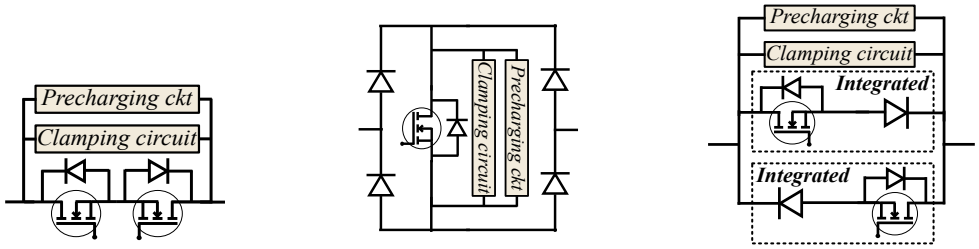
FCS-based SSPC/ SSCB Topologies

Most commonly used FCS-based SSPC/ SSCB topologies are anti-series, diode-bridge, and anti-parallel [10, 13, 16, 57], illustrated in Fig. 2.10. FETs are considered for illustration purpose, however, any FCS device is a valid choice.

As the name suggests, anti-series topology has two FCS devices connected in mirrored configuration, as shown in Fig. 2.10(a). During steady state, one FCS device and one diode are in the load current path. The main advantage of this topology is that it requires only one gate driver for both FCS devices.

The diode-bridge topology has one FCS device and four diodes, as shown in Fig. 2.10(b). Two diodes and one FCS device are in the load current path, thus, the power loss is higher than the anti-series topology. However, the diode-bridge topology has a lower number of FCS devices compared to the anti-series topology.

The anti-parallel topology is shown in Fig. 2.10(c). This type of configuration is used for FCS devices/ modules with reverse blocking capability. This topology has one FCS device and one diode in the load current path, thus, the power loss of this topology is comparable to the anti-series topology and is lower than the diode-bridge topology. However, this topology requires a larger number of gate drivers compared to the anti-series topology.



(a) (b) (c)

Figure 2.10: (a) Anti-series, (b) diode-bridge, and (c) anti-parallel SSPC/ SSCB topologies.

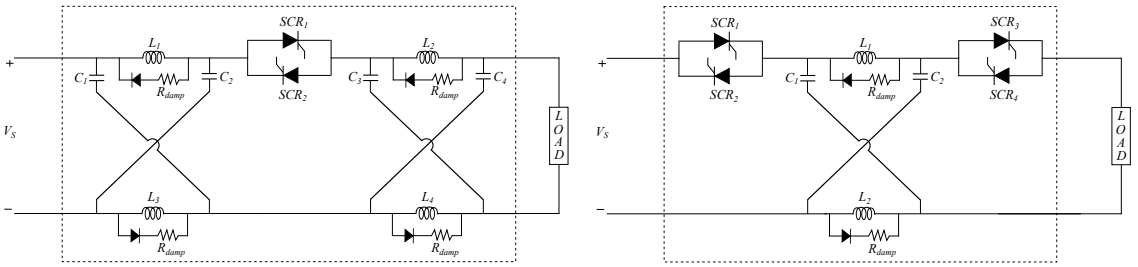
SCR-based SSPC/ SSCB Topologies

SCR-based SSPC/ SSCB topologies are broadly divided into two categories on the basis of operating principle, as shown in Fig. 2.9. ZSBs are emerging SCR-based SSPC/ SSCB topologies [9, 10, 47–49, 51–53, 58–69]. ZSBs have inductors and capacitors arranged in such a way that a shortcircuit fault is automatically isolated. The other category, manual CBs require an external tripping command, similar to conventional CBs. These topologies (precharging circuit is not shown in the circuit diagram) are discussed as follows,

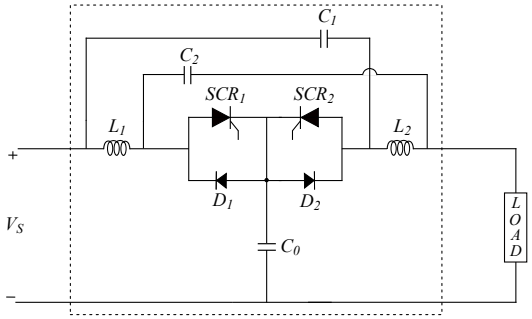
1. Bidirectional ZSB Topologies

   ZSB topologies have SCRs as the active components and, inductors and capacitors as the passive components. These passive components enable autonomous shortcircuit fault protection.

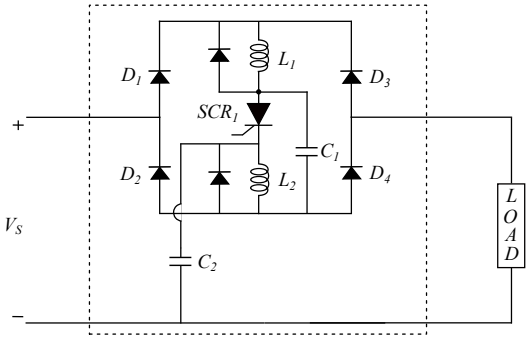
   Classical bidirectional ZSBs are proposed in [66, 67], shown in Fig. 2.11(a). These are able to automatically isolate source and load sides in case of fault. Due to fast and self-triggered protection, the control complexity is less. However, they have inductors in the return path, due to which negative terminals of source and load are not connected. Thus, they are not applicable for protection of those electrical networks which have a common ground.



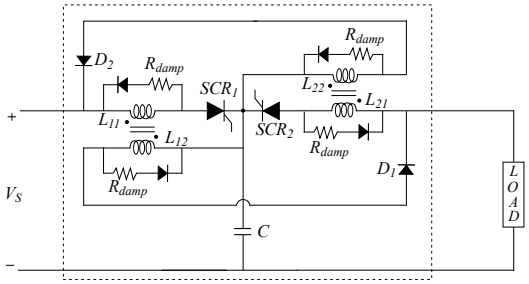
(a)



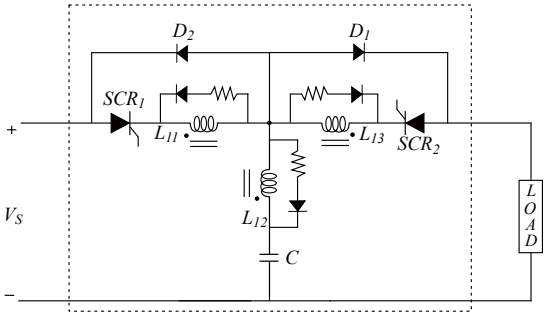
(b)



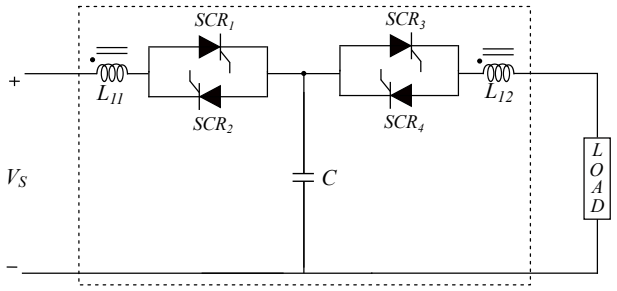
(c)



(d)



(e)



(f)

Figure 2.11: (a) Classical bidirectional ZSB topologies [66, 67], (b) ZSB-based fault current limiter and interrupter (FCLI) [68], (c) bidirectional series ZSB [69], (d) bidirectional ZSB (coupled inductor) [53], (e) three winding ZSB [49], and (f) modified bidirectional ZSB [48].

ZSB-based fault current limiter and interrupter (FCLI) was proposed in [68], shown in Fig. 2.11(b). This topology has no component in the return path, because of which it is suitable for architectures which have same ground for source and all loads. The modes of operation of this topology are explained as follows,

- During steady-state operation, depending on the current flow direction, one of the SCRs (SCR_1 or SCR_2) and diodes (D_2 or D_1) conduct to supply the load current, while inductors (L_1 and L_2) and capacitors (C_0, C_1 and C_2) behave as short circuit and open circuit elements, respectively. To facilitate the analysis, the current is assumed to flow through the path $V_s - L_1 - SCR_1 - D_2 - L_2$.
- During a fault condition, the source and capacitors supply the fault current through the high-frequency low-impedance path ($C_0 - SCR_1 - C_2$ and $V_s - C_1 - D_2 - SCR_1 - C_2$), opposing the original steady-state current flow through SCR_1. SCR_1 commutates naturally after the current through it reaches zero.
- During the post commutation stage, source (V_s), capacitors (C_0, C_1 and C_2), inductors (L_1 and L_2), and fault conductance resonate. Post resonance, the fault is isolated with the capacitors C_1 and C_2 charged to the source voltage.

A bidirectional series ZSB topology is shown in Fig. 2.11(c) [69]. The operating principle of all ZSB topologies is the same, however, the high-frequency low-impedance path is different. $C_2 - SCR_1 - C_1 - D_4$ is the high-frequency low-impedance path in this case. This topology has a lower number of SCRs and capacitors compared to FCLI. However, it has a higher number of semiconductor devices in the load current path, due to which the power loss is higher than FCLI.

Simple inductors are used in the topologies discussed until this point. Coupled inductor based ZSB topologies are discussed in the remaining part of this subsection. A bidirectional ZSB (coupled inductor) topology is proposed in [53], and is illustrated in Fig. 2.11(d). This topology has a lower number of capacitors compared to the previously discussed topologies. The modes of operation of this topology are explained as follows,

- During steady-state operation, depending on the current flow direction, one of the SCRs (SCR_1 or SCR_2) and diodes (D_1 or D_2) conduct to supply the load current. Inductors (L_{11} and L_{12}) and capacitor behave as short-circuit and open-circuit elements, respectively. To facilitate the analysis, the current is assumed to flow through the path $V_s - L_{11} - SCR_1 - L_{12} - D_1$.
- During fault condition, the capacitor supplies the fault current through the high-frequency low-impedance path ($C - L_{12} - D_1$). This transient current in L_{12} induces current in L_{11} opposing the original steady-state current flow through SCR_1. After the current through the SCR_1 reaches a value lower than the holding current, it commutates naturally.
- During the next interval, capacitor C, L_{12}, and fault conductance resonate. The diode across the inductor starts conducting once the voltage across it changes polarity, dissipating the remaining energy stored in the inductor.

A ZSB topology with three coupled windings is proposed in [49], shown in Fig. 2.11(e). The operating principle of this topology is similar to the previous topology (Fig. 2.11(d)). However, the high-frequency low-impedance path is different. This topology has simplified structure and a lower number of components compared to the previous case. This is achieved by coupling more windings.

A modified version of bidirectional ZSB (coupled inductor) topology is proposed in [48], shown in Fig. 2.11(f). This topology has a lower number of magnetic structures compared to the bidirectional ZSB (coupled inductor) and three winding ZSB. However, it requires a higher number of SCRs. In addition, this topology is constrained to have equal value of inductance for both inductors, in order to preserve bidirectional symmetricity.

The topologies discussed in this section, have complex structure and a high number of components in the load current path. In **Section 5.1 of Chapter 5**, a novel coupled-inductor-based bidirectional ZSB (CI-BZSB) topology is proposed. The proposed topology has a simple structure and only one semiconductor device in the load current path. In addition, the proposed topology is symmetric even with unequal values of inductors.

2. Manual CB Topologies

As discussed in the previous section, ZSBs have automatic mechanism and the value of tripping current is dependent on the value of passive components. Due to automatic mechanism, the faulty section is quickly isolated from the healthy system. However, it poses a major challenge in designing its coordination in an interconnected architecture. In addition, transients and step-load changes of high magnitude cause false tripping of the ZSB [9]. To overcome these limitations, active SCR-based SSPC/ SSCB topologies have been proposed in the literature, these are trigged using an external command, similar to conventional CBs.

In [6], an SCR-based active SSPC/ SSCB topology is proposed, shown in Fig. 2.12(a). During steady-state operation, depending on the current flow direction, one of the main SCRs (T_{m1} or T_{m2}) conducts to supply the load current. To explain further, the steady-state current is assumed to flow through the device T_{m1}. The commutation capacitor (C_{b1}) is charged through the path $V_s - T_{m1} - C_{b1} - R_{c1}$. During fault condition, T_{b1} is triggered to initiate the fault isolation process. C_{b1} creates a negative voltage across T_{m1} and opposes the current flow through T_{m1}. The current through T_{m1} reaches a value less than the holding current and it commutates naturally. Thereafter, C_{b1} and line inductor resonate until C_{b1} is charged to a value equal to the breakdown voltage of the MOV. Consequently, the MOV starts conducting and it opposes the flow of current. After a short while, the current reaches zero and thus, the faulty side is electrically isolated from the healthy system. This topology has a reliable triggering mechanism. However, it cannot provide reclosing functionality. This is because the bypass capacitor (C_{b1} or C_{b2}), which is used for commutating the respective main SCR (T_{m1} or T_{m2}), is charged only when the main SCR is conducting. Hence, reclosing to a permanent fault leaves the fault uncleared.

An SSPC/ SSCB topology having reclosing/ operating duty functionality is proposed in [7], shown in Fig. 2.12(b). This topology has this capability because the capacitor is charged directly from the source and independent of the load. However, the current and voltage stress on the breaker and system components, during reclosing is high. This is because source and faulty side are directly connected in case of normal reclosing.

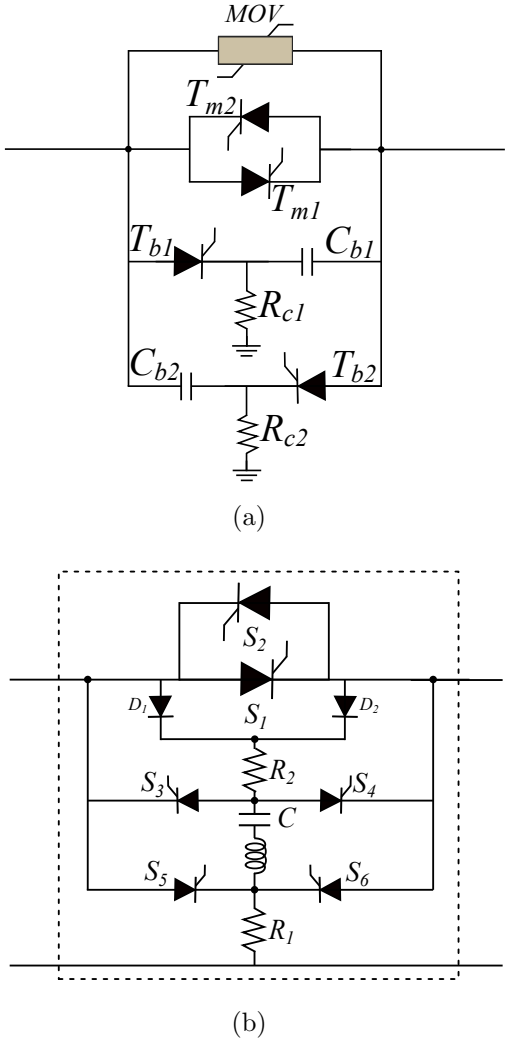


Figure 2.12: SCR-based (a) active SSPC/ SSCB [6] and (b) SSPC/ SSCB (operating duty functionality) [7].

In **Section 5.2 of Chapter 5**, a novel SCR-based SSPC/ SSCB topology is proposed. This topology has soft reclosing functionality, which helps in reducing stress on semiconductor devices, capacitors, surge suppression devices, and current feeding components. The TVS diode heat loss during reclosing is negligible. Moreover, a higher number of reclosing attempts is possible compared to the normal reclosing strategy.

2.3.3 Precharging Methods for SSPCs/ SSCBs

Precharging/ soft-start functionality is required for SSPCs/ SSCBs, which are connected to the capacitive loads. The equivalent circuit of a dc subsystem in an aircraft is shown in Fig. 2.13. V_s represents a dc bus or output of a ac/dc converter.

The SSPC/ SSCB is connected in series with the source and load. L_μ and R_μ are the line inductor and resistor, respectively. C_L is the capacitor associated with the power electronic converter.

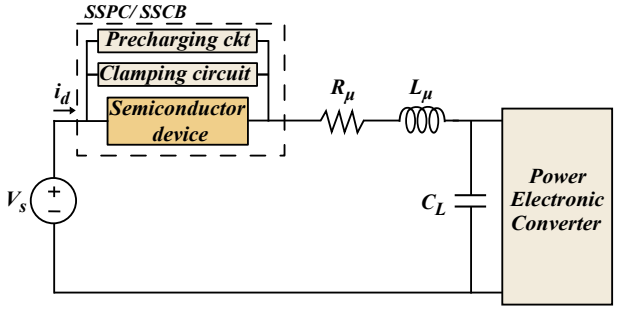


Figure 2.13: Equivalent circuit of a subsystem in an aircraft.

Initially, C_L is completely discharged. The direct connection of V_s and C_L causes high inrush current, resulting in voltage oscillation at various nodes. Fig. 2.14 shows simulation results of uncontrolled charging of capacitor. The parameter values for the simulation are: $V_s = 270$ V, $L_\mu = 18.48$ μH, $R_\mu = 70$ mΩ, and $C_L = 500$ μF. Using Kirchhoff's voltage law, the variation in current with time can be calculated as,

$$i_c(t) = \frac{V_{in}}{L_\mu \omega} \sin(\omega t)\, e^{-\alpha t} \tag{2.1}$$

where,

$$\alpha = \frac{R_\mu}{2L_\mu} \tag{2.2}$$

$$\omega = \sqrt{\frac{1}{L_\mu C_L} - \left(\frac{R_\mu}{2L_\mu}\right)^2} \tag{2.3}$$

Differentiating (2.1), the time instant at which the peak value of $i_c(t)$ occurs, can be calculated as,

$$t_p = \frac{\tan^{-1}(\gamma)}{\omega} \tag{2.4}$$

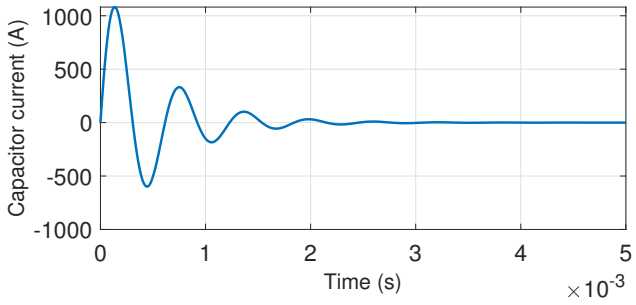
where,

$$\gamma = \frac{\omega}{\alpha} \tag{2.5}$$

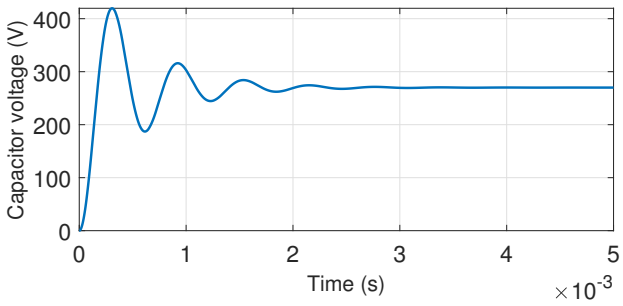
Substituting (2.4) in (2.1), the peak value of $i_c(t)$ can be calculated as,

$$I_{c\,max} = \frac{V_{in}}{L_\mu \omega}\left(\sin\left(\tan^{-1}(\gamma)\right)e^{-\alpha\frac{\tan^{-1}(\gamma)}{\omega}}\right) \tag{2.6}$$

High peak value oscillations results in high stress on the semiconductor devices and current feeding components, which may lead to circuit or system failures. Moreover, oversizing the components might also be required in some cases. The main objective of the precharging methods is to mitigate or suppress these oscillations.



(a)



(b)

Figure 2.14: Simulation results of uncontrolled charging of capacitor.

Several precharging methods for SSPCs/ SSCBs have been proposed in the literature. These precharging methods are broadly classified into two categories. In the first category, an additional precharge circuit is connected in parallel with the main semiconductor device [14,15]. The main limitation of these methods is that the additional precharge circuit adds to the weight, size and cost of the system. In the second category, the main semiconductor device is utilized for precharging [8, 16], instead of additional circuitry as in the previous case. These two categories of precharging methods are discussed in detail next.

Precharging using Additional Circuit

In this section, precharging methods, which fall under the first category, are discussed. In these methods, a precharging circuit is connected in parallel with the main semiconductor device, which is used for charging the load capacitor. R+SW and buck converter methods fall under this category, and are explained in detail as follows,

1. R+SW Method

   This method is widely used in industry [14,70]. The precharging circuit is integrated by a resistor (R_{pc}) connected in series with a switching device (SW), as shown in Fig. 2.15(a). This switching element can be a mechanical contractor or a semiconductor device. However, in most of the cases, it is a mechanical contactor because the switching frequency of SW is low. The modes of operation of the R+SW method are explained as follows,

   - During the off state, SW is in open circuit, and thus, no current flows through the precharging circuit, as shown in Fig. 2.15(a). The source and load sides are electrically isolated.
   - In order to charge the load capacitor, SW is closed. The current flows through the path $V_s - SW - R_{pc} - R_{\mu} - L_{\mu} - C_L$, as shown in Fig. 2.15(b). R_{pc} is the dominant term and its value affects the peak value of current. In most of the cases $L_{\mu} << C_L$, and thus, neglecting the effect of L_{μ}, this circuit is simplified to a first order system. The time required to charge the capacitor to ≈ 99 % of V_s is 5τ, where τ is approximately equal to R_{pc} C_L.

- Once the capacitor is completely charged, the semiconductor device is switched from the off state to the on state. Subsequently, SW is switched from closed circuit to open circuit. Thereafter, the power electronic converter starts switching and supplying the load current, as shown in Fig. 2.15(c).

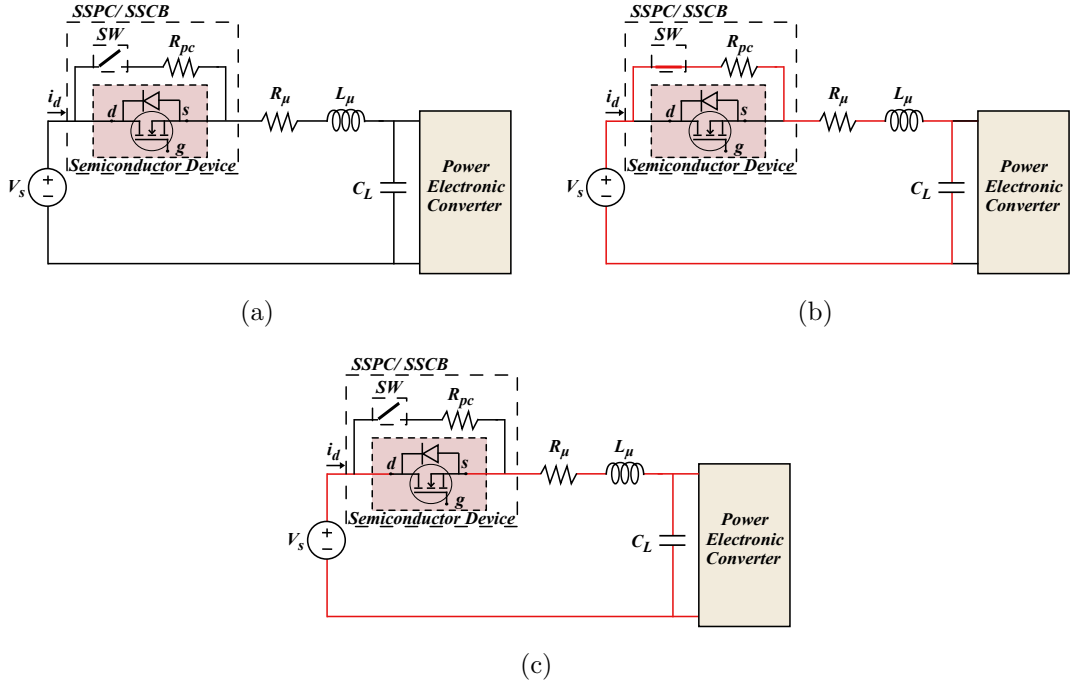


Figure 2.15: Modes of operation of R+SW precharging method: (a) off state, (b) precharging state, and (c) steady state.

The R+SW method is simple and easy to implement [70]. However, the precharge circuit contributes to the system weight, size, and complexity, which are critical factors in aerospace applications. Moreover, reselection of components is required in case of change in the values of V_s and C_L [70]. Thus, adaptability to changes of system parameters is low.

2. Buck Converter Method

This precharging method is proposed in [15]. The precharge circuit topology is the same as the buck converter circuit, and is connected in parallel with the semiconductor device, as shown in Fig. 2.16(a). This circuit also has a switching element, SW. In this case, SW is required to switch in the kHz range, due to which it is a semiconductor device. L_{pc} is an inductor, which is connected in series with SW. The cathode terminal of diode D is connected in between SW

and L_{pc}, the anode terminal of D is connected to the return path. The modes of operation of buck converter precharging method are discussed in detail as follows,

- During the off state, SW is electrically non-conductive. Therefore, source and load sides are electrically isolated from each other, shown in Fig. 2.16(a).
- During the precharging state, SW is switched as per a PWM signal send by the controller, as shown in Fig. 2.16(b). During the on time of SW, the current flows through the path $V_s - SW - L_{pc} - R_\mu - L_\mu - C_L$, and it rises. During the off time of SW, the diode conducts and the current flows through the path $D - L_{pc} - R_\mu - L_\mu - C_L$. The current decreases in this interval. The duty ratio of the PWM signal is adjusted by the controller, depending on the sensed voltage and current values, and control objective.
- The main semiconductor device is turned on after the capacitor is completely charged. Subsequently, the converter starts its operation and feeds the load, as shown in Fig. 2.16(c).

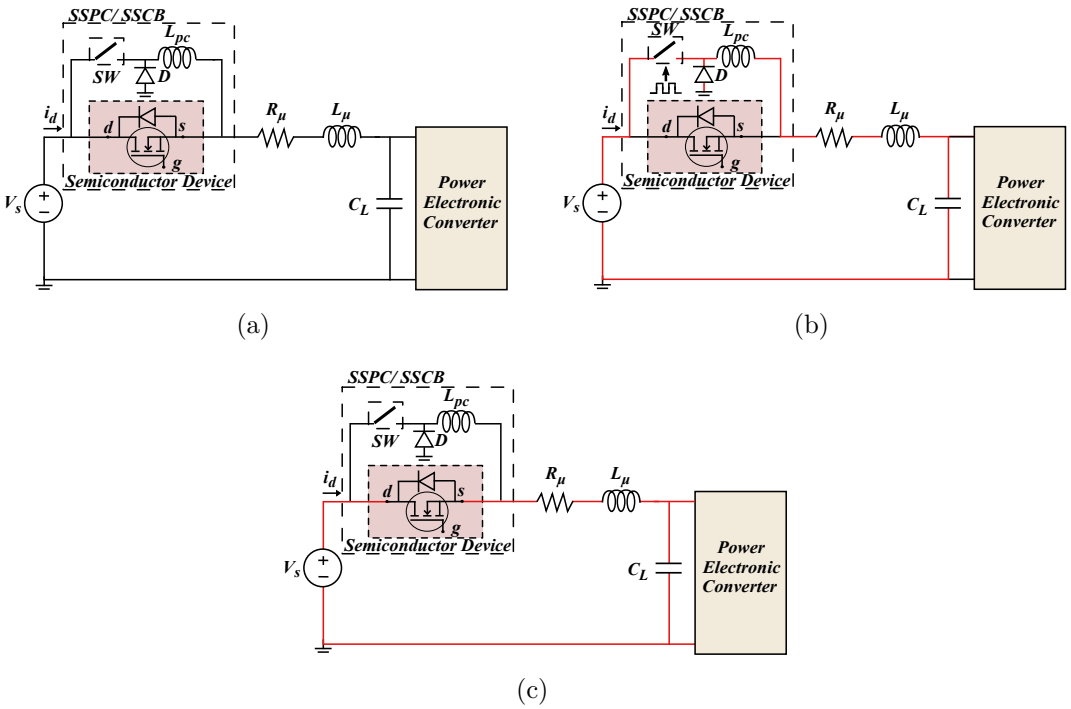


Figure 2.16: Modes of operation of buck converter method: (a) off state, (b) precharging state, and (c) steady state.

In R+SW and buck converter precharging methods, additional hardware is used and this circuit is responsible for initial charging of the capacitor. This

precharging circuit contributes to the overall weight and size of the system. To overcome this limitation, precharging methods, which make use of the main semiconductor device instead of additional hardware, are proposed in the literature and these methods are discussed in the next section.

Precharging using Main Semiconductor Device

In this section, the second category of precharging methods are discussed. In these methods, the main semiconductor device of the SSPC/ SSCB is employed for charging the capacitor. Thus, weight, size, and complexity, are less because no additional circuit is required. Safe operating area (SOA) and three-step precharging methods belong to this category and are explained in more detail as follows,

1. SOA Method

   The SOA method is proposed in [8]. During precharging, the semiconductor device of the SSPC/ SSCB is controlled in such a way that its operating point follows the SOA curve. The functional diagram of hardware implementation of this method is shown in Fig. 2.17 (Fig. 4 in [8]). The operating curve is stored in a look-up table, which generates the reference depending on the sensed voltage and current values. An MOSFET is the main semiconductor device. This method does not require any additional precharging circuit. However, the SOA is not provided in some of the power semiconductor device datasheets. In addition, this method is a curve-driven method due to which recalculation of the operating curve is necessary in case of change in source voltage value. Thus, adaptability to change of source parameters is low.

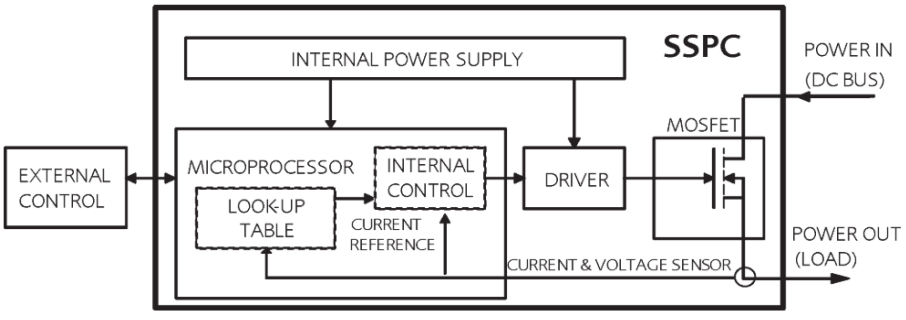


Figure 2.17: Functional diagram of hardware implementation of SSPC in [8].

2. Three-Step Method

   The three-step method is proposed in [16], where an MOSFET is considered as the main semiconductor device. In this precharging method, the gate-source voltage is regulated in such a way that its value is close to the threshold voltage. This method requires minimal datasheet parameter values. However, this method is implemented in an open loop manner due to which it is an indeterministic method. Closed-loop precharging methods are proposed in this thesis.

The SOA method discussed in this section, has a look-up table to store the curve. The data in this look-up table, is defined for specific operating conditions. In addition, some of the power semiconductor device datasheets do not have SOA curve. To overcome these limitations, a constant current precharging algorithm is proposed in **Chapter 3**. The proposed method has higher adaptability because only minor modifications in the firmware are required with the change of source parameters. In addition, it is applicable to a wide range of semiconductor devices because the prerequisites for the calculation of current reference are easily available in power semiconductor device datasheets.

SOA curves are defined for the following conditions, maximum junction temperature of the semiconductor device and constant case temperature of 25 °C. Thus, thermal stress on the semiconductor device, in the case of the SOA precharging method is high. Similar to the SOA precharging method, in the case of the constant current precharging method, an initial ambient temperature of 25 °C is assumed. However, the operating ambient temperature is not constant, especially in aerospace applications [5], and it varies depending on several factors such as geographic location. In order to address these issues, a constant temperature precharging algorithm is proposed in **Chapter 4**. The gate-source voltage of the semiconductor device is controlled in such a way that its junction temperature follows a given reference. In this method, the case temperature is measured and processed by the controller. As a result, the proposed constant temperature precharging algorithm takes into account the variation in operating temperature. Therefore, this method has high adaptability to change of source parameters as well as operating temperature. In addition, the thermal stress on the semiconductor device during precharging is regulated to a low value. This is important because high thermal stress may lead to reliability issues.

2.4 Discussion and Summary

A brief outlook of MEA has been presented in this chapter. Advantages of adoption of dc grids into electrical systems have been discussed, and protection challenges associated with dc grids have been explained.

The most commonly used switchgear and protection devices: fuses, MeCBs, SSPCs/ SSCBs, and HCBs, are presented in this chapter. Operating principle, advantages, and limitations of these devices, are thoroughly explained. SSPCs/ SSCBs have several advantages and based on these advantages, it has been concluded that they are a promising solution for protection of dc grids, which motivates to conduct research in this area.

The general structure of SSPC/ SSCB and its modes of operation have been discussed. Power semiconductor devices are one of the main components of SSPCs/ SSCBs and these have been reviewed in this chapter. On-state power loss of semiconductor devices is an important parameter because weight, size, and volume of SSPCs/ SSCBs is dependent on this parameter. Based on the type of power semiconductor devices, various SSPC/ SSCB topologies have been proposed in the literature. The operating principles of these topologies have been discussed, along with their advantages and limitations. Novel topologies are proposed in this thesis to overcome these limitations.

Precharging is one of the main tasks of SSPCs/ SSCBs, and simulation results of uncontrolled charging of the capacitor, have been presented to highlight the importance of precharging. Subsequently, existing precharging methods have been explained in detail. Pros and cons of these methods are elaborated. In order to address the drawbacks of these methods, novel precharging methods are proposed in this thesis.

Chapter 3

Constant Current Precharging Algorithm for SSPCs/ SSCBs

This chapter presents a constant current precharging algorithm for control of SSPCs/ SSCBs. The main aim of the proposed algorithm is to ensure that the current through the semiconductor device follows a constant reference. A brief overview of the existing precharging methods, and the novelty of the proposed algorithm, are discussed in Section 3.1. The proposed algorithm is introduced in Section 3.2. Equations of various key parameters are derived and analyzed in Section 3.3. Description of the hardware setup, and experimental results for verification of the proposed algorithm, are presented in Section 3.4. The main conclusions of this work are discussed in Section 3.5.

3.1 Introduction

The SSPC/ SSCB technology has been discussed in Section 2.3. One of the main responsibilities of SSPCs/ SSCBs is to charge the load capacitor in a controlled manner. The importance of precharging, and various existing precharging methods for SSPCs/ SSCBs, have been presented in Section 2.3.3. In some of the precharging methods/ techniques, a hardware circuit is used to fufill this task, and these methods have been discussed in Section 2.3.3. The main limitation of these methods is that the hardware circuit has a contribution in the overall weight and size of the system. In order to address this issue, precharging methods/ techniques in which the main semiconductor device is used for precharging, have been proposed in research articles.

These methods have been explained in Section 2.3.3. In the SOA precharging method, the semiconductor device voltage and current parameter values are controlled in such a way that these follows the SOA curve. However, SOA curves are not provided in some of the power semiconductor device datasheets. In addition, adaptability to change in the source parameters is low, this is because recalculation of the operating curve is necessary in the case of change in source voltage value. To overcome these limitations, constant current precharging algorithm is proposed.

A constant current precharging algorithm is proposed in this chapter. The main objective of the proposed algorithm is to regulate the device current in such a way that it follows a given current reference. In the case of change in the source voltage value, only minor modifications in the firmware are required, and thus, the proposed algorithm has higher adaptability. Moreover, the parameters used for the calculation of current reference, are easily available in power semiconductor device datasheets. Therefore, the proposed algorithm is employable for a wide range of semiconductor devices. Mathematical derivation of expressions of various key parameters, is presented in this chapter. Hardware experiments have been carried out to verify the proposed algorithm, and the experimental results are illustrated and explained in this chapter.

3.2 Proposed Constant Current Precharging Algorithm

SSPCs/ SSCBs are broadly classified into unidirectional SSPCs/ SSCBs and bidirectional SSPCs/ SSCBs, depending on the power flow controllability. SSPC/ SSCB topologies have been discussed in Section 2.3.2. The general SSPC/ SSCB configuration in dc power system in an aircraft is shown in Fig. 3.1(a). Generally, these MEA architectures have 270 V dc bus [25, 35]. Accordingly, in this chapter, experimental results at source voltage value of 270 V are presented. An SSPC/ SSCB topology for unidirectional fault isolation is shown in Fig. 3.1(b). Devices connected in anti-series configuration is the most commonly used SSPC/ SSCB topology for bidirectional fault isolation [16], illustrated in Fig. 3.1(c). A clamping circuit is used to clip the high voltage transients caused by the inductance in the circuit. Several overvoltage protection strategies have been proposed in the literature [9, 10, 16–18, 44].

These techniques can be employed to suppress the voltage overshoot during current breaking process. The majority of the over-voltage protection techniques utilize an additional hardware circuit. Most commonly used components in these over-voltage protection circuits are transient voltage suppression (TVS) diodes, metal oxide varistor (MOV), snubber capacitors, resistors, and diodes, as shown in Fig. 3.2. In the case of nominal working voltage, TVSs and MOVs behave as open circuits. In the case of over-voltage scenarios, TVSs and MOVs clamp the voltage across the sensitive devices, and concurrently, serve as low impedance current path. The variation in the clamping voltage with the current is lower in the case of TVS diodes compared to MOVs. However, MOVs are available for higher voltage ratings, and they have a lower cost [71]. Similarly, in the case of a snubber circuit, the capacitor stores the energy during transients, and thereby, limits the voltage. The equivalent circuit during precharging is shown in Fig. 3.3. L_μ and R_μ are the line inductor and resistor, respectively. C_L is the capacitor associated with the power electronic converters.

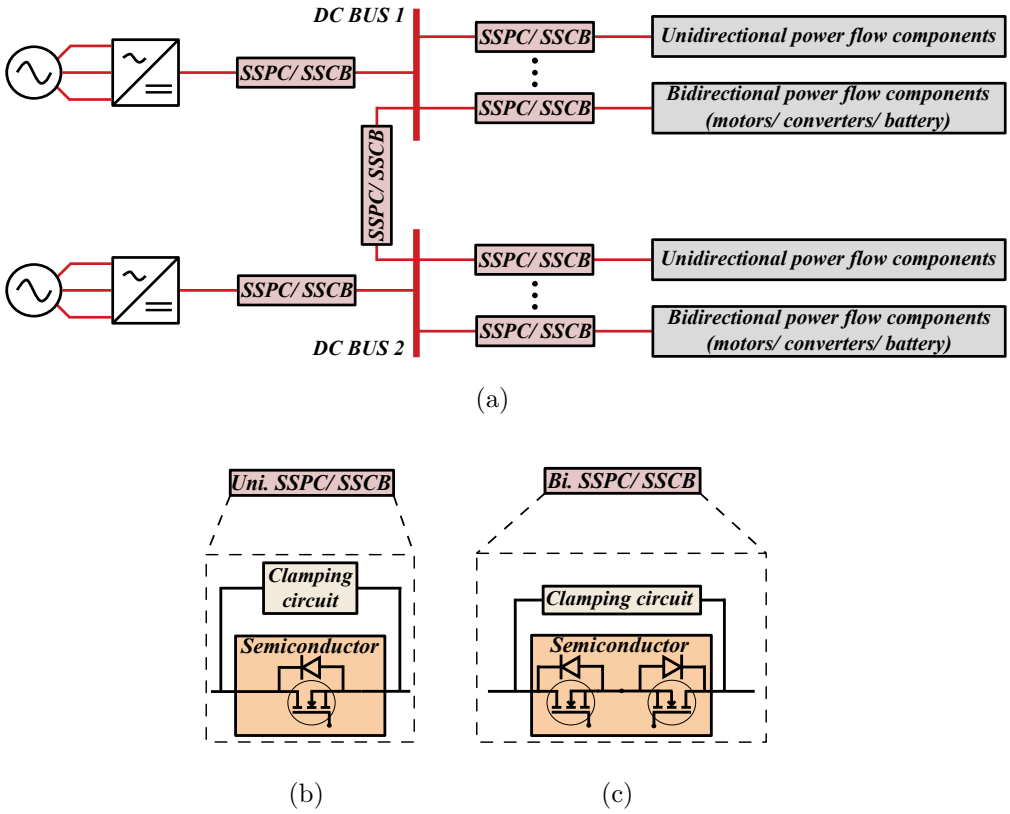


Figure 3.1: (a) SSPC/ SSCB configuration in an aerospace dc power system, (b) unidirectional SSPC/ SSCB topology, and (c) bidirectional SSPC/ SSCB topology.

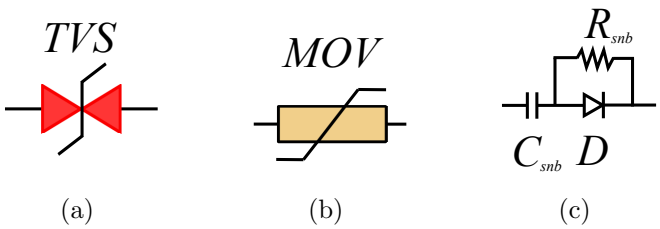


Figure 3.2: Over-voltage protection devices. (a) TVS, (b) MOV, and (c) RCD snubber.

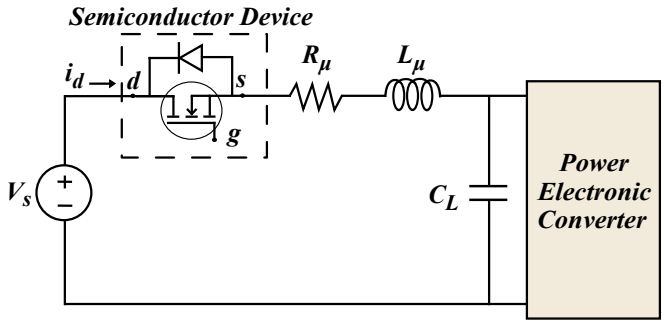


Figure 3.3: Equivalent circuit during precharging.

The output characteristics of an N-channel FET are shown in Fig. 3.4. An FET behaves as a resistor in the ohmic region. In the saturation region, an FET behaves as a gate controlled source, i.e., the current flowing through the FET is dependent on the voltage across the gate-source terminals.

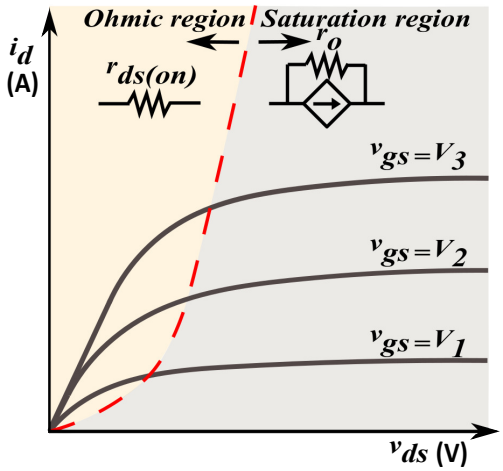


Figure 3.4: Output characteristics of an N-channel FET.

In this chapter, the device current is regulated such that it follows a given current reference. This is achieved by varying the gate-source voltage (v_{gs}) of the semiconductor device while it is operating in the saturation region. Although a single semiconductor has been considered in this chapter, the proposed algorithm and derived equations, are also valid for bidirectional SSPCs/ SSCBs. This is because in the latter case, an additional diode is present in the conduction path, which has a negligible effect on the transient characteristics. The gate-source voltage of the semiconductor device is varied using an analog gate driver, the functional diagram is shown in Fig. 3.5. The control algorithm is implemented in a microcontroller, TMDSDOCK28335 from Texas Instruments. A serial peripheral interface (SPI) communication protocol is used for communication between the microcontroller and the digital-to-analog (DAC) converter. The AD5628 (12-bit) DAC with an internal reference of 1.25V and gain of 2, is used in the hardware setup [72]. The analog output of the DAC follows the expression:

$$v_{out} = 2.5\left(\frac{D}{2^{12}}\right) \tag{3.1}$$

where D is the binary data (decimal format) sent by the microcontroller. v_{out} is fed into an isolated amplifier, which serves the purpose of isolating the high and low voltage sides. The output of the isolated amplifier is further amplified using a high current operational amplifier, in order to achieve the desired voltage level that is suitable for driving the gate of the semiconductor device. A high bandwidth RC low-pass filter is used at the output stage of the operational amplifier, to attenuate noise from the signal.

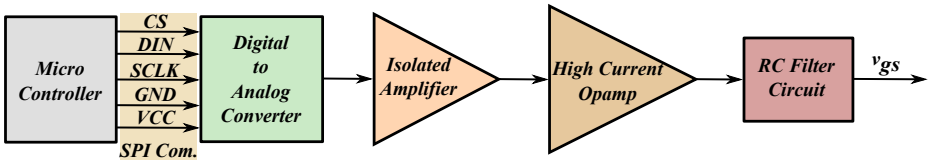


Figure 3.5: Functional diagram of analog gate driver.

The flowchart of the proposed constant current precharging algorithm is shown in Fig. 3.6. The capacitor voltage and drain current are measured using hall effect sensors, and these signals are processed by the microcontroller. The algorithm is executed in software interrupt service routine, which is triggered repeatedly after a

time interval of t_{step}. i_d is regulated to follow a current reference (I_{ref}), by varying the value of the gate-source voltage in steps, by means of incrementing/ decrementing the value of the DAC register. The gate-source voltage step is a fixed value. The step value of the gate-source voltage is selected in such a way that it is less than the threshold voltage of the semiconductor device. After a certain time delay (t_{delay}) of N cycles, the algorithm checks if the actual value of the capacitor voltage is less than the expected value in order to make sure that the circuit is healthy. In the case of a fault condition, the expected value of the capacitor voltage is dependent on the fault resistance. The expression of the maximum value of capacitor voltage is as follows, $V_{Cm} = I_{ref}$ x R_{fm}, where R_{fm} is the maximum value of fault resistance. In order to detect fault, the controller compares the actual value of v_C with V_{Cm}. In most of the cases, V_{Cm} is a few volts and is in close proximity to zero. If the fault exists, the semiconductor device is turned off. If the circuit is healthy, the algorithm continues regulating the current. Once the capacitor voltage reaches a value which is approximately equal to the source voltage, the gate-source voltage is increased fully. If the circuit is healthy, the algorithm continues regulating the current. Once the capacitor voltage reaches a value, which is approximately equal to the source voltage, the gate-source voltage is increased fully.

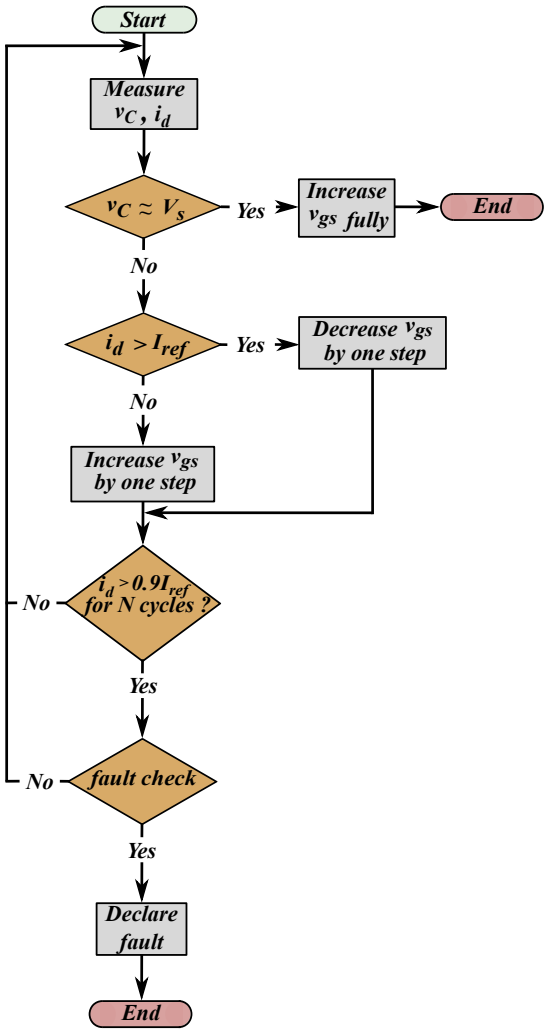


Figure 3.6: Flowchart of the proposed constant current precharging algorithm.

3.3 Analytical Evaluation

The control algorithm is executed in the microcontroller by applying a software interrupt service routine repeatedly after a fixed time interval of t_{step}. In Section 3.3.1, expressions are derived to determine the limits of the t_{step}. In Section 3.3.2, the upper limit of the current reference is derived to ensure that the device remains safe during precharging.

3.3.1 Current Dynamics

In the saturation region, the current flowing through the semiconductor device, is dependent on the voltage across the gate source terminals [73]. Electrical models

of the semiconductor device in this operating region are shown in Fig. 3.7, these models are obtained by assuming linear transfer characteristics in the vicinity of the threshold voltage. The value of v_{ov} is equal to $v_{gs} - V_T$. g_m is the transconductance of the semiconductor device. r_o incorporates the variation in drain current due to the Early effect. The equivalent circuit during precharging with the model of the semiconductor device is shown in Fig. 3.8. Since $R_\mu << r_o$, $r_o + R_\mu$ has been assumed to be approximately equal to r_o in the subsequent analysis. $V_{ds} > v_{gs} - V_T$ is the necessary condition for the semiconductor device to remain in the saturation region, thus, derived equations in this section are valid as long as this inequality holds true. Using Kirchhoff's voltage law and Laplace domain analysis, the drain current variation with the gate source voltage can be calculated as,

$$i_d = Ae^{\alpha_1 t} + Be^{\alpha_2 t} \tag{3.2}$$

where,

$$A = \frac{V_s + g_m V_{ov} r_o}{\sqrt{r_o^2 - \frac{4L_\mu}{C_L}}} \tag{3.3}$$

$$B = -\frac{V_s + g_m V_{ov} r_o}{\sqrt{r_o^2 - \frac{4L_\mu}{C_L}}} \tag{3.4}$$

$$\alpha_1, \alpha_2 = \frac{-r_o \pm \sqrt{r_o^2 - \frac{4L_\mu}{C_L}}}{2L_\mu} \tag{3.5}$$

Assuming $\left(\frac{L_\mu}{C_L}\right) \approx 0$, a simplified expression of the drain current can be represented as,

$$i_d = \frac{V_s + g_m V_{ov} r_o}{r_o}\left(1 - e^{\frac{-r_o t}{L_\mu}}\right) \tag{3.6}$$

The time required for i_d to be within $\pm 5\%$ of the steady-state value is 3τ, where τ is $\frac{L_\mu}{r_o}$. The algorithm updates the DAC register after a certain time interval (t_{step}), which value is selected such that $t_{step} > 3\tau$.

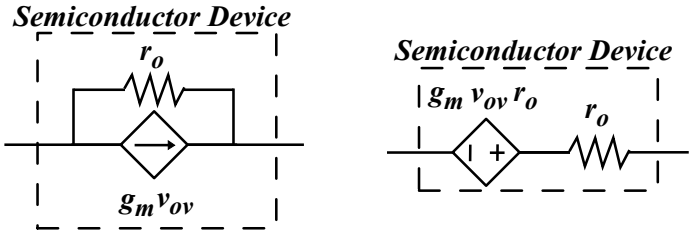


Figure 3.7: Electrical model of the semiconductor device.

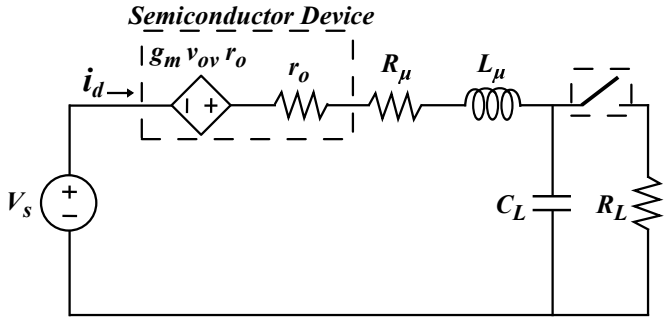


Figure 3.8: Thevenin equivalent mathematical circuit during precharging.

3.3.2 Current Reference

In this subsection, some expressions are derived to compute the maximum value of current reference for the device to operate within its safe limits. Current and voltage waveforms during precharging are shown in Fig. 3.9. Assuming $i_d \approx I_{ref}$, the variation in voltage across the capacitor with time can be calculated as,

$$v_C(t) = \frac{I_{ref}}{C_L} t \tag{3.7}$$

Rearranging the terms, the time required for charging the capacitor can be calculated as,

$$t_{pc} = \frac{V_s C_L}{I_{ref}} \tag{3.8}$$

Using (3.7), the variation of power dissipated by the FET can be calculated as,

$$p_d(t) = \begin{cases} \left(V_s - \frac{I_{ref}}{C_L} t\right) I_{ref} & 0 < t < t_{pc} \\ 0 & \text{Otherwise} \end{cases} \tag{3.9}$$

The waveshape of p_d is triangular with respect to time. In order to simplify the calculation, an equivalent square power pulse $\left(p_{eq}(t)\right)$ is considered in the subsequent analysis. Using the methods stated in [74], $p_{eq}(t)$ can be calculated as,

$$p_{eq}(t) = \begin{cases} V_s I_{ref} & 0 < t < \frac{t_{pc}}{2} \\ 0 & \text{Otherwise} \end{cases} \tag{3.10}$$

Multiplying (3.10) by the thermal resistance $\left(R_{th(j-c)}\right)$, temperature rise (ΔT) due to p_{eq} can be calculated as,

$$\Delta T = T_{junc.} - T_{case} = V_s I_{ref} R_{th(j-c)} \tag{3.11}$$

Heat sinks and lead frame in general have a very large thermal capacity [75] due to which the case temperature varies during transient condition. A margin of 25 °C is assumed in order to incorporate the rise in case temperature above the ambient temperature. This assumption is validated in the later part of the analysis. The ambient temperature is assumed to be 25 °C in this analysis. Substituting $T_{junc.} =$ 150 °C in (3.11), the maximum value of current reference (I_{rm}) for the device to remain within its thermal limits can be calculated as,

$$I_{rm} = \frac{100}{V_s R_{th(j-c)}} \tag{3.12}$$

I_{rm} in (3.12) is a conservative approximation. In the subsequent part of the analysis, the condition for the case temperature to stay within 25 °C margin is derived. Dynamics of the case temperature are governed by:

$$p(t) = C_{case} \frac{dT_{case}}{dt} \tag{3.13}$$

where C_{case} is the thermal capacitance of the case in Joules/°C, and T_{case} is the case temperature in °C. Substituting (3.10) in (3.13), and imposing $\Delta T_{case} < 25$°C, the limit on the C_{case} upon simplification can be represented as,

$$C_{case} > \frac{V_s I_{rm} t_{pc}}{50} \tag{3.14}$$

If the inequality (3.14) does not hold true, then the temperature margin is increased until the condition is fulfilled. I_{rm} and the corresponding t_{pc}, for different values of V_s are specified in Table 3.1. These values are calculated using parameters from the datasheet of the FET [76].

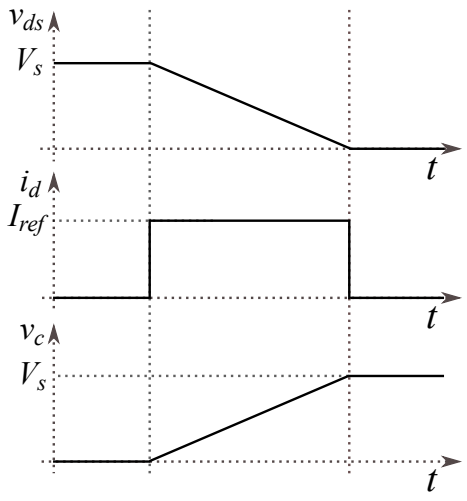


Figure 3.9: Current and voltage waveforms during precharging.

Table 3.1: Analytical Solution of I_{rm} and t_{pc} for Different Values of V_s

V_s (V)	I_{rm} (A)	t_{pc} (ms)
270	1.322	102.11
235	1.519	77.35
200	1.785	56.02

3.4 Prototype Description and Experimental Validation

Experiments on a laboratory prototype are carried out to verify the proposed algorithm for different values of source voltage. The parameters used are specified in Table 3.2. The FET is selected in such a way that the drain-source breakdown voltage is within the generally accepted peak voltage range [10]. However, the proposed constant current precharging algorithm is applicable to any semiconductor device with output characteristics similar to the selected device. $I_{c\,max}$ increases with the decrease in the value of L_μ. Thus, the algorithm is verified for both scenarios, $L_\mu \approx 0$ and $L_\mu \approx 18.48$ μH.

Table 3.2: Circuit Parameters for Verification of Constant Current Precharging Algorithm

Parameter	**Value**
Source voltage, V_s	270 V, 235 V, 200 V
Line inductance, L_μ	18.48 μH, 0 μH
Line resistance, R_μ	70 mΩ
Capacitance, C_L	500 μF
FET device	STW65N65DM2AG

Fig. 3.10 illustrates the experimental setup used to validate the precharging algorithm. A Tektronix MDO4104B-3 mixed domain oscilloscope (bandwidth: 3 GHz), THDP0200 voltage probes (bandwidth: 200 MHz), and TCP0030 current probes (bandwidth: 120 MHz), are utilized for the experiments. The dc power supply is TDK lambda gen3300w (maximum voltage: 300 V, maximum current: 11 A). The auxiliary power supply is MATRIX MPS-3005TK-3.

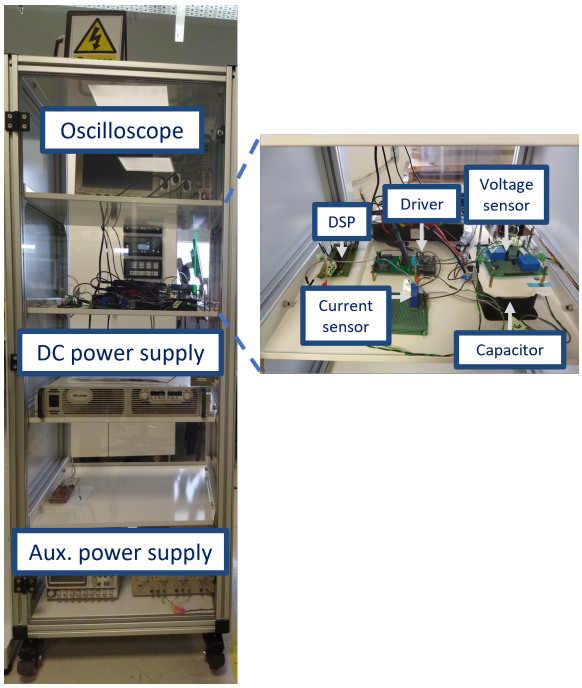


Figure 3.10: Picture of the experimental setup.

The circuit configuration for the experimental results is shown in Fig. 3.11. Hall effect sensors are used for measuring voltages and currents. Low tolerance measurement resistors are used in the sensor board to achieve high accuracy of measurement. The current reference is selected such that its value is less than I_{rm} specified in Table 3.1. The proposed control algorithm is executed in an interrupt service routine, repeatedly after a time interval of 13.33 μs. Experimental results for precharging with $L_\mu \approx 0$, for different values of source voltage are shown in Figs. 3.12 - 3.14. At the time instant labeled as ⓐ, the capacitor voltage starts to build up. v_{gs} is regulated by the controller in order that i_d follows I_{ref}. At the time instant labeled as ⓑ, the capacitor is fully charged. A comparison of precharging time for different values of source voltages is shown in Table 3.3.

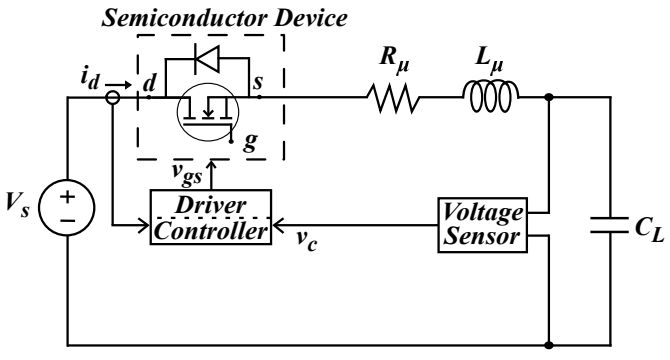


Figure 3.11: Equivalent circuit for experimental verification.

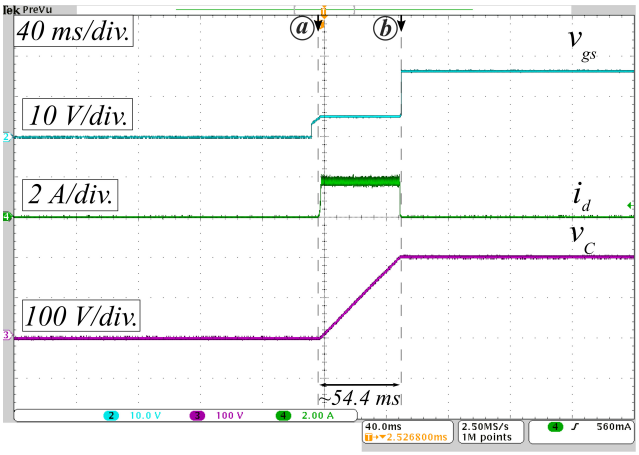


Figure 3.12: Experimental results for precharging with $L_\mu \approx 0$ at $V_s = 200$ V & $I_{ref} = 1.75$ A.

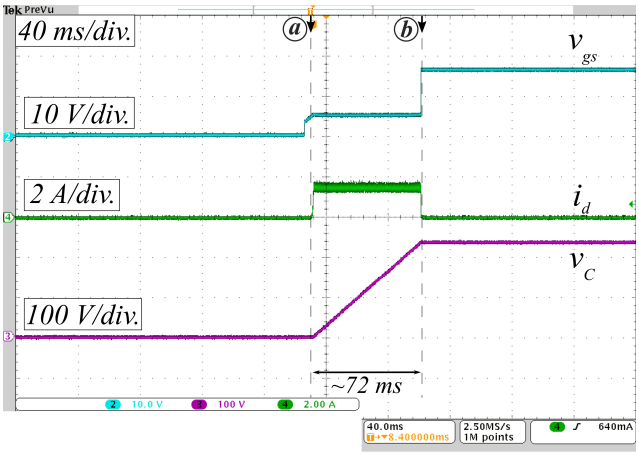


Figure 3.13: Experimental results for precharging with $L_\mu \approx 0$ at $V_s = 235$ V & $I_{ref} = 1.50$ A.

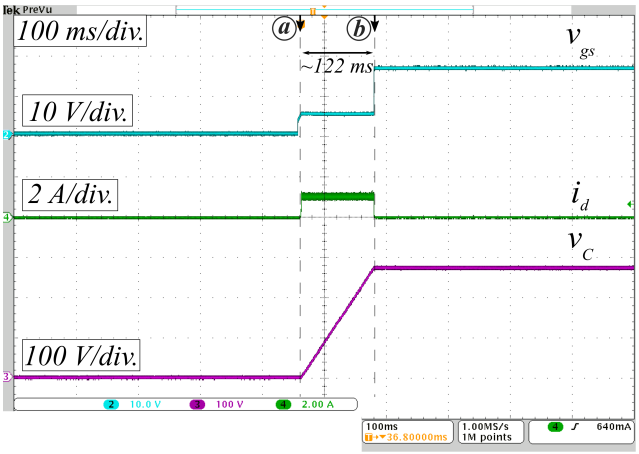


Figure 3.14: Experimental results for precharging with $L_\mu \approx 0$ at $V_s = 270$ V & $I_{ref} = 1$ A.

Table 3.3: Precharging Time Comparison

Source voltage, V_s	200 V	235 V	270 V
I_{ref}	1.75 A	1.5 A	1 A
Analytical t_{pc}	57.14 ms	78.33 ms	135 ms
Experimental t_{pc}	54.4 ms	72 ms	122 ms

Experimental results for precharging with fault are shown in Fig. 3.15. At the time instant labeled as ⓐ, i_d is approximately equal to I_{ref}. After 300 cycles or 4 ms, represented by the time instant labeled as ⓑ, the controller detects that the capacitor is not being charged, and declares it as a fault. Thereafter, the semiconductor device is turned off by reducing the gate voltage to zero.

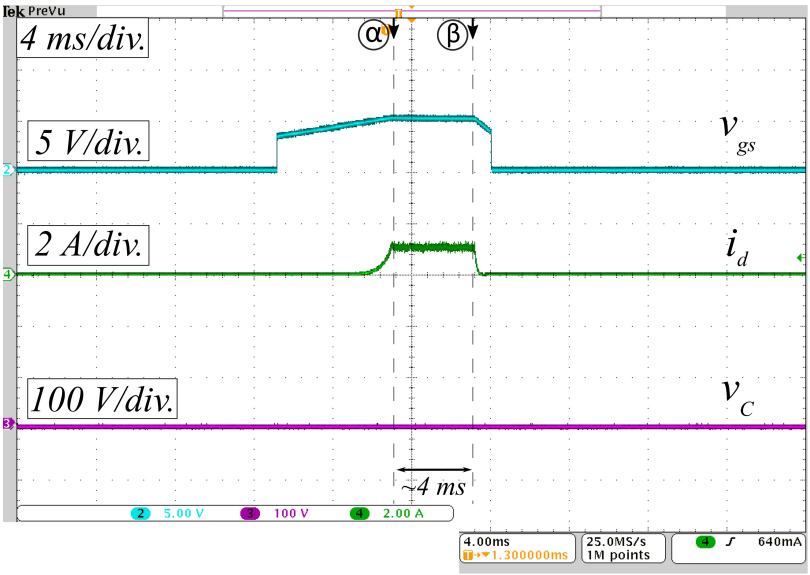


Figure 3.15: Experimental results for precharging with fault at $V_s = 270$ V, $L_\mu \approx 0$ & $I_{ref} = 1$ A.

Experimental results for precharging with $L_\mu \approx$ 18.48 μH are shown in Fig. 3.16. The capacitor voltage starts increasing at the time instant labeled as ⓖ. During the precharging interval, i_d follows the current reference. At the time instant labeled as ⓓ, the capacitor is charged to a value which is approximately equal to the source voltage.

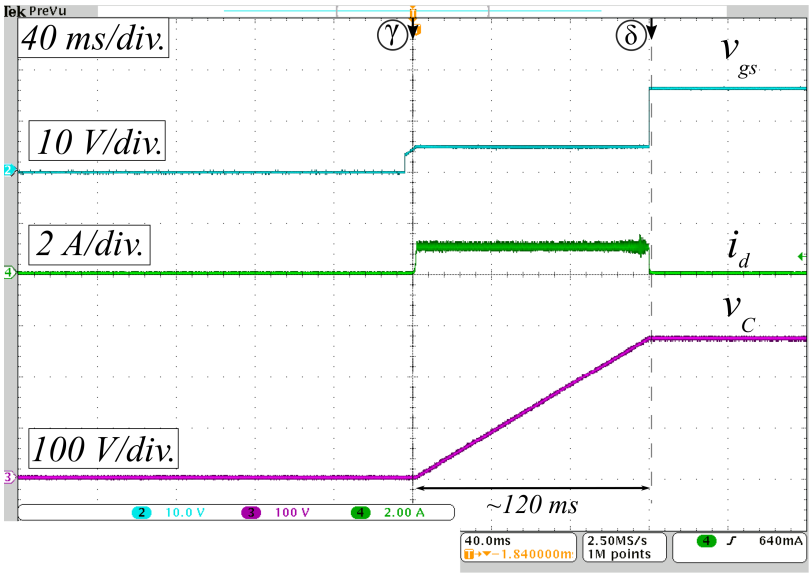


Figure 3.16: Experimental results for precharging with $L_\mu \approx$ 18.48 μH at $V_s = 270$ V & $I_{ref} = 1$ A.

3.5 Discussion and Summary

In this chapter, a constant current precharging algorithm for SSPCs/ SSCBs has been proposed. The precharging method utilizes the main semiconductor device to limit the inrush current, thus, no additional precharge circuitry is required. In addition, the proposed algorithm can operate with a wide range of source parameters. Moreover, the parameters used for the calculation of the current reference, are easily available in most of the power semiconductor device datasheets, thus, the algorithm can be implemented in different semiconductor devices. The algorithm has been verified by experiments under various operating conditions.

In this chapter, an initial ambient temperature of 25 °C has been assumed. However, the operating temperature varies in aerospace applications [5]. This issue is addressed in the next chapter.

Chapter 4

Active Thermal Control of SSPCs/ SSCBs During Precharging Interval

An active thermal control algorithm is introduced in this chapter. The proposed precharging algorithm regulates the junction temperature of the semiconductor device, such that it follows a constant reference value. The key innovations of this method are presented in Section 4.1. The flow chart of the proposed control strategy is illustrated and discussed in Section 4.2. Hardware experiments have been carried out for verification of the proposed algorithm, and the experimental results are presented in Section 4.3. The main conclusions of this work are summarized in Section 4.4.

4.1 Introduction

The main purpose of the precharging, has been discussed in Section 2.3.3. In addition, operating principle, advantages, and limitations of various precharging methods, have been explained. In the case of the SOA precharging method, the semiconductor device electrical parameters are regulated in such a way that these follows the SOA curve. However, in most of the cases, conditions for deriving SOA curves are maximum junction temperature and constant case temperature of 25 °C. Hence, in this method, the semiconductor device experiences high thermal stress. In the previous chapter, a constant current precharging algorithm was proposed, and it was assumed that the initial ambient temperature was 25 °C. However, the operating temperature

varies in aerospace applications [5], and is a function of various factors. In order to overcome these drawbacks, a constant temperature precharging algorithm is proposed in this chapter. In the proposed strategy, the junction temperature of the semiconductor device is controlled in such a way that it follows a reference temperature, this is achieved by regulating the gate-source voltage of the semiconductor device. Case temperature measurement is used in the proposed algorithm for estimating real-time junction temperature. Consequently, the proposed algorithm has high adaptability to change of operating temperature. In addition, the adaptability to change of source parameters is also high. Moreover, in this method, the thermal stress on the semiconductor device is regulated to a low value. The flowchart of the proposed algorithm is presented and explained in this chapter. The proposed algorithm is verified using a laboratory prototype, and the experimental results obtained using this setup are also discussed.

4.2 Active Thermal Control of SSPCs/ SSCBs

The precharging circuit diagram is thoroughly explained in the previous chapters, thus, it is briefly discussed in this chapter. The equivalent circuit of a subsystem in an aircraft is shown in Fig. 4.1. The dc source is denoted by V_s. The SSPC/ SSCB is connected in series in the circuit. Resistor (R_μ) and inductor (L_μ) are the line parameters. C_L is the load capacitor, which is connected to the power electronic converter.

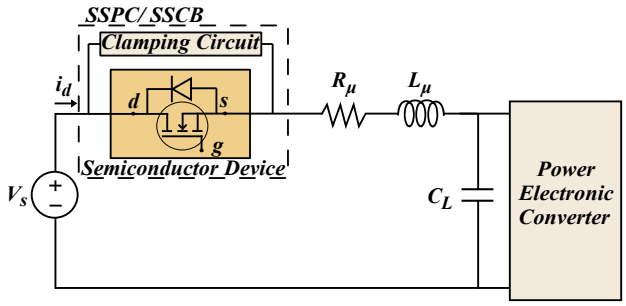


Figure 4.1: Equivalent circuit of a dc subsystem with SSPC/ SSCB protection in an aircraft.

The output characteristics of an N-channel FET has been discussed in Section 3.2, and are illustrated in Fig. 3.4. In summary, the FET has two main operating regions, the ohmic and the saturation regions. In the ohmic region, the FET behaves as a

resistor of value equal to the inverse of the slope of the curve. In the saturation region, the FET behaves as a gate-controlled current source. In the equivalent circuit model, the effect of v_{ds} on i_d is modeled using a resistor of value r_o. In this chapter, the main semiconductor device of the SSPC/ SSCB is utilized for precharging, and is operated in its saturation region. The gate voltage of the device is adjusted by the controller, in such a way that the junction temperature of the device follows a given reference. An analog gate driver is used to regulate the gate-source voltage of the semiconductor device. The details of the gate driver have been discussed in Section 3.2.

4.2.1 Proposed Constant Temperature Precharging Algorithm

Real time estimation of the junction temperature (t_j) of the semiconductor device, is required for the implementation of the proposed algorithm. Several junction temperature estimation methods have been proposed in the literature, and these methods are implemented using either an observer, or sensor-on-die, or are based on switching and steady-state characteristics of the semiconductor device [77]. During precharging, the semiconductor device is in its saturation region, due to which junction temperature estimation methods based on switching and steady-state characteristics, are not suitable. Sensor-on-die methods are difficult to implement because these are invasive methods. Thus, in this chapter, a closed-loop t_j observer is used, which calculates t_j directly from the power loss (p_d) in the semiconductor device. A comparison of first-order, second-order, and third-order estimator has been presented in [78]. The second order model is computationally faster than other higher-order estimators, and has sufficient accuracy. Therefore, the second-order foster electro-thermal model is used in this implementation, which is presented in Fig. 4.2. p_d is the power loss in the semiconductor device. R_1 (°C/W) and R_2 (°C/W) are thermal resistors, C_1 (J/°C) and C_2 (J/°C) are thermal capacitors. The case temperature of the semiconductor device (t_{case}) is measured by means of a thermocouple and an AD595 amplifier IC. This temperature sensor is able to measure slow variations in operating temperature.

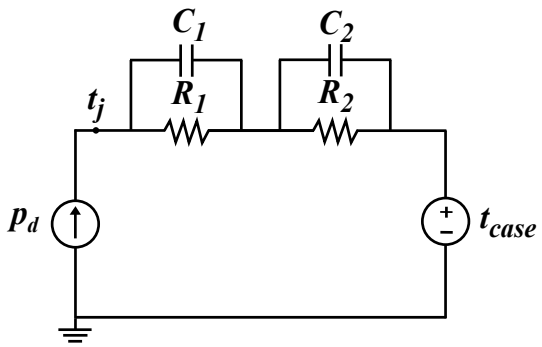


Figure 4.2: Foster electro-thermal model of a semiconductor device.

Thermal resistors (R_1 and R_2) and thermal capacitors (C_1 and C_2) values, are calculated using PLECS toolbox by curve fitting single pulse thermal impedance curve provided in the datasheet [76] of the semiconductor device. The values of R_1, R_2, C_1, and C_2 are 0.0335 °C/W, 0.2465 °C/W, 0.0114 J/°C, and 0.128 J/°C, respectively. The thermal model is discretized using the methods stated in [79]. The expressions for the calculation of t_j for a step/ sampling time of 30 μs are as follows:

$$x_1^k = 0.9248 \;\; x_1^{k-1} + 0.0025175 \;\; p_d \tag{4.1}$$

$$x_2^k = 0.99905 \;\; x_2^{k-1} + 0.00023258 \;\; p_d \tag{4.2}$$

$$t_j^k = x_1^k + x_2^k + t_{case} \tag{4.3}$$

where x_1 and x_2 are state variables. x_1^k and x_2^k are the values of the state variables at the k^{th} step. x_1^{k-1} and x_2^{k-1} are the values of state variables at the $(k\text{-}1)^{\text{th}}$ step. The initial value of these state variables is zero because $t_j^0 \approx t_{case}$. p_d is the power dissipated by the semiconductor device, and is the product of i_d and v_{ds}. Since the voltage across the inductor is low, v_{ds} has been assumed to be approximately equal to $V_s - v_c$. t_{case} is the case temperature of the semiconductor device.

The flow chart of the proposed constant temperature precharging algorithm is shown in Fig. 4.3. The control algorithm is implemented in a software interrupt service routine, which is triggered repeatedly after a fixed time interval of 30 μs. The capacitor voltage, device current, and case temperature are measured using sensors. t_j of the semiconductor device is estimated by solving (4.1) - (4.3). The gate-source

voltage (v_{gs}) of the semiconductor device is varied depending on t_j. v_{gs} has an effect on t_j because the semiconductor device is in its saturation region where it behaves as a gate controlled source. v_{gs} has 4,096 steps because the DAC IC has 12 bit resolution. In case of t_j greater than T_{ref}, v_{gs} is decreased by one step and vice-versa. Subsequent part of the algorithm makes sure that there is no fault at the load side. The expected value of the capacitor voltage, v_{Cexp}, is calculated by the controller using the following expression,

$$v_{Cexp} = \frac{\sum i_d^k \, T_s}{C_L} \tag{4.4}$$

where T_s is the step/ sampling time. In case of voltage mismatch, i.e., $v_{Cexp} > 10$ V and measured $v_C \approx 0$, a fault is declared, and v_{gs} is reduced to zero. If no shortcircuit is detected, the controller continues to regulate t_j. Once the capacitor is completely charged, v_{gs} is increased to its maximum value.

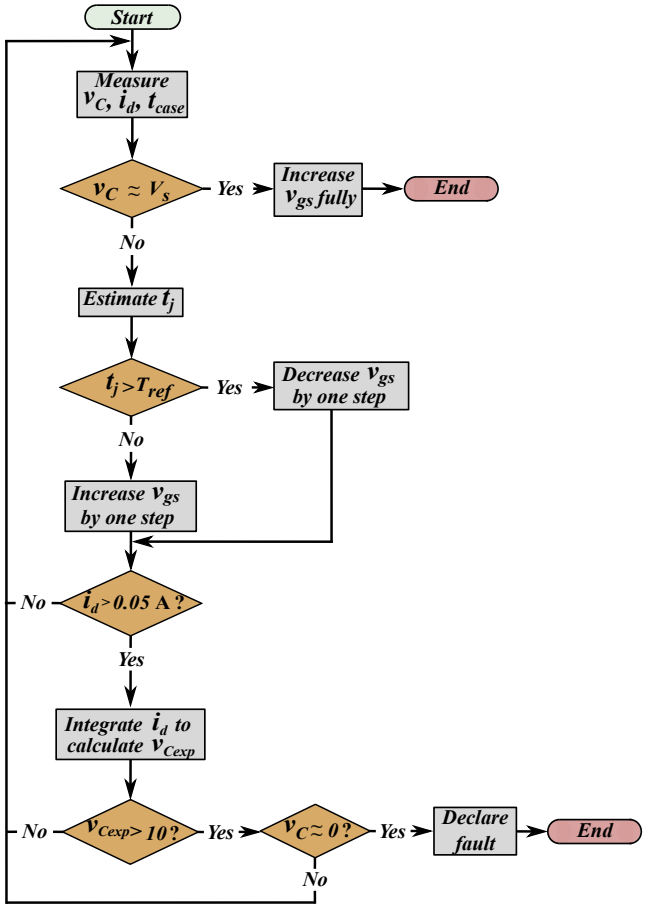


Figure 4.3: Flowchart of the proposed constant temperature precharging algorithm.

Table 4.1: Circuit Parameters for Experimental Verification

Parameter	**Value**
Source voltage, V_s	270 V, 235 V
Line inductance, L_μ	18.48 μH
Line resistance, R_μ	70 mΩ
Capacitance, C_L	500 μF
FET part number	STW65N65DM2AG

4.3 Prototype Description and Experimental Verification

Experiments are performed to verify the proposed constant temperature precharging algorithm. The hardware setup is shown in Fig. 4.4. The electrical circuit representation is shown in Fig. 4.5, and the parameter values are listed in Table 4.1. LEM hall effect current and voltage sensors are used in the hardware setup. Type K thermocouple is used for temperature sensing, one end of the thermocouple is attached through a 1-mm hole in the heat sink [80] and the other end is connected to the AD595 thermocouple amplifier IC.

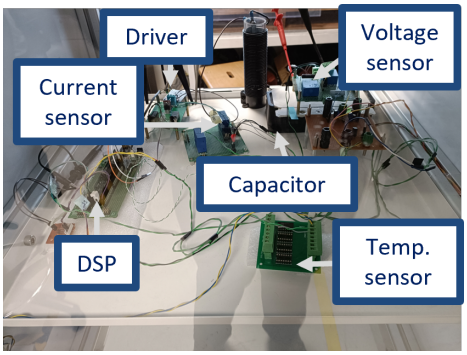
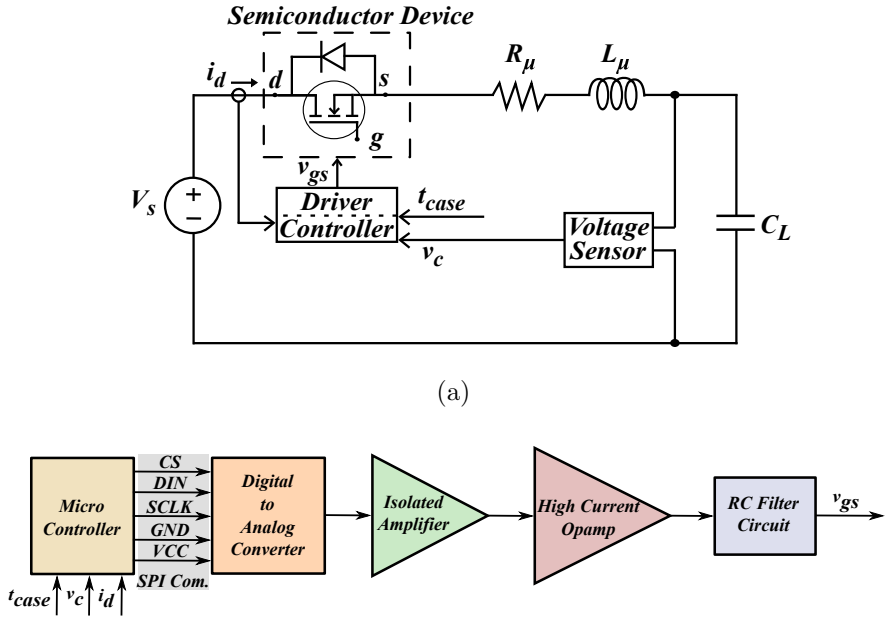


Figure 4.4: Picture of the hardware setup.

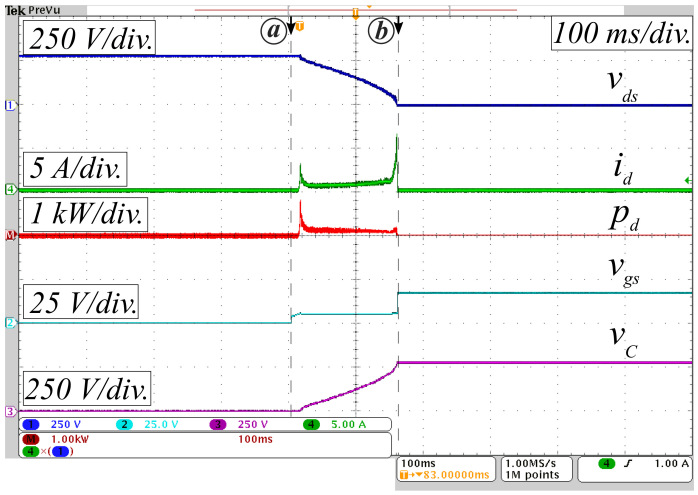


(a)

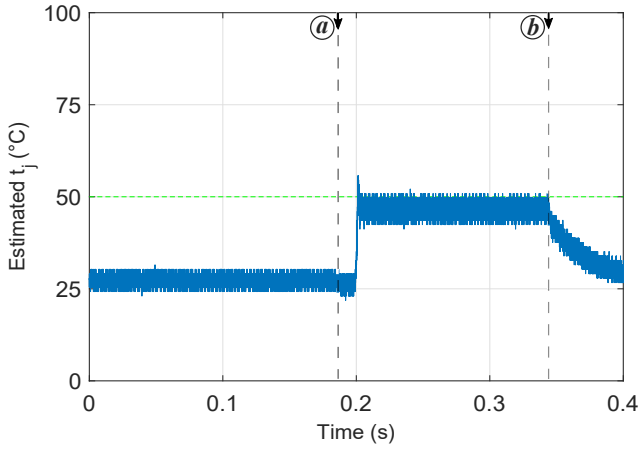
(b)

Figure 4.5: Electrical circuit representation of hardware setup.

In order to validate constant temperature precharging, experiments have been carried out at $V_s = 270$ V and $T_{ref} = 50$ °C, results are presented in Fig. 4.6(a). The value of temperature reference is selected in such a way that the thermal stress on the semiconductor device is low. The estimated t_j by the controller, is measured by using a PWM-to-analog converter. The duty cycle of 1.5 MHz PWM signal is varied depending on the estimated t_j value. This PWM signal is filtered using an RC low-pass filter with a cutoff frequency of 80 KHz. The output of the filter is measured using an oscilloscope and, scaled and plotted using MATLAB, as shown in Fig. 4.6(b). At the time instant labeled as ⓐ, the controller starts executing the constant temperature precharging algorithm, illustrated in Figs. 4.6(a) and (b). t_j of the semiconductor device follows the 50 °C reference. Towards the end of the precharging interval, the voltage across the drain-source terminals is low. Consequently, the current flowing through the semiconductor device is high, since the junction temperature follows the reference. At the time instant labeled as ⓑ, the capacitor is charged to a value approximately equal to the source voltage. Consequently, v_{gs} is increased to its maximum value.



(a)



(b)

Figure 4.6: (a) Experimental results and (b) estimated t_j by the controller, for precharging at $V_s = 270$ V & $T_{ref} = 50$ °C.

In order to verify the adaptability of the proposed algorithm to the change in source voltage value, an experiment is performed at $V_s = 235$ V and $T_{ref} = 50$ °C, as shown in Fig. 4.7. In this case, only minor modifications are made in the variables declaration section of the code. At the time instant labeled as ⓐ, the controller starts regulating t_j. At the time instant labeled as ⓑ, the capacitor is completely charged. In this case, the time required for the capacitor to completely charge is less than in the previous case (Fig. 4.6(a)). This is because the energy required by the capacitor is proportional to the square of V_s.

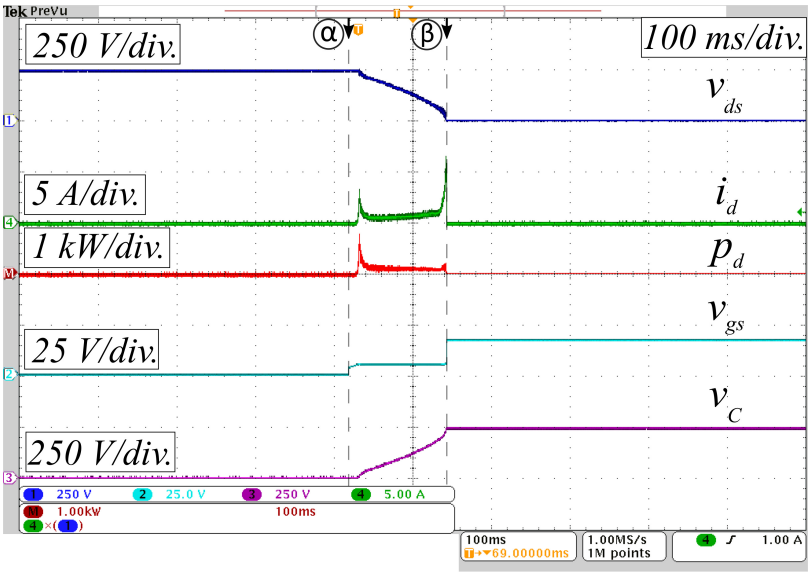


Figure 4.7: Experimental results for precharging at $V_s = 235$ V & $T_{ref} = 50$ °C.

An experiment is carried out to validate the operation of the proposed algorithm in the case of a fault at the load side, as shown in Fig. 4.8. The controller calculates the expected value of the capacitor voltage using the drain current. Once the expected value of capacitor voltage exceeds a certain threshold, the controller compares the sensed value of the capacitor voltage to ensure that the system is healthy. The controller declares it as a fault because the capacitor voltage is zero. Thereafter, v_{gs} is reduced to zero to electrically isolate the source and load side.

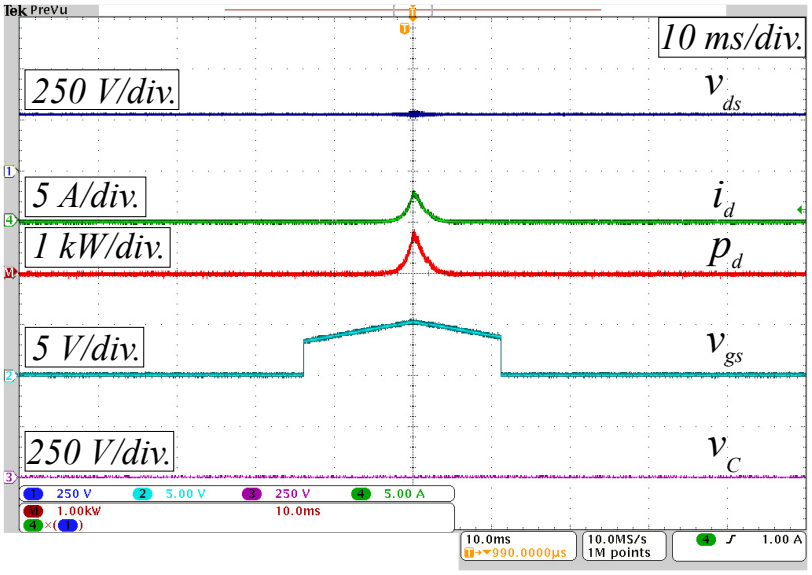


Figure 4.8: Experimental results for precharging with fault at $V_s = 270$ V.

4.4 Discussion and Summary

In this chapter, a constant temperature precharging algorithm for SSPCs/ SSCBs, has been proposed. The main objective of this algorithm is to maintain a constant junction temperature during the precharging interval. The proposed algorithm has been verified through experiments using a laboratory hardware setup. Adaptability of the proposed algorithm to change in parameter values is high. Moreover, thermal stress on the semiconductor device during charging of capacitor is low.

SSPCs/ SSCBs have high on state power loss, because high-voltage semiconductor devices are in the load current path. On state power loss directly affects the efficiency and heat-sink size, which are important parameters. This motivates to explore ways to reduce power loss. SCR based SSPCs/ SSCBs are emerging and promising candidates, as SCRs have low voltage drop and superior fault handling capability. These topologies are considered in the next chapter.

Chapter 5

SCR-Based Bidirectional SSPC/ SSCB Topologies

SSPC/ SSCB cooling requirements are derived from the power loss, or in other words, the heat sink size increases with the increase in the power loss. Thus, low power loss is beneficial and accordingly, it is important to explore technologies and topologies to achieve this. Power loss is a function of square of current, due to which, high current applications require even greater attention.

Fig. 5.1 shows a simplified diagram of aircraft electrical system. This circuit does not include any auxiliary power unit and many other components, only the dc subsystem is illustrated. SSPCs/ SSCBs, which are directly connected to the power converters and in between the two buses, carry the maximum current. The SSPC/ SSCB, which is used for interconnecting and protecting the two buses, is also known as tie SSPC/ SSCB. The two buses are connected using inductors, the main role of these inductors is to prevent failure of the healthy bus in case of fault at one of the buses. In other words, these inductors ensure that the voltage of a healthy bus is within its normal range [81], even in case of fault at the other bus. Low loss semiconductor devices are preferred for tie SSPC/ SSCB because they carry high current. The SCR is a low loss semiconductor device, which is a promising candidate for tie SSPC/ SSCB, and has recently gained attention in academia and industry [9, 10]. The SCR is a unidirectional and half-controlled semiconductor device. In addition to low on-state power loss, there are several other advantages of SCRs, and these are valuable for SSPCs/ SSCBs [9, 10]. These have excellent shortcircuit current handling capability. Moreover, The cost of SCRs is low. However, some of the SCR-based SSPCs/ SSCBs

have slower response time compared to FCS-based SSPCs/ SSCBs. Novel SCR-based SSPC/ SSCB topologies are proposed in this chapter.

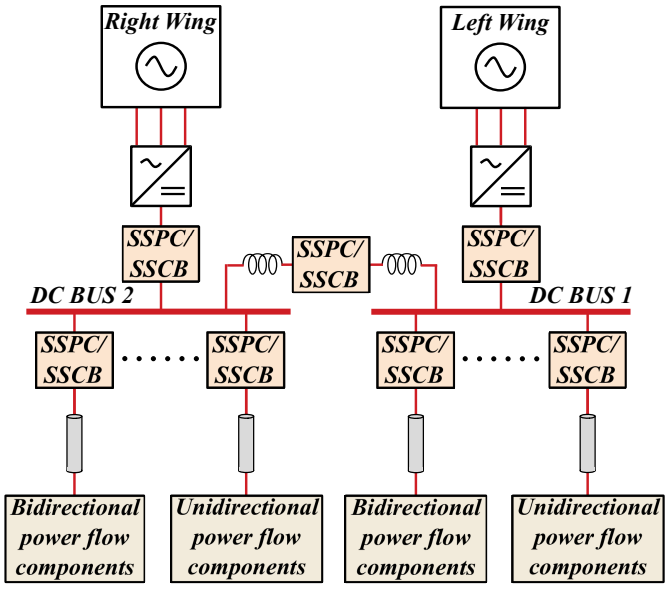


Figure 5.1: Simplified diagram of aircraft electrical system.

In Section 5.1, coupled inductor-based bidirectional ZSB topology is proposed. The proposed ZSB topology has lower power loss and has simple structure. Various operation modes of the proposed ZSB topology are explained in Section 5.1.1. Analysis of the proposed ZSB under fault condition is presented in Section 5.1.2. There are some limitations of ZSBs, and these are discussed in this chapter. In Section 5.2, a novel SCR-based SSPC/ SSCB topology is proposed. The key novelty is that the proposed topology has soft reclosing feature. Moreover, it overcomes the limitations of ZSBs. Various operation modes of the proposed topology are explained in Section 5.2.1. Equations of various key parameters are derived and its variation with circuit components values is analyzed, in Section 5.2.2 & 5.2.3. Simulation and experimental results for verification of the proposed topology are presented in Section 5.2.4. Summary of this work is discussed in Section 5.3.

5.1 Coupled Inductor–Based Bidirectional ZSB for DC Fault Protection

ZSBs are SCR-based SSPCs/ SSCBs, and these have been discussed in Section 2.3.2. One of the main advantages of ZSBs is that the shortcircuit fault is

automatically isolated, or in other words, the control command is not required to isolate the faulty section. This is achieved by making use of inductors and capacitors. These passive components are connected in such a way that the current through the SCR is forced to zero in case of fault condition. In this section, a novel ZSB topology is proposed, which is an evolution of exiting topologies. It has lower power loss compared to other ZSBs. Moreover, it has the same characteristics in both directions, for all values of inductors. In addition, the proposed topology has a simpler structure.

5.1.1 Proposed CI-BZSB Topology

The proposed Coupled Inductor–Based Bidirectional ZSB (CI-BZSB) topology is shown in Fig. 5.2. SCR_1 and SCR_2 are the main SCRs used for steady-state bidirectional power flow operation. SCR_3 and SCR_4 are auxiliary SCRs, which conduct only during fault condition. L_{11}, L_{12}, and C are two coupled inductors and a capacitor, respectively.

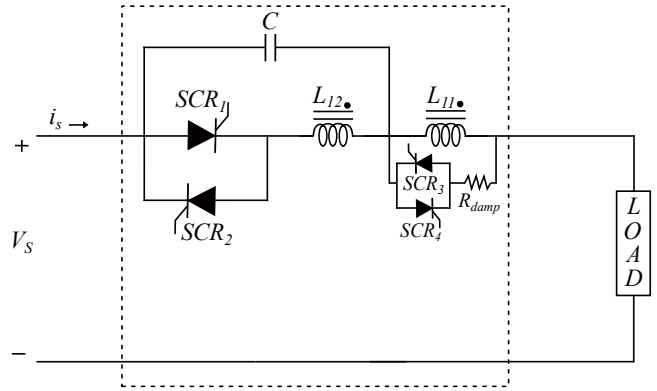


Figure 5.2: Coupled inductor based bidirectional Z-source breaker (CI-BZSB).

- During steady state condition, one of the two pairs of SCRs (SCR_1, SCR_3 or SCR_2, SCR_4) is gated depending on the direction of current flow. The gating signal to the main SCR (SCR_1 or SCR_2) is withdrawn once the current through the SCR exceeds the latching current, while the auxiliary SCR (SCR_3 or SCR_4) is continuously gated. In the example shown in Fig. 5.3, the load current flows through the path $V_S - SCR_1 - L_{12} - L_{11} - R_L$.

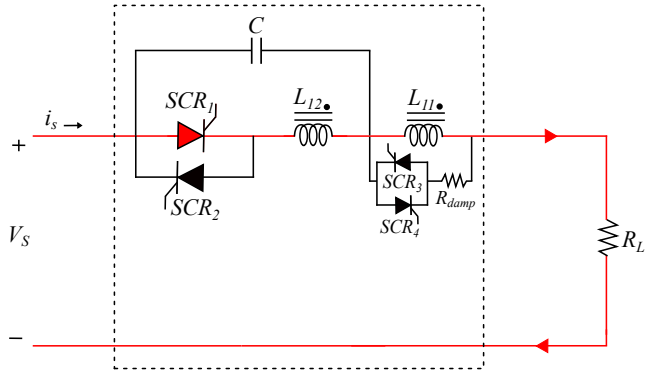


Figure 5.3: Steady-state interval of CI-BZSB.

- During fault condition, represented by a conductance of value G_{fault}, the source supplies the transient current through the high-frequency low-impedance current path $(V_s - C - L_{11})$ shown in Fig. 5.4. This transient current through the inductor L_{11} induces voltage across inductor L_{12}, such that the induced voltage opposes the original steady-state current flow through the SCR_1. As a result, SCR_1 current reaches zero, and thus, it commutates.

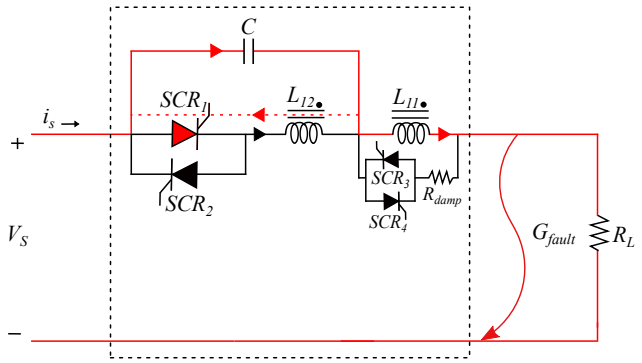


Figure 5.4: Fault condition of CI-BZSB.

- During the post-commutation stage, source, C, and L_{11} resonate, as shown in Fig. 5.5. Resonance continues until the voltage across the inductor L_{11} becomes negative. Thereafter, R_{damp} (damping resistor) and SCR_3 starts conducting, and this circuit dissipates the remaining inductor energy. After a short while, the current in this circuit decays to zero, and the capacitor voltage is equal to the source voltage. Hence, the source and faulty side are electrically isolated.

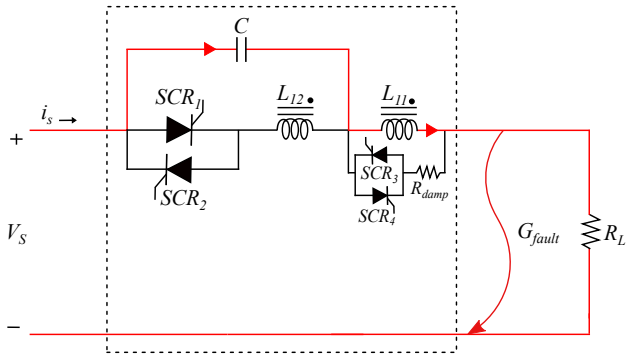


Figure 5.5: Post-commutation stage of CI-BZSB.

- In case of reverse power flow condition, SCR_2 and SCR_4 are used, and these are gated in a way similar to the SCR_s in the previous case. In case of a fault, the source supplies the transient current through the high-frequency low-impedance current path $(V_s - L_{11} - C)$, shown in Fig. 5.6. The induced voltage across L_{12}, opposes the steady-state current through SCR_2, consequently, SCR_2 commutates. Post-commutation stage is similar to the previous case.

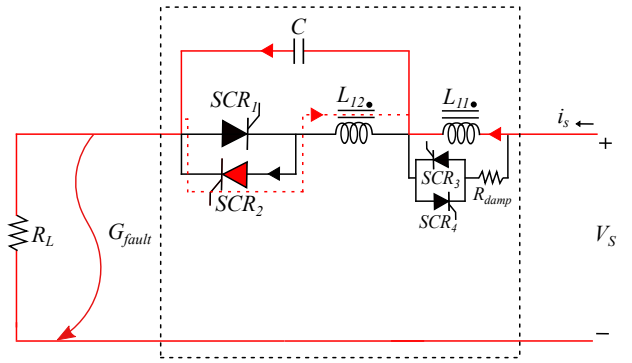


Figure 5.6: Fault condition during reverse power flow operation of CI-BZSB.

5.1.2 Design and Analysis of Proposed CI-BZSB

In this section, equations of SCR reverse recovery time and peak value of fault current are derived. Variation of these equations with respect to inductors and capacitor values, is also analysed. The expressions are derived with time origined at the fault instant. The expressions are valid for the time interval before the conduction of damping resistor. The parameter values used in this analysis are described in Table 5.1. The equivalent circuit for the analysis is shown in Fig. 5.7. SCR voltage drop has been assumed to be negligible. The inductor windings are assumed to be strongly

coupled ($K = 1$).

Table 5.1: Simulation Parameters for the Verification of CI-BZSB

Parameter	Value
Source voltage, V_s	270 V
Inductance, L_{11}	100 μH
Inductance, L_{12}	100 μH
Capacitance, C	220 μF
Load current, I_L	90 A

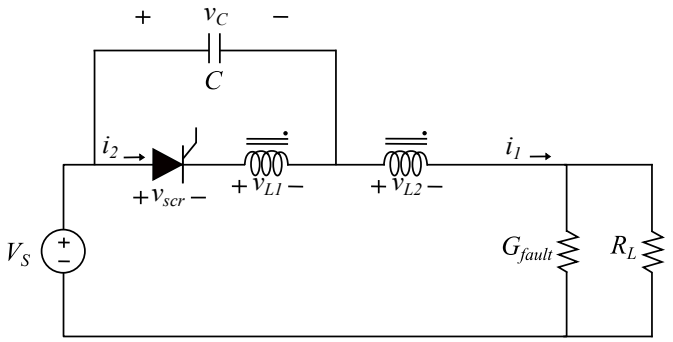


Figure 5.7: Equivalent circuit of CI-BZSB.

5.1.2.1 SCR Reverse Recovery Time

Immediately after the main SCR current reaches zero, the circuit imposes a negative voltage across this device for a certain time interval. This time interval is termed as reverse recovery time. During this interval, the device undergoes a reverse recovery of the charge carriers. Using Kirchoff's Voltage Law in Laplace domain, loop equations are derived. Applying the inverse Laplace transform to $V_{scr}(s)$, the variation of the voltage with time can be represented as,

$$v_{scr}(t) = \alpha + \frac{\beta \cos(\omega t) e^{-\delta t}}{L_{11} C} + \frac{(\gamma - \beta\delta) \sin(\omega t) e^{-\delta t}}{\omega L_{11} C} \tag{5.1}$$

where,

$$\alpha = V_s \tag{5.2}$$

$$\beta = (R_f \parallel R_L) I_{load} MC - V_s C(M + L_{11}) \tag{5.3}$$

$$\gamma = I_{load}(M + L_{11}) - V_s C(R_f \parallel R_L) \tag{5.4}$$

$$\delta = \frac{R_f \parallel R_L}{2L_{11}} \tag{5.5}$$

$$\omega = \sqrt{\frac{1}{L_{11}C} - \left(\frac{R_f \parallel R_L}{2L_{11}}\right)^2} \tag{5.6}$$

Equation (5.1) is solved numerically using Newton-Raphson method, to calculate the instant t_{off} at which $v_{scr}(t) = 0$. t_{off} represents the time interval during which the SCR voltage is negative. The value of t_{off} is calculated for different values of inductors and capacitor, shown in Fig. 5.8. Inductors L_{11} and L_{12} are assumed to be equal in this analysis. Inductors and capacitor should be sized such that t_{off} is greater than the turn off time value specified in the datasheet of the SCR. Inverter grade SCRs have turn off times in the range of few μs, and these are preferred because minimum requirement of inductors and capacitor values is less compared to standard SCRs.

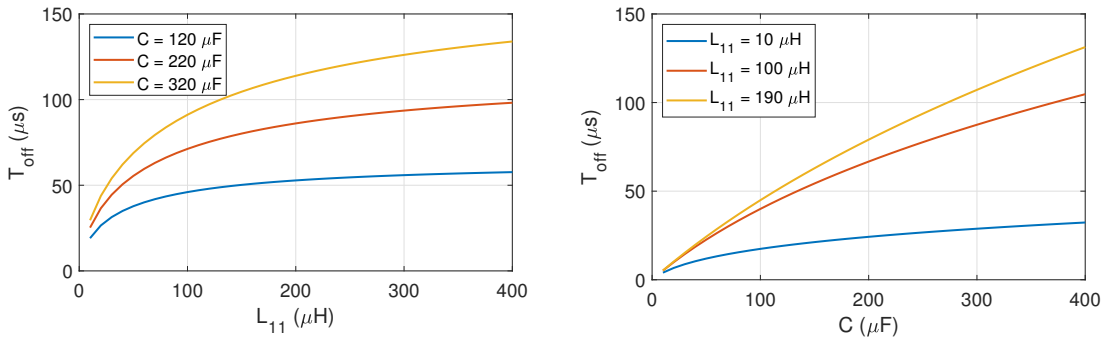


Figure 5.8: Variation in t_{off} versus variation in inductance and capacitance.

5.1.2.2 Peak Value of Fault Current Reflected to the Source Side

An analysis is performed to calculate the expression of $I_1(s)$. Applying the inverse Laplace transform to this equation, the source current variation with time can be

represented as,

$$i_1(t) = \alpha cos(\omega_d t)e^{-\delta t} + \beta sin(\omega_d t)e^{-\delta t} \tag{5.7}$$

where,

$$\alpha = \frac{2V_s}{R_L} \tag{5.8}$$

$$\beta = \frac{2V_s}{R_L \omega_d}\left(\frac{R_L}{2L_{11}} - \delta\right) \tag{5.9}$$

$$\omega_d = \sqrt{\frac{1}{L_{11}C} - \left(\frac{R_f \parallel R_L}{2L_{11}}\right)^2} \tag{5.10}$$

$$\delta = \frac{R_f \parallel R_L}{2L_{11}} \tag{5.11}$$

Differentiating equation (5.7) w.r.t t, equating it to zero and rearranging the terms of the resultant expression, the time instant, t_{max}, at which $i_1(t)$ reaches its maximum value can be calculated as,

$$t_{max} = \frac{1}{\omega_d} tan^{-1}\left(\frac{R_L\omega_d - 4L_{11}\delta\omega_d}{2L_{11}\omega_d^2 + \delta R_L - 2L_{11}\delta^2}\right) \tag{5.12}$$

Detailed derivation of (5.12) is presented in Appendix A. The peak value of the fault current reflected to the source side ($I_{1(max)}$) is calculated by substituting the value of t_{max} into (5.7). L_{11} and L_{12} have been assumed to be equal in this analysis. Variation in $I_{1(max)}$ for different values of inductors and capacitor is shown in Fig. 5.9.

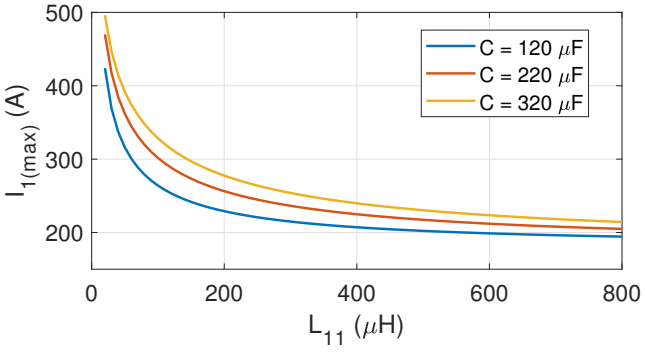
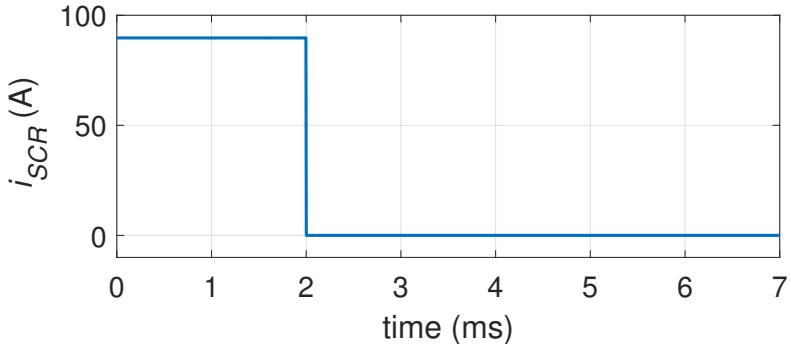


Figure 5.9: Variation in $I_{1(max)}$ versus variation in inductance and capacitance.

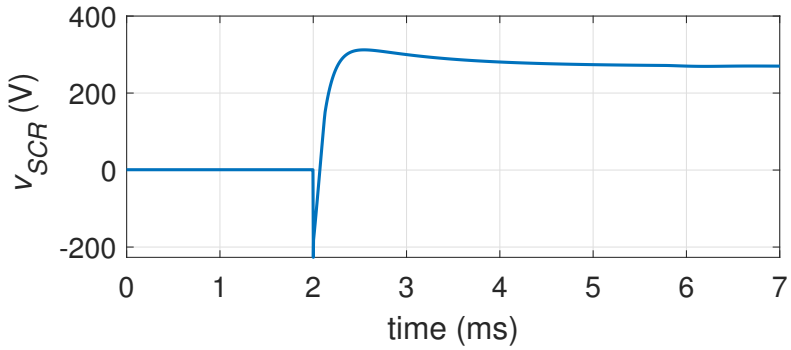
Simulations have been performed to verify the proposed topology, and the results are shown in Fig. 5.10. At $t = 2$ ms, a fault is initiated in the circuit, and it is realized using G_{fault} of value 2 Ω^{-1}, which is capable of generating a very high current. i_1 suddenly increases due to this fault. The CI-BZSB isolates the source and the fault, by forcing the SCR current to zero, as shown in Fig. 5.10(a). Subsequently, a negative voltage is imposed across the device, which helps in the reverse recovery of charge carriers, as shown in Fig. 5.10(b). The circuit components resonate until the voltage across the inductor L_{11} becomes negative, and accordingly, the current is diverted to the branch containing R_{damp} and SCR_3, shown in Figs. 5.10(c) and (d). Manual tripping for overload condition can be introduced by adding additional circuitry as suggested in [50,51]. A comparison of the proposed topology with existing bidirectionally symmetric topologies is shown in Table 5.2. The proposed topology has lower semiconductor power loss. Moreover, it has a simpler structure.

Table 5.2: ZSB Topologies Comparison

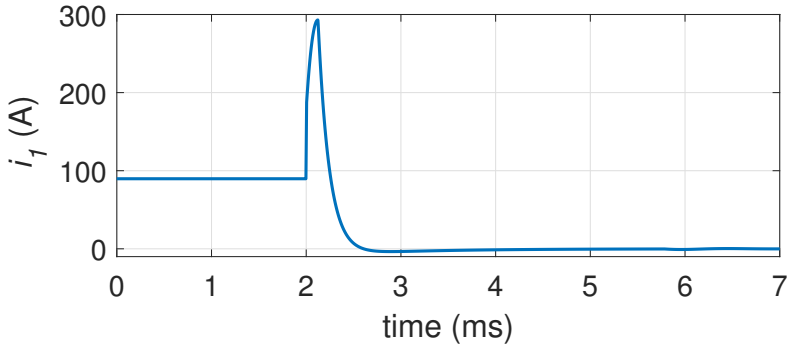
	Fig. 2.11(a)	Fig. 2.11(b)	Fig. 2.11(c)	Fig. 2.11(d)	Fig. 2.11(e)	Proposed topology
Reference	[66, 67]	[68]	[69]	[53]	[49]	-
Common ground	No	Yes	Yes	Yes	Yes	Yes
Number of power semiconductor devices	4	4	5	4	4	2
Number of inductors	2	2	2	4	3	2
Number of capacitors	2	3	2	1	1	1
Reflected fault current	Low	High	Medium	Low	Low	High
Semiconductor losses	Moderate	Moderate	High	Moderate	Moderate	Low



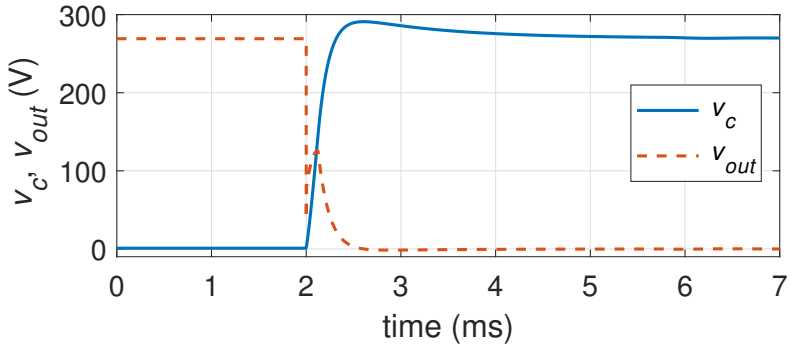
(a)



(b)



(c)



(d)

Figure 5.10: Simulation results for a fault condition.

5.2 SCR-Based Bidirectional SSPC/ SSCB with Soft Reclosing Capability

There are many existing SCR-based ZSB topologies, and these topologies have been discussed in previous section and Section 2.3.2. In the majority of existing ZSBs, the shortcircuit fault isolation mechanism is automatic and is highly dependent on the passive components used in the circuit. Automatic operation is advantageous in quickly isolating the fault. However, in an interconnected architecture, designing coordination is challenging. In addition, high-magnitude step-load changes can cause false tripping of the ZSB [9]. Thus, active control of the breaker, is an important functionality to ensure highly selective protection.

One of the recent SCR-based active SSPC/ SSCB topology is proposed in [6]. This topology is illustrated in Fig. 2.12(a), and its operating principle is discussed in Section 2.3.2. This topology is operated using low voltage signals from logic circuitry or micro-controller, thus, it has reliable trip-control mechanism. However, it does not have reclosing capability. In [7], a dc SSPC/ SSCB topology is proposed, which has the normal reclosing capability, this topology is discussed in Section 2.3.2, and is illustrated in Fig. 2.12(b). The main problem in these topologies is that the current and voltage stress during reclosing is very high.

In this section, an SCR-based bidirectional SSPC/ SSCB (SCR-BCB) topology is proposed. The proposed topology is able to isolate the faulty section with the initiation of a manual tripping command. Additionally, the proposed topology has soft reclosing capability, which helps in reducing stress on semiconductor devices, capacitors, surge suppression devices, and current feeding components. This capability is achieved by using a capacitor discharge approach [82]. The energy dissipated by the surge suppression devices during reclosing is negligible. In addition, multiple reclosing attempts are possible with no detrimental and adverse impact on the breaker as well as current feeding components.

Reclosing subsequent to fault isolation in ac grids, is very well standardized and practised [83, 84]. Analogous to ac grids, reclosing in dc grids is also considered as one of the essential requirements [18, 44, 83, 84]. In [9], reclosing is indicated as an important step in dc system protection process. Normal reclosing in case of a permanent fault causes high stress on power electronic components, surge suppression devices and fault current feeding components due to repeated surge events. Moreover,

it leads to oversizing of the breaker as well as system components. Hence, it is important to determine the nature of the fault prior to performing a reclosing attempt [85]. This technique is known as soft reclosing [86]. Various soft reclosing methods have been proposed in the literature. However, most of these methods either require complex converter control or are based on HCBs [18, 87].

5.2.1 Proposed SCR-BCB Topology

The proposed SCR-BCB topology is shown in Fig. 5.11. SCR_1, SCR_2, SCR_3, and SCR_4 are the main SCRs used for conducting the load current. SCR_5 and SCR_6 are secondary commutation SCRs used for fault isolation. C is a negative current injecting capacitor, used for commutating the main SCR. R_2 is a resistor with a very large resistance value, used for limiting the inrush current during the initial charging of the capacitor. It also provides a path for the capacitor to remain connected with the source during steady-state operation. BS is a bidirectional switch, which is used during soft reclosing, and is connected in series with R_1. There are many different ways in which a BS can be realized such as a mechanical switch, anti-series configuration of transistors, diode bridge and transistor, anti-parallel configuration of transistors, and anti-parallel configuration of SCRs. A mechanical switch has been utilized in this study. A TVS diode is used as a clamping circuit because it offers superior characteristics compared to metal oxide varistors (MOVs) [10]. In high power applications, the TVS diode can be replaced with a MOV due to lower cost [10, 71] and higher energy dissipation capability. However, MOVs degrade with surge events, and hence, these have limited lifetimes [10].

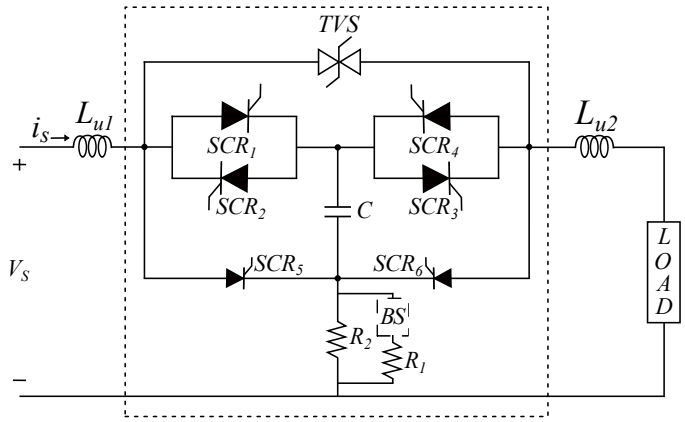


Figure 5.11: Proposed SCR-BCB topology.

The breaker operation is divided into two intervals: fault isolation and soft reclosing. To facilitate the analysis, steady-state current is assumed to flow in the direction indicated in Fig. 5.12(b). These intervals are explained as follows,

- *Fault isolation*

  - *Charging subinterval:* SCR_1 is continuously gated to charge the capacitor (C) through the path $V_s - L_{\mu 1} - SCR_1 - C - R_2$, shown in Fig. 5.12(a). The SCR behaves similar to a diode when gated continuously [88]. BS remains in open circuit for the entire fault isolation interval.

  - *Steady-state subinterval:* Once the capacitor is fully charged, SCR_3 is triggered by a gate pulse to supply the load current through the path $V_s - L_{\mu 1} - SCR_1 - SCR_3 - L_{\mu 2} - Load$, as shown in Fig. 5.12(b).

  - *Fault subinterval:* During fault condition, the current flowing through the circuit rises very rapidly. There are many fault detection algorithms in the existing literature, which can detect faults in the range of a few microseconds [9, 34, 89–91]. Once a fault is detected, SCR_5 is triggered by a gate pulse to initiate the fault isolation process. The capacitor imposes a negative voltage across SCR_1, and opposes the current flow through SCR_1. Consequently, SCR_1 current reaches a value lower than the holding current. Thereafter, SCR_1 undergoes reverse recovery of charge carriers due to which it regains its forward blocking capability.

  - *Resonance subinterval:* During the post commutation stage, $V_s - L_{\mu 1} - SCR_5 - C - SCR_3 - L_{\mu 2} - Load$ resonate for a short time, illustrated in Fig. 5.12(c). Resonance continues until either $i_s \approx 0$ & $|V_C| < V_{BR}$ or $i_s > 0$ & $|V_C| = V_{BR}$, where V_{BR} is the breakdown voltage of the TVS diode. In the latter case, the current is diverted to the TVS diode (clamping subinterval). SCR_3 and SCR_5 naturally commutate in either of the above cases, since the current through these devices reaches a value lower than the holding current.

  - *Clamping subinterval:* During this interval, the TVS diode conducts to dissipate the remaining energy stored in the line inductor, as shown in Fig. 5.12(d).

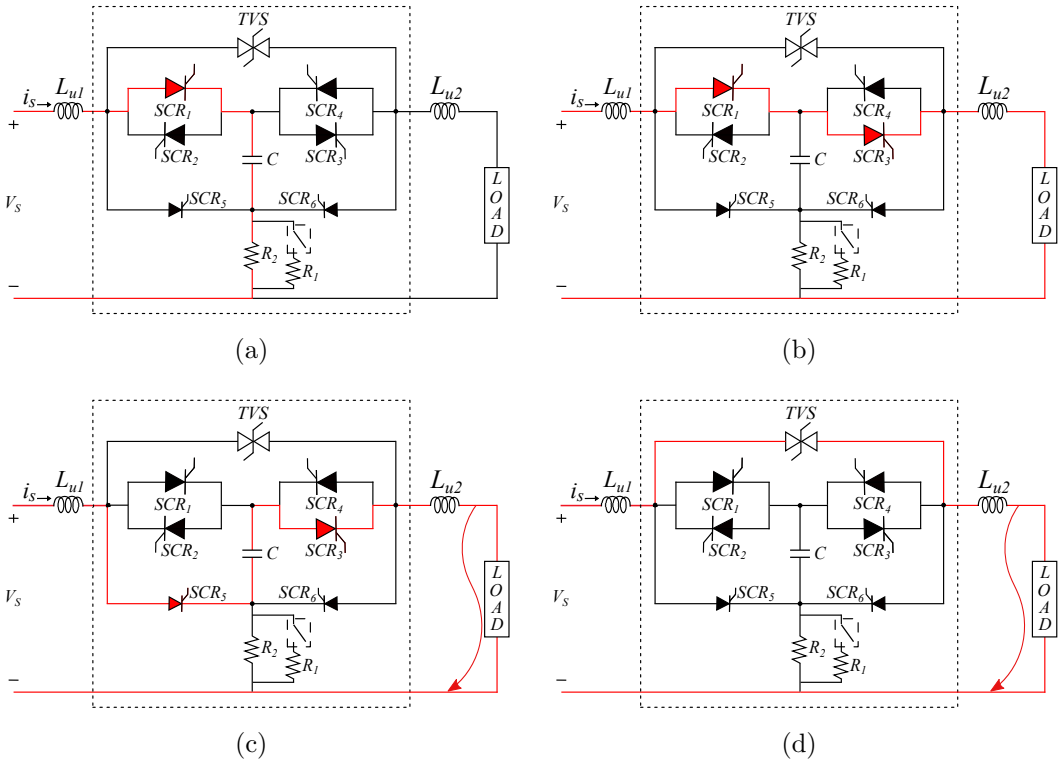


Figure 5.12: Operation modes of the proposed SCR-BCB. (a) Charging subinterval, (b) steady state subinterval, (c) resonance subinterval, and (d) clamping subinterval.

- *Soft reclosing*

  Reclosing subsequent to fault isolation, is important to determine the nature of the fault, and to reduce the downtime in the event of temporary faults. Normal reclosing causes high stress on the breaker and the current feeding components [18,86,87]. To overcome this limitation, the proposed topology has soft reclosing capability. Several soft reclosing methods have been proposed in the literature. However, most of these methods are either proposed for HCBs or require complex converter control [18,87].

  – *Capacitor charge subinterval:* BS is switched from open circuit to closed circuit. SCR_1 is gated to charge the capacitor through the path $V_s - L_{\mu 1} - SCR_1 - C - R_1||R_2$, shown in Fig. 5.13(a).

  – *Capacitor discharge subinterval:* SCR_3 is gated to discharge the capacitor, shown in Fig. 5.13(b). The load side inductor current and load voltage are the key indicators of the nature of the fault. In the case of a temporary fault, the peak value of the load current is lower, and the peak value of

load voltage is higher compared to a permanent fault.

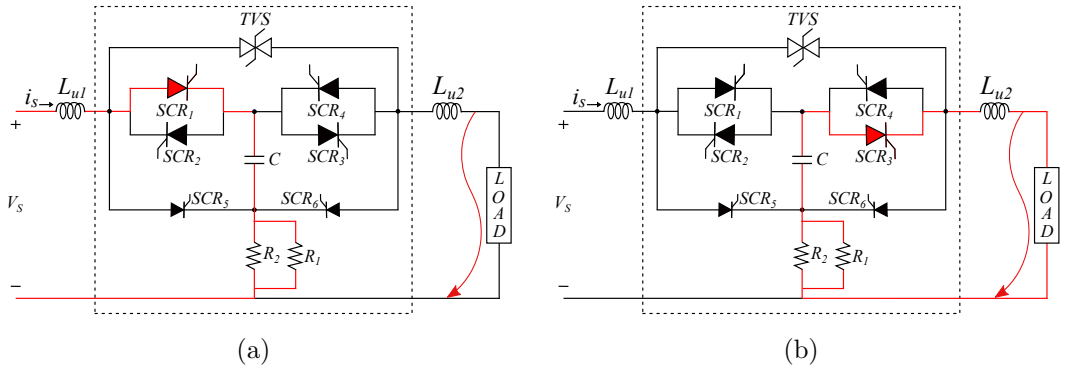


Figure 5.13: Soft reclosing modes of the proposed SCR-BCB. (a) Capacitor charge subinterval and (b) capacitor discharge subinterval.

Regular maintenance and servicing of the components, necessitates the breaker to trip during normal operating conditions. This can be realized by triggering SCR_5 when required. As the topology is symmetric, the analysis in the reverse power flow is similar to the case presented above.

5.2.2 Fault Analysis of Proposed SCR-BCB

In this section, expressions of reverse recovery time, peak value of fault current, and fault clearing time, are derived and analyzed for a worst-case scenario of short-circuit fault. Reverse recovery time is dependent on the circuit parameters, and it should be greater than the turn-off time specified in the datasheet of the SCRs, to ensure that the SCR is completely turned off. The peak value of the fault current and fault clearing time are also important parameters because these affect the design and performance of interfaced power electronic converters [9]. Conducting and non-conducting SCRs are considered as short circuit and open circuit, respectively. The effect of voltage, current, and frequency change on the inductance value, is neglected in this analysis. In this section, the value of L is equal to the sum of the inductance on the source side $L_{\mu 1}$ and the load side $L_{\mu 2}$. The source is represented as a constant dc voltage because it is the worst case scenario as the fault current is the maximum in this case. This type of source representation is used for initial circuit-level design, analysis, and testing of dc circuit breakers [18, 92]. The parameters used in this section are described in Table 5.3.

5.2.2.1 Reverse Recovery Time

Immediately after the secondary commutation SCR (SCR_5 or SCR_6) is triggered, the current flowing through the main SCR (SCR_1 or SCR_4) is forced to zero. The capacitor imposes a negative voltage across the main SCR for reverse recovery of charge carriers. Consequently, the main SCR regains its forward blocking capability. Reverse recovery time (t_{rr}) is defined as this time interval during which the voltage across the main SCR (SCR_1 or SCR_4) is negative, as shown in Fig. 5.14.

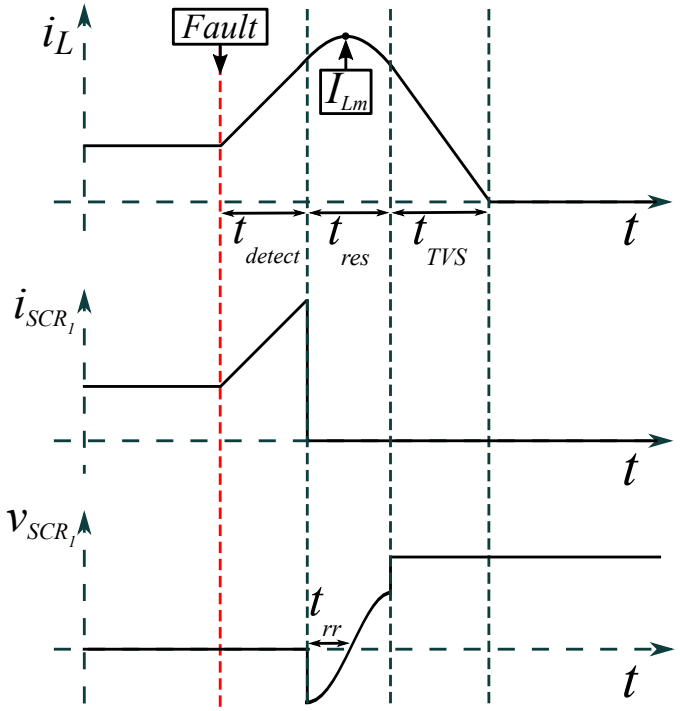


Figure 5.14: Current and voltage waveforms during fault isolation process.

Without the loss of generality, the expressions are derived with the time origined at the start of the resonance subinterval. The equivalent circuit during this interval is shown in Fig. 5.15. The main current conduction path in this interval is highlighted in red. v_{SCR} is the voltage across the SCR_1, which is undergoing a reverse recovery of charge carriers. i_L is the load side inductor current, v_c is the voltage across the capacitor, v_{L1} is the voltage across the inductor $L_{\mu 1}$, and v_{L2} is the voltage across the inductor $L_{\mu 2}$. The current flowing through the inductor during the previous interval (fault condition), follows the expression,

$$V_s = L\frac{di_L}{dt}. \tag{5.13}$$

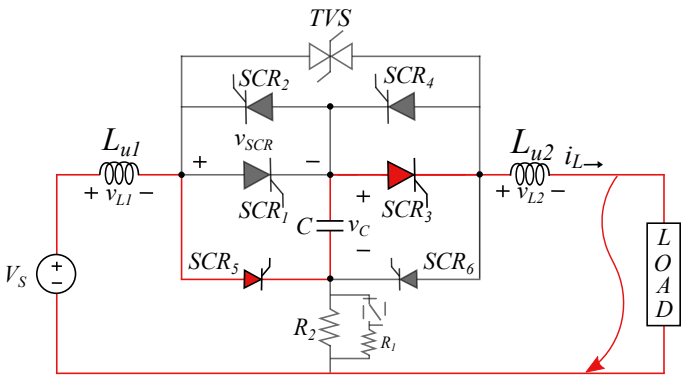


Figure 5.15: Equivalent circuit during the resonance subinterval.

Table 5.3: Experimental Parameters for Verification of SCR-BCB

Parameter	**Value**
Source voltage, V_s	50 V
Load resistance	25 Ω
Fault resistance	≈ 0.75 Ω
Line inductance, $L_{\mu 1}, L_{\mu 2}$	360 μH
Capacitance, C	60 μF
Fault isolation delay, t_{detect}	400 μs
Resistance, R_2	2.2 kΩ
Resistance, R_1	20 Ω
TVS breakdown voltage, V_{BR}	73.4 V
TVS diode resistance, R_{BR}	2.938 Ω
TVS diodes in parallel, N	4
Turn-off time, t_q	10 μs
SCR part number	S7412M

The rate of change of fault current $\left(\frac{di_L}{dt}\right)$ is dependent on the source voltage and line inductor value. Integrating (5.13), the inductor current at the start of the resonance subinterval, denoted by $I_{Lres}(0)$, can be calculated as,

$$I_{Lres}(0) = i_{Load} + \frac{V_s t_{detect}}{L}, \tag{5.14}$$

where t_{detect} is the fault isolation delay (time required to detect the fault) and i_{Load} is the steady-state load current. Using Kirchhoff's voltage law, v_{SCR} in the Laplace domain, during resonance interval, can be calculated as,

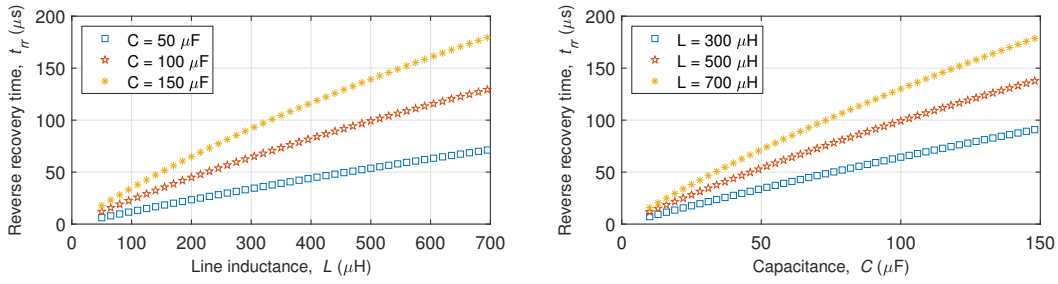
$$V_{SCR}(s) = \frac{-V_s LCs^2 + LI_{Lres}(0)s + V_s}{s(LCs^2 + 1)} \tag{5.15}$$

Applying the inverse Laplace transform, variation in the voltage across the SCR with time, can be calculated as,

$$v_{SCR}(t) = V_s - 2V_s \cos(\omega t) + \frac{I_{Lres}(0)\sin(\omega t)}{\omega C} \tag{5.16}$$

where $\omega = \frac{1}{\sqrt{LC}}$.

Eq. (5.16) is solved numerically using Newton-Raphson method, to calculate the instant t_{rr} at which $v_{SCR}(t) = 0$. The error band for the numerical method is 0.1 ns. The time t_{rr} for different values of capacitor and line inductor, is shown in Fig. 5.16. The capacitor should be sized such that the value of t_{rr} is greater than the turn off time (t_q) specified in the data sheet of the SCR. R_2 should be sized such that the current flowing through the secondary commutation SCR (SCR_5 or SCR_6) drops below the holding current by the end of the resonance subinterval.



(a) (b)

Figure 5.16: Variation in reverse recovery time (t_{rr}) versus capacitance and line inductance.

5.2.2.2 Peak Value of Fault Current

The fault current, which is equal to the current flowing through the inductors, attains its peak value I_{Lm} during the resonance subinterval because the capacitor voltage (same as SCR voltage) changes from a positive value to a negative one in this interval, as shown in Fig. 5.14. Using Kirchhoff's voltage law, i_L in the Laplace

domain during resonance interval, can be calculated as,

$$I_{Lres}(s) = \frac{2V_sC + LCsI_{Lres}(0)}{LCs^2 + 1} \tag{5.17}$$

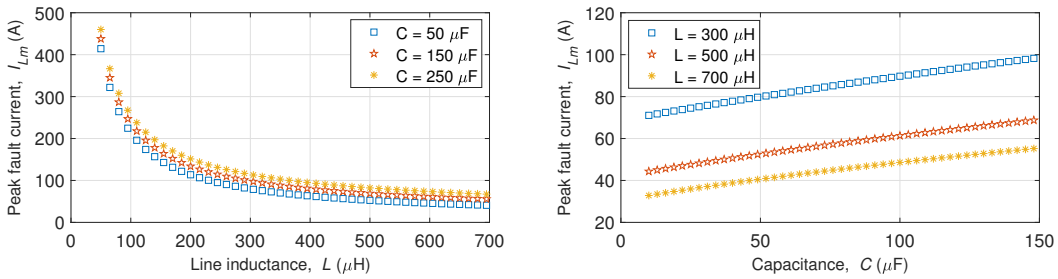
Applying the inverse Laplace transform, the variation in inductor current with time, can be calculated as,

$$i_{Lres}(t) = \frac{2V_s}{\omega L}\sin(\omega t) + I_{Lres}(0)\cos(\omega t) \tag{5.18}$$

Differentiating (5.18) and equating it to zero, the time instant at which I_{Lm} occurs can be calculated as,

$$t_{max} = \frac{tan^{-1}\left[\frac{2V_s}{\omega L I_{Lres}(0)}\right]}{\omega} \tag{5.19}$$

I_{Lm} is calculated for different values of capacitor and line inductor by substituting the value of t_{max} into (5.18), as shown in Fig. 5.17. A higher value of line inductor is advantageous, as the capacitance value needed is reduced for a given t_{rr} requirement. Moreover, the peak value of the fault current is also reduced.



(a) (b)

Figure 5.17: Variation in peak fault current (I_{Lm}) versus capacitance and line inductance.

5.2.2.3 Fault Clearing Time

The fault clearing time (t_{fc}) is defined as the time interval starting at fault occurrence, and until the current flowing in the circuit decays to zero. t_{fc} is divided into three subintervals, which can be mathematically expressed as,

$$t_{fc} = t_{detect} + t_{res} + t_{TVS} \tag{5.20}$$

where t_{detect} is the fault isolation delay, which is defined as the time required to detect the fault and send the tripping signal to the breaker. t_{detect} varies in the range of few μs to ms [18, 34, 91]. t_{detect} has been assumed to be 400 μs in this section. t_{res} is the resonance time interval, and t_{TVS} is the clamping time interval.

1. Resonance Time Interval

   t_{res} is defined as the time interval, which starts at the instant at which secondary commutation SCR is triggered to initiate the fault isolation process, and ends at the instant at which the voltage across the capacitor reaches the breakdown voltage of the TVS diode, as shown in Fig. 5.14. Hence, t_{res} satisfies the equality,

$$v_{SCR}(t_{res}) = V_{BR} \tag{5.21}$$

   where time is origined at the start of the resonance interval. Substituting (5.16) in (5.21), it becomes:

$$(V_s - V_{BR}) - 2V_s \cos(\omega t_{res}) + \frac{I_{Lres}(0)\sin(\omega t_{res})}{\omega C} = 0 \tag{5.22}$$

   Since (5.22) is an implicit function of time, t_{res} is solved numerically using Newton-Raphson method. t_{res} is a root of the function

$$f(t) = v_{SCR}(t) - V_{BR} \tag{5.23}$$

Using (5.23), the mathematical formulation of the Newton-Raphson method, can be expressed as,

$$t_{res}^{n+1} = t_{res}^{n} - \frac{f(t_{res}^{n})}{f'(t_{res}^{n})} \tag{5.24}$$

substituting $n = 0$ in (5.24),

$$t_{res}^{1} = t_{res}^{0} - \frac{f(t_{res}^{0})}{f'(t_{res}^{0})} \tag{5.25}$$

where t_{res}^{0} is the initial estimate of the actual solution. Subsequently, t_{res}^{2} is calculated by substituting the value of t_{res}^{1} from (5.25) into (5.24). This process is continued until the condition: $t_{res}^{n+1} - t_{res}^{n} < 0.1$ ns is satisfied. The calculated values of t_{res} are substituted into (5.20).

2. Clamping Time Interval

t_{TVS} is defined as the time interval during which the TVS diode conducts to force the current flowing in the circuit to zero, as shown in Fig. 5.14. The equivalent circuit during this interval is shown in Fig. 5.18. The TVS diode is modeled as a voltage source in series with a resistor [71]. R_{BR} incorporates the effect of increase in the voltage with the increase in the current flowing through its terminals.

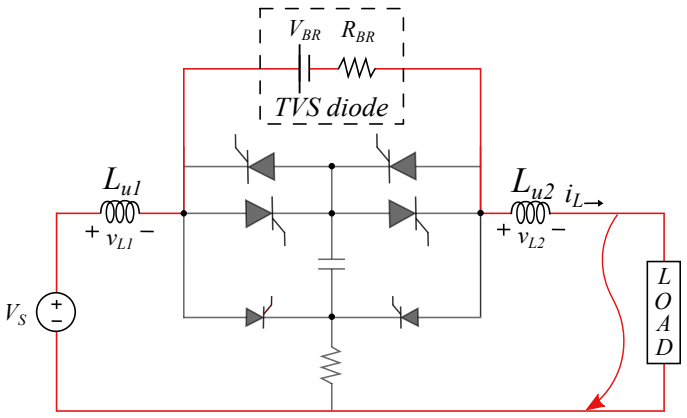


Figure 5.18: Equivalent circuit during the clamping subinterval.

The expressions are calculated with the time origined at the start of this interval. Using Kirchhoff's voltage law, i_L in the Laplace domain during the clamping interval, can be calculated as,

$$I_{LTVS}(s) = \frac{(V_s - V_{BR}) + Ls\, i_{Lres}(t_{res.})}{s(Ls + \frac{R_{BR}}{N})} \tag{5.26}$$

Applying inverse Laplace transform, variation in inductor current with time can be calculated as,

$$i_{LTVS}(t) = \frac{(V_s - V_{BR})N}{R_{BR}}(1 - e^{-\alpha t}) + i_{Lres}(t_{res}) \tag{5.27}$$

where

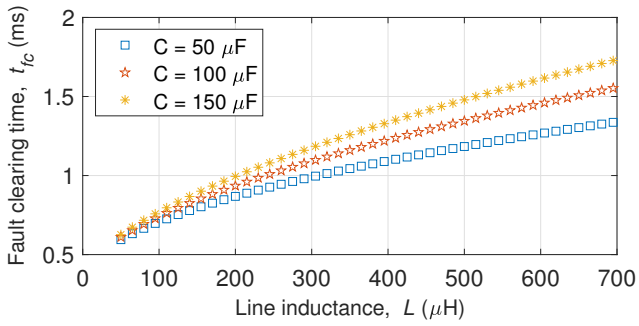
$$\alpha = \frac{R_{BR}}{NL} \tag{5.28}$$

Imposing (5.27) to zero, and rearranging the terms, t_{TVS} can be mathematically expressed as,

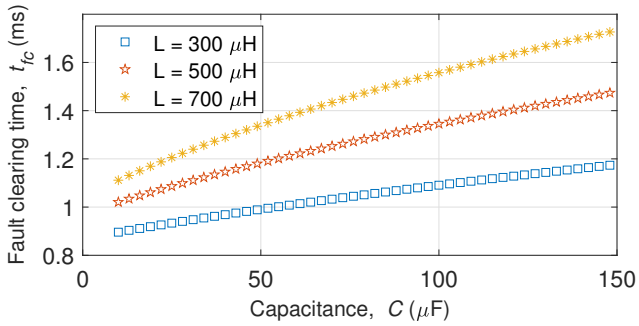
$$t_{TVS} = \frac{\log_e \beta}{\alpha} \tag{5.29}$$

where $\beta = 1 - \left(\frac{i_{Lres}(t_{res})}{A}\right)$.

t_{fc} is calculated for different values of line inductor and capacitor using (5.22) and (5.29), as shown in Fig. 5.19. The times t_{fc}, t_{res} and t_{TVS}, increase with the increase in the value of inductors and capacitor. In case of a fixed value of line inductor, the t_{fc} can be reduced by reducing the value of capacitor.



(a)



(b)

Figure 5.19: Variation in fault clearing time (t_{fc}) versus capacitance and line inductance.

Table 5.4: Simulation Parameters for Verification of SCR-BCB

Parameter	**Value**
Source voltage, V_s	270 V
Load resistance	2.7 Ω
Line inductance, $L_{\mu 1}, L_{\mu 2}$	360 μH
Capacitance, C	20 μF
Fault isolation delay, t_{detect}	400 μs
Resistance, R_2	20 kΩ
Resistance, R_1	10 Ω
TVS breakdown voltage, V_{BR}	422 V
TVS diode resistance, R_{BR}	98 mΩ

5.2.3 Soft Reclosing Analysis

In this section, expressions of current during capacitor charge and capacitor discharge subintervals, are derived and analyzed. Since $R_1 << R_2$, $R_1||R_2$ has been assumed to be approximately equal to R_1 for simplification purposes. The current paths during capacitor charge and discharge subintervals are shown in Figs. 5.13(a)

and (b), respectively. Using Kirchhoff's voltage law in Laplace domain, the source current during the capacitor charge subinterval, can be calculated as,

$$I_s(s) = \frac{(V_s + V_c)}{L_{\mu 1}\left(s^2 + \frac{R_1 s}{L_{\mu 1}} + \frac{1}{L_{\mu 1} C}\right)} \tag{5.30}$$

where V_c is the voltage across the capacitor prior to capacitor charge subinterval. Imposing, the discriminant of the quadratic equation in the denominator, to be greater than zero. The inequality can be mathematically expressed as follows:

$$R_1^2 > \frac{4L_{\mu 1}}{C} \tag{5.31}$$

In order to prevent any current oscillation, (5.31) is satisfied while sizing the components. Using Kirchhoff's voltage law, the load side inductor current during capacitor discharge subinterval can be calculated as,

$$i_L(t) = \frac{V_s}{\sqrt{\left((R_\beta)^2 - \frac{4L_{\mu 2}}{C}\right)}}(e^{(\alpha_2 t)} - e^{(\alpha_1 t)}) \tag{5.32}$$

where

$$\alpha_2, \alpha_1 = \frac{-R_\beta \pm \sqrt{(R_\beta)^2 - \frac{4L_{\mu 2}}{C}}}{2L_{\mu 2}} \tag{5.33}$$

$$R_\beta = R_1 + R_f || R_l \tag{5.34}$$

R_f is the fault resistance, and R_l the load resistance. Differentiating (5.32) and equating it to zero, the time instant at which the peak value of the load side inductor current (I_m) occurs, can be calculated as,

$$t_m = \frac{ln\left(\frac{\alpha_2}{\alpha_1}\right)}{(\alpha_1 - \alpha_2)} \tag{5.35}$$

Substituting the value of t_m into (5.32), I_m can be calculated as,

$$I_m = \frac{V_s}{\sqrt{\left((R_\beta)^2 - \frac{4L_{\mu 2}}{C}\right)}} \left(e^{\left(\frac{\alpha_2 ln(\frac{\alpha_2}{\alpha_1})}{(\alpha_1 - \alpha_2)}\right)} - e^{\left(\frac{\alpha_1 ln(\frac{\alpha_2}{\alpha_1})}{(\alpha_1 - \alpha_2)}\right)} \right) \tag{5.36}$$

I_m varies depending on the nature of the fault. Hence, it is used as an indicator to discriminate between temporary and permanent fault.

5.2.4 Prototype Description and Performance Validation

Simulations in LTspice platform, and experiments on a scaled-down laboratory prototype, are carried out to verify the fault isolation and soft reclosing capability of the breaker. The parameters used are specified in Tables 5.3 and 5.4. These simulation results are obtained using source voltage value of 270 V. The value of source voltage for the experiments is selected in such a way that it is less than the breakdown voltage of the TVS diode. A picture of the hardware setup is illustrated in Fig. 5.20. TMDSDOCK28335 microcontroller from Texas Instruments, is used in the hardware setup. This microcontroller has a clock frequency of 150 MHz, and the value of million-instructions-per-second is 150. Inverter grade SCRs [93] are selected because of their fast recovery time compared to standard SCRs. A line inductance is connected in series with the breaker to limit the rate of rise of fault current. The capacitor is sized such that the inequality: $t_{rr} > t_q$ is satisfied. R_2 is sized such that the current flowing through the auxiliary commutation SCR reaches a value lower than the holding current, by the end of the resonance subinterval. R_1 is sized such that (5.31) is satisfied. The gating sequence of the SCRs is shown in Fig. 5.21. Experimental results are presented in this section, and these are obtained using fault resistance of value $\approx 0.75\ \Omega$. Simulation and experimental results are divided into various time intervals, and are correlated with the operating modes specified in Section 5.2.1.

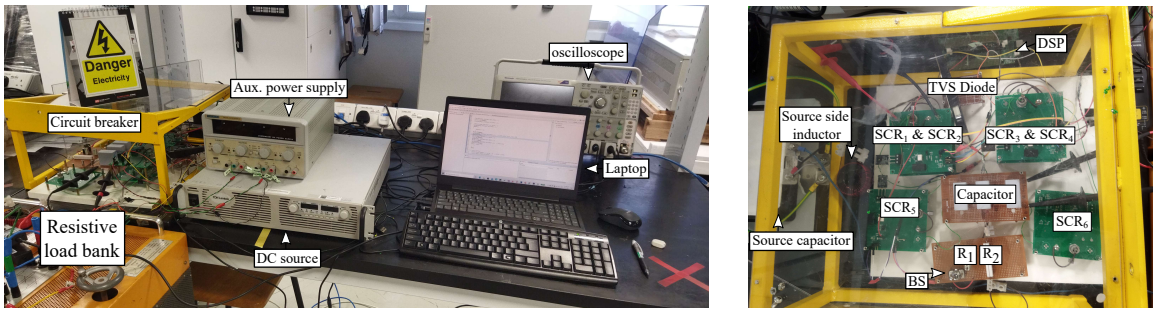


Figure 5.20: (a) Experimental setup and (b) circuit breaker.

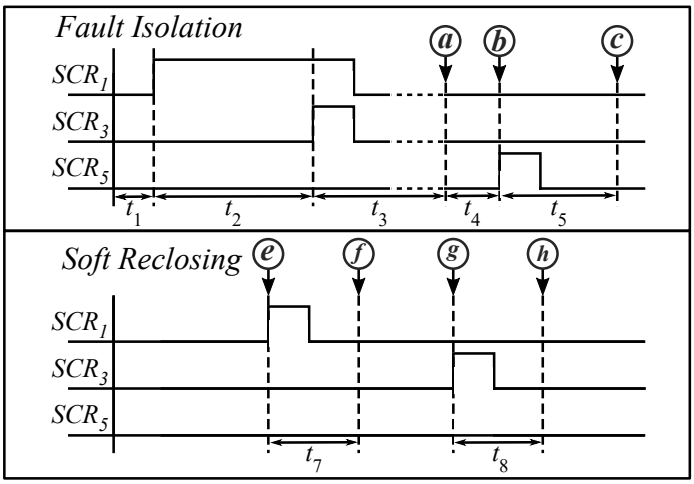


Figure 5.21: Gating sequence of the SCRs.

- *Fault isolation capability*

  – During the subinterval t_1 or off-state, source and load are electrically isolated from each other. The voltage across the SCR_1 is V_s, and C has no charge, as shown in Figs. 5.22 and 5.23(a).

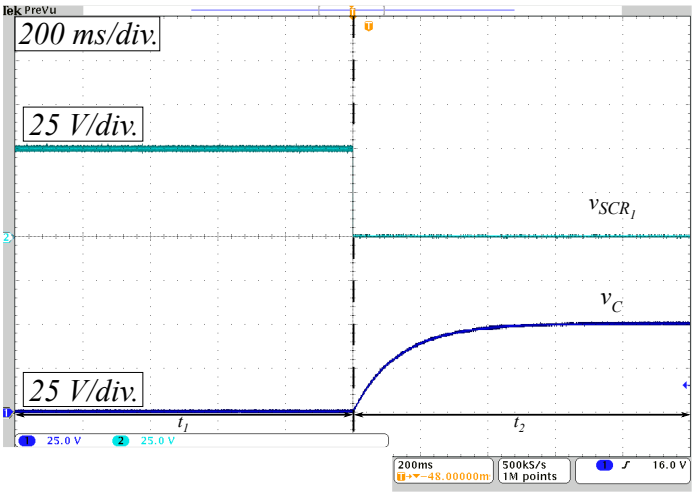
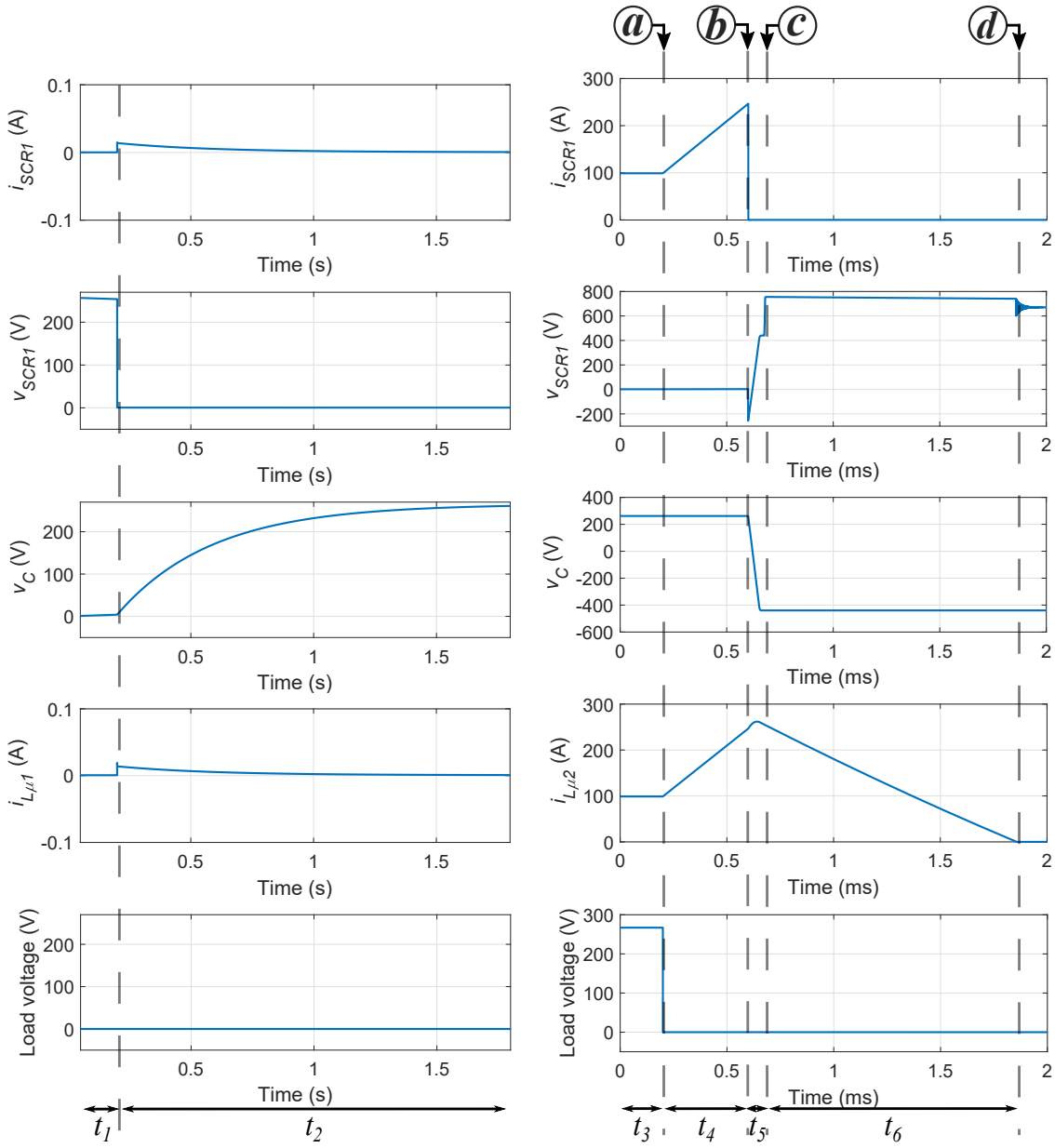


Figure 5.22: Experimental results for charging subinterval.



(a) (b)

Figure 5.23: Simulation results[1] for: (a) Charging interval and (b) fault condition.
[1]Current and voltage waveforms shown in Fig. 5.23(b) is advanced by a value of 2.1s from the origin defined in Fig. 5.23(a).

– During the subinterval t_2 or charging subinterval, SCR_1 is gated for 4 s as this value is greater than 4τ $(\tau = R_2C)$. By the end of this interval, C is charged to a value approximately equal to the source voltage, as shown in Figs. 5.22 and 5.23(a).

– During the subinterval t_3 or steady-state subinterval, SCR_3 is triggered for 10 μs to initiate the flow of load current, as shown in Figs. 5.24 and 5.23(b).

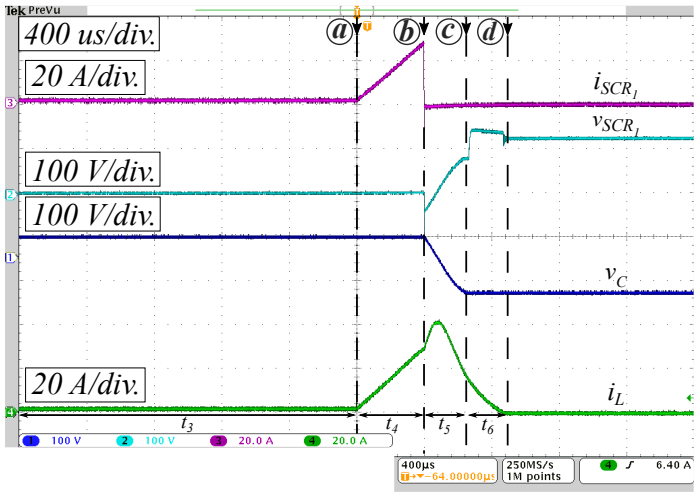


Figure 5.24: Experimental results for fault condition.

– During the subinterval t_4 or fault subinterval, a fault is initiated at time instant labeled as ⓐ. The current flowing through the circuit rises very rapidly, as shown in Figs. 5.24 and 5.23(b). It is assumed that the fault isolation delay is 400 μs, represented by time instant labeled as ⓑ. At this instant, SCR_5 is triggered for a time interval of 50 μs to initiate the fault isolation process. The current flowing through SCR_1 is forced to zero, and a negative voltage is imposed across the device to facilitate the reverse recovery of the charge carriers.

– During the subinterval t_5 or resonance subinterval, the breaker and circuit components resonate, as shown in Figs. 5.24 and 5.23(b). At the time instant labeled as ⓒ, the voltage across the capacitor reaches the value of V_{BR}, signifying the end of the resonance subinterval. Thereafter, the current flowing through the circuit is diverted to the TVS diode, which starts dissipating the remaining energy stored in the line inductor. SCR_3 and SCR_5 naturally commutate due to this transfer of current to the TVS diode.

- During the subinterval t_6 or clamping subinterval, the TVS diode conducts to clamp the voltage across the capacitor, and simultaneously dissipate the remaining energy stored in the line inductors $L_{\mu 1}$ and $L_{\mu 2}$, as shown in Figs. 5.24 and 5.23(b). At the time instant labeled as ⓓ, the current flowing through the inductor decays to zero. Hence, the source and load sides are electrically isolated from each other.

- *Soft reclosing capability*

  - During the subinterval t_7 or capacitor charge subinterval, SCR_1 is gated at the time instant labeled as ⓔ to charge the capacitor, as shown in Figs. 5.25(a) and 5.26(a). At the time instant labeled as ⓕ, the capacitor is charged to a value approximately equal to the source voltage.
  - Experimental results for capacitor discharge subinterval (t_8) in case of permanent and temporary faults are shown in Figs. 5.25(b) and (c), respectively. Simulation results for capacitor discharge subinterval are shown in Fig. 5.26(b). At the time instant labeled as ⓖ, SCR_3 is triggered to discharge the capacitor. The peak value of the load side inductor current is used as an indicator of the nature of the fault, which is much higher in the case of permanent faults compared to temporary faults. Experimental results for normal reclosing in case of a permanent fault is shown in Fig. 5.25(d). Stress on the semiconductor devices, TVS diode and fault current feeding components, in the event of a permanent fault, is much higher in the case of normal reclosing than soft reclosing.

The current and voltage waveforms during the load current breaking operation are shown in Fig. 5.25(e). SCR_5 is triggered at the time instant labelled as ⓘ to initiate the process. During the time interval t_a, the current flows through the path $V_s - L_{\mu 1} - SCR_5 - C - SCR_3 - L_{\mu 2} - LOAD$. The load current decays to zero at the time instant labelled as ⓙ. Hence, the source and load sides are electrically isolated from each other. Fig. 5.25(f) shows experimental results for a step change in the load current. The effect of the step change on the capacitor voltage is negligible.

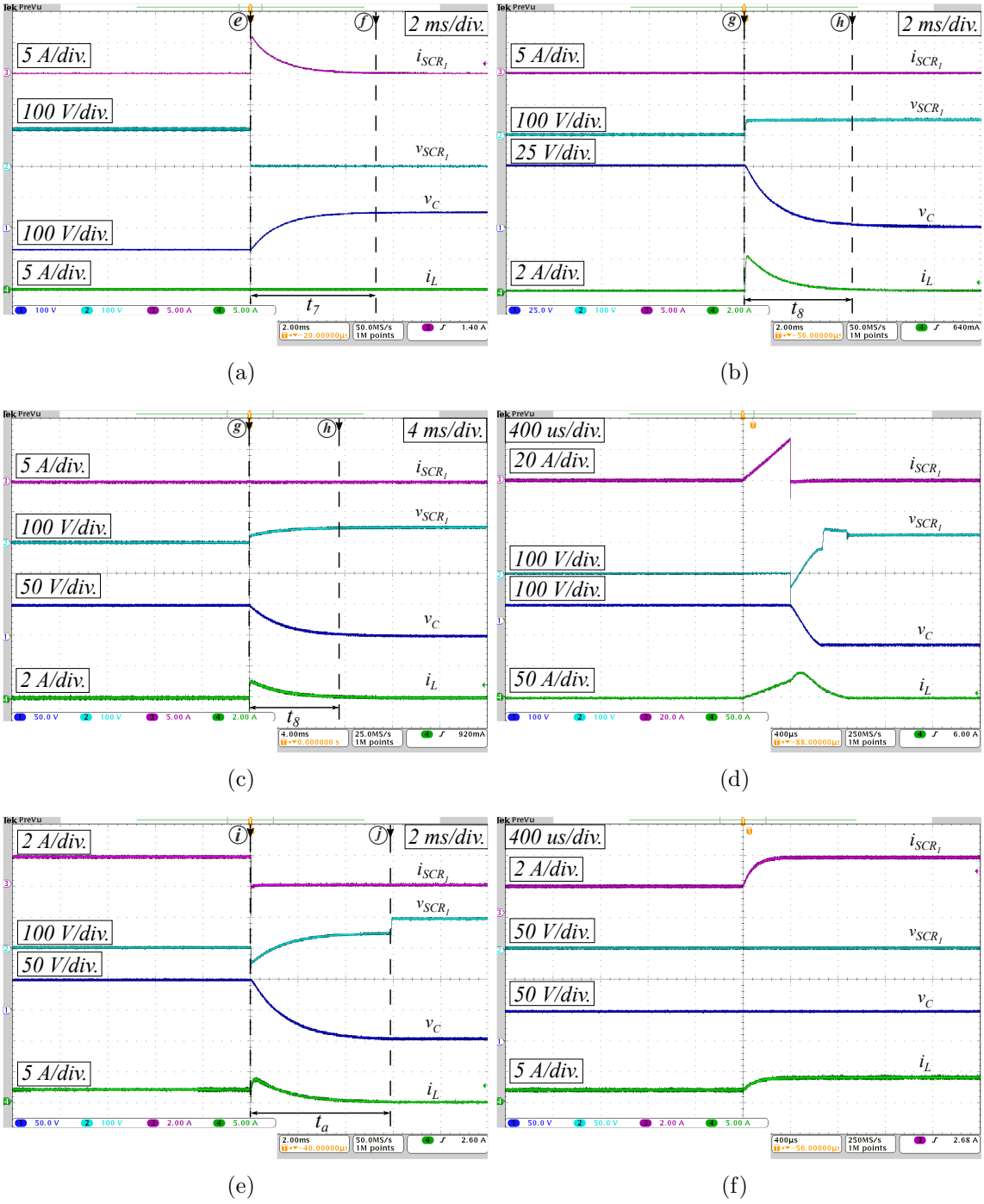
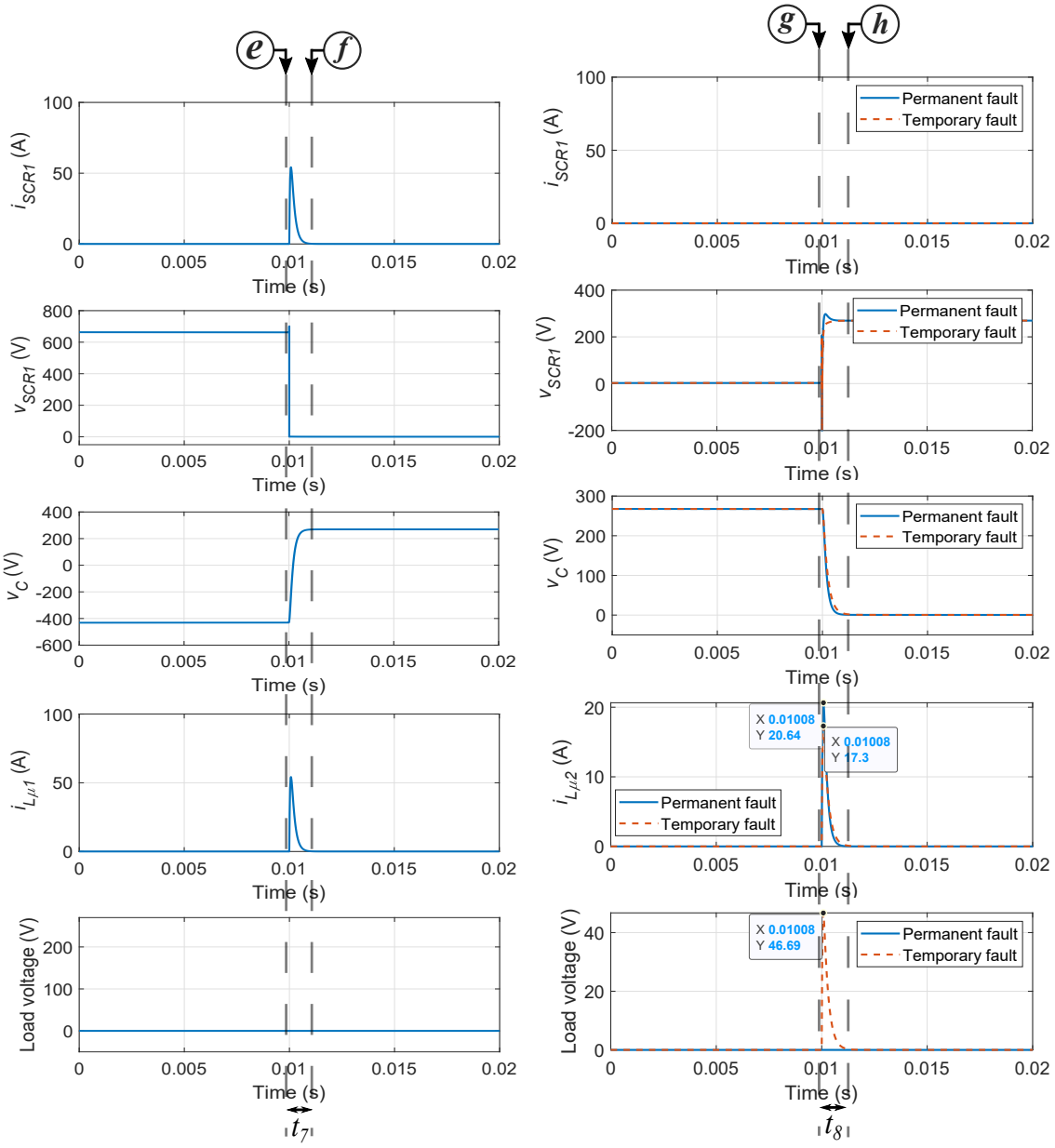


Figure 5.25: Experimental results for: (a) capacitor charge subinterval, (b) capacitor discharge subinterval in case of a permanent fault, (c) capacitor discharge subinterval in case of a temporary fault, (d) normal reclosing in case of a permanent fault, (e) load current breaking, and (f) step change in the load.



(a) (b)

Figure 5.26: Simulation results[1] for: (a) capacitor charge subinterval and (b) capacitor discharge subinterval.

[1]Current and voltage waveforms shown in Figs. 5.26(a) and (b) are advanced by a value of 2.19s and 2.39s, respectively from the origin defined in Fig. 5.23(a).

Table 5.5: Comparison of SCR-Based SSPC/ SSCB Topologies

Figure	–	–	2.12(a)	2.12(b)	Proposed topology
Reference	[83]	[84]	[6]	[7]	
Category	ZSB	ZSB	DCCB	DCCB	DCCB
Short-circuit fault isolation mechanism	Auto	Auto	Manual	Manual	Manual
Normal reclosing capability	Yes	Yes	No	Yes	Yes
Semiconductor devices in the load current path	2	2	1	1	2
Bounded range of step load change	Yes	Yes	No	No	No
Soft reclosing capability	No	No	No	No	Yes
SCR_s	4	4	4	6	6
Diodes	4	1	0	2	0
Capacitors	3	1	2	1	1
Inductors	4	1	0	1	0
Coupled inductors	0	1	0	0	0
Resistors	4	1	2	2	2
Mechanical switches	0	0	0	0	1
Surge arrestors	0	0	1	0	1

A comparison of the proposed topology with existing manual CBs and some ZSB topologies, is shown in Table 5.5. The SCR is a half-controlled semiconductor device due to which SCR-based SSPCs/ SSCBs have auxiliary circuitry to force the commutation of the main SCRs. The topology, proposed in [6], has the active bidirectional fault isolation capability. However, it is unable to provide reclosing functionality. The topology proposed in [7], has both manual fault isolation and normal reclosing capability. However, the current and voltage stress during reclosing is high. The proposed SCR-BCB topology has a manual SC fault isolation mechanism, which is essential for improving selectivity. In addition, it has soft reclosing functionality, which helps in reducing stress on semiconductor devices, capacitors, surge suppression devices, and current feeding components. Moreover, the energy dissipated by the surge suppression devices during reclosing is negligible. Additionally, multiple reclosing attempts are possible with no detrimental and adverse impact on the breaker as well as current feeding components.

5.3 Discussion and Summary

A novel coupled-inductor-based bidirectional ZSB topology has been proposed in Section 5.1. The proposed topology has lower on state power loss, this is because, only one semiconductor device is in the load current path. In addition, the proposed topology has simple structure, and is symmetric for all values of inductors. Performance of the proposed topology is verified using simulations, and the simulation results have been presented in this section.

There are two main limitations of ZSBs. The first limitation is that the selective protection coordination design, in case of these breakers, is complicated. This is because of its unique operating principle. The second limitation is that these have a maximum value of step-load change [9], beyond this value the breaker trips. To overcome these drawbacks, an SCR-based bidirectional dc SSPC/ SSCB has been proposed in Section 5.2. The proposed topology can isolate the faulty section with manual tripping command, and it has soft reclosing functionality by means of which the stress on the breaker and current feeding components is reduced. In addition, the TVS diode heat loss during reclosing is negligible. Expressions for the SCR reverse recovery time, peak value of fault current and fault clearing time have been derived and analyzed. The performance of the breaker has also been verified by simulation and hardware experiments.

Chapter 6

Conclusion and Recommendations

This chapter discusses the conclusion and summary of the work presented in this thesis. In addition, some areas are suggested, which can be considered for future research.

6.1 Conclusion and Summary

Global temperature has been rising, and as a result, extreme climatic behaviors have been observed. Many countries have introduced measures to tackle with global warming. In this regard, aviation industry is also putting efforts to cut down carbon emissions. One of the promising ways to reduce emissions is by means of electrification. In addition, more electric aircraft offers several other advantages such as fuel saving, less maintenance requirement, high efficiency, and extended control. Operational efficiency can further be improved by adopting dc grids. These grids have numerous advantageous properties such as, no skin and proximity effect, absence of reactive power, and easier integration of energy storage systems. Despite the above-mentioned advantages, fault isolation is one of the major challenges in these dc power networks, due to the absence of current zero-crossing. MeCBs are being extensively used in ac grids. However, these MeCBs have many limitations for dc applications, such as slow response time, limited dc current breaking capability, and additional auxiliary circuit requirement. SSPCs/ SSCBs are emerging as a promising alternative for dc system protection, as these offers several advantages. Some of these advantages are fast fault isolation, improved controllability, reduced fault current magnitude, and advanced load management capability. This motivates to conduct research on SSPC/ SSCB technology. One of the main tasks of SSPCs/

SSCBs is precharging, and this is an important task because uncontrolled charging of the capacitor can cause damage to the circuit components. The first and second contributions of the thesis are improved precharging methods. One of the limitations of SSPCs/ SSCBs is that these devices have high on-state power loss because semiconductor devices are in the load current path. In this regards, SCR-based SSPCs/ SSCBs have recently gained attention. The third and fourth contributions of the thesis are novel SCR-based SSPCs/ SSCBs.

A review of switchgear and protection devices, has been presented in Chapter 2. The operating principle of these devices has been explained. In addition, advantages and limitations are also presented. These devices have been compared, and based on the comparison, it has been concluded that SSPC/ SSCB is an attractive and promising technology. General SSPC/ SSCB configuration has been presented in this chapter. Semiconductor devices are one of the key components of SSPCs/ SSCBs, and accordingly, various power semiconductor devices that are most commonly used for SSPC/ SSCB applications, have been discussed. Subsequently, existing SSPC/ SSCB topologies have been reviewed. Operating principle, advantages, and drawbacks, of these topologies have been explained. Furthermore, existing precharging methods for SSPCs/ SSCBs, have been discussed. Improved precharging methods and novel SSPC/ SSCB topologies have been proposed in this thesis, and the key novelty has been discussed in Chapter 2.

A constant current precharging algorithm has been proposed in Chapter 3. The proposed algorithm controls the gate voltage of the semiconductor device to regulate the device current. The proposed algorithm requires no additional precharge circuitry. Moreover, it can easily adapt to changes in source voltage, and this feature has been verified experimentally. Furthermore, the expression of current reference is simple, and the values of the terms in this expression, are easily available in most of the power semiconductor device datasheets. Hardware experiments have been carried out to verify the proposed algorithm, and the experimental results have been illustrated and explained. The operating temperature has been assumed constant in this chapter. However, in aerospace applications, operating temperature in not constant. This point has been addressed in Chapter 4.

A constant temperature precharging algorithm has been proposed in Chapter 4. The proposed precharging algorithm regulates the junction temperature of the semiconductor device, during precharging interval, by controlling the gate-source voltage.

It has high adaptability to change of source parameters as well as operating temperature. Furthermore, thermal stress on the semiconductor device is regulated to a low value. The proposed algorithm has been verified using a laboratory setup.

On-state power loss of SSPCs/ SSCBs is high because the load current flows through branch containing semiconductor devices. The power loss is a critical parameter, and accordingly, this has motivated to investigate ways to reduce power loss. In this regard, SCR-based SSPCs/ SSCBs have recently gained attention in academic community, because SCRs have low voltage drop. Furthermore, SCRs have many properties, which are advantageous for this application. SCR-based SSPCs/ SSCBs have been considered in Chapter 5.

ZSBs are SCR-based SSPCs/ SSCBs, and these automatically isolates the short-circuit fault. A novel ZSB topology has been proposed in Section 5.1 of Chapter 5. The semiconductor device power loss in the proposed topology, is lower than in other existing topologies. Furthermore, it is electrically symmetric and has simple structure. The proposed topology has been verified using simulations, and the simulation results have been presented in this thesis. However, there are some limitations of ZSBs, and these have been discussed. In Section 5.2 of Chapter 5, a novel SCR based SSPC/ SSCB topology has been proposed, which overcomes these limitations. Additionally, it has soft reclosing capability. The proposed topology has been verified using simulation and hardware experiments, and these results have been presented in this thesis.

6.2 Recommendations for Future Research

In this section, research areas which are interesting to explore as future work are listed. Future works 1 and 2 are more closely related to the contributions of the thesis and are more relevant for future dc grids.

- The inductor value has been assumed constant in this thesis. However, the inductance varies within specified tolerance band. The variation in inductor value is dependent on many parameters such as core material, current through its winding, and air gap. The impact of these parameters on the inductor value, and subsequently, on the proposed solutions can be analyzed as future work.
- In Chapter 3, it has been assumed that the value of the capacitor is known and

this value is used in the proposed constant current precharging algorithm. This algorithm can be further extended to include the case in which the value of the capacitor is unknown. In this case, the controller can estimate the value of the capacitor, prior to executing the precharging portion of the code. This can be achieved by regulating the current through the capacitor for initial few milli seconds and measuring the voltage across it. Using the expression $C = i_C \frac{dt}{dv_c}$, capacitor value can be estimated. However, this additional code increases the computational burden on the controller.

- In this thesis, precharging methods have been proposed and experimentally verified for single SSPC/ SSCB. From a system-level perspective, capacitors are distributed and multiple SSPCs/ SSCBs are used. The positioning and interconnection of SSPCs/ SSCBs is dependent on the system architecture. Thus, precharging operation sequence varies depending on the system architecture. System-level coordination study and analysis of precharging methods proposed in this thesis, is an interesting domain and can be explored in the future.

- Electrical components deteriorate with the time of operation and thus, these have limited lifetime. Various external and internal factors influences the lifetime of a component. For the study of the solutions proposed in this thesis, the components of the SSPC/ SSCB are considered healthy. The effect of failure of the components of the SSPC/ SSCB on system operation, can be studied as future work. This study can be further extended to include design and analysis of system-level protection coordination. In a system, multiple layers of protection are designed and implemented, these layers constitute of fuses, ac side circuit breakers, breakers at the ends of the transmission lines/ cables, etc. In an event of fault, if the breaker accountable for isolating the fault, fails to operate, then secondary protection layer clears the fault. Design of secondary protection layer is dependent on various factors such as system topology, cable insulation, ac side grid stability, and semiconductor devices technology. This is an interesting area of research and can be examined in the future.

- ZSBs are emerging SSPC/ SSCB topologies and the short-circuit fault isolation mechanism of these ZSBs is automatic. Due to its unique working principle, these are well suited for some specific applications. Some of these applications have been studied in the literature. However, extensive system-level evaluation

of ZSBs is required for its widespread adoption. This is a possible direction for future research.

ZSBs have inductors and capacitors, due to which the transfer function is not a straight line. In other words, the magnitude and phase of output with respect to input is frequency dependent. This transfer function is dependent on the placement of inductors and capacitors, and thus, it is not same for all ZSB topologies. In some cases, the transfer characteristic of the ZSB is similar to a filter and in those cases, the filter size can be reduced because the ZSB fulfill some of the filtering requirements. However, these requirements are dependent on the system topology. Thus, extensive system-level frequency domain analysis of ZSB topologies is required and this can be investigated in the future.

- In this thesis, experimental results have been obtained from a scaled-down laboratory prototype. Engineering challenges associated with the design of the SSPC/ SSCB are expected when leveraging at high technology readiness level. These challenges can be investigated in the future. Some of these challenges are detailed as follows:
  Paralleling of semiconductor devices: Operating at high current levels necessitates paralleling of semiconductor devices, which introduces issues related to the current sharing among the semiconductor devices in transient and steady-state operation.
  Thermal management: Cooling multiple devices on the same heat sink/ cold plate/ cooling tube causes uneven temperature variation and hot spots, which affects the reliability of semiconductor devices. Innovative heat sink designs are required to mitigate temperature hot spots.

Appendix A

Mathematical Derivation

A mathematical derivation of (5.12) is presented in this appendix. Expression of $i_1(t)$ has been derived in Section 5.1.2.2.

$$i_1(t) = \alpha cos(\omega_d t)e^{-\delta t} + \beta sin(\omega_d t)e^{-\delta t} \tag{A.1}$$

where,

$$\alpha = \frac{2V_s}{R_L} \tag{A.2}$$

$$\beta = \frac{2V_s}{R_L \omega_d}\left(\frac{R_L}{2L_{11}} - \delta\right) \tag{A.3}$$

$$\omega_d = \sqrt{\frac{1}{L_{11}C} - \left(\frac{R_f \parallel R_L}{2L_{11}}\right)^2} \tag{A.4}$$

$$\delta = \frac{R_f \parallel R_L}{2L_{11}} \tag{A.5}$$

The expression of derivative of $i_1(t)$ with respect to time can be calculated as,

$$\frac{d(i_1(t))}{dt} = cos(\omega_d t)(-\alpha\delta + \beta\omega_d) - sin(\omega_d t)(\beta\delta + \alpha\omega_d) \tag{A.6}$$

$\frac{d(i_1(t))}{dt} = 0$ and $t = t_{max}$ is substituted in (A.6). The resultant expression can be represented as,

$$cos(\omega_d t_{max})(-\alpha\delta + \beta\omega_d) - sin(\omega_d t_{max})(\beta\delta + \alpha\omega_d) = 0 \tag{A.7}$$

The terms of (A.7) can be rearranged as follows,

$$tan(\omega_d t_{max}) = \frac{-\alpha\delta + \beta\omega_d}{\beta\delta + \alpha\omega_d} \tag{A.8}$$

Inverse tan is applied on both sides of (A.8), the resultant expression can be represented as,

$$\omega_d t_{max} = tan^{-1}\left(\frac{-\alpha\delta + \beta\omega_d}{\beta\delta + \alpha\omega_d}\right) \tag{A.9}$$

The values of α and β from (A.2) and (A.3) are substituted in (A.9). The t_{max} can be calculated as,

$$t_{max} = \frac{1}{\omega_d} tan^{-1}\left(\frac{R_L\omega_d - 4L_{11}\delta\omega_d}{2L_{11}\omega_d^2 + \delta R_L - 2L_{11}\delta^2}\right) \tag{A.10}$$

List of Publications

[1] **M. Marwaha**, K. Satpathi, M. H. M. Sathik, J. Pou, C. J. Gajanayake, A. K. Gupta, D. Molligoda, and R. K. Surapaneni, "SCR-Based Bidirectional Circuit Breaker for DC System Protection with Soft Reclosing Capability," *IEEE Trans. Ind. Electron. [Early Access].*

2 articles to be submitted to Journal.

Conferences:

[2] **M. Marwaha**, K. Satpathi, J. Pou, D. A. Molligoda, C. Gajanayake, and A. K. Gupta, "Coupled-Inductor-Based Bidirectional Z-Source Breaker for DC System Protection," in *Proc. 46th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, pp. 3433-3438, Oct. 2020.

[3] **M. Marwaha**, M.H.M. Sathik, K. Satpathi, Y. Yu, F. Sasongko, J. Pou, C. Gajanayake, and A. K. Gupta, "Comparative Analysis of Si, SiC and GaN Field-Effect Transistors for DC Solid-State Power Controllers in More Electric Aircraft," in *Proc. IEEE Energy Convers. Congr. Expo. - Asia (ECCE-Asia)*, pp. 592-597, May 2021.

References

[1] Cat net zero target evaluations. [Online]. Available: https://climateactiontracker.org/global/cat-net-zero-target-evaluations/

[2] Climate change and flying: what share of global co2 emissions come from aviation? [Online]. Available: https://ourworldindata.org/co2-emissions-from-aviation

[3] J. Chen, C. Wang, and J. Chen, "Investigation on the selection of electric power system architecture for future more electric aircraft," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 2, pp. 563–576, Jun. 2018.

[4] V. Madonna, P. Giangrande, and M. Galea, "Electrical power generation in aircraft: Review, challenges, and opportunities," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 3, pp. 646–659, Sep. 2018.

[5] A. Valko, J. Petrella, D. Murray, D. Frederick, and K. Alves, "Solid-State Secondary Power Distribution," *U.S. Department of Transportation*, Mar. 2014.

[6] J. Shu, J. Ma, S. Wang, Y. Dong, T. Liu, and Z. He, "A new active thyristor-based DCCB with reliable opening process," *IEEE Trans. Power Electron.*, vol. 36, no. 4, pp. 3617–3621, Apr. 2021.

[7] Z. Ayubu, J.-Y. Kim, J.-Y. Yu, S.-M. Song, and I.-D. Kim, "Novel bidirectional dc solid-state circuit breaker with operating duty capability," *IEEE Trans. Ind. Electron.*, vol. 68, no. 10, pp. 9104–9113, Oct. 2021.

[8] D. Izquierdo, A. Barrado, C. Fernández, M. Sanz, and A. Lázaro, "SSPC active control strategy by optimal trajectory of the current for onboard system applications," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, pp. 5195–5205, Nov. 2013.

[9] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC microgrid protection: A comprehensive review," *IEEE Trans. Emerg. Sel. Topics Power Electron. [Early Access]*.

[10] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[11] J. Hafner and B. Jacobson, "Proactive hybrid HVDC breakers-a key innovation for reliable HVDC grids," in *Proc. CIGRE Bologna Symposium*, pp. 1-8, Sep. 2011.

[12] D. Izquierdo, A. Barrado, C. Raga, M. Sanz, and A. Lazaro, "Protection devices for aircraft electrical power distribution systems: State of the art," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 47, no. 3, pp. 1538–1550, Jul. 2011.

[13] D. A. Molligoda, P. Chatterjee, C. J. Gajanayake, A. K. Gupta, and K. Tseng, "Review of design and challenges of DC SSPC in more electric aircraft," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf.*, pp. 1-5, Dec. 2016.

[14] T. Feehally and A. J. Forsyth, "A MOSFET based solid-state power controller for aero dc networks," in *Proc. 7th IET Int. Conf. Power Electron. Mach. Drives*, pp. 1-7, Apr. 2014.

[15] Z. Liu, R. Fuller, and W. Pearson, "Solid state power control system for aircraft high voltage dc power distribution," Nov. 24 2015, US Patent 9,197,056.

[16] S. Bal, P. Chatterjee, C. J. Gajanayake, A. I. Maswood, and A. K. Gupta, "Design considerations of bidirectional SiC based DC solid-state power controller for MEA systems," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, pp. 5745–5752, Oct. 2018.

[17] F. Mohammadi, K. Rouzbehi, M. Hajian, K. Niayesh, G. B. Gharehpetian, H. Saad, M. Hasan Ali, and V. K. Sood, "HVdc circuit breakers: A comprehensive review," *IEEE Trans. Power Electron.*, vol. 36, no. 12, pp. 13 726–13 739, Dec. 2021.

[18] Z. Liu, S. Mirhosseini, L. Liu, M. Popov, K. Ma, W. Hu, S. Jamali, P. Palensky, and Z. Chen, "A contribution to the development of high-voltage dc circuit breaker technologies: A review of new considerations," *IEEE Ind. Electron. Mag.*, vol. 16, no. 1, pp. 42–59, Mar. 2022.

[19] Jet zero strategy. [Online]. Available: https://assets.publishing.service.gov.uk/government/uploads/system/uploads/attachment_data/file/1095952/jet-zero-strategy.pdf

[20] Net-zero carbon emissions by 2050. [Online]. Available: https://www.iata.org/en/pressroom/pressroom-archive/2021-releases/2021-10-04-03/

[21] W. Cao, B. C. Mecrow, G. J. Atkinson, J. W. Bennett, and D. J. Atkinson, "Overview of electric motor technologies used for more electric aircraft (mea)," *IEEE Trans. Ind. Electron.*, vol. 59, no. 9, pp. 3523–3531, Sep. 2012.

[22] F. Guo, T. Yang, C. Li, S. Bozhko, and P. Wheeler, "Active modulation strategy for capacitor voltage balancing of three-level neutral-point-clamped converters in high-speed drives," *IEEE Trans. Ind. Electron.*, vol. 69, no. 3, pp. 2276–2287, Mar. 2022.

[23] C. Wang, T. Yang, H. Hussaini, and S. Bozhko, "Using dc–dc converters as active harmonic suppression device for more electric aircraft applications," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6508–6518, Jul. 2022.

[24] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-board microgrids for the more electric aircraft—technology review," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5588–5599, Jul. 2019.

[25] P. Wheeler and S. Bozhko, "The more electric aircraft: Technology and challenges." *IEEE Electrific. Mag.*, vol. 2, no. 4, pp. 6–12, Dec. 2014.

[26] C. Wang, T. Yang, H. Hussaini, Z. Huang, and S. Bozhko, "Power quality improvement using an active power sharing scheme in more electric aircraft," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3588–3598, Apr. 2022.

[27] K. Satpathi, Y. M. Yeap, A. Ukil, and N. Geddada, "Short-time Fourier transform based transient analysis of VSC interfaced point-to-point dc system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 5, pp. 4080–4091, May 2018.

[28] C. Jin, P. Wang, J. Xiao, Y. Tang, and F. H. Choo, "Implementation of hierarchical control in dc microgrids," *IEEE Trans. Ind. Electron.*, vol. 61, no. 8, pp. 4032–4042, Aug. 2014.

[29] M. Hamzeh, A. Ghazanfari, Y. A.-R. I. Mohamed, and Y. Karimi, "Modeling and design of an oscillatory current-sharing control strategy in dc microgrids," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 6647–6657, Nov. 2015.

[30] N. Geddada, Y. M. Yeap, and A. Ukil, "Experimental validation of fault identification in VSC-based dc grid system," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4799–4809, Jun. 2018.

[31] F. Sasongko, P. Yaxin, J. Pou, and R. Simanjorang, "One-kilohertz fundamental frequency operation of a SiC power converter for future aircraft system," in *Proc. Conf. Power Eng. Renew. Energy*, pp. 1-6, Oct. 2018.

[32] M. Tariq, A. I. Maswood, C. J. Gajanayake, and A. K. Gupta, "Modeling and integration of a lithium-ion battery energy storage system with the more electric aircraft 270 V DC power distribution architecture," *IEEE Access*, vol. 6, pp. 41 785–41 802, 2018.

[33] B. Rahrovi and M. Ehsani, "A review of the more electric aircraft power electronics," in *Proc. IEEE Texas Power Energy Conf.*, pp. 1-6, Feb. 2019.

[34] A. Ukil, Y. M. Yeap, and K. Satpathi, *Fault Analysis and Protection System Design for DC Grids*. Springer Singapore, 2020.

[35] M. Tariq, A. I. Maswood, C. J. Gajanayake, and A. K. Gupta, "Aircraft batteries: Current trend towards more electric aircraft," *IET Elect. Syst. Transportation*, vol. 7, no. 2, pp. 93–103, Jun. 2017.

[36] K. Satpathi, A. Ukil, and J. Pou, "Short-circuit fault management in DC electric ship propulsion system: Protection requirements, review of existing technologies and future research trends," *IEEE Trans. Transport. Electrific.*, vol. 4, no. 1, pp. 272–291, Mar. 2017.

[37] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids—Part ii: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron.*, vol. 31, no. 5, pp. 3528–3549, May 2016.

[38] J. Huang, X. Zhang, Z. Shuai, X. Zhang, P. Wang, L. H. Koh, J. Xiao, and X. Tong, "Robust circuit parameters design for the CLLC-type dc transformer in the hybrid ac–dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1906–1918, Mar. 2019.

[39] P. Yang, Y. Xia, M. Yu, W. Wei, and Y. Peng, "A decentralized coordination control method for parallel bidirectional power converters in a hybrid ac–dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 65, no. 8, pp. 6217–6228, Aug. 2018.

[40] A. Heidary, H. Radmanesh, K. Rouzbehi, and J. Pou, "A dc-reactor-based solid-state fault current limiter for HVdc applications," *IEEE Trans. Power Del.*, vol. 34, no. 2, pp. 720–728, Apr. 2019.

[41] S. Zhang, G. Zou, X. Wei, and C. Zhang, "Bridge-type multiport fault current limiter for applications in MTdc grids," *IEEE Trans. Ind. Electron.*, vol. 69, no. 7, pp. 6960–6972, Jul. 2022.

[42] R. M. Cuzner and G. Venkataramanan, "The status of dc micro-grid protection," in *Proc. IEEE Ind. Appl. Soc. Annu. Meeting*, pp. 1-8, Oct. 2008.

[43] D. B. Durocher and T. Domitrovich, "Reconditioned low-voltage circuit breakers: Considering electrical safety for applications in industry," *IEEE Ind. Appl. Mag.*, vol. 28, no. 3, pp. 68–81, May 2022.

[44] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage dc microgrid," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3007–3021, Apr. 2017.

[45] D. Izquierdo, A. Barrado, C. Raga, M. Sanz, and A. Lazaro, "Protection devices for aircraft electrical power distribution systems: State of the art," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 47, no. 3, pp. 1538–1550, Jul. 2011.

[46] J. Shu, S. Wang, J. Ma, T. Liu, and Z. He, "An active z-source dc circuit breaker combined with SCR and IGBT," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10 003–10 007, Oct. 2020.

[47] K. A. Corzine and R. W. Ashton, "A new z-source dc circuit breaker," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 2796–2804, Jun. 2012.

[48] S. Savaliya and B. G. Fernandes, "Performance evaluation of a modified bi-directional z-source breaker," *IEEE Trans. Ind. Electron.*, vol. 68, no. 8, pp. 7137–7145, Aug. 2021.

[49] Y. Wang, W. Li, X. Wu, and X. Wu, "A novel bidirectional solid-state circuit breaker for dc microgrid," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 5707–5714, Jul. 2019.

[50] K. A. Corzine, "A new-coupled-inductor circuit breaker for dc applications," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1411–1418, Feb. 2017.

[51] A. H. Chang, B. R. Sennett, A. Avestruz, S. B. Leeb, and J. L. Kirtley, "Analysis and design of dc system protection using z-source circuit breaker," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1036–1049, Feb. 2016.

[52] A. Maqsood, A. Overstreet, and K. A. Corzine, "Modified z-source dc circuit breaker topologies," *IEEE Trans. Power Electron.*, vol. 31, no. 10, pp. 7394–7403, Oct. 2016.

[53] S. G. Savaliya and B. G. Fernandes, "Analysis and experimental validation of bidirectional z-source dc circuit breakers," *IEEE Trans. Ind. Electron.*, vol. 67, no. 6, pp. 4613–4622, Jun. 2020.

[54] Z. Zhou, J. Jiang, S. Ye, C. Liu, and D. Zhang, "A γ-source circuit breaker for dc microgrid protection," *IEEE Trans. Ind. Electron.*, vol. 68, no. 3, pp. 2310–2320, Mar. 2021.

[55] V. Raghavendra, S. N. Banavath, and S. Thamballa, "Modified z-source dc circuit breaker with enhanced performance during commissioning and reclosing," *IEEE Trans. Power Electron.*, vol. 37, no. 1, pp. 910–919, Jan. 2022.

[56] A. Nawawi, C. F. Tong, Y. Liu, A. Sakanova, S. Yin, Y. Liu, K. Men, K. Y. See, K. J. Tseng, R. Simanjorang, C. J. Gajanayake, and A. K. Gupta, "Design of high power density converter for aircraft applications," in *Proc. 2015 Int. Conf. Electr. Syst. Aircr. Railway Ship Propulsion Road Vehicles*, pp. 1-6, Mar. 2015.

[57] Z. Liu, R. Fuller, and W. Pearson, "SSPC technologies for aircraft high voltage dc power distribution applications," SAE Technical Paper, Tech. Rep., 2012.

[58] K. A. Corzine and R. W. Ashton, "A new Z-source dc circuit breaker," in *Proc. IEEE Int. Symp. on Ind. Elect.*, pp. 585-590, Jul. 2010.

[59] K. A. Corzine and R. W. Ashton, "Structure and analysis of the Z-source MVDC breaker," in *Proc. IEEE Electr. Ship Technol. Symp.*, pp. 334-338, Apr. 2011.

[60] P. Prempraneerach, M. G. Angle, J. L. Kirtley, G. E. Karniadakis, and C. Chryssostomidis, "Optimization of a Z-source DC circuit breaker," in *Proc. IEEE Electr. Ship Technol. Symp.*, pp. 480-486, Apr. 2013.

[61] A. H. Chang, A. Avestruz, S. B. Leeb, and J. L. Kirtley, "Design of DC system protection," in *Proc. IEEE Electr. Ship Technol. Symp.*, pp. 500-508, Apr. 2013.

[62] K. Corzine, "DC micro grid protection with the z-source breaker," in *Proc. 39th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, pp. 2197-2204, Nov. 2013.

[63] A. Maqsood and K. Corzine, "Z-source dc circuit breakers with coupled inductors," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, pp. 1905-1909, Sep. 2015.

[64] A. Maqsood and K. A. Corzine, "Integration of Z-source breakers into zonal DC ship power system microgrids," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 5, no. 1, pp. 269–277, Mar. 2017.

[65] K. Corzine, A. Overstreet, and P. E. T. Baragona, "Solid-state breaker protection in MVDC systems," in *Proc. IEEE Electr. Ship Technol. Symp.*, pp. 414-418, Aug. 2017.

[66] A. Maqsood and K. Corzine, "The Z-source breaker for fault protection in ship power systems," in *Proc. Int. Symp. Power Electron. Electr. Drives Autom. Motion*, pp. 307-312, Jun. 2014.

[67] A. Maqsood and K. A. Corzine, "The Z-source breaker for ship power system protection," in *Proc. IEEE Electr. Ship Technol. Symp.*, pp. 293-298, Jun. 2015.

[68] D. Keshavarzi, T. Ghanbari, and E. Farjah, "A Z-source-based bidirectional DC circuit breaker with fault current limitation and interruption capabilities," *IEEE Trans. Power Electron.*, vol. 32, no. 9, pp. 6813–6822, Sep. 2017.

[69] D. J. Ryan, H. D. Torresan, and B. Bahrani, "A bidirectional series Z-source circuit breaker," *IEEE Trans. Power Electron.*, vol. 33, no. 9, pp. 7609–7621, Sep. 2018.

[70] B. Munari and A. Schneer, "How to design a precharge circuit for hybrid and electric vehicle applications," Technical White Paper, Sensata Technologies, 2020.

[71] A. Forbes, *How to select a Surge Diode.* Texas Instruments Incorporated.

[72] *AD5628*, Low power, small footprint, pin-compatible octal DAC, Analog Devices.

[73] A. Sedra, K. Smith, T. C. Carusone, and V. Gaudet, "Microelectronic circuits 8th edition."

[74] "Power MOSFET Thermal Design and Attachment of a Thermal Fin," Application Note, TOSHIBA, Jul. 2018.

[75] M. März and P. Nance, "Thermal modeling of power electronic systems," *Infineon Technologies AG Munich*, 2000.

[76] *N-channel power MOSFET*, STW65N65DM2AG, STMicroelectronics.

[77] H. Niu and R. D. Lorenz, "Evaluating different implementations of online junction temperature sensing for switching power semiconductors," *IEEE Trans. Ind. Appl.*, vol. 53, no. 1, pp. 391–401, Jan. 2017.

[78] M. Andresen, M. Schloh, G. Buticchi, and M. Liserre, "Computational light junction temperature estimator for active thermal control," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, pp. 1-7, Sep. 2016.

[79] V. Blasko, R. Lukaszewski, and R. Sladky, "On line thermal model and thermal management strategy of a three phase voltage source inverter," in *Proc. Conf. Rec. IEEE Ind. Appl. Conf. 34th IAS Annu. Meeting*, vol. 2, pp. 1423-1431, Oct. 1999.

[80] D. Edwards and H. Nguyen, "Semiconductor and IC Package Thermal Metrics," Application Report, Texas Instruments, Apr. 2016.

[81] T. Kostakis, P. J. Norman, S. J. Galloway, and G. M. Burt, "Demonstration of fast-acting protection as a key enabler for more-electric aircraft interconnected architectures," *IET Electr. Syst. Transp.*, vol. 7, no. 2, pp. 170–178, May 2017.

[82] P. Chatterjee, C. J. Gajanayake, E. D. Schneider, D. A. Molligoda, and A. K. Gupta, "Pre-charging circuit for power converters," Jun. 23 2020, US Patent 10,693,367.

[83] S. Savaliya and B. G. Fernandes, "Comparative analysis and coordination study of Bi-directional Z-source breaker with reclosing capabilities," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, pp. 1-10, Sep. 2017.

[84] S. G. Savaliya and B. G. Fernandes, "Modified bi-directional z-source breaker with reclosing and rebreaking capabilities," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, pp. 3497-3504, Mar. 2018.

[85] S. Zhang, G. Zou, C. Xu, and W. Sun, "A reclosing scheme of hybrid dc circuit breaker for MMC-HVDC systems," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 6, pp. 7126–7137, Dec. 2021.

[86] S. Zhang, G. Zou, X. Wei, and C. Zhang, "Multiport hybrid dc circuit breaker with reduced fault isolation time and soft reclosing capability," *IEEE Trans. Ind. Electron.*, vol. 69, no. 4, pp. 3776–3786, Apr. 2022.

[87] X. Fan and B. Zhang, "Dc line soft reclosing sequence for HVdc grid based on hybrid dc breaker," *J. Eng.*, vol. 2019, no. 16, pp. 1095–1099, Mar. 2019.

[88] D. Grafham and J. Hey, *SCR manual*. Semiconductor Products Department, General Electric, 1972.

[89] C. Yuan, M. A. Haj-ahmed, and M. S. Illindala, "Protection strategies for medium-voltage direct-current microgrid at a remote area mine site," *IEEE Trans. Ind. Appl.*, vol. 51, no. 4, pp. 2846–2853, Jul. 2015.

[90] L. Qi, A. Antoniazzi, and L. Raciti, "Dc distribution fault analysis, protection solutions, and example implementations," *IEEE Trans. Ind. Appl.*, vol. 54, no. 4, pp. 3179–3186, Jul. 2018.

[91] S. D. A. Fletcher, P. J. Norman, K. Fong, S. J. Galloway, and G. M. Burt, "High-speed differential protection for smart dc distribution systems," *IEEE Trans. Smart Grid*, vol. 5, no. 5, pp. 2610–2617, Sep. 2014.

[92] A. Raza, A. Mustafa, U. Alqasemi, K. Rouzbehi, R. Muzzammel, S. Guobing, and G. Abbas, "HVdc circuit breakers: Prospects and challenges," *Appl. Sci.*, vol. 11, no. 11, p. 5047, May 2021.

[93] *Silicon Controlled Rectifiers*, S7412M, New Jersey Semi-Conductor Products, Inc.

END