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HOT CARRIER RELIABILITY PERSPECTIVE ON SILICON-ON-INSULATOR LATERAL DOUBLE-DIFFUSED MOSFET (LDMOS)

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Table of Acronyms

A-BCD:	Advanced Bipolar/CMOS/DMOS
BOX:	Buried silicon Oxide (Buried Oxide)
CHE:	Channel Hot Electron
DAHC:	Drain Avalanche Hot Carrier
DMOS:	Double-diffused MOSFET
FOX:	Field Oxide
HCD:	Hot Carrier Degradation
HCI:	Hot Carrier Induced
HNWD:	High NWD implant dose Device
II:	Impact Ionization
LNWD:	Low NWD implant dose Device
LDMOSFET:	Lateral Double-diffused MOSFET
LOCOS:	Local Oxidation of Silicon
MOSFET:	Metal-Oxide-Semiconductor Field-Effect Transistor
NBO:	n-type Body Region
NWD:	Extended n-type Drift Region
ONWD:	Original (medium) NWD implant dose Device
PBO:	p-type implant Body Region
RESURF:	Reduced Surface Field
SGHE:	Secondary Generated Hot Electron

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SHE: Substrate Hot Electron

SOI: Silicon-on-Insulator

STI: Shallow Trench Isolation

TCAD: Technology Computer-Aided Design

ULSI: Ultra Large Scale Integration

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Summary

Silicon-on-insulator (SOI) device has a buried silicon oxide (Buried Oxide, or BOX) layer extending across the entire wafer. Recently, there is an increased interest in SOI wafers for application to the fabrication of advanced CMOS ICs. SOI technologies offer a large number of advantages in terms of capacitances, less cross-talk and high integration density [1]. One of the most common power MOSFETs used in smart power applications is SOI lateral double-diffused metal-oxide-semiconductor field-effect transistor (LDMOSFET) because of its high speed, low on-state resistance, as well as the fabrication processes are compatible with the standard low voltage CMOS process [2]. The performance of the SOI LDMOSFET is increased dramatically compared to the bulk technologies. However, SOI LDMOSFET is prone to hot carrier induced (HCI) degradation because the high operational voltages applied to the drain and/or gate will degrade the device electrical performance after prolonged operation. Many researches showed that the hot carrier reliability of a device is strongly dependent on its geometrical configuration, operational conditions, as well as the process parameters [3-5].

In this work, the electrical performances of a power SOI LDNMOSFET with hallow trench isolation (STI) structure under different bias conditions and with various doping concentration in the drift region are investigated. The HCI degradation test under various stress conditions of the SOI LDNMOSFET is also

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performed. Two-dimensional (2-D) technology computer-aided design (TCAD) numerical device simulations are employed to achieve better physical insights and understanding on its electrical behaviors with respect to the hot carrier problem.

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Chapter 1. Introduction

1.1 Motivation

Silicon-on-Insulator (SOI) device has many advantages over its bulk counterpart, and becomes one of the main-streams in Ultra Large Scale Integration (ULSI) technology. SOI wafers provide a way to increase the speed performance of CMOS circuits, as well as reduce the power (and voltage) requirements to achieve high performance [6]. High voltage (HV) LDMOS transistors have been used as the basic devices in power discrete and integrate circuits in the power amplifier or power switching due to their high current and high voltage capability [7]. However, since SOI LDNMOS devices are operated in the high current and high voltage environment, their hot carrier reliability problem has been recognized as one of the major constraints for the SOI device performances. It will trigger various physical processes that can drastically change the device characteristics during normal operation over prolonged periods, and eventually cause the circuit to fail. Therefore, hot carrier induced (HCI) degradation has been the subject of numerous studies over the past several decades; many fabrication strategies have been devised to reduce it without compromising the circuit performance [3, 5]. The study of various fundamental physical processes under different application conditions that result in device performance variation due to hot carrier problem is

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essential to provide guidelines for avoiding such failures in future integrated circuits (ICs).

1.2 Objectives

The objective of this project is to study the latest HV component SOI LDNMOS device of a SOI-based advanced bipolar CMOS DMOS (A-BCD) technology, and obtain a clearer and comprehensive understanding on its hot carrier reliability. Measurements and simulations are done to predict the influences of the doping level in the extended n-type drift region on the device's electrical performance under various bias conditions. Hot carriers generation is investigated by looking at the substrate current (I_{SUB}) in the active layer, as well as the distributions of electric field, potential, electron current density (J_E) and impact ionization (II) generation rate all over the entire device. Finally, HCI degradation test was performed to investigate the hot carrier damage of the devices with different doping levels in the drift region under different stress conditions. All these studies provided useful insights into the physical mechanisms involved in the device's HCI degradation and aided the development of the fabrication and design techniques to mitigate the associated reliability problems.

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1.3 Major Contribution of the Thesis

The HCI degradation of power device has been studied over the past several decades. All solutions proposed to alleviate the hot carrier reliability problem are based on a good understand of the fields distribution in the device, the mechanisms by which the carriers are injected into the insulator, the location of the injected carriers, the reaction-diffusion model for the silicon/silicon-oxide interface charges and the shift of the electrical characteristics resulting from such hot carrier injection. In spite of the vast amount of research performed to understand the HCI degradation phenomenon, few researches were done on the power SOI LDNMOS with shallow trench isolation (STI). The HCI degradation mechanisms could be different due to small changes of the device's process and structure. In this work, the hot carrier generation was studied by both experimental measurement and simulation analysis for this power SOI LDNMOS with STI structure. The cause of the hot carrier generation, the impacts of the bias condition and doping level in the drift region on its electrical characteristics due to the hot carrier problem were investigated. From the HCI degradation test, the different HCI degradation mechanisms were concluded from its abnormal HCI degradation behaviours. The effects of the stress conditions and the doping level in the extended drift region on the device's HCI degradation behaviours were also examined. Technology computer-aided design (TCAD) simulation tool is employed to provide the explanations in this work.

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1.4 Organization of the Thesis

In Chapter 2 the literature review part, the basic background knowledge of the hot carrier reliability and the SOI LDNMOS device are introduced. In chapter 3, the details of the device structure and doping profile, as well as the methodologies of the experimentation and simulation is presented.

Chapter 4 investigates the details of the II behavior of the device. Measurements of the drain and substrate currents are done to verify the simulations. These studies contribute to the understanding of the hot carrier generation peak location and the possible hot carrier injection sites. The effects of different doping levels in the drift region are shown in Chapter 5.

Chapter 6 extends the study to the HCI degradation test. The test is done on the SOI LDNMOS devices with different doping levels in the drift region under different stress conditions. Selected parameters are monitored during the stress test. From the analysis and comparisons of the degradation parameters, some abnormal HCI degradation behaviors are observed. This leads to interesting conclusions concerning the presence of two different hot carrier injection sites in the device.

Finally, Chapter 7 summarizes and concludes the work.

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Chapter 2. Literature Review

2.1 Silicon-On-Insulator (SOI) Technology

SOI refers to the use of a layered silicon-insulator-silicon substrate in place of conventional silicon substrates as shown in Fig 1. A SiO_2 layer lies on the substrate to provide a vertical isolation from active layer. The insulator, usually is an insulated buried oxide (BOX) layer, provides excellent intrinsic vertical isolation of active layer from the substrate, which effectively reduces device leakage and latch-up. Owing to the presence of the buried insulator, the field isolation schemes are simpler for SOI technology than normal bulk silicon technology. Standard Local Oxidation of Silicon (LOCOS) or Shallow Trench Isolation (STI) processes are employed to provide the lateral isolation from adjacent devices [6].

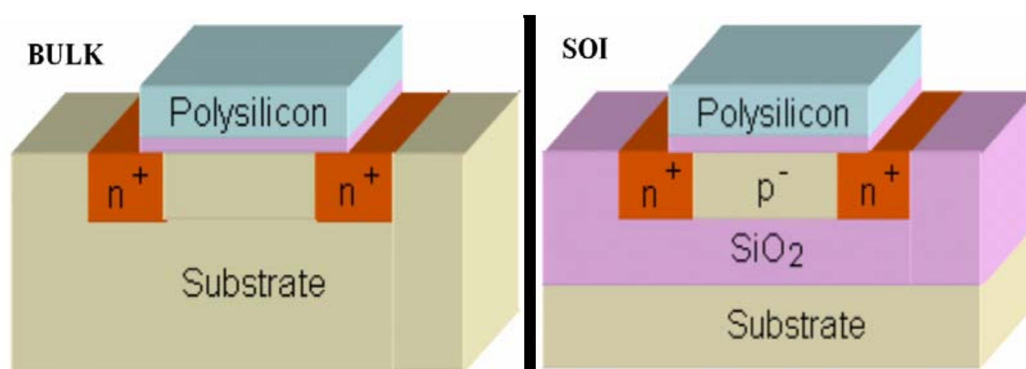

Figure 1. Bulk Silicon vs. SOI Silicon

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At present, SOI technology exhibits many advantages over bulk silicon technology, which makes it as a leading candidate to replace the bulk silicon for ULSI applications. Firstly, it has excellent transistor isolation, which makes it have lower leakage and elimination of vertical latch-up. The source and drain regions extend to the insulator and only their lateral sides serve as junctions. This yields a substantial reduction in leakage current and parasitic capacitances, and provides resistance to latch-up due to the complete vertical isolation of the n- and p-structures (dielectric isolation) [8]. Secondly, it has faster device operation due to its lower parasitic capacitance. This is because the BOX acts as a boundary layer, thus limiting capacitance transfer to the substrate material. A reduction in capacitance also allows less operation voltage, thus increases power consumption efficiency. Thirdly, SOI CMOS technology offers a tighter layout design rules (higher integration density) compared with bulk CMOS. This higher density results mainly from the absence of wells in SOI, and the possibility of direct contact between P+ and N+ junctions in NMOS and PMOS transistors [6]. All these will reduce the STI layout area required for the lateral junction isolation and make more functions per die area, thus higher packing density.

The flexibility of SOI structures (variable film, oxide thicknesses, buried oxide, interrupted oxides, electric shield engineering, etc) makes it more suitable than isolated bulk-Si technology for fabrication of high and medium power/voltage devices. Therefore, SOI wafers are now viewed as the most important emerging wafer engineering technology for use in leading edge CMOS IC production.

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2.2 Self Heating Effect

SOI transistor is thermally insulated from substrate by the BOX layer. As a result, removal of excess heat generated by Joule effect within the device is less efficient than in bulk silicon, which yields to substantial elevation of device temperate. This is called self heating effect. One important feature of this effect is it takes place as power is dissipated into the device. The time constants involved in the self heating of SOI transistor are on the order of several tens of nanoseconds [6]. Self-heating effect can influence the device performance significantly since the device's characteristics are a function of the temperature. The current reduction at high bias condition can be seen in the output characteristics of SOI MOSFET is due to a mobility reduction caused by the self heating effect. At room temperature, the mobility can be determined by:

$$\mu_n(T) = 1360 \cdot \left(\frac{T}{300}\right)^{-2.42}, \quad \mu_p(T) = 495 \cdot \left(\frac{T}{300}\right)^{-2.20} \tag{1}$$

where μ_n and μ_p are the electron and hole mobility, respectively, in cm^2 per volt second; and T is the absolute temperature in degrees Kelvin. As seen from this equation, the decrease of mobility with temperature for electron is more significant than that of hole. A general expression can be used to predict the variation of the on-resistance of a power MOSFET based on the temperature dependence of the mobility is [9]:

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$$R_{ON}(T) = R_{ON}(25^{\circ}C) \cdot \left(\frac{T}{300}\right)^{2.3} \tag{2}$$

In the absence of a work function difference and oxide charge, the threshold voltage is given by:

$$V_T = \frac{\sqrt{4\varepsilon_S \cdot q \cdot N_A \cdot \Psi_B}}{C_{OX}} + 2 \cdot \Psi_B \tag{3}$$

where ψ_B is the potential difference between the intrinsic and Fermi levles, N_A is the net doping concentration in the channel region, C_{OX} is the gate oxide capacitance and ε_S is the dielectric constant of silicon.

Differentiating this equation with respect to temperature, we can get the temperature dependence of the threshold voltage:

$$\frac{dV_T}{dT} = \frac{d\Psi_B}{dT}\left(\frac{\sqrt{\varepsilon_S \cdot q \cdot N_A / \Psi_B}}{C_{OX}} + 2\right) \tag{4}$$

This expression is valid even in the presence of a work function difference and oxide charge because these parameters are not strongly affected by temperature. ψ_B varies with temperature because the enrgy gap changes with temperature [9].

2.3 Lateral Double-Diffused MOSFET (LDMOS)

The full dielectric isolation provided by SOI substrate allows fabricating HV devices without the use of a complicated junction isolation process. Power devices can be integrated on the same substrate as CMOS logic to produce “smart power” circuits [6]. Double-diffused MOSFET (DMOS) is one of these power devices. It is formed by using a double ion implantation with two separate implantation masks.

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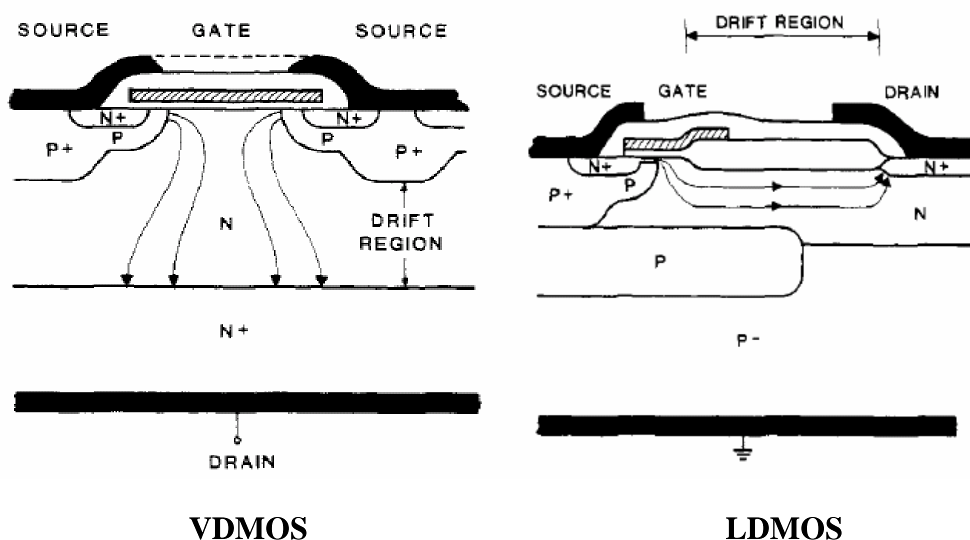
The DMOS structure uses a diffused junction rather than photolithography to form the MOS channel. Two types of DMOS transistors are presently in use as shown in Fig 2: vertical DMOS (VDMOS) transistors utilizing both sides of the chip; and lateral DMOS (LDMOS) transistors which have electrodes located only on the top of the chip [10]. Typically, LDMOS transistors are chosen for integrated smart-power applications as they are more compatible with standard CMOS processing and can be easily integrated by the addition of some extra process layers. VDMOS transistors, however, are less cost-effective to integrate because the current has to be collected at the surface of the silicon and not at the backside, as is the case in discrete devices [2]. The DMOS transistor has some major advantages such as low on-resistance (R_{ON}), high transconductance, small parasitic capacitance, high current and power gain, high voltage operation, as well as fast switching speed without the necessity of extraordinary processing and mask [11].



VDMOS **LDMOS**

Figure 2. Cross Section of VDMOS & LDMOS

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In general, a LDMOS transistor distinguished from a typical MOS transistor is that LDMOS transistor additionally has a drift region extending in a lateral direction between an edge of a control gate and a drain region of the transistor. Reduced surface field (RESURF) technique is usually adopted to design LDMOS transistors to reduce the electric field in this relatively long drift region, thereby avoiding an electric field peak at PN junctions [6]. The higher doping concentration in the drift region, the lower conduction resistance it has. These characteristics can be utilized to have a MOS transistor with high breakdown voltage (BV) and low specific on-resistance (R_{ON}) [12]. The typical SOI LDMOS is shown in Fig 3. Above BOX layer is the active layer, which has a lateral extended drift region to stand the high BV and meanwhile provide a relative low R_{ON}. This drift region usually adopts a retrograde doping profile to reduce the electric field. N+ and P+ regions inside the P- body region compose the source of the device. For some technologies, the P+ region also can be separated from N+ region, forming a backgate/substrate contact.

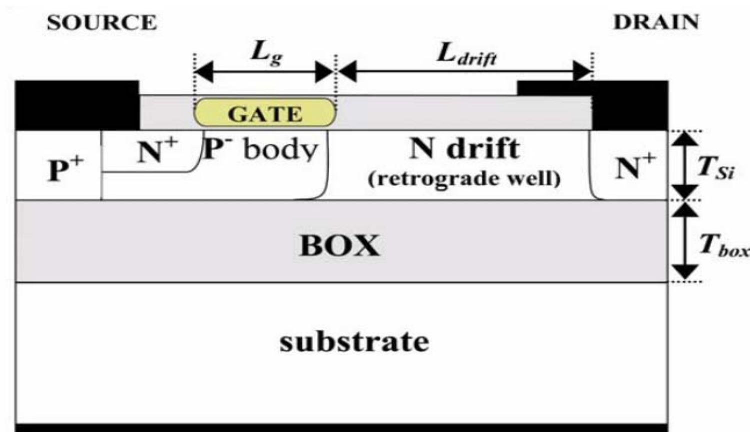

Figure 3. Typical SOI LDMOS Structure

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SOI Bipolar/CMOS/DMOS (BCD) device is used in devices/circuit requiring a mix of transistors characteristics and/or operation voltages. It enables simultaneously handling analog and digital power to realize smart power devices for automotive, telecommunication and consumer electronics [13]. Bipolar component is used for analog control; CMOS component is used for digital control; and DMOS component is used for high currents/voltage application.

2.4 Hot Carrier Reliability

Long-term reliability of MOS VLSI circuits is becoming an important issue as the density of VLSI chips increases with shrinking design rules. Reliability, in general, is a complex problem and related to many different physical failure mechanisms. Some of the physical degradation mechanisms appear themselves by abrupt and catastrophic changes in the device characteristics and the circuit performance; while other mechanisms, such as hot carrier effects, cause noncatastrophic failures which develop gradually over time and change the circuit performance [14]. Hot carrier reliability has been the subject of numerous studies over the past several decades.

The presence of large electric field in MOSFET implies the presence of high energy carriers, referred to as “hot-carriers”, which have a much higher kinetic energy than the average carrier population. It can be illustrated by comparing the

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kinetic energies and the corresponding temperatures with those for carriers in thermal equilibrium. The electrons in a semiconductor material in thermal equilibrium have energy E slightly higher than the bottom of the conduction band E_C, i.e., $E - E_C \approx kT$, where T is the device temperature, and k is Boltzmann's constant. Under non-equilibrium conditions, carriers possessing kinetic energies larger than the thermal equilibrium contribute to current flow. If the carriers encounter a large electric field, like moving along the channel of a MOSFET, their kinetic energies increase in a relatively short distance. The kinetic energy of an accelerated electron can be expressed by $E - E_C \approx kT_e > kT$, where T_e is the effective temperature. This T_e can be much higher than the ambient temperature T of the device. Therefore, these high energy electrons and holes are described as "hot carriers", referring to their effective temperature T_e [15]. The carriers gaining sufficiently high energies and momenta in the high electric field can get injected from the semiconductor into the surrounding dielectric films such as the gate and sidewall oxides as well as the buried oxide in the case of SOI device to form defects. The presence of these defects in the oxide will induce device parameter' shifts, such as transconductance degradation, threshold voltage shift, both linear and saturation currents decrease. Fig 4 shows the HCI degradation mechanisms [16]. High electric field induces high energy hot carriers, which will cause carrier scattering or impact ionization. As a result, charge injection occurs at the Si/SiO_2 interface, forming charge trapping and interface trap generation, which finally renders "localized oxide damage".

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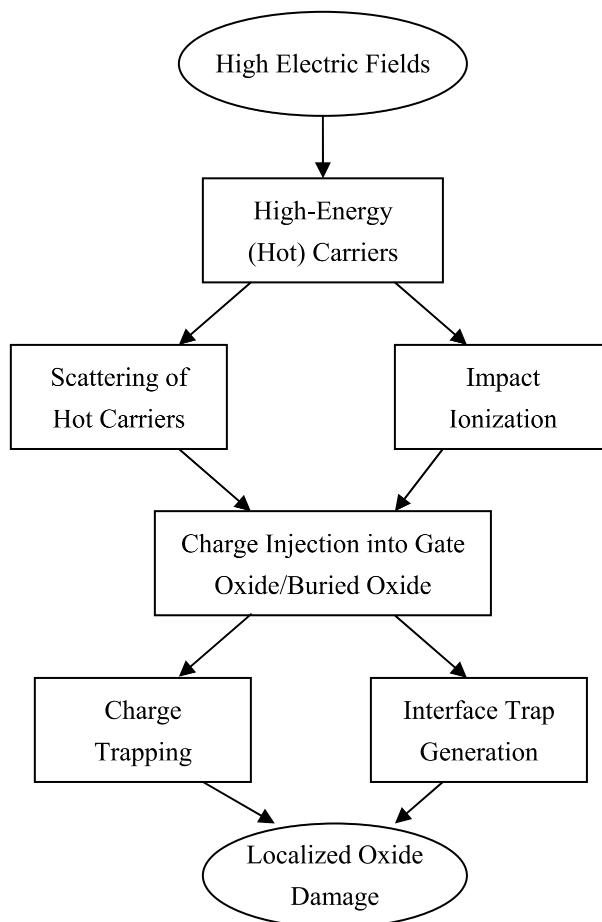

Figure 4. Hot Carrier Induced Oxide Degradation Mechanisms

When carriers in silicon gain energies above a certain threshold, they can generate electron-hole pairs through impact ionization (II) process. II is a process when an electron in the conduction band excites an electron from the valence band resulting in two electrons in the conduction band and a hole in the valence band. Both the total energy and momentum are conserved during this process. In general, the impact ionization process itself has no dependence on the electric field as long as the electron has enough energy it can trigger impact ionization. However, the carrier energy is usually expressed as a function of the local electric field. This relation is usually extended to express the impact ionization rate as a function of

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the electric field. Electrons and holes generated due to impact-ionization in the high field region of the device can themselves gain large enough energies to be injected into the silicon oxide as an additional source of hot-carriers. In fact, in n-channel MOSFETs these impact-generated carriers are responsible for the majority of HC degradation [16].

The energetic carriers lose their energy via II resulting in high substrate current (I_{SUB}) consisting of II generated majority carriers, hence I_{SUB} serves as a good measure of the II generation rate in MOSFET [17]. In our case, for this SOI LDNMOS, I_{SUB} in the active SOI layer, which is also called back gate current, is used as the indicator for hot carrier generation due to the real substrate layer (handler wafer) is isolated by BOX. This I_{SUB} is mainly composed by the holes generated by the II in the active SOI layer.

The hot carrier effect of SOI PMOSFET is much less than that of SOI NMOSFET. This is because under the condition of given electric field, the II generation rate of holes is two or three orders of magnitude less than that of electrons. At the same time, the height of the potential barrier for holes is much higher than that of electrons [3].

According to the 5th Edition Hitachi Semiconductor Device Reliability Handbook, there are four commonly encountered hot carrier injection mechanisms as shown in Fig 5 and discussed below.

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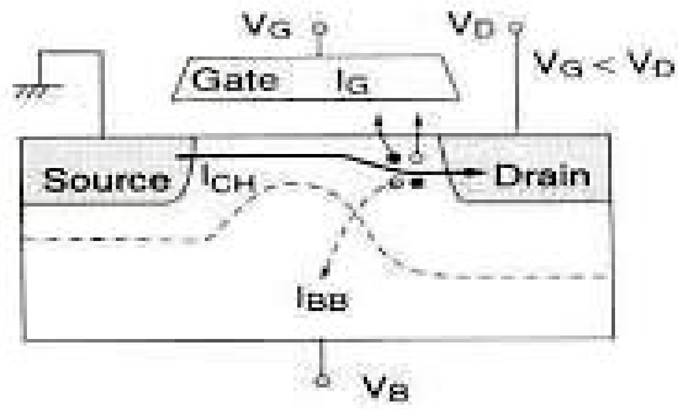

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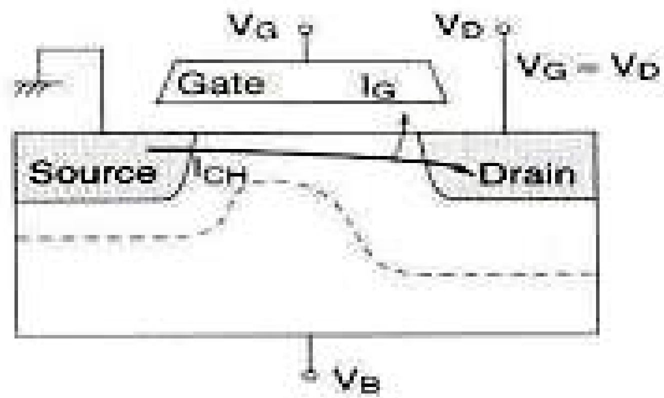

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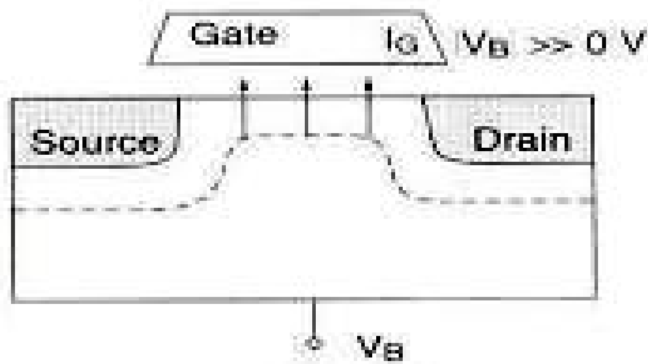

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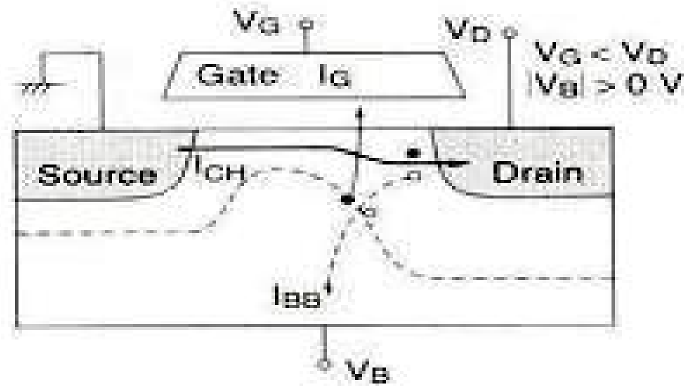

(d)

Figure 5. Four HCI Mechanisms

(a) DAHC Injection; (b) CHE Injection; (c) SHE Injection; (d) SGHE Injection

1. Drain Avalanche Hot Carrier (DAHC) Injection: It occurs when a high voltage applied at the drain under non-saturated conditions (V_D>V_G) resulting in a very high electric field near the drain, which accelerates channel carriers into the drain's depletion region. This produces the worst device degradation under normal operating temperature range. The acceleration of the channel carriers causes them to collide with Si lattice atoms, creating dislodged electron-hole pairs in the process (impact ionization). Under the influence of high electric field, hot carriers that overcome the electric potential barrier between the silicon substrate and the gate oxide get injected into the gate oxide layer. This hot carrier injection process occurs mainly in a narrow injection zone near the drain end where the lateral field is at its maximum. Hot carriers can be trapped at the Si-SiO_2 interface (interface states) or within the oxide itself, forming a space charge (volume charge). Injected carriers that do not get trapped become gate current. The majority of the generated

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holes flow back to the substrate, comprising a large portion of the substrate current.

2. Channel Hot Electron (CHE) Injection: It occurs when both V_G and V_D are significantly higher than V_S, with $V_G \approx V_D$. Channel carriers that travel from the source to the drain are sometimes driven towards the gate oxide even before they reach the drain because of the high V_G.

3. Substrate Hot Electron (SHE) Injection: It occurs when the substrate back bias is very positive or negative, i.e., $|V_B| >> 0$. Under this condition, carriers of one type in the substrate are driven by the substrate field toward the surface Si-SiO_2 interface. As they move toward the interface, they further gain kinetic energy from the high field in the surface depletion region; eventually overcome the surface energy barrier and get injected into the gate oxide, where some of them are trapped. This mechanism is not applicable for SOI device. Therefore, in our case, this mechanism no needs to be considered.

4. Secondary Generated Hot Electron (SGHE) Injection: It involves the generation of hot carriers from II process involving a secondary carrier that was likewise created by an earlier incident of II. It has similar conditions as mechanism 1, i.e., $V_D > V_G$. The main difference is the influence of the substrate back bias in the hot carrier generation. This back bias results in a field that tends to drive the hot carriers generated by secondary carriers toward the surface region, where they further gain kinetic energy to overcome the surface energy barrier.

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The general guide lines to suppress the hot carrier effects are from device structure and processing two aspects [18]:

1. Device Structure Aspect: It works on two perspectives:

1). Suppress Hot Carrier Generation:

a). Reduce the high electric field;

b). Move the main current path away from high electric field regions.

2). Suppress Hot Carrier Injection:

a). Push the high II region deep into the active silicon layer;

b). Position the injection inside the gate edge.

2. Processing Aspect: It mainly works on hot carrier trapping problem:

1). Reduce the amount of trapping centers in the gate oxide:

a). Start the process with a high-quality initial oxide (better oxidation techniques);

b). Maintain good oxide during processing by reducing radiation damage.

2). Reduce the bond breakage rate during hot carrier injection:

a). Reduce the hydrogen (catalyst) content in the process, since the creation of interface traps by hot carriers is linked to hydrogen-bond breakage at the interface.

In device design, we usually develop the device structures which are less sensitive to hot carrier problem by reducing the high lateral electric field and/or separating the main current path from the high electric field regions.

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2.5 Interface Traps Generation

One of the most important hot carrier reliability issues is the interface traps' generation. Interface traps are one type of defect associated with device hot carrier degradation (HCD) at the Si/SiO_2 interface. These interfacial defects introduce energy states, usually referred to as "interface states", in the Si bandgap at the interface. The occupancy of these interface states depends on the local surface potential [16, 19, 20]. The atomic structure associated with interface traps in MOSFETs is believed to be silicon dangling bond site at the interface known as the P_b-center. In fully processed MOSFETs, the dangling bonds are passivated with hydrogen and are expected to be electrically inactive. Hydrogen released by carrier trapping in the oxide can migrate to the Si-SiO_2 interface and react with the passivated dangling bonds (P_b-H). This reaction results in depassivation of the dangling bonds producing electrically active P_b-centers [21, 22]. Hot carriers have been observed to directly result in depassivation of P_b-H sites rendering the interface traps. Based on this multi-vibrational hydrogen release mechanism, modified reaction-diffusion model for HCI degradation was proposed and studied by many researchers [23, 24].

2.6 Hot Carrier Induced (HCI) Degradation Test

The HCI degradation of MOS transistor has been found to result from either trapping of carriers on defect sites in the oxide or the creation of interface states at

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the silicon-oxide interface, or both. For NMOS transistor, electron trapping is the dominate charge trapping mechanism, and the generated interface traps are mostly acceptor-type, i.e., negatively charged when occupied by an electron, and neutral otherwise [25]. Capacitance-voltage (CV) measurement can be performed to determine the total amount of trapping charge in the oxide. For electrical characterization of interface traps, charge pumping techniques are developed and applied. It allows simple determination of the type of interface states generated, their exact amount and spatial distribution. The damage caused by hot carrier injection affects the transistor characteristics by causing degradation in transconductance, a shift in the threshold voltage and a decrease in drain current capability. All these performance degradations in the devices lead to the degradation of circuit performance over time.

Trapped charges in the gate oxide form the fixed oxide change, which will influence the surface potential, the oxide electric field, and hence the local flat-band voltage. Positive shift of the threshold voltage is indicative for the negative trapped charges, and negative shift for the positive trapped charge. For NMOS transistor, the accumulating negative charges (electrons trapping) shift the local flat-band voltage into the positive direction, and increase the threshold voltage.

When the interface traps locate at the gate-oxide/ silicon interface of the channel region, they will start to be occupied by the carriers from the substrate as the surface is biased from accumulation first into weak inversion, and then strong

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inversion. This will influence the local flat-band voltage which is similar to the influence of the fixed oxide charges. For n-type MOSFET, the acceptor-type interface states at the gate-oxide/ silicon interface are charged by the electrons in the channel under strong inversion for practical bias conditions. Therefore, the local flat-band voltage shifts into positive direction due to the negatively charged interface traps. The increase of the local flat-band due to both the gate-oxide trapping charges and the interface traps in NMOS transistor will increase the threshold voltage, and decrease the channel current.

The interface charges may also vary the charges distribution near the interface, and change the doping concentration locally. Consequently, the resistance and the electric field will be affected, which are reflected as a shift of I_D and I_{SUB}.

The carrier mobility near the interface will be decreased locally as a result of the increased surface scattering caused by the present of interface states, which will lead a reduction of the drain current, and the channel transconductance G_m [26-28].

It is well known that the HCI degradation reaches a maximum when the stress bias condition is in the middle range of V_G. The position of this HCI degradation peak has been found to coincide with the maximum of I_{SUB}, which is linked with the carriers generated by II [15]. Therefore, usually the HCI degradation stress test is done at this degradation peak condition, i.e. stressed at the maximum I_{SUB} bias conditions. Electrical parameters are monitored during the stress time interval.

In contrast to most reliability problem, the generation of hot carriers is enhanced when the operation temperature is low. HCI degradation is recognized to be severe

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at room temperature [29]. As a result, the degradation stress test usually is done at the constant room temperature.

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Chapter 3. Experimental Measurement and Simulation

3.1 Device Description

A cross sectional view of the SOI LDNMOS device structure is shown in Fig 6 (not to scale). The device consists of a channel region which is a combination of p-type implant body region (PBO) and P-Well, an extended lightly n-type doped drift region (NWD) above the buried oxide (BOX) layer, an n-type body region (NBO) and a lightly n-type doped handle wafer. The STI depth is 370 nm. The SOI layer and long poly-gate plate are used as a double reduced surface field (RESURF) design to increase the breakdown voltage significantly. Its off-state breakdown voltage is around 175 V, which is verified experimentally. The aimed supply voltage V_{DD} is 3.3 V. Other details for the device cannot be disclosed due to company's confidentiality.

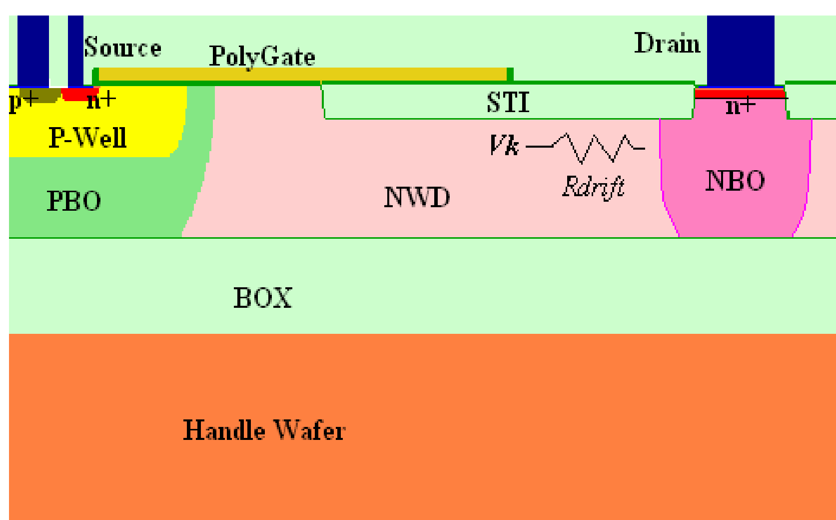

Figure 6. The Cross-Sectional View of the SOI LDNMOSFET

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During the impact ionization process in the SOI active layer, electron-hole pairs are generated. The generated holes go to the substrate contact at the P+ region in P-well and form the substrate current. This substrate contact is separated from the source contact as shown in Fig 6. In Fig 6, V_K refers to the potential in the drift region under the right edge of the poly-silicon gate; and R_{drift} refers to the drift region resistance between the drain side and V_K.

3.2 Experimental Measurement

HP4156 Parameter Analyzer is used for the measurement with a detection limit of about 1pA, and the handle wafer and source contact are grounded during the measurement. Range of the applied V_G is 0 ~ 3.3 V, and the step size of V_G sweep is 0.05 V; range of V_D is 0 ~ 40 V, and the step size of V_D sweep is 0.5 V. The SOI LDNMOS device has its SOI substrate contact separated from its source contact, so that the source and substrate currents can be measured independently. The measured I_{SUB} is the SOI active layer substrate current collected at the p+ contact region in the p-well, which is also known as I_{BG}, i.e. back gate current. The current collected at the n+ contact region in the p-well is taken as $I_{SOURCE.}$

The details of the experimental setup and design of the HCI degradation test will be introduced in Chapter 6 “Hot Carrier Induced (HCI) Degradation Test”.

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Since the operation V_D of our device is much higher than V_G as it is a high power device, the channel hot electron (CHE) injection mechanism can be avoided in our consideration in this work. Also, because the substrate of our device, i.e. the handler wafer, is isolated by BOX layer and grounded, the substrate hot electron (SHE) and secondary generated hot electron (SGHE) injection mechanisms can also be neglected. Therefore, the main hot carrier injection mechanism in our device is the drain avalanche hot carrier (DAHC) mechanism. This degradation mechanism is induced by the hot carrier generation due mainly to the II in the SOI active layer. The holes generated by II in the active SOI layer contribute to a larger portion of I_{SUB} as defined previously. Therefore, I_{SUB} is determined by both the number of carriers in the channel and the electric field [29]. In this work the severity of the hot carrier generation on this SOI LDNMOS is investigated by measuring and simulating I_{SUB} in the SOI active layer.

As mentioned before, one particular hot carrier problem is concerned with hot electrons injected from the channel into the gate. The severity of hot carrier generation can be assessed/predicted using either the I_G or I_{SUB} [30]. As shown in our experiment results, Fig 7 is the experimental measurements of I_G under bias conditions of $V_G = 2$ V, while V_D is sweeping from 0 to 40 V; and of $V_D = 40$ V, while V_G is sweeping from 0 to 3.3 V respectively. The solid line and dot line denote I_G from two repeated measurements. It can be seen that the measured I_G in our device behaviors like noise. Physically, both substrate and gate currents are derived from the same source of hot carriers in the high II site. The holes generated

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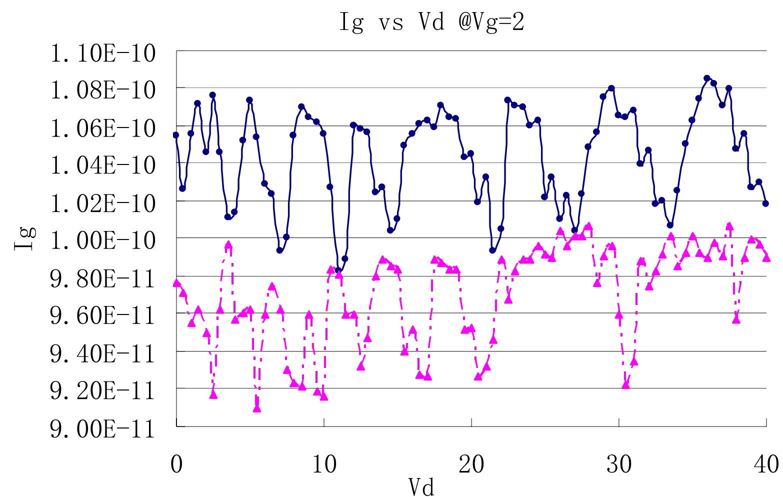
by impact ionization go to the back gate contact forming I_{SUB}. Due to the high V_D and the location of the II peak in our device is quite far below the gate as will be seen in later analysis, most of the electrons generated by II go to the drain side, and just small part of them go to the gate forming the gate leakage current. Therefore, I_G is not used in this work as the indicator of the hot carrier problem.



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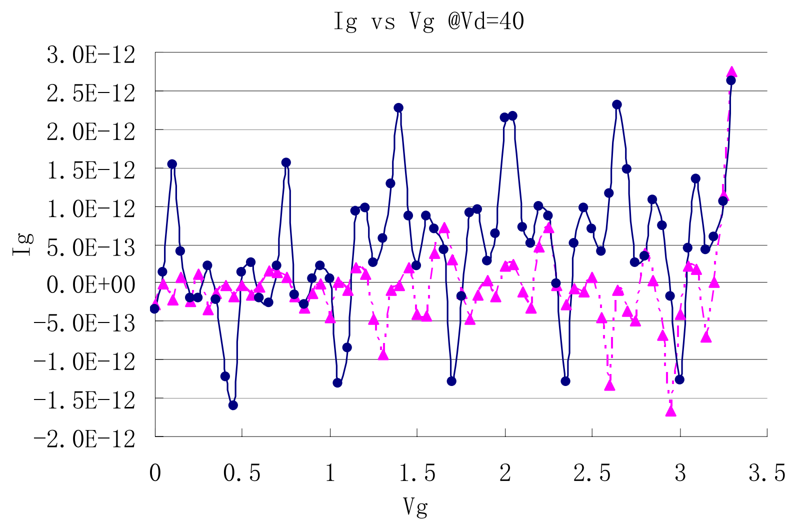

(b)

Figure 7. I_G Measurements

(a) @V_G = 2 V, V_D = 0 ~ 40 V; (b) @V_D = 40 V, V_G = 0 ~ 3.3 V

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3.3 Simulation Structure

Fig 8 shows the device mesh structure created by Tsuprem4 process simulation program. Only the top 2.5 μm of the handle wafer is shown for clear illustration of the electrical characteristics distributions in the SOI active layer. The horizontal scale is the length of the device, and the vertical scale is the depth of the device.

In Fig 8, the sharp STI corners, especially the left corner which is near the PBO-NWD junction, are suspected to induce high electric field locally and have crowded electron current flow, thereby having high II generation rate nearby. To suppress the hot carrier problem, we rounded the STI corners both in the real device production and the Tsuprem4 process simulation.

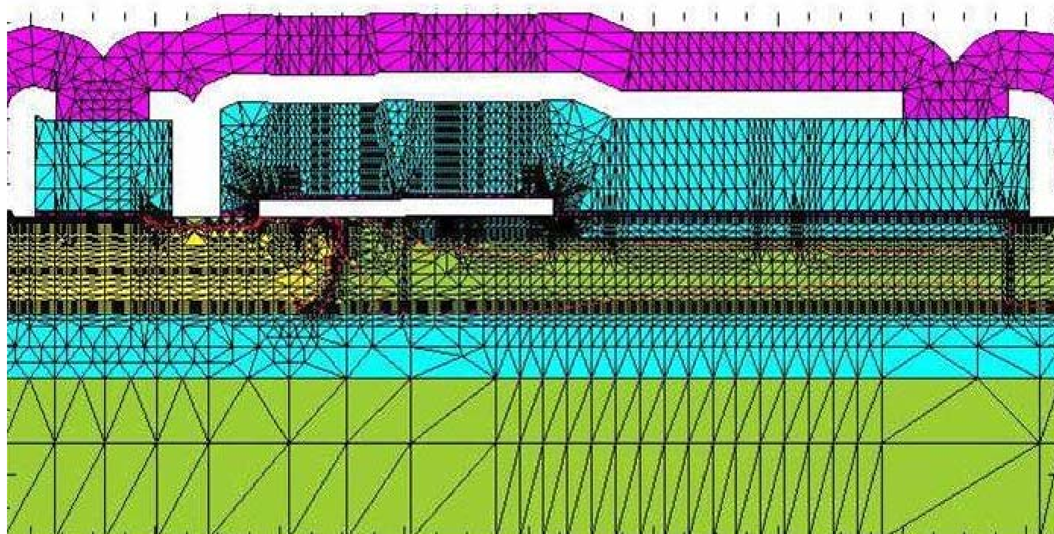

Figure 8. Device Mesh Structure created by Tsuprem4

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3.4 Simulation Methodology

In this work, Tsuprem4 [31] is used for the process simulation to obtain the doping profiles and contact layers of the device structure as shown in Fig 7. The structure and doping profiles of the device are then imported to MEDICI [32] program for the II analysis by using IMPACT.I in MODEL and SOLVE statements. The IMPACT.I enables us to obtain the I_{SUB} which is mainly formed due to the II process. In our simulation, LAT.TEMP and COUP.LAT are also used in SYMBOLIC statement to include the lattice temperature effects on the device's electrical characteristics, i.e. the self-heating effect in the SOI active layer in our case. The LAT.TEMP specifies that the simulation is done for the Poisson and continuity equations, as well as lattice temperature determination. COUP.LAT specifies that the lattice temperature equation is fully coupled with the Poisson and continuity equations during device simulation [32].

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Chapter 4. Hot Carrier Generation Analysis

In this chapter, the hot carrier generation of the SOI LDNMOS device is investigated under different biasing conditions. I_{SUB} is used as an indicator for the hot carrier generation. Experimental measurement and simulation of I_D and I_{SUB} are performed, which provide a better insight for its hot carrier generation process by looking at the electric field, J_E and II generation rate distributions in the devices.

4.1 Drain Current Results and Discussion

Fig 9 shows the simulation and experiment comparison of I_D at $V_G = 2$ V, with V_D sweeping from 0 to 40 V. The simulation and experiment results fit very well. One phenomenon for I_D characteristics is that it reduces a little bit as V_D further increased. This is due to the self-heating effect as discussed in Chapter 2. At high V_D operation condition, due to the low thermal conductivity of BOX (about two orders of magnitude less than that of silicon), the temperature locally increases in the active SOI layer resulting in the carrier mobility (μ) reduction with temperature increasing [33]. The $I_{D,SAT}$ equation below clearly shows that I_D mainly depends on μ for a given V_G and device dimensions. Therefore, the reduction of μ with temperature increasing results in a lower I_D.

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$$I_{D,SAT} = \mu \cdot C_{OX} \frac{W}{L} \cdot \frac{(V_G - V_{TH})^2}{2} \quad (5)$$

where μ is the carrier mobility, C_{OX} is the oxide capacitance, V_{TH} is the threshold voltage, W and L are the width and length of the transistor respectively.

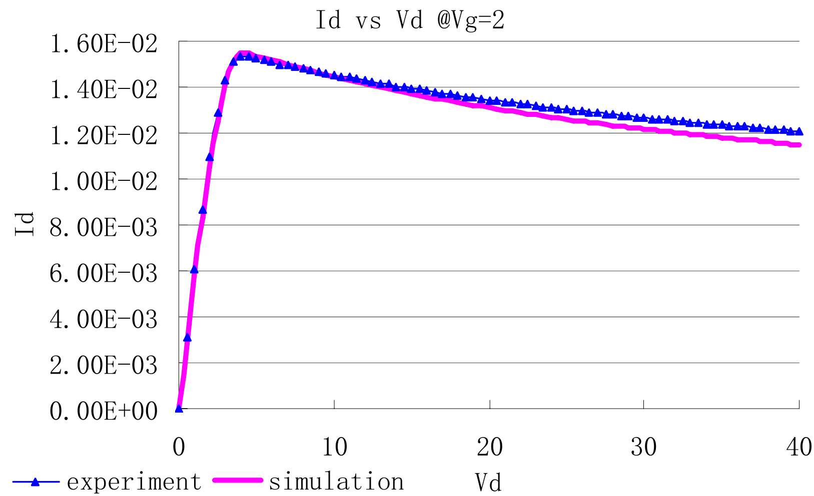

Figure 9. I_D Measurement & Simulation Comparison @V_G = 2 V, V_D = 0 ~ 40 V

Fig 10 gives the lattice temperature distributions at different V_D and V_G. Please refer to Fig 8, which shows the device structure corresponding to that in Fig 10. The x-axis is corresponding to the length of the device, and the y-axis is corresponding to the depth of the device. Same descriptions for X and Y are applied for the later figures. As seen in Fig 10, the handler wafer is treated as the thermal electrode (heat sink) at room temperature 300 K. The temperature in the active SOI layer increases due to the self-heating effect. The temperature drops over BOX to 300 K in the handler wafer. At V_D=10 V and V_G =1.5 V, the

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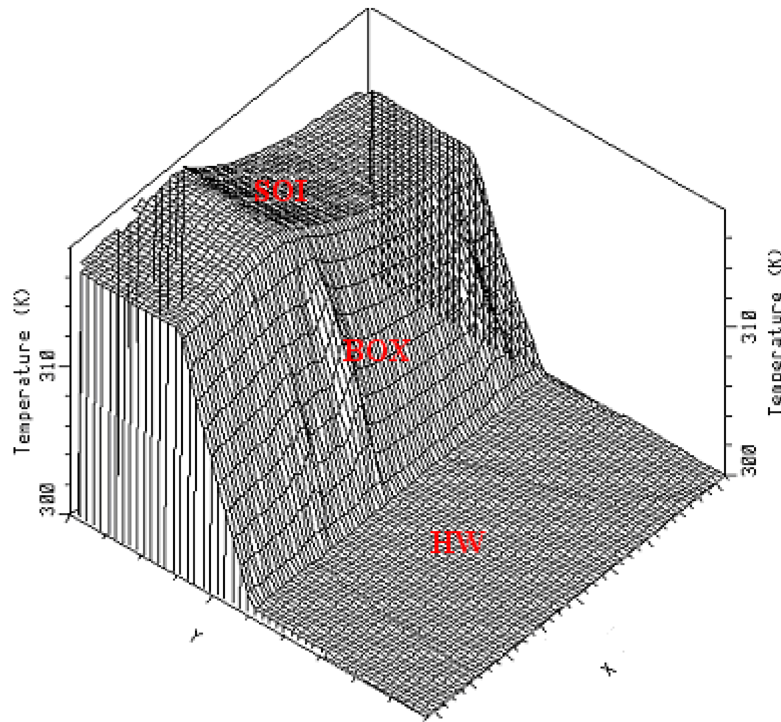
temperature in the active SOI layer is around 320 K, which increases to 360 K when V_D increases to 40 V. At V_D=40 V and higher V_G =2.5, the temperature further increases to 480 K. Therefore, both higher V_D and/or V_G will induce larger self-heating effect in SOI layer.



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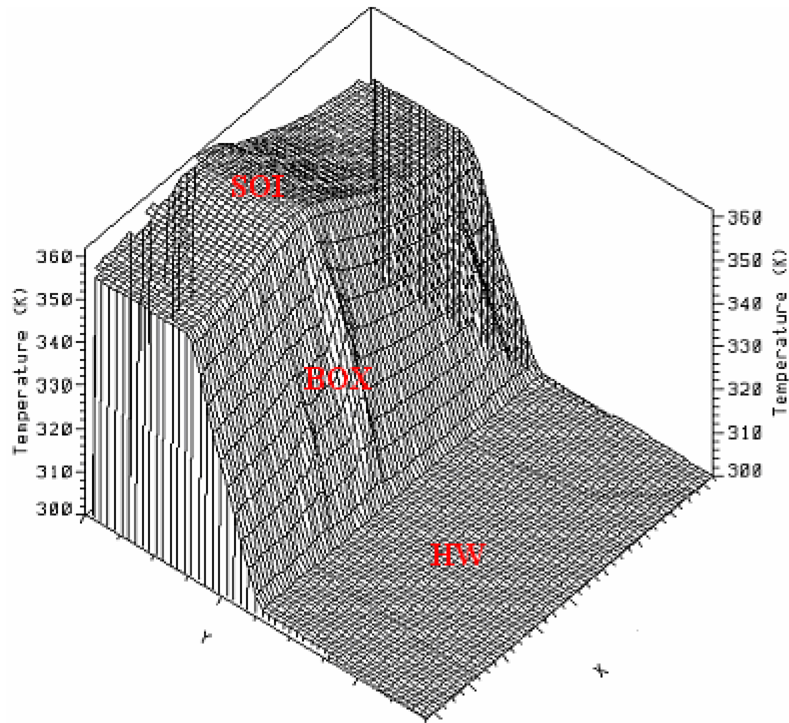

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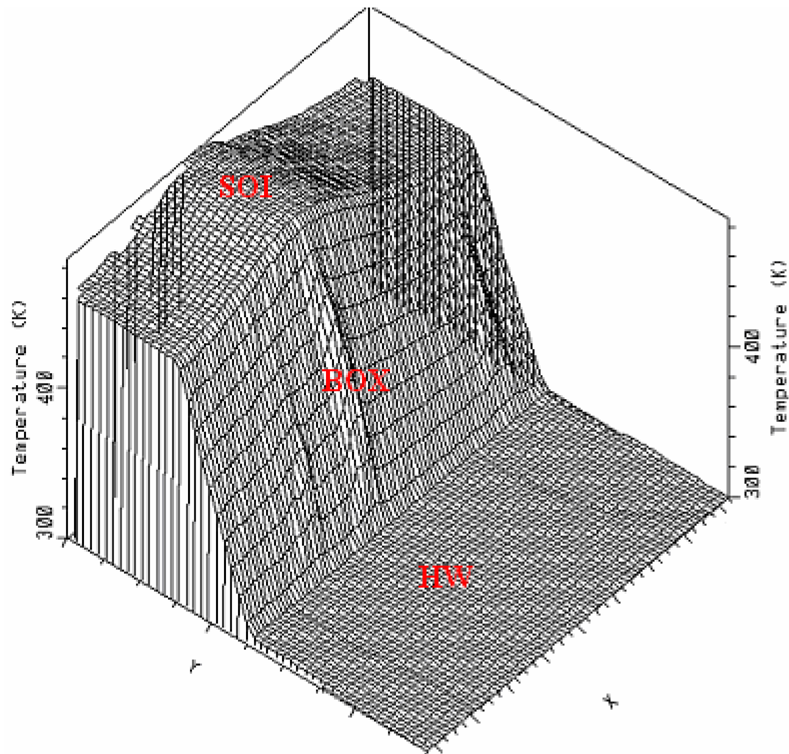

(c)

Figure 10. Lattice Temperature Distributions at Different V_G & V_D

(a) V_D=10 V & V_G=1.5 V; (b) V_D=40 V & V_G=1.5 V; (c) V_D=40 V & V_G=2.5 V

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4.2 Substrate Current Results and Discussion

Experimental result of I_{SUB} vs. V_G at V_D = 40 V is shown in Figure 11, which shows a typical behavior observed in standard MOSFET, indicating the presence of different degree of II under various biasing conditions.

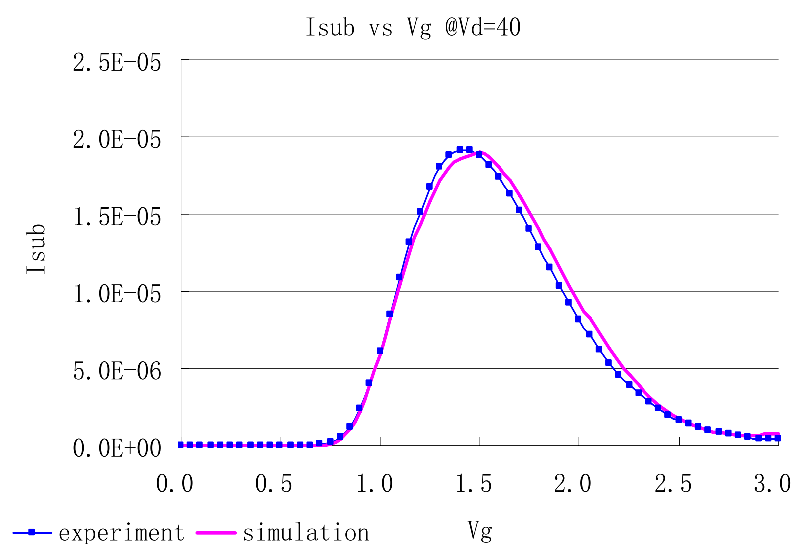

Figure 11. I_{SUB} Measurement & Simulation Comparison @V_D = 40 V, V_G = 0 ~ 3 V

In Fig 11, we can see the reasonable good agreement between the experiment and simulation results. We also compared the value of R_{ON} from our simulation result with that of the real device, and we found that they are very close. Since R_{ON} is closely associated to the doping profile in SOI active layer, the closeness of R_{ON} value indicates that the doping profile of the simulation and the real device is indeed close to each other.

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As can be seen in Fig 11, I_{SUB} increases with V_G in the low V_G region. This is due to the increase in the channel current as V_G increases as can be seen in Fig 12. On the other hand, I_{SUB} decreases with V_G in the high V_G region due to a decrease of the electric field peak which will be elaborated later. As a result, there is a point within the sweeping range of V_G where I_{SUB} is maximum [34].

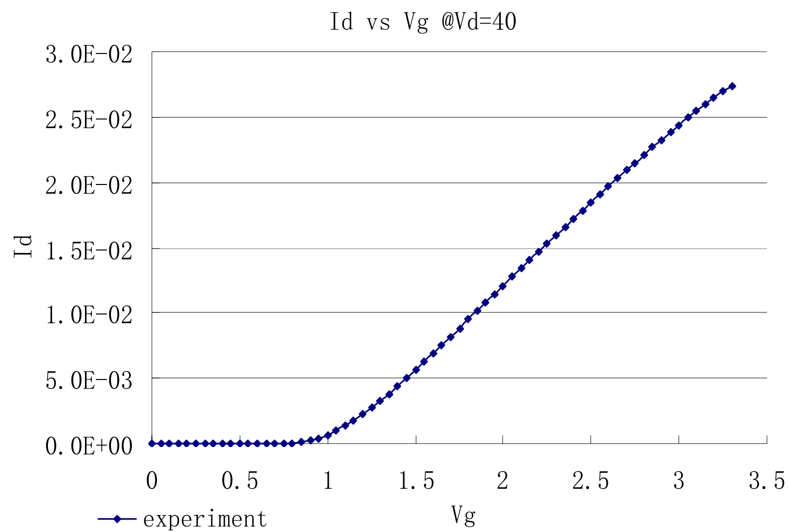

Figure 12. I_D Measurement Results @V_D = 40 V, V_G = 0 ~ 3.3 V

4.2.1 Electric field Distribution

Since I_{SUB} is mainly due to the holes generated by II in the high field region, details about the electric field distribution in the device are necessary in order to study the hot carrier generation in the devices [29].

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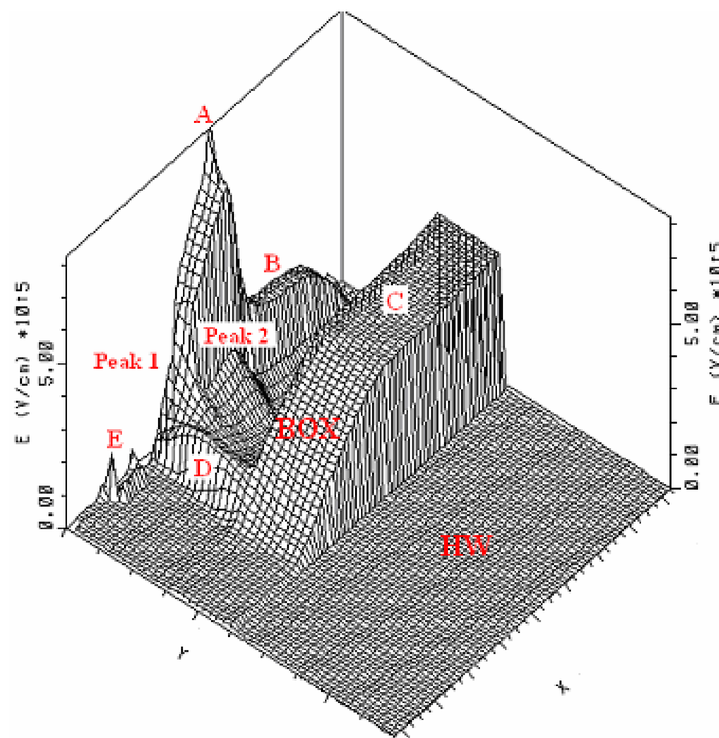
4.2.1.1 Effect of V_G on Electric field Distribution

Fig 13 shows the electric field distributions in the device at V_D = 40 V and different values of V_G. An electric field peak is observed at the right edge of the poly-silicon gate (Peak A). This peak is formed due to the large voltage difference between V_G and V_K (the voltage in the drift region below STI at the right edge of the poly-silicon gate in Fig 6) across the STI layer. Voltage drops from 40 V at the hard-drain side to 0 V at the source side. Below the right edge of the poly-silicon gate, the voltage in the drift region is still quite high (around 30 V) as can be explained in Fig 14.



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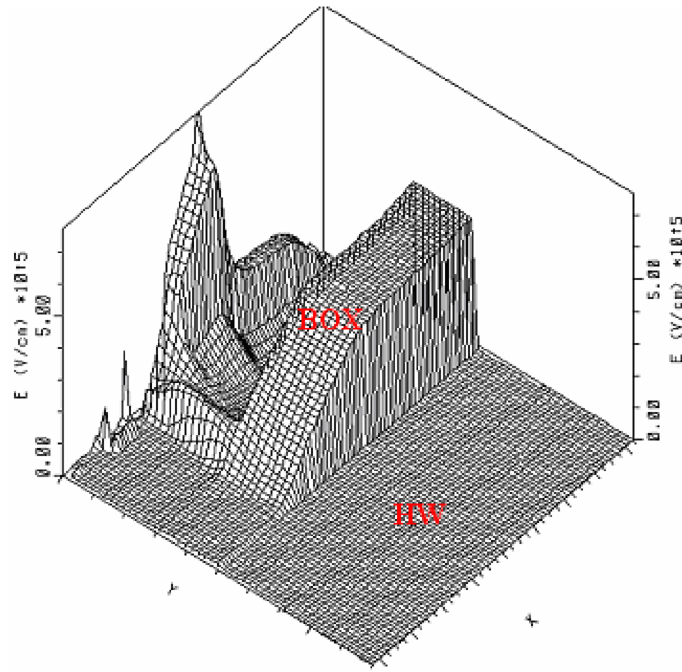

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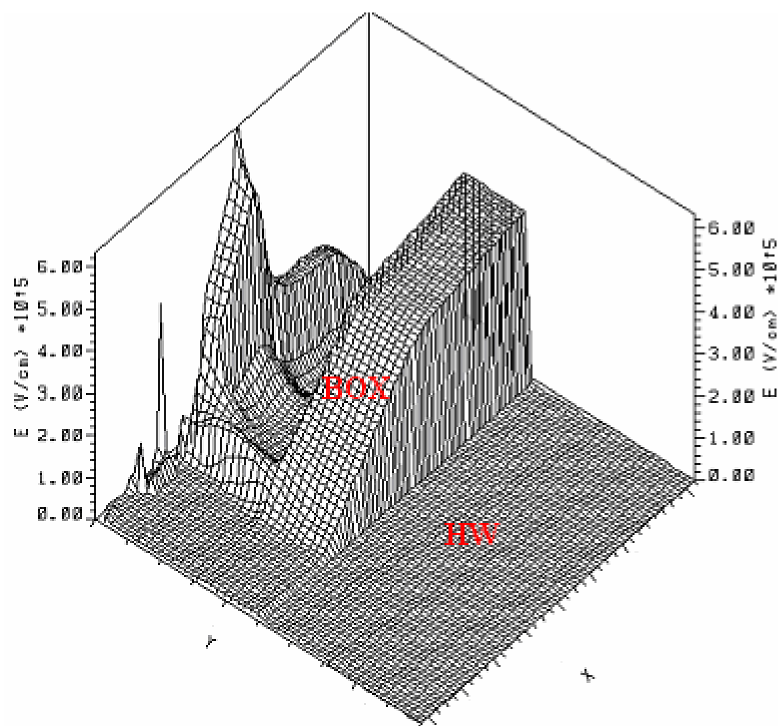

(c)

Figure 13. Electric field Distribution in the Device @ V_D = 40 V, and

(a) V_G = 0.5 V; (b) V_G =1.5 V; (c) V_G = 2.5 V

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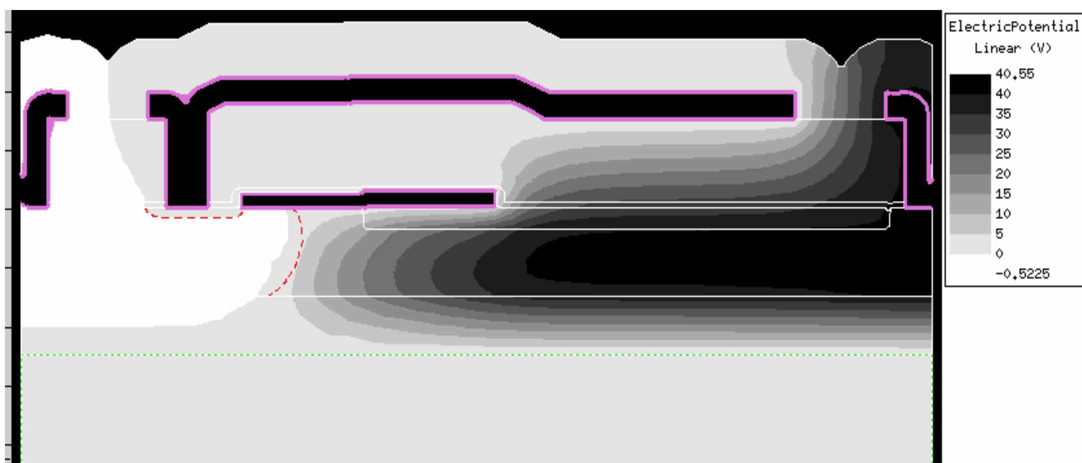
Fig 14 is the potential contours at $V_D = 40$ V with different V_G. We can see that the potential contour lines are very dense in the PBO/NWD region, indicating a significant potential drop along the SOI active layer near the PBO/NWD junction. On the other hand, as the right side of the drift region is not yet depleted at $V_D = 40$ V, the potential does not drop significantly in the non-depleted drift region, rendering V_K (in Fig 6) remains high with its value close to V_D. But it drops faster at high V_G, which is due to the larger current in the drift region at higher V_G.



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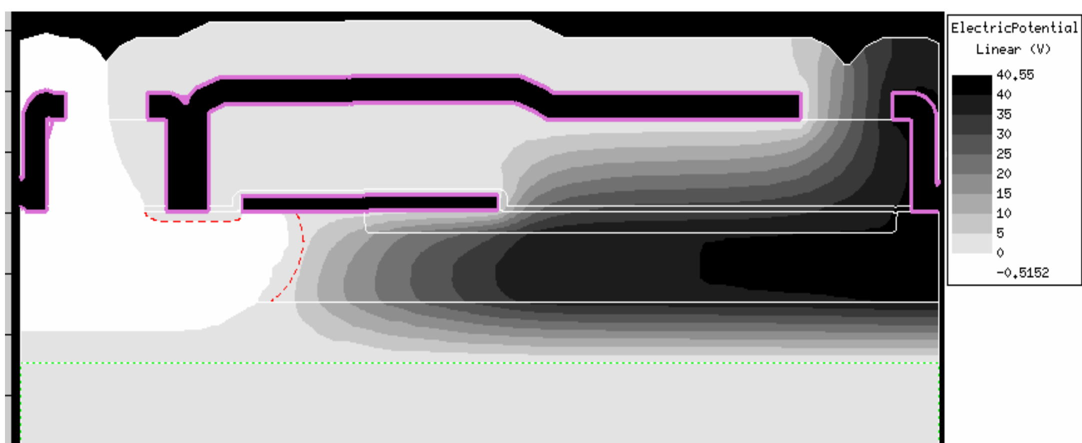

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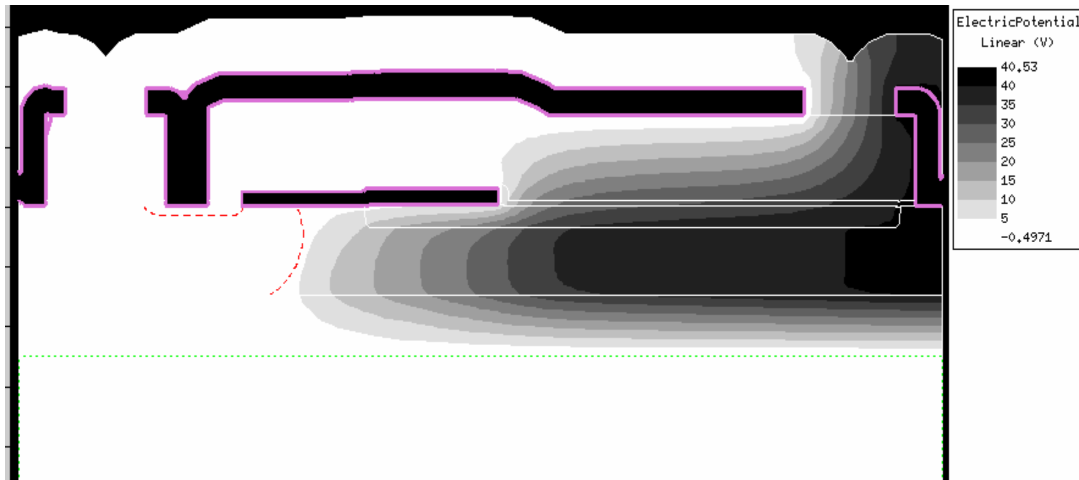

(c)

Figure 14. Potential Contour @ V_D = 40 V, and

(a) V_G = 0.5 V; (b) V_G =1.5 V; (c) V_G = 2.5 V

In Fig 13, we can see that the value of the electric field peak at point A reduces from $8*10^5$ V/cm to $7.5*10^5$ V/cm, and further to $6*10^5$ V/cm as V_G increasing from 0.5 V to 1.5 V, 2.5 V. This is because as I_D increases with V_G, the voltage drop between V_D and V_K in the non-depleted part of the drift region ($R_{DRIFT}*I_D$) is also increased for a given R_{DRIFT}. Therefore, at a fixed V_D = 40 V, V_K ($V_K = V_D - R_{DRIFT}*I_D$) in the drift region below the STI will reduce as V_G increases, which can also be seen in Fig 14. Hence, the reduction in the voltage difference between the poly-silicon gate (V_G) and the voltage in the drift region (V_K) results in a reduction in the electric field Peak A.

Also, due to the continuity of the electric displacement in the perpendicular direction across the interface of two materials, the electric field at position V_K in the drift region (Peak 2) follows the trend of Peak A via a ratio of the permittivity

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of silicon oxide and silicon ($\varepsilon_{SiO_2}/\varepsilon_{Si} = 3.9/11.7$) [6]. Therefore, Peak 2 also decreases with V_G increasing as Peak A.

Electric field at position B is due to the voltage difference between the metal field-plate (0 V) (top blank contact layer in Fig 8) and the voltage in drift region (close to 40V). This large voltage difference across a thickness of 1.8 μm oxide layer (top azure layer in Fig 8) leads to an electric field of around 40/1.8 μm ≈ 2×10^5 V/cm.

Electric field in position C is due to the voltage drop across the 1 μm BOX layer. Since both the handle wafer side and the source side are grounded, the electric field in BOX is 40 V/1 μm = 4×10^5 V/cm at the drain side. The large slope in the BOX near the PBO/NWD depletion region is due to the large voltage drop in the junction of NWD drift region and the source side (PBO).

Small electric field peak at positions D and E are due to the build-in electric field of the PBO/NWD and N+/P-well junctions respectively. We can see that the electric field peak at the left edge of the poly-silicon gate (Peak 1) increases from $0.5*10^5$ V/cm to $2*10^5$ V/cm and further to $4*10^5$ V/cm with V_G increasing from 0.5 V to 2.5 V. This peak is caused by V_G voltage drop across the gate-oxide/oxide spacer, so the higher the V_G, the higher this peak value is.

Similar comparison of the electric field distribution at V_D = 10 V and various values of V_G is shown in Fig 15. The electric field distribution for V_D = 10 V is quite similar to that of V_D = 40 V. Two peaks located at right edge of the poly-silicon gate in the drift region and the left edge of the poly-silicon gate

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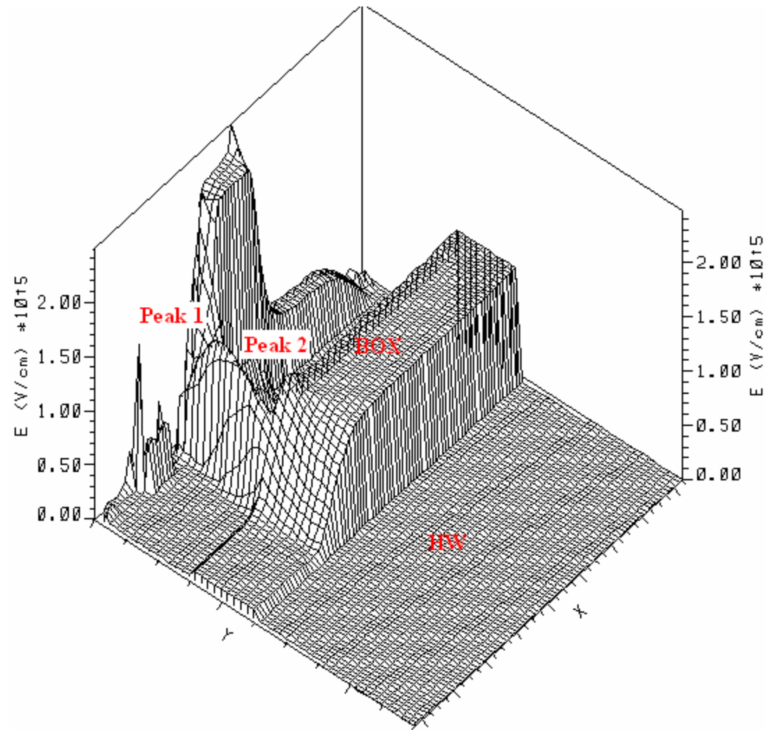
respectively. Similar to the case of $V_D = 40$ V, Peak 1 increases with V_G; and Peak 2 follows with peak A which is reducing as V_G increasing.



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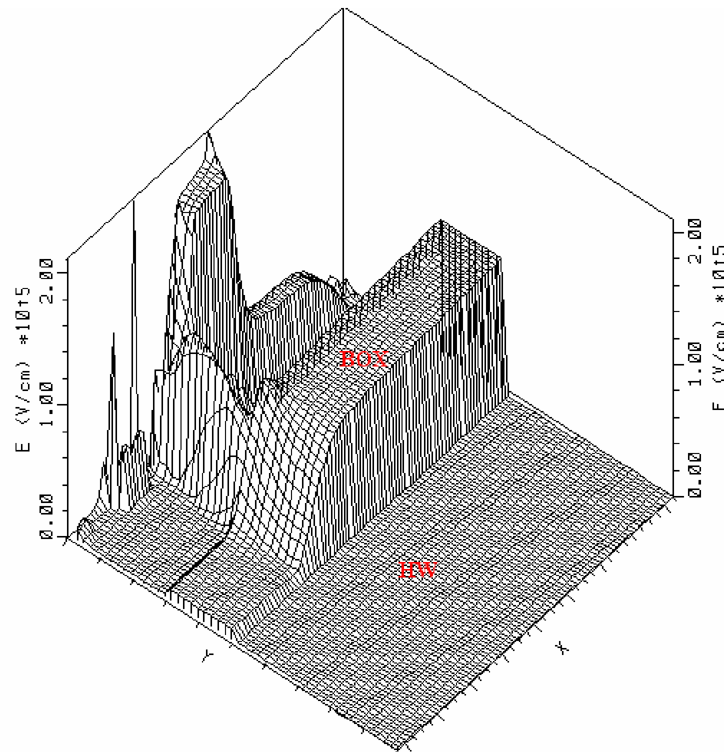

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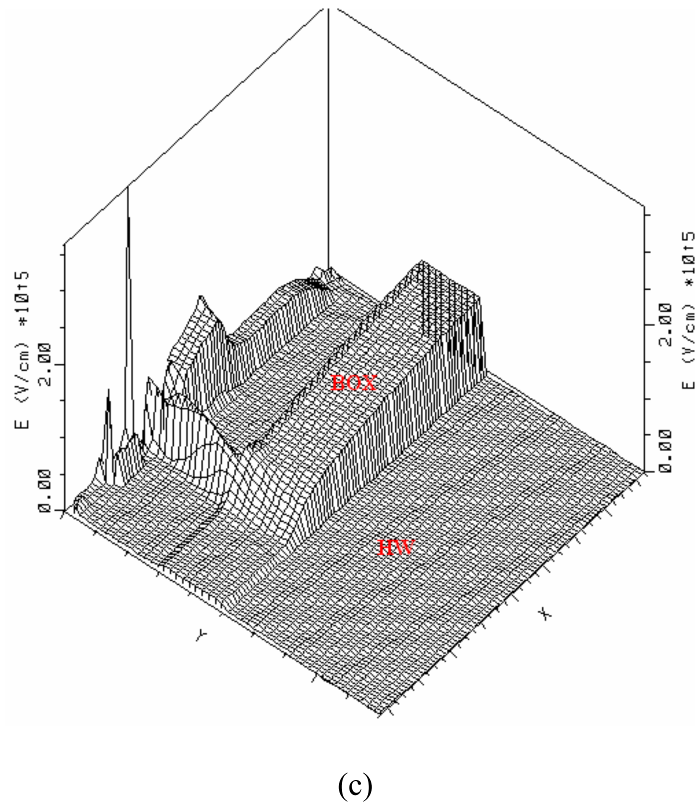

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Figure 15. Electric field Distribution in the Device @ V_D = 10 V, and

(a) V_G = 0.5 V; (b) V_G = 1.5 V; (c) V_G = 2.5 V

4.2.1.2 Effect of V_D on Electric field Distribution

As previous I_{SUB} vs. V_G curve shows that maximum I_{SUB} occurs around V_G = 1.5 V, we look at the electric field distributions at a fixed V_G = 1.5 V, and V_D = 10 V and 40 V respectively in order to study the effect of V_D on hot carrier generation. Fig 16 shows the electric field Peak A increases from $2*10^5$ V/cm at V_D = 10 V to $7.5*10^5$ V/cm at high V_D = 40 V. This is because, at a given V_G, V_K increases for higher V_D, and hence the voltage difference between V_G and V_K is larger, which makes both Peak A and Peak 2 increase.

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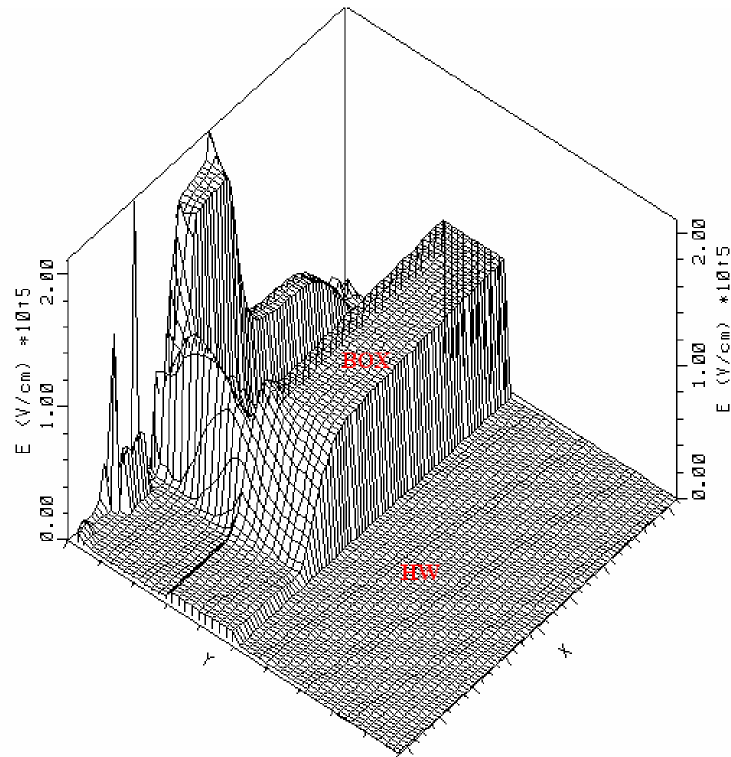

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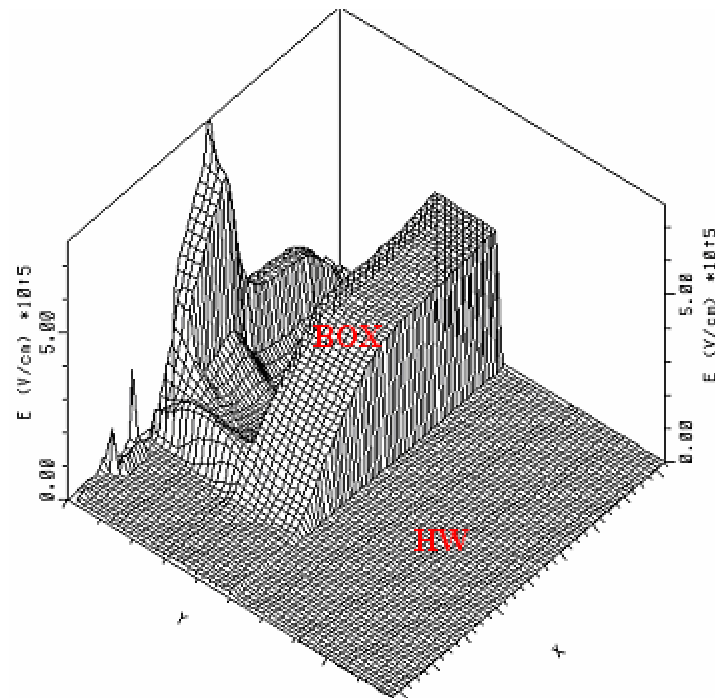

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Figure 16. Electric field Distribution in the Device @ $V_G = 1.5$ V, and

(a) $V_D = 10$ V; (b) $V_D = 40$ V

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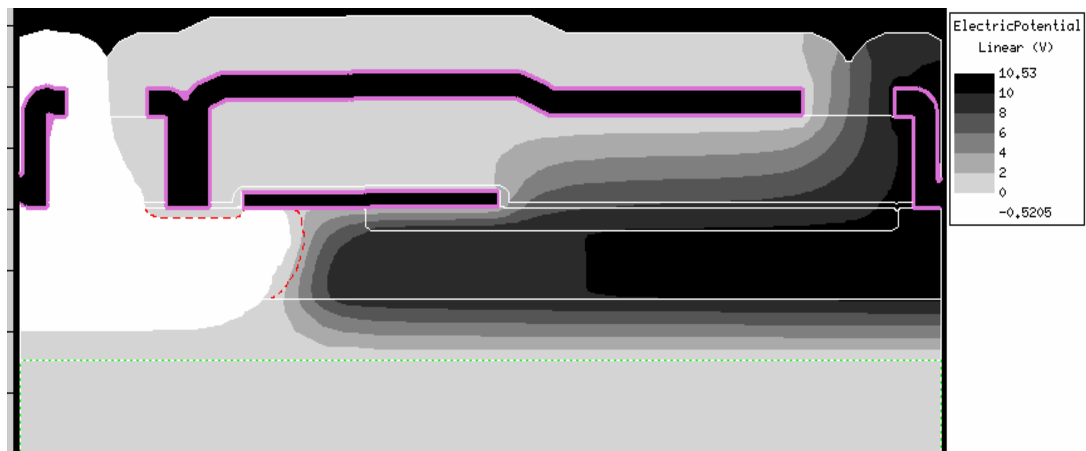
At V_D = 40 V, the electric field at position D (PBO/NWD junction) also increases slightly due to the larger potential drops there for higher drain side potential as can be seen in Fig 17 the potential contour plot at V_G = 1.5 V and V_D = 10 V and 40 V respectively. At V_D = 10 V, potential cross NWD/PBO drops from 8 V to 0 V, while at V_D = 40 V, it drops from around 20 V to 0 V.



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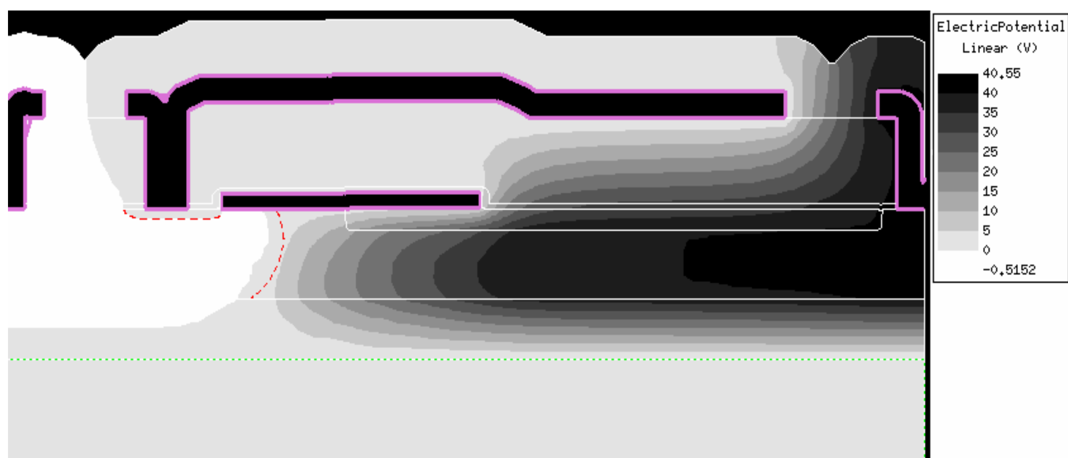

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Figure 17. Potential Contour @ V_G = 1.5 V, and (a) V_D =10 V; (b) V_D = 40 V

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4.2.2 Electron Current Density Distribution

In addition to the electric field, J_E also affects the hot carriers generation. The location where the electric field is high to invoke the II generation process and J_E is also high to supply hot carriers as the source of the II will be the most likely hot carrier generation damage sites in the devices.

4.2.2.1 Effect of V_D on Electron Current Density Distribution

Fig 18 is J_E distribution with $V_D = 40$ for different V_G. We can see that J_E increases as V_G increasing which is consistent with the I_D vs. V_G trend in Fig 12. Peak 1 is due to the electron current crowding at the right edge of the source metal contact as it flows from the channel, rendering a much higher J_E as compared to J_E in the channel. This is called “current crowding effect” [35]. We need to note that the Peak 1 in Fig 18 is near the right edge of the source contact n+, which has a bit distance from the electric field Peak 1 in Fig 13 locating at the left edge of the poly-silicon gate. Therefore, there is not an II generation rate peak. On the other hand, another peak (Peak 2) in Fig 18 is near the PBO/NWD junction area, where is also a high electric field region, and thus peak II generation rate should appear here as can be seen in the later part of this work. Peak 3 in the drift region under poly-silicon gate area is due to the high potential difference between the poly-silicon gate and the drift region. This high potential difference induces high

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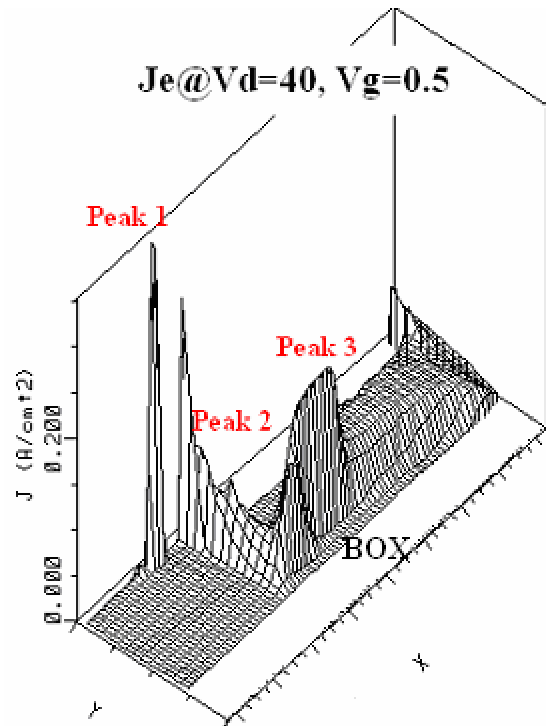
electric field in this area which pushes the electrons into the narrow center region of the drift region, renders high J_E.



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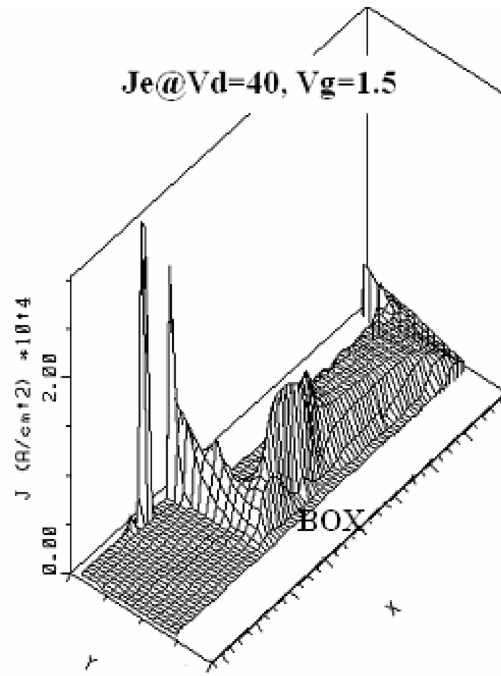

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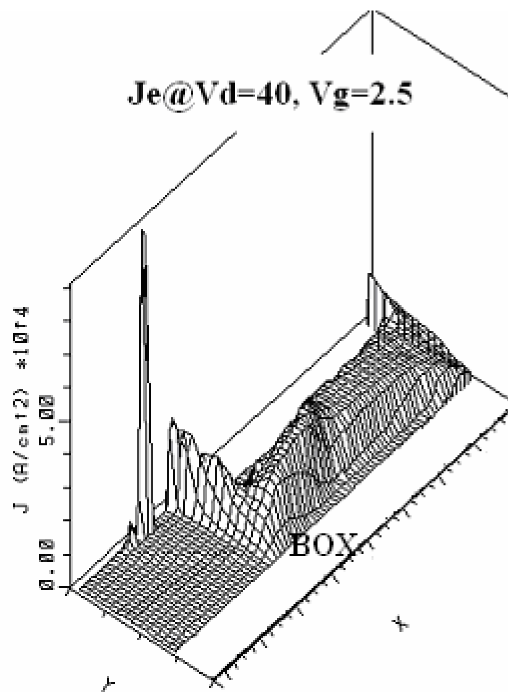

(c)

Figure 18. Electron Current Density Distribution in the Device @ V_D = 40 V, and (a) V_G = 0.5 V; (b) V_G = 1.5 V; (c) V_G = 2.5 V

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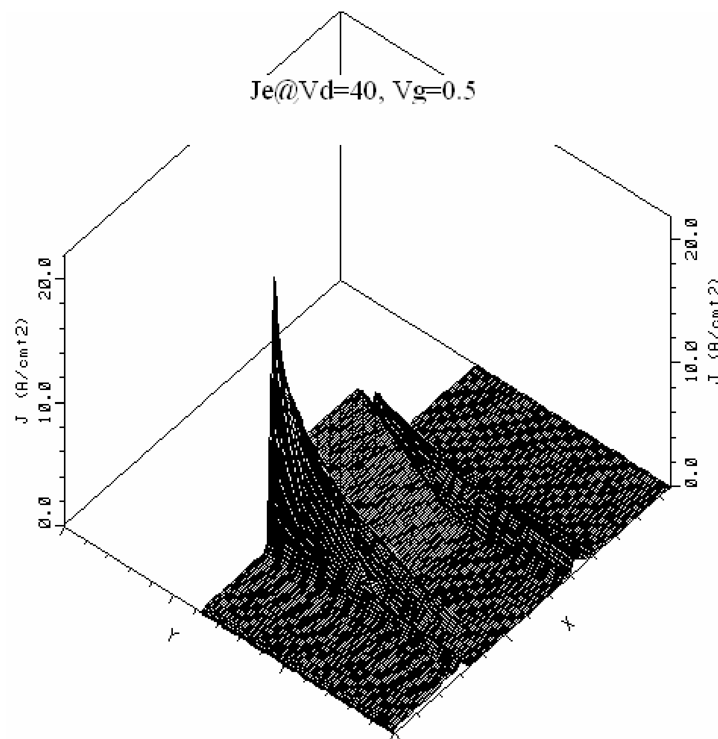
Due to the limitation of the number of lines the software can plot in a figure, Fig 18 cannot show the real J_E distribution near the gate oxide/channel interface, where has much high J_E. Fig 19 shows J_E distribution near the interface region in the channel region. In Fig 19 we can also see that J_E increases in the channel region with V_G as explained previous. The highest peak is always at the right edge of the source metal contact due to the current crowding effect regardless the value of V_G. J_E in Fig 19 is much higher than that in Fig 18 is because that in Fig 18 the plotting lines jump over this high J_E area which is very close to the interface due to the large space between the plotting lines.



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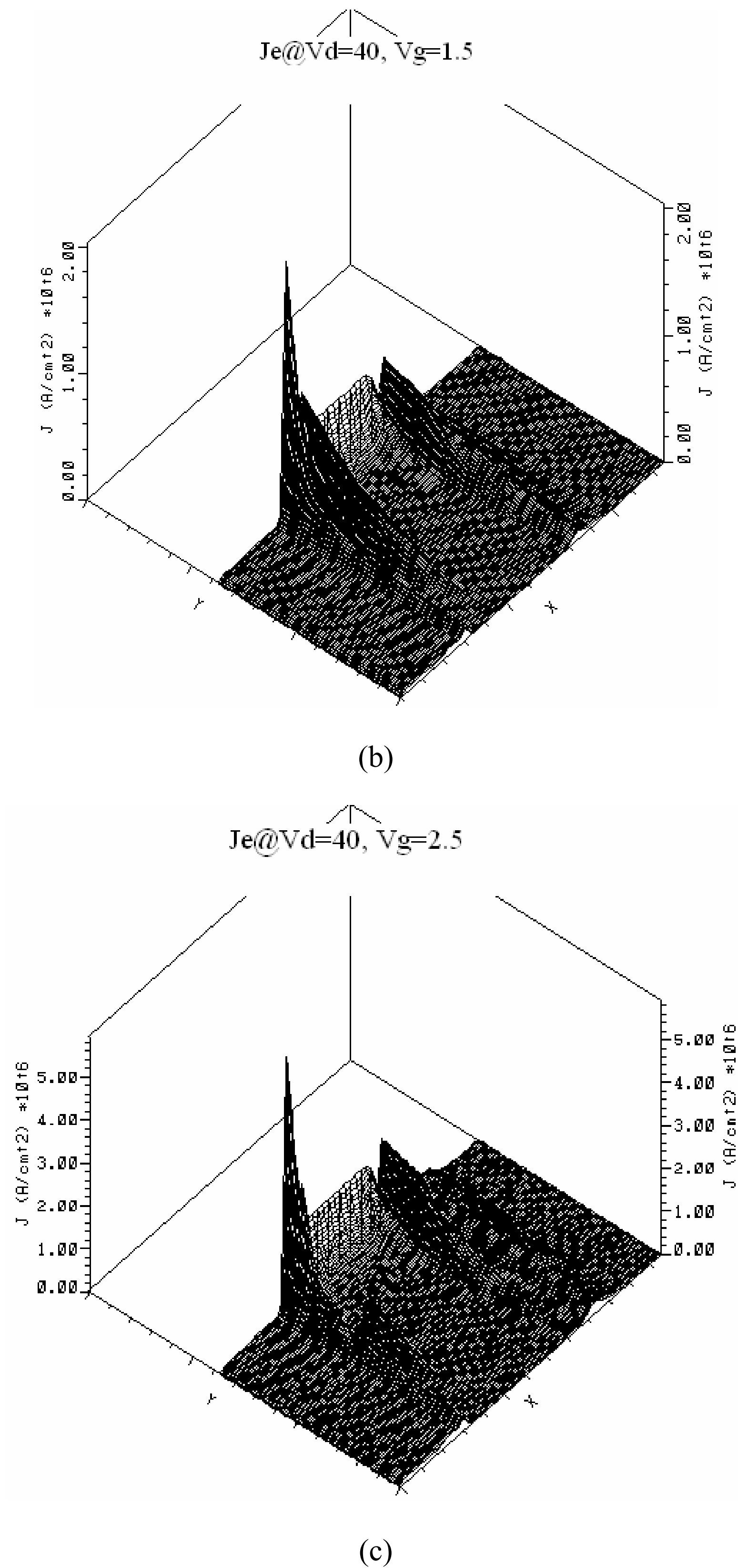

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Figure 19. Electron Current Density Distribution in the Channel Region

@ V_D = 40 V, and (a) V_G = 0.5 V; (b) V_G = 1.5 V; (c) V_G = 2.5 V

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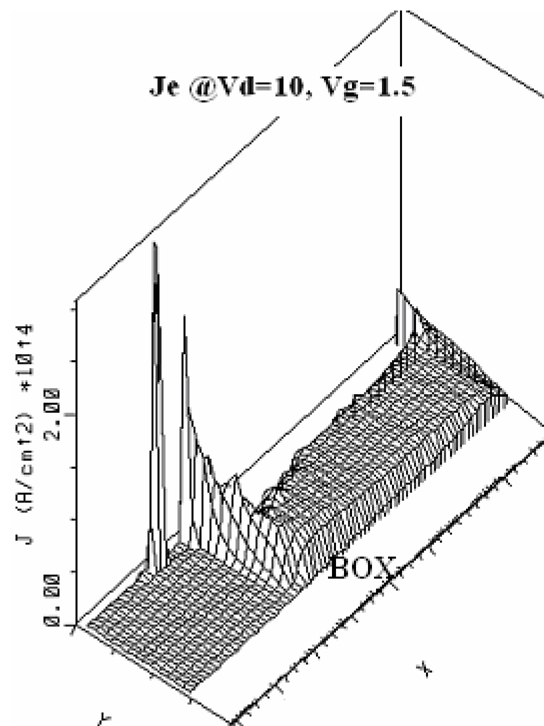
4.2.2.2 Effect of V_G on Electron Current Density Distribution

Fig 20 is J_E distribution at V_G=1.5 V with V_D = 10 V and 40 V respectively. The J_E Peak 1 ($3*10^4$ A/cm^2) and Peak 2 ($2*10^4$ A/cm^2) are almost the same at V_D = 10 V and 40 V. However, for Peak 3, due to the potential in the drift region under the poly-silicon gate area is higher at V_D = 40 V, the larger potential difference between the gate and the drift region induces a higher electric field that force the electrons to flow near the center portion of the drift region under the poly-silicon gate, thus higher J_E.



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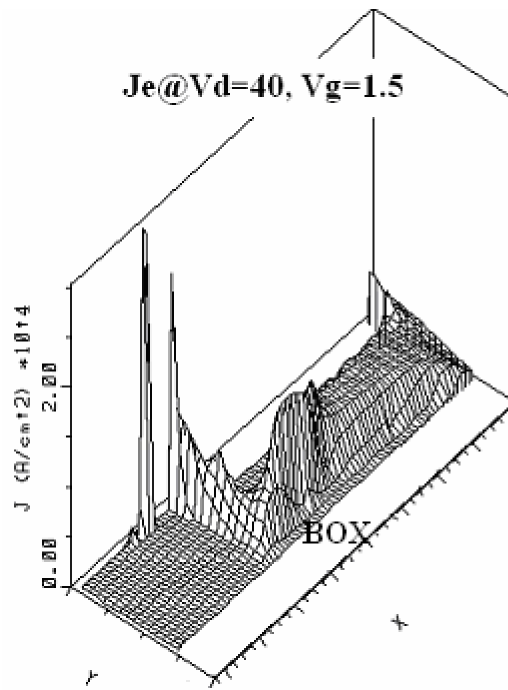

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Figure 20. Electron Current Density Distribution in the Device at V_G = 1.5 V, and (a) V_D =10 V; (b) V_D = 40 V

Due to the similar reason for J_E distributions at different V_G for V_D = 40 V, J_E distributions at different V_D for V_G = 1.5 V in the channel region should also be plotted separately as shown in Fig 21. J_E in the channel region near the right edge of source metal contact is still very high as shown before. Since I_D at V_G = 1.5 V with V_D = 10 and 40 V are quiet close, J_E in the channel for these different V_D are almost the same.

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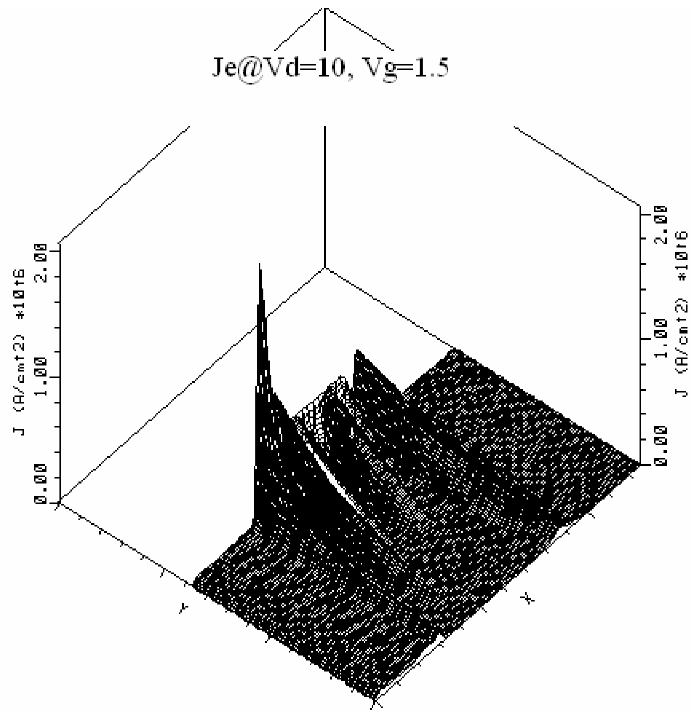

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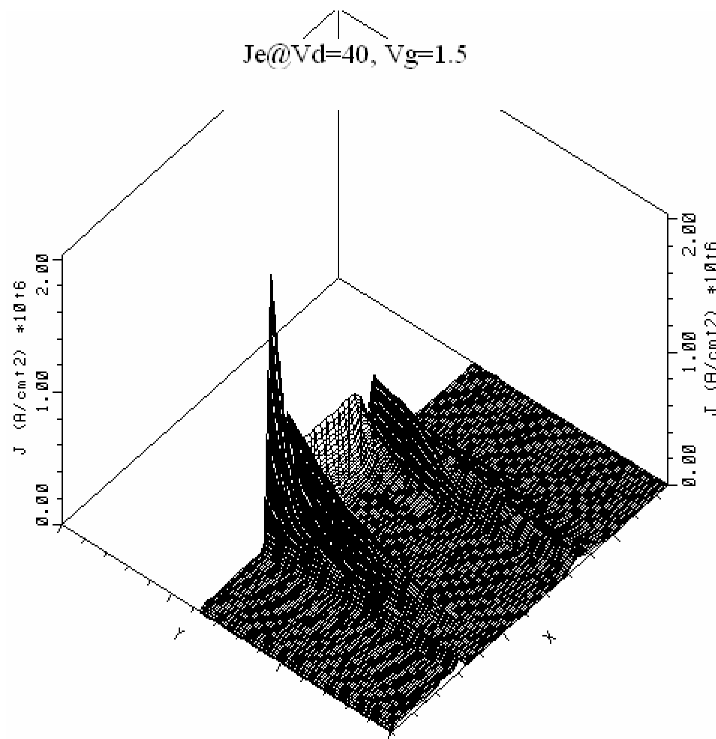

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Figure 21. Electron Current Density Distribution in the Channel Region

@ V_G = 1.5 V, and (a) V_D =10 V; (b) V_D = 40 V

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4.2.3 Impact Ionization Generation Rate Distribution

The most direct indicator for hot carrier injection is the II generation rate, because most of the hot carriers are generated through the II process. II generation rate also gives an intuitive way to explain I_{SUB}. Therefore, by looking at the spatial distribution and magnitude of the II generation rate in the device, we can deduce the likely hot carrier damage sites.

4.2.3.1 Effect of V_G on Impact Ionization Generation Rate Distribution

Fig 22 is the II generation rate distribution at $V_D = 40$ with different V_G. The II generation rate peak is located near the PBO/NWD junction (near STI left corner), where both the J_E and electric field are relatively large. Under the same bias condition of V_D = 40 V, the II generation rate peak initially is around $5x10^{19}$ pairs/(cm^3*s) at V_G = 0.5, and it increases with V_G to $2x10^{24}$ pairs/(cm^3*s) at V_G = 1.5 V, and thereafter reduces with V_G to $2.5x10^{23}$ pairs/(cm^3*s) at V_G = 2.5 V, i.e. maximum II generation rate occurs within the V_G range, which is consistent with the analysis of I_{SUB}. In the later Chapter 6, we will see that as V_G further increasing beyond 3 V, the II generation rate in the channel region may become comparable with this II generation rate peak near the STI left corner.

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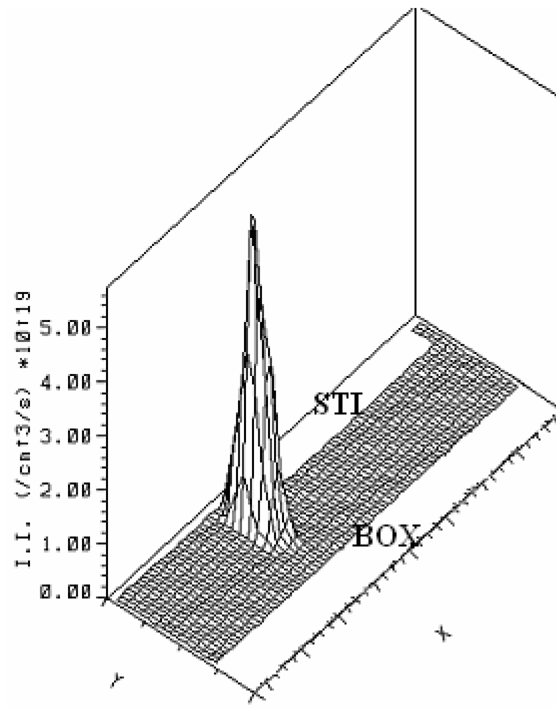

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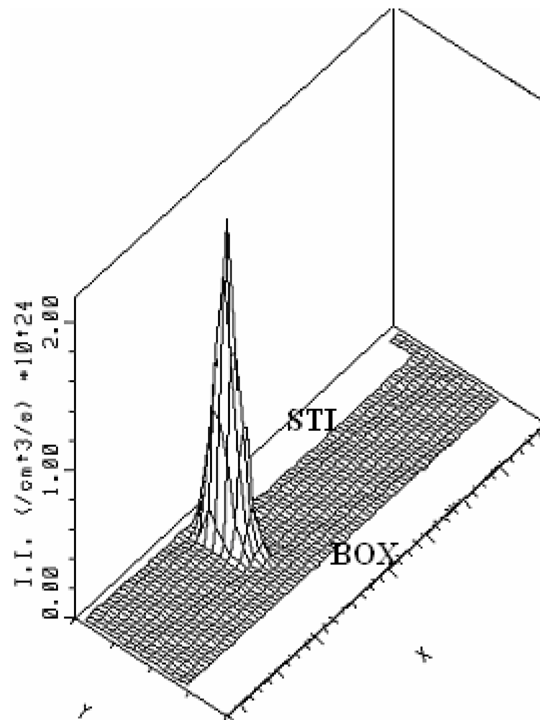

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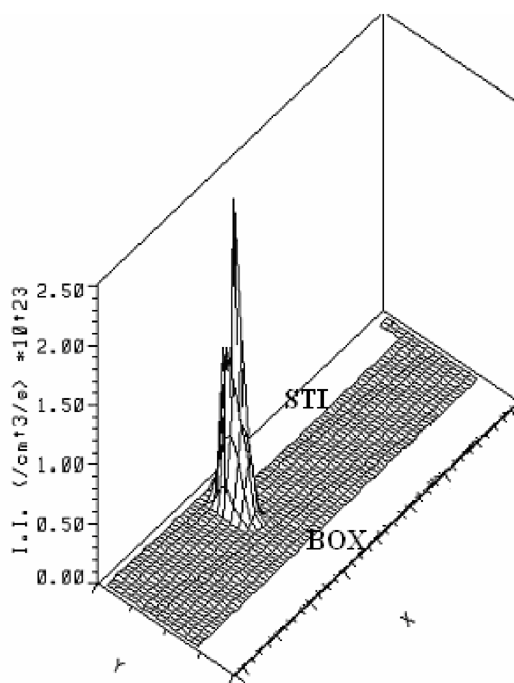

(c)

Figure 22. Impact Ionization Generation Rate Distribution in the Device

@ V_D = 40 V, and (a) V_G =0.5 V; (b) V_G = 1.5 V; (c) V_G = 2.5 V

4.2.3.2 Effect of V_D on Impact Ionization Generation Rate Distribution

Fig 23 is the II generation rate distribution at V_G = 1.5 V with V_D = 10 V and 40 V respectively. The peak is still located near the PBO/NWD junction. At the same gate bias condition of V_G = 1.5 V, where the II generation rate is maximum, the II generation rate peak increases from $1.4x10^{22}$ pairs/(cm3*s) at V_D = 10 V to $2x10^{24}$ pairs/(cm3*s) at V_D = 40 V. This can be explained as under the same V_G, the higher the V_D, the larger the voltage drop across PBO/NWD junction and the higher electric field causes higher II generation rate.

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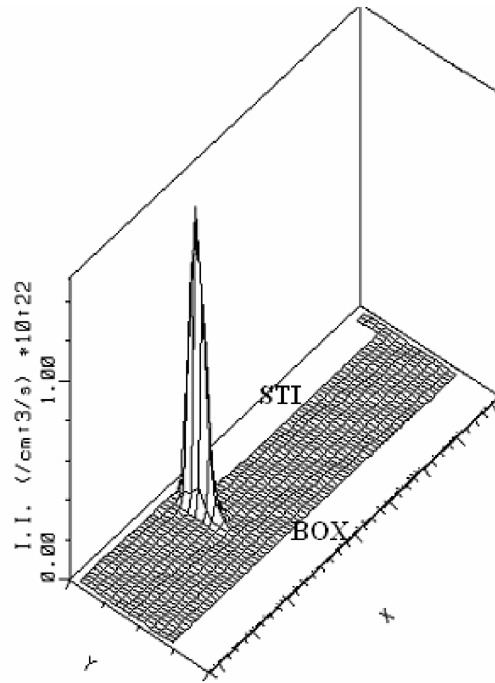

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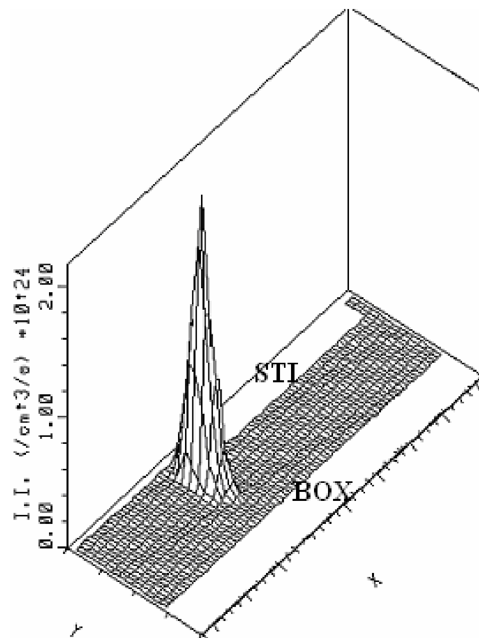

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Figure 23. Impact Ionization Generation Rate Distribution in the Device

@ V_G = 1.5 V, and (a) V_D =10 V; (b) V_D = 40 V

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Chapter 5. Effects of Different Doping Levels in the n-type Drift Region

Many simulation works showed that the electric field as well as J_E distributions could be altered by changing the doping profile in the drift region [1]. While complex doping profile can be used to optimize LDNMOS, its complexity could render its manufacturing unviable. In this chapter, we explored the simple variation of the implant dose in the extended lightly n-type doped epitaxial drift region (NWD) instead, and study the effect of this variation on the device performances under high V_D bias condition (up to 40 V) through both experiment and simulation results.

5.1 Drain Current Comparison

Fig 24 shows the experimental results of I_D for different NWD implant doses under the bias conditions of V_G = 3.3 V with V_D sweeping from 0 to 40 V. HNWD (solid line) denotes the high NWD implant dose device; and LNWD (dash line) denotes the low NWD implant dose device.

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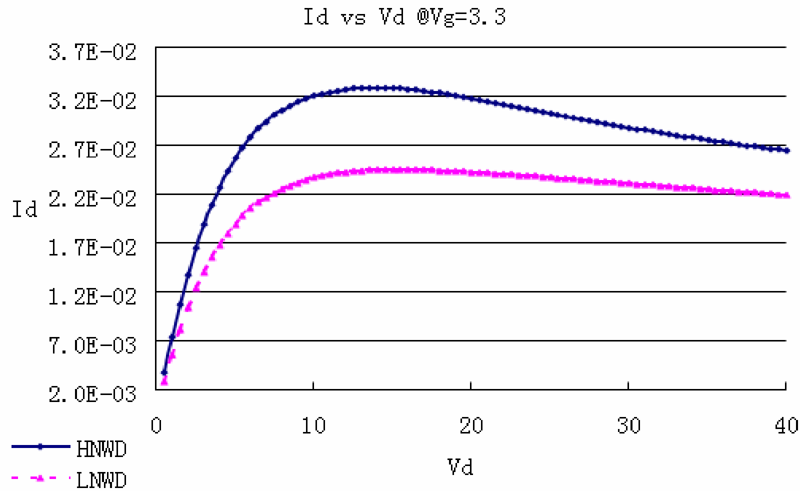

Figure 24. Measured I_D vs. V_D @V_G = 3.3 V

As we can see in Fig 24, HNWD has larger I_D as compared to that of LNWD under the same bias condition. This is because higher doping concentration in NWD region has lower series resistance, rendering higher I_D [36] as elaborated below.

A LDMOS has three major series resistance components, namely the metal resistance, the channel resistance and the drift region resistance. The metal resistance is generally very small as compared to the other two series resistances [37]. The channel resistance can be varied by the gate oxide thickness, channel length and width, doping level, and the applied gate voltage as in typical MOSFET. The drift region resistance is essentially only a function of device geometry and doping in the drift region [38]. With high gate voltage applied (e.g. V_G = 3.3 V), the channel resistance decreases significantly and R_{ON} becomes dominated by the drift region resistance [38]. Since the increase of the doping in NWD region will reduce the drift region resistance, it is expected that HNWD will have a higher I_D at high V_G as shown in Fig 24.

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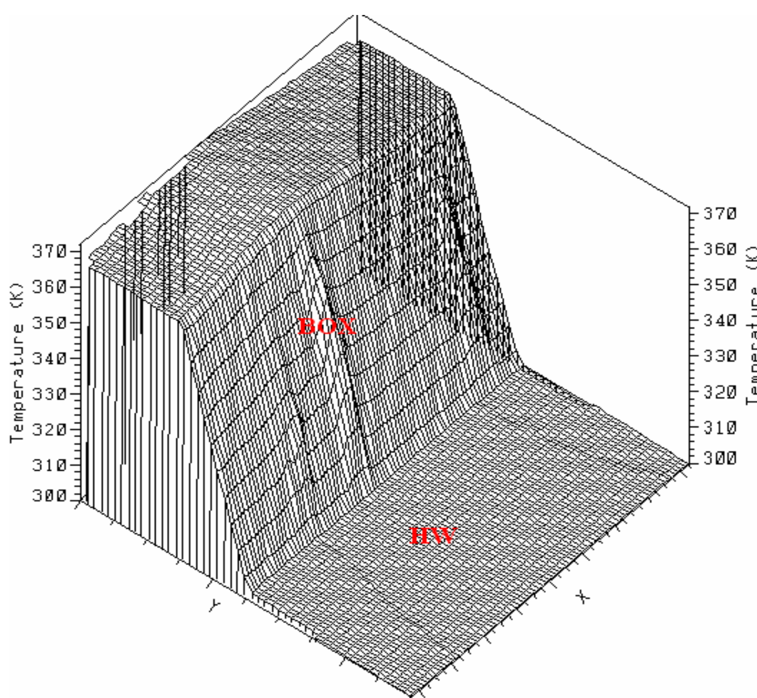
From Fig 24, we also find that the I_D of both HNWD and LNWD reduce as V_D going beyond 15 V. This is because of the self-heating effect in the SOI active layer at high V_D as explained before [33, 39].

Another phenomenon shown in Fig 24 is that the reduction of I_D for HNWD at high V_D is larger than that of LNWD. This implies that the carrier mobility reduction due to the thermal effect is more significant for HNWD. This is expected since the self-heating effect is larger for HNWD due to its higher I_D as explained previously [33, 39]. The lattice temperature distributions of these two devices under low and high V_D are shown in Fig 25. For LNWD, its lattice temperature in the active SOI layer is around 370 K at V_G = 3.3 V and V_D = 10 V, and it increases to about 540 K when V_D is increased to 40 V. On the other hand, for HNWD, the lattice temperature in active SOI layer increases from 390 K at V_G = 3.3 V and V_D = 10 V to 580 K V_G = 3.3 V and V_D = 40 V.



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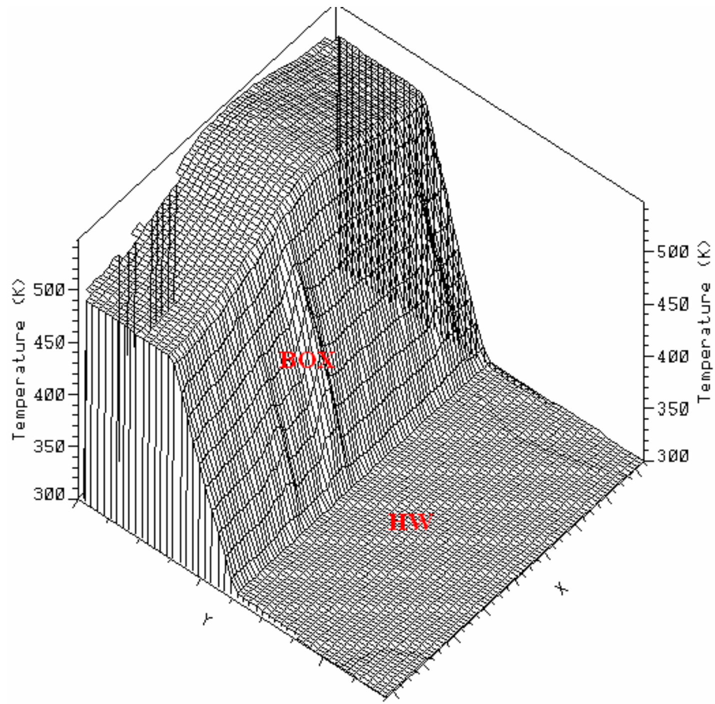

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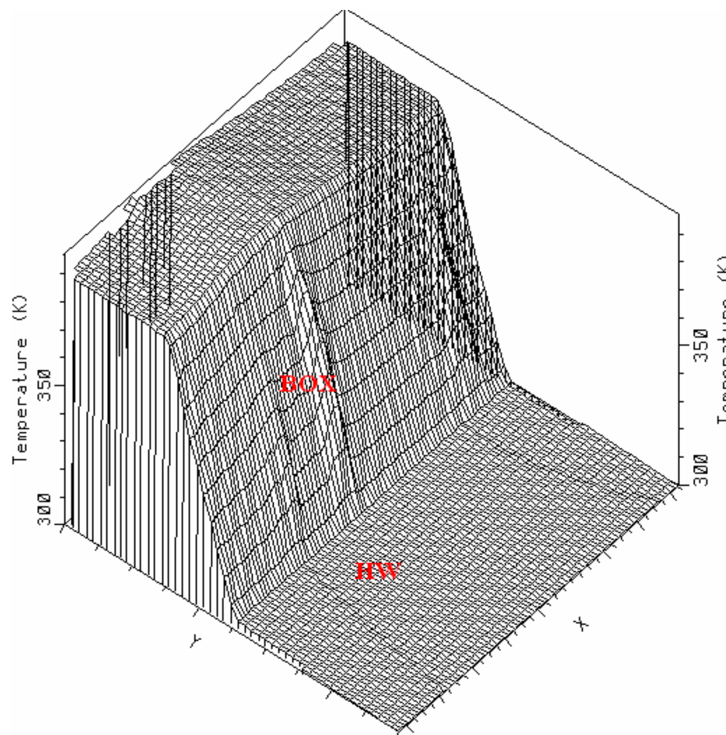

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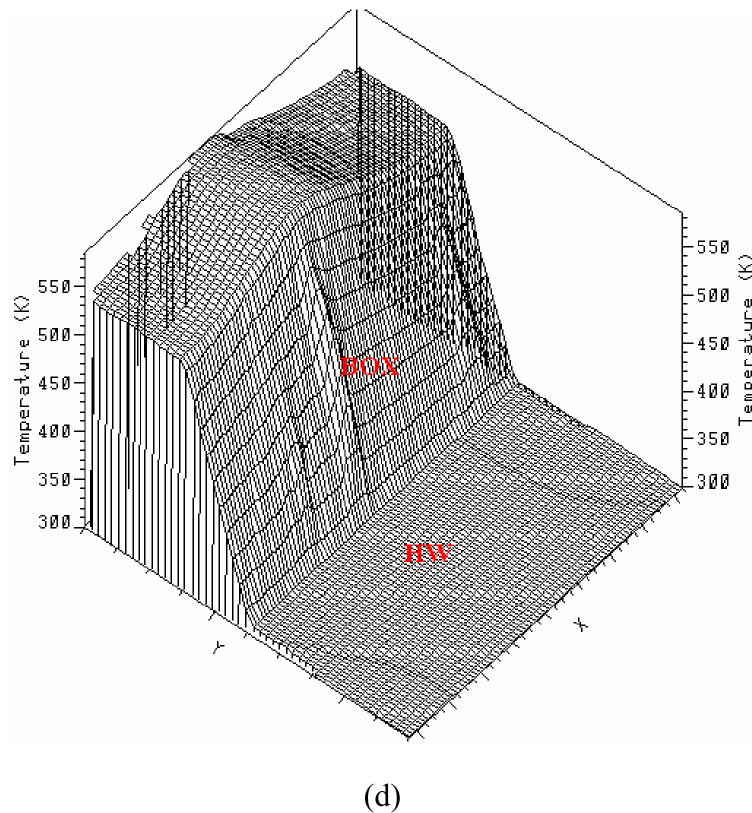

(d)

Figure 25. Lattice Temperature Distributions of L/HNWD under Different V_D

(a) LNWD @V_G = 3.3 V & V_D = 10 V; (b) LNWD @V_G = 3.3 V & V_D = 40 V;

(c) HNWD @V_G = 3.3 V & V_D = 10 V; (d) HNWD @V_G = 3.3 V & V_D = 40 V

Fig 26 shows the experimental results of I_D under bias conditions of V_D = 40 V with V_G sweeping from 0 to 3.3 V. As mentioned before, the LDMOS consists of three major series resistances. At a given high V_D, the variation of the channel resistance is controlled by V_{GS} in the saturation region as [17]:

$$R_{Ch} = \frac{L_{Ch}}{W\mu_{eff} C_{OX} [(V_{GS} - V_{th}) - V_{DS} / 2]} \quad (6)$$

where L_{Ch} is the channel length, W is the width of the device, μ_{eff} is the electron effective mobility and C_{OX} is the gate oxide capacitance which is determined by the thickness of the gate oxide.

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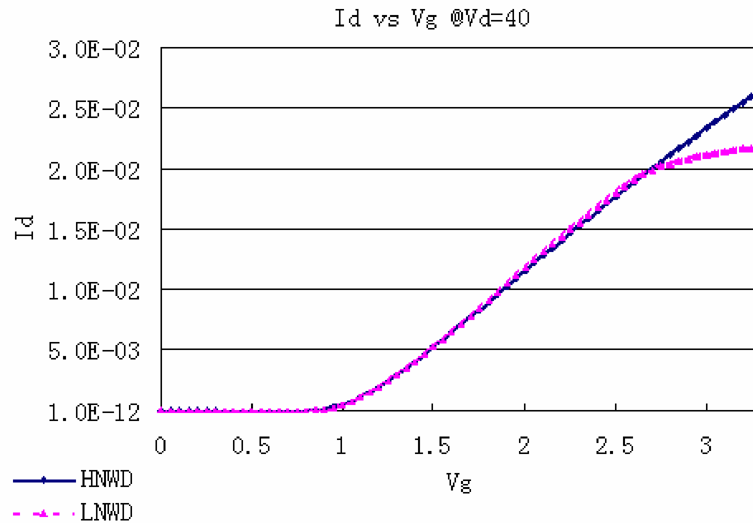

Figure 26. Measured I_D vs. V_G @V_D = 40 V

For a given V_D, the channel resistance as a function of V_{GS} reduces with V_{GS} increasing which can be seen from Eqn (6). At low V_G, R_{Ch} is larger than the drift region resistance, and thus it dominates the total series resistance of the LDNMOS. Since the doping concentration in the channel region and the bias condition are almost the same for both devices, R_{Ch} is similar for both HNWD and LNWD. Therefore, at high V_D = 40 V and in the low V_G region, the I_D for both devices are almost equal.

As V_{GS} increases further, R_{Ch} decreases as can be seen in Eqn (6) and finally becomes smaller than the drift region resistance at around V_{GS} = 2.5 V. The drift region resistance then begins to dominate the total series resistance. As HNWD has smaller drift region resistance as explained previously, it has higher I_D at high V_G region as observed in Figure 26 with a deviation in I_D at around V_G = 2.5 V.

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5.2 Substrate Current Comparison

Fig 27 is the experimental results of I_{SUB} at V_D = 40 V with sweeping V_G. As mentioned before, this I_{SUB} is determined by both the number of carriers and the electric field in active SOI layer [29].

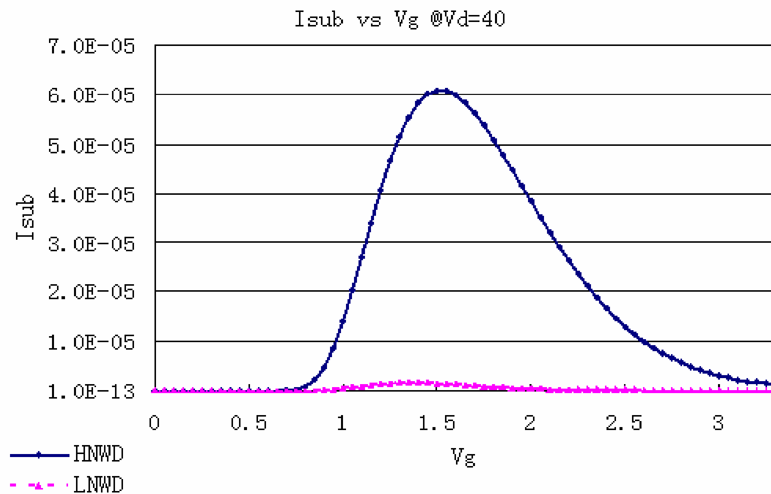

Figure 27. I_{SUB} vs. V_G @ V_D = 40 V

The shape of I_{SUB} curves in Fig 27 for both devices are similar, and this is a typical I_{SUB} vs. V_G curve under high V_D for MOSFET. As I_{SUB} is proportional to both the electric field and J_E in the active SOI layer, the increase in V_G will reduce the electric field in the drain side of the device and increase J_E. A trade-off between increasing J_E and decreasing electric field at increasing V_G will occur that causes I_{SUB} to be peaked somewhere in the middle of the V_G sweeping range [32, 34].

In Fig 27, we can also see that I_{SUB} for HNWD is much larger than its low doping counterpart, especially for the peak value. This may be due to the following two reasons. Firstly, the junction depletion region is narrower for HNWD; hence the

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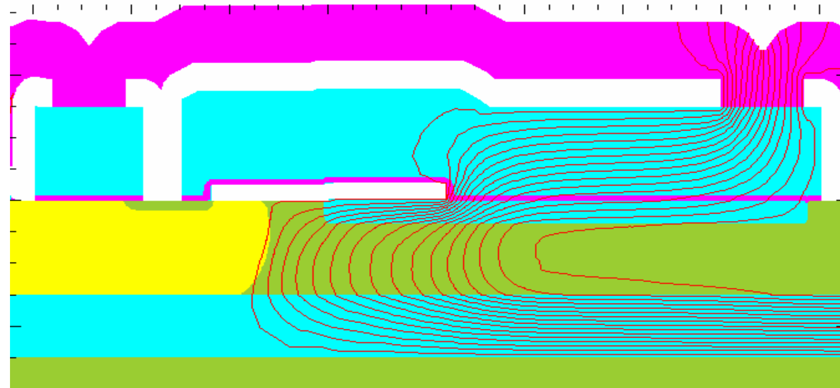
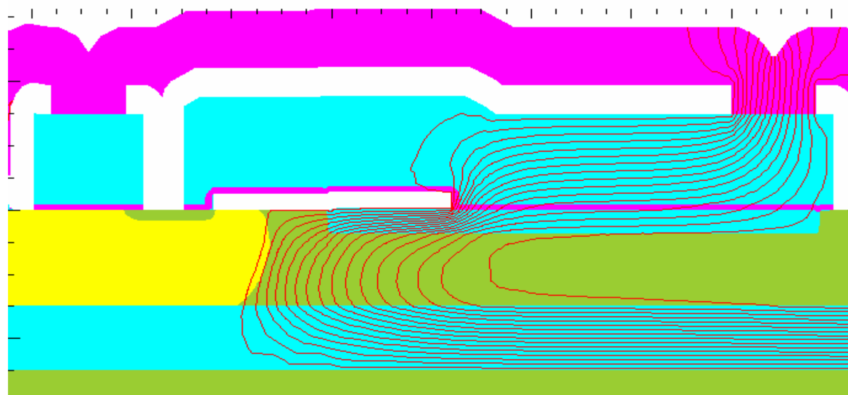
maximum electric field within the narrower depletion region is higher for HNWD at a given V_D. Secondly, as I_D is higher for HNWD at high V_G region which was showed in Fig 24 and Fig 26, J_E is also higher for HNWD, which leads higher I_{SUB}. Fig 28 shows the potential contour of HNWD and LNWD at V_D = 40 V and V_G = 1.5 V which is the peak location of I_{SUB}. The difference between successive contour line is 2.5V. We can see in Fig 28 that HNWD has denser potential contour lines near the PBO/NWD junction, indicating a larger voltage drop there. As a result, a larger electric field for HNWD leads to the higher I_{SUB}.



(a)



(b)

Figure 28. Potential Contour @ V_D = 40 V & V_G = 1.5 V

(a) LNWD; (b) HNWD

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At the high V_D, the drift region depletes from the channel side. Depletion means that there is a net charge present, which is also called the background charge. This background charge will induce build-up electric field in the depletion region according to Poisson's equation [17]:

$$\frac{\partial^2 V}{\partial x^2} = -\frac{\partial E}{\partial x} = \frac{-Q(x)}{\varepsilon} = \frac{qN(x)}{\varepsilon} \quad (3)$$

Where E is the build-up electric field, Q is the charge in the depletion region, q is the electron charge, N(x) is the doping concentration which varies with x position, and ε is the dielectric constant of the semiconductor.

Larger N(x) means higher dE/dx and d^2V/dx^2 values according to Poisson's equation. Therefore, this denser potential contour in HNWD is due to the higher background charge in NWD region. For the same voltage drop over the drift region (40 V), the higher dE/dx leads to a higher electric field peak.

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Chapter 6. Hot Carrier Induced (HCI) Degradation Test

In this chapter, HCI degradation test is performed on the power SOI LDNMOS with different doping concentrations in the NWD region under the maximum I_{SUB} condition at different V_D stresses. ONWD denotes the original NWD doping device, and LNWD denotes the low NWD doping device. The implant dose of ONWD is approximately 30% higher than that of LNWD. The degradation parameters including I_D, $G_{M,MAX}$, V_{TH} and the peak value of the substrate current ($I_{SUB\text{-}P,SAT}$) are investigated according to JEDEC standard. Due to the lack of p-type buried/bulk layer and the effects of STI structure, the II peak location and its movement may not exhibit the same behavior as in normal LDNMOS. Some anomalies are observed experimentally due to the distinctive hot carrier injection mechanisms in the SOI LDMOS with STI. $I_{SUB\text{-}P,SAT}$ is chosen for the degradation data analysis because of its better linear degradation behavior.

6.1 Parameters Definition

During the HCI degradation test, some measured parameters are defined according to JEDEC standard as follow [40].

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6.1.1 Maximum Transconductance ($G_{M,MAX}$)

The maximum slope of the I_D-V_G curve in linear and/or saturation regions, are called linear and/or saturation maximum transconductance ($G_{M,MAX}$) respectively. The transconductance (G_M) is a measure of the rate of change of the output current to a change in the input voltage as described in equation [4].

$$G_M = \frac{\partial \log I_D}{\partial V_G} A/V \tag{4}$$

6.1.2 Threshold Voltage (V_{TH})

Threshold voltage is the applied V_G to achieve the onset of strong inversion at the surface of the semiconductor interface. Strong inversion happens when the total band bending at the surface is equal to double the potential in bulk semiconductor, i.e. difference between the intrinsic Fermi level and the Fermi level in the substrate ($\Phi_S = 2\Phi_F$). For a NMOS, at this band bending, the electron concentration at the insulator semiconductor interface becomes equal to the hole concentration in the bulk. This situation is called inversion or as strong inversion, and the layer of free electrons induced at the surface is called an inversion layer. At this point, any further increase in V_G would not increase the depletion layer any more. The $G_{M,MAX}$ extraction method is used here to determine V_{TH} [33].

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6.1.3 Drain Current (I_D)

The linear drain current ($I_{D,LIN}$) is defined as the dc drain current measured at V_D = 0.1 V and V_G = 3.3 V, while the saturation drain current ($I_{D,SAT}$) is defined as the dc drain current measured at V_D = 20 V and V_G = 3.3 V in our experiment.

6.1.4 Substrate Current (I_{SUB})

I_{SUB} is composed of the holes generated by II and collected at the substrate contact as mentioned previously. In this work, a new parameter "the peak value of I_{SUB} ($I_{SUB\text{-}P,SAT}$)" in I_{SUB} vs. V_G characteristic curve in saturation region is defined to do the degradation analysis and comparison because of its better linear degradation behavior which will be shown later.

6.1.5 Degradation Index

The HCI degradation index is defined as the change values of the corresponding parameter. It is calculated as [Y(t)-Y(0)]/Y(0), where Y(0) is the initial parameter value before the stress testing; and Y(t) is the parameter value after t seconds stress testing [40]. Since the typical HCI degradation follows a power-law with stress time t given as $\Delta Y = \dfrac{Y(t) - Y(0)}{Y(0)} = C \cdot t^n$ [41], $Log(|\Delta Y|)$ vs. t is plotted in log-log with X axis as the stress time (second) in log scale; and Y axis is the logarithmic value of the absolute value of the degradation index.

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6.2 Experiment Design

Constant DC stress HCI degradation experiments are performed using Keithley 4200-SCS Semiconductor Characterization System at room temperature. The stress conditions are V_D = 20 V and 40 V, with V_G around 1.5 V in order to have the maximum I_{SUB} condition. Parametric measurement is performed after the devices are stressed for a pre-specific time interval. During the parametric measurements, V_G is sweeping from 0 to 3.3 V with a step size of 0.05 V at both linear (V_D = 0.1 V) and saturation (V_D = 20 V) regions to monitor the degradations of $G_{M,MAX}$, V_{TH}, I_D as well as I_{SUB}. The cumulative stress times used are: 100, 250, 500, 1000, 2500, 5000, 7000, 10000, 15000, 20000, 25000 and 30000 seconds. At low V_D = 20 V stress conditions, devices were stressed up to 50000 seconds. Under each stress condition, five units are used for the degradation measurements to ensure experimental accuracy. Statistical hypothesis testing is performed on the measurement data of the five units with 90% confidence level so that only the statistically significant variations are considered when comparisons of the degradation and degradation rate (i.e. the slope of the degradation vs. time) are performed. The HCI test procedure is shown in Figure 29.

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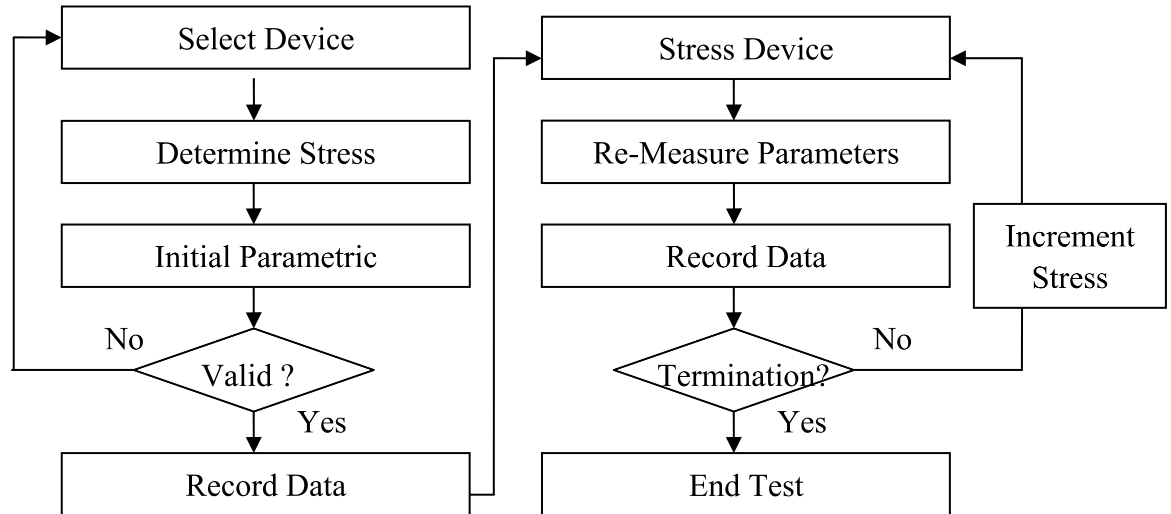

Figure 29. Hot Carrier Stress Test Procedure

6.3 Results Discussion

6.3.1 Abnormal behavior of $G_{M, MAX}$ and V_{TH} Degradations

The degradations of $G_{M, MAX}$ and V_{TH} under stress condition of V_D = 20 V and V_G = 1.5 V are measured in both the linear and saturation operating regions for ONWD. The degradation of $V_{TH, LIN}$ is shown in Fig 30 where the x-axis is the stress time in second; and y-axis is the degradation index of $V_{TH, LIN}$. The degradation index of the corresponding parameter is calculated as [Y(t)-Y(0)]/Y(0) as mentioned before. Degradation measurements are performed on five individual devices subjected to the same stress condition.

As can be seen in Fig 30, the degradation of $V_{TH, LIN}$ does not behave linearly as expected according to the earlier works [15, 42]. No functional relationship seems

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to exist between the degradation index and the stress time. Similar degradation behaviors are also obtained for $V_{TH,SAT}$ and $G_{M,\ MAX}$ in both the linear and saturation regions.

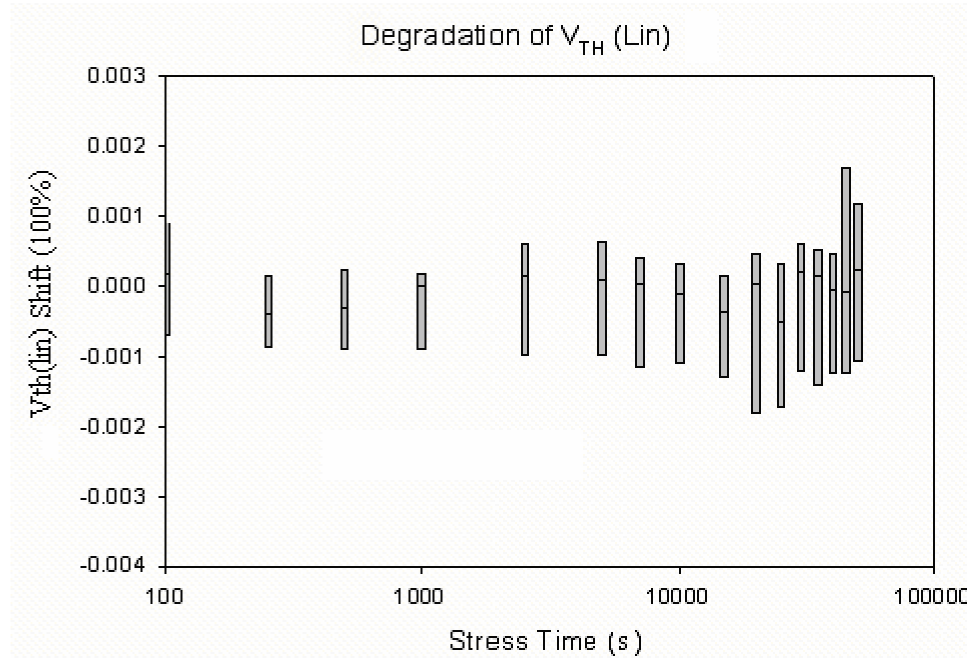

Figure 30. $V_{TH,\ LIN}$ Degradation under stress V_D = 20 V & V_G = 1.5 V

The abnormal behavior of $G_{M,\ MAX}$ and V_{TH} observed is because the main II location is not in the channel region for our devices under maximum I_{SUB} condition as can be seen in Fig 31. In normal NMOSFET, the interface charges in the gate oxide of the channel region generated by II will cause the flat-band voltage to shift, and induce linear degradation of $G_{M,\ MAX}$ and V_{TH} [43]. Fig 31 shows the contour plot of II generation rate computed using MEDICI simulations under the stress of V_D = 20 V, V_G = 1.5 V. The II peak locates at the STI bottom left corner, which is at the level of 3.16×10^{24} pairs/(cm^3*s). As the II peak is not in the channel, the interface damage in the gate oxide is not severe. This is also verified by the I_G

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measurement which shows a small noisy signal with V_G sweeping as shown in Figure 32.

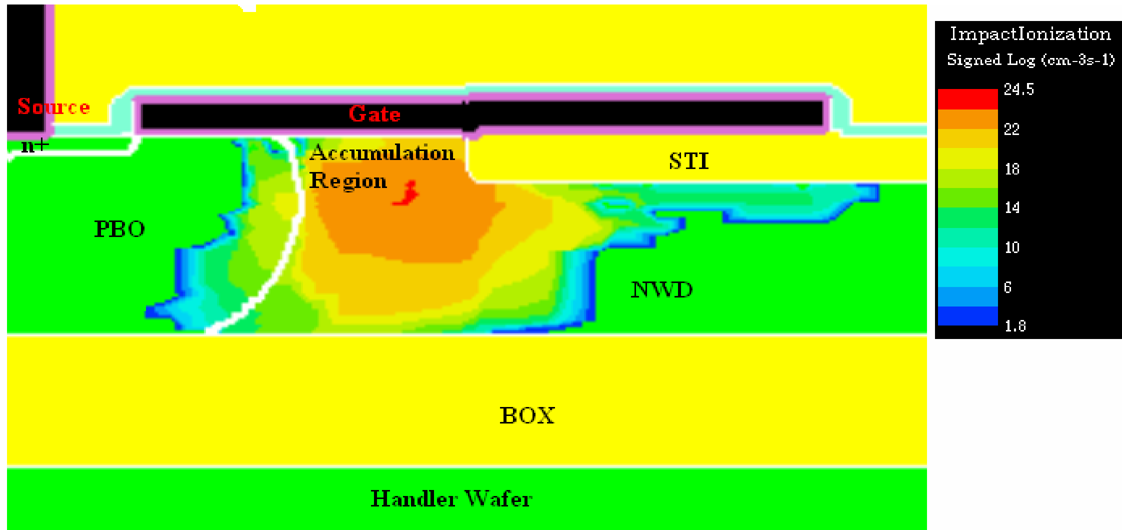
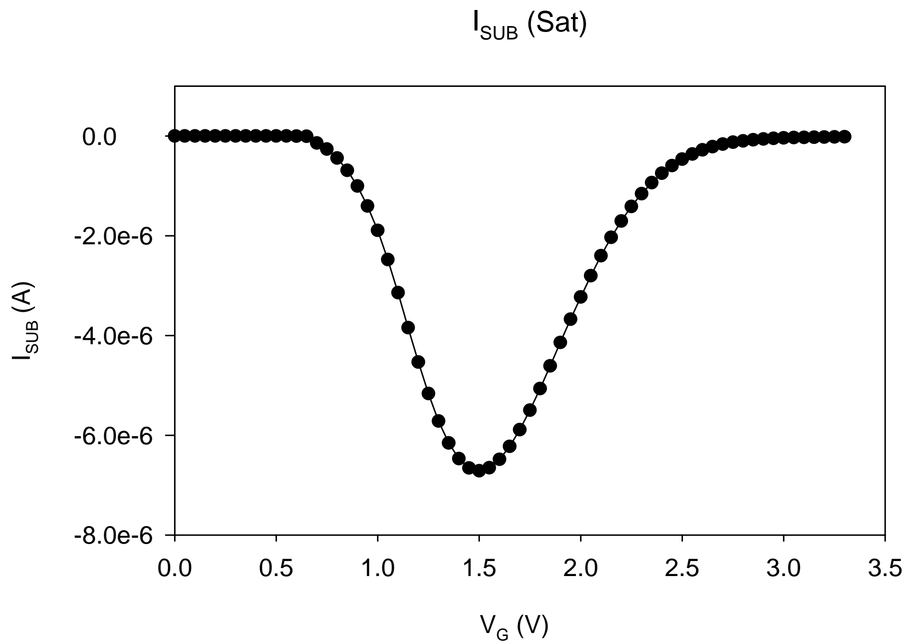


Figure 31. Impact Ionization Generation Rate Contour Plot at V_D=20V & V_D=1.5V



(a)

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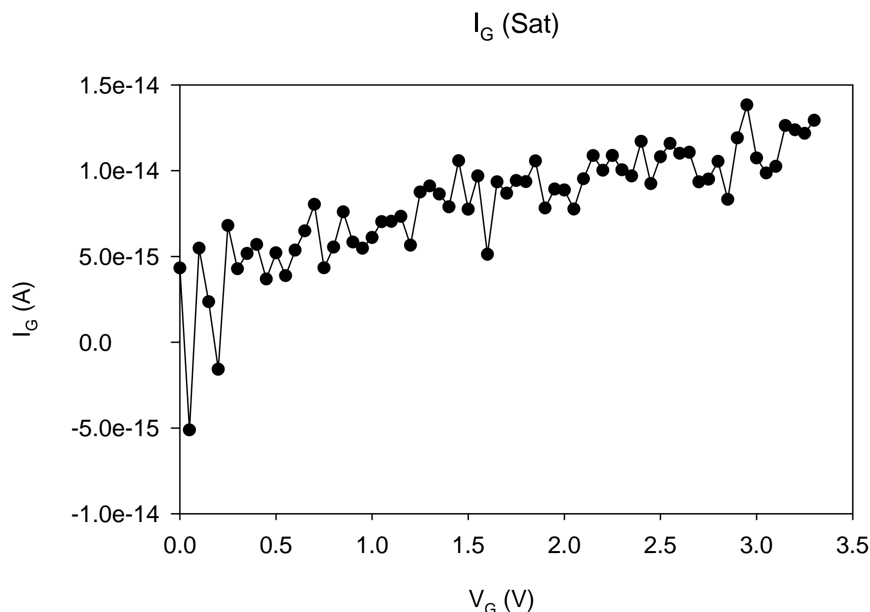

(b)

Figure 32. I_{SUB} and I_G Measurements at Saturation Region (V_D=20 V, V_G=0~3.3 V) (a) I_{SUB} vs. V_G; (b) I_G vs. V_G

Fig 32 is the I_{SUB} and I_G measurements in the saturation region (V_D = 20 V) of ONWD with V_G sweeping from 0 to 3.3 V. Most of the generated electrons do not reach to the gate as in the standard MOSFET but instead they go to the high biased drain side. In Fig. 32, I_{SUB} is at the level of μA in the saturation region measurement. If all the electrons generated by II go to the gate contact forming I_G, the level of I_G should be the same as I_{SUB}'s. However, as seen in Fig 32, I_G is at the level of 1×10^{-14} A, which is much smaller than I_{SUB}. The negligible damage in the gate oxide of the channel region under maximum I_{SUB} stress condition due to the hot carrier injection for LDMOS was also observed in [44].

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6.3.2 $I_{SUB\text{-}P,SAT}$ Degradation

$I_{SUB\text{-}P,SAT}$ is the peak value of I_{SUB} in the I_{SUB} vs. V_G characteristic curve with devices biased in the saturation region with V_D = 20 V. Fig 33 is the $I_{SUB\text{-}P,SAT}$ degradation at stress condition of V_D = 20 V and V_G = 1.5 V for ONWD. X axis is the stress time (in second) in log scale; and Y axis is $Log(\left|\frac{I_{SUB\text{-}P,SAT}(t) - I_{SUB\text{-}P,SAT}(0)}{I_{SUB\text{-}P,SAT}(0)}\right|)$. The absolute value is used here since $I_{SUB\text{-}P,SAT}$ is reducing with stress time in our experiment. Similar definitions are applied for the following degradation figures in this work.

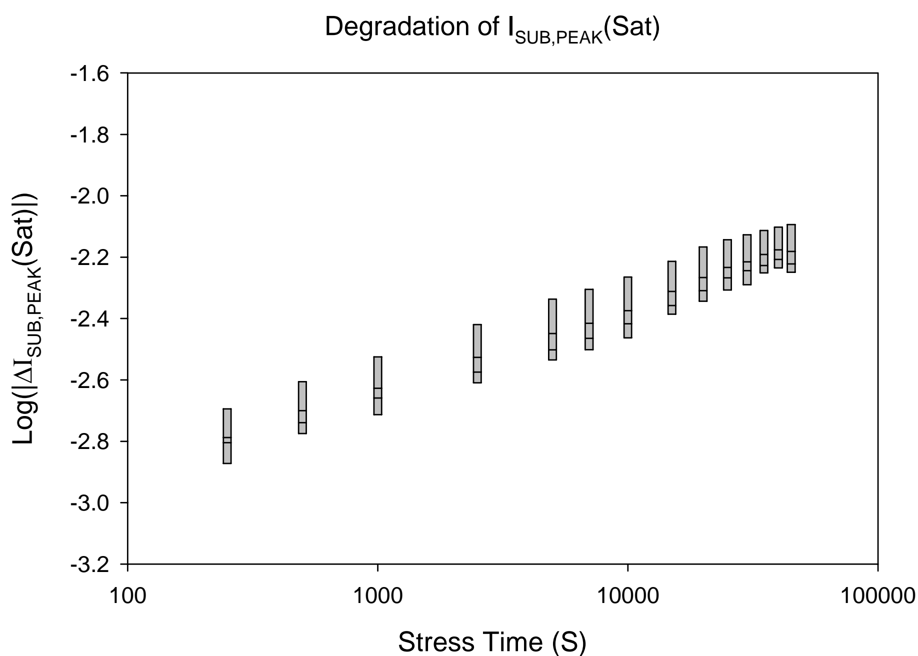

Figure 33. $I_{SUB\text{-}P,SAT}$ Degradation at Stress V_D = 20 V & V_G = 1.5 V

In Fig 33, the degradation of $I_{SUB\text{-}P,SAT}$ follows the power-law with stress time as expected. As $I_{SUB\text{-}P,SAT}$ is due to the holes generated by II process, and the peak of

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II is found to be near the bottom-left corner of STI as shown in Figure 31, the left corner of STI should be the main hot carrier injection site. To investigate the degradation behavior of $I_{SUB-P,SAT}$, simulation of I_{SUB} with positive and negative interface charges in the STI left corner (X = 0 ~ 0.5 μm) is performed, and the results are shown in Fig 34.

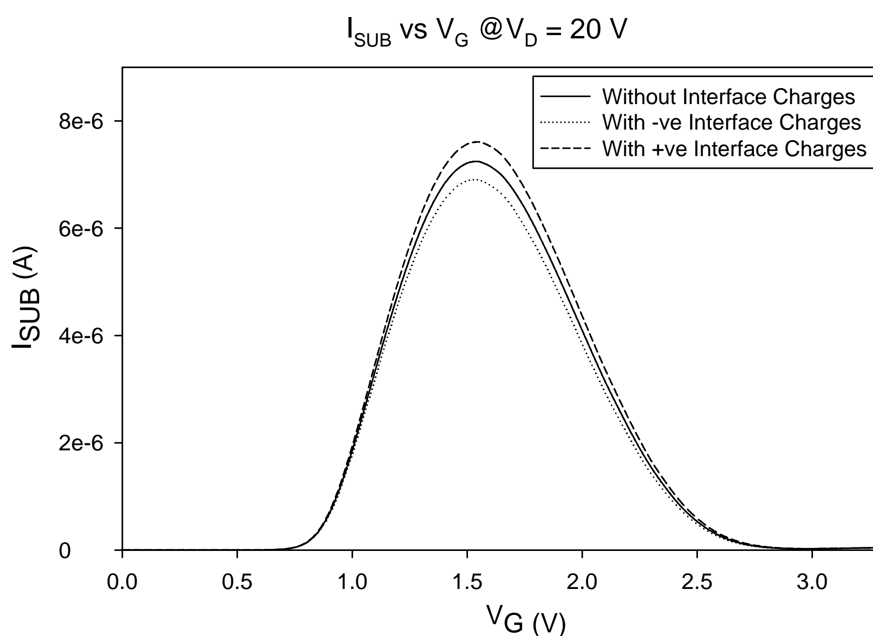

Figure 34. Effect of Different Interface Charges on I_{SUB} @ V_D = 20 V

As can be seen in Fig 34, negative interface charges in the STI left corner will reduce I_{SUB}, while positive interface charges will increase I_{SUB}. This is because negative charges built-up in the STI bottom-left corner induce positive mirror charges, resulting in a reduction in the effective electron concentration, and thus a reduction in the electric field at this II peak location. As a result, the II generated $I_{SUB-P,SAT}$ will decrease [44]. Similar explanation is applied for the positive

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interface charges which increase the electric field, thereby increase $I_{SUB-P,SAT}$. Since our experimental observations show a reduction of I_{SUB}, negative interface charges are deduced in the STI left corner.

6.3.3 $I_{D,LIN}$ & $I_{D,SAT}$ Degradations

Fig 35 and 36 show the degradations of $I_{D,LIN}$ and $I_{D,SAT}$ for ONWD under the stress condition of V_D = 20 V and V_G = 1.5 V respectively.

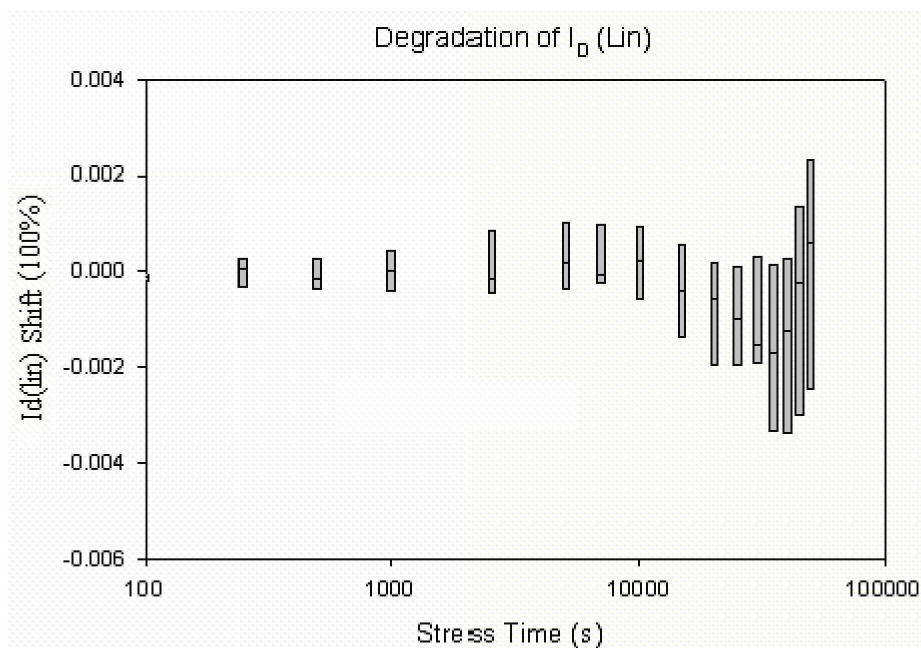

Figure 35. $I_{D,LIN}$ Degradation under stress V_D = 20 V & V_G = 1.5 V

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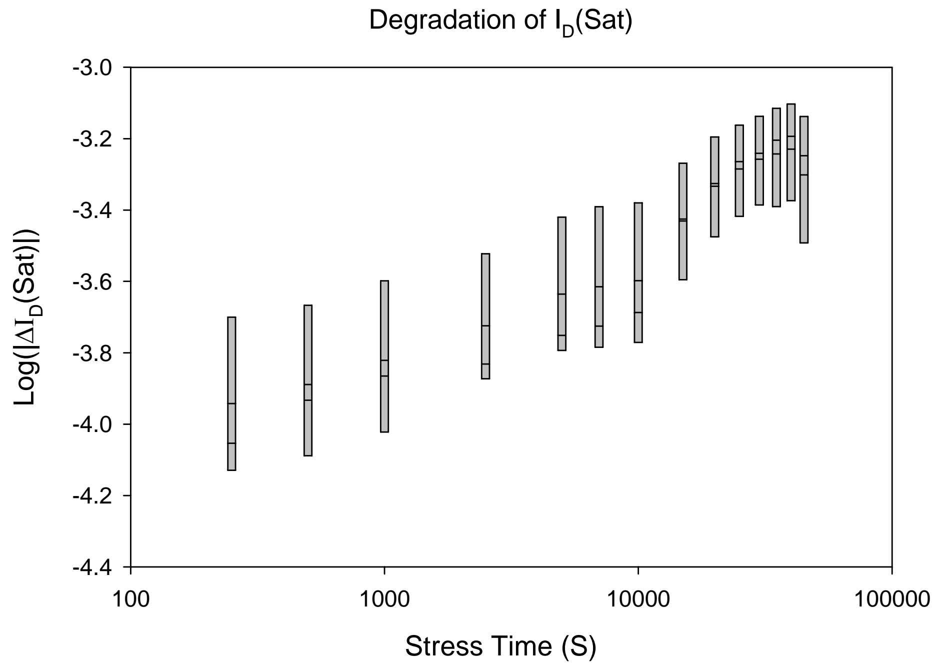

Figure 36. $I_{D,SAT}$ Degradation under stress V_D = 20 V & V_G = 1.5 V

From the previous $I_{SUB\text{-}P,SAT}$ degradation analysis, we know that there are negative interface charges in the STI left corner, which will reduce the effective electron concentration in the drift region near the STI corner. Thus the drift region resistance should increase, resulting in a reduction in I_D. However, as seen in Fig 35, $I_{D,LIN}$ does not decrease with stress time. Furthermore, the degradation index of $I_{D,SAT}$ is negative in our measurement, which means that $I_{D,SAT}$ decreases with stress time, but the degradation is not as linear as that of $I_{SUB\text{-}P,.SAT}$ as can be seen from Figures 33 and 36. From the above-mentioned abnormal degradations of $I_{D,LIN}$ and $I_{D,SAT}$, another damaged site besides the STI left corner is suspected.

As seen in Fig 31, near the II peak, another suspected hot carrier injection site should be the gate oxide at the surface of the accumulation layer. This location is a little far from the II peak near the STI left corner, and hence it has less impact on

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I_{SUB}. However, since I_D flows near the interface of the gate oxide/accumulation layer, it will be affected by these interface charges. If the interface charges in this gate oxide interface within the accumulation region are also negative, it will reduce I_D as the same reason of the negative interface charges in the STI corner, which is again not consistent with our experimental observations. Therefore, we suggested that there are positive interface charges at the interface.

The two different types of interface charges mentioned above can be explained as follows. Fig 37 shows the vertical and horizontal electric field components 0.02 μm below the interface under the stress condition of V_D = 20 V and V_G = 1.5 V. Positive E_Y indicates that the direction of E_Y is pointing downward and is favorable for electron injection into the gate oxide. On the contrary, negative E_Y is pointing upward and favorable for hole injection into the gate oxide. Positive E_X indicates that the direction of E_X is pointing right; negative E_X is pointing left. In the channel region, as the gate is stressed at 1.5 V, the vertical electric field is positive $4*10^5$ V/cm as shown in Fig 37 (a), which means that it is favorable for electron injection into the gate oxide/channel interface. However, since the II along the gate oxide interface in the channel is not significant at V_G = 1.5 V as discussed previously, the interface damage at the interface is negligible. On the other hand, in the accumulation region, the vertical electric field changes to negative $-2*10^5$ V/cm, and the holes generated by the nearby II peak in the STI left corner are favorable to be injected into the gate oxide. As a result, positive interface charges are formed as suggested previously.

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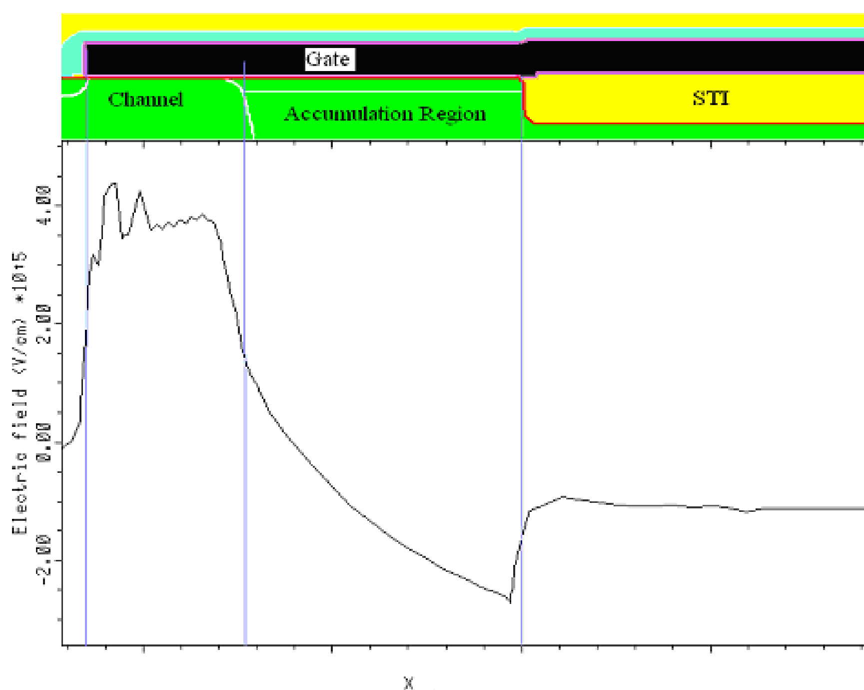
As for the STI left edge, though the direction of the vertical electric field is still favorable for hole injection, the magnitude of vertical electric field ($1x10^5$ V/cm) is smaller than that at the gate oxide/accumulation region interface ($2x10^5$ V/cm). More importantly, the horizontal electric field at the STI left edge is pointing to the left due to the high V_D, which is favorable for electron injection [45].

In summary, during the hot electron-hole pairs generation at the II peak near the STI bottom-left corner, the hot holes are forced to the gate oxide/accumulation region interface by the vertical electric field, inducing positive interface charges at the interface. The energetic hot electrons instead are injected to nearby STI, forming negative interface charges in the STI left corner.



(a)

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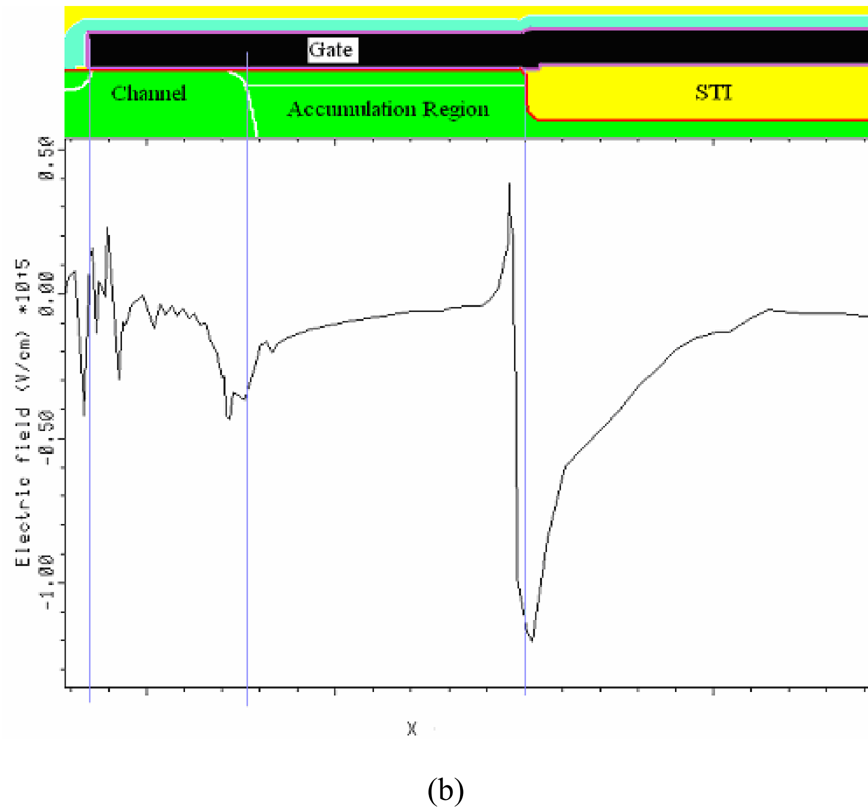

(b)

Figure 37. E-Field distribution along the Si/Si-O_2 interfaces 0.02 µm below at Stress Condition V_D = 20 V and V_G = 1.5 V

(a) Vertical E-Field; (b) Horizontal E-Field

The observed abnormal degradation behaviors of $I_{D,LIN}$ and $I_{D,SAT}$ can now be explained as the interface charges at the oxide/accumulation region affect $I_{D,LIN}$. significantly. Within the linear region (V_D = 0.1 V), the current ($I_{D,LIN}$) is more confined to the surface of the accumulation region as compared with $I_{D,SAT}$ (V_D = 20 V) as seen in Fig 38. The high electron current density only concentrates very close to the interface for linear case, while it distributes deeper inside the device for saturation region. Hence the carriers will experience greater effect of the positive interface charges at the gate oxide/ accumulation region interface.

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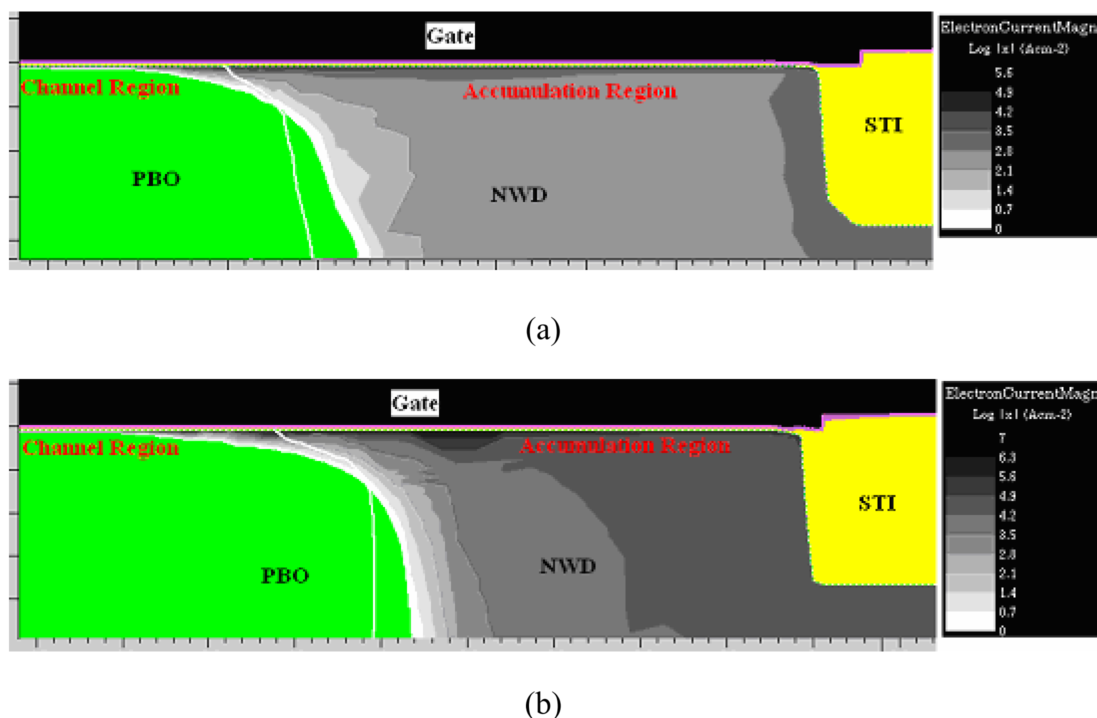

Figure 38. Electron Current Distribution in the Accumulation Region under the biasing condition of (a) $I_{D,LIN}$ @V_G = 3.3 V &V_D = 0.1 V; (b) $I_{D,SAT}$ @V_G = 3.3 V &V_D = 20 V

A schematic drawing of the electron flow in the device is shown in Figure 39. During the $I_{D,LIN}$ measurement condition, small V_D (V_D = 0.1 V) causes the electric field to point downward in the accumulation region, and the channel is not pinched off, thus the electrons flowing in the accumulation region are directional and near the surface. As a result, both positive interface charges in the oxide/accumulation interface and the negative interface charges in the STI left corner affect the degradation of $I_{D,LIN}$, resulting in its degradation behavior observed. The positive charges at the oxide/accumulation interface increases the electron concentration in

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the accumulation region, thus enhances the drain current, rendering an increase in I_D with stress time.

However, in the saturation region, the electrons will be scattered and dispersed when they cross the pinch-off point, thus the effect of the interface charge at the oxide/accumulation region is reduced, and the negative interface charges in the STI left corner will dominate the degradation of $I_{D,SAT}$, and renders it decreasing with the stress time. However, the degradation is not a perfect linear as that of $I_{SUB-P,SAT}$ because of the small effect of the positive interface charges at the gate oxide interface in the accumulation region, which has a tendency to cause the current to increase as mentioned earlier.

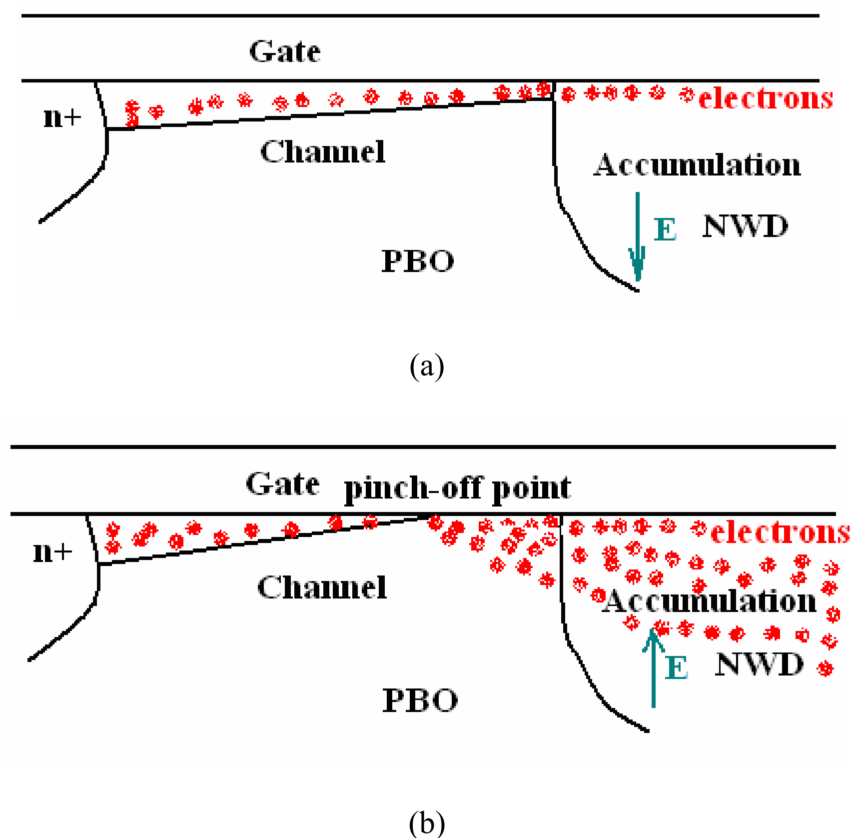

Figure 39. Schematic Draw of Electrons Flowing across the Channel

(a) Linear Region (V_D = 0.1 V); (b) Saturation Region (V_D = 20 V)

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6.3.4 $I_{SUB\text{-}P,SAT}$ Degradation Comparison for LNWD and ONWD

Due to the imperfect linear degradation of $I_{D,SAT}$ as discussed previously, $I_{SUB\text{-}P,SAT}$ is used here instead of other conventional parameters for the HCI degradation analysis and comparisons in this work. Fig 40 shows the comparison of $I_{SUB\text{-}P,SAT}$ degradations between LNWD and ONWD under the stress condition of V_D = 40 V.

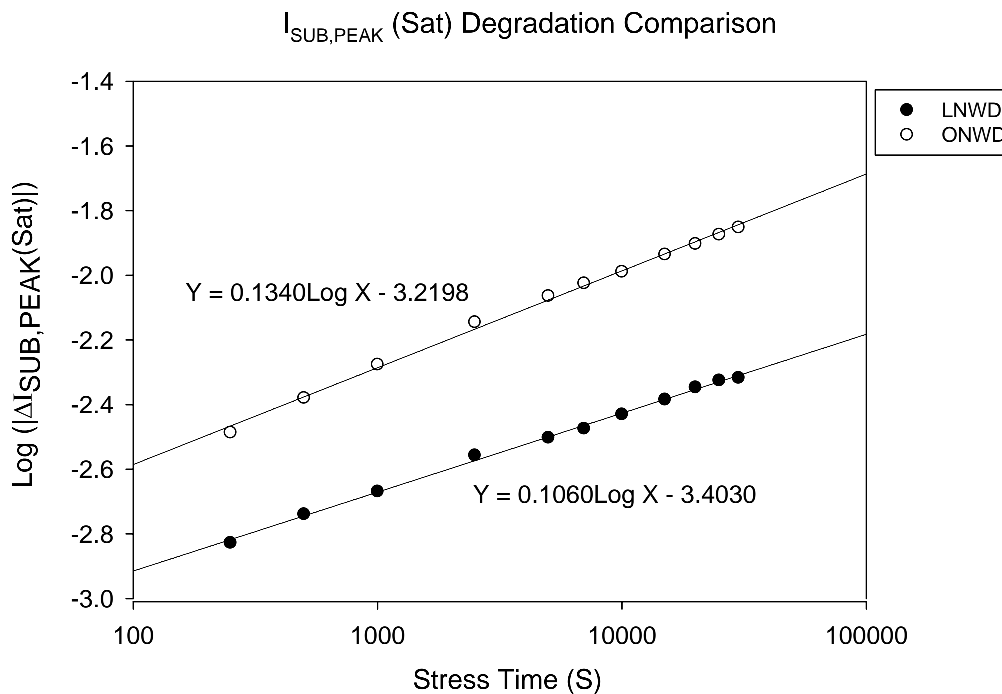

Figure 40. $I_{SUB\text{-}P,SAT}$ Degradation Comparison between ONWD & LNWD under Stress V_D = 40 V & V_G(@$I_{SUB,PEAK}$)

As seen in Fig 40, both the degradation (Y-axis) and the degradation rate (slope) of $I_{SUB\text{-}P,SAT}$ for ONWD is larger than that of LNWD. This can be understood from Fig 41 which shows the contour plot of the II generation rate for both ONWD and

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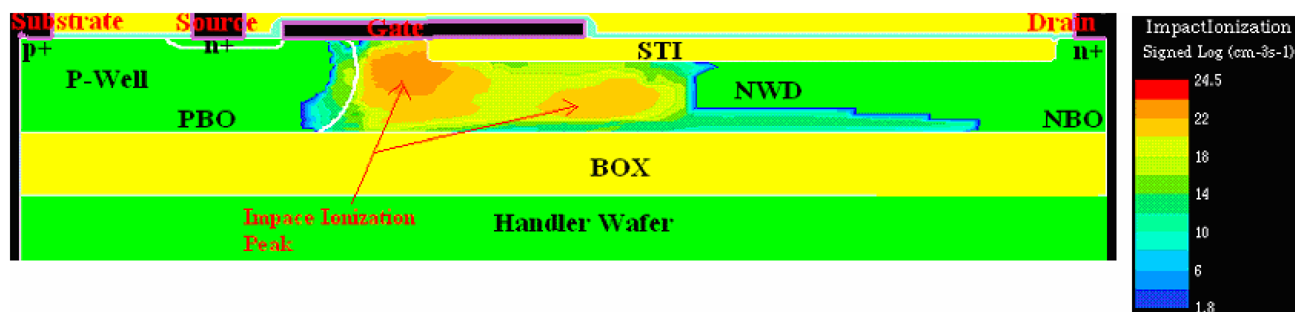
LNWD under stress condition V_D = 40 V and $V_G \approx 1.5$ V (maximum I_{SUB}). The II generation peak near the STI bottom left corner for ONWD is $3.16*10^{24}$ pairs/(cm^3*s), which is higher than that of LNWD $1*10^{22}$ pairs/(cm^3*s). This is because the higher doping concentration in the NWD region of ONWD induces higher electric field and J_E near this II peak, thereby increase the II generation rate [46, 47]. This is also verified by the I_{SUB} measurements as shown in Fig 42 where ONWD has higher I_{SUB}, implying that it has higher II generation rate. As a result, more negative interface charges [44] are generated near the STI left corner for ONWD, rendering a larger $I_{SUB\text{-}P,SAT}$ degradation and its rate. Another II peak in the drift region under the right edge of the ploy-silicon gate for LNWD is due to its faster depletion behavior.



(a)

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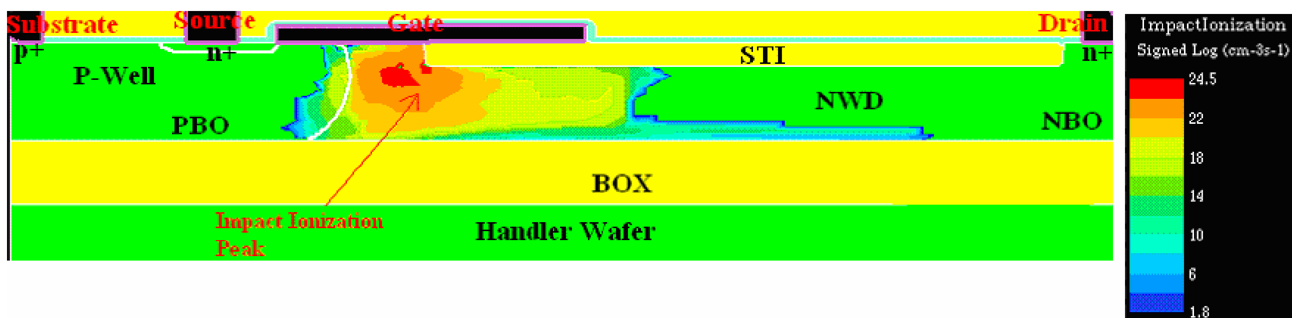

(b)

Figure 41. Impact Ionization Generation Rate at V_D = 40 V & $V_G(@I_{SUB,PEAK})$

for (a) LNWD; (b) ONWD

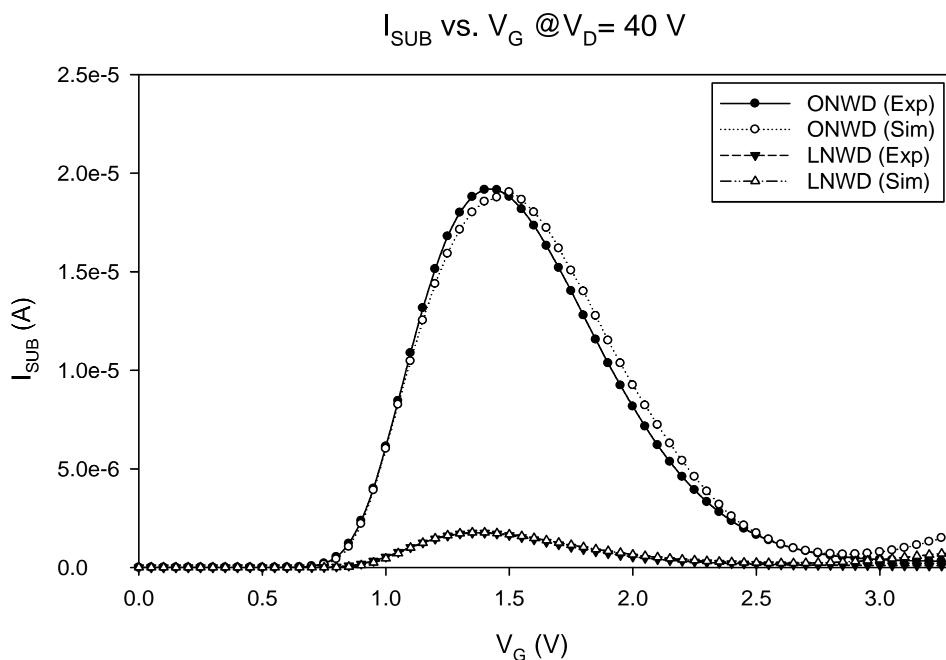

Figure 42. Measurement and Simulation of I_{SUB} vs. V_G at V_D = 40 V

From Fig 41, we can also see that there is a shifting of II peak site from the left STI corner near the source side to the center of the NWD region under STI as the doping concentration in NWD decreases. This is consistent with the finding by

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Brisbin *et al* in [47]. They found that the peak II site will move away from the left corner of the field oxide (FOX) near the source side towards the drift region under FOX by deceasing the doping in the n-type drift region.

6.3.5 $I_{SUB-P,SAT}$ Degradation Comparison at two stress conditions: V_D = 20 V & V_D = 40 V

Fig 43 shows the comparison of $I_{SUB-P,SAT}$ degradations for ONWD under stress condition V_G = 1.5 V (maximum I_{SUB}) and V_D = 20 V and 40 V respectively. Both the degradation and degradation rate are smaller at lower stress condition V_D = 20 V than that of V_D = 40 V as expected.

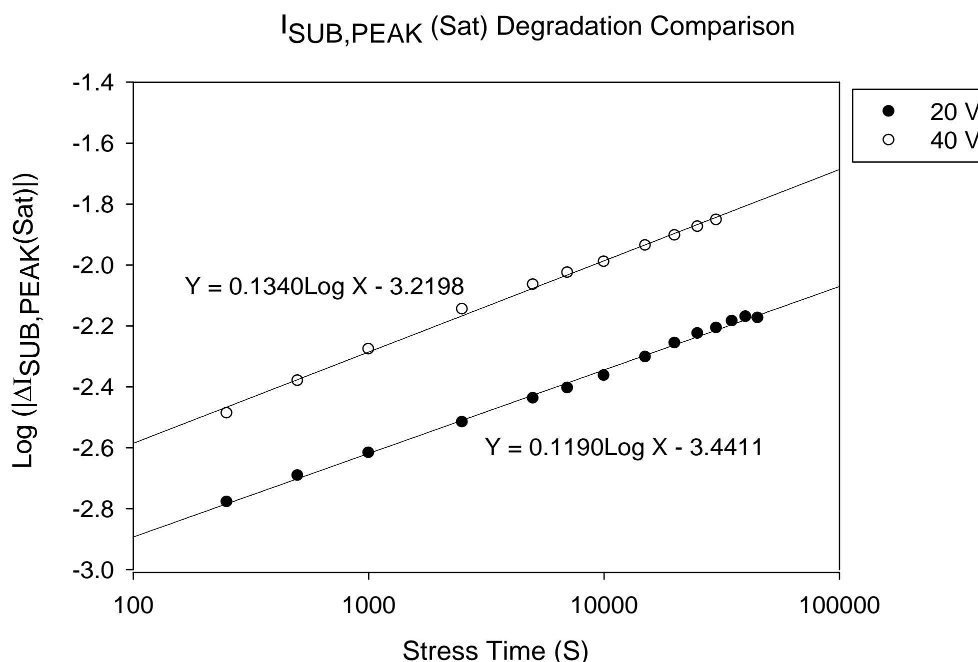

Figure 43. $I_{SUB-P,SAT}$ Degradation Comparison between Stress V_D = 20 V & V_D = 40 V with $V_G(@I_{SUB,PEAK})$ for ONWD

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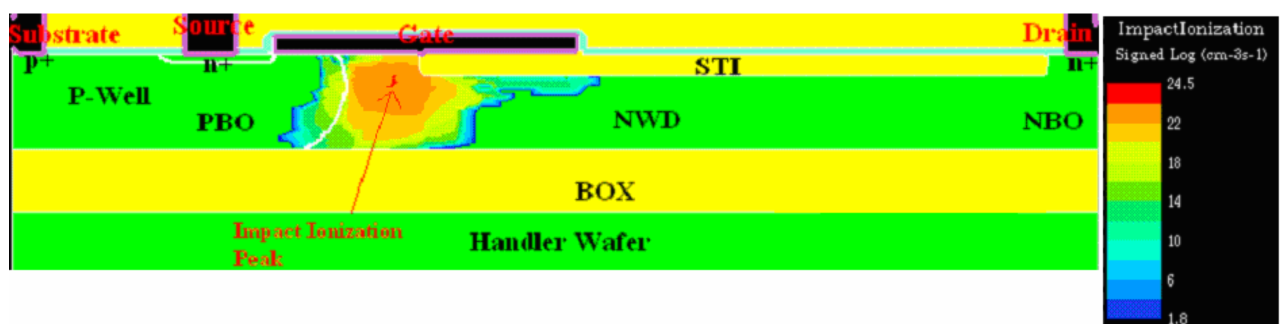
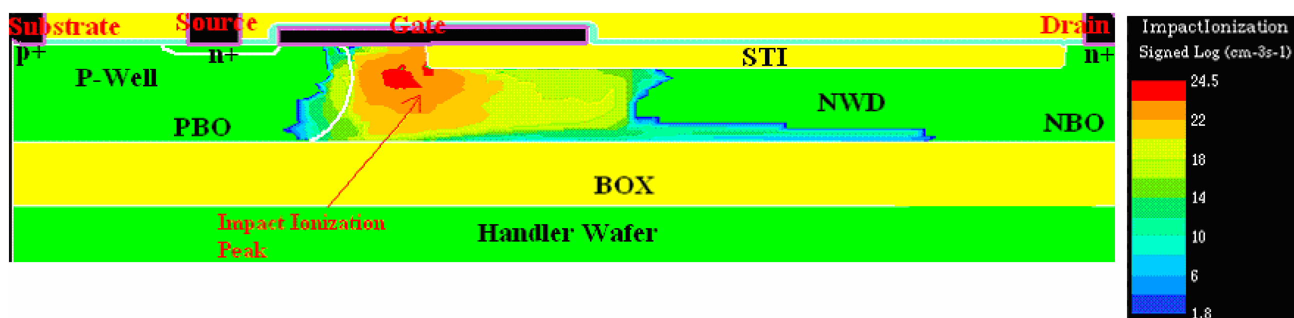
The observations shown in Fig 43 can be explained using Fig 44. Fig 44 is the contour plot of the II generation rate for ONWD at V_G = 1.5 V (maximum I_{SUB}) and V_D = 20 V and 40 V respectively. The peak area of II generation rate is larger at V_D = 40 V as shown in Fig 44. This is because at high V_D = 40 V, the potential near the STI left corner is also higher as discussed in Fig 17, which causes a higher electric field. Higher electric field induces larger II, resulting in more negative interface charges formed near the STI left corner. Therefore, at high stress condition V_D = 40 V, it has larger $I_{SUB\text{-}P,SAT}$ degradation and degradation speed.



(a)



(b)

Figure 44. Impact Ionization Generation Rate at V_D = 20 V & 40 V with $V_G(@I_{SUB,PEAK})$ for ONWD (a) V_D = 20 V; (b) V_D = 40 V

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6.3.6 I_{SUB} Degradation vs. V_G

I_{SUB} is measured at fixed $V_D = 20$ V with V_G swept from 0 to 3.3 V under stress condition $V_G \approx 1.5$ V (maximum I_{SUB}) and $V_D = 20$ V. Besides the degradation of the $I_{SUB\text{-}P,SAT}$, the degradation of I_{SUB} with V_G is also measured as shown in Fig 45. The y-axis is the degradation index of I_{SUB}. V_G from 1 V to 3.3 V is used as x-axis because I_{SUB} is too small at $V_G < 1$ V. Different lines denote the degradation after different lengths of stress interval in kilo-second (ks) as shown in legends. There are several findings from this comparison as follows:

a. The I_{SUB} degradation of ONWD is larger than that of LNWD over the entire range of V_G as expected from the previous explanation;

b. The I_{SUB} degradation increases with stress time. This is apparent since longer stress time will induce more interface defects as expected;

c. I_{SUB} reduces with stress time at low V_G range (shown as negative Y value), and then increases with stress time at high V_G (positive Y value). The threshold V_G where the degradation of I_{SUB} changes sign for ONWD (around 2.7 V) is larger than that of LNWD (around 2.4 V). In the other words, the increase of I_{SUB} appears earlier for LNWD.

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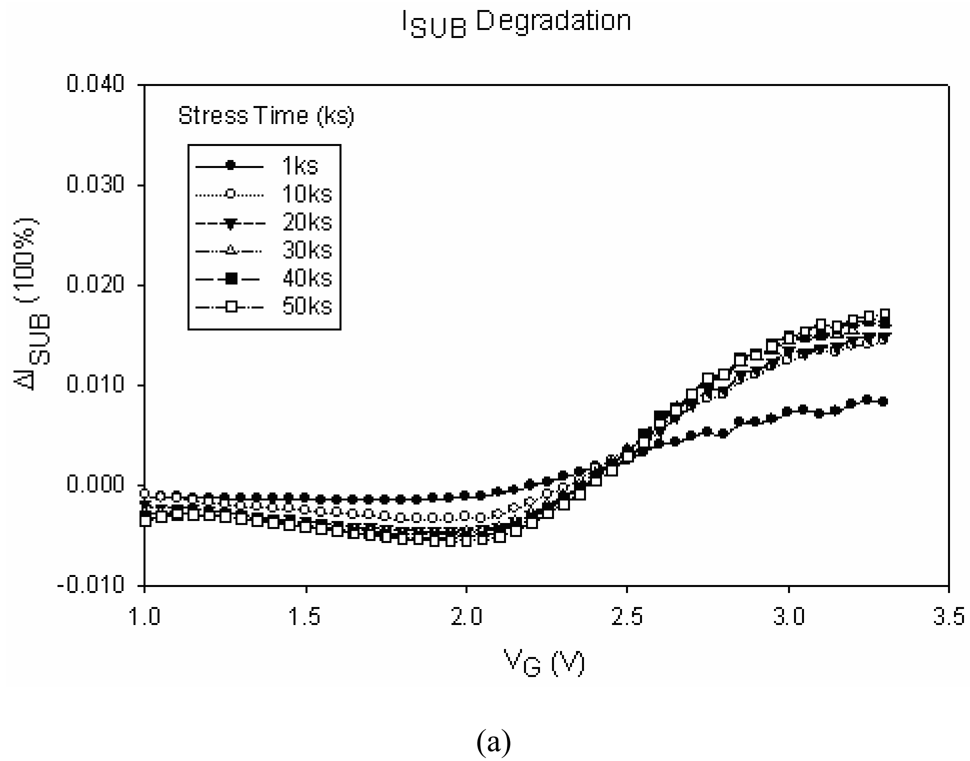
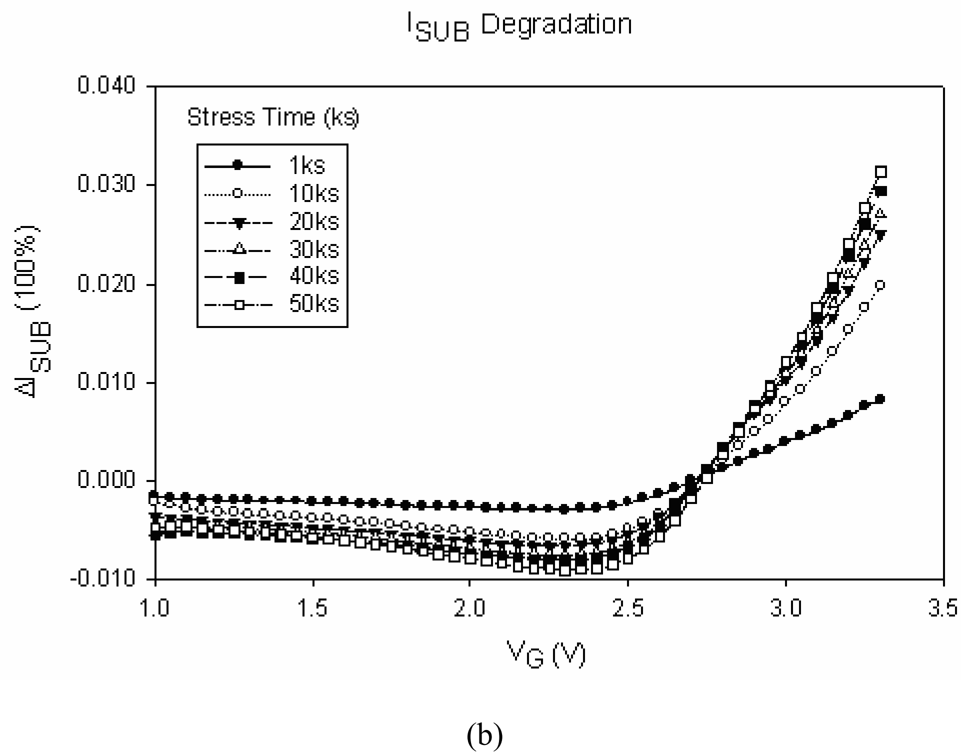


(a)



(b)

Figure 45. I_{SUB} Degradation vs. V_G Comparison under Stress Condition of V_D = 20 V & $V_G(@I_{SUB,PEAK})$ for (a) LNWD; (b) ONWD

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The change of sign for the I_{SUB} degradation in Fig 45 is due to the shift in the II peak. Fig 46 is the contour plot of the II generation rate at V_D = 20 V and V_G = 3 V for LNWD and ONWD respectively. A new II peak appears in the channel region at high V_G as shown in Fig 46. This is because as V_G increases, I_D increases and the voltage drop over the extended drift region increases. This leads to a decrease in the potential near the STI left corner, and hence a reduction in the electric field at the corner as discussed in section 4.2.1.1. Therefore, the II peak near the STI left corner reduces. Meanwhile, as V_G increasing, both the electric field and J_E in the channel region increase, which forms this new II peak. As a result, the electric field in the channel region becomes important for I_{SUB}. Hot electrons generated in the channel will be injected into the gate oxide, forming negative interface charges at the interface. These negative interface charges induce positive mirror charges near the channel surface, and cause an effective increase of the top P-Well concentration. Therefore, the electric field increases near the channel/oxide interface, inducing an increase of I_{SUB} at high V_G [44]. As V_G further increasing, the old II near the STI left corner continues to decrease, while the new II peak in the channel keeps increasing, resulting in a further increase of I_{SUB} as shown in Fig 45.

At the same V_G = 3V, the shift of the II peak from the STI left corner to the channel region is more obvious for LNWD as compared to ONWD as shown in Fig 46. In Fig 46 (a) LNWD, the II peak area at STI left corner is smaller than the II peak in the channel region; while for ONWD, the II peak at STI left corner is

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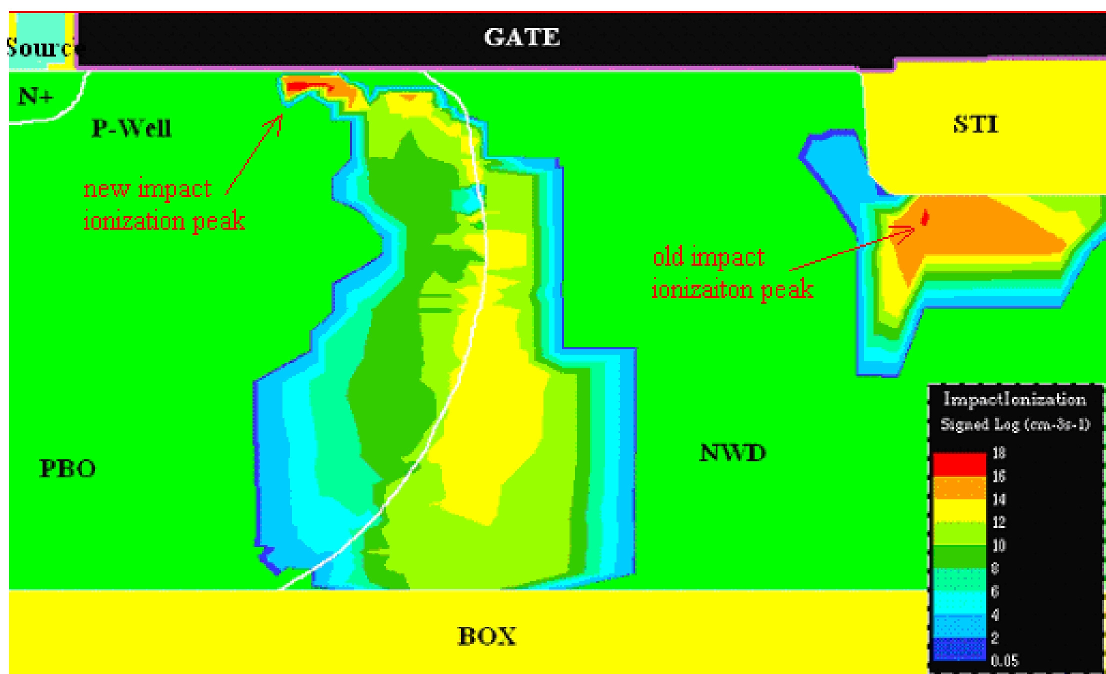
still a bit larger than that in the channel region. This verifies our previous experimental observations where, the I_{SUB} degradation changes sign at lower V_G for LNWD. The lower V_G for LNWD is attributed to the larger drift region resistance, thus the voltage drop over the drift region is larger and faster as V_G is increasing.



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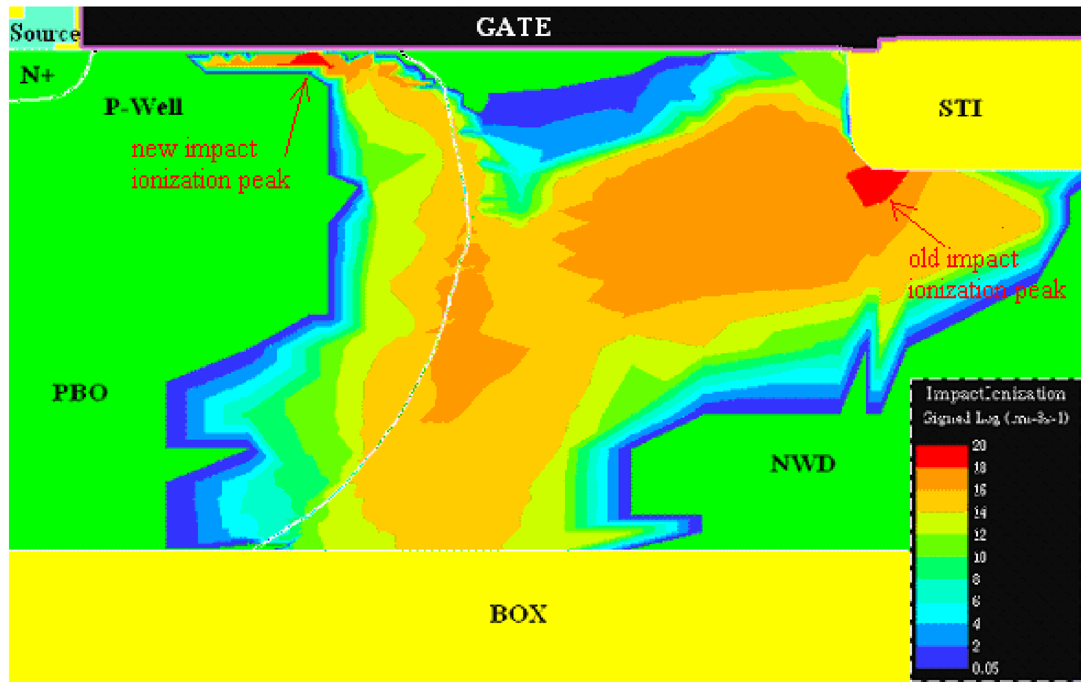

(b)

Figure 46. Impact Ionization Generation Rate at V_D = 20 V & V_G = 3 V

(a) LNWD; (b) ONWD

6.3.7 Abnormal Degradation Behavior of LNWD at V_D = 20 V

Abnormal large degradation rate (slope) of LNWD under stress condition V_D = 20 V as shown in Fig 47 is observed in our work. Its degradation (Y-axis) is small due to its low NWD doping and the low stress condition, which is consistent with the previous results and explanations. However, its degradation speed (slope) is larger than that of ONWD under the same stress condition V_D = 20 V (Figure 43); and it is also larger than that of the same LNWD under higher stress condition V_D = 40 V (Figure 40). As seen in Fig 48 the II contour comparison between LNWD and

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ONNWD at V_D = 20 V with V_G at maximum I_{SUB} stress condition, the II peak for both devices is at the STI bottom-left corner. As shown in Fig 48, the II generation rate for ONWD is a bit higher than that of LNWD, which is because of its higher electric field and higher current density as discussed previously. Since the theoretical explanation leads to an opposite conclusions as the real experiment results, the explanation to this abnormal observation still remains unclear. Hence, the further investigation for this actual mechanism will be our future work.

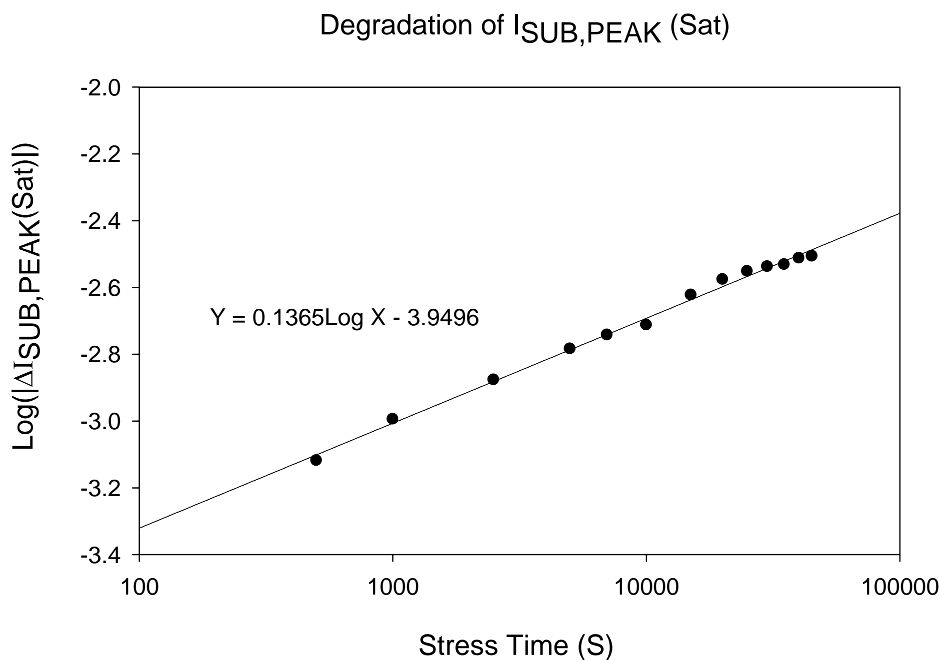

Figure 47. $I_{SUB-P,SAT}$ Degradation at Stress Condition of V_D = 20 V & $V_G(@I_{SUB,PEAK})$ for LNWD

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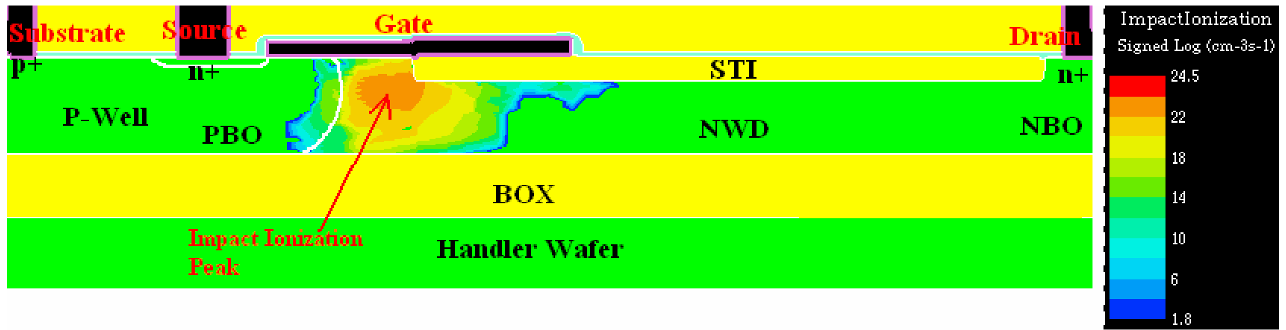
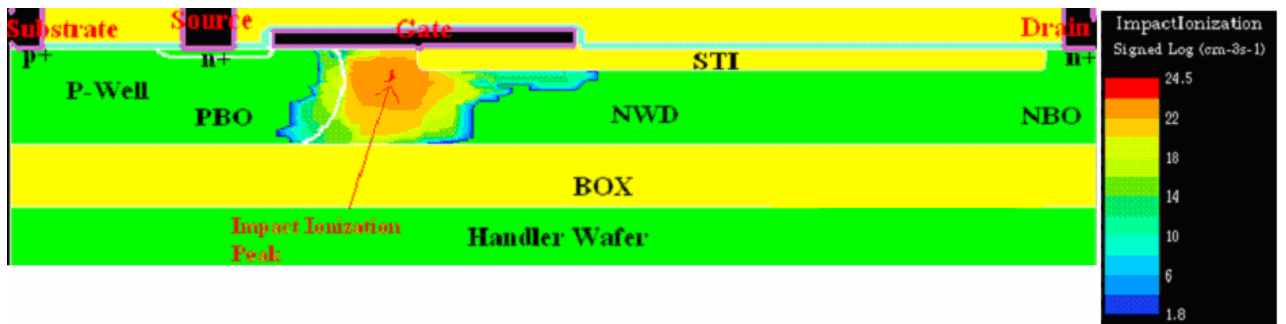


(a)



(b)

Figure 48. Impact Ionization Generation Rate at V_D = 20 V & V_G (@$I_{SUB,PEAK}$) for (a) LNWD; (b) ONWD

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Chapter 7. Conclusion and Recommendations

7.1 Conclusion

The electrical characteristics of the SOI LDNMOS transistors with respect to hot carrier reliability under different bias conditions and with different implant dose in the extended drift region (NWD) are measured and analyzed in this project. The experimental result shows that I_{SUB} instead of I_G is chosen as the indicator of the hot carrier reliability problem in our work, because most of the II generated electrons go to the high drain contact instead of the gate.

The effects of the different NWD doping levels on the hot carrier generation and HCI degradation are compared and studied. The results show that the device with higher implant dose in the NWD region has higher I_D and I_{SUB}, as well as severer HCI degradation. This is due to the different drift region doping has different R_{ON}, carrier mobility, electric field, self-heating effect and II generation rate, which work together to have complex impacts on its electrical performance.

HCI degradations test under different stress conditions are performed by monitoring key electrical parameters. Abnormal degradation behaviors are found due to the different HCI degradation mechanisms for this SOI LDNMOS with STI structure compared with standard HV LDNMOS. Negligible HCI damage in the channel region under maximum I_{SUB} stress condition is found because the II peak is near the STI left corner. Positive interface charges in the accumulation region

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and negative interface charges in the STI left corner are concluded from experimental results and simulation analysis.

Degradation analysis for I_{SUB} at different V_G region is also performed. At low V_G, I_{SUB} reduces due to the negative interface charges near the STI left corner. As V_G increasing, a new II peak in the channel appears which induces negative interface charges formed in the channel region, thereby increases I_{SUB}. For LNWD, this new II peak appears at lower V_G due to its faster electric field drop in the STI left corner.

7.2 Recommendations for Further Research

Due to the limitation of the experiment equipment, the higher V_D ($V_D > 40$ V) measurement of the SOI LDNMOS is not performed in this work. The electrical performances and the HCI degradation behaviors at $V_D > 40$ V could be different from that at $V_D \leq 40$ V. Measurement and HCI degradation test could be performed at higher V_D if the equipment is available to study the influence of the higher V_D on the shift of the II peak and the hot carrier injection location.

The simulation analysis for other process parameters variation such as the length of the poly-silicon gate and length of the STI could also be studied to see their effects on the device's electrical performance and hot carrier problem. If the real devices are available for these process parameter variations, measurement could be done to

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verify the simulation result. This will give us an understanding of how these process parameter variations will influence the electrical characteristics.

The abnormal high degradation rate of LNWD stressed at V_D = 20 V remains unclear, which needs further investigation.

Based on the results of all these studies we could optimize the process, and get an advanced power device with high electrical performances and less hot carrier problems.

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Author's Publications

1. Jie Liao, Cher Ming Tan and Geert Spierings, *Behavior of hot carrier generation in power SOI LDNMOS with shallow trench isolation (STI)*, Microelectronics Reliability, 2009. **49**: p. 1038-43
2. Jie Liao, Cher Ming Tan and Geert Spierings, *Hot Carrier Reliability of Power SOI EDNMOS.* (Submitted to IEEE Transactions on Power Electronics)
3. Jie Liao, Cher Ming Tan and Geert Spierings, *Hot carrier induced (HCI) degradation in power SOI LDNMOS with different drift doping*. (Submitted to Microelectronics Reliability)

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