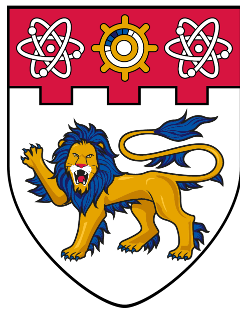

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HIGH FREQUENCY GAN HIGH ELECTRON MOBILITY TRANSISTORS FOR MM-WAVE POWER AMPLIFIER APPLICATIONS

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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LI HANCHAO

SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

A thesis submitted to the Nanyang Technological University

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Doctor of Philosophy

2026

Statement of Originality

I hereby certify that the work embodied in this thesis is the result of original research, is free of plagiarized materials, and has not been submitted for a higher degree to any other University or Institution.

5 January 2026

Date

Li Hanchao

Supervisor Declaration Statement

I have reviewed the content and presentation style of this thesis and declare it is free of plagiarism and of sufficient grammatical clarity to be examined. To the best of my knowledge, the research and writing are those of the candidate except as acknowledged in the Author Attribution Statement. I confirm that the investigations were conducted in accord with the ethics policies and integrity standards of Nanyang Technological University and that the research data are presented honestly and without prejudice.

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Ng Geok Ing

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This thesis contains material from 3 paper(s) published in the following peer-reviewed journal(s) in which I am listed as the first author.

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- Prof. Geok Ing Ng provided overall research guidance and reviewed the manuscript
- I conducted the research, performed data analysis, prepared the initial manuscript drafts, and coordinated contributions from all co-authors to ensure quality and coherence
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"Two roads diverged in a wood, and I—

I took the one less travelled by,

And that has made all the difference."

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Table of Contents

Acknowledgement VIII
Abstract XIII
List of Figures XV
List of Tables XIX
Publications XX
Chapter. 1 Introduction 1
1.1 Background and Motivation 1
1.2 Research Objectives 10
1.3 Major Contributions 13
1.4 Organization of the thesis 15
Chapter. 2 Device Fabrication Technology and Characterization Methods 17
2.1 Polarization Effects and Operation Principles of GaN-Based Heterostructures 17
2.1.1 Structure Properties and Polarization Effects in GaN-Based HEMTs 17
2.1.2 Piezoelectric Polarization in AlGaN/GaN Heterostructures 19
2.1.3 Formation of Two-Dimensional Electron Gas 20
2.1.4 2DEG Density and Device Characteristics 21
2.1.5 Operational Principles and Advantages of AlGaN/GaN HEMTs 22
2.2 GaN HEMT fabrication process 24
2.2.1 Mesa Isolation 25
2.2.2 Ohmic Contact Formation 26
2.2.3 T-gate Formation Technology 29
2.2.4 Passivation Techniques 31
2.3 Device Characteristics Methods 33
2.3.1 DC Characteristics 33
2.3.2 Pulsed iv characteristics 34
2.3.3 Small Signal RF Characteristics and Modelling 37
2.3.4 Noise Characteristics and modelling 46
2.3.5 Large Signal Power Characteristics 49

Chapter. 3 AlN/GaN/AlGaN DH HEMTs for low-voltage FR2 Mobile Applications 55
3.1 Technology Development and Research Motivation 55
3.2 Limiting factors in III-V GaN HEMTs for high frequency operation 57
3.2.1 Advantage in AlN as barrier 57
3.2.2 Role of Back Barrier 58
3.3 Device fabrication 61
3.4 Device characterizations 63
3.4.1 DC Characterization...63
3.4.2 Small Signal RF Characterization..64
3.4.3 Noise Characterization...65
3.4.4 Large Signal Characterization..67
3.5 Contributions to GaN mm-Wave Development.......................................69
3.6 Summary 71
Chapter. 4 First demonstration on D-band GaN-on-Si Power Amplifier 73
4.1 Technology Development and Research Motivation 73
4.2 Ultra-high Frequency GaN HEMT RF Device Research 75
4.2.1 Design Challenges for D-band Power Amplifiers 75
4.2.2 Device Scaling and Parasitic Effects for D-band Operation................77
4.3 Epitaxial Material Characterization and Device Fabrication....................81
4.4 Device Characterization 84
4.4.1 DC Characterization...84
4.4.2 Small Signal Characterization..85
4.4.3 Large signal characterization 88
4.5 Contributions to GaN mm-Wave Development.......................................91
4.6 Summary 93
Chapter. 5 Multi-channel AlN/GaN Schottky barrier diodes 94
5.1 Technology Development and Research Motivation 94
5.2 Issues on Current III-V Technology...96
5.2.1 Current Status on Single-Channel GaN HEMT 96
5.2.2 Challenges in Multi-channel Implementation.....................................97
5.3 Device Fabrication 98

5.3.1 Epitaxial Growth and Material Analysis 98
5.4 Device Characteristics 104
5.4.1 C–V characteristics 104
5.4.2 Forward and Reverse IV Characteristics 105
5.4.3 Analysis of Current Transportation 107
5.5 Contributions to GaN mm-Wave Development 110
5.6 Summary 111
Chapter. 6 GaN HEMTs using GaN-on-Insulator Technology via 200 mm Wafer Bonding 112
6.1 Technology Development and Research Motivation 112
6.2 Advantages and Challenges of Bonding Technology 115
6.2.1 Thermal Management Analysis of GaNOI Structure 115
6.2.2 Process Integration Challenges in GaNOI Bonding Technology 117
6.3 Device Fabrication 119
6.4 Characterization and Mechanism Analysis 122
6.4.1 XRD and Raman Analysis 122
6.4.2 DC Characterization 125
6.4.3 Small Signal RF Characterization 126
6.5 Conclusion 129
Chapter. 7 Conclusion and Recommendation for Future Work 130
7.1 Conclusions 130
7.2 Recommendations for Future Work 132
Bibliography 133

Abstract

This dissertation presents a comprehensive investigation into the design, optimization, and high-frequency characterization of Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) on silicon substrates for millimeter -wave applications. GaN-on-Si technology offers a compelling combination of high-power handling, superior frequency performance, and cost-effective manufacturing, making it particularly promising for next-generation wireless communication systems.

The research begins with a fundamental analysis of III-nitride semiconductor properties, emphasizing the unique wurtzite crystal structure and polarization mechanisms that facilitate the formation of a two-dimensional electron gas (2DEG) at heterojunction interfaces. This inherent material advantage endows GaN HEMTs with exceptional electron transport properties, surpassing those of conventional semiconductor devices. An examination of the interplay between heterostructure design, material quality, and device performance lays the groundwork for subsequent device optimizations.

For 5G FR2 applications, the dissertation demonstrates state-of-the-art low-voltage performance. Under a drain bias of 3.5 V and 5 V, continuous-wave load-pull measurements at 30 GHz yielded saturated output powers of 0.6 W/mm and 1.3 W/mm, respectively, with corresponding power-added efficiencies of 43% and 42%. These results set new performance benchmarks for low-voltage GaN-on-Si HEMTs in the 5G FR2 band, even when using conventional alloyed contacts and a conservative gate length of 120 nm.

Looking toward future 6G communication systems, the research provides essential technological solutions for operation in the D-band and beyond. The demonstration of power amplification at 123 GHz with GaN-on-Si HEMTs not only extends the operational frequency into the sub-THz regime but also establishes a solid foundation for the development of next-generation power amplifiers capable of meeting the demands of emerging wireless standards.

This dissertation also investigates the multi-channel AlN/GaN heterostructures for Schottky barrier diode applications. Through temperature-dependent current-voltage characterization, the study reveals that both thermionic emission and tunnelling mechanisms contribute to current transport. This dual-mechanism insight is crucial for device designs to specific operational conditions and paves the way for further performance optimization.

In addition to these device-level innovations, the integration of GaN devices with complementary metal-oxide-semiconductor (CMOS) technology is explored. The successful implementation of GaN-on-Insulator (GaNOI) substrates via 200 mm wafer bonding demonstrates improved thermal management and electrical performance, thereby facilitating more compact, efficient systems that combine high-power and high-frequency capabilities on a single chip. This integrated approach addresses a critical barrier to the widespread adoption of GaN technology in commercial communication systems.

By advancing both the theoretical understanding and practical implementation of GaN-on-Si technology, this work addresses key technological challenges while charting a clear path towards cost-effective, high-performance solutions for future wireless communication systems. The contributions of this dissertation not only establish new performance benchmarks but also offer valuable design guidelines and theoretical insights that will inspire future research in high-frequency power amplifier technologies.

List of Figures

Fig. 1-1 GaN in satcom marketplace [18]........5

Fig. 1-2 Electromagnetic Spectrum Frequency Bands and Applications in RF Communications [23].6

Fig. 1-3 Comparison of power density versus frequency for GaN devices compared to traditional Si and GaAs technologies in RF applications [25]. 7

Fig. 1-4 Roadmap showing the projected evolution of GaN RF device technologies with performance metrics and timeline estimates [22]. 8

Fig. 2-1 (a) Diagram illustrating the atomic configuration within GaN wurtzite crystal lattice, depicting both Ga(Al)-face and N-face orientations; (b) Directional representation of P_{SP} and P_{PE} polarization in AlGaN/GaN heterostructures for both orientations, and the resulting polarization-induced interface charges. 18

Fig. 2-2 Energy-band diagram of AlGaN/GaN heterostructure. (b)Charge distribution at different interfaces, and formation of 2DEGwith electrons supplied by surface donor states [39]. 20

Fig. 2-3 The schematic of fabrication process flow for a deep-submirometre GaN HEMTs........24

Fig. 2-4 (a) Schematic diagram of the Transmission Line Method (TLM) test structure, (b) Plot showing the relationship between total resistance to TLM pad spacing d and width w, (c) Current-voltage (I-V) measurements from the TLM structures, (d) Plot of the total resistance R_{tot} versus distance, used for extraction of contact resistance and sheet resistance for metal contacts annealed at 775 °C........27

Fig. 2-5 Overview of the Bi-layer T-gate Fabrication Process 29

Fig. 2-6 T-gates with 120 nm gate foot length fabricated using PMMA/PMMA-MAA bilayer resist. (a) Gate head width of 300 nm; (b) Gate head width of 350 nm; (c) Gate head width of 500 nm........30

Fig. 2-7 Detailed drain voltage biasing conditions in above pulsed I-V measurement. (a)Pulsed Id-Vd and (b) I_d-V_g measurements with cold quiescent, gate lag and drain quiescent conditions are plotted. 35

Fig. 2-8 Schematic cross section of AlN/GaN HEMT, showing electron trapping location [8]. 36

Fig. 2-9 S-parameters of 2-port network with arbitrary source and load impedances 37

Fig. 2-10 Schematic flowchart of the S-parameter extraction and de-embedding procedure for isolating intrinsic device characteristics. 39

Fig. 2-11 22-element model of GaN HEMT considering parasitic conduction 41

Fig. 2-12 Flow chart of small signal parameter extract using ASM-HEMT and ANN modelling......43

Fig. 2-13 Measured (blue symbols), ASM model simulated (black dashed lines) and proposed hybrid model simulated (red lines) S-parameters in 1-40 GHz of (a) 2 × 50 μm, V_{GS} = −2.0 V, V_{DS} = 10 V; (b) 2 × 50 μm, V_{GS} = 1.5 V;V_{DS} = 10 V, (c) 2 × 100 μm, V_{GS} = −2 V, V_{DS} = 10 V, and (d) 2 × 100 μm, V_{GS} = −1.5 V, V_{DS} = 10 V [68]........45

Fig. 2-14 Equivalent noise modelling circuit........46

Fig. 2-15 Procedure of noise parameters modelling 47

Fig. 2-16 The diagram of load line for Class A amplifier. 50

Fig. 2-17 Performance comparison between CW and pulsed-mode load-pull characterization at 10 GHz, revealing dispersion effects in GaN HEMT operation. 53

Fig. 3-1 Bandgap of InAlN and AlGaN compound 57

Fig. 3-2 (a) Band diagrams of the proposed double heterostructure (DH) and a conventional single heterostructure (SH). 59

Fig. 3-3 (a) A cross-sectional schematic of the proposed AlN/GaN/AlGaN DH HEMT. (b) Elemental composition of the proposed heterostructure, as determined by energy dispersive X-ray spectroscopy (EDX). (c) STEM image of the proposed heterostructure and (d) T-shaped gate profile. 61

Fig. 3-4 Key fabrication process of AlN/GaN MISHEMT 62

Fig. 3-5. DC characteristics. (a) Output characteristics. (b) Transfer characteristics (linear scale). (c) Transfer characteristics (logarithmic scale). (d) Three-terminal breakdown characteristics 63

Fig. 3-6 De-embedded RF small-signal characteristics. (a) Gain vs. frequency. (b) f_T and f_{max} vs. V_d. (c) f_T and (d) f_{max} vs. V_g at different V_d. 65

Fig. 3-7 (a) NF_{min} and G_a (scatter points: measured, dashed lines: simulated), and (b) Measured Rn and Rn/$|Z_{opt}|$ versus frequency at I_{ds} = 200mA/mm and V_{ds} = 5 V. 66

Fig. 3-8 NF_{min} versus L_g benchmarking of this work against state-of-the-art GaN HEMTs at the frequency range of 26-30 GHz. 67

Fig. 3-9 (a) Power sweep at 30 GHz CW, V_{ds}=5 V, and Class AB operation. (b) Load-pull performance vs. V_{ds}. 68

Fig. 3-10 (a) Benchmark of P_{sat} vs. V_{ds} for LV 5G FR2 operation. (b) Comparison of v_{sat} vs. V_{knee} (normalized by L_{sd}) for reported LV GaN-on-Si transistors in FR1, FR2, and FR3. 71

Fig. 4-1 Comparison of Shannon Capacity Limit and Practical Modulation Schemes........ 75

Fig. 4-2 Benchmarking with state-of-the-art (a) f_T (b) f_{max} versus L_g for GaN HEMTs on Si substrates. 78

Fig. 4-3 GaN HEMT structure and its corresponding small-signal equivalent circuit model........ 79

Fig. 4-4 Proposed AlN/GaN/AlGaN-on-Si MIS-HEMT. (a) Schematic. (b) Cross-sectional image obtained by transmission electron microscopy (TEM), showing Lg / Lgs / Lgd=140 / 480 / 680 nm, giving Lsd=1.3 μm. 81

Fig. 4-5 STEM-EDXS mapping of in-situ SiN/AlN/GaN epitaxy. (a) cross-sectional STEM image (b) the corresponding EDXS mapping of Ga, Al, N, Si, O atoms. (c) Atomic fraction element profile as indicated by line scan 82

Fig. 4-6 DC characteristics. (a) Output characteristics, showing I_{dmax}=2 A/mm, and R_{on}=1.1 Ω·mm. (b) Transfer characteristics, showing g_{mmax}=0.65 S/mm. (c) Three-terminal breakdown characteristics. (d) Pulsed I-V characteristics. 84

Fig. 4-7 RF small-signal characteristics. (a) Small-signal current and power gain vs. frequency, showing f_T / f_{max}=112 / 205 GHz. (b) Small-signal equivalent circuit model. (c) Comparison of equivalent circuit modelling results and measured s parameters, showing a close fit of s_{11}, s_{12}, s_{21}, s_{22} (deviation of <5 %)........ 87

Fig. 4-8 RF large-signal performance at 123 GHz CW. (a) Measurement setup, which supports tuning at the fundamental frequency. (b) Power sweep results at V_{ds} = 5 V. A maximum PAE of 5.3 % was achieved at P_{out} = 0.36 W/mm. (c) Power sweep results at V_{ds}=10 V. A P_{sat} of 0.67 W/mm was achieved. 88

Fig. 4-9 Benchmark of RF large-signal performance of GaN HEMTs and MMICs at 120 – 140 GHz. (a) P_{out} vs. V_{ds}. The epitaxial structure and L_g are specified. (b) PAE vs. P_{out}. The L_g and V_{ds} are specified. The name of the foundry, if different from the publishing affiliation, is written in parentheses. 90

Fig. 4-10 The progress of GaN-on-Si HEMTs in terms of frequency. 91

Fig. 5-1 (a) N_s, μ, and R_{sh} as a function of the number of channels in multi-channel structures (b) N_s vs μ for single (hollow points) and multi-channel (soild points) heterostructures [168]. 96

Fig. 5-2**.** Heterostructure and SBD demonstrated in this work. (a) Schematic of the epitaxy structure of the proposed 5-channel AlN/GaN heterostructure on 4" SiC substrate. (b) STEM image for the cross-section of the proposed heterostructure. (c)–(e) EDS elemental mappings of the proposed heterostructure. 98

Fig. 5-3 (a) Band diagram and the calculated spatial distribution of polarization-induced charge. In the calculations, the heterostructure is assumed to be unintentionally doped. Material characterization of a 5-channel AlN/GaN heterostructure. (b) Reciprocal space mapping, and (c) Measured (002) GaN X-ray diffraction spectrum. (d) Benchmarking of N_s and μ (based on Hall measurements) for reported multi-channel III-nitride heterostructures. Solid symbols indicate that there are reports of fabricated devices on these heterostructures, such as this work, and hollow symbols indicate otherwise. 99

Fig. 5-4 Key fabrication Process of multi-channel AlN/GaN diode 100

Fig. 5-5 Optimization of ohmic contact technology for the proposed heterostructure. (a) schematic illustration of the device structure based on the proposed five-channel AlN/GaN heterostructure, (b) Cross-sectional focused ion beam scanning electron microscope analysis of the ohmic contact with the sidewall angle. (c) Two sets of TLM data which illustrates the improvement in R_c after ohmic recess. (d) Impact of recess depth on R_c. A minimal R_c=0.38 Ω·mm was achieved after recessing to the mid-point of the 4th channel. The vertical dashed lines serve as a guide to the eye to indicate the location of the 4th channel. Device Processing and Contact Formation 101

Fig. 5-6 (a) C–V characteristics of the proposed heterostructure, measured at a frequency of 200 kHz and an AC amplitude of 50 mV. (b) Spatial distribution of electrons among five channels in the proposed heterostructure as measured and simulated. 104

Fig. 5-7 (a) Forward I–V characteristics of the proposed devices with varying L_{AC}. (b) Reverse I–V characteristics of the proposed devices with varying L_{AC}. 105

Fig. 5-8 Channel current and buffer leakage current. The corresponding device structures used to measure these currents are presented in the inset. 106

Fig. 5-9 High temperature (up to 125°C) electrical characterization of a SBD with L_{AC}=3 μm. (a) Forward and reverse I–V characteristics in logarithmic scale. (b) Ideality factor (η) and Schottky barrier height (ϕ_B) as a function of temperature. The line indicates calculation of η by Equation 5. 2. 108

Fig. 6-1. The schematic illustrates the integration of Si-CMOS, RF devices, and potential high-power devices, comprising HEMTs on both III-N and III-As/P layers, onto a single wafer forming a hybrid substrate 113

Fig. 6-2 Comparison of the heat dissipation power density at channel temperature of 150 ºC [157]. 115

Fig. 6-3 (a) Schematic diagram of the GaNOI-on-Si wafer fabrication flow. (b) Cross-sectional TEM image illustrating the layered structure of a GaNOI wafer, including the GaN buffer, seed layer, bonding material, and new Si substrate. (c) AFM Characterization of Surface Topography Following the Bonding Process for the 10×10 μm^2 scan. 119

Fig. 6-4 Key fabrication processes for InAlN/GaNOI HEMTs 120

Fig. 6-5 Wafer bowing images measured by FLX Thin Film Stress Measurement Systems (a) GaN-on-Si wafer (bowing: 7.57 µm, concave), (b) GaNOI-on-Si wafer after SiO2 double bonding and layer transfer process (bowing: 3.88 µm, convex). 122

Fig. 6-6 Raman spectra of both GaN-on-Si and GaNOI-on-Si samples, high resolution E2 modes. 123

Fig. 6-7 (a) Extraction of R_c and R_{sh} through a linear fit of the TLM, plotting the relationship between total resistance and distance between pad contacts. (b) transfer and (c) output characteristics of a 120-nm gate GaNOI device. (d) Semi-log-scale transfer curves at V_{ds} = 1 V and gate leakage characteristics. 125

Fig. 6-8 The RF small-signal characteristics of the device after de-embedding pad parasitics with a bias of (a) V_{ds} = 5 V and V_{gs} = –3 V, (b) V_{ds} = 10 V and V_{gs} = –3 V. 126

Fig. 6-9 Comparison of the f_T of our GaNOI HEMTs on Si against the reported f_T data for GaN HEMTs on Si from other research groups. 127

List of Tables

Table 1.1 Material properties of common semiconductors at 300 K 2

Table 3.1 LV(≤5V) GaN-on-Si HEMTs for 5G FR2 operation. 6 9

Table 4.1 The extracted parameters for AlN/GaN/AlGaN MISHEMTS on Si with W_g = 2×16 μm, L_g = 120 nm and calculated delay components 87

Table 6.1 Comparison of Key XRD Parameters. 123

Table 6.2 Comparison of Hall measurement results. 124

Publications

Journal papers:

1. **Li, H**., Xie, Q., Lu, Z., Xie, H., Zhuang, Y., Liu, S., ... & Ng, G. I. (2025). GaN-on-Si HEMT for D-Band Power Amplification Demonstrating 0.67 W/mm at 10 V. IEEE Electron Device Letters.
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5. Liu, S., Zhuang, Y., **Li, H**., Cui, P., Xie, Q., Wang, Y., ... & Ng, G. I. (2025). Analysis of Leakage Channel with Different Al Composition back Barriers in AlN/GaN High-Electron-Mobility Transistors on Silicon. physica status solidi (a), 222(23), 2400983.
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Conference papers:

1. Lu Z, **Li H**, Zhuang Y, Xie H, Ng GI, Zheng Y. An ANN-Physical Hybrid GaN HEMT Model for 5G Power Amplifiers. In: 2024 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS). p. 414–8.
2. **Li H**, et al. “Low-Voltage AlN/GaN/AlGaN-on-Si MISHEMT with Record Pout of 1.7 W/mm at 6V and 30GHz.” 12th International Workshop on Nitride Semiconductors (IWN 2024). (Oral Presentation)
3. **Li H**, et al. “First Demonstration of Schottky Barrier Diodes in Multi-Channel AlN/GaN Heterostructures.” 12th International Workshop on Nitride Semiconductors (IWN 2024). (Oral Presentation)

4. **Li H**, et al. "First Demonstration of GaN-on-Si HEMT for D-Band Power Amplification." 12th International Workshop on Nitride Semiconductors (IWN 2024). (Oral Presentation)
5. Liu S, **Li H**, et al. "Analysis of Leakage Channel with Different Al composition Back-barrier in AlN/GaN High Electron Mobility Transistor on Si." 12th International Workshop on Nitride Semiconductors (IWN 2024). (Oral Presentation)
6. Zhuang Y, **Li H**, et al. "Characterization of deep region trapping effects in AlN/GaN HEMTs with an AlGaN back barrier Utilizing tri-state pulsed IV technique. 12th International Workshop on Nitride Semiconductors (IWN 2024).
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8. **Li H**, et al. "Improved DC and RF Performance of InAlN/GaN HEMT using GaN-on Insulator Technology." 14th International Conference on Nitride Semiconductors (ICNS-14). (Oral Presentation)
9. Xie H, **Li H**, et al. "High-Al-Composition Al0.65Ga0.35N/GaN MISHEMTs on Si Fabricated with CMOS-Compatible Metallization for mm-Wave Applications." 14th International Conference on Nitride Semiconductors (ICNS-14). (Oral Presentation)
10. Xie H, **Li H**, et al. "Enhancement-mode AlN/GaN HEMTs on Si for RF applications." 11th International Workshop on Nitride Semiconductors (IWN 2022).

Awards:

1. Singapore International Graduate Award (SINGA)
2. The 14th International Conference on Nitride Semiconductors (ICNS-14) 2023 (November 12-17) at Fukuoka (Japan): "Best Student Award"

Chapter. 1 Introduction

1.1 Background and Motivation

Over the past decades, semiconductor technology has progressed through several distinct generations, each with advantages and its applications. First-generation semiconductors, primarily silicon (Si) and Germanium (Ge), have been extensively studied and commercialized, supported by well-established theoretical frameworks, mature fabrication technologies, and low manufacturing costs. These advantages have enabled their widespread adoption in highly integrated, cost-effective electronic systems. Subsequently, Second-generation compound semiconductors such as gallium arsenide (GaAs) and indium phosphide (InP) were developed, offering superior electron mobility, high-frequency performance, and low-noise characteristics. These properties made them suitable for high-speed and radiofrequency (RF) applications, including power amplifiers (PAs) and high-frequency communication systems. However, their relatively narrow bandgap and limited electron saturation velocity have imposed constraints on their ability to satisfy emerging requirements for higher power density, efficiency, and operating frequency in next-generation devices.

To address these limitations, third-generation semiconductors, particularly gallium nitride (GaN) and silicon carbide (SiC), have attracted significant attention over the past two decades due to their outstanding material properties. As shown in Table 1.1, GaN possesses a bandgap several times wider than Si, GaAs, and InP, along with a breakdown field strength nearly ten times higher, making it particularly suitable for high-voltage, high-power applications. Furthermore, the high breakdown voltage of GaN electronic devices significantly enhances circuit robustness. As a wide bandgap semiconductor, GaN exhibits intrinsic carrier concentrations far lower than first and second-generation semiconductor materials, allowing GaN devices to maintain very low leakage currents even when operating at high voltages. Additionally, heterojunctions formed between GaN and other III-V nitrides such as aluminum

Table 1.1 Material properties of common semiconductors at 300 K

	Si	GaN	AlN	GaAs	SiC
Bandgap (eV)	1.12	3.4	6.2	1.42	3.26
Dielectric constant (ε_r)	11.8	8.9	8.5	13.1	-
Electron mobility (cm^2/V.s)	1400	1200 (bulk) 2000 (2DEG)	300	8500	700
Breakdown field (MV/cm)	0.3	3.3	11	0.4	3
Thermal conductivity (W/cm. K)	1.5	1.3	-	0.5	4.9
Velocity (10^7 cm/s)	1	3	-	2	2
Lattice constant (Å)	5.43	3.19	3.11	5.65	3.08

nitride (AlN) can produce high-density two-dimensional electron gas (2DEG) with high electron mobility and high electron saturation velocity, making them ideal for microwave power applications.

The development of GaN technology began in 1969, when H. Maruska et al. first demonstrated the epitaxial growth of GaN single-crystal films. After more than over two decades of challenging research, M. Asif Khan et al. successfully fabricated the first AlGaN/GaN high-electron-mobility transistor (HEMT) in 1993 [1]. Soon after, this milestone was followed by the demonstration of microwave power capabilities in 1996, when Y. Wu et al. reported a power density of 1.1 W/mm and a power-added efficiency (PAE) of 18.6% at 2 GHz [2]. Though modest by today's standards, these early results laid the foundation for the rapid development of GaN RF devices.

In the years that followed, the power density, frequency, and efficiency of AlGaN/GaN HEMTs advanced dramatically. In 1997, Y. Wu et al. reported devices achieving 3.3 W/mm power density and 18.2% PAE at 18 GHz [3]. By 2001, J. Moon et al. achieved a cutoff frequency of 85 GHz and a maximum oscillation frequency of 140 GHz in devices with 2 μm source-drain spacing and 0.15 μm gate length, while also demonstrating 6.6 W/mm power density and 35% PAE at 20 GHz. [4]. In 2003, Y. Ando et al. increased device breakdown voltage to 160 V using gate field plate

structures for field flattening technology, measuring 10 W/mm power density and 47.3% power-added efficiency at 2 GHz. [5]. In 2004, Y. Wu et al. had further improved AlGaN/GaN device performance from 30 W/mm power density and 49.6% power-added efficiency at 8 GHz to a record-breaking 40 W/mm power density and 60% PAE at 4 GHz [6].

Significant advancements in millimeter-wave frequencies followed, with T. Palacios et al. reporting that GaN-on-SiC devices grown by Molecular Beam Epitaxy (MBE) with 0.16 μm gate length achieved 10.5 W/mm power density and 34% power-added efficiency at 40 GHz. [7]. In addition, in 2019, Harrouche et al. reported an AlN/GaN HEMT operating at Ka band, which achieved an output power of 8 W/mm under pulsed operation. [8]. These research advances have decisively demonstrated the power advantages of GaN RF devices, which enable higher power density, reduced module size, lower system costs, and improved system energy efficiency compared to GaAs and InP RF devices, thereby facilitating their rapid adoption in both military and civilian applications [9], [10], [11].

With the evolution of 5G and future communication technologies, devices increasingly need to provide higher output power density at higher frequencies within the millimeter wave spectrum, ranging from 24 GHz to 94 GHz and beyond. These advanced communication systems demand semiconductor materials capable of delivering reliable performance under challenging operating conditions, making GaN an especially promising candidate. [12], [13]. Although SiC substrates are widely used with GaN due to their high thermal conductivity, they face limitations in cost and supply availability. In contrast, Si substrates offer greater cost-effectiveness and are better suited for large-scale applications, presenting an important alternative for commercial deployment. [14].

Despite the promising attributes of GaN-on-Si technology, several challenges remain. Traditionally, thick buffer layers (several micrometers) have been used to reduce lattice mismatch between GaN and Si substrates; however, this approach degrades thermal dissipation and increases epitaxial wafer costs [15]. Moreover, conventional AlGaN/GaN high electron mobility transistor (HEMT) structures require thick barrier layers to achieve sufficient carrier density, which fundamentally limit device scaling

to higher frequencies. These thick barrier layers prevent effective gate length reduction and increase parasitic capacitances, ultimately constraining the maximum operating frequency of these devices [16].

To address these challenges, this work aims to develop submicron GaN technology on silicon substrates for high-frequency applications, specifically targeting the 5G market. By addressing current limitations while preserving the intrinsic performance advantages of GaN, this research seeks to unlock new opportunities for efficient, cost-effective RF front-end solutions in next-generation wireless communication systems. As 5G deployment intensifies and 6G research accelerates, envisioning terahertz frequencies and data rates reaching 1 bps by 2030—advancements in GaN technology will be critical for meeting the stringent requirements of future networks.

The global GaN RF device market is gaining substantial momentum, driven by increasing demand in telecommunications, defense, and satellite communications. According to Yole Group's 2024 forecast, the market is expected to reach $2 billion by 2029, highlighting its growing relevance in high-frequency, high-power applications. [17].

In telecom infrastructure, the shift from remote radio heads (RRH) to active antenna systems (AAS) is being accelerated by the global 5G rollout. This transition increases RF line density, thereby imposing stricter performance demands on PAs. GaN-on-SiC has become the mainstream solution due to its high-power density and superior thermal properties, with key industry players including Ericsson, Nokia, and Samsung actively deploying this technology. At the same time, RF GaN continues to penetrate defense applications, such as radar and electronic warfare, thanks to its robustness and wide bandwidth. Satellite communication systems have also embraced GaN for its compactness and high efficiency, crucial for weight- and power-constrained platforms.

While GaN-on-SiC currently dominates high-power markets, GaN-on-Si is emerging as a cost-effective alternative for low-to-moderate power RF front-ends. Its compatibility with mainstream CMOS processes and scalability to larger wafer sizes (6", with 8" and 12" under development) offer significant advantages for commercial

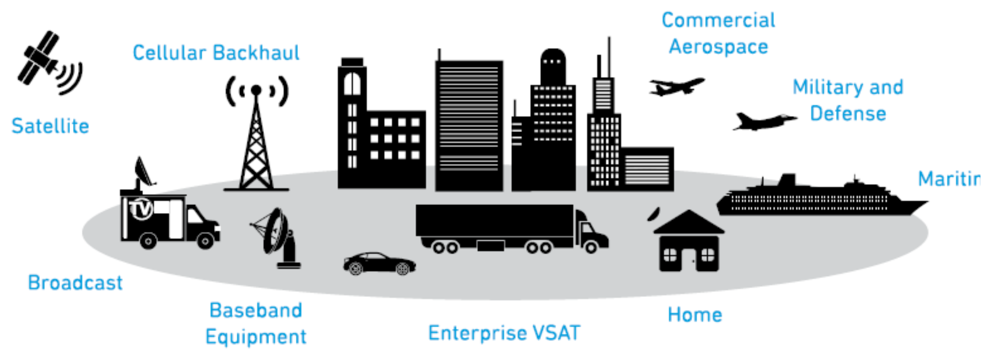


Fig. 1-1 GaN in satcom marketplace [18]

applications, such as sub-6 GHz small cells and massive MIMO (mMIMO) systems, where output power requirements are typically under 10 W.

The GaN-on-Si ecosystem is maturing rapidly. Companies such as STMicroelectronics, Infineon Technologies, and MACOM are developing GaN-on-Si products. Notably, MACOM's recent acquisitions have strengthened its capabilities across both GaN-on-Si and GaN-on-SiC platforms, ensuring competitiveness across telecom and satellite markets. Therefore, future telecom infrastructure is expected to rely more heavily on GaN-on-Si technology. This motivates the present work, which focuses on the development and characterization of GaN-on-Si RF devices optimized for low-voltage, high-efficiency operation in next-generation wireless systems.

Furthermore, GaN-based RF devices have rapidly established themselves as critical components in modern wireless communication systems and radar applications due to their exceptional performance characteristics (Fig. 1-1) [18]. The intrinsic material properties of GaN—including high electron mobility, wide bandgap leading to a high breakdown electric field, and excellent thermal conductivity —make it particularly highly suitable for high-power, high-frequency applications, where traditional silicon-based technologies face significant limitations [19]. In 5G networks, GaN HEMTs enable efficient power amplification across sub-6 GHz and millimeter-wave

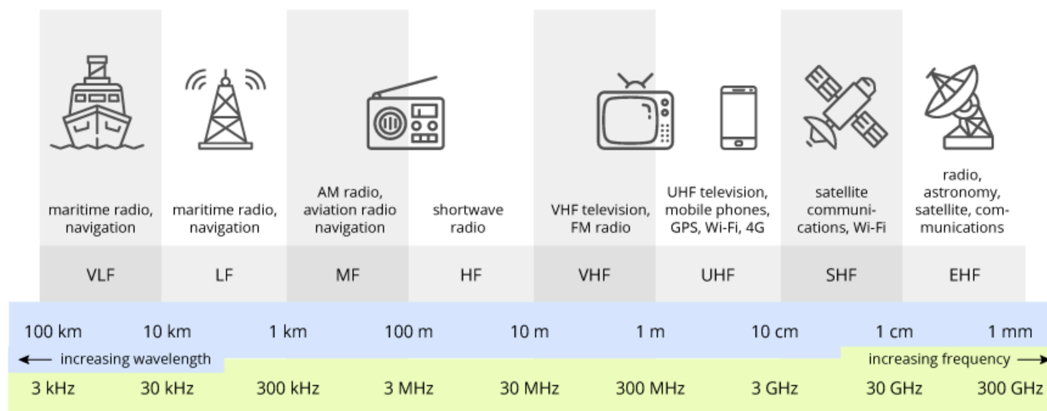


Fig. 1-2 Electromagnetic Spectrum Frequency Bands and Applications in RF Communications [23].

bands, supporting the high bandwidth and power demands of modern cellular infrastructure. [12].

The high thermal threshold and heat dissipation capabilities of GaN material make it ideal for withstanding the thermal stresses in mission-critical defense applications. Advanced radar systems, particularly active electronically scanned array (AESA) configurations, increasingly rely on GaN-based transmit/receive (T/R) modules to achieve enhanced detection range and resolution with reduced power consumption. [20]. In satellite applications, GaN's radiation hardness and high power efficiency are essential for payloads operating in the harsh environment of space. [21].

The RF GaN market is projected to grow at a compound annual growth rate (CAGR) of approximately 14% between 2021 and 2026, exceeding $2 billion in market value [22], driven primarily by global 5G infrastructure expansion, increased defense budgets, and the continued evolution of satellite communication systems.

Looking ahead, as technology nodes continue to scale, RF device development is pushing toward higher frequency platforms targeting Ku/K/Ka bands, with increasing interest in sub-0.1 μm nodes to enable sub-terahertz operation. These trends align with anticipated demands from future 6G applications. While GaN-on-Si platforms have shown promise for cost-effective deployment in sub-6 GHz small cell infrastructure, offering competitive efficiency and bandwidth at lower power levels,

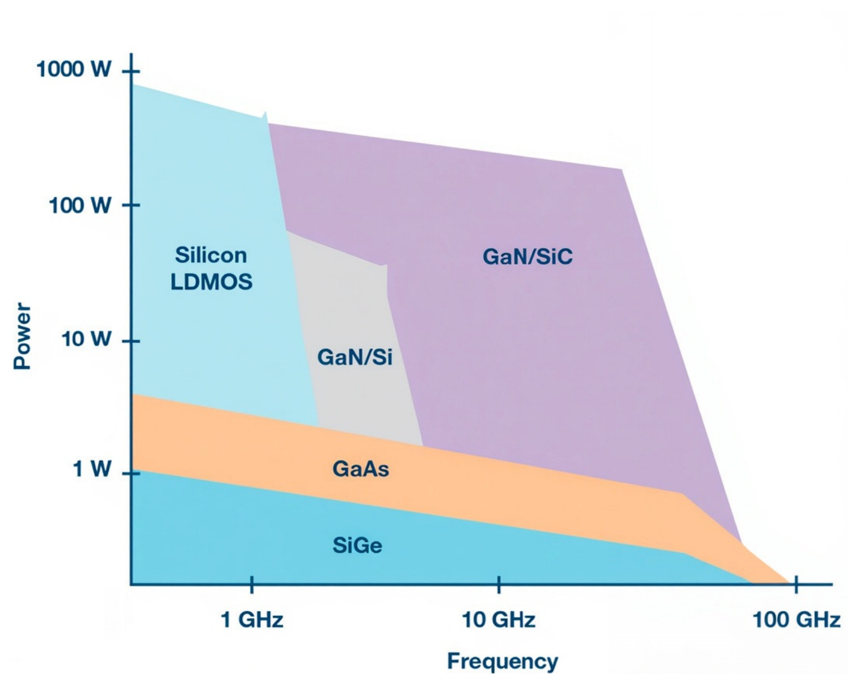


Fig. 1-3 Comparison of power density versus frequency for GaN devices compared to traditional Si and GaAs technologies in RF applications [25].

their integration into handset systems remains a longer-term objective due to stringent design constraints.

Currently, the commercial RF market spans several key frequency bands, as illustrated in Fig. 1-2 [23]. From VLF (3 kHz) maritime communications to EHF (300 GHz) satellite and astronomy applications, each band serves specific purposes based on its propagation characteristics. This spectrum allocation drives the development of specialized GaN RF devices optimized for different operational requirements across telecommunications, broadcasting, navigation, and aerospace sectors.

Driven by intensive R&D, GaN RF performance continues to improve. State-of-the-art GaN power amplifiers have demonstrated power densities exceeding 5 W/mm and power-added efficiencies (PAE) approaching 60% at 10 GHz in specific use cases [24]. Fig. 1.3 illustrates the comparison of power density versus operating frequency for GaN devices, highlighting their superiority over traditional Si LDMOS and GaAs technologies in RF applications [25].

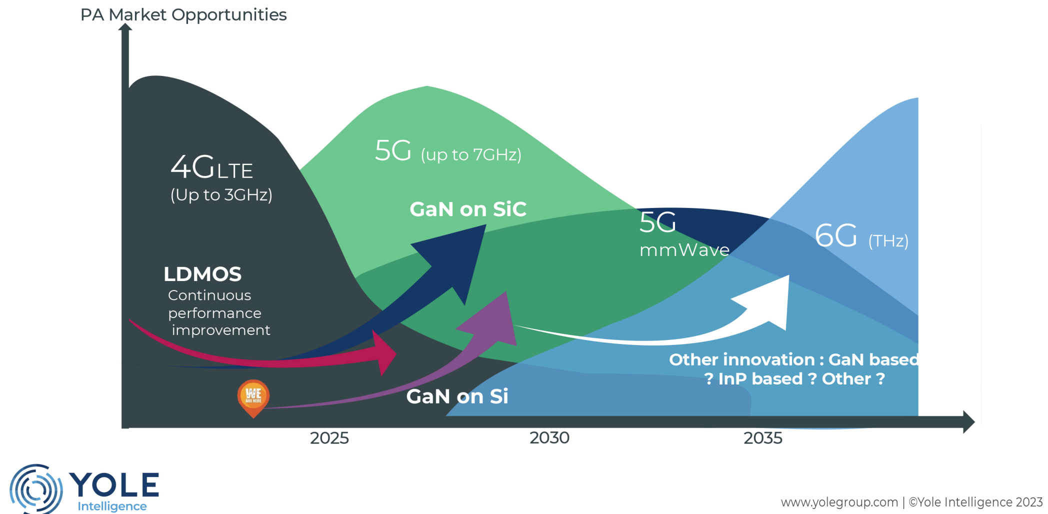


Fig. 1-4 Roadmap showing the projected evolution of GaN RF device technologies with performance metrics and timeline estimates [22].

Despite the significant progress in GaN RF technology, several challenges and research opportunities remain that could further enhance device performance. Key research areas include advanced epitaxial growth techniques to minimize defect densities in GaN-based heterostructures, which directly impact critical device metrics such as breakdown voltage, leakage current, and reliability. [26].

Fig. 1-4 Presents a roadmap outlining the projected performance metrics and technological evolution of GaN RF devices, indicating the ongoing trends toward higher frequency and power applications. To support next-generation RF systems, several emerging research directions are under exploration:

- N-polar GaN HEMTs: Compared to conventional Ga-polar counterparts, N-polar structures offer enhanced electron confinement and lower contact resistance. These characteristics enable superior high-frequency performance, making N-polar GaN a strong candidate for advanced 5G and future 6G applications [27], [28], [29], [30].

- Double-heterojunction AlGaN/GaN/AlGaN HEMTs: These structures improve carrier confinement and electron transport, with demonstrated benefits in linearity and efficiency over single-heterojunction counterparts [31], [32], [33], [34].
- Gate scaling and advanced lithography: Reducing gate length below 100 nm and optimizing device geometry are key to enabling efficient operation at frequencies approaching 300 GHz. Techniques such as e-beam lithography and self-aligned processes are under active development [35].
- Passivation and field plate engineering: To mitigate surface trapping effects and RF dispersion, novel passivation layers and field plate designs are being implemented, targeting improved stability and reliability under high-frequency operation [36].

Current research challenges for GaN RF devices include the development of improved processing techniques to reduce parasitic resistances, optimization of device structures to maximize frequency performance, implementation of effective thermal management strategies, and enhancement of long-term reliability [37].

Recent innovations in GaN-based MMICs (Monolithic Microwave Integrated Circuits) have further demonstrated the platform's integration potential. MMICs combining power amplification, switching, and low-noise functions on a single chip offer compact, efficient solutions for future RF front-end modules [38].

In summary, as technology matures, GaN is expected to play a central role in diverse emerging applications, including automotive radar, high-throughput satellite communication, and beyond-5G wireless networks. With its unique combination of high power, high frequency, and high efficiency, GaN remains a key enabler in meeting the evolving demands of advanced RF systems [39],[40].

1.2 Research Objectives

The main goal of this research is to develop, optimize and systematically characterize high-performance GaN HEMT technologies optimized for millimeter -wave power amplifier applications, with a specific focus on 5G FR2 frequency bands (24-52 GHz) and an extension toward higher-frequency operation for future wireless systems. As mm-wave communication becomes a key enabler for next-generation mobile and wireless platforms, power amplifiers are required to simultaneously deliver high output power, high efficiency, and robust linearity under increasingly stringent constraints on supply voltage, form factor, and manufacturing cost. While GaN-on-SiC technology represents the current benchmark for mm-wave performance, its high cost significantly limits its adoption in large-volume consumer applications. In contrast, GaN-on-Si technology offers a compelling pathway toward cost-effective and scalable integration, but faces intrinsic challenges related to substrate loss, thermal management, and high-frequency performance degradation. This research addresses these challenges through coordinated device design, epitaxial engineering, and parasitic-aware optimization, aiming to establish GaN-on-Si–based platforms suitable for low-voltage, high-frequency mm-wave power amplification.

A primary research objective is the development of novel AlN/GaN/AlGaN double-heterostructure (DH) HEMTs on Si substrates capable of delivering superior RF performance at frequencies relevant to 5G FR2 frequency range. As conventional GaN-on-Si HEMTs often suffer from increased knee voltage, degraded carrier transport, and limited efficiency when operated at reduced drain bias, this chapter focuses on leveraging the strong polarization fields and enhanced carrier confinement enabled by AlN-based heterostructures. Through careful epitaxial design and aggressive gate-length scaling, the work aims to achieve simultaneously high cutoff and maximum oscillation frequencies, high saturation current density, and strong transconductance, while maintaining efficient large-signal power performance at drain voltages of 5 V and below. Comprehensive DC, small-signal RF, and large-signal power characterization are employed to establish clear correlations between device structure and mm-wave performance, thereby defining practical design guidelines for GaN-on-Si HEMTs targeting 5G FR2 power amplifier applications.

This research further extends the GaN-on-Si HEMT platform developed for FR2 applications toward D-band frequencies (110–170 GHz), serving as a forward-looking exploration for future 6G and sub-THz communication systems. In this regime, at these frequencies, device performance becomes increasingly constrained by intrinsic carrier transit time, parasitic capacitances, and gate resistance, making conventional scaling approaches insufficient. The research investigates how targeted optimization of gate geometry, device layout, and parasitic components can enable GaN-on-Si HEMTs to achieve meaningful RF gain and output power at D-band frequencies despite the inherent limitations of silicon substrates. Experimental demonstration of D-band RF and power performance provides insight into the ultimate frequency limits of GaN-on-Si technology and identifies the dominant physical and technological bottlenecks that must be addressed for future sub-THz power amplifier applications.

Beyond transistor-based power amplification, multi-channel AlN/GaN heterostructures for Schottky barrier diodes (SBDs) as a complementary GaN device technology is investigated, which aimed at improving current handling and reducing sheet resistance. The objective of this chapter is to explore how vertically stacked AlN/GaN channels can increase total carrier density and current-carrying capability without relying on aggressive lateral scaling or complex three-dimensional device architectures. This work focuses on the design, fabrication, and electrical characterization of lateral multi-channel SBDs, with particular attention to current transport mechanisms, contact resistance, and reverse-bias behavior. By systematically evaluating the impact of channel stacking on diode performance, this chapter seeks to clarify the advantages and limitations of multi-channel GaN heterostructures and to provide device-level insights relevant to high-current and high-frequency power applications.

To address long-term scalability and integration challenges, this research further explores 200 mm GaN-on-Insulator (GaNOI) technology enabled by wafer bonding as a pathway toward CMOS-compatible GaN integration. Oxide-mediated wafer bonding offers a means to mitigate lattice mismatch and thermal stress issues associated with direct GaN-on-Si growth while enabling large-diameter substrates

suitable for high-volume manufacturing. The investigation examines the bonding process, material quality, and fundamental electrical characteristics of GaNOI structures, with particular emphasis on their suitability for RF and mm-wave device integration. By demonstrating the feasibility of transferring high-quality GaN epitaxial layers onto insulating substrates at the 200 mm wafer scale, this work establishes GaNOI as a promising platform for heterogeneous integration of GaN RF devices with silicon CMOS technologies.

In summary, this research advances GaN-based mm-wave device technologies through a comprehensive investigation spanning low-voltage GaN-on-Si HEMTs for 5G FR2 applications, frequency scaling toward D-band operation, multi-channel AlN/GaN Schottky diodes for enhanced current handling, and wafer-scale GaN-on-Insulator integration. By systematically addressing performance, scalability, and integration challenges, this work demonstrates viable pathways for GaN-on-Si and GaNOI technologies to meet the demanding requirements of next-generation wireless communication systems. The results presented in this thesis not only push the performance limits of GaN-on-Si platforms but also lay a solid foundation for future 6G and heterogeneous GaN–CMOS technologies.

1.3 Major Contributions

This dissertation achieves several groundbreaking contributions in the field of high-frequency GaN HEMTs, particularly in millimeter-wave power amplifiers and the application of GaN-on-Si technology:

1. **Heterostructure Design and Breakthrough in Low-Voltage RF Performance:**
   By employing an innovative AlN/GaN/AlGaN double heterostructure design, this research significantly enhances device performance under low-voltage RF operation. The optimized structure not only attains a maximum drain current of 1.9 A/mm and a maximum transconductance of 0.66 S/mm but also achieves f_T/f_{max} of 145 GHz/195 GHz. This breakthrough provides a low-power, high-performance solution that is ideal for mobile device integration.

2. **First Demonstration of Power Amplification for GaN-on-Si HEMTs in the D-Band:**
   Addressing the demands of 6G communication systems, this work is the first to demonstrate power amplification of GaN-on-Si HEMTs in the D-band (110–170 GHz). Utilizing a 140 nm gate-length AlN/GaN/AlGaN metal-insulator-semiconductor (MIS) HEMT, continuous-wave load-pull measurements at 123 GHz yielded a saturated output power of 0.67 W/mm and a maximum power-added efficiency of 5.3% (at a drain bias of 5 V). This success effectively expands the application range of GaN-on-Si technology into the sub-THz domain.

3. **Optimization of Multi-Channel Heterostructures and Schottky Barrier Diodes:**
   Through the growth of multi-channel AlN/GaN heterostructures via metal-organic chemical vapor deposition (MOCVD), the study achieves an exceptionally low sheet resistance of 69 Ω/□, attributed to a high sheet carrier density of 6.7×10^{13} cm^{-2}. This advancement establishes the technical basis for high-performance Schottky barrier diodes, resulting in a low turn-on

voltage (0.5 V), a minimal forward voltage drop (1.1 V), and a high current handling capability (1050 mA/mm).

4. **Innovation in GaN-on-Insulator (GaNOI) Technology and Substrate Integration:**
   By fabricating GaNOI structures using a 200 mm wafer bonding process, this research effectively mitigates the thermal management and electrical performance challenges inherent in traditional GaN-on-Si processes. X-ray diffraction and micro-Raman spectroscopy analyses confirm a reduction in lattice strain by approximately 5%, leading to a decrease in sheet resistance from 301 to 284 Ω/□. Furthermore, GaNOI HEMTs with a 120 nm gate length achieve a cutoff frequency as high as 96 GHz and demonstrate excellent integration with CMOS technology, paving the way for future on-chip integration of high-power and high-frequency RF functionalities.

5. **Optimization for 5G FR2 and Future 6G Applications:** For current 5G FR2 communication standards, devices have been optimized for low-voltage power amplification, achieving saturated output powers of 0.6 W/mm and 1.3 W/mm at drain biases of 3.5 V and 5 V respectively, with power-added efficiencies of 43% and 42%. These results set a benchmark for low-voltage, high-efficiency power amplifiers. Simultaneously, experimental validation at 123 GHz for 6G communication systems provides valuable insights and design guidelines for devices targeting the sub-THz frequency range.

6. **In-Depth Analysis of Device Current Transport Mechanisms:** Through temperature-dependent I–V measurements, the dissertation reveals that both thermionic emission and tunnelling mechanisms jointly govern current transport in multi-channel AlN/GaN Schottky barrier diodes. This in-depth analysis offers essential theoretical support for further optimizing device designs

1.4 Organization of the thesis

The organization of this thesis is outlined as follows:

Chapter 1 introduces the research field, providing background on semiconductor evolution, GaN technology development, and the rising demand for high-frequency devices in 5G/6G communications. It articulates the research objectives and key contributions.

Chapter 2 provides a structured overview of the operation principles, design optimization, and characterization techniques for GaN-based HEMTs targeting millimeter-wave applications. It begins with the fundamental principles governing GaN-based heterostructures, including polarization effects and carrier transport mechanisms. Next, it discusses key device design and fabrication strategies aimed at optimizing performance, particularly for GaN-on-Si platforms. The characterization methodologies section presents measurement techniques for device evaluation. DC and pulsed characterization approaches are detailed, followed by small-signal RF measurement procedures. A small-signal equivalent circuit model is presented that combines the conventional Angelov-based Small-Signal Model for HEMTs (ASM-HEMT) with Artificial Neural Network (ANN) techniques to extract intrinsic and extrinsic device behavior across a wide frequency range. The noise characterization section introduces a physics-based noise model for GaN HEMTs. Finally, large-signal power characterization methodologies are presented for evaluating HEMT performance at millimeter-wave frequencies.

Chapter 3 introduces a novel double heterostructure (DH) AlN/GaN/AlGaN-on-Si HEMT designed specifically for low voltage operation in 5G FR2 bands. The chapter begins with the design rationale and fabrication methodology of the proposed structure. It then presents characterization results, including DC parameters, RF small-signal metrics, large signal load pull performance and noise characteristics. The chapter proceeds to analyze the continuous-wave load-pull measurements at 30 GHz, highlighting the record-setting output power and efficiency achieved at low operating voltages. The correlation between saturation velocity, knee voltage, and power

amplification performance is examined in detail. The chapter concludes with a comparative analysis against state-of-the-art devices reported in literature.

Chapter 4 extends the investigation to higher frequency regimes, documenting the first demonstration of GaN-on-Si HEMTs for power amplification in the D-band. The chapter outlines the design modifications required to achieve operation at these frequencies. It presents the DC and RF characterization results, with particular emphasis on the load-pull measurements at 123 GHz. The chapter analyses the power-added efficiency and output power trade-offs at different bias conditions. The significance of this breakthrough for sub-THz 6G communication is discussed in detail, positioning GaN-on-Si as a viable technology for emerging wireless standards.

Chapter 5 shifts focus on Schottky barrier diodes (SBDs) based on multi-channel AlN/GaN heterostructures. The chapter begins with the rationale for multi-channel design and details the metal-organic chemical vapor deposition growth process. It then presents the electrical characterization results, highlighting the exceptionally low sheet resistance and high current-carrying capability achieved. The temperature-dependent current-voltage characteristics are analyzed to elucidate the underlying transport mechanisms. The chapter ends with a discussion on the implications of these findings for RF and power applications.

Chapter 6 explores an alternative substrate technology—GaN-on-Insulator (GaNOI)—for $In_{0.17}Al_{0.83}N$/GaN HEMTs. The chapter describes the 200 mm wafer bonding technique employed and presents material characterization results from X-Ray diffraction and micro-Raman spectroscopy. The impact of reduced lattice strain on device performance is analyzed through DC and RF measurements. The chapter concludes with a discussion on the potential for integrating GaN devices with CMOS technology on a single chip, highlighting the advantages for compact and efficient system design in future millimeter-wave applications.

Finally, Chapter 7 concludes the thesis by summarizing key findings and contributions while outlining promising directions for future research in GaN-on-Si technology for millimeter-wave and sub-THz applications.

Chapter. 2 Device Fabrication Technology and Characterization Methods

2.1 Polarization Effects and Operation Principles of GaN-Based Heterostructures

The exceptional performance of GaN-based High Electron Mobility Transistors (HEMTs) derives from the unique material properties of III-nitride semiconductors and the deliberate engineering of their heterostructures. These devices have demonstrated remarkable capabilities in high-frequency, high-power, and high-temperature applications, surpassing the theoretical limits of conventional silicon-based technologies. A thorough understanding of the fundamental physical principles underlying their operation is crucial to fully appreciate the advantages offered by GaN HEMTs. This section examines the polarization phenomena intrinsic to the wurtzite crystal structure and their consequential effects on device performance. The interplay between spontaneous and piezoelectric polarization in these materials creates the foundation for the distinctive operational behavior that makes GaN HEMTs particularly advantageous for next-generation electronic systems.

2.1.1 Structure Properties and Polarization Effects in GaN-Based HEMTs

Gallium nitride and related III-nitride compounds crystallize in the wurtzite structure, which fundamentally differs from conventional semiconductor materials like silicon (Si) or gallium arsenide (GaAs). As shown in Fig. 2-1(a), the wurtzite crystal structure of GaN is characterized by a hexagonal unit cell with distinct Ga-face (0001) and N-face (000-1) polarities[41]. The wurtzite structure's most significant feature is its lack of inversion symmetry along the c-axis, which contributes to a charge separation within each unit cell, resulting in spontaneous polarization (P_{SP}). At the microscopic level, this polarization arises from the formation of charge dipoles within each unit

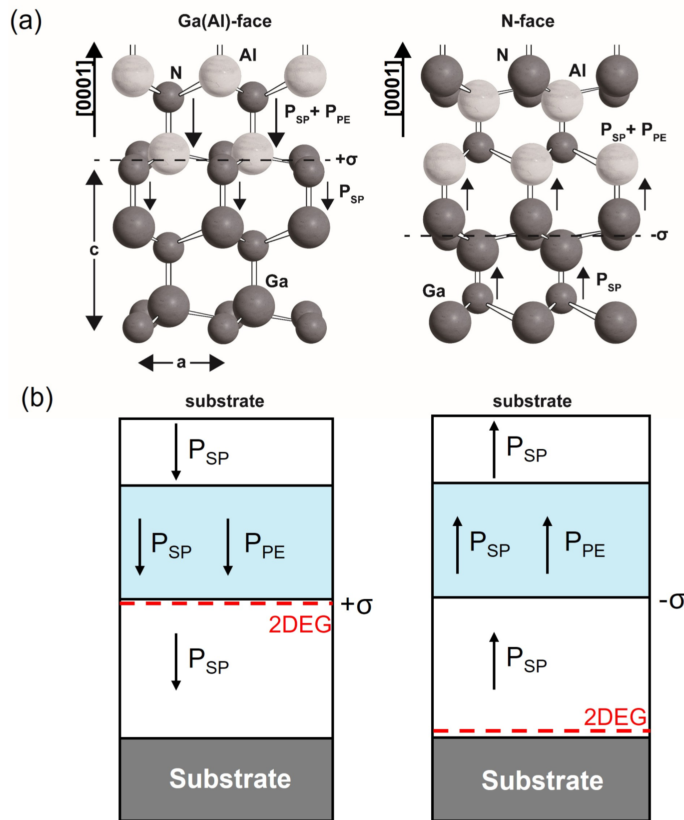


Fig. 2-1 (a) Diagram illustrating the atomic configuration within GaN wurtzite crystal lattice, depicting both Ga(Al)-face and N-face orientations; (b) Directional representation of P_{SP} and P_{PE} polarization in AlGaN/GaN heterostructures for both orientations, and the resulting polarization-induced interface charges.

cell. The Ga-N bond in GaN demonstrates partial ionic character, with electron density shifted toward the more electronegative nitrogen atoms. Simultaneously, the geometric arrangement of these atoms—with the Ga-N bonds not perfectly aligned along the c-axis—creates a net displacement between the centers of positive and negative charges. Consequently, each unit cell effectively behaves as a microscopic dipole, with positive and negative charges separated along the c-axis.

In the bulk material, these dipoles align and interact with adjacent dipoles, leading to internal charge compensation throughout the crystal interior. However, at material surfaces or interfaces, this neutralization cannot occur completely, resulting in net bound charges. These surface charges, generated through polarization effects, serve a fundamental function in determining the electrical characteristics of GaN HEMT devices.

2.1.2 Piezoelectric Polarization in AlGaN/GaN Heterostructures

The growth of an AlGaN layer upon GaN introduces an additional polarization mechanism arising from the lattice mismatch between these two materials. As illustrated in Fig. 2-1(b), this strain-induced polarization, known as piezoelectric polarization (P_{PE}), works in concert with spontaneous polarization to enhance the total polarization effect. The origin of piezoelectric polarization lies in two key factors: lattice mismatch and disparities in thermal expansion behavior between substrate materials and epitaxial films, which together generate piezoelectric charge carriers. The lattice constant of AlGaN decreases with increasing Al content, creating a mismatch when grown on a GaN buffer layer. During pseudomorphic growth processes, the AlGaN layer undergoes tensile strain because its in-plane lattice constant is constrained to match that of the underlying GaN layer.

This mechanical deformation alters the relative positions of atoms in the crystal structure, further separating the centers of positive and negative charges.

The piezoelectric polarization can be expressed as:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \quad (2.\ 1)$$

where e_{33} and e_{31} are piezoelectric coefficients, and ε_z, ε_x, and ε_y represent strain components along different crystallographic directions. For AlGaN grown on GaN, the in-plane strain increases proportionally with Al content, leading to stronger piezoelectric polarization at higher Al compositions.

Importantly, the direction of piezoelectric polarization depends on the growth polarity (Ga-face or N-face) and the type of strain (tensile or compressive). In conventional Ga-face growth, where the AlGaN layer experiences tensile strain, the piezoelectric polarization points in the same direction as spontaneous polarization, reinforcing the total polarization effect.

2.1.3 Formation of Two-Dimensional Electron Gas

The interplay between spontaneous and piezoelectric polarization at the AlGaN/GaN interface constitutes the fundamental mechanism behind the formation of the two-dimensional electron gas (2DEG) that enables HEMT operation. As illustrated in Fig. 2-1(b), both polarization components contribute to a polarization discontinuity at the heterojunction. This discontinuity brings about a sheet of bound positive charge along the AlGaN/GaN interface for Ga-face structures (or negative charge for N-face structures). This fixed polarization charge induces significant band bending at the heterojunction, causing the conduction band edge to form a triangular quantum well at the interface, where the band drops below the Fermi level as illustrated in Fig. 2-2 [42].

The system preserves charge neutrality as free electrons collect within this quantum well, establishing a high-density 2DEG. These electrons originate primarily from surface states or unintentional donor-like defects in the AlGaN barrier layer. One of

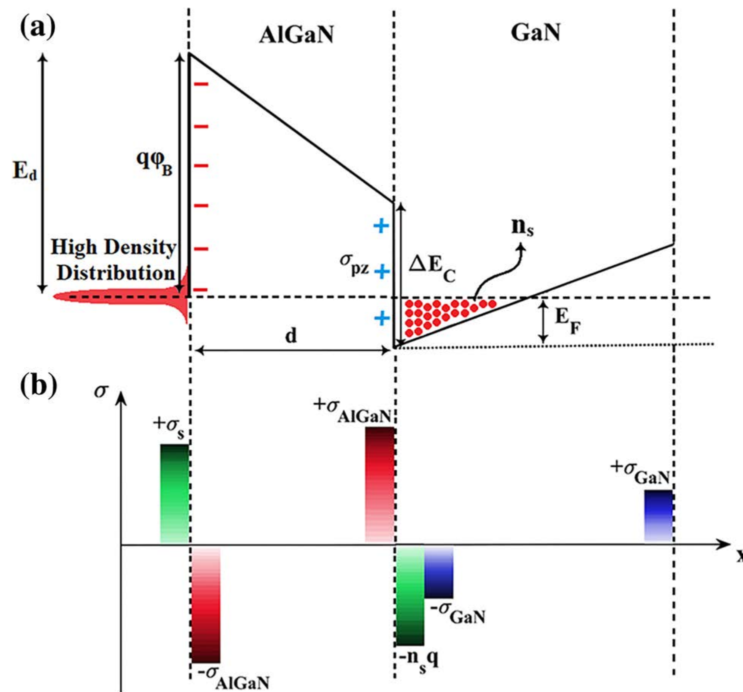


Fig. 2-2 (a) Energy-band diagram of AlGaN/GaN heterostructure. (b) Charge distribution at different interfaces, and formation of 2DEGwith electrons supplied by surface donor states [39].

the critical advantages of this polarization-induced 2DEG formation mechanism is that it does not rely on intentional doping, unlike conventional modulation-doped heterostructures in other material systems. This absence of dopants eliminates impurity scattering that would otherwise reduce electron mobility. As a result, AlGaN/GaN HEMTs achieve exceptionally high electron mobilities while maintaining high carrier densities, a combination that directly translates to superior device performance.

The depth of the quantum well and the resulting 2DEG density depend on several factors, including the Al composition in the barrier, the thickness of the $Al_xGa_{1-x}N$ layer, and the specific crystal orientation. Optimizing these parameters allows for precise engineering of device characteristics to meet specific application requirements.

2.1.4 2DEG Density and Device Characteristics

For typical AlGaN/GaN HEMTs, the 2DEG density (n_s) can be expressed by the following equation [43]:

$$n_s = \frac{\varepsilon_{AlGaN}}{qd}\left[V_{GS} - \left(\phi_b - V_{p2} + \frac{1}{q}E_{fi} - \frac{1}{q}\Delta E_c\right)\right] \quad (2.\ 2)$$

where ε_{AlGaN} is the AlGaN barrier dielectric constant, q represents the electron charge, d is the thickness of the AlGaN barrier layer, V_{gs} denotes the gate-source voltage, φ_b indicates the Schottky barrier height, E_{fl} represents the fermi level position relative to the channel layer's conduction band edge, ΔE_c is the conduction band discontinuity between AlGaN and GaN layer, and V_{p2} related to donors in the AlGaN and d_d is the doped barrier layer thickness.

$$V_{p2} = qN_d d_d^2 / 2\varepsilon_{AlGaN} \quad (2.\ 3)$$

Therefore, Equation (2. 1) can be simplified as

$$n_s = \frac{\varepsilon_{AlGaN}}{qd}(V_{GS} - V_T) \quad (2.\ 4)$$

The aluminum fraction within the AlGaN barrier layer plays a key role in determining polarization effects and electrical properties of AlGaN/GaN HEMTs. When Al content increases, the barrier layer develops a wider bandgap and generates an enhanced electric field that improves electron confinement in the quantum well. This deepening of the quantum well allows for greater electron confinement and higher 2DEG densities. Without any intentional doping, typical sheet carrier concentrations range from ~1×10^{13} cm^{-2} for $Al_{0.2}Ga_{0.8}N$/GaN structures to over 2×10^{13} cm^{-2} for AlN/GaN structures[44].

However, these benefits come with certain trade-offs. Higher Al content increases the lattice mismatch between AlGaN and GaN, potentially leading to greater strain and more structural defects. These defects can act as trapping centers and scattering sites, degrading carrier mobility and device reliability. Additionally, as Al content increases, the surface roughness of the AlGaN layer may worsen, further compromising electron mobility through increased interface scattering. Moreover, when using high Al content, the primary challenge becomes ohmic contact formation. The wider bandgap in high-Al-content AlGaN raises the Schottky barrier height at metal-semiconductor boundaries, increasing the difficulty of achieving low-resistance ohmic contacts. This increased contact resistance can negate some of the benefits gained from higher 2DEG density, particularly for high-frequency applications where parasitic resistances severely impact performance.

2.1.5 Operational Principles and Advantages of AlGaN/GaN HEMTs

The polarization mechanisms in heterostructures enable several key advantages that make these devices particularly well-suited for high-power and high-frequency applications. The high electron velocity in the 2DEG channel, coupled with reduced parasitic capacitances, enables operation at extremely high frequencies. The strong quantum confinement of electrons reduces out-of-plane scattering, while the high carrier density maintains sufficient current even as device dimensions shrink. Modern

AlGaN/GaN HEMTs have demonstrated excellent performance at millimeter -wave frequencies up to and beyond 100 GHz [45], [46], [47], [48].

During operation, an AlGaN/GaN HEMT exhibits three primary operating regimes:

1. Linear region: When a low drain-source voltage (V_{ds}) is applied with gate-source voltage (V_{gs}) above threshold voltage, current increases proportionally with V_{ds}. The 2DEG channel conducts uniformly across its length.

2. Saturation region: As V_{ds} increases, electron velocity near the drain reaches saturation, creating a pinch-off point. A depletion region forms beyond this point, expanding with increasing V_{ds}, while channel current remains relatively constant. This saturation occurs due to velocity saturation rather than channel pinch-off as in conventional GaN HEMTs.

3. Cut-off region: When V_{gs} falls below the threshold voltage, the 2DEG channel becomes fully depleted, turning the device off.

These operational characteristics, combined with the inherent material advantages of GaN technology, establish GaN HEMTs as leading candidates for next-generation power and RF technologies.

2.2 GaN HEMT fabrication process

The realization of high-performance GaN-based HEMTs requires precise fabrication techniques that preserve the intrinsic material properties while enabling optimal device operation. Following our understanding of the fundamental polarization effects and operational principles discussed in the previous section, we now turn our attention to the critical fabrication processes that translate theoretical device designs into functional transistors. Fig. 2-3 illustrated the conventional fabrication steps for AlN/GaN HEMTs using 5-layer mask sets. This section details the methodologies employed for device isolation, making low-resistance ohmic contacts, patterning gate electrode, and surface passivation— all crucial processes in developing GaN HEMTs

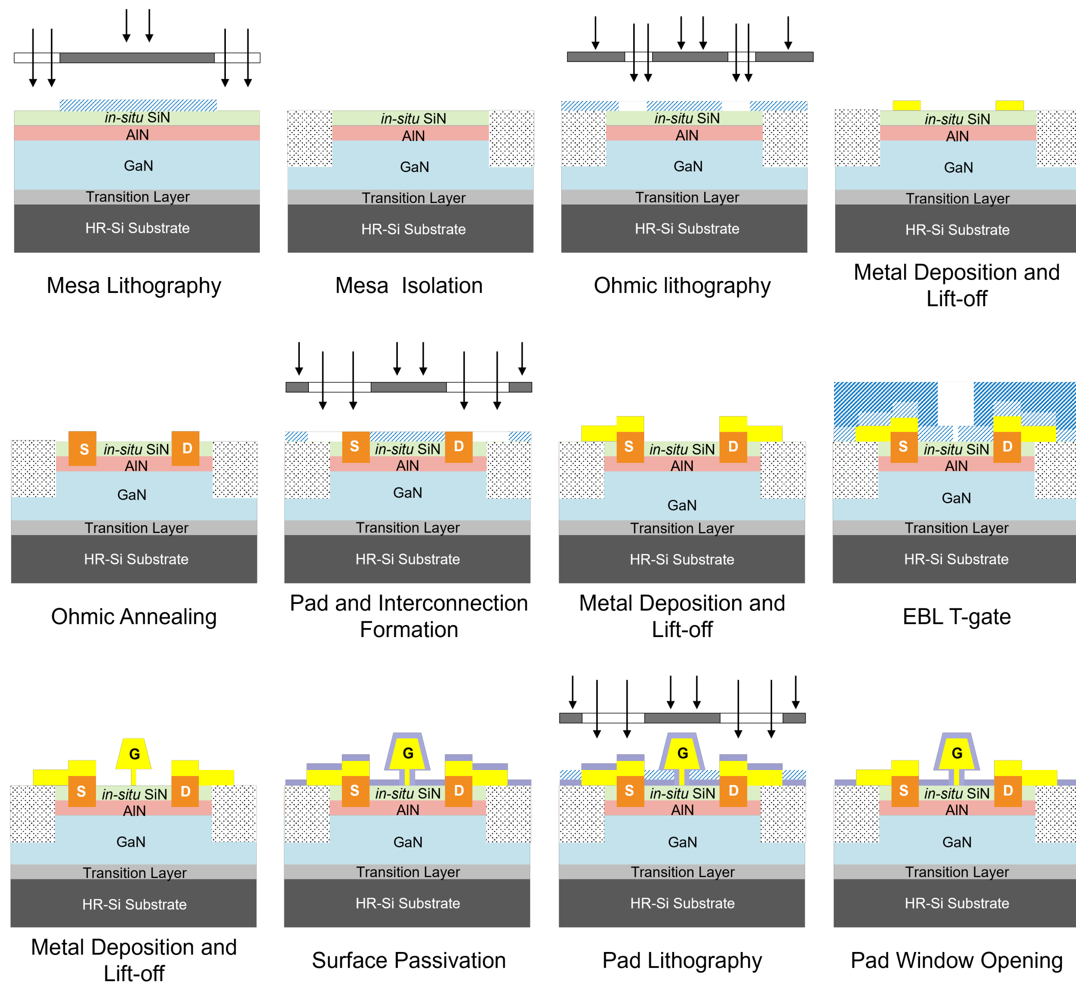


Fig. 2-3 The schematic of fabrication process flow for a deep-submirometre GaN HEMTs

that meet the tough standards for upcoming high-frequency and high-power technologies.

2.2.1 Mesa Isolation

Device isolation through mesa formation represents a fundamental step in our GaN-based HEMT fabrication process, serving to electrically separate the 2DEG connections between individual devices across the wafer. In our approach, we implement mesa isolation using inductively coupled plasma reactive ion etching (ICP-RIE) with BCl_3/Cl_2 gas chemistry, which offers precise control over the etching profile while maintaining acceptable etch rates. The process begins with thorough organic cleaning of the sample surface, followed by coating with AZ5214 photoresist and pattern definition using hard-contact UV photolithography. After developing the exposed mesa pattern areas with CD-26 developer, we perform ICP-RIE etching using optimized parameters of 10/20 sccm Cl_2/BCl_3 gas flow, 100/250 W RF forward power, and 100 mTorr chamber pressure.

While mesa etching offers a relatively straightforward isolation approach that has gained widespread acceptance among researchers, we have addressed potential challenges associated with this technique. The plasma etching process can potentially introduce damage to the mesa sidewalls, leading to degradation in device performance. Furthermore, when passivation layers directly contact the exposed 2DEG at the mesa edges, additional leakage paths may form, resulting in increased leakage current and non-uniform V_{BD} characteristics. To mitigate these effects, we systematically optimized our ICP-RIE process parameters, including precise control of RF power ratio, gas flow rates and etching depth. By reducing the ICP power from 300 W to 250 W while maintaining RF power at 100 W, we achieved a more controlled etch rate with reduced plasma-induced damage. Additionally, adjusting the Cl_2/BCl_3 flow ratio to 10/20 sccm provided optimal sidewall profiles with minimal roughness. The etch depth was carefully calibrated to extend 150 nm beyond the 2DEG layer, ensuring complete isolation while minimizing damage to the GaN buffer layer underneath.

Through optimization of our mesa etching process, we consistently achieve leakage currents below 1 μA/mm at a bias of 20V, meeting the requirements for high-performance GaN HEMT operation. This precise control over isolation characteristics proves essential for maximizing the power potential of our GaN technology by effectively managing leakage currents and mitigating the impact of high electric fields across the device structure. The high-quality mesa isolation achieved through our optimized process contributes to superior device performance, particularly in high-power RF applications where electrical isolation integrity becomes increasingly critical.

2.2.2 Ohmic Contact Formation

The performance of GaN-based electronic devices heavily depends on ohmic contacts, as their quality strongly affects device behavior. In our fabrication process, the creation of low resistance ohmic contacts begins with thorough cleaning of the mesa isolated wafer, followed by coating with AZ5214 photoresist. This photoresist is processed as a negative resist through a sequence of short exposure, 2-minute hard bake, and flood exposure, creating precisely defined windows for the ohmic contacts. After developing with CD-26 developer, the wafer undergoes descum treatment to eliminate resist residue, followed by buffered oxide etch (BOE) treatment to remove any native oxide layers that might compromise contact quality. The ohmic metal stack consisting of Ti/Al/Ni/Au is then deposited using e-beam evaporation, with the metal thickness carefully calibrated to ensure optimal performance. Following deposition, a lift-off process in acetone removes excess metal, leaving behind well-defined contact patterns. The final step involves rapid thermal annealing (RTA) at 775°C for 60 seconds, facilitating the formation of low-resistance ohmic contacts through solid-phase reactions between the metal layers and the semiconductor.

To evaluate the quality of the fabricated ohmic contacts, Transmission Line Method (TLM) is used to provide a standardized approach for extracting contact resistance (R_c) and sheet resistance (R_{sh}). As shown in Fig. 2-4 (a), the TLM patterns consists of contact pads with increasing spacing between them (d_0 = 3μm, d_1 = 6μm, d_2 = 9μm,

$d_3 = 12\mu m$, $d_4 = 15\mu m$), where W represents the contact width. Fig. 2-4 (b) illustrates the on-wafer testing configuration for these structures, where the R_{sh} is calculated from the fitted line's slope, while the R_c is derived from the intercept on the y-axis. The fundamental principle of TLM involves measuring the total resistance between

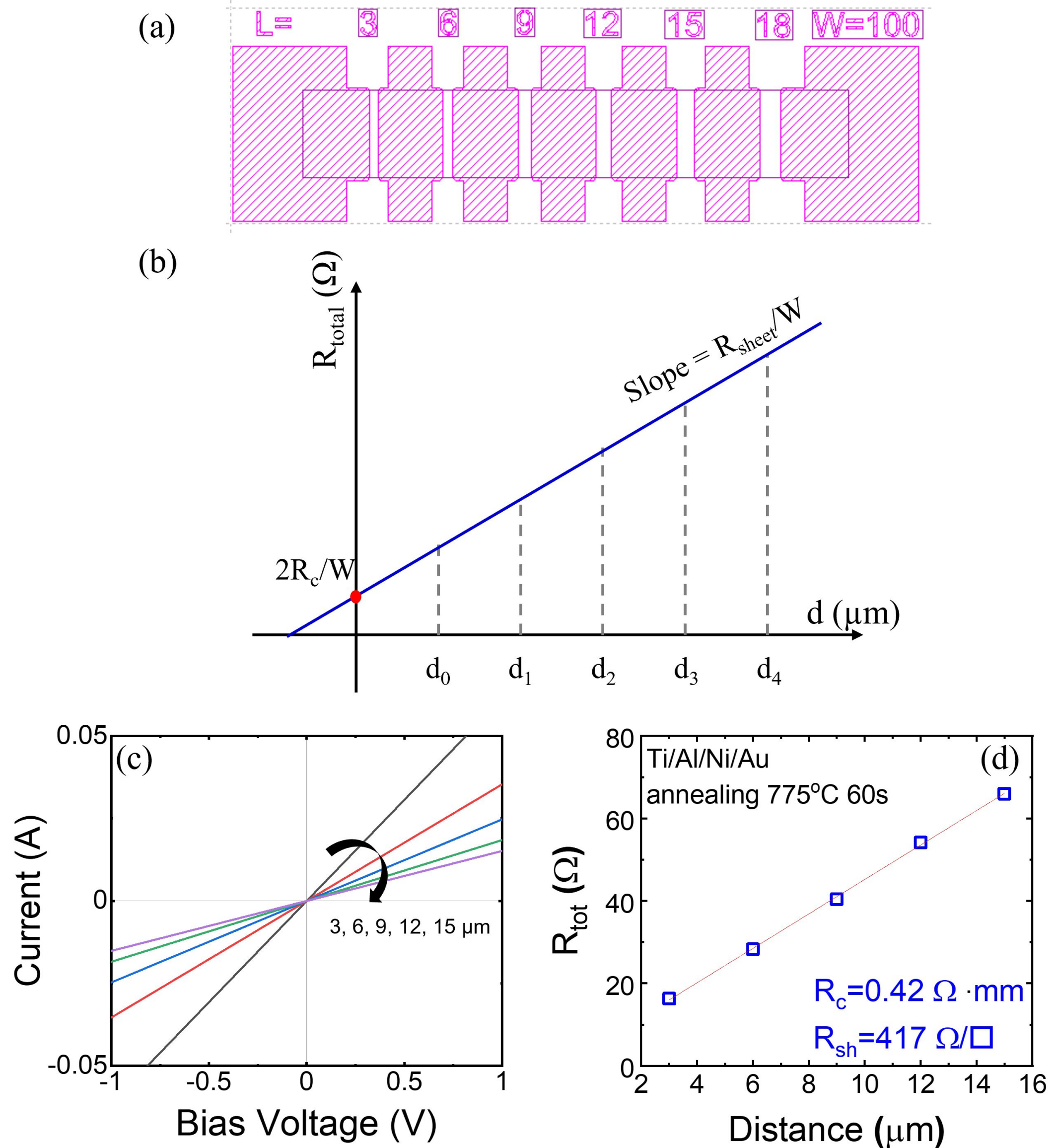


Fig. 2-4 (a) Schematic diagram of the Transmission Line Method (TLM) test structure, (b) Plot showing the relationship between total resistance to TLM pad spacing d and width w, (c) Current-voltage (I-V) measurements from the TLM structures, (d) Plot of the total resistance R_{tot} versus distance, used for extraction of contact resistance and sheet resistance for metal contacts annealed at 775 °C

adjacent ohmic pads separated by different distances. The measured resistance represents the sum of two ohmic contact resistances and the GaN channel resistance in series. The total resistance (R_{tot}) between contacts can be expressed as

$$R_{tot} = \frac{2R_c}{W} + \left(\frac{R_{sh}}{W}\right) \cdot d \quad (2.5)$$

where R_c represents the contact resistance, R_{sh} indicates the sheet resistance, and d is the spacing between contacts.

GaN-based devices usually have ohmic contacts made through metal alloying methods. This approach uses deposited metal stacks (commonly Ti/Al/Ni/Au) that undergo high-temperature annealing, as demonstrated in our study with annealing at 775°C for 30s. Fig. 2-4(c) displays I-V characteristic confirming the linear behavior that defines true ohmic contacts. Through plotting total resistance values against contact spacing d, in Fig. 2-4(d), a linear relationship is established., R_c and R_{sh} can be extracted through linear fitting of this data:

More recently, regrown n^+-GaN ohmic contacts using Molecular Beam Epitaxy (MBE) have emerged as a promising technology to reduce parasitic access resistances in GaN devices. This method creates a direct connection between heavily doped n^+-GaN and the 2DEG layer, resulting in much lower resistance at the interface. Regrown contacts are particularly advantageous for deeply scaled device designs requiring reduced gate-to-source distances, resulting in excellent high-frequency performance. Several studies have reported exceptional ohmic contacts using the regrowth approach, achieving R_c as low as 0.05 Ω·mm [49]. Despite these impressive results, it should be noted that the regrowth method introduces additional process complexity and increases manufacturing costs, potentially limiting its suitability for large-scale foundry processes.

Future work in our laboratory will explore alternative approaches such as recessed and ion implantation techniques to further reduce contact resistance and enhance overall device performance.

2.2.3 T-gate Formation Technology

The gate electrode geometry profoundly influences both DC and RF performance of GaN HEMTs. However, the maximum oscillation frequency (f_{max}) for HEMTs with a rectangular gate is limited by high gate metal resistance. T-shaped gate technology has become widely implemented in RF GaN HEMTs to address this limitation, as this configuration provides low resistance while maintaining short gate foot geometries critical for high-frequency operation.

Electron beam lithography (EBL) is widely regarded as one of the most effective exposure techniques for T-gate fabrication, particularly for sub-100-nm gate definition. This study involves the optimization of the T-gate profile which is defined by VISTEC EBL system using a bi-layer electron beam resist patterning and single exposure technology. The principal steps include initially spin-coating a low-sensitivity photoresist on the substrate, followed by spin-coating a high-sensitivity photoresist layer.

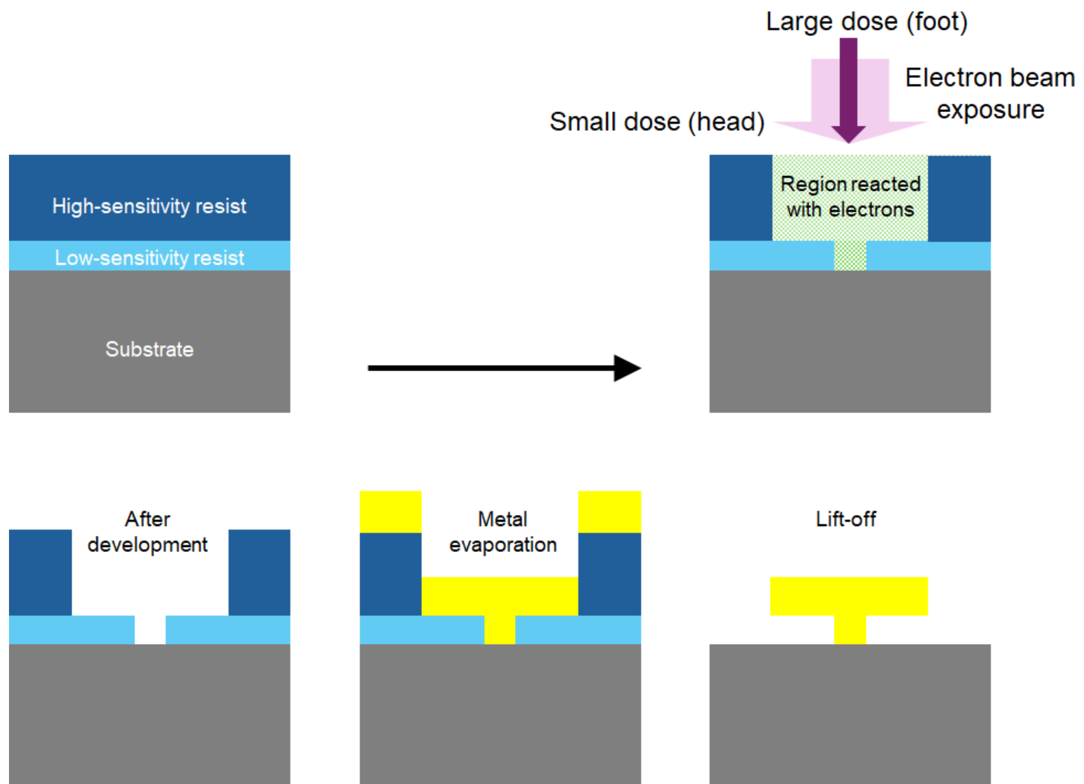


Fig. 2-5 Overview of the Bi-layer T-gate Fabrication Process

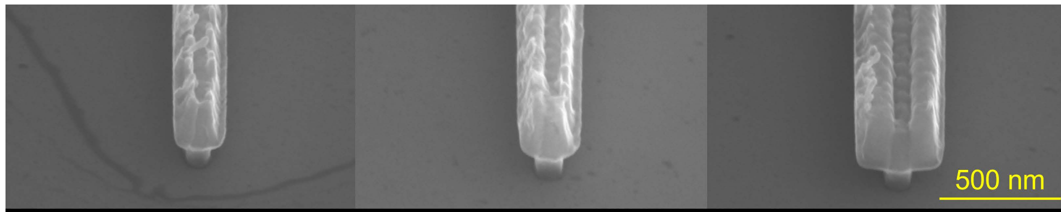


Fig. 2-6 SEM images of T-gate structures fabricated using a PMMA/PMMA-MAA bi-layer resist process. All three devices have the same gate length (foot width of 120 nm) defined by an exposure dose of 1300 μC/cm², while the gate head widths differ (≈ 300 nm, 350 nm, and 500 nm) due to the 3–4× sensitivity ratio between PMMA and PMMA-MAA resists. The variation in gate head width is intentionally controlled through resist undercut and development conditions. All images are shown at the same scale.

In contrast to grayscale or proximity-effect-based patterning approaches, the sensitivity difference between the two resist layers should be maximized to ensure a pronounced linewidth contrast between the gate head and gate foot. Subsequently, electron beam exposure is performed, followed by development in a MIBK: IPA (1:3) solution. This developer selectively enhances the differential dissolution rates between the two resist layers, enabling the formation of a well-defined T-shaped photoresist profile. The sample is then rinsed in IPA and gently dried with nitrogen. Subsequently, metal evaporation and lift-off processes are carried out, resulting in a T-shaped metal gate, as illustrated in Fig. 2-5.

When the gate length of the T-gate is scaled down to approximately 120 nm, control of the T-gate morphology becomes particularly crucial. Although approaches utilizing sensitivity differences between electron beam resists for T-gate morphology fabrication are widely employed, this section specifically investigates the minimum achievable gate foot dimensions using PMMA/PMMA-MMA bilayer resist combinations under single electron beam exposure.

The sensitivity ratio between PMMA and PMMA-MAA photoresists is 3-4-fold as shown in Fig. 2-6, at an exposure dose of 1300 μC/cm², the PMMA/PMMA-MAA foot width measures 120 nm, while the gate head widths are 300 nm, 350 nm, and 500 nm respectively. Increased electron scattering within the resist stack, including both forward scattering and backscattering effects, inevitably contributes to additional exposure in the underlying gate foot region. This effectively increases the

local exposure dose and leads to gate foot linewidth broadening. Although simulations predict a theoretical gate length of approximately 80 nm in PMMA photoresist, practical fabrication results are strongly influenced by resist chemistry, exposure conditions, and development parameters. Consequently, bilayer resist systems employing single-exposure processes typically yield PMMA gate foot linewidths on the order of 120 nm. Following exposure and development, Schottky gate formation is completed by electron beam evaporation of Ni/Au (30/420 nm), followed by a lift-off process.

2.2.4 Passivation Techniques

Surface passivation layer optimization plays a crucial role in GaN HEMT device performance, particularly for millimeter-wave applications where reliability and stability are paramount. Traditional passivation approaches often face limitations in simultaneously addressing several performance metrics such as surface leakage, breakdown voltage, and current collapse. In our work, a layer of Al_2O_3 is deposited as a passivation layer to minimize surface states and parasitic capacitance. The exposed areas between source and drain electrodes commonly exhibit surface defects that compromise both direct current and radio frequency capabilities of GaN HEMTs. The origin of these surface states includes damage from fabrication-related damage, dangling bonds on the semiconductor surface, or external contaminants.

Various dielectrics can suppress surface states, including Si_3N_4, SiO_2, and Al_2O_3. Among these, Al_2O_3 offers excellent passivation properties with high dielectric constant and good thermal stability. In this work, 10 nm of Al_2O_3 deposited by atomic layer deposition (ALD). After conventional Acetone/IPA cleaning and removal of the native oxide layer by HF acid, the wafer was loaded into the ALD chamber. First, a 5-cycle water treatment was performed to introduce surface hydroxyl groups, leading to improved nucleation, resulting in high-quality dielectric films with low interface trap density, excellent gate control, and superior electrical performance [50]. Each TMA cycle consisted of a 0.05 s TMA pulse followed by a 20 s N_2 purge at 250°C. Subsequently, Al_2O_3 was deposited using alternating pulses of TMA and H_2O at

250°C with a chamber pressure of 200 mTorr. Each ALD cycle (0.05 s TMA pulse / 20 s N_2 purge / 0.05 s H_2O pulse / 20 s N_2 purge) resulted in approximately 0.1 nm/cycle growth rate. After finishing 100 deposition cycles to achieve a 10 nm Al_2O_3 coating, contact access windows were defined using photolithographic techniques and then opened via BOE wet processing to enable electrical measurements.

Additionally, our passivation approach can be extended beyond Al_2O_3 to other dielectric materials such as HfO_2 and TiO_2 [51]. Moreover, bilayer Al_2O_3/SiN_x stacks have demonstrated effectiveness in restraining dispersive effects [52], providing flexibility for different device architectures and application requirements. Different passivation methods enable targeted optimization strategies for specific device designs and operating conditions.

2.3 Device Characteristics Methods

2.3.1 DC Characteristics

DC characteristics of fabricated GaN HEMTs are typically evaluated using precision semiconductor parameter analyzers such as the Agilent B1500A. The fundamental output characteristics demonstrate a distinctive relationship between drain current (I_d) and drain bias (V_d) at fixed gate voltages. At low drain biases, the current exhibits a linear relationship with voltage, following Ohm's law. The gradient of this linear section gives the on-resistance (R_{on}), which encompasses multiple resistance components including contact resistance at the electrodes, drain and source access resistance, and channel resistance.

As the drain bias increases, the I_d eventually reaches saturation, a regime where the current becomes relatively independent of further increases in drain voltage. This saturated current level is primarily regulated by the gate bias, as the gate electrode adjusts the carrier concentration within the 2DEG channel. This relationship illustrates the fundamental field-effect operation principle of HEMTs.

Transfer characteristics measurements—plotting drain current against gate voltage—provide additional critical information about device performance. Using the linear extrapolation method at maximum transconductance, we determine the threshold voltage (V_{th}). Transconductance (g_m), which represents the ratio between drain current change and gate bias change ($\partial I_d/\partial V_g$), serves as a key indicator of the gate's ability to modulate channel conductivity and directly correlates with high-frequency performance potential.

For devices with submicron gate lengths, the intrinsic transconductance ($g_{m,\,int}$) can be approximated as:

$$g_{m,int} \approx \frac{W \cdot v_{sat} \cdot \varepsilon}{d} \tag{2. 6}$$

where W represents the transistor width, v_{sat} represents the electron saturation velocity, ε is the dielectric constant, and d is the distance between the gate electrode and the 2DEG (approximately equivalent to the barrier layer thickness).

This relationship highlights a critical design trade-off in GaN HEMTs. Reducing the barrier thickness enhances transconductance but simultaneously decreases the 2DEG sheet carrier density (n_s). To mitigate this compromise, researchers have increasingly focused on materials with stronger polarization fields, transitioning from conventional AlGaN barriers to high-Al-content alternatives such as InAlN, InAlGaN, and AlN. These materials maintain high carrier densities even with reduced barrier thicknesses, optimizing both transconductance and channel conductivity.

2.3.2 Pulsed iv characteristics

While DC measurements provide valuable baseline characterization, they cannot fully capture dynamic device behaviors, particularly those related to trapping phenomena and self-heating effects that significantly impact real performance. Pulsed I-V measurements address these limitations by applying short voltage pulses to minimize thermal effects and reveal trap-related phenomena.

In this work, pulsed I-V characteristics were implemented using DIVA pulsed I-V system and Focus Auriga's pulsed I-V systems. The measurement sequence typically involves setting the device to the specified quiescent bias condition for the measurement cycle, briefly pulsing to measurement bias points to capture the I-V characteristics, returning to the quiescent condition, and repeating multiple measurement points to construct complete I-V curves. The analysis of these measurements provides valuable insights into device physics and informs strategies for mitigating trapping effects that can limit device performance in RF and power switching applications operating in the moderate voltage range.[53], [54].

To identify and quantify trapping effects that impact transistor performance, pulsed I-V measurements are conducted using several quiescent bias points. During these measurements, gate and drain terminals receive pulses from specific quiescent bias points ($V_{gs,q}$, $V_{ds,q}$). To minimize self-heating while focusing on trapping phenomena, the on-state pulse width remains brief (500 ns) compared to the significantly longer off-state duration (5 ms). The relationship between pulse width and period, referred to as duty cycle, maintained at approximately 1%.

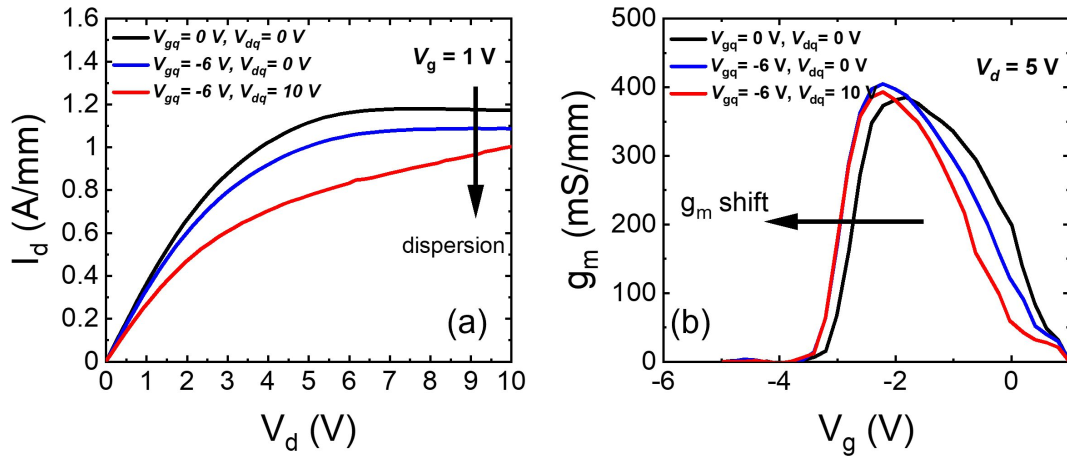


Fig. 2-7 Detailed drain voltage biasing conditions in above pulsed I-V measurement. (a)Pulsed I_d-V_d and (b) I_d-V_g measurements with cold quiescent, gate lag and drain quiescent conditions are plotted.

A systematic approach employing specific trapping-focused pulsed I-V measurements based on I_d-V_d and I_d-V_g characteristics has been established using distinct quiescent bias conditions:

1. Cold condition ($V_{gs,q}$ = 0.0 V, $V_{ds,q}$ = 0.0 V): This approach minimizes self-heating by maintaining the device in an unbiased state throughout most of the measurement cycle, providing reference I-V characteristics that approximate isothermal conditions.

2. Gate-lag quiescent condition ($V_{gs,q} < V_{th}$, $V_{ds,q}$ = 0.0 V): This configuration promotes electron trapping primarily in the gate region: (i) surface trapping and (ii) trapping under the gate Fig. 2-8 [8]. During this off-state operation, electric fields penetrate the GaN buffer layer, elevating the quasi-Fermi level above specific trap energy states. This mechanism becomes particularly significant when gate leakage current provides electrons that populate buffer traps[55].

3. High V_{ds} (Drain-lag) quiescent condition ($V_{gs,q} < V_{th}$, $V_{ds,q}$ = high voltage): This indicates gate electrons tunneling to the surface and channel electrons being excited, both of which can readily become trapped within the buffer. The resulting threshold voltage shifts manifest primarily when sufficient field

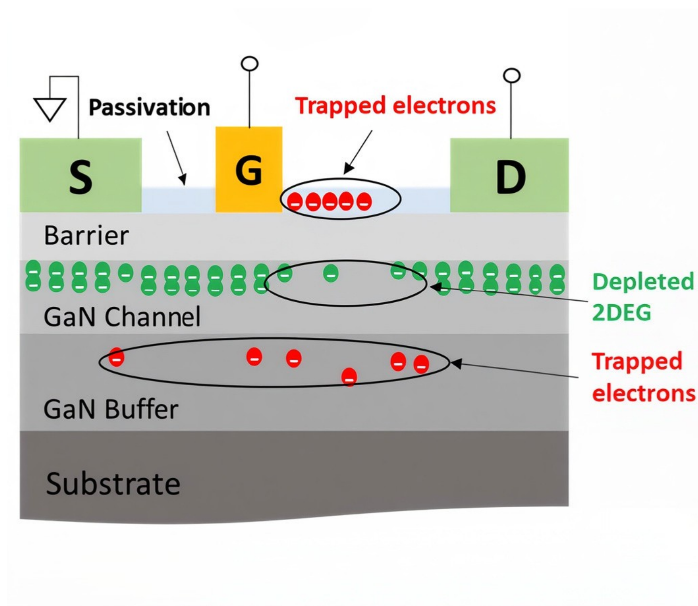


Fig. 2-8 Schematic cross section of AlN/GaN HEMT, showing electron trapping location [8].

penetration occurs in the GaN buffer and maintains proportionality with drain voltage within moderate bias ranges.

Pulsed I_d-V_g and I_d-V_d measurements provide complementary perspectives on trap-related phenomena in GaN HEMTs through gate lag and drain lag characterization, as illustrated in Fig. 2-7. Gate lag measurements reveal that buffer traps manifest as positive threshold voltage shifts in pulsed I_d-V_g characteristics, indicating charge capture in the buffer layer affecting channel control. Conversely, surface traps primarily manifest as reduced maximum transconductance peaks, signaling degraded carrier transport efficiency at the AlGaN/GaN interface. Therefore, pulsed I_d-V_d measurements quantify current collapse phenomena, dynamic R_{on} degradation, and self-heating effects under various bias conditions. The combination of these characterization approaches enables comprehensive trap analysis by differentiating between surface-dominated and buffer-dominated trapping mechanisms, providing essential information for developing mitigation strategies to enhance GaN HEMT performance and reliability

2.3.3 Small Signal RF Characteristics and Modelling

The exceptional material properties of GaN HEMTs have made them primary candidates for high-frequency, high-power applications. These devices have maintained research prominence since their 1990s breakthrough, driven by their key advantages: extensive bandgap, superior electron mobility, enhanced thermal conductivity, and beneficial relative permittivity.

To properly evaluate the radio frequency (RF) capabilities of GaN devices, two fundamental figures of merit are widely employed: cutoff frequency (f_T) and maximum oscillation frequency (f_{max}). The cutoff frequency represents the frequency at which the small-signal current gain drops to unity when the device operates in a common-source configuration. More precisely, f_T is defined as the highest operating frequency at which the output alternating current equals the input alternating current, marking the limit of the device's current amplification capability. While f_{max} provides insight into the device's power handling capabilities at high frequencies. This parameter refers to the maximum frequency where the unilateral power gain (G_u) becomes equal to unity under conditions where there is no feedback from load to source and both terminals are perfectly impedance matched. Together, these metrics establish the upper boundaries of a device's frequency performance and serve as essential benchmarks for comparing different technologies and device designs.

Microwave small-signal measurements were conducted using the Keysight N5244-A PNA-X Network Analyzer system. The system combines DC bias voltage generated from the Agilent B2900A source with the high-frequency low-magnitude signals of

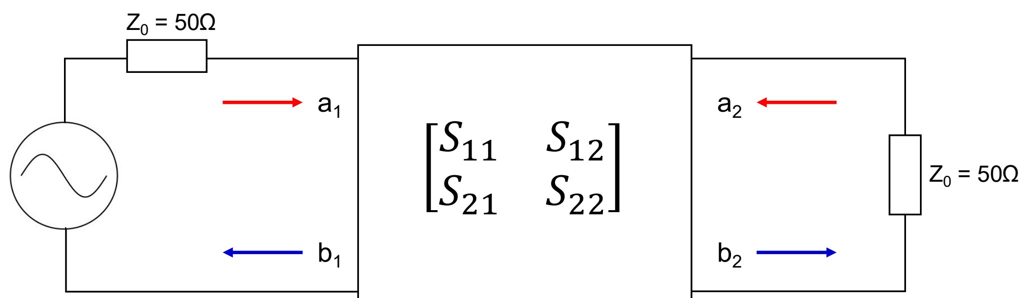


Fig. 2-9 S-parameters of 2-port network with arbitrary source and load impedances

the VNA through the network analyzer's internal bias circuitry. This integrated signal is subsequently transmitted to the device under test (DUT) via microwave probes featuring a 150 μm round-Signal-Ground (GSG) geometry.

In small-signal characterization, GaN HEMTs operate as two-port networks connected to source (Z_S) and load (Z_L) impedances. The RF behavior is characterized by a 2×2 matrix of S-parameters, where S_{11} and S_{22} represent input and output reflection coefficients when the opposite port is terminated with the characteristic impedance Z_0. Parameters S_{21} and S_{12} correspond to forward and reverse transmission coefficients, respectively. These S-parameters are conventionally referenced to a characteristic impedance of $Z_S = Z_L = Z_0 = 50\ \Omega$, though they can be converted to other high-frequency parameters such as impedance (Z) or admittance (Y) parameters for specific analysis requirements.

Accurate device characterization requires elimination of the influence of measurement system, such as cables, adapters, and internal VNA components. Prior to S-parameter measurements, the measurement reference planes at the probe tips are established through implementation of a typical Short-Open-Load-Through (SOLT) calibration methodology, eliminating systematic errors from cables, adapters, and internal VNA components.

However, the fabricated device incorporates both intrinsic and extrinsic elements. The interconnect pads and access regions introduce parasitic resistance, capacitance, and inductance that must be accounted for to isolate the intrinsic device behavior. This necessitates the fabrication of dedicated "open" and "short" test patterns on the same wafer for precise de-embedding:

1. The "open" structure, consisting of metal pads without the active device region, enables extraction of parallel parasitic capacitances.
2. The "short" calibration structure, characterized by source and drain electrodes connected through a metallic conductor, facilitates extraction of series parasitic resistances and inductances.

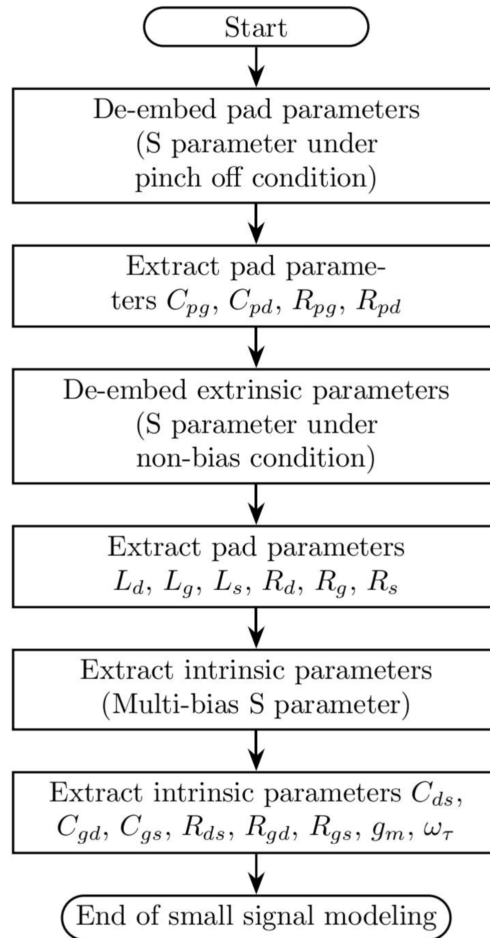


Fig. 2-10 Schematic flowchart of the S-parameter extraction and de-embedding procedure for isolating intrinsic device characteristics.

Fig. 2-10 illustrates the comprehensive S-parameter extraction and de-embedding methodology, which effectively removes these parasitic effects, yielding accurate intrinsic S-parameters that represent the active device region.

By analyzing the de-embedded S-parameters, several important figures-of-merit can be derived to assess the maximum achievable RF performance of the GaN HEMT technology:

Short-circuit current gain (h_{21}) calculation from S-parameters follows:

$$h_{21}(f_T) = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} = 1 \quad (2.7)$$

As frequency increases, current gain reduces primarily due to gate and drain coupling directly through gate-drain capacitance. Therefore, extraction of f_T involves fitting the de-embedded h_{21} data with a -20 dB/decade slope in the lower frequency range and determining the intersection point with the frequency axis.

Maximum oscillation frequency represents the frequency point at which unilateral gain (U) in a two-port network reaches unity. Unilateral gain, introduced by Mason in 1954 [56], represents the maximum achievable power gain when the device is unilaterally configured. It is determined under conditions of conjugate matching at both input and output ports, while mitigating the influence of gate-drain capacitance feedback.

Mason's formulation allows for direct calculation of unilateral gain using the measured S-parameters:

$$U(f_{max}) = \frac{\left|\frac{S_{21}}{S_{12}}-1\right|^2}{2k\left|\frac{S_{21}}{S_{12}}\right|-2\Re\left(\frac{S_{21}}{S_{12}}\right)} = 1 \quad (2.8)$$

At higher frequencies, the impact of gate-drain feedback becomes significant, causing deviation from the theoretically predicted −20 dB/decade slope. To determine f_{max}, an extrapolation technique is employed by fitting a tangent line with a −20 dB/decade slope to the measured U data in the lower frequency range.

To assess the stability of linear two-ports, Rollett proposed a simple metric in 1962[57]. This metric, defined as

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2|}{2|S_{12}S_{21}|} \quad (2.9)$$

The auxiliary condition must be simultaneously satisfied to ensure the fulfilment of the requirement.

$$|\Delta| = |S_{12}S_{12} - S_{12}S_{12}| < 1 \quad (2.10)$$

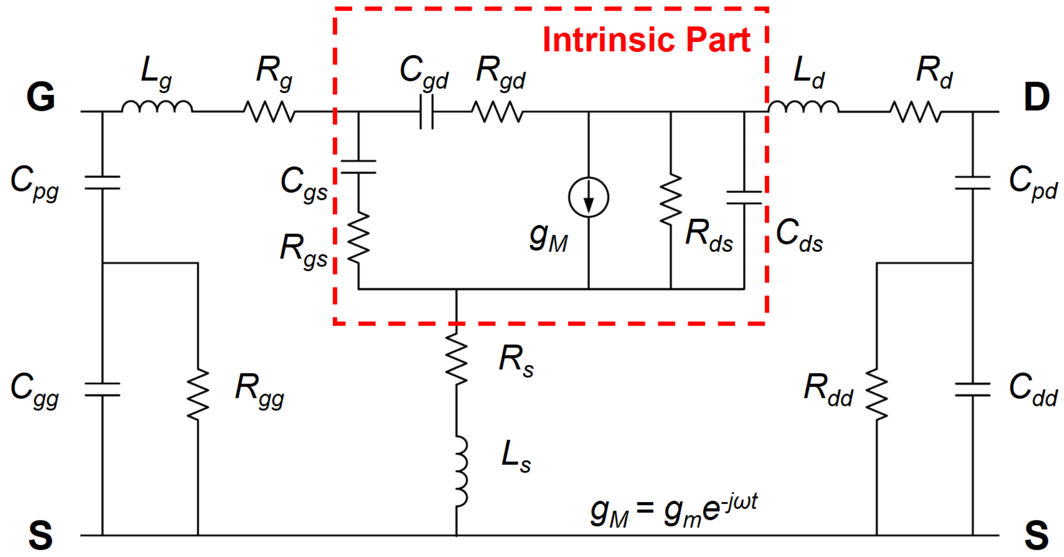


Fig. 2-11 22-element model of GaN HEMT considering parasitic conduction

The value k = 1 represents the threshold that separates the frequency range of unconditional stability from that of conditional stability for the analyzed two-port system. This boundary also establishes the demarcation between the maximum stable gain (MSG) and the maximum available gain (MAG). When the transistor exhibits unconditional stability, characterized by $k \geq 1$ and $|\Delta| < 1$, the MSG and MAG can be defined as follows:

$$MSG = \left|\frac{S_{21}}{S_{12}}\right| \tag{2. 11}$$

$$MAG = \left|\frac{S_{21}}{S_{12}}\right|(k - \sqrt{k^2 - 1}) \tag{2. 12}$$

Among the three primary modelling approaches for GaN HEMTs (physics-based, behavior-based, and equivalent circuit models), equivalent circuit models have gained the widest adoption[58]. An accurate small-signal model serves as the foundation for characterizing the large-signal behavior of GaN HEMT devices. Consequently, researchers have proposed various methods for small-signal equivalent circuit modelling [59], [60], [61], [62].

Fig. 2-11 presents the fundamental small-signal equivalent circuit of a GaN HEMT with its intrinsic and extrinsic elements. This circuit layout reveals that GaN HEMTs' response speed mainly depends on how quickly the input capacitance (C_{gs}) and feedback capacitance (C_{gd}) charge through the input resistance (R_{in}). Using this model, we can express the cutoff frequency—key measure of high-frequency performance that occurs when current gain reaches unity—as:

$$f_T = \frac{g_m}{2\pi(C_{gd}+C_{gs})[1+(R_s+R_d)G_{ds}+g_m(R_s+R_d)C_{gd}]} \tag{2. 13}$$

And the maximum oscillation frequency (f_{max})can be formulated as:

$$f_{max} = \frac{f_T}{2\sqrt{(R_i+R_s+R_g)\times G_{ds}+2\pi f_T R_g C_{gd}}} \tag{2. 14}$$

where C_{gs} represents gate-source capacitance, C_{gd} indicates the gate drain capacitance, g_m refers to the transconductance, R_s is the source resistance, R_g is gate resistance, G_{ds} is drain-source transconductance, R_i is the input resistance.

According to these equations, the f_T can be further enhanced by reducing the gate length to minimize gate capacitance. To improve the f_{max}, T-shaped gate structures can be implemented to minimize gate resistance without introducing excessive parasitic gate capacitance. The optimization of ohmic contacts and T-shaped gate configurations plays a crucial role in mitigating the adverse effects of parasitic resistance, thereby enhancing high-frequency performance. These optimizations constitute key objectives driving this research. Specifically, the height and width of the T-shaped gate require careful optimization to achieve an optimal balance between capacitance and resistance values.

Analysis of the relationship between cutoff frequency and gate length (L_g), as demonstrated in previous studies [63], [64], [65], [66], underscores the significance of reducing gate length to enhance f_T. Notable achievements in this domain include those from NTU [67] and Intel [68], who successfully fabricated GaN HEMTs on silicon substrates with gate lengths as small as 40 nm, resulting in fT values exceeding 300 GHz. It is noteworthy that Intel currently holds the record with an fmax reaching 400 GHz.

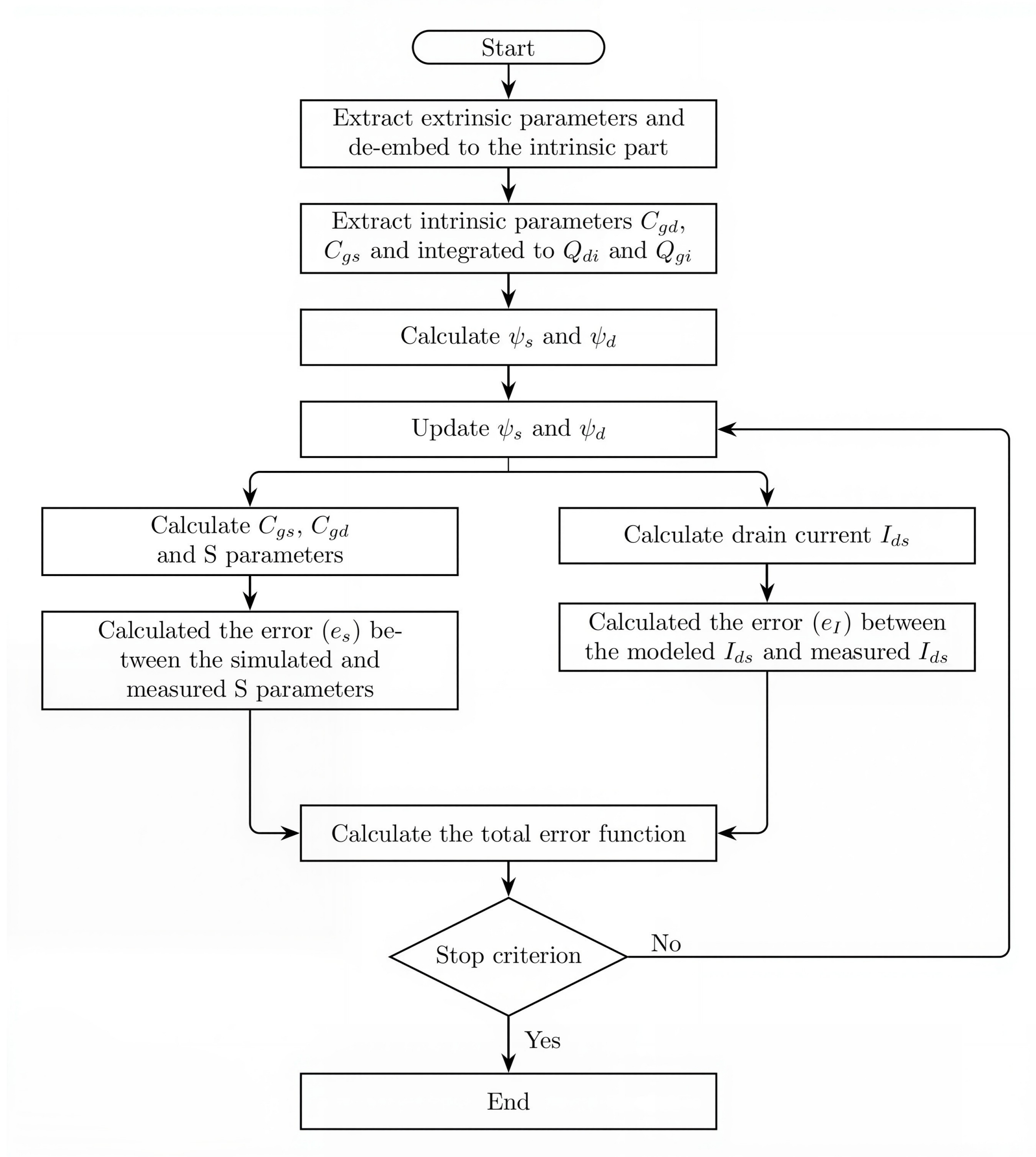


Fig. 2-12 Flow chart of small signal parameter extract using ASM-HEMT and ANN modelling.

Recent developments in GaN HEMT modelling have introduced a hybrid approach that combines artificial neural network (ANN) techniques with physical modelling principles from the Advanced SPICE Model (ASM-GaN-HEMT) [61], [69]. This innovative methodology addresses the fundamental challenge of balancing physical accuracy with computational efficiency in GaN device modelling [70].

The modelling framework employs a systematic parameter extraction procedure centered on surface potential optimization. Using Multi-Objective Particle Swarm Optimization (MOPSO), Lu et al. derived precise surface potential values (ψ_s and ψ_d) that serve as key parameters in the ASM-GaN-HEMT model. These optimized parameters simultaneously satisfy measured S-parameters, resulting in a model that accurately represents RF behaviors across various operating conditions, and the de-embedding procedure and parameter extraction procedure follows Fig. 2-12.

The accurately de-embedded S-parameters enable derivation of several important figures-of-merit that assess the maximum achievable RF performance of AlGaN/GaN HEMT technology. These metrics provide essential insights into device capabilities for high-frequency applications and establish benchmarks for technology optimization [70]. In Fig. 2-13, these optimized parameters simultaneously satisfy measured S-parameters, resulting in a model that accurately represents RF behaviors. Additional fitting results over multiple bias conditions are provided in the referenced publication and show consistent agreement between measured and modeled DC and S-parameters.

This comprehensive small-signal characterization and modelling approach provides a robust foundation for understanding and predicting GaN HEMT behavior in RF circuit applications, facilitating reliable design of high-performance power amplifiers, switches, and other RF components.

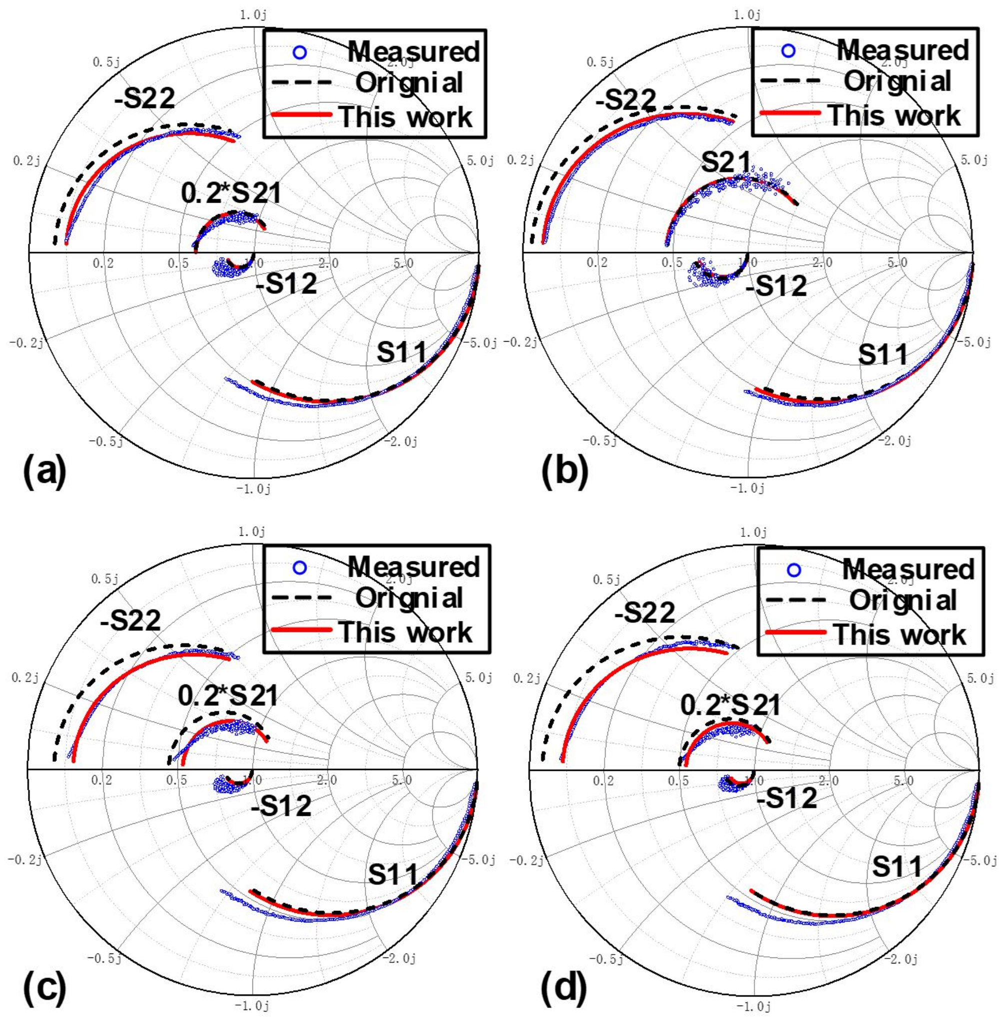


Fig. 2-13 Measured (blue symbols), ASM model simulated (black dashed lines) and proposed hybrid model simulated (red lines) S-parameters in 1-40 GHz of (a) 2 × 50 μm, $V_{GS} = -2.0$ V, $V_{DS} = 10$ V; (b) 2 × 50 μm, $V_{GS} = 1.5$ V;$V_{DS} = 10$ V, (c) 2 × 100 μm, $V_{GS} = -2$ V, $V_{DS} = 10$ V, and (d) 2 × 100 μm, $V_{GS} = -1.5$ V, $V_{DS} = 10$ V [68].

2.3.4 Noise Characteristics and modelling

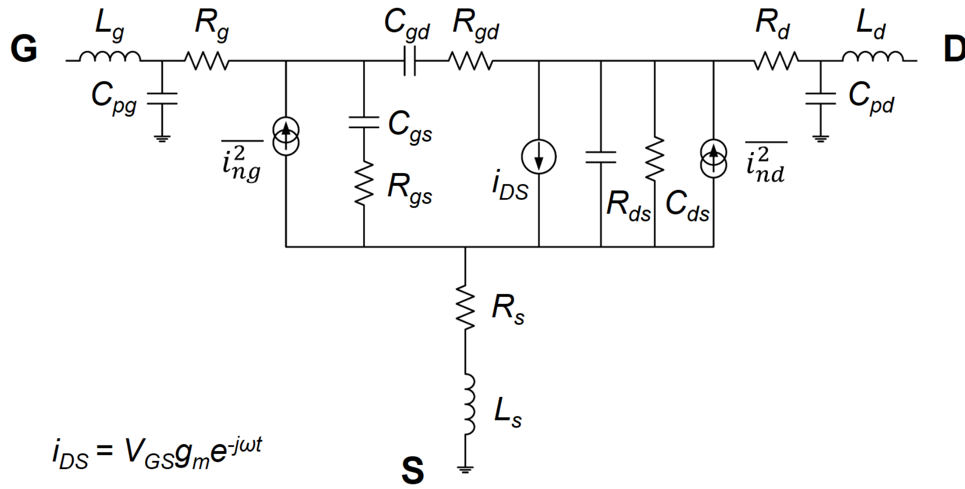


Fig. 2-14 Equivalent noise modelling circuit

In the realm of noise modelling for GaN HEMTs, Pucel's theory has been widely applied [71]. The complete noise model topology based on the aforementioned 22-element small-signal model is illustrated in Fig. 2-14. In this representation, noise sources placed in parallel with R_s, R_d, and R_g characterize thermal noise, which becomes particularly significant in high-frequency operations. The small-signal equivalent circuit can be extended with noise sources that account for various noise mechanisms including thermal noise, channel noise, drain-induced gate noise and shot noise. The thermal noise source in parallel with resistive elements such as Ri can be expressed as:

$$i_{nRi}^2 = 4kT\Delta f/R_i \tag{2. 15}$$

where k is Boltzmann's constant, T is temperature, and Δf is bandwidth.

The noise sources in parallel with the intrinsic part of the model are used to characterize the shot noise and thermal noise induced by the channel in GaN layer. Channel noise and gate current noise source can be expressed as

$$i_{nd}^2 = 4kT\Delta f g_m P \tag{2. 16}$$

$$i_{ng}^2 = 4kT\Delta f \cdot \omega^2 \cdot C_{gs}^2 \cdot R/g_m \tag{2. 17}$$

Where P represents a fitting parameter typically between 2-3 for GaN HEMTs and R denotes another fitting parameter. These noise sources exhibit partial correlation, expressed as:

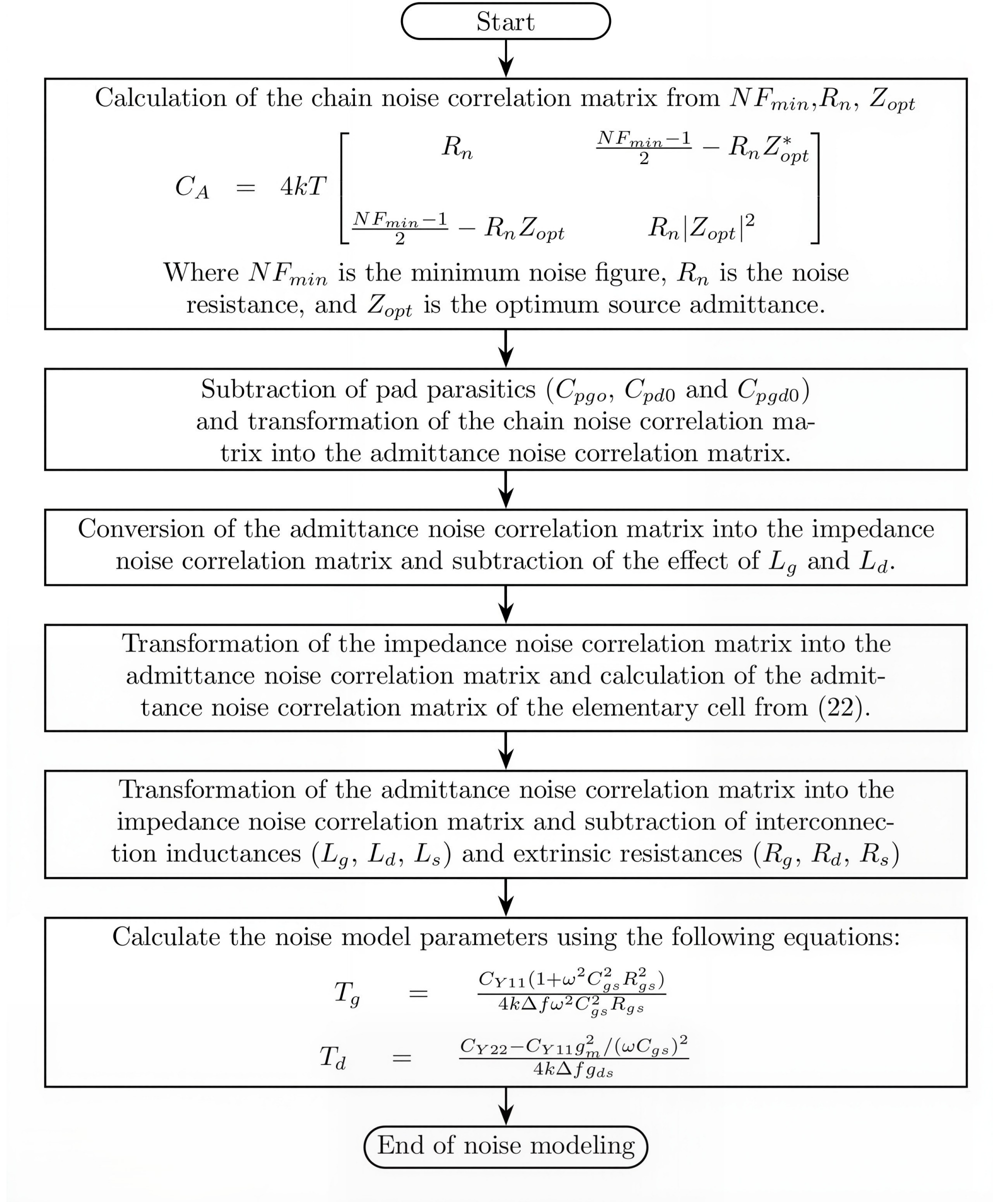


Fig. 2-15 Procedure of noise parameters modelling

$$i_{ng} \cdot i_{nd} = C\sqrt{i_{nd}^2 \cdot i_{ng}^2} = 4kT\Delta f \cdot j\omega \cdot C_{gs} \cdot C\sqrt{PR} \tag{2. 18}$$

Where C is the correlation coefficient (typically ranging from 0.4 to 0.6 for GaN devices).

Based on the established small-signal and noise models, the minimum noise figure can be expressed as:

$$NF_{min} = 1 + 2(f/f_T)\sqrt{P \cdot R \cdot (R_g + R_s) \cdot g_m} \tag{2. 19}$$

This equation demonstrates that NF_{min} is directly related to the ratio of operating frequency to cutoff frequency (f/f_T), highlighting the critical importance of high f_T values for achieving superior noise performance. This relationship also illustrates the fundamental trade-offs in device design, as optimizations that enhance f_T also tend to improve noise performance.

When implementing small-signal and noise modelling approaches for GaN HEMTs, several practical considerations warrant attention. Noise parameters should be extracted across relevant bias conditions to ensure model validity within the intended operating range. While flicker (1/f) noise is generally not a direct contributor to microwave/mm-wave noise figure, low-frequency noise in GaN HEMTs is closely related to trapping phenomena and bias-dependent fluctuations, and may therefore be relevant indirectly, for example through parameter modulation or potential noise upconversion in nonlinear operation. The dominant contributors to mm-wave noise figure remain thermal and channel-related noise mechanisms.

Temperature effects can influence small-signal and noise behavior through self-heating and mobility degradation; however, detailed temperature-dependent noise measurements are beyond the scope of this thesis.

A comprehensive modelling framework that accounts for high-frequency characteristics and noise properties enables reliable prediction of RF performance metrics and noise figures. This is particularly relevant for both power amplifiers and receiver front-end devices, where GaN HEMTs are valued for their high breakdown voltage, robustness, and resulting high linearity and wide dynamic range.

2.3.5 Large Signal Power Characteristics

Power amplifiers can be categorized based on their primary applications and operating principles. According to their bias point positions and switching characteristics, they can be classified into several categories:

1. Wideband linear power amplifiers (such as Class A, Class B, and Class AB)
2. Tuned power amplifiers (such as Class C and Class F)
3. Switching power amplifiers (such as Class D and Class E)
4. Other specialized classes (such as Class G, Class H, and Class S)

Since this work primarily focuses on linear RF power amplifiers, this section will use Class A amplifiers as an example to illustrate the performance parameters of linear RF power amplifiers.

For power amplifiers, the primary concern is extracting maximum output power from the device. Therefore, two key design considerations emerge:

1. The amplifier is designed to operate under impedance-matched conditions at both source and load to achieve maximum stable gain
2. The load impedance of the intrinsic device must be optimized along an ideal load line to ensure maximum output power

To provide physical insight into these design principles and establish fundamental power limits, an ideal Class-A operation is first considered here as a reference case. Although practical RF power amplifiers are commonly biased in Class-AB operation, the Class-A formulation offers a convenient and widely used framework for illustrating load-line behavior and defining key power figures of merit.

Fig. 2-16 illustrates a load line diagram for a Class A. The optimum load impedance ($R_{L,opt}$) is given by:

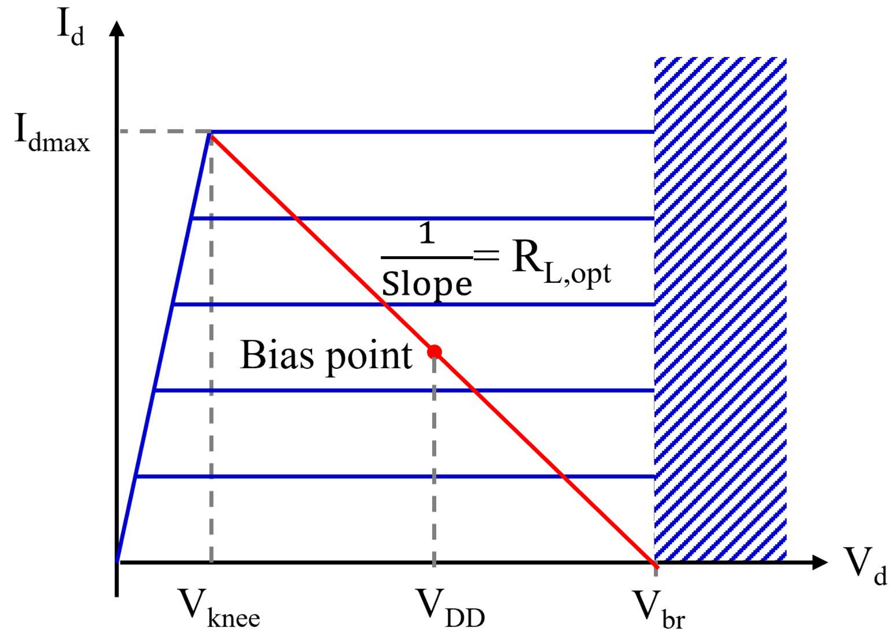


Fig. 2-16 The diagram of load line for Class A amplifier.

$$R_{L,opt} = \frac{V_{br} - V_{knee}}{I_{max}} \tag{2. 20}$$

Where V_{br} is the breakdown voltage, V_{knee} is the knee voltage where the device transitions from linear to saturation region, and I_{max} is the maximum drain current.

Simultaneously, the theoretical maximum output power (P_{max}) for a Class A amplifier can be expressed as:

$$P_{max} = \frac{1}{8}(V_{br} - V_{knee}) \times I_{max} \tag{2. 21}$$

Beyond power performance, efficiency represents another critical parameter for amplifiers. High efficiency extends battery life and can simplify thermal management systems. Two primary efficiency metrics are used: Drain Efficiency (DE) and Power-Added Efficiency (PAE). The DE is defined as the ratio of the total output power (P_{out}) to the DC power supplied by the power source (PDC), expressed as:

$$DE = \frac{P_{out}}{P_{DC}} \tag{2. 22}$$

DE is independent of the power amplifier's gain. Different classes of power amplifiers have different theoretical maximum drain efficiencies: Class A and Class B amplifiers have theoretical maximum DE values of 50% and 78.5% respectively, while Class C and switching-class amplifiers can theoretically approach 100% efficiency.

PAE is defined as the ratio of the net power added by the amplifier to the DC power supplied by the power source, expressed as:

$$PAE = \frac{P_{out} - P_{in}}{P_{DC}} \tag{2. 23}$$

where P_{in} is the RF input power. Compared to DE, PAE provides a more comprehensive representation of the amplifier's operational efficiency. PAE and DE are related by the following relationship:

$$PAE = \left(1 - \frac{1}{Gain}\right) \cdot DE \tag{2. 24}$$

where Gain represents the power gain of the amplifier.

This formulation demonstrates that as the gain increases, PAE approaches DE, while for low-gain scenarios, PAE can be significantly lower than DE. This relationship highlights the importance of considering both power gain and efficiency in amplifier design, particularly for high-frequency applications where achieving high gain becomes increasingly challenging.

GaN technology offers a promising solution for RF applications where the mix of output power density and PAE serves as a critical metric for assessing device performance. Beyond technology hurdles, proper non-linear device characterization is essential to unlock the full capabilities of this new wide-band gap technology. Our research group built an active load-pull measurement system in 2016 for 'Load-Pull' testing up to 40 GHz in both CW and pulsed modes [150]. To test devices at even higher frequencies in the D-band, we created a load-pull large signal characterization system working at 123 GHz, detailed demonstrated in chapter 5.

When evaluating RF performance of GaN HEMTs at a specific frequency, three key metrics are considered:

1. P_{out} shows the power density a transistor can deliver, usually measured in W/mm to allow fair comparison between different sized devices. While using saturated power (P_{sat})—the highest power the transistor can provide—and various compression points that reflect the large-signal compression behavior of the device,
2. Power gain: This metric indicates how well a transistor amplifies RF signals and can be calculated as the ratio between P_{out} and P_{in}. Higher gain helps achieve better power density and PAE.
3. PAE measures the ratio between power gain and consumed power (P_{DC}) and can be calculated using Equation (2.24). Higher PAE reduces heating problems and lowers energy use, which many applications require.

Load-pull measurements involve implementing various load impedances at the transistor output to determine the optimum load (typically$\neq$ 50Ω) for achieving maximum P_{out} or PAE. This impedance adaptation serves another critical purpose, which is preventing instability or oscillation issues that could potentially lead to transistor degradation. The measurement procedure follows a systematic approach, initially establishing the transistor bias in the desired operating class. Subsequently, the load impedance at the transistor output is set to a fixed value. The input power is then swept until the device reaches saturation to identify conditions that maximize either output power or PAE. This procedure is repeated for different load impedance settings. Throughout the entire load-pull measurement process, the gate leakage current undergoes continuous monitoring to ensure the transistor maintains its integrity.

For conducting load-pull measurements, three distinct methodologies exist: passive, active, and hybrid load-pull measurement techniques. The selection of the large-signal characterization approach is discussed here from a methodological perspective. The active load-pull technique offers a significant advantage in its ability to achieve high values of $|\Gamma_L|$, particularly for small devices with high reflection coefficients; however, this work adopts a passive tuner-based load-pull implementation for on-wafer D-band measurements.

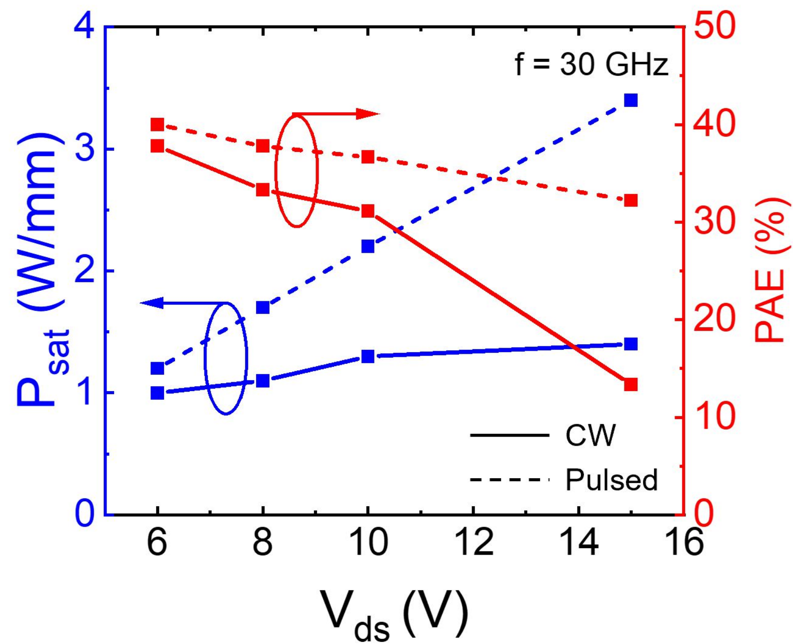


Fig. 2-17 Performance comparison between CW and pulsed-mode load-pull characterization at 10 GHz, revealing dispersion effects in GaN HEMT operation.

Load-pull measurements can be performed under two excitation modes: continuous-wave (CW) and pulsed operation. CW mode represents the conventional approach for nonlinear characterization, in which the transistor is continuously biased during measurement. In contrast, pulsed operation employs a pulsed DC bias with a pulse width of 1 μs and a duty cycle of 1%, enabling the separation of trapping and self-heating effects by reducing thermal accumulation while preserving large-signal operating conditions.

Load-pull measurements are conducted at multiple V_{DS} values in both CW and pulsed modes while maintaining a constant drain current. Throughout the load-pull sweep, the gate current I_g is continuously monitored as a function of V_{DS}. A predefined threshold (e.g., $I_g > 100$ μA/mm) is used as an indicator of device degradation or failure at the applied drain bias.

By comparing results obtained under CW and pulsed excitation, the relative contributions of trapping and thermal effects can be systematically evaluated, as illustrated in Fig. 2-17. To ensure valid comparison, identical measurement

configurations are maintained for both modes, except for the load impedance, which is independently optimized. Devices are biased in deep class-AB operation to prioritize power-added efficiency (PAE), a key metric for power amplifier applications. The optimum load impedance (Γ_{load}) differs between CW and pulsed modes due to changes in the device S-parameters arising from distinct trapping dynamics and self-heating behavior, highlighting the necessity of mode-specific load optimization for different duty-cycle applications

Prior to load-pull measurements, potential instability regions of the transistor are evaluated using S-parameter analysis and Keysight's Advanced Design System (ADS) software. This preliminary stability assessment is essential to prevent oscillations or device degradation during large-signal excitation. This section focuses on the fundamental principles and measurement concepts of load-pull characterization. Detailed descriptions of the experimental setup, calibration procedures, and measurement considerations are provided in Chapter 3 and Chapter 4.

Chapter. 3 AlN/GaN/AlGaN DH HEMTs for low-voltage FR2 Mobile Applications

3.1 Technology Development and Research Motivation

The evolution of 5G/6G telecommunications has created unprecedented demands for efficient transmitters operating in millimeter -wave bands, particularly in 5G Frequency Range 2 (FR2, >24 GHz), where achieving high uplink/downlink rates of 10/20 Gbps is crucial [72]. This technological advancement presents a unique set of challenges, especially for cellular handsets and battery-powered devices that must operate at low voltage (LV, ≤5 V) while maintaining high power density.

Among the various technologies, GaN-on-Si technology has emerged as a promising platform for these applications, combining GaN's superior power amplification capabilities with the cost-effectiveness and scalability of silicon substrates up to 300 mm [73]. The industry's progress in this direction has been marked by various implementations of single heterostructure (SH) designs, including AlGaN/GaN [74], [75], [76], [77] InAlN/GaN [66], [78], [79], [80], [81], [82], [83], and AlN/GaN [72], [84], [85]. While these conventional structures have shown promising results, they face inherent limitations in meeting the requirements of FR2 operation at low voltage.

The fundamental challenge lies in the need for sub-150 nm gate lengths to boost high-frequency performance, which introduces significant short channel effects. These effects necessitate vertical scaling methods to maintain device performance. Moreover, low-voltage operation demands a balance between achieving low knee voltage (V_{knee}) through high electron mobility (μ) while maintaining the high saturation velocity (v_{sat}) essential for efficient RF power amplification. This complex interplay of requirements has pushed the boundaries of conventional single heterostructure designs.

In response to these challenges, we propose the AlN/GaN/AlGaN double heterostructure (DH) architecture as a solution. This advanced design combines two critical elements: a thin AlN barrier layer with high polarization and an engineered

AlGaN back barrier for enhanced carrier confinement [34], [77], [86]. The DH approach represents a significant evolution from single heterostructure designs, offering unique advantages in managing the trade-offs between mobility and carrier velocity. While previous investigations have demonstrated the potential of this heterostructure for high-voltage applications [32], [33], [77], [86], its performance in low-voltage power amplification remain unexplored.

The AlN/GaN/AlGaN DH design enables more precise control over the two-dimensional electron gas (2DEG) distribution and transport properties. The ultra-thin AlN barrier provides strong carrier confinement and high sheet carrier density, while the AlGaN back barrier helps mitigate short channel effects and improve overall carrier transport characteristics. This sophisticated band engineering approach allows for optimization of both the vertical electric field distribution and carrier confinement, leading to enhanced device performance at low operating voltages.

This work proposes the use of the AlN/GaN/AlGaN DH in LV GaN-on-Si HEMTs, for the first time, achieving record power performance in 5G FR2 among reported GaN-on-Si devices. The superior performance is attributed to the optimized combination of v_{sat} and V_{knee} (normalized by L_{sd}), enabled by the unique properties of the double heterostructure design. Our comprehensive investigation encompasses device design, fabrication considerations, and detailed characterization of RF performance, providing crucial insights into the potential of this architecture for next-generation mobile communication systems.

3.2 Limiting factors in III-V GaN HEMTs for high frequency operation

3.2.1 Advantage in AlN as barrier

The implementation of AlN as a barrier layer in GaN HEMTs represents a significant advancement in device design for high-frequency applications. The fundamental advantage of AlN stems from its large spontaneous and piezoelectric polarization fields, which enable the formation of a high-density 2DEG even with ultra-thin barrier layers. This characteristic becomes particularly crucial when scaling devices for high-frequency operation.

The impact of barrier layer thickness on device performance manifests through several key mechanisms. As the barrier thickness is reduced, the gate-to-channel distance decreases, leading to enhanced electrostatic control and improved g_m. Theoretically, the transconductance is inversely proportional to the barrier thickness, following the relationship:

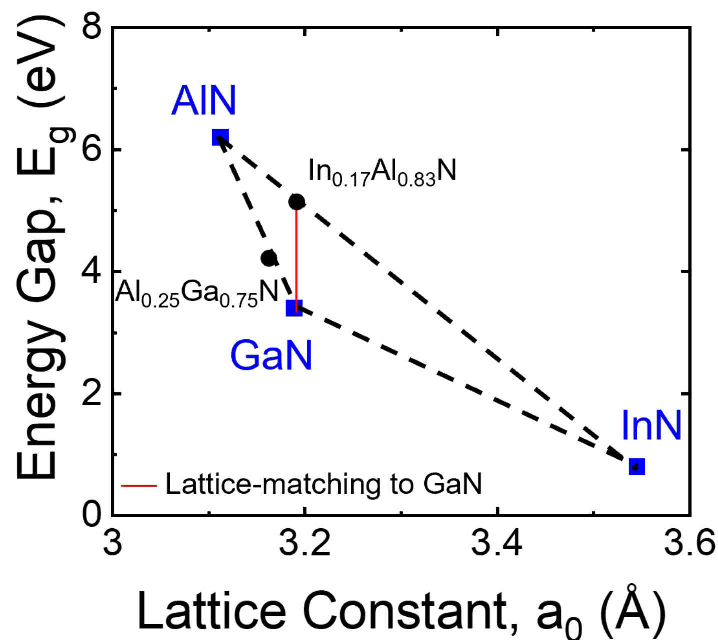


Fig. 3-1 Bandgap of InAlN and AlGaN compound

$$g_m \propto v_{sat}/(d + \Delta d)$$

where d represents the barrier thickness and Δd accounts for the quantum well width of the 2DEG. Due to the strong polarization fields of AlN, it can maintain a high 2DEG density (typically $>2\times10^{13}$ cm^{-2}) with barrier thicknesses as thin as 4-5 nm, whereas conventional AlGaN barriers require thicknesses of 15-20 nm to achieve comparable carrier densities[33], [87], [88].

The ultra-thin AlN barrier also plays a crucial role in mitigating short-channel effects, which become increasingly significant as gate lengths scale below 150 nm. The reduced gate-to-channel separation improves the aspect ratio (L_g/d) of the device, enhancing gate control over the channel and suppressing drain-induced barrier lowering (DIBL). This improvement in electrostatic integrity is essential for maintaining good pinch-off characteristics and reducing output conductance in short-channel devices.

Furthermore, the higher conduction band offset between AlN and GaN (approximately 2.1 eV) compared to conventional AlGaN/GaN structures (typically 0.5-1.0 eV) provides better carrier confinement [89]. This enhanced confinement reduces gate leakage current and improves the overall reliability of the device, particularly critical for low-voltage operation in FR2 applications.

3.2.2 Role of Back Barrier

The incorporation of an AlGaN back barrier in the double heterostructure design serves multiple critical functions in optimizing device performance for high-frequency applications. The fundamental purpose of the AlGaN back barrier resides in its capability to generate a supplementary conduction band discontinuity at the lower interface of the GaN channel, effectively forming a quantum well that enhances vertical carrier confinement. This confinement mechanism becomes particularly significant when scaling devices to shorter gate lengths, where maintaining strong control over the channel carriers is essential for high-frequency operation[32], [33], [90], [91].

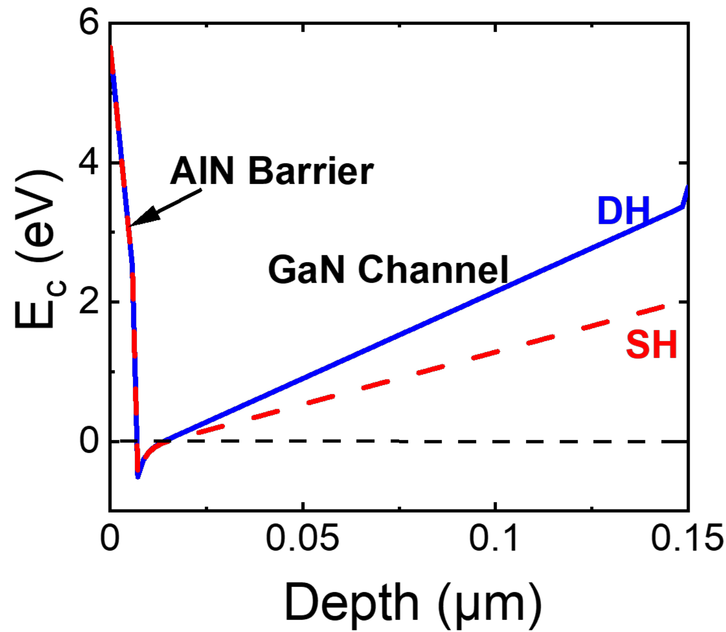


Fig. 3-2 Band diagrams of the proposed double heterostructure (DH) and a conventional single heterostructure (SH).

The physics behind the back barrier's effectiveness stems from its influence on the potential distribution within the device. Based on 1D Schrödinger–Poisson calculations focusing on electron confinement, DH achieves significantly better carrier confinement as compared to SH (Fig. 3-2). The conduction band profile created by the AlGaN back barrier introduces an energy barrier that restricts electron penetration into the buffer layer, effectively reducing the channel thickness. It should be noted that Fig. 3-2 is a schematic illustration of the conduction band and electron distribution and does not imply hole accumulation in the buffer or back-barrier region. This quantum confinement effect has several important implications for device performance. First, it leads to improved carrier transport properties by reducing scattering events associated with channel-buffer interface roughness. Second, enhanced vertical confinement helps maintain a high aspect ratio between the effective channel length and thickness, which is crucial for suppressing short-channel effects in scaled devices. In the unintentionally doped GaN buffer, the Fermi level remains far from the valence band, and stable hole accumulation is therefore not expected under normal operating conditions.

Furthermore, the presence of the AlGaN back barrier significantly reduces drain-induced barrier lowering (DIBL) and helps maintain better saturation characteristics. This improvement in output conductance directly translates to enhanced voltage gain and higher f_{max}, critical parameters for FR2 applications.

3.3 Device fabrication

The epitaxial structure used in this work consists of (from top) in-situ SiN_x layer (5 nm), AlN top barrier (5 nm), GaN channel (180 nm), AlGaN back barrier (150 nm), and GaN buffer (1 μm) grown on high resistivity (HR)-Si substrate by metal-organic chemical vapor deposition (MOCVD) (Fig. 3-3(a)–(b)). The Al content of the BB was found to be 8% (Fig. 3-3 (c)). Hall measurement indicates a sheet charge density of 1.7×10^{13} cm^{-2} and mobility of 1400 $cm^2/V \cdot s$, giving a sheet resistance of 260 Ω/□ at room temperature.

The process flow starts from the formation of ohmic contacts using Ti/Al/Ni/Au (20/120/40/50 nm) alloyed in N_2 ambient at 775 °C. Device isolation was carried out

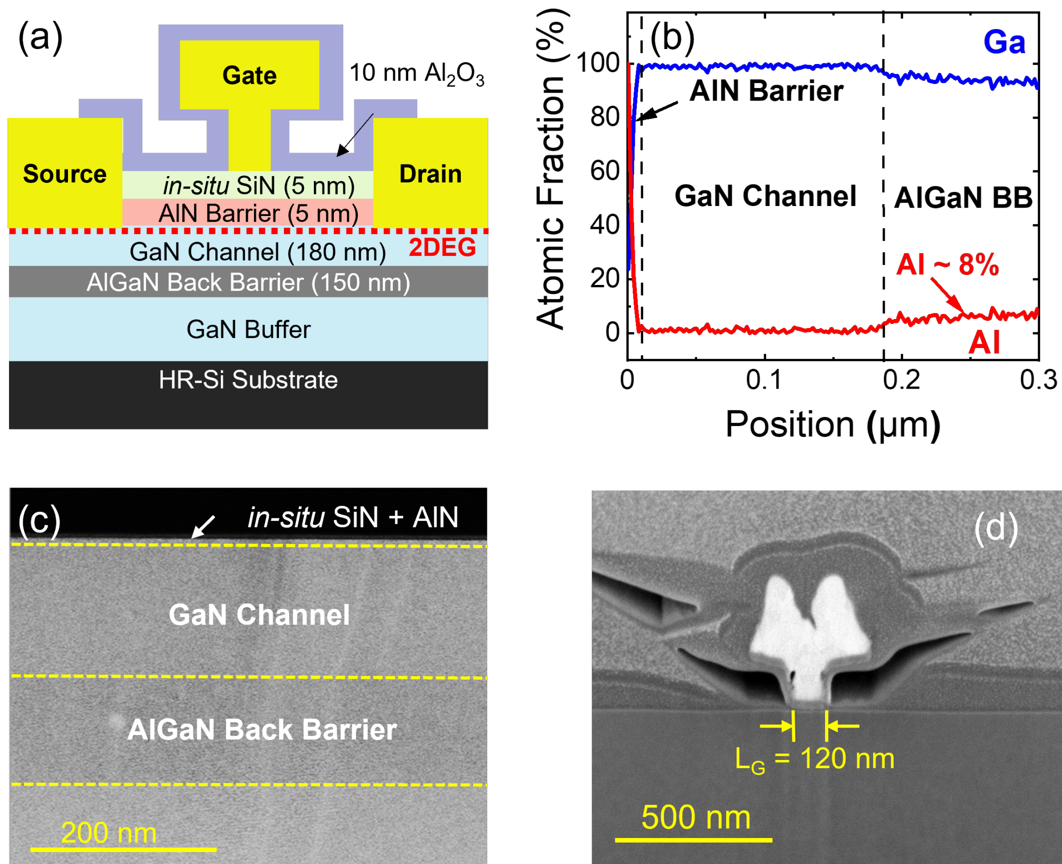


Fig. 3-3 (a) A cross-sectional schematic of the proposed AlN/GaN/AlGaN DH HEMT. (b) Elemental composition of the proposed heterostructure, as determined by energy dispersive X-ray spectroscopy (EDX). (c) STEM image of the proposed heterostructure and (d) T-shaped gate profile.

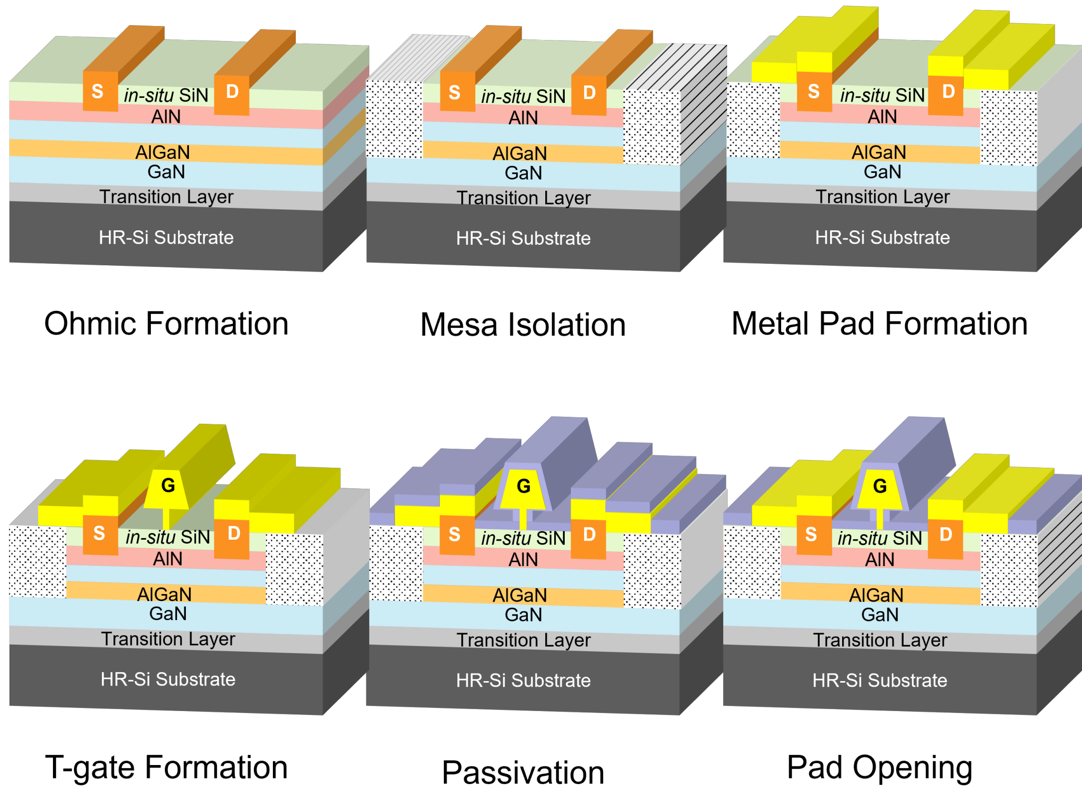


Fig. 3-4 Key fabrication process of AlN/GaN MISHEMT

using mesa etching in Cl_2-based plasma. Low ohmic contact resistance (R_c) of 0.26 Ω·mm and sheet resistance (R_{sh}) of 261 Ω/□ were achieved, as determined by transmission line model (TLM) analysis. The T-shaped gates were formed by Ni/Au (50/300 nm). Lastly, 10 nm of Al_2O_3 was deposited using thermal Atomic Layer Deposition (ALD, Triethylaluminium (TMA) + H_2O at 250 ºC), to serve as passivation [92]. The thin ALD-Al_2O_3 passivation layers could reduce the parasitic capacitance, while avoiding plasma-induced damage associated with PECVD processes, thereby offering more effective protection to the device's access region [93], [94], [95]. The fabricated transistor features a L_g of 120 nm, gate-source spacing (L_{gs}) and gate-drain spacing (L_{gd}) of 690 nm. A gate width (W_g) was 2×16 μm. The small W_g was intended to minimize self-heating, therefore evaluating the performance of the intrinsic transistor based on the proposed heterostructure.

3.4 Device characterizations

3.4.1 DC Characterization

DC I-V characterization of the in-situ SiN/AlN/GaN HEMTs were carried out using a Keysight B1500A Semiconductor Parameter Analyzer. DC output characteristics of the proposed transistor are shown in Fig. 3-5(a). A maximum drain current (I_{dmax}) of 1.9 A/mm and an ON-resistance (R_{on}) of 1.6 Ω·mm were obtained. DC transfer characteristics show that a threshold voltage of −2.9 V and a maximum transconductance g_{mmax} of 0.66 S/mm were obtained (Fig. 3-5 (b)). As presented in Fig. 3-5 (c), sub-threshold slope (SS) of 89 mV/dec and drain-induced barrier lowering (DIBL) of 43 mV/V were achieved. The employment of the thin in-situ SiN layer as gate dielectric effectively suppressed the forward-bias gate leakage, despite

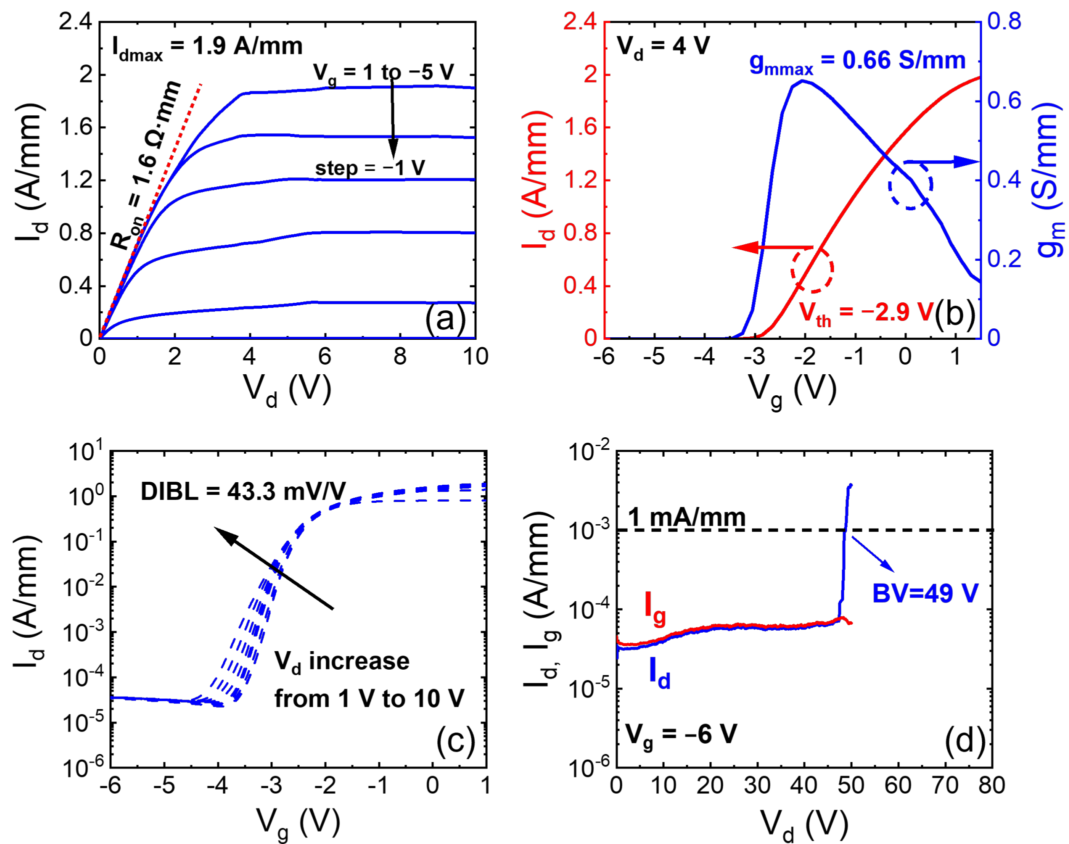


Fig. 3-5. DC characteristics. (a) Output characteristics. (b) Transfer characteristics (linear scale). (c) Transfer characteristics (logarithmic scale). (d) Three-terminal breakdown characteristics

a thin AlN top barrier. Before the passivation, the gate leakage current was <3 μA/mm. After passivation, the on/off current ratio was up to 5×10^4. Fig. 3-5 (d) presents the three-terminal breakdown characteristics, showing a breakdown voltage of 49 V. This corresponds to a source–drain lateral average breakdown electric field of approximately 0.327 MV/cm under an I_d-based breakdown criterion. At the breakdown point, while I_d rapidly increases, I_g exhibits a downward trend. This confirms that the breakdown event is not gate-limited and that the quoted electric field represents a device-level average field rather than the peak electric field or a gate–drain–normalized field. The breakdown mechanism is attributed to source-drain punch-through, which benefits from the design of the floating gate structure and the high quality of in-situ SiN.

3.4.2 Small Signal RF Characterization

S-parameter measurements were conducted using a Keysight N5244-A PNA-X Vector Network Analyzer with frequency capabilities spanning from 1 MHz to 43 GHz at room temperature.

Fig. 3-6 (a) shows the small-signal microwave characteristics of the proposed transistor. The system calibration was performed using short-open-load-through (SOLT) calibration, and the parasitic pad effects were de-embedded using on-wafer open and short test structures, which allowed for the extraction of intrinsic device parameters unaffected by measurement system limitations or interconnect parasitics. A cut-off frequency (f_T) of 147 GHz and a maximum oscillation frequency (f_{max}) of 202 GHz were achieved at V_d = −2.5 V and V_d = 6 V for a AlN/GaN/AlGaN MISHEMT with a 120 nm gate length, which were obtained by extrapolating $|h_{21}|^2$ and MAG/MSG using -20dB/decade slope after pad parasitic de-embedding. The extrinsic f_T/f_{max} before pad de-embedding are 70/138 GHz at V_d = 5V. Fig. 3-6 (c) reports the f_T and f_{max} as a function of V_d. The f_T and f_{max} maintained consistently high values (in the range of 140–150 GHz, and 190–200 GHz, respectively) at V_d > 3 V, which indicates the potential of the proposed transistor for RF applications. The proposed transistor achieved high values of $f_T \times L_g$ (17.4 GHz·μm) and $f_{max} \times L_g$ (23.4

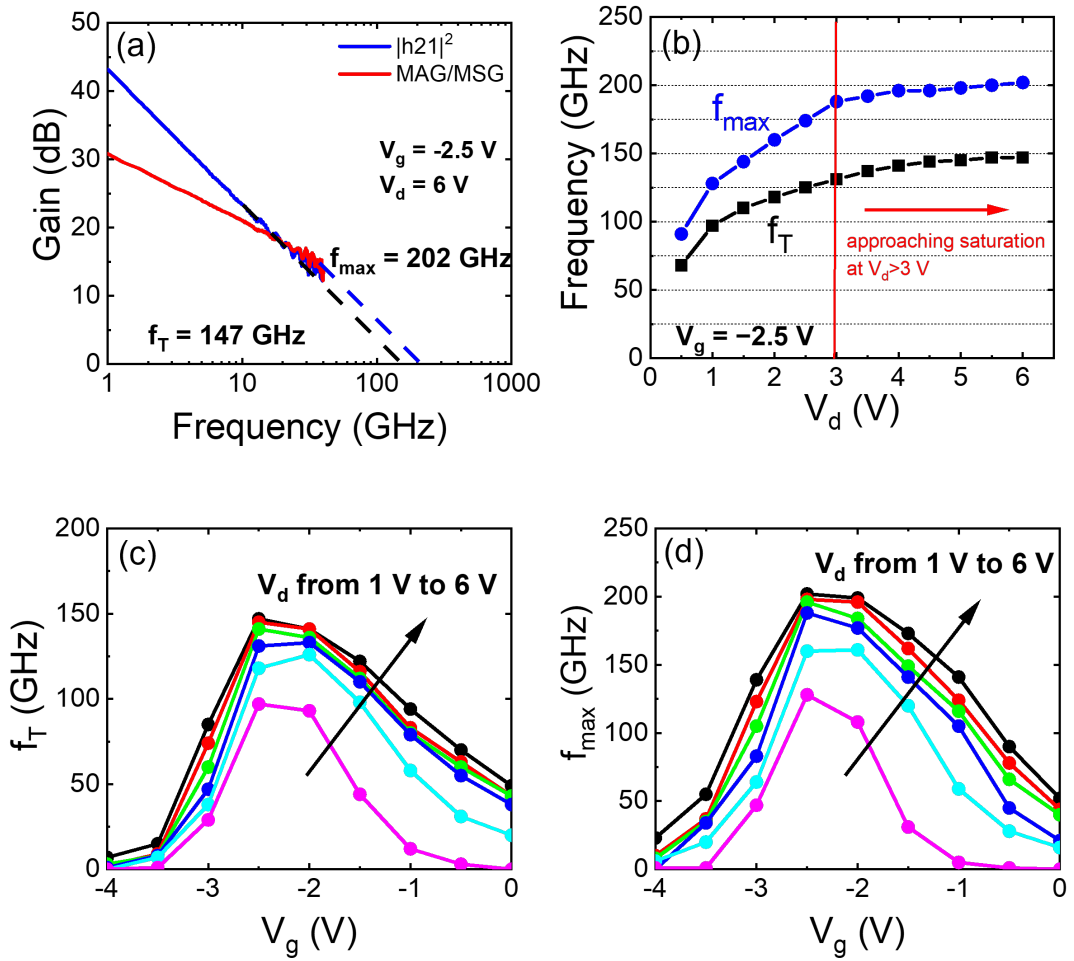


Fig. 3-6 De-embedded RF small-signal characteristics. (a) Gain vs. frequency. (b) f_T and f_{max} vs. V_d. (c) f_T and (d) f_{max} vs. V_g at different V_d.

GHz·μm), despite having a relatively large L_g of 120 nm and L_{sd} of 1.5 μm. Fig. 3-6 (c) and (d) show f_T and f_{max} as a function of V_g. A rough estimate of v_{sat} (= $2\pi f_T \times L_g$ = 1.1×10^7 cm/s) was obtained in the proposed transistor.

3.4.3 Noise Characterization

Fig. 3-7 (a) plots the NF_{min} and the G_a as functions of frequency for 10–32 GHz biased at V_d = 5 V and I_{ds} = 200 mA/mm for L_g of 120 nm AlN/GaN/AlGaN MISHEMTs on Si. The devices also demonstrate NF_{min} of 0.4 dB and 0.95 dB at 10 and 30 GHz, respectively, while maintaining high gain (G_a > 10 dB) across the frequency range

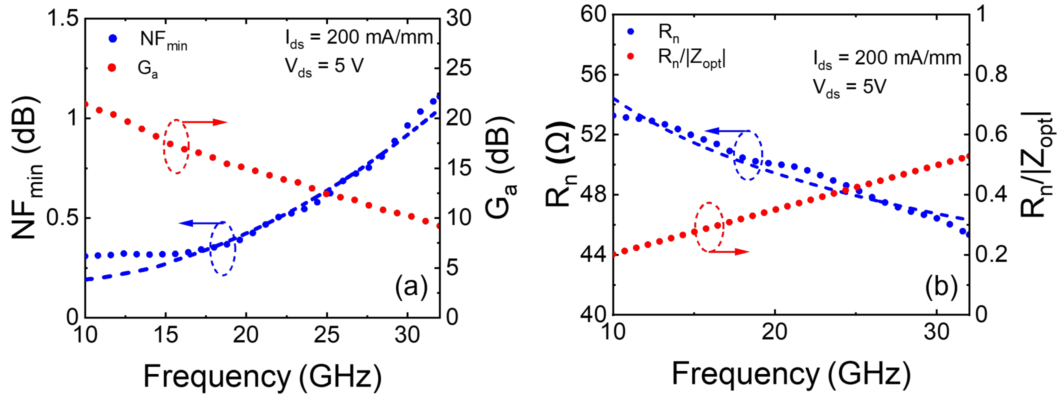


Fig. 3-7 (a) NF_{min} and G_a (scatter points: measured, dashed lines: simulated), and (b) Measured Rn and Rn/|Z_{opt}| versus frequency at I_{ds} = 200mA/mm and V_{ds} = 5 V.

(10 GHz to 32 GHz). The measured noise characteristics align closely with our simulation model (dashed line) and follow [71]

$$NF_{min} = 1 + 2\omega C_{gs}/g_m \times \sqrt{(R_g + R_s)/R_i}$$

where the enhanced g_m/C_{gs} ratio through the heterostructure engineering and minimized parasitic resistances play important roles. This is due to the optimized epitaxial structure with a 4 nm in-situ SiN cap layer and 5nm AlN barrier layer features a reduced gate-to-channel distance of 9 nm, which is 1.5× and 4× thinner than conventional InAlN/GaN and AlGaN/GaN structures, respectively. Fig. 3-7 (b) presents the measured equivalent noise resistance (R_n) and normalized R_n/|Z_{opt}|, demonstrating promising characteristics for broadband LNA design. The value of R_n/|Z_{opt}| characterizes the sensitivity of to the input source impedance mismatch. The value should be as small as possible, which facilitates the realization of high performance broadband low-noise amplifier [96], [97]. The R_n/|Z_{opt}| value of 0.2 and 0.52 was obtained at 10 GHz and 30 GHz, respectively, which slightly higher than the value of 30 GHz reported in [98]. Further optimization through barrier layer engineering and surface treatment could potentially reduce R_n/|Z_{opt}|, enabling more robust noise performance and simplified matching network design, showing potential for low-noise broadband performance. Notably, as shown in Fig. 3-8, our devices

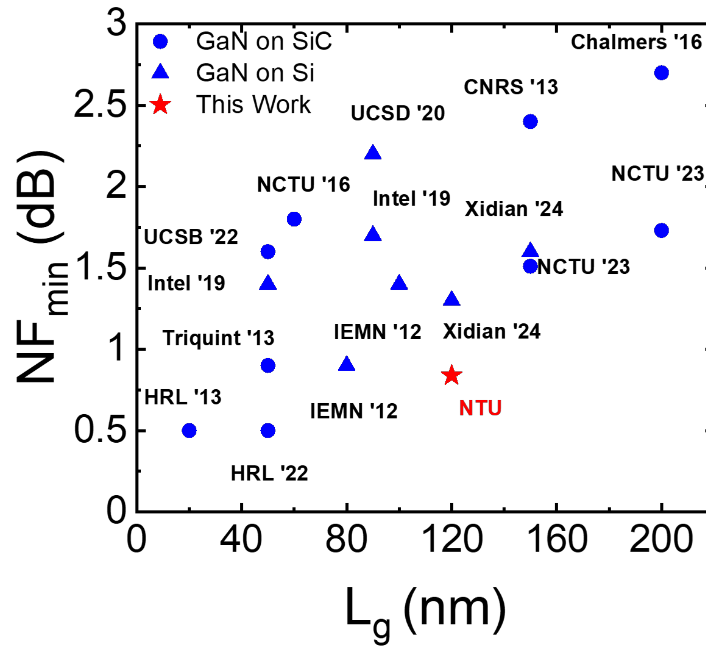


Fig. 3-8 NF_{min} versus L_g benchmarking of this work against state-of-the-art GaN HEMTs at the frequency range of 26-30 GHz.

achieve competitive noise performance compared to previously reported GaN HEMTs in the 26-30 GHz range despite having a relatively large gate length[89], [96], [97], [98], [99], [100], [101], [102], [103], [104], [105], [106], [107], [108], [109], [110].

3.4.4 Large Signal Characterization

To evaluate the high-frequency power characteristics of the device under low supply voltage and Ka band conditions, we utilized an on-wafer load-pull test system manufactured by Focus Microwave, coupled with a Keysight N5247B PNA-X vector network analyzer. The large-signal RF power characterization measurements. The large-signal performance of the proposed transistor was conducted at room temperature. Source and load impedance tuning were conducted at the fundamental frequency of 30 GHz. Fig. 3-9 (a) shows the power sweep results at a quiescent drain bias (V_{ds}) of 5 V, in Class AB operation ($I_{ds,Q}$ = 0.23 A/mm, 12% of I_{dmax}), and in continuous wave (CW) mode. The source and load impedances at the fundamental

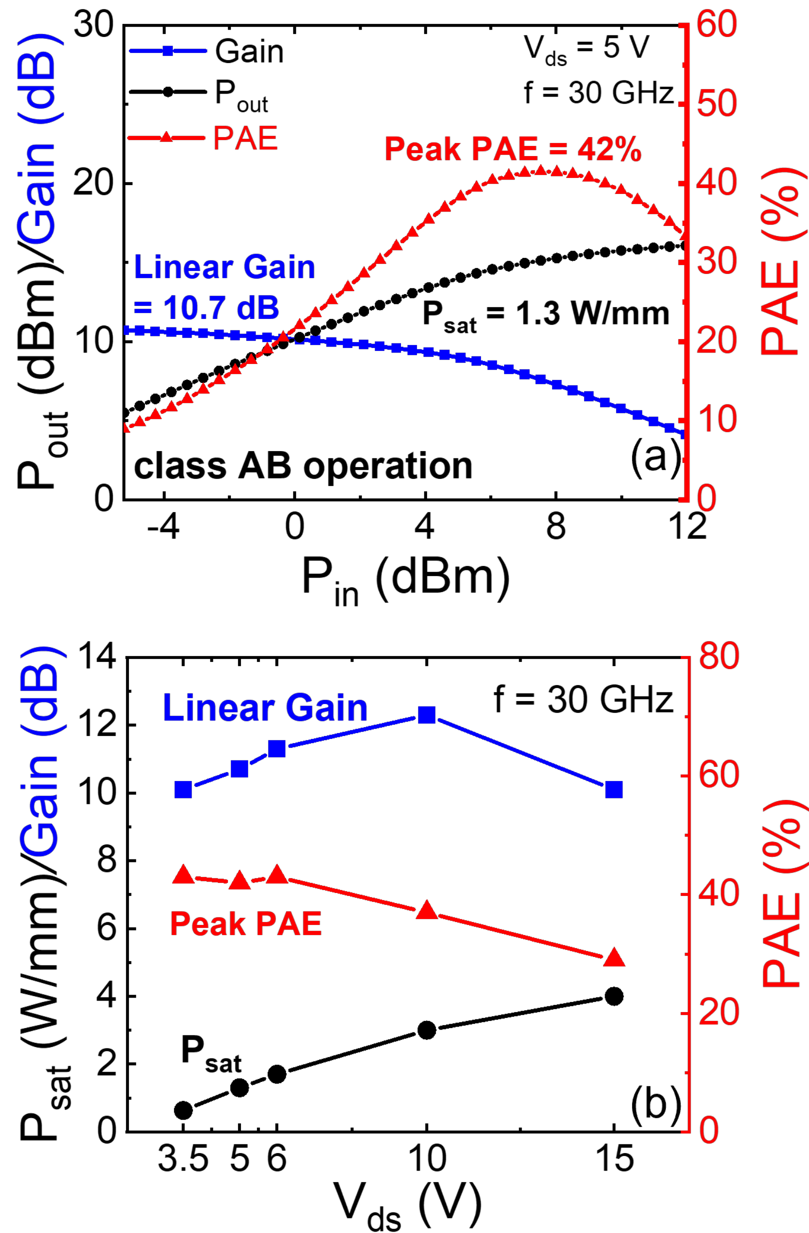


Fig. 3-9 (a) Power sweep at 30 GHz CW, V_{ds}=5 V, and Class AB operation. (b) Load-pull performance vs. V_{ds}.

frequency were tuned for maximum power-added efficiency (PAE). The source and load reflection coefficients (Γ_S, Γ_L) were 0.601∠55.4°, and 0.675∠27.5°, respectively. The proposed transistor achieved a saturated output power (P_{sat}) of 16.12 dBm (1.3 W/mm) with an associated PAE of 32% and gain of 3.7 dB. The peak PAE was 42 % with an associated output power (P_{out}) of 1.1 W/mm and gain of 7.3 dB. The linear

gain was 10.7 dB. Fig. 3-9 (b) shows the load pull performance as a function of V_{ds}. At V_{ds} of 3.5 V, the P_{sat} of 0.63 W/mm (associated PAE of 37%, gain of 4.6 dB), and peak PAE of 43% (associated P_{out} of 0.52 W/mm, gain of 7.2 dB) were achieved. It should be noted that these measurements were performed under CW operation, under which the achievable peak PAE is inherently constrained compared with pulsed conditions. This trend arises because the DC power consumption increases linearly with V_{ds}, while the achievable RF output power is limited by finite knee voltage, output resistance, and parasitic losses; trapping and self-heating effects may further aggravate this behavior. While this work focuses on low voltage applications, the performance was explored for higher voltages (V_{ds} > 5 V). As the V_{ds} increased from 3.5 V to 15 V, there is approximately linear increase in P_{sat} (reaching 4.0 W/mm at V_{ds} = 15 V). The peak PAE decreased, mostly due to increased effect of traps and limited available load impedance tuning results of non-optimal matching condition [111].

3.5 Contributions to GaN mm-Wave Development

A benchmark of RF power performance (represented by P_{sat}) of LV GaN-on-Si HEMTs in 5G FR2 is shown in Fig. 3-10(a). To the best of the authors' knowledge,

Table 3.1 LV (≤5 V) GaN-on-Si HEMTs for 5G FR2 operation

L_g (nm)	Freq. (GHz)	V_{ds} (V)	P_{sat} (W/mm)	Peak PAE (%)	Epitaxial Structure	Ref.
200	28	4	0.56	42	AlGaN/GaN	[50]
90	28	5	1.25	57	InAlN/GaN	[54]
80	28	3.5	0.36	40	AlN/GaN	[28]
		5	0.73	42		
250	26	5	0.83	45	AlGaN/GaN	[52]
120	30	3.5	0.63	43	AlN/GaN/ AlGaN	This Work
		5	1.3	42		

the P_{sat} achieved in this work sets a record among GaN-on-Si HEMTs, at the respective V_{ds} values. It is insightful to analyze the origins of the excellent LV performance by analyzing the V_{knee} and v_{sat}, which are critical parameters in the LV power amplification by the transistor [34]. Here v_{sat} is extracted from the measured f_T using $v_{sat}=2\pi\times L_g\times f_T$ and therefore represents an effective saturation velocity. It is noted that prior studies have reported a weak dependence of the saturation velocity on sheet carrier concentration, approximately following a square-root relationship under certain transport regimes; however, in this work v_{sat} is treated as an effective parameter to highlight device-level trends and electrostatic design effects. Fig. 3-10(b) compares the V_{knee} (normalized by L_{sd}) and v_{sat} values for reported LV GaN-on-Si transistors (not limited to FR2). Despite the use of conventional alloyed ohmic contacts, the V_{knee} (normalized by L_{sd}) remains comparable to other reported transistors. This is likely the result of the high μ. Moreover, a relatively high v_{sat} was obtained in the proposed heterostructure (DH). These desirable characteristics ensure high P_{out} even at lower V_{ds}. A summary of the LV GaN-on-Si HEMTs in 5G FR2 is presented in Table 3.1. Till date, all the reported demonstrations are achieved using SH epitaxies, and the majority use deeply scaled gates ($L_g < 100$ nm). In comparison, the proposed transistor achieves excellent performance using a longer L_g of 120 nm, and conventional ohmic and gate processes. The results indicate the promising potential of proposed heterostructure (DH) for LV application. Nevertheless, several areas of improvement in the transistor, based on the proposed heterostructure, are identified. These include, passivation, aggressive scaling, and ohmic contacts. Notably, achieving E-mode operation would be highly desired for handset applications [78], [112], [113], [114], [115], [116].

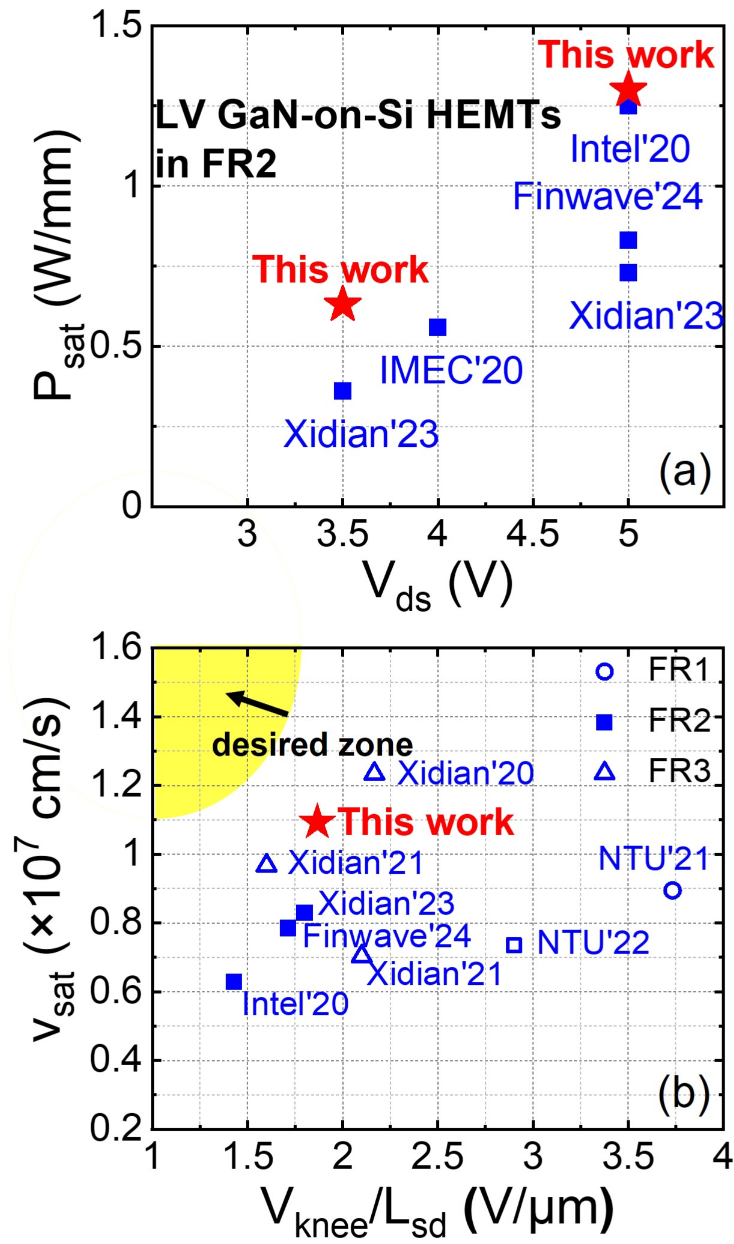


Fig. 3-10 (a) Benchmark of P_{sat} vs. V_{ds} for LV 5G FR2 operation. (b) Comparison of v_{sat} vs. V_{knee} (normalized by L_{sd}) for reported LV GaN-on-Si transistors in FR1, FR2, and FR3.

3.6 Summary

This work advances the state-of-the-art in GaN-on-Si HEMTs for 5G FR2 handsets by demonstrating the low-voltage power performance of an AlN/GaN/AlGaN-on-Si HEMT. A simultaneously high f_T/f_{max} of 145/195 GHz was achieved using L_g of 120 nm and conventional alloyed contacts. Load-pull at 30 GHz CW indicated P_{sat} of 0.6 (1.3) W/mm, which are record values for GaN-on-Si HEMTs in 5G FR2 at V_{ds} = 3.5 (5) V, respectively. The results are attributed to the desired combination of V_{knee} (normalized by L_{sd}) and v_{sat}, which are significant for LV power amplification, in DH. Further improvements to the transistor, based on the proposed heterostructure, would make GaN-on-Si HEMT technology the preferred candidate for 5G FR2 handset applications.

Chapter. 4 First demonstration on D-band GaN-on-Si Power Amplifier

4.1 Technology Development and Research Motivation

Building upon our successful demonstration of AlN/GaN/AlGaN double heterostructure HEMTs for FR2 low-voltage applications discussed in Chapter. 3, we now explore pushing the frequency frontier further into the D-band regime (110 −170 GHz). While the fundamental device architecture remains consistent with our previous design, the optimization shifts toward sub-THz operation. The exceptional benefits offered by the double heterostructure—specifically its improved carrier containment and enhanced electron transport characteristics—become increasingly significant as device operation extends into frequency domains exceeding 100 GHz.

The transition from FR2 to D-band operation presents challenges that require careful optimization of device parameters. The ultra-thin AlN barrier layer, which proved effective in reducing short-channel effects in our FR2 devices, becomes increasingly crucial for D-band operation where parasitic effects can severely impact device performance. Similarly, the role of the AlGaN back barrier in maintaining excellent carrier confinement takes on renewed importance as we push toward higher frequencies where maintaining high output power and gain becomes more challenging.

Sub-THz frequencies (>0.1 THz) are expected to play a critical role in the 6G cellular network, where massive amounts of compact cell arrays support extremely high data rates (up to 1 Tbps) [117]. Furthermore, sub-THz millimeter-wave integrated circuits (MMICs) are useful for atmospheric remote sensing, and for realizing THz power sources [118]. These emerging applications have sparked renewed interest in semiconductor technologies capable of power amplification in the D-band (110 – 170 GHz), including Si CMOS, SiGe HBT, and InP HBT [48], [119]. D-band MMICs based on GaN-on-SiC/sapphire HEMTs have been reported [118], [120], [121], [122],

[123], [124], with a latest report of a N-polar GaN/AlGaN MMIC achieving 2 W/mm [125].

Compared to these more established technologies, a promising development has been GaN-on-Si HEMT technology, which combines the merits of the III-N heterostructure and Si substrate (high breakdown voltage, high charge density, good mobility, and wafers up to 300 mm diameter) [126]. GaN-on-Si HEMTs have achieved impressive values of f_T=310 GHz [92], and f_{max}=680 GHz [127]. As compared to other compound semiconductor technologies considered for D-band (e.g., GaN-on-SiC, InP HBTs), the GaN-on-Si platform offers opportunities for compact integration with Si CMOS [128], [129], [130]. Despite significant progress in GaN-based technologies, the implementation of GaN-on-Si HEMTs for power amplification applications has predominantly been confined in the K_a-band [131], and W-band [132], [133]. Despite significant advancements in GaN-on-Si HEMT technology over the past decade, its potential in sub-THz applications remains largely unexplored, presenting a timely opportunity to extend this promising platform into higher frequency domains.

This work demonstrates the first successful implementation of GaN-on-Si HEMT technology for power amplification in the D-band frequency range. The significance of this achievement extends beyond power performance metrics, representing an important advancement in the progression of Si-based GaN technology toward sub-THz applications. Using the optimized AlN/GaN/AlGaN double heterostructure design, we achieved power performance with P_{out} = 0.67 W/mm at 123 GHz under continuous wave (CW) operation and V_{ds} = 10 V. These results are remarkable considering the relatively conservative design choices, including conventional alloyed contacts and a relatively large gate length of 140 nm, suggesting substantial room for further performance enhancement through advanced process optimization, which opens new possibilities for cost-effective, high-performance solutions in emerging sub-THz applications, while maintaining compatibility with Si-based platforms.

4.2 Ultra-high Frequency GaN HEMT RF Device Research

4.2.1 Design Challenges for D-band Power Amplifiers

The evolution toward 6G wireless communications presents unprecedented challenges in achieving ultra-high data rates. While current 5G systems rely heavily on advanced modulation schemes such as high-order QAM (Quadrature Amplitude Modulation) to increase spectral efficiency, this approach alone faces fundamental limitations. As modulation order increases from 64-QAM to 256-QAM and beyond, the system becomes increasingly sensitive to noise and distortion, requiring significantly higher signal-to-noise ratios (SNR) to maintain acceptable bit error rates. This trade-off between spectral efficiency and system robustness necessitates exploration of alternative approaches to enhance data throughput.

As shown in Fig. 4-1, the relationship is clearly illustrated in the spectral efficiency versus E_b/N_0 graph, which plots the theoretical Shannon capacity limit alongside practical modulation schemes from BPSK to 4096QAM. The graph shows that within

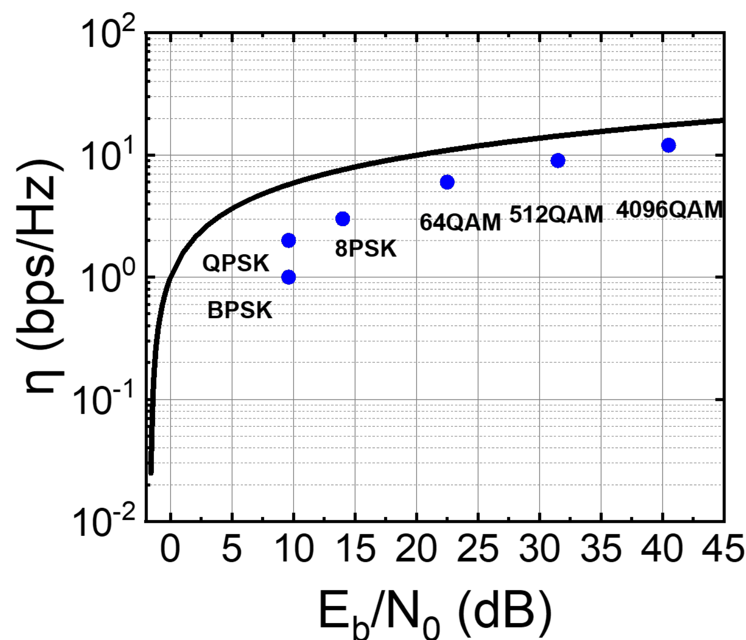


Fig. 4-1 Comparison of Shannon Capacity Limit and Practical Modulation Schemes

practical SNR ranges, lower-order modulations such as QPSK can operate with a relatively small gap to the Shannon limit at their corresponding spectral efficiencies, whereas very high-order modulations (e.g., 512QAM and 4096QAM) require substantially higher Eb/N0 to achieve their theoretical spectral efficiencies.

The fundamental relationship between channel capacity (C), bandwidth (B), and SNR is governed by Shannon's theorem:

$$C = B \times log_2(1 + SNR)$$

This equation reveals that while increasing modulation order provides logarithmic improvements in capacity, expanding bandwidth offers linear scaling potential. As shown in the graph, doubling spectral efficiency from 6 bits/Hz (64QAM) to 12 bits/Hz (4096QAM) requires approximately 15 dB higher E_b/N_0—a power increase of over 30 times. Conversely, doubling the bandwidth would directly double capacity without requiring higher SNR. This insight drives the push toward higher frequency bands, particularly the D-band, where substantially wider bandwidth is available, offering the possibility of multi-gigabit-per-second data rates even with moderate modulation schemes.

However, operating in the D-band introduces significant design challenges. At frequencies above 100 GHz, millimeter-wave losses become increasingly pronounced through multiple mechanisms. These losses effectively reduce achievable SNR, potentially forcing systems to operate with lower-order modulations despite the theoretical availability of higher spectral efficiency options. The skin effect in conductors intensifies, leading to higher resistive losses in transmission lines and interconnects. Dielectric losses in substrates and passivation layers grow more significant, as material loss tangent typically increases with frequency.

The reduced wavelength at D-band frequencies presents both opportunities and challenges. While it enables more compact antenna arrays suitable for mobile devices, it also makes the design more sensitive to manufacturing tolerances and process variations.

4.2.2 Device Scaling and Parasitic Effects for D-band Operation

The pursuit of D-band power amplification necessitates a fundamental understanding of device scaling and parasitic effects, as their impact becomes increasingly dominant at frequencies above 100 GHz. The intrinsic performance of a GaN HEMT is primarily determined by the electron transit time under the gate, which scales inversely with gate length. However, this seemingly straightforward relationship becomes considerably more complex when parasitic elements are considered at D-band frequencies.

The scaling of GaN HEMTs toward shorter gate lengths significantly impacts high-frequency performance through multiple delay mechanisms. The relationship between cutoff frequency (f_T) and device dimensions can be understood through the expression for total delay time includes transit time components and parasitic delays [134]:

$$\tau = \frac{1}{2\pi f_T} = \frac{C_{gd}+C_{gs}}{g_m} + C_{gd}(R_s + R_d)\left[1 + \left(1 + \frac{C_{gs}}{C_{gd}}\right)\frac{g_d}{g_m}\right] \quad (2.\ 25)$$

As gate length (L_g) decreases in deeply scaled devices, the intrinsic transit time under the gate is reduced, which theoretically should lead to linear improvements in f_T. However, when examining the relationship between f_T and $1/L_g$, deeply scaled GaN HEMTs demonstrate performance limitations that cannot be overcome by gate length scaling alone. These limitations arise from the increased prominence of parasitic charging delays, access region delays, and short-channel effects as dimensions shrink. The scaling of source-drain distance (L_{sd}) and gate-drain spacing (L_{gd}) also become critical in deeply scaled devices, as these dimensions affect the parasitic resistances and capacitances that contribute to the overall delay mechanisms. The significant increase in output conductance (g_d) in shorter devices creates additional delay components that were negligible in longer-gate devices.

Consequently, optimizing high-frequency performance in deeply scaled GaN HEMTs requires comprehensive consideration of all delay components, with particular attention to the parasitic elements that become increasingly significant as dimensions decrease beyond the 100 nm threshold. Fig. 4-2 shows the benchmarking of (a) f_T and

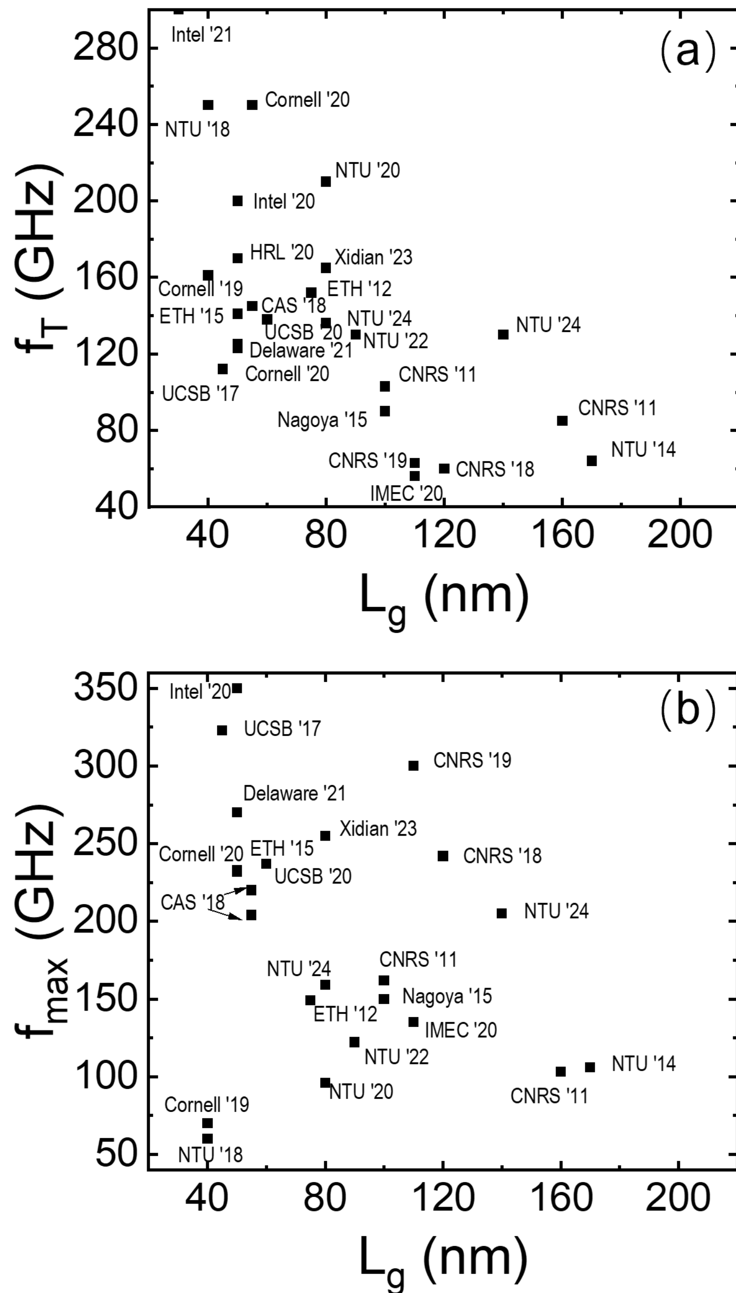


Fig. 4-2 Benchmarking with state-of-the-art (a) f_T (b) f_{max} versus L_g for GaN HEMTs on Si substrates.

(b) maximum oscillation frequency (f_{max}) as a function of L_g for state-of-the-art GaN HEMTs reported in literature. As demonstrated in these plots, the general trend of f_T follows an inverse relationship with gate length, though this scaling advantage diminishes at extremely short gate lengths due to the increasing significance of

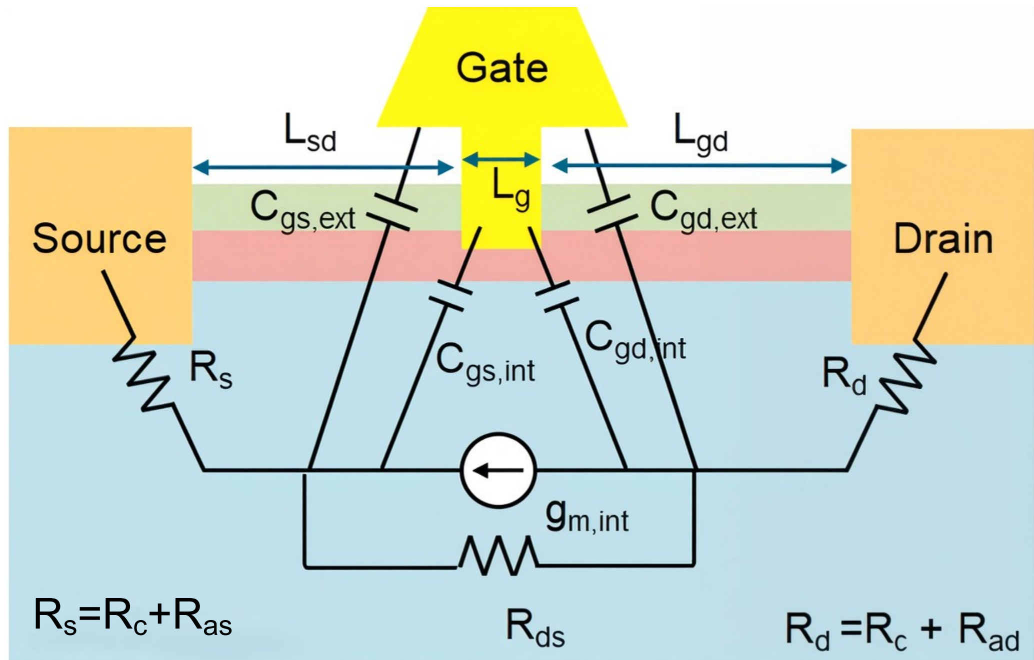


Fig. 4-3 GaN HEMT structure and its corresponding small-signal equivalent circuit model.

parasitic effects and short-channel limitations. However, the f_{max} trend exhibits less distinct scaling behavior, as it is dependent on gate resistance (R_g), which partially masks the direct scaling relationship evident in f_T. The R_g can be reduced through optimization of gate geometry, which is discussed in detail in Chapter 2.2.3.

The scaling of gate length presents a multi-faceted challenge. While reducing L_g from conventional dimensions (> 250 nm) to deep submicron levels (< 150 nm) theoretically improves the intrinsic transit frequency ($f_{T,int}$), the actual device performance is increasingly limited by parasitic delays. These delays can be categorized into three main components: the charging time of gate capacitance (τ_{RC}), the drain delay time (τ_d), and the parasitic charging time (τ_{par}). The total gate delay time can be expressed as:

$$\tau_{total} = \tau_{RC} + \tau_{transit} + \tau_d + \tau_{par}$$

At D-band frequencies, the parasitic charging time becomes particularly critical. As illustrated in Fig. 4-3, the R_g and parasitic capacitances (C_{gs} and C_{gd}) form an RC network that can significantly degrade the maximum achievable frequency. This relationship is described by:

$$f_{T,ext} \approx \frac{1}{2\pi\sqrt{R_g \times C_{gs} \times C_{gd}}}$$

Therefore, reducing gate resistance while maintaining short L_g requires sophisticated gate engineering approaches. The gate head size must balance resistance reduction with parasitic capacitance, as excessive gate head width can introduce additional parasitic effects that become significant above 100 GHz [135], [136]. In this work, this is achieved through an optimized T-gate geometry, which lowers R_g without incurring excessive overlap or fringing capacitance. Together with aggressive access-length scaling, this parasitic-focused optimization directly enables the substantially enhanced f_T and f_{max} performance.

Source and drain access resistances (R_s and R_d) present another critical scaling challenge. These resistances not only affect DC characteristics but also impact RF performance through their contribution to power gain and noise figure. The optimization of ohmic contacts becomes increasingly crucial, as even small variations in contact resistance can significantly impact device performance at D-band frequencies [137].

The scaling process must also consider the thermal implications of reduced device dimensions. As the active region becomes more concentrated, thermal management becomes increasingly challenging. This is particularly critical for GaN-on-Si platforms, where the thermal conductivity of the silicon substrate is lower than SiC substrates. The thermal resistance must be carefully managed to prevent performance degradation and ensure reliable operation at high frequencies. Therefore, the complex interplay between device scaling and parasitic effects defines the achievable performance in D-band operation.

4.3 Epitaxial Material Characterization and Device Fabrication

The starting material consists of (from top) *in-situ* SiN_x (4 nm), AlN (5 nm), GaN (150 nm), $Al_{0.08}Ga_{0.92}N$ back barrier (100 nm), and GaN buffer (1 μm) epitaxially grown on high resistivity (HR, rated > 5 kΩ·cm) Si (111) substrate by metal-organic chemical vapor deposition (MOCVD) (Fig. 4-4(a)). The AlN/GaN/AlGaN double heterostructure effectively suppresses short-channel effects [35], [138], [139] and achieves significantly higher 2DEG density compared to conventional AlGaN/GaN HEMTs, owing to its larger conduction band offset and stronger polarization effects [140], [141]. A sheet charge density (n_s) of 1.7×10^{13} cm^{-2}, and mobility (μ) of 1400 $cm^2/V\cdot s$ (giving a sheet resistance (R_{sh}) of 260 Ω/□) were obtained by Hall measurement. As shown in Fig. 4-5(a), the STEM image reveals distinct layers with sharp interfaces between the SiN, AlN, and GaN regions. The corresponding EDXS mapping in Fig. 4-5(b) confirms the distribution of Ga, Al, N, Si, and O atoms across the heterostructure and demonstrates well-defined boundaries of elemental mapping. The atomic fraction profile obtained from the line scan analysis (Fig. 4-5(c)) confirms negligible Ga incorporation in the barrier region, and further quantifies the compositional transitions at the interfaces, showing abrupt changes in elemental

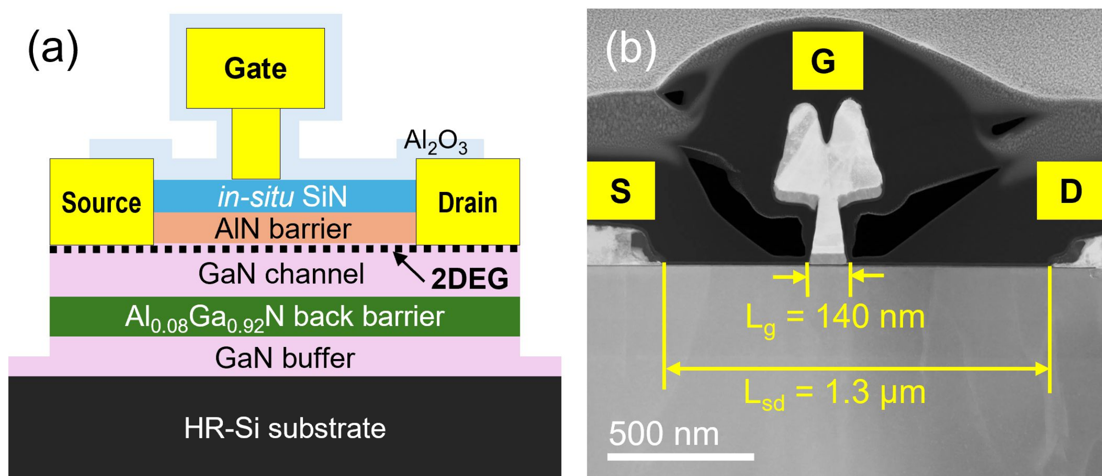
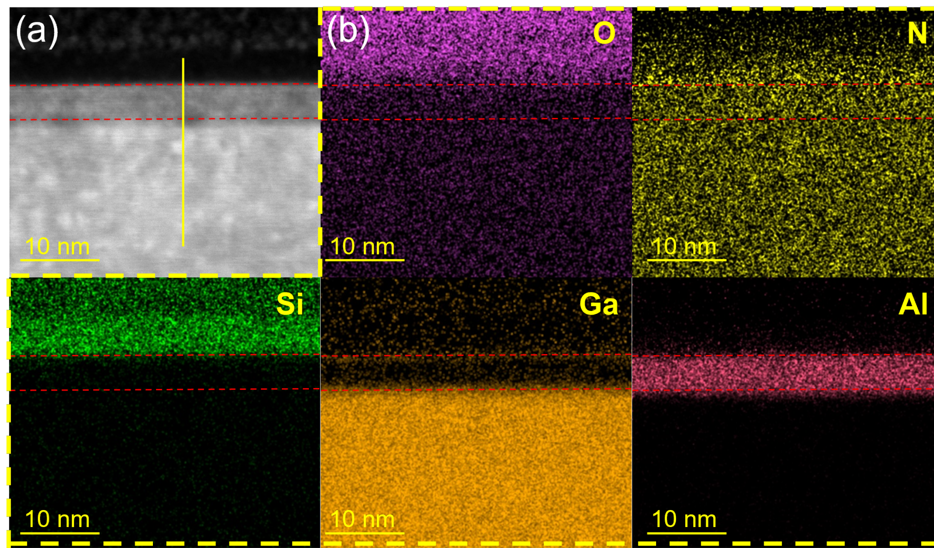


Fig. 4-4 Proposed AlN/GaN/AlGaN-on-Si MIS-HEMT. (a) Schematic. (b) Cross-sectional image obtained by transmission electron microscopy (TEM), showing Lg / Lgs / Lgd=140 / 480 / 680 nm, giving Lsd=1.3 μm.



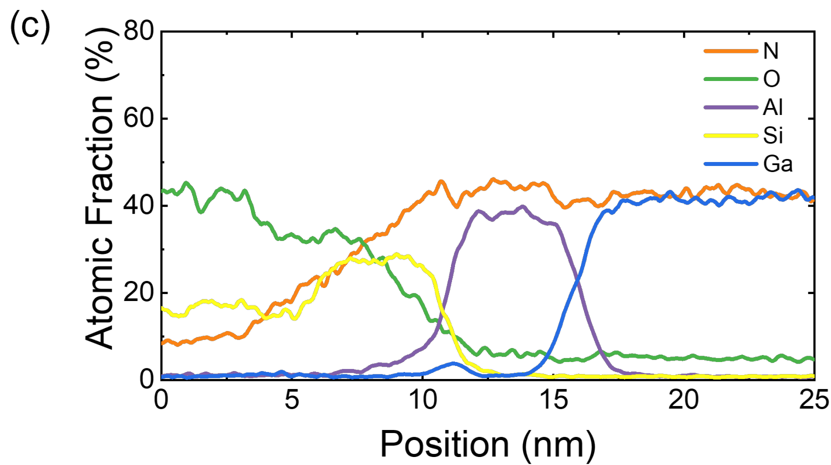


Fig. 4-5 STEM-EDXS mapping of in-situ SiN/AlN/GaN epitaxy. (a) cross-sectional STEM image (b) the corresponding EDXS mapping of Ga, Al, N, Si, O atoms. (c) Atomic fraction element profile as indicated by line scan

concentrations that indicate high-quality epitaxial growth. The AlN barrier has a nominal thickness of 5 nm and is treated as an ultrathin, high-bandgap barrier layer. Although this thickness is close to the reported critical thickness of AlN on GaN, its role in electron confinement remains effective.

The fabrication process begins with device isolation through mesa formation using Cl_2/BCl_3 inductively coupled plasma reactive ion etching (ICP-RIE). The metal stack Ti/Al/Ni/Au (20/120/40/50 nm) was deposited and underwent thermal annealing at 775 ºC in nitrogen environment for 30 seconds, yielding ohmic contacts with contact

resistance (R_c) of 0.3 Ω·mm. The T-shaped gates were defined by a bi-layer resist, and lift-off of Ni/Au (50/300 nm). After a quick dip in buffered oxide etch (BOE) solution, a thin layer of Al_2O_3 (10 nm) was formed by thermal atomic layer deposition (ALD) at 300 ºC. The ALD process offers advantages over PECVD approaches by avoiding plasma-induced damage to the device surface. Throughout the process, the preserved in-situ SiN serves as the gate dielectric and minimizes interface contamination and defect formation, resulting in lower D_{it} compared to ex-situ deposited dielectric [142], [143], [144]. Furthermore, the thin (14 nm) SiN/Al_2O_3 stack minimized the parasitic capacitances [145]. The reported transistor features L_g / L_{gs} / L_{gd}=140 / 480 / 680 nm, giving L_{sd}=1.3 µm (Fig. 4-4(b)). The gate periphery is 2×16 µm. The small finger width was intended to minimize signal propagation delay ("transverse delay") while maintaining low gate resistance, which is critical for minimizing RF signal attenuation along the gate finger and improving the maximum oscillation frequency (f_{max}) [146], [147].

4.4 Device Characterization

4.4.1 DC Characterization

DC I-V characterization of the in-situ SiN/AlN/GaN HEMTs were carried out using a Keysight B1500A Semiconductor Parameter Analyzer. The pulse characteristics were measured at room temperature using a Nanometric/Accent Optical Technologies DiVA D265 dynamic I-V analyzer. Fig. 4-6(a) shows the DC output characteristics of the proposed transistor. A maximum drain current (I_{dmax}) of 2.0 A/mm, and an ON-resistance (R_{on}) of 1.1 Ω·mm were achieved. Fig. 4-6(b) details the transfer characteristics, showing a threshold voltage (V_{th}) of −2.9 V (extracted at 1 mA/mm) and a decent I_{ON}/I_{OFF} ratio exceeding 10^5. The maximum

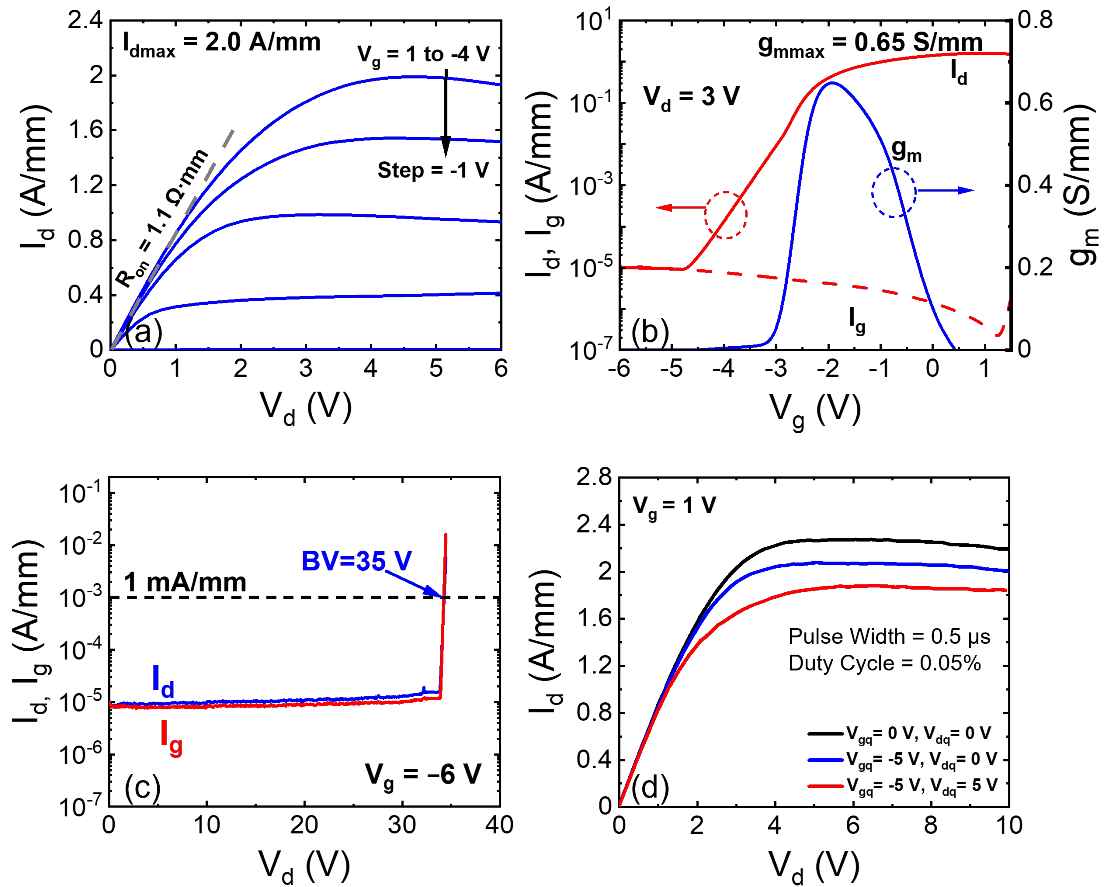


Fig. 4-6 DC characteristics. (a) Output characteristics, showing I_{dmax}=2 A/mm, and R_{on}=1.1 Ω·mm. (b) Transfer characteristics, showing g_{mmax}=0.65 S/mm. (c) Three-terminal breakdown characteristics. (d) Pulsed I-V characteristics.

transconductance (g_{mmax}) was 0.65 S/mm. The gate current (I_g) does not show significant increase at $V_g > 0$ V, which can be attributed to both the high Schottky barrier between the gate metal and AlN, and the additional barrier provided by the gate dielectric. Fig. 4-6(c) displays the three-terminal breakdown characteristics, showing a breakdown voltage of 35 V, where I_d and I_g rapidly increase. The breakdown mechanism is attribute to the impact ionization of carriers at the drain edge of gate, which lead to the sudden increase in both I_d and I_g currents [148], [149]. Pulsed I-V measurements were performed as shown in Fig. 2(d). The current collapse ratio for I_{dmax} is 8.6% and 15.2% at (V_{gq}, V_{dq}) = (−5 V, 0 V) and (−5 V, 5 V), respectively.

4.4.2 Small Signal Characterization

S-parameter measurements were conducted using a Keysight N5244-A PNA-X Vector Network Analyzer with frequency capabilities spanning from 1 MHz to 43 GHz at room temperature. The system calibration was performed using short-open-load-through (SOLT) calibration, and the parasitic pad effects were de-embedded using on-wafer open and short test structures, which allowed for the extraction of intrinsic device parameters unaffected by measurement system limitations or interconnect parasitic. As resented in Fig. 4-7, a cut-off frequency (f_T) of 112 GHz and a maximum oscillation frequency (f_{max}) of 205 GHz were achieved at V_d = 10 V.

The small-signal parameters were extracted to gain insights into the transistor performance. The small-signal equivalent circuit model (based on [150]) is presented in Fig. 4-7 (b). Good agreement was achieved between the measured and modelled values of f_T and f_{max}, with deviations of <6 % (Fig. 4-7 (c)).

Analysis of effective parasitic delay components in the AlN/GaN MISHEMT, based on the parameter extraction described above, indicates the channel charging time (τ_{RC} = 0.75 ps) is the dominant contribution among the delay terms listed Table 4.1. These combined delays (τ_{total} = 1.45 ps) directly correspond to the measured intrinsic cutoff frequency ($\tau_{total} = 1/2\pi f_T$), providing critical insights for optimizing high-frequency

performance by primarily targeting channel charging time reduction. This calculated f_T value of 110 GHz is aligned with measured (112 GHz) f_T values in the Table 4.1.

This consistency serves as a self-check of the delay decomposition and suggests that further improvement in high-frequency performance would primarily benefit from reducing the channel charging time, for example through optimized electrostatics and reduced access resistance.

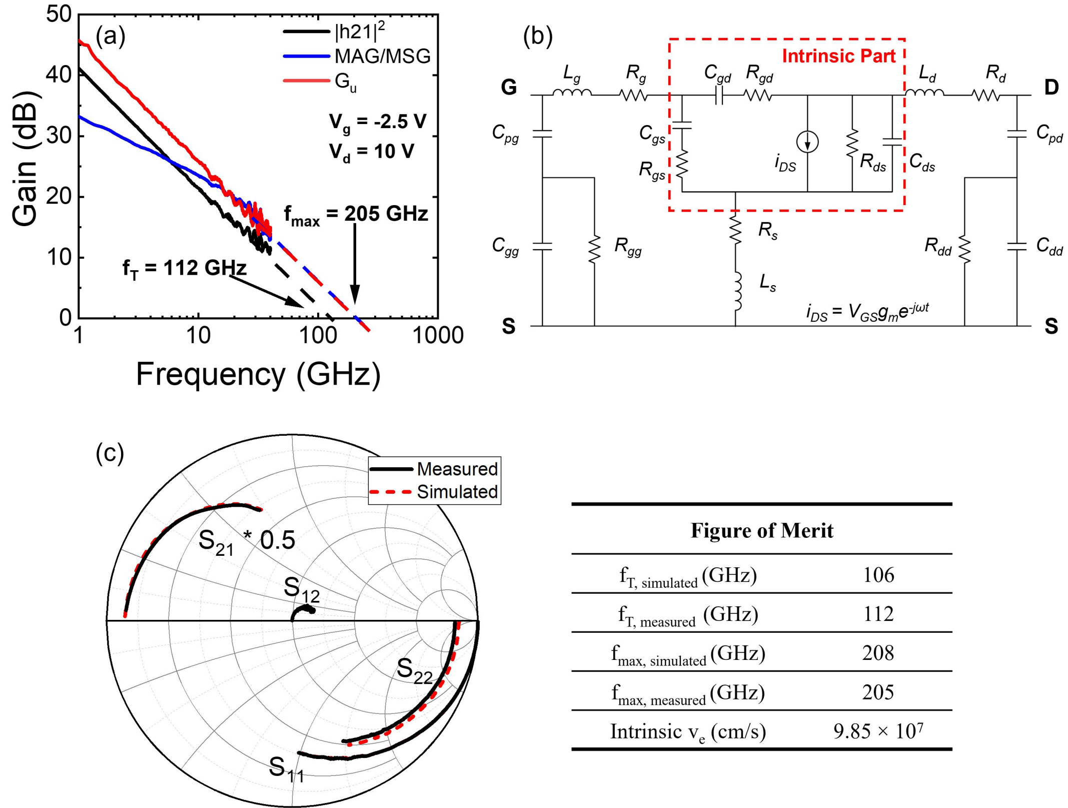


Figure of Merit	
$f_{T,\ simulated}$ (GHz)	106
$f_{T,\ measured}$ (GHz)	112
$f_{max,\ simulated}$ (GHz)	208
$f_{max,\ measured}$ (GHz)	205
Intrinsic v_e (cm/s)	9.85×10^7

Fig. 4-7 RF small-signal characteristics. (a) Small-signal current and power gain vs. frequency, showing f_T / f_{max}=112 / 205 GHz. (b) Small-signal equivalent circuit model. (c) Comparison of equivalent circuit modelling results and measured s parameters, showing a close fit of s_{11}, s_{12}, s_{21}, s_{22} (deviation of <5 %)

Table 4.1 The extracted parameters for AlN/GaN/AlGaN MISHEMTS on Si with $W_g = 2\times16$ µm, L_g = 120 nm and calculated delay components

L_g = 110 nm W_g = 2 × 16 µm	Bias Conditions V_{gs}/V_{ds} = -2.6/10V
R_{gs} (Ω·mm)	0.5
R_{ds} (Ω·mm)	12.5
R_{gd} (Ω·mm)	0.05
R_g (Ω/mm)	92
R_s (Ω·mm)	0.38
R_d (Ω·mm)	0.41
C_{gs} (fF/mm)	862.5
C_{ds} (fF/mm)	780
C_{gd} (fF/mm)	200.5
g_m (mS/mm)	710

Delay components	
τ_{RC} (ps)	0.08
τ_d (ps)	0.75
τ_{par} (ps)	0.16
$\tau_{transit}$ (ps)	0.46
τ_{total} (ps)	1.45
$f_{T,intrinsic}$ (GHz)	112
$f_{T,theoretical}$ (GHz)	110

4.4.3 Large signal characterization

The RF large-signal performance was characterized using an on-wafer D-band passive load-pull measurement system, as shown in Fig. 4-8 (a). The Keysight PNA-X (N5247B) was employed as the signal source, and the test frequency was upconverted to the D-band (110–170 GHz) using VNA extenders (VNAX, VDI WR6.5). Ground–signal–ground (GSG) probes with a 50 μm pitch (Infinity) were used for on-wafer measurements. The source and load reflection coefficients (Γ_S and Γ_L were controlled by computer-driven tuners (Focus W1701100BV) at the fundamental frequency of 123 GHz.

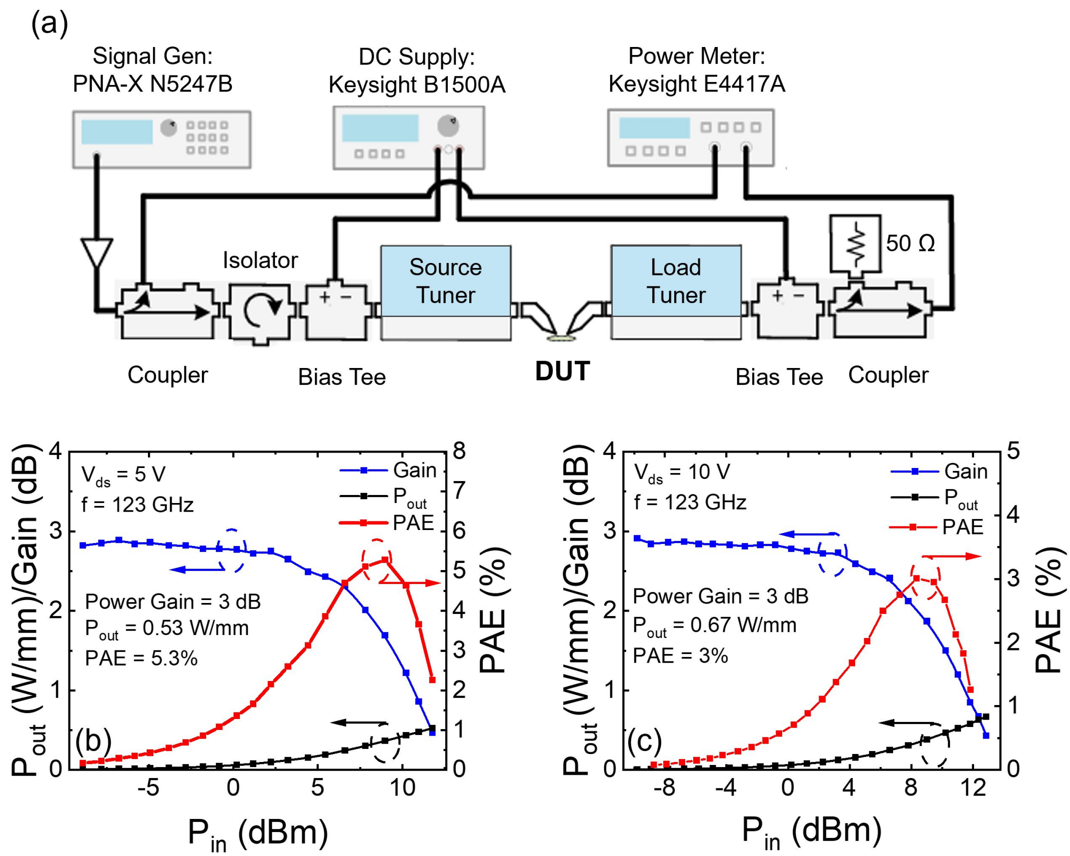
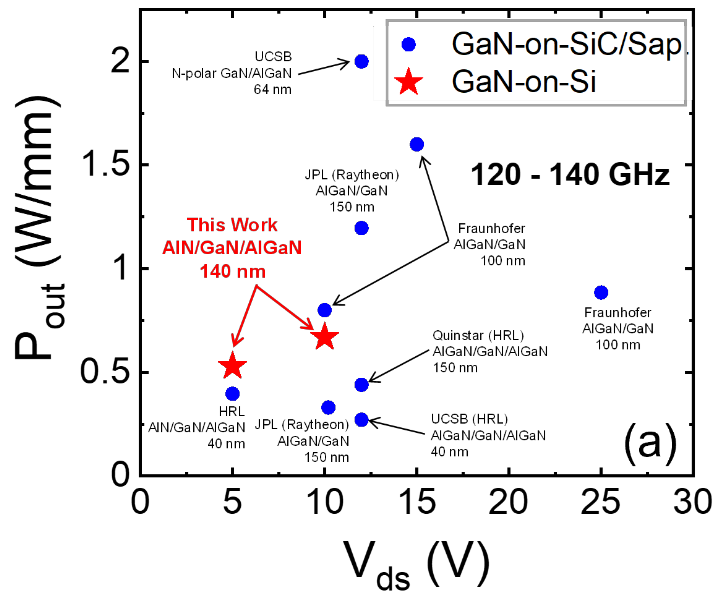


Fig. 4-8 RF large-signal performance at 123 GHz CW. (a) Measurement setup, which supports tuning at the fundamental frequency. (b) Power sweep results at V_{ds} = 5 V. A maximum PAE of 5.3 % was achieved at P_{out} = 0.36 W/mm. (c) Power sweep results at V_{ds}=10 V. A P_{sat} of 0.67 W/mm was achieved.

Prior to large-signal testing, a small-signal measurement configuration was established using the PNA-X and VNAX modules to verify device functionality and perform calibration. The calibration procedure sequentially included the VNAX modules, couplers, tuners, probes, power source, and power receiver, followed by a power calibration. After calibration, the system was capable of delivering an input power range from −10 to 10 dBm. However, this power level exceeded the requirement for accurate large-signal characterization of the designed power amplifier devices.

Therefore, a dedicated passive load-pull setup was implemented for large-signal measurements, in which the PNA-X served as the signal generator with an additional attenuator to precisely control the input power. The output power was measured using the VNAX receiver module. This load-pull configuration enabled systematic tuning of the source and load impedances under large-signal excitation, allowing accurate evaluation of output power, gain compression, and power-added efficiency of the D-band devices. As device size scales down, the required optimal load impedance moves closer to the edge of the Smith chart, placing more stringent demands on the achievable $|\Gamma|$ range of the load-pull system.

Fig. 4-8 (b) and (c) report the 123 GHz CW power sweep characteristics of Class AB operation ($I_{ds,Q}$=0.28 A/mm, 14 % of I_{dmax}) at V_{ds} = 5 V and V_{ds} = 10 V. When source impedance and load impedance points were tuned for optimal PAE points, the proposed transistor achieved a P_{sat} of 0.53 W/mm with an associated PAE of 2.3 % at V_{ds} = 5 V. Fig. 4-8 (c) show the results at V_{ds} = 10 V, the maximum P_{out} reaches 0.67 W/mm and peak PAE is 5.3 %.



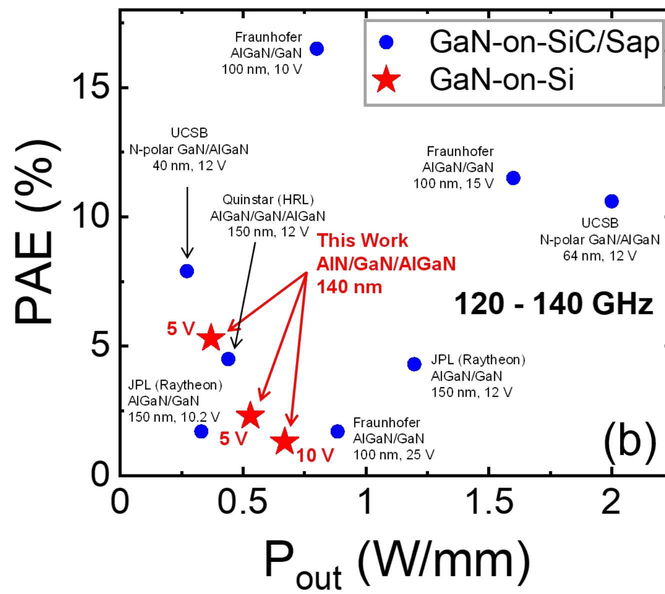


Fig. 4-9 Benchmark of RF large-signal performance of GaN HEMTs and MMICs at 120 – 140 GHz. (a) P_{out} vs. V_{ds}. The epitaxial structure and L_g are specified. (b) PAE vs. P_{out}. The L_g and V_{ds} are specified. The name of the foundry, if different from the publishing affiliation, is written in parentheses.

4.5 Contributions to GaN mm-Wave Development

The RF large-signal performance of the proposed transistor was benchmarked against that of published GaN HEMTs and MMICs in the frequency range of 120 – 140 GHz. MMIC designs typically involve optimizing multiple parameters, including bandwidth, gain, and stability, which may trade off with maximum achievable power and efficiency. Therefore, this comparison aims to provide technological context rather than a direct performance benchmark. As shown in Fig. 4-9(a) At the measured V_{ds} of 5 and 10 V, the proposed GaN-on-Si HEMT shows competitive performance relative to the earlier reported GaN-on-SiC HEMTs at the same V_{ds}. As presented in Fig. 4-9(b) The proposed GaN-on-Si HEMT achieved comparable PAE and P_{out} values to several reports based on GaN-on-SiC HEMTs. To the best of the authors' knowledge, these results represent the first demonstration of GaN-on-Si HEMTs for D-band power amplification (Fig. 4-10), representing a significant breakthrough beyond previous frequency limitations of GaN-on-Si HEMTs and opening new possibilities for future wireless communication systems. This is in addition to the

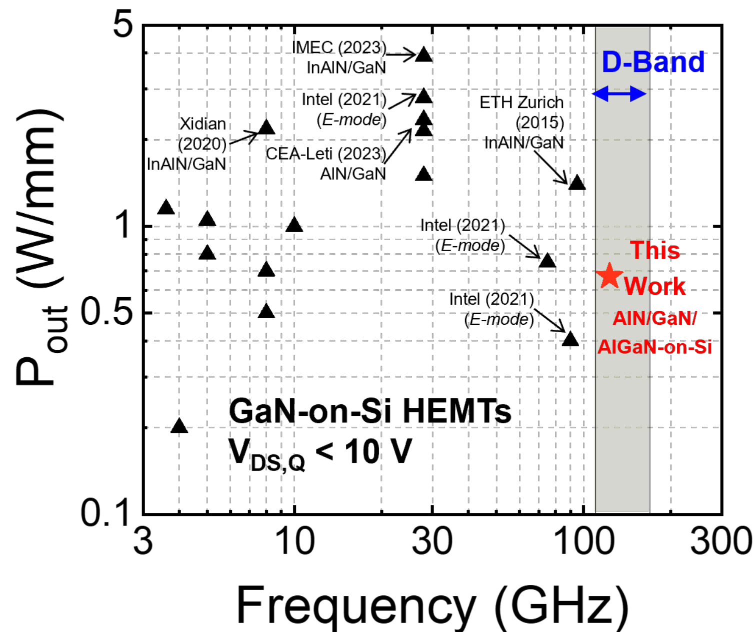


Fig. 4-10 The progress of GaN-on-Si HEMTs in terms of frequency.

numerous merits of GaN-on-Si HEMT technology, including availability of large wafer diameters, cost-effectiveness, and compact integration with Si CMOS.

Nevertheless, there remains significant room for improvement for GaN-on-Si HEMTs in power amplification at D-band and beyond. Notably, the PAE remains low (< 6%). Minimizing the parasitic channel, which originated from melt-back etching of Si, would reduce propagation loss to levels comparable to GaN-on-SiC. [133]. Device-level strategies, such as regrown contacts and improved passivation, would improve transistor performance. [132]. The optimum load and source impedances are found near the boundary of the tuner coverage, suggesting that the extracted performance is constrained by the achievable $|\Gamma_S|$ and $|\Gamma_L|$ at D-band. The use of active tuners are expected to further improve matching and performance, which would be beneficial for transistors of small gate periphery.

4.6 Summary

This work pushes the boundaries of GaN-on-Si HEMT technology by demonstrating its feasibility for D-band power amplification, for the first time. The proposed GaN-on-Si HEMT with L_g = 140 nm achieved I_{dmax} = 2.0 A/mm, and f_T / f_{max} = 112 / 205 GHz. P_{out} of 0.67 W/mm (V_{ds} = 10 V) was demonstrated at 123 GHz, which is the highest frequency in power amplification among published GaN-on-Si HEMTs. The maximum PAE of 5.3 % was achieved at P_{out} = 0.36 W/mm (V_{ds} = 5 V). With further optimization, GaN-on-Si HEMT technology is expected to emerge as a strong candidate for low-cost sub-THz cellular infrastructure in the 6G era.

Chapter. 5 Multi-channel AlN/GaN Schottky barrier diodes

5.1 Technology Development and Research Motivation

The pursuit of higher frequency performance in GaN-based HEMTs has primarily focused on lateral scaling and parasitic reduction strategies. However, as devices are pushed toward D-band and beyond, these conventional approaches begin to encounter fundamental physical limitations. This presents an opportunity to explore novel vertical architecture designs that could potentially overcome these barriers. While previous investigations of the AlN/GaN/AlGaN double heterojunction demonstrated promising results for both FR2 and D-band applications, the continuous drive for higher power density and improved frequency response necessitates exploration of more sophisticated channel engineering approaches.

Multichannel architecture offers several theoretical advantages. By distributing the current flow across multiple parallel two-dimensional electron gas (2DEG) channels, this approach could potentially increase the total current density while maintaining high electron mobility in each channel. This is particularly significant given that conventional single-channel devices often face a trade-off between carrier density and mobility due to increased scattering at higher carrier concentrations. The implementation of multichannel structures in the millimeter-wave HEMT technologies, while presenting significant fabrication challenges, provides insights through fundamental investigation of current transport mechanisms in the multichannel architecture. It should be clarified that, in this work, the lateral multi-channel diode is not intended as a stand-alone RF device. Instead, it is employed as a process-compatible lateral transport structure that shares the same epitaxial stack, channel configuration, and contact technology as scaled GaN HEMTs. By eliminating the gate electrode and its associated parasitic capacitances, this structure enables focused evaluation of contact resistance and channel transport mechanisms that are directly relevant to high-frequency GaN HEMT design.

The development of multichannel devices aligns with the broader trend in GaN technology toward more sophisticated vertical engineering solutions. Just as the introduction of the AlGaN back barrier improved carrier confinement in conventional HEMTs, the multichannel approach represents another step in vertical device architecture evolution. The fundamental current transport mechanisms in these structures prove crucial for evaluating their potential in future high-frequency applications.

Early reports on multi-channel III-N heterostructures have demonstrated promising performance in RF and power devices. [151], [152], [153], [154], [155], [156], [157], [158], [159], [160], [161], [162], [163], [164], [165], [166], [167], [168], [169], [170], [171], [172]. These III-N materials were specifically chosen for their strong piezoelectric polarization effects, which are crucial for enhancing the carrier concentration in the channels. The AlN/GaN multi-channel heterostructures exhibit several distinct advantages over conventional AlGaN/GaN and InAlN/GaN configurations. A single AlN/GaN heterostructure demonstrates higher polarization-induced charge density, as evidenced by the excellent performance of single-channel AlN/GaN HEMTs for RF applications [173], [174], [175]. Previous research has shown that a double-channel AlN/GaN heterostructure achieved a lower sheet resistance of 180 Ω/□, compared to 300 Ω/□ for a double-channel AlGaN/GaN heterostructure [176], [177]. Additionally, the thin AlN barrier enables excellent electrostatic control of the channels in the vertical direction, while the underlying AlN layer serves as a more effective back barrier to the channel above, ensuring excellent carrier confinement for multiple channels.

These technological developments indicate a shift in GaN device architecture, moving from conventional lateral scaling toward more sophisticated vertical integration strategies. The potential advantages of multi-channel structures, combined with the unique properties of AlN/GaN interfaces, present a promising direction for advancing high-frequency and high-power device performance beyond current limitations.

5.2 Issues on Current III-V Technology

5.2.1 Current Status on Single-Channel GaN HEMT

Despite remarkable advancements in gallium nitride (GaN) devices for RF and power applications, a major limitation persists in the limited current conduction capability of the single 2DEG channel. In general, increasing sheet carrier concentration tends to reduce mobility due to enhanced scattering; however, in polarization-based heterostructures this trade-off is strongly structure-dependent and can be partially mitigated by multi-channel designs, as illustrated in Fig. 5-1 [178], [179], [180]. This fundamental constraint has driven the proposal of multi-channel heterostructures as a solution, potentially enabling several-fold improvement in N_s without significantly compromising mobility, thereby emerging as leading candidates for high-power GaN RF and high-voltage devices. By spreading a large N_s into several vertically stacked channels, this trade-off can be overcome, which enables increasing Ns without impacting the mobility of the structure, thus achieving much reduced R_{sh}.

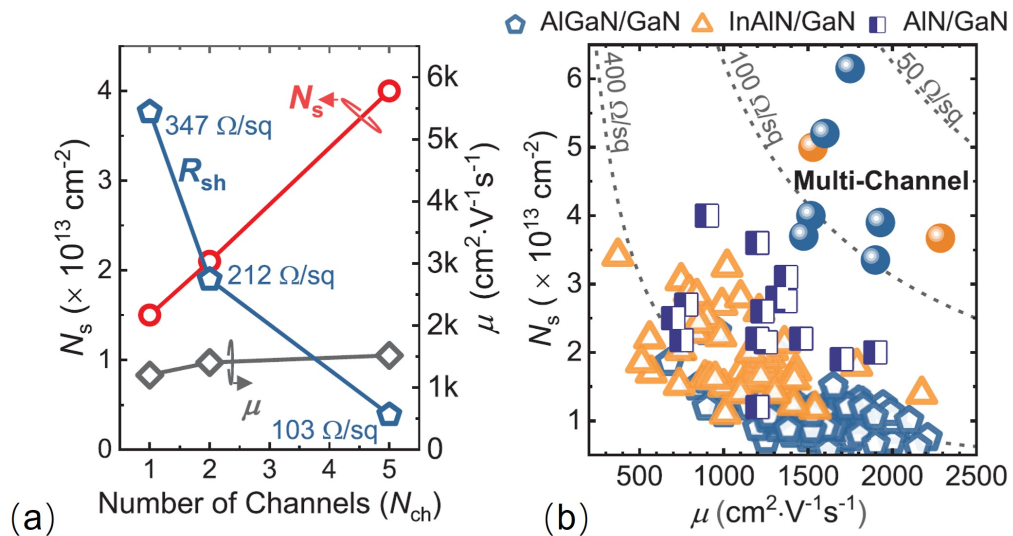


Fig. 5-1 (a) N_s, μ, and R_{sh} as a function of the number of channels in multi-channel structures. (b) N_s vs μ for single (hollow points) and multi-channel (solid points) heterostructures. [168].

5.2.2 Challenges in Multi-channel Implementation

Achieving optimal sheet resistance in multi-channel heterostructures requires careful engineering considerations. Various parameters can be modified, including the dimensions of barriers and channels, doping concentrations, and barrier compositions. When determining the ideal configuration, designers must ensure sufficient carrier population across all embedded channels while maintaining minimal stack thickness to streamline device fabrication processes [168].

Although promising in concept, multi-channel AlN/GaN heterostructures face unique challenges compared to their more extensively documented counterparts based on AlGaN/GaN and InAlN/GaN technologies. This is because the growth of high-quality AlN layers presents significant challenges compared to AlGaN layers, primarily due to the larger lattice mismatch between AlN and GaN. This mismatch can lead to higher dislocation densities and potential crack formation, especially as AlN layer thickness increases in multi-channel structures [181]. Cao et al. reported a 9-channel AlN/GaN (2.6/55.2 nm) heterostructure grown by molecular beam epitaxy (MBE), which showed a net N_s of 1.08×10^{14} cm^{-2} and sheet resistance (R_{sh}) of 37 Ω/□, corresponding to an average N_s of 1.2×10^{13} cm^{-2} and R_{sh} of 333 Ω/□ for a single channel [141]. No fabricated device was reported on this heterostructure. While the initial results are encouraging, several roadblocks remain in pushing multi-channel AlN/GaN technology for practical applications. The high-quality growth of this heterostructure by Metal-Organic Chemical Vapor Deposition (MOCVD) would be much desired, thanks to the high throughput of MOCVD. Moreover, process technology, including ohmic contact formation, would need to be developed for multi-channel AlN/GaN heterostructures to demonstrate electronic devices. Forming alloyed ohmic contacts with low contact resistance to AlN/GaN heterostructures could be more difficult due to the wider bandgap of AlN compared to typical AlGaN compositions. Therefore, higher annealing temperatures would be required for alloyed ohmic contacts, or regrown contacts would have to be used.

5.3 Device Fabrication

5.3.1 Epitaxial Growth and Material Analysis

The multi-channel heterostructure wafers were grown by Enkris Semiconductor using proprietary MOCVD processes. While detailed reactor conditions cannot be disclosed, the structural parameters and design principles relevant to device operation are summarized below. The epitaxial structure proposed in this work consists of (from top) 4.5 nm *in-situ* SiN cap, 5 pairs of (4.9 nm AlN barrier and 46.7 nm GaN channel), and 450 nm GaN buffer grown on 4 in. 4H-SiC substrate by MOCVD, as shown in Fig. 5-2 (a). The epitaxial structure is unintentionally doped. A cross-sectional view of the proposed epitaxial structure and its elemental compositions is shown in Fig. 5-2(b)–(e). Self-consistent Schrodinger-Poisson calculations indicate the presence of 5 layers of 2DEGs, therefore giving rise to 5 channels within the proposed epitaxial structure (Fig. 5-3 (a)) [182]. Extensive material characterization of the proposed heterostructure reveals high-quality material growth. Scanning transmission electron microscope (STEM) of the cross-section indicates that sharp interfaces between

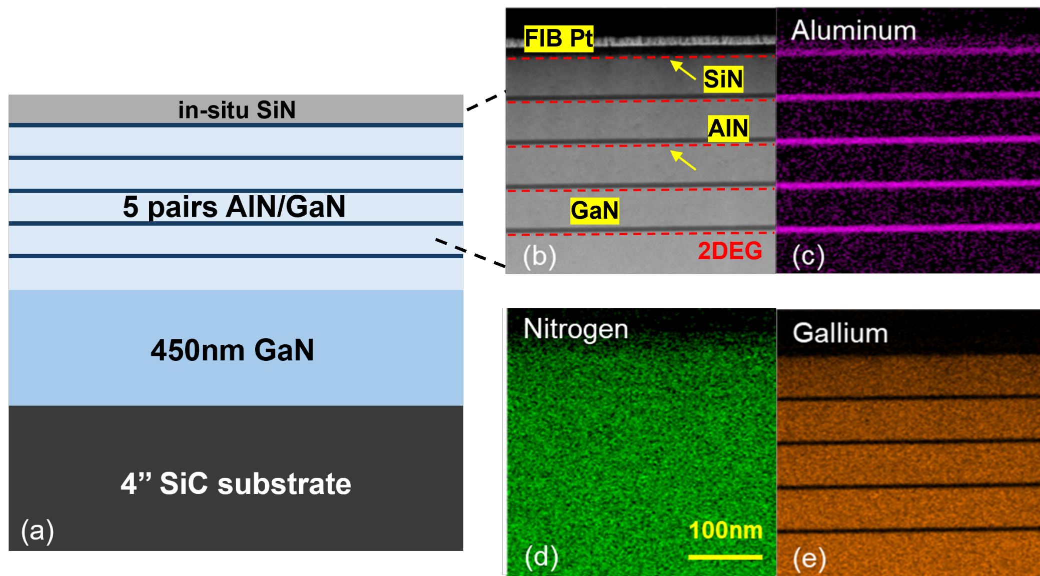


Fig. 5-2. Heterostructure and SBD demonstrated in this work. (a) Schematic of the epitaxy structure of the proposed 5-channel AlN/GaN heterostructure on 4" SiC substrate. (b) STEM image for the cross-section of the proposed heterostructure. (c)–(e) EDS elemental mappings of the proposed heterostructure.

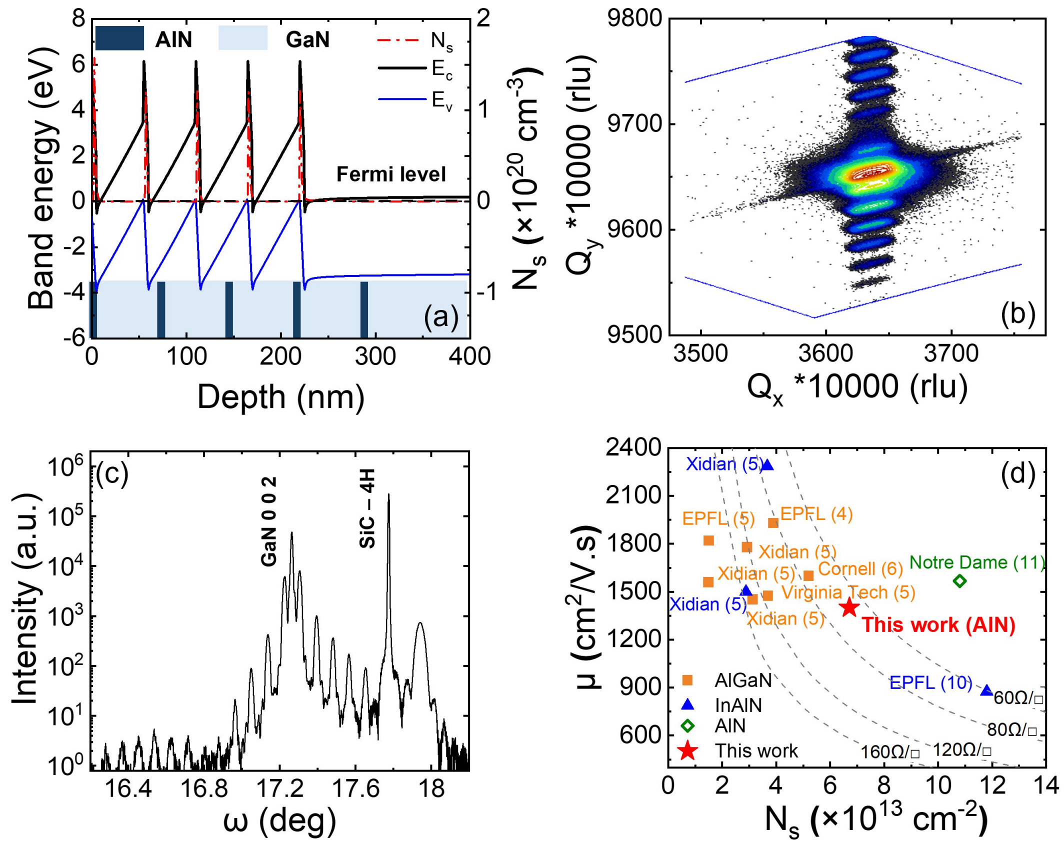


Fig. 5-3 (a) Band diagram and the calculated spatial distribution of polarization-induced charge. In the calculations, the heterostructure is assumed to be unintentionally doped. Material characterization of a 5-channel AlN/GaN heterostructure. (b) Reciprocal space mapping, and (c) Measured (002) GaN X-ray diffraction spectrum. (d) Benchmarking of N_s and μ (based on Hall measurements) for reported multi-channel III-nitride heterostructures. Solid symbols indicate that there are reports of fabricated devices on these heterostructures, such as this work, and hollow symbols indicate otherwise.

layers, as illustrated in Fig. 5-3(b). This observation is reinforced by the reciprocal space mapping (RSM) data presented in Fig. 5-3(c), where the high-resolution 2θ−ω scan around the (002) reflection for the proposed epitaxial structure shows well-defined, distinct peaks characteristic of high-quality epitaxial growth. The spectral analysis is characterized by a prominent GaN peak at 17.26°, stemming from the underlying GaN buffer layer. Notably, the presence of distinct superlattice satellite peaks provides strong evidence of the high quality and periodicity of the heterojunction interfaces, which indicates a well-ordered structure with consistent layer thicknesses and compositions throughout the multi-layer stack. Non-contact

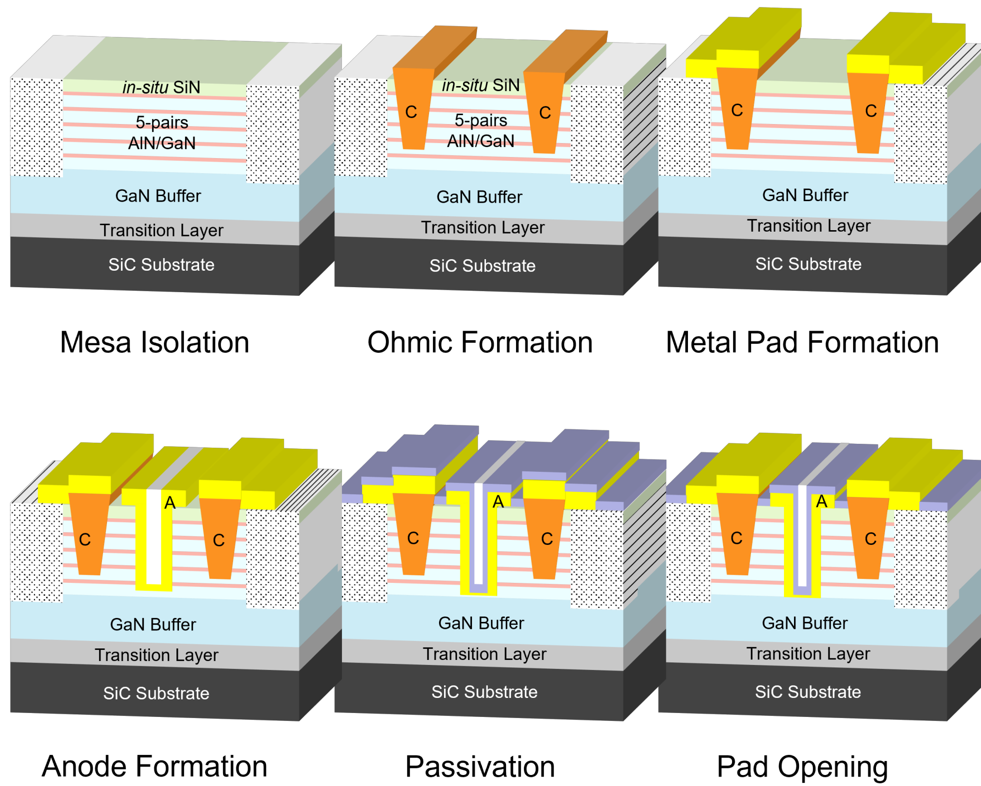


Fig. 5-4 Key fabrication Process of multi-channel AlN/GaN diode

(Lehighton) Hall-effect measurements of the proposed heterostructure indicate a total N_S of 6.7×10^{13} cm^{-2}, and μ of 1401 $cm^2/V\cdot s$ at room temperature, resulting in an extremely low R_{sh} of 69 Ω/□. The average N_S of 1.34×10^{13} cm^{-2} per channel is higher than the earlier report [174], thanks to the growth of a thicker AlN. A benchmarking of N_S vs. μ for multi-channel heterostructures is illustrated in Fig. 5-3(d).

Compared to other reports of multi-channel heterostructures based on AlGaN/GaN and InAlN/GaN in the R_{sh}=60~160 Ω/□ range, and on which devices were demonstrated, the proposed heterostructure exhibits a good balance between N_s and μ . The desired properties outlined above make the proposed heterostructure a promising candidate for GaN device demonstrations, which were subsequently pursued in this work.

SBDs were fabricated using the proposed heterostructure. As illustrated in Fig. 5-4, the process flow begins with the formation of alloyed ohmic contacts (cathode),

which is a challenge considering the multiple channels and AlN barrier. To this end, the ohmic recess process was developed for the proposed heterostructure. The ohmic recess area was then metallized by a standard Ti/Al/Ni/Au (20/120/40/50 nm) stack annealed at 800 ºC in N_2 ambient for 60 s. Next, fully recessed Schottky contacts (anode) were formed. The anode area was etched using Cl_2/BCl_3 plasma, therefore enabling direct sidewall contact between the 2DEG and the anode. Ni/Au (30/320 nm)

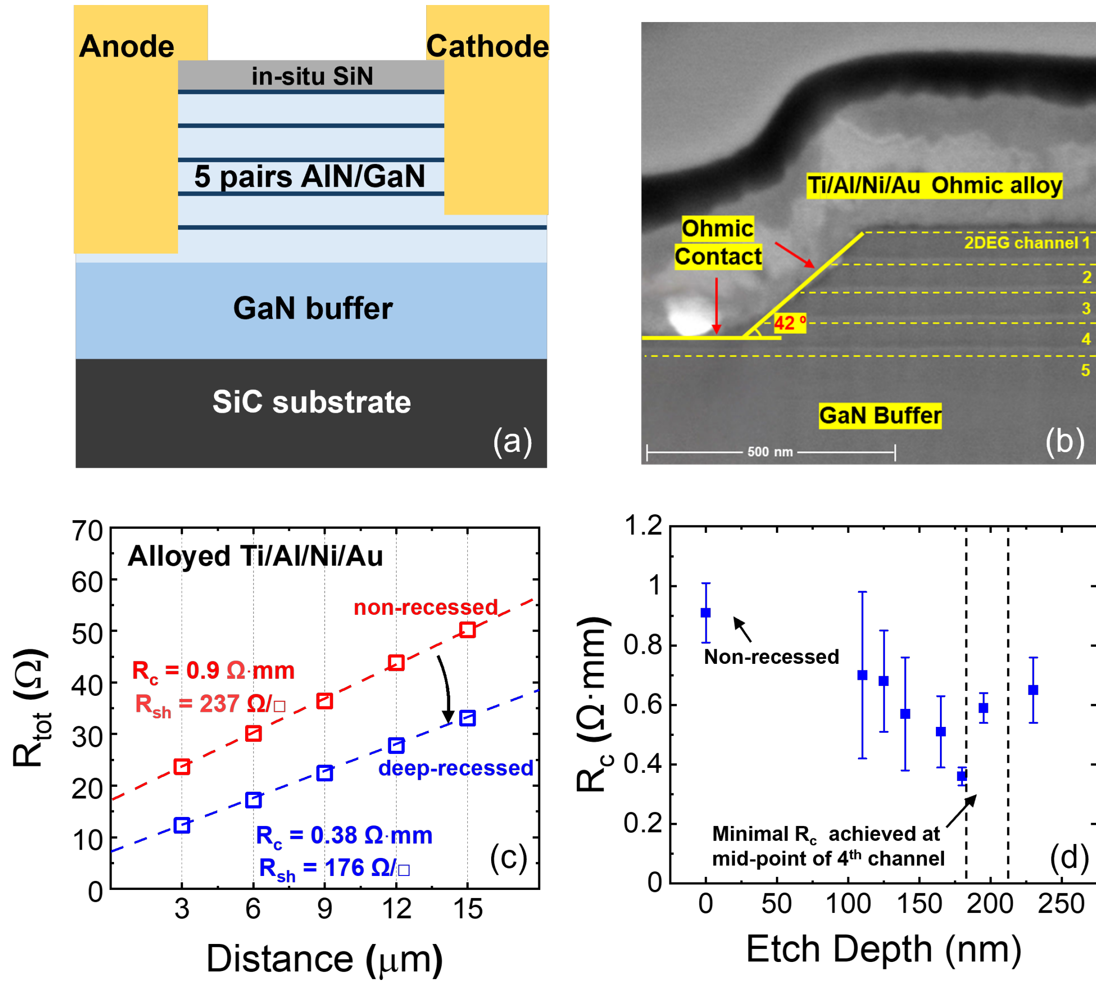


Fig. 5-5 Optimization of ohmic contact technology for the proposed heterostructure. (a) schematic illustration of the device structure based on the proposed five-channel AlN/GaN heterostructure, (b) Cross-sectional focused ion beam scanning electron microscope analysis of the ohmic contact with the sidewall angle. (c) Two sets of TLM data which illustrates the improvement in R_c after ohmic recess. (d) Impact of recess depth on R_c. A minimal R_c=0.38 Ω·mm was achieved after recessing to the mid-point of the 4th channel. The vertical dashed lines serve as a guide to the eye to indicate the location of the 4th channel. Device Processing and Contact Formation

was deposited using electron beam evaporation and patterned by lift-off technique. To recover the nitrogen vacancies caused by the etching process, a post-anode annealing process was conducted in N_2 ambient at 350 ºC for 5 min [183].

Fig. 5-5 presents a schematic illustration of the device structure based on the proposed five-channel AlN/GaN heterostructure, while Fig. 5-5 (b) provides a cross-sectional focused ion beam scanning electron microscope of the alloyed ohmic contact. An optimization of the ohmic etching depth was conducted and the contact resistance (R_c) extracted by the transmission line method (TLM) significantly reduced from 0.9 Ω·mm (as grown heterostructure, no recess) to 0.38 Ω·mm (deep recess down to 4th channel, measured from the top cap layer downward), as shown in Fig. 5-5 (c). In Fig. 5-5 (d), the optimal R_c was found to be with small peak-to-peak variation of 0.05 Ω·mm at an etch depth of 180 nm, which corresponds to the mid-point of the 4th channel. which indicated the effectiveness of ohmic recess in the proposed heterostructure. Any shallower or deeper recess resulted in higher R_c>0.5 Ω·mm.

The experimental results demonstrate that etching down to the 4th channel (from top) resulted in the lowest R_c. As illustrated in Fig. 5-5 (d), the device structure enables sidewall contact to 4 channels while maintaining top contact to one channel. Although contacting a larger number of channels would intuitively be expected to reduce R_c, the overall contact resistance is in practice dominated by the least efficient carrier injection path. The significant difference in R_c between four-channel (0.38 Ω·mm) and five-channel (0.64 Ω·mm) devices suggests that fully etching through all channels leads to a significantly higher R_c, which can be attributed to inefficient carrier injection into the bottom channel when relying predominantly on sidewall contacts.

In the fully etched five-channel configuration, the bottom channel is accessed mainly through sidewall interfaces, where the effective contact area is limited and the alloyed metal–semiconductor interface is less uniform than that formed on the top surface. This results in increased series resistance and effectively makes the bottom channel a current bottleneck. On the other hand, when the recess depth terminates within the 4th channel, a mixed injection geometry is realized: the bottom channel retains a top-surface ohmic contact with a larger effective contact area, while the upper channels

are accessed through sidewall contacts. This hybrid top-and-sidewall contact configuration improves the overall current injection efficiency, leading to the observed minimum R_c.

The relatively higher R_c observed in multi-channel devices compared with single-channel structures can be attributed to non-uniform current distribution among channels, additional vertical current spreading resistance, and inter-channel coupling effects, which collectively introduce an inherent trade-off between increased channel count and contact efficiency. Similar ohmic contacts with recess down to (but not including) the last channel has been reported [157]. Self-aligned ohmic contacts have been reported elsewhere [162]. Alternatives such as regrown contacts or ion-implanted contacts could be considered to enhance the effectiveness of ohmic contacts to multiple channels[184], [185], [186].

5.4 Device Characteristics

5.4.1 C–V characteristics

Fig. 5-6(a) shows the C–V characteristics measured on a lateral Schottky diode with a ring-shaped Schottky contact at 200 kHz. The extracted capacitance is governed by vertical depletion beneath the Schottky contact, similar to standard GaN HEMT gate C–V analysis. Five distinct turn-ons were observed in the C–V characteristics, confirming the existence of 5 channels and the formation of ohmic contact to these channels. The electron densities were calculated from C–V characteristics using the following equation:

$$N_A(D) = \frac{2}{q\varepsilon_0\varepsilon_s A^2 n}\frac{dV}{d(1/C^2)} \quad (5.\ 1)$$

where D is the depth into the heterostructure, C is the capacitance of reverse biased junction, ε_0 is the vacuum dielectric constant, ε_s is the dielectric constant of AlN, A is the area of Schottky contact electrode, and q is the elementary charge. Fig. 5-6(b) presents the carrier concentration (N_{3D}) estimated from C–V characteristics, which closely resembles the N_{3D} value obtained from the 1D Poisson-Schrodinger equation (Fig. 5-3(a)). In the Poisson- Schrodinger calculation, unintentional doping was

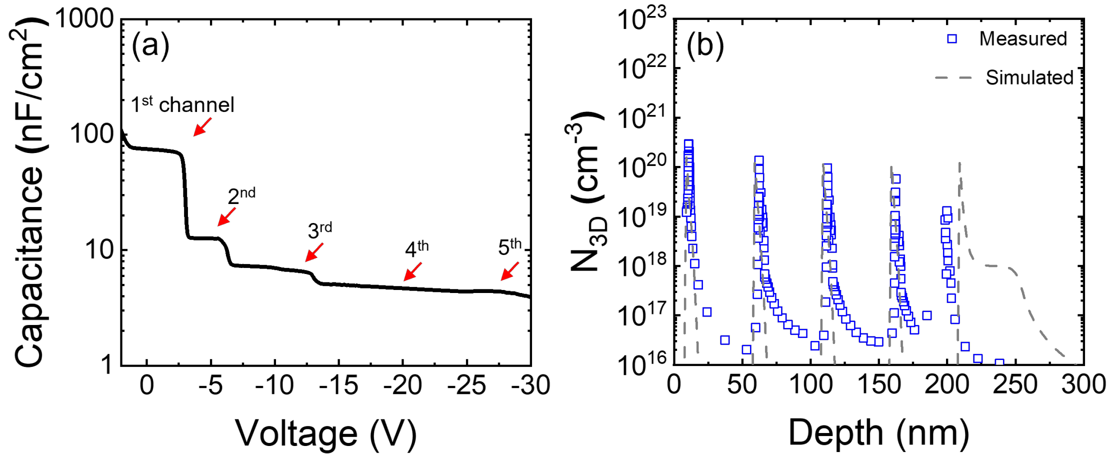


Fig. 5-6 (a) C–V characteristics of the proposed heterostructure, measured at a frequency of 200 kHz and an AC amplitude of 50 mV. (b) Spatial distribution of electrons among five channels in the proposed heterostructure as measured and simulated.

assumed. The total electron density in each channel (N_{2D}) is (2.9+1.4+0.9+0.6+0.2) $\times 10^{13}$ = 6×10^{13} cm^{-2}, which is close to the value obtained from the Hall-effect measurement (6.7×10^{13} cm^{-2}).

5.4.2 Forward and Reverse IV Characteristics

Fig. 5-7 (a) presents the forward characteristics of the multi-channel AlN/GaN SBDs with varying lateral anode-cathode distance (L_{AC}). The V_F at a forward current of 100

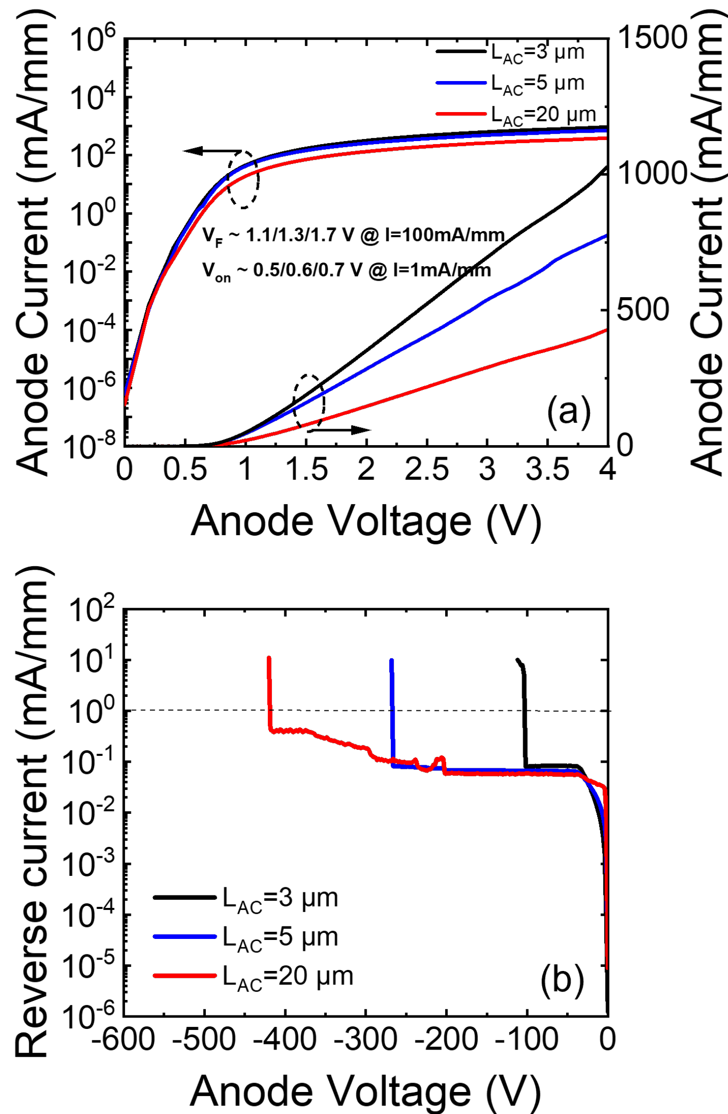


Fig. 5-7 (a) Forward I–V characteristics of the proposed devices with varying L_{AC}. (b) Reverse I–V characteristics of the proposed devices with varying L_{AC}.

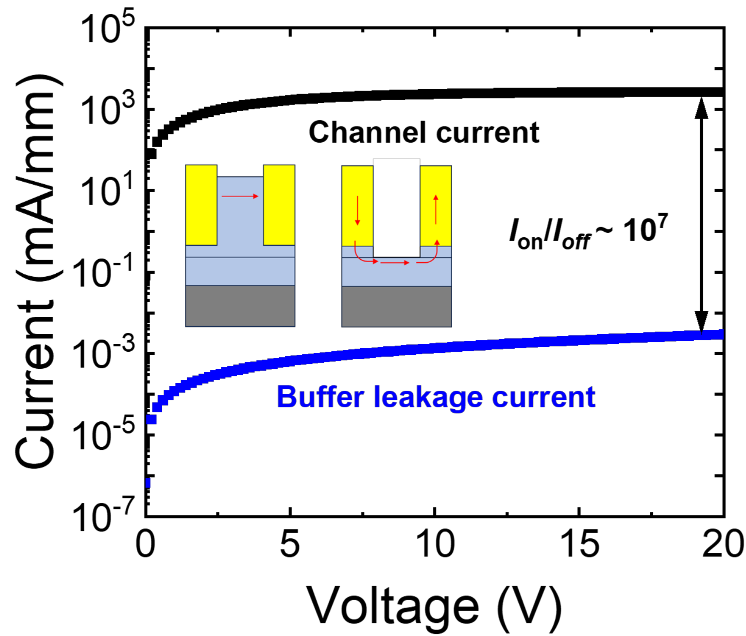


Fig. 5-8 Channel current and buffer leakage current. The corresponding device structures used to measure these currents are presented in the inset.

mA/mm is determined to be {1.1, 1.3, 1.7} V for L_{AC} = {3, 5, 20} µm, respectively. The existence of vertically stacked multiple channels significantly improves the current density of the proposed device, which achieved a peak forward current of 460 mA/mm for L_{AC}=20 µm. No significant V_F degradation was observed with increasing L_{AC}.

The reverse I–V characteristics is presented in Fig. 5-7(b). For devices with L_{AC} of 3/5/20 µm, the breakdown voltages (BV) are determined to be 104/268/422 V, respectively, as define by threshold current of 1 mA/mm. The relatively low breakdown field observed in these devices can be attributed to two major factors: (1) the absence of electric field management structures, such as field plates and guard rings, which leads to non-uniform electric field distribution and premature breakdown; (2) the multiple cycles of AlN/GaN growth may introduce material quality issues, resulting in increased dislocation density and interface states at the heterostructure interfaces, which significantly compromise the breakdown characteristics of the device. In addition to intrinsic multi-channel effects, the etched

anode/cathode process introduces sidewall states that contribute to leakage current, which is a known process-induced effect. The observed relatively low on-off ratio of 10^7 as illustrated in Fig. 5-8 is attributed to the optimized etching process, which minimizes surface defects and therefore leakage currents.

5.4.3 Analysis of Current Transportation

The temperature-dependent characteristics of a representative L_{AC}=3 μm SBD are reported in Fig. 5-9(a) At a temperature of 425 K, the on/off ratio, measured at 4 V and 0 V, is >10^6, which indicates the high quality of the Schottky interface. An increase in current under forward bias with increasing temperature was observed. Such a trend matches that of thermionic emission (TE); therefore, an initial attempt was made to apply the TE model [187]

$$J_{TE} = J_0\left[\exp\left(\frac{qV_F}{\eta k_B T}\right) - 1\right] \approx J_0 \exp\left(\frac{qV_F}{\eta k_B T}\right) \quad (5.\ 2)$$

assuming $qV_D \gg k_B T$, and J_0 may be expressed as

$$J_0 = AA^* T^2 \exp\left(-\frac{q\phi_B}{k_B T}\right) \quad (5.\ 3)$$

where J_{TE} is the forward current density by TE, J_{TE} is the saturation current, V_F is the forward voltage, A is the contact area, and A* is the effective Richardson constant. ϕ_B is the Schottky barrier height and η is the ideality factor [188]. To address the challenge of defining the contact area for a fully recessed anode, the Richardson plot of $\ln(1/T^2)$ vs. $1/kT$ was plotted and a linear fit was applied to the temperature ranges of 300–425 K to extract the effective contact area A_{eff}.

The values of ϕ_B (T) and η(T) as extracted from Equation. (5. 2) and (5. 3) are plotted in Fig. 5-9(b). ϕ_B exhibits slight temperature dependency, which is not anticipated by the TE model. Such a phenomenon is frequently attributed to the inhomogeneity of the metal/AlN barrier [189]. As the temperature increases, a noticeable reduction in η is observed, indicating a shift in the current transport mechanism from one assisted by defects or traps to a behavior more closely aligning with ideal TE model.

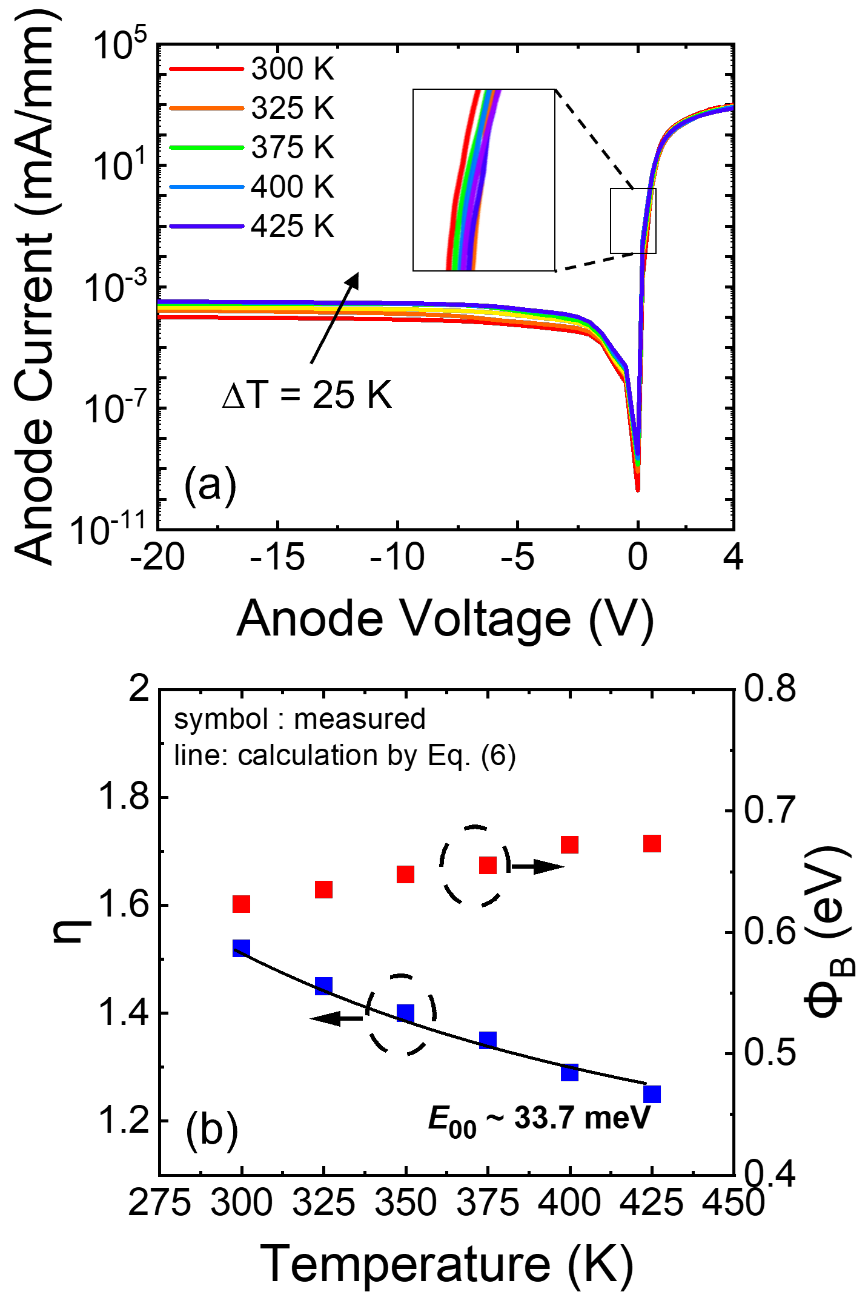


Fig. 5-9 High temperature (up to 125ºC) electrical characterization of a SBD with L_{AC}=3 μm. (a) Forward and reverse I–V characteristics in logarithmic scale. (b) Ideality factor (η) and Schottky barrier height (ϕ_B) as a function of temperature. The line indicates calculation of η by Equation 5. 2.

Furthermore, the deviation of η from unity at 300 K implies that there are mechanisms other than TE which would contribute to the current transport.

Another likely mechanism is tunnelling, which originates from the material defects, interface states, or the metal/AlN interface. Tunnelling current may be expressed as [190].

$$J_F = J_0 \exp\left(\frac{qV_F}{E_0}\right) \tag{5. 4}$$

where E_0 It is a tunneling parameter. However, it is necessary to separate the effect of tunneling from TE in Equation. (5. 2). Padovani and Stratton give the tunnelling current parameter. E_0 as follows [191].

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \tag{5. 5}$$

Therefore, the Ideality factor may be expressed as follows:

$$n = \frac{E_0}{kT} = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \tag{5. 6}$$

where E_{00} is defined as the characteristic energy quantifying the tunneling contribution in the conduction.

By fitting the experimental data using the Equation. (5. 6), it was determined that E_{00}=33.7 meV. The tunneling contribution increases with the increase of E_{00} value, resulting in higher ideality factors with a strong temperature dependence. The value of E_{00} calculated for the proposed heterostructure falls within the range of values for multi-channel GaN-based heterostructures reported in the literature (30–42.8 meV)[163], [187]. The E_{00} value of the proposed heterostructure is at the lower end of the range for multi-channel heterostructures. This suggests that, in the reported SBD (based on the proposed heterostructure), tunneling effects are less dominant than in other reports. This reduction in tunneling reflects the reduction in material and device imperfections in this work.

5.5 Contributions to GaN mm-Wave Development

This work presents several significant contributions to the field of GaN-based mm-Wave devices, particularly through the development and characterization of multi-channel AlN/GaN Schottky barrier diodes. The research advances our understanding in multiple key areas that are crucial for future mm-Wave applications.

First, this work demonstrates the successful implementation of a five-channel AlN/GaN heterostructure grown by MOCVD, addressing one of the fundamental challenges in multi-channel device development. The achievement of high-quality epitaxial growth with sharp interfaces and consistent layer thicknesses represents a significant step forward in material engineering for high-frequency applications.

Second, the development of an optimized ohmic contact formation process for multi-channel structures provides valuable insights for the broader GaN device community. The systematic study of recess depth effects on contact resistance offers practical guidelines for future device designs, while the demonstration of effective sidewall contacts to multiple channels presents a novel approach to accessing parallel conducting layers.

The characterization of transport mechanisms in multi-channel structures through diode measurements establishes important baseline knowledge for future mm-Wave device development. While this work focuses on Schottky barrier diodes, the findings regarding carrier transport and channel access strategies are directly applicable to the development of other mm-Wave devices, including HEMTs and advanced heterojunction devices.

Furthermore, the demonstration of low contact resistance (0.38 Ω·mm) in a multi-channel structure through optimized recess etching process addresses one of the key challenges in high-frequency GaN device development. This achievement provides a pathway for future work in developing more complex mm-Wave devices based on multi-channel architectures.

5.6 Summary

This chapter has presented a comprehensive investigation of multi-channel AlN/GaN heterostructures for high-frequency applications, with particular focus on the development and characterization of Schottky barrier diodes. Through careful material engineering and process optimization, this work demonstrates the successful implementation of a five-channel AlN/GaN heterostructure grown by MOCVD, achieving high-quality interfaces and consistent layer periodicity throughout the structure. The material quality is evidenced by the exceptional electrical characteristics, with the heterostructure exhibiting a low sheet resistance of 69 Ω/□ and high total carrier density of 6.7×10^{13} cm^{-2}, corresponding to an average of 1.34×10^{13} cm^{-2} per channel. The fabricated SBDs demonstrate promising performance metrics, including a turn-on voltage of 0.5 V, barrier height of 1.1 V, current density of 1050 mA/mm, and breakdown voltage of 104 V at L_{AC} = 3 μm. Temperature-dependent current-voltage characteristics reveal the presence of both thermionic emission and tunnelling mechanisms in current transport, providing valuable insights into carrier behavior in multi-channel structures. The achieved contact resistance ranks among the lowest reported for multi-channel heterostructures, validating the effectiveness of the optimized fabrication process. While this work focuses on diode structures, the findings regarding material growth, contact formation, and carrier transport establish important foundations for future development of high-frequency GaN devices. With continued optimization of device design and fabrication processes, multi-channel AlN/GaN technology shows promise for pushing the boundaries of GaN RF and power electronics performance.

Chapter. 6 GaN HEMTs using GaN-on-Insulator Technology via 200 mm Wafer Bonding

6.1 Technology Development and Research Motivation

In the realm of future wireless communication, there is an emerging trend towards higher operating frequencies, particularly the shift to millimeter -wave (mm-wave) technology, in response to the increasing demand for devices with high-power, high-speed, and improved efficiency. To realize this technology, III-Nitrides HEMTs offer best solutions [192], [193], [194]. Recently, InAlN/GaN heterostructure has been explored as a highly promising alternative to AlGaN/GaN-based HEMTs, primarily due to its strong spontaneous polarization that leads to increased carrier densities while supporting gate length shrinkage—critical aspects for high-power RF applications.[129], [130], [195].

The integration of GaN HEMTs with CMOS technology on a unified silicon platform represents a significant opportunity to revolutionize wireless communication systems. This heterogeneous integration would enable comprehensive system-on-chip solutions that combine the high-frequency power capabilities of GaN with the high-density digital signal processing of CMOS. Such integration offers multiple system-level benefits, including reduced form factor, decreased parasitic inductances through shortened interconnects on-chip and chip-to-chip interconnects, lower packaging costs, and enhanced signal integrity. Furthermore, integrated GaN-CMOS platforms could enable advanced power management schemes, and reconfigurable RF front-end architectures—features that are increasingly critical for next-generation wireless systems [196], [197].

While the previous chapters covered our work on pushing GaN HEMT performance for high-frequency applications—from low-voltage Ka-band operation to D-band power amplifiers, as well as multi-channel designs to overcome limitations of single-channel devices, these advancements have primarily focused on enhancing the frequency and power capabilities of GaN technology. The ultimate integration of

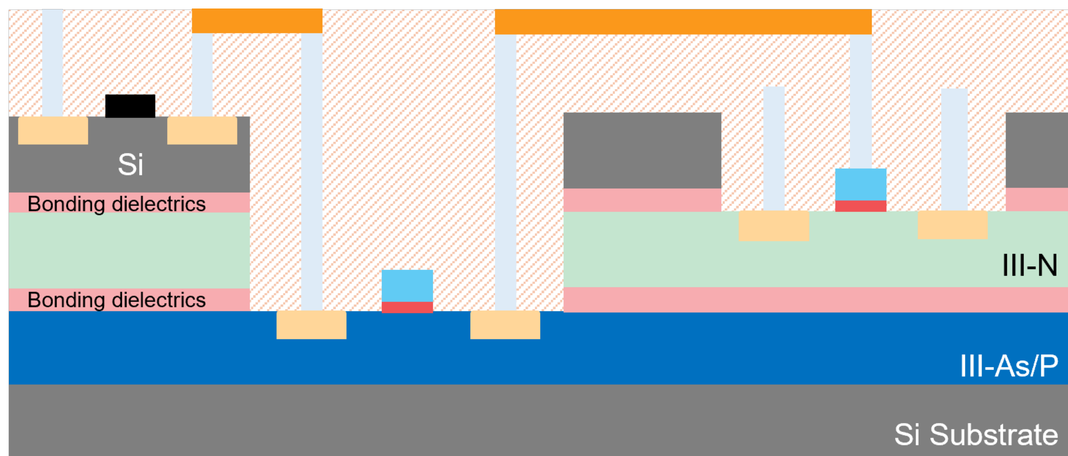


Fig. 6-1. The schematic illustrates the integration of Si-CMOS, RF devices, and potential high-power devices, comprising HEMTs on both III-N and III-As/P layers, onto a single wafer forming a hybrid substrate

these high- performance devices into practical systems represents another critical dimension of development. At mm-wave frequencies, this transition is increasingly governed by interconnection parasitics and integration constraints rather than intrinsic device limits alone.

Compared with CMOS technology, GaN's superior power-handling capacity delivers significant advantages in mm-Wave applications. Nevertheless, the integration of GaN HEMTs into the CMOS platform poses substantial technical challenges. This integration barrier arises from multiple specific factors: First, conventional GaN-on-Si epitaxial growth requires high temperatures (>1000°C) that exceed the thermal budget of CMOS processes. Second, the thick transition layers (typically 1−5 μm) needed to accommodate lattice mismatch create significant topographical variations that complicate subsequent lithography and interconnect formation. Third, these buffer layers introduce thermal resistance that impedes heat dissipation in high-power applications. Finally, potential cross-contamination between GaN and Si process modules presents additional manufacturing complexities [198], [199].

An innovative approach to overcome these challenges is the heterogeneous integration of GaN HEMTs and Si CMOS through GaN-on-Insulator (GaNOI) technology, employing wafer bonding methods [200]. The process of multilayer

transfer facilitates the coalescence of diverse materials from Group IV and Group III–V onto a single Si platform. The primary advantage of this technique is the ability to harness distinct material functionalities within a unified silicon framework, enabling the integration of Si-CMOS logic, high-frequency GaN devices, and high-power components on a single wafer, as illustrated in Fig. 6-1. While reported literature to date primarily focuses on AlGaN/GaN HEMT GaNOI devices for high breakdown voltage power applications [201], its implications for interconnect parasitics, RF signal integrity, and high-frequency device operation remain largely unexplored. The thermal characteristics of the GaNOI structure, particularly the thermal conductivity of the insulator material, are crucial for efficient heat dissipation, thereby contributing to enhanced performance and reliability. GaNOI technology offers numerous additional benefits, including complete electrical isolation, improved electrostatic control, and greater device scalability. By utilizing wafer bonding technology, challenges like cross-contamination are effectively mitigated, paving the way for mass production by leveraging established Si-CMOS manufacturing infrastructure and business models [192], [198], [202].

This chapter investigates how GaNOI technology influences the DC and RF characteristics of InAlN/GaN HEMT devices, contributing to our understanding of its potential advantages in high-frequency applications. Rather than performing a direct device-to-device performance comparison with previously reported HEMTs, the analysis emphasizes the impact of wafer bonding on material quality, channel transport, and RF integrity. Our detailed material characterizations reveal a significant reduction in lattice strain (5%) and modifications in crystalline defects. These structural improvements enhance the mobility and sheet resistance properties of the InAlN/GaN heterostructure, resulting in no observable RF performance degradation and, in some cases, modest improvements, consistent with the benchmarking results presented in this chapter.

6.2 Advantages and Challenges of Bonding Technology

6.2.1 Thermal Management Analysis of GaNOI Structure

The RF performance of GaN-on-Si HEMTs is significantly constrained by their thermal characteristics, particularly when compared to GaN-on-SiC devices. This thermal limitation stems from two fundamental physical mechanisms. First, the thermal conductivity of Si substrates (approximately 1.5 W/cm·K) is substantially lower than that of SiC substrates (up to 3.8 W/cm·K) [203]. Second, the large lattice mismatch between GaN and Si necessitates thick transition layers, which exhibit poor thermal conductivity due to high dislocation density [92], [204], [205]. These transition layers, typically comprising either multiple AlGaN layers with varying Al composition or GaN/AlN super-lattices, create additional thermal barriers in conventional GaN-on-Si structures. The proposed GaNOI structure addresses these thermal challenges through a novel approach: eliminating the transition layers and transferring the essential GaN layers (barrier, channel, and buffer) onto a new Si substrate using wafer bonding technology. However, this solution introduces its own thermal consideration - the thermal conductivity of the bonding interface. Our

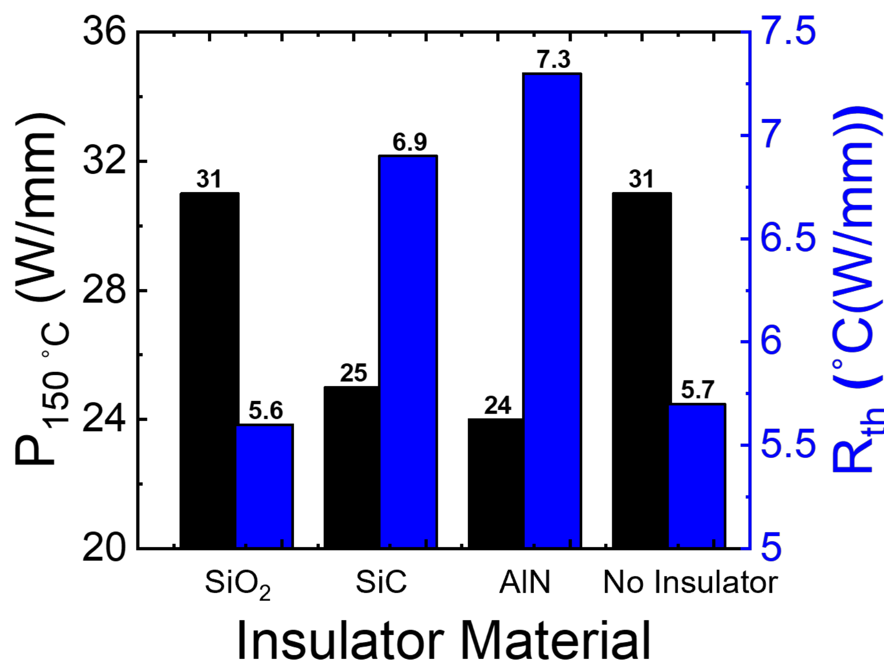


Fig. 6-2 Comparison of the heat dissipation power density at channel temperature of 150 ºC [157].

previous studies [201], [206] revealed that while SiO_2 bonding layers provide excellent electrical isolation, they create a thermal bottleneck due to their low thermal conductivity.

3-dimensional electrothermal simulations using ATLAS (Silvaco TCAD) were conducted to understand these thermal effects. The simulation employed temperature-dependent thermal conductivity for all device regions, following the relationship:

$$k(T) = k_{RT}(300/(273 + T))^{\alpha}$$

where k_{RT} represents the room temperature conductivity, and α denotes the characteristic power index. The thermal resistance of a device is defined as:

$$R_{th} = \frac{T_j - T_R}{P_{dis}}$$

where T_j is the junction temperature when the device temperature reaches steady state, T_R is the reference point temperature and assumed to be room temperature, and P_{dis} is the heat dissipation power. With the silicon substrate's bottom surface maintained at 300 K, the simulations compared heat dissipation capabilities with different device structures at a channel temperature of 150 ºC and extracted R_{th} value were extracted and displayed in Fig. 6-2 [207].

Recent advances in bonding technology have demonstrated promising solutions to the thermal management challenge. Reported study highlights the critical role of dielectric material thermal conductivity and process quality in the thermal management of GaNOI-on-Si HEMTs. Due to the low thermal conductivity of amorphous SiC/AlN films, thickness variation has minimal impact on heat dissipation, while increasing the thickness of SiO_2, which has a much lower thermal conductivity, exacerbates heat accumulation. Thus, optimizing the crystalline quality of dielectric materials is more effective than merely increasing their thickness. In Fig. 6-2, the replacement of SiO_2 with AlN as the bonding layer has shown significant improvements in thermal dissipation, increasing the maximum power dissipation from 5.6 W/mm to 7.3 W/mm. This enhancement brings the thermal performance of GaNOI structures better than that of traditional GaN-on-Si devices, suggesting that

high power density operations are achievable while maintaining device integrity. Based on this understanding, our future GaNOI designs will incorporate high-quality AlN as a bonding layer to enhance thermal management performance.

6.2.2 Process Integration Challenges in GaNOI Bonding Technology

The implementation of wafer bonding technology in GaNOI fabrication presents several critical process integration challenges that need to be carefully addressed. Surface preparation plays a crucial role in achieving high-quality bonding interfaces. The GaN surface, particularly after epitaxial growth, often exhibits microroughness and potential contamination that can significantly impact bonding quality. To achieve void-free bonding, stringent surface cleaning protocols and chemical mechanical polishing (CMP) processes must be developed while ensuring minimal damage to the GaN active layers.

Temperature compatibility poses another significant challenge in the bonding process. While higher temperatures typically enhance bonding strength, the thermal budget must be carefully controlled to prevent degradation of the GaN heterostructure and maintain the integrity of the 2DEG channel. The thermal expansion coefficient mismatch between GaN, the bonding layer (whether SiO_2 or AlN), and the handling substrate can introduce additional stress during the high temperature bonding process, potentially leading to wafer bow or crack formation.

The choice of bonding interface material presents a complex trade-off between process compatibility and device performance. While AlN offers superior thermal conductivity compared to SiO_2, its implementation as a bonding layer requires more sophisticated process control. The deposition conditions of AlN must be optimized to achieve both adequate surface activation for bonding and optimal thermal properties. Additionally, the interfacial oxide formation during AlN deposition needs to be minimized to maintain its thermal advantages.

The scaling of the bonding process to larger wafer sizes introduces additional challenges in maintaining uniform bonding strength and preventing void formation across the wafer. The requirement for precise alignment during bonding becomes more demanding with increasing wafer size, particularly for devices requiring critical back-side processing. Furthermore, the substrate removal process after bonding must be carefully optimized to prevent damage to the transferred GaN layer while ensuring complete removal of the growth substrate.

These integration challenges highlight the need for comprehensive process optimization and careful consideration of material interfaces in GaNOI fabrication. Future developments in bonding technology will need to focus on enhancing process robustness while maintaining compatibility with existing semiconductor manufacturing processes.

6.3 Device Fabrication

The $In_{0.17}Al_{0.83}N$/GaN HEMTs epitaxial structure is grown on a 200 mm high-resistivity (HR) silicon substrate by metal-organic chemical vapor (MOCVD) system. From top to bottom, the structure consists of a 10-nm-thick InAlN barrier, a 0.8-nm-thick AlN spacer layer, a 1-μm- thick GaN channel layer, a 300-nm-thick GaN buffer layer. The fabrication process starts from a SiO_2-SiO_2 double bonding and layer transfer process, facilitating the substitution of the original Si (111) substrate with a new Si (100) substrate. The methodology for preparing a GaNOI-on-Si wafer is

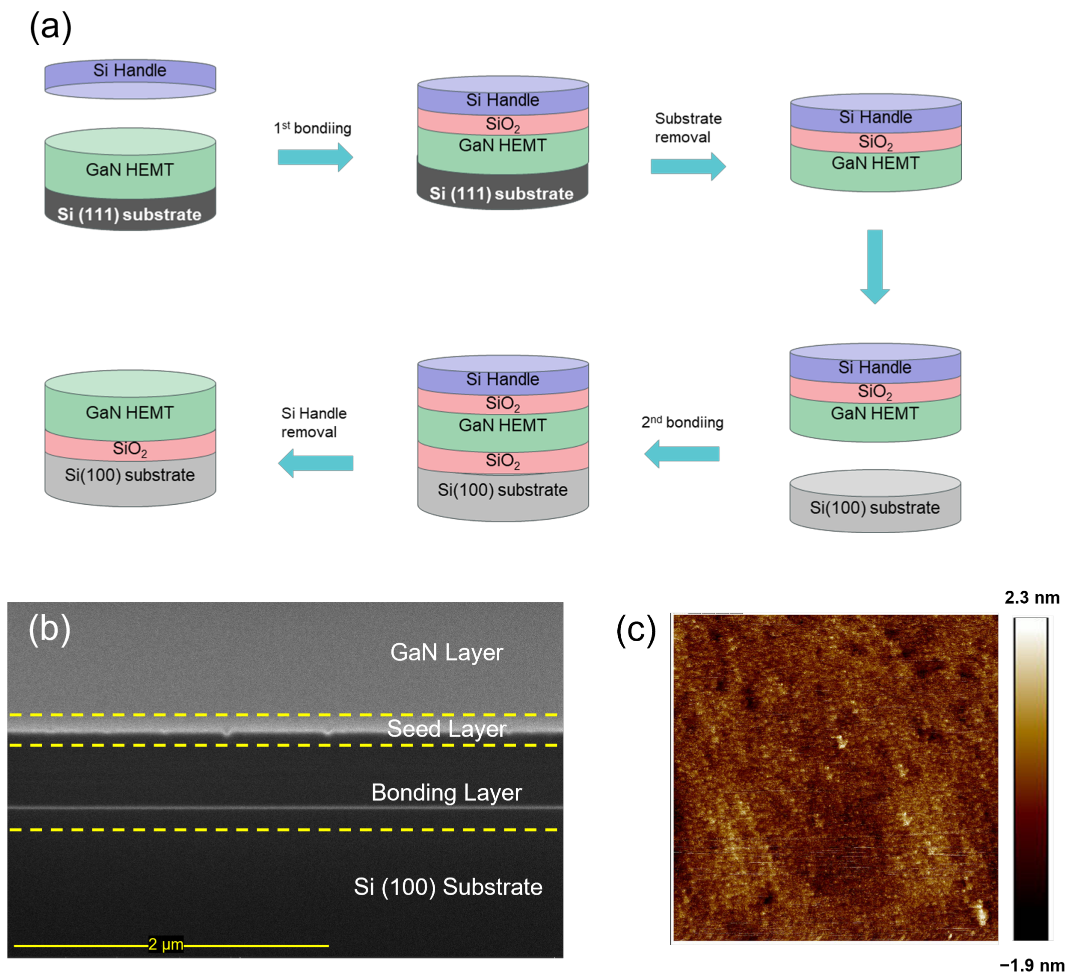


Fig. 6-3 (a) Schematic diagram of the GaNOI-on-Si wafer fabrication flow. (b) Cross-sectional TEM image illustrating the layered structure of a GaNOI wafer, including the GaN buffer, seed layer, bonding material, and new Si substrate. (c) AFM Characterization of Surface Topography Following the Bonding Process for the 10×10 μm^2 scan.

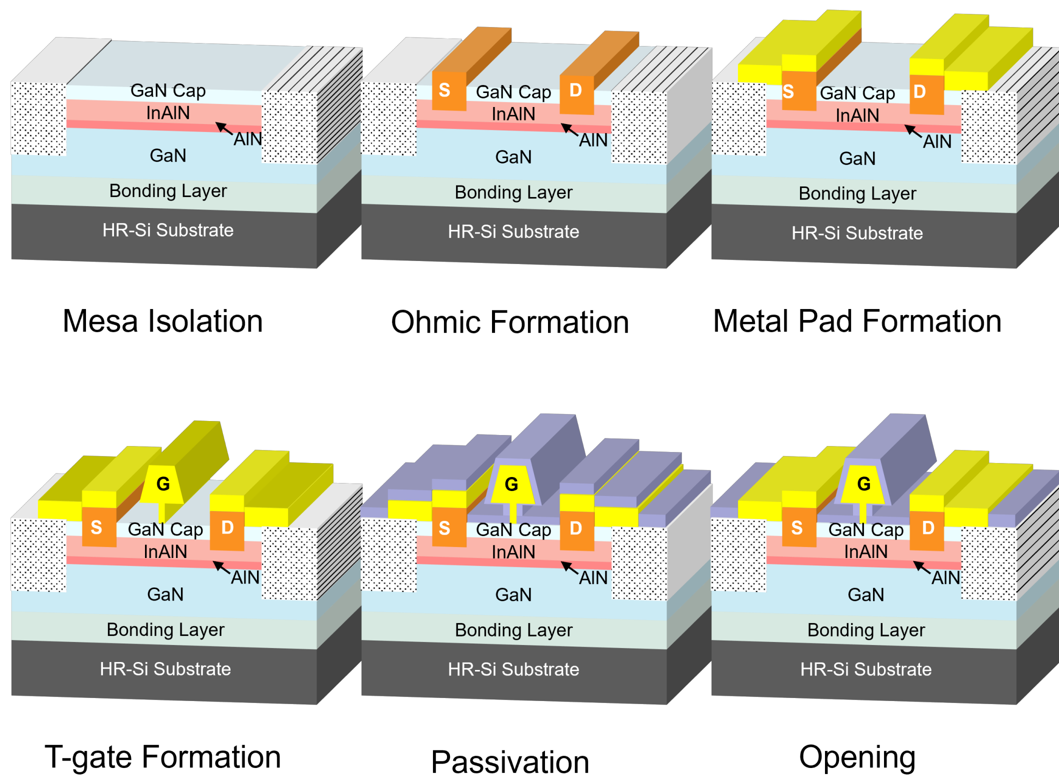


Fig. 6-4 Key fabrication processes for InAlN/GaNOI HEMTs

detailed in Fig. 6-3 (a). During the bonding procedure, two Si wafers underwent a pre-cleaning step to eliminate any organic and metallic impurities, namely(i) the Si handle wafer and (ii) the Si (100) substrate. This was succeeded by the deposition of a 200 nm SiO_2 through plasma-enhanced chemical vapor deposition (PECVD). The initial bonding stage involved the GaN HEMT wafer and the thermally oxidized Si handle wafer. Following the first wafer bonding, the original Si substrate was thoroughly eliminated by mechanical grinding and wet etching in tetramethylammonium hydroxide (TMAH) solution. The impact of deposition and oxide layer etching on the InAlN/GaN layers during the first bonding process is negligible in terms of altering the 2DEG properties. The GaN HEMT wafer and Si (100) substrate wafer were deposited with 200 nm oxide by PECVD. The densification process was performed at 600°C for 5 hours in a nitrogen (N_2) environment, aimed at eliminating the residual gas molecules and by-products trapped in SiO_2 during oxide deposition. Following densification, CMP was

employed to smoothen the PECVD oxide layer, preparing it for the second bonding process. The bonded wafer pair underwent a post-bonding annealing process at 300 °C in an N_2 ambient for 3 hours to further enhance the bond strength. After the second bonding process, the Si handle wafer was removed through mechanical grinding and wet chemical etching. The TEM image of wafer cross-sectional profile in Fig. 6-3 (b) depicts the GaNOI-on-Si substrate after completing the double SiO_2-to-SiO_2 layer transfer process. The absence of micro voids at the bonding interface of the two PECVD SiO_2 layers indicates a uniform and superior microscale bonding quality. The morphological image of the top surface in Fig. 6-3 (c) reveals minimal roughness, suggesting that the bonding process did not impact the epi surface.

After the backside process was completed, the frontside fabrication process of the GaNOI HEMTs is shown in Fig. 6-4, which initiates with mesa isolation, conducted through ICP-RIE utilizing a Cl_2-based plasma. The ohmic contact regions for the source and drain were established using the conventional gold based ohmic metal stack Ti/Al/Ni/Au (20/120/40/50 nm). And the ohmic contacts were annealed by rapid thermal annealing (RTA) for 60 s at a temperature of 775 ºC in nitrogen ambient. The T-shaped gates were defined utilizing an electron beam lithography (EBL) system, employing bi-layer PMMA/MMA electron beam resist technology for patterning. Following the EBL process, Ni/Au (50 nm/300 nm) were deposited via electron beam evaporation, and the process concluded with a lift-off to finalize the gate structures. The formed T-gate exhibited a gate foot length (L_g) of 120 nm, a head length of 500 nm, and a stem height of 170 nm. In this study, gate width (W_g) of 2×20 µm, gate-source distance (L_{gs}) and gate-drain distance (L_{gd}) of both 1.5 µm was investigated.

6.4 Characterization and Mechanism Analysis

6.4.1 XRD and Raman Analysis

To understand the effects of bonding and substrate replacement on the GaN heterostructure, we conducted multi-faceted characterization analyses. The evolution of stress states was systematically investigated through XRD, micro-Raman spectroscopy, and FLX Thin Film Stress Measurement Systems.

The wafer bow measurements revealed a reduction in the average bow value from 7.57 μm to 3.88 μm concave/convex profile (Fig. 6-5), suggesting the relaxation of residual stress. XRD analysis was employed to evaluate the strain level in the GaN layer, with the results summarized in Table 6.1, revealing a 5% reduction in lattice strain along a-axis calculated using the unstrained lattice constant and the perpendicular lattice constant. This reduction could be attributed to the release of stress and the reduction of lattice mismatch [208].

The stress relaxation was further confirmed by micro-Raman spectroscopy measurements for both GaN on Si sample and GaNOI on Si sample. As shown in Fig. 6-6, a clear shift in the GaN E2 peak position and a reduction in its full width at half maximum (FWHM) were observe, which correlates well with the XRD results.

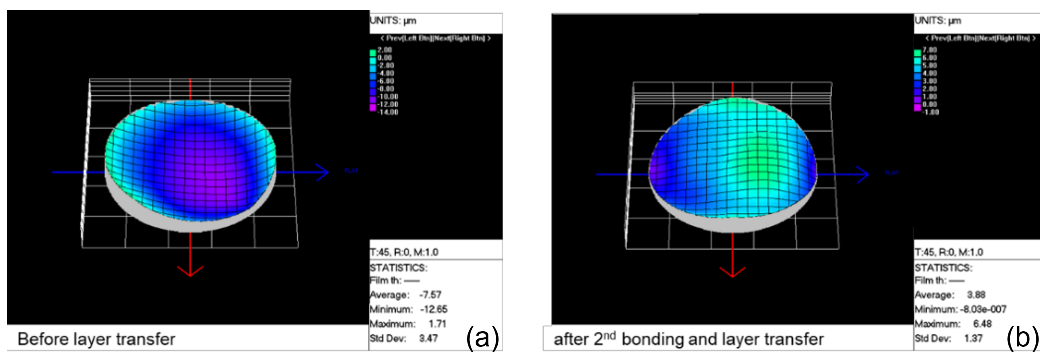


Fig. 6-5 Wafer bowing images measured by FLX Thin Film Stress Measurement Systems (a) GaN-on-Si wafer (bowing: 7.57 μm, concave), (b) GaNOI-on-Si wafer after SiO2 double bonding and layer transfer process (bowing: 3.88 μm, convex).

This peak shift occurs because changes in the lattice constant influence lattice vibrations, thereby affecting the phonon scattering energy. The stress within the GaN channel (σ_{xx}) was quantitatively derived from the Raman wavenumber shift using the formula

$$\sigma_{xx} = \Delta\omega \,/\, k \tag{6. 1}$$

where k is a pressure coefficient of 4.3 [209]. The calculations showed that the GaNOI structure exhibits a reduction in stress of 0.1 GPa compared to the original GaN-on-Si structure.

Table 6.1 Comparison of Key XRD Parameters.

Sample	Lattice parameter a_0=b0 (Å)	a Spread (Å)	Lattice parameter c_0 (Å)	c Spread (Å)	a Strain (%)
Before bonding	3.19099	4.25E-04	5.18402	4.81E-05	5.60E-02
After bonding	3.191079	1.29E-04	5.18399	3.17E-05	5.30E-02

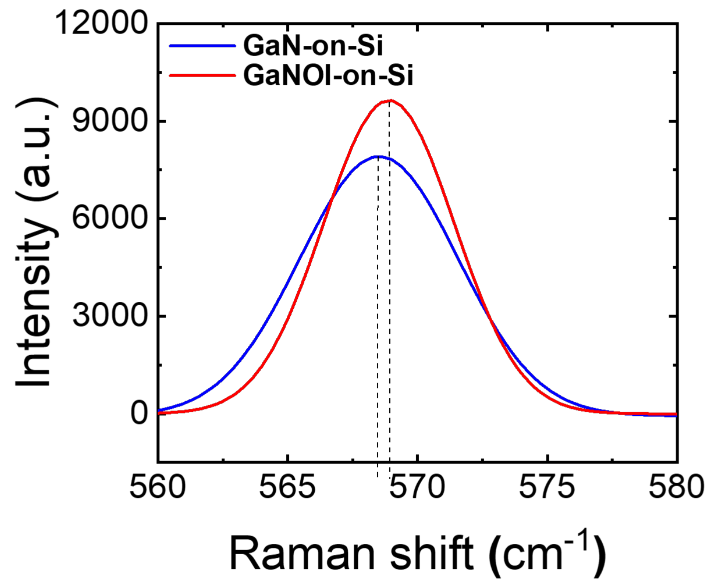


Fig. 6-6 Raman spectra of both GaN-on-Si and GaNOI-on-Si samples, high resolution E2 modes.

Table 6.2 Comparison of Hall measurement results.

Sample	Sheet Carrier Conc. [$\times 10^{13}$ cm^{-2}]	Mobility [cm^2 V^{-1} s^{-1}]	Sheet Resistance [Ω □$^{-1}$]
Before bonding	1.97	930	301
After bonding	1.89	1380	284

Additionally, the E2(high) mode in the GaNOI-on-Si wafer showed decreased FWHM values and increased peak intensity compared to the GaN-on-Si wafer. These improvements suggest that the layer transfer process effectively reduces stress while maintaining good crystalline quality [210]. The overall stress reduction, evidenced by reduced wafer bowing and decreased strain in the GaN layer, contributes to enhanced 2DEG mobility and electron density within the InAlN/GaN heterostructure [211]. Drawing insights from studies on similar material systems, these observed changes in structural and optical properties likely originate from the relaxation of residual stress during the bonding process and adjustments in lattice matching conditions [198], [210], [212]. These characterization results collectively reveal the impact of layer transfer processes on the crystal lattice and strain states, providing crucial insights into the formation mechanism of GaN-on-insulator structures. The observed stress reduction is expected to significantly influence the electrical properties of the 2DEG channel at the heterointerface. To quantitatively evaluate this impact, room temperature Hall effect measurements under Van der Pauw configuration were carried out on both GaN-on-Si and GaNOI-on-Si wafers to determine the 2DEG properties, as summarized in Table II. After substrate replacement, the mobility of the $In_{0.17}Al_{0.83}N$/GaN heterostructure improved from 930 cm^2 V^{-1} s^{-1} to 1380 cm^{2}V^{-1} s^{-1}, and the 2DEG density slightly decreased from 1.97×10^{13} to 1.89×10^{13} cm^{-2}, leading to an improvement of the R_{sh} from 301 to 284 Ω □$^{-1}$, which yields to the enhancement of the device performance for the GaNOI-on-Si devices

6.4.2 DC Characterization

DC characterization of the GaNOI HEMTs were carried out using a Keysight B1500A Semiconductor Parameter Analyzer. Fig. 6-7 (a) illustrates the observation of low ohmic contact resistance (R_c) of 0.21 Ω·mm and a sheet resistance (R_{sh}) of 307 Ω $\square^{-1}$ were achieved, as determined by linear transmission line model (TLM) analysis. Fig. 6-7 (b) shows the transfer characteristics which exhibited the maximum transconductance (g_m) of 318 mS/mm and the threshold voltage (V_{th}) of −3.9 V. Fig. 6-7 (c) shows the output characteristics of the GaNOI device. The device demonstrates a maximum saturation current density (I_{dmax}) of 1.28 A mm^{-1} at V_{gs} = 2 V, and the on-resistance (R_{ON}) is 2.3 Ω·mm. Furthermore, Fig. 6-7 (d) depicted the

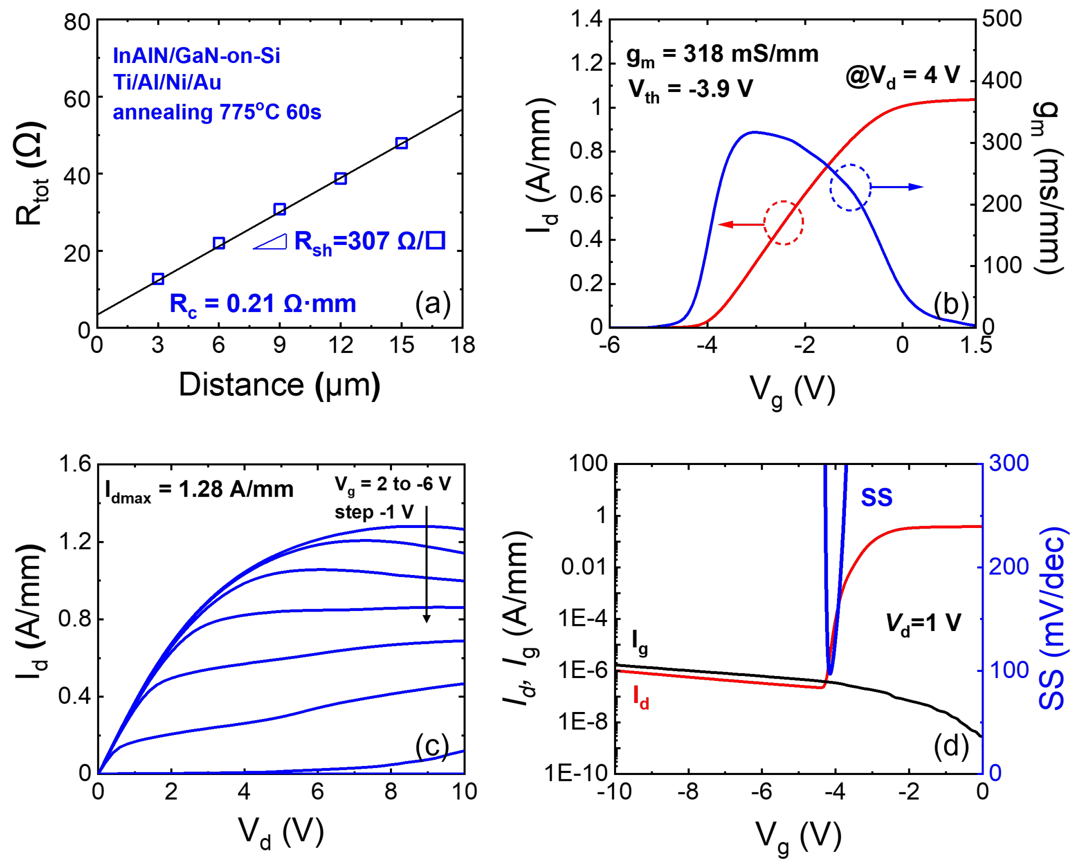


Fig. 6-7 (a) Extraction of R_c and R_{sh} through a linear fit of the TLM, plotting the relationship between total resistance and distance between pad contacts. (b) transfer and (c) output characteristics of a 120-nm gate GaNOI device. (d) Semi-log-scale transfer curves at V_{ds} = 1 V and gate leakage characteristics.

semi-log-scale transfer curves, at $V_{ds} = 1$ V. In the reverse bias direction, the I_{ON}/I_{OFF} ratio of GaNOI device is 2.6 x10^6 and the subthreshold slope (SS) is 89 mV dec^{-1}. And the off-state gate leakage current is about 117 μA mm^{-1} measured at −10 V, which suggests that there is no noticeable electron tunnelling through the barrier layer, despite the high localized electron density near the gate. From these parameters, it is clear that the fabricated GaNOI HEMTs have good gate control.

6.4.3 Small Signal RF Characterization

For small-signal RF characterization, the Keysight N5244-A PNA-X Network Analyzer was used to measure S-parameters. The vector network analyzer operates at room temperature with a frequency range of 1 MHz to 43 GHz. Prior to device measurements, the analyzer was calibrated using the Short-Open-Load-Through (SOLT) method to eliminate system errors. Due to significant RF losses between the probe pads and the Si substrate, the measured device S-parameters required de-embedding using Open and Short structure S-parameters.

Measurements on InAlN/GaNOI HEMTs with 120 nm gate length and 1.5 μm source-drain spacing showed enhanced high-frequency performance after substrate transfer.

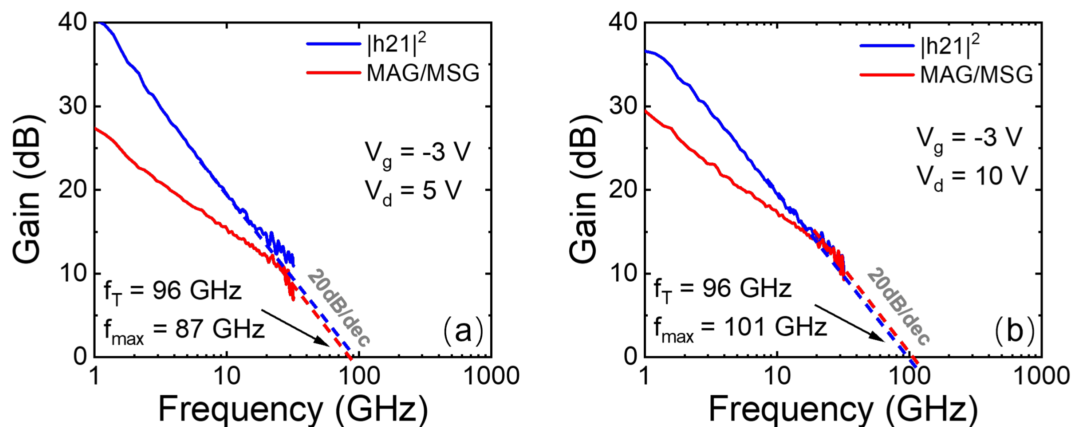


Fig. 6-8 The RF small-signal characteristics of the device after de-embedding pad parasitics with a bias of (a) $V_{ds} = 5$ V and $V_{gs} = -3$ V, (b) $V_{ds} = 10$ V and $V_{gs} = -3$ V.

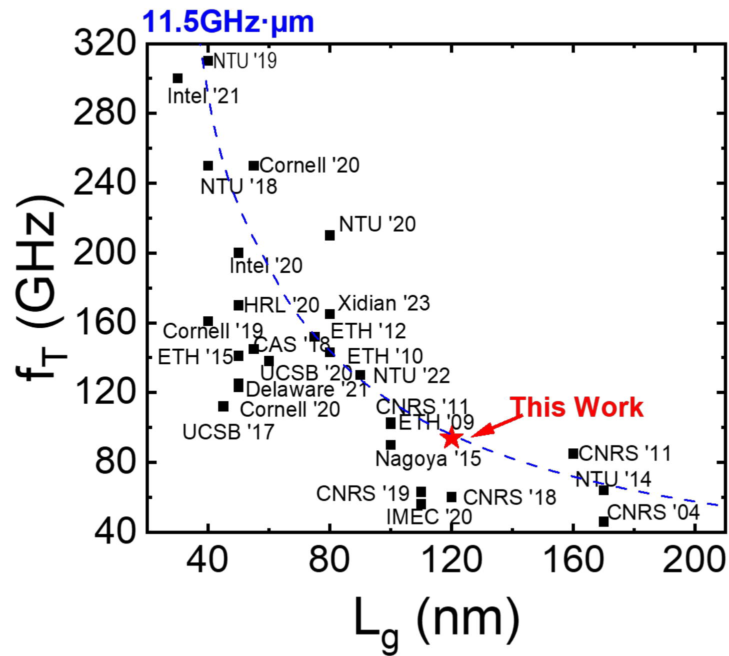


Fig. 6-9 Comparison of the f_T of our GaNOI HEMTs on Si against the reported f_T data for GaN HEMTs on Si from other research groups.

The relatively lower Fmax value is primarily attributed to excessive T-gate resistance, which can be addressed through T-gate methodology optimization.

Fig. 6-8 (a) and (b) show the small-signal frequency characteristics of the InAlN/GaNOI HEMTs with a 120 nm gate length and 1.5 μm source-drain spacing after de-embedding. Current gain ($|h21|^2$) and maximum available gain/maximum stable gain (MAG/MSG) were characterized at $V_{gs} = -3$ V under $V_{ds} = 5$V and 10V, extrapolation at −20 dB/dec roll-off revealed cutoff frequency (f_T) improvement from 77 GHz to 96 GHz and maximum oscillation frequency (f_{max}) increase from 75 GHz to 101 GHz at $V_{ds} = 5$V and 10V, respectively. Although both f_T and f_{max} improve after bonding, the f_{max} enhancement is lower than expected from the improved channel transport, which is primarily attributed to an elevated gate resistance arising from a non-ideal T-gate profile (limited gate head width and insufficient stem height). This limitation can be mitigated through further T-gate geometry optimization.

The achieved $f_T \times L_g$ product of 11.5 GHz·μm demonstrates excellent RF performance compared to other GaN-based HEMTs on Si substrates. [33], [65], [78],

[85], [92], [137], [213], [214], [215], [216], [217], [218], [219], [220], [221], [222], [223], [224], [225], [226], [227], [228], [229], [230], [231], [232], [233], [234], as illustrated in Fig. 6-9. This enhancement correlates with the observed increase in transconductance from 289 mS/mm to 320 mS/mm following substrate transfer.

6.5 Conclusion

In summary, high-frequency $In_{0.17}Al_{0.83}N$ /GaN HEMT on GaNOI-on-Si substrate using wafer bonding and substrate replacement technology has been successfully achieved for the first time. This approach has led to the successful creation of bonded wafers with exceptional uniformity and reduced lattice stress, resulting in an enhancement in 2DEG mobility. Furthermore, our investigation has revealed that high drain current, transconductance, and cut-off frequency can be achieved with this GaNOI device. The figure of merit, $f_T \times L_g$, obtained from our work is comparable to the other reports on GaN-based HEMTs on Si, highlighting the promise of GaNOI-on-Si technology for future mm-Wave applications. These advancements make GaNOI technology a promising platform for addressing the demands of advanced wireless communication systems and opening up new possibilities in high-frequency electronics.

Chapter. 7 Conclusion and Recommendation for Future Work

7.1 Conclusions

This thesis has presented several significant advancements in GaN-based high electron mobility transistor (HEMT) technology for millimeter-wave power amplifier applications. The research systematically addressed key limitations of conventional GaN-on-Si devices while extending their operational capabilities into previously unattained frequency regimes.

In Chapter 1, a novel double heterostructure (DH) AlN/GaN/AlGaN-on-Si HEMT was engineered specifically for low-voltage applications. The device demonstrated exceptional DC and RF performance, achieving a maximum drain current density of 1.9 A/mm, a peak transconductance of 0.66 S/mm, and cutoff/maximum oscillation frequencies of 145 GHz and 195 GHz, respectively. Notably, the transistor delivered record-setting saturated output powers of 0.6 W/mm at 3.5 V and 1.3 W/mm at 5 V during 30 GHz load-pull measurements, with a peak power-added efficiency of approximately 43%. These results establish a new benchmark for low-voltage GaN-on-Si HEMTs in the 5G FR2 band.

Chapter 2 reported the first demonstration of GaN-on-Si HEMT operation in the D-band—a critical frequency range for emerging 6G communication systems. The AlN/GaN/AlGaN-on-Si MIS-HEMT, featuring a 140 nm gate length, achieved fT/fmax values of 112 GHz and 205 GHz, respectively, and demonstrated power amplification at 123 GHz with a saturated output power of 0.67 W/mm. This breakthrough effectively extends the operational frequency of GaN-on-Si technology into the sub-THz regime, significantly broadening its application space.

In Chapter 3, multi-channel AlN/GaN heterostructures were investigated for Schottky barrier diode applications. By employing a five-channel design, the study achieved an exceptionally low sheet resistance of 69 Ω/□, attributed to a high sheet carrier density. The resulting devices exhibited outstanding electrical performance, including

a low turn-on voltage of 0.5 V and a high current density of 1050 mA/mm. Temperature-dependent measurements revealed a dual-mechanism transport process, involving both thermionic emission and tunneling, providing valuable insights for future device optimization.

Chapter 4 explored $In_{0.17}Al_{0.83}N$/GaN HEMTs on GaN-on-Insulator (GaNOI) substrates fabricated via 200 mm wafer bonding. This approach reduced lattice strain by approximately 5%, which in turn improved the sheet resistance from 301 Ω/□ to 284 Ω/□. The resulting devices achieved a peak f_T of 96 GHz with a 120 nm gate length, yielding an $f_T \times L_g$ product of 11.5 GHz·μm—comparable to or better than current GaN-on-Si technologies.

In conclusion, these contributions advance the state-of-the-art in GaN HEMT technology for millimeter-wave applications, addressing the growing demands of both 5G and emerging 6G wireless communication systems. This work not only establishes new performance benchmarks but also provides valuable design guidelines and theoretical insights that pave the way for future research and development in high-frequency power amplifier technologies.

7.2 Recommendations for Future Work

While this thesis has made substantial progress in extending the capabilities of GaN-based HEMTs, several promising research directions warrant further investigation:

1. Advanced Epitaxial Structures: Future work should explore more sophisticated multi-channel and composite channel designs to further enhance electron confinement and transport properties. Incorporation of quaternary barrier layers and graded heterojunctions may provide additional degrees of freedom for device optimization.
2. Thermal Management and Reliability: As GaN-based devices are pushed toward higher power densities, thermal dissipation and reliability become increasingly critical. Future work should incorporate device temperature projection and temperature-dependent characterization, while advanced thermal management strategies—including diamond heat spreaders, substrate thinning, and through-substrate vias—will be essential for reliable high-power GaN-on-Si operation.
3. Circuit and Heterogeneous Integration: Transitioning from discrete devices to monolithic microwave integrated circuits (MMICs), together with further exploration of GaN-on-Insulator technology, represents a natural progression toward system-level integration. Development of compatible passive components, interconnect technologies, and CMOS-compatible integration schemes will be crucial for enabling compact, scalable system-on-chip solutions.
4. Operation Beyond D-band: Extending GaN HEMT operation into the future 6G regime (>100 GHz) would open new application spaces in imaging, sensing, and ultra-high-speed communications.

The continued advancement of GaN HEMT technology for millimeter-wave applications holds strong promises for meeting the escalating demands of wireless communication systems. This thesis establishes a solid foundation for future innovations toward high-frequency, high-power electronic systems enabling next-generation wireless connectivity.

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