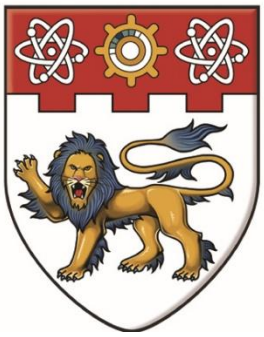

NANYANG TECHNOLOGICAL UNIVERSITY

INVESTIGATION AND IMPLEMENTATION OF MULTILEVEL POWER CONVERTERS FOR LOW/MEDIUM/HIGH POWER APPLICATIONS

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SCHOOL OF ELECTRICAL AND ELECTRONIC ENGINEERING

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For my father Ooi Kong Eow and mother Goh Sok Cheng

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List of Abbreviations

Acronyms

ADC	Analog-to-digital
AC	Alternating current
ACC	Average current control
ANPC	Active neutral-point-clamped
BCM	Boundary conduction mode
CCM	Continuous conduction mode
CMI	Cascaded multilevel inverter
CSI	Current source inverter
DC	Direct current
DCLP-FC	Hybrid diode-clamped and flying capacitor rectifier
DCM	Discontinuous conduction mode
EMI	Electromagnetic interference
EV	Electric vehicle
FACT	Flexible ac transmission
FHBCC	Fix hysteresis band current control
GMI	General multilevel inverter
GTO	Gate turn off thyristor
HCC	Hysteresis current control
HVAC	Heating, ventilation, and air conditioning
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
JFET	Junction gate-field transistor
LC	Low pass inductor-capacitor filter
LSPWM	Level shifted pulse width modulation
MDCI	Multilevel diode-clamped inverter
MEA	More electric aircraft
MFCI	Multilevel flying capacitor inverter
MMI	Modular multilevel inverter

MOSFET	Metal-oxide-semiconductor field-effect transistor
M^2C	Modular multilevel converter
NEA	National Environmental Agency
NPC	Neutral-point-clamped
ODE4	Fourth order ordinary differentiation equation
PCB	Printed circuit board
PFC	Power factor correction
PI	Proportional + Integrator
PLL	Phase lock loop
PMSM	Permanent magnet synchronous generator
PS-PWM	Phase shifted pulse width modulation
PUC	Pack U cells multilevel converter
PWM	Pulse width modulation
RMS	Root-mean-square
RPC-DCR	Reduced-part-count diode-clamped rectifier
SCR	Silicon-controlled rectifier
SGCT	Symmetric gate commutated thyristor
SiC	Silicon Carbide
SIMO	Single-input multiple-output
SRF	Synchronous-reference-frame
SVM	Space vector modulation
THD	Total harmonic distortion
UPF	Unity power factor
VHBCC	Variable hysteresis band current control
VSD	Variable speed drive
VSI	Voltage source inverter
3D	Three dimensional
5L-M^2DCI	Five-level/multiple-pole multilevel diode-clamped inverter
5L-M^2DCR	Five-level/multiple-pole multilevel diode-clamped rectifier
5L- M^2UPFR	Five-level/multiple-pole multilevel unity power factor rectifier

5L-M^2SCR	Five-level/multiple-pole multilevel switch-clamped rectifier
5L-M^2S^2CI	Five-level/multiple-pole multilevel single-switch-clamped inverter
5L-M^2T^2CI	Five-level/multiple-pole multilevel t-type-clamped inverter
5L-M^2VR	Five-level/multiple-pole multilevel VIENNA rectifier
7L- M^2DCI	Seven-level/multiple-pole multilevel diode-clamped inverter
7L- AM^2DCI	Seven-level/ active-clamped multiple-pole multilevel diode-clamped inverter

Variables

C_{eq}	Equivalent capacitance value in the DC-link
C_{fa}, C_{fb}, C_{fc}	RC filter capacitance value of phase (a, b, c)
h	Hysteresis band value
$I_a(t)$, $I_b(t)$, $I_c(t)$	Input or output current of the rectifier or inverter circuit for phase (a, b, c)
$I_{ca}(t)$, $I_{cb}(t)$, $I_{cc}(t)$	Inner capacitor current terminal (a, b, c) of 3L-MFCI
$I_{dc}(t)$	Output rectifier current
$I_m(t)$	Neutral-point current of the multilevel rectifier or inverter topologies
$I_o(t)$	Zero sequence current through the virtual ground voltage of the rectifier center point capacitor to the ground of the grid
$I_s(t)$	Output measurement of grid phase current and ‘s’ represent as terminal (a, b, c)
$I_x(t)$	DC positive rail current
$I_y(t)$	DC negative rail current

K_p	Proportional gain of the controller
K_f	Feed-forward gain
K_r	Resonant gain
L_a, L_b, L_c	Inductance value of phase (a, b, c)
L(s)	Open-loop transfer function of the controller
$M_a(t)$, $M_b(t)$, $M_c(t)$	Modulation control signal
m	Modulation amplitude
n	Number of voltage level
R_a, R_b, R_c	Resistance value of the inductive component for phase (a, b, c)
R_{fa}, R_{fb}, R_{fc}	RC filter resistance value of phase (a, b, c)
$S_a(t)$, $S_b(t)$, $S_c(t)$	Switching function of phase (a, b, c) of the VIENNA rectifier's switches
sign($I_a(t)$), sign($I_b(t)$), sign($I_a(t)$)	Function of the polarity of the current
$V_{am}(t)$, $V_{bm}(t)$, $V_{cm}(t)$	Input or output pole terminal (a, b, c) voltages referenced to node 'm'
$V_{an}(t)$, $V_{bn}(t)$, $V_{cn}(t)$	Input grid phase (a, b and c) voltages referenced to ground 'n'
$V_{ao}(t)$, $V_{bo}(t)$, $V_{co}(t)$	Output phase terminal (a, b, c) voltage referenced to node 'o' of the RC filter
$V_{Cfa}(t)$, $V_{Cfb}(t)$, $V_{Cfc}(t)$	RC filter phase terminal (a, b, c) voltage referenced to node 'o'
$V_{c1}(t)$, $V_{c2}(t)$, $V_{c3}(t)$, $V_{c4}(t)$	Capacitor voltage in DC bus
$V_{dc}(t)$	DC-link voltage
V_{peak}	Peak value of the grid phase voltage
$V_{mn}(t)$	Virtual ground voltage of the rectifier circuit
$V_{om}(t)$	Virtual ground voltage of the RC filter at the output terminal of inverter circuit
ΔE_{dc}	Rate of change of the energy stored
$\Delta I_{Lx}(t)$	Ripple current of the grid
ΔP_{dc}	Rate of change of the power store in the DC capacitor

φ_1	Displacement angle between the fundamental component of grid phase voltage and current
α	Firing angle
δ	Power factor

Abstract

The presented research work explores and proposes an efficient multilevel converter for single dc bus configuration without any isolated dc sources connected in the dc-link. The experimental prototype in a three-phase/three-level rectifier topology is focused on four functionalities of the unity power factor controller: (a) dc-link voltage balancing, (b) switching frequency range to achieve low THD current, (c) fault tolerance capability for two-phase operation, and (d) dynamic response of a feed-forward current control. The dc-link voltage balancing method for the three-phase/three-level and three-phase/five-level inverter topologies for neutral-point-clamped (NPC) inverter and flying capacitor (FC) inverter are also investigated. According to the experimental results, balanced capacitor voltage in the dc-link of a three-phase/three-level NPC inverter are achieved by using the dc offset modulation. However, three-phase/five-level/multilevel diode-clamped inverter (5L-MDCI) topologies require additional active balancing circuit in order to achieve stable and balanced capacitor voltages in the dc-link. The RC filter voltage balancing approach is well suited for flying capacitor inverter topology with more than three-levels based on PS-PWM technique.

The optimum reduction on the component count in five-level converters (rectifier and inverter) is proposed. Both five-level rectifier and inverter topologies are developed based on the multiple-pole concept. This approach reduces the number of power semiconductor devices with distributed voltage sources in a single dc bus configuration. By observing the switching operation of a level-shifted pulse width modulation (LS-PWM) in multiple-pole multilevel converters, zero current switching is achieved in the inner cell switch naturally.

The multiple-pole multilevel rectifier with reduced number of physical measurements sensors is achieved by implementing an observer control technique. Even when single phase fault is experienced, continuous operation is achieved for the five-level multiple-pole unity power factor rectifier topology using the proposed sensorless grid voltage and load current method. A high control bandwidth for two-phase operation is possible under severe unbalanced three-phase grid condition. The two-phase operation in a three-phase multiple-pole multilevel UPF rectifier is carried out with an in-phase current

control technique based on balanced power condition in a three-phase three-level rectifier. A 1 kHz LS-PWM is developed for five-level rectifier topologies in order to take advantage of its simplicity and well regulated switching profile.

In order to limit the switching loss to minimum a shorter conduction period control is proposed for a three-phase/five-level/six-switch multiple-pole multilevel UPF rectifier configuration. The hybrid-switching scheme based on LS-PWM/PS-PWM and shorter conduction period minimizes the switching losses incurred by inner cell switches THD of the input grid current under light load conditions.

Overall, the hardware prototypes of proposed converters have been totally realized and experimental results of Chapters 3 to 12 (except Chapter 11) are verify all analytical results and guarantee an optimum performance converter.

Chapter 1 - Introduction

This chapter briefly discusses the growth of power electronic drives with the supported statistical results. The statistical analysis investigates several factors such as electricity consumption in Singapore context, industrials' market overview, future trend of power electronic technology and international standard requirement for the need of power electronic converters.

1.1 Statistical Report on Energy Consumption in Singapore Region

The trends in development of power electronic topologies for both low voltage medium power and medium voltage high power drives have been introduced in many leading industries. Traditional mechanical equipment has been replaced by power electronic equipment due to its fast and precise acting control and ultra-high power density. Moreover, power electronic converters are the most dominant power conversion systems for several applications such as renewable and clean energy power systems (i.e. photovoltaic, fuel cell, wind generation, etc.), electric vehicle (EV), utility grid interface, high voltage direct current (HVDC), variable speed drive (VSD), HVAC (heating, ventilation and air conditioning), telecommunication center, etc. Further investigation of Singapore's electricity consumption it is known that, most of the energy is consumed by commerce and services-related sector followed by industrial sector [1] as shown in Fig 1.1. The high power demand as shown in Fig 1.1 is consumed by industrial use of machines and air-conditioning [2]. Hence, developing smart energy saving techniques for electrical machines and air-conditioning would result in greater financial savings and environmental benefits.

Looking at Singapore's context, a minimum requirement of energy performance standards in buildings have been addressed under National Environment Agency (NEA) to improve the overall efficiency of appliances in every building [3]. As shown in Fig 1.2 the major energy demand in Singapore arises from Air-cooling system, refrigerator and lighting.

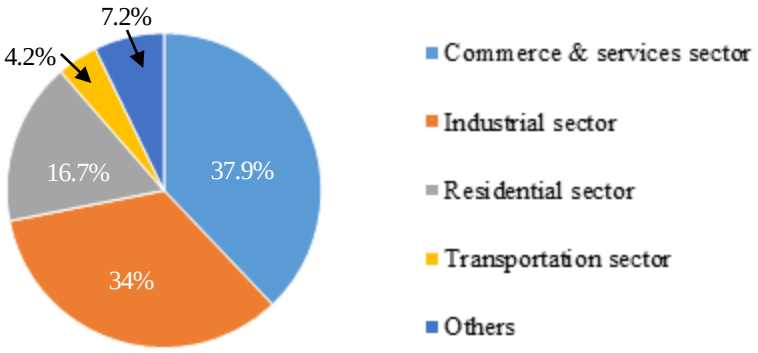


Fig. 1.1 Chart of energy consumption by sectors.

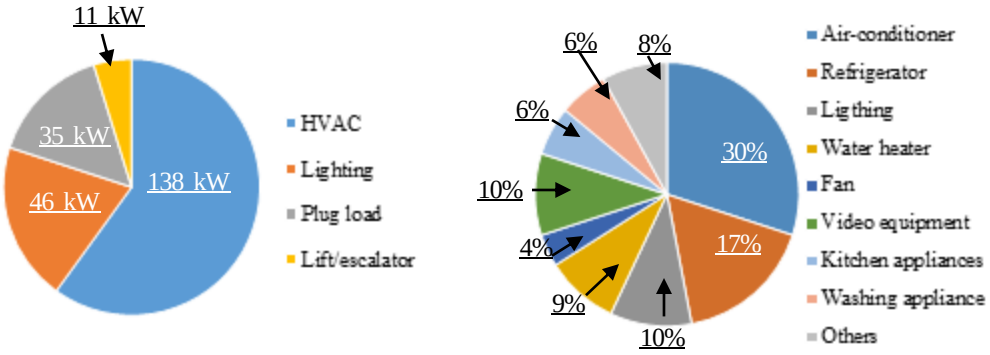


Fig. 1.2 Chart of energy consumption in buildings in Singapore. (Left Figure) Energy demand in buildings and (right Figure) Energy demand for typical household appliances.

Therefore, a comprehensive solution for high energy savings in power converter drives has to be developed and further research has to be carried out in order to improve the efficiency of the drives to meet the power demands of rapid growth in urbanization.

To achieve a highly efficient and high power density power system network, a proper interfacing (efficient ac/dc rectification and dc/ac inversion drives) between utility supply and load is required. However, such modern converter used for fluorescent lamp, variable speed drive, switch-mode power supply, air-conditioner and others may distort the grid distribution line due to non-sinusoidal current waveform created by the load. Hence, a fast acting controller to mitigate the effects generated by this non-linear load is required.

1.2 Harmonic Distortion Effect on Grid Side

Harmonic distortions in the grid are usually known as pulses operation. This type of phenomenon can influence the power quality of the grid, which result in high injected current distortion into the bus and unbalanced the three-phase supply voltage. In general, high harmonic current distortion can be found in AC line, interaction between the grid and the equipment loads. High distortion value in AC line can cause high voltage stress along the line and increase noise level of the transformer, as well as high energy loss is consumed in the network and efficiency of the converter are also affected.

Energy loss of the passive filter, AC transformer and cables are mainly caused by the current distortion [4, 5]. Every electrical network system is consisting of core resistance, where the loss and heat is dissipated from the core resistance. The basic principle of loss analysis can be analyzed as I^2R and I is the RMS current distortion where the square of product of harmonic current order is summing up together. As the percentage level of the harmonic distortion is increased, the power factor of the grid is significantly reduced. Therefore, most of the system components are usually oversized in practice to tolerate the maximum injected harmonic currents and reactive power circulates around the electric network.

1.3 International Standard for Harmonic Distortion Limit

The power electronic converters are commonly used to drive non-linear loads. This results in high harmonic distortion in voltage and current waveforms. The electronic equipment installed in the system causes harmonic distortion (as discussed in subsection 1.2). High harmonic content has many deteriorating effects such as, fluctuating power factor, mismatch in meter reading and other possible effects on the grid [6, 7]. In order to avert such power quality problems IEEE Standard 519-1992 has been introduced to provide a direction on dealing with harmonics introduced by static power electronic converters. International Electrotechnical Commision (IEC) [6-8]. Table 1.1 and 1.2 lists the least possible minimum voltage/current harmonic content injected by power electronic equipment into the grid or any other sensitive load.

TABLE 1.1

CURRENT DISTORTION LIMITS FOR GENERAL DISTRIBUTION SYSTEMS (120V THROUGH 69 000V)

Maximum Harmonic Current Distortion in Percent of I_L						
Individual Harmonic Order (Odd Harmonics)						
I_{sc}/I_L	< 11	11 < h < 17	17 < h < 23	23 < h < 35	35 < h	TDD (%)
< 20	4.0	2.0	1.5	0.6	0.3	5.0
20 < 50	7.0	3.5	2.5	1.0	0.5	8.0
50 > 100	10.0	4.5	4.0	1.5	0.7	12.0
100 < 1000	12.0	5.5	5.0	2.0	1.0	15.0
> 1000	15.0	7.0	6.0	2.5	1.4	20.0

I_{sc} = maximum short circuit current at PCC

I_L = maximum demand load current (fundamental frequency component) at PCC

TABLE 1.2

LOW-VOLTAGE SYSTEM CLASSIFICATION AND DISTORTION LIMITS

	Special Application[1]	General System	Dedicated System[2]
Notch Depth	10%	20%	50%
THD (voltage)	3%	5%	10%
Notch Area (A_N)[3]	16 400	22 800	36 500

Note: The value A_N for other than 480V system should be multiplied by V/480

[1] Special applications include hospital and airports

[2] A dedicated system is exclusively dedicated to the converter load

[3] In volt-microseconds at rated voltage and current

1.4 Power Electronic Market and Technology Overview

In mid-1970s, a multilevel neutral-point clamped inverter (NPC) topology has been patented by MIT researcher, Baker. The development of multilevel inverter topologies for low and high power drives have been widely used in many leading industries as

listed in Table 1.3 and 1.4. The multilevel inverter provides the dc-link voltage with staircase waveform shape and is approximated to be equivalent to a sinusoidal wave form. This approach has been implemented for various industrial applications. Many leading industries are facing a challenge to design and build an advanced multilevel converter for high power applications. A 200MW voltage source converter for HVDC with multiple voltage steps has been successfully introduced by ABB, Siemens and Alstom companies. This type of inverter topology is known as modular multilevel converter (M^2C) [9, 10]. Besides, the trend of power electronic converter in the global market is estimated around 15% to 20% growth until 2015. The steep estimated growth of power electronics market is attributed to astronomical investments on renewable and clean energy and this was reported by Yole Developpement, France [11].

As reported by U.S Department of Energy and GE Lineage Power industry in the year 2011, global energy consumption in telecom industry is estimated at around 160 billion kWh. 60% of the energy is used by the network equipment and remaining energy is consumed by HVAC system [12]. A highly efficient rectifier suitable for low voltage, medium power applications with power factor correction (PFC) unit can be implemented as front-end rectifier for higher level inverter to improve the overall plant efficiency and decrease the production cost.

Among the economic statistics reported by the government and industry, the key factors that propel research and development on advance power electronic converter are to increase the overall efficiency of the plant and to reduce the energy consumption in the near future. To achieve the above mentioned objectives it is a necessity to increase the number of operating levels of an advanced multi-level inverter. By increasing the number of operating voltage levels, the voltage stress on the inverter switches reduces by a great extent. Hence, semiconductor switches with lower voltage/current rating is used. This as well results in lower device dependent losses.

TABLE 1.3

Revolution of Industries' Multilevel Inverter Drives Platform for High Power and Medium Voltage Application

Manufacturer	Model	Power Rating (MVA)	Voltage Rating (kV)	Topology Type
ABB	ACS 5000	22	6 - 6.9/ (optional : 4.16)	5L-VSI-MF
Schneider Electric	Altivar 1000	10	2.3 - 3.3/ (optional: 4.16 - 6.6)	3L-NPC
Ansaldo Sistemi Industriali	Silconvert TN	1.3/5.2, 3.6/7.2	3.3	3L-NPC
	Silconvert GN	9 - 24	3.3	3L-NPC
Alstom Power Conversion	ALSPA VDM6000	0.3 – 3/ 2.2 - 8	2.3/ 3.3/ 4.2	4L-FCI
	ALSPA VDM7000	7 – 9.5	3.3	3L-NPC
LS Industrial Systems	LSMV Series	0.2/ 0.3/ 0.4/ 0.5/ 0.6/ 0.75/ 1.0/ 1.2/ 1.5/ 2/ 2.5/ 3/ 3.7	3/ 3.3/ 4.16/ 6/ 6.6/ 10	25L- HB-MC
Converterteam The Power Conversion Company	MV7000	3.75, 7.5, 10.5, 15, 21/ 15, 21, 30, 42	3.3/ 6.6	3L-NPC
Toshiba Mitsubishi-Electric Industrial Systems-Corporation	TMdrive-30 TMdrive-50 TMdrive-70 TMdrive-80	4	1.25	3L-NPC
	TMdrive-MVG	5.7/ 11.4/ 19.5	3.3/ 6.6 (7L-HB-MC)/ 10/ 11 (13L-HB-MC)	7L-HB-MC/ 13L-HB-MC
Yaskawa	Varispeed G7	0.11/ 0.3	0.20 – 0.24/ 0.38 – 0.48	3L-NPC
	FSDrive MV1S	0.132 – 2.5 (7L-HB-MC)/ 0.25 – 5 (13L-HB-MC)	3/ 3.3 (7L-HB-MC)/	7L-HB-MC/ 13L-HB-MC
	FSDrive MV1000	0.2 - 3.7 (9L- HB-NPC)/ 0.4 - 7.5 (13L-HB-NPC)	3 (9L- HB-NPC)/ 6 (13L-HB-NPC)	9L- HB-NPC/ 13L-HB-NPC
Fuji Electric	FRENIC4600FM5e	0.35 – 4.75 (9L-HB-NPC)/ 0.42 – 9.5 (17L-HB-NPC)/ 0.5 – 5.3 (21L-HB-NPC)	3 (9L-HB-NPC)/ 6 (17L-HB-NPC)/ 10 (21L-HB-NPC)	9L-HB-NPC/ 17L-HB-NPC/ 21L-HB-NPC

Note: VSI-MF is voltage source inverter multilevel-fuse less topology, NPC is neutral-point-clamped inverter topology, FCI is flying capacitor inverter topology, HB-MC is H-bridge-modular cell inverter topology and HB-NPC is H-bridge multilevel neutral-point-clamped inverter topology.

TABLE 1.4

Number of Component Count for Industries' Multilevel Inverter Drives Platform

Manufacturer	Model	Component Count		
		Capacitor	Diode	Semiconductor Switch
ABB	ACS 5000	6	12	24
Schneider Electric	Altivar 1000	2	6	12
Ansaldo Sistemi Industriali	Silconvert TN	2	6	12
	Silconvert GN	2	6	12
ALSTOM Power Conversion	ALSPA VDM6000	6	0	18
	ALSPA VDM7000	2	6	12
LS Industrial Systems	LSMV Series	18	0	72
Converterteam The Power Conversion Company	MV7000	2	6	12
Toshiba Mitsubishi-Electric Industrial Systems-Corporation	TMdrive-30 TMdrive-50 TMdrive-70 TMdrive-80	2	6	12
	TMdrive-MVG	9 (7L-HB-MC)/ 18 (13L-HB-MC)	0	36 (7L-HB-MC)/ 72 (13L-HB-MC)
Yaskawa	Varispeed G7	0	6	12
	FSDrive MV1S	9(7L-HB-MC)/ 18 (13L-HB-MC)	0	36 (7L-HB-MC)/ 72 (13L-HB-MC)
	FSDrive MV1000	12 (9L- HB-NPC)/ 18 (13L-HB-NPC)	24 (9L- HB-NPC)/ 36 (13L-HB-NPC)	48 (9L- HB-NPC)/ 72 (13L-HB-NPC)
Fuji Electric	FRENIC4600FM5e	12/ 24/ 30	24/ 48/ 60	48 (9L-HB-NPC)/ 96 (17L-HB-NPC)/ 120 (21L-HB-NPC)

1.5 Current and Future Trend of Multilevel Converters

As discussed in subsection 1.4, the utilization of multilevel converters increases rapidly as the cost of semiconductor devices goes down. More industries are willing to invest and develop new multilevel converters topologies for low-high power application such as renewable energy, more electric aircraft (MEA), locomotive and other possible application as listed in Table 1.5. Power electronic researchers are also looking towards an alternative solution for reducing the number of components per converter alongside reducing/eliminating the size of transformer and filter. The purpose of reducing the amount of active and passive components is: (1) to increase in reliability, (2) to reduce the initial cost of investment, (3) to maintain low maintainability for spare parts required, (4) to achieve compact and efficient converters, as well as (5) to avoid the complexity of multi winding transformer.

Current research trend in multilevel converters aligns with investigation of new modulation techniques and alternative rectifier/inverter topologies. Both methods are implemented to improve the efficiency of the power system network by reducing the total harmonic distortion in the grid with active multilevel rectifiers. The impact of grid interfacing is affected by the harmonic content as mentioned in previous section 1.2. Besides, switching and conduction losses and global reliability of the multilevel converters can be improve by reducing the amount of components count, as well as wider control bandwidth in PWM technique has to be further explore the possible modification.

The milestones of success in multilevel converters for academia research are shown in Fig. 1.4. Numerous new topologies have been developed for various range of application. The trends in the development of multilevel converter as illustrated in Fig. 1.4, suggest that multilevel converters are highly applicable for low power utilities as well. The major advantages that multilevel converters offer are improved power quality, higher efficiency, lower THD and reduced utilization of filter while operating at very low frequency (500-700 Hz).

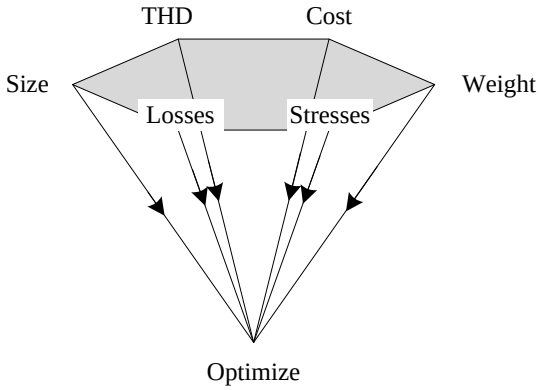


Fig. 1.3 Future trend of advance multilevel converters based on reference [13].

The desired characteristics so far mentioned form the guidelines for further development of compact electrical systems as indicated in Fig. 1.3. The size and weight reduction are a major concern for certain applications as in transportation industry and offshore wind turbines. The power electronic equipment for offshore wind turbines is installed on top of the tower integrated to the mechanical part of the turbine and generator. Hence, the converter plays an important role in weight and size reduction so as to relieve additional stress on tower and overall size of the turbine. In addition, the space occupied by electrical installation in sustainable energy building with the renewable energy sources in Singapore is a critical consideration for optimizing the space usage.

TABLE 1.5

COMMERCIALIZE PRODUCTS AND ACADEMIA RESEARCH ON MULTILEVEL CONVERTERS FOR VARIETY APPLICATION

Applications		Academia		Industrials		
		References	Topologies	Manufactures	Models	Topologies
Transportations	More Electric Aircraft	[14, 15]	3L-VIENNA Rectifier, 5L-Cascaded H-Bridge VSC			
	High Speed Train	[16-18]	3L-NPC, 3L/4L-MFCI, 27L-Asymmetrical Cascaded H-Bridge Inverter	Fuji Electric	TCI100-Model	BTB 3L-NPC
				Siemens	Sitras SFC Plus	Modular Multilevel Inverter
	Marine	[19, 20]	17L- Modular Multilevel Inverter, Unidirectional Multilevel Rectifier	ABB	ACS 6000	BTB 3L-NPC
Automotive	Electric Vehicle	[21, 22]	5L-Cascaded H-Bridge Inverter, 3L-NPC			
	Hybrid Electric Vehicle	[21-23]	5L-Cascaded H-Bridge Inverter, 3L-NPC, Multilevel Modular Capacitor-Clamped Converter			
Renewable Energy	Solar	[24-26]	3L-NPC, 4L/6L-MDCI	Power-One	Aurora Ultra	Centralize PV Multilevel Inverter
				TMEIC	Solar Ware 630	Grid Connected PV Multilevel Inverter
	Wind	[27, 28]	3L-NPC	ALSTOM	ALSPA VDM7000	BTB 3L-NPC
				ABB	PCS 6000	BTB 3L-NPC
	Hydro			ABB	PCS 8000	5L-ANPC
Energy Storage	Fuel Cell	[29]	Multilevel High Frequency Inverter	ABB	PCS 6000 ESS	3-NPC
	Batteries	[30, 31]	7L-Cascaded H-Bridge Inverter	ABB	PCS 6000 ESS	3-NPC
	Supercapacitor/Ultracapacitor	[22, 32]	3L-NPC, 81L-Asymmetrical Cascaded H-Bridge Inverter			

				Hitachi	HIVECTOL-HVI	Modular Multilevel Inverter
Industries/Commercial	Pump/Blower/Mining/Motor	[33, 34]	5L-MDCI	TMEIC-GE	DURA-BILT5 MV	5L-Cascaded NPC
				Fuji Electric	FRENIC4600FM5e	21L-Cascaded NPC
	Telecommunication Equipments	[35]	3L-VIENNA Rectifier	Toshiba	G9000 UPS	3L-NPC
	UPS	[36]	4L-MFCI			
Utilities Grid	HVDC	[37-39]	7L- Modular Multilevel Converter, 3L-MFCI, 5L-MDCI	Siemens	HVDC Plus	Modular Multilevel Converter
	SVC	[40]	5L- Cascaded H-Bridge Inverter	Siemens	SVC Plus	Modular Multilevel Converter
	STATCOMs	[41, 42]	4L- Cascaded H-Bridge Inverter, 5L-MDCI	ABB	PCS 6000 STATCOM	3L Double Phase IGCT Converter
	Active Filter	[32]	81L- Asymmetrical Cascaded H-Bridge Inverter			
Small Signls	Class-D Amplifier	[43]	9L- Cascaded H-Bridge Inverter			
	RF Amplifier	[44]	3L- Cascaded H-Bridge Inverter			

1.6 Objective and Contributions of this Thesis

The research work done so far constitutes the study and development of novel multilevel converter topologies (rectifier and inverter configurations), design of suitable dc-link voltage balancing techniques and various control strategies to improve efficiency and reliability of the drive systems. Three-phase five-level and seven-level converter topologies are selected for high power conversion with low switching frequency operation. Optimum size of multilevel converter topologies is achieved by reducing the number of semiconductors devices. Furthermore, an alternate switching strategy is developed to maintain a stable and regular switching pattern for higher-level voltage source converter.

A Feasibility study of the novel multilevel inverters and rectifiers are evaluated through the experimental set up and several control strategies are also introduced to achieve wider control bandwidth in the unity power factor control scheme. The study shows that with proposed control strategy, better reliability is achieved during two-phase operation (one phase down) for three-phase power supply system.

A significant reduction on the components count utilize in the external circuit board of amplifier circuit and measurement sensors are achieved by implementing new control measurement techniques. This type control technique reduces the possibility of device failure and production cost. In addition, switching schemes for minimizing switching losses higher-level voltage source rectifiers are also investigated.

The main objectives, proposed methods and contributions of this thesis are listed in Table 1.6. The proposed concepts as mentioned in the following Table are experimentally verified with a laboratory prototype.

TABLE 1.6

RESEARCH CONTRIBUTION LIST

Description of this Work	Objective	Contribution	Chapter	Page
Near unity power factor operation under unbalanced grid condition with three-phase/three-switches/three-level unidirectional rectifier.	• Achieving near unity power factor throughout the operation independent of load and source condition. • Reduction in size of input line inductance and hence increasing the power density of the drive while limiting current distortion to minimum. • To achieve a balanced dc-link and equalized voltage across all the floating capacitors in dc-link.	• Power balanced control technique is proposed and implemented to achieve unity power factor. • Hysteresis current control method with high switching frequency operation is adopted to achieve a possible size reduction of the input line inductance, to limit the error current and to provide a good dynamic current control through the feed-forward load current control. • Decoupled current control strategy is developed to obtain a balanced dc-link to obtain better current regulation within the hysteresis band limit.	3	27 ~ 50
Analysis of three-phase three-level diode clamped and flying capacitor inverter.	• To study the possibility and understand the limitation of operating with higher number of voltage levels. • To improve the stability of the dc-link by minimizing the offset dc voltage or differential voltage between any two series connected capacitors in the dc-link.	• Laboratory prototype is built a detailed mathematical and analytical study is done on both the topologies concerning harmonic content and power quality. • Two proposed dc-link voltage balancing techniques are designed (RC filter and modulation control techniques. [ref. Chapter 6] to improve the steady state voltage stability of the dc-link.	5 and 6	59 ~ 79 and 80 ~ 100

Description of this Work	Objective	Contribution	Chapter	Page
Analysis and comparison of three-phase five-level diode-clamped and flying capacitor inverter for transformerless applications which incorporate single dc-link.	• Investigate the performance of AC/DC/AC drive with both the inverter topologies and three-level unidirectional rectifier as the front-end rectifier. • Study and implement a suitable voltage balancing technique when the number of voltage levels is greater than three.	• Laboratory prototype of three-phase five-level diode-clamped and flying capacitor inverters are built and performance is evaluated considering various factors such as load range, percentage of total harmonic distortion (THD) and stability of dc-link. • Flying capacitor inverter voltage stability of the floating capacitors is improved by using phase-shifted pulse width modulation (PS-PWM) technique and by incorporating additional RC filter at the load terminal.	7	101 ~ 128
Investigate and study on five-level inverter topologies.	• To explore any possible modification for five-level inverter topologies based on diode-clamped approach. • To achieve low switching and conduction losses of the inverters.	• Reduce components count and achieve zero current switching without any additional passive and active components. • First derived topology is known as five-level/multiple-pole multilevel diode-clamped inverter, which has reduced 6 diodes for three-phase inverter. • Second propose five-level inverter topologies are derived from the first proposed inverter topology and both are known as multiple-pole multilevel t-type-clamped inverter and multiple-pole multilevel single-switch-clamped inverter for low voltage and low power application.	8	129 ~ 175

Description of this Work	Objective	Contribution	Chapter	Page
Balancing circuit for seven-level inverter topologies with single DC bus configuration.	• Distribute six distinct voltage levels for the series connected dc capacitors in the dc-link. • Improve voltage blocking capability for medium voltage and high power application.	• Single input and multiple outputs DC/DC balancing circuit is implemented and designed based on the buck/boost converter configuration. • Seven-level/multiple-pole multilevel diode-clamped inverter is connected to the DC/DC balancing circuit to ensure the balancing circuit is operating at stable and balance dc capacitor voltage in the dc-link. • Active switch clamped multiple-pole diode-clamped inverter is proposed to reduce the voltage stress of the IGBT and improve the circulating current by using the inductive components.	9	176 ~ 194
Five-level unity power factor rectifier topologies with reduced components, cost and loss optimization technique.	• Achieving near unity power factor with reduce number of physical measurement sensors through the virtual measurement technique. • Reduction in size of input line inductance and hence eliminating/ reducing the EMI filters of the drive while operating at 1 kHz switching frequency. • Investigating the possible switching strategy to minimize the switching loss to the minimum while maintaining the voltage level with low THD current.	• Reduce active components in five-level rectifier topologies are derived based on the multiple-pole approach. • Observer control technique is proposed with the in-phase current control method to extend the fault tolerance under two-phase operation with the minimum voltage and current sensors. • Short conduction period control for very low switching frequency operation is proposed. This type of switching scheme does not contain any high frequency chop over the fundamental period, which provides the minimum switching loss across the switching devices.	10, 11 and 12	195 ~ 213, 214 ~ 225 and 226 ~ 246

Chapter 2 – Review on Existing Rectifier Topologies

Rectifiers are usually connected to ac grid to transfer power to industrial loads. In many cases, ac loads are fed from high frequency inverter, which may inject high harmonic current into the grid. Hence, a front-end rectifier with nearly sinusoidal current will boost the energy savings and provides the grid with a minimum maintenance life cycle and cost.

In this chapter, a short survey on the existing topologies, starting from the basic diode bridge rectifier till present day pulse width modulation (PWM) rectifier [45-49] with a high power factor control is presented.

2.1 Fundamental Rectifier Topologies

The fundamental rectifier topologies are classified into three basic groups and a short introduction of those are given in the following sub-sections.

2.1.1 Unidirectional Diode Bridge Rectifier

A conventional three-phase diode bridge rectifier (shown in Fig. 2.1) is one of the basic structures to develop for low and medium power applications. However, topology shown in Fig. 2.1 does not meet the harmonic standards listed in IEC61000-3-4 and requires a bulky input filter to compensate the input harmonic current. Majority of the leading industries are manufacturing a series stack of multiple modules on unidirectional bridge rectifier circuit for high power application as shown in Fig. 2.2. The series stack of multiple modules of unidirectional bridge rectifier is known as multi-pulse diode rectifier and is usually connected to a three-phase isolated phase-shifted transformer for a high transformer utilization factor [45]. This type of topology serves the advantages of naturally fixed output dc voltage, cancelling input current harmonics, reduction in size of the dc capacitor/input filter or even without any dc capacitor/input filter, and neglecting any energy process for the active switching

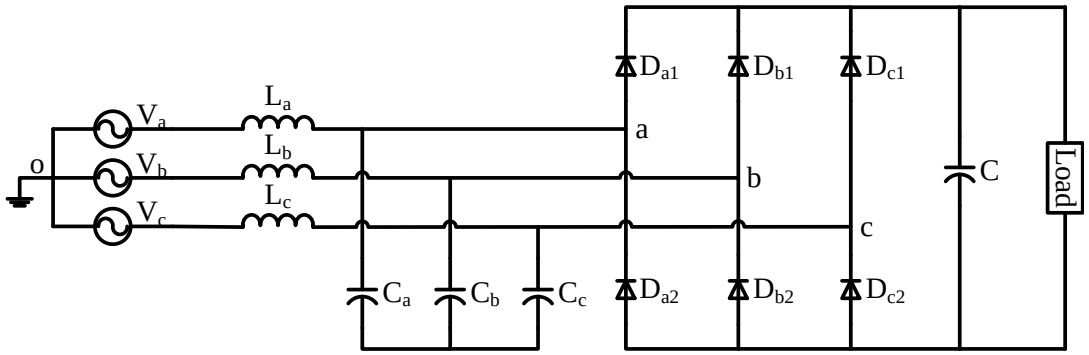


Fig. 2.1 Traditional uncontrolled three-phase bridge rectifier.

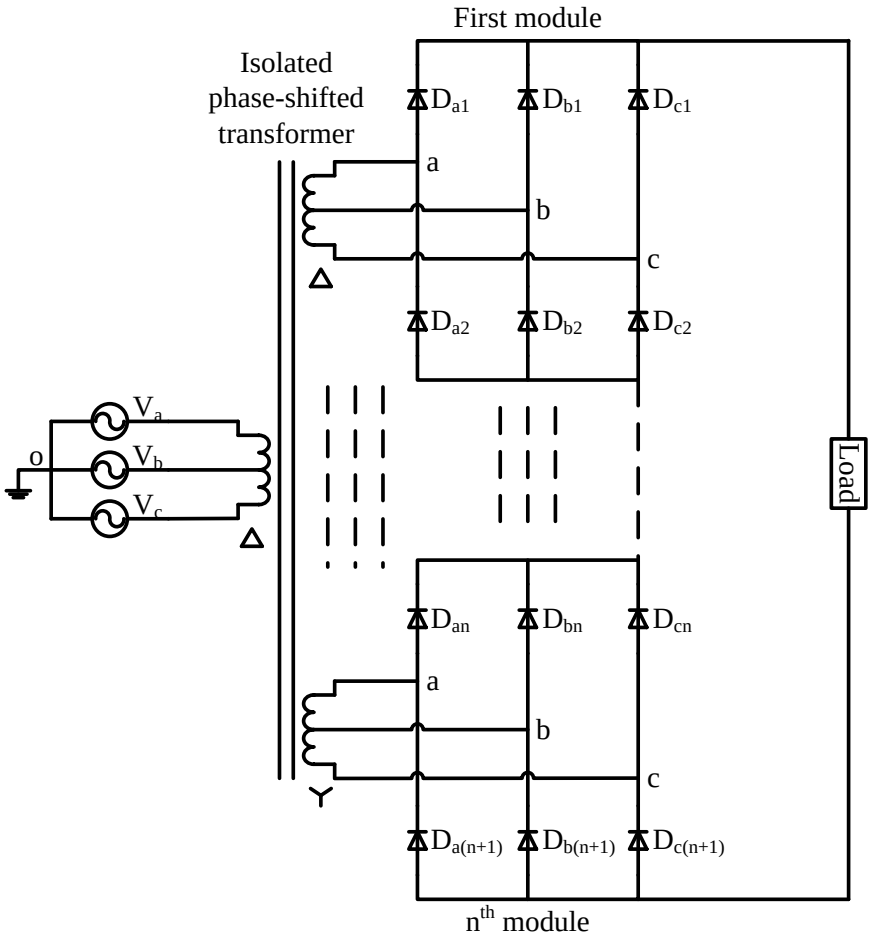


Fig. 2.2 Classical uncontrolled three-phase multi-pulse bridge rectifier.

device [45, 50, 51]. Although this topology serves as a benefit for high power applications, but in terms of the physical size it is relatively large, costly and even involves a complicated transformer design.

2.1.2 Thyristor Controlled Rectifier

In Fig 2.3 the first development of traditional controlled rectifier is shown. It is further constructed into a modular configuration similar to a multi-pulse diode bridge rectifier. This approach of multi-pulse configuration of thyristor controlled rectifier is able to achieve higher power capacity and reduction in harmonic content through a phase-shifted transformer. A few years back, multi-pulse thyristor controlled rectifier was one of the most favorable topology in industry and this configuration is usually installed in VSDs, FACT devices and HVDC system. When compared with three phase diode bridge rectifier multi-pulse thyristor controlled rectifier has advantages such as: controlled output dc voltage, high forward current and fast reverse recovery current as compared to three-phase diode bridge rectifier [45, 52, 53]. The design structure of this topology is simple and controller is easily implemented. But the design of the gate pulse triggering unit for thyristor devices is complex.

Both the Topologies (shown in Figs. 2.1 and 2.2) do not meet the requirement of the harmonic limit as dictated by IEEE Standard 519-1992 and IEC61000-3-4. Due to high harmonic content, several undesirable factors may occur in the system. High harmonic current injection into the system will distort the source voltage and results in low input power factor operation, low efficiency and requires a large input/output filter [54].

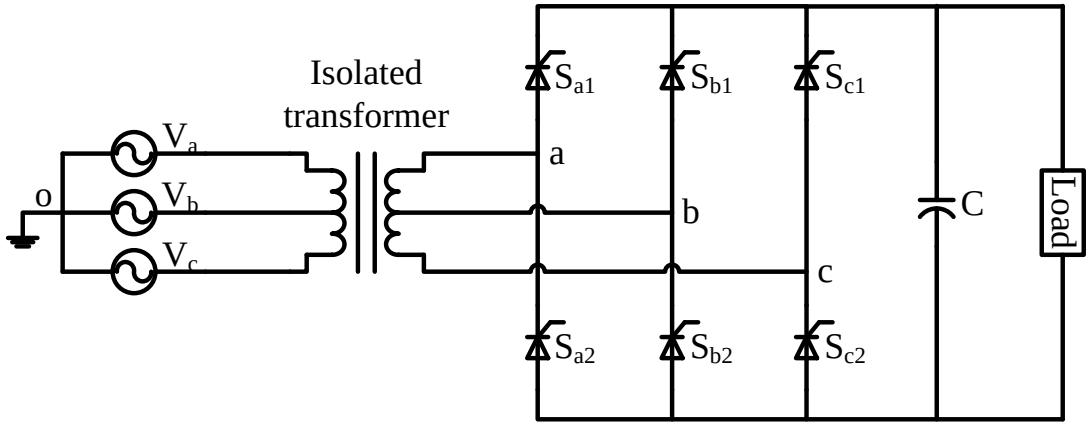
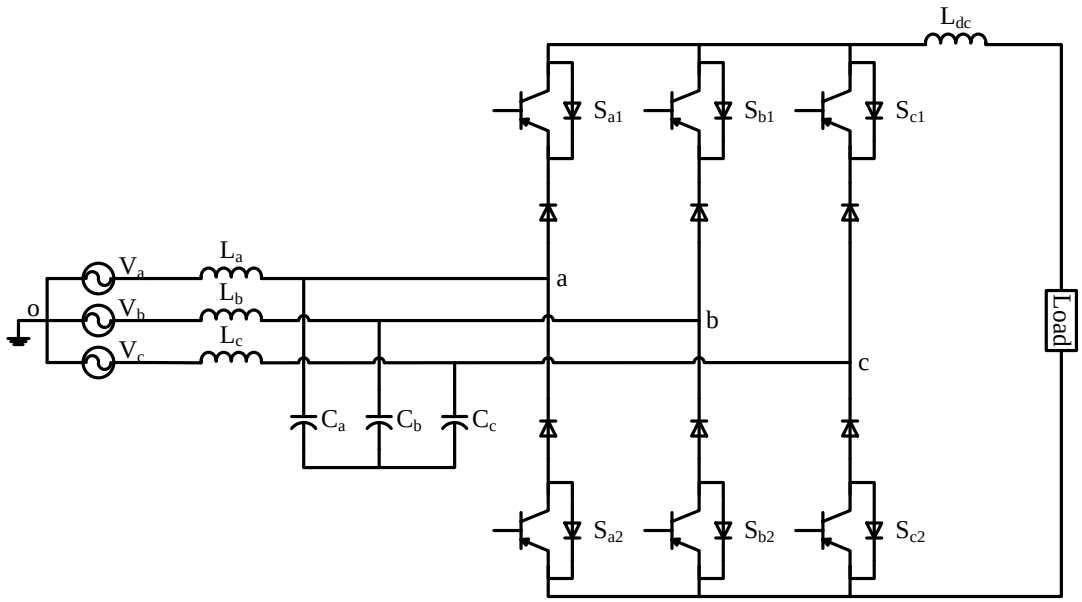


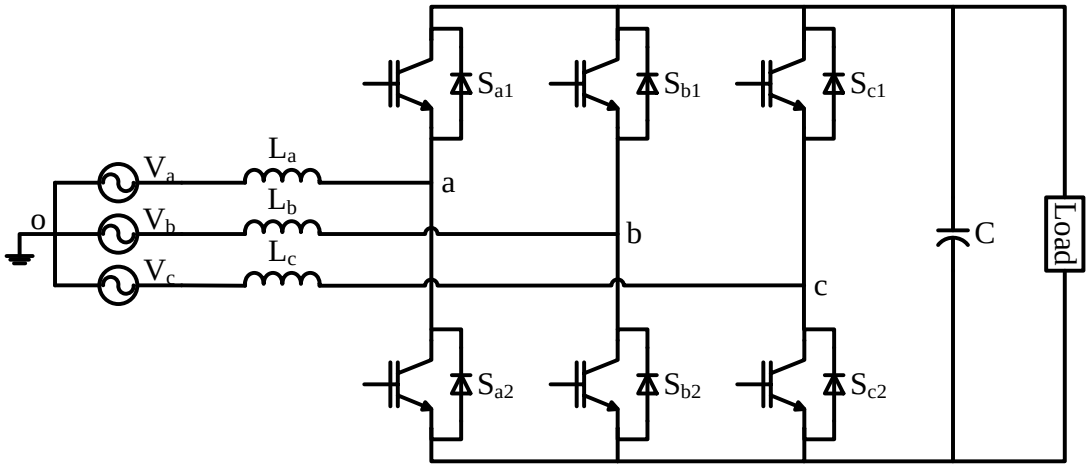
Fig. 2.3 Traditional thyristor controlled rectifier.

2.1.3 Pulse Width Modulation (PWM) Rectifier

The advancement of power semiconductor industry has enabled a rapid growth on the development of high power switching devices like insulated gate bipolar transistor (IGBT), metal oxide semiconductor field-effect transistor (MOSFET) and gate turn-off thyristor (GTO) with flexibility in self-commutation characteristics. A PWM strategy is applied to these switching devices for the linear control operating mode. Hence, most



(a)



(b)

Fig. 2.4 PWM rectifier topologies (a) Current-source converter and (b) voltage-source converter.

of the classical thyristor controlled rectifiers have been replaced by this technology due to its capability to switch at high frequencies [49].

Beyond that, several types of PWM rectifier is easily developed with the solid-state switching devices. A minimum power quality standard at the input grid is achieved with unity power factor control in the utility grid interfacing. Fig 2.4 (a) and (b) illustrates the two different types of PWM controlled rectifier configuration, a current-source converter (bidirectional buck rectifier) and a voltage-source converter (bidirectional boost rectifier) respectively. Both topologies have different safety mode of operation. In current-source converter, an unintended open circuit operation at the output dc link terminal must be avoided. Besides, short-circuit operation of the output dc terminal should not applied for the voltage-source converter.

Current-source rectifiers with LC filters at the ac terminal are usually implemented for harmonic cancellation. This type of circuit configuration requires complex control algorithm to control input displacement factor or additional hardware to compensate ac capacitor current. Moreover, transient oscillations may occur in the supply current due to the resonant circuit. To nullify the oscillations in the supply current, large resistances are required for damping purpose. Hence, this type of current-source converter may lead to high power loss and a complex controller design is required [55, 56].

The voltage-source rectifier is one of the simplest solutions to overcome the resonant effect in the current-source rectifier. This type of voltage-source converter consists of an AC inductor in the input terminal to compensate for the harmonic content. However, this configuration requires bulky ac inductor and dc capacitor for unity power factor control. And to reduce the physical size of the dc capacitor a complex control algorithm is essential for this system [57].

2.2 Power Factor Correction Rectifier Topologies

Active and passive filters are commonly used for harmonic current reduction along with conventional rectifier. However, implementing these filters has limitations such as, bulky, uneconomical and efficiency of the complete system is reduced due to the passive

resistance of the filter. Thus, new rectifier topologies are recommended for filtering harmonic current to gain unity power factor performance eliminating the use of any active or passive filters in the system [54].

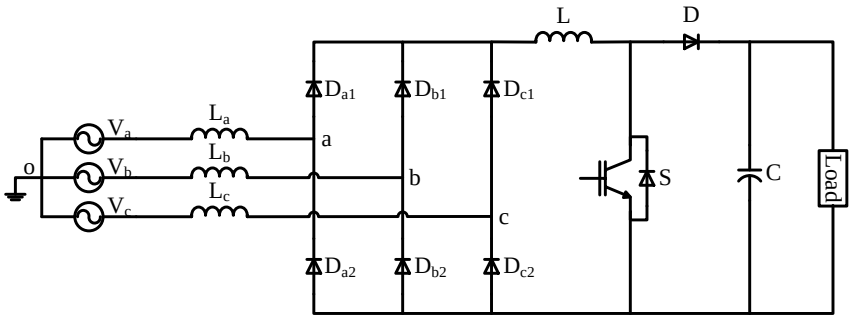
2.2.1 Unidirectional Boost Rectifier

Unidirectional power factor correction rectifiers have been widely used in industrial applications for low and medium power range; this serves the benefit of less active switching devices, low conduction losses and natural short circuit protection at dc bus terminal [50]. Several unidirectional boost rectifier topologies have been addressed in many publications on unity power factor control. Fig 2.5 is a single stage boost rectifier with single switching device, a boost inductor and capacitor for a harmonic current compensation at the utility interface. This type of topology is operated at very high switching frequency in order to obtain reduction in the size of the dc boost inductor. However, high operating switching frequency will lead to higher conduction loss of this converter [47] and complicates the common choke design for medium power application. Single switch boost rectifier in Fig 2.5 (a) is operated in different conduction modes, such as discontinues conduction mode (DCM), and continues conduction mode (CCM) and boundary conduction mode (BCM) control [49]. To provide a good current waveform shaping with DCM, a low cost and simple control method is used. But high ripple current will occur in a boost inductor and this approach will limit to medium power applications [49, 58]. Due to the occurrence of higher peak current in DCM, a higher rating of power semiconductor device has to be selected for the design. However, higher rating of power semiconductor devices are usually quite expensive and result in more device dependent losses than the low power rated devices [59].

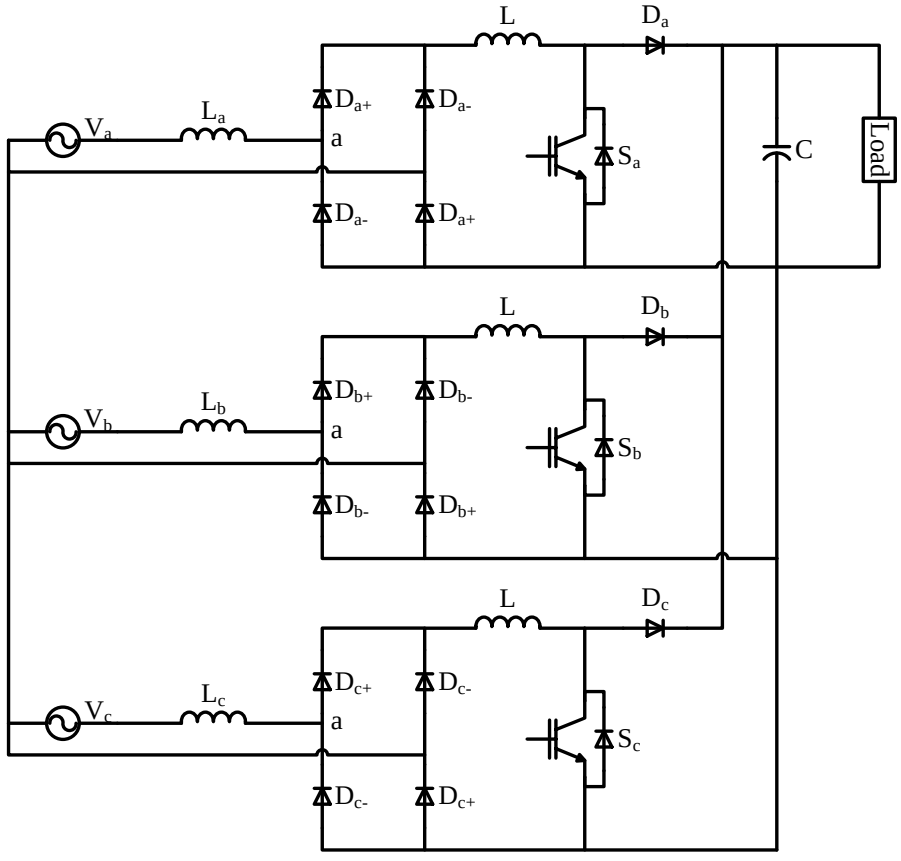
Thus, an alternative boost rectifier in Fig 2.5 (b) is easily constructed in DCM mode with switching devices of lower power rating to overwhelm the problem of a single switch boost rectifier as mention above. The circuit design is known as modular single-phase boost rectifier in three-phase system and it consists of three single phase single switch boost rectifier connected in parallel mode of operation. The modular single-phase boost rectifier in three-phase system is implemented for achieving high power density,

low di/dt and simple control strategy for an unbalanced grid condition [58]. Although such topology allows one to operate on higher power level, but complexity in synchronizing the gate signals increases and as well size of the converter increases. The switching frequency of the dc-dc converter depends on load [60].

2.2.2 Unidirectional Buck Rectifier



(a)



(b)

Fig. 2.5 Three-phase unidirectional boost rectifier topologies. (a) Single switch boost rectifier and (b) modular single-phase boost rectifier.

Three-phase two-stage buck type rectifiers are commonly used in high power telecommunication industry [50, 61-64]. A bidirectional rectifier which acts as a front-end rectifier has limited applications in telecommunication industry [50]. Hence a unidirectional rectifier which is more reliable, cost effective and requiring a simple control technique would be the possible solution. A basic configuration of a single switch buck rectifier as shown in Fig 2.6 (a) is suitable for low power applications. However, in high power applications this topology does not achieve the optimum efficiency as semiconductor switches of higher rating are used in single switch configuration. The operating modes of a single switch buck rectifier have similar limitations as that of single switch boost rectifier [61] mentioned in subsection 2.2.1.

In advance telecommunication power supply systems, multiple modules of DC/DC buck converters are usually connected in parallel with output dc link terminal. Several authors have proposed numerous rectifier topologies for telecommunication system with low input THD current achieving unity power factor with a grid interface [61-65]. Fig 2.6 (b) shows an isolated three-phase buck rectifier with two units of DC/DC buck converters based on Scott transformer. This type of topology requires two single-phase transformers to form a Scott connection and transform three-phase input grid voltages into two-phase output voltage to feed the bridge rectifiers. This type of Scott configuration reduces the harmonic content in input current and eliminates large ripple dc current due to DCM mode. Hence, power density of this topology is improved compared to converter configuration shown in Fig 2.6 (a).

Both topologies in Fig 2.6 (a) and (b) promise good power quality by achieving low THD in the input current and improved dc ripple current in DCM conduction mode. But these benefits come alongside increasing of the physical size of the converters and higher blocking voltage/current stress on the devices. So rating of the switching devices have to be safely selected and such architecture design will lead to relatively low efficiency of the power conversion [64]. The single stage buck rectifier topology in, Fig 2.6 (c) gives a reduced physical size converter circuit and lower rating of the power semiconductor devices, which makes it suitable for high power

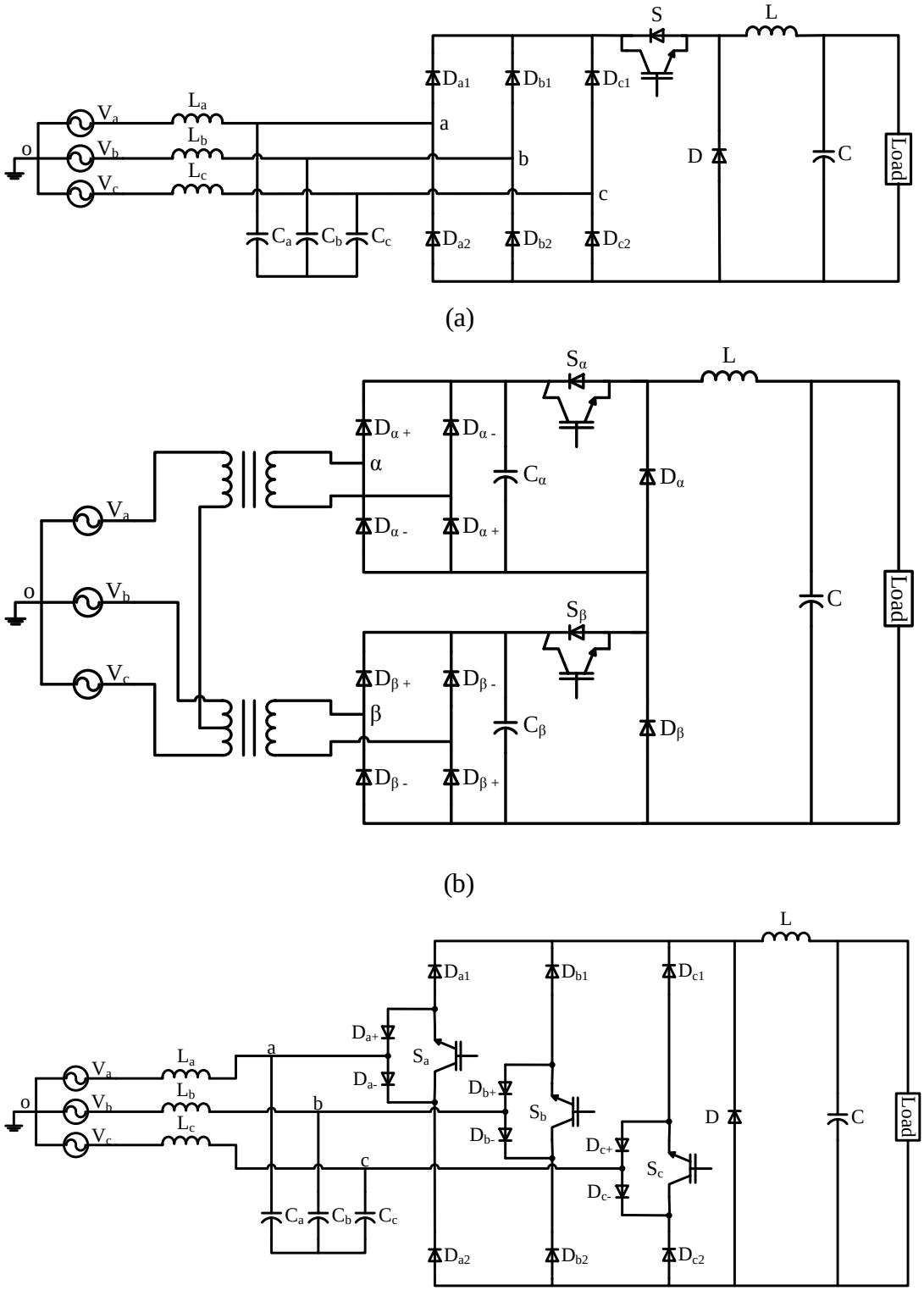


Fig. 2.6 Three-phase unidirectional buck rectifier topologies. (a) Single switch buck rectifier, (b) isolated buck rectifier based on Scott transformer configuration and (c) three-switch buck rectifier.

telecommunication industry. This converter is used to regulate the output voltage for wide input voltage range from 280 to 480Vrms [63].

2.2.3 Unidirectional Multilevel Rectifier

In variable speed drive applications and future electric aircraft system a high dc link voltage is necessary, [14, 66]. A booster rectifier to generate high dc link voltage is achieved by a two-stage topology approach and this is connected to form AC-to-DC then DC-to-DC energy conversion as discussed before. However, DCM conduction mode in two-stage topology will lead to high current stress on single switching devices of a DC/DC converter and large filter size is necessary for mitigating the electromagnetic interference (EMI). Hence, this approach is reduced into a single-stage rectifier (Vienna Rectifier, Fig. 2.7) to optimize the cost-to-performance ratio.

A detailed analysis of Vienna rectifier is presented in [67] and this topology has excellent features like lower blocking voltage stress, lower conduction loss and requires a filter of smaller size as compared to the classical single-stage boost rectifier in Fig 2.4 (b). In Vienna rectifier, the current can flow through the neutral point of the two series connected dc capacitors and through upper/lower diodes. The direction of the current flowing through the diodes is determined by the switching state of the semiconductor switches. Therefore, the peak current flowing through each phase is reduced and blocking voltage stress on the diodes is greatly minimized (half of the dc-link voltage). The reduction in the peak of the phase current leads to lower EMI effect. Since the dc link capacitor is clamped to the center point, the phase/ pole voltage has a shape of a

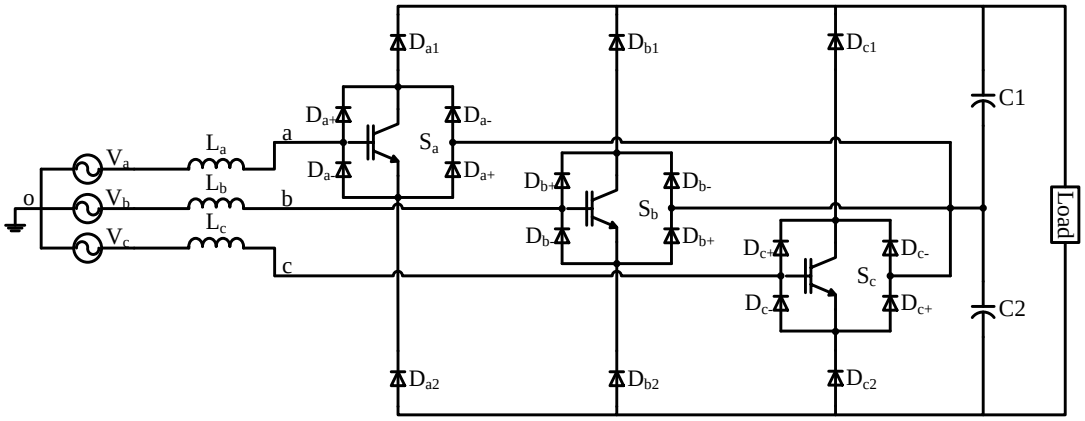


Fig. 2.7 Three-Phase unidirectional Vienna rectifier

three level stepped voltage waveform. This results in lower THD and requirement of filter is minimized.

2.3 Discussion

In this chapter, an overview of the unidirectional rectifier topologies for low-to-high voltage application is presented. Basic unidirectional bridge rectifier topology can be classified into topology with uncontrolled operation and single/multi-stage controlled rectifier. The most commonly used rectifier topology in many land based system is the unidirectional uncontrolled bridge rectifier. This type of topology is usually developed with isolated phased shifted transformer to shape the grid current waveform by increasing the number of secondary outputs. However, this topology with uncontrolled feature does not achieve unity power factor performance. In order to attain both features, a control switch (i.e. IGBTs, MOSFET, etc.) in the topology with the power factor control is required.

Among many topologies with the controlled switches presented in the literature review, a multilevel rectifier topology has been considered for investigation study. Multilevel rectifier topology is one of the most well-known topology that reduces the size of the filter inductance and eliminates the use of isolated transformer, hence achieving high efficiency and compact size.

Therefore, research work performing on the three-level rectifier (VIENNA) topology is firstly explored. The possible modification on the higher-level rectifier topology is also further investigated. Basic converter operation and feedback control scheme for achieving unity power factor and low current distortion is analyzed in the following Chapters 3, 10, 11 and 12.

Chapter 3 – High Power Factor Rectifier with Instantaneous Power Balanced Control Strategy under Unbalanced/Distorted Grid Condition

This chapter introduces a three-phase three-level unity power factor control rectifier as shown in Fig. 3.1 with the power balanced control strategy based on decoupling hysteresis current control. Such decoupling current control is the new reference current generated by the grid current control and zero sequence current control. The proposed controller is able to minimize the input current THD as well as achieving near unity power factor under unbalanced and distorted grid voltage condition with wide load variation. Such control scheme is designed to maintain a power balance between the ac and dc bus, stable input current with low THD and fast dc-link voltage tracking. To obtain the least possible THD, the voltage across the capacitors C_1 and C_2 must be balanced. In order to achieve equal dc voltages across both the capacitors for a wide load range, a decoupling hysteresis current control is implemented as illustrated in Fig. 3.2. The control algorithm is divided into two control loops, an inner loop with decoupling current control for a balanced capacitor voltages and dc-link voltage regulator as an outer loop. The detailed theoretical analysis of the controller design is presented in the following sub-sections and is verified by extensive simulation and experimental results.

3.1 Power Factor Correction Rectifier Topologies

The rectifier topology is shown in Fig. 3.1(a), this topology consists of two series connected capacitors and three bi-directional switches S_b, S_b and S_c. The bi-directional switch in each phase is constructed with four diodes and an IGBT to accommodate for a bi-directional current flow as in Fig. 3.1(b) [68, 69]. Referring to Fig. 3.1, the rectifier circuit is examined under balanced or unbalanced supply condition without considering the switching losses. The analysis of a three-phase instantaneous voltage supply is formulated as:

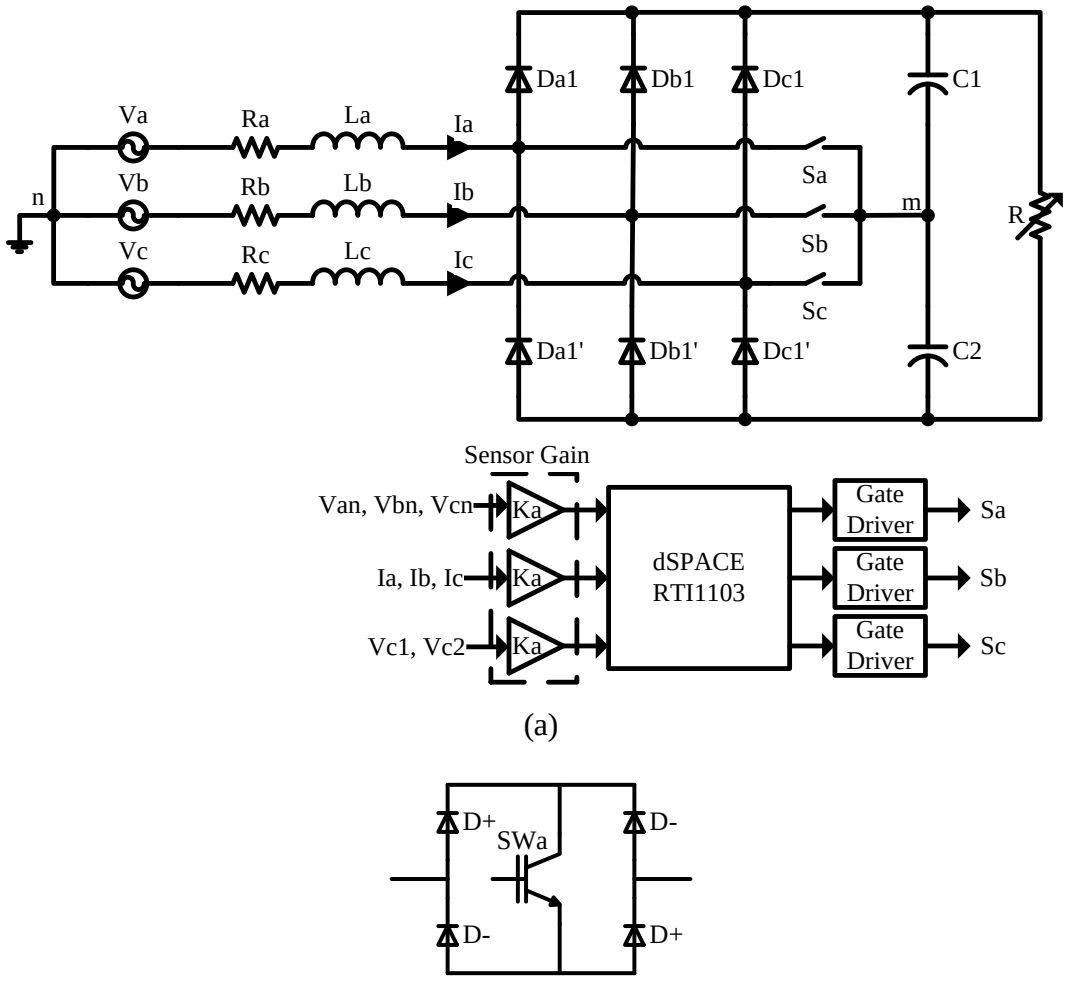


Fig. 3.1 A three-phase three-level unity-PF control rectifier with unidirectional power flow. (a) Rectifier configuration with bi-directional switches and (b) implementation of bi-directional switches Sa, Sb and Sc.

$$\begin{bmatrix} V_{an}(t) \\ V_{bn}(t) \\ V_{cn}(t) \end{bmatrix} = \begin{bmatrix} V_{am}(t) + V_{mn}(t) + L_a \dfrac{dI_a(t)}{dt} + I_a(t)R_a \\ V_{bm}(t) + V_{mn}(t) + L_b \dfrac{dI_b(t)}{dt} + I_b(t)R_b \\ V_{cm}(t) + V_{mn}(t) + L_c \dfrac{dI_c(t)}{dt} + I_c(t)R_c \end{bmatrix} \tag{3.1}$$

where $V_{am}(t)$, $V_{bm}(t)$ and $V_{cm}(t)$ are rectifier input voltage of node a, b and c referring to node m. $V_{mn}(t)$ is the voltage of the virtual ground measured across dc link midpoint

(node m) and the supply ground (node n). The rectifier phase voltage is expressed as a function of switching states as shown below:

$$\begin{bmatrix} V_{am}(t) \\ V_{bm}(t) \\ V_{cm}(t) \end{bmatrix} = \begin{bmatrix} (1-S_a(t))\dfrac{V_{dc}(t)}{2}\text{sign}(I_a(t)) \\ (1-S_b(t))\dfrac{V_{dc}(t)}{2}\text{sign}(I_b(t)) \\ (1-S_c(t))\dfrac{V_{dc}(t)}{2}\text{sign}(I_c(t)) \end{bmatrix} \tag{3.2}$$

$$V_{mn}(t) = \frac{-V_{dc}(t)}{6}\begin{Bmatrix} [1-S_a(t)]\text{sign}(I_a(t)) \\ +[1-S_b(t)]\text{sign}(I_b(t)) \\ +[1-S_c(t)]\text{sign}(I_c(t)) \end{Bmatrix} \tag{3.3}$$

$S_a(t)$, $S_b(t)$ and $S_c(t)$ denote the switching function of $SW_a(t)$, $SW_b(t)$ and $SW_c(t)$ of the bi-directional switch respectively. Whereas the function of sign(.) defines the direction of the filter inductor current flow, which is represented as:

$$\text{sign}(I_a(t)) = \begin{cases} 1 & \text{if } I_a(t) \geq 0 \\ -1 & \text{if } I_a(t) < 0 \end{cases} \tag{3.4}$$

The total per-phase input current is the sum of currents flowing through the diodes and bidirectional switch of that particular phase. This is expressed in equation (3.5).

$$\begin{cases} I_{SWa}(t) = S_a(t)I_a(t) \\ I_{SWb}(t) = S_b(t)I_b(t) \\ I_{SWc}(t) = S_c(t)I_c(t) \end{cases}$$

$$\begin{cases} I_{Da1}(t) = [1-S_a(t)]I_a(t)\text{fcn}(V_{am}(t)) \\ I_{Db1}(t) = [1-S_b(t)]I_b(t)\text{fcn}(V_{bm}(t)) \\ I_{Dc1}(t) = [1-S_c(t)]I_c(t)\text{fcn}(V_{cm}(t)) \end{cases}$$

$$\begin{cases} I_{Da1'}(t) = \left[1 - S_a(t)\right] I_a(t)\, fcn\left(-V_{am}(t)\right) \\ I_{Db1'}(t) = \left[1 - S_b(t)\right] I_b(t)\, fcn\left(-V_{bm}(t)\right) \\ I_{Dc1'}(t) = \left[1 - S_c(t)\right] I_c(t)\, fcn\left(-V_{cm}(t)\right) \end{cases} \quad (3.5)$$

where $I_{SWa}(t)$, $I_{SWb}(t)$ and $I_{SWc}(t)$ are the bi-directional switch currents flowing through the star-connected point. $I_{Da1}(t)$, $I_{Db1}(t)$ and $I_{Dc1}(t)$ are the current through the upper diodes and $I_{Da1'}(t)$, $I_{Db1'}(t)$, $I_{Dc1'}(t)$ are the currents flowing through their respective complementary diodes. Where the function of fcn(.) is written as:

$$fcn\left(V_{am}(t)\right) = \begin{cases} 1 & \text{if } V_{am}(t) > 0 \\ 0 & \text{if } V_{am}(t) \le 0 \end{cases} \quad (3.6)$$

The injected current at the midpoint of dc link is written as:

$$I_m(t) = S_a(t) I_a(t) + S_b(t) I_b(t) + S_c(t) I_c(t) \quad (3.7)$$

Based on the above analysis the voltage $V_{mn}(t)$ is assumed to be balanced. However, unbalanced and distorted grid supply can create an unbalanced neutral point, hence the expression of voltage $V_{mn}(t)$ is different from equation (3.3). Such unbalanced grid condition can complicate the control algorithm if direct voltage control is applied for this system and yields to unbalanced capacitor voltages. Therefore, a simple instantaneous power balanced control strategy is used, based on decoupled current control for dc voltage balancing.

3.2 Proposed Controller Scheme

Fig. 3.2 shows the power balanced algorithm with the unity power factor control. Proposed control algorithm -decoupled current control based on equation (3.7) is derived from an AC equivalent circuit of the star-connected bi-directional switches. In the case of balance grid condition and identical capacitor parameters, the injected current through the virtual ground is zero. However, in practical cases supply is

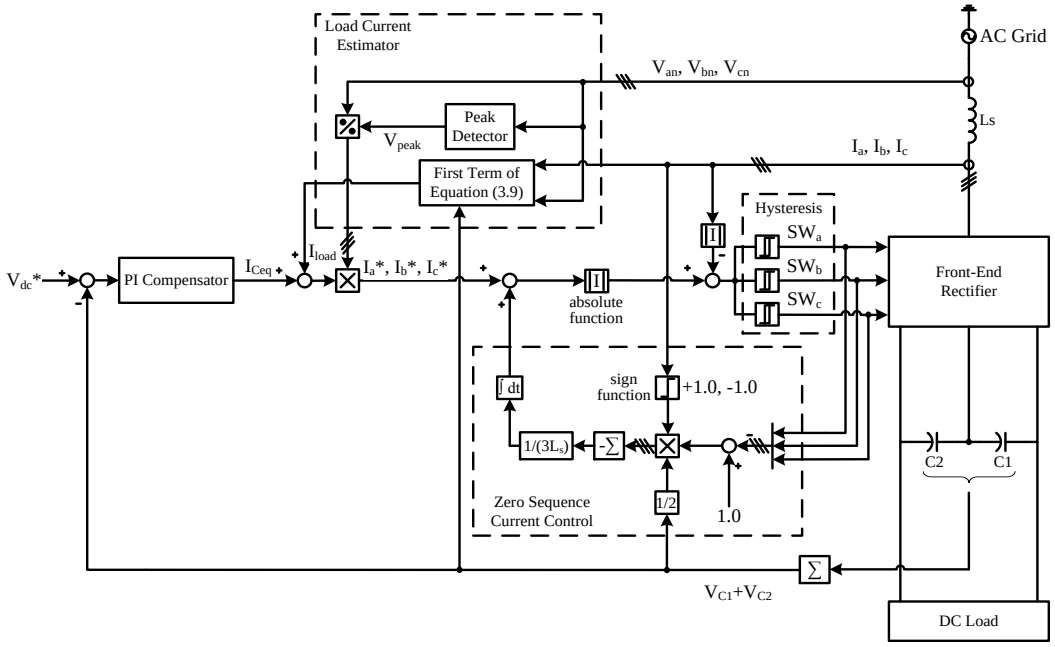


Fig. 3.2 A decouple current control with instantaneous power balanced control strategy based on fixed hysteresis band algorithm.

unbalanced and due to non-identical parameters of the passive elements. Hence, a zero sequence current component is injected into virtual ground of two series connected capacitors. This additional zero sequence current will cause the virtual ground to float at a certain dc offset value, which results in unbalanced dc-link. Moreover, the instantaneous peak current of the grid does not shape uniformly as no switching during the transition of the fundamental peak current [70].

To achieve a unity power factor under balanced or unbalanced grid condition, the net input reactive power of the rectifier must be zero with the power angle, $\theta = 0$. With this scheme, the net input active power is the sum of the output dc power and rate of change of the energy stored in the passive elements irrespective of the grid condition. The active power balance expression is obtained in the following equation (3.8).

$$V_{dc}(t)I_{dc}(t)=\begin{bmatrix}V_{an}(t) & V_{bn}(t) & V_{cn}(t)\end{bmatrix}\begin{bmatrix}I_a(t)\\ I_b(t)\\ I_c(t)\end{bmatrix}-L_s\begin{bmatrix}I_a(t)\dfrac{dI_a(t)}{dt}\\ I_b(t)\dfrac{dI_b(t)}{dt}\\ I_c(t)\dfrac{dI_c(t)}{dt}\end{bmatrix}-R_s\begin{bmatrix}I_a^2(t)\\ I_b^2(t)\\ I_c^2(t)\end{bmatrix}-C_{eq}V_{dc}(t)\frac{dV_{dc}(t)}{dt} \quad (3.8)$$

L_s and R_s denote three phase filter inductance and filter resistance [L_a L_b L_c] and [R_a R_b R_c] respectively. Whereas, C_{eq} is the equivalent dc capacitance value of the output rectifier.

Assume that the switching loss to be zero and the active power after filtering is fully transferred to the dc-link. Based on this assumption, the dc load current is directly estimated from the net active power of the ac side. The generated reference dc current is formulated by equating with equation (3.8) in summation with the rate of change voltage across the equivalent capacitors. According to the power balancing principle, the dc reference current of the inner control loop is obtained in equation (3.9).

$$I_{dc}^{*}(t) = I_{load}(t) + I_{Ceq}(t) = \underbrace{\frac{\sum\left(V_{sn}(t) - L_s\frac{dI_s(t)}{dt} - R_sI_s(t)\right)I_s(t)}{V_{dc}(t)}}_{\text{First term}} + \underbrace{C_{eq}\frac{dV_{dc}(t)}{dt}}_{\text{Second term}} \quad (3.9)$$

$I_s(t)$ is the input grid current. $I_a(t)$, $I_b(t)$ and $I_c(t)$ are the phase current. $V_{sn}(t)$ is the grid voltage of phase a, b and c when referred to node n. The desired instantaneous reference grid current in Fig 3.2 is formulated as shown in equation (3.10):

$$\begin{cases} I_a^{*}(t) = \left[I_{load}(t) + I_{Ceq}(t)\right]\sin_a \text{ reference} \\ I_b^{*}(t) = \left[I_{load}(t) + I_{Ceq}(t)\right]\sin_b \text{ reference} \\ I_c^{*}(t) = \left[I_{load}(t) + I_{Ceq}(t)\right]\sin_c \text{ reference} \end{cases} \quad (3.10)$$

where $I_{Ceq}(t)$ is the dc current flow in the energy stored in the passive elements of the rectifier as stated in the second term of equation (3.9). The dc current $I_{Ceq}(t)$ is obtained by a simple first order PI(s) controller as mentioned in sub-section 3.2.1.

During unsymmetrical grid condition, the phase angles between any two phases of a three-phase supply system are unequal. The measurement of unequal phase angles under such conditions is difficult using phase lock loop as the design of PLL gets complicated. Therefore, a sine template generator for the proposed converter is calculated from the reference peak voltage and phase voltage of the grid. While the

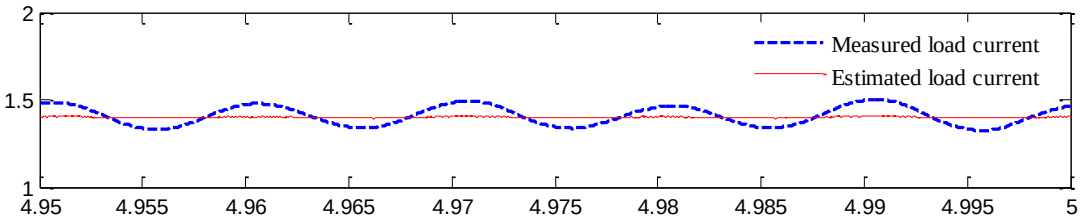


Fig. 3.3 DC load current referred to measured and estimated value under ±10% unbalanced grid condition.

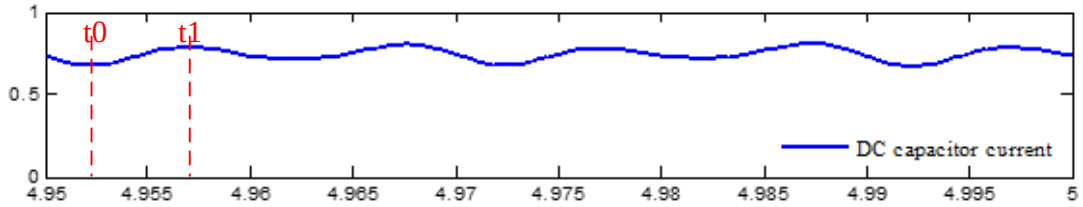


Fig. 3.4 Output control signal of the outer voltage controller under ±10% unbalanced grid condition.

phase voltage of the grid is measured using the hall-effect voltage transducers and the reference peak voltage is obtained by the peak detector based on the following equation.

$$V_{peak} = \left\{ \left[\frac{2}{3} V_{an}(t) - \frac{1}{3} V_{bn}(t) - \frac{1}{3} V_{cn}(t) \right]^2 + \left[\frac{1}{\sqrt{3}} V_{bn}(t) - \frac{1}{\sqrt{3}} V_{cn}(t) \right]^2 \right\}^{1/2}$$

(3.11)

where $V_{an}(t)$, $V_{bn}(t)$ and $V_{cn}(t)$ are the instantaneous phase voltage of the input grid supply.

Using equation (3.11), a simple reference sine template for unbalanced grid supply is obtained by the following equation (3.12).

$$\sin_s \text{ reference} = \frac{V_{sn}(t)}{V_{peak}} \qquad (3.12)$$

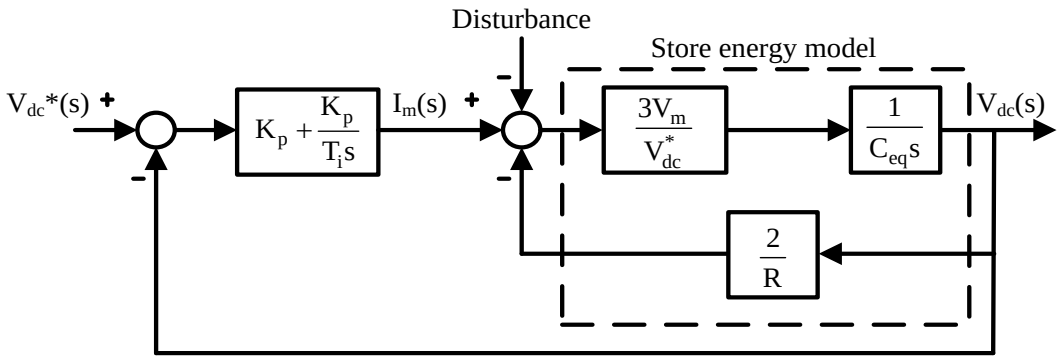


Fig. 3.5 Outer loop voltage controller of Fig. 3.2.

$\sin_s$reference is known as the reference sine wave template for the instantaneous reference current in equation (3.10). The small letter's' denotes phase a, b and c of the three-phase grid voltage measurement.

3.2.1 DC-Link Voltage Control

Fig. 3.5 shows the closed loop model of the outer loop voltage control. The PI regulator tracks the dc-link voltage with respect to the reference control value. The disturbance shown in Fig. 3.5 is the injected current during load change. To design the parameters of the PI regulator, the rate of change of stored energy in the dc-link is formulated as follows.

The dc current of the equivalent capacitors is given by

$$I_{Ceq}(s) = \left[V_{dc}(s) - V_{C1}(s) - V_{C2}(s)\right]\left[K_p + \frac{K_p}{T_i s}\right] \tag{3.13}$$

where K_p is the proportional gain constant of the voltage control loop and T_i is the settling time of the dc-link voltage. The dc capacitor is charged by the three-phase instantaneous grid power during the time interval (t_0 – t_1) as shown in Fig. 3.4. This results in dc-link voltage variation due to the rate of change of the energy stored, ΔE_{dc}. The proportional gain is obtained by the following equation:

$$\Delta E_{dc} = \frac{1}{2} C_{eq} \left[V_{dc}^2 (t_1) - V_{dc}^2 (t_0) \right] \tag{3.14}$$

Based on three-phase power balancing principle, the energy stored in the inductor is assumed to be equal to that of energy stored in the dc capacitors during the power transferred. Hence, the peak of the fundamental input current is equivalent to the peak of the capacitor current. With this assumption, the amplitude of the instantaneous dc current $I_{dc}(t)$ is obtained from the instantaneous grid power and expressed as follows:

$$V_{an}(t) I_a(t) + V_{bn}(t) I_b(t) + V_{cn}(t) I_c(t) = \frac{3}{2} V_m I_m \tag{3.15}$$

where V_m and I_m are the amplitude of the instantaneous ac voltage and current parameters respectively. Based on equation (3.14) and (3.15), the rate of change of power is defined by the relationship between the output dc power and load power. Thus, rate of change of power in the equivalent dc-link capacitor is simplified as:

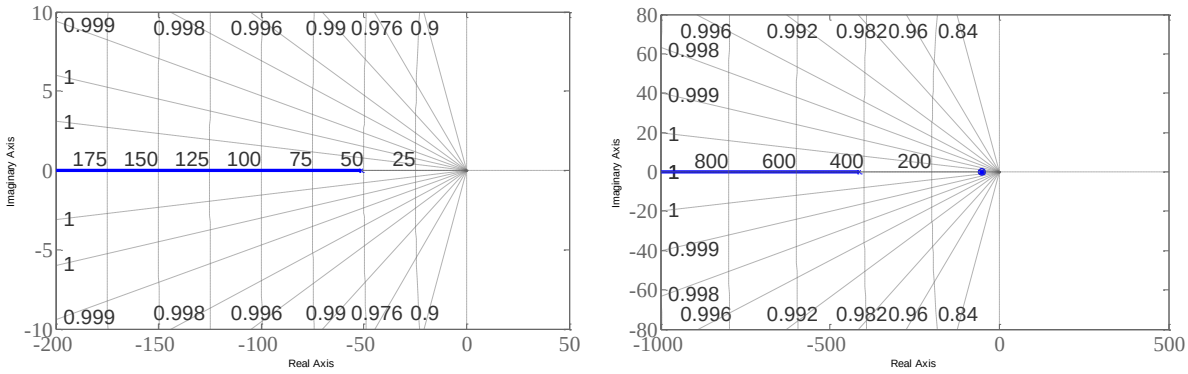
$$\Delta P_{dc} = \frac{C_{eq}}{2} \frac{dV_{dc}^2(t)}{dt} = \frac{3}{2} V_m I_m - \frac{V_{dc}^2(t)}{R} \tag{3.16}$$

where R is known as the load resistance of the rectifier. From equation (3.16), the capacitor current in equation (3.9) is calculated as

$$\begin{aligned} I_{Ceq}(t) &= I_{dc}(t) - I_{load}(t) \\ C_{eq} \frac{dV_{dc}(t)}{dt} &= \frac{3V_m I_m}{V_{dc}(t)} - \frac{2V_{dc}(t)}{R} \end{aligned} \tag{3.17}$$

From equation (3.17), the proportional gain of the outer loop voltage control is designed accordingly to the open-loop transfer function of the voltage control as shown in Fig. 3.5. Therefore, the open-loop transfer function L(s) is written as

$$L(s) = K_p \left(1 + \frac{1}{T_i s} \right) \times \frac{3V_m}{V_{dc} C_{eq}} \times \frac{1}{s + 6V_m / V_{dc} C_{eq} R} \tag{3.18}$$



(a) (b)

Fig. 3.6 Root locus of respective system in (a) open-loop system and (b) close-loop system with $K_p = 0.16$ (frequency unit: rad/s).

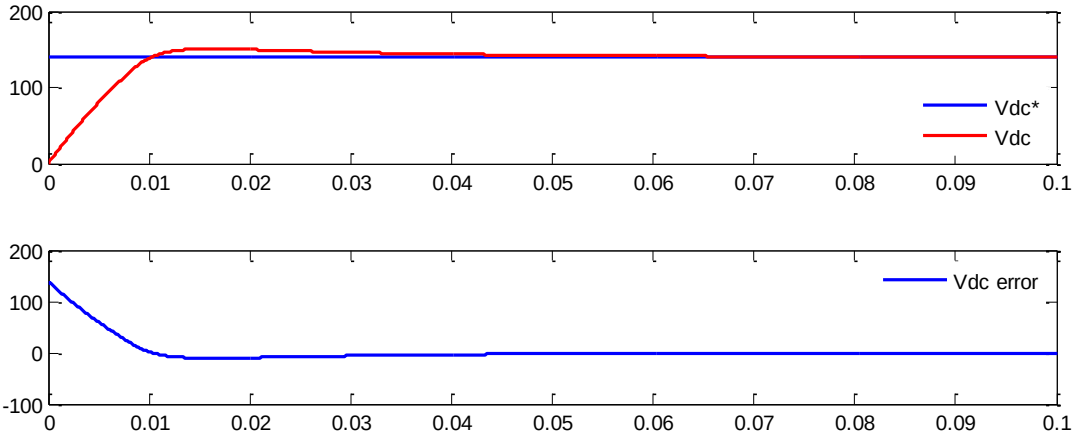


Fig. 3.7 Obtained results of voltage control in Fig. 3.2.

where the parameter of K_p is selected based on the pole cancellation for a stable system as given in the following.

$$K_p = \frac{V_{dc} C_{eq} R}{6 V_m} \tag{3.19}$$

The root locus of the energy store model is shown in Fig. 3.6(a). Based on the pole trajectory in Fig. 3.6, the gain K_p is selected as $0.16A^{-1}$ and T_i is 0.02s. With this control parameter, the pole of the close-loop system is placed at the left-half-plane and it gives a stable close-loop system.

With control parameter $K_p = 0.16A^{-1}$ and $T_i = 0.02$s, the voltage control shows a good tracking performance as shown in Fig. 3.7. From Fig. 3.7, one can see that the steady-state error of the dc voltage is zero at time t = 0.065s, this shows that the controller tracked the desired reference value.

3.2.2 Current Control

Average current control (ACC) and hysteresis current control (HCC) are often used for current error compensation [69-71]. Both the above current control techniques are used to reduce the harmonic content at the grid side. In ACC, the current error is shaped with a carrier waveform. Whereas current error of HCC is suppressed within the hysteresis band limit as shown in Fig. 3.8. However, HCC provide better dynamic behavior than the ACC method when there is a step change in the reference current [70].

This sub-section provides a study on the HCC method with the decoupling current control. The switching function of the bidirectional switches is given in the following equation.

$$SW_s(t) = \begin{cases} 1, & \text{if} \quad I_s^*(t) - I_s(t) < -h \\ 0, & \text{else} \quad I_s^*(t) - I_s(t) > +h \end{cases} \tag{3.20}$$

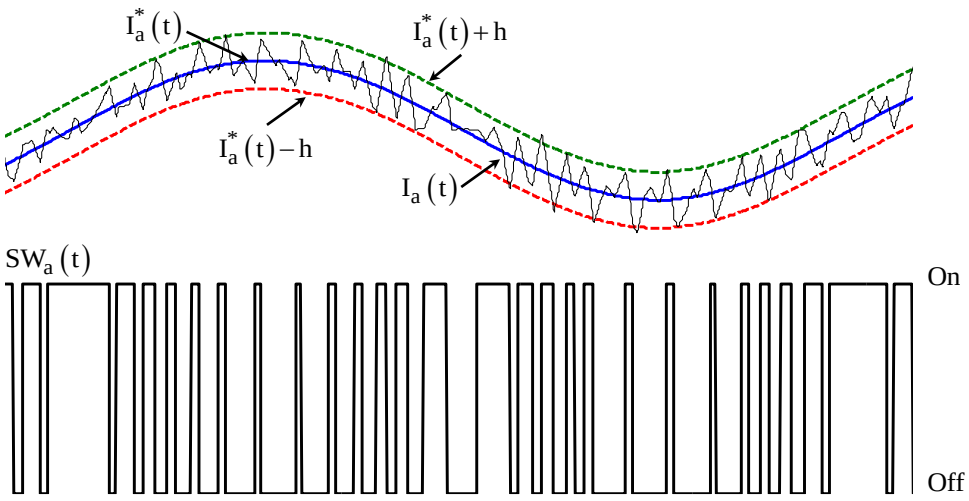


Fig. 3.8 Hysteresis current control in the controller of Fig. 3.2.

With HCC method, the dc voltages across the capacitors are not equal due to non-uniform charging. Furthermore, unbalanced grid can inject zero sequence current components into the neutral-point of the dc-link capacitors. Therefore, a decoupling current control is employed to eliminate the zero sequence current from entering into the neutral-point as shown in Fig. 3.2.

Assume the three-phase supply is operating under balanced condition; summation of phase voltages of the grid and pole voltages of the rectifier are

$$\begin{cases} V_{an}(t)+V_{bn}(t)+V_{cn}(t)=0 \\ V_{am}(t)+V_{bm}(t)+V_{cm}(t)=0 \end{cases} \tag{3.21}$$

Substituting equation (3.21) into (3.1) is obtained by

$$\frac{3V_{mn}(t)}{L}=\frac{dI_a(t)}{dt}+\frac{dI_b(t)}{dt}+\frac{dI_c(t)}{dt} \tag{3.22}$$

From equation (3.22), it is clear that an additional zero sequence current is flowing through the virtual ground. Based on this assumption, a zero sequence current is added in the current control loop to compensate the zero sequence components in the floating ground. This is expressed as

$$\frac{V_{mn}(t)}{L}=\frac{dI_o(t)}{dt} \tag{3.23}$$

Hence, the zero sequence current from equation (3.33) is decoupled with the reference current as given in the following expression.

$$\begin{cases} I_a^*(t)=I_a(t)-I_o(t) \\ I_b^*(t)=I_b(t)-I_o(t) \\ I_c^*(t)=I_c(t)-I_o(t) \end{cases} \tag{3.24}$$

where $L = L_a = L_b = L_c$ of the input filter inductance and $I_o(t)$ is written as

$$I_o(t) = \frac{-V_{dc}(t)}{6L} \int \begin{bmatrix} (1-S_a(t))\,\mathrm{sign}(I_a(t)) \\ +(1-S_b(t))\,\mathrm{sign}(I_b(t)) \\ +(1-S_c(t))\,\mathrm{sign}(I_c(t)) \end{bmatrix} dt \qquad (3.25)$$

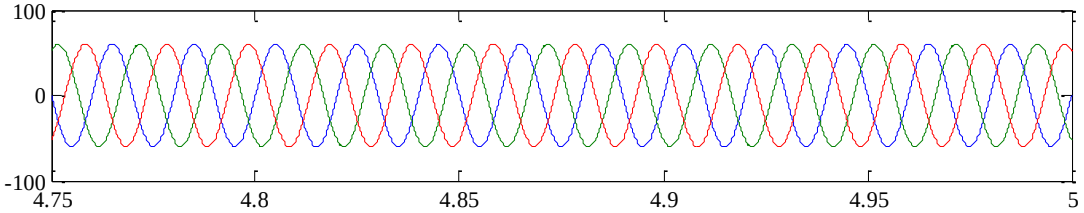
Thus the capacitor voltage unbalance is successfully eliminated by the new reference currents in (3.34) under balanced and unbalanced grid conditions.

3.3 Simulation and Measurement Results

The operation behavior of the three-phase unity power factor rectifier under several operating conditions is verified in MATLAB Simulink with SimCoupler PSIM simulator. The obtained results show the reliability and robustness of the proposed power balanced control strategy with the decoupling current control based on hysteresis fix band in three difference operating conditions. Three cases are simulated from balanced to extreme unbalanced grid condition as shown from Fig. 3.9 to Fig. 3.14.

CASE 1 illustrates the input and output performance of the unity power factor rectifier under balanced and clean grid condition: (Fig. 3.9 and Fig. 3.10).

Balanced grid operation (Fig 3.9) results in low THD content in the input grid current and zero phase shifts on the main phase voltage. Besides, the dynamic behavior (load change) of the converter shows that the dc voltage is tracked well even during a short interval of the voltage dip. With stable dc-link voltage, the voltage across each capacitor is balanced before and after the load change as shown in Fig. 3.10.



(a)

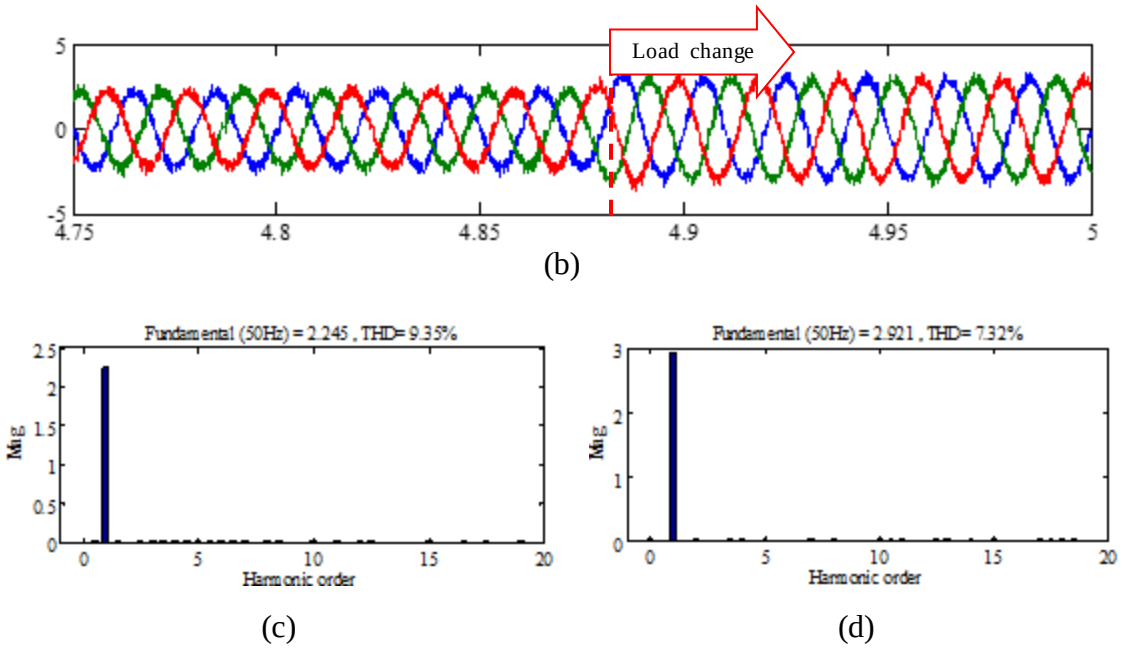


Fig. 3.9 Three-phase voltage and current in CASE 1. (a) Grid voltage, (b) grid current, (c) THD on grid current before load change and (d) THD on grid current after load change at t = 4.875s.

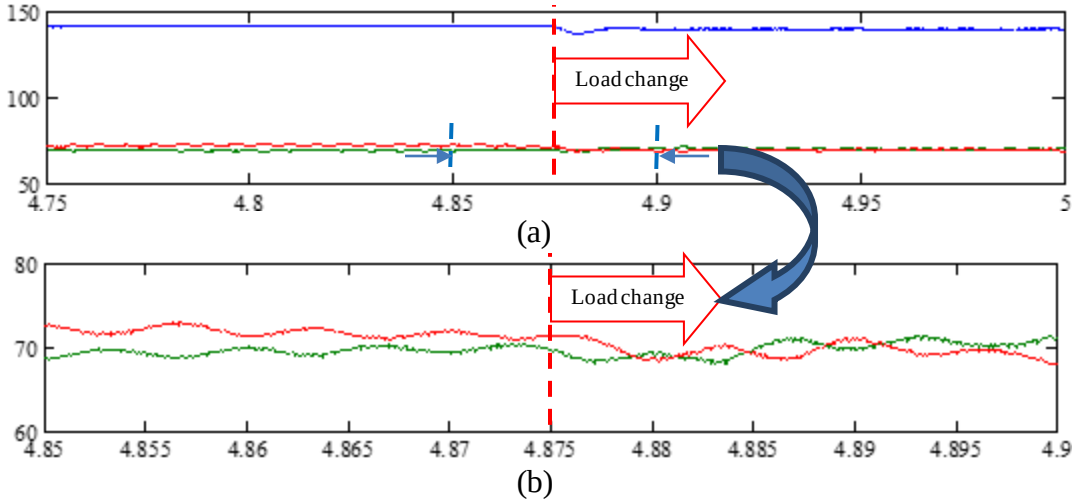


Fig. 3.10 DC bus in CASE 1. (a) DC-link voltage and voltage across capacitor C1 and C2 and (b) balance capacitor voltage before and after load change at t = 4.875s.

CASE 2 illustrates the input and output performance of the unity power factor rectifier under ±10% unbalanced and distorted grid condition: (Fig. 3.11 and Fig. 3.12).

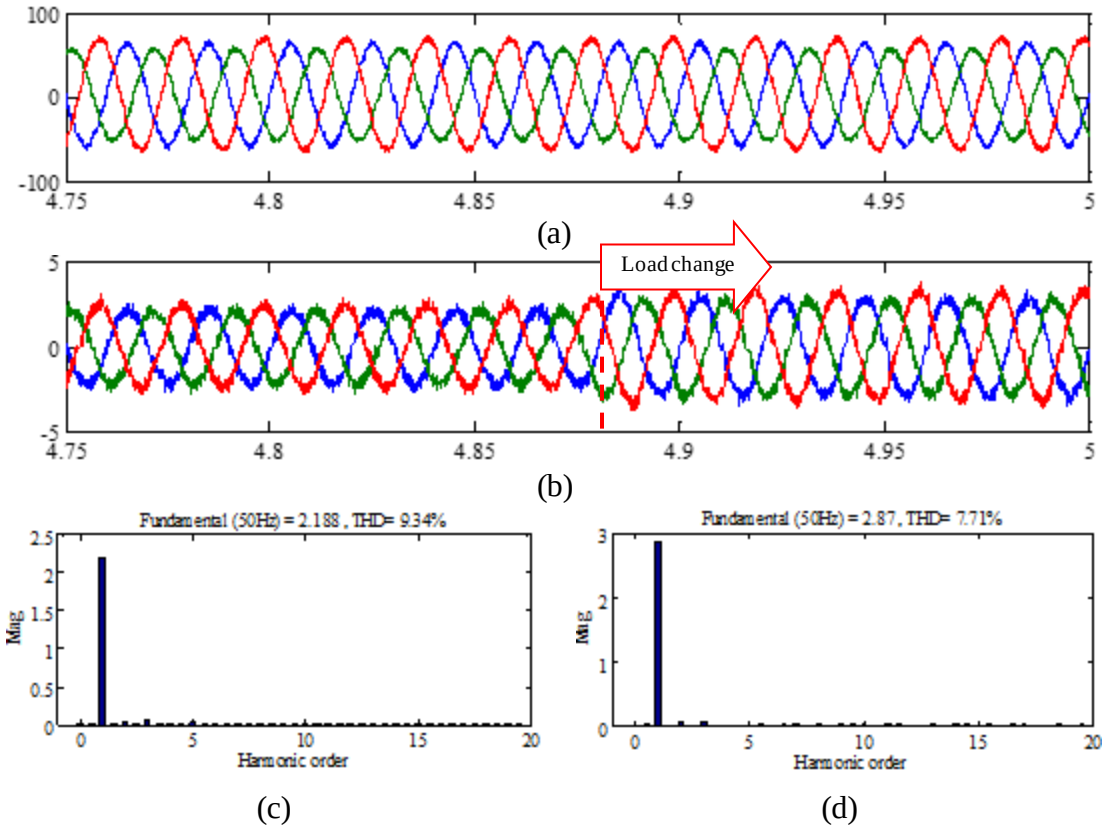


Fig. 3.11 Three-phase voltage and current in CASE 2. (a) Grid voltage, (b) Grid current, (c) THD on grid current before load change and (d) THD on grid current after load change at t = 4.875s.

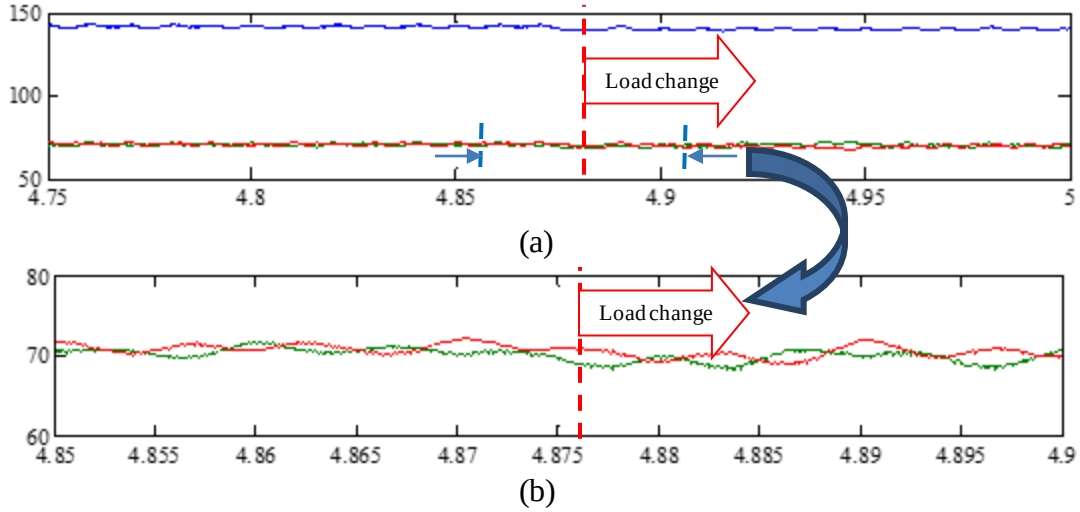


Fig. 3.12 DC bus in CASE 2. (a) DC-link voltage and voltage across capacitor C1 and C2 and (b) balance capacitor voltage before and after load change at t = 4.875s.

To visualize the feasibility of the proposed power balanced control strategy, two operating modes under unbalanced grid condition are analyzed. In CASE 2, the inner

loop current control limits the harmonic current to minimum. The quality of the grid current in CASE 2 is similar to balanced grid operation as shown in Fig. 3.9(c), (d) and Fig. 3.11(c), (d). Under CASE 2 operating conditions, the dynamic performance of the dc-link voltage is well tracked and both capacitor voltages are balanced as shown in Fig. 3.12.

CASE 3 illustrates the input and output performance of the unity power factor rectifier under ±10% unbalanced with phase c short to ground and distorted grid condition: (Fig. 3.13 and Fig. 3.14).

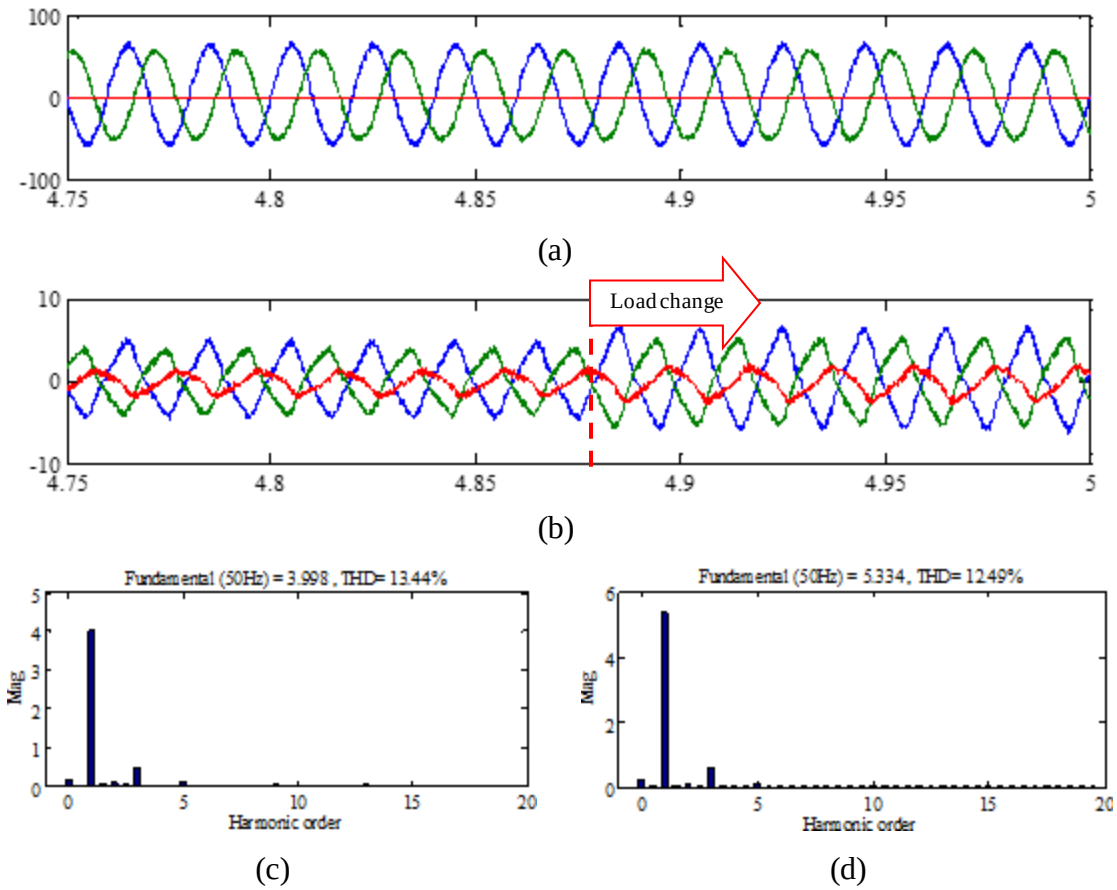


Fig. 3.13 Three-phase voltage and current in CASE 3. (a) Grid voltage, (b) grid current, (c) THD on grid current before load change and (d) THD on grid current after load change at t = 4.875s.

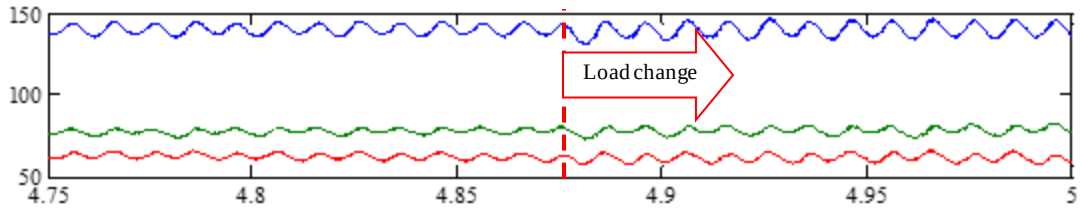


Fig. 3.14 Voltage across each capacitor and DC-link voltage in CASE 3 before and after load change at t = 4.875.

In extreme unbalanced grid conditions, the proposed controller is able to regulate two line currents in phase with their respective phase voltages while the remaining phase is shorted to ground. Besides, the THD current in this CASE 3 is high as compared to CASE 1 and CASE 2. This is due to the occurrence of dominant second order harmonic content in the dc-link. This as well causes distortion in the reference current wave in the inner loop. Furthermore, dc voltage across each capacitor is not balanced due to the existence of negative and zero sequence line current which are heavily injected into the neutral point. However, the proposed controller regulates the power near to unity power factor by which one can extract optimum active power from the grid.

Fig. 3.15 shows the performance of the voltage balancing property with and without decoupling current control. Due to the non-identical parameters of dc-link capacitors, the voltage across each capacitor will be unequal due to non-uniform charging and discharging. In contrast with additional decoupling current control, both the capacitor

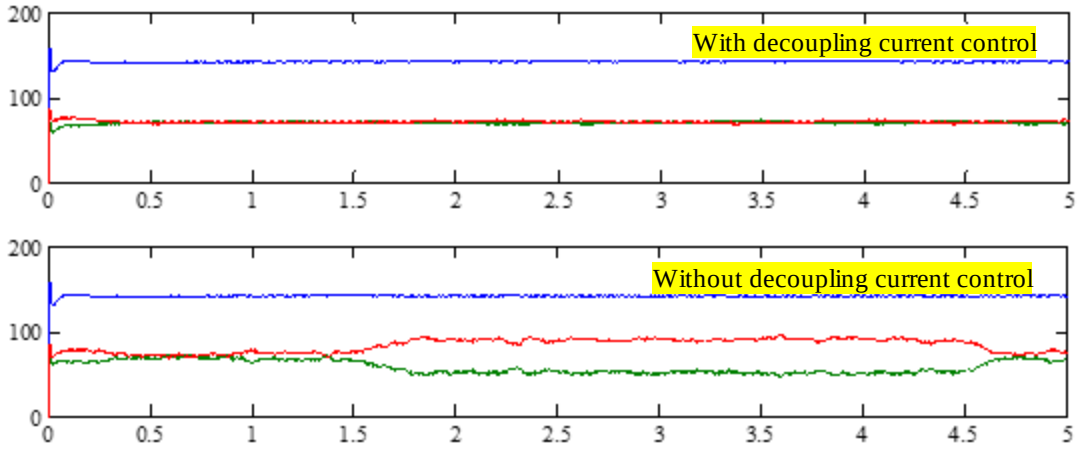


Fig. 3.15 DC-link voltage and voltage across each capacitor in DC bus with and without decoupling current control.

RTI1103 with the MATLAB Simulink program and sampling time of the proposed controller is set to 60μs.

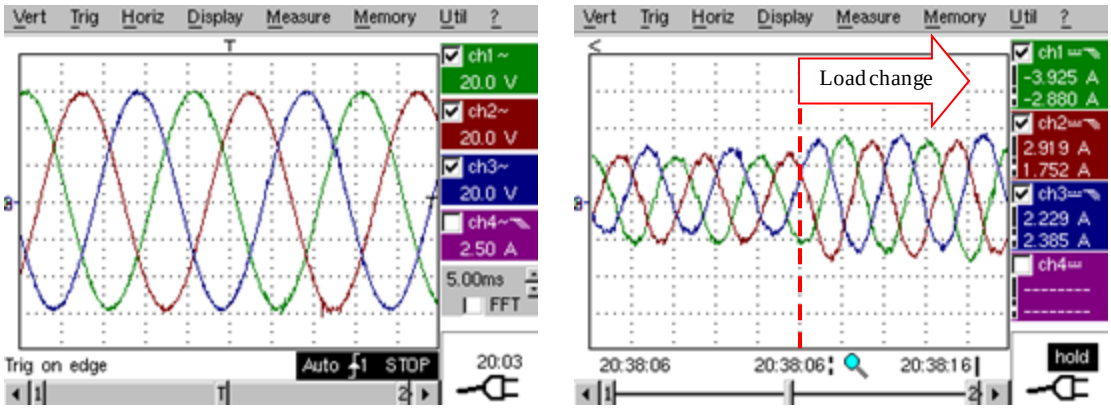
From the obtained experimental results, one can notice that the proposed controller is working well for three operating grid conditions. The obtained results for case 2 and case 3 are constructed based on three isolated single-phase variac transformers.

CASE 1 - Balanced and clean grid condition

TABLE 3.1

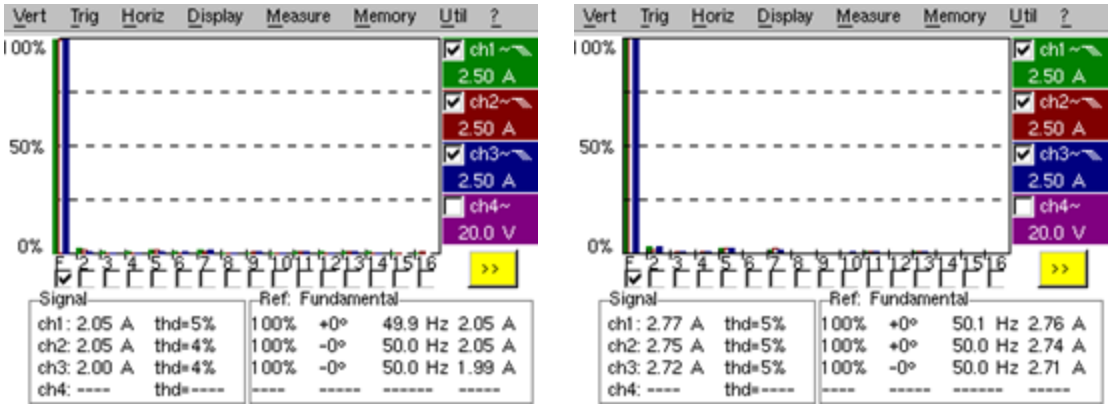
Parameters rating for both simulation and experiment converter test

SIMULATED PARAMETER				EXPERIMENTAL PARAMETER			
Description	Grid Condition			Description	Grid Condition		
	Balanced	Unbalanced	Extremely Unbalanced		Balanced	Unbalanced	Extremely Unbalanced
Grid voltage	42.43 Vrms, 42.43 Vrms, 42.43 Vrms	42.43 Vrms, 38.18 Vrms, 46.67 Vrms	42.43 Vrms, 38.18 Vrms, 0 Vrms	Grid voltage	42.43 Vrms, 42.43 Vrms, 42.43 Vrms	42.43 Vrms, 38.18 Vrms, 46.67 Vrms	42.43 Vrms, 38.18 Vrms, 2.14 Vrms
5^{th}-harmonic voltage	0	0.77 Vrms, 0.76 Vrms, 0.93 Vrms	0.77 Vrms, 0.76 Vrms, 0 Vrms				
Noise voltage (random variable)	0	3.5 Vpeak	3.5 Vpeak				
Frequency	50 Hz	50 Hz	50 Hz	Frequency	50 Hz	50 Hz	50 Hz
Filter Inductor	5 mH	5 mH	5 mH	Filter Inductor	5 mH ± 5%	5 mH ± 5%	5 mH ± 5%
Filter Resistor	0.2 Ω	0.2 Ω	0.2 Ω	Filter Resistor	0.2 Ω ± 1%	0.2 Ω ± 1%	0.2 Ω ± 1%
DC capacitor C1	1050 μF	1050 μF	1050 μF	DC capacitor C1	1000 μF ± 20%	1000 μF ± 20%	1000 μF ± 20%
ESR resistor C1	110 m Ω	110 m Ω	110 m Ω	ESR resistor C1	100 m Ω	100 m Ω	100 m Ω
DC capacitor C2	920 μF	920 μF	920 μF	DC capacitor C2	1000 μF ± 20%	1000 μF ± 20%	1000 μF ± 20%
ESR resistor C2	80 m Ω	80 m Ω	80 m Ω	ESR resistor C2	100 m Ω	100 m Ω	100 m Ω



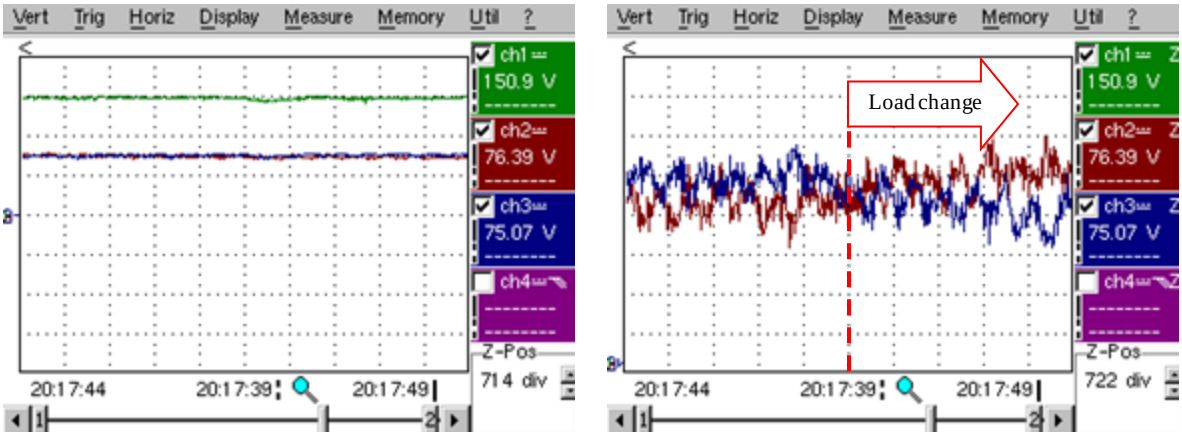
(a) (b)

Fig. 3.16 Three-phase voltage and current for CASE 1. (a) Grid voltage and (b) grid current.



(a) (b)

Fig. 3.17 FFT of the three-phase grid current for CASE 1. (a) Before load change and (b) after load change.



(a) (b)

Fig. 3.18 DC bus voltage for CASE 1. (a) DC-link voltage and voltage across each dc capacitor and (b) voltage across both dc capacitors.

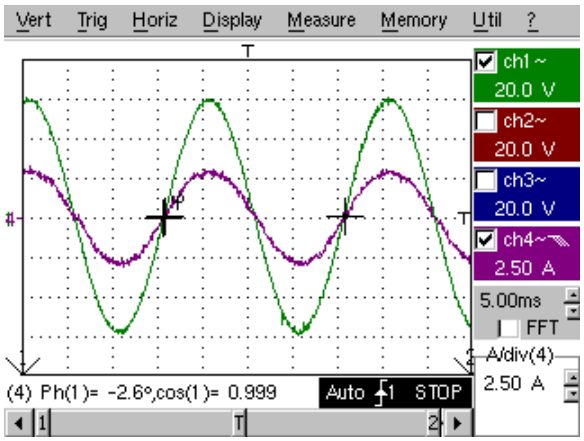
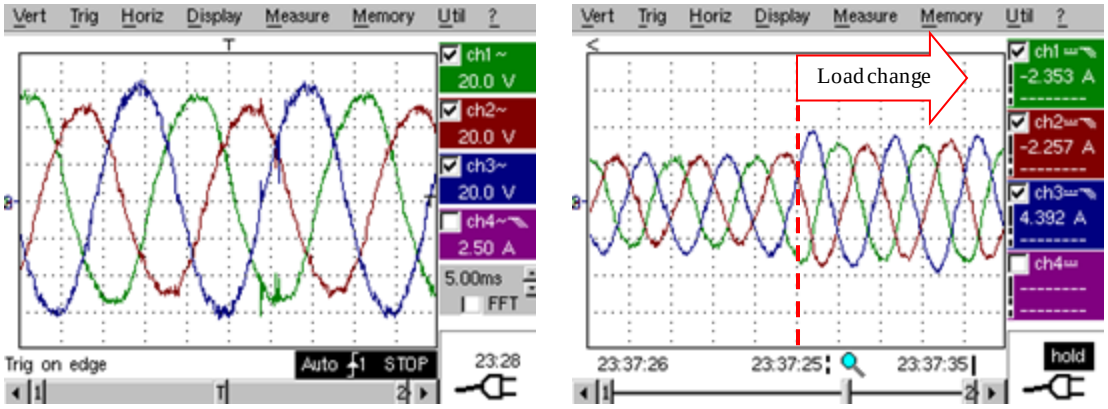


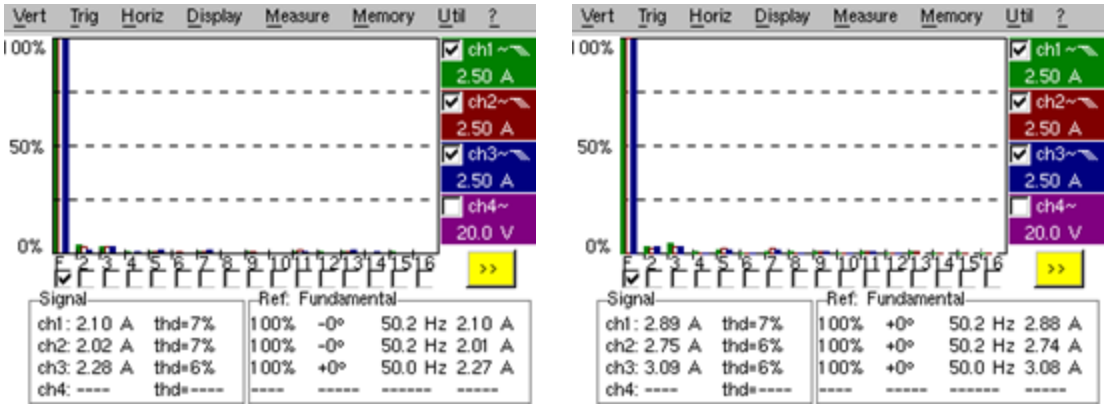
Fig. 3.19 Power factor measurement is defined by the phase 'a' voltage and current for CASE 1.

CASE 2 - Unbalanced and distorted grid condition with ±10% of the nominal phase voltage



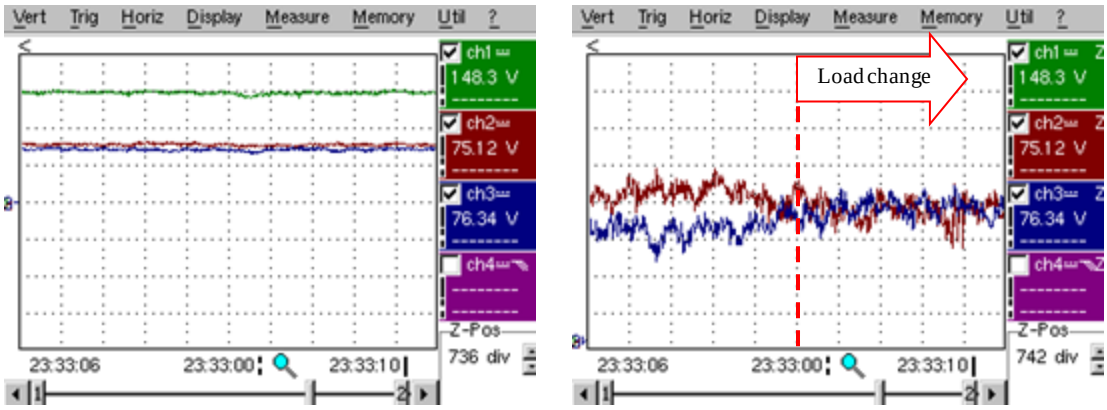
(a) (b)

Fig. 3.20 Three-phase voltage and current for CASE 2. (a) Grid voltage and (b) grid current.



(a) (b)

Fig. 3.21 FFT of the three-phase grid current for CASE 2. (a) Before load change and (b) after load change.



(a) (b)

Fig. 3.22 DC bus voltage for CASE 2. (a) DC-link voltage and voltage across each dc capacitor and (b) voltage across both dc capacitors.

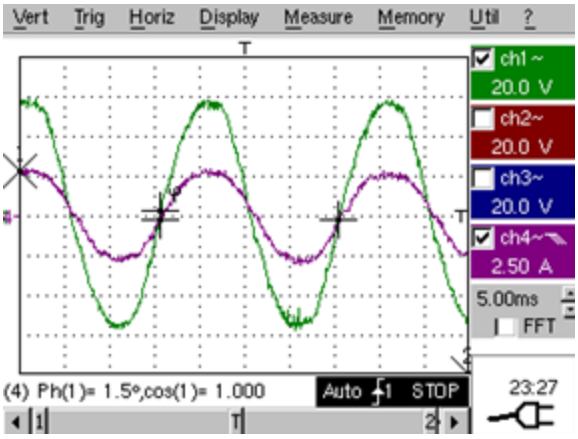
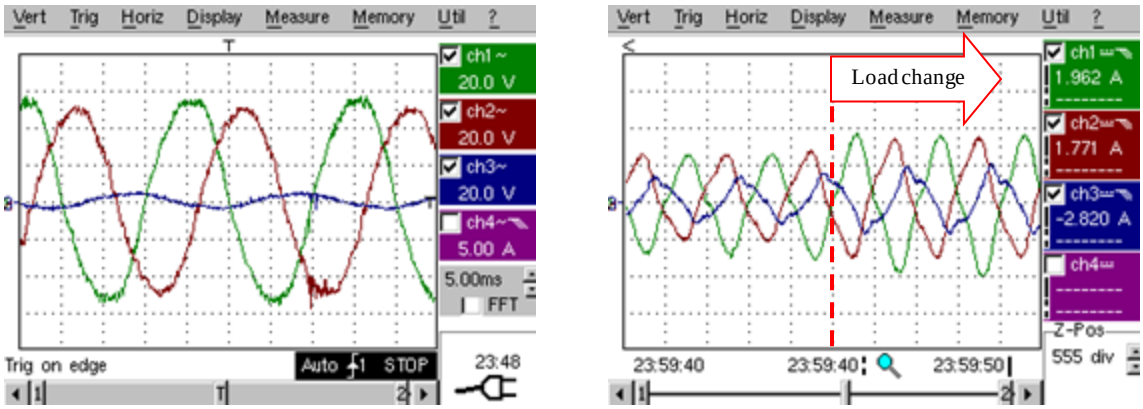


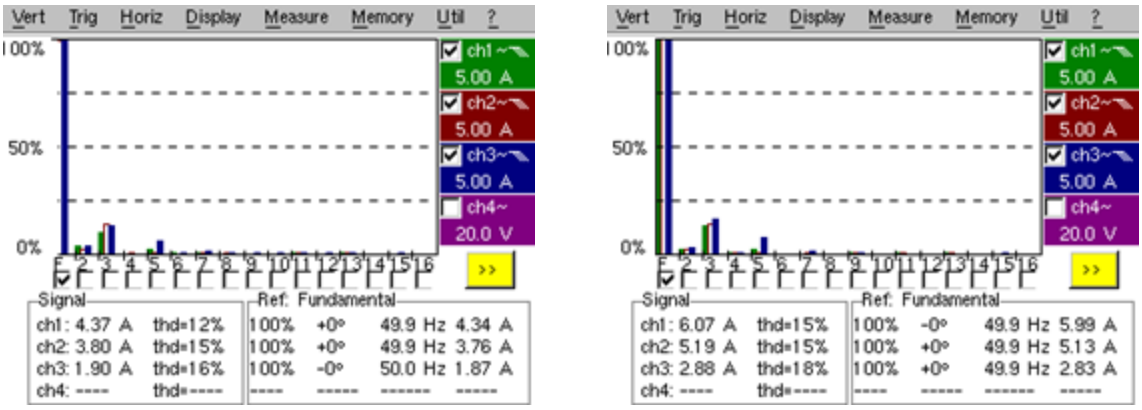
Fig. 3.23 Power factor measurement is defined by the phase 'a' voltage and current for CASE 2.

CASE 3 - Unbalanced and distorted grid condition with phase c down



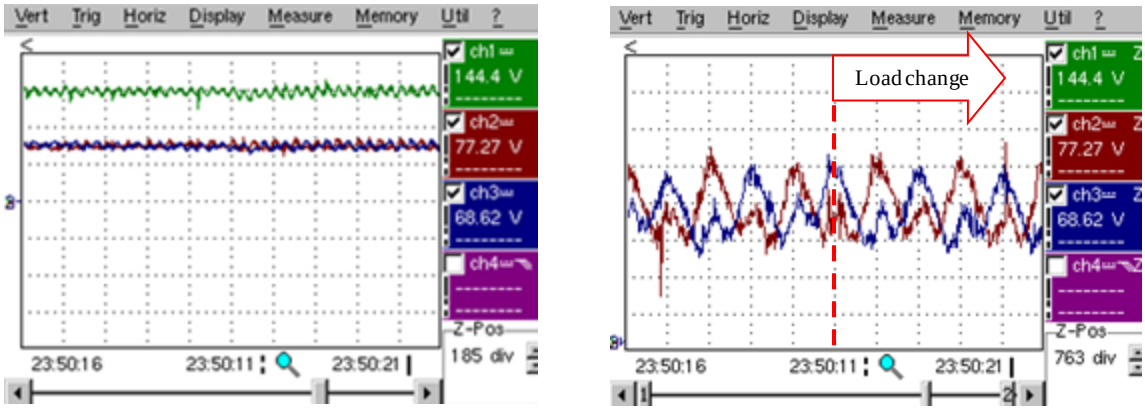
(a) (b)

Fig. 3.24 Three-phase voltage and current for CASE 3. (a) Grid voltage and (b) grid current.



(a) (b)

Fig. 3.25 FFT of the three-phase grid current for CASE 3. (a) Before load change and (b) after load change



(a) (b)

Fig. 3.26 DC bus voltage for CASE 3. (a) DC-link voltage and voltage across each dc capacitor and (b) voltage across both dc capacitors.

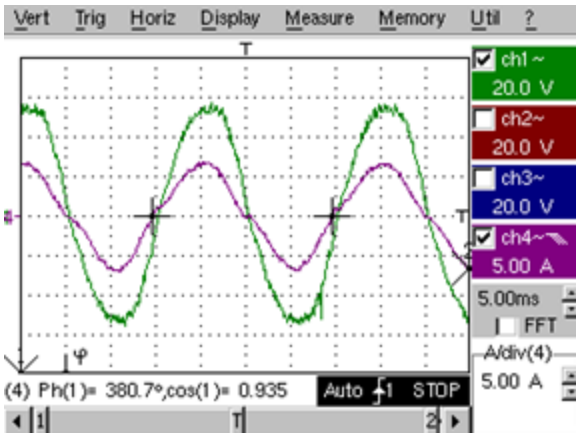


Fig. 3.27 Power factor measurement is defined by the phase ‘a’ voltage and current for CASE 3.

The voltage across capacitors in case 1, 2 and 3 are balanced with reduced zero sequence current through the neutral-point of the star-connected bidirectional switches as shown in Fig. 3.18, Fig 3.22 and Fig. 3.26 respectively. The phase currents in the grid for case 1, 2 and 3 are shaped closely to a sinusoidal waveform with hysteresis current regulator as shown in Fig. 3.16, Fig. 3.20 and Fig. 3.24 respectively. However, the phase currents in the grid under balanced condition in Fig. 3.16(b) are slightly unbalanced. This is due to the limitation of the sampling time of the dSPACE controller board, which results an error in current within the limits of fixed hysteresis band. Hence, the peak current of the grid can cause small overshoot current error. However, the THD of the three-phase currents in case 1 and 2 are still considerably low and THD is limited in the range of 3 to 7%.

Such proposed power balance control strategy with the decoupled current control, a good current compensation is obtained, voltage across the capacitors in the dc-link is balanced and near to unity power factor operation is achieved.

3.5 Discussion

The objective of this chapter was to introduce the power balanced control strategy with decoupling current control in this unidirectional three-level rectifier. With this proposed control method, the rectifier does not require any bulky and expensive passive filters to eliminate the input current harmonic while yielding low output dc ripple voltage. Hence, the current compensation effort in the L filter (first order filter) is low due to the synthesizing of zero pole voltage through the aid of three switches.

The experiment results in this chapter proved that the proposed current control can be an alternative solution without the need of using complicated control algorithms. Based on the obtained experiment results, the grid current has a sinusoidal waveform with low harmonic distortion contents. Unity power factor is also achieved even after a sudden load change is performed. Hence, the three-level rectifier behaves like a symmetrical resistive load. Moreover, the voltages distributed across the two dc capacitors are almost equal. This is achieved with the compensation from the zero sequence current control.

Such power balanced control method with the zero sequence current control for the multilevel rectifier can be an excellently retrofit for grid connected or PMSG connected in wind turbine applications.

Chapter 4 – Review on Existing Multilevel Inverter Topologies

Variable speed drives have been widely used in many industrial applications. They basically consist of an inverter to drive the machine. Besides, renewable energy such as wind and solar is integrated with the inverter to supply the consumer loads. The high power applicability of such systems for implementation in rural area is being investigated.

Since the voltage source inverters (VSI) are allowed to conduct with high switching speed and fast transient response VSI topologies will be reviewed instead of current source inverter (CSI). CSI based on SGCT, GTO or SCR, as switching devices, will limit the switching frequency range and involves a complex the gate circuitry design. This contributes to more losses in CSI than in VSI configuration [72, 73]. Furthermore, an inverter operating at low switching frequency and driving an induction motor can cause a high ripple current and excessive heating of the windings of the motors [72]. Therefore, VSI topologies will be further investigated in this report.

4.1 Traditional Two-Level Inverter

A traditional two-level voltage source inverter is shown in Fig. 4.1. This type of inverter topology has been widely used for induction motor drives since 1990s due to its fast switching characteristic performance. The high switching frequency (at least 6 kHz) must be selected for this converter [74] to suppress the magnitude of low order harmonic component, which results in reduction in filter size.

The thumb rule in control theory of the operating switching frequency range for two-level inverter must be 10 times higher than the resonant frequency of the LC filter, which is proven by Steinke [74]. If a 5 kHz switching frequency is to be used for a two-level inverter driving a load of 50 Hz, the resonant frequency of the LC filter must be set to a minimum of 500 Hz. This shows that a reduction of filter requirement with high resonant

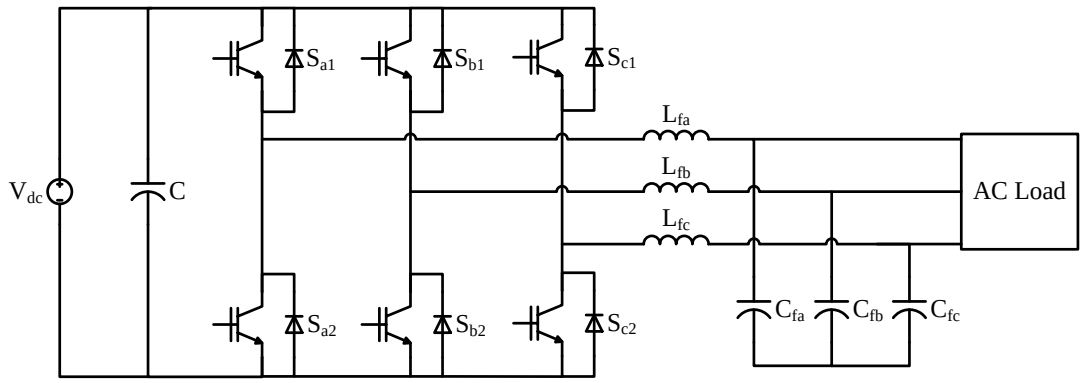


Fig. 4.1 Traditional two-level inverter circuit.

frequency is done by selecting very high switching frequency. However, two-level inverter with high switching frequency may cause high dv/dt across power semiconductor devices. Under such condition, the switching device may experience high voltage spike which is higher than the dc-link voltage. Hence, a device with higher voltage rating must be selected. Devices with such high voltage rating incur an additional switching loss due to additional stray losses occurring during the switching transition.

4.2 Multilevel Inverter Topologies

In the late 1990s, multilevel inverters are the most attractive solution for high power and medium voltage drive when high power IGBTs is commercially available in the market. Multilevel inverters are implemented to overcome the disadvantages of traditional two-level inverter due to several factors, and a few are:

(1) The converter is operated at lower switching frequency as the number of incremental output voltage steps increase. This serves the advantages of low switching losses and low dv/dt which leads to low electromagnetic interference (EMI) and a requirement of snubber circuit is minimized.

(2) The LC filter in n-level inverter topologies is designed to operate at high resonant frequency at the same carrier frequency than the one obtained in two-level inverter. High resonant frequency gives reduction in the filter size. The factor of the resonant frequency is at least 10 times fundamental frequency (50 Hz) multiple by the number of level [74].

(3) THD is reduced as the number of incremental output voltage levels is increased. This serves as a benefit when the induction motor is connected to the drive system with a long cable as the cable inductance is predominantly high. This acts as a filter and results in reduced core losses in the machine and voltage stress at the contact point of cables and motor.

(4) Semiconductor devices of lower rating can be used for low and high power inverter applications. This is because the conduction loss is low as compared to higher rating device.

The following sub-section will introduce several topologies of multilevel inverter.

4.2.1 Cascaded Multilevel Inverter (CMI)

Fig. 4.2 shows a three-phase cascaded H-bridge multilevel inverter. Each cell consists of four switching device and a minimum of one dc capacitor to form a single-phase H-

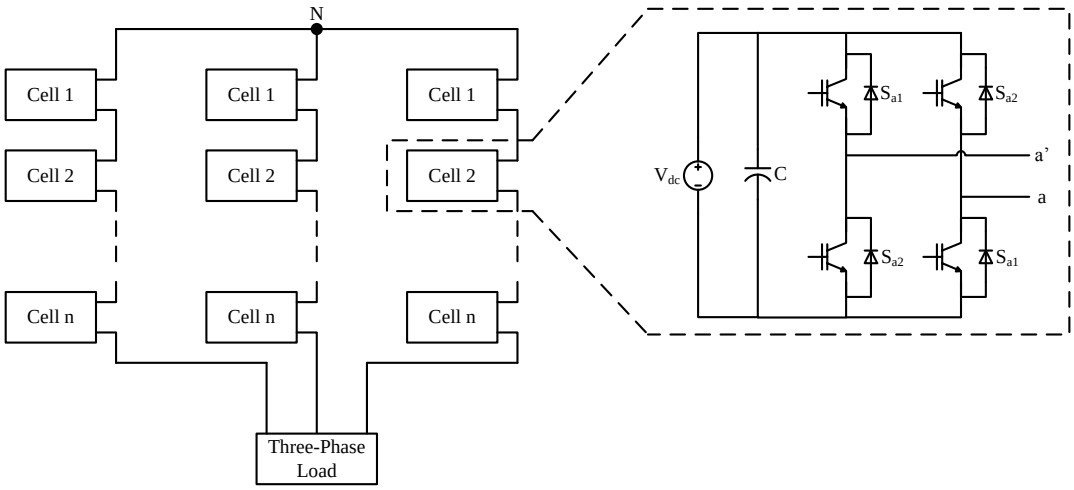


Fig. 4.2 Cascaded H-bridge multilevel inverter.

bridge inverter. The different cells are connected as depicted in Fig 4.2 to construct a three-phase configuration. With this configuration, each cell in a leg will provide three-level output phase voltage (V_{aN}, V_{bN} and V_{cN}) and five level line voltages (V_{ab}, V_{bc} and V_{ca}). The number of incremental voltage step is increased by connecting additional cell in series, where the number of phase voltage level is formulated as (n^{th}-cell × 2) + 1.

This type of multilevel inverter topologies can reduce the number of switching devices, but it requires multiple isolated dc supply to operate the converter [75].

4.2.2 Modular Multilevel Inverter (MMI)

Fig. 4.3 shows a three-phase modular multilevel inverter. Each cell can either be constructed as a single-phase half-bridge or full-bridge inverter. The configuration of

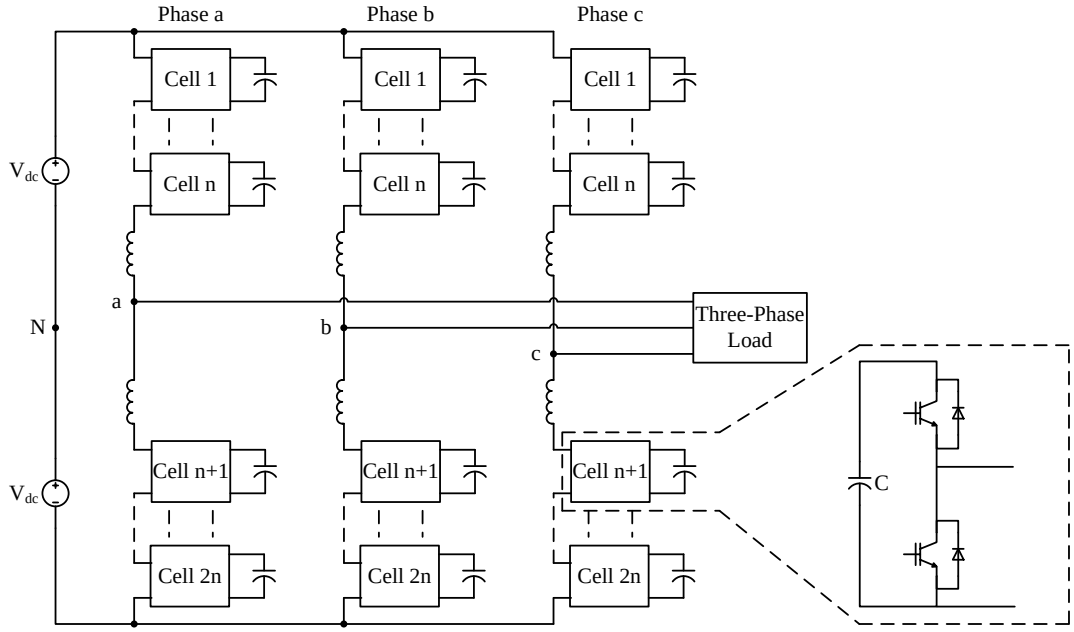


Fig. 4.3 Modular multilevel inverter.

the cell in Fig. 4.3 is based on single-phase half-bridge inverter. This type of inverter is seen in HVDC application due to its merits on high power capability and single dc bus [76, 77]. Such converter with single dc bus supply does not require any isolated phase-shifted transformer as compared to cascaded H-bridge inverter. However, this converter requires number of components which are bulky when compared to multilevel flying capacitor inverter (MFCI). The increase in number of voltage levels causes floating voltage across the capacitors [77].

4.2.3 Multilevel Diode-Clamped Inverter (MDCI)

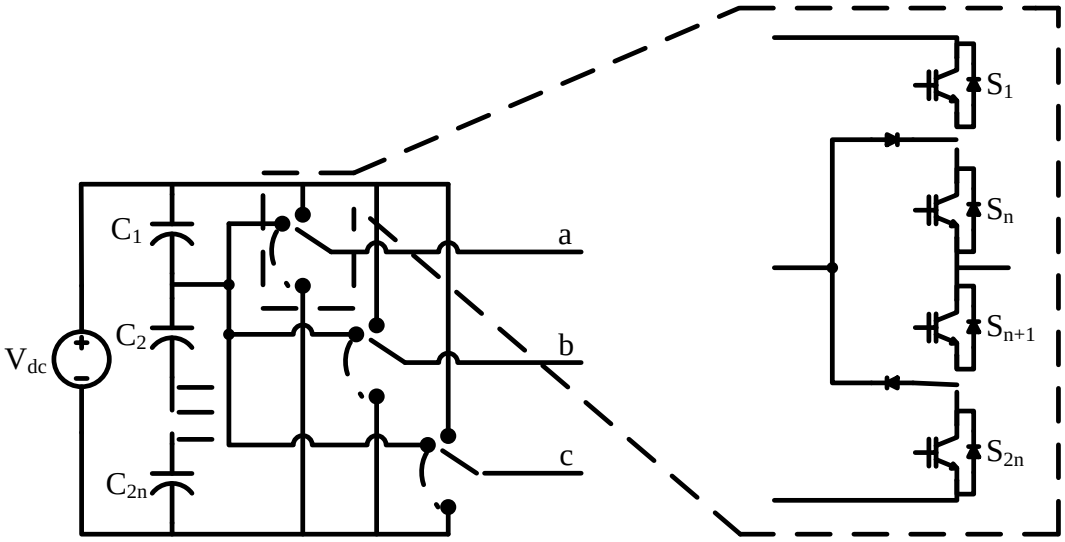


Fig. 4.4 n-level diode-clamped inverter.

Fig. 4.4 shows per-phase leg n-level diode-clamped inverter circuit (right) and three-phase single-pole multilevel diode-clamped inverter diagram (left). The incremental output voltage level is supplied by the series capacitors clamped through the diodes in the single dc bus. The switching devices and diode elements are simplified into a single switching pole as depicted in Fig. 4.4 (left diagram), which forms a per-phase single-pole nth-level diode-clamped circuit. The capacitor voltage in dc bus for converters with output voltage levels greater than three is unbalanced. Hence, the differential voltage between the dc-link capacitors voltages is minimized with modified space vector modulation [78] or dc voltage balancing circuit [34, 79-81], etc. Such problems and proposed solutions for this converter will be further discussed in the following chapters.

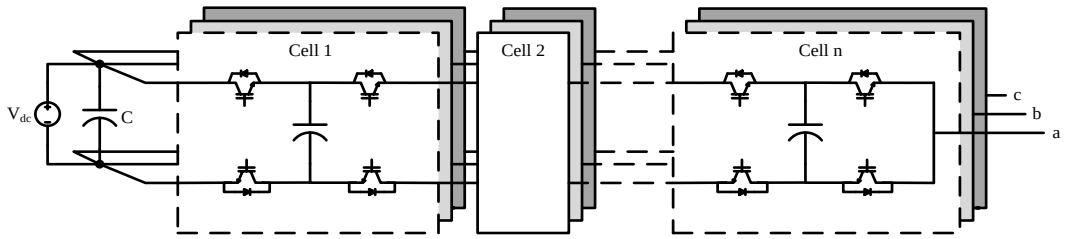


Fig. 4.5 n-level flying capacitor inverter

4.2.4 Multilevel Flying Capacitor Inverter (MDCI)

Instead of diode clamped, Fig. 4.5 shows an alternative multilevel inverter with the same amount of switching devices for the n-level approach. Each capacitor is supplied with their respective dc voltage level and forms an incremental output voltage. This topology has certain advantages when compared to MDCI topology i.e. simple balancing method and better efficiency as compared to five-level diode-clamped inverter. The analysis and proposed solution of this topology will be discussed in the following chapters.

4.2.5 Generalized Multilevel Inverter (GMI)

Fig. 4.6 shows the n-level generalized multilevel inverter, which is proposed by Fang [82]. This topology serves the advantage of self-voltage balancing property and high incremental voltage level. However, this topology is limited to certain power level due to the higher rating switching devices required at the terminal connecting to the load. Besides, this topology requires more number of switches and capacitors, which results an increase in size of the converter and high production cost. Thermal aging and capacitor sizing for unequal voltage stress level across each capacitor is complicated to design. Therefore, this topology is applicable in low power application such as an automobile system.

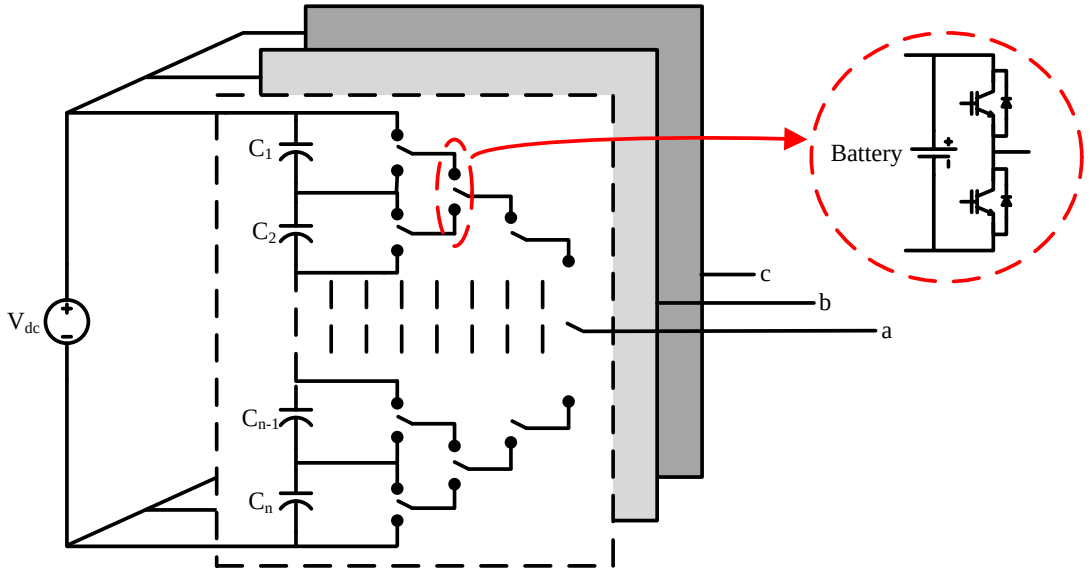


Fig. 4.7 n-level generalized multilevel inverter.

4.2.6 Multilevel Flying Capacitor based ANPC Inverter

Fig. 4.7 shows a modification of flying capacitor multilevel inverter based on ANPC inverter [83]. ANPC inverter is known as the active neutral-point-clamped, where both

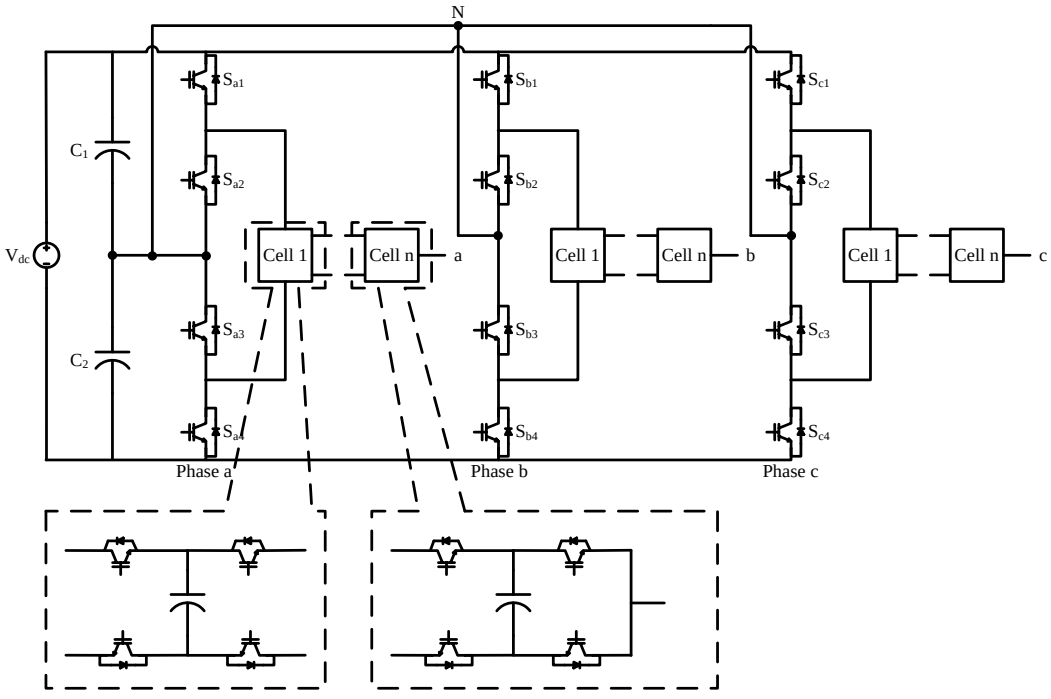


Fig. 4.6 n-level flying capacitor based ANPC inverter.

active switching devices are clamped at the neutral-point of the dc capacitors as shown in Fig. 4.7. The number of levels in this topology can be increased by adding more cells in series. However, this type of topology will complicate the control algorithm for the floating capacitor voltage when more cells are added in series.

Chapter 5 – Mathematical Model for Three-Level Inverter Topologies under Steady-State Condition

This chapter demonstrates the mathematical analysis of operating modes of the two basic multilevel inverter topologies: three-level diode-clamped inverter and flying capacitor inverter. Mathematical analysis in this section is examined on balanced load and balanced dc bus voltage under steady-state condition. Where the analysis of a three-level diode-clamped inverter in section 5.1 is adopted based on [84]. Moreover, theoretical analysis in this section is verified in simulation and experimental results. To obtain a better performance, voltage across each dc capacitor must be equally distributed. Achieving balanced dc-link and balanced load has several perceived advantages such as good output voltage/current quality and distributes the voltage stress equally across the semiconductor devices [85].

5.1 Three-Level Diode-Clamped Inverter Topology

A three-level diode-clamped inverter circuit is shown in Fig. 5.1. This topology requires six identical fast recovery diodes (i.e. D_{s+} and D_{s-}) connected to the virtual ground node 'm', two dc capacitors and twelve identical insulated gate bipolar transistors (IGBT) to generate a three-level output voltages waveform. The switching pattern of a three-level diode-clamped inverter requires two unipolar triangular carrier and modulated control signal ($M_a(t)$, $M_b(t)$ and $M_c(t)$) as shown in Fig. 5.2. The modulating signal is compared with level shifted triangular waves to generate gate signals for switches in each leg. Thus, switching requirement for per-phase leg 'a' is determined as:

$$\begin{cases} S_{a1} + S_{a3} = 1 \\ S_{a2} + S_{a4} = 1 \end{cases} \tag{5.1}$$

S_{a1}, S_{a2}, S_{a3} and S_{a4} is represent the switching logic in 1 or 0 (turn on = 1 and turn off = 0).

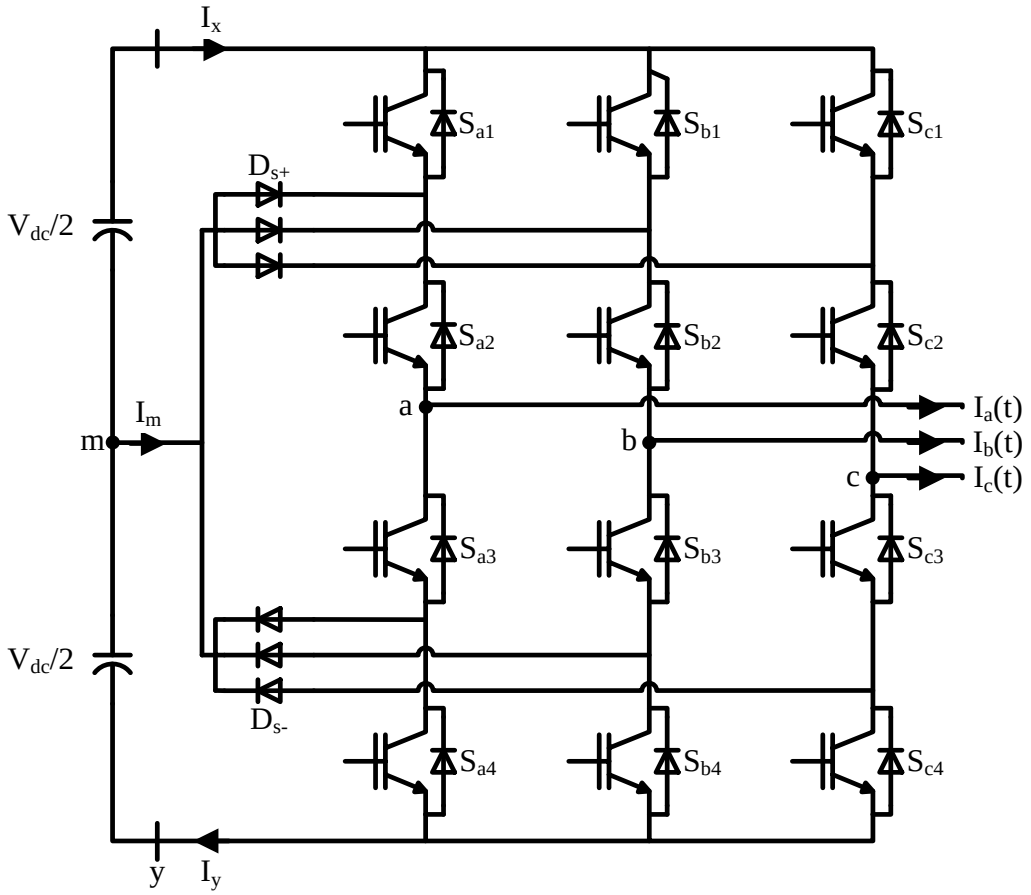


Fig. 5.1 Three-level diode-clamped inverter circuit.

Fig. 5.2 shows the switching pattern for positive modulation signal with a level shifted pulse width modulation (LSPWM) technique for both three-level diode-clamped inverter and flying capacitor inverter. The modulation signals of phase 'a' is separated into two sub-modulation ($M_{a1}(t)$ and $M_{a2}(t)$) to operate in a linear region within the carrier frequency range. The positive modulation equation is expressed as:

$$M_{a1}(t) = \frac{-2}{T_s} t_{a1} + 1$$
$$M_{a2}(t) = \frac{-2}{T_s} t_{a2} \tag{5.2}$$

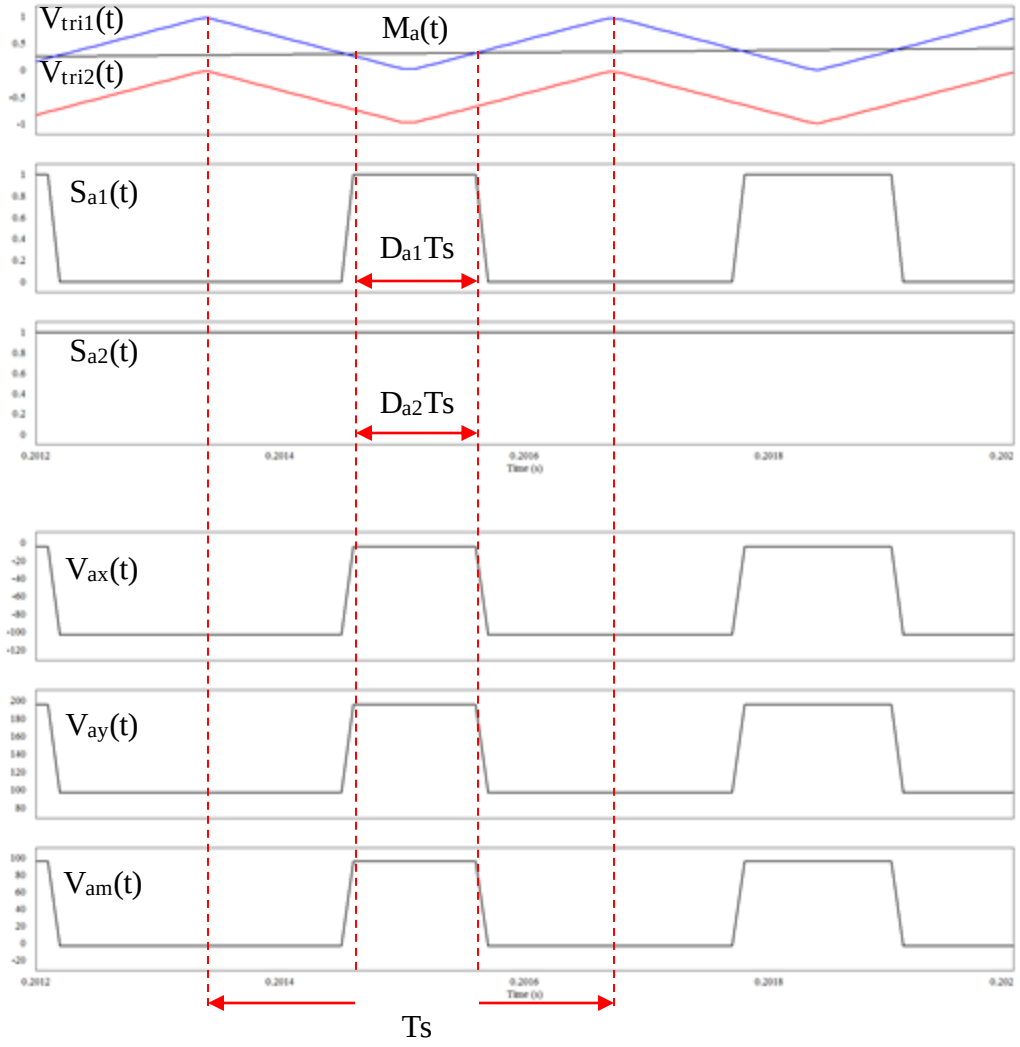


Fig. 5.2 Switching pattern with a specific duty ratio at particular positive modulation signal.

T_s is the time period of carrier wave. Assume the duty ratio D at any value between 0 and 1, then at a specific amplitude of modulation signal, the time interval of $t = T_s(1-D)/2$ is shown in Fig. 5.2. Hence, equation (5.2) is simplified as:

$$m_{a1} = \frac{-2}{T_s}\frac{T_s\left(1-D_{a1}\right)}{2}+1 = D_{a1}$$
$$m_{a2} = \frac{-2}{T_s}\frac{T_s\left(1-D_{a2}\right)}{2} = D_{a2}-1 \qquad (5.3)$$

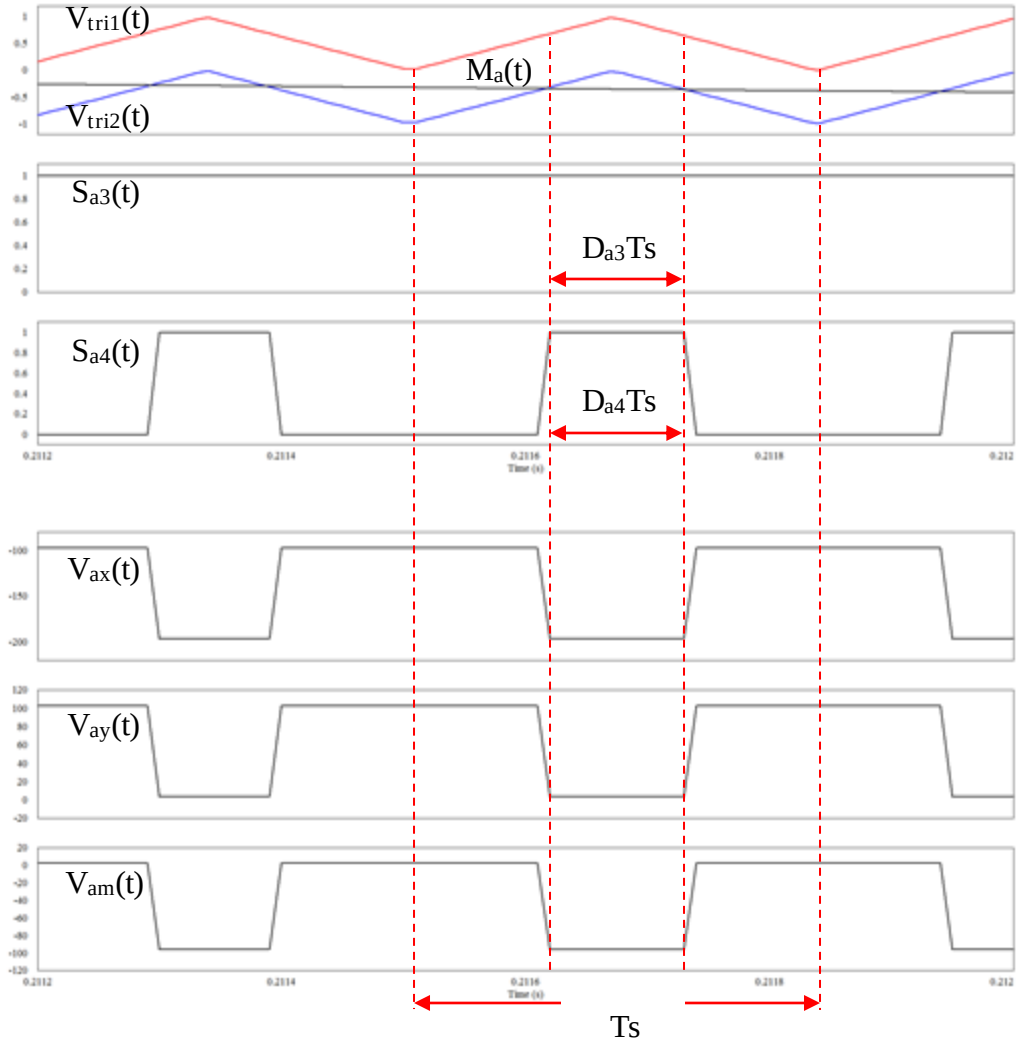


Fig. 5.3 Switching pattern with a specific duty ratio at particular negative modulation signal.

Positive amplitude of modulation for both topologies (three-level diode-clamped inverter and three-level flying capacitor inverter) is expressed as:

$$m = m_{a1} + m_{a2} = D_{a1} + D_{a2} - 1 = S_{a1} + S_{a2} - 1 \tag{5.4}$$

Fig. 5.3 shows the switching pattern on negative modulation signal with a level shifted pulse width modulation (LSPWM) technique for three-level diode-clamped inverter. The switching patterns on a negative modulation signal for a flying capacitor inverter are opposite with the respect to the three-level diode-clamped inverter, equation (5.5) to (5.7) are depicted for diode-clamped inverter. The derivation of negative modulation

signals applied on phase 'a' are similar to the method presented in equation (5.2) to (5.4). The negative sub-modulation equation is expressed as:

$$\begin{aligned} M_{a3}(t) &= \frac{-2}{T_s} t_{a3} + 1 \\ M_{a4}(t) &= \frac{-2}{T_s} t_{a4} \end{aligned} \tag{5.5}$$

Let $t = DT_s/2$ and substitute t into equation (5.5)

$$\begin{aligned} m_{a3} &= \frac{-2}{T_s} \frac{D_{a3} T_s}{2} + 1 = 1 - D_{a3} \\ m_{a4} &= \frac{-2}{T_s} \frac{D_{a4} T_s}{2} = -D_{a4} \end{aligned} \tag{5.6}$$

Hence, the negative amplitude modulation signal for three-level diode-clamped inverter is:

$$m = m_{a3} + m_{a4} = 1 - D_{a3} - D_{a4} = 1 - S_{a3} - S_{a4} \tag{5.7}$$

For three-level flying capacitor inverter the negative amplitude modulation signal is:

$$m = m_{a3} + m_{a4} = 1 - D_{a3} - D_{a4} = 1 - S_{a3} - S_{a4} \tag{5.8}$$

From the above details, the output pole voltage is derived from the two consecutive equations as:

$$\begin{cases} V_{sx}(t) = V_{xm}\left[S_{s1}(t) + S_{s2}(t)\right] - V_{dc}(t) = \dfrac{V_{dc}(t)}{2}\left[S_{s1}(t) + S_{s2}(t)\right] - V_{dc}(t) \\ V_{sy}(t) = V_{ym}\left[S_{s3}(t) + S_{s4}(t)\right] + V_{dc}(t) = -\dfrac{V_{dc}(t)}{2}\left[S_{s3}(t) + S_{s4}(t)\right] + V_{dc}(t) \\ V_{sm}(t) = \dfrac{V_{sx}(t) + V_{sy}(t)}{2} = \dfrac{V_{xm}}{2}\left[S_{s1}(t) + S_{s2}(t)\right] + \dfrac{V_{ym}}{2}\left[S_{s3}(t) + S_{s4}(t)\right] \\ \qquad = \dfrac{V_{dc}(t)}{4}\left\{\left[S_{s1}(t) + S_{s2}(t)\right] - \left[S_{s3}(t) + S_{s4}(t)\right]\right\} \end{cases}$$

(5.9)

$V_{sx}(t)$ and $V_{sy}(t)$ is the voltage occurring at the lower and upper terminal of the three-level diode-clamped inverter with respect to node 'x' and 'y' respectively. Whereas $V_{sm}(t)$ is the phase voltage for the individual leg of the inverter with respect to the neutral point 'm'. Based on equation (5.1) and (5.4), the average phase voltage $\bar{\upsilon}_{sm}(t)$ is regulated between the duty ratio and amplitude of the modulating signals. If m_s change from -1 to 1, then the average phases voltage $\bar{\upsilon}_{sm}(t)$ change linearly from $-V_{dc}/2$ to $+V_{dc}/2$. Thus, the average phase voltage $\bar{\upsilon}_{sm}(t)$ is known as:

$$\begin{aligned}\bar{v}_{sm}(t) &= \frac{V_{dc}}{4}\left\{\left[S_{s1}(t)+S_{s2}(t)\right]-\left[1-S_{s1}(t)+1-S_{s2}(t)\right]\right\}\\ &= \frac{V_{dc}}{2}\left[S_{s1}(t)+S_{s2}(t)-1\right]\\ &= \frac{V_{dc}}{2}m_s\end{aligned} \tag{5.10}$$

where $\bar{\upsilon}_{sm}(t)$ is the individual average phase voltage ($\bar{\upsilon}_{am}(t)$, $\bar{\upsilon}_{bm}(t)$ and $\bar{\upsilon}_{cm}(t)$) and m_s is the modulation signal (m_a, m_b and m_c) as stated in equation (5.4). For the simplicity of control, a sinusoidal voltage/ current are given at the AC terminal of a three-level diode-clamped inverter. The control loop must able to changes the amplitude of a modulation signals with sinusoidal time function with the angular operating frequency ωt and initial phase angle θ_0. Thus, the phase voltages of the three-phase terminal are expressed as:

TABLE 5.1

THREE-LEVEL DIODE-CLAMPED INVERTER CORRESPONDING SWITCHING STATES

State	**Switching States**				**Per-Phase Leg Voltage**		
	S_{s1}	**S_{s2}**	**S_{s3}**	**S_{s4}**	**V_{sx}**	**V_{sy}**	**V_{sm}**
1	1	1	0	0	0	V_{dc}	$V_{dc}/2$
2	0	1	1	0	$-V_{dc}/2$	$V_{dc}/2$	0
3	0	0	1	1	$-V_{dc}$	0	$-V_{dc}/2$

Where 's' represent phase a, b and c and S_{s1} to S_{s4} are presented as the IGBT switching devices for individual leg. Logic 1 represent as turn on and logic 0 represent as turn off for S_{s1}, S_{s2}, S_{s3} and S_{s4}

$$\begin{cases} V_{am}(t) = \dfrac{V_{dc}}{2} M_a(t) = \dfrac{V_{dc} m \cos(\omega t + \theta_0)}{2} \\ V_{bm}(t) = \dfrac{V_{dc}}{2} M_b(t) = \dfrac{V_{dc} m \cos\left(\omega t + \theta_0 - \dfrac{2\pi}{3}\right)}{2} \\ V_{cm}(t) = \dfrac{V_{dc}}{2} M_c(t) = \dfrac{V_{dc} m \cos\left(\omega t + \theta_0 - \dfrac{4\pi}{3}\right)}{2} \end{cases} \tag{5.11}$$

In Table 5.1, the DC terminal current is determined by the switching states and both node 'x' and 'y' currents. If switching pattern is occurring in state 1, $I_y(t)$ = 0A and $I_x(t)$ is expressed as:

$$I_x(t) = \begin{bmatrix} S_{a1} I_a(t) \operatorname{sgn}(M_a(t)) \\ +S_{b1} I_b(t) \operatorname{sgn}(M_b(t)) \\ +S_{c1} I_c(t) \operatorname{sgn}(M_c(t)) \end{bmatrix} \tag{5.12}$$

If switching pattern is occurring in state 3, $I_x(t)$ = 0A and $I_y(t)$ is formulated as:

$$I_y(t) = -\begin{bmatrix} S_{a4} I_a(t) \operatorname{sgn}(-M_a(t)) \\ +S_{b4} I_b(t) \operatorname{sgn}(-M_b(t)) \\ +S_{c4} I_c(t) \operatorname{sgn}(-M_c(t)) \end{bmatrix} \tag{5.13}$$

where sgn(.) function is defined as:

$$\operatorname{sgn}(M_s(t)) = \begin{cases} 1, & \text{if } M_s(t) \geq 0 \\ 0, & \text{otherwise} \end{cases} \tag{5.14}$$

Applying the same modulation analysis as stated in equation (5.2) to (5.7) into equation (5.12) and (5.13). One can obtain that; the DC current is changed by the modulation signal, which is shown in the following equation:

$$\begin{aligned} I_x(t) &= \begin{bmatrix} I_a(t)M_a(t)\mathrm{sgn}\left(M_a(t)\right) \\ +I_b(t)M_b(t)\mathrm{sgn}\left(M_b(t)\right) \\ +I_c(t)M_c(t)\mathrm{sgn}\left(M_c(t)\right) \end{bmatrix} \\ I_y(t) &= \begin{bmatrix} I_a(t)M_a(t)\mathrm{sgn}\left(-M_a(t)\right) \\ +I_b(t)M_b(t)\mathrm{sgn}\left(-M_b(t)\right) \\ +I_c(t)M_c(t)\mathrm{sgn}\left(-M_c(t)\right) \end{bmatrix} \end{aligned} \tag{5.15}$$

From equation (5.15), the neutral point clamped current is formulated by KCL and it is shown in the following expression. The neutral point clamped current consists of two current components, one is the three-phase current at the AC terminal $I_a(t) + I_b(t) + I_c(t)$ and another is harmonic dc injection current $fcn_a(t) + fcn_b(t) + fcn_c(t)$. The derivation of this neutral point current will be further elaborated in the following sections.

$$I_m(t) = I_a(t) + I_b(t) + I_c(t) - I_x(t) + I_y(t) \tag{5.16}$$

$$I_m(t) = \left[I_a(t) + I_b(t) + I_c(t)\right] - \left[fcn_a(t) + fcn_b(t) + fcn_c(t)\right] \tag{5.17}$$

where $I_a(t)$, $I_b(t)$ and $I_c(t)$ is the output current of a three-phase three-level diode-clamped inverter with the power factor angle of δ and $fcn_a(t)$, $fcn_b(t)$ and $fcn_c(t)$ are the dc current function with respect to three-phase AC terminal current and modulation index respectively. Both current equations are written as:

$$\begin{aligned} I_a(t) &= i\cos\left(\omega t + \theta_0 - \delta\right) \\ I_b(t) &= i\cos\left(\omega t + \theta_0 - \delta - \frac{2\pi}{3}\right) \\ I_c(t) &= i\cos\left(\omega t + \theta_0 - \delta - \frac{4\pi}{3}\right) \end{aligned} \tag{5.18}$$

$$\begin{aligned} fcn_a(t) &= I_a(t)M_a(t)\left[\mathrm{sgn}\left(M_a(t)\right) - \mathrm{sgn}\left(-M_a(t)\right)\right] \\ fcn_b(t) &= I_b(t)M_b(t)\left[\mathrm{sgn}\left(M_b(t)\right) - \mathrm{sgn}\left(-M_b(t)\right)\right] \\ fcn_c(t) &= I_c(t)M_c(t)\left[\mathrm{sgn}\left(M_c(t)\right) - \mathrm{sgn}\left(-M_c(t)\right)\right] \end{aligned} \tag{5.19}$$

where sgn(.) - sgn(-.) in one cycle is defined as:

$$\operatorname{sgn}(.)-\operatorname{sgn}(-.)=\begin{cases}-1, & -\pi \le t < -\dfrac{\pi}{2}\\ +1, & -\dfrac{\pi}{2} \le t \le \dfrac{\pi}{2}\\ -1, & \dfrac{\pi}{2} < t \le \pi\end{cases} \tag{5.20}$$

In equation (5.19), sgn(.) - sgn(-.) is extended into a simple Fourier Series as below:

$$\begin{cases}\operatorname{sgn}(M_a(t))-\operatorname{sgn}(-M_a(t))=\dfrac{1}{\pi}\displaystyle\sum_{n=1,2,3,\ldots}^{\infty}\left\{\int_{-\pi}^{\pi}\begin{bmatrix}\operatorname{sgn}(M_a(t))\\ -\operatorname{sgn}(-M_a(t))\end{bmatrix}\cos(nt)\,dt\right\}\cos\left[n(\omega t+\theta_0)\right]\\ \operatorname{sgn}(M_b(t))-\operatorname{sgn}(-M_b(t))=\dfrac{1}{\pi}\displaystyle\sum_{n=1,2,3,\ldots}^{\infty}\left\{\int_{-\pi}^{\pi}\begin{bmatrix}\operatorname{sgn}(M_b(t))\\ -\operatorname{sgn}(-M_b(t))\end{bmatrix}\cos(nt)\,dt\right\}\cos\left[n\left(\omega t+\theta_0-\dfrac{2\pi}{3}\right)\right]\\ \operatorname{sgn}(M_c(t))-\operatorname{sgn}(-M_c(t))=\dfrac{1}{\pi}\displaystyle\sum_{n=1,2,3,\ldots}^{\infty}\left\{\int_{-\pi}^{\pi}\begin{bmatrix}\operatorname{sgn}(M_c(t))\\ -\operatorname{sgn}(-M_c(t))\end{bmatrix}\cos(nt)\,dt\right\}\cos\left[n\left(\omega t+\theta_0-\dfrac{4\pi}{3}\right)\right]\end{cases}$$

$$\begin{cases}\operatorname{sgn}(M_a(t))-\operatorname{sgn}(-M_a(t))=\dfrac{4}{\pi}\displaystyle\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\cos\left(n(\omega t+\theta_0)\right)\sin\left(\frac{n\pi}{2}\right)\\ \operatorname{sgn}(M_b(t))-\operatorname{sgn}(-M_b(t))=\dfrac{4}{\pi}\displaystyle\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\cos\left(n\left(\omega t+\theta_0-\dfrac{2\pi}{3}\right)\right)\sin\left(\frac{n\pi}{2}\right)\\ \operatorname{sgn}(M_c(t))-\operatorname{sgn}(-M_c(t))=\dfrac{4}{\pi}\displaystyle\sum_{n=1,3,5,\ldots}^{\infty}\frac{1}{n}\cos\left(n\left(\omega t+\theta_0-\dfrac{4\pi}{3}\right)\right)\sin\left(\frac{n\pi}{2}\right)\end{cases}$$

(5.21)

Substituting equation (5.14) and (5.17) into equation (5.15), one can obtain

$$\mathrm{fcn_a}(t)=\frac{mi}{\pi}\left[\begin{array}{l}2\cos\delta\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0\right)\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n-2)\left(\omega t+\theta_0\right)+\delta\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n+2)\left(\omega t+\theta_0\right)-\delta\right)}{n}\end{array}\right]$$

$$\mathrm{fcn_b}(t)=\frac{mi}{\pi}\left[\begin{array}{l}2\cos\delta\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0-\frac{2\pi}{3}\right)\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n-2)\left(\omega t+\theta_0-\frac{2\pi}{3}\right)+\delta\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n+2)\left(\omega t+\theta_0-\frac{2\pi}{3}\right)-\delta\right)}{n}\end{array}\right] \quad (5.22)$$

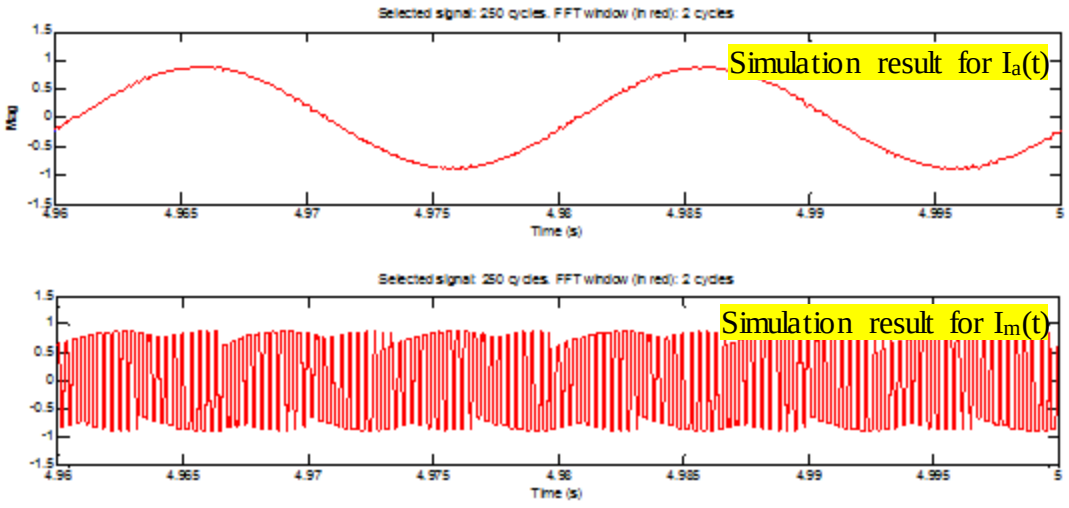
$$\mathrm{fcn_c}(t)=\frac{mi}{\pi}\left[\begin{array}{l}2\cos\delta\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0-\frac{4\pi}{3}\right)\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n-2)\left(\omega t+\theta_0-\frac{4\pi}{3}\right)+\delta\right)}{n}\\+\sum\limits_{n=1,3,5,\ldots}^{\infty}\dfrac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n+2)\left(\omega t+\theta_0-\frac{4\pi}{3}\right)-\delta\right)}{n}\end{array}\right]$$

If the AC terminal of the inverter is under balanced condition, then the first term of the neutral point current equation as stated in equation (5.17) is neglected and the neutral point clamped current is equal to the second component current as stated in the following equation.

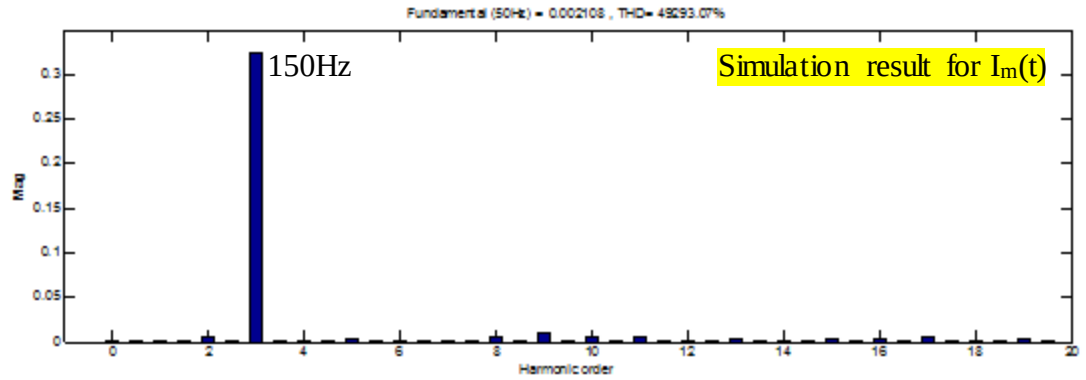
$$I_m(t) = -\left[fcn_a(t) + fcn_b(t) + fcn_c(t)\right] \tag{5.23}$$

Substituting equation (5.21) into (5.23), the neutral point current is obtained in equation (5.24). As a result, three-level diode-clamped inverter will experience triplen harmonic currents and zero DC components in the neutral point clamped as shown in Fig. 5.4 and 5.5. Hence, to obtain a balanced dc voltage across the DC capacitors, the DC components at the node of two series connected DC capacitor must be zero.

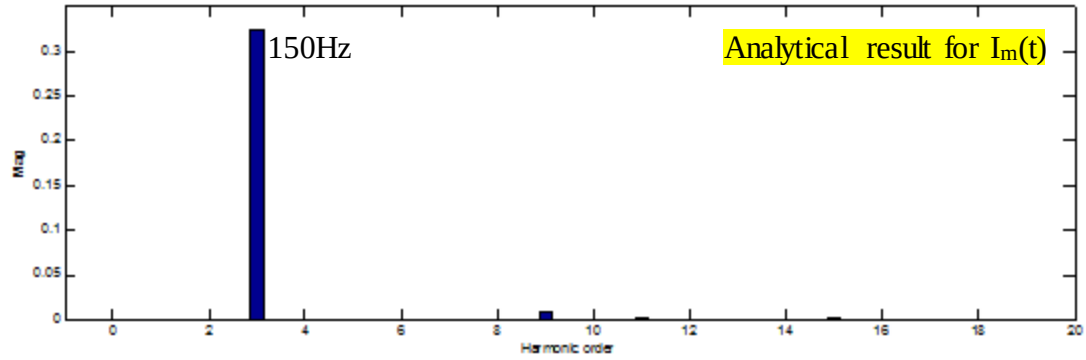
$$I_m(t) = -\frac{3mi}{\pi}\left[\begin{array}{l} 2\cos\delta \sum_{n=3,9,15,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0\right)\right)}{n} \\ -\sum_{n=3,9,15,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0\right)+\delta\right)}{n+2} \\ -\sum_{n=3,9,15,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t+\theta_0\right)-\delta\right)}{n-2} \end{array}\right] \tag{5.24}$$



(a)

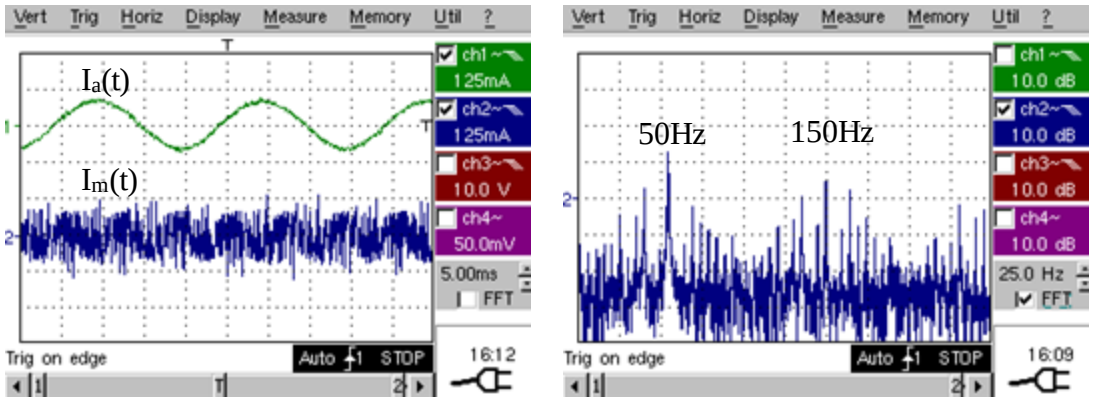


(b)



(c)

Fig. 5.4 Simulation results based on neutral point clamped current.



(a) (b)

Fig. 5.5 Experimental results based on neutral point clamped current.

Based on equation (5.24), the high harmonic current is dominated with the third order harmonics. This is expressed in a simplify equation based on trigonometric properties expressed in the following equation.

$$I_m(t) \approx \frac{12mi}{5\pi}\left[-\frac{2}{3}\cos(\delta)\cos\left(3(\omega t+\theta_0)\right)-\sin(\delta)\sin\left(3(\omega t+\theta_0)\right)\right] \quad (5.25)$$

From the above equation (5.25), the neutral point current is depended on the load angle which is also known as power factor angle (δ). Hence, neutral point clamped current is regulated within $0 \le \delta \le 90^{\circ}$ and this is presented as:

$$[0.5093mi]\cos(3\omega t+3\theta_0-\pi) \le I_m(t) \le [0.7639mi]\sin(3\omega t+3\theta_0-\pi) \quad (5.26)$$

The mathematical expression of I_m in Equation (5.26) is defined to determine the maximum current required for designing the PCB trace current capacity.

5.2 Three-Level Flying-Capacitor Inverter Topology

A three-phase three-level flying-capacitor inverter is shown in Fig. 5.6 and this type of topology usually requires 12 identical IGBT devices and minimum of 4 DC capacitors to generate a three-level output voltages. The switching strategy for this capacitor-clamped inverter is similar to the three-level diode-clamped inverter as presented in section 2.1 and switching states for upper leg and lower leg per phase is depicted in Table 5.2. To generate all gating signals for safety operation, switching devices in per-phase leg is expressed in the following equation.

$$\begin{cases} S_{a1}+S_{a4}=1 \\ S_{a2}+S_{a3}=1 \end{cases} \quad (5.27)$$

The output phase voltage of a three-level flying capacitor inverter is expressed in term of the switching functions, similar to section 5.1. Since both topologies employ LSPWM technique, the output voltage expression of the flying capacitor is the same as a diode-clamped inverter and it is:

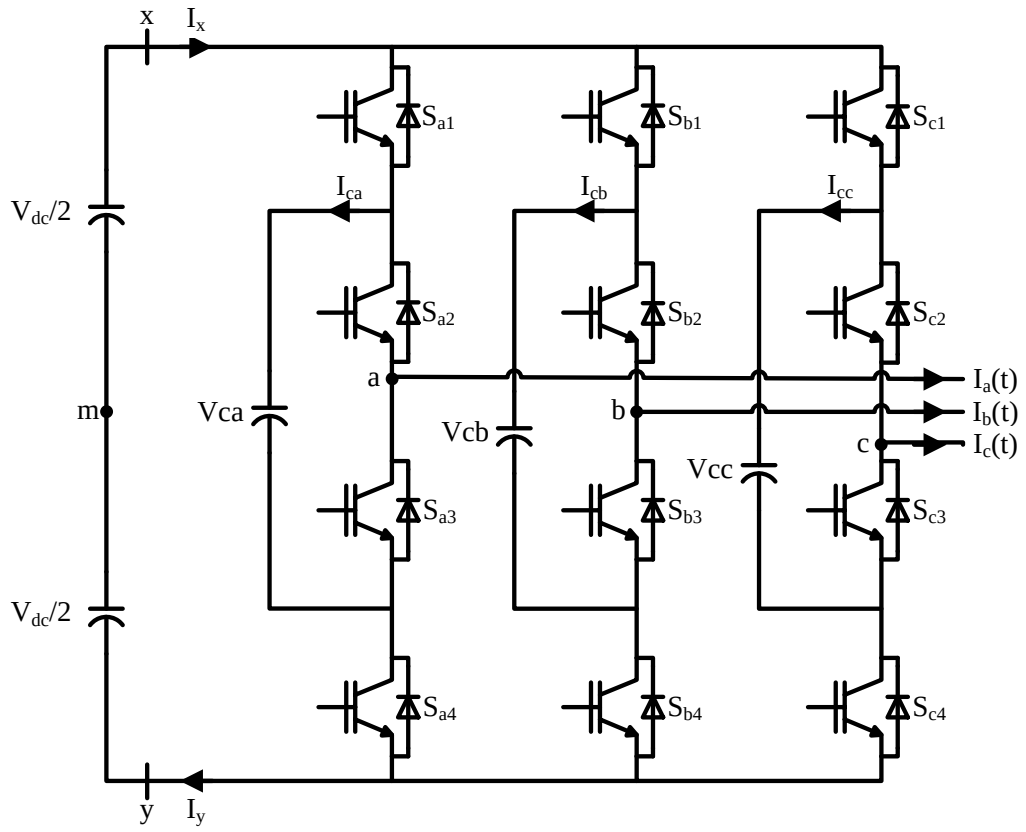


Fig. 5.6 Three-level flying-capacitor inverter circuit.

TABLE 5.2

THREE-LEVEL FLYING CAPACITOR INVERTER CORRESPONDING SWITCHING STATES

State	**Switching States**				**Per-Phase Leg Voltage**		
	S_{s1}	**S_{s2}**	**S_{s3}**	**S_{s4}**	**V_{sx}**	**V_{sy}**	**V_{sm}**
1	1	1	0	0	0	V_{dc}	$V_{dc}/2$
2	0	1	0	1	$-V_{dc}/2$	$V_{dc}/2$	0
3	0	0	1	1	$-V_{dc}$	0	$-V_{dc}/2$

Where s represent phase a, b and c and S_{s1} to S_{s4} are presented as the IGBT switching devices for individual leg. Logic 1 represent as turn on and logic 0 represent as turn off for S_{s1}, S_{s2}, S_{s3} and S_{s4}.

$$\begin{cases} V_{sx}(t) = V_{xm}\left[S_{s1}(t)+S_{s2}(t)\right] - V_{dc}(t) = \dfrac{V_{dc}(t)}{2}\left[S_{s1}(t)+S_{s2}(t)\right] - V_{dc}(t) \\ V_{sy}(t) = V_{ym}\left[S_{s3}(t)+S_{s4}(t)\right] + V_{dc}(t) = -\dfrac{V_{dc}(t)}{2}\left[S_{s3}(t)+S_{s4}(t)\right] + V_{dc}(t) \\ V_{sm}(t) = \dfrac{V_{sx}(t)+V_{sy}(t)}{2} = \dfrac{V_{xm}}{2}\left[S_{s1}(t)+S_{s2}(t)\right] + \dfrac{V_{ym}}{2}\left[S_{s3}(t)+S_{s4}(t)\right] \\ \qquad = \dfrac{V_{dc}(t)}{4}\left\{\left[S_{s1}(t)+S_{s2}(t)\right] - \left[S_{s3}(t)+S_{s4}(t)\right]\right\} \end{cases}$$

(5.28)

Based on the switching states given in Table 5.2, the instantaneous upper and lower dc current are solely dependent on switching functions of that particular switch. For a stable and balanced floating capacitor voltage, the instantaneous dc current for upper and lower terminal ($I_x(t)$ and $I_y(t)$) must flow complementing each other.(for i.e. $I_x(t)$ = const, $I_y(t)$ = 0 and $I_x(t)$ = 0, $I_y(t)$ = const). Thus, dc link current is known as:

$$\begin{cases} I_x(t) = \begin{bmatrix} S_{a1}I_a(t)\,\mathrm{sgn}\left(M_a(t)\right) \\ +S_{b1}I_b(t)\,\mathrm{sgn}\left(M_b(t)\right) \\ +S_{c1}I_c(t)\,\mathrm{sgn}\left(M_c(t)\right) \end{bmatrix} \\ I_y(t) = \begin{bmatrix} S_{a3}I_a(t)\,\mathrm{sgn}\left(-M_a(t)\right) \\ +S_{b3}I_b(t)\,\mathrm{sgn}\left(-M_b(t)\right) \\ +S_{c3}I_c(t)\,\mathrm{sgn}\left(-M_c(t)\right) \end{bmatrix} \end{cases} \tag{5.29}$$

The inner capacitor current of phase a, b and c ($I_{ca}(t)$, $I_{cb}(t)$ and $I_{cc}(t)$) of a three-level capacitor clamped inverter is defined by the current division law and superposition theorem. Fig. 5.7 shows the equivalent circuit for the derivation of the inner capacitor current of phase a.

From Fig. 5.7, the inner capacitor current is found to be

$$\begin{cases} I_{ca}(t) = I_{ca1}(t) + I_{ca2}(t) \\ I_{cb}(t) = I_{cb1}(t) + I_{cb2}(t) \\ I_{cc}(t) = I_{cc1}(t) + I_{cc2}(t) \end{cases} \tag{5.30}$$

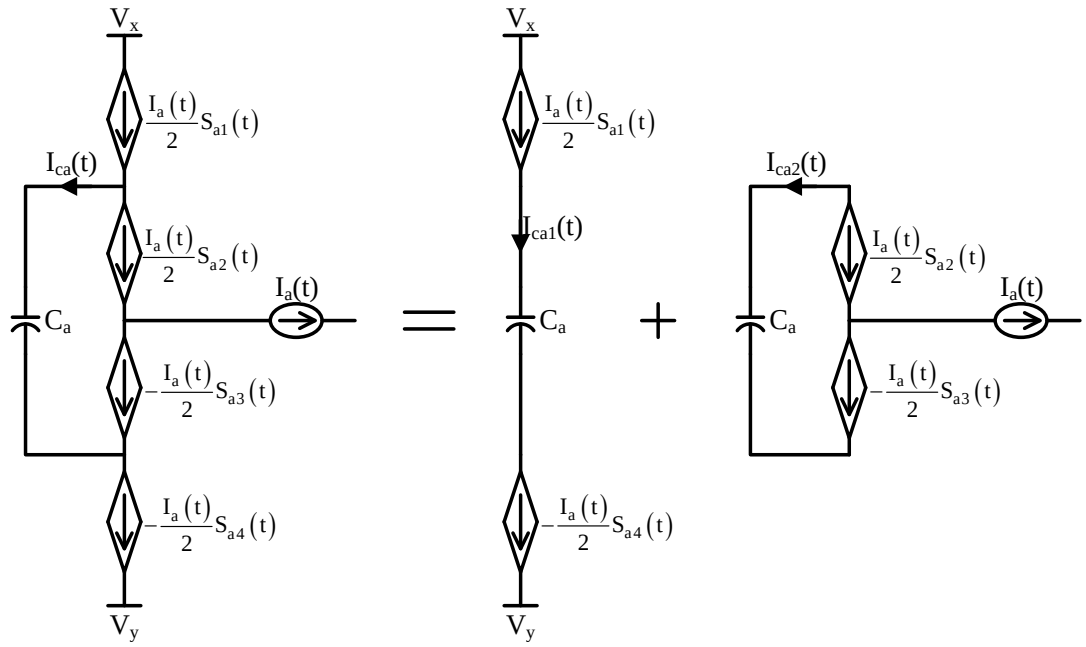


Fig. 5.7 Equivalent circuit of phase 'a' three-level flying capacitor inverter with derivation of inner capacitor current of phase 'a'.

Rearranging equation (5.30) in terms of switching function we get:

$$\begin{cases} I_{ca}(t) = \dfrac{I_a(t)}{2}\left[S_{a1}(t) - S_{a2}(t) + S_{a3}(t) - S_{a4}(t)\right] \\ \qquad = I_a(t)\left[-1 + S_{a1}(t)\,\mathrm{sgn}\left(M_a(t)\right) + S_{a3}(t)\,\mathrm{sgn}\left(-M_a(t)\right)\right] \\ I_{cb}(t) = \dfrac{I_b(t)}{2}\left[S_{b1}(t) - S_{b2}(t) + S_{b3}(t) - S_{b4}(t)\right] \\ \qquad = I_b(t)\left[-1 + S_{b1}(t)\,\mathrm{sgn}\left(M_b(t)\right) + S_{b3}(t)\,\mathrm{sgn}\left(-M_b(t)\right)\right] \\ I_{cc}(t) = \dfrac{I_c(t)}{2}\left[S_{c1}(t) - S_{c2}(t) + S_{c3}(t) - S_{c4}(t)\right] \\ \qquad = I_c(t)\left[-1 + S_{c1}(t)\,\mathrm{sgn}\left(M_c(t)\right) + S_{c3}(t)\,\mathrm{sgn}\left(-M_c(t)\right)\right] \end{cases} \tag{5.31}$$

Simplifying equation (5.31),

$$\begin{cases} I_{ca}(t) = I_a(t)\left\{-1 + M_a(t)\left[\operatorname{sgn}\left(M_a(t)\right) - \operatorname{sgn}\left(-M_a(t)\right)\right]\right\} \\ I_{cb}(t) = I_b(t)\left\{-1 + M_b(t)\left[\operatorname{sgn}\left(M_b(t)\right) - \operatorname{sgn}\left(-M_b(t)\right)\right]\right\} \\ I_{cc}(t) = I_c(t)\left\{-1 + M_c(t)\left[\operatorname{sgn}\left(M_c(t)\right) - \operatorname{sgn}\left(-M_c(t)\right)\right]\right\} \end{cases}$$

$$\begin{cases} I_{ca}(t) = -I_a(t) + fcn_a(t) \\ I_{cb}(t) = -I_b(t) + fcn_b(t) \\ I_{cc}(t) = -I_c(t) + fcn_c(t) \end{cases} \tag{5.32}$$

Functions $fcn_a(t)$, $fcn_b(t)$ and $fcn_c(t)$ are same as discussed in equation (5.18). Hence, the equation (5.32) can be extended to a compact Fourier series form. This is expressed as the following equation.

$$I_{ca}(t) = -i\cos\left(\omega t + \theta_0 - \delta\right) + \frac{mi}{\pi}\left[\begin{array}{l} 2\cos\delta \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t + \theta_0\right)\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(\left(n-2\right)\left(\omega t + \theta_0\right) + \delta\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(\left(n+2\right)\left(\omega t + \theta_0\right) - \delta\right)}{n} \end{array}\right]$$

$$I_{cb}(t) = -i\cos\left(\omega t + \theta_0 - \frac{2\pi}{3} - \delta\right) + \frac{mi}{\pi}\left[\begin{array}{l} 2\cos\delta \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t + \theta_0 - \frac{2\pi}{3}\right)\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(\left(n-2\right)\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) + \delta\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(\left(n+2\right)\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) - \delta\right)}{n} \end{array}\right]$$

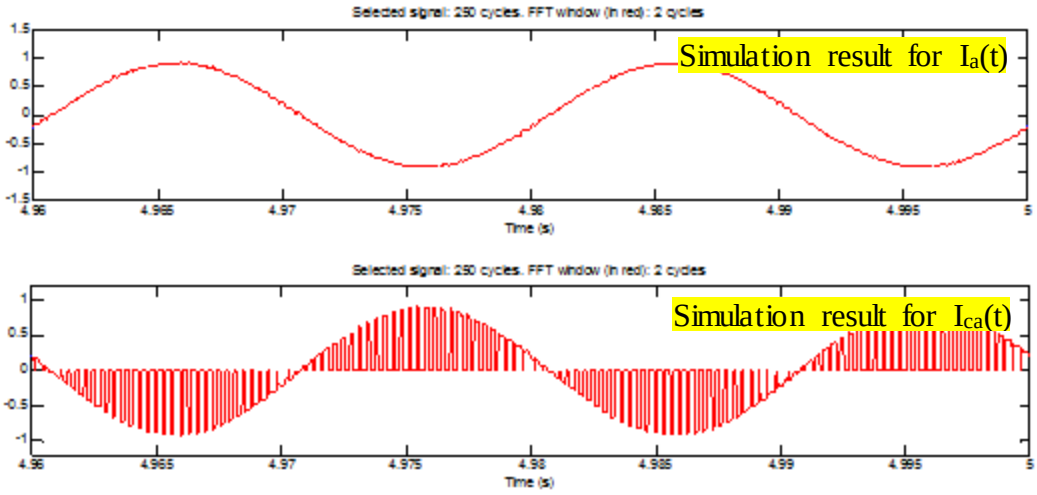
$$I_{cc}(t) = -i\cos\left(\omega t + \theta_0 - \frac{4\pi}{3} - \delta\right) + \frac{mi}{\pi}\left[\begin{array}{l} 2\cos\delta \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left(n\left(\omega t + \theta_0 - \frac{4\pi}{3}\right)\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n-2)\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) + \delta\right)}{n} \\ + \sum_{n=1,3,5,\ldots}^{\infty} \frac{\sin\left(\frac{n\pi}{2}\right)\cos\left((n+2)\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) - \delta\right)}{n} \end{array}\right] \quad (5.33)$$

Equation (5.33) shows a general expression for the inner capacitor current pertaining to each phase of the three-level flying capacitor inverter. Based on equation (5.33), inner capacitor current consists of fundamental and odd harmonic components. To simplify the equation, the inner capacitor current is determined by the dominant current component which is shown in Fig. 5.8 and 5.9. Therefore, the inner current is written as:

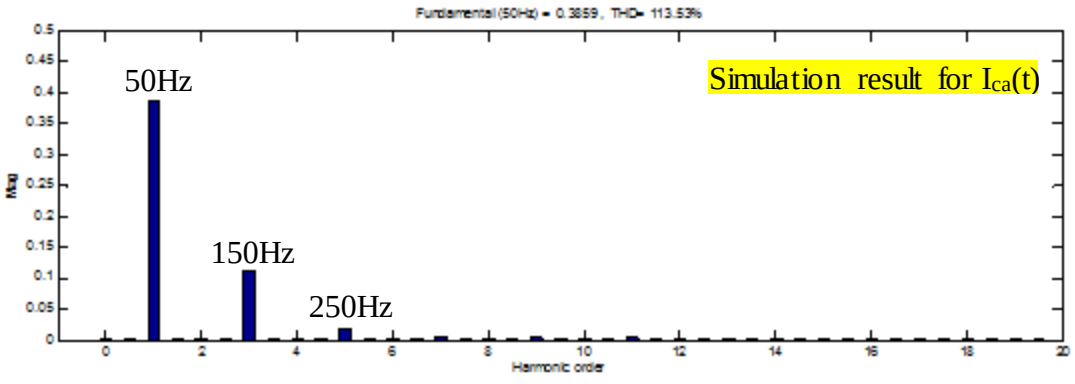
$$I_{ca}(t) \approx -i\cos(\omega t + \theta_0 - \delta) + \frac{mi}{\pi}\left[\begin{array}{l} 2\cos(\omega t + \theta_0 - \delta) \\ + \frac{2}{3}\cos(\omega t + \theta_0 + \delta) \\ + \frac{2}{3}\cos\left[3(\omega t + \theta_0) - \delta\right] \\ - \frac{1}{3}\cos\left[3(\omega t + \theta_0) + \delta\right] \end{array}\right]$$

$$I_{cb}(t) \approx -i\cos\left(\omega t + \theta_0 - \frac{2\pi}{3} - \delta\right) + \frac{mi}{\pi}\left[\begin{array}{l} 2\cos\left(\omega t + \theta_0 - \frac{2\pi}{3} - \delta\right) \\ + \frac{2}{3}\cos\left(\omega t + \theta_0 - \frac{2\pi}{3} + \delta\right) \\ + \frac{2}{3}\cos\left[3\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) - \delta\right] \\ - \frac{1}{3}\cos\left[3\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) + \delta\right] \end{array}\right] \quad (5.34)$$

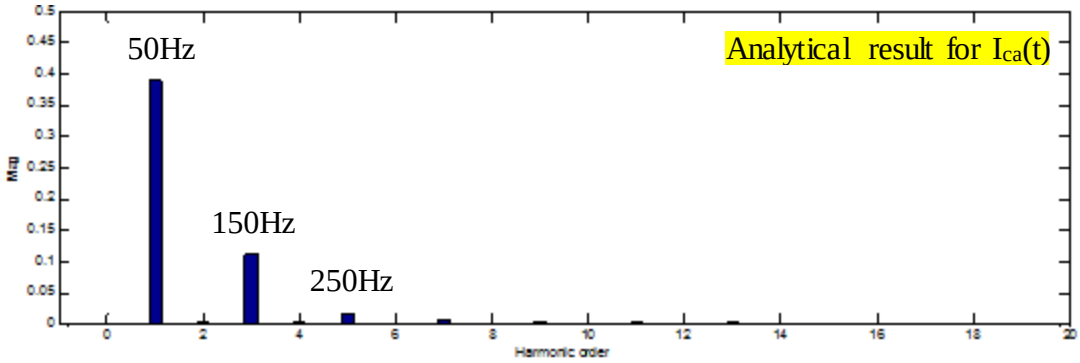
$$I_{cc}(t) \approx -i\cos\left(\omega t+\theta_0-\frac{4\pi}{3}-\delta\right)+\frac{mi}{\pi}\left[\begin{array}{l}2\cos\left(\omega t+\theta_0-\frac{4\pi}{3}-\delta\right)\\+\frac{2}{3}\cos\left(\omega t+\theta_0-\frac{4\pi}{3}+\delta\right)\\+\frac{2}{3}\cos\left[3\left(\omega t+\theta_0-\frac{4\pi}{3}\right)-\delta\right]\\-\frac{1}{3}\cos\left[3\left(\omega t+\theta_0-\frac{4\pi}{3}\right)+\delta\right]\end{array}\right]$$



(a)

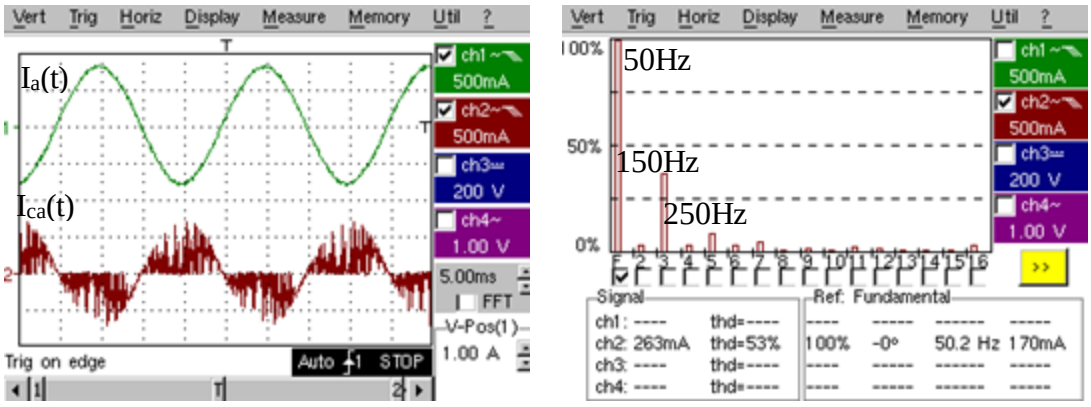


(b)



(c)

Fig. 5.8 Simulated results based on inner capacitor current



(a) (b)

Fig. 5.9 Experimental results for load current and inner capacitor current.

5.3 Discussion

The current expressions derived based on the switching function for the three-level inverters are presented in this chapter. The derived switching function of the LS-PWM is verified with the relationship between the pole voltage and the modulation. After expanding the pole voltage expressions, the final mathematical expression of the modulation is expressed as $2V_{am}/V_{dc}$. In conclusion, the modulation index for any voltage level power converters is similar to the two-level inverter as long as the inverter is operated under voltage-source inverter (VSI) operation.

Besides that, the amplitude of the low frequency harmonic order of the diode-clamped and flying capacitor is also expressed by expanding the switching function. Analytical

results based on the calculation method are verified through the experimental and simulation results. According to the obtained results, the Fourier Series analysis only provides correct amplitude for low harmonic order. To achieve the exact solution of the amplitude for the remaining high frequency components, Double Fourier Series analysis can be adopted in the future work. However, the method of achieving the switching function expression is sufficient for the other mathematical analysis such as power losses analysis and stresses analysis of the semiconductor devices.

Chapter 6 – DC Voltage Balancing Strategies for Three-Level Inverter Topologies

This chapter investigates the different voltage balancing schemes for dc-link capacitors in three-level inverters. The major unbalanced voltage condition across the DC capacitors is caused as the series connected diodes are clamped to the neutral point of the two series connected capacitors. This gives rise to unequal flow of charging and discharging currents in DC capacitors. Besides, in practical environment active/passive elements also contribute to the unbalanced condition due to the existence of unequal parameters. This introduces a dc component in the output voltage spectrum. This high amplitude dc component is carried through the load terminal and results in excessive heating [86].

6.1 Proposed DC Voltage Balancing Method

Voltage balancing with RLC elements for single-phase full bridge three-level diode-clamped inverter has been proposed by Robert Stala [85] and analytical study based on LC filter for three-phase three-level diode-clamped inverter has been discussed by Toit Mouton [87]. However, the balancing method in [87] is required to connect the common virtual ground in between LC filter and resistive load, which does not practically solve for resistive-inductive load (RL load) application and without any common connected virtual ground. In most of the cases, practical RL loads usually occur in the AC bus, which is known as electrical drives. Furthermore, the analysis of the RLC elements for the natural balancing properties proposed by Robert Stala does not discuss in detail. Hence, this sub-section will introduce the dc voltage balancing method in terms of both the control and passive filter (RC) balancing method.

Two types of dc voltage balancing methods will be discussed in the following sub-section. The first proposed method is known as reduction of dc components with an offset modulating control signals. This type of control strategy requires additional two voltage sensors for the input dc voltage measurement. The dc components of the

modulation function are obtained by the equation (6.6). The second balancing method is based on the RC filter, which is also known as first order low pass filter. This type of balancing method is solely depends on the natural reduction of the dc components. The dc components of the three-phase voltage are injected through the RC star-connected filter, which provides a balanced dc voltage for each capacitor and rejects the high frequency current components from entering the load terminal.

6.1.1 DC Components Offset for Modulation Control Signals

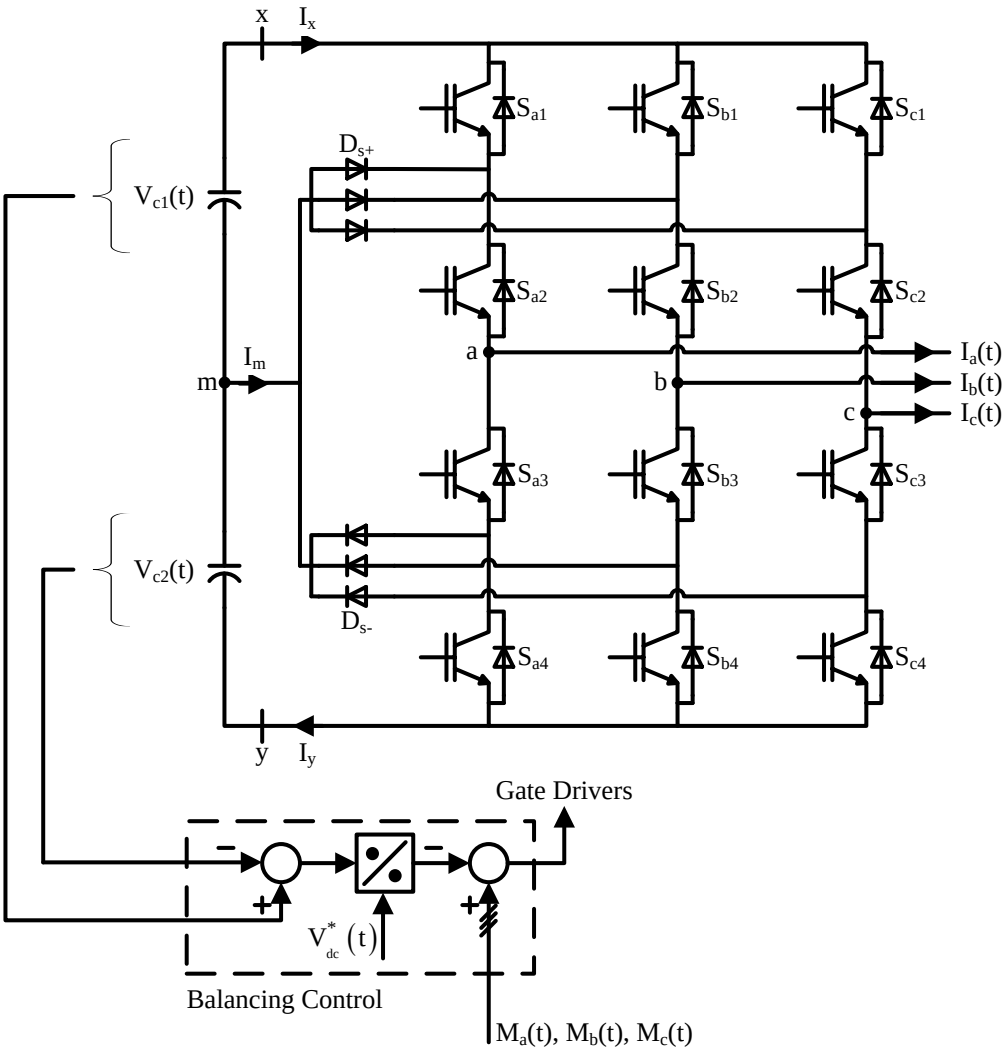


Fig. 6.1 Three-phase three-level diode-clamped inverter with dc voltage balancing control without RC filter.

Based on Fig. 6.1, the pole voltage across phase (a, b and c) and center point 'm' will experience an additional dc component $V_o(t)$ and high frequency components are created by the switching devices. Thus, the pole voltages of the three-phase three-level diode-clamped inverter are expressed as:

$$\begin{cases} V_a(t) = V_{am}(t) + V_o(t) \\ V_b(t) = V_{bm}(t) + V_o(t) \\ V_c(t) = V_{cm}(t) + V_o(t) \end{cases} \tag{6.1}$$

If the dc link capacitor voltages are not equal ($V_{c1}(t) \neq V_{c2}(t)$) due to tolerance value of capacitance, then the three-phase pole voltages are shown as:

$$\begin{cases} V_{am}(t) = \dfrac{V_{c1}(t)}{2}\left[S_{a1}(t) + S_{a2}(t)\right] - \dfrac{V_{c2}(t)}{2}\left[2 - S_{a1}(t) - S_{a2}(t)\right] \\ V_{bm}(t) = \dfrac{V_{c1}(t)}{2}\left[S_{b1}(t) + S_{b2}(t)\right] - \dfrac{V_{c2}(t)}{2}\left[2 - S_{b1}(t) - S_{b2}(t)\right] \\ V_{cm}(t) = \dfrac{V_{c1}(t)}{2}\left[S_{c1}(t) + S_{c2}(t)\right] - \dfrac{V_{c2}(t)}{2}\left[2 - S_{c1}(t) - S_{c2}(t)\right] \end{cases} \tag{6.2}$$

By replacing switching function by modulation function, the phase voltages are illustrated as linear modulation function below.

$$\begin{cases} V_{am}(t) \approx \dfrac{V_{c1}(t)}{2}\left[M_a(t) + 1\right] - \dfrac{V_{c2}(t)}{2}\left[1 - M_a(t)\right] \\ V_{bm}(t) \approx \dfrac{V_{c1}(t)}{2}\left[M_b(t) + 1\right] - \dfrac{V_{c2}(t)}{2}\left[1 - M_b(t)\right] \\ V_{cm}(t) \approx \dfrac{V_{c1}(t)}{2}\left[M_c(t) + 1\right] - \dfrac{V_{c2}(t)}{2}\left[1 - M_c(t)\right] \end{cases} \tag{6.3}$$

Equation (6.3) is derived from the following properties with the linear modulation function under steady-state condition based on equation (5.4) and (5.7).

$$S_{x1}(t) + S_{x2}(t) = S_{x1}(t)\,\mathrm{sgn}\left(M_x(t)\right) - S_{x4}(t)\,\mathrm{sgn}\left(-M_x(t)\right) + 1 \tag{6.4}$$

Then,

$$\begin{aligned} & S_{x1}(t)\,\mathrm{sgn}\left(M_x(t)\right) - S_{x4}(t)\,\mathrm{sgn}\left(-M_x(t)\right) + 1 \\ & \approx M_x(t)\,\mathrm{sgn}\left(M_x(t)\right) + M_x(t)\,\mathrm{sgn}\left(-M_x(t)\right) + 1 \end{aligned} \tag{6.5}$$

using $\mathrm{sgn}(M_x(t))+\mathrm{sgn}(-M_x(t)) = 1$, the updated three-phase modulation signal is shown in the following.

$$\begin{cases} M_a^*(t) = 2\dfrac{V_{am}(t)}{V_{dc}(t)} - \dfrac{V_{c1}(t) - V_{c2}(t)}{V_{dc}(t)} = M_a(t) - M_0(t) \\ M_b^*(t) = 2\dfrac{V_{bm}(t)}{V_{dc}(t)} - \dfrac{V_{c1}(t) - V_{c2}(t)}{V_{dc}(t)} = M_b(t) - M_0(t) \\ M_c^*(t) = 2\dfrac{V_{cm}(t)}{V_{dc}(t)} - \dfrac{V_{c1}(t) - V_{c2}(t)}{V_{dc}(t)} = M_c(t) - M_0(t) \end{cases} \tag{6.6}$$

6.1.2 Measurement Results for DC Offset Modulation Control

The simulated results shown in Fig. 6.2 and 6.3 are used to evaluate the dc voltage balancing with and without adding the dc offset voltage value while considering various dc capacitor parameters. Fig. 6.2 shows the simulated results of the dc voltage across each of the capacitor C1 and C2, and both of the capacitor voltages are balanced at 0.5 second with the proposed balancing control as given in Fig. 6.1. The unbalanced state of the dc voltage without the balancing control is shown in Fig. 6.2. All the results are based on parameters C1 = 1050 µF, R_{ESR1} = 120mΩ and C2 = 950 µF, R_{ESR2} = 105mΩ.

The nominal capacitance value of 1000 µF with a tolerance value of ±20% in Fig. 6.3 shows an extreme unbalanced dc capacitor voltage. Such an unbalanced scheme will tend to inject dc components of higher value into the ac load as compared to the case shown in Fig. 6.2.

To evaluate the performance of the balancing control, experimental results are shown in Fig. 6.4 (ref. to page 77). Both dc capacitors of 1000µF value are selected for the laboratory prototype. Fig. 6.4(c) shows the voltage across each capacitor in the dc bus

is unbalanced without any balancing properties. With the proposed balancing control, the dc voltage across each capacitor is balanced as shown in Figs. 6.4(a) and (b). To achieve a balanced dc voltage bus the controller is required to track the voltage error precisely. This requires an accurate measurement from the voltage sensors. Such accuracy voltage sensor is tuned by the gain of the analog amplifier circuit.

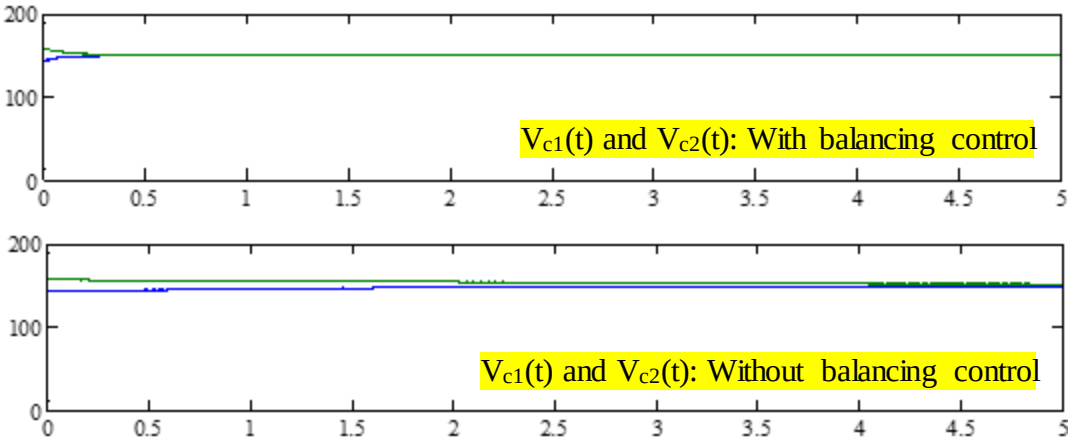


Fig. 6.2 Simulation results with the parameter of C1= 1050µF, C2 = 950µF, R_{ESR} = 120mΩ and R_{ESR} = 105mΩ of the dc voltage across each capacitor $V_{c1}(t)$ and $V_{c2}(t)$.

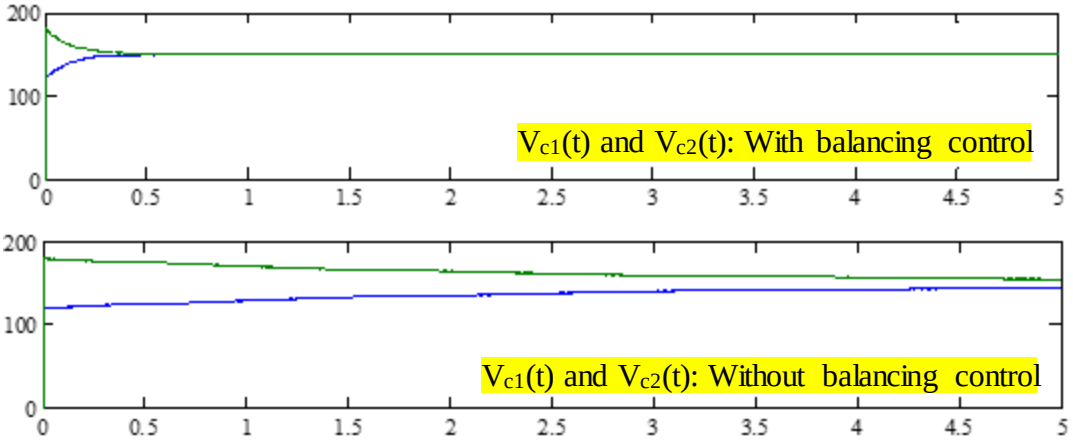


Fig. 6.3 Simulation results with the parameter of C1= 1200µF, C2 = 800µF, R_{ESR} = 110mΩ and R_{ESR} = 88mΩ of the dc voltage across each capacitor $V_{c1}(t)$ and $V_{c2}(t)$.

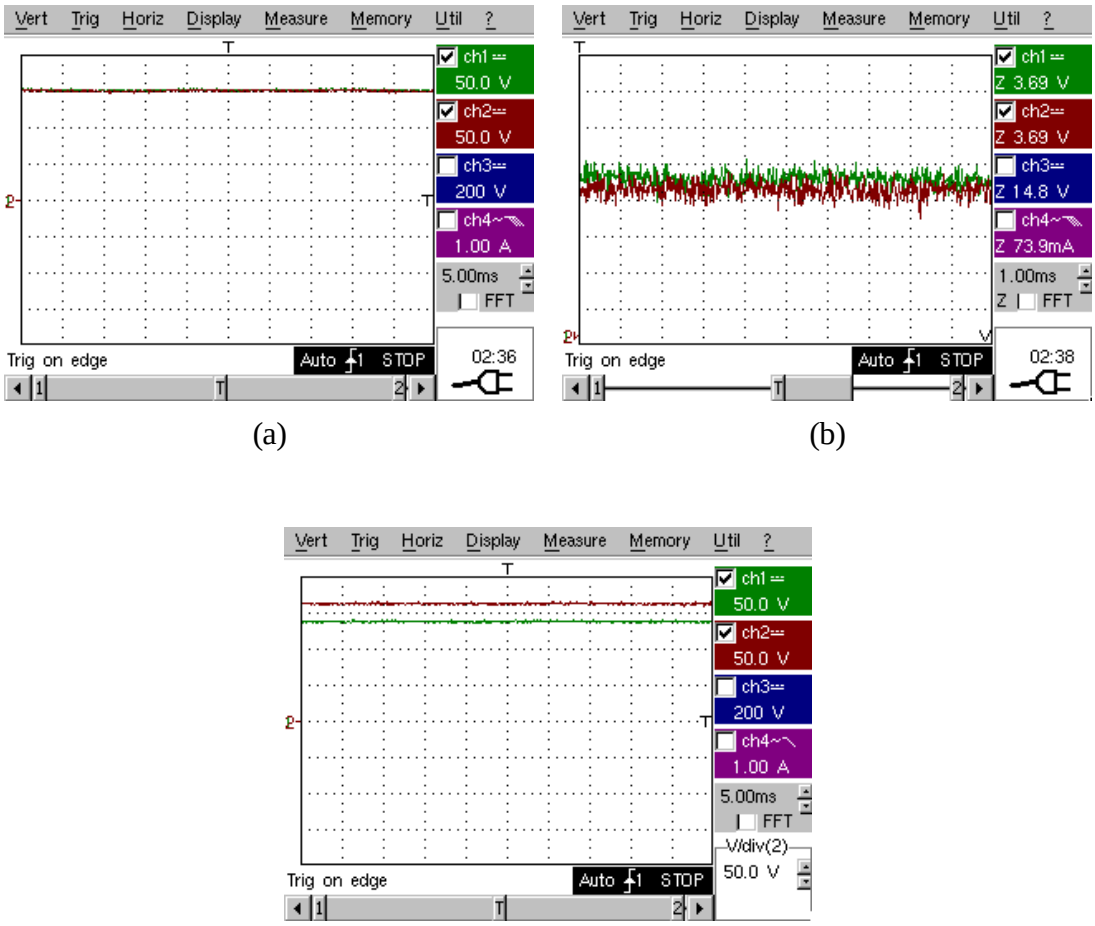


Fig. 6.4 Experimental results with the specification of C1 ≈ C2 ≈ ±1.2 × 1000μF and $R_{ESR1} \approx R_{ESR2} \approx 110m\Omega$ of the dc capacitor voltages of Vc1(t) and Vc2(t). (a) With balancing modulation control, (b) Zoom in of Fig. 6.4(a), and (c) Without balancing modulation control.

The neutral-point-clamped current waveform shown in Figs. 6.5 (simulated results) and 6.6 (experimental results) are almost same as Fig. 5.4. One can notice that the dc voltage for each of the capacitor is not affected by the high frequency harmonic component and third-order harmonic component. With the proposed balancing control, a third harmonic current component will pass through the neutral-point-clamped without any dc current component into the ac load during the switching state 2 as presented in Table 5.1.

The simulated and experimental results of the pole voltage (phase 'a') are illustrated in Figs. 6.7(a) and 6.8(a) respectively. The harmonic spectrum of phase 'a' voltage in Fig. 6.7(a) shows that no dc component has been injected into ac load terminal. The simulated and experimental results of output load current waveform and its harmonic order are shown in Figs. 6.7(b) and 6.8(b) respectively.

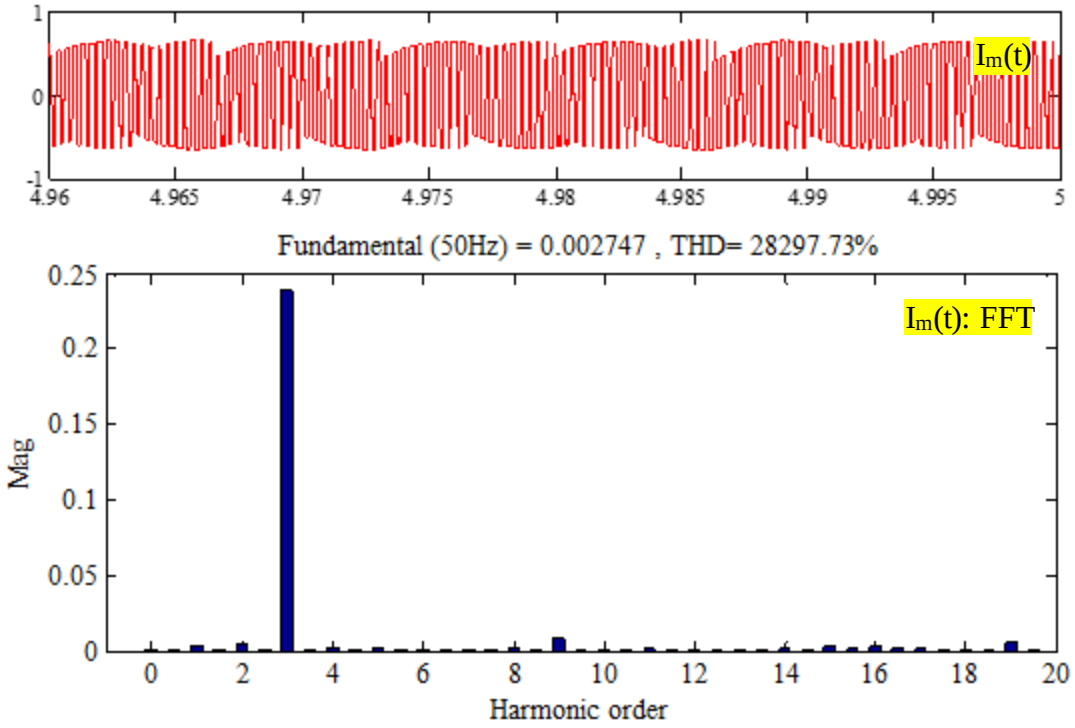
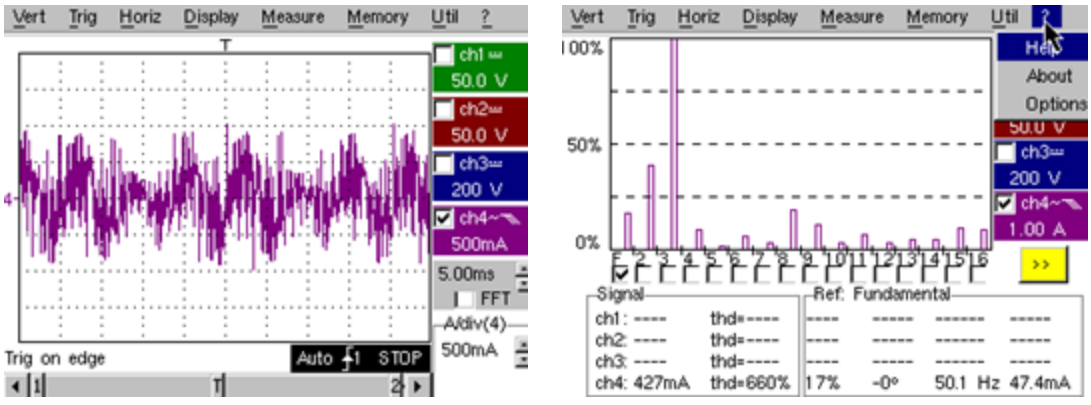
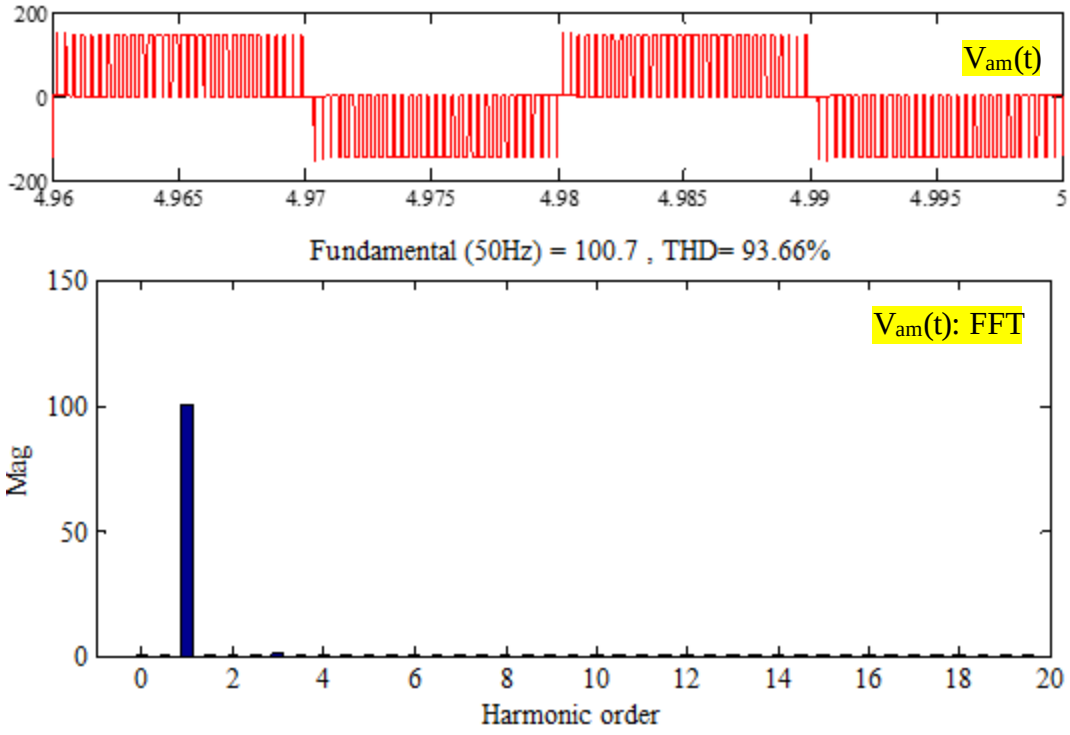


Fig. 6.5 Simulation results with the neutral-point-clamped current waveform and FFT analyzer of the two series connected dc capacitor.

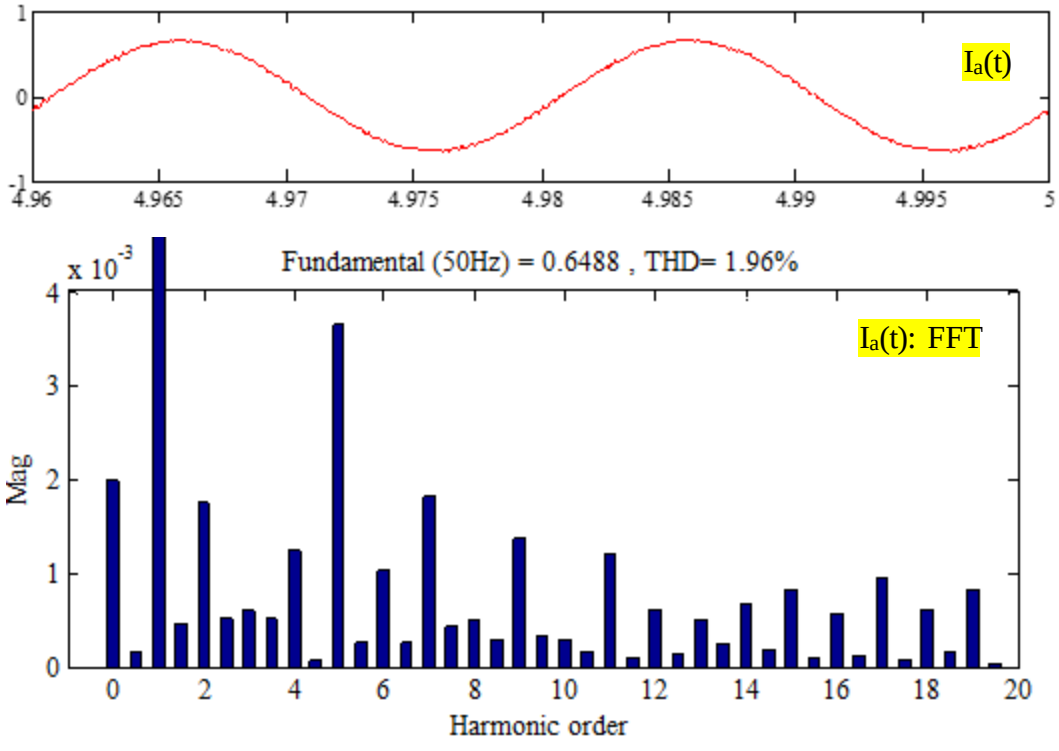


(a) (b)

Fig. 6.6 Experimental results with the neutral-point-clamped current waveform and FFT analyzer of the two series connected dc capacitor. (a) Neutral-point-clamped current waveform, and (b) FFT of the neutral-point-clamped current.



(a)



(b)

Fig. 6.7 Simulation results with the output voltage and current of a three-phase three-level diode-clamped inverter with the voltage balancing controller. (a) Voltage waveform (top figure) and respective FFT (bottom figure), and (b) Current waveform (top figure) and respective FFT (bottom figure).

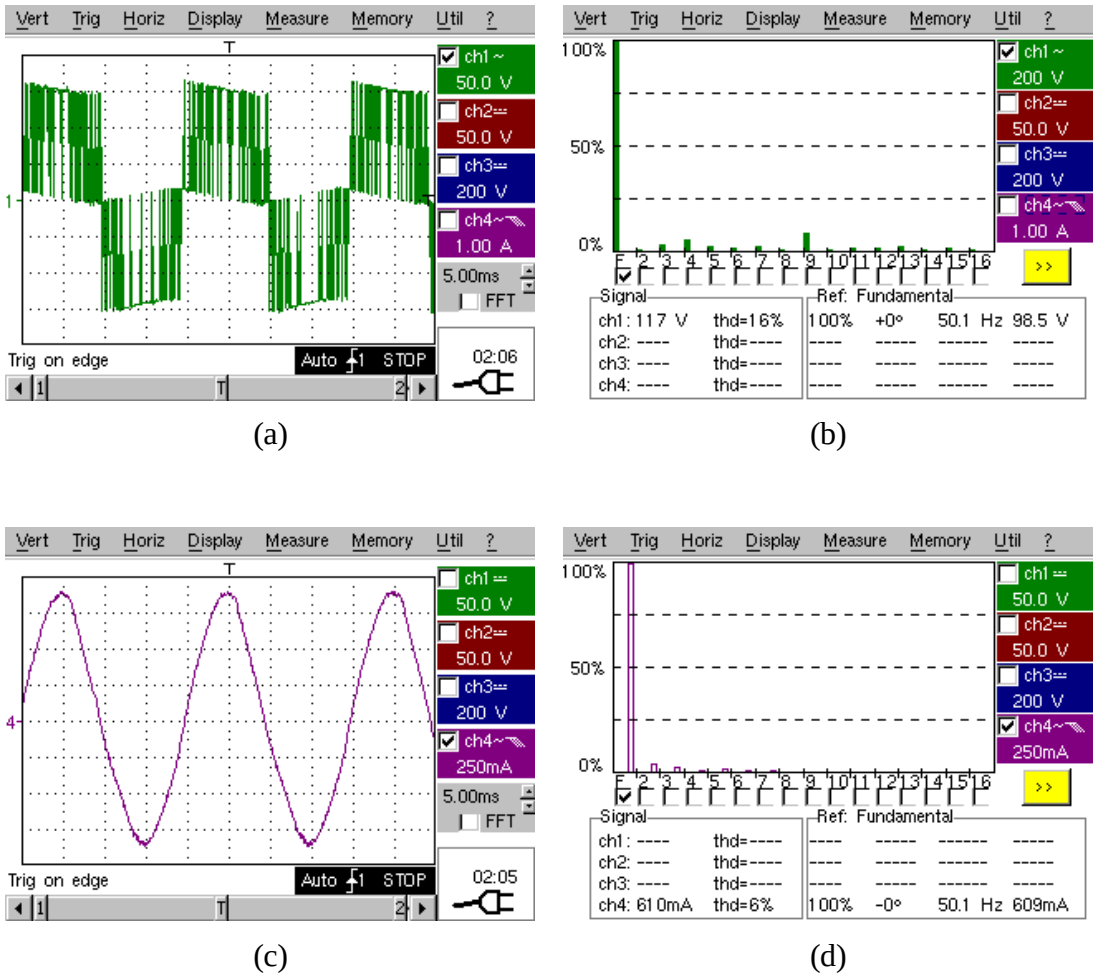


Fig. 6.8 Experimental results with the output voltage and current of a three-phase three-level diode-clamped inverter with the voltage balancing controller. (a) Phase or pole voltage waveform, (b) FFT of the Fig. 6.8(a), (c) Output load current waveform (R = 150Ω and L = 122mH), and (d) FFT of Fig. 6.8(c).

6.1.3 Natural Balancing Star-Connected RC Filter Circuit

Fig. 6.10 shows the natural balancing technique for DC capacitor voltage with star-connected passive element for three-phase three-level diode-clamped inverter. In Fig. 6.11 shows the current through the neutral point is based on a zero crossing voltage occurring in either of the phase terminals of a three-level diode-clamped inverter as shown in Fig. 6.9. The variation of both DC-link capacitor voltages is observed by the neutral point current $I_m(t)$ flowing in and out of the node. It can be inferred that the neutral point 'm' is a floating point of DC voltage across each DC capacitor

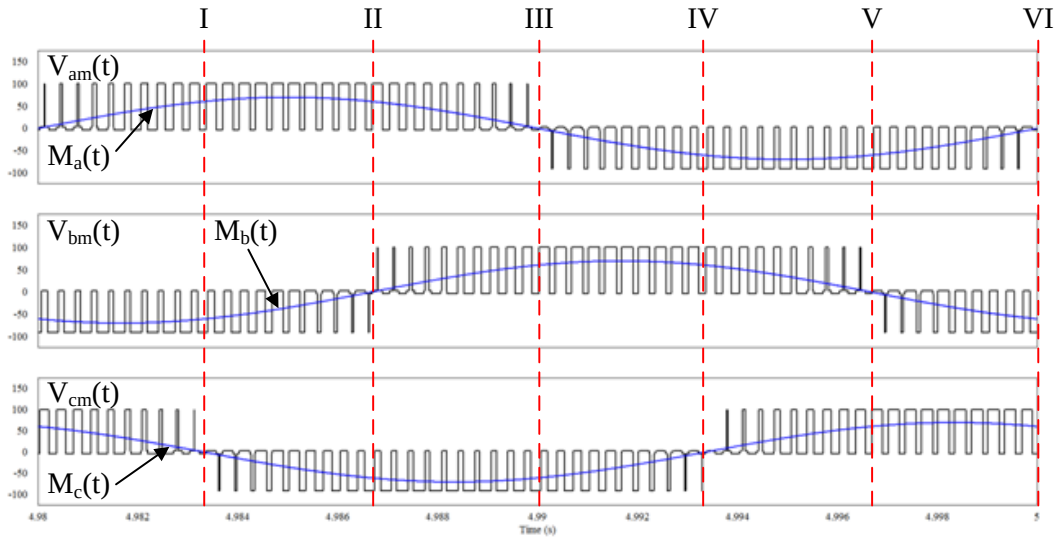


Fig. 6.9 Waveform of the output phase voltage and modulation signals [Vam(t), Vbm(t) and Vcm(t)] and [Ma(t), Mb(t) and Mc(t)] respectively with zero crossing per-phase leg output voltage analysis.

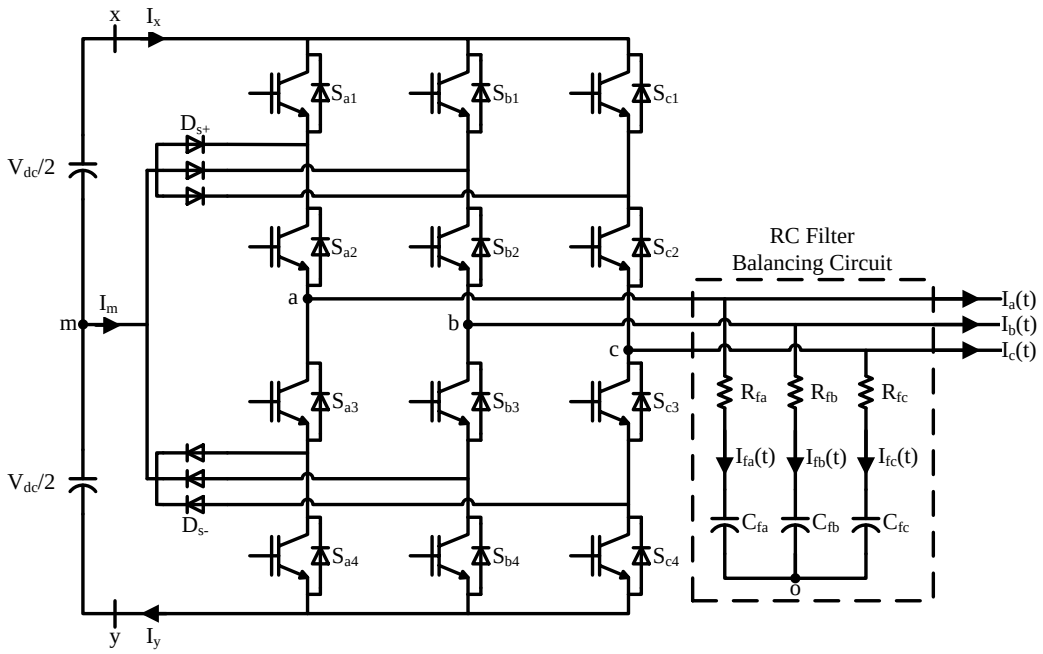
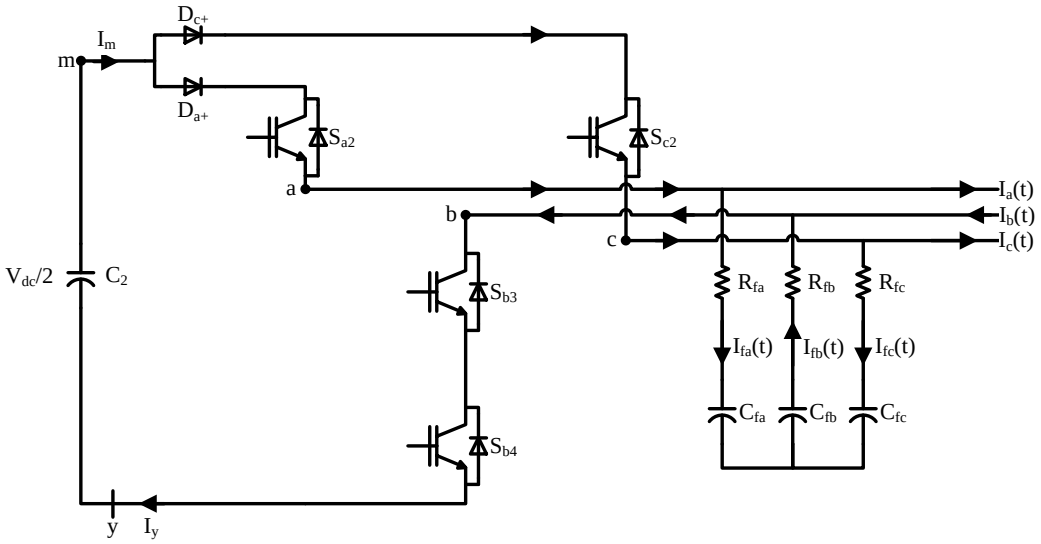
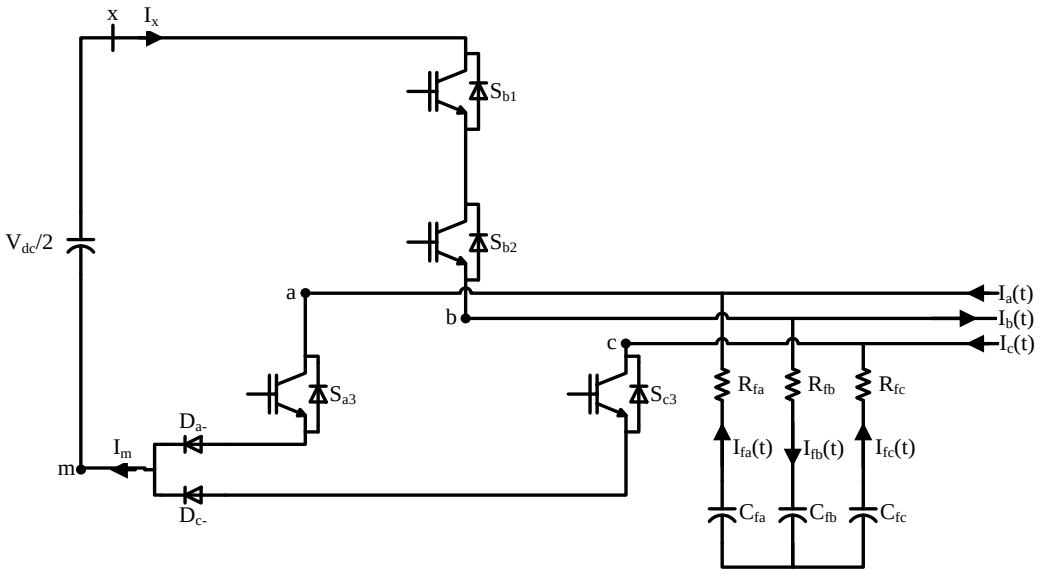


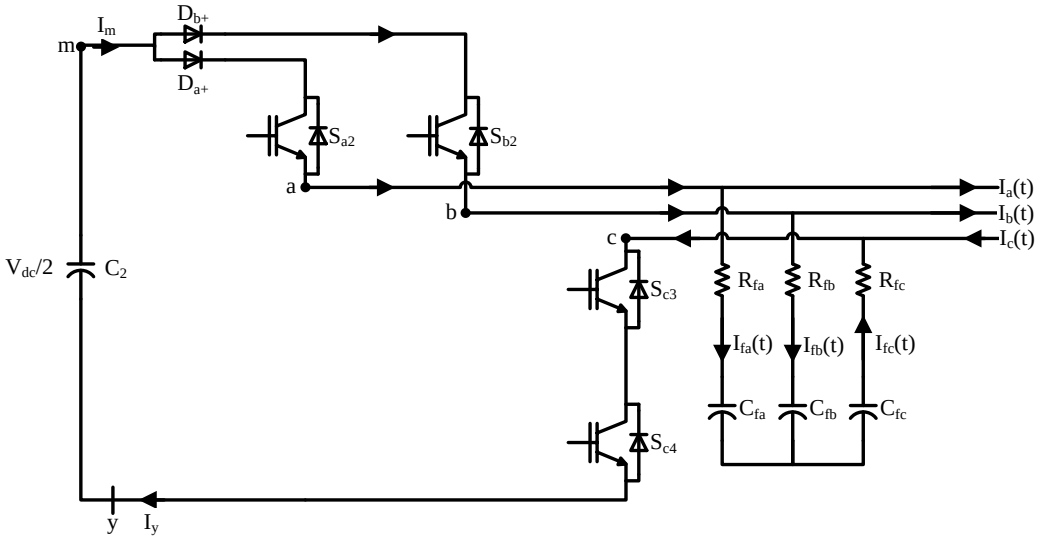
Fig. 6.10 Three-phase three-level diode-clamped inverter with star-connected RC filter balancing circuit.


Dc+
Im
m
Da+
Sa2
Sc2
a
b
c
Ia(t)
Ib(t)
Ic(t)
Vdc/2
C2
Sb3
Rfa
Rfb
Rfc
Ifa(t)
Ifb(t)
Ifc(t)
Cfa
Cfb
Cfc
Sb4
y
Iy

(a)


x
Ix
Sb1
Vdc/2
Sb2
a
b
c
Ia(t)
Ib(t)
Ic(t)
Sa3
Sc3
Rfa
Rfb
Rfc
Da-
Im
m
Ifa(t)
Ifb(t)
Ifc(t)
Dc-
Cfa
Cfb
Cfc

(b)


Db+
Im
m
Da+
Sa2
Sb2
a
b
c
Ia(t)
Ib(t)
Ic(t)
Vdc/2
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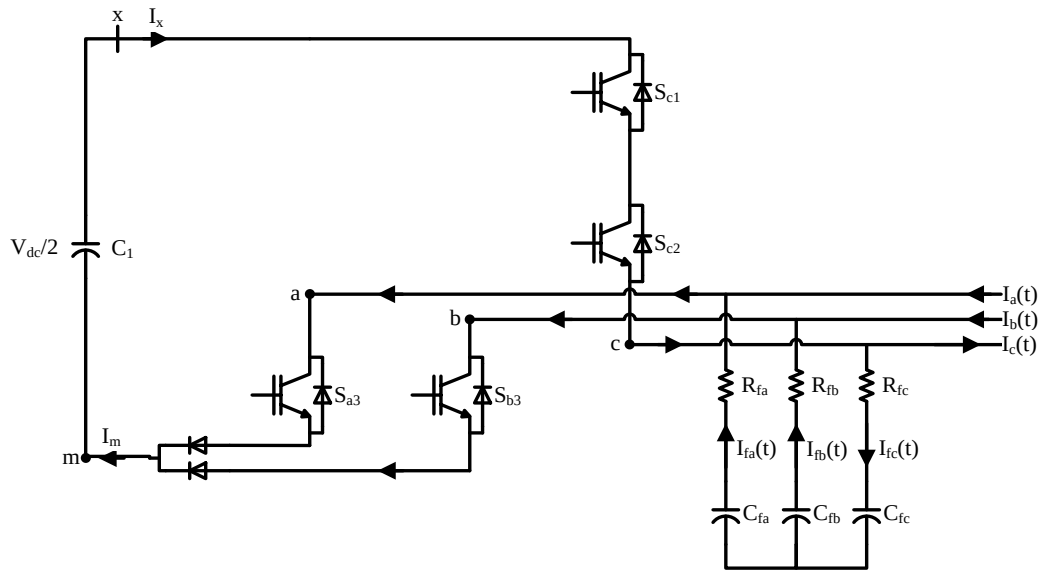
Rfa
Rfb
Rfc
Ifa(t)
Ifb(t)
Ifc(t)
Cfa
Cfb
Cfc
Sc4
y
Iy

(c)



(d)

Fig. 6.11 Switching state for zero crossing voltage per-phase leg as stated in Fig. 6.9. (a) Intersection point I and VI, (b) intersection point IV, (c) intersection point II and III, and (d) intersection point V.

and generates a zero sequence output voltage in a three-level diode-clamped inverter. With the natural balancing star-connected RC filter circuit, the zero sequence output voltage can be diverted into the RC filter circuit. Whereby, the high switching harmonic current will flow through the RC filter. The effect of the few high frequency harmonic currents entering the load terminal can be neglected as the magnitude of such currents is very low. The expression of the output per-phase RC filter voltages are given in the following equation.

$$\begin{cases} V_{ao}(t) = V_{am}(t) - V_{om}(t) \\ V_{bo}(t) = V_{bm}(t) - V_{om}(t) \\ V_{co}(t) = V_{cm}(t) - V_{om}(t) \end{cases} \tag{6.7}$$

where $V_{om}(t)$ is the zero sequence output voltage between ‘o’ and ‘m’. The zero sequence output voltage with natural balancing RC filter circuit is express as:

$$V_{om}(t)=\frac{V_{am}(t)+V_{bm}(t)+V_{cm}(t)}{3} \tag{6.8}$$

As discussed in the previous sub-section on balancing control method, the voltage across the RC filter is expressed in the terms of the given switching function equation. By substituting equation (5.9) and (6.8) into equation (6.7), the output three phase voltages of inverter with star connected the RC filter is expressed in the following form.

$$\begin{cases} V_{ao}(t)=\dfrac{2V_{am}(t)-V_{bm}(t)-V_{cm}(t)}{3} \\ V_{bo}(t)=\dfrac{-V_{am}(t)+2V_{bm}(t)-V_{cm}(t)}{3} \\ V_{co}(t)=\dfrac{-V_{am}(t)-V_{bm}(t)+2V_{cm}(t)}{3} \end{cases} \tag{6.9}$$

Extending equation (6.9) by substituting (6.3), we get

$$\begin{cases} V_{ao}(t)\approx\dfrac{1}{3}\left\{\begin{array}{c}\left[V_{c1}(t)+V_{c2}(t)\right]\left[M_a(t)-\frac{1}{2}M_b(t)-\frac{1}{2}M_c(t)\right] \\ +\left[V_{c1}(t)-V_{c2}(t)\right]\left[1-\frac{1}{2}-\frac{1}{2}\right]\end{array}\right\} \\ V_{bo}(t)\approx\dfrac{1}{3}\left\{\begin{array}{c}\left[V_{c1}(t)+V_{c2}(t)\right]\left[M_b(t)-\frac{1}{2}M_a(t)-\frac{1}{2}M_c(t)\right] \\ +\left[V_{c1}(t)-V_{c2}(t)\right]\left[1-\frac{1}{2}-\frac{1}{2}\right]\end{array}\right\} \\ V_{co}(t)\approx\dfrac{1}{3}\left\{\begin{array}{c}\left[V_{c1}(t)+V_{c2}(t)\right]\left[M_c(t)-\frac{1}{2}M_a(t)-\frac{1}{2}M_b(t)\right] \\ +\left[V_{c1}(t)-V_{c2}(t)\right]\left[1-\frac{1}{2}-\frac{1}{2}\right]\end{array}\right\} \end{cases} \tag{6.10}$$

Based on the equation (6.10), the dc component term on the right hand side of ($V_{C1}(t)$-$V_{C2}(t)$) is zero. This type of star-connected RC filter is able to perform self-cancellation of the dc component during the initial period of the dc capacitor charge and discharge.

Hence, the output phase voltage of a three-level diode-clamped inverter can operate at the balanced voltage waveform during steady-state condition.

Since dc component of the output phase voltage is cancelled by the RC filter property, the voltage across each capacitor of the dc-link terminal is approximately equal. Then, the expression of the output voltage with RC filter is written as:

$$\begin{cases} V_{ao}(t) \approx \frac{V_{dc}}{3}\left[M_a(t) - \frac{1}{2}M_b(t) - \frac{1}{2}M_c(t) \right] \\ \qquad = \frac{V_{dc}}{3}\left[m\cos(\omega t + \theta_0) - \frac{1}{2}m\cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) - \frac{1}{2}m\cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) \right] \\ V_{bo}(t) \approx \frac{V_{dc}}{3}\left[M_b(t) - \frac{1}{2}M_a(t) - \frac{1}{2}M_c(t) \right] \\ \qquad = \frac{V_{dc}}{3}\left[m\cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) - \frac{1}{2}m\cos(\omega t + \theta_0) - \frac{1}{2}m\cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) \right] \\ V_{co}(t) \approx \frac{V_{dc}}{3}\left[M_c(t) - \frac{1}{2}M_a(t) - \frac{1}{2}M_b(t) \right] \\ \qquad = \frac{V_{dc}}{3}\left[m\cos\left(\omega t + \theta_0 - \frac{4\pi}{3}\right) - \frac{1}{2}m\cos(\omega t + \theta_0) - \frac{1}{2}m\cos\left(\omega t + \theta_0 - \frac{2\pi}{3}\right) \right] \end{cases}$$

(6.11)

Based on the above approximation, the dominant harmonic present in output voltage across RC filter is the fundamental component without any dc component occurs in the system. The simulated and analytical results are illustrated in Fig. 6.12 (ref. to page 93), both results shows that, the fundamental component of voltage are equal.

The RC filter current is expressed in terms of rate of change of capacitor voltages and by using Laplace transformation. The final expression of the capacitor voltages of the RC filter network are derived as:

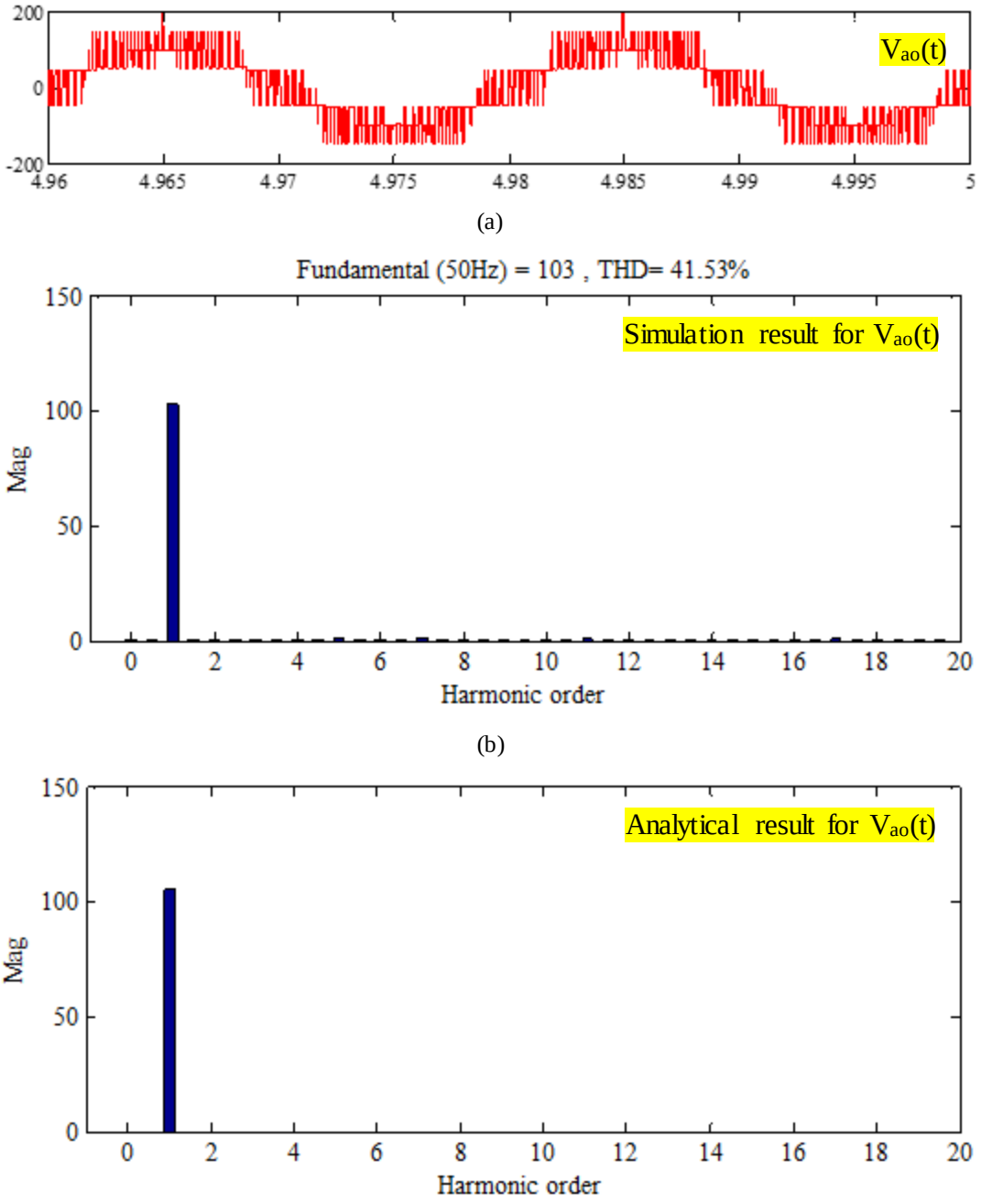


Fig. 6.12 RC filter voltage across node 'a' to node 'o'. (a) Simulation result for instantaneous pole voltage, (b) Simulated result for FFT analysis of pole voltage, and (c) analytical result of equation (6.11) in FFT analysis.

$$\begin{cases} V_{Cfa}(t) = \dfrac{V_{ao}(t)}{R_{fa}C_{fa}} e^{\frac{-(t+\theta_0)}{\tau}} \\ V_{Cfb}(t) = \dfrac{V_{bo}(t)}{R_{fb}C_{fb}} e^{\frac{-\left(t+\theta_0-\frac{2\pi}{3}\right)}{\tau}} \\ V_{Cfc}(t) = \dfrac{V_{co}(t)}{R_{fc}C_{fc}} e^{\frac{-\left(t+\theta_0-\frac{4\pi}{3}\right)}{\tau}} \end{cases} \tag{6.12}$$

Assume three-phase RC filter parameters are equal value, then $R_{fa} = R_{fb} = R_{fc} = R$ and $C_{fa} = C_{fb} = C_{fc} = C$. Thus, (6.12) is rewritten as:

$$\begin{cases} V_{Cfa}(t) = \dfrac{V_{ao}(t)}{RC} e^{\frac{-1}{RC}(t+\theta_0)} \\ V_{Cfb}(t) = \dfrac{V_{bo}(t)}{RC} e^{\frac{-1}{RC}\left(t+\theta_0-\frac{2\pi}{3}\right)} \\ V_{Cfc}(t) = \dfrac{V_{co}(t)}{RC} e^{\frac{-1}{RC}\left(t+\theta_0-\frac{4\pi}{3}\right)} \end{cases} \tag{6.13}$$

Based on the above assumption, filter currents expression with the periodic time interval are shown in the following.

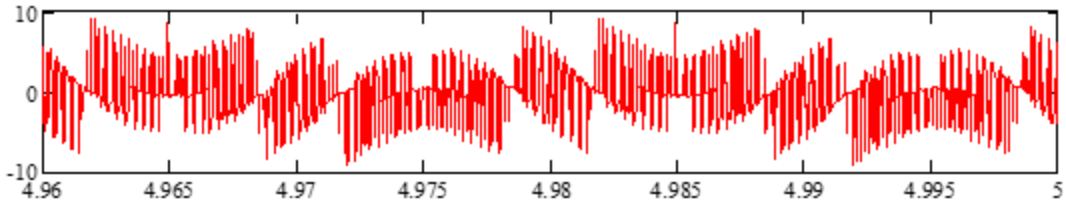
$$\begin{cases} I_{fa}(t) = -\dfrac{V_{dc}m}{2R} e^{-\frac{t+\theta_0}{RC}} \left[\omega \sin(\omega t+\theta_0) + \dfrac{1}{RC}\cos(\omega t+\theta_0) \right] \\ I_{fb}(t) = -\dfrac{V_{dc}m}{2R} e^{-\frac{t+\theta_0-\frac{2\pi}{3}}{RC}} \left[\omega \sin\left(\omega t+\theta_0-\dfrac{2\pi}{3}\right) + \dfrac{1}{RC}\cos\left(\omega t+\theta_0-\dfrac{2\pi}{3}\right) \right] \\ I_{fc}(t) = -\dfrac{V_{dc}m}{2R} e^{-\frac{t+\theta_0-\frac{4\pi}{3}}{RC}} \left[\omega \sin\left(\omega t+\theta_0-\dfrac{4\pi}{3}\right) + \dfrac{1}{RC}\cos\left(\omega t+\theta_0-\dfrac{4\pi}{3}\right) \right] \end{cases}$$

(6.14)

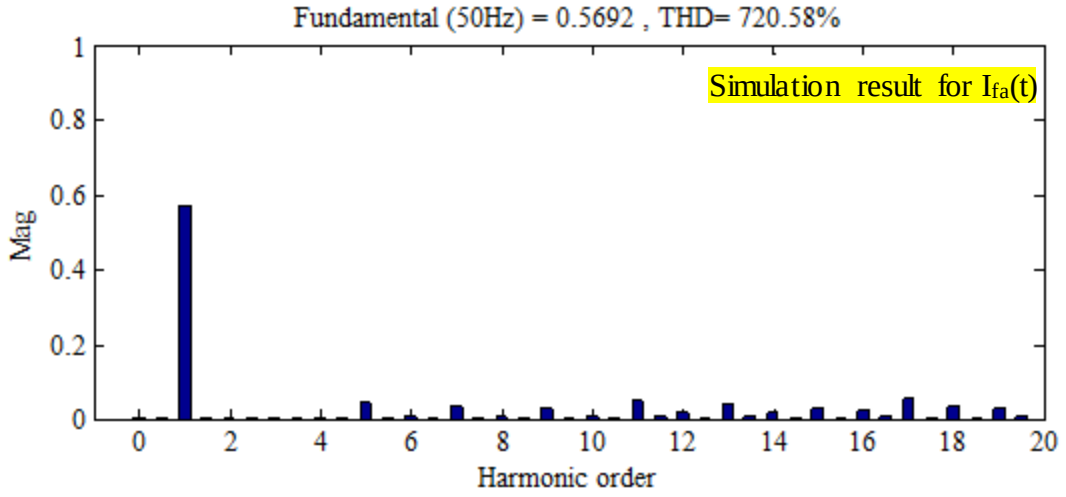
6.1.4 Measurement Results for Natural Balancing Method

The simulated results are used to evaluate the analytical solution of the three-level diode-clamped inverter topology with a mismatch in dc capacitance (C1 = 1200μF and C2 = 800μF). The analytical solution of equation (6.14) is illustrated in Fig. 6.13(c) and simulated harmonic order of the filter current is shown in Fig. 6.13(b). By comparing both results, analytical solution shows order of the dominant harmonic component of the filter current, where high switching frequency components are not included in the Fourier analysis.

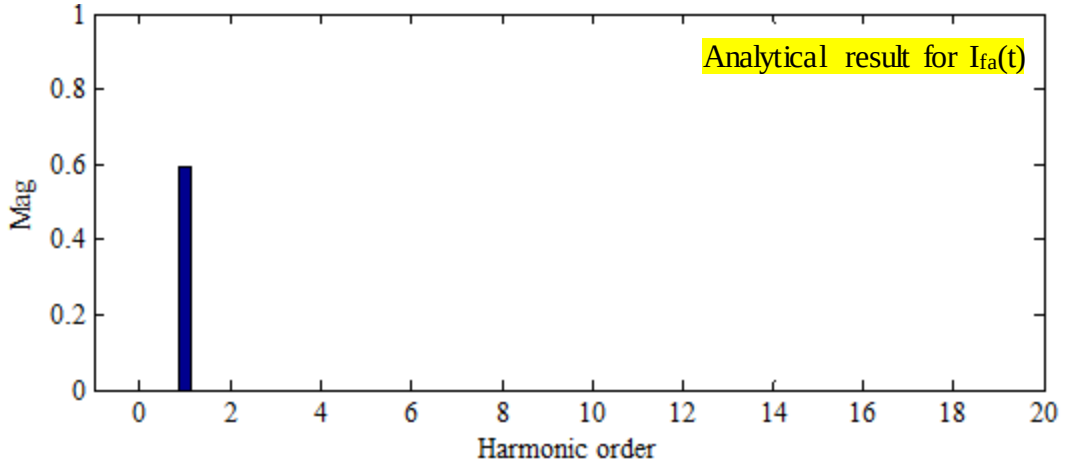
Fig. 6.14 (a) show the output pole voltage is stable and balanced under steady-state condition. Ripple current of the load is low due to the highly inductive load and RC filter as shown in Fig. 6.14 (b). This method can eliminate the additional sensors for the hardware implementation and production cost is also reduced.



(a)

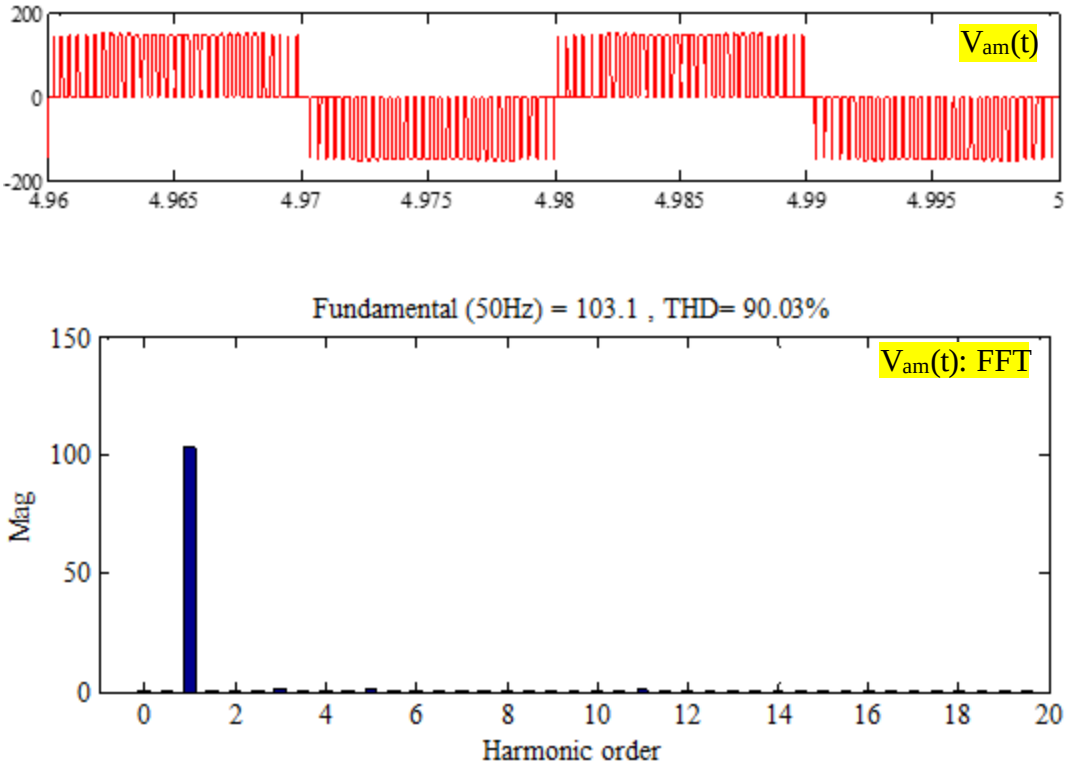


(b)

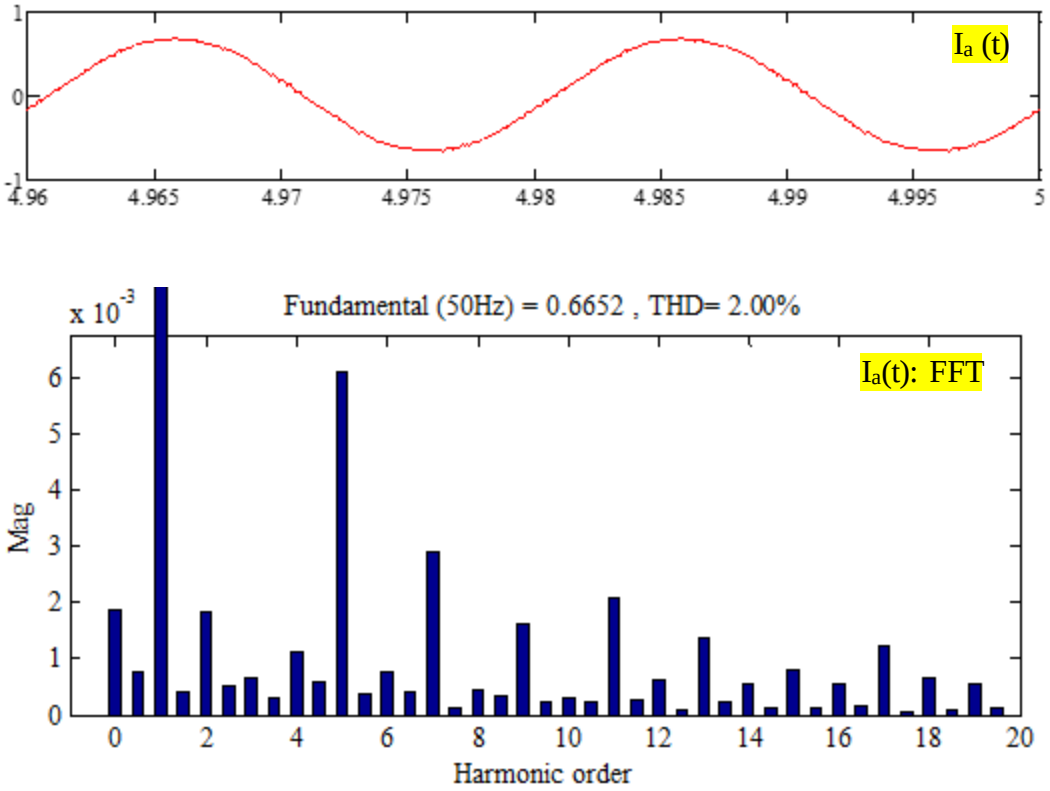


(c)

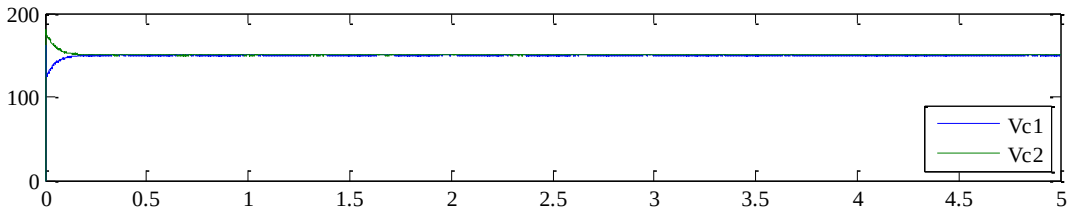
Fig. 6.13 RC filters current flow of phase 'a' terminal. (a) Simulation result for instantaneous filter current, (b) simulated result for FFT analysis of filter current, and (c) Analytical result of equation (6.14) in FFT analysis.


$V_{am}(t)$
Fundamental (50Hz) = 103.1 , THD= 90.03%
$V_{am}(t)$: FFT
Mag
Harmonic order

(a)


I_a (t)
x 10^{-3}
Fundamental (50Hz) = 0.6652 , THD= 2.00%
$I_a(t)$: FFT
Mag
Harmonic order

(b)



(c)

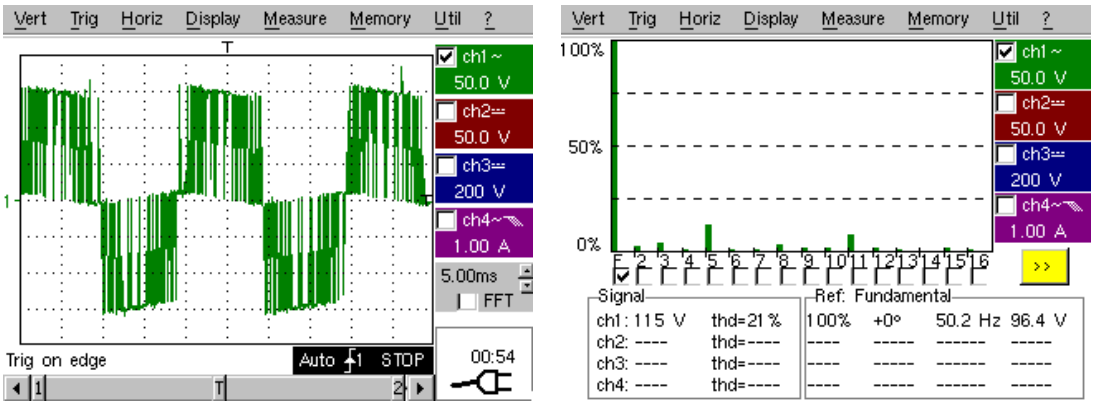
Fig. 6.14 Simulation results with the output voltage and current of a three-phase three-level diode-clamped inverter with the balancing RC filter circuit. (a) Voltage waveform (top figure) and respective FFT (bottom figure), (b) current waveform (top figure) and respective FFT (bottom figure), and (c) distribution voltage level of each capacitor in the dc bus.

To verify the balancing circuit with RC filter, experimental results are used to evaluate the output performance of the three-phase/three-level diode-clamped inverter. Fig. 6.15(a) presents the output pole voltage waveform and respective harmonic order of a three-level diode-clamped inverter. From the obtained results, one can observe that the RC filters circuit has the balancing feature and does not comprise any dc component in the output voltage. Thus, both the capacitor voltages in the dc bus are equally distributed as shown in Fig. 6.14(c) and 6.15(c).

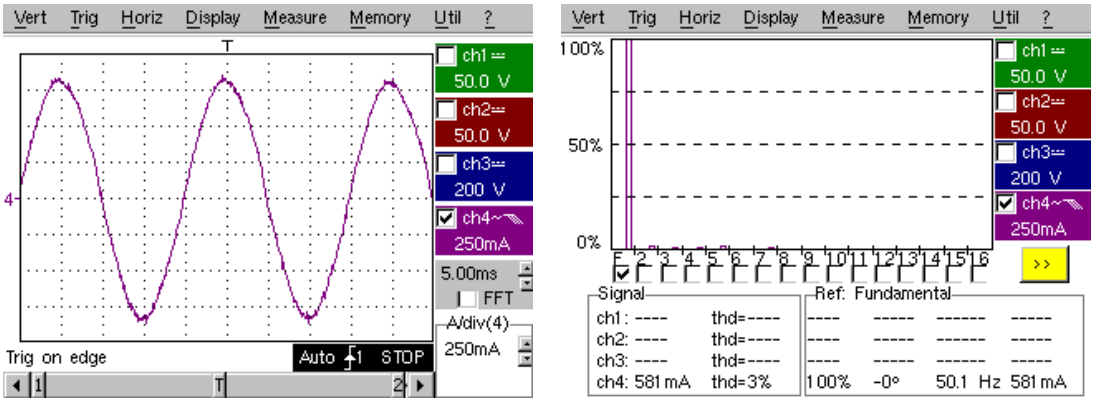
The limitations of RC filter balancing technique in multilevel inverters are the losses caused by the resistors and value of the RC parameter is to be selected according to the load power requirement. However, the RC filter balancing technique is a simple and cost effective solution for obtaining a balanced DC-link voltage.

6.2 Discussion

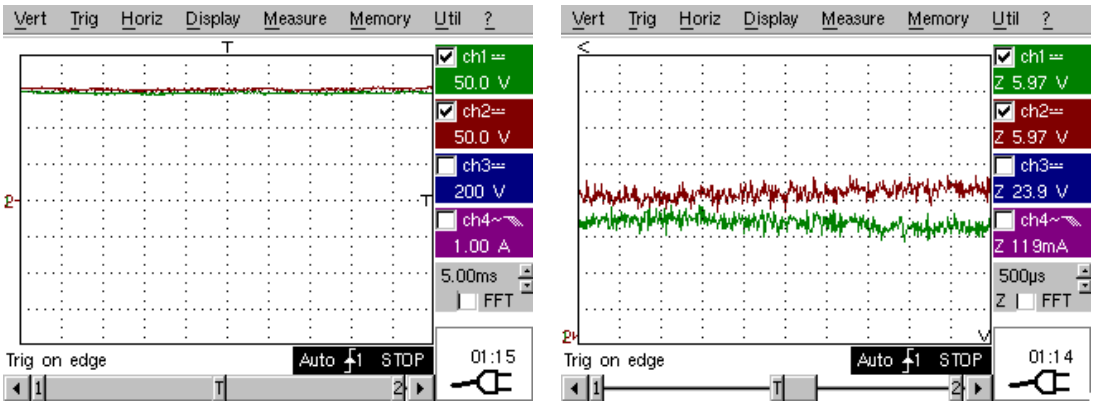
A short description of the voltage balancing for a three-level diode-clamped inverter topology is introduced. The unbalanced voltage in the DC link is critical for the load and especially high voltage stress across each IGBT is experienced. This unbalanced phenomenon can cause even order harmonic distortion in the neutral-point clamped as well as the output AC terminal which may severely damage the motor winding.



(a)



(b)



(c)

Fig. 6.15 Experimental results with the output voltage and current of a three-phase three-level diode-clamped inverter with the balancing RC filter circuit. (a) Voltage waveform (left figure) and respective FFT (right figure), (b) current waveform (left figure) and respective FFT (right figure), and (c) distribution voltage level of each capacitor in the dc bus.

Therefore, a voltage balancing in the DC link with the active and passive balancing methods is proposed. By comparing both methods, the active balancing method does not contain any additional loss in the system. But this method requires high resolution measurement for the voltage especially implementing in the DSP. When the DC link voltage level is high, the measurement of both capacitors must be precisely tuned. However, this active balancing method does not require any additional cost for the RC filter as well as reduce the space required.

Chapter 7 – Comparative Study on Multilevel AC/DC/AC Drives under Unbalanced Capacitor Voltage in DC Bus

This chapter explores the possibility of AC/DC/AC drive with near unity power factor front-end rectifier and rear-ends multilevel inverters. The proposed front-end rectifier is presented in chapter 3, which is used for AC to DC power conversion. Rear-end five-level inverters provide low THD and better efficiency as no voltage oscillation is occurred in the dc-link. Five-level inverters are usually employed with low switching frequency to suppress the resonant filter size. Besides, the low switching frequency will lead to low electromagnetic interference (EMI) and even allow us to use switching devices of lower rating with better switching and conduction performance as compared to the switching devices rated at full dc-link voltage in two-level inverter.

Five-level inverter topologies have perceived advantages such as low THD and better efficiency when compared to two/three-level inverter topologies for high power application. But in terms of AC/DC/AC drive with a single dc bus, rear-end multilevel inverter will cause extreme unbalance in capacitor voltages in dc bus. Therefore, an appropriate rear-end multilevel inverters for more than five-level incremental voltage steps has to be selected.

Based on the analysis, modeling and experimentation results rear-end flying capacitor inverters with number of voltage levels more than five result in a very low output THD due to its self-balancing property when compared to diode-clamped inverter topology. Having no diode components clamped in the neutral-point terminal, the flying capacitor inverter produce better efficiency and good quality output voltage. The analytical performance of the AC/DC/AC drives is verified on the 1.35kW laboratory prototype.

7.1 Switching Function Analysis for Five-Level Inverters

Two types of five-level switching schemes will be covered in this sub-section. The switching schemes are level-shifted pulse width modulation (5L LS-PWM) and phase-shifted pulse width modulation (5L PS-PWM). 5L-LS-PWM and 5L-PS-PWM are utilized in five-level diode-clamped inverter and five-level flying capacitor inverter respectively. The analysis of both switching strategies is calculated based on the linear modulating function, which is similar to chapter 5. [**Note**: The switching function analysis is applied when the switching frequency is 10 times greater than the fundamental frequency of the control signal.]

7.1.1 Five-Level PWM Referred to Level-Shifted Carrier Base (5L LS-PWM)

Fig. 7.1 shows the level-shifted PWM for a five-level diode-clamped inverter topology. Two positive carrier signals are modulated with the positive amplitude control signal and similarly for both negative carrier signals as shown in Fig. 7.1. In one sampling period, the control signal will intersect at both edges of the periodic carrier wave. The intersection point for positive amplitude modulating control signal is formulated in a form of linear expression. The half of the time interval between the intersection points of the carrier signal and the turn on intervals of the switching device is expressed as:

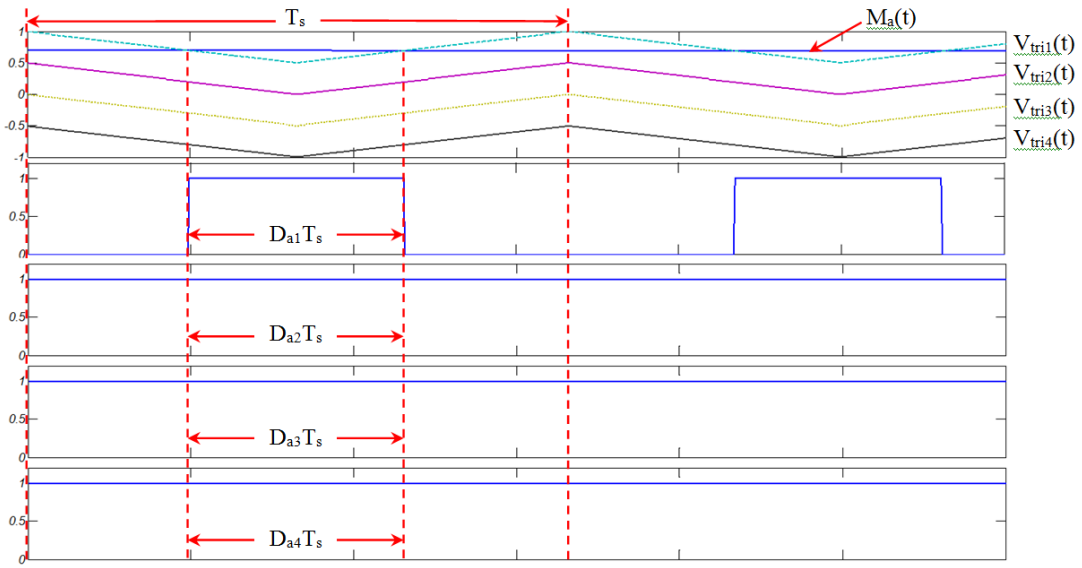


Fig. 7.1 5L LS-PWM for respective switching device from S_{a1} to S_{a4} of phase 'a'.

$$\begin{cases} t_{a1} = \dfrac{T_s\left(1-D_{a1}\right)}{2} \\ t_{a2} = \dfrac{T_s\left(1-D_{a2}\right)}{2} \\ t_{a3} = \dfrac{T_s\left(1-D_{a3}\right)}{2} \\ t_{a4} = \dfrac{T_s\left(1-D_{a4}\right)}{2} \end{cases} \tag{7.1}$$

where t_{a1} to t_{a4} is the intersecting point for the initial turn on period of the switching device S_{a1} to S_{a4} and T_s is one sampling time of the carrier frequency.

D_{a1} to D_{a4} is the duty ratio of the conduction period for the linear modulation control signal, which is operating in the range of $0 \leq [\ D_{a1}$ to $D_{a4}\ ] \leq 1$. The duty ratio of the conduction period defines the relationship between the amplitude of the modulation control signal and the edge of triangular waveform at half of the carrier frequency. The linearized expressions for points of intersection is written as

$$\begin{cases} M_{a1}\left(t\right) = \dfrac{-1}{T_s} t_{a1} + 1 \\ M_{a2}\left(t\right) = \dfrac{-1}{T_s} t_{a2} + \dfrac{1}{2} \\ M_{a3}\left(t\right) = \dfrac{-1}{T_s} t_{a3} \\ M_{a4}\left(t\right) = \dfrac{-1}{T_s} t_{a4} - \dfrac{1}{2} \end{cases} \tag{7.2}$$

Let assume $S_{a1}(t)$ to $S_{a4}(t)$ is equal to the duty ratio of D_{a1} to D_{a4} respectively. Then, substituting equation (7.1) into equation (7.2), we get

$$\begin{cases} S_{a1}\left(t\right) \approx 2M_{a1}\left(t\right) - 1 \\ S_{a2}\left(t\right) \approx 2M_{a2}\left(t\right) \\ S_{a3}\left(t\right) \approx 2M_{a3}\left(t\right) + 1 \\ S_{a4}\left(t\right) \approx 2M_{a4}\left(t\right) + 2 \end{cases}$$

$$\begin{aligned} M_a(t) &= M_{a1}(t) + M_{a2}(t) + M_{a3}(t) + M_{a4}(t) \\ &= \frac{S_{a1}(t) + S_{a2}(t) + S_{a3}(t) + S_{a4}(t) - 2}{2} \end{aligned} \tag{7.3}$$

Equation (7.3) is the switching function with the change of the linear modulation with respect to time and the complementary switching function is known as

$$\begin{cases} S_{a5}(t) \approx 1 - S_{a1}(t) = 2\left[1 - M_{a5}(t)\right] \\ S_{a6}(t) \approx 1 - S_{a2}(t) = 1 - 2M_{a6}(t) \\ S_{a7}(t) \approx 1 - S_{a3}(t) = -2M_{a7}(t) \\ S_{a8}(t) \approx 1 - S_{a4}(t) = -\left[1 + 2M_{a8}(t)\right] \end{cases}$$

$$\begin{aligned} M_a(t) &= M_{a5}(t) + M_{a6}(t) + M_{a7}(t) + M_{a8}(t) \\ &= \frac{2 - S_{a5}(t) - S_{a6}(t) - S_{a7}(t) - S_{a8}(t)}{2} \end{aligned} \tag{7.4}$$

7.1.2 Five-Level PWM Referred to Phase-Shifted Carrier Based (5L PS-PWM)

Fig. 7.2 shows the phase-shifted PWM for a five-level capacitor-clamped inverter topology, which consists of four carrier waves. Each carriers wave are shifted by (360˚/ (n-1)) apart from each other, where n is the number of level consisting in the inverter circuit (i.e. five-level capacitor clamped inverter, n=5).

The analysis of the switching function explained in sub-section 7.1.1 is applied here, while the expression of the initial conduction period in phase-shifted carrier is calculated based on half modulation index for the ease of the analysis. The analysis of modulation function with respect to the switching function does not consist of any sub-modulation function as compared the LS-PWM, this is due to the fact that each carrier base is shifted 90° apart from the reference 0° carrier wave and each carrier slope is in line with the same carrier wave. Hence, modulation analysis can be directly calculated with the respective switching function. The initial period for the modulation signal cross over the edge of the carrier wave is defined as

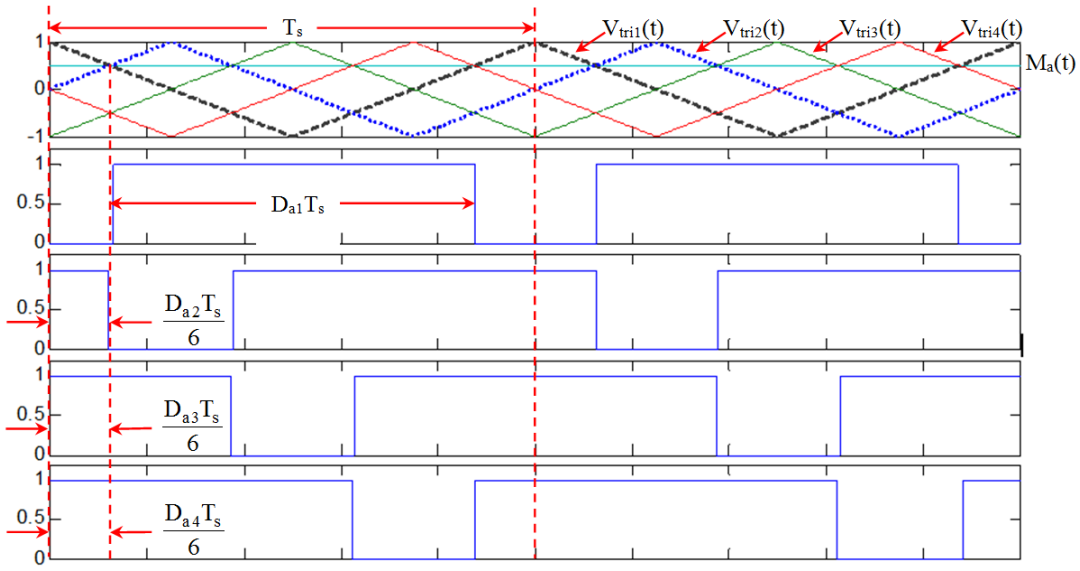


Fig. 7.2 5L PS-PWM for respective switching device from S_{a1} to S_{a4} of phase 'a'

$$\begin{cases} t_{a1} = \dfrac{T_s\left(1-D_{a1}\right)}{2} \\ t_{a2} = \dfrac{D_{a2}T_s}{6} \\ t_{a3} = \dfrac{D_{a3}T_s}{6} \\ t_{a4} = \dfrac{D_{a4}T_s}{6} \end{cases} \tag{7.5}$$

Based on equation (7.5), the linear expression for each phase-shifted carrier wave is set at the reference slope of $DT_s/6$. Hence, the slope for each crossing edge at $0 \leq t \leq DT_s/6$ of the modulation signal is known as

$$\begin{cases} M_{a1}(t) = \dfrac{-4}{T_s} t_{a1} + 1 \\ M_{a2}(t) = \dfrac{4}{T_s} t_{a2} \\ M_{a3}(t) = \dfrac{4}{T_s} t_{a3} - 1 \\ M_{a4}(t) = \dfrac{-4}{T_s} t_{a4} \end{cases} \tag{7.6}$$

$$\langle M_{a1}(t), M_{a2}(t), M_{a3}(t), M_{a4}(t) \rangle \leftrightarrow M_a(t) \quad \text{for PS-PWM technique only}$$

The Duty ratio from D_{a1} to D_{a4} are determined by the switching function $S_{a1}(t)$-$S_{a4}(t)$. While the complementary switching function from $S_{a5}(t)$ to $S_{a8}(t)$ in a five-level flying capacitor inverter are complementary to switching functions $S_{a1}(t)$ – $S_{a4}(t)$. The switching functions are

$$\begin{cases} S_{a1}(t) \approx \dfrac{M_a(t)+1}{2} \\ S_{a2}(t) \approx \dfrac{3}{2} M_a(t) \\ S_{a3}(t) \approx \dfrac{3\left[M_a(t)+1\right]}{2} \\ S_{a4}(t) = \dfrac{-3}{2} M_a(t) \end{cases}$$

$$\begin{cases} S_{a5}(t) = 1 - S_{a4}(t) \approx \dfrac{3\left[M_a(t)+\frac{2}{3}\right]}{2} \\ S_{a6}(t) = 1 - S_{a3}(t) \approx \dfrac{-3}{2} M_a(t) \\ S_{a7}(t) = 1 - S_{a2}(t) \approx \dfrac{-\left[3M_a(t)+\frac{2}{3}\right]}{2} \\ S_{a8}(t) = 1 - S_{a1}(t) = \dfrac{-1}{2} M_a(t) \end{cases} \tag{7.7}$$

7.2 AC/DC/AC Drive with Rear-End Five-Level Inverter Topologies

Multilevel AC/DC/AC drives are well adopted solutions for wind power systems constituting permanent magnet synchronous generator (PMSG) and utility grid [68, 69, 88]. Topologies in Figs. 7.3 and 7.4 can be implemented for wind powered PMSG system. Both the presented ac sources are required to operate at a very low THD and at unity power factor.

The proposed multilevel AC/DC/AC converter is constructed based on unity power factor front-end rectifier and rear-end five-level multilevel inverter, which is used for high power renewable energy conversion. The comparison study of both topologies is shown in Figs. 7.3 and 7.4. Both DC/AC configurations are connected to single dc-bus, which is able to fit in the output terminal of a unity power factor front-end rectifier. The proposed AC/DC/AC topologies address major limitations of existing inverter topologies such as high voltage stress and high rate of change of voltage without using any sort of snubber circuits.

7.2.1 Rear-End Five-Level Diode-Clamped Inverter (5L-MDCI)

A rear-end 5L-MDCI topology is shown in Fig. 7.3, which consist of 24 IGBT devices and 18 diode components. The individual node of 4 series connected dc capacitors is clamped with the respective node of two diodes connected in series. To achieve five-level output voltage, each of the switching devices has to block one-quarter of the dc-link voltage. Table 7.1 illustrates the five switching combination of the output pole voltage level under balanced capacitor voltage in the dc-link. According to Table 7.1, the output pole voltage per-phase leg of the 5L-MDCI is expressed as:

$$V_{sm\langle balance\rangle}(t)=\frac{V_{dc}(t)}{4}\begin{bmatrix} S_{s1}(t)\,\mathrm{sign}\left(M_s(t)\right)+S_{s2}(t)\,\mathrm{sign}\left(M_s(t)\right) \\ -S_{s5}(t)\,\mathrm{sign}\left(-M_s(t)\right)-S_{s6}(t)\,\mathrm{sign}\left(-M_s(t)\right) \end{bmatrix} \quad (7.8)$$

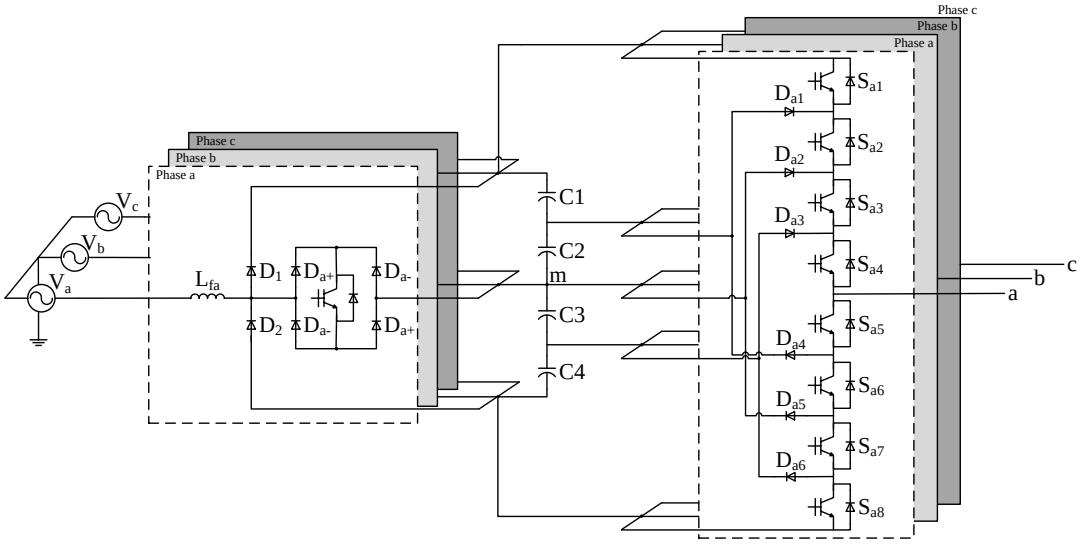


Fig. 7.3 Multilevel AC/DC/AC converter ith a rear-end five-level diode-clamped inverter (5L-MDCI).

TABLE 7.1

REAR-END 5L-MDCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

State	Switching States								Per-Phase Leg Voltage		
	S_{s1}	S_{s2}	S_{s3}	S_{s4}	S_{s5}	S_{s6}	S_{s7}	S_{s8}	V_{sx}	V_{sy}	V_{sm}
1	1	1	1	1	0	0	0	0	0	V_{dc}	$V_{dc}/2$
2	0	1	1	1	1	0	0	0	$-V_{dc}/4$	$3V_{dc}/4$	$V_{dc}/4$
3	0	0	1	1	1	1	0	0	$-V_{dc}/2$	$V_{dc}/2$	0
4	0	0	0	1	1	1	1	0	$-3V_{dc}/4$	$V_{dc}/4$	$-V_{dc}/4$
5	0	0	0	0	1	1	1	1	$-V_{dc}$	0	$-V_{dc}/2$

Where s represent phase a, b and c and S_{s1} to S_{s8} are presented as the IGBT switching devices for individual leg. Logic 1 represent as turn on and logic 0 represent as turn off for S_{s1}, S_{s2}, S_{s3} and S_{s4}

where sign ($M_a(t)$), sign ($M_b(t)$) and sign ($M_c(t)$) are the unipolar sign function with respect to the control sign of the modulation function $M_a(t)$, $M_b(t)$ and $M_c(t)$. The sign (Ma(t)) is expressed as:

$$\text{sign}\left(M_a(t)\right)=\begin{cases}1 & \text{if } M_a(t)\geq 0\\ 0 & \text{otherwise}\end{cases} \tag{7.9}$$

If the dc capacitor voltage in the dc bus is balanced, then the final expression of the output pole voltage is written as:

$$V_{sm\langle balance\rangle}(t)=\frac{V_{dc}(t)}{4}\left[S_{s1}(t)+S_{s2}(t)+S_{s3}(t)+S_{s4}(t)-2\right] \tag{7.10}$$

However in practice, the series connected node of the dc capacitors in the dc bus does not distributed equally as presented in chapter 5 ($V_{c1}(t) \neq V_{c2}(t) \neq V_{c3}(t) \neq V_{c4}(t)$). Hence, the expression of the output pole voltage is obtained from equation (7.8) and is written as

$$V_{sm\langle unbalance\rangle}(t)=\begin{bmatrix}V_{c1}(t)S_{s1}(t)\text{sign}\left(M_s(t)\right)\\ +V_{c2}(t)S_{s2}(t)\text{sign}\left(M_s(t)\right)\\ -V_{c3}(t)S_{s7}(t)\text{sign}\left(-M_s(t)\right)\\ -V_{c4}(t)S_{s8}(t)\text{sign}\left(-M_s(t)\right)\end{bmatrix} \tag{7.11}$$

Substitute the respective switching function based on LS-PWM scheme in sub-section 7.1.1 into equation (7.11), the expression of the output pole voltage with the dc component injection is shown in the following derivation.

$$V_{sm\langle unbalance\rangle}(t)\approx\frac{1}{2}V_{dc}(t)M_s(t)+V_o(t)\approx V_{sm\langle balance\rangle}(t)+V_o(t) \tag{7.12}$$

where $V_o(t)$ is the zero sequence voltage that cause the neutral-point voltage $V_m(t)$ float and this is written as

$$V_o(t)\approx\frac{V_{c1}(t)+V_{c2}(t)-V_{c3}(t)-V_{c4}(t)}{V_{dc}(t)} \tag{7.13}$$

Each of the dc capacitor will charge one quarter of the dc-link voltage during initial period and discharge the energy at $t = 0^+$. When the dc capacitor is discharge at $t = 0^+$, the output voltage will produce a certain magnitude of zero sequence voltage during steady-state condition. Based on equations from (7.11) to (7.13), the final expression of the output pole voltage is expressed as:

$$V_{sm\langle unbalance\rangle}(t) = 2\left[V_{c1}(t)S_{s1}(t) - V_{c4}(t)S_{s8}(t)\right] \tag{7.14}$$

From the above analysis, voltage across C2 and C3 are tending to decay at zero value during steady-state condition, which is caused by the zero sequence voltage in equation (7.13). The zero sequence voltage will force the dc voltage of C1 and C4 to be double amplitude, which results the performance of a 5L-MDCI topology to behave like a three-level diode-clamped inverter.

7.2.2 Rear-End Five-Level Flying Capacitor Inverter (5L-MFCI)

An alternative rear-end five-level inverter topology is shown in Fig. 7.4. This topology is illustrated the flying capacitor inverter with the capacitor clamped to each switch. The nominal voltage across each floating capacitor (for phase 'a') is $V_{Ca1} = 3V_{dc}/4$, $V_{Ca2} = V_{dc}/2$ and $V_{Ca3} = V_{dc}/4$ respectively. The output voltage level is synthesized through the PS-PWM scheme as stated in Table 7.2. Theoretically, this switching scheme provides equally distribution voltage level for each floating capacitors with the redundancy switching state. The theoretical voltage level for each capacitor is realized through the

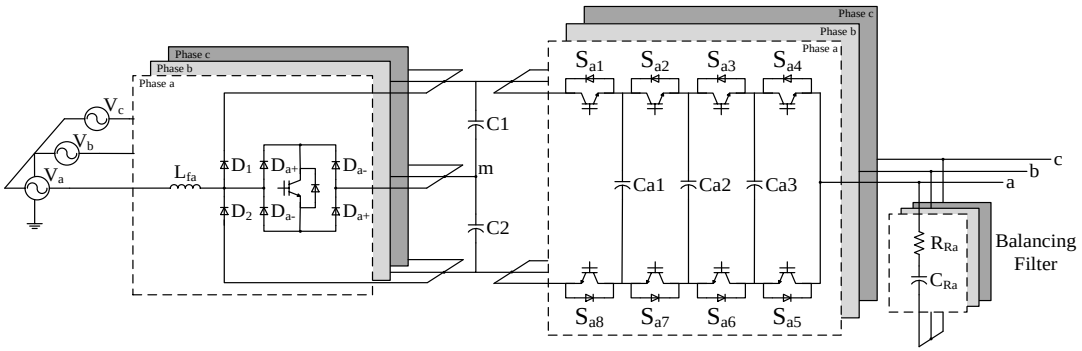


Fig. 7.4 Multilevel AC/DC/AC converter with a rear-end five-level flying capacitor inverter (5L-MFCI).

switching combination of Table 7.2. Few switching combination is illustrated in the following points based on the given Fig. 7.5.

1) When S_{a1} to S_{a4} is off, each voltage stress of the IGBTs is occurred at ¼ of the dc-link voltage.
2) When S_{a1} is on and S_{a2} to S_{a4} is off, the voltage stress across the complementary switching device of S_{a1} (S_{a8}) is ¼ of the dc-link voltage as stated in the first point. Voltage across the floating capacitor of C_{a1} is analyzed from the highest to lowest potential. Based on this assumption, the highest potential is directly clamped to the dc-link and lowest potential is $V_{dc}/4$. Hence, C_{a1} is distributed at $3V_{dc}/4$.
3) When S_{a1} to S_{a2} is on and S_{a3} to S_{a4} is off, the highest potential of C_{a2} is V_{dc} and lowest potential of C_{a2} is the summation of the voltage stress across S_{a7} and S_{a8} is $V_{dc}/2$. Then voltage across C_{a2} is appeared at half V_{dc}.
4) Similarly, when S_{a1} to S_{a3} is on and S_{a4} is off. Total voltage stress across S_{a6} to S_{a8} is $3V_{dc}/4$ and the highest potential of C_{a3} is at V_{dc}. Then voltage across C_{a3} is $V_{dc}/4$.

Note: $S_{a5} – S_{a8}$ are the complementary of $S_{a1} – S_{a4}$.

According to the nominal voltage level of each floating capacitor, MFCI configuration exhibits equal voltage stresses, approximately equal to ¼ of the dc-link voltage in theory.

However, practical design for more than four-level capacitor clamped inverter topology does not provide the nominal voltage level for the floating capacitors. Although, most of the paper has presented a PS-PWM has the self-balance property.

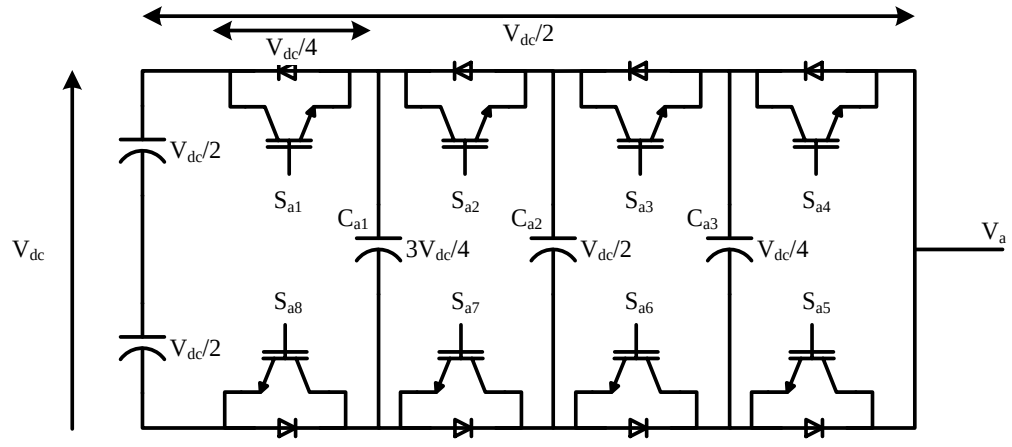


Fig. 7.5 5L-MFCI topology for phase ‘a’.

TABLE 7.2

REAR-END 5L-MFCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

State	Switching States								Per-Phase Leg Voltage		
	S_{s1}	S_{s2}	S_{s3}	S_{s4}	S_{s5}	S_{s6}	S_{s7}	S_{s8}	V_{sx}	V_{sy}	V_{sm}
1	1	1	1	1	0	0	0	0	0	V_{dc}	$V_{dc}/2$
	1	1	1	0	1	0	0	0			
2	1	1	0	1	0	1	0	0	$-V_{dc}/4$	$3V_{dc}/4$	$V_{dc}/4$
	1	0	1	1	0	0	1	0			
	1	1	0	0	1	1	0	0			
3	1	0	1	0	1	0	1	0	$-V_{dc}/2$	$V_{dc}/2$	0
	1	0	0	1	0	1	1	0			
4	1	0	0	0	1	1	1	0	$-3V_{dc}/4$	$V_{dc}/4$	$-V_{dc}/4$
5	0	1	1	1	0	0	0	1	$-V_{dc}/4$	$3V_{dc}/4$	$V_{dc}/4$
	0	1	1	0	1	0	0	1			
6	0	1	0	1	0	1	0	1	$-V_{dc}/2$	$V_{dc}/2$	0
	0	0	1	1	0	0	1	1			
	0	1	0	0	1	1	0	1			
7	0	0	1	0	1	0	1	1	$-3V_{dc}/4$	$V_{dc}/4$	$-V_{dc}/4$
	0	0	0	1	0	1	1	1			
8	0	0	0	0	1	1	1	1	$-V_{dc}$	0	$-V_{dc}/2$

Where s represent phase a, b and c and S_{s1} to S_{s8} are presented as the IGBT switching devices for individual leg. Logic 1 represent as turn on and logic 0 represent as turn off for S_{s1}, S_{s2}, S_{s3} and S_{s4}.

But in term of more than four level approach, the most inner capacitor voltage does not reach it's desire voltage level. Therefore, an additional passive balancing circuit is needed to filter the dc offset voltage in the floating capacitors.

Based on the valid switching states in Table 7.2 of the output phase voltage (5L-MFCI topology) under unbalance dc voltage in the floating capacitors, the expression of the output pole voltage based on the PS-PWM scheme is written as:

$$V_{sm\langle unbalance\rangle}(t)=\left\{\begin{array}{c} V_{dc}(t)S_{s1}(t)+V_{Cs1}\left[S_{s2}(t)-S_{s1}(t)\right] \\ +V_{Cs2}\left[S_{s3}(t)-S_{s2}(t)-1\right]+V_{Cs3}\left[S_{s4}(t)-S_{s3}(t)\right] \end{array}\right\} \quad (7.15)$$

where $V_{Cs1}(t)$, $V_{Cs2}(t)$ and $V_{Cs3}(t)$ are referring to the floating capacitor voltage of phase a, b and c of the rear-end 5L-MFCI topology. Each of the floating capacitor voltages is defined by the desire voltage level and additional dc offset voltage. The floating capacitor voltages are written as:

$$\left\{\begin{array}{l} V_{Cs1}(t)=\frac{3}{4}V_{dc}(t)-V_{o1}(t) \\ V_{Cs2}(t)=\frac{1}{2}V_{dc}(t)-V_{o2}(t) \\ V_{Cs3}(t)=\frac{1}{4}V_{dc}(t)-V_{o3}(t) \end{array}\right. \quad (7.16)$$

$V_{o1}(t)$, $V_{o2}(t)$ and $V_{o3}(t)$ are the dc offset voltage of the floating capacitors voltage. Where the dc offset voltages (small in magnitude) is estimated from the ESR resistance of the dc capacitors.

The dc offset is reduced by the RC filter. This filter serves the balancing feature for a 5L-MFCI topology. RC filter is implemented in the output of a 5L-MFCI topology and three RC filters are connected in a star configuration. The output phase voltage across each RC filter is defined by the relationship between the output pole voltage of a 5L-MFCI topology and the virtual ground across node ‘z’ to node ‘m’. This is expressed as:

$$\left\{\begin{array}{l} V_{az}(t)=V_{am\langle unbalance\rangle}(t)-V_{zm}(t) \\ V_{bz}(t)=V_{bm\langle unbalance\rangle}(t)-V_{zm}(t) \\ V_{cz}(t)=V_{cm\langle unbalance\rangle}(t)-V_{zm}(t) \end{array}\right. \quad (7.17)$$

where $V_{zm}(t)$ is the virtual ground voltage, which is referred from node z to node m. The expression of $V_{zm}(t)$ is known as:

$$V_{zm}(t) = \frac{V_{am}(t) + V_{bm}(t) + V_{cm}(t)}{3} \tag{7.18}$$

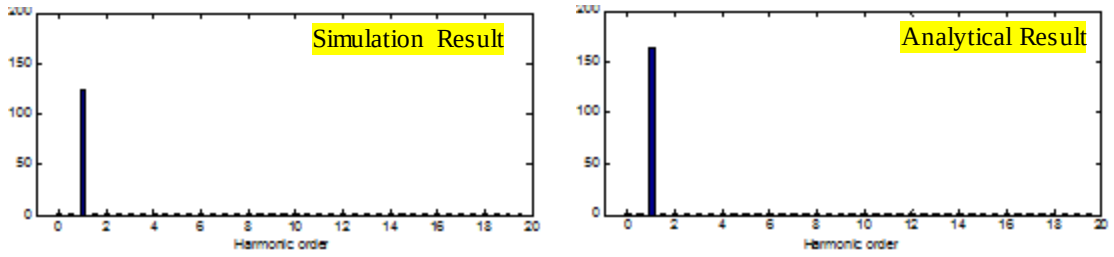
Expand equation (7.17) with the virtual ground voltage in (7.18), we get

$$\begin{cases} V_{az}(t) = \dfrac{2V_{am\langle unbalance\rangle}(t) - V_{bm\langle unbalance\rangle}(t) - V_{cm\langle unbalance\rangle}(t)}{3} \\ V_{bz}(t) = \dfrac{-V_{am\langle unbalance\rangle}(t) + 2V_{bm\langle unbalance\rangle}(t) - V_{cm\langle unbalance\rangle}(t)}{3} \\ V_{cz}(t) = \dfrac{-V_{am\langle unbalance\rangle}(t) - V_{bm\langle unbalance\rangle}(t) + 2V_{cm\langle unbalance\rangle}(t)}{3} \end{cases} \tag{7.19}$$

Then, substitute the pole voltage of equation (7.15) with their respective switching function as stated in equation (7.7) into (7.19). The final expressions of the output phase voltage of the RC filters are

$$\begin{cases} V_{az}(t) \approx \dfrac{M_a(t)V_{dc}(t) - \frac{1}{2}M_b(t)V_{dc}(t) - \frac{1}{2}M_c(t)V_{dc}(t)}{3} \\ V_{bz}(t) \approx \dfrac{-\frac{1}{2}M_a(t)V_{dc}(t) + M_b(t)V_{dc}(t) - \frac{1}{2}M_c(t)V_{dc}(t)}{3} \\ V_{cz}(t) \approx \dfrac{-\frac{1}{2}M_a(t)V_{dc}(t) - \frac{1}{2}M_b(t)V_{dc}(t) + M_c(t)V_{dc}(t)}{3} \end{cases} \tag{7.20}$$

where $M_a(t)$, $M_b(t)$ and $M_c(t)$ are the modulation index of phase a, b and c respectively. It is obvious that equation (7.20) does not contain any dc component injection in the output terminal of a rear-end 5L-MFCI topology. By expanding the modulation index in equation (7.20), fundamental magnitude phase voltage in the RC network is appeared



(a) (b)

Fig. 7.6 Harmonic spectrum of the output RC phase voltage of terminal a.

at the output terminal of 5L-MFCI. Both Analytical and simulated results shows the fundamental component of the RC phase voltage, which is shown in Fig. 7.6.

If the phase voltage of equation (7.20) does not contain any dc component injection, then the load current will not produce large magnitude dc component current. Hence, the average current of the dc capacitors clamped in this topology is assumed to be zero during steady-state condition. The average current through the dc capacitors is expressed as

$$\begin{bmatrix} I_{cs1}(t) \\ I_{cs2}(t) \\ I_{cs3}(t) \end{bmatrix}_{avg} = \frac{1}{T}\sum_{n=1}^{\delta} \begin{bmatrix} \left(S_{s1,n}(t) - S_{s2,n}(t)\right) \\ \left(S_{s2,n}(t) - S_{s3,n}(t)\right) \\ \left(S_{s3,n}(t) - S_{s4,n}(t)\right) \end{bmatrix} I_{s,n} t \approx 0 \qquad (7.21)$$

Since the average capacitor current is assumed to be zero, the voltage variation across each capacitor is approximately equal to zero. Therefore, one can conclude that the voltage balancing of each capacitor is at stable condition.

$$\begin{bmatrix} \frac{\partial V_{Cs1}(t)}{\partial t} \\ \frac{\partial V_{Cs2}(t)}{\partial t} \\ \frac{\partial V_{Cs3}(t)}{\partial t} \end{bmatrix} = \begin{bmatrix} \frac{\left(I_{Cs1}(t)\right)_{avg}}{C_{s1}} \\ \frac{\left(I_{Cs2}(t)\right)_{avg}}{C_{s2}} \\ \frac{\left(I_{Cs3}(t)\right)_{avg}}{C_{s3}} \end{bmatrix} \approx 0 \qquad (7.22)$$

7.3 Controller Design

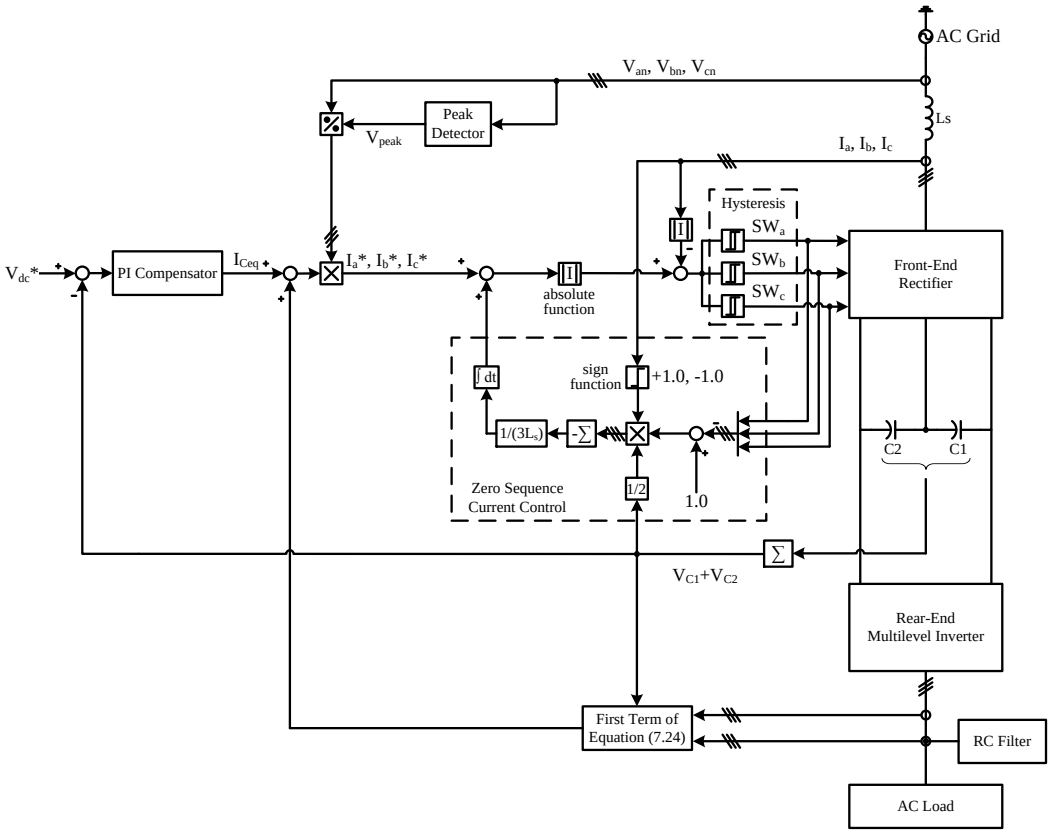


Fig. 7.7 A decouple current control with instantaneous power balanced control strategy based on fix hysteresis band algorithm for the front-end rectifier.

The controllers for both front-end rectifiers of the AC/DC/AC drives are implemented with the power balance control strategy based on hysteresis current control as illustrated in Fig. 7.7. The operating principle of this controller is similar to the presented controller in chapter 3, except the load current estimation of this controller is obtained from the ac side of the rear-end multilevel inverters. The power balance equation of the rear-end multilevel inverter is written as

$$V_{dc}(t)I_{dc}(t)=\sum V_{sm\langle inverter\rangle}(t)I_{s\langle inverter\rangle}(t)+C_{eq}V_{dc}(t)\frac{dV_{dc}(t)}{dt} \qquad (7.23)$$

From equation (7.23), the reference magnitude current for the inner current loop is,

$$I_{dc}^{*}(t) = I_{ac\langle inverter\rangle}(t) + I_{Ceq}(t) = \frac{\sum V_{sm\langle inverter\rangle}(t) I_{s\langle inverter\rangle}(t)}{V_{dc}(t)} + C_{eq}\frac{dV_{dc}(t)}{dt} \quad (7.24)$$

$V_{sm<inverter>}(t)$ is the phase voltage of the RC filter and $I_{s<inverter>}(t)$ is the line current of the rear-end multilevel inverter, where s is referred to phase a, b and c.

Thus, the final expression of the ac reference current with the injected zero sequence current as presented in chapter 3 with the estimated rear-end inverter current in equation (7.24) is written as

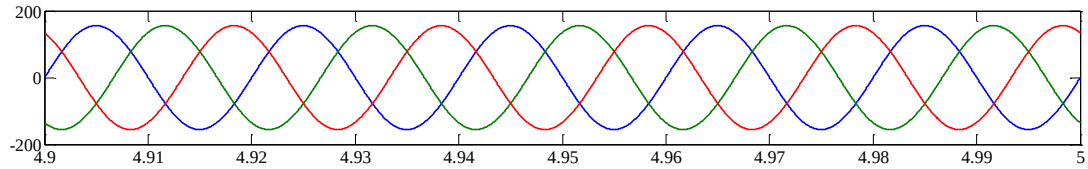
$$\begin{cases} I_a^{*}(t) = I_{dc}^{*}(t)\sin_a \text{ reference} + I_o(t) \\ I_b^{*}(t) = I_{dc}^{*}(t)\sin_b \text{ reference} + I_o(t) \\ I_c^{*}(t) = I_{dc}^{*}(t)\sin_c \text{ reference} + I_o(t) \end{cases} \quad (7.25)$$

Since the dc-link voltage is regulated by the front-end side, an open loop control of the rear-end multilevel inverters will be used for the comparison of both 5L-MDCI and 5L-MFCI topologies performance. The modulation index of both rear-end multilevel inverters will be set at 0.9.

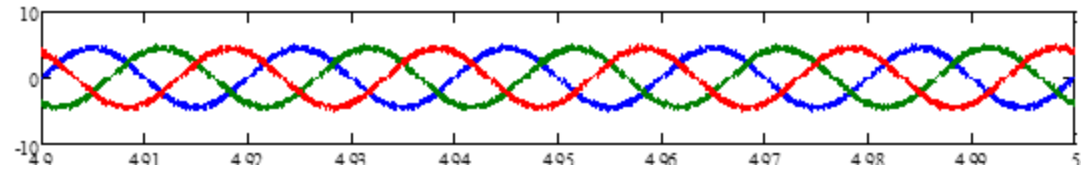
7.4 Simulation Results

The results of the front-end rectifier were presented with hysteresis current controller for unity power factor control with the fixed hysteresis band of 0.2A. All results are co-simulated between MATLAB/ Simulink® and PSIM Simcouple. The switching frequency of both the multilevel inverter configurations is set to 3 kHz.

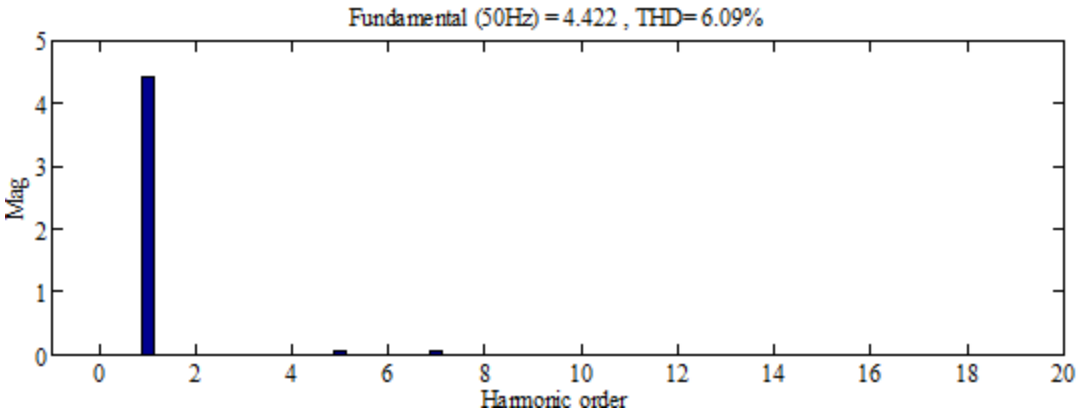
AC/DC/AC drive constructed with rear-end five-level diode-clamped inverter:



(a)

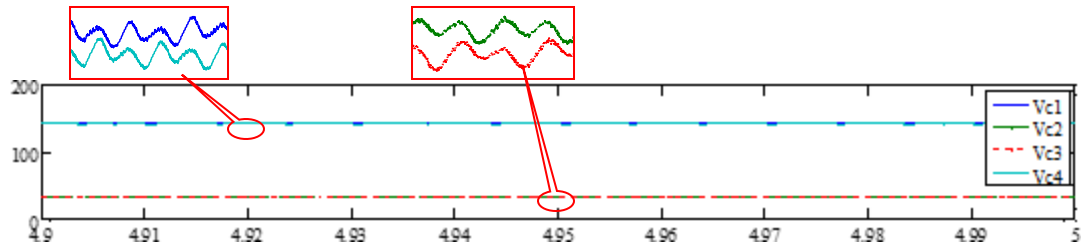


(b)

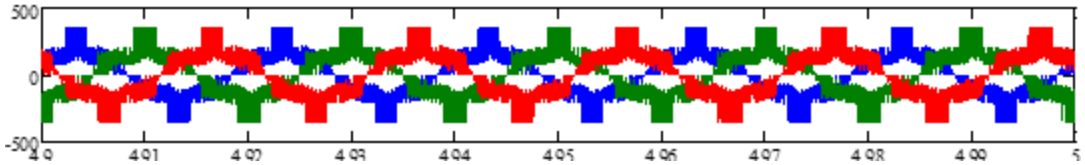


(c)

Fig. 7.8 Simulation results for a front-end rectifier based on rear-end 5L-MDCI topology. (a) Three-phase grid voltage, (b) three-phase grid current and (c) THD grid current of phase 'a'.



(a)



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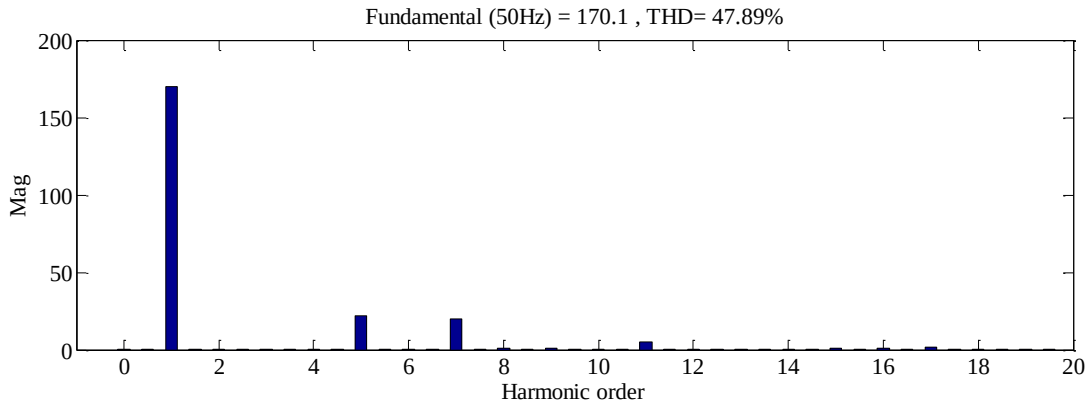
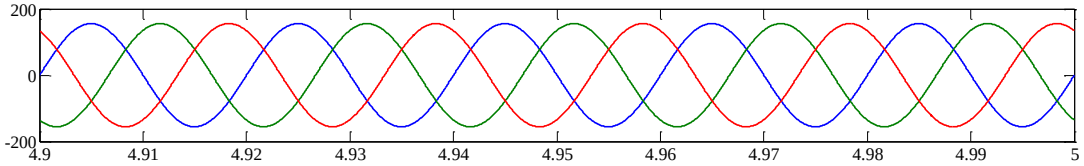


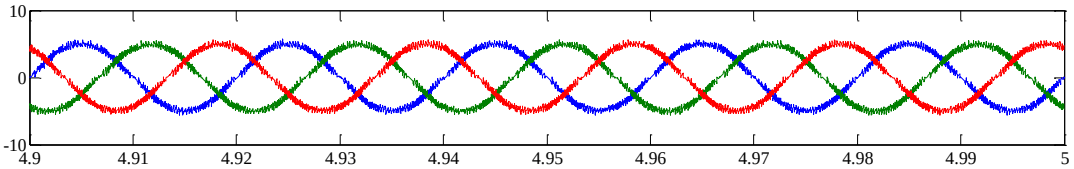
(c)

Fig. 7.9 Simulation results for rear-end 5L-MDCI topology. (a) DC-link voltage and voltage across each dc capacitor of phase 'a', (b) three-phase output line-to-line voltage and (c) THD output line-to-line voltage of phase 'a'.

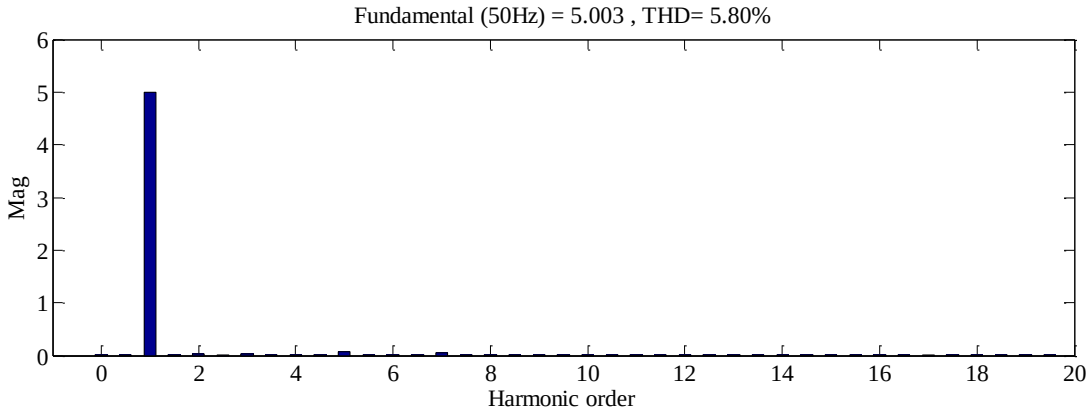
AC/DC/AC drive constructed with rear-end five-level flying capacitor inverter:



(a)

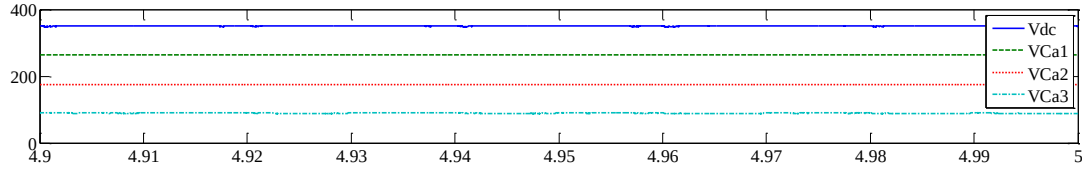


(b)

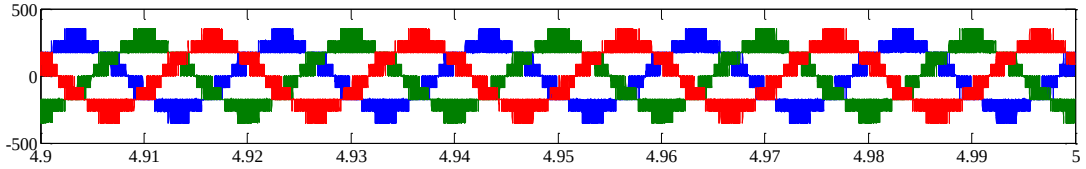


(c)

Fig. 7.10 Simulation results for a front-end rectifier based on rear-end 5L-MFCI topology. (a) Three-phase grid voltage, (b) three-phase grid current and (c) THD grid current of phase 'a'.



(a)



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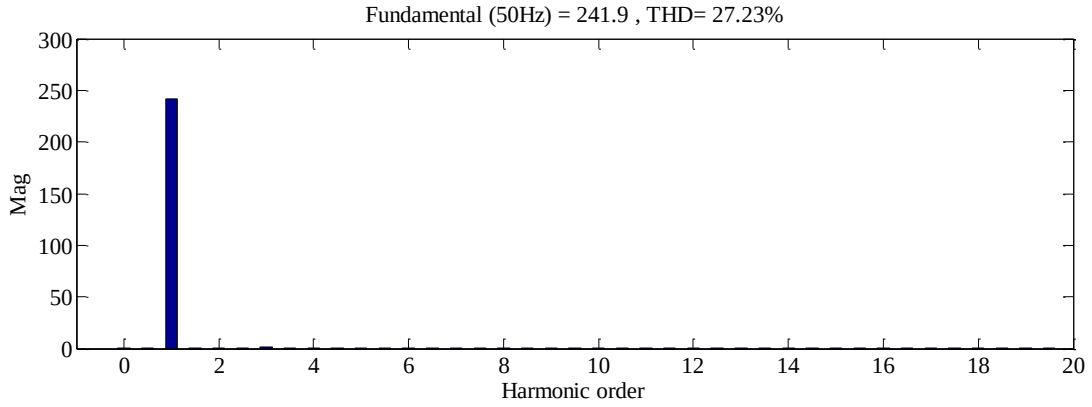


(c)

Fig. 7.11 Simulation results for rear-end 5L-MFCI topology. (a) DC-link voltage and voltage across each dc capacitor of phase 'a', (b) three-phase output line-to-line voltage and (c) THD output line-to-line voltage of phase 'a'

The performance comparison of AC/DC/AC drive constructed with both the 5L-MDCI and MFCI are done in this sub-section. Level-shifted PWM and phase-shifted PWM scheme are used to synthesis five-level output voltage for the rear-end 5L-MDCI topology and 5L-MFCI topology respectively. By comparing both topologies on AC/DC/AC drive with unbalance capacitor voltage in a single dc bus, results show that-rear-end 5L-MDCI topology has poorer performance as compared to 5L-MFCI topology. Although, a front-end rectifier with decoupling current control is able to distribute the voltages equally, four capacitors connected in series for 5L-MDCI topology will still yield to unbalance state. This is due to the inner two capacitors voltage are tend to decay nearly to zero value and lead to high THD quantity as shown in Fig. 7.9.

The front-end rectifier of the AC/DC/AC drive constructed with both the 5L-MDCI and MFCI topology gives a low harmonic current as shown in both Figs. 7.8(c) and 7.10(c). However, a rear-end 5L-MFCI topology with single dc bus has the self-balancing voltage properties, which makes this topology suitable for AC/DC/AC drive application with a reduced value of THD in voltage (Fig. 7.11). In addition, experimental results verify the performance results of both configurations in AC/DC/AC drive.

7.5 Experimental Results

The performance results of AC/DC/AC drive with both rear-end MDCI and MFCI topologies were tested experimentally using a 1.5kW laboratory prototype that is readily configured to work as either 5L-MDCI or 5L-MFCI. The front-end rectifier controller was implemented using a dSPACE RTI1103 development processor board under MATLAB Simulink Real-Time Workshop (RTW) provided by Math Works environment to generate the switching pattern from the hysteresis current regulator as presented in chapter 3. The four numbers of level shifted carrier waves are generated from a 3 kHz analog oscillator. The developed laboratory prototype is shown in Fig. 7.12 and detail parameters of the prototype are given as in Table 7.3.

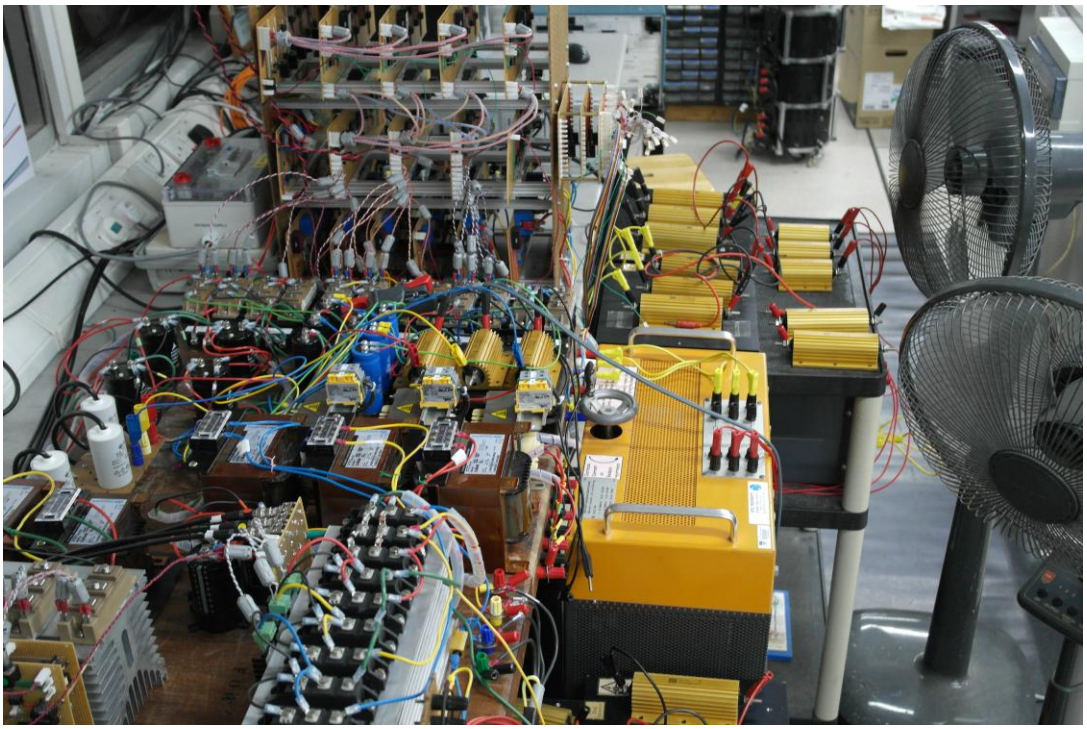
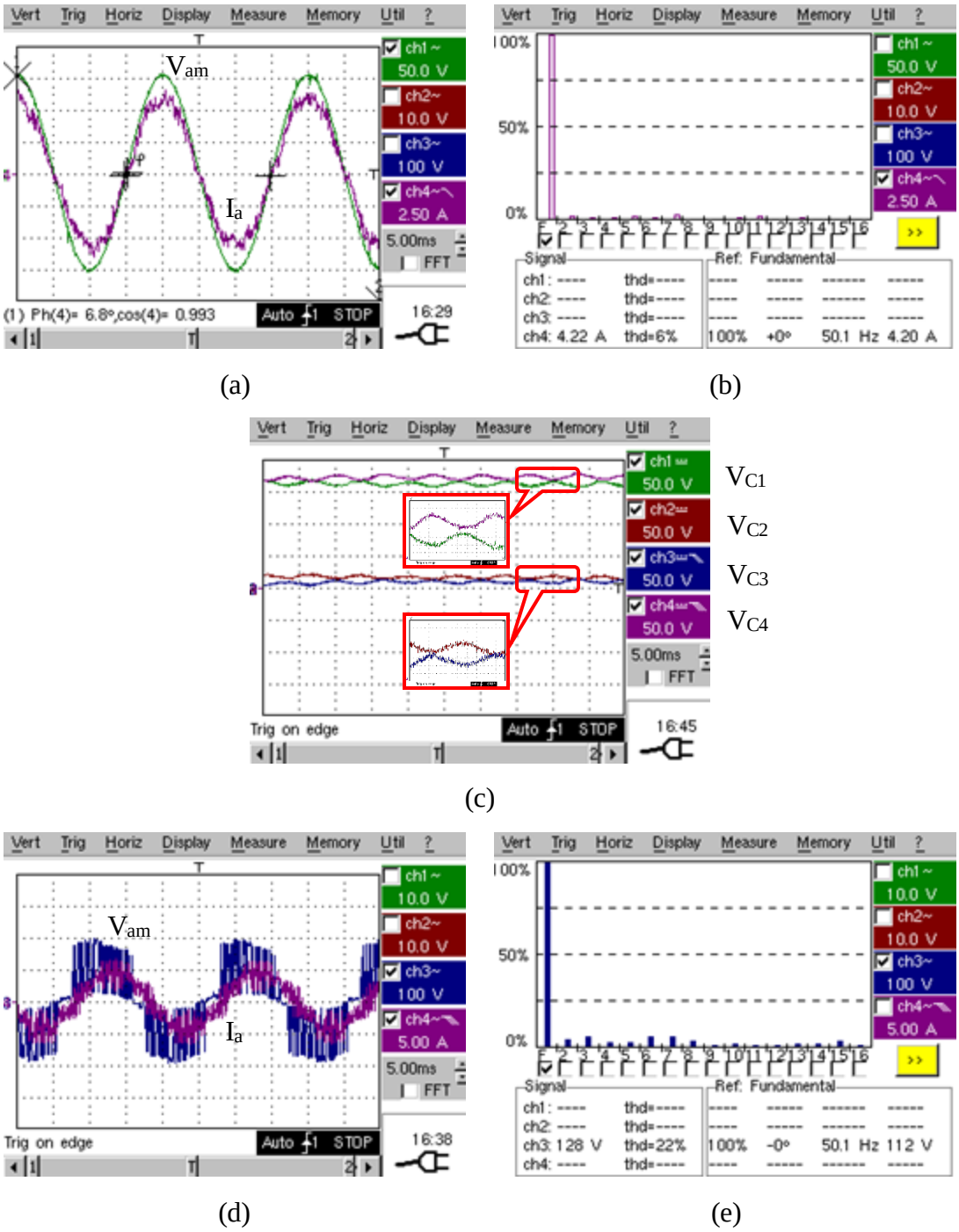


Fig. 7.12 Laboratory prototype for AC/DC/AC drive with resisteve-inductive load bank application.

TABLE 7.3

AC/DC/AC POWER DRIVE PARAMETERS FOR EXPERIMENTAL HARDWARE PROTOTYPE

AC/DC/AC Drive for 5L-MDCI		**AC/DC/AC Drive for 5L-MFCI**	
2MBI100TA-060	Inverter switch IGB S_{s1} to S_{s8}	2MBI100TA-060	Inverter switch IGB S_{s1} to S_{s8}
IRG4PH50UPbF	Bidirectional switch IGBT SW_a, SW_b and SW_c	IRG4PH50UPbF	Bidirectional switch IGBT SW_a, SW_b and SW_c
IXYS MDD26	Diode rectifier D_1 to D_6	IXYS MDD26	Diode rectifier D_1 to D_6
BYT200PIV	Bidirectional diode D_{s+} to D_{s-}	BYT200PIV	Bidirectional diode D_{s+} to D_{s-}
AC choke inductor	L_a, L_b and L_c 5mH	AC choke inductor	L_a, L_b and L_c 5mH
DC-link capacitor	C1 to C4 1500µF	DC-link capacitor	C1 to C2 1500µF
VS-VSKD56/12	Diode clamp D_{s1} to D_{s6}	Capacitor clamp	C_{s1} 560µF C_{s2} 470µF C_{s3} 330µF



(a) (b)

(c)

(d) (e)

Fig. 7.13 Experimental results obtained from AC/DC/AC drive constructed with 5L-MDCI topology. (a) Per-phase grid voltage and current with 50V/div and 2.5A/div of a front-end rectifier, (b) total harmonic distortion of the grid current of a front-end rectifier, (c) capacitors voltage in dc bus, (d) Output line-to-line voltage V_{ab} and load current I_a with 100V/div and 5A/div of a rear-end 5L-MDCI, and (e) total harmonic distortion of the line-to-line voltage V_{ab} of a rear-end 5L-MDCI.

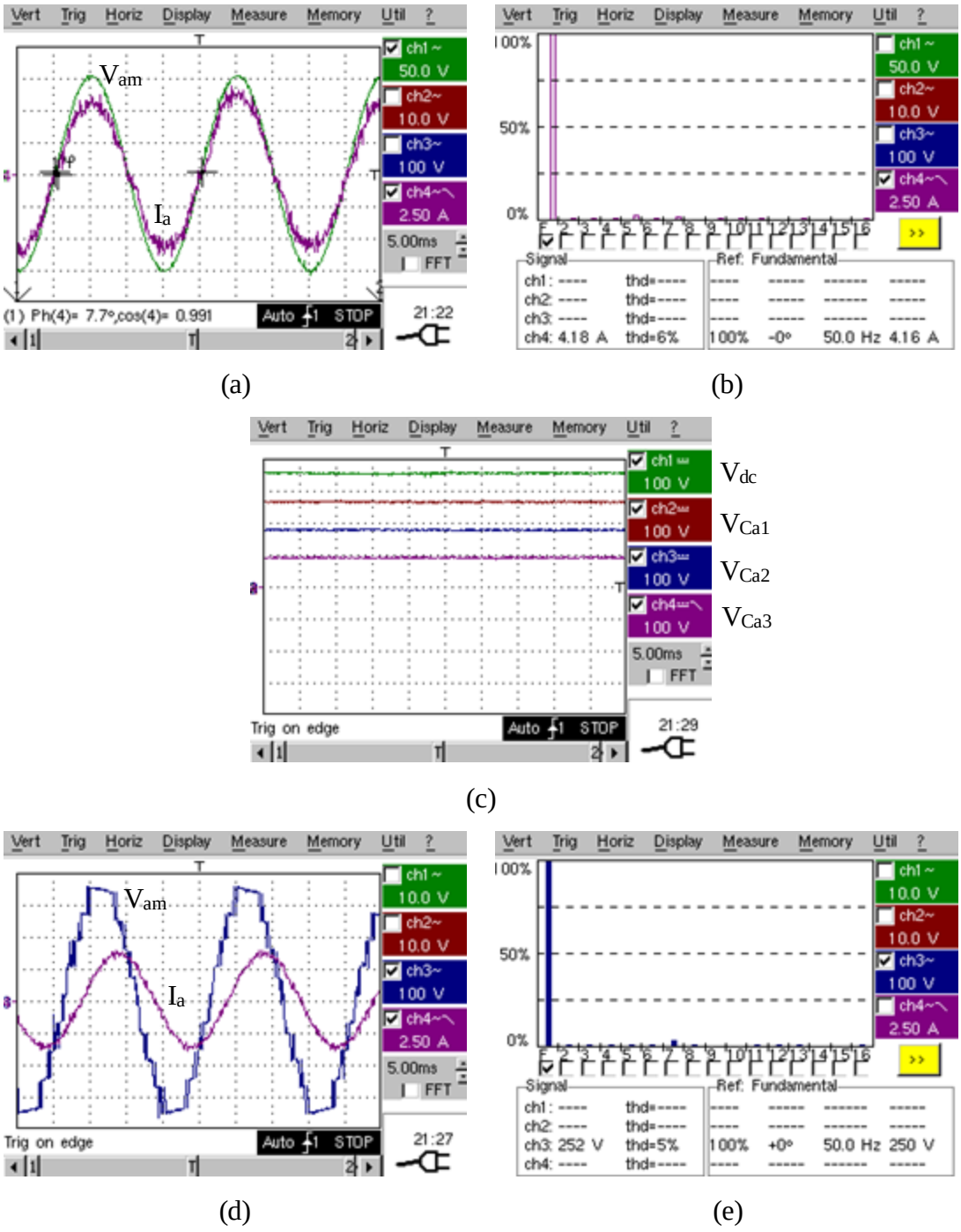
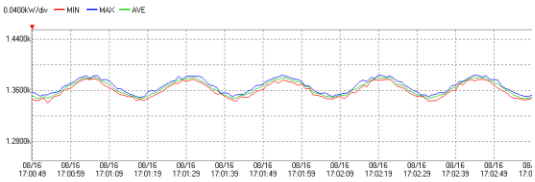


Fig. 7.14 Experimental results obtained from AC/DC/AC drive constructed with 5L-MFCI topology. (a) Per-phase grid voltage and current with 50V/div and 5A/div of a front-end rectifier, (b) total harmonic distortion of the grid current of a front-end rectifier, (c) DC-link voltage and capacitors clamped voltage, (d) Output line-to-line voltage V_{ab} and load current I_a with 100V/div and 5A/div of a rear-end 5L-MFCI, and (e) total harmonic distortion of the line-to-line voltage V_{ab} of a rear-end 5L-MFCI.

The experimental results in Fig. 7.13(e) and 7.14(e), confirm that the AC/DC/AC drive with a rear-end 5L-MFCI topology has low output line-to-line voltage distortion. But the rear-end 5L-MDCI topology has a poor quality as it contains high harmonic content, and gives a two-level output voltage which depends on the output power as shown in Fig. 7.13(d),. The distorted output line-to-line voltage in Fig. 7.13(d) is mainly caused by the poor voltage balancing in the dc bus as shown in Fig. 7.13(c). As discussed in the previous chapters 3 and 5, the impact of unbalanced capacitor voltage in the dc bus can be analyzed in various viewpoints. Firstly, front-end rectifier with the star-connected bidirectional switches does not provide zero neutral point current. Secondly, series connected dc capacitor in the dc bus will lead to unequal amount of charge and discharge current flow. This will cause some floating dc offset voltage across each capacitor as explained earlier. Thirdly, high injection of dc component in the inner two dc capacitors will lead to unbalance state during the switching transition. Finally, in practice due to unforced manufacturing errors all the passive elements of equal value do not have identical internal parameters. Hence, rear-end 5L-MDCI topology has to be installed with a precise voltage balancing circuit to achieve better output voltage waveform. However, 5L-MFCI topology appears to have a better balanced and stable dc voltage across each capacitor, as shown in Fig. 7.14(c). This is mainly because of the rear-end 5L-MFCI topology not being directly clamped to the neutral-point of the series connected capacitor in the dc bus. Moreover, RC filter with the star connected configuration provides good distribution of voltage level across each floating capacitor as presented in sub-section 7.2.2. Hence, one can conclude that, self-balanced voltage across each capacitor in rear-end 5L-MFCI topology depends on the net dc-link voltage provided by the unity power factor front-end rectifier. Rear-end 5L-MFCI topology does not contain any even harmonic components in output line-to-line and pole voltage as compared to rear-end 5L-MDCI topology and this fact is evident in Fig. 7.13(e) and 7.14(e).

To determine the efficiency of both rear-end multilevel inverter configurations in AC/DC/AC drive a HIOKI 3196 power quality analyzer is used. The input power is measured before the input filter inductors (L_{fa}, L_{fb} and L_{fc}) and output power is measured after the RC filter balancing circuit. The efficiency measurement results are obtained from a relatively low power prototype of the AC/DC/AC drives.

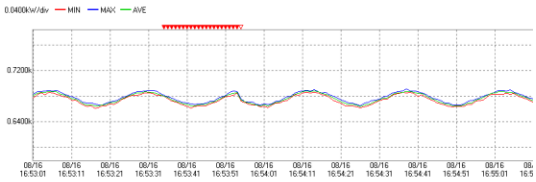
Input Power of a Front-End 3L-Rectifier



TIME PLOT - RMS P, sum

		MIN	MAX	AVE
A	08/16 17:00:49	1.3460k	1.3569k	1.3522k
B	08/16 17:00:49	1.3460k	1.3569k	1.3522k
	00:00:01	0.0000k	0.0000k	0.0000k
	MAX values			
	AVE values			
	MIN values			

Output Power of a Rear-End 5L-MDCI

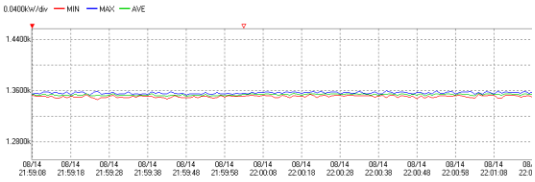


TIME PLOT - RMS P, sum

		MIN	MAX	AVE
A	08/16 16:53:01	0.6771k	0.6833k	0.6807k
B	08/16 16:53:01	0.6771k	0.6833k	0.6807k
	00:00:01	0.0000k	0.0000k	0.0000k
	MAX values			
	AVE values			
	MIN values			

(a)

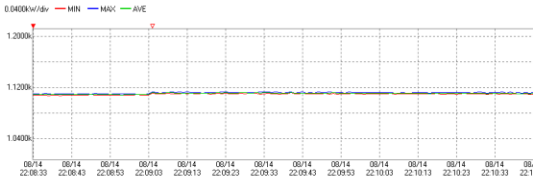
Input Power of a Front-End 3L-Rectifier



TIME PLOT - RMS P, sum

		MIN	MAX	AVE
A	08/14 21:59:08	1.3524k	1.3549k	1.3536k
B	08/14 21:59:08	1.3524k	1.3549k	1.3536k
	00:00:01	0.0000k	0.0000k	0.0000k
	MAX values			
	AVE values			
	MIN values			

Output Power of a Rear-End 5L-MFCI



TIME PLOT - RMS P, sum

		MIN	MAX	AVE
A	08/14 22:08:33	1.1079k	1.1094k	1.1089k
B	08/14 22:08:33	1.1079k	1.1094k	1.1089k
	00:00:01	0.0000k	0.0000k	0.0000k
	MAX values			
	AVE values			
	MIN values			

(b)

Fig. 7.15 Experimental results of input and output power of AC/DC/AC drives with the respective rear-end multilevel inverter configuration. (a) Rear-end 5L-MDCI, and (b) rear-end 5L-MFCI.

The input and output power measurements of both the AC/DC/AC drives constructed with rear-end 5L-MDCI and 5L-MFCI configurations are shown in the Fig. 7.15(a) and 7.15(b) respectively. In Fig. 7.15(a), it is obvious that both the input and output power of the AC/DC/AC drive consist of high harmonic component and large ripple power. This high harmonic power oscillation and large ripple power is mainly because of the high voltage distortion in the rear-end 5L-MDCI topology, which is due to unbalance capacitors voltage in the dc bus. The voltage and current quality of the output rear-end

TABLE 7.4

PERFORMANCE PARAMETERS COMPARISON

Configuration	Grid				Efficiency, η (%)
	Voltage, V_{am} (V_{rms})	Current, I_a (A_{rms}/phase)	THD I_a (%)	PF	
AC/DC/AC Drive for 5L-MDCI	110	3.5	6	0.993	50
AC/DC/AC Drive for 5L-MFCI	110	3.5	6	0.991	82

5L-MDCI topology is low, which results in low overall efficiency. Under extreme unbalance, rear-end 5L-MDCI topology requires a higher current rating to drive a 1.3kW load to meet the load power.

For the same input power, the efficiency of the rear-end 5L-MFCI topology is observed to be higher than the 5L-MDCI topology. AC/DC/AC drive with rear-end 5L-MFCI topology can achieve at least 82%, while a rear-end 5L-MDCI configuration has an optimum efficiency of 50%. This proves that unbalance in capacitor voltage does not provide the optimal power efficiency. And output voltage having low THD value will lead to high current density and thus high conduction loss in diodes of a rear-end 5L-MDCI topology. Therefore, rear-end 5L-MFCI topology has the advantage to overcome the limitation of unbalanced capacitor voltage in single dc bus architecture and hence yields better efficiency.

7.6 Discussion

The comparative study of the rear-end 5L-MDCI and 5L-MFCI topologies for the unbalance capacitor voltage in a single dc bus architecture design has been conducted in this chapter. Different voltage level inverters is used as a rear-end inverter with the

proposed front-end unity power rectifier. If a diode-clamped inverter is required to design for an AC/DC/AC drive, a three-level diode-clamped inverter is the preferred topology for this AC/DC/AC drive where the voltage balancing is done by using either dc offset modulation or RC filters balancing circuit as discussed in chapter 6.

For a given rear-end five-level inverter topologies in a single dc bus configuration, 5L-MFCI topology is implemented for high power application. According to the analytically and experimental results obtained, one can conclude that poor balancing of capacitor voltages in the dc bus may result in a low harmonic distortion of output voltage and lead to poor efficiency of the complete circuit. In conclusion, for a five-level inverter with a unity power factor front-end rectifier, the five-level flying capacitor inverter topology with the RC filter circuit is sure a winner, due to self-voltage balancing characteristics of the capacitor.

Chapter 8 – Transformerless Five-Level/Multiple-Pole Multilevel Inverters with Single DC Bus Configuration

In this chapter, a new concept of five-level (5L) inverter topology is presented. Numerous topologies on higher-level voltage source inverter have been detailed in Chapters 4 and 7. Reduction in utilization of number of components has been quite trending among researcher and industrial product developers around the globe [89]. In order to maintain a high operational efficiency it is necessary to develop multilevel converter with lower part count while achieving primary objectives such as low THD and lower EMI. The importance of reduction in part count has been discussed in Chapter 1 previously. The prices of the power electronic equipment are decreasing due to tremendous improvements in fabrication technologies and logistics. Only potential energy savings in power converters only would probe the customers and manufacturers to search for innovative converter designs. The key factors for achieving such optimization are low overall cost, high conversion efficiency and most importantly reduced utilization of semiconductor devices.

The focus of this chapter is to design a transformer less, low loss and a lightweight converter with lower device ratings. The proposed converter achieves significant

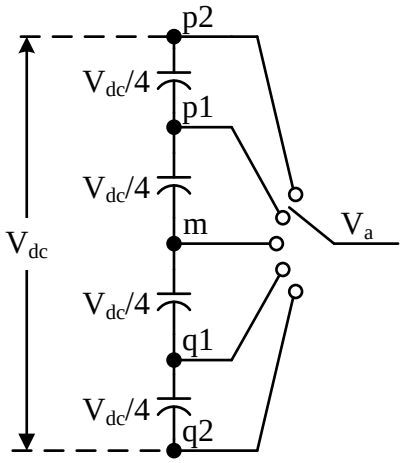


Fig. 8.1. Circuit diagram of per-phase leg single-pole existing 5L-MDCI topology with switching position.

reduction in components count and cost. The new multilevel inverter concept is based on the single-pole inverter (ref. to Fig. 8.1) of a MDCI (Chapter 4, subsection 4.2.3) topology. The topologies are developed based on the concept of multiple-pole hierarchy as shown in Fig. 8.2. This type of hierarchy utilizes lesser number of switching elements resulting in better efficiency while operating at a lower switching frequency for higher level incremental voltage stepped waveform.

As mentioned earlier in Chapter 7, the dc-link capacitor voltage of a five-level diode-clamped inverter is unbalanced. The total average current at each node of the dc-link capacitors connected in series is not equal to zero. Thus, a balancing circuit is incorporated to balance the capacitor voltage in order to achieve a balanced output voltage. The balancing circuit as well regulates equal voltage among the dc-link capacitors at the input of the 5L inverter.

The balancing circuit for the input distribution voltage level of the five-level inverter circuit was first proposed by Newton [90] and this type of configuration has been successfully installed in the motor drive application [34, 79, 91]. The following sections will present the proposed five-level inverter topologies with balancing circuits. A

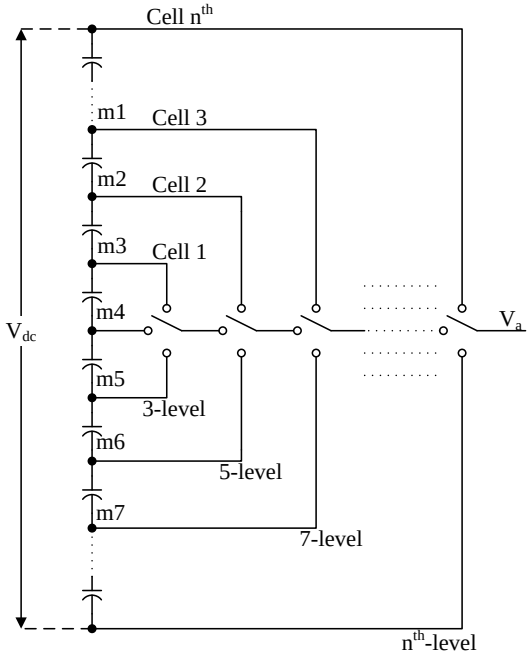


Fig. 8.2. Circuit diagram of per-phase leg multiple-pole nL-MDCI topology with switching position.

comparative study between the proposed and classical inverter is presented in the following subsection.

8.1 Five-Level Multiple-Pole Concept

The basic idea of this multiple-pole is based on a single-pole hierarchy by separating the pole into a parallel structure. Each pole is connected with its respective desired dc voltage value and each pole is operated at three-level incremental voltage stepped. A higher the voltage level is achieved as the number of poles increase as shown in Fig. 8.2.

8.2 Operating Principle of 5L-Inverter Topologies

Operating principle of the proposed 5L-inverters is presented in this section. The proposed topologies are classified as multiple-pole multilevel diode-clamped inverter (M^2DCI), multiple-pole multilevel t-type-clamped inverter (M^2T^2CI) and multiple-pole multilevel single-switch-clamped inverter (M^2S^2CI). The topological design aspects, output characteristics and power quality are proven to be on par with conventional MDCI configuration. The losses of the discrete components will be investigated later in this chapter and performance of the gate control for respective inverters will be verified through the laboratory prototype.

8.2.1 Five-Level/Multilevel Diode-Clamped Inverter (5L-MDCI)

The basic operation of 5L-MDCI topology with the switching scheme on LS-PWM is detailed in Chapter 7. The expression of both output voltage and current flow through the devices is obtained based on the following assumption. 1) Balance dc capacitors voltage in the dc-link, 2) no ripple voltage in each dc capacitors, and 3) parasitic passive elements are neglected. Based on the given assumption, the output voltage is expressed as

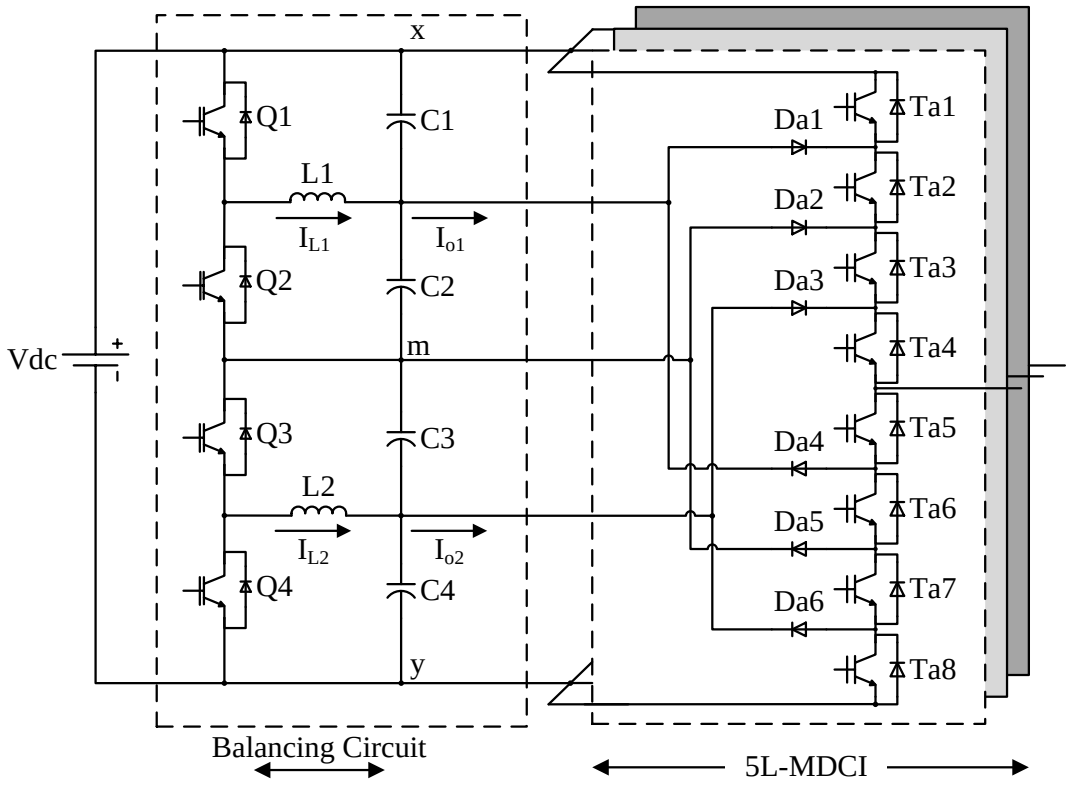


Fig. 8.3. Circuit diagram of the classical 5L-MDCI topology associated with the 5L-DC/DC balancing circuit.

$$V_{sm}(t)=\frac{V_{dc}(t)}{4}\left[T_{s1}(t)+T_{s2}(t)+T_{s3}(t)+T_{s4}(t)-2\right] \tag{8.1}$$

The instantaneous current through active switches with their respective operating angles for different modulation depths are listed in Table 8.1. The operating angle is determined by the commutation period for one cycle. For a topology requires a complementary switch to synthesize the voltage stepped waveform, the active components in the upper phase leg conduct only during the positive half cycle. While the lower phase leg devices conduct only during the negative half cycle. Since, upper phase leg devices and lower phase leg devices have the same current expression. The instantaneous current expression for the switches in upper half of the leg is listed in Table 8.1.

TABLE 8.1

INSTANTANEOUS PHASE 'A' CURRENT EXPRESSION OF 5L-MDCI WITH THE RESPECTIVE ANGLE OF THE OPERATING SYSTEM AND THE RANGE OF MODULATION DEPTH

Current	Equation	Operating Angle	Modulation
$I_{Da1}(t)$	$I_a(t)T_{a2}(t)\left[1-T_{a1}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Da2}(t)$	$I_a(t)T_{a3}(t)\left[1-T_{a2}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Da3}(t)$	$I_a(t)T_{a4}(t)\left[1-T_{a3}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Ta1}(t)$	$I_a(t)T_{a1}(t)$	$\sin^{-1}\frac{1}{2M_a} \le \omega t < \pi - \sin^{-1}\frac{1}{2M_a}$	$M_a \ge \frac{1}{2}$
$I_{Ta2}(t)$	$I_a(t)T_{a2}(t)$	$0 \le \omega t < \pi$	
$I_{Ta3}(t)$	$I_a(t)T_{a3}(t)$	$0 \le \omega t < \pi$	
$I_{Ta4}(t)$	$I_a(t)T_{a4}(t)$	$0 \le \omega t < \pi$	
$I_{Da1}(t)$	$I_a(t)T_{a2}(t)$	$0 \le \omega t < \pi$	
$I_{Da2}(t)$	$I_a(t)T_{a3}(t)\left[1-T_{a2}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Da3}(t)$	0	$0 \le \omega t < \pi$	
$I_{Ta1}(t)$	0	$0 \le \omega t < \pi$	$M_a < \frac{1}{2}$
$I_{Ta2}(t)$	$I_a(t)T_{a2}(t)$	$0 \le \omega t < \pi$	
$I_{Ta3}(t)$	$I_a(t)T_{a3}(t)$	$0 \le \omega t < \pi$	
$I_{Ta4}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	

Note: Ia(t) is the phase 'a' output current of the inverter, which consists of power factor angle between the load and pole voltage. As the switches in upper and lower leg have similar operating principle, the instantaneous current expression for currents through complementary switches is same.

8.2.2 Five-Level/Multiple-Pole Multilevel Diode-Clamped Inverter (5L-M^{2}DCI)

Fig. 8.4 shows the circuit diagram of the proposed 5L-M^{2}DCI topology. In order to operate a stable five-level output pole voltage waveform (i.e. V_{am} = -V_{dc}/2, -V_{dc}/4, 0, +V_{dc}/4, +V_{dc}/2), two cells/pole are connected in each phase. Each of the cells is configured based on the classical NPC/MDCI topology and a five-level/level-shifted PWM technique is used for generating required gating signals. The switching state of the corresponding output voltage level is shown in Table 8.2.

The inner cell switches (Ta1–Ta4) conduct only when the voltage level is operated at ±Vdc/4 and 0. By obtaining this switching condition, the middle two carrier based comparison is selected for the switching commutation. The output five level voltage stepped waveform is then finalized by the outer cell switches, where the first and last carrier comparison is selected for the outer cell switches. The switching scheme and switching state selection for the 5L-M^{2}DCI topology is shown in Fig. 8.5.

TABLE 8.2

5L-M^{2}DCI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	Switching States								Per-Phase Leg Voltage		
	T_{s1}	T_{s2}	T_{s3}	T_{s4}	T_{s5}	T_{s6}	T_{s7}	T_{s8}	V_{sx}	V_{sy}	V_{sm}
1	1	1	0	0	1	1	0	0	0	V_{dc}	V_{dc}/2
2	1	1	0	0	0	1	1	0	-V_{dc}/4	3V_{dc}/4	V_{dc}/4
3	0	1	1	0	0	1	1	0	-V_{dc}/2	V_{dc}/2	0
4	0	0	1	1	0	1	1	0	-3V_{dc}/4	V_{dc}/4	-V_{dc}/4
5	0	0	1	1	0	0	1	1	-V_{dc}	0	-V_{dc}/2

where ‘s’ represent phase a, b and c and S_{s1} to S_{s8} are IGBT switching devices for individual leg. Logic 1 represent as turn-on and logic 0 represent as turn-off for T_{s1}, T_{s2}, T_{s3} and T_{s4}.

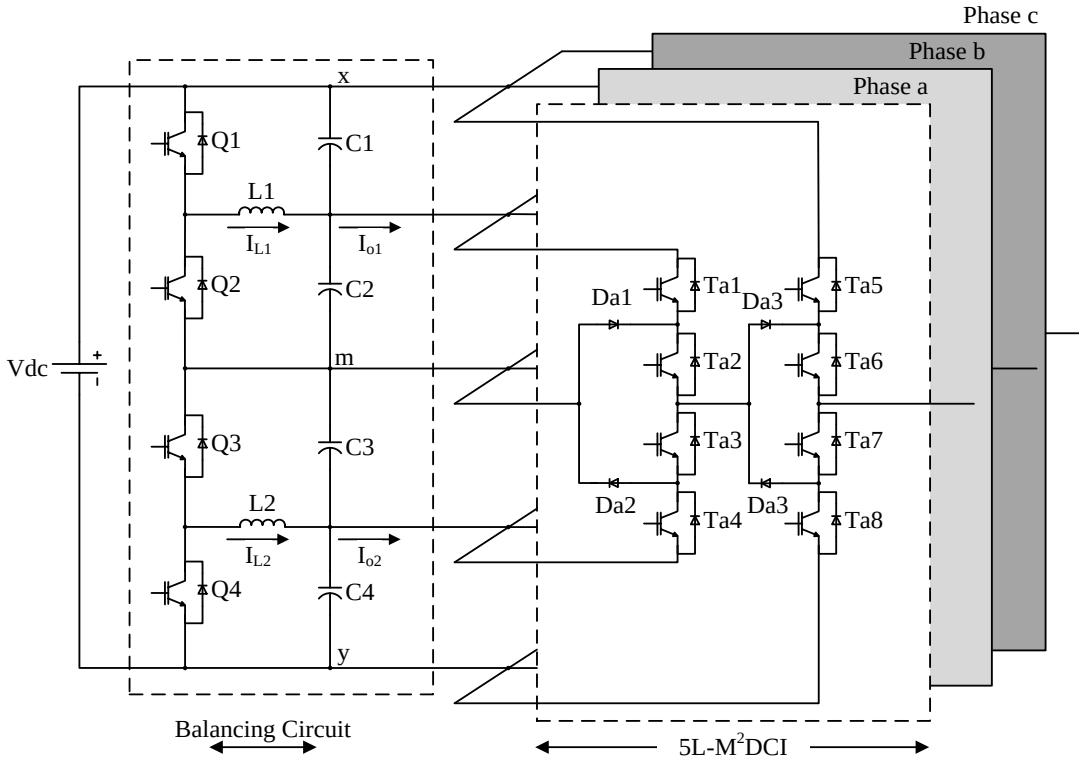


Fig. 8.4. Circuit diagram of the proposed 5L-M^{2}DCI topology associated with the 5L-DC/DC balancing circuit.

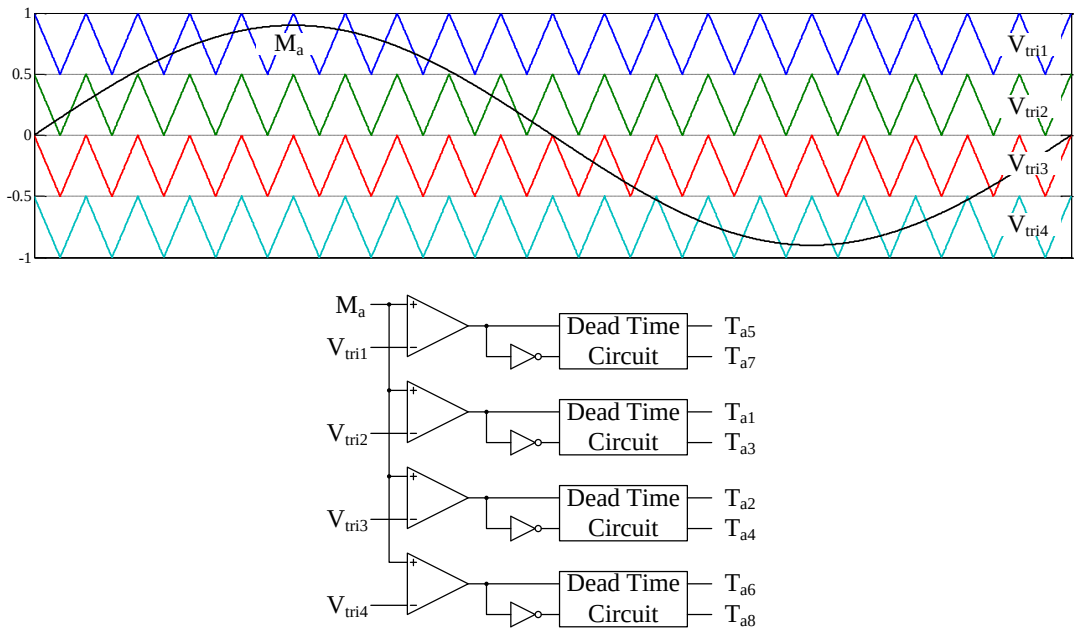


Fig. 8.5. Switching scheme based on LS-PWM strategy with the corresponding gating signal of phase 'a'.

TABLE 8.3

INSTANTANEOUS PHASE 'A' CURRENT EXPRESSION OF 5L-M^{2}DCI WITH THE RESPECTIVE ANGLE OF THE OPERATING SYSTEM AND THE RANGE OF MODULATION DEPTH

Current	Equation	Operating Angle	Modulation
$I_{Da1}(t)$	$I_a(t)T_{a2}(t)\left[1-T_{a1}(t)\right]\left[1-T_{a5}(t)\right]$	$0 \le \omega t < \pi$	$M_a \ge \frac{1}{2}$
$I_{Da3}(t)$	$I_a(t)\left[1-T_{a5}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Ta1}(t)$	$I_a(t)T_{a1}(t)\left[1-T_{a5}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Ta2}(t)$	$I_a(t)T_{a2}(t)\left[1-T_{a5}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Ta5}(t)$	$I_a(t)T_{a5}(t)$	$\sin^{-1}\frac{1}{2M_a} \le \omega t < \pi - \sin^{-1}\frac{1}{2M_a}$	
$I_{Ta6}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	
$I_{Da1}(t)$	$I_a(t)\left[1-T_{a1}(t)\right]$	$0 \le \omega t < \pi$	$M_a < \frac{1}{2}$
$I_{Da3}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	
$I_{Ta1}(t)$	$I_a(t)T_{a1}(t)$	$0 \le \omega t < \pi$	
$I_{Ta2}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	
$I_{Ta5}(t)$	0	$0 \le \omega t < \pi$	
$I_{Ta6}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	

Note: Ia(t) is the phase 'a' output current of the inverter, which consists of power factor angle between the load and pole voltage. While the principle of operating instantaneous current expression for each complementary switch is similar to the upper phase leg switches.

According to the level-shifted PWM technique, the output pole-voltage expression for amplitude modulation greater than 0.5, under the balance capacitor voltage condition is written as:

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t) + T_{s2}(t) + T_{s5}(t) + T_{s6}(t) - 2\right] \tag{8.1}$$

For amplitude modulation less than 0.5, where the modulation wave is fall within two center carrier waves. The output pole voltage is expressed as:

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t) + T_{s2}(t) - 1\right] \tag{8.2}$$

From equations (8.1) and (8.2), it is noted that the modulation indices determine the synthesis of output pole-voltage levels and selection of particular switching states. The expression of the output pole-voltage for the five-level voltage source inverter with LS-PWM is given by equation (8.1) which is similar to (7.10).

The current flow through the switches is determined by the power factor angle between the output pole voltage and current of the inverter with the dependent modulation depth of the switching state selection at positive half cycle. Expressions of the current flow through the switches are given in Table 8.3.

8.2.3 Five-Level/Multiple-Pole Multilevel T-Type-Clamped Inverter (5L-M^{2}T^{2}CI)

The schematic of multiple-pole multilevel T-type-clamped inverter topology (M^{2}T^{2}CI) is shown in Fig. 8.6. The T-type-clamped concept is derived according to the direction of the current flow of the diode-clamped inverter as shown in Fig. 8.9 with the corresponding switching states commutation. According to the switching states in Table 8.2, the current through the center switch (Ta2-Ta3 and Ta6-Ta7) is bidirectional and is illustrated in Fig. 8.6. The bidirectional switching scheme is observed by the transition of switching states (1 1) ↔ (0 1) ↔ (0 0) of the upper two switches. The transition involves cumulating of NPC topology and T-clamped inverter into a multiple-pole approach to form a five-level output voltage stepped waveform operation.

The switching states of five-level output voltage stepped waveform are shown in Table 8.4 with the corresponding switching commutation. In order to perform the desired

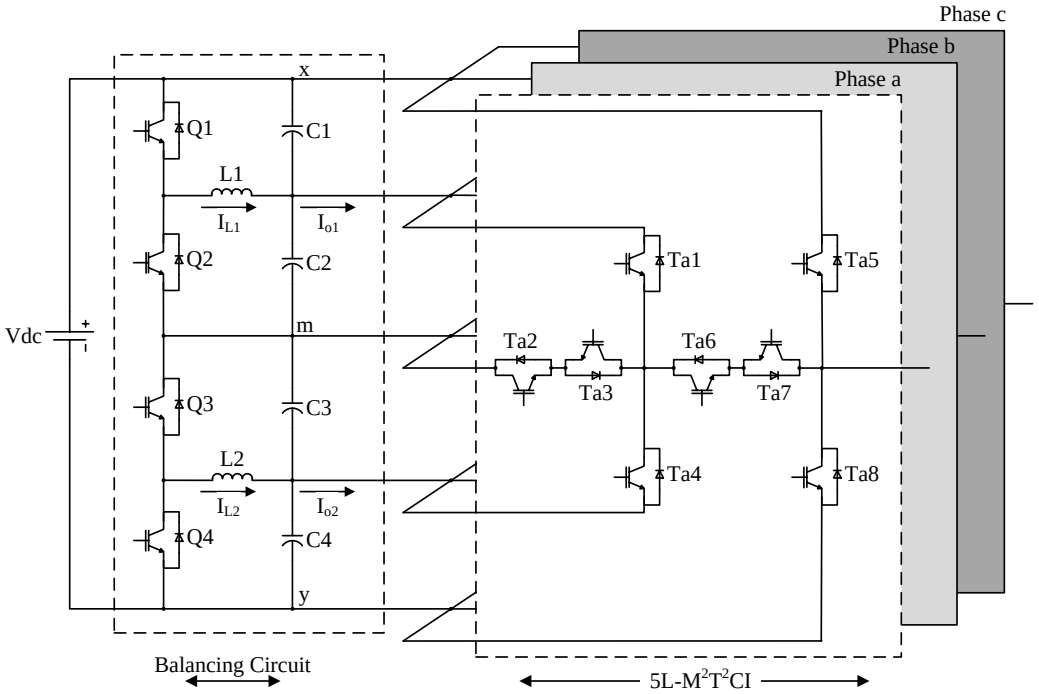


Fig. 8.6. Circuit diagram of the proposed 5L-M²T²CI topology associated with the 5L-DC/DC balancing circuit.

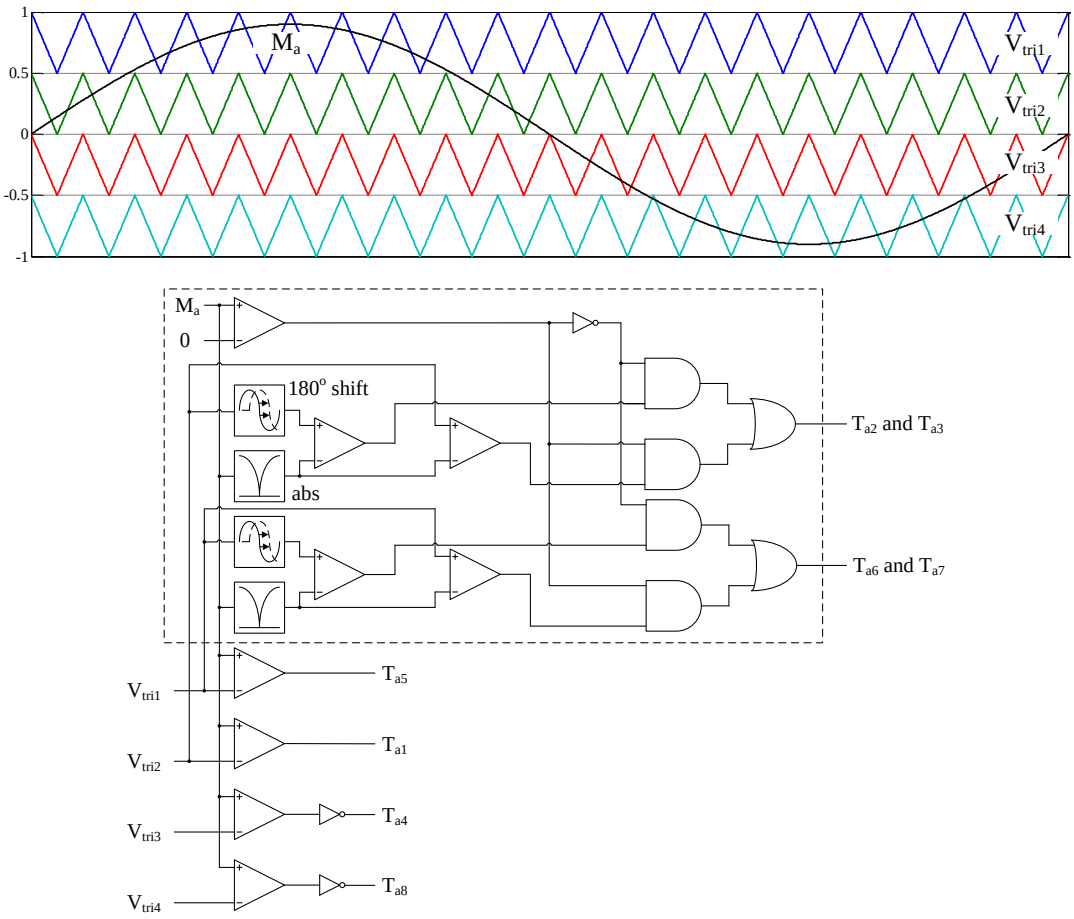


Fig. 8.7. Proposed six carriers switching scheme based on LS-PWM strategy with the corresponding gating signal of phase 'a'.

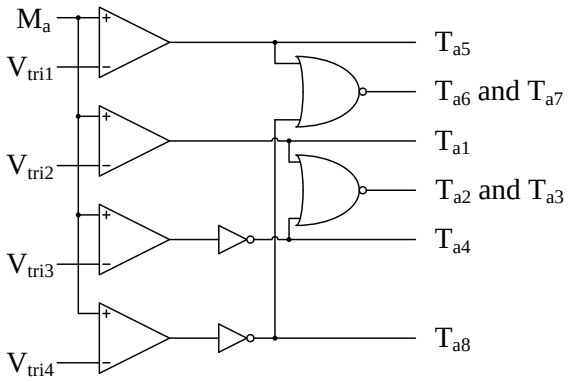


Fig. 8.8. Proposed modify four carriers switching scheme based on LS-PWM strategy with the corresponding gating signal of phase 'a'.

output voltage level with the corresponding switching states as listed in Table 8.4, simple logic gates circuitry is developed to control two series switches connected in between the node of each phase and center point of the dc-link. The control gate circuitry for the 5L-M^2T^2CI topology is shown in Fig. 8.7.

In Fig. 8.7, the control signals of two switches connected in series is obtained from indirect carrier based comparison. The bidirectional switches for (Ta2, Ta3) and (Ta6, Ta7) are generated by comparing the absolute function of the modulation reference signals with four upper carriers wave (Vtri1, Vtri2, 180° phase shifted of Vtri1 and Vtri2) to achieve the desired switching states.

However, the development of this control unit as indicated in the dotted box as shown in Fig. 8.7 is more complex and costly for the hardware development, as well as requires higher computation time for digital control. Thus, Fig. 8.8 shows the modification of the control gating circuit to achieve the same switching states pattern in Table 8.4.

According to the switching states selection based on the LS-PWM technique, the output pole voltage of 5L-M^2T^2CI under high modulation for more than half amplitude is expressed as

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t) - T_{s4}(t) + T_{s5}(t) - T_{s8}(t)\right] \tag{8.3}$$

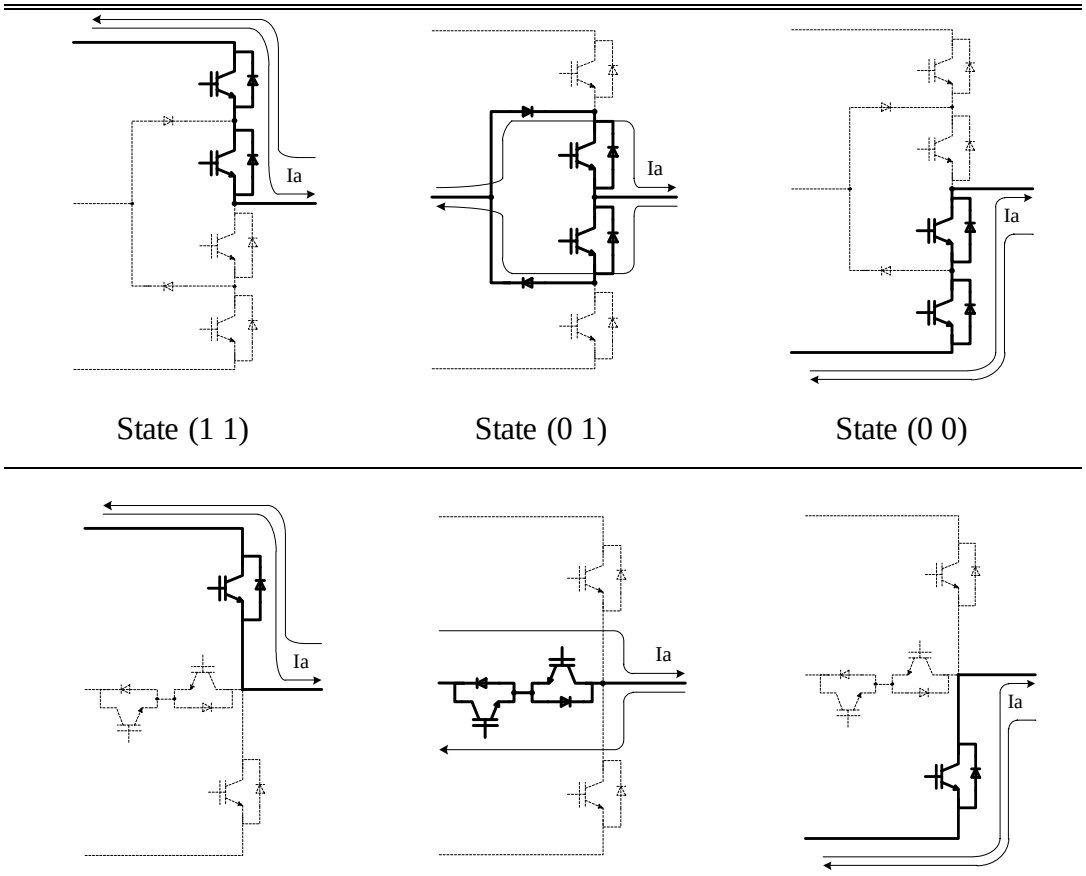


Fig. 8.9. Derivation of bidirectional currents flow of the t-type-clamped switches based on the switching states transition of the NPC topology.

TABLE 8.4

5L-M^2T^2CI VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	**Switching States**								**Per-Phase Leg Voltage**		
	T_{s1}	T_{s2}	T_{s3}	T_{s4}	T_{s5}	T_{s6}	T_{s7}	T_{s8}	V_{sx}	V_{sy}	V_{sm}
1	1	0	0	0	1	0	0	0	0	V_{dc}	$V_{dc}/2$
2	1	0	0	0	0	1	1	0	$-V_{dc}/4$	$3V_{dc}/4$	$V_{dc}/4$
3	0	1	1	0	0	1	1	0	$-V_{dc}/2$	$V_{dc}/2$	0
4	0	0	0	1	0	1	1	0	$-3V_{dc}/4$	$V_{dc}/4$	$-V_{dc}/4$
5	0	0	0	1	0	0	0	1	$-V_{dc}$	0	$-V_{dc}/2$

Where s represent phase a, b and c and S_{s1} to S_{s8} are presented as the IGBT switching devices for individual leg. Logic 1 represent as turn on and logic 0 represent as turn off for T_{s1}, T_{s2}, T_{s3} and T_{s4}

TABLE 8.5

INSTANTANEOUS PHASE 'A' CURRENT EXPRESSION OF 5L-M^2T^2CI WITH THE RESPECTIVE ANGLE OF THE OPERATING SYSTEM AND THE RANGE OF MODULATION DEPTH

Current	Equation	Operating Angle	Modulation
$I_{Ta1}(t)$	$I_a(t)\left[T_{a1}(t)-T_{a5}(t)\right]$	$0 \le \omega t < \pi$	$M_a \ge \frac{1}{2}$
$I_{Ta2}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a4}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta4}(t)$	$I_a(t)\left[T_{a4}(t)-T_{a8}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Ta5}(t)$	$I_a(t)T_{a5}(t)$	$\sin^{-1}\frac{1}{2M_a} \le \omega t < \pi - \sin^{-1}\frac{1}{2M_a}$	
$I_{Ta6}(t)$	$I_a(t)\left[1-T_{a5}(t)-T_{a8}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta8}(t)$	$I_a(t)T_{a8}(t)$	$\pi + \sin^{-1}\frac{1}{2M_a} \le \omega t < 2\pi - \sin^{-1}\frac{1}{2M_a}$	
$I_{Ta1}(t)$	$I_a(t)T_{a1}(t)$	$0 \le \omega t < \pi$	$M_a < \frac{1}{2}$
$I_{Ta2}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a4}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta4}(t)$	$I_a(t)\left[T_{a4}(t)-T_{a8}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Ta5}(t)$	0	$0 \le \omega t < 2\pi$	
$I_{Ta6}(t)$	$I_a(t)$	$0 \le \omega t < 2\pi$	
$I_{Ta8}(t)$	0	$0 \le \omega t < 2\pi$	

For amplitude modulation lower than 0.5, the output pole voltage is written as:

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t)-T_{s4}(t)\right] \tag{8.4}$$

Similarly, the current expressions for switches are determined by the switching function with the range of the modulation depth. The expression of the current through the switch is finalized in Table 8.5 based on one cycle of the commutation period.

According to Table 8.5, voltage quality of a 5L-M^2T^2CI is poor at low modulation index for M < 0.5. Poor output voltage quality will lead to three-level output pole voltage operation and this increases the common-mode voltage level when a motor is loaded. Three-level output pole voltage stepped waveform due to low modulation is operated at the inner cell inverter and clamping power device of the output terminal of the inner cell inverter is operated at continuous mode. However, a low modulation indices operation is a rare occurrence in most of the applications. However, a momentary period of high modulation indices will occur during the motor start up. Therefore, low modulation indices will not be the primary focus for this work. Similarly, poor quality of the classical MDCI and proposed M^2DCI topology during low modulation index for LS-PWM technique.

8.2.4 Five-Level/Multiple-Pole Multilevel Single-Switch-Clamped Inverter (5L-M^2S^2CI)

Fig. 8.10 shows a five-level/multiple-pole multilevel single-switch-clamped inverter (5L-M^2S^2CI) topology. The structure of this topology is configured based on the bidirectional switch, which allows bidirectional flow of current. Since 5L-M^2T^2CI is sharing the same gating signal for two switches connected in series to form bidirectional current flow. Then, a simple structure of single switch bidirectional current flow is implemented by incorporating with the diode bridge circuit as shown in Fig. 8.11. Similarly, the same gating logic circuit is used, as shown in Fig. 8.12. The output pole-voltage of this topology under high modulation depth is expressed as

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t) - T_{s3}(t) + T_{s4}(t) - T_{s6}(t)\right] \tag{8.5}$$

where the output pole voltage of the inverter for low modulation depth is written as

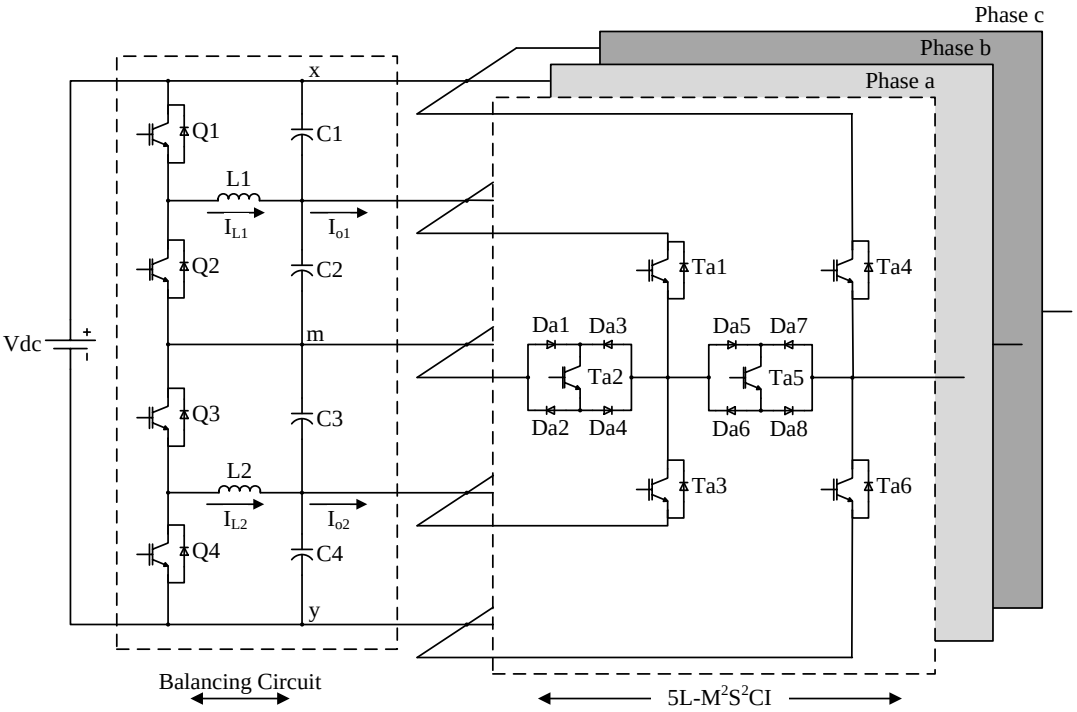


Fig. 8.10. Circuit diagram of the proposed 5L-M^{2}S^{2}CI topology associated with the 5L-DC/DC balancing circuit.

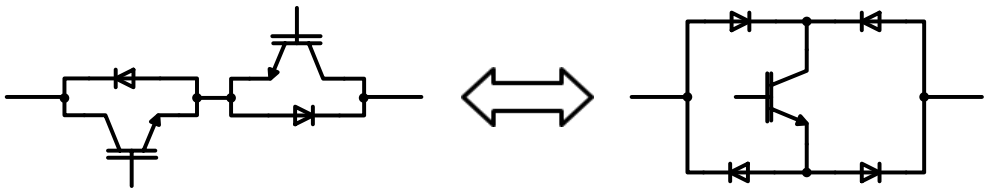


Fig. 8.11. Alternative bidirectional switch.

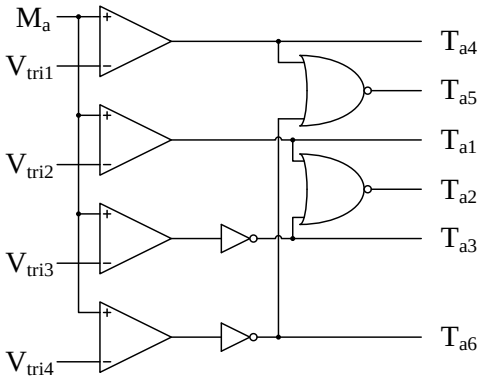


Fig. 8.12. Switching scheme based on LS-PWM strategy with the corresponding gating signal of phase ‘a’.

TABLE 8.6

INSTANTANEOUS PHASE 'A' CURRENT EXPRESSION OF 5L-M^2S^2CI WITH THE RESPECTIVE ANGLE OF THE OPERATING SYSTEM AND THE RANGE OF MODULATION DEPTH

Current	Equation	Operating Angle	Modulation
$I_{Da1}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$0 \le \omega t < \pi$	$M_a \ge \frac{1}{2}$
$I_{Da3}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Da5}(t)$	$I_a(t)\left[1-T_{a4}(t)-T_{a6}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Da7}(t)$	$I_a(t)\left[1-T_{a4}(t)-T_{a6}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Ta1}(t)$	$I_a(t)\left[T_{a1}(t)-T_{a4}(t)\right]$	$0 \le \omega t < \pi$	
$I_{Ta2}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta3}(t)$	$I_a(t)\left[T_{a3}(t)-T_{a6}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Ta4}(t)$	$I_a(t)T_{a4}(t)$	$\sin^{-1}\frac{1}{2M_a} \le \omega t < \pi - \sin^{-1}\frac{1}{2M_a}$	
$I_{Ta5}(t)$	$I_a(t)\left[1-T_{a4}(t)-T_{a6}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta6}(t)$	$I_a(t)T_{a6}(t)$	$\pi \le \omega t < 2\pi$	
$I_{Da1}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$0 \le \omega t < \pi$	$M_a < \frac{1}{2}$
$I_{Da3}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$\pi \le \omega t < 2\pi$	
$I_{Da5}(t)$	$I_a(t)$	$0 \le \omega t < \pi$	
$I_{Da7}(t)$	$I_a(t)$	$\pi \le \omega t < 2\pi$	
$I_{Ta1}(t)$	$I_a(t)T_{a1}(t)$	$0 \le \omega t < \pi$	
$I_{Ta2}(t)$	$I_a(t)\left[1-T_{a1}(t)-T_{a3}(t)\right]$	$0 \le \omega t < 2\pi$	
$I_{Ta3}(t)$	$I_a(t)T_{a3}(t)$	$\pi \le \omega t < 2\pi$	
$I_{Ta4}(t)$	0	$0 \le \omega t < \pi$	
$I_{Ta5}(t)$	$I_a(t)$	$0 \le \omega t < 2\pi$	
$I_{Ta6}(t)$	0	$\pi \le \omega t < 2\pi$	

$$V_{sm}(t) = \frac{V_{dc}(t)}{4}\left[T_{s1}(t) - T_{s3}(t)\right] \tag{8.6}$$

Similarly, a low modulation operation is not recommended to operate as presented in subsection 8.2.3. This is due to the design requirement for preventing oversizing and improves the output quality of the inverter of both proposed five-level inverter topologies with the bidirectional switch configuration. The instantaneous current expression is shown in Table 8.6 with the range of modulation depth.

8.3 Switching Function of 5L-Inverters

The basic derivation of the switching function is detailed in Chapters 5. 5L-MDCI topology with the use of LS-PWM technique is been derived and explained in Chapter 7 and is shown in Table 8.7.

The switching function expression for the proposed 5L-inverter topologies is listed in Table 8.8. The switching function is selected according to the required switching state as stated in the instantaneous current table (e.g., Table 8.1 for 5L-MDCI) for the proposed topologies. The switching function expression for global current stress analysis is discussed in the following sections. Power loss derivation for each switches are also determined by the global stress analysis with the given switching function expression.

TABLE 8.7

SWITCHING FUNCTION OF CLASSICAL FIVE-LEVEL INVERTER TOPOLOGIES

5L-Inverters Topologies	Switches	Switching Function Expression
MDCI	$T_{a1}(t)$	$2M_a(t)$-1
	$T_{a2}(t)$	$2M_a(t)$
	$T_{a3}(t)$	$2M_a(t)$+1
	$T_{a4}(t)$	$2M_a(t)$+2

where $M_a(t)$ is the phase 'a' modulation signal, $M_a(t) = m_a \sin\omega t$.

TABLE 8.8

SWITCHING FUNCTION OF PROPOSED FIVE-LEVEL INVERTER TOPOLOGIES

5L-Inverters Topologies	Switches	Switching Function Expression
M^2DCI	$T_{a1}(t)$	$2M_a(t)$
	$T_{a2}(t)$	$2M_a(t)+1$
	$T_{a5}(t)$	$2M_a(t)-1$
	$T_{a6}(t)$	$2M_a(t)+2$
M^2T^2CI	$T_{a1}(t)$	$2M_a(t)$
	$T_{a4}(t)$	$-2M_a(t)$
	$T_{a5}(t)$	$2M_a(t)-1$
	$T_{a8}(t)$	$-2M_a(t)-1$
M^2S^2CI	$T_{a1}(t)$	$2M_a(t)$
	$T_{a3}(t)$	$-2M_a(t)$
	$T_{a4}(t)$	$2M_a(t)-1$
	$T_{a6}(t)$	$-2M_a(t)-1$

Note: For global stress analysis, modulation function for the respective switches is known as $M_{ai}(t) = M_a(t)$ for all <i = 1, 2, 3,…..>.

If voltage expression of the output characteristic is derived, then product of each local modulation

8.4 Stresses on Power Devices

The following stress analysis in this subsection is used to calculate the conduction and switching losses of the power devices. Average and RMS current stress approximation is derived with the given switching function in Tables 8.7 and 8.8. The power devices for 5L-Inverter topologies are selected according to the maximum voltage and current stresses level. The chosen power devices rating are calculated based on the

TABLE 8.9

VOLTAGE STRESS EXPRESSION FOR 5L-MDCI AND 5L-M^{2}DCI TOPOLOGIES

5L-Inverters Topologies	Switches	Voltage Stress Expression
MDCI	T_{a1}	$\frac{V_{dc}(t)}{4}\left[1-T_{a1}(t)\right]$
	T_{a2}	$\frac{V_{dc}(t)}{4}\left[1-T_{a2}(t)\right]$
	T_{a3}	$\frac{V_{dc}(t)}{4}\left[1-T_{a3}(t)\right]$
	T_{a4}	$\frac{V_{dc}(t)}{4}\left[1-T_{a4}(t)\right]$
	D_{a1}	$\frac{V_{dc}(t)}{4}T_{a1}(t)$
	D_{a2}	$\frac{V_{dc}(t)}{4}\left[T_{a1}(t)+T_{a2}(t)\right]$
	D_{a3}	$\frac{V_{dc}(t)}{4}\left[T_{a1}(t)+T_{a2}(t)+T_{a3}(t)\right]$
M^{2}DCI	T_{a1}	$\frac{V_{dc}(t)}{4}\left[1-T_{a1}(t)\right]$
	T_{a2}	$\frac{V_{dc}(t)}{4}\left[1-T_{a2}(t)\right]$
	T_{a5}	$\frac{V_{dc}(t)}{2}\left[1-T_{a5}(t)\right]\cdot\left[1-\frac{1}{2}\left[T_{a1}(t)+T_{a2}(t)-T_{a6}(t)\right]\right]$
	T_{a6}	$\frac{V_{dc}(t)}{2}\left[1-T_{a6}(t)\right]$
	D_{a1}	$\frac{V_{dc}(t)}{4}T_{a1}(t)$
	D_{a3}	$\frac{V_{dc}(t)}{4}\left[T_{a1}(t)+T_{a2}(t)-1\right]\cdot\left[T_{a5}(t)-\frac{1}{2}+\frac{T_{a6}(t)}{2}\right]$

TABLE 8.10

VOLTAGE STRESS EXPRESSION FOR 5L-M^2T^2CI AND 5L-M^2S^2CI TOPOLOGIES

5L-Inverters Topologies	Switches	Voltage Stress Expression
M^2T^2CI	T_{a1}	$\frac{V_{dc}(t)}{4}\left[1-T_{a1}(t)+T_{a4}(t)\right]$
	T_{a2}	$\frac{V_{dc}(t)}{4}T_{a4}(t)$
	T_{a4}	$\frac{V_{dc}(t)}{4}\left[1-T_{a4}(t)+T_{a1}(t)\right]$
	T_{a5}	$\frac{V_{dc}(t)}{4}\left[2-T_{a1}(t)+T_{a4}(t)-T_{a5}(t)+T_{a8}(t)\right]$
	T_{a6}	$\frac{V_{dc}(t)}{4}T_{a8}(t)$
	T_{a8}	$\frac{V_{dc}(t)}{4}\left[2+T_{a1}(t)-T_{a4}(t)+T_{a5}(t)-T_{a8}(t)\right]$
M^2S^2CI	T_{a1}	$\frac{V_{dc}(t)}{4}\left[1-T_{a1}(t)+T_{a3}(t)\right]$
	T_{a2}	$\frac{V_{dc}(t)}{4}\left[T_{a1}(t)+T_{a3}(t)\right]$
	T_{a3}	$\frac{V_{dc}(t)}{4}\left[1+T_{a1}(t)-T_{a3}(t)\right]$
	T_{a4}	$\frac{V_{dc}(t)}{4}\left[2-T_{a1}(t)+T_{a3}(t)-T_{a4}(t)+T_{a6}(t)\right]$
	T_{a5}	$\frac{V_{dc}(t)}{4}\left[T_{a4}(t)+T_{a6}(t)\right]$
	T_{a6}	$\frac{V_{dc}(t)}{4}\left[2+T_{a1}(t)-T_{a3}(t)+T_{a4}(t)-T_{a6}(t)\right]$
	D_{a1}	$\frac{V_{dc}(t)}{4}T_{a1}(t)$
	D_{a3}	$\frac{V_{dc}(t)}{4}T_{a3}(t)$
	D_{a5}	$\frac{V_{dc}(t)}{4}T_{a4}(t)$
	D_{a7}	$\frac{V_{dc}(t)}{4}T_{a6}(t)$

approximation stress analysis as presented in [92-94]. The voltage and current stress expressions are determined based on the following assumptions:

1) Current and voltage waveforms are ripple free from the load and dc-link.
2) Balanced dc-link capacitors voltage.
3) Zero voltage spike caused by the parasitic element due to low switching frequency range.
4) Pure sinusoidal current due to highly inductive load.

8.4.1 Voltage Stress on Power Devices

Voltage stress expressions for each of the power devices in the upper phase leg are listed in the following Table 8.9. The rest of the power devices are not listed in the Table 8.9 is the power devices of the lower phase leg, which is also known as the symmetrical components of the upper phase leg devices. For symmetrical components, maximum voltage stress level is same as compared to the upper phase leg power devices. With this expression, the final value of the maximum voltage stress level is calculated by

TABLE 8.11

MAXIMUM VOLTAGE STRESS LEVEL FOR 5L-MDCI AND 5L-M^{2}DCI TOPOLOGIES

5L-Inverters Topologies	Maximum Voltage Stress Level Based on Table 8.9
MDCI	$\begin{cases} V_{Ta1} = V_{Ta2} = V_{Ta3} = V_{Ta4} = V_{Ta5} \\ \quad = V_{Ta6} = V_{Ta7} = V_{Ta8} = V_{Da1} = V_{Da6} = \frac{1}{4}V_{dc} \\ V_{Da2} = V_{Da5} = \frac{1}{2}V_{dc} \\ V_{Da3} = V_{Da4} = \frac{3}{4}V_{dc} \end{cases}$
M^{2}DCI	$\begin{cases} V_{Ta1} = V_{Ta2} = V_{Ta3} = V_{Ta4} = V_{Da1} = V_{Da2} = V_{Da3} = V_{Da4} = \frac{1}{4}V_{dc} \\ V_{Ta5} = V_{Ta8} = \frac{3}{4}V_{dc} \\ V_{Ta6} = V_{Ta7} = \frac{1}{2}V_{dc} \end{cases}$

TABLE 8.12

MAXIMUM VOLTAGE STRESS LEVEL FOR 5L-M^2T^2CI AND 5L-M^2S^2CI TOPOLOGIES

5L-Inverters Topologies	Maximum Voltage Stress Level Based on Table 8.9
M^2T^2CI	$\begin{cases} V_{Ta1} = V_{Ta4} = \dfrac{V_{dc}}{2} \\ V_{Ta2} = V_{Ta3} = V_{Ta6} = V_{Ta7} = \dfrac{V_{dc}}{4} \\ V_{Ta5} = V_{Ta8} = V_{dc} \end{cases}$
M^2S^2CI	$\begin{cases} V_{Ta1} = V_{Ta3} = \dfrac{V_{dc}}{2} \\ V_{Ta2} = V_{Ta5} = V_{Da1} = V_{Da2} = V_{Da3} \\ \qquad = V_{Da4} = V_{Da5} = V_{Da6} = V_{Da7} = V_{Da8} = \dfrac{V_{dc}}{4} \\ V_{Ta4} = V_{Ta6} = V_{dc} \end{cases}$

substituting the switching states into the mathematical expression to obtain the maximum voltage stress level as finalized in the following Tables 8.11 and 8.12.

8.4.2 Current Stress on Power Devices

This section is to calculate the current stress of the power devices based on the global stress analysis with the local averaged values over fundamental period of the switching period as detailed in [92]. The accuracy of the analysis is found to be commendable as the analytical results are on par with simulation results. In addition, the loss modeling is supported by using the approximation of current stress based on the derived switching function. This approach has been adopted by the Infineon described in the application note [95].

The adopted average and RMS current stress analysis is analyzed over one fundamental period of the load requirement without any product of sum of the

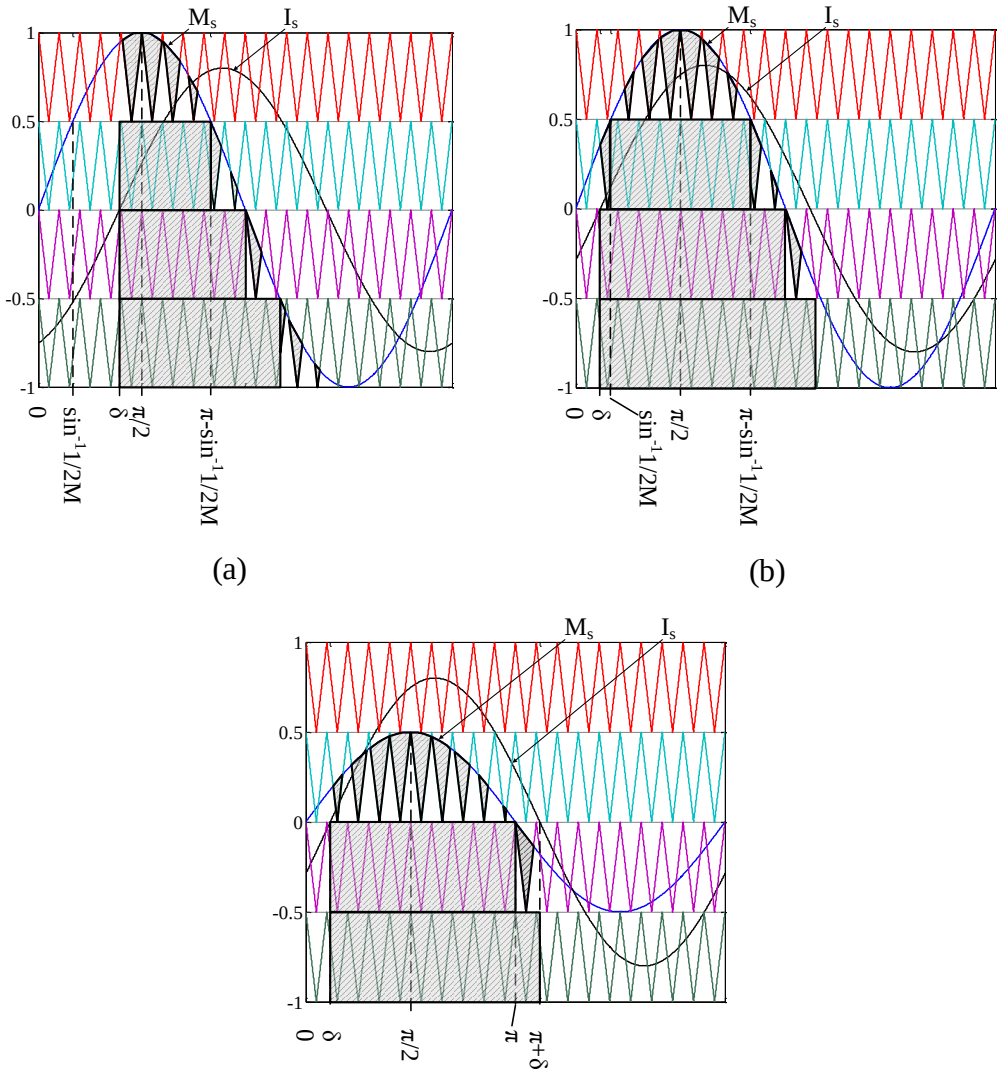


Fig. 8.13. Current commutaion in the respective switches as shaded in the carriers region for different operating condition of a 5L-MDCI operation. (a) $\sin^{-1}1/2M_a \leq \delta$ for $M_a \geq 0.5$, (b) $\sin^{-1}1/2M_a > \delta$ for $M_a \geq 0.5$ and (c) $M_a < 0.5$.

harmonic order of the load current. The load current is assumed to be purely sinusoidal and is dependent on operating power factor angle, δ. The summation of the pulse current during the switching commutation of the power device can be simplified by using the integral of local values over one fundamental period of the switching states. For simplification, the general expression of the average and RMS current stress with respect to switching function is approximated (as stated in Table 8.7 and Table 8.8) and expressed in the following equation:

$$
\begin{aligned}
I_{Tai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{S_{Tai}} I_a\left(kt_p,\omega t\right)\right]d\omega t \approx \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{S_{Tai}t_p} I_a\left(\omega t\right)dt_\mu\right]d\omega t \\
I_{Dai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{S_{Dai}} I_a\left(kt_p,\omega t\right)\right]d\omega t \approx \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{S_{Dai}t_p} I_a\left(\omega t\right)dt_\mu\right]d\omega t
\end{aligned}
\tag{8.7}
$$

$$
\begin{aligned}
I_{Tai\langle rms\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{S_{Tai}} I_a^2\left(kt_p,\omega t\right)\right]d\omega t} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{S_{Tai}t_p} I_a^2\left(\omega t\right)dt_\mu\right]d\omega t} \\
I_{Dai\langle rms\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{S_{Dai}} I_a^2\left(kt_p,\omega t\right)\right]d\omega t} = \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{S_{Dai}t_p} I_a^2\left(\omega t\right)dt_\mu\right]d\omega t}
\end{aligned}
\tag{8.8}
$$

where S_{Tai} is the switching function of the switching scheme as presented in Tables 8.7 and 8.8 and i = 1,2,3,… of the respective power devices, t_p is the time interval of the pulses generated within one period of the switching scheme. α and β is the range of the occurring switching pulse during one cycle. Based on equations 8.7 and 8.8, the final general expression of the current stress analysis is shown in the following.

$$
\begin{aligned}
I_{Tai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a\left(\omega t\right)\cdot S_{Tai}\left(\omega t\right)d\omega t = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_{Tai}\left(\omega t\right)d\omega t \\
I_{Dai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a\left(\omega t\right)\cdot S_{Dai}\left(\omega t\right)d\omega t = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_{Dai}\left(\omega t\right)d\omega t
\end{aligned}
\tag{8.9}
$$

$$
\begin{aligned}
I_{Tai\langle rms\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2\left(\omega t\right)\cdot S_{Tai}\left(\omega t\right)d\omega t} \\
I_{Dai\langle rms\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2\left(\omega t\right)\cdot S_{Dai}\left(\omega t\right)d\omega t}
\end{aligned}
\tag{8.10}
$$

$I_{Tai}(\omega t)$ and $I_{Dai}(\omega t)$ are the local currents through the power device with respect to the switching function of the respective device. The local current is expressed as a function of load current and switching function as shown in Tables 8.1, 8.3, 8.5 and 8.6 for the respective 5L-inverter topologies.

Substitute the boundary limit in the integral form of equations 8.9 and 8.10 to have better visualization of the current stress expression in term of amplitude current, power factor angle (operating load angle, δ) and amplitude modulation. Simple graphical approach of the current commutation period with the range of the modulation depth is shown in Fig. 8.13. These figures illustrate the current through the switches during the switching commutation period of a 5L-MDCI topology with the LS-PWM techniques under various operating condition. The shaded area represents the current commutation in the power devices of the 5L-MDCI topology and analytical approximation of the compact form of average current stress for the classical 5L- MDCI topology is written in Tables A.1, A.2 and A.3 (ref. to Appendix A) for various operating condition. The boundary limit for the integration calculus obtained from the graphical approach as shown in Fig. 8.13. Similarly, the approximation of the RMS current stress of the power devices as presented in equation 8.8 are finalized in Tables A.4, A.5 and A.6 (ref. to Appendix A) with the various operating condition and the commutation period are shown in Fig. 8.13 for the boundary limit of the integration.

5L-M^{2}DCI Topology: With similar mathematical approach on the current stress analysis used in 5L-MDCI topology is applied for the proposed 5L-inverter topologies. The current commutation of the power devices within one full period of the switching cycle is shown in Fig. 8.14. With this graphical approach, the boundary limit of the local current for the average and RMS current calculation is analyzed for the lower and upper limit of the integration.

Based on Fig. 8.14, a zero current switching is achieved for particular switching states (states 1 and 5 of Table 8.2). The zero current switching occurs in T_{a1}-T_{a4} during switching states 1 and 5 is clearly shown in Fig. 8.14 and it is not shaded in the middle two operating region of the LS-PWM of Fig. 8.14.

The current stress expressions for the average and RMS current value for the proposed 5L-M^{2}DCI topology are listed in the following Tables A.7 to A.12 (ref. to Appendix). The average current stress expressions with the various operating conditions are shown in Tables A.7 to A.9. RMS current stress expression with the consideration of the zero current switching under high modulation is written in Tables A.10 to A.11. For low

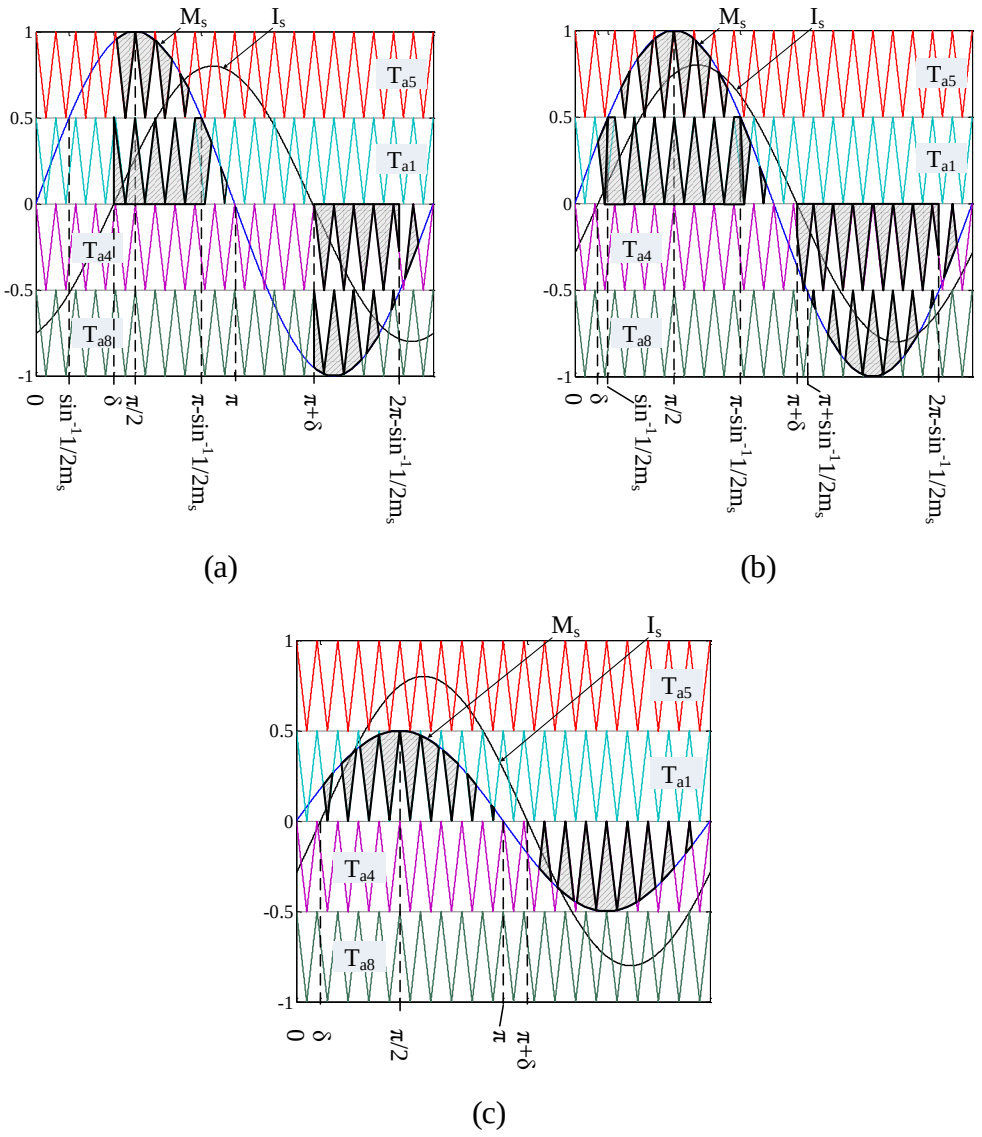


Fig. 8.15. Current commutaion mode of the respective power switches as shown in the shaded area under different operating condition of a 5L-M^2T^2CI operation. (a) $\sin^{-1}1/2M_a \leq \delta$ for $M_a \geq 0.5$, (b) $\sin^{-1}1/2M_a > \delta$ for $M_a \geq 0.5$ and (c) $M_a < 0.5$.

modulation indices, no zero current switching is achieved in the inner cell switches and the expression of the average and RMS current expression is shown in Tables A.9 and A.12. This is due to the output three-level operation in the inner cell switches and only one switches of the outer cell converter is continuously conducting for full cycle operation.

5L-M^2T^2CI and 5L-M^2S^2CI Topologies: The graphical approach of the boundary limit for the integration calculus of the current stress analysis of both proposed 5L-M^2T^2CI

and 5L-M^2S^2CI topologies are shown in Fig. 8.15. Zero current switching is also achieved in the power device of the inner-cell switches for both topologies as illustrated in the two switching states 1 and 5 of Table 8.4. The average current stress expression of both topologies based on the boundary limit and various operations are shown in Tables A.13 to A.15 for 5L-M^2T^2CI and Tables A.19 to A.21 for 5L-M^2S^2CI. RMS current expressions are indicated in the following Tables A.16 to A.18 for 5L-M^2T^2CI and Tables A.22 to A.24 for 5L-M^2S^2CI.

According to Fig. 8.15, the boundary limit of the current pulses of the bidirectional switches are commutated within the range of 0 to 2π of the sinusoidal load current depending on the power angle and the switching states selection. The current stress rating of each discrete diode elements of the bidirectional switches in 5L-M^2S^2CI is half that of the active switch of the bidirectional switches in 5L-M^2T^2CI. The remaining devices of 5L-M^2S^2CI have the same current rating as compared to the 5L-M^2T^2CI topology, a list of current stress rating of each of the power device in 5L-M^2T^2CI topology is shown in the following Tables.

8.5 Accuracy of the Current Stress Calculation

It is important to know the deviation margin of experimental results with respect to simulation results. Approximation of the stress level of the power device may not be same as compared to the simulation results but it is sufficient to prove the concept of current commutation and prevent any oversizing of the converter. The main reason of the error calculation is to validate the previous assumptions. Therefore, the accuracy of the current stress analysis in the previous section is limited based on the assumptions made.

The deviation in the calculated current stress for active switches is partly due to the reverse recovery current through the anti-parallel diode. The current commutation for every active switch and anti-parallel diode in every pulse during fundamental period is calculated individually by the analytical solution, In order to determine the individual losses incurred in active switch and anti-parallel diode, the analysis is carried out separately. The on-state resistance for the active switch and anti-parallel diode are listed

at different value and characteristics in the manufacturer's datasheet, while the simulation results of the reverse recovery current commutation for the active switch cannot be determined through simulation results.

To verify the current stress expression as stated in the previous section 8.4.2, data for comparative analysis is presented in Tables 8.13 to 8.16 for the respective 5L-inverters. The simulated and analytical results for the analytical comparison are obtained from Simulation tools PSIM and MATLAB R2010b. The current stress on the discrete components is determined by modeling and simulating device in PSIM. Analytical results are validated using MATLAB Script by setting boundary limits for integration.

Based on the data listed in Tables 8.13 to 8.16 with the supported simulation toolbox, one of the power devices at the neutral-point-clamped for the presented 5L-inverter topologies does not equal to the simulated results. This is due to the neutral-point clamped diode or bidirectional switches in the inner cell dependent on the accuracy of the current stress of the series connected switch of the bridge leg of the inner cell.

Although, one of the power device may deviate to some error value based on the global stress approximation with the local average switching current integration method. However, it is sufficient to analyze the overall loss distribution of the power device, where the concept of zero current switching is occurred in the multiple-pole hierarchy. The loss modeling of the power device will be discussed in the following sections. The efficiency of the proposed topology is to be significantly high due to reduction in the number of active components.

TABLE 8.13

COMPARISON RESULTS OF THE CURRENT STRESS ON THE POWER DEVICE BETWEEN THE ANALYTICAL RESULTS AND SIMULATION RESULTS FOR CLASSICAL 5L-MDCI TOPOLOGY

Topologies	Devices	$\sin^{-1}1/2m_a \leq \delta$ and $M_a \geq 0.5$				$\sin^{-1}1/2m_a > \delta$ and $M_a \geq 0.5$				$M_a < 0.5$			
		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)	
		Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
5L-MDCI	$T_{a1} = T_{a8}$	0.6371	0.5291	1.6595	1.3945	0.6232	0.5936	1.5479	1.4873	0	0	0	0
	$T_{a2} = T_{a7}$	1.3982	1.1450	2.2496	2.0911	1.2599	1.2186	2.0718	2.0579	0.2072	0.1897	0.4930	0.4724
	$T_{a3} = T_{a6}$	1.4761	1.3997	2.2717	2.2704	1.3320	1.3483	2.0923	2.1166	0.4398	0.4334	0.6909	0.6889
	$T_{a4} = T_{a5}$	1.4762	1.4669	2.3556	2.2926	1.3320	1.3531	2.0923	2.1174	0.4398	0.4343	0.6909	0.6891
	$D_{a1} = D_{a4}$	0.7610	0.6159	1.5188	1.5583	0.6367	0.6250	1.3770	1.4223	0.2072	0.1897	0.4930	0.4724
	$D_{a2} = D_{a5}$	0.1213	0.2547	0.2332	0.8844	0.0721	0.1296	0.2922	0.4950	0.2326	0.2438	0.4840	0.5014
	$D_{a3} = D_{a6}$	0.0728	0.0672	0.3019	0.3181	0	0.0049	0	0.0585	0	0.0009	0	0.0165
	D_{Ta1} to D_{Ta8}	0.0364	N.A	0.2135	N.A	0	N.A	0	N.A	0	N.A	0	N.A

Note: N.A is not applicable to obtain the value of the anti-parallel diode in the discrete components from the digital simulation software (PSIM Simcoupler).

TABLE 8.14

COMPARISON RESULTS OF THE CURRENT STRESS ON THE POWER DEVICE BETWEEN THE ANALYTICAL RESULTS AND SIMULATION RESULTS FOR PROPOSED 5L-M^{2}DCI TOPOLOGY

Topologies	Devices	$\sin^{-1}1/2m_a \le \delta$ and $M_a \ge 0.5$				$\sin^{-1}1/2m_a > \delta$ and $M_a \ge 0.5$				$M_a < 0.5$			
		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)	
		Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
5L-M^{2}DCI	$T_{a1} = T_{a4}$	0.7622	0.5579	1.5212	1.6045	0.6392	0.6214	1.6388	1.4356	0.2072	0.1887	0.4938	0.4729
	$T_{a2} = T_{a3}$	0.8402	0.8173	1.5538	1.8379	0.7463	0.7514	1.7707	1.5192	0.4396	0.4334	0.6906	0.6896
	$T_{a5} = T_{a8}$	0.6382	0.5359	1.6621	1.4117	0.6256	0.5989	1.6212	1.5004	0	0	0	0
	$T_{a6} = T_{a7}$	1.4785	1.4835	2.3592	2.3173	1.3373	1.3642	2.3703	2.1347	0.4396	0.4354	0.6906	0.6896
	$D_{a1} = D_{a4}$	0.0781	0.2593	0.3166	0.8964	0.1071	0.1300	0.6708	0.4971	0.2325	0.2447	0.4838	0.5019
	$D_{a3} = D_{a5}$	0.8404	0.9477	1.6744	1.8376	0.7117	0.7652	1.7291	1.5184	0.4396	0.4354	0.6906	0.6896
	D_{Ta1} to D_{Ta4}	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta5} to D_{Ta8}	0.0365	N.A	0.2138	N.A	0	N.A	0	N.A	0	N.A	0	N.A

TABLE 8.15

COMPARISON RESULTS OF THE CURRENT STRESS ON THE POWER DEVICE BETWEEN THE ANALYTICAL RESULTS AND SIMULATION RESULTS FOR PROPOSED 5L-M^2T^2CI TOPOLOGY

Topologies	Devices	$\sin^{-1}1/2m_a \le \delta$ and $M_a \ge 0.5$				$\sin^{-1}1/2m_a > \delta$ and $M_a \ge 0.5$				$M_a < 0.5$			
		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)	
		Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
5L-M^2T^2CI	T_{a1}	0.7633	0.5511	1.5234	1.5949	0.6426	0.6196	1.3898	1.4341	0.2073	0.1888	0.4932	0.4731
	$T_{a2} = T_{a3}$	0	0.0003	0.4484	1.2516	0	0.0013	0.4171	0.7084	0	0	0.6848	0.7118
	T_{a4}	0.5929	0.5316	1.4095	1.5604	0.6426	0.6112	1.3898	1.4122	0.2073	0.1932	0.4932	0.4780
	T_{a5}	0.6390	0.5302	1.6644	1.3984	0.6289	0.5971	1.5623	1.4964	0	0	0	0
	$T_{a6} = T_{a7}$	0	0.0192	2.3733	2.5583	0	0.0071	2.2094	2.1336	0	0	0.9775	0.9792
	T_{a8}	0.6390	0.4979	1.6644	1.3430	0.6289	0.5695	1.5623	1.4611	0	0	0	0
	D_{Ta1}	0.0730	N.A	0.3029	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta4}	0.0730	N.A	0.3029	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta5}	0.0365	N.A	0.2142	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta8}	0.0365	N.A	0.2142	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	$D_{Ta2} = D_{Ta3} = D_{Ta6} = D_{Ta7}$	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A

TABLE 8.16

COMPARISON RESULTS OF THE CURRENT STRESS ON THE POWER DEVICE BETWEEN THE ANALYTICAL RESULTS AND SIMULATION RESULTS FOR PROPOSED 5L-M^2S^2CI TOPOLOGY

Topologies	Devices	$\sin^{-1}1/2m_a \leq \delta$ and $M_a \geq 0.5$				$\sin^{-1}1/2m_a > \delta$ and $M_a \geq 0.5$				$M_a < 0.5$			
		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)		Average Values (A)		RMS Values (A)	
		Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated	Analytical	Simulated
5L-M^2S^2CI	T_{a1}	0.7621	0.5578	1.5210	1.6042	0.6392	0.6214	1.3824	1.4356	0.2071	0.1886	0.4928	0.4728
	T_{a2}	0.1561	0.5140	0.0443	1.2485	0.1448	0.2608	0.4149	0.7038	0.4649	0.4913	0.3389	0.7112
	T_{a3}	0.5919	0.5238	1.4073	1.5441	0.6392	0.6041	1.3824	1.3957	0.2071	0.1929	0.4928	0.4771
	T_{a4}	0.6381	0.5357	1.6619	1.4113	0.6256	0.5989	1.5540	1.5001	0	0	0	0
	T_{a5}	1.0696	1.8564	3.1068	2.5527	0.9846	1.5140	2.1977	2.1222	0.8791	0.8767	0.9766	0.9782
	T_{a6}	0.6381	0.4931	1.6619	1.3300	0.6256	0.5622	1.5540	1.4424	0	0	0	0
	D_{a1} to D_{a4}	0.0781	0.2594	0.0222	0.8965	0.0724	0.1301	0.2075	0.4972	0.2325	0.2447	0.1695	0.5018
	D_{a5} to D_{a8}	0.5348	0.9476	1.5534	1.8374	0.4923	0.7654	1.0989	1.5184	0.4396	0.4352	0.4883	0.6895
	D_{Ta1}	0.0729	N.A	0.3023	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta3}	0.0729	N.A	0.3023	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta4}	0.0365	N.A	0.2138	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	D_{Ta6}	0.0365	N.A	0.2138	N.A	0	N.A	0	N.A	0	N.A	0	N.A
	$D_{Ta2} = D_{Ta5}$	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A	0	N.A

8.6 Losses in Power Devices

A loss modeling of power device is discussed in this section. The important aspect of this modeling is to observe the loss distribution across each power device. This allows us to design more economical 5L-inverter topologies with an optimum cost-to-performance ratio.

The correlation between the voltage stress and current stress are related to the losses occurring in every pulse during one cycle. The stress is applied for the conduction and switching losses calculation. The summation of these two losses is the total loss distribution in each power devices of the 5L-inverter topologies. The device losses depend on various factors such as temperature, switching frequency, gate voltage level and power level of the load. For a proper development of the application, each of the devices is selected based on the range of the switching frequency and power level of the application as shown in Fig. 8.16.

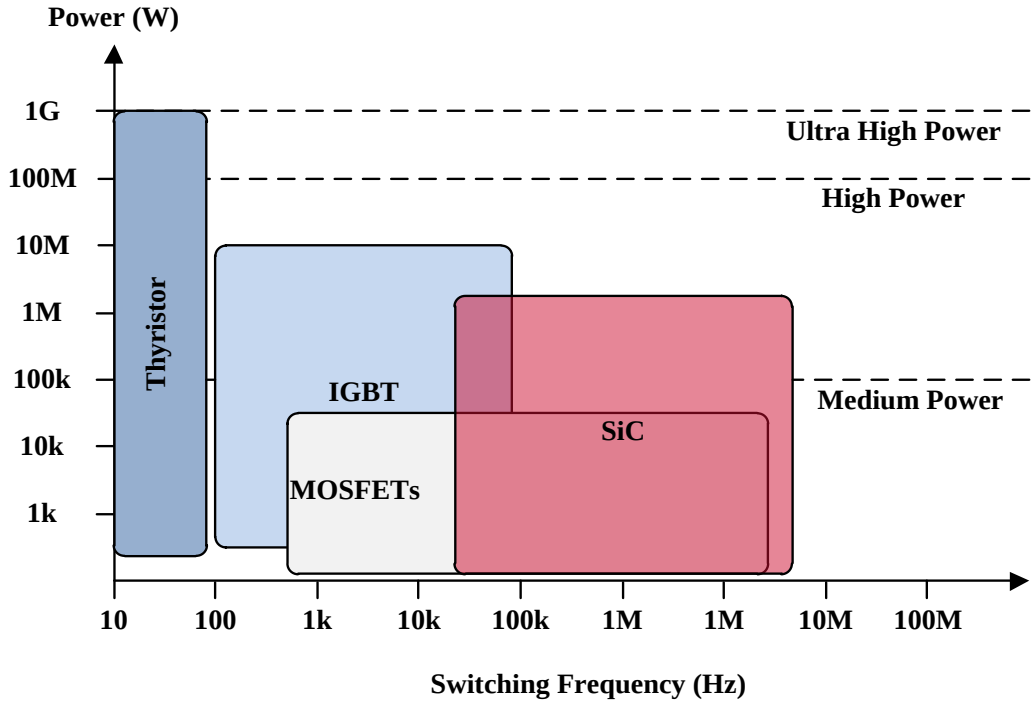


Fig. 8.16. Power versus frequency characteristics of the power semiconductor devices (this data is obtained from the application notes of the manufacturer Infineon [96]).

8.6.1 Conduction Loss in Power Devices

The approximation of the conduction loss of the power devices in inverter operation mode is mainly based on the multiple pulse calculation. This is also known as the current stress commutation of the power device during every pulse in one fundamental period as discussed in the previous subsection. The conduction losses are also calculated based on the characteristic curve of the individual power semiconductor device. Since a low switching frequency range is used for 5L-inverter topologies, two types of semiconductor devices such as power MOSFET and IGBT devices are selected for the possible implementation.

In general, a simple approximation of the conduction loss in power MOSFET device is approximated by using the on-state resistance for temperature dependency [97, 98]. For a conduction loss in IGBT device, a linear operation curve of the voltage drop that implies with the gate voltage and typical junction temperature of the device is selected for the loss approximation [95, 99, 100]. The linear operation curve can be selected from any manufacturer datasheet that provide the output characteristic of collector current versus collector-emitter voltage. Similarly, the conduction loss for the power diode can also be calculated based on the linear expression of the forward voltage drop. The conduction loss expressions for the respective power device are shown in the following.

MOSFET:

$$P_{Tai\langle avg\rangle} = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(\omega t)\cdot\alpha_{Tai}\cdot R_{DS\langle on\rangle}\,d\omega t = I_{Tai\langle rms\rangle}\cdot R_{DS\langle on\rangle} \tag{8.11}$$

IGBT:

$$\begin{aligned} P_{Tai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a(\omega t)\cdot\alpha_{Tai}\cdot\left[\frac{\Delta V_{CE}}{\Delta I_{Tai}} I_a(\omega t) + V_{CEO}\right] d\omega t \\ &= I_{Tai\langle rms\rangle}\cdot\frac{\Delta V_{CE}}{\Delta I_{Tai}} + I_{Tai\langle avg\rangle}\cdot V_{CEO} \end{aligned} \tag{8.12}$$

Diode device:

$$P_{Dai\langle avg\rangle} = \frac{1}{2\pi}\int_{\alpha}^{\beta} I_a^2(\omega t)\cdot\alpha_{Dai}\cdot R_{d\langle on\rangle}\,d\omega t = I_{Dai\langle rms\rangle}\cdot R_{d\langle on\rangle} \tag{8.13}$$

$I_{Tai<rms>}$ and $I_{Dai<rms>}$ are the root-mean-square (RMS) pulse current of active switch and diode respectively. $R_{DS<on>}$ and $R_{d<on>}$ are the on-state resistance of the power MOSFET and diode respectively, where V_{CEO} is the on-state zero current collector-emitter voltage and $\Delta V_{CE}/\Delta I_C$ is the slope of the on-state resistance of the IGBT device.

8.6.2 Switching Loss in Power Devices

The theoretical calculations of the switching energy loss in power device of the MOSFET and IGBT devices is the summation of the turn on and turn off energy loss resulting within the switching pulse generated by the LS-PWM technique. The average switching loss is the summation of each switching losses occurring at every switching pulse during one cycle period. Summation of the discrete pulse of the switching energy loss at switching frequency, F_s can be replaced by the integration limits, which is given by

$$\begin{aligned} P_{Tai\langle avg\rangle} &= \frac{1}{2\pi}\sum_{\lambda=\alpha}^{\beta}\left[E_{on}(\lambda,\omega t)+E_{off}(\lambda,\omega t)\right]\cdot F_s \\ &\approx \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[E_{on}(\omega t)+E_{off}(\omega t)\right]\cdot F_s\,d\omega t \end{aligned} \tag{8.14}$$

The derivation of each turn on energy loss, $E_{on}(\omega t)$ and turn off energy loss, $E_{off}(\omega t)$ has been detailed in [99]. However, the PSIM thermal module does not consider switching periods versus collector current for the simulation result. Hence, a simple approximation of the switching energy loss can be expressed in term of voltage stress ratio as a polynomial function of collector current [100]. For the theoretical analysis, the tail current of the IGBT device during turn off period is assumed very small value and small amplitude of overvoltage pulse is also neglected for low switching frequency operation.

Based on equation (8.14) with the available information given in the datasheet of the manufacturer Infineon, the final average switching loss expression is given by

$$P_{sw\_Tai\langle avg\rangle} \approx \frac{V_{Tai} F_s}{2\pi V_{nom}} \int_{\alpha}^{\beta} \left[a + b \cdot i_a \sin(\omega t - \delta) + c \cdot i_a^2 \sin^2(\omega t - \delta) \right] d\omega t \qquad (8.15)$$

V_{Tai} is the voltage stress across the power device during turn off. V_{nom} is the nominal voltage of the semiconductor device. a, b and c are the slope factor of the polynomial function of the energy loss as presented in the datasheet with the respective current rating during operation. As a result, the expression of the total switching energy loss of the device is formulated as a linear function.

8.6.3 Distribution of Power Loss in Device

The comparative study on the theoretical and simulation results on the discrete components loss of the 5L-inverter topologies is discussed. Theoretical and simulated results of the average conduction and switching losses in each power device for 5L-inverter topologies are shown in the following Figs 8.17 to 8.20.

Obtained results show theoretical calculation is almost same as compared to the simulated results. The error between the analytical and simulated results is due to the deviation of the approximation of the current stress and some of the information in the datasheet is not provided. However, the theoretical approximation of the discrete components loss is acceptable to prove the overall efficiency. On top of that, the analytical approximation can prevent over sizing of thermal management and cost of the production.

The simulated results with PSIM Thermal Module is based on the available components in the laboratory and all parameters/specification of the components used in the simulation tools are listed in Table 8.17.

TABLE 8.17

SPECIFICATION OF THE SELECTED POWER DEVICES FOR EACH MULTILEVEL INVERTER TOPOLOGIES TEST

Topologies	Switches	Manufacturer	Device Rating	
			Voltage (V)	Current (A)
5L-MDCI	$T_{a1} = T_{a2} = T_{a3} = T_{a4} = T_{a5} = T_{a6} = T_{a7} = T_{a8}$	Infineon IKW30N60T	600	30
5L-M^{2}DCI	$T_{a1} = T_{a2} = T_{a3} = T_{a4}$	Infineon IKW30N60T	600	30
	$T_{a5} = T_{a8}$	Infineon IKW25T120	1200	25
	$T_{a6} = T_{a7}$	Infineon IHW30N90T	900	30
5L-M^{2}T^{2}CI	$T_{a1} = T_{a4} = T_{a5} = T_{a8}$	Infineon IKW25T120	1200	25
	$T_{a2} = T_{a3} = T_{a6} = T_{a7}$	Infineon IKW30N60T	600	30
5L-M^{2}S^{2}CI	$T_{a1} = T_{a3} = T_{a4} = T_{a6}$	Infineon IKW25T120	1200	25
	$T_{a2} = T_{a5}$	Infineon IKW30N60T	600	30

Note: Manufacturer specification of the power diodes on IXYS DSP45-12A is selected for the entire multilevel inverters test.

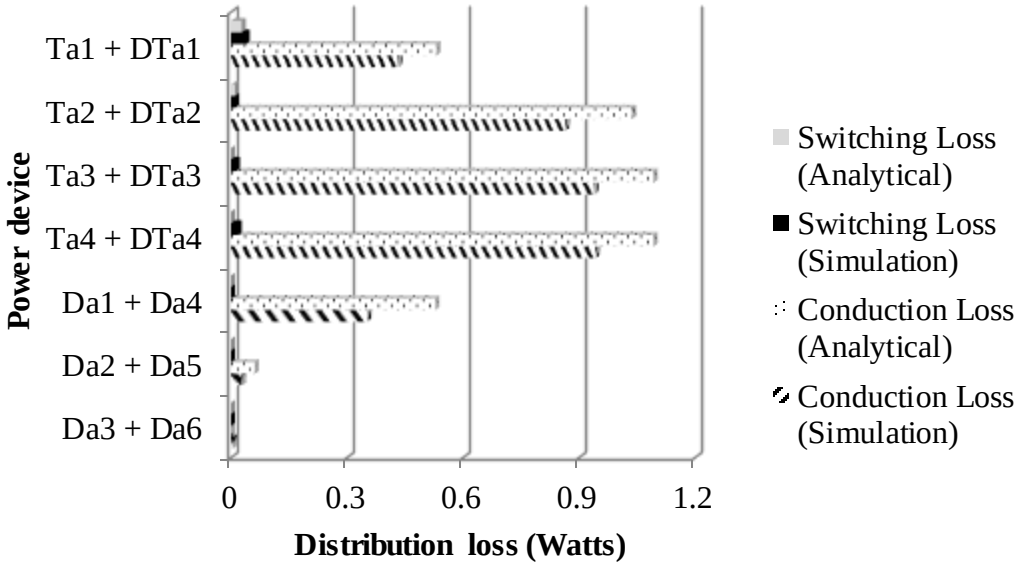


Fig. 8.17. Simulation and analytical results of the switching and conduction losses of each power device in 5L-MDCI topology obtained from PSIM Thermal Module toolbox

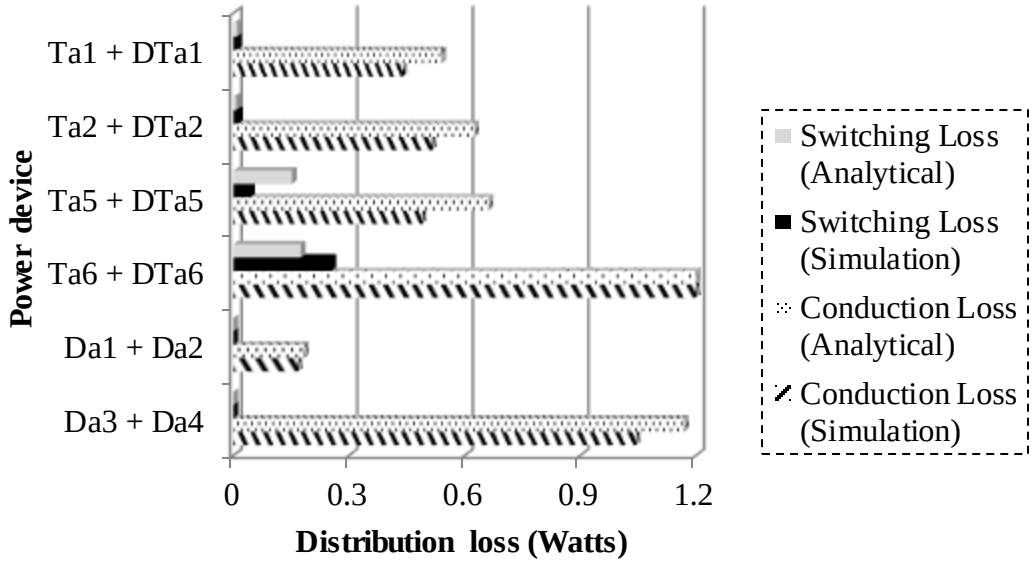


Fig. 8.18. Simulation and analytical results of the switching and conduction losses of each power device in 5L-M^{2}DCI topology obtained from PSIM Thermal Module toolbox.

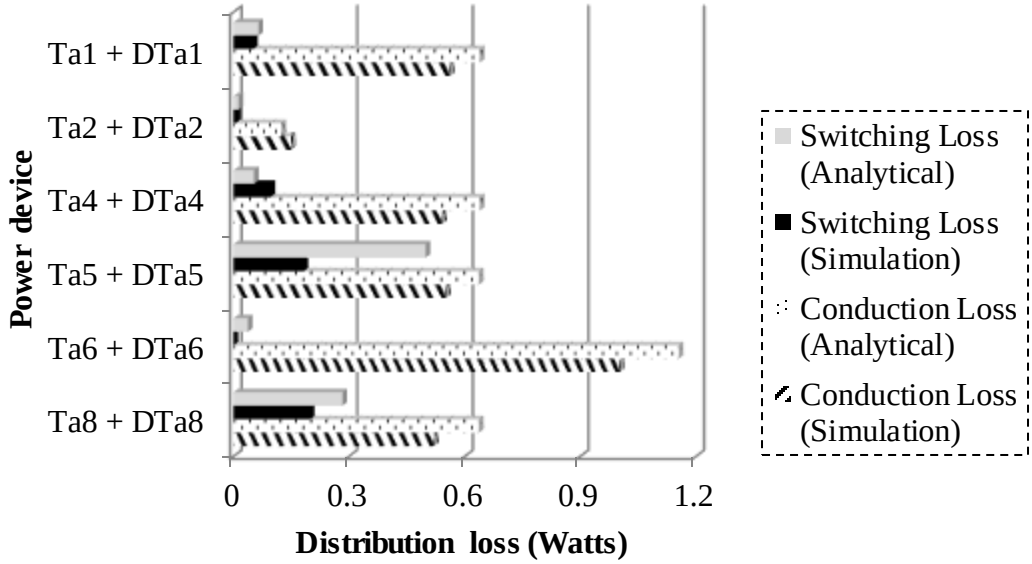


Fig. 8.19. Simulation and analytical results of the switching and conduction losses of each power device in 5L-M^{2}T^{2}CI topology obtained from PSIM Thermal Module toolbox.

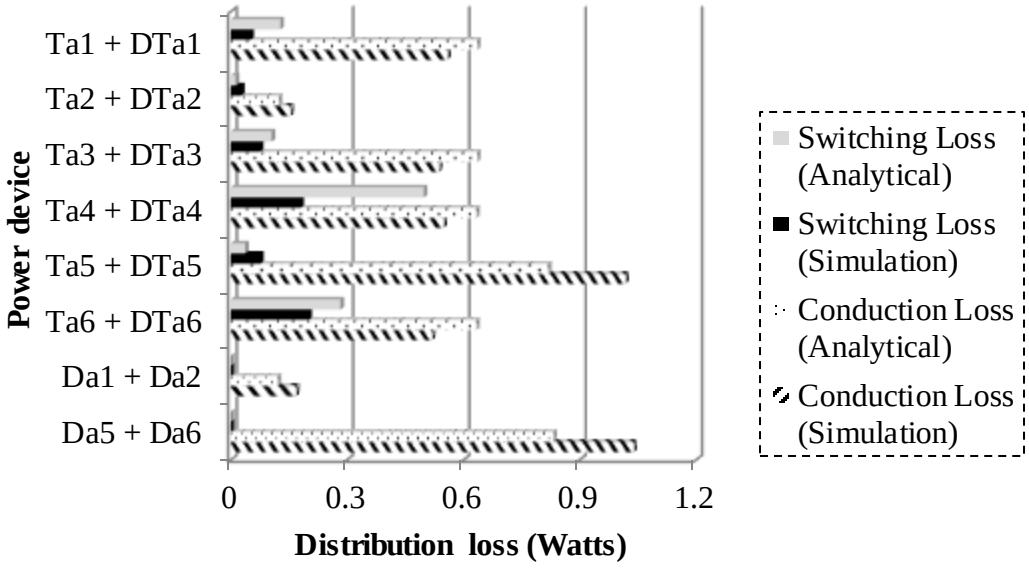


Fig. 8.20. Simulation and analytical results of the switching and conduction losses of each power device in 5L-M^2S^2CI topology obtained from PSIM Thermal Module toolbox.

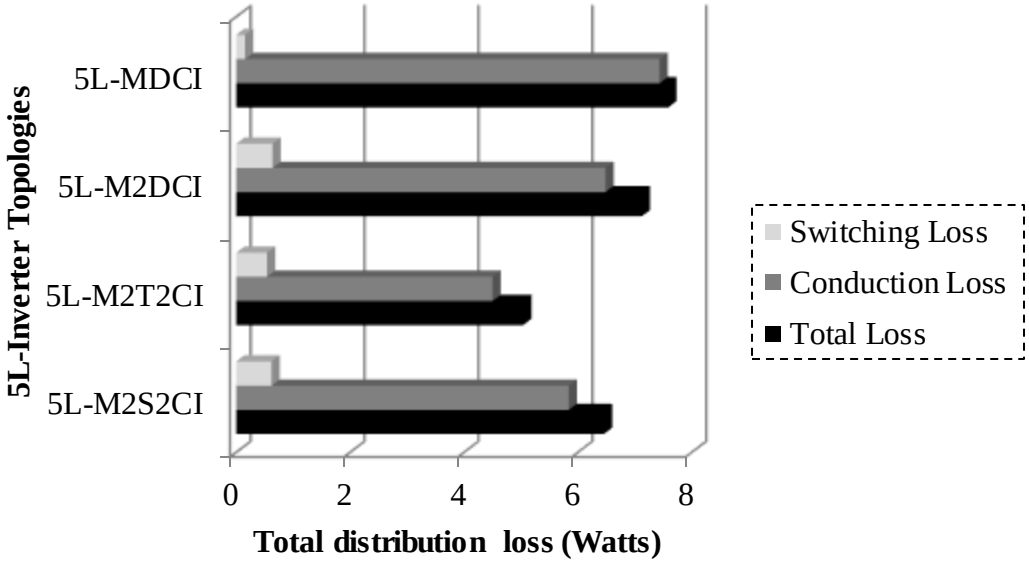


Fig. 8.21. Simulation results of the per-phase leg total loss, switching and conduction losses of multilevel inverter topologies obtained from PSIM Thermal Module toolbox.

According to the simulated results, efficiency of a multiple-pole hierarchy has been improved even when higher rating devices are selected for the outer cell switch. The total loss reduction in multiple-pole hierarchy is due to the zero current switching occurred in the inner cell switches as discussed in the previous subsection of this Chapter.

For low and medium motor drive application with better output voltage quality and energy efficient converters, two types of transformerless and filterless multiple-pole multilevel inverters (5L-M^2T^2CI and 5L-M^2S^2CI) are suitable. The device rating of the switches connected on the outer cell switches of the arm are larger than the inner cell switch and bidirectional switch. Hence, high conduction and switching losses are incurred due to high on state resistance and high voltage stress across the semiconductor switches respectively. Therefore, both topologies are suitable for low voltage and medium power application with the current available power semiconductor market.

On the other hand, 5L-M^2DCI topology is applicable for medium voltage and high power application. The total losses are significantly higher than the other two proposed topologies (5L-M^2T^2CI and 5L-M^2S^2CI). This topology has several advantages as compared to the 5L-M^2T^2CI and 5L-M^2S^2CI topologies. The advantages 5L-M^2DCI offers are: lower voltage stress across the outer cell switches, lower device rating and no shoot-through in the dc-link capacitors during one switch fault. The concept of proposed multiple-pole hierarchy has reduced the total power consumption by a semiconductor device resulting in higher efficiency and a compact converter compared to the classical multilevel diode-clamped inverter particularly for utility application.

8.6.4 Cost Overview

In this subsection, cost analysis of the 5L-inverter topologies is presented in order to illustrate the benefits of energy efficient converter with lesser number of semiconductor devices with higher power ratings. Total cost calculation considers cost of power devices, passive elements and complete analog circuit board for the comparative study between the classical and proposed 5L inverter topologies.

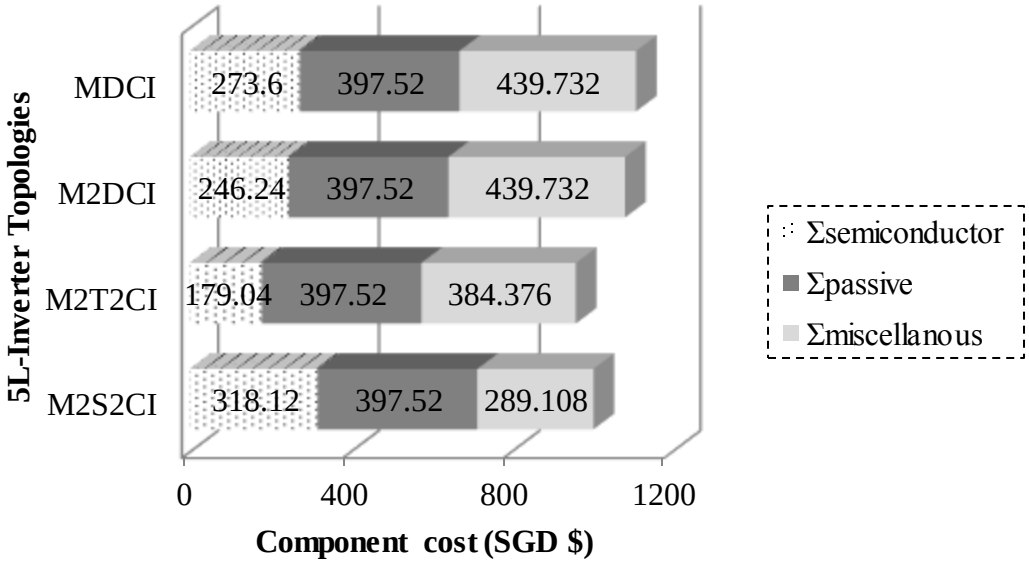


Fig. 8.22. Components costs structure for 5L inverter topologies.

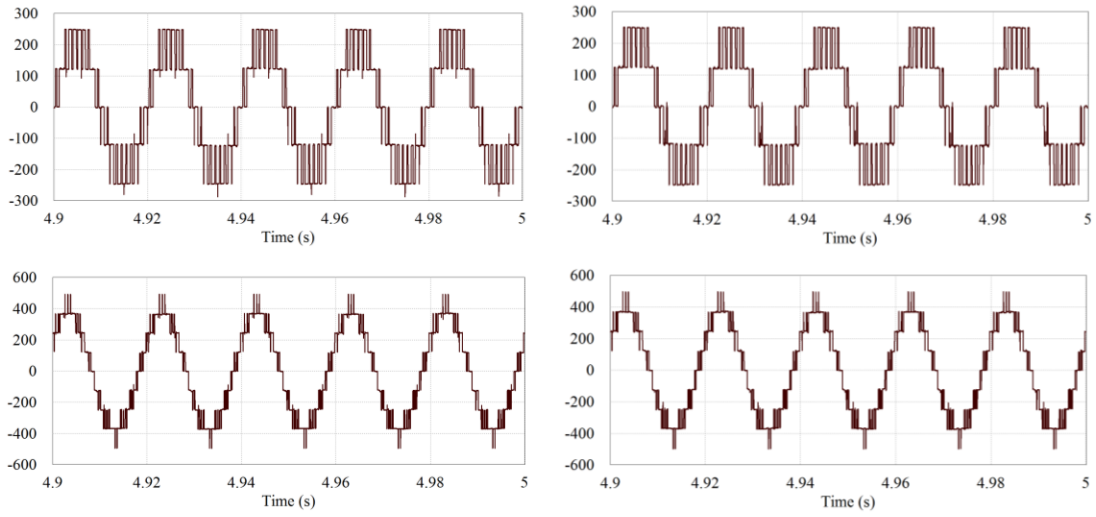
The component cost of 5L-inverter topologies considers factors such as:

1) Random cost factor include country, negotiation, shipment tax and order quantity.
2) Different materials used in the components, design and fabrication process.
3) Time dependence on global economy includes market strategy and raw material price.

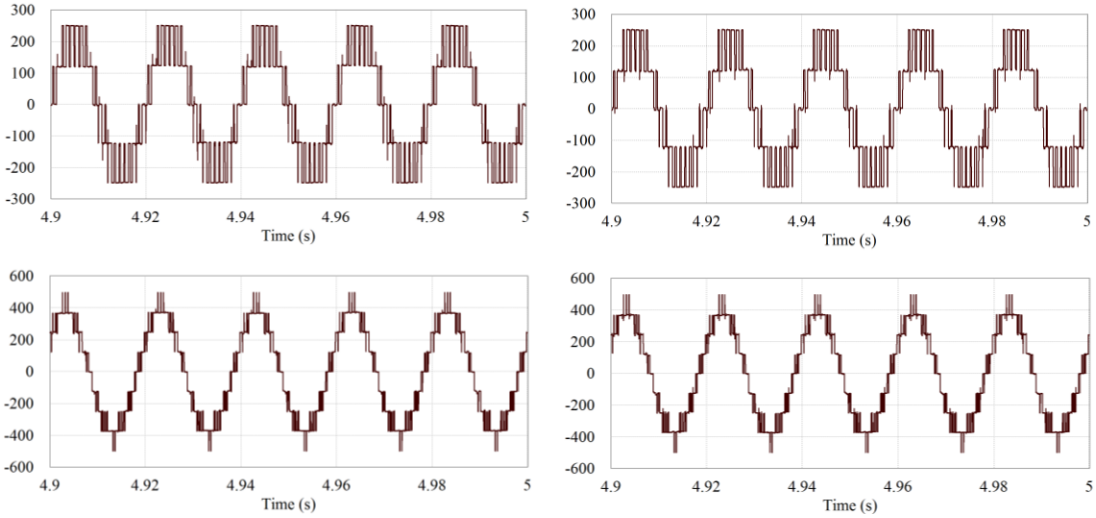
However, the cost analysis for each components used in the laboratory prototype is based on the components available in Singapore market. Besides, the approximation of the development cost is also depends on the hardware circuit design and type of material selected. With the partial cost calculation shown in Fig. 8.22, 5L-M^2T^2CI and 5L-M^2S^2CI topologies offer the less development cost with high energy efficiency for low and medium power application. While for high power application, 5L-M^2DCI topology still offers higher energy efficiency and lesser production cost as compared to the classical 5L-MDCI topology as shown in Fig. 8.22.

8.6.5 Measured Results

In order to verify the output performance of the proposed and classical 5L-inverter topologies, $500V_{dc}$ with two star connected output three-phase 50Hz load (R1 = 100Ω L1 = 122mH and R2 = 100Ω, L2 = 104mH) associated with the RC filter (Rf = 10Ω and Cf = 18µF) for the enhancement of the balancing features are simulated in PSIM with SimCoupler MATLAB dynamic tools. The control signals of the LS-PWM technique is set at modulation index, M = 0.9 and switching frequency, Fs = 1 kHz.



(a) (b)



(c) (d)

Fig. 8.23. Simulation results for the output pole voltage waveform (upper trace) and line-to-line voltage waveform (lower trace) for various 5L-inverter topologies. (a) 5L-MDCI, (b) 5L-M^2DCI, (c) 5L-M^2T^2CI and (d) 5L-M^2S^2CI.

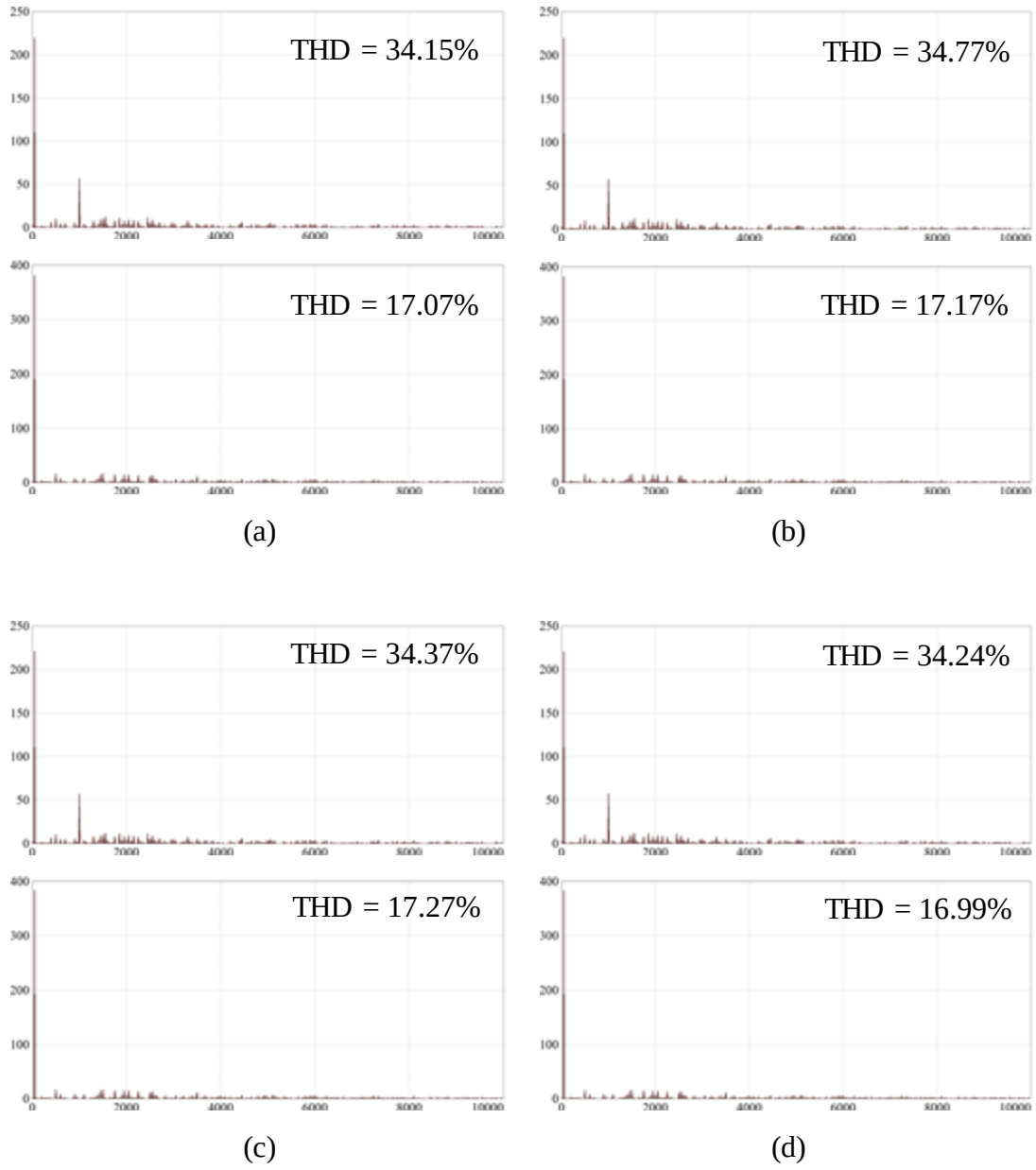


Fig. 8.24 Simulation results for the output pole voltage THD (upper trace) and line-to-line voltage THD (lower trace) for different 5L-inverter topologies. (a) 5L-MDCI, (b) 5L-M^2DCI, (c) 5L-M^2T^2CI and (d) 5L-M^2S^2CI.

The simulation results in Fig. 8.23 shows the output pole and line-to-line voltages of the respective 5L-inverter topologies. Output voltage THD performance of the respective 5L-inverters topologies is 34% for the pole voltage and 17% for the line-to-line voltage as shown in Fig. 8.24. As a result, the proposed 5L-inverter topologies have the similar output characteristic as compared to the classical 5L-MDCI topology.

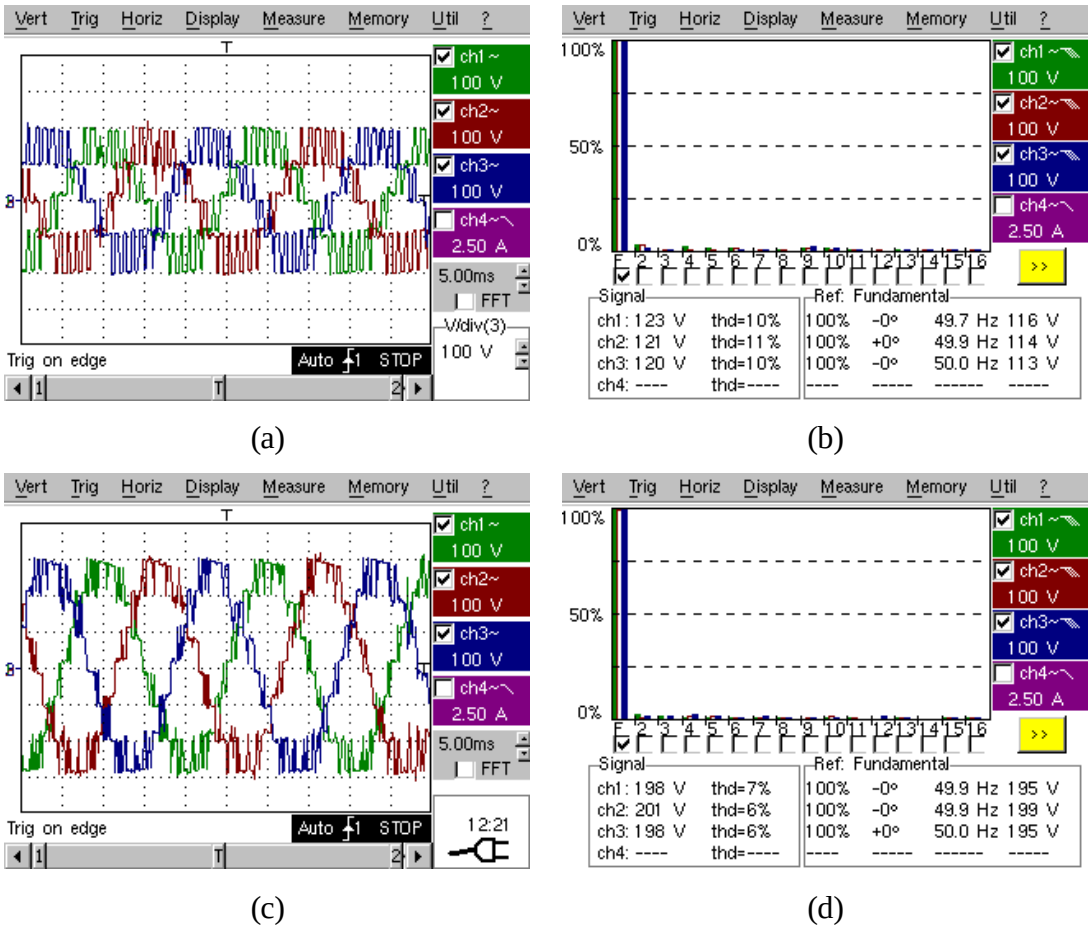


Fig. 8.25. Experimental results for the output characteristics performance of a 5L-M^{2}DCI topology. (a). Output pole voltage waveform, (b) THD of the output pole voltage, (c) output line-to-line voltage waveform, and (d) THD of the output line-to-line voltage.

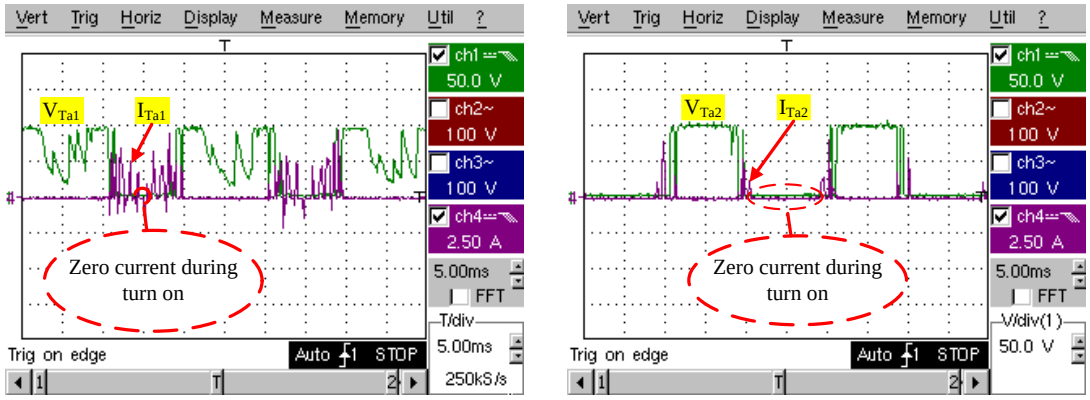


Fig. 8.26. Experimental results of the zero current switching of the inner cell switch of 5L-M^{2}DCI during switching state Ta1 = Ta2 = Ta3 = Ta4 = 1 or 0 condition. (a) Ta1 and (b) Ta2.

TABLE 8.18

PERFORMANCE PARAMETER COMPARISON OF FIVE-LEVEL INVERTERS

Five-Level Inverter Topologies	Maximum Voltage Stress Level		Cost (SGD $)	Total Loss (Watts)
	IGBT	Diode		
MDCI	$V_{dc}/4$	$3V_{dc}/4$	1074.852	7.5856
M^2DCI	$3V_{dc}/4$	$V_{dc}/4$	1083.492	7.1203
M^2T^2CI	V_{dc}	0	960.936	5.0376
M^2S^2CI	V_{dc}	$V_{dc}/4$	1004.748	6.4557

For the sake of simplicity, the experimental results are shown in Fig. 8.25 only for 5L-M^2DCI topology with 400V supply. However, the results of the output performance of other proposed 5L-inverter topologies are not listed in this report since the output features of other proposed 5L-inverters are similar to 5L-MDCI as proven in the simulation results.

In order to validate the performance of the zero current switching of the multiple-pole hierarchy, experimental results of the inner cell switches (Ta1 and Ta2) of phase ‘a’ is measured. In general, the built up voltage and current of the active switch for LS-PWM technique in multilevel inverters have the same characteristic (Example: when the switch is turning off, voltage will rise to the desired value and current falls to zero value, similarly for turning-on switching). However, in multiple-pole hierarchy, the current and voltage fall to zero value when the switch is turning on during the particular switching states condition as discussed previous subsection. Fig. 8.26 shows the experimentally obtained results of the voltage across the switch and current through the switch during one cycle period.

8.7 Discussion

A new approach of multilevel inverter topologies is based on multiple-pole approach. The proposed inverters structure can develop into different types of multiple-pole

multilevel inverter topologies such as M^2DCI, M^2T^2CI and M^2S^2CI. Among all these topologies, M^2T^2CI and M^2S^2CI have the lowest components cost as compared to MDCI and M^2DCI topologies (Fig. 8.22). However, the power rating of the converter is limited to low and medium power depending on the device rating of the manufacturer.

Mathematical analysis is provided for the device rating selection based on the voltage and current stresses. On top of that, voltage and current stress expression can be applied to the loss analysis, which proves that the conduction loss is reduced due to the zero current switching of the inner cell switch. The overall performances of the five-level inverters are compared in Table 8.36. The multiple-pole approach, higher level and energy efficient converter with optimum cost and components count can be investigated for future development associated with the proper balancing circuit on the DC side.

Chapter 9 – Proposed Single Input Multiple Output (SIMO) Balancing Circuit for Transformerless Seven-Level (7L)/Multiple-pole Multilevel Inverter Topologies

Solid state devices of high current and voltage rating are utilized in high voltage and high power application in order to tolerate high voltage/current stress. To reduce the amount of voltage or current stress on semiconductor devices, a multilevel approach with more than one switch connected in series for upper phase leg is being chosen. Low output voltage THD with low switching frequency operation can be further improve by implementing a multilevel inverter topology for more than five-level output voltage characteristics performance.

Due to its unbalanced capacitor voltage in the dc-link for seven-level inverter topologies, these topologies have not been practically used in many applications. However, several balancing methods have been reported in the literature, such as: balancing algorithm in generic n-level inverter [101] and isolated multi-winding transformer [102]. The first method requires more effort and time for engineers to design the control algorithm due to the complexity involved, and this method has not yet been verified practically. Second method is not well suited particularly for the applications where space and weight are a major concern. Although in this type, transformer provides galvanic isolation between dc and ac side of the converter, the capital cost and losses incurred are significantly high. Therefore, an active balancing circuit for seven-level inverter topologies is presented in this Chapter. The seven-level balancing circuit is known as single-input multiple outputs (SIMO) balancing circuit, which maintains six identical voltage levels in the dc bus.

In order to verify the performance of the SIMO balancing circuit, a new seven-level active-clamped multiple-pole multilevel diode-clamped inverter (7L-AM^{2}DCI) and a multiple-pole multilevel diode-clamped inverter (7L-M^{2}DCI) topologies are chosen.

9.1 Basic Operating Principle

In this section, the basic operating principle of the new seven-level inverter topologies and DC/DC balancing circuit is discussed. The derived concept of a multiple-pole hierarchy is detailed in Chapter 8 with the complete mathematical analysis. The proposed seven-level inverter topologies achieve zero current switching for particular switching state in LS-PWM technique. The realization of zero-current switching is similar to 5L multiple-pole multilevel inverter topologies. Hence, the following subsection will briefly explain the switching operation of the converters.

9.1.1 Seven-Level/Multiple-Pole Multilevel Diode-Clamped Inverter (7L-M^{2}DCI)

Fig. 9.1 shows a complete schematic diagram of per-phase three-poles half bridge 7L-M^{2}DCI topology. The mathematical analysis for the output phase voltage of phase 'a' n-level M^{2}DCI topology is presented here. A generalized equation for the output phase voltage is given as follows:

$$V_{am}(t) = \frac{V_{dc}(t)}{n-1}\left\{\sum\begin{bmatrix}\text{upper switching devices}\\ \text{per}-\text{phase leg}\end{bmatrix} - \frac{n-1}{2}\right\} \tag{9.1}$$

where n is representing the number of incremental output voltage steps for a single-phase n-level multiple-pole multilevel diode-clamped inverter (nL-M^{2}DCI). From equation (9.1), a seven-level output phase voltage as a function of switching states is written as:

$$V_{am}(t) = \frac{V_{dc}(t)}{6}\left\{T_{a1}(t) + T_{a2}(t) + T_{a5} + T_{a6} + T_{a9} + T_{a10} - 3\right\} \tag{9.2}$$

From equation (9.2), we can infer that accurate switching sequence is required to synthesize a good seven-level output. The switching states and sequence along with corresponding output phase voltage is shown in Table 9.1.

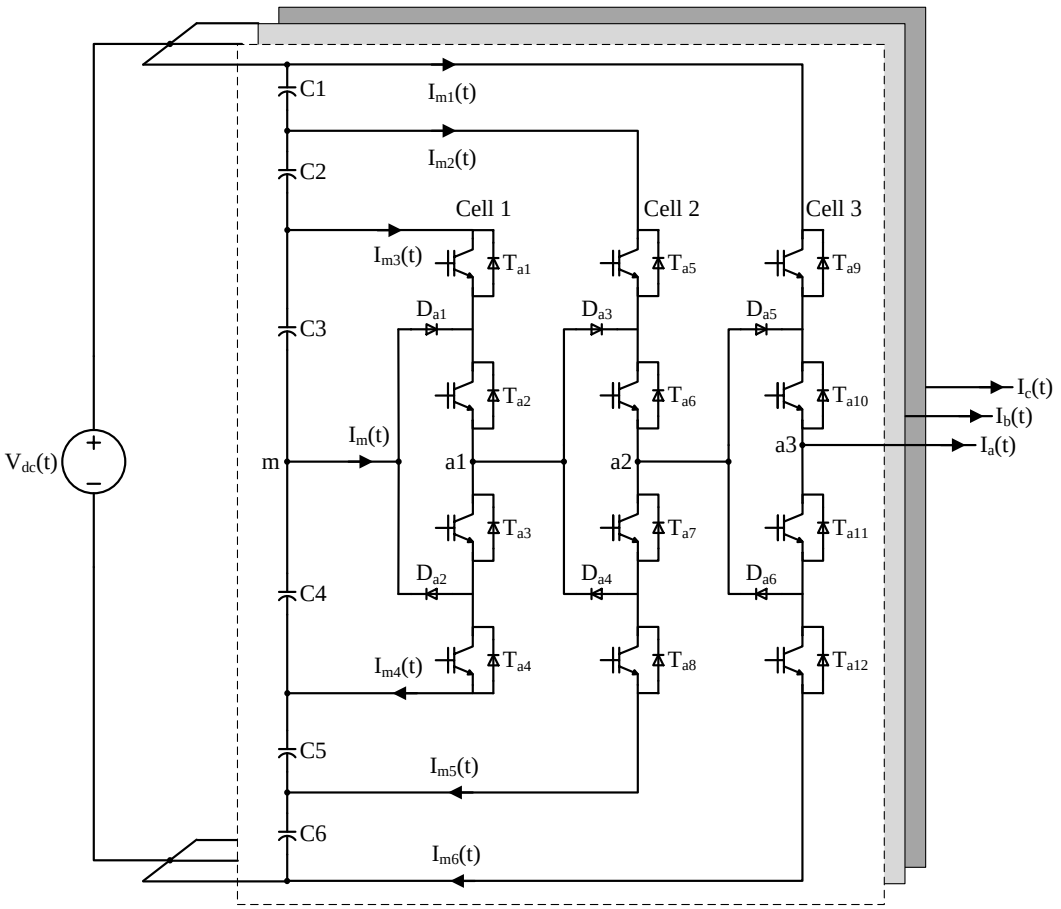


Fig. 9.1. Configuration of a three-phase seven-level/multiple-pole multilevel diode-clamped inverter (7L-M^{2}DCI).

TABLE 9.1

7L-M^{2}DCI OUTPUT VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	**Switching States**						**Pole Voltage**
	$\mathbf{T_{s1}}$	$\mathbf{T_{s2}}$	$\mathbf{T_{s5}}$	$\mathbf{T_{s6}}$	$\mathbf{T_{s9}}$	$\mathbf{T_{s10}}$	$\mathbf{V_{sm}}$
1	1	1	1	1	1	1	$V_{dc}/2$
2	1	1	1	1	0	1	$V_{dc}/3$
3	1	1	0	1	0	1	$V_{dc}/6$
4	0	1	0	1	0	1	0
5	0	0	0	1	0	1	$-V_{dc}/6$
6	0	0	0	0	0	1	$-V_{dc}/3$
7	0	0	0	0	0	0	$-V_{dc}/2$

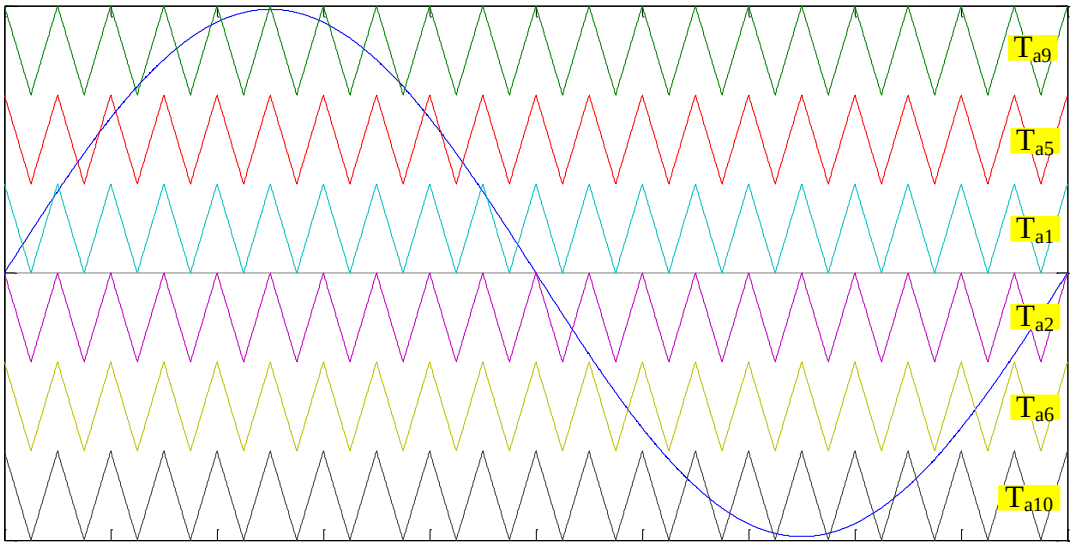


Fig. 9.2. Level-shifted PWM technique for 7L-M^{2}DCI topology.

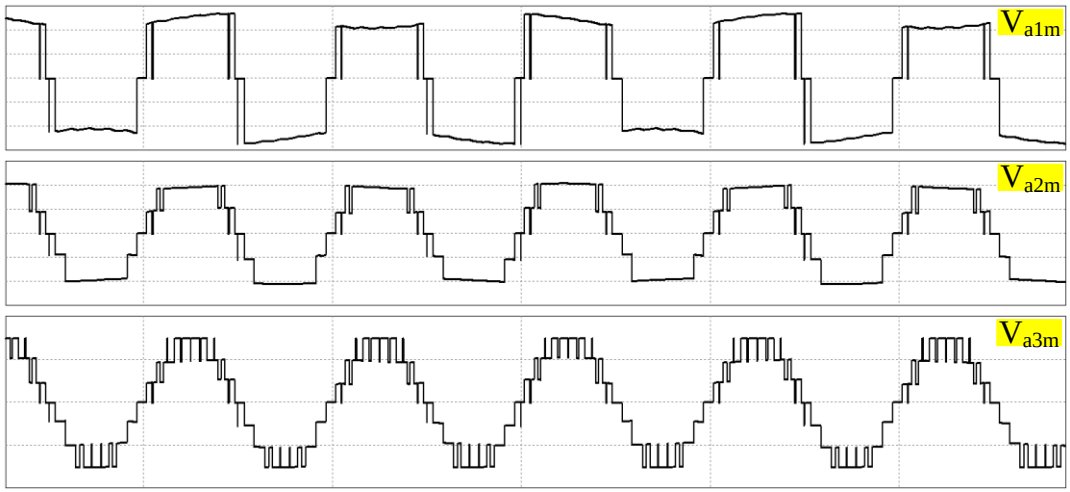


Fig. 9.3. Output pole voltage waveform of each inverter cell of a 7L-M^{2}DCI topology, across node a1 to node m of cell 1, node a2 to node m of cell 2, and node a3 to node m of cell 3 (ref., Fig. 9.1) under balanced dc-link voltage condition.

The output voltage levels for 7L-M^{2}DCI topology are obtained by comparing modulation control signal and each carrier frequency zone of Fig. 9.2. Each of the modulated signals with the respective carrier zone is fed to the respective switching device as shown in Fig. 9.2. The output pole voltage waveform of each cell in 7L-M^{2}DCI topology in Fig. 9.3 are obtained modulation index is high (e.g., reference control signals above amplitude of carrier frequency of upper most triangle wave of Fig. 9.2). In the

case of low modulation index (e.g,. reference control signals below amplitude of second top and second bottom carrier wave of Fig. 9.2) will lead to five-level output voltage waveform, which does not recommend to operate at low modulation index in this topology.

9.1.2 Seven-Level/Active-Clamped-Multiple-Pole Multilevel Diode-Clamped Inverter (7L-AM^{2}DCI)

While extending the 7L-M^{2}DCI topology concept to a 7L-AM^{2}DCI configuration of Fig. 9.4 with the same incremental output voltage level, it is important to use switches of lower rating so as to limit the conduction losses to minimum. The load terminal of this proposed topology is connected to cell 2 with a seven-level switching characteristic. Fulfilling the above mentioned design considerations; two series connected switching

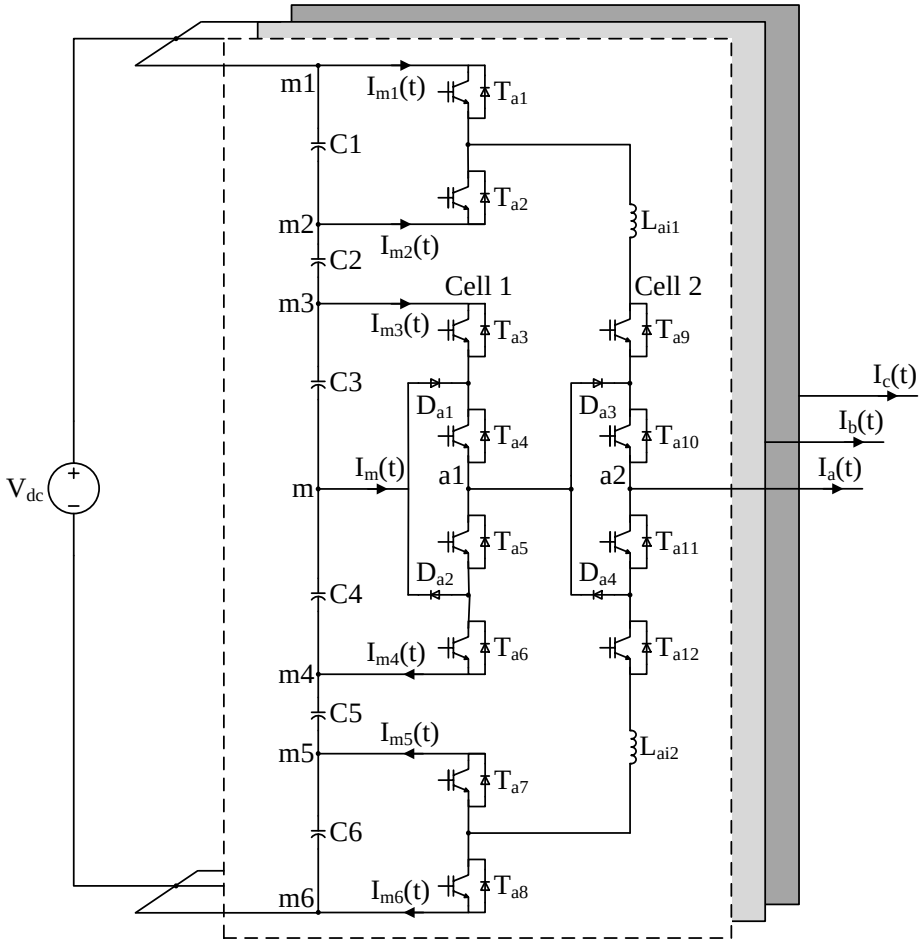


Fig. 9.4. Configuration of a three-phase seven-level/active-clamped multiple-pole multilevel diode-clamped inverter (7L-AM^{2}DCI).

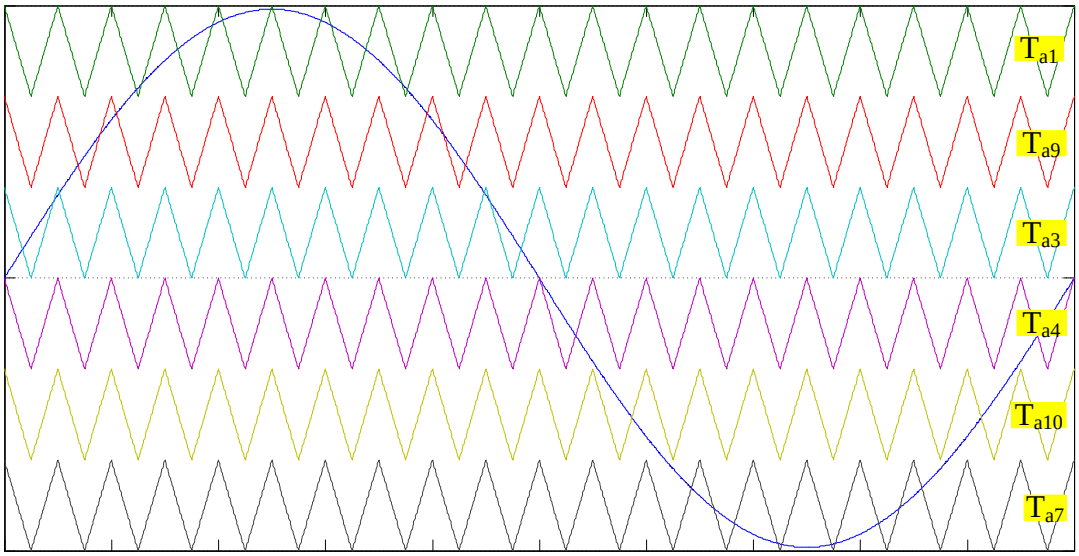


Fig. 9.5. Level-shifted PWM technique for 7L-AM^{2}DCI topology.

TABLE 9.2

7L-AM^{2}DCI OUTPUT VOLTAGE LEVEL AND CORRESPONDING SWITCHING STATES

States	**Switching States**						**Pole Voltage**
	T_{s1}	T_{s3}	T_{s4}	T_{s7}	T_{s9}	T_{s10}	V_{sm}
1	1	1	1	1	1	1	$V_{dc}/2$
2	0	1	1	1	1	1	$V_{dc}/3$
3	0	1	1	1	0	1	$V_{dc}/6$
4	0	0	1	1	0	1	0
5	0	0	0	1	0	1	$-V_{dc}/6$
6	0	0	0	1	0	0	$-V_{dc}/3$
7	0	0	0	0	0	0	$-V_{dc}/2$

devices are directly connected to each dc capacitors of C1 and C6 through a small inductance (L_{ai1} and L_{ai2}). The purpose of connecting an inductor in between the active switch clamp of C1 and C6 and cell 2 – NPC inverter is to prevent circulating current which causes high voltage stress across each IGBT devices.

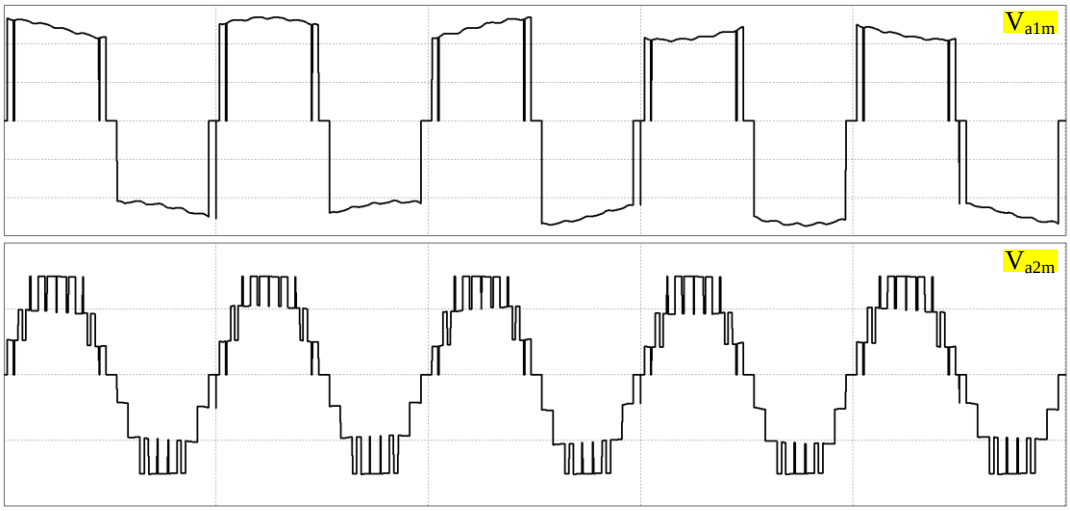


Fig. 9.6. Output pole voltage waveform of each inverter cell of a 7L-AM^{2}DCI topology, across node a1 to node m of cell 1, and node a2 to node m of cell 2 under (ref., Fig. 9.4) balanced dc-link voltage condition.

Similar switching strategy is applied, as in Fig. 9.5 and is used in Fig. 9.4. This generates multiple gate signals required to synthesize seven-level switching characteristic. The PWM signals are generated by the comparison of carrier frequency with three sinusoidal waveforms shifted in phase by 120° with each other. The PWM signals are connected to each switching devices T_{a1}-T_{a12} respectively. Note that the upper most gating signal and bottom most gating signal are connected to the switching devices of T_{a1} and T_{a7} respectively (similarly for phase 'b' and 'c').

Based on the switching sequence shown in Fig. 9.5, the seven-level output voltage steps with the corresponding gating signals per-phase are listed in Table 9.2 and output pole voltage waveform of each cell in 7L-AM^{2}DCI topology is shown in Fig. 9.6.

Referring to Table 9.2, the final output distinct voltage levels with the corresponding switching function of a per-phase configuration can be written as:

$$V_{am}(t) = \frac{V_{dc}(t)}{6}\left\{T_{a1}(t) + T_{a3}(t) + T_{a4} + T_{a7} + T_{a9} + T_{a10} - 3\right\} \tag{9.3}$$

9.1.3 Single Input Multiple Output (SIMO) Voltage Balancing Circuit

The proposed voltage balancing circuit is shown in Fig. 9.7. The voltage balancing circuit is comprised of three dc/dc converters. Two identical balancing converters are connected to the upper two dc capacitors (C1 and C2) and lower two dc capacitors (C5 and C6). This two balancing converters are operated at half the duty cycle in order to distribute equal dc voltage across C1 and C2 for upper converter and C5 and C6 for the lower converter. The dc capacitors connected to the neutral-point are connected to a dual-buck/boost converter to obtain a balance dc voltage across C3 and C4. Accurate switching periods are required for the switching devices for obtaining equalized voltage across C3 and C4. These capacitors operate with step down voltage functionality. These switches are operated at one-third the duty cycle of the inverter switches. Q_{inner1} and Q_{inner4} are connected to switching devices Q_{inner2} and Q_{inner3} for the step down voltage operating mode. The duty cycle for switching devices $Q_{inner1}$and Q_{inner4} can be expressed as:

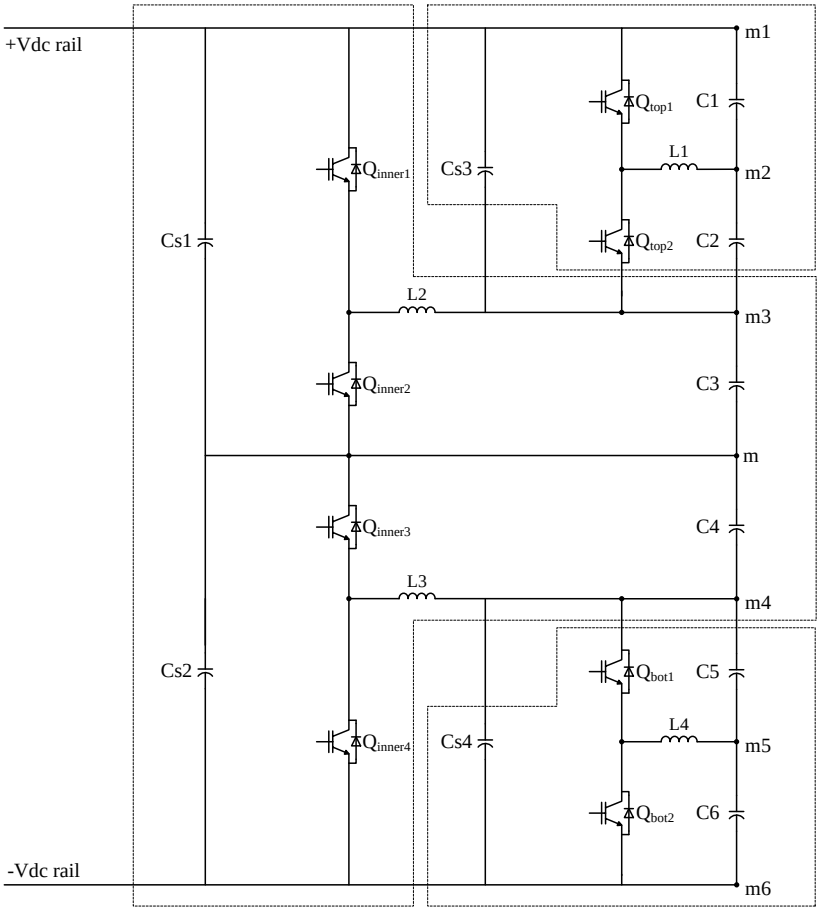


Fig. 9.7. Single input multiple output (SIMO) balancing circuit.

$$\frac{V_{C3}}{V_{Cs1}} = \frac{V_{C4}}{V_{Cs2}} = d_{inner} \approx \frac{1}{3} \tag{9.4}$$

where d_{inner} is the duty cycle of dual-buck-boost balancing converter. As it can be seen from equation (9.4), the voltage across dc capacitor (C3-C4) is one-third the main dc-link voltage. The voltage transfer gain (V_{C3}/V_{dc}) is equal to the duty ratio of the inner dual-buck/boost balancing converter.

The voltage across the capacitors (C3 and C4) connected to neutral point m in Fig. 9.7 is one third of half the dc-link voltage. Then the voltage across the node (m1, m3) and (m4, m6) is also two-third of half the dc-link voltage. This is due to the transfer of energy from higher potential (C1, C2) to lower potential (C3, C4). From Fig. 9.7, the voltage transfer gain for the upper converters and lower converter can be expressed as:

$$\begin{cases} \dfrac{V_{C1}}{V_{Cs3}} = \dfrac{V_{C2}}{V_{Cs3}} = d_{top} \approx \dfrac{1}{2} \\ \dfrac{V_{C5}}{V_{Cs4}} = \dfrac{V_{C6}}{V_{Cs4}} = d_{bot} \approx \dfrac{1}{2} \end{cases} \tag{9.5}$$

where d_{top} and d_{bot} are the duty ratios of the upper converter of C1 and C2, and lower converter of C5 and C6 respectively. The switching sequence for the voltage balancing circuit is shown in Fig. 9.8.

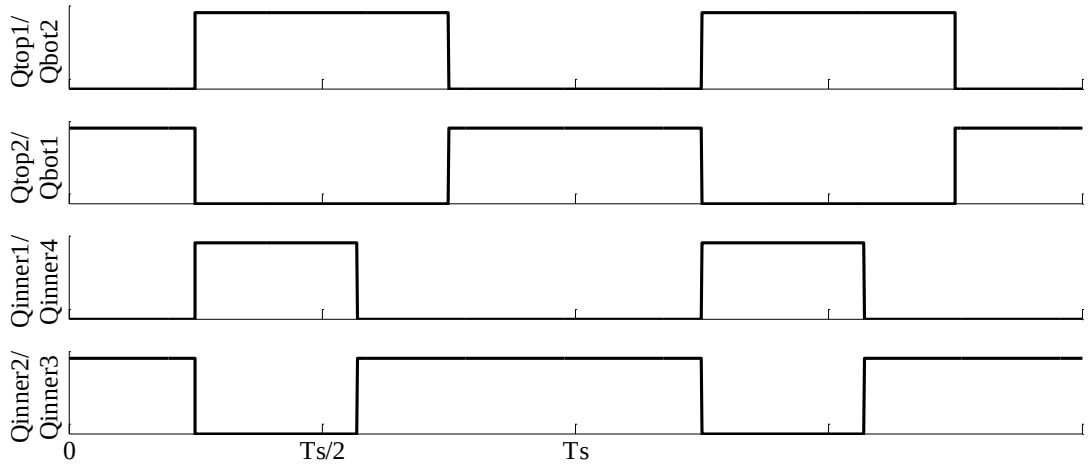


Fig. 9.8. Single input multiple output (SIMO) balancing circuit.

9.2 Device Stress

In order to provide a general guideline of the components selection for the minimum safety operation of the 7L-converters design, the stresses of the active components of the converters are calculated analytically with dependence on the switching states operation. The analytical approximation of the current stress for each active component is not provided in this Chapter. However, the analytical derivation the current stresses can be done by using the global and local current stresses approximation, which is detailed in Chapter 8.

9.2.1 Voltage Stress on 7L-M^{2}DCI Topology

Voltage stress on inverter switches for 7L-M^{2}DCI topology can be written as:

$$\begin{cases} V_{Ta1}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a1}(t)\right] \\ V_{Ta2}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a2}(t)\right] \\ V_{Ta3}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a3}(t)\right] \\ V_{Ta4}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a4}(t)\right] \end{cases} \tag{9.6}$$

Similarly, the voltage stress for each of the IGBT devices on cell 2 can be written as:

$$\begin{cases} V_{Ta5}(t) = \dfrac{V_{dc}(t)}{3}\left[1 - T_{a5}(t)\right] \cdot \left[1 - \dfrac{1}{2} T_{a6}(t)\left[T_{a1}(t) + T_{a2}(t) - 1\right]\right] \\ V_{Ta6}(t) = \dfrac{V_{dc}(t)}{3}\left[1 - T_{a6}(t)\right] \\ V_{Ta7}(t) = \dfrac{V_{dc}(t)}{3}\left[1 - T_{a7}(t)\right] \\ V_{Ta8}(t) = \dfrac{V_{dc}(t)}{3}\left[1 - T_{a8}(t)\right] \cdot \left[1 - \dfrac{1}{2} T_{a7}(t)\left[T_{a3}(t) + T_{a4}(t) - 1\right]\right] \end{cases} \tag{9.7}$$

and voltage stress across each IGBT on cell 3 can be written as:

$$\begin{cases} V_{Ta9}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a9}(t)\right]\cdot\left[1-\dfrac{1}{3}T_{a10}(t)\left[T_{a1}(t)+T_{a2}(t)+T_{a5}(t)+T_{a6}(t)-2\right]\right] \\ V_{Ta10}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a10}(t)\right] \\ V_{Ta11}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a11}(t)\right] \\ V_{Ta12}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a12}(t)\right]\cdot\left[1-\dfrac{1}{3}T_{a11}(t)\left[T_{a3}(t)+T_{a4}(t)+T_{a7}(t)+T_{a8}(t)-2\right]\right] \end{cases}$$

(9.8)

From equations (9.6), (9.7) and (9.8), a generalized mathematical expression for voltage stress on each IGBT for above cell 2 can be formulated as:

$$\begin{cases} V_{Ta(5+4i)}(t)=\dfrac{V_{dc}(t)}{n-1}\left[1-T_{a(5+4i)}(t)\right]\cdot\left\{[i+2]-T_{a(6+4i)}(t)\left[\begin{matrix}T_{a1}(t)+T_{a2}(t)-i-1\\ +\sum_{m\neq 0}^{i}\left[\begin{matrix}T_{a(1+4m)}(t)\\ +T_{a(2+4m)}(t)\end{matrix}\right]\end{matrix}\right]\right\} \\ V_{Ta(6+4i)}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a(6+4i)}(t)\right] \\ V_{Ta(7+4i)}(t)=\dfrac{V_{dc}(t)}{2}\left[1-T_{a(7+4i)}(t)\right] \\ V_{Ta(8+4i)}(t)=\dfrac{V_{dc}(t)}{n-1}\left[1-T_{a(8+4i)}(t)\right]\cdot\left\{[i+2]-T_{a(7+4i)}(t)\left[\begin{matrix}T_{a3}(t)+T_{a4}(t)-i-1\\ +\sum_{m\neq 0}^{i}\left[\begin{matrix}T_{a(3+4m)}(t)\\ +T_{a(4+4m)}(t)\end{matrix}\right]\end{matrix}\right]\right\} \end{cases}$$

(9.9)

where n and i are the incremental voltage level and number of cell count for nth-level M^2DCI converter respectively. The range of any incremental cell I can be determined as:

TABLE 9.3

7L-M^{2}DCI VOLTAGE STRESS AND CORRESPONDING SWITCHING STATES

Voltage Stress (Volts)	**States**						
	1	**2**	**3**	**4**	**5**	**6**	**7**
V_{Ta1}	0	0	0	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_{Ta2}	0	0	0	0	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_{Ta3}	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	0	0	0	0
V_{Ta4}	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	0	0	0
V_{Ta5}	0	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/3$
V_{Ta6}	0	0	0	0	0	$V_{dc}/3$	$V_{dc}/3$
V_{Ta7}	$V_{dc}/3$	$V_{dc}/3$	0	0	0	0	0
V_{Ta8}	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0	0
V_{Ta9}	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$	$2V_{dc}/3$	$5V_{dc}/6$	$V_{dc}/2$
V_{Ta10}	0	0	0	0	0	0	$V_{dc}/2$
V_{Ta11}	$V_{dc}/2$	0	0	0	0	0	0
V_{Ta12}	$V_{dc}/2$	$5V_{dc}/6$	$2V_{dc}/3$	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0

$$\min\langle 0\rangle \le i \le \max\left\langle \frac{n-5}{2} \right\rangle \tag{9.10}$$

Applying equations (9.6) to (9.9), the maximum voltage stress on each IGBT for 7L-M^{2}DCI configuration is listed in Table 9.3 with the corresponding switching states. From Table 9.3, the maximum voltage stress level for each of the inverter switches in 7L-M^{2}DCI topology is described in the following parameters:

$$\begin{cases} V_{Ta1}(t) = V_{Ta2}(t) = V_{Ta3}(t) = V_{Ta4}(t) = V_{dc}(t)/6 \\ V_{Ta5}(t) = V_{Ta8}(t) = V_{Ta10}(t) = V_{Ta11}(t) = V_{dc}(t)/2 \\ V_{Ta6}(t) = V_{Ta7}(t) = V_{dc}(t)/3 \\ V_{Ta9}(t) = V_{Ta12}(t) = 5V_{dc}(t)/6 \end{cases} \quad (9.11)$$

9.2.2 Voltage Stress on 7L-AM^{2}DCI Topology

The voltage stress across each of the switching devices in the clamping circuit and cell-1 NPC inverter can be estimated as:

$$\begin{cases} V_{Ta1}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a1}(t)\right] \\ V_{Ta2}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a2}(t)\right] \\ V_{Ta3}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a3}(t)\right] \\ V_{Ta4}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a4}(t)\right] \\ V_{Ta5}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a5}(t)\right] \\ V_{Ta6}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a6}(t)\right] \\ V_{Ta7}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a7}(t)\right] \\ V_{Ta8}(t) = \dfrac{V_{dc}(t)}{6}\left[1 - T_{a8}(t)\right] \end{cases} \quad (9.12)$$

The voltage stress across each switching device on cell-2 NPC inverter can be estimated by measuring the voltage across the switching devices (T_{a5}-T_{a8}). Each IGBT in cell-2 NPC inverter will experience distinct voltage stress level depending on the conduction period of each IGBT.

The voltage across collector and node m ($V_{c5m(Ta5)}$, $V_{c6m(Ta6)}$, $V_{c7m(Ta7)}$ and $V_{c8m(Ta8)}$) of each series connected IGBT devices in cell-2 NPC inverter can be calculated as a function of switching states shown in the following equation (9.13):

$$\begin{cases} V_{c9m(Ta9)}(t) = \dfrac{V_{dc}(t)}{6}\left[2+T_{a1}(t)\right]\left[1-T_{a9}(t)\right] \\ V_{c10m(Ta10)}(t) = \dfrac{V_{dc}(t)}{6}\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a10}(t)\right] \\ V_{c11m(Ta11)}(t) = \dfrac{V_{dc}(t)}{6}\left[2+T_{a1}(t)\right]\left[1-T_{a11}(t)\right] \\ V_{c12m(Ta12)}(t) = \dfrac{V_{dc}(t)}{6}T_{a11}(t)\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a12}(t)\right] \end{cases} \quad (9.13)$$

The voltage across emitter and node m ($V_{e5m(Ta5)}$, $V_{e6m(Ta6)}$, $V_{e7m(Ta7)}$ and $V_{e8m(Ta8)}$) of each series connected IGBT devices in cell-2 NPC inverter can be calculated as a function of switching states shown in the following equation (9.14):

$$\begin{cases} V_{e9m(Ta9)}(t) = \dfrac{V_{dc}(t)}{6}T_{a10}(t)\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a9}(t)\right] \\ V_{e10m(Ta10)}(t) = \dfrac{V_{dc}(t)}{6}\left[T_{a7}(t)-3\right]\left[1-T_{a10}(t)\right] \\ V_{e11m(Ta11)}(t) = \dfrac{V_{dc}(t)}{6}\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a11}(t)\right] \\ V_{e12m(Ta12)}(t) = \dfrac{V_{dc}(t)}{6}\left[T_{a7}(t)-3\right]\left[1-T_{a12}(t)\right] \end{cases} \quad (9.14)$$

The above equations (9.13) and (9.14) do not consider the voltage drop across the inductors as it is negligible when compared to the dc-link voltage. A low switching frequency at 1 kHz does not create any voltage spike with slow rate of voltage change (dv/dt). The voltage stress across each IGBT of cell-2 NPC inverter is obtained in (9.15) by subtracting (9.13) and (9.14).

TABLE 9.4

7L-AM^{2}DCI VOLTAGE STRESS AND CORRESPONDING SWITCHING STATES

Voltage Stress (Volts)	**States**						
	1	**2**	**3**	**4**	**5**	**6**	**7**
V_{Ta1}	0	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_{Ta2}	$V_{dc}/6$	0	0	0	0	0	0
V_{Ta3}	0	0	0	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_{Ta4}	0	0	0	0	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$
V_{Ta5}	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	0	0	0	0
V_{Ta6}	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	0	0	0
V_{Ta7}	0	0	0	0	0	0	$V_{dc}/6$
V_{Ta8}	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	$V_{dc}/6$	0
V_{Ta9}	0	0	$V_{dc}/6$	$V_{dc}/3$	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/3$
V_{Ta10}	0	0	0	0	0	$V_{dc}/6$	$V_{dc}/3$
V_{Ta11}	$V_{dc}/3$	$V_{dc}/6$	0	0	0	0	0
V_{Ta12}	$V_{dc}/3$	$V_{dc}/3$	$V_{dc}/2$	$V_{dc}/3$	$V_{dc}/6$	0	0

$$\begin{cases} V_{Ta9}(t) = \dfrac{V_{dc}(t)}{6}\left[1-T_{a9}(t)\right]\left\{2+T_{a1}(t)-T_{a10}(t)\left[T_{a3}(t)+T_{a4}(t)-1\right]\right\} \\ V_{Ta10}(t) = \dfrac{V_{dc}(t)}{6}\left\{\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a10}(t)\right]-\left[T_{a7}(t)-3\right]\left[1-T_{a10}(t)\right]\right\} \\ V_{Ta11}(t) = \dfrac{V_{dc}(t)}{6}\left\{\left[2+T_{a1}(t)\right]\left[1-T_{a11}(t)\right]-\left[T_{a3}(t)+T_{a4}(t)-1\right]\left[1-T_{a11}(t)\right]\right\} \\ V_{Ta12}(t) = \dfrac{V_{dc}(t)}{6}\left[1-T_{a12}(t)\right]\left\{3-T_{a7}(t)+T_{a11}(t)\left[T_{a3}(t)+T_{a4}(t)-1\right]\right\} \end{cases}$$

(9.15)

Based on the above equations (9.12) and (9.15), a maximum voltage stress level for each of the switches with their respective switching states is listed in Table 9.4. From Table 9.4 it can be inferred that each of the 7L-AM^{2}DCI switches have a different maximum voltage stress level. For optimum efficiency and performance, IGBTs with suitable voltage ratings have to be selected.

From Table 9.4, the maximum voltage stress level for each of the inverter switches in 7L-AM^{2}DCI topology is described in the following parameters:

$$\begin{cases} V_{Ta1}(t) = V_{Ta2}(t) = V_{Ta3}(t) = V_{Ta4}(t) = V_{dc}(t)/6 \\ V_{Ta5}(t) = V_{Ta6}(t) = V_{Ta7}(t) = V_{Ta8}(t) = V_{dc}(t)/6 \\ V_{Ta9}(t) = V_{Ta12}(t) = V_{dc}(t)/2 \\ V_{Ta10}(t) = V_{Ta11}(t) = V_{dc}(t)/3 \end{cases} \tag{9.16}$$

9.2.3 Voltage Stress on SIMO Balancing Circuit

The voltage stress of the IGBT in SIMO balancing circuit is calculated based on voltage ripple free across each dc capacitor and zero voltage drops across each buck/boost inductor and the voltage stress of the switching device are approximated as:

$$\begin{cases} V_{Qinner1}(t) = V_{Qinner2}(t) = V_{Qinner3}(t) = V_{Qinner4}(t) = V_{dc}(t)/2 \\ V_{Qtop1}(t) = V_{Qtop2}(t) = V_{Qbot1}(t) = V_{Qbot2}(t) = V_{dc}(t)/3 \end{cases} \tag{9.17}$$

9.3 Experimental Results

A down-scale experimental setup is shown in Fig. 9.9 was used to demonstrate the balancing capacitors voltage of SIMO balancing circuit on 7L-inverter with low power load. The parameter of the laboratory prototype is listed as follows:

[1] DC supply, V_{dc} = 100V

[2] Switching frequency, F_s = 1kHz

[3] Modulation frequency, F = 50Hz

[4] Switching frequency of balancing circuit, F_b = 5kHz

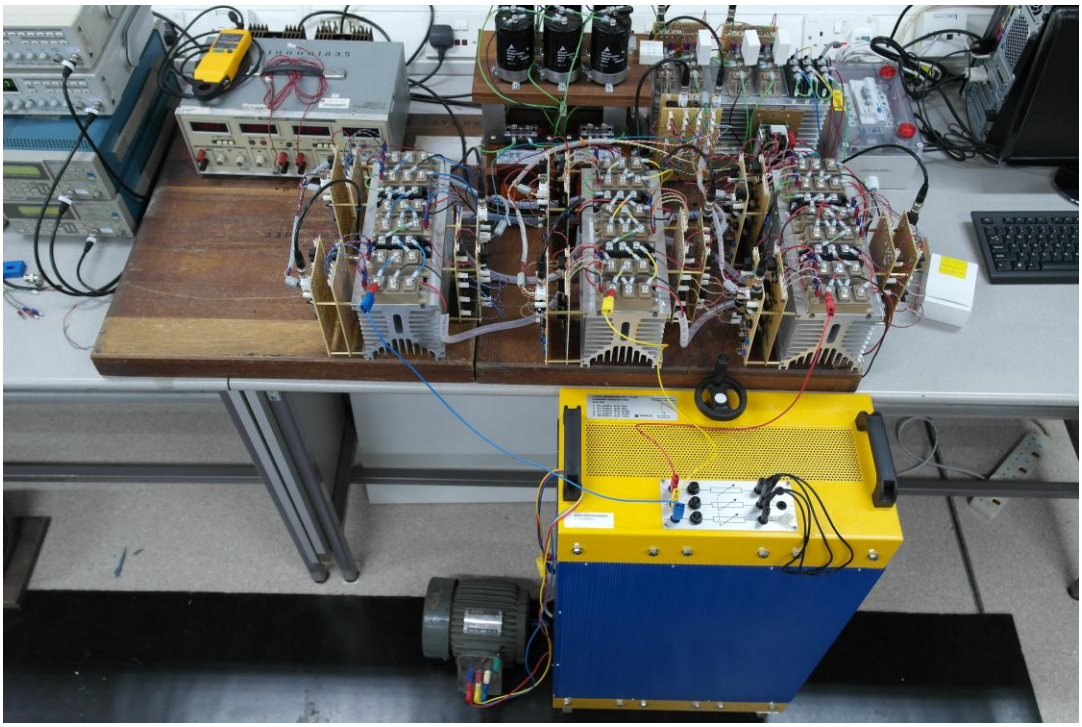


Fig. 9.9. Experimental setup on 7L inverter configuration with SIMO balancing circuit.

[5] Resistive load, R = 150Ω

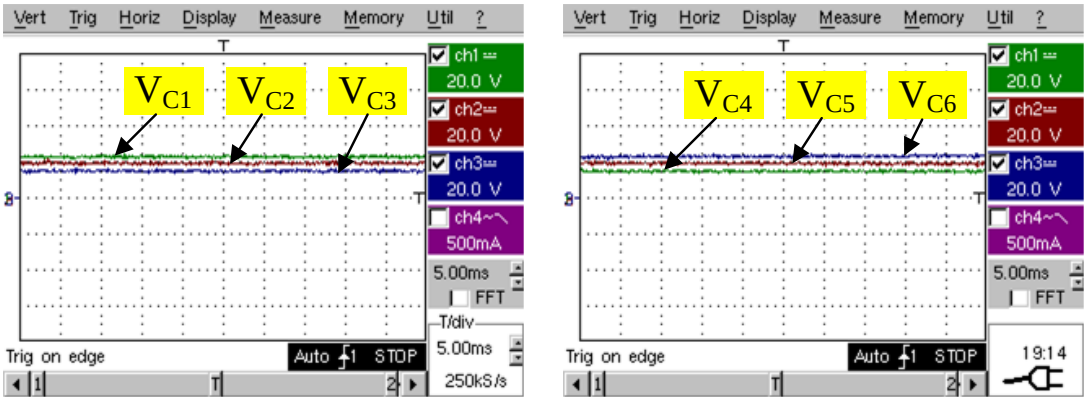
[6] Inductive load, L = 122mH

[7] Balancing inductor, L1 = L2 = L3 = L4 = 5mH

[8] DC capacitor, C1 = C2 = C3 = C4 =C5 =C6 = 2200μF

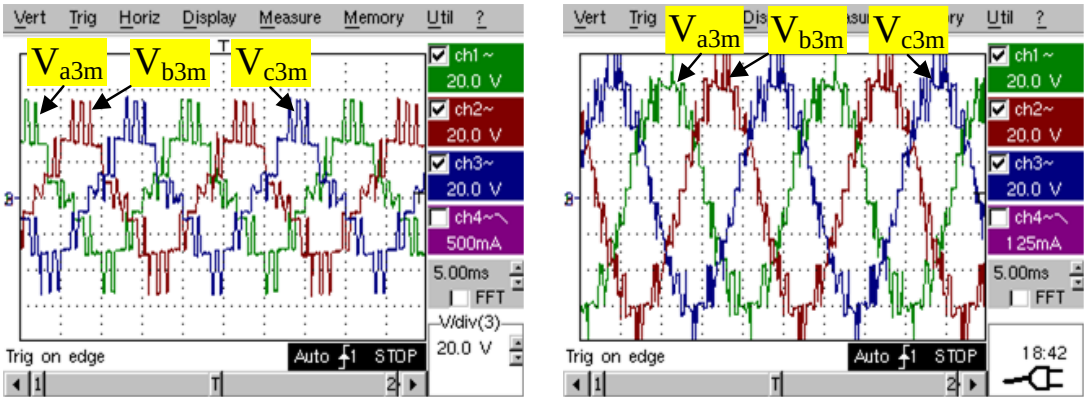
The output resistive and inductive loads of the inverter are connected in series and finally form a star configuration for three-phase system.

Fig. 9.10 shows the output voltage waveform of the SIMO balancing circuit. The dc capacitor voltages are almost equalized for an open loop control. However, there is a significant small error between the actual dc capacitor voltage value and desired value. This is due to the unregulated duty cycle of the SIMO balancing circuit, which is manually set at a fix duty cycle by using the function generator. But in this thesis, a 7L SIMO balancing circuit with the open loop system is used to demonstrate the concept of the equal capacitor voltage is able to achieve with the proposed circuit diagram in Fig. 9.6.



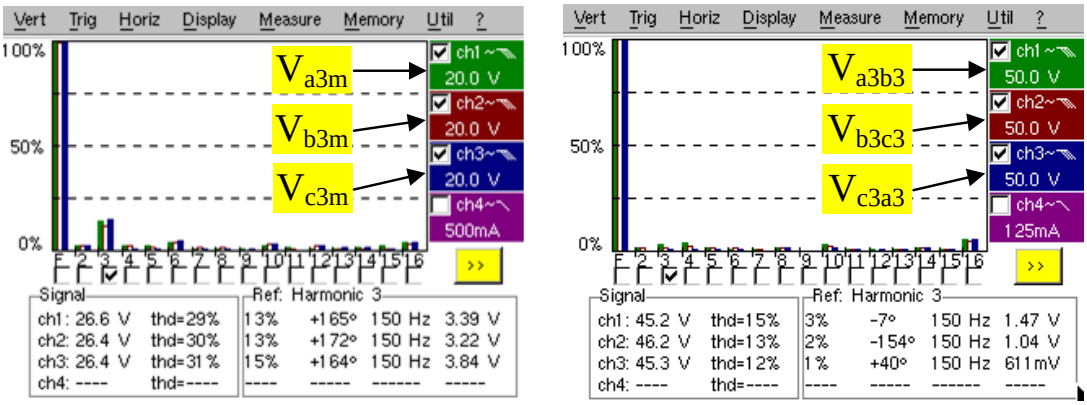
(a) (b)

Fig. 9.10. Experimental results of the dc-link voltage waveform for upper three dc capacitors (V_{c1}, V_{c2} and V_{c3}) and lower three dc capacitors (V_{c4}, V_{c5} and V_{c6}) of the output SIMO balancing circuit.



(a) (b)

Fig. 9.11. Experimental results of the output voltage waveform of the 7L-M^{2}DCI topology. (a) Pole voltage and (b) line-to-line voltage.



(a) (b)

Fig. 9.12. Experimental results of the output voltage THD of the 7L-M^{2}DCI topology. (a) Pole voltage and (b) line-to-line voltage.

With the balancing circuit connected at the input terminal of the 7L-M^{2}DCI topology, the output voltage waveform of the 7L-M^{2}DCI is shown in Fig. 9.11. Output THD value of the line-to-line voltage terminal (ref. to Fig. 9.11(b)) is noted to be less distorted due to the thirteen-level incremental voltage steps (shown in Fig. 9.12 (b)), as well as the THD of the output pole voltage (shown in Fig. 9.12 (a)). The voltage quality of a three-phase 7L-inverter is improved due to low THD is observed in the output voltage waveform with components count reduction.

9.4 Discussion

This Chapter presents a new balancing circuit for 7-level inverter topology with a multi input dc capacitors components connected in series in a single dc-link configuration. The balancing circuit is able to provide six distinct voltage levels for the 7L-inverter topologies.

Besides, two proposed 7L-inverter topologies (M^{2}DCI and AM^{2}DCI) are discussed in this Chapter. By comparing both proposed inverter topologies, 7L-AM^{2}DCI topology is able to limit the circulating current to the minimum and provide low voltage stress across the IGBT devices. However, six discrete inductive components are required to prevent any voltage spike occurring across the switches. However, the size of the high frequency inductors can be reduced by using the mutual inductor (4 terminals with single core) design. Therefore, a significant improvement is needed for the future development, such as: balancing control algorithm for the SIMO balancing circuit and inductive components design with different materials and configuration.

Chapter 10 – Bidirectional and Unidirectional Five-Level/Multiple-Pole Multilevel Rectifier Topologies for High Power Factor Performance

Maintaining high quality of utility power supply is very important for the AC bus when a single-phase or three-phase non-linear electronic load is installed. Non-linear electronic loads like rectifiers system are frequently carried out with the power factor correction (PFC) to make sure the input grid voltage and current are operating at the same phase angle, as well as achieving low input current distortion. The power electronic supply for high power electrical drive is usually implemented through two stages of energy conversion. The first stage of energy conversion is the main ac voltage converted into the dc voltage level and then the load voltage can be adapted with the dc-dc converter with or without galvanic isolation for the AC electrical drive of the inverter side. Often only three conductors are connected to the first stage of the AC-DC conversion without any neutral conductor, which can be known as three-phase three wire rectifier system.

In some application, three-phase/three-wire single stage energy conversion system has implemented for medium and high power electrical drive such as the VIENNA rectifier as presented in Chapters 3 and 7. However, the boost inductors at the input side of this rectifier occupy a significant amount of space. Although the voltage stress across the power devices are half of the dc-link voltage, which allow the high switching frequency rectifier to operate at higher power density as compared to the conventional two-level rectifier or diode bridge rectifier. But in term of low switching frequency operation for high power inductive component with minimum cost implementation, volume and weight of the rectifier is required to optimize.

Therefore, proposed new bidirectional and unidirectional five-level multilevel rectifier based on multiple-pole approach is presented in this chapter to optimize the inductive component with the low switching frequency operation. The derivation of multiple-pole concept has discussed in chapter 8 and [103].

10.1 Operating Principle of Five-Level AC/DC Topologies

This section presents the operating principle of two different 5L PWM AC/DC based on the multiple-pole approach for bidirectional and unidirectional rectifiers. The 5L PWM inverter can be retrofit as a load for the 5L AC/DC/AC drive with unity power factor operation. The derivation of the proposed M^{2}DCR and M^{2}SCR topologies are explained in the following subsection.

10.1.1 Proposed Bidirectional Front-End 5L-M^{2}DCR in AC/DC/AC drive

The proposed bidirectional 5L-M^{2}DCR topology used in an AC/DC/AC drive with a 5L-M^{2}DCI topology as a dynamic load are presented in Fig. 10.1. This back-to-back topology requires only eight power diodes in each phase to achieve same input and output quality as the classical five-level diode-clamped converter presented in [91]. However, when the number of cell on this proposed topology increases, a total number of 6(n-3) diode components are reduced.

Five-level voltage stepped waveform of the input rectifier side is achieved with the same switching positions of 5L-M^{2}DCI topology as describe in Chapter 8. The incremental

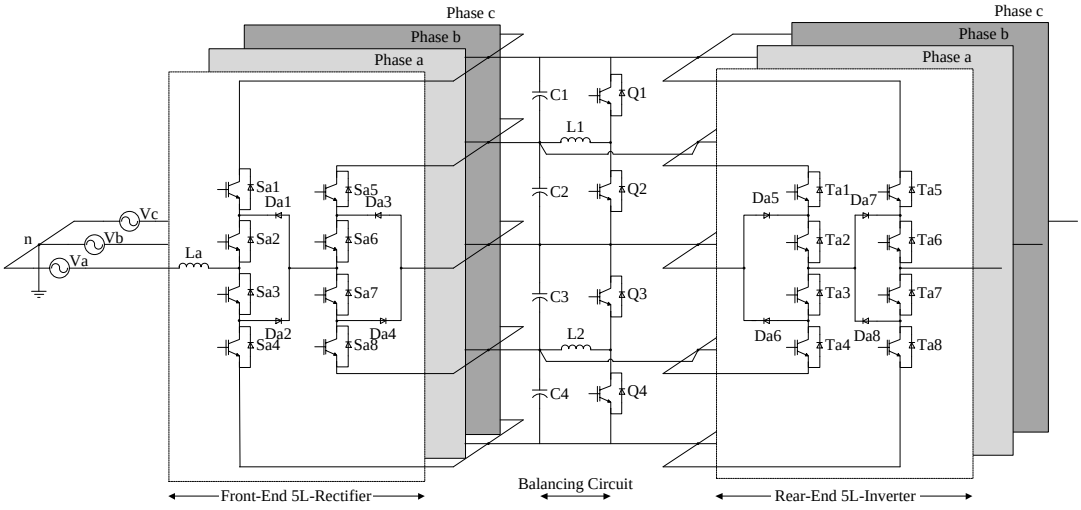


Fig. 10.1. Proposed bidirectional 5L-M^{2}DCR at the front-end side of the AC/DC/AC drive.

TABLE 10.1

SWITCHING LOGIC FOR RESPECTIVE IGBT IN FRONT-END 5L-M^{2}DCR TOPOLOGY

Vom / Switch	Vdc/2 (Sector II)	Vdc/4 (Sector I & III)	0 (Sector I, III, IV & VI)	-Vdc/4 (Sector IV & VI)	-Vdc/2 (Sector V)
Sa1, Ta1	1	0	0	0	0
Sa2, Ta2	1	1	1	1	0
Sa3, Ta3	0	1	1	1	1
Sa4, Ta4	0	0	0	0	1
Sa5, Ta5	1	1	0	0	0
Sa6, Ta6	1	1	1	0	0
Sa7, Ta7	0	0	1	1	1
Sa8, Ta8	0	0	0	1	1

input voltage step level can be classified into different sectors and switching states as shown in Table 10.1.

10.1.2 Proposed Unidirectional Front-End 5L-M^{2}SCR in AC/DC/AC drive

A bidirectional front-end rectifier is not necessary needed for load application such as propulsion, compressor or other contain non-regenerative braking system. Thus, a proposed unidirectional multilevel rectifier is re-configured and modified from Fig. 10.1 by arranging and replacing the semiconductor devices to form a unidirectional power flow.

By observing the current flow through two IGBTs and diode (i.e. Sa1, Sa2 and Da1 of phase ‘a’) connected at the T-junction of the upper phase ‘a’ with the unidirectional power flow operation, the current flow through the respective device is determined by

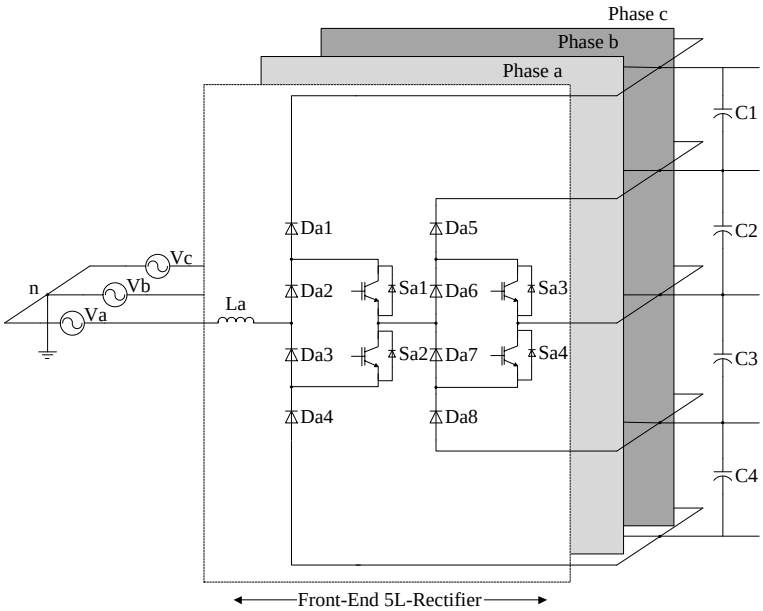


Fig. 10.2. Proposed unidirectional five-level/multiple-pole multilevel switch-clamped rectifier (5L-M^{2}SCR).

the switching states as stated in Table 10.1, as well as the polarity of the grid current (For example: When Da1 is conducting, Sa1 = 0 and Sa2 = 1, current can either flow through Da1 or Da2 depending on the polarity of the grid current. When Da1 is off, Sa1 = Sa2 = 1, current will charge to the filter dc capacitor by passing through Sa1 and Sa2). Based on this switching current operation, Sa1 and Sa2 can replace with the diode and Da1 is replaced by IGBT to form a unidirectional power flow. Hence, the unidirectional 5L-rectifier in Fig. 10.2 is named as multiple-pole multilevel switch-clamped rectifier (M^{2}SCR).

In short, each phase-leg of the proposed unidirectional 5L-M^{2}SCR consists of two cells with four IGBTs and eight diodes to achieve five-level input pole voltage. In Fig. 10.2, two switching devices (Sa3 and Sa4) of the inner cell are connected directly to the neutral-point-clamped of the four dc-link capacitors, while other two switching devices (Sa1 and Sa2) of the outer cell are clamped to the output terminal of the inner cell. With this unidirectional rectifier configuration, higher power density is achieved due to lower switching and conduction losses.

10.1.3 General Characteristic of Proposed 5L Rectifier Topologies for the AC/DC/AC Drive

The hardware implementation of the front-end rectifier and rear-end inverter of 5L AC/DC/AC drives are operated independently with the LS-PWM technique. The LS-PWM of the front-end rectifier and rear-end inverter are set at 1 kHz switching frequency operation.

The switching function of the LS-PWM technique for the 5L rectifier and inverter topologies as presented in the previous Chapter 8 is expressed as:

$$\begin{cases} S_{a1}(t) = T_{a1}(t) = 2m_a \sin \omega t - 1 \\ S_{a2}(t) = T_{a2}(t) = 2m_a \sin \omega t + 2 \\ S_{a5}(t) = T_{a5}(t) = 2m_a \sin \omega t \\ S_{a6}(t) = T_{a6}(t) = 2m_a \sin \omega t + 1 \end{cases} \tag{10.1}$$

where m_a is the ratio of two times the fundamental component of the pole voltage to the dc-link voltage.

Under the condition of steady-state and balanced capacitors voltage in the dc bus, the general expression of the incremental output pole voltage is written as:

$$V_{xm}(t) = \frac{V_{dc}(t)}{n-1}\left(\sum_{i=1}^{n-1} S_{xi} - \frac{n-1}{2}\right) \tag{10.2}$$

where x represents as phase ‘a’, ‘b’ and ‘c’ and n is the number of voltage level. S_{xi} is the switching states of each switching device depicted in the rectifier side.

The voltage transfer ratio of the both front-end and rear-end converters between the dc bus voltage to the input and output voltage are defined as:

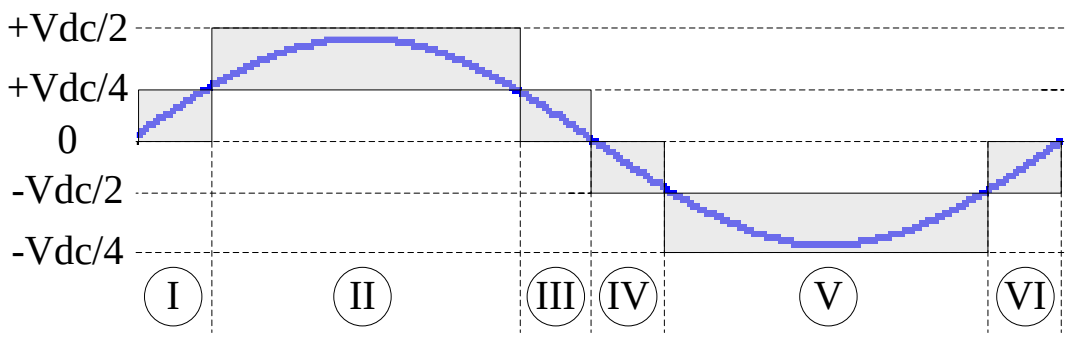


Fig. 10.3. Incremental input pole voltage stepped waveform with the appropriate sector occurring.

$$\begin{cases} M_{x,rectifier}(t) \approx \dfrac{V_{dc}(t)}{V_{x,L-L}(t)} \quad , \quad M_{x,rectifier}(t) > 1 \\ M_{x,inverter}(t) \approx \dfrac{2V_{xm}(t)}{V_{dc}(t)} \quad , \quad M_{x,rectifier}(t) \le 1 \end{cases} \tag{10.3}$$

$V_{x,L\text{-}L}(t)$ is the line-to-line voltage measured from the grid side and $V_{xm}(t)$ is the output pole voltage referred to the inverter side.

In general, high modulation index ($M_{x,rectifier}(t) > 1$) of the front-end rectifier is required to mitigate high input current distortion and achieve good dc-link voltage tracking due to its boosting effect in nature. Meanwhile the modulation index of the rear-end inverter is usually operate at the linear region ($M_{x,inverter}(t) < 1$) to prevent any higher order harmonic components incurred in the AC load. But high modulation index of the inverter side will occur when an AC machine is loaded and during startup condition.

Thus, a low switching frequency can be used for 5L rectifier to achieve low ripple current and better power conversion efficiency due to five-level voltage step. The ripple current is expressed in the following equation (10.4) and is based on the previous equations (10.2) and (10.3).

$$\Delta I_{Lx}(t) \approx \frac{k}{L_x F_s}\left\{\begin{array}{c} \dfrac{3V_{x,L-L}(t) - 3\sqrt{3}V_{mn}(t)}{3\sqrt{3}} \\ -\dfrac{M_{x,rectifier}(t)V_{x,L-L}(t)}{(n-1)\sqrt{3}}\left[\sum_{i=1}^{n-1} S_{xi,d} - \dfrac{n-1}{2}\right] \end{array}\right\} \tag{10.4}$$

F_s is the switching frequency of the rectifier and $V_{mn}(t)$ is the virtual ground voltage referred from node m to node n in Fig. 10.1. $S_{xi,d}$ is the switching state with the respective sectors shown in Fig. 10.3. k is the duty ratio of the switching state selection occur in the sector (Fig. 10.3) and this is expressed as:

$$\begin{cases} 0 \le \left[k = 2\sin\omega t\right] \le 1 & 0 \le \omega t \le \pi/6 \\ 0 \le \left[k = 2\left(\sin\omega t - 1/2\right)\right] \le 1 & \pi/6 \le \omega t \le \pi/2 \end{cases} \tag{10.5}$$

The reduction of input inductance value for the 5L rectifier topologies can be estimated with the duty cycle and the switching states with respect to the sectors shown in Fig. 10.3. According to equation (10.4), the maximum peak value of the input current ripple is determined using differential equation at $\omega t = 30°$ (assume $V_{mn} = V_{dc} = 1$p.u). Thus, the critical inductance value is estimated as follows:

$$L_{x,max} \approx \frac{4\left(V_{xn} - V_{mn}\right) - V_{dc}}{4\Delta I_{Lx} F_s} \tag{10.6}$$

V_{xn} is the peak value of the grid phase voltage.

10.2 Comparative Evaluation of Three-Phase 5L-M²DCR and 5L-M²SCR Topologies

Comparative evaluation of the design and implementation of the high power factor rectifiers with 5L incremental voltage stepped waveform is discussed. The comparative study of the proposed topologies will covers on the device rating, components count and control algorithm as given in the following subsection.

10.2.1 Semiconductors Voltage and Current Stresses

Voltage and current stresses are the dominant factors considered in the hardware development process, so that the converter can achieve optimum performance and higher reliability. Proper selection of the device rating for the proposed 5L rectifier topologies are determined based on the local and global stress analysis.

The voltage and current stress expressions for the respective front-end rectifiers are derived with the switching function in equation (10.1) and based on the following assumptions: (a) high power factor, (b) current and voltage ripple free, (c) constant switching frequency, (d) balanced electrolytic capacitors voltage in the dc-link, and € zero voltage dropped across boost inductor, L_x.

The maximum voltage stress across the power devices of the unidirectional 5L-M^2SCR and bidirectional 5L-M^2DCR topologies are expressed respectively in the following equations (10.7) and (10.8).

$$\begin{cases} V_{Da1} = \dfrac{3V_{dc}}{4} \\ V_{Da2} = V_{Sa1} = \dfrac{3V_{dc}}{8} \\ V_{Da5} = V_{Da6} = V_{Sa3} = \dfrac{V_{dc}}{4} \end{cases} \tag{10.7}$$

$$\begin{cases} V_{Sa1} = \dfrac{3V_{dc}}{4} \\ V_{Sa2} = \dfrac{V_{dc}}{2} \\ V_{Sa5} = V_{Sa6} = V_{Da1} = V_{Da3} = \dfrac{V_{dc}}{4} \end{cases} \tag{10.8}$$

Since the maximum voltage stress expressed in equations (10.7) and (10.8) are for the power devices in the upper phase-leg, hence the respective complimentary power devices in the lower phase-leg are also determined using the same expressions.

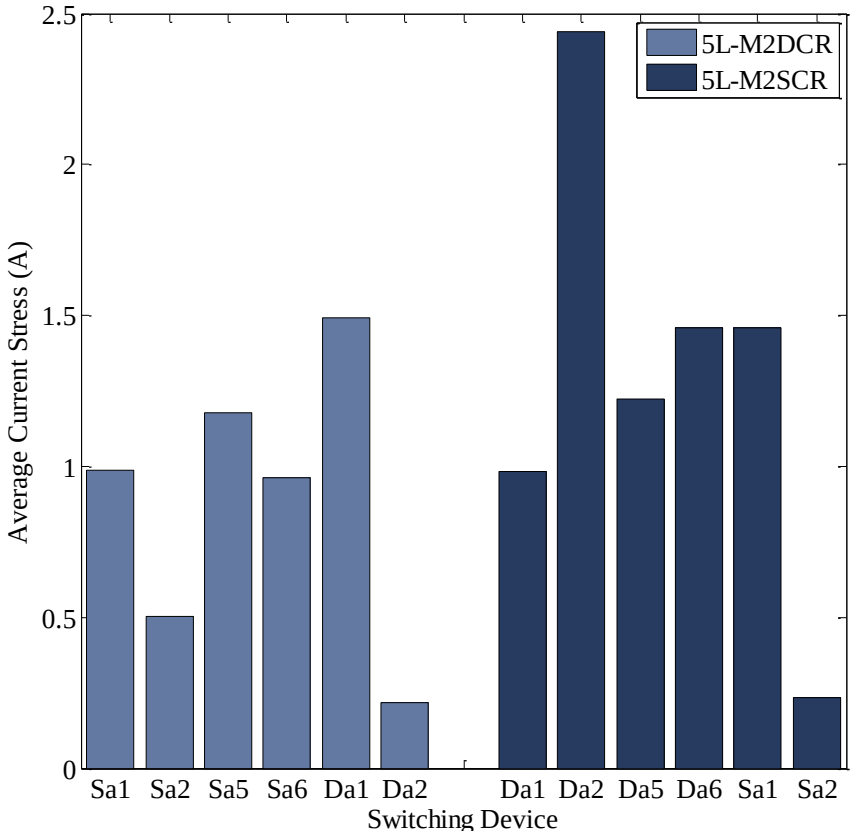


Fig. 10.4. Average current stress level for each device of the respective front-end rectifier topologies.

The average current stress is analyzed over one period of the fundamental frequency based on the assumed factors (a) to (e). For simplification, the average current stress is approximated as follows based on the respective switching function in (10.1).

$$\begin{cases} I_{Sa\langle Outer\ Cell\rangle}(t) = I_{Da\langle Outer\ Cell\rangle}(t) = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} I_a \sin(\omega t) S_{a\langle Outer\ Cell\rangle} d\omega t \\ I_{Sa\langle Inner\ Cell\rangle}(t) = I_{Da\langle Inner\ Cell\rangle}(t) = \dfrac{1}{2\pi}\displaystyle\int_0^{2\pi} I_a \sin(\omega t)\left[2 - \dfrac{4V_{am1}}{V_{dc}}\right] S_{a\langle Inner\ Cell\rangle} d\omega t \end{cases}$$

(10.9)

V_{am1} is the peak value of the fundamental component of the grid phase voltage. With the equation (10.9), the final expression of the average current and RMS current stresses flow through each power device in the upper phase-leg of the proposed rectifier topologies are shown in Fig. 10.4 according to the expression defined in Tables 10.2 and 10.3.

TABLE 10.2

EXPRESSION OF AVERAGE CURRENT AND RMS CURRENT STRESSES FOR 5L-M^{2}DCR UNDER UNITY POWER FACTOR OPERATION

	Average Current Stress	RMS Current Stress
Da1 Da2	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\begin{array}{c}\frac{V_{dc}}{V_{am1}}\left[1+\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\\ -2\left[\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)\right]\end{array}\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\frac{V_{dc}}{V_{am1}}\left[\begin{array}{c}\frac{1}{2}\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)-\frac{V_{dc}}{8V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ -2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)+\pi\end{array}\right]\\ +\frac{2}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-6\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right\}}$
Da3 Da4	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\frac{V_{dc}}{V_{am1}}\left[1-\frac{1}{2}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]-2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\frac{V_{dc}}{2V_{am1}}\left[\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)-\frac{V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\\ -\frac{16}{3}\sin^4\left(\frac{1}{2}\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\cdot\left[2+\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\end{array}\right\}}$
Sa1 Sa4	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\begin{array}{c}\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)\\ -\frac{V_{dc}}{V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\frac{V_{dc}}{2V_{am1}}\left[\begin{array}{c}\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)-\frac{\pi}{2}\\ -\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\cdot\left[\frac{V_{dc}}{4V_{am}}-\frac{6V_{am}}{V_{dc}}\right]\end{array}\right]\\ -\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right\}}$
Sa2 Sa3	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\begin{array}{c}2\pi+2\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-4\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)\\ -\frac{5V_{dc}}{V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\frac{V_{dc}}{V_{am1}}\end{array}\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\left[\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\left[1+\frac{V_{dc}}{2V_{am1}}\right]\\ -\left[2+\frac{V_{dc}}{2V_{am1}}\right]\sin^{-1}\frac{V_{dc}}{4V_{am1}}\\ -\left[3+\frac{2V_{dc}}{V_{am1}}+\frac{1}{8}\left(\frac{V_{dc}}{V_{am1}}\right)^2\right]\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ +\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right\}}$
Sa5 Sa8	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\begin{array}{c}4\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)+2\left[2-\frac{V_{dc}}{4V_{am1}}\right]\cdot\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ -\pi-\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\frac{16}{3}\sin^4\left(\frac{1}{2}\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\cdot\left[\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)+2\right]\\ +\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ +\frac{V_{dc}}{2V_{am1}}\left[\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right]\end{array}\right\}}$
Sa6 Sa7	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\begin{array}{c}6\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)+\frac{1}{2}\left[9-\frac{V_{dc}}{V_{am1}}\right]\cdot\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ -\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\pi-1\end{array}\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\begin{array}{c}\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\\ +\frac{V_{dc}}{2V_{am1}}\left[\begin{array}{c}\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\sin^{-1}\frac{V_{dc}}{4V_{am1}}\\ -\frac{V_{dc}}{2V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\end{array}\right]\end{array}\right\}}$

TABLE 10.3

EXPRESSION OF AVERAGE CURRENT AND RMS CURRENT STRESSES FOR 5L-M^{2}SCR UNDER UNITY POWER FACTOR OPERATION

	Average Current Stress	RMS Current Stress
Da1 Da4	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)-\frac{V_{dc}}{V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\frac{V_{dc}}{2V_{am1}}\left[\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\frac{\pi}{2}-\frac{V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]+3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right\}}$
Da2 Da3	$\frac{i_a}{\pi}$	$\frac{i_a}{2}$
Da5 Da8	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{4\sin^{-1}\frac{V_{dc}}{4V_{am1}}+\frac{7V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\pi\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\frac{V_{dc}}{2V_{am1}}\left[\pi+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right]+\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)+\frac{16}{3}\sin^4\left(\frac{1}{2}\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\cdot\left[2+\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\right\}}$
Da6 Da7	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{2\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\pi+\frac{V_{dc}}{V_{am1}}\left[1+\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\frac{V_{dc}}{2V_{am1}}\left[\pi+\sin^{-1}\frac{V_{dc}}{4V_{am1}}+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\frac{V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]+\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right\}}$
Sa1 Sa2	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{2\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-\pi+\frac{V_{dc}}{V_{am1}}\left[1+\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\frac{V_{dc}}{2V_{am1}}\left[\pi+\sin^{-1}\frac{V_{dc}}{4V_{am1}}+\sin\left(2\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-2\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\frac{V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]+\frac{1}{3}\cos\left(3\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)-3\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right\}}$
Sa3 Sa4	$\frac{V_{am1}i_a}{V_{dc}\pi}\left\{1-2\sin^{-1}\left(\frac{V_{dc}}{4V_{am1}}\right)-\frac{V_{dc}}{2V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right\}$	$i_a\sqrt{\frac{V_{am1}}{V_{dc}\pi}\left\{\frac{V_{dc}}{2V_{am1}}\left[\sin^{-1}\frac{V_{dc}}{4V_{am1}}-\frac{V_{dc}}{4V_{am1}}\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\right]-\frac{16}{3}\sin^4\left(\frac{1}{2}\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)\cdot\left[\cos\left(\sin^{-1}\frac{V_{dc}}{4V_{am1}}\right)+2\right]\right\}}$

Note: M_a is the phase a modulation index, which is expressed as $M_a = (2V_{am1}/V_{dc})\sin\omega t$.

The data obtained in Fig. 10.4 has verified the analytical expression (10.9). It is proven that during the negative cycle of the conduction period, the reverse current through the semiconductor switches in the bidirectional 5L-M^{2}DCR will be cancelled out from

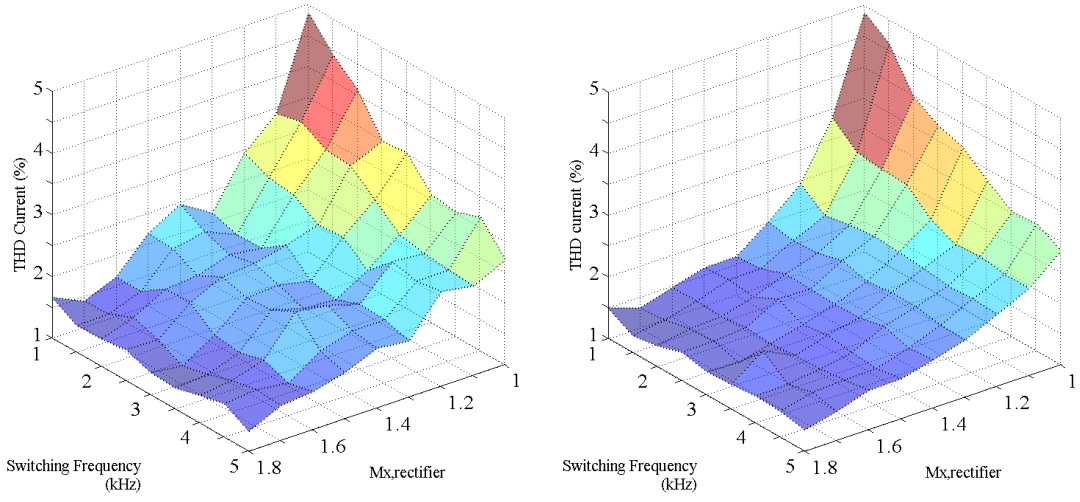
current stress during positive cycle period. Unlike the case for unidirectional 5L-M^{2}SCR, the current only flows through the diodes during positive cycle conduction period. Hence, the final net average current stress of 5L-M^{2}DCR in Fig. 7 is found to be lower compared to 5L-M^{2}SCR.

10.2.2 Input Current Shaping in 5L-M^{2}DCR and 5L-M^{2}SCR Topologies

The performances of the grid current response for the proposed front-end unidirectional and bidirectional rectifiers are carried out with the simulation as shown in Figs. 10.5(a) and 10.5(b) respectively. The harmonic current distortions are obtained based on the switching frequency (F_s) and the voltage transfer ratio ($M_{x,rectifier}$).

Fig. 10.5 shows that both the proposed front-end rectifiers have the highest current distortions when the $M_{x,rectifier}$ is as low as 1. The harmonic current distortion can be minimized in this case by increasing the F_s to 5 kHz and above.

However, the grid current distortion does not deviate much with any range of switching frequency utilized when the voltage transfer ratio $M_{x,rectifier}$ is more than 1.3. This can be proved by substituting equations (10.6) into (10.4), where the F_s is found to be cancelled away.



(a) (b)

Fig. 10.5. Harmonic current distortion characteristics of the respective front-end 5L-rectifier. (a) Unidirectional 5L-M^{2}SCR and (b) bidirectional 5L-M^{2}DCR.

The harmonic current distortion varies non-linearly for the unidirectional 5L-M^{2}SCR as shown in Fig. 10.5(a), while the results obtained for bidirectional 5L-M^{2}DCR in Fig. 10.5(b) has a smoother curve. This is caused by the forward blocking voltage where the current flows from the grid to the dc-link in one direction for the 5L-M^{2}SCR topology.

Even though there is slight difference in the performances, both proposed front-end rectifiers have met the adopted standard current THD requirements of 6% below even at a low switching frequency. Hence, the proposed low switching frequency rectifiers are also found attractive for relatively high power applications.

10.2.3 Components Count

The number of components count in the front-end rectifiers is shown in Table 10.4. One can observe that the number of the diodes used in the proposed bidirectional rectifier topology is reduced. This yields better efficiency because of low conduction loss. For unidirectional rectifier, the proposed topology reduces six MOSFET/IGBT devices. On top of that, the required six isolated gate driver is also eliminated.

TABLE 10.4

NUMBER OF COMPONENTS USED IN FRONT-END RECTIFIER TOPOLOGIES

Devices	Topologies				
	Unidirectional Rectifier			Bidirectional Rectifier	
	Classical 5L-MDCI (ref. to [20] of Fig. 6)	Classical 5L-MDCI (ref. to [20] of Fig. 7)	Proposed 5L-M^{2}SCR	Classical 5L-MDCI	Proposed 5L-M^{2}DCR
Diode	24	24	24	18	12
IGBT/MOSFET	18	18	12	24	24
Capacitors	4	4	4	4	4
Complementary Switch	0	9	0	12	12
Isolated Gate Driver	18	18	12	24	24
Cost (USD)	$7472.72	$8943.56	$5698.07	$6616.08	$7410.76
Efficiency (%)	77.37	80.44	85.42	80.99	82.30
Weight (kg)	8.01	9.63	6.17	7.14	7.91

Moreover, the proposed rectifier topology also reduces the cost of implementation, as well as the size of the converters. The overall components reduction not only consists of the active switches, but also the number of necessary control circuit, and the size of the heat sink. This can also improve the complexity of the control gating signals through less isolated power supply requirement.

10.2.4 Synchronous-Reference-Frame Current Control Scheme

The proposed control algorithm with power factor correction technique is shown in Fig. 10.6. Two control loops, i.e. Synchronous-Reference-Frame Current Control and Constant Switching Frequency Modulation are implemented to regulate the dc-link voltage and mitigate the current distortions. Due to the simplicity of the control strategy, low cost integrated control circuit can be designed. The balancing control for the dc-dc balancing circuit is presented in [90, 91].

The unity power factor (UPF) controller for the front-end five-level rectifiers (M^2DCR or M^2SCR) designed in Fig. 10.6 is based on the synchronous-reference-frame (SRF) current control with the LS-PWM technique. The detailed analysis of the outer-loop dc-link voltage control and inner-loop current control are both presented in [104].SRF controller provides a good dynamic response to achieve high quality input sinusoidal current with constant unity power factor performance.

The open-loop transfer function of the dc-link voltage control under steady-state condition is expressed as follows to achieve a stable control system:

$$L(s) = \frac{K_p s + K_I}{s} \cdot \frac{L_x I_d}{C_{eq} V_{dc}} \cdot \frac{\left(\sqrt{3} V_p / L_x I_d\right) - s}{s + \left(I_{dc} / C_{eq} V_{dc}\right)} \tag{10.10}$$

K_p and K_I are the PI parameters of the DC voltage control loop. C_{eq} and L_x are the equivalent capacitance value of the dc bus and the input (phase ‘a’, ‘b’ and ‘c’) filter inductance value respectively. V_p is the rms value of the grid phase voltage and V_{dc} is the mean value of the dc-link voltage.

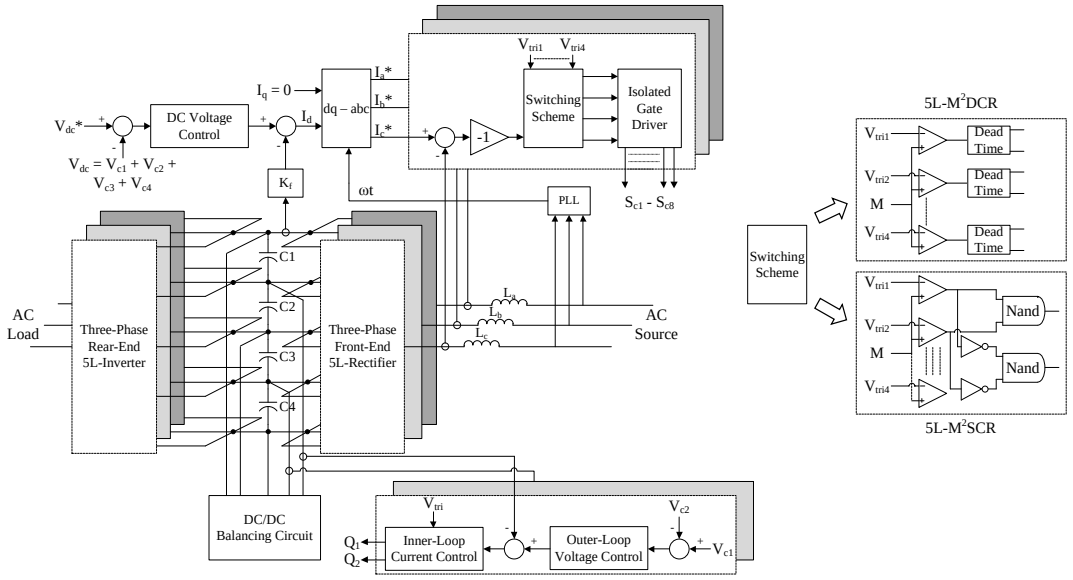


Fig. 10.6. Proposed front-end rectifier controller for 5L-AC/DC/AC drive based on Synchronous-Reference-Frame (SRF) Current Control.

As for I_d is the peak value of the reference current which is obtained from the summation of I_{dc} (output of dc voltage control) and feed-forward current (output of K_f). The feed-forward current control loop under steady-state condition is derived based on the power balanced principle, which is expressed as the following:

$$K_f = \frac{V_{dc}}{\sqrt{3}V_p} \tag{10.11}$$

10.3 Experimental Results

The AC/DC/AC hardware prototypes in Fig. 10.7 are constructed based on the proposed circuit diagrams of Figs. 10.1 and 10.2 with the controller loop as shown in Fig. 10.6. The controller is implemented utilizing the dSPACE RTI1103 controller board. The experimental results are obtained based on chosen system parameters values shown in Table 10.5.

The input current shaping of the two proposed front-end rectifiers is achieved through the application of proper gating signals based on the LS-PWM. Since the front-end bidirectional 5L-M^{2}DCR consists complementary switches, therefore additional dead

TABLE 10.5

PARAMETER SETTING FOR EXPERIMENTAL AC/DC/AC CONVERTERS

System Parameters	Values
Input Grid Voltage	60 Vrms (50 Hz)
DC-Link Voltage	200 Vdc
Input Inductors (Lx)	5 mH
Mx,inverter	0.8
Switching Frequency	1 kHz

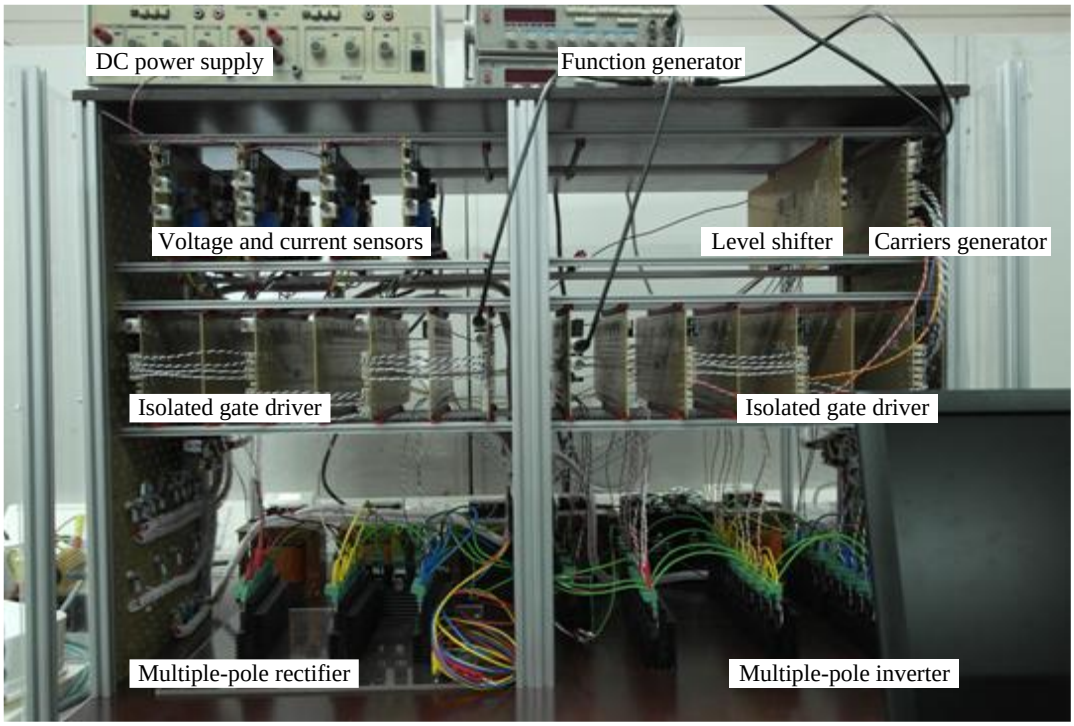


Fig. 10.7. Experimental setup on AC/DC/AC converter with different configuration based on bidirectional and unidirectional 5L unity power factor rectifiers.

time circuits are needed to prevent short circuit. Unlike the 5L-M^{2}DCR, the unidirectional 5L-M^{2}SCR does not have any complementary switches. Hence, the gating signals for 5L-M^{2}SCR are generated with the four logic NAND gates as shown in Fig. 10.6.

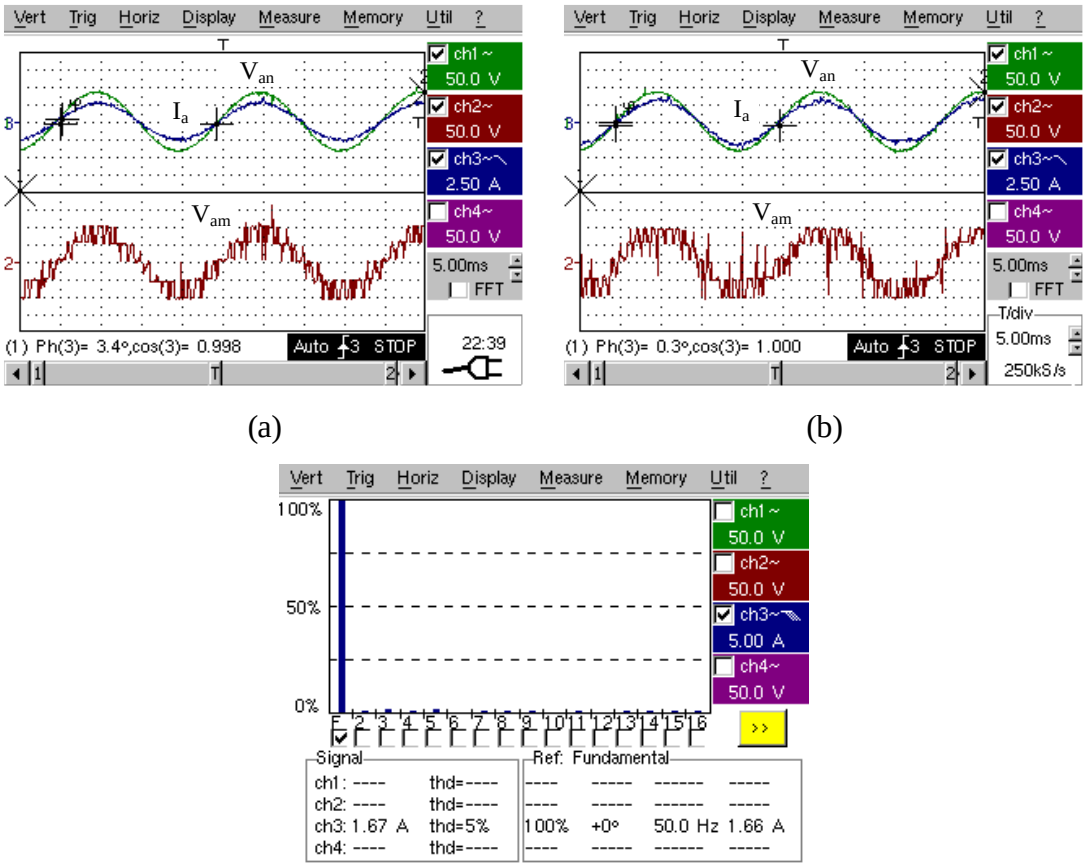


Fig. 10.8. Input voltage and current waveform (Upper trace: grid phase voltage, and current, lower trace: rectifier pole voltage) based on respective front-end multilevel rectifier topologies. (a) 5L-M^{2}SCR, (b) 5L-M^{2}DCR, and (c) THD of the grid current of Fig. 10.8 (a), the THD of the grid current is also similar result for 5L-M^{2}DCR.

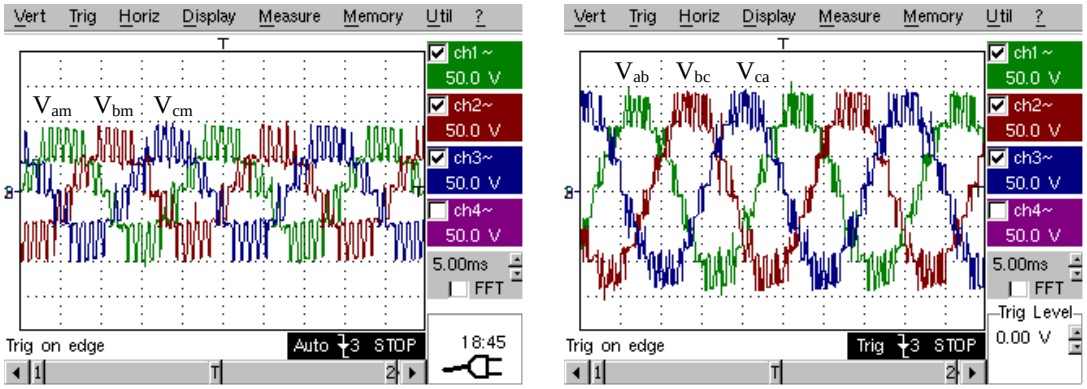


Fig. 10.9. Output voltage of rear-end 5L-M^{2}DCI topology in both AC/DC/AC configuration. (a) Output pole voltage, and (b) output line-to-line voltage.

The experimental results obtained in Figs. 10.8 (a) and (b) show the input voltage and current quality of front-end unidirectional 5L-M^{2}SCR and bidirectional 5L-M^{2}DCR respectively. Both proposed topologies achieve low input current distortions (as shown in Fig. 10.8(c)) yielding a 0.99 power factor. The input pole voltage in Fig. 10.8 (b) is slightly distorted as compared to the Fig. 10.8 (a). This is due to the instantaneous high reverse peak I_{dc} current fed into the close-loop controller. Thus the current error signal is affected and the input pole voltage is synthesized from positive voltage step to the negative voltage step or vice versa.

Same rear-end 5L-M^{2}DCI topology is implemented for both front-end uni and bidirectional topologies. The experimental results of the output pole voltages and output line-to-line voltages are obtained and shown in the Figs. 10.9 (a) and (b) respectively.

10.4 Discussion

A new generation of front-end unidirectional 5L-M^{2}SCR and bidirectional 5L-M^{2}DCR topologies are introduced to reduce the number of semiconductor devices usually required in conventional converters. The experimental results show have proven the theory, analysis and also verified the feasibility of the proposed AC/DC/AC topologies.

Excellent performance and low input current distortion with high power factor is achieved even while operating at low switching frequency of 1 kHz. This is without the use of any bulky LC passive filter. Low voltage/current stress and low switching losses due to reduce components count lead to better converter efficiency. The size of input reactors requirement is also reduced thanks to the number of voltage level increased while operating at low switching frequency. This is at the small cost of an additional balancing capacitor voltage circuitry to balance the capacitors voltages in the dc-link.

Alternatively dc-link balancing strategies such as modulation schemes or control algorithms can be implemented to replace the additional balancing circuit. These will provide a more cost effective and energy efficient solution for a higher-level AC/DC/AC drive and can especially be suitable for renewable energy conversion where high efficiency is paramount.

Chapter 11 – New PWM Switching Technique with Low Conduction Period Control on Five-Level/Multiple-Pole Multilevel VIENNA Rectifier Topologies for Energy Efficiency

This chapter introduces a new unidirectional three-phase five-level rectifier topology that requires only a minimum of six IGBT devices as shown in Fig. 11.1. The concept of this rectifier topology with reduced number of operating device is derived and modified from the unidirectional multiple-pole multilevel switch-clamped rectifier topology presented in Chapter 10. Hence, this rectifier is named as Multiple-pole multilevel VIENNA rectifier (M^2VR) topology. The M^2VR topology achieves high power factor in the main line requiring only a small inductor with the five-level input voltage stepped waveform. The reliability of this converter is improved by employing lesser number of components as compared to the unidirectional 5L rectifier topology in Chapter 10, which does not require any dead time circuitries and additional isolated gate drivers. However, alternative method for reducing the losses in unidirectional 5L rectifier is required to investigate not only reducing the number of components count.

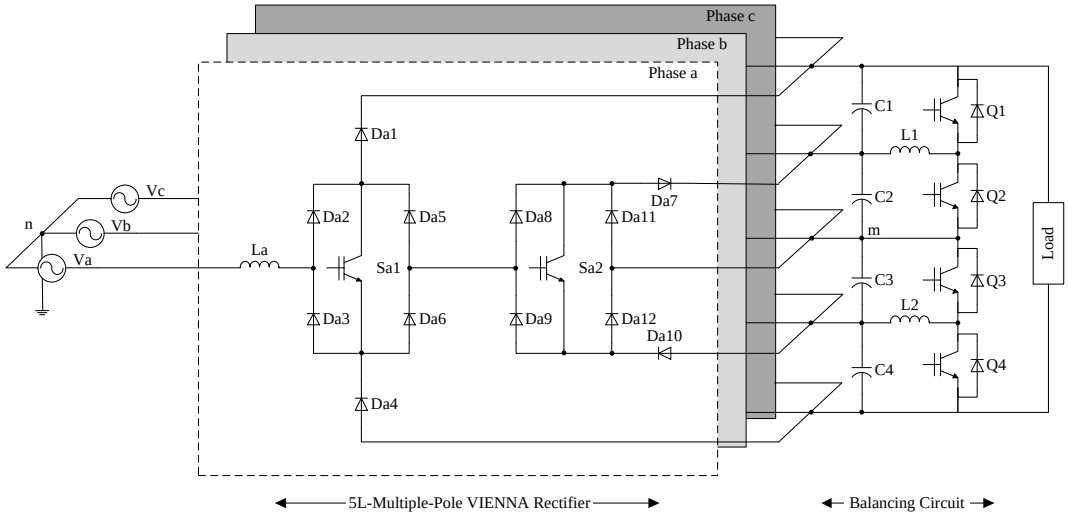


Fig. 11.1. Proposed unidirectional five-level/multiple-pole multilevel VIENNA rectifier (5L-M^2VR) with balancing circuit.

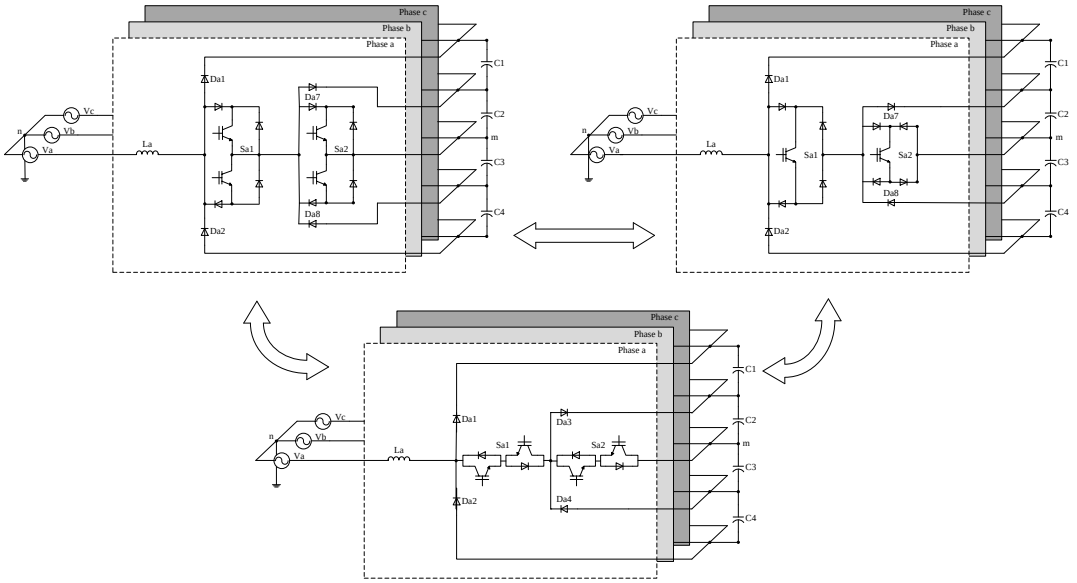


Fig. 11.2. Alternative configuration of proposed unidirectional 5L Multiple-Pole Multilevel Rectifier Topologies based on various types of four quadrant switches.

Several methods for reducing the stress and switching loss across the semiconductor devices have been proposed based on: (1) low conduction period control [105, 106], (2) resonant DC-link circuit [107], and (3) transformer-assisted PWM zero voltage switching technique [108].

The proposed method (1) has the advantage of reducing the losses and stresses on the semiconductor devices, but the converter would still need a large input reactor for lower conduction angles [69]. The proposed methods (2) and (3) achieve lower switching losses due to zero voltage and zero current switching. However, the disadvantage of both methods will increase the complexity of the control scheme and the overall weight of the converters.

A new switching scheme in this Chapter is proposed to achieve lower losses by remaining the minimum number of switches in unidirectional 5L rectifier topologies in Fig. 11.1. Two types of switching schemes – PWM techniques and low conduction period control [105, 106] are applied to the outer cell and inner cell switches respectively to achieve low switching and conduction losses as compared to the classical switching method. PWM techniques such as Level-Shifted PWM (LS-PWM) or Phase-Shifted

PWM (PS-PWM) can be applied to this topology. The performances of both the PWM techniques are evaluated in the following section.

11.1 Operating Principle and Device Rating

A conventional three-phase VIENNA rectifier topology consists of three switches. Each of the switches is connected across the four adjacent diodes to enable a bidirectional current flow between the grid and the neutral-point-clamped of the two dc-link capacitors. Zero voltage conduction across the switching device is achieved due to the configuration of VIENNA topology. Thus, three voltage levels (+Vdc/2, 0 and –Vdc/2) are synthesized.

The proposed five-level rectifier topology (5L-M^{2}VR) in Fig. 11.1 is configured with two VIENNA rectifier cells in each phase, which are constructed based on the multiple-pole hierarchy. According to the pole diagram concept (Fig. 8.2), alternative structures of the bidirectional switches are configured as shown in Fig. 11.2. Therefore, the five-level stepped input voltage waveform is obtained with the proposed M^{2}VR configuration.

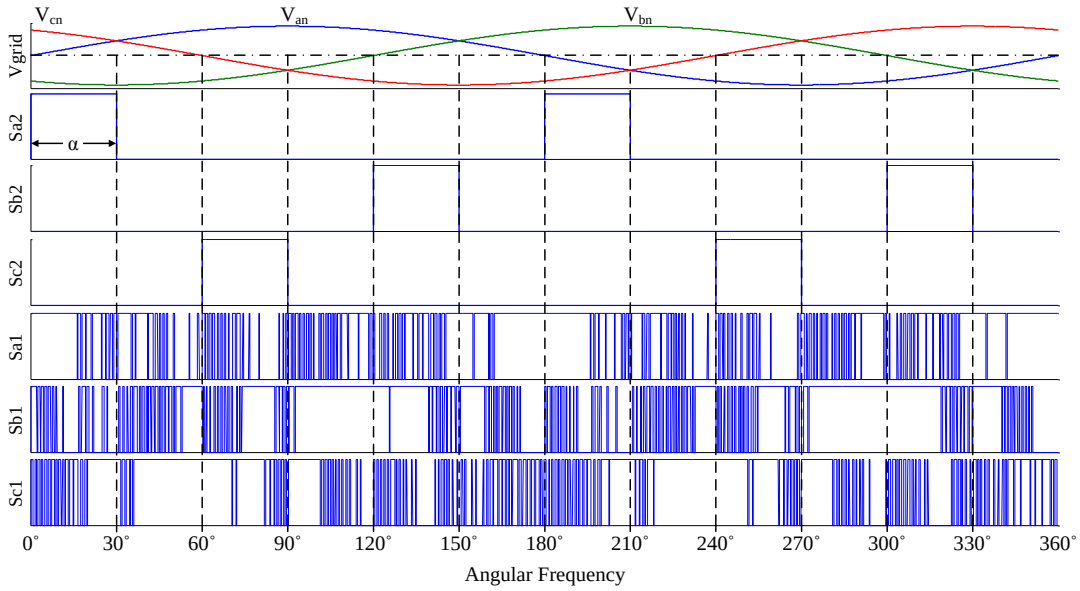


Fig. 11.3. Two proposed switching scheme: switching angle firing method for Sx1 and LS-PWM techniques through the logic gate for Sx2.

Two types of switching schemes are utilized to modulate the gate signals for both outer and inner cells, in order to achieve low current distortion. The switches (S_{a2}, S_{b2} and S_{c2}) in the outer cell of rectifier are operated with the PWM techniques as shown in Fig. 11.4. While the switches (S_{a1}, S_{b1} and S_{c1}) in the inner cell of rectifier start conducting at each zero crossing point of the grid voltage with a switching angle (α) of 30° as shown in Fig. 11.3.

The approximated maximum current (peak value of the current) flow through the power device can be estimated using differential equation together with the summation of an initial value. This initial value is determined by the maximum input current obtained from previous group of 30° switching angle, which is explained in [109].

11.1.1. Current Stresses on Power Device

The average current and RMS current stresses are estimated using the local and global stress analysis as presented in Chapter 8. Theoretical analysis of the switching function of the local current stress of all the power devices mainly depends on the switching states selection of the outer cell switch. While the average value of the global current stress estimation on particular devices like Sa2, Da11 and Da12 in the inner cell are form by the integration limit within the switching angle period, α over one main period ($\omega t = 2\pi$) of the grid.

The expression of the average and RMS current stress on each power device based on the integral limit with the switching function analysis is expressed in Tables 11.1 and 11.2. The final expression of the current stress is extended in term of modulation amplitude and with or without the switching angle depending on the conduction period of the power device. Derivation of the switching function for the switching device is detailed in Chapter 5. The amplitude of the carrier waveform in LS-PWM technique is normalized at 1 p.u, which is set at 0 to 1 p.u for the upper triangle wave and 0 to -1 p.u for the lower triangle wave. Similarly for the PS-PWM, both carrier waves are normalized at -1 to 1 p.u. With the LS-PWM through the logic gate, the final switching function expression can be written in equation (11.1). Similarly for a PS-PWM can expressed with the same derivation concept as presented in Chapter 5 and remaining

TABLE 11.1

AVERAGE CURRENT STRESS BASED ON INTEGRAL LIMIT WITH THE SWITCHING FUNCTION EXPRESSION

Power Device	Average Current Stress Expression	Final Expression of the Average Current Stress
Da1	$\frac{1}{2\pi}\int_0^{\pi} i_a \sin\omega t\left[1-S_{a1}(\omega t)\right]d\omega t$	$\frac{m_a i_a}{4}$
Da2	$\frac{1}{2\pi}\int_0^{\pi} i_a \sin\omega t d\omega t$	$\frac{i_a}{\pi}$
Da5	$\frac{1}{2\pi}\int_0^{\pi} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{2\pi}\left\{2-\frac{\pi m_a}{2}\right\}$
Da7	$\frac{1}{2\pi}\int_{\alpha}^{\pi} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{2\pi}\left\{1+\cos\alpha-\frac{1}{2}m_a\left[\begin{matrix}\pi-\alpha\\+\sin\alpha\cos\alpha\end{matrix}\right]\right\}$
Da8	$\frac{1}{2\pi}\int_0^{\pi} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{2\pi}\left\{2-\frac{\pi m_a}{2}\right\}$
Da11	$\frac{1}{2\pi}\int_0^{\alpha} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{2\pi}\left\{1-\cos\alpha+\frac{1}{4}m_a\left[\sin 2\alpha-2\alpha\right]\right\}$
Sa1	$\frac{1}{\pi}\int_0^{\pi} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{\pi}\left\{2-\frac{\pi m_a}{2}\right\}$
Sa2	$\frac{1}{\pi}\int_0^{\alpha} i_a \sin\omega t\cdot S_{a1}(\omega t)d\omega t$	$\frac{i_a}{\pi}\left\{1-\cos\alpha+\frac{1}{4}m_a\left[\sin 2\alpha-2\alpha\right]\right\}$

current stress analysis for PS-PWM technique will not be further discussed in this Thesis.

$$S_{a1}(\omega t)=1-m_a\sin\omega t \tag{11.1}$$

TABLE 11.2

RMS CURRENT STRESS BASED ON INTEGRAL LIMIT WITH THE SWITCHING FUNCTION EXPRESSION

Power Device	Average Current Stress Expression	Final Expression of the Average Current Stress
Da1	$i_a\sqrt{\frac{1}{2\pi}\int_0^{\pi}\sin^2\omega t\left[1-S_{a1}(\omega t)\right]d\omega t}$	$i_a\sqrt{\frac{2m_a}{3\pi}}$
Da2	$i_a\sqrt{\frac{1}{2\pi}\int_0^{\pi}\sin^2\omega t d\omega t}$	$\frac{i_a}{2}$
Da5	$i_a\sqrt{\frac{1}{2\pi}\int_0^{\pi}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{4}-\frac{2m_a}{3\pi}}$
Da7	$i_a\sqrt{\frac{1}{2\pi}\int_{\alpha}^{\pi}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{2\pi}\left\{\begin{array}{l}\frac{4}{3}m_a(\cos\alpha-2)\cos^4\left(\frac{\alpha}{2}\right)\\ +\frac{1}{2}[\pi+\sin\alpha\cos\alpha-\alpha]\end{array}\right\}}$
Da8	$i_a\sqrt{\frac{1}{2\pi}\int_0^{\pi}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{4}-\frac{2m_a}{3\pi}}$
Da11	$i_a\sqrt{\frac{1}{2\pi}\int_0^{\alpha}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{2\pi}\left\{\begin{array}{l}\frac{1}{2}[\alpha-\sin\alpha\cos\alpha]\\ -\frac{4}{3}m_a\sin^4\left(\frac{\alpha}{2}\right)[\cos\alpha+2]\end{array}\right\}}$
Sa1	$i_a\sqrt{\frac{1}{\pi}\int_0^{\pi}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{2}-\frac{4m_a}{3\pi}}$
Sa2	$i_a\sqrt{\frac{1}{\pi}\int_0^{\alpha}\sin^2\omega t\cdot S_{a1}(\omega t)d\omega t}$	$i_a\sqrt{\frac{1}{\pi}\left\{\begin{array}{l}\frac{1}{2}[\alpha-\sin\alpha\cos\alpha]\\ -\frac{4}{3}m_a\sin^4\left(\frac{\alpha}{2}\right)[\cos\alpha+2]\end{array}\right\}}$

11.1.2. Voltage Stresses on Power Device

The maximum voltage across the switches can be determined based on the switching conditions. Thus, the maximum voltage stress for Sx2 is obtained when Sx1 is switched off and vice versa. Therefore, the maximum voltage across the inner cell switches (Sx2) and outer cell switches (Sx1) will be $V_{dc}/4$ and $V_{dc}/2$ respectively.

11.2 Controller Design

The proposed power balance control technique outlined in Chapter 3 is applied for this 5L-M^2VR topology. Two control loops (DC-Link Voltage Control and Carrier-Based Current Control) in Fig. 11.4 are derived according to the power balance principle, which are briefly explained in the following subsections:

11.2.1. Power Balance Principle

High input power factor can be achieved for both balanced and unbalanced grid conditions with the simplest power balance control technique based on the dynamic current control. According to the power balance principle, the reference current is equivalent to the summation of load current estimator (first current component) and the equivalent capacitor current (second current component) is as given below:

$$I_a^*(t)=\begin{bmatrix} i_{load}(t) \\ +i_{Ceq}(t) \end{bmatrix}\sin\omega t=\left[\begin{array}{c} \underbrace{\dfrac{\sum\left(V_{xn}(t)-L_x\dfrac{dI_x(t)}{dt}-R_xI_x(t)\right)I_x(t)}{V_{dc}(t)}}_{\text{First current component}} \\ +\underbrace{C_{eq}\dfrac{dV_{dc}(t)}{dt}}_{\text{Second current component}} \end{array}\right]\sin\omega t \tag{11.2}$$

'x' is denoted as the phase 'a', 'b' and 'c' for the grid phase voltage $V_{xn}(t)$ and input current $i_x(t)$. C_{eq} is the equivalent capacitance value of the dc-link capacitors.

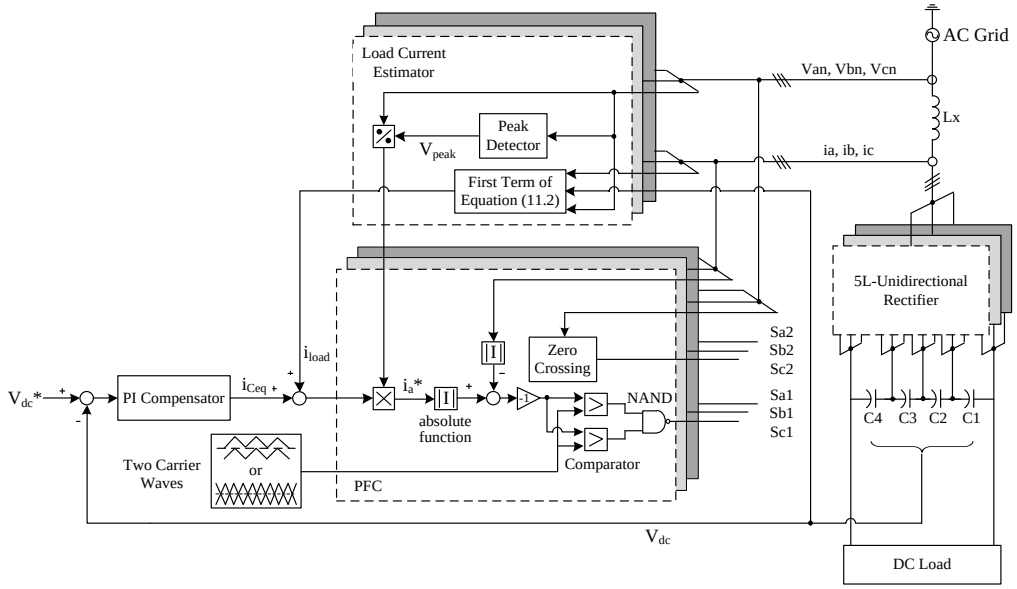


Fig. 11.4. Proposed power balanced control technique for 5L-M^{2}VR topology.

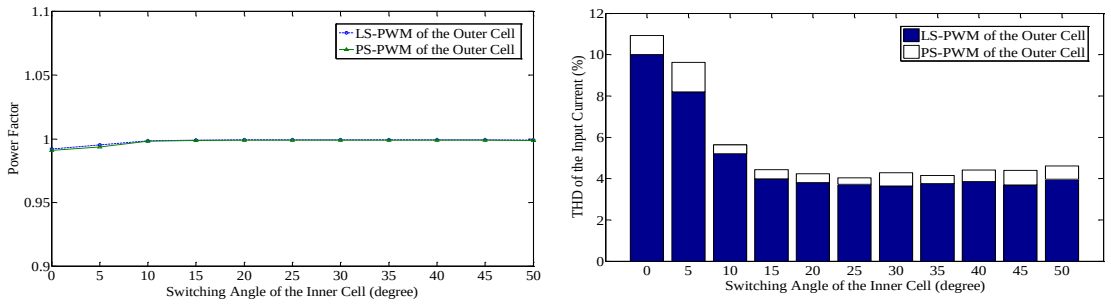
The equivalent capacitor current (i_{Ceq}) in (11.2) is obtained from the dc-link voltage control. The unit template of the supply voltage, sin(ωt), in (11.2) for the reference current phase 'a' is formulated as follows:

$$V_{peak} = \left[\left(\frac{2}{3} V_{an}(t) - \frac{1}{3} V_{bn}(t) - \frac{1}{3} V_{cn}(t) \right)^2 + \left(\frac{1}{\sqrt{3}} V_{bn}(t) - \frac{1}{\sqrt{3}} V_{cn}(t) \right)^2 \right]^{1/2} \tag{11.3}$$

$$\sin \omega t = \frac{V_{an}(t)}{V_{peak}} \tag{11.4}$$

11.2.2. DC-Link Voltage Control

The second current component depends on the variation of the dc-link voltage. Therefore, the energy storage model can also be derived based on the power balance principle. With this model, a simple PI control is implemented to regulate the dc-link voltage in the outer control loop. Thus, the open-loop transfer function of the energy storage model is written as:



(a) (b)

Fig. 11.5. Input characteristic performance of the novel rectifier with the proposed switching technique based on 1 kHz PWM with the respective switching angle range between 0° to 50°. (a) Input power factor and (b) THD of the input grid current.

$$L(s) = K_p\left(1+\frac{1}{T_i s}\right)\times\frac{3V_m}{V_{dc}C_{eq}}\times\frac{1}{s+6V_m/V_{dc}C_{eq}R_{load}} \tag{11.5}$$

Based on equation (11.5), the proportional gain K_p is selected accordingly to the pole cancellation in order to achieve a stable output dc voltage.

11.2.3. Carrier-Based Current Control

Two types of low switching modulation schemes are applied to the switches (Sx1 and Sx2) in the 5L-M^{2}VR topology. For the outer cell switches (Sx1), the PWM techniques are implemented by comparing the two triangular carrier waves of 1 kHz frequency with the current error. Thus, two modulated signals are generated. However, only single gate signal drives the switch (Sx1), therefore the two modulated signals are fed into logic NAND gate.

As mentioned, the inner cell switches (Sx2) are controlled by the switching angle during zero crossing point of the grid voltage. In order to achieve optimal performances for the 5L-M^{2}VR, it is very important to define the range of the switching angle for Sx2 due to the combination with the PWM techniques applied for Sx1.

An input power factor of 0.99 is achieved with switching angle more than 10° as shown in Fig. 11.5 (a). Besides that, the range of switching angle to achieve low current distortion is defined between 20° to 30°, which can be observed from Fig. 11.5 (b). The comparison results of two PWM techniques (LS-PWM and PS-PWM) are presented in Figs. 11.5 (a) and (b) are obtained based on the same constant modulation index. These results have clearly shown that the optimum performances can be achieved by the combination of LS-PWM with the switching angle of 30° or PS-PWM with 25°.

In the closed-loop control strategy (Fig. 11.4), the inner cell switches driven by the fixed switching angle are unable to control the dc-link voltage. Due to 5L-M^{2}VR configuration, only the outer cells are directly connected between the input grid and the output dc-bus terminal. Hence, the dc-link voltage is regulated with the outer loop voltage control involving only outer cell switches.

Such power balance control technique does not include any balancing control for the dc-link capacitors voltage. Thus, additional DC/DC balancing circuit is required to balance the capacitor voltage in the dc-link. The voltage balancing DC/DC converter is not discussed in this chapter. The voltage balancing control strategy and analysis are detailed in [90, 91].

11.3 Simulation Results

The results for the proposed 5L-M^{2}VR topology with the proposed controller scheme are obtained with the aid of MATLAB simulator. The results are shown in Figs. 11.6 to 11.8 with the implementation of LS-PWM technique for Sx1 and a fixed switching angle of 30° for Sx2.

In Fig. 11.6, the input characteristic of 5L-M^{2}VR (Fig. 11.1) results in a good approximation of current ripple reduction with the time varying DT_s, which is expressed in following equation (11.6):

$$\Delta I_a(t) = \int_0^{DT_s} \frac{V_{an}(t) - V_{am}(t) - V_{mn}(t)}{L_a} dt \qquad (11.6)$$

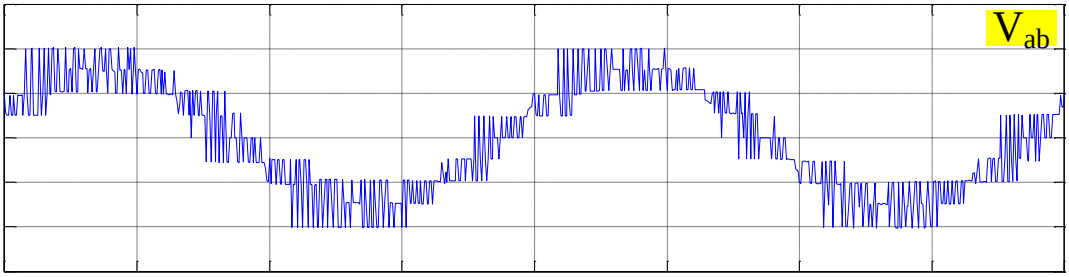


Fig. 11.6. Input rectifier line-to-line voltage (voltage referred from node 'a' to node 'b') refers to Fig. 11.1.

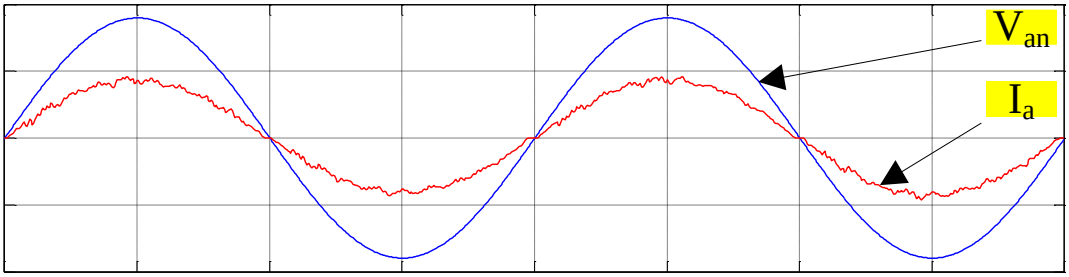


Fig. 11.7. Grid phase voltage (voltage referred from node 'a' to node 'n') and line current of phase 'a' with power factor of 0.99.

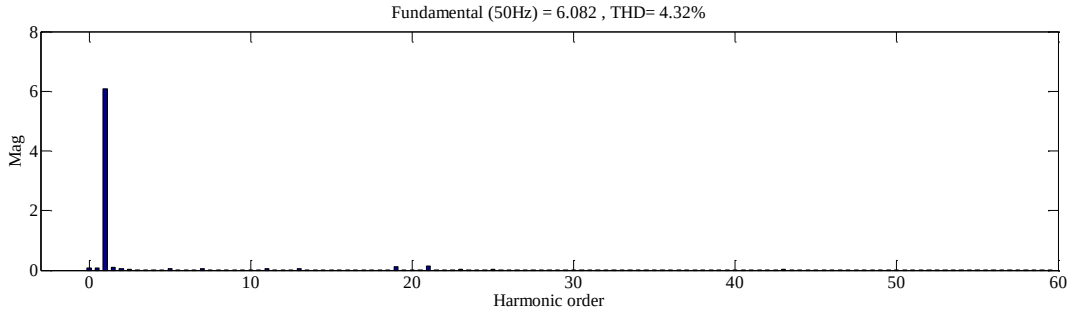


Fig. 11.8. Input line current THD of phase 'a'.

With this approximation, the rate of change of the current depends on the variable duty cycle ($0 \leq D \leq 1$) of PWM signals. Due to the advantage of having higher-level stepped voltage waveform, low switching frequency of PWM signals for Sx1 are sufficient to improve the quality of the line current, together with a fixed switching angle of 30° conducted by Sx2. As the number of synthesized voltage steps increase, the shape of the input voltage is more sinusoidal in nature. This results in a drastic reduction in the size of the input line inductance with lower switching and conduction losses.

The input line current THD obtained from the FFT analysis tool is below 6% as shown in Fig. 11.8. Having such low THD current results high power factor (cos φ) near to unity (Fig. 11.7), THD and power factor are related as shown in the equation (11.7):

$$PF = \frac{\cos \varphi_1}{\sqrt{1-(THD_i)^2}} \tag{11.7}$$

As a result, the displacement factor (cos φ_1) in (11.7) is approximately equal to 1 due significantly low distortion in the input current and voltage waveform.

11.4 Discussion

In this Chapter, a high power factor five-level rectifier topology (5L-M^2VR) based on the concepts of three-phase three-switch three-level rectifier (VIENNA rectifier) is discussed. The proposed 5L-M^2VR utilizes lesser number of components as compared to the conventional unidirectional diode-clamped rectifier.

The advantages of this topology over conventional topologies are discussed in the followings:

(a) Good performance is achieved even while operating at lower switching frequency requiring no complicated EMI filter.
(b) Low cost integrated control unit for two semi-conductor switches in each phase.
(c) Wide bandwidth control for achieving low THD current and high power factor as compared to [105].
(d) Elimination of short circuit fault due to the failure of switching devices results in high reliability of the converter.

Chapter 12 – Five-Level/Multiple-Pole Multilevel Rectifier Topology Based on Observer Control Technique with Reduce Components Count

Most of the commercially available multilevel inverters require a bulky phase-shifted transformer with multiple bridge rectifiers (Fig. 2.2 in Chapter 2) connected at the front-end side [89]. However, the volume and the weight of such configuration are large and heavy. In addition, more losses are experienced in the transformer during low utilization due to its core resistance. Several new transformerless multilevel rectifier topologies with low switching frequency operation have been reported in the literature. Recent developments on high incremental voltage level rectifier topologies with reduced number of components are found namely: (i) packed U cells multilevel converter (PUC) [110], (ii) reduced-part-count diode-clamped rectifier (RPC-DCR) [20], and (iii) hybrid diode-clamped and flying capacitor rectifier (DCLP-FC) [111].The mentioned low-cost topologies have achieved good efficiency and also proven that the filter size can be drastically reduced even with the low switching frequency operation as discussed in Chapter 10.

However, each of these topologies has its limitations and disadvantages. For instance, a complex control algorithm is required to balance the flying capacitors of the three-phase star-configured PUC topology. While in the case of RPC-DCR topology, only two switches are reduced in each phase-leg but the total component counts are not significantly optimized. Hence, huge number of gate drivers and isolated gate supplies are still required. As for the DCLP-FC topology, a good arrangement of hybrid approach is introduced to reduce 50% of the switching devices as compared to both conventional diode-clamped and flying capacitor rectifiers. Nevertheless, a total of thirteen dc capacitors are still needed for this three-phase topology to synthesize a five-level phase voltage stepped waveform. Due to the involvement of dc electrolytic capacitors, the lifetime of the power converter will eventually be affected by the thermal aging.

TABLE 12.1

SWITCHING STATES FOR CORRESPONDING PHASE 'A' VOLTAGE LEVEL

States	Switching		sign(Ia)	Input Pole Voltage Level, Vam
	Sa1	Sa2		
1	0	0	+	Vdc/2
2	1	0	+	Vdc/4
3	1	1	+ or -	0
4	1	0	-	-Vdc/4
5	0	0	-	-Vdc/2

sign(Ia) is the phase 'a' current direction flow from the grid through the switching devices.

This Chapter presents a components count optimization for the proposed five-level/multiple-pole multilevel unity power factor rectifier (5L-M^{2}UPF) topology in Fig 12.1 with a simple design and cost effective control algorithm based on the proposed observer control technique. This observer control technique is implemented with the in-phase quantity current control, which can eliminate some of the physical measurement sensors in the feedback control loop and provide excellent dynamic response for two-phase operation in the grid. As a result, more compact size and high reliability of three-phase five-level/multiple-pole multilevel unity power factor rectifier is achieved.

12.1 Basic Operating Principle

A proposed five-level (5L) M^{2}UPFR topology shown in Fig. 12.1 is constructed using two three-level (3L) VIENNA rectifier cells in each phase-leg. The multiple-pole structure is similar to Fig. 11.1 and the multiple-pole concept is presented in Chapters 10. The output terminals of both VIENNA rectifier cells are connected to the respective dc capacitors with the aid of balancing circuit.

Since each cell is characterized with a three-level input voltage stepped waveform, the overall performance for a five-level incremental voltage stepped is synthesized based on the switching state selection and the direction of the corresponding grid phase current stated in Table 12.1. Therefore, the expression for the input pole voltages of the proposed 5L-M^{2}UPFR is written as follows:

$$\begin{cases} V_{am}(t) = \dfrac{V_{dc}(t)}{4}\left[2 - S_{a1}(t) - S_{a2}(t)\right] \cdot \text{sign}\left(I_a(t)\right) \\ V_{bm}(t) = \dfrac{V_{dc}(t)}{4}\left[2 - S_{b1}(t) - S_{b2}(t)\right] \cdot \text{sign}\left(I_b(t)\right) \\ V_{cm}(t) = \dfrac{V_{dc}(t)}{4}\left[2 - S_{c1}(t) - S_{c2}(t)\right] \cdot \text{sign}\left(I_c(t)\right) \end{cases} \tag{12.1}$$

where $V_{dc}(t)$ is the dc-link voltage and sign(.) indicates the directional flow of the respective phase current according to the condition given in (12.2). For simplicity, the equations in this paper expressed with phase ‘a’ term are applied for the other phases ‘b’ and ‘c’ as well.

$$\text{sign}\left(I_a(t)\right) = \begin{cases} 1 & \text{for } I_a(t) \geq 0 \\ -1 & \text{for } I_a(t) < 0 \end{cases} \tag{12.2}$$

The current through the four quadrant switch of the outer VIENNA rectifier cell is expressed in following equation (12.3) based on the respective switching states in Table 12.1.

$$\begin{cases} I_{a1}(t) = I_a(t) S_{a1}(t) \\ I_{b1}(t) = I_b(t) S_{b1}(t) \\ I_{c1}(t) = I_c(t) S_{c1}(t) \end{cases} \tag{12.3}$$

The output bidirectional current ($I_{a2}(t)$, $I_{b2}(t)$ and $I_{c2}(t)$) of the inner cell is depending on the current expression in (12.3) and the corresponding switching states of the inner cell switch. Hence, the neutral-point-clamped current $I_m(t)$ through node ‘m’ written in (12.4) is the summation of these three-phase output bidirectional current.

$$\begin{aligned} I_m(t) &= I_{a1}(t)S_{a2}(t) + I_{b1}(t)S_{b2}(t) + I_{c1}(t)S_{c2}(t) \\ &= I_a(t)S_{a1}(t)S_{a2}(t) + I_b(t)S_{b1}(t)S_{b2}(t) + I_c(t)S_{c1}(t)S_{c2}(t) \end{aligned} \tag{12.4}$$

The bidirectional current through outer and inner switches (Sa1 and Sa2) of the 5L-M^{2}UPFR expressed in (12.5) is always positive over the fundamental period due to the floating diodes ($D_{a3} – D_{a6}$ and $D_{a9} – D_{a12}$).

$$\begin{cases} I_{Sa1}(t) = \left| I_a(t)S_{a1}(t) \right| \\ I_{Sa2}(t) = \left| I_a(t)S_{a1}(t)S_{a2}(t) \right| \end{cases} \tag{12.5}$$

The instantaneous current through the respective diode elements of both outer and inner cell are determined by the current flow over the fundamental period and expressed as follows:

Outer Cell 5L-M^{2}UPFR:

During positive half cycle

$$\begin{cases} I_{Da1}(t) = I_a(t)\left[1 - S_{a1}(t)\right] \\ I_{Da2}(t) = 0 \\ I_{Da3}(t) = I_{Da6}(t) = I_a(t)S_{a1}(t) \\ I_{Da4}(t) = I_{Da5}(t) = 0 \end{cases} \tag{12.6}$$

During negative half cycle

$$\begin{cases} I_{Da1}(t) = 0 \\ I_{Da2}(t) = I_a(t)\left[1 - S_{a1}(t)\right] \\ I_{Da3}(t) = I_{Da6}(t) = 0 \\ I_{Da4}(t) = I_{Da5}(t) = I_a(t)S_{a1}(t) \end{cases} \tag{12.7}$$

Inner Cell 5L-M^{2}UPFR:

During positive half cycle

$$\begin{cases} I_{Da7}(t) = I_a(t)S_{a1}(t)\left[1-S_{a2}(t)\right] \\ I_{Da8}(t) = 0 \\ I_{Da9}(t) = I_{Da12}(t) = I_a(t)S_{a1}(t)S_{a1}(t) \\ I_{Da10}(t) = I_{Da11}(t) = 0 \end{cases} \tag{12.8}$$

During negative half cycle

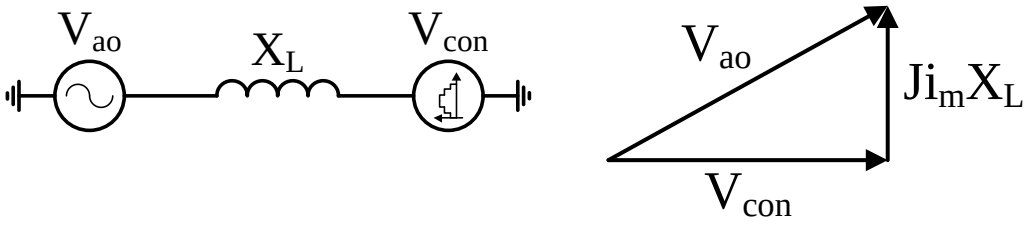
$$\begin{cases} I_{Da1}(t) = 0 \\ I_{Da2}(t) = I_a(t)S_{a1}(t)\left[1-S_{a2}(t)\right] \\ I_{Da3}(t) = I_{Da6}(t) = 0 \\ I_{Da4}(t) = I_{Da5}(t) = I_a(t)S_{a1}(t)S_{a1}(t) \end{cases} \tag{12.9}$$

12.2 Switching Function

The gating signals for the switches Sa1 and Sa2 based on the switching states given in Table 12.1 are obtained by comparing the absolute function of the modulation signal with the triangular carriers as shown in Fig. 12.2. The switching states are achieved according to the condition given in (12.10).

$$\begin{aligned} S_{a1}(t) &= \begin{cases} 1 & \text{if } M_a(t) \le V_{tri1}(t) \\ 0 & \text{otherwise} \end{cases} \\ S_{a2}(t) &= \begin{cases} 1 & \text{if } M_a(t) \le V_{tri2}(t) \\ 0 & \text{otherwise} \end{cases} \end{aligned} \tag{12.10}$$

where $V_{tri1}(t)$ and $V_{tri2}(t)$ are the triangular carriers and $M_a(t)$ is the phase 'a' modulation signal.



(a) (b)

Fig. 12.3. Space vector calculation for the amplitude modulation. (a) Schematic diagram, and (b) phasor diagram.

The switching function of the respective phase 'a' switches is expressed in (12.11), which describes the corresponding duty cycle distribution following the condition in (12.10) when the modulation signal crosses the edge of triangular carriers.

$$\begin{cases} S_{a1}(t) = 2[1 - m\sin\omega t] \\ S_{a2}(t) = 1 - 2m\sin\omega t \end{cases} \tag{12.11}$$

where m is the modulation amplitude obtained according to the space vector diagram in Fig. 12.3 and is expressed as follows:

$$m = \frac{2\sqrt{V_m^2 - \left(\frac{2\omega LP_{dc}}{3V_m}\right)^2}}{V_{dc}} \tag{12.12}$$

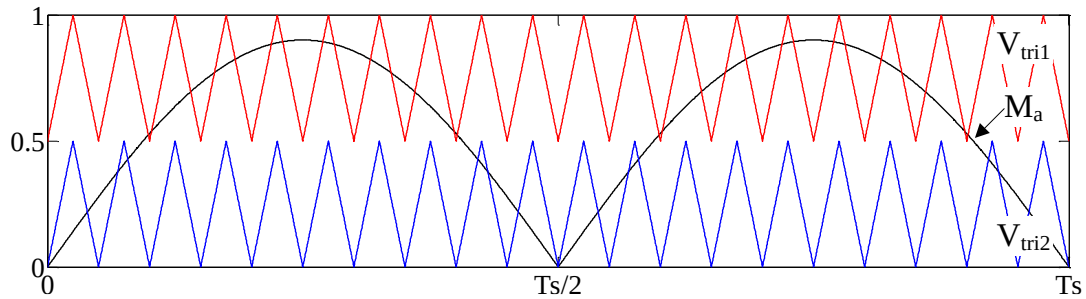


Fig. 12.2. Switching scheme for 5L-M^{2}UPFR topology.

V_m is the amplitude of the grid voltage, L is the input line inductance, ω is the angular frequency of the grid side expressed in terms of rad/s and P_{dc} is the output power of the rectifier.

12.3 Device Stresses for 5L-M^{2}UPFR Topology

In order to maintain a minimum safety requirement for the rectifier operation in the grid, an analytical approximation of the device stress level is calculated based on the presented analytical method as detailed in Chapters 10 and 11. To select the components rating for a 5L-M^{2}UPFR topology, a worst case operating condition is considered. The voltage stress level across the power device is selected according to the dc voltage reference set by the feedback control loop in the control algorithm and current stress of the power device can be determined by the minimum modulation indices as given in equation (12.12) for the minimum worst case scenario. The analytical approximation of the minimum voltage and current stresses is presented in the following subsection.

12.3.1 Voltage Stress

Voltage stress analysis is essential to prevent the power devices from being damaged and affect the reliability of the converter. Thus, minimum safety requirements and smooth operations can be assured with the proper blocking capability. Two conditions are assumed for the voltage stress analysis which are: (i) negligence of overvoltage caused by the parasitic inductance due to low switching frequency operation, and (ii) negligence of transient output dc voltage caused by the inrush current since pre-charging circuit is typically employed in the dc-link for practical cases.

The overall voltage stress for outer and inner cell of 5L-M^{2}UPFR is approximately V_{dc} and $3V_{dc}/4$ across the respective clamped dc-link capacitors to the negative dc rail. Therefore, the maximum voltage stress across each active component during the steady-state operation is expressed in the following.

Switching Elements:

$$\begin{cases} V_{Sa1} = \dfrac{V_{dc}}{3} \\ V_{Sa2} = \dfrac{V_{dc}}{4} \end{cases} \tag{12.13}$$

Switching Elements:

$$\begin{cases} V_{Da1} = V_{Da2} = V_{dc} \\ V_{Da3} = V_{Da4} = V_{Da5} = V_{Da6} = \dfrac{V_{dc}}{3} \\ V_{Da7} = V_{Da8} = \dfrac{V_{dc}}{2} \\ V_{Da9} = V_{Da10} = V_{Da11} = V_{Da12} = \dfrac{V_{dc}}{4} \end{cases} \tag{12.14}$$

12.3.2 Current Stresses

Several assumptions are made for the current stress analysis: (i) pure sinusoidal grid current without any ripple content, (ii) unity power factor, (iii) zero voltage dropped across the inductors, (iv) constant switching frequency, (v) balanced input grid condition and (vi) negligence of any losses in the balancing circuit. Hence, the average and RMS of the approximated global current stress are expressed in equations (12.15) to (12.16).

$$\begin{aligned} I_{Sai\langle avg\rangle} &= \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{\gamma_{ai}} I_a\left(kt_p,\omega t\right)\right]d\omega t \\ &\approx \frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{\gamma_{ai}t_p} I_a\left(\omega t\right)dt_\mu\right]d\omega t \end{aligned} \tag{12.15}$$

$$\begin{aligned} I_{Sai\langle avg\rangle} &= \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\sum_{k=t_{on}/t_p}^{\gamma_{ai}} I_a^2\left(kt_p,\omega t\right)\right]d\omega t} \\ &\approx \sqrt{\frac{1}{2\pi}\int_{\alpha}^{\beta}\left[\frac{1}{t_p}\int_{0}^{\gamma_{ai}t_p} I_a^2\left(\omega t\right)dt_\mu\right]d\omega t} \end{aligned} \tag{12.16}$$

γ_{ai} is the switching state function of the instantaneous grid current. k is the duty cycle during turn on period. α and β is the switching time occurring one fundamental period. Similarly, the current stress for the diode elements can also be expressed using the same expressions in (12.15) and (12.16).

Based on current stresses expression, the final expression of the current stresses for each power device is written as:

Average current stress:

$$\begin{cases} I_{Sa1\langle avg\rangle} = \dfrac{i_a}{\pi}\left\{2+2\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)+m_a\left[2\sin^{-1}\dfrac{1}{2m_a}-\pi-\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)\right]\right\} \\ I_{Sa2\langle avg\rangle} = \dfrac{i_a}{\pi}\left\{2-2m_a\sin^{-1}\dfrac{1}{2m_a}-\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)\right\} \\ I_{Da1\langle avg\rangle} = I_{Da2\langle avg\rangle} = \dfrac{i_a}{\pi}\left\{\dfrac{m_a}{2}\left[\pi+\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)-2\sin^{-1}\dfrac{1}{2m_a}\right]-\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)\right\} \\ I_{Da3\langle avg\rangle} = I_{Da4\langle avg\rangle} = I_{Da5\langle avg\rangle} = I_{Da6\langle avg\rangle} = \dfrac{I_{Sa1\langle avg\rangle}}{2} \end{cases}$$

$$\begin{cases} I_{Da7\langle avg\rangle} = I_{Da8\langle avg\rangle} = \dfrac{i_a}{\pi}\left\{\dfrac{3}{2}\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)-\dfrac{m_a}{2}\left[\pi+\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)-4\sin^{-1}\dfrac{1}{2m_a}\right]\right\} \\ I_{Da9\langle avg\rangle} = I_{Da10\langle avg\rangle} = I_{Da11\langle avg\rangle} = I_{Da12\langle avg\rangle} = \dfrac{I_{Sa2\langle avg\rangle}}{2} \end{cases}$$

(12.17)

RMS current stress:

$$\begin{cases} I_{Sa1\langle RMS\rangle} = i_a\sqrt{\dfrac{1}{\pi}\left\{\begin{array}{c}\pi+\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)-\sin^{-1}\dfrac{1}{2m_a}-\dfrac{1}{2m_a}\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)\\ +\dfrac{m_a}{3}\left[\cos\left(3\sin^{-1}\dfrac{1}{2m_a}\right)-9\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)\right]\end{array}\right\}} \\ I_{Sa2\langle RMS\rangle} = i_a\sqrt{\dfrac{1}{\pi}\left\{\begin{array}{c}\sin^{-1}\dfrac{1}{2m_a}-\dfrac{1}{2m_a}\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)\\ -\dfrac{16}{3}m_a\sin^4\left(\dfrac{1}{2}\sin^{-1}\dfrac{1}{2m_a}\right)\cdot\left[\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)+2\right]\end{array}\right\}} \end{cases}$$

$$
\begin{cases}
I_{Da1\langle RMS\rangle} = I_{Da2\langle RMS\rangle} = i_a \sqrt{\dfrac{1}{\pi}\left\{\begin{array}{l}\dfrac{m_a}{6}\left[9\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)-\cos\left(3\sin^{-1}\dfrac{1}{2m_a}\right)\right] \\ -\dfrac{1}{4}\left[\pi+\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)-2\sin^{-1}\dfrac{1}{2m_a}\right]\end{array}\right\}} \\
I_{Da3\langle RMS\rangle} = I_{Da4\langle RMS\rangle} = I_{Da5\langle RMS\rangle} = I_{Da6\langle RMS\rangle} = \dfrac{I_{Sa1\langle RMS\rangle}}{\sqrt{2}} \\
I_{Da7\langle RMS\rangle} = I_{Da8\langle RMS\rangle} = i_a \sqrt{\dfrac{1}{\pi}\left\{\begin{array}{l}\dfrac{1}{2}\left[\pi+\sin\left(2\sin^{-1}\dfrac{1}{2m_a}\right)-2\sin^{-1}\dfrac{1}{2m_a}\right] \\ +\dfrac{m_a}{6}\left[\begin{array}{l}\cos\left(3\sin^{-1}\dfrac{1}{2m_a}\right)-9\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right) \\ +16\sin^4\left(\dfrac{1}{2}\sin^{-1}\dfrac{1}{2m_a}\right)\cdot\left[\cos\left(\sin^{-1}\dfrac{1}{2m_a}\right)+2\right]\end{array}\right]\end{array}\right\}} \\
I_{Da9\langle RMS\rangle} = I_{Da10\langle RMS\rangle} = I_{Da11\langle RMS\rangle} = I_{Da12\langle RMS\rangle} = \dfrac{I_{Sa2\langle RMS\rangle}}{\sqrt{2}} \\
I_{C1\langle RMS\rangle} = I_{C4\langle RMS\rangle} = \sqrt{3\left(I^2_{Da1\langle RMS\rangle} - 3I^2_{Da1\langle avg\rangle}\right)} \\
I_{C2\langle RMS\rangle} = I_{C3\langle RMS\rangle} = \dfrac{I_{C1\langle RMS\rangle}}{2}
\end{cases}
\tag{12.18}
$$

12.4 Proposed Controller Design

The proposed control algorithm is implemented by employing MATLAB Simulink toolbox with the configuration parameter of fix time step based on Runge-Kutta ODE4 and the sampling time of the control algorithm is set at 90μs. The close-loop control system based on the proposed observer technique and power factor correction control loop is discussed in the following subsection:

12.4.1 Unity Power Factor Control

The proposed unity power factor control with both grid voltage and load current observers is shown in Fig. 12.4. The basic structure of this controller is constructed using Synchronous-Reference-Frame (SRF) current control [104]. However, the d-q transformation in SRF control requires complicated phase lock loop (PLL) design which limits the control bandwidth. Therefore, the in-phase quantities current control technique in the proposed control is implemented to eliminate the mentioned disadvantages of the d-q transformation. Moreover, two-phase operation is allowed with this proposed control which provides higher reliability in a three-phase power supply system [112].

This control method consists of dc-link voltage control at the outer loop and current control at the inner loop. The outer loop control computes the dc equivalent capacitors current and regulates the output dc-link voltage. Meanwhile, the load current is formulated from the power balanced principle as shown in the following:

$$V_{dc}I_{dc}(t)=\sum\left[V_{sn}(t)-L_s\frac{dI_s(t)}{dt}-R_sI_s(t)\right]I_s(t)+C_{eq}V_{dc}(t)\frac{dV_{dc}(t)}{dt} \quad (12.19)$$

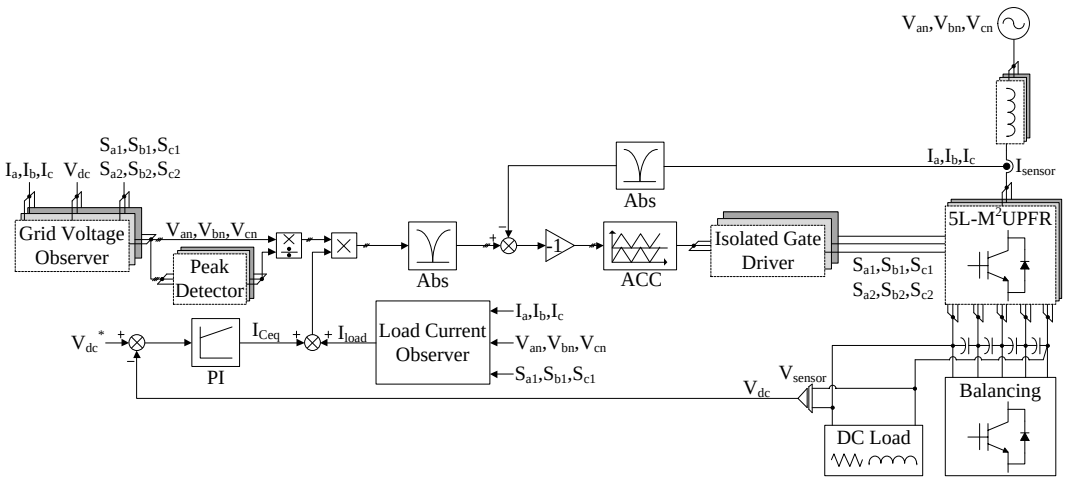


Fig. 12.4. Block diagram of the unity power factor controller with the proposed grid phase voltage and load current observers.

The actual load current measurement is replaced with the load current control loop of Fig. 12.5. The feed-forward observer technique is implemented to achieve better dc-link voltage tracking response during load change. The load current expression in (12.20) can be estimated from equation (12.19) assuming that the average power in the energy storage elements is zero.

$$I_{load} = \frac{V_{dc}\left(I_{Da1} + I_{Db1} + I_{Dc1}\right)}{V_{an} + V_{bn} + V_{cn}} \tag{12.20}$$

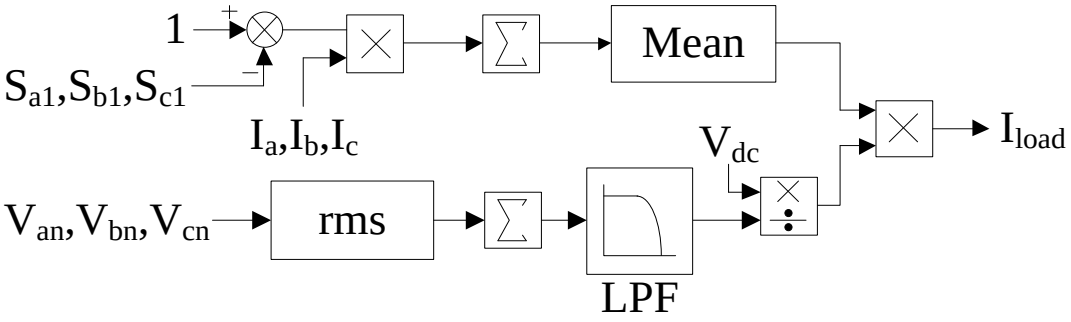
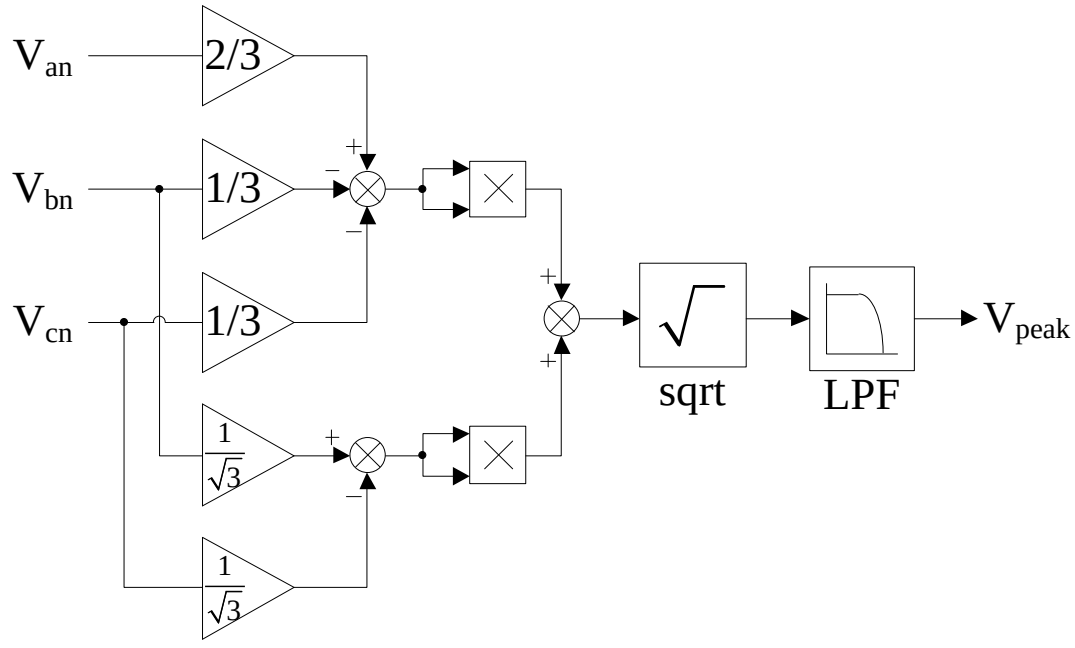


Fig. 12.5. Load current observer of Fig. 12.4 based on presented equation (12.20).



V_{an}, V_{bn} and V_{cn} are the rms value of grid phase voltage. V_{dc} and I_{dc} are the mean value of the dc-link voltage and output rectifier current respectively. Since six IGBTs are used in this rectifier configuration, the I_{dc} current can be easily obtained by using the feedback gating signals and the summation of the diodes current (I_{Da1}, I_{Db1} *and* I_{Dc1}) from equation (6) during the positive half period.

12.4.2 Voltage Control

In order to compute the equivalent dc capacitor current in the second term of (12.19), the dc-link voltage is regulated with a simple PI controller which is expressed as follows:

$$I_{Ceq} = K_p \frac{T_i s + 1}{T_i s}\left[V_{dc}^{*}(t) - V_{dc}(t)\right] \tag{12.21}$$

where K_p is the proportional gain of the dc-link voltage regulator and T_i is the settling time of the dc-link voltage tracking.

The approximation value of K_p is obtained from the energy storage model as shown in Fig. 12.7. The derivation of this model is based on the power balanced principle to determine the output equivalent dc capacitor current.

During the time interval from (t_0-t_1) of the charging period of the capacitors, the voltage variation due to the charge of energy storage, ΔE_{dc} is shown in the following expression.

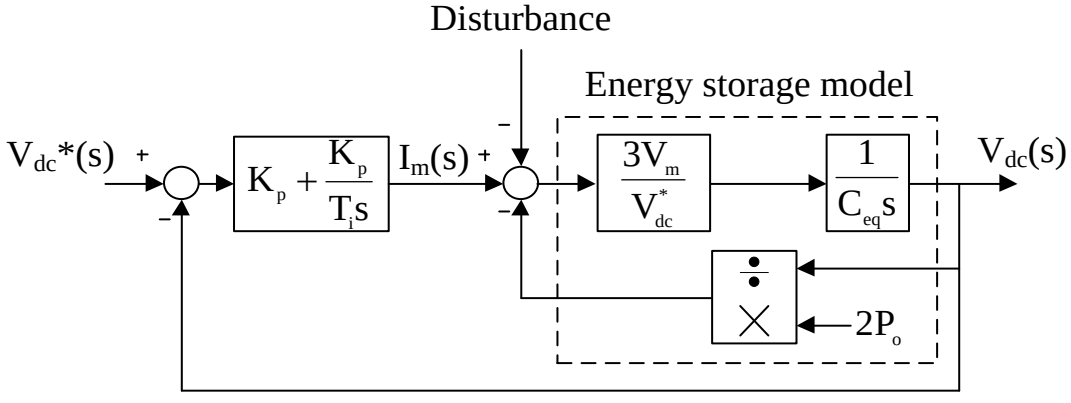


Fig. 12.7. Energy storage model of the output rectifier.

$$\Delta E_{dc} = \frac{C_{eq}}{2}\left[V_{dc}^2(t_1) - V_{dc}^2(t_0) \right] \tag{12.22}$$

The power of the C_{eq}, ΔP_{dc} in (12.23) is obtained from derivative of energy stored.

$$\Delta P_{dc} = \frac{C_{eq}}{2}\frac{dV_{dc}^2(t)}{dt} = \frac{3}{2}V_m I_m - P_o(t) \tag{12.23}$$

where V_m and I_m are the amplitude of the grid voltage and grid current. Assuming losses are neglected for the balanced three-phase system in this case.

According to stability criteria, the proportional gain of the control system expressed in (12.24) is derived from open-loop transfer function of Fig. 12.7 with the pole cancellation.

$$K_p = \frac{V_{dc}^3 C_{eq}}{6 P_o V_m} \tag{12.24}$$

where C_{eq} is the equivalent dc-link capacitors and P_o is the average output load power.

12.4.3 Current Control

The grid current control technique of the active rectifier can be classified into four main categories such as space vector modulation (SVM) [113], fix hysteresis band current control (FHBCC) [69, 71, 104], variable hysteresis band current control (VHBCC) [114],and average current control (ACC) [71, 115].The SVM scheme requires high computational effort due to the complex sector control algorithm required for higher voltage stepped level rectifier topology [116].Both HBCC and ACC can overcome the stated problems of SVM scheme. However, FHBCC scheme exhibits the disadvantage of variable switching frequency which complicates the design of the input inductance filter. The comparison performance of the FHBCC and ACC method is detailed in [71].

The carrier based ACC scheme is applied for the proposed 5L-M^2UPFR and allows the desired voltage space vector to be modulated using simple analog comparators. By doing so, lower cost implementation and lesser computational effort needed are achieved.

The input current shaping of 5L-M^2UPFR depends on the carrier based modulation scheme in Fig. 12.2 and the condition given in (12.10). Hence, the current error which is the difference between the measured current and the sinusoidal reference current template will be the modulation signal $M_a(t)$ of Fig. 12.2.

The sinusoidal reference current template is realized from the grid voltage and the peak detector as shown in the Fig. 12.4. The peak detector is designed based on the mathematical analysis of the space vector diagram as shown in in Figs. 12.3 and 12.6.

12.4.4 Grid Voltage Observer

Several observer techniques have been proposed for various types of rectifier configuration [66, 117, 118]. Besides the advantage of eliminating the sensors needed, the observer technique reduces the size of converter and provides a lower production cost as well. A PWM rectifier without voltage measurements is presented by Ohnuki *et al* in [66]. Even though the information of three-phase grid currents are sufficient to derive and estimate the AC and DC voltages, but large dc-link voltage ripples are experienced during the computational process. Hence, causing the input current THD to be considerably high. As a result, a bulky input inductor is required to filter the current distortion.

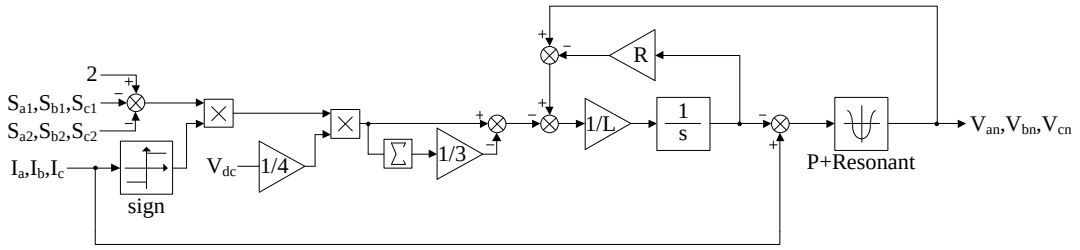


Fig. 12.8. Grid voltage observer of Fig. 12.4 based on equations (12.25) and (12.26).

In [66], a three-level VIENNA rectifier without current sensors is proposed. The power factor control is designed based on the phase angle difference between the grid and pole voltages of the rectifier, which is determined for calculating the modulation index space vector. Although this method provides a good dynamic response during load change, but unbalanced grid condition is not considered in this case.

The grid voltage observer of the proposed controller shown in Fig. 12.8 is modified from the single-phase two-stages PWM rectifier in [118]. High accuracy of grid phase voltage is estimated with three-phase grid currents and dc-link voltage measurements using the proportional + resonant control method. Low input current THD is achieved with the proposed observer and good dynamic response is performed as well for the case of one phase grid voltage down during operation.

The voltage across the input phase 'a' inductor is expressed as follows:

$$\begin{aligned} V_{La}(t)+V_{Ra}(t) &= V_{an}(t)-V_{am}(t)-V_{mn}(t) \\ &= V_{an}(t)-\frac{V_{dc}(t)}{12}\begin{Bmatrix} 2\left[2-S_{a1}(t)-S_{a2}(t)\right]\cdot \text{sign}\left(I_a(t)\right) \\ -\left[2-S_{b1}(t)-S_{b2}(t)\right]\cdot \text{sign}\left(I_b(t)\right) \\ -\left[2-S_{c1}(t)-S_{c2}(t)\right]\cdot \text{sign}\left(I_c(t)\right) \end{Bmatrix} \end{aligned}$$

(12.25)

$V_{mn}(t)$ is the virtual ground voltage of node m referred to the ground terminal of node n. $V_{Ra}(t)$ is the voltage drop across the inductor core resistor of phase 'a'.

The grid phase voltage can be calculated by expanding the voltage expression in (12.25) and it is given by

$$\tilde{I}_a(t)=\frac{1}{L_a}\int\left\{\begin{array}{c} V_{an}(t)-R_a\tilde{I}_a(t) \\ -\frac{V_{dc}(t)}{12}\left\{\begin{array}{l} 2\left[2-S_{a1}(t)-S_{a2}(t)\right]\cdot\mathrm{sign}\left(I_a(t)\right) \\ -\left[2-S_{b1}(t)-S_{b2}(t)\right]\cdot\mathrm{sign}\left(I_b(t)\right) \\ -\left[2-S_{c1}(t)-S_{c2}(t)\right]\cdot\mathrm{sign}\left(I_c(t)\right) \end{array}\right. \end{array}\right\}dt \qquad (12.26)$$

From equation (12.26), a proportional + resonant controller is used for the grid phase voltage estimation and is expressed in the following equation (12.27).

$$V_{an}(t)=\left[I_a(t)-\tilde{I}_a(t)\right]\cdot\left[K_p+\frac{K_r s}{s^2+\omega^2}\right] \qquad (12.27)$$

ω is the angular frequency of the grid side (ω = 314 rad/s) and proportional gain and resonant gain is chosen to be K_p = 3.25 and K_r = 125 respectively.

12.5 Simulation and Experimental Results

The laboratory prototype is developed with the control algorithm implemented in the dSPACE DS1103 development controller board to verify the performance of 5L-M^2UPFR. Both simulation and experimental results have proven the feasibility of the

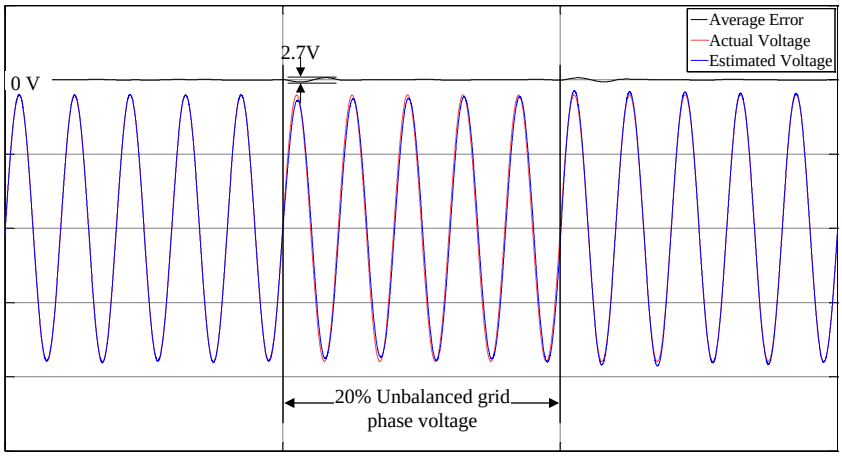


Fig. 12.9. Grid phase voltage of the estimation method and actual measurement.

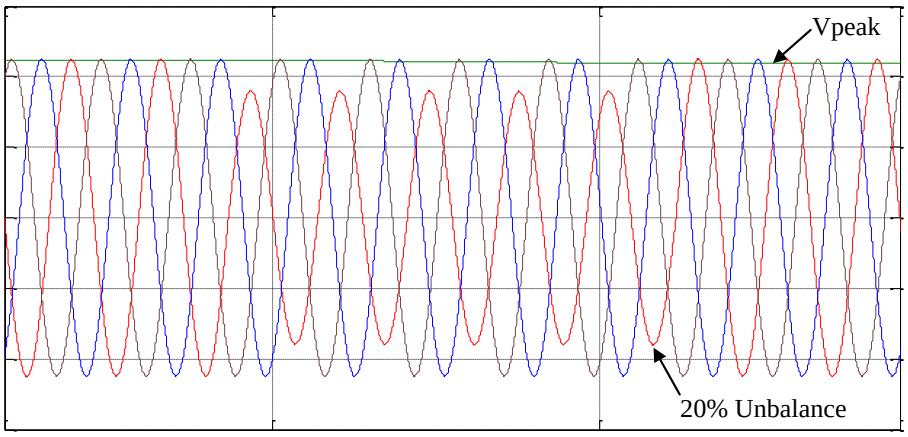


Fig. 12.10. Peak voltage measurement and three-phase grid phase voltage with one phase 20% unbalance.

proposed rectifier topology with the controller based on grid phase voltage and load current observers.

The dynamic response of the grid phase voltage estimation during unbalanced grid condition is verified with both estimation and actual measurement as shown in Fig. 12.9. In addition to that, the peak value of the grid phase voltage obtained by the peak detector is stable in Fig. 12.10 even during sudden grid phase voltage changed.

The experimental results in Fig. 12.11 show the input characteristic performance of the new 5L-M^{2}UPFR with the proposed controller under balanced grid supply condition. The power factor for balanced grid supply is high and low THD current is achieved with low input inductance filter.

On top of that, the experimental results in Fig. 12.12 show the feasibility study of the converter response during two phase operation with the same in-phase quantity current control. Even though one of the phase voltages is down during the operation, comparatively low THD current in Fig.12.12(c) is achieved with the same input inductance filter. With the supported experimental results, the proposed controller proved that high reliability of the three-phase power supply unit is achievable under extreme unbalanced grid condition.

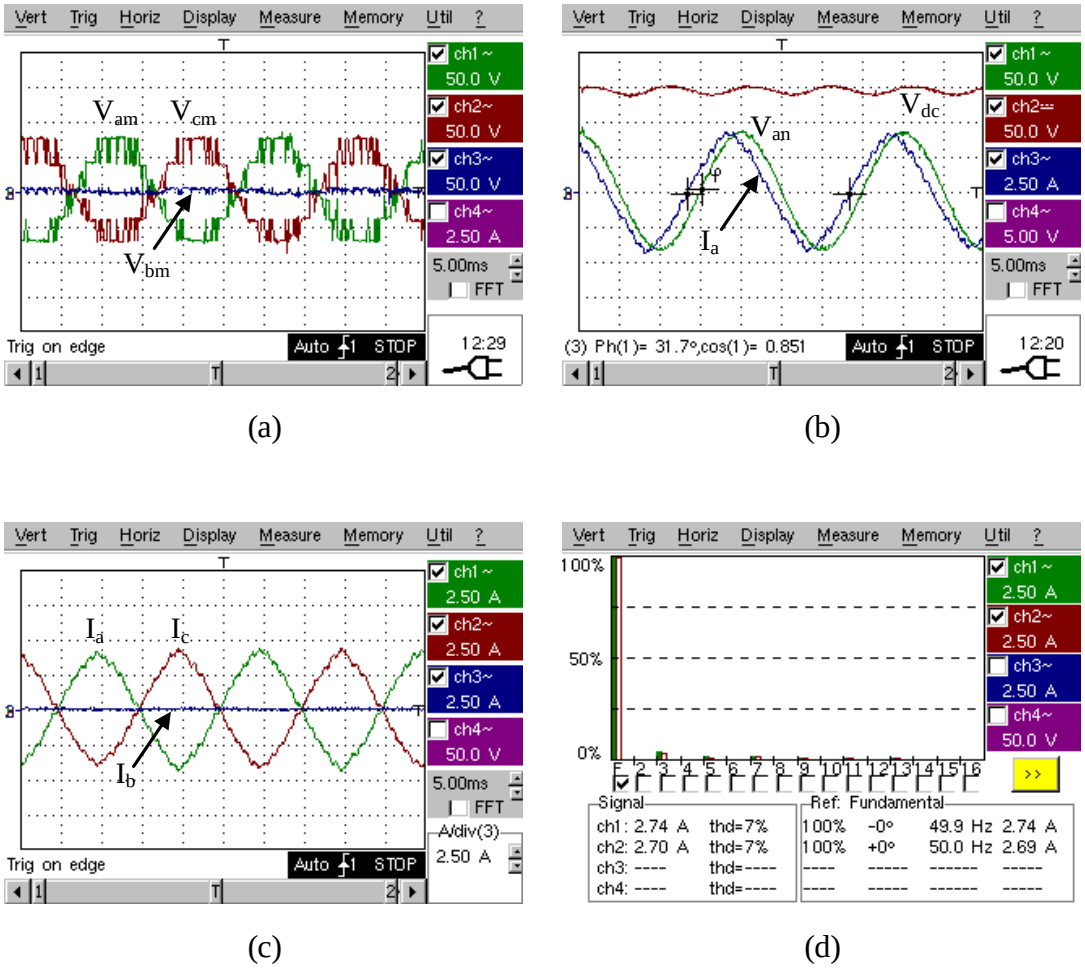


Fig. 12.12. Input voltage and current performance of a 5L-M^{2}UPFR topology under extreme unbalanced grid condition. (a) Input pole voltage, (b) dc-link voltage (upper trace), grid phase voltage and line current (lower trace), input line current, and (d) THD of line current.

Based on both experimental results obtained for balanced and unbalanced grid operation, five-level incremental stepped waveform is synthesized with the proposed low switching frequency carrier based ACC scheme. The proposed dynamic control with the observers reduces the cost implementation and the complexity of the algorithm.

12.6 Discussion

A new cost-effective 5L-M^{2}UPFR topology is introduced in this Chapter to achieve high power factor and low current distortion with drastically reduced in the total number of switching devices and sensors. Moreover, no isolated gate power supply is required for the rectifier side since there are no complementary switches used in this proposed rectifier topology. The great advantage of this proposed rectifier is that low grid current THD is achievable with constant low switching frequency operation and the reduced input inductance filter size

Both simulation and experimental results proved the dynamic response of the proposed in-phase quantities current control using observer technique. Therefore, the proposed controller provides higher reliability of the three-phase power supply even during the extreme unbalanced grid condition. Since grid voltage and load current observers are designed in the control loop, the reduction of sensors can avoid technical issues such as sensor failure and measurement errors. On top of that, light weight and high power density can be achieved for the proposed 5L-M^{2}UPFR topology.

Several technical challenges and improvements need to be considered for future development such as dc balancing and dc voltage ripple content occurred during extreme unbalance grid condition. However the dc voltage ripple can be filtered out by replacing larger filter capacitor. Thanks to the use of in-phase quantities current control using observer technique, a 0.85 power factor with low current distortion of 7% is achievable. The proposed rectifier with the control technique is recommended for high power application on AC/DC/AC drives for energy efficiency.

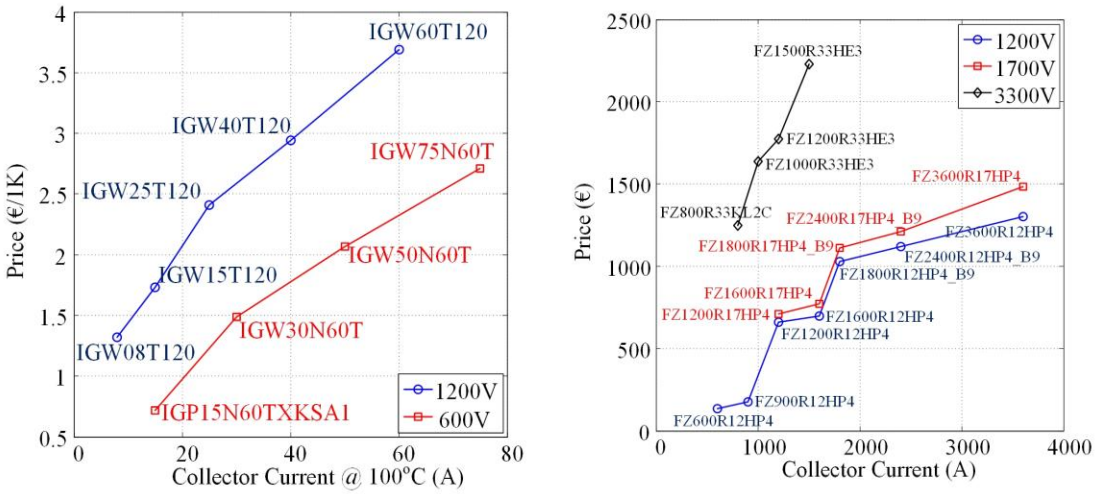
Chapter 13 – Comparative Evaluation and Selection of Multilevel Power Converters for Power Application

In this chapter, both switch-clamped and diode-clamped multilevel inverter/rectifier topologies are selected for the fair comparison including the two-level power converter. By analyzing the statistical results of all the physical performance, hence the type of multilevel power converters can be selected appropriately for the suitable power application. In order to verify the overall performances of these multilevel power converters with the single DC link configuration, several factors are considered for analyzing the comparative evaluation.

13.1 Cost Comparison

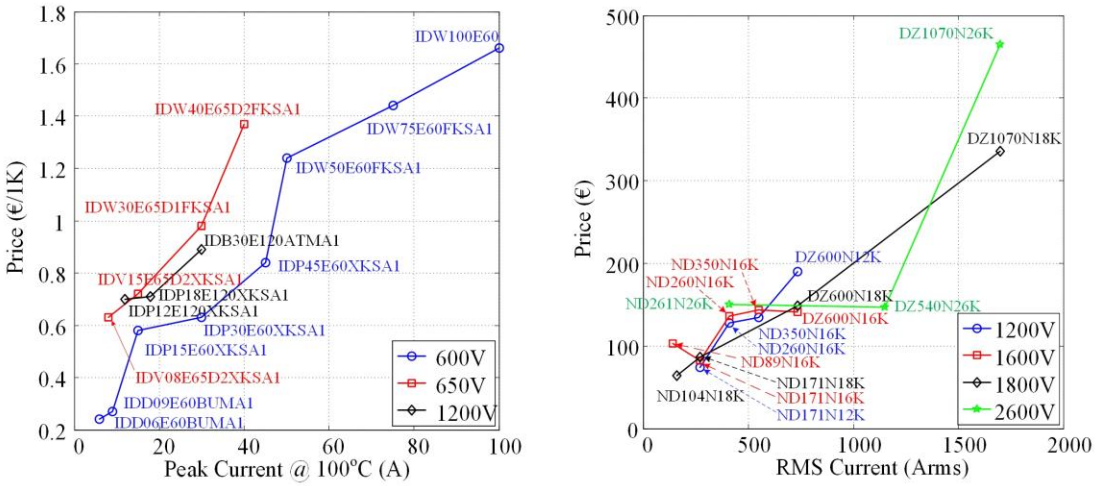
The selection of power semiconductor devices with the lowest cost possible is the core consideration for any industry, especially for constructing the multilevel power converters. Many existing multilevel power converters have been addressed with the improvement of the physical performance (i.e. efficiency, voltage and current quality and physical components dimension) as compared to other topologies. But the cost comparison of the multilevel power converters is not shown in many papers.

By observing the prices of the semiconductor devices in Figs. 13.1 and 13.2, the cost of the single IGBT device is linearly increased as a function of the current rating. When constructing a medium power application, a power module is usually selected for developing higher voltage and lower current application. For the minimized development cost consideration, the lower voltage rating with higher current switching device is much cheaper than the 3300V switching device as shown in Fig. 13.1 (b). Based on the statistical results given in Figs. 13.1 (a) and (b), the design of the multilevel power converters is good to have lower voltage stress for the cost saving, similarly for the diode components.



(a) (b)

Fig. 13.1 Cost comparison of single IGBT device rating reference to Infineon Technology. (a) Cost versus collector current rating – IGBT discrete component and (b) cost versus collector current rating – IGBT module.



(a) (b)

Fig. 13.2 Cost comparison of single diode device rating reference to Infineon Technology. (a) Cost versus anode current rating – diode discrete component and (b) cost versus anode current rating – diode module.

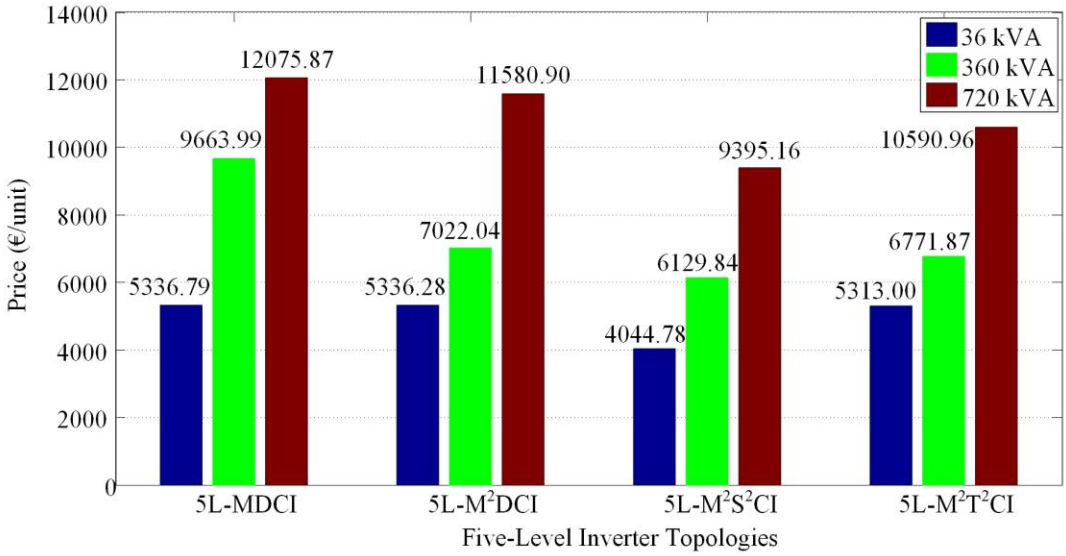


Fig. 13.3 Cost comparison of three-phase five-level inverter topologies include gate drives (F3L300R07PE4), IGBTs and Power Diodes.

In order to evaluate the cost of the multilevel power converters, few topologies are selected for the comparison with the classical five-level diode-clamped inverter as shown in Fig. 13.3. Based on the statistical result in Fig. 13.3, the 5L-M^2S^2CI topology offer the minimum cost for the low power application.

13.2 Filter Size Comparison

The AC filter of the AC supply or AC load are required to design in such a way that the quality of the input/output of the system are kept within the specified requirement as listed in the international IEEE standard. Taken into the consideration of the 50 Hz application, the minimum requirement of system is described shortly in the following.

[1] Peak-to-peak current ripple of the filter inductor must achieve as low as possible depending on the power level of the system. Low current ripple will lead to low grid current THD. The current distortion must be achieved less than 5% for the grid connected system.

[2] Peak-to-peak output voltage ripple of the L-C filter must achieve less than 5% THD of the output voltage which means a maximum of 5% of the peak-to-peak voltage ripple is allowed.

TABLE 13.1

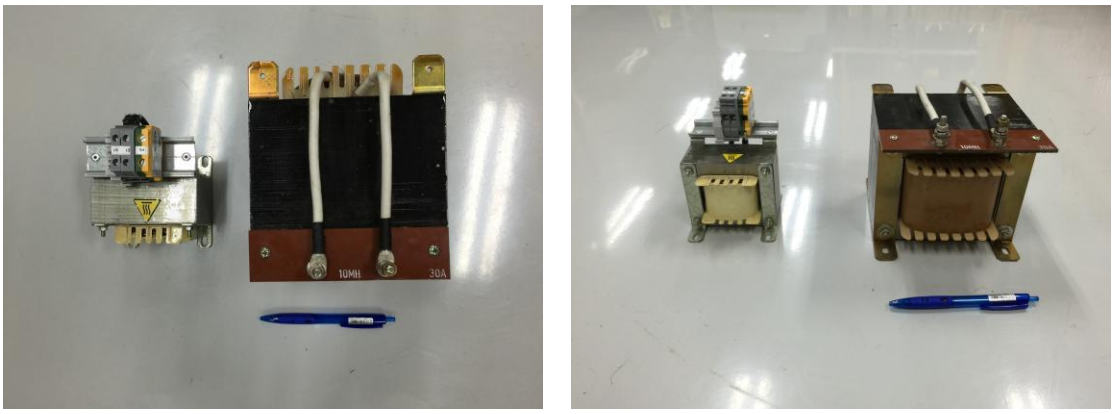
CURRENT RIPPLE EXPRESSION WITH RESPECTIVE MODULATION ANGLE

Voltage Level	Current Ripple Expression	
	$0^o \le \omega t < 30^o$	$30^o \le \omega t < 90^o$
2	$\Delta i_{L,rec,S(111)} = \frac{mV_{dc}}{8LF_s}\left[1+\frac{m}{2}\right]$ $\Delta i_{L,rec,S(101)} = \frac{V_{dc}}{2LF_s}\left[1+\frac{m}{2}\right]\left[\frac{m}{4}-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(001)} = \frac{V_{dc}}{2LF_s}\left[1+\frac{m}{2}\right]\left[\frac{m}{4}+\frac{1}{3}\right]$	$\Delta i_{L,rec,S(111)} = \frac{mV_{dc}}{4LF_s}[1+m]$ $\Delta i_{L,rec,S(101)} = \frac{V_{dc}}{2LF_s}[1+m]\left[\frac{m}{2}-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(100)} = \frac{V_{dc}}{2LF_s}[1+m]\left[\frac{m}{2}-\frac{2}{3}\right]$
3	$\Delta i_{L,rec,S(+0+)} = \frac{mV_{dc}}{4LF_s}\left[\frac{m}{2}-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(00+)} = \frac{V_{dc}\cdot m^2}{8LF_s}$ $\Delta i_{L,rec,S(-0-)} = \frac{mV_{dc}}{4LF_s}\left[\frac{m}{2}-\frac{1}{3}\right]$	$\Delta i_{L,rec,S(+-+)} = \frac{mV_{dc}}{2LF_s}\left[m-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(100)} = \frac{mV_{dc}}{2LF_s}[m-1]$ $\Delta i_{L,rec,S(100)} = \frac{mV_{dc}}{2LF_s}\left[m-\frac{1}{3}\right]$
5	$\Delta i_{L,rec,S(P_2N_1P_1)} = \frac{V_{dc}}{4LF_s}[m-1]\left[m-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(N_2N_1P_1)} = \frac{V_{dc}}{4LF_s}[m-1]\left[m+\frac{1}{3}\right]$ $\Delta i_{L,rec,S(N_20P_2)} = \frac{V_{dc}}{4LF_s}[m-1]\left[m-\frac{1}{3}\right]$	$\Delta i_{L,rec,S(P_1N_1P_2)} = \frac{V_{dc}}{LF_s}[2m-1]\left[\frac{m}{2}-\frac{1}{3}\right]$ $\Delta i_{L,rec,S(P_1N_1N_2)} = \frac{V_{dc}}{2LF_s}[2m-1]\left[m-\frac{5}{6}\right]$ $\Delta i_{L,rec,S(P_1N_1P_2)} = \frac{V_{dc}}{LF_s}[2m-1]\left[\frac{m}{2}-\frac{1}{3}\right]$

Theoretically, the volume of the inductor is linearly increased with the inductance value as detailed in [119] and the volume of two to n-level power converter ratio is expressed as.

$$V_{n-level} = \frac{L_{n\text{-level}}}{L_{2L}} V_{2L} \tag{13.1}$$

$V_{n\text{-level}}$ is the volume of the inductor for n-level converter, similarly for V_{2L} is the volume of the inductor for two-level converter. $L_{n\text{-level}}$ and L_{2L} is the inductance value for n-level



(a) (b)

Fig. 13.4 Physical size of the AC inductor. (a) Top view and (b) side view.

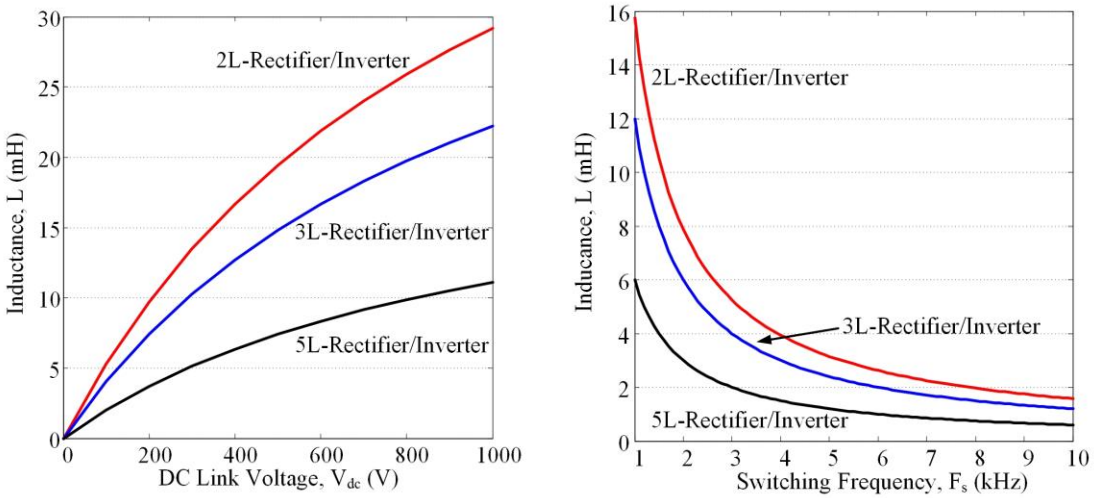
and two-level converters respectively. The physical dimension of 10 mH and 1.6 mH with the current rating of 30 and 26 A_{rms} is shown in Figs 13.4 (a) and (b). This shows that the volume of the inductor is scaled proportionally to the inductance value.

Moreover, the losses of the inductor are also proportionally scaled with the volume of the inductor [120] and the relationship between the inductance and power loss of the inductor is expressed as:

$$P_{loss,L} \propto L^{2/3} \tag{13.2}$$

In order to obtain the inductance value, the current ripple expression has to be analyzed first. The final current ripple expression of the general two, three and five level power converters are given in Table 13.1. Detailed derivation of the current ripple for the respective converters is presented in Appendix B.

According to the formulated current ripple expression in Table 13.1, the maximum current ripple is selected for obtaining the minimum inductance as shown in (13.3). Based on the maximum current ripple, the modulation index of 1 has the highest peak-to-peak current ripple value for all converters as shown in Fig. 13.5 (a).



(a) (b)

Fig. 13.6 Inductance comparison curve for the respective n-level rectifier/inverter based on 30% of the nominal AC amplitude current of 25 A and modulation, m =1. (a) Inductance versus DC link voltage and (b) Inductance versus switching frequency with V_{dc} = 270 V.

$$\begin{cases} \Delta i_{L,2L} = \dfrac{V_{dc}}{2LF_s}\left[1+\dfrac{m}{2}\right]\left[\dfrac{m}{4}+\dfrac{1}{3}\right] \\ \Delta i_{L,3L} = \dfrac{mV_{dc}}{2LF_s}\left[m-\dfrac{1}{3}\right] \\ \Delta i_{L,5L} = \dfrac{V_{dc}}{LF_s}\left[2m-1\right]\left[\dfrac{m}{2}-\dfrac{1}{3}\right] \end{cases} \tag{13.3}$$

Comparing the current ripple for various n-level power converters, the five-level power converter achieves the smallest ripple among the two and three-level power converters at high modulation range. By observing the current ripple versus switching frequency range in Fig. 13.5 (b), high switching frequency is not required for 5L power converter. Therefore, 1~5 kHz switching frequency range is sufficient for 5L power converter operation.

According to maximum current ripple in (13.3) with the 30% of the nominal AC current limit consideration, the minimum inductance is analyzed in Figs. 13.6 (a) and (b). By

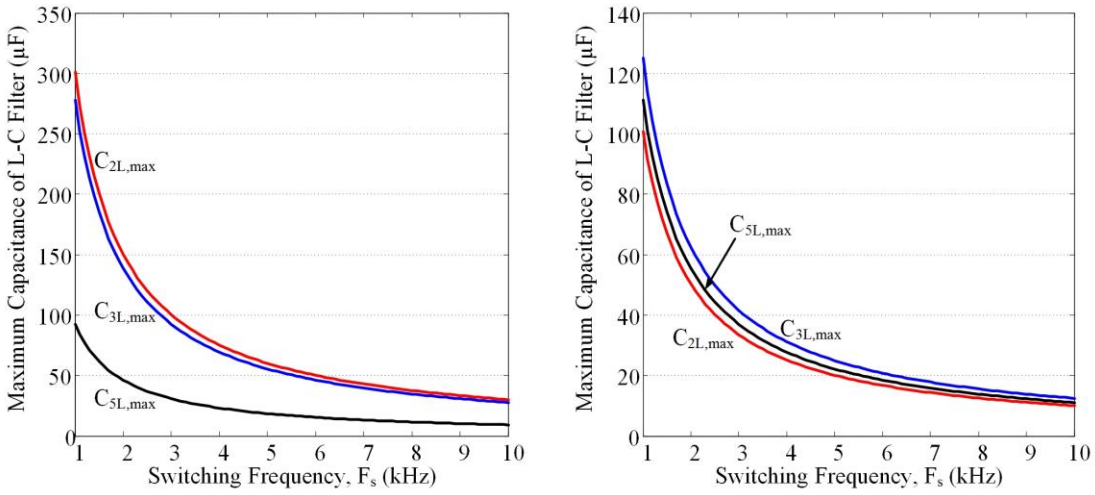


Fig. 13.7 AC Capacitance comparison curve for the respective n-level inverter based on 30% of the nominal AC amplitude current of 25 A and 5% of the nominal output voltage of the LC filter under V_{dc} = 270 V. (a) Inductance versus switching frequency at m = 0.6 and (b) Inductance versus switching frequency at m = 0.9.

observing the inductance expression formulated in (13.3), the inductance value depends on the relationship between the DC link voltage and the AC voltage amplitude, as well as the PWM switching technique used. The reduction of the inductance also depends on the current rating of the load as stated in the current ripple expression. One can finalize that the volume and losses of the filter inductor for five-level rectifier/inverter can be reduced significantly based on the relation given in equations (13.1) and (13.2).

L-C filter design is often implemented with the inverter for the motor drive application to minimize the risk of experiencing high voltage stress in the motor winding or even designing an AC power supply. To stabilize the output performance of the L-C filter, the maximum cut-off frequency is selected according to the switching frequency of the inverter. With this assumption consideration, one can calculate the final expression of the minimum capacitance value for n-level inverter topologies, $C_{n\text{-level,min}}$ is given as:

$$C_{n-level,min} \geq \frac{1}{4L_{n-level}\pi^2 F_s^2} \tag{13.4}$$

Besides that, the maximum capacitance of the filter for achieving low peak-to-peak output voltage ripple of the L-C filter can be calculated based on the capacitive current expression. Further simplifying the analysis of the capacitive current, let assumes the current ripple of the capacitor is similar to the inductive current ripple in the single-stage L-C filter. Therefore, the current ripple expression of the inductor in the L-C filter (second order filter) is assumed to be similar to the filter inductor (first order L filter) in the rectifier operation. With the assumptions stated above, the relationship between the permissible voltage ripple and the maximum capacitance of the L-C filter referred to the inductor current ripple in equation (13.3) is finalized as:

$$\begin{cases} C_{2L,max} = \dfrac{V_{dc}}{16L_{2L}\Delta V_C F_s^2}\left[\dfrac{m}{4}+\dfrac{1}{3}\right]\left[1+\dfrac{m}{2}\right]^2 \\ C_{3L,max} = \dfrac{V_{dc}m^2}{8L_{3L}\Delta V_C F_s^2}\left[m-\dfrac{1}{3}\right] \\ C_{5L,max} = \dfrac{V_{dc}}{4L_{5L}\Delta V_C F_s^2}\left[\dfrac{m}{2}-\dfrac{1}{3}\right]\left[2m-1\right]^2 \end{cases} \tag{13.5}$$

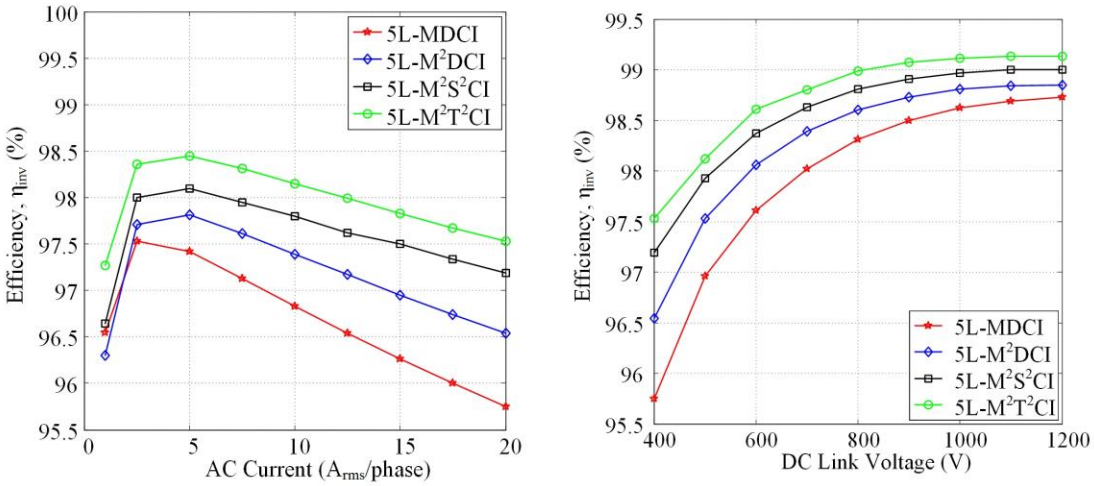
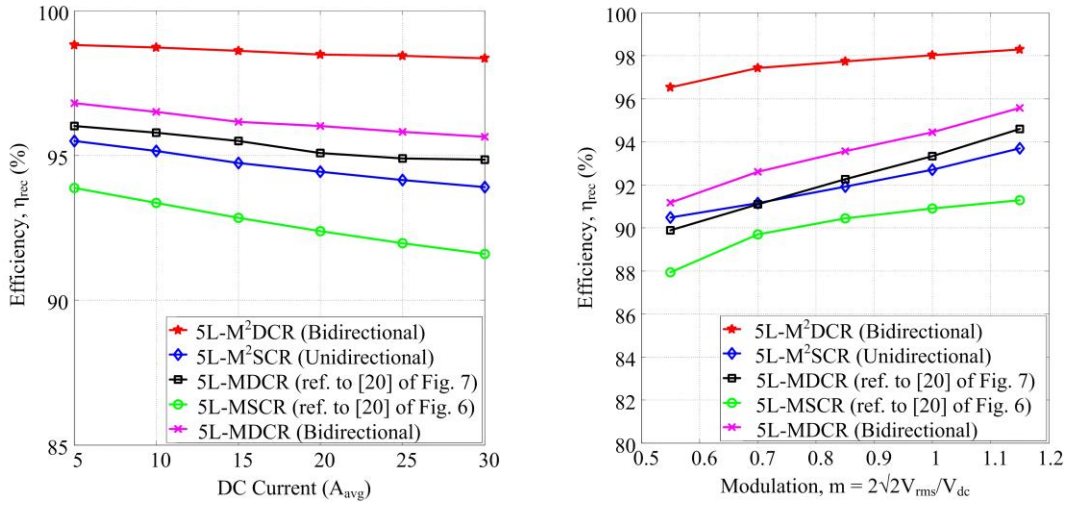


Fig. 13.8 Simulated efficiency based on five-level diode-clamped and switched clamped inverters family with the parameters of 1 kHz, PF = 1 and M = 0.9. (a) Efficiency versus output per-phase current rating based on constant DC link voltage, V_{dc} = 400 V and (b) efficiency versus input DC link voltage rating based on constant power, $P_{ac,3\phi}$ = 7.15 kW ± 2%.



(a) (b)

Fig. 13.9 Simulated efficiency for unidirectional and bidirectional rectifiers based on five-level diode-clamped and switched clamped rectifiers family with the parameters of 1 kHz and PF = 1. (a) Efficiency versus DC load current at V_{ac} = 110V_{rms}/phase and V_{dc} = 270V, and (b) efficiency versus modulation depth at P_{dc} = 9.33 kW.

The maximum capacitance curve with respect to the permissible voltage ripple at 5% of the nominal output AC voltage is low for five-level inverter as compared to the two and three-level inverters. But for a high modulation operation, the required AC capacitance is higher than the two and three-level inverter (ref. to Fig. 13.7), which is used for the practical consideration. However, the overall weight and volume of passive element including the inductive component employed in the inverter is still consider small as compared to the two and three-level inverter.

13.3 Efficiency Comparison

The mathematical loss analysis of the semiconductor devices for the presented power converters are detailed in Chapter 8. With the analytical assumptions given, the efficiency of the power converters in this Chapter considered only the semiconductor devices losses. However, the passive components loss is not included for the efficiency comparison since the same switching PWM technique is used. Therefore, the efficiency of the 5L inverters and 5L rectifiers are determined directly from the PSIM circuit

simulator with the supported Thermal Module version 9.0.3. The efficiency of the power converters is determined by the ratio between the output power and the input power of the power converter. The input power is determined by summing up the output power of the converter with the individual active components losses. Finally, the efficiency is represented as:

$$\eta = \frac{P_{out}}{P_{out} + P_{IGBT,loss} + P_{Diode,loss}} \tag{13.6}$$

Figs. 13.8(a) and (b) show the efficiency curve comparison of the 5L inverters. The proposed 5L inverter topologies with the multiple-pole hierarchy achieved higher efficiency as compared to the conventional 5L inverter due to the zero current switching performance. Among the proposed 5L inverters, the efficiency rate of the power inverter is increased with the reduction of total amount of semiconductor devices used (ref. to 5L-M^2T^2CI has the highest efficiency as compared to other topologies). The efficiency of the 5L inverter also depends on the DC link voltage operation, which can observed from Fig. 13.8(b). Due to the relatively low switching frequency operation, the switching loss of the semiconductor device is not affected much by the DC link voltage operation with constant output AC power.

On top of that, the efficiency comparison of the 5L rectifiers configuration with the system operation close to unity power factor is shown in Figs. 13.9(a) and (b). Low grid current distortion is exhibited with the near unity power factor operated rectifier. This system operation allows the DC link voltage to be controlled which particularly fit for the rear-end 5L inverters so that a wider input voltage range can be achieved. The Fig. 13.9 shows that the efficiency of the bidirectional 5L-M^2DCR topology achieves better efficiency as compared to other 5L rectifier topologies (ref. to [20] of Figs. 6 and 7) under modulation index, m = 1.15. On top of that, the efficiency curve of the 5L-M^2DCR topology is almost constant as a function of DC current as shown in Fig. 13.9(a). For high modulation range above 0.7, the efficiency of the conventional 5L-MDCR is higher than the proposed 5L-M^2SCR topology. Due to the high conduction loss experienced in the inner pole, the unidirectional 5L-MDCR has lesser diode component count connected in the series from DC+ to DC- terminal as compared to the proposed

unidirectional 5L-M^{2}SCR topology. Therefore, reduced series-connected diode components count between the DC+ to DC- terminal has to be considered for designing a unidirectional power rectifier.

13.4 Discussion

Comparative evaluation of both 5L inverters and 5L rectifiers is presented to determine the overall performances of 5L power converters based on the proposed multiple-pole hierarchy. The advantage of designing higher voltage level power converters (inverter and rectifier) is to reduce the size of the passive element in the three-phase system. The volume of the inductive components can be reduced by minimizing the inductance value as well the power loss of the core. Although the size of the capacitive component in the LC-filter is large for particular modulation index, but the weight of the inductor is remained significantly lower than the two to three-level power converters. Therefore, the volume and weight of the AC capacitor in the L-C filter is not a critical issue as compared to the inductor filter.

In addition to that, a short comparison of both cost and efficiency are also presented in this Chapter for the 5L power converters. For the given 5L inverters including the proposed multiple-pole hierarchy, the efficiency of the 5L-M^{2}T^{2}CI topology is still better than the other presented 5L inverters. However, the cost of the 5L-M^{2}S^{2}CI topology is much lower than the cost of the 5L-M^{2}T^{2}CI. Due to the reduced number of high power IGBT modules and gate drivers used in the 5L-M^{2}S^{2}CI, the cost can reduce approximately by 1k ~ 3k euro when compared to the rest of the presented topologies as shown in Fig. 13.3. The cost is not much reduced for developing 5L power converters with the discrete IGBTs since the cross sectional area of the chip is small.

In the rectifier operation, the efficiency comparison of the selected 5L rectifier is presented. The efficiency of the diode-clamped topology (ref. to Bidirectional 5L-MDCR) with the IGBTs connected in series from the positive to negative DC rail can be increased when compared to those series-connected diodes type in the phase leg (ref. to [20] of Fig. 6, 5L-MSCR topology). Therefore, the only possibility of improving the efficiency to the maximum is achieved by reducing the amount of diode-clamped such

as developing the bidirectional 5L-M^2DCR topology. However, the cost of developing the 5L-M^2DCR topology is high which results similar to the 5L inverters. Overall, this concluded that there is a tradeoff between the cost and efficiency of the 5L power converters.

Chapter 14 – Conclusion and Future Works

14.1 Summary

In Chapter 3, a proposed power balance control strategy based on in-phase current control principle with a novel fixed hysteresis band switching scheme is presented. The propose feedback controller for a three-phase/three-switch/three-level rectifier is implemented with an additional control loop to balance the output rectifier's capacitor voltage. Balanced dc-link capacitor voltages algorithm is based on the decoupling zero sequence current control. Detailed analysis and theoretical concept of the control algorithm is provided. The fixed hysteresis band current control allows the rectifier to shape the current near to sinusoidal and achieve near unity power factor at input grid. This topology can be operated at high switching frequency in order to reduce the size of the input line-inductance. In-phase current control method as well allows two-phase operation with good dynamic response on the AC side.

In Chapter 5, a mathematical model of three-level NPC and flying capacitor inverters is presented. Mathematical model of both converters is derived according to the switching state function analysis. The switching function of the respective switches is calculated based on the control signal edge crossover of the carrier waveform. This analysis is used to observe the dominant low order harmonic of the neutral-point-clamped current (3L-MDCI/NPC) and flying capacitor current (3L-MFCI) during balance capacitor voltage condition The experimental analysis of diode-clamped NPC demonstrates that during balanced voltage condition triplen harmonic current flows through the neutral point of the dc-link capacitor bank. In flying capacitor operation, the harmonic current through the floating capacitors is of even order. In the sense that both three-level inverters is operating at symmetrical three-level output voltage waveform when the dc capacitor voltages is balanced.

In Chapter 6, a passive and active balancing method for three-level NPC topology is proposed and analyzed. In a passive balancing approach, RC filter is connected at the output terminal of the three-level NPC inverter. While the active balancing method is the developed with an additional DC offset modulation. This modulation signals scheme

is used to compensate an actual DC component of the output voltage, which limits the dc capacitor voltage error to minimum. By comparing both the methods, passive balancing method does not require any additional dc capacitor voltage measurement and this can be simply designed with any film type capacitive material. As for the active balancing method, it does not require any passive elements to balance the capacitor voltage. This allows the converter to operate at a higher efficiency as ohmic losses occurring in capacitors are eliminated.

In Chapter 7, AC/DC/AC drives with two types of five-level rear-end multilevel inverter (5L-MDCI and 5L-MFCI) topologies are constructed and investigated. Both topologies for a front-end rectifier and rear-end inverter are connected through an intermediate single dc-bus. With the single dc bus configuration, both rear-end multilevel inverters will experience an unbalanced capacitor voltage in dc-link (for 5L-MDCI) and floating capacitors (for 5L-MFCI). However, 5L-MFCI topology can be balanced by simply using the phase-shifted PWM technique and RC filter. In 5L-MDCI configuration, the voltages across both the capacitors connected to neutral point decay to zero resulting in a three-level output voltage waveform. By observing the obtained experimental results, the efficiency of the drive is dependent on the THD content of the voltage and current waveform. A 5L-MDCI topology associated with a balancing circuit can be considered as an alternative topology with its reduced capacitive component count. Reduction in component count improves reliability as it mitigates the adverse effect of thermal aging and inrush current. This type of configuration can improve the overall efficiency if the number of components count is reduced.

In Chapter 8, several new topologies for five-level inverters with reduced part count are proposed. The proposed topologies are classified as multiple-pole multilevel diode-clamped inverter (M^2DCI), multiple-pole multilevel t-type-clamped inverter (M^2T^2CI) and multiple-pole multilevel single-switch-clamped inverter (M^2S^2CI). The first proposed topology is known as 5L-M^2DCI, which is modified from single-pole hierarchy to multiple-pole. The number of diode components is reduced by increasing the number of poles. This allows the converter to achieve low conduction loss and low capital cost. On top of that, 5L-M^2DCI topology achieves zero current switching for a particular switching state. The current through the clamped diode and switches can be

replaced by a bidirectional switch to form a more compact and an optimum 5L-inverter topologies. This type of configuration is more suitable for low voltage, and low to medium power applications. Although, devices of higher rating are required for the outer cell switches.

In Chapter 9, a single input multiple outputs (SIMO) balancing circuit for 7L-M^{2}DCI and 7L-AM^{2}DCI topologies are proposed. The balancing circuit equalizes the voltage across the six dc-capacitors supplying power to a 7L inverter. Open-loop control algorithm examines the balancing capability of the circuit with a fix duty ratio. The balancing circuit allows the switching devices to operate at a lower voltage stress. 7L-AM^{2}DCI topology is an alternative seven level inverter topology, which reduces the number of diode units. However, this topology requires additional inductive components to limit the circuiting current flow and prevent any additional voltage spike across the switches. The 7L-AM^{2}DCI provides low voltage stress across each power device as compared to the M^{2}DCI topology. Hence, switches of lower power rating are to limit the losses to the minimum.

In Chapter 10, an experimental prototype demonstrates the possible modifications of a multiple-pole multilevel diode-clamped inverter to operate as a rectifier. Two types of five-level rectifier configuration (bidirectional and unidirectional topologies) investigate the input and output performance for the AC to DC power conversion. A simple synchronous reference frame (SRF) current control technique based on level-shifted PWM scheme applied in 5L rectifiers is proposed. According to the obtained experimental results, both configurations provides below 6% THD at 1 kHz switching frequency operation and 0.99 power factor with balance three-phase supply. By comparing both configuration (5L-M^{2}DCR and 5L-M^{2}SCR), the unidirectional 5L-M^{2}SCR provides more uniform current ripple and more regular switching pattern for the power switches. Moreover, five-level incremental input pole voltage waveform helps in reducing the inductive components size at low switching frequency operation. Theoretical analysis of the proposed front-end 5L rectifiers in AC/DC/AC based on multiple-pole approach has been discussed and experimentally verified.

In Chapter 11, the proposed control switching scheme for five-level multiple-pole VIENNA rectifier topology (5L-M^2VR) is discussed where the optimum efficiency of the rectifier is considered. The structure of this rectifier is derived based on a multiple-pole approach as detailed in Chapter 10. Switching loss of a 5L-M^2VR topology is reduced if the switching frequency of the carrier waveforms is reduced. A very low switching frequency range applies in a 5L rectifier topology, the input inductors are required more effort to minimize the ripple current. Hence, alternative control method for achieving optimum performance on low THD current and better efficiency of the rectifier can be simply designed by using the proposed independent switching scheme for the respective switches. The switching scheme of achieving low discrete components loss incorporates short conduction period control for inner cell switch and low switching frequency like LS-PWM or PS-PWM technique for outer cell switch. With the combination switching operation of a 5L-M^2VR, the output DC voltage is well regulated and low THD current (below 6%) is achieved with the short conduction period occur in the inner cell switch.

In Chapter 12, the size and cost of a propose five-level/multiple-pole multilevel unity power factor rectifier (5L-MUPFR) is optimized by developing with the observer control technique. The observer control technique includes grid phase voltage and load current estimators. Both estimated measurement is to replace the actual measurement sensors to achieve more compact fabrication board with reduce number of physical isolation circuits board. The observer control technique is implemented for the in-phase current control to achieve high dynamic response on the three-phase grid for two-phase operation. A feed-forward current control technique based on the load current observer is to maintain good dynamic response for sudden load change as discussed in Chapter 3. Besides having the advantage of this observer control technique, several technical issues such as sensor failure and measurement errors can be minimized. Theoretical analysis of the observer control technique with the in-phase current control is experimentally verified.

The entire work of this thesis is to conclude the contribution of the proposed method and topologies, and several recommendations for the future works are also provided in the following sections.

14.2 Thesis Conclusion

The multilevel rectifier and inverter topologies are primarily analyzed and experimentally verified. In order to understand the characteristics of higher-level multilevel inverters, a three-level converter is thoroughly analyzed initially. Classical three-level converters will partially possess unbalanced dc capacitor voltages. This unbalanced condition will increase the amplitude of low order harmonic components, which are injected from the neutral-point-clamp to load. Thus, active and passive balancing control methods for the partial unbalanced capacitor voltage condition in three-level inverter are proposed and analyzed. The analysis demonstrates that passive balancing method offers inherent advantage of equalizing dc-bus capacitor voltage in three-level diode-clamped inverter and also for more than three-level flying capacitor inverter topologies. While active balancing method can balance two capacitor voltages in the dc-link and stabilize the neutral-point-clamped current. This is achieved by injecting a dc-offset modulation to the control signal.

For a three-phase/three-switch/three-level rectifier operation, a decoupled current control method with fixed hysteresis band operating at high switching frequency is proposed. The control method is to limits the input current ripple to the minimum and achieves a stable balanced capacitor voltage. This is achieved by injecting a zero sequence current component to compensate for the circulating current flow from neutral-point of the dc-link to the ground potential of the grid.

In practice, a three-level rectifier and a higher-level inverter are combined form a drive system in order to minimize the switching frequency range and reduce/eliminate the requirement of the filter. By operating at a lower switching frequency, multilevel converters eliminate the necessity to resort to various soft-switching techniques and snubber circuits. In addition to that, no EMI filter is required when operating at a switching frequency range is less than 10 kHz. In a single dc-bus configuration, 5L flying capacitor topology can be a preferable solution for self and natural balance of the floating capacitor voltage as compared to a 5L diode-clamped inverter topology. However, higher number of floating capacitors is required to achieve five-level

incremental voltage stepped waveform. This will lead to poor thermal aging of the dc capacitors and it requires slow start up for preventing any inrush current flow through to the floating capacitors.

The proposed five-level inverter topology with reduce components count is known as five-level/multiple-pole multilevel diode-clamped inverter. This topology offers advantages such as reduction in component number and zero current switching for a particular switching state which result in lower device losses. To obtain a further lower component count (isolated gate driver and switches), T-type clamped and single-switch clamped inverter based on multiple-pole approach is proposed. The proposed 5L-M^2T^2CI and 5L-M^2S^2CI topologies consist of 6 isolated gate drivers (Toshiba TLP250) to control the IGBT devices and minimize/eliminate the use of any dead-time analog or digital circuit for preventing any shoot-through in the dc-link capacitors.

A five-level/multiple-pole multilevel inverter can as well operate in rectifier mode provided the converter has a UPF control system. The experimental results demonstrate the reduction of the filter size at 1 kHz switching frequency operation with THD well below 6%. Moreover, total number of power switches utilized in unidirectional rectifier is greatly reduced. The diodes connected in the top and bottom phase leg of each respective cell provide more regular and stable switching pattern, which are switch on and off based on the switching pattern of the adjacent IGBT clamped. Two types of feedback controls (Synchronous-Reference-Frame (SRF) current control and In-Phase Quantity Current Control) are experimentally tested in the laboratory. Both control methods provide stable input grid current with low THD under balanced three-phase grid supply. However, a three-phase five-level rectifier with SRF current control method has poor current regulation during two phase operation, while PLL cannot track the phase angle obtained efficiently.

With the in-phase current control method, overall components count and global reliability of 5L rectifier is further optimized by incorporating observer control technique. This observer control technique only requires three current measurements and one dc-link voltage measurement to estimate the three-phase grid voltage and load current. By employing this observer control into an in-phase current control technique,

the number of physical measurements required and impact of environmental factors (i.e., accuracy and failure) are reduced. The sensors for physical measurement used are based on LEM voltage and current transducers. The closed loop LEM transducers using the principle of Hall Effect to isolate high power side and low power side of an analog-to-digital (ADC) port. Accuracy of this sensor measurement is important for wide variety load power applications and the accuracy depends on the resistance value of the output measurement, which varies due to loading effect of the power level. To achieve better accuracy measurement, linear operational amplifier is connected to the output pin of LEM transducer to achieve minimal error at the ADC port. The experimental prototype with observer control technique achieves 50% error reduction in physical measurement of parameters and as well the isolation space between high power and low power sides is minimized.

In order to optimize the switching loss to the minimum, alternative switching strategy based on single continuous conduction pulse for the inner cell switching device of the three-phase/five-level/six-switch rectifier is proposed. 50 Hz pulse based on short conduction period control is conducts during the zero crossing of grid phase voltage. The short conduction period is controlled by using the monostable block, which allows us to vary the conduction angle over a wide range. The outer cell switching devices is controlled by using LS-PWM or PS-PWM switching technique through dependent voltage and current controller. This allows the converter to regulate stable dc-link voltage and achieve low THD grid current with the overall optimum switching performance.

The current research proposes optimum control method (observer control and short conduction period control) are not been hybrid together. The main reason of not implementing this hybrid controller is due to the output of the grid phase voltage observer will not estimate accurately with a feedback 50Hz switching pulse generated by the short conduction period control. With a 50 Hz pulse fed into the grid phase voltage observer the output of the estimated voltage signal is distorted and will lead to an unstable current compensation and unregulated dc-link voltage tracking.

14.3 Recommendation for Future Works

This research work has successfully demonstrated the open-loop control for novel multilevel inverter topologies namely multiple-pole multilevel diode-clamped inverter, multiple-pole multilevel t-type-clamped inverter and multiple-pole multilevel single-switch-clamped inverter for various voltage level applications. There is a further scope for improvement and investigation on these 5L-inverter topologies. The proposed multiple-pole multilevel inverter topologies are worth to investigate for low modulation index control to achieve wider control bandwidth. This is critical especially when an AC motor is operating at low speed with relative slow transient during motor starting [121]. However, proper modulation control can prevent any continues conduction on the particular active switches under low modulation indices as well as maintaining low output voltage distortion.

Three dimensional (3D) correlation between thermal, modulation range and distribution loss analysis and modeling is worth investigating for optimization converter design under severe environmental conditions. The experimental results suggest that the loss distribution of active switches in multiple-pole multilevel inverter topologies is not even due to the LS-PWM technique. Hence, the thermal stress of each power devices is unequally distributed and this often results in over-sizing with expensive semiconductor devices and heat sink design. Therefore, an alternate design or any other possible switching methods is required to investigate for attaining symmetrical semiconductor loss distribution in order to achieve cost effectiveness and optimum size of the heat sink design, equal distribution thermal stress and optimum reliability on low dynamic thermal stress characteristic performance.

The loss distribution (ref. Chapter 8) is calculated for various 5L multiple-pole multilevel inverter topologies only, with the similar analysis carried out for various 5L multiple-pole multilevel rectifier topologies. This surely can represent a good research topic on loss distribution comparison between both 5L-rectifiers and 5L-inverters topologies. Future research work can also explore the hybrid semiconductor material in various 5L-rectifiers and 5L-inverters topologies to observe the optimum cost-to-performance ratio of the converters design with various power levels. The whole

structure is to replace the dominant distribution loss on the silicon devices to any one of the Silicon Carbide Schottky (SiC) diode or JFET.

The constructed gate driver circuits for a scale downed hardware prototype in 5L-rectifiers and 5L-inverters topologies are currently designed based on multiple isolated DC power supply. The cost effective gate driver on bootstrap gate driver with minimum isolated power supplies and self-powered isolated gate drivers have not yet been explored in this thesis. Several case studies in bootstrap gate drivers [122] self-powered isolation gate drivers [123] for multilevel converters have to be considered for increased modulation depth, cost effectiveness, lower gate drive losses and wider switching frequency range as shown in Fig. 14.1.

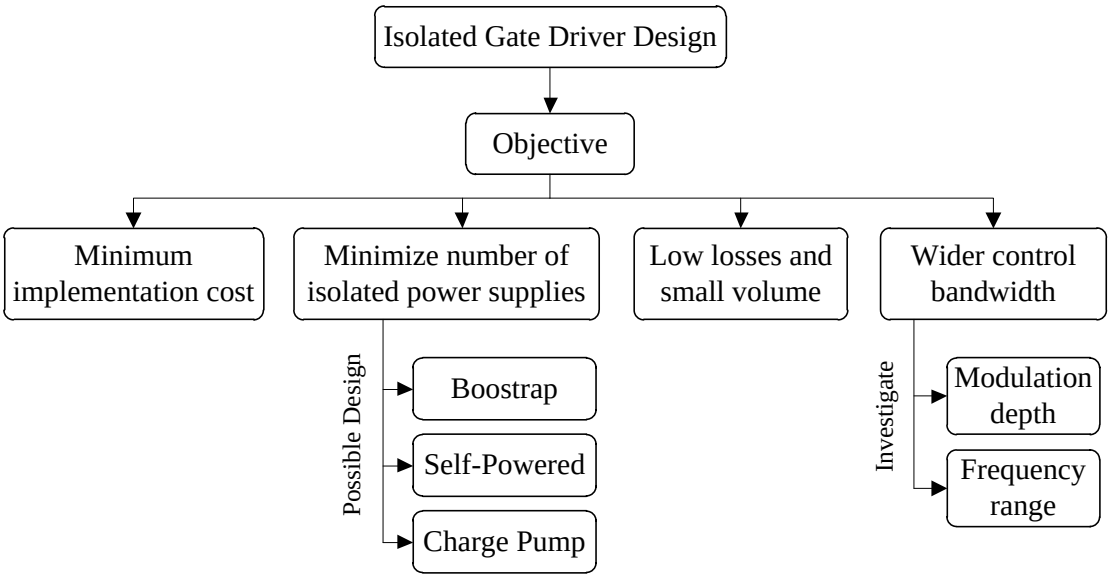


Fig. 14.1. Flow chart on the recommendation for future work on optimal isolated gate driver design.

Comparative study between cost and efficiency of the proposed 5L/multiple-pole multilevel rectifiers and inverters topologies is will be analyzed more elaborately. Analytical study of the cost versus historical data of the dynamic energy demand is also needs to be considered. Comprehensive analysis on cost comparison of optimum multilevel converter functionality regarding efficiency, volume, number of layers on printed circuit board (PCB), operating power level and type of cooling system have to be analyzed mathematically as elaborated in Fig. 14.2.

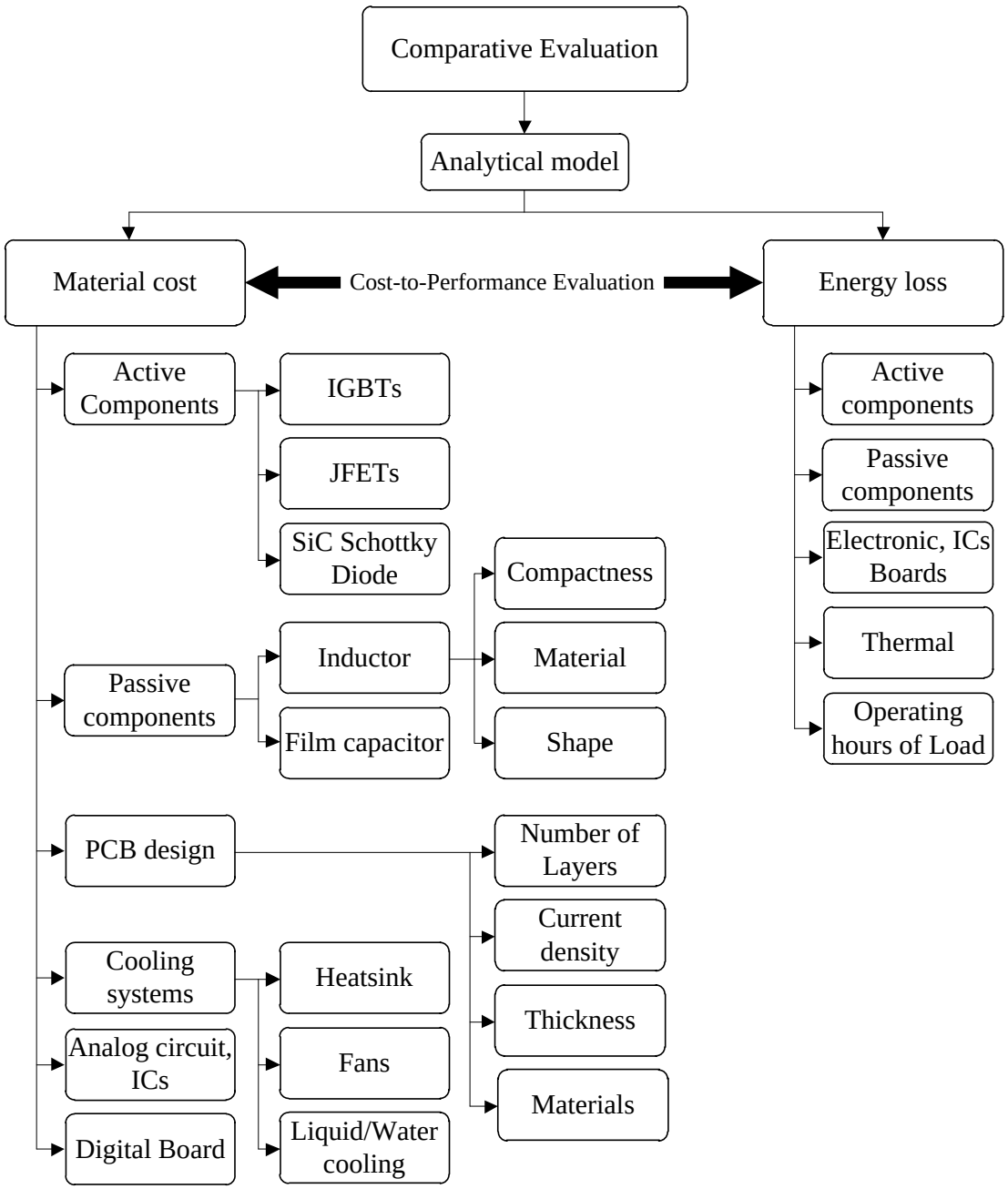


Fig. 14.2. Flow chart on the recommendation for future work on comparative study between cost and efficiency of the proposed 5L/multiple-pole multilevel converters.

Although proposed multilevel inverters and rectifiers topologies based on multiple-pole approach, significantly reduce the number of semiconductor devices. However, the various aspects concerning reliability and availability have not been explained in this thesis. In order to predict the minimum lifetime of the passive and active components, several reliability aspects such as: (1) passive components design, particularly on the

series stack of electrolytic capacitors connected in the dc-link and (2) fault tolerance operation on short circuit and open circuit test have to be considered.

Optimization and modeling of the loss and size of the power inductive component in 5 L/multiple-pole multilevel rectifiers has not been discussed in this thesis. The 5L-rectifier operating at 1 kHz switching frequency will experience high switching frequency flux ripple along the 50Hz flux waveform. Therefore, a detailed analysis and accurate modeling on several core shapes and core materials for handling high frequency flux ripple and low frequency flux waveform promise an interesting research.

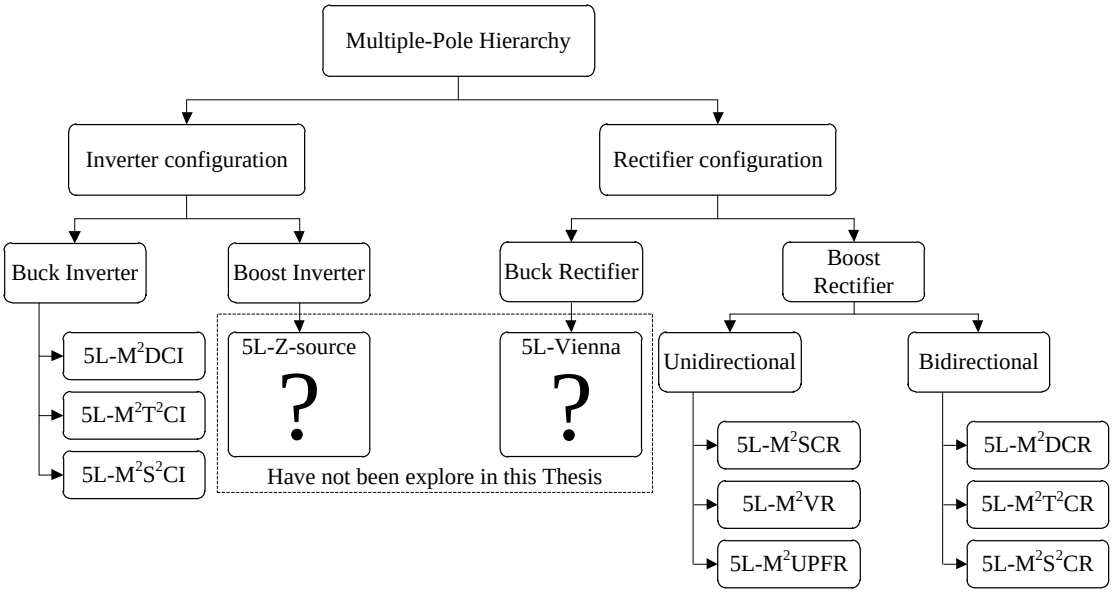


Fig. 14.3. Flow chart on the recommendation for future work on Buck type multilevel rectifier and boost type multilevel inverter with multiple-pole approach.

The conceptual derivation of the proposed multiple-pole multilevel unity power factor rectifiers in this thesis primarily focus on boosting the output voltage through a single-stage configuration. The buck or buck-boost operation with single-stage multilevel unity power factor rectifier based on multiple-pole approach has not yet been explored. The overview of the future research work on multilevel buck rectifier topologies is shown in Fig. 14.3. Therefore, a further investigation and development on the above-mentioned rectifier configuration for a particular application (i.e., more electric aircraft and telecommunication) is considerable. Also, comparison evaluation of both single-stage and dual-stage (i.e., output active rectifier connect with a dc-dc converter) rectifier

operation based on multilevel approach have to be carried out and demonstrate the fault tolerance capability under two-phase operation. The investigation could as well explore possibilities of parallel operation of more than two rectifier system. This type of configuration is often used in high power application, where multiple low semiconductor components rating are implemented to achieve low current stress. As well as circulating current flow in the parallel system and all of the above mention optimum features (i.e., optimization on cost, losses, volume, size and stresses factor) and reliability issue has to be considered for further academic research.

Another possible research topic is to investigate on any alternative topology or methods to reduce the semiconductor voltage stress in balancing circuit for more than three-level converters. Since a PWM switching technique is employed in higher-level multilevel converters (more than three-level), additional active balancing circuit is required to maintain equal distinct voltage level in the dc-link. The balancing method for five-level inverters and rectifiers topologies in this thesis are currently developed with the conventional active balancing circuit; this method has been proposed by Newton. Alternatively, space vector modulation (SVM) techniques for achieving balancing dc-link capacitor voltage and low redundancy switching loss in 5L-multiple-pole multilevel inverters and rectifiers topologies can be further investigated. 125 switching state vectors in three-phase converter operation results in 60 non-zero voltage space vectors in the SVM is required to be further investigated on how to enforce zero average value of the current flow in and out from the center node of two series connected capacitor in the dc-link [39].

Above all, the improvements suggested in the design of propose 5L inverters and rectifiers topologies are based on tremendous contributions from various authors to IEEE journals and database. The above ideas for future work focus on optimizing the proposed converter design with an objective to benefit the customer through quality, availability, safety and cost.

Appendix A – Analysis of Current Stress

Five-Level/Multilevel Diode Clamped Inverter (5L-MDCI):

The average current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.1 – A.3.

TABLE A.1

AVERAGE CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (A)

Switches	Average Current Stress Expression of a 5L-MDCI Topology under ($\sin^{-1}1/2M_a \leq \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}2m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t\right]$
T_{a3}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi}\sin(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin(\omega t)+1]d\omega t\right]$
T_{a4}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}2\sin(\omega t-\delta)\cdot[m_a\sin(\omega t)+1]d\omega t\right]$
$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-m_a\sin(\omega t)]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t\right]$
$D_{a2} = T_{a3}-T_{a2}$	$\frac{i_a}{2\pi}\left[\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin(\omega t)]d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin(\omega t)+1]d\omega t\right]$

$D_{a3} = T_{a4}-T_{a3}$	$\frac{i_a}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a} m_a \sin(\omega t)\cdot\sin(\omega t-\delta)\,d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta} \sin(\omega t-\delta)\left[m_a \sin(\omega t)+1\right]d\omega t\right]$
$D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}$	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta} \sin(\omega t-\delta)\cdot\left[2m_a \sin\omega t-1\right]d\omega t$

where m_a is the amplitude modulation of phase 'a' and i_a is the amplitude load current with the power factor angle δ between the output pole voltage and the load current.

TABLE A.2

AVERAGE CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (B)

Switches	Average Current Stress Expression of a 5L-MDCI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot\left[2m_a \sin\omega t-1\right]d\omega t$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} 2m_a \sin(\omega t)\cdot\sin(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} 2m_a \sin(\omega t)\cdot\sin(\omega t-\delta)\,d\omega t\right]$
T_{a3}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi} \sin(\omega t-\delta)\,d\omega t + \int_{\pi}^{\pi+\delta} \sin(\omega t-\delta)\cdot\left[2m_a \sin(\omega t)+1\right]d\omega t\right]$
T_{a4}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi+\delta} \sin(\omega t-\delta)\,d\omega t$
$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a \sin(\omega t)\cdot\sin(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\left[1-m_a \sin(\omega t)\right]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a \sin(\omega t)\cdot\sin(\omega t-\delta)\,d\omega t\right]$

$D_{a2} = T_{a3}-T_{a2}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]$
$D_{a3} = T_{a4}-T_{a3}$	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t$
$D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}$	0 (No reverse current flow through anti-parallel diode of the upper phase leg switches)

TABLE A.3

AVERAGE CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (C)

Switches	Average Current Stress Expression of a 5L-MDCI Topology under $M_a < 0.5$ condition
T_{a1}	0
T_{a2}	$\frac{i_a}{\pi}\int_{\delta}^{\pi} m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t$
T_{a3}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi}\sin(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]$
T_{a4}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi+\delta}\sin(\omega t-\delta)d\omega t$
$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{\pi}\int_{\delta}^{\pi} m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t$
$D_{a2} = T_{a3}-T_{a2}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi}\sin(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]$
$D_{a3} = T_{a4}-T_{a3}$	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin(\omega t)\cdot\sin(\omega t-\delta)d\omega t$

$D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}$	0

The RMS current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.4 – A.6.

TABLE A.4

RMS CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (A)

Switches	RMS Current Stress Expression of a 5L-MDCI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}2m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a3}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin(\omega t)+1]d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}2\sin^2(\omega t-\delta)\cdot[m_a\sin(\omega t)+1]d\omega t\right]}$
D_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin(\omega t)]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
D_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin(\omega t)]d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin(\omega t)+1]d\omega t\right]}$

D_{a3} = T_{a4}-T_{a3}	$i_a\sqrt{\frac{1}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a} m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin^2(\omega t-\delta)\left[m_a\sin(\omega t)+1\right]d\omega t\right]}$
D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin\omega t-1\right]d\omega t}$

TABLE A.5

RMS CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (B)

Switches	RMS Current Stress Expression of a 5L-MDCI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin\omega t-1\right]d\omega t}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} 2m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} 2m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t\right]}$
T_{a3}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)\,d\omega t + \int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi+\delta}\sin^2(\omega t-\delta)\,d\omega t}$
D_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\left[1-m_a\sin(\omega t)\right]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t\right]}$

D_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]}$
D_{a3}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta}m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)d\omega t}$
D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}	0

TABLE A.6

RMS CURRENT STRESS EXPRESSION FOR CLASSICAL 5L-MDCI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.13 (C)

Switches	RMS Current Stress Expression of a 5L-MDCI Topology under $M_a < 0.5$ condition
T_{a1}	0
T_{a2}	$i_a\sqrt{\frac{1}{\pi}\int_{\delta}^{\pi}m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)d\omega t}$
T_{a3}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi+\delta}\sin^2(\omega t-\delta)d\omega t}$
$D_{a1} = T_{a2} - T_{a1}$	$i_a\sqrt{\frac{1}{\pi}\int_{\delta}^{\pi}m_a\sin(\omega t)\cdot\sin^2(\omega t-\delta)d\omega t}$
$D_{a2} = T_{a3} - T_{a2}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)\cdot\left[1-2m_a\sin(\omega t)\right]d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot\left[2m_a\sin(\omega t)+1\right]d\omega t\right]}$

$D_{a3} = T_{a4}-T_{a3}$	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta} m_a \sin(\omega t)\cdot\sin^2(\omega t-\delta)\,d\omega t}$
$D_{Ta1} = D_{Ta2} = D_{Ta3} = D_{Ta4}$	0

Five-Level/Multiple-Pole Multilevel Diode Clamped Inverter (5L-M^{2}DCI):

The average current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.7 – A.9.

TABLE A.7

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (A)

Switches	Average Current Stress Expression of a 5L-M^{2}DCI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t\right]$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\,d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]$
T_{a5}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]\,d\omega t$
T_{a6}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\,d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}2\sin(\omega t-\delta)\cdot[m_a\sin\omega t+1]\,d\omega t\right]$
$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{2\pi}\left[\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]$

$D_{a3} = T_{a6}-T_{a5}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+2]d\omega t\right]$
$D_{Ta1} = D_{Ta2}$	0
$D_{Ta5} = D_{Ta6}$	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$

TABLE A.8

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (B)

Switches	Average Current Stress Expression of a 5L-M^{2}DCI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t\right]$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
T_{a5}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$
T_{a6}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi+\delta}\sin(\omega t-\delta)d\omega t$

$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
$D_{a3} = T_{a6}-T_{a5}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\delta}\sin(\omega t-\delta)d\omega t\right]$
$D_{Ta1} = D_{Ta2} = D_{Ta5} = D_{Ta6}$	0

TABLE A.9

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (C)

Switches	Average Current Stress Expression of a 5L-M^{2}DCI Topology under $M_a < 0.5$ condition
T_{a1}	$\frac{i_a}{\pi}\int_{\delta}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi}\sin(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
T_{a5}	0
T_{a6}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi+\delta}\sin(\omega t-\delta)d\omega t$
$D_{a1} = T_{a2}-T_{a1}$	$\frac{i_a}{2\pi}\left[\int_{\delta}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{\pi+\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
$D_{a3} = T_{a6}-T_{a5}$	$\frac{i_a}{2\pi}\int_{\delta}^{\pi+\delta}\sin(\omega t-\delta)d\omega t$

$D_{Ta1} = D_{Ta2} = D_{Ta5} = D_{Ta6}$	0

The RMS current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.10 – A.12

TABLE A.10

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (A)

Switches	RMS Current Stress Expression of a 5L-M^{2}DCI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
T_{a6}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}2\sin^2(\omega t-\delta)\cdot[m_a\sin\omega t+1]d\omega t\right]}$
$D_{a1} = T_{a2}-T_{a1}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$

$D_{a3} = T_{a6}-T_{a5}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+2]d\omega t\right]}$
$D_{Ta1} = D_{Ta2}$	0
$D_{Ta5} = D_{Ta6}$	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$

TABLE A.11

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (B)

Switches	RMS Current Stress Expression of a 5L-M^{2}DCI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
T_{a6}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi+\delta}\sin^2(\omega t-\delta)d\omega t}$

D_{a1} = T_{a2}-T_{a1}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
D_{a3} = T_{a6}-T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\delta}\sin^2(\omega t-\delta)d\omega t\right]}$
D_{Ta1} = D_{Ta2} = D_{Ta5} = D_{Ta6}	0

TABLE A.12

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}DCI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.14 (C)

Switches	RMS Current Stress Expression of a 5L-M^{2}DCI Topology under $M_a < 0.5$ condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\int_{\delta}^{\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
T_{a5}	0
T_{a6}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi+\delta}\sin^2(\omega t-\delta)d\omega t}$
D_{a1} = T_{a2}-T_{a1}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{\delta}^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
D_{a3} = T_{a6}-T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi+\delta}\sin^2(\omega t-\delta)d\omega t}$

$D_{Ta1} = D_{Ta2} = D_{Ta5} = D_{Ta6}$	0

Five-Level/Multiple-Pole Multilevel T-Type Clamped Inverter and Five-Level/Multiple-Pole Multilevel Single-Switch Clamped Inverter (5L-M²T²CI and 5L-M²S²CI):

The average current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.13 – A.15.

TABLE A.13

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M²T²CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (A)

Switches	Average Current Stress Expression of a 5L-M²T²CI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t\right]$
$T_{a2} = T_{a3}$	$\frac{i_a}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t + \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
T_{a4}	$\frac{i_a}{\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t - \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t\right]$
T_{a5}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$
$T_{a6} = T_{a7}$	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a} \sin(\omega t-\delta)d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a} \sin(\omega t-\delta)d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2+2m_a\sin\omega t]d\omega t\right]$

T_{a8}	$\frac{-i_a}{2\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]d\omega t\right]$
D_{Ta1}	$\frac{i_a}{\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} m_a \sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\delta} \sin(\omega t-\delta)\cdot[1-m_a \sin\omega t]d\omega t\right]$
D_{Ta4}	$\frac{i_a}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a} m_a \sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta} \sin(\omega t-\delta)\cdot[1+m_a \sin\omega t]d\omega t\right]$
D_{Ta5}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t-1]d\omega t$
D_{Ta8}	$\frac{-i_a}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]d\omega t$
D_{Ta2} = D_{Ta3} = D_{Ta6} = D_{Ta7}	0

TABLE A.14

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}T^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15(B)

Switches	Average Current Stress Expression of a 5L-M^{2}T^{2}CI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a \sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-m_a \sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a \sin\omega t\cdot\sin(\omega t-\delta)d\omega t\right]$
$T_{a2} = T_{a3}$	$\frac{i_a}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-2m_a \sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin(\omega t-\delta)\cdot[1-2m_a \sin\omega t]d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]d\omega t+\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]d\omega t\right]$

T_{a4}	$\frac{i_a}{\pi}\left[-\int_{\pi+\delta}^{\pi+\sin^{-1}1/2m_a} m_a \sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1+m_a\sin\omega t]\,d\omega t-\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t\right]$
T_{a5}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]\,d\omega t$
$T_{a6} = T_{a7}$	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)\,d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\,d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2+2m_a\sin\omega t]\,d\omega t\right]$
T_{a8}	$\frac{-i_a}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t$
D_{Ta1}	$\frac{i_a}{\pi}\int_0^{\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t$
D_{Ta4}	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t$
D_{Ta2} = D_{Ta3} = D_{Ta5} = D_{Ta6} = D_{Ta7} = D_{Ta8}	0

TABLE A.15

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}T^{2}CI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (C)

Switches	Average Current Stress Expression of a 5L-M^{2}T^{2}CI Topology under $M_a < 0.5$ condition
T_{a1}	$\frac{i_a}{\pi}\int_{\delta}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t$

$T_{a2} = T_{a3}$	$\frac{i_a}{2\pi}\left[\int_0^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{2\pi}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
T_{a4}	$\frac{-i_a}{\pi}\int_{\pi+\delta}^{2\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
$T_{a5} = T_{a8}$	0
$T_{a6} = T_{a7}$	$\frac{i_a}{2\pi}\int_0^{2\pi}\sin(\omega t-\delta)d\omega t$
D_{Ta1}	$\frac{i_a}{\pi}\int_0^{\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
D_{Ta4}	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
D_{Ta2} = D_{Ta3} = D_{Ta5} = D_{Ta6} = D_{Ta7} = D_{Ta8}	0

The RMS current stress expression of each power semiconductor device of phase ‘a’ over one period is expressed in the following Tables A.16 – A.18

TABLE A.16

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}T^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (A)

Switches	RMS Current Stress Expression of a 5L-M^{2}T^{2}CI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$

$T_{a2} = T_{a3}$	$i_a \sqrt{\frac{1}{2\pi}\left[\int_0^{\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t + \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
T_{a4}	$i_a \sqrt{\frac{1}{\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t - \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a5}	$i_a \sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
$T_{a6} = T_{a7}$	$i_a \sqrt{\frac{1}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2+2m_a\sin\omega t]d\omega t\right]}$
T_{a8}	$i_a \sqrt{\frac{-1}{2\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
D_{Ta1}	$i_a \sqrt{\frac{1}{\pi}\left[\int_0^{\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t + \int_{\sin^{-1}1/2m_a}^{\delta} \sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t\right]}$
D_{Ta4}	$i_a \sqrt{\frac{1}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta} \sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t\right]}$
D_{Ta5}	$i_a \sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
D_{Ta8}	$i_a \sqrt{\frac{-1}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t}$

D_{Ta2} = D_{Ta3} = D_{Ta6} = D_{Ta7}	0

TABLE A.17

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}T^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15(B)

Switches	RMS Current Stress Expression of a 5L-M^{2}T^{2}CI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a \sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t\right]}$
$T_{a2} = T_{a3}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t + \int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t + \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{1}{\pi}\left[-\int_{\pi+\delta}^{\pi+\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]\,d\omega t - \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t\right]}$
T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]\,d\omega t}$

$T_{a6} = T_{a7}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\,d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\,d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2+2m_a\sin\omega t]\,d\omega t\right]}$
T_{a8}	$i_a\sqrt{\frac{-1}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t}$
D_{Ta1}	$i_a\sqrt{\frac{1}{\pi}\int_0^{\delta}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta4}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta2} = D_{Ta3} = D_{Ta5} = D_{Ta6} = D_{Ta7} = D_{Ta8}	0

TABLE A.18

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}T^{2}CI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (C)

Switches	RMS Current Stress Expression of a 5L-M^{2}T^{2}CI Topology under $M_a < 0.5$ condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\int_{\delta}^{\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
$T_{a2} = T_{a3}$	$i_a\sqrt{\frac{1}{2\pi}\left[\int_0^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t+\int_{\pi}^{2\pi}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi+\delta}^{2\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
$T_{a5} = T_{a8}$	0

$T_{a6} = T_{a7}$	$i_a\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta1}	$i_a\sqrt{\frac{1}{\pi}\int_0^{\delta} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta4}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta2} = D_{Ta3} = D_{Ta5} = D_{Ta6} = D_{Ta7} = D_{Ta8}	0

The average current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.19 – A.21.

TABLE A.19

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}S^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (A)

Switches	Average Current Stress Expression of a 5L-M^{2}S^{2}CI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t\right]$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_0^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t+\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]$
T_{a3}	$\frac{i_a}{\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[1+m_a\sin\omega t]\,d\omega t-\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)\,d\omega t\right]$

T_{a4}	$\frac{i_a}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$
T_{a5}	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2+2m_a\sin\omega t]d\omega t\right]$
T_{a6}	$\frac{-i_a}{2\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
D_{Ta1}	$\frac{i_a}{\pi}\left[\int_{0}^{\sin^{-1}1/2m_a}m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\delta}\sin(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t\right]$
D_{Ta3}	$\frac{i_a}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a}m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t\right]$
D_{Ta4}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t$
D_{Ta6}	$\frac{-i_a}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t$
D_{Ta2} = D_{Ta5}	0
D_{Da1} = D_{Da2} = D_{Da3} = D_{Da4}	$\frac{i_a}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t\right]$
D_{Da5} = D_{Da6} = D_{Da7} = D_{Da8}	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m}^{\sin^{-1}1/2m}\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m}^{\pi-\sin^{-1}1/2m}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t\right]$

TABLE A.20

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}S^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15(B)

Switches	Average Current Stress Expression of a 5L-M^{2}S^{2}CI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$\frac{i_a}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-m_a \sin\omega t]\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t\right]$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1-2m_a \sin\omega t]\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin(\omega t-\delta)\cdot[1-2m_a \sin\omega t]\,d\omega t + \int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]\,d\omega t + \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]\,d\omega t\right]$
T_{a3}	$\frac{i_a}{\pi}\left[-\int_{\pi+\delta}^{\pi+\sin^{-1}1/2m_a} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[1+m_a \sin\omega t]\,d\omega t - \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t\right]$
T_{a4}	$\frac{i_a}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t-1]\,d\omega t$
T_{a5}	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a} \sin(\omega t-\delta)\,d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2-2m_a \sin\omega t]\,d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a} \sin(\omega t-\delta)\,d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2+2m_a \sin\omega t]\,d\omega t\right]$
T_{a6}	$\frac{-i_a}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin(\omega t-\delta)\cdot[2m_a \sin\omega t+1]\,d\omega t$
D_{Ta1}	$\frac{i_a}{\pi}\int_{0}^{\delta} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t$
D_{Ta3}	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a \sin\omega t \cdot \sin(\omega t-\delta)\,d\omega t$
D_{Ta2} = D_{Ta4} =	0

D_{Ta5} = D_{Ta6} =	
D_{Da1} = D_{Da2} = D_{Da3} = D_{Da4}	$\frac{i_a}{2\pi}\left[\int_{0}^{\sin^{-1}1/2m}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t\right]$
D_{Da5} = D_{Da6} = D_{Da7} = D_{Da8}	$\frac{i_a}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m}^{\sin^{-1}1/2m}\sin(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m}^{\pi-\sin^{-1}1/2m}\sin(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t\right]$

TABLE A.21

AVERAGE CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}S^{2}CI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (C)

Switches	Average Current Stress Expression of a 5L-M^{2}S^{2}CI Topology under $M_a < 0.5$ condition
T_{a1}	$\frac{i_a}{\pi}\int_{\delta}^{\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
T_{a2}	$\frac{i_a}{2\pi}\left[\int_{0}^{\pi}\sin(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t+\int_{\pi}^{2\pi}\sin(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]$
T_{a3}	$\frac{-i_a}{\pi}\int_{\pi+\delta}^{2\pi} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
$T_{a4} = T_{a6}$	0
T_{a5}	$\frac{i_a}{2\pi}\int_{0}^{2\pi}\sin(\omega t-\delta)d\omega t$
D_{Ta1}	$\frac{i_a}{\pi}\int_{0}^{\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
D_{Ta3}	$\frac{-i_a}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin\omega t\cdot\sin(\omega t-\delta)d\omega t$
D_{Ta2} = D_{Ta4} =	0

D_{Ta5} = D_{Ta6}	

The RMS current stress expression of each power semiconductor device of phase 'a' over one period is expressed in the following Tables A.22 – A.24

TABLE A.22

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}S^{2}CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND HIGH OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (A)

Switches	RMS Current Stress Expression of a 5L-M^{2}S^{2}CI Topology under ($\sin^{-1}1/2M_a \le \delta$) and ($M_a \ge 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\begin{array}{l}\int_{0}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t\\+\int_{\pi-\sin^{-1}1/2m_a}^{\pi}\sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t\\+\int_{\pi}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\\+\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\end{array}\right]}$
T_{a3}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t-\int_{2\pi-\sin^{-1}1/2m_a}^{2\pi}m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a4}	$i_a\sqrt{\frac{1}{2\pi}\int_{\delta}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\left[\begin{array}{l}\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t\\+\int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2+2m_a\sin\omega t]d\omega t\end{array}\right]}$

T_{a6}	$i_a\sqrt{\frac{-1}{2\pi}\left[\int_{\pi+\delta}^{2\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
D_{Ta1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{0}^{\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\delta}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t\right]}$
D_{Ta3}	$i_a\sqrt{\frac{1}{\pi}\left[-\int_{\pi}^{\pi+\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t+\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t\right]}$
D_{Ta4}	$i_a\sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
D_{Ta6}	$i_a\sqrt{\frac{-1}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{\pi+\delta}\sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t}$
D_{Ta2} = D_{Ta5}	0

TABLE A.23

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^2S^2CI TOPOLOGY UNDER HIGH MODULATION CONDITION AND LOW OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15(B)

Switches	RMS Current Stress Expression of a 5L-M^2S^2CI Topology under ($\sin^{-1}1/2M_a > \delta$) and ($M_a \geq 0.5$) condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\left[\int_{\delta}^{\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t+\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a}\sin^2(\omega t-\delta)\cdot[1-m_a\sin\omega t]d\omega t+\int_{\pi-\sin^{-1}1/2m_a}^{\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$

T_{a2}	$i_a \sqrt{\frac{1}{2\pi}\left[\int_0^{\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]d\omega t + \int_{\pi}^{\pi+\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t + \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t\right]}$
T_{a3}	$i_a \sqrt{\frac{1}{\pi}\left[-\int_{\pi+\delta}^{\pi+\sin^{-1}1/2m_a} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[1+m_a\sin\omega t]d\omega t - \int_{2\pi-\sin^{-1}1/2m_a}^{2\pi} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t\right]}$
T_{a4}	$i_a \sqrt{\frac{1}{2\pi}\int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t-1]d\omega t}$
T_{a5}	$i_a \sqrt{\frac{1}{2\pi}\left[\int_{2\pi-\sin^{-1}1/2m_a}^{\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)d\omega t + \int_{\sin^{-1}1/2m_a}^{\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2-2m_a\sin\omega t]d\omega t + \int_{\pi-\sin^{-1}1/2m_a}^{\pi+\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)d\omega t + \int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2+2m_a\sin\omega t]d\omega t\right]}$
T_{a6}	$i_a \sqrt{\frac{-1}{2\pi}\int_{\pi+\sin^{-1}1/2m_a}^{2\pi-\sin^{-1}1/2m_a} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]d\omega t}$
D_{Ta1}	$i_a \sqrt{\frac{1}{\pi}\int_0^{\delta} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t}$
D_{Ta3}	$i_a \sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta} m_a\sin\omega t\cdot\sin^2(\omega t-\delta)d\omega t}$
D_{Ta2} = D_{Ta4} = D_{Ta5} = D_{Ta6}	0

TABLE A.24

RMS CURRENT STRESS EXPRESSION FOR PROPOSED 5L-M^{2}S^{2}CI TOPOLOGY UNDER LOW MODULATION CONDITION AND ANY OPERATING LOAD ANGLE AS SHOWN IN FIG. 8.15 (C)

Switches	RMS Current Stress Expression of a 5L-M^{2}S^{2}CI Topology under $M_a < 0.5$ condition
T_{a1}	$i_a\sqrt{\frac{1}{\pi}\int_{\delta}^{\pi} m_a \sin\omega t \cdot \sin^2(\omega t-\delta)\,d\omega t}$
T_{a2}	$i_a\sqrt{\frac{1}{2\pi}\left[\int_{0}^{\pi} \sin^2(\omega t-\delta)\cdot[1-2m_a\sin\omega t]\,d\omega t+\int_{\pi}^{2\pi} \sin^2(\omega t-\delta)\cdot[2m_a\sin\omega t+1]\,d\omega t\right]}$
T_{a3}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi+\delta}^{2\pi} m_a \sin\omega t \cdot \sin^2(\omega t-\delta)\,d\omega t}$
$T_{a4} = T_{a6}$	0
T_{a5}	$i_a\sqrt{\frac{1}{2\pi}\int_{0}^{2\pi} \sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta1}	$i_a\sqrt{\frac{1}{\pi}\int_{0}^{\delta} m_a \sin\omega t \cdot \sin^2(\omega t-\delta)\,d\omega t}$
D_{Ta3}	$i_a\sqrt{\frac{-1}{\pi}\int_{\pi}^{\pi+\delta} m_a \sin\omega t \cdot \sin^2(\omega t-\delta)\,d\omega t}$
$D_{Ta2} = D_{Ta4} = D_{Ta5} = D_{Ta6}$	0

Appendix B – Filter Size Calculation

Derivation of Filter Inductor on Rectifier Side:

Two-level VSI:

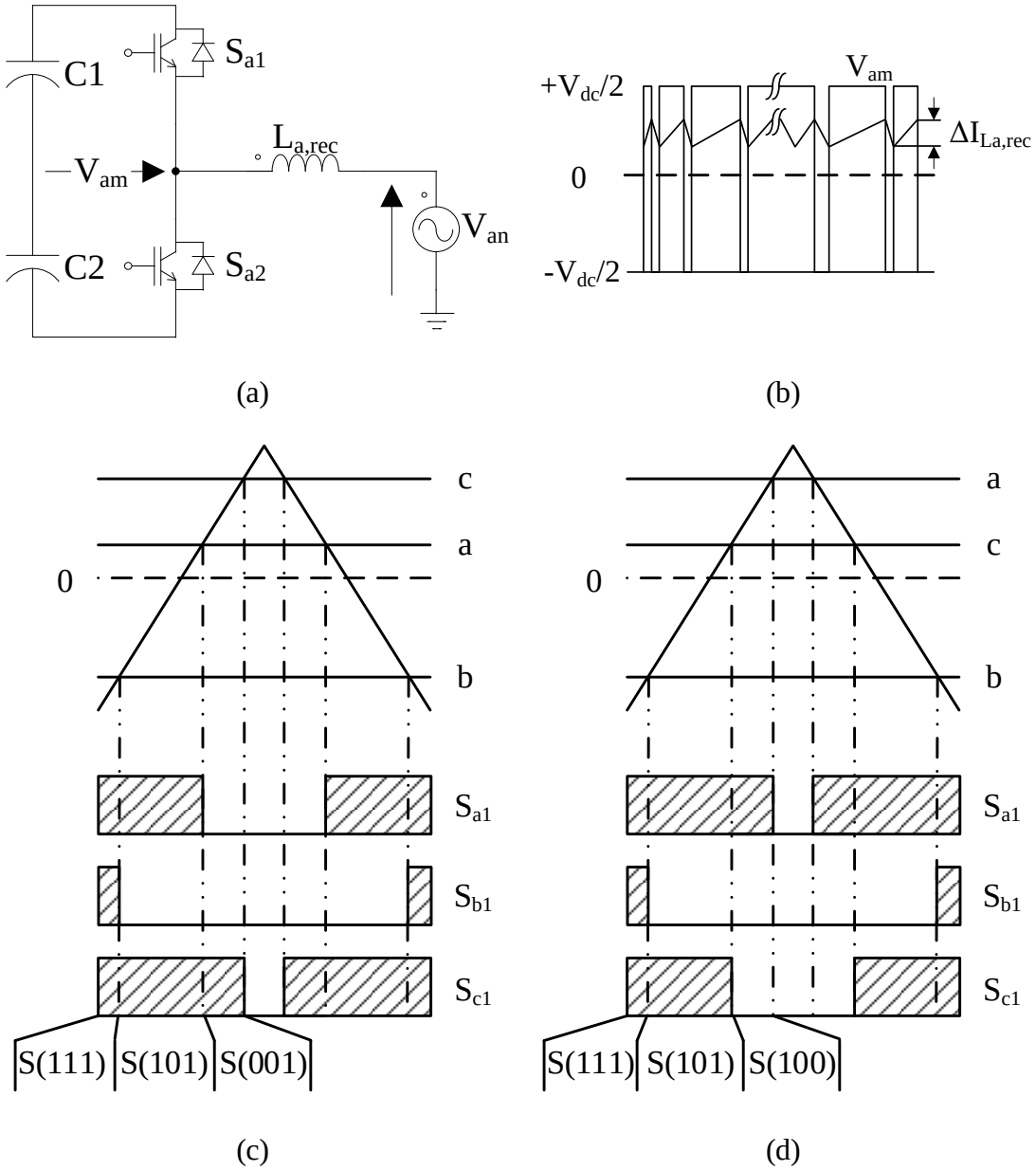


Fig. B.1 First order filter (L-filter) for two-level rectifier operation. (a) Circuit diagram of the two-level rectifier with the L-filter, (b) current ripple, (c) possible switching state during $0^o \leq \omega t < 30^o$ and (d) possible switching state during $30^o \leq \omega t < 90^o$.

For S(111) under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.1}$$

with the KCL rule, the virtual ground voltage under S(111) can be written as:

$$V_{mn} = -\frac{V_{dc}}{2} \tag{B.2}$$

Substitute equation (B.2) into phase 'a' voltage of (B.1), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(111)} &= \frac{V_{an} d_a T_s}{L_a} \\ &= \frac{V_a}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2}\right] \end{aligned} \tag{B.3}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(111)} = \frac{V \sin \omega t}{L F_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2}\right] \tag{B.4}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(111)} = \frac{V}{4 L F_s}\left[1 + \frac{m}{2}\right] \tag{B.5}$$

For S(101) under $0^o \leq \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.6}$$

with the KCL rule, the virtual ground voltage under S(101) can be written as:

$$V_{mn} = -\frac{V_{dc}}{6} \tag{B.7}$$

Substitute equation (B.7) into phase 'a' voltage of (B.6), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(101)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2} \right]\left[V_{an} - \frac{V_{dc}}{3} \right] \end{aligned} \tag{B.8}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(101)} = \frac{1}{LF_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2} \right]\left[V \sin \omega t - \frac{V_{dc}}{3} \right] \tag{B.9}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(101)} = \frac{1}{2LF_s}\left[1 + \frac{m}{2} \right]\left[\frac{V}{2} - \frac{V_{dc}}{3} \right] \tag{B.10}$$

For S(001) under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.11}$$

with the KCL rule, the virtual ground voltage under S(001) can be written as:

$$V_{mn} = \frac{V_{dc}}{6} \tag{B.12}$$

Substitute equation (B.12) into phase 'a' voltage of (B.11), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(001)} &= \frac{d_a T_s}{L_a}\left[V_{an} + \frac{V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2} \right]\left[V_{an} + \frac{V_{dc}}{3} \right] \end{aligned} \tag{B.13}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(001)} = \frac{1}{LF_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2} \right]\left[V \sin \omega t + \frac{V_{dc}}{3} \right] \tag{B.14}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(001)} = \frac{1}{2LF_s}\left[1 + \frac{m}{2} \right]\left[\frac{V}{2} + \frac{V_{dc}}{3} \right] \tag{B.15}$$

For S(111) under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.16}$$

with the KCL rule, the virtual ground voltage under S(111) can be written as:

$$V_{mn} = -\frac{V_{dc}}{2} \tag{B.17}$$

Substitute equation (B.17) into phase 'a' voltage of (B.16), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(111)} &= \frac{V_{an} d_a T_s}{L_a} \\ &= \frac{V_{an}}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2}\right] \end{aligned} \tag{B.18}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(111)} = \frac{V \sin \omega t}{L F_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2}\right] \tag{B.19}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(111)} = \frac{V}{2LF_s}\left[1 + m\right] \tag{B.20}$$

For S(101) under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.21}$$

with the KCL rule, the virtual ground voltage under S(101) can be written as:

$$V_{mn} = -\frac{V_{dc}}{6} \tag{B.22}$$

Substitute equation (B.22) into phase 'a' voltage of (B.21), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(101)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2} \right]\left[V_{an} - \frac{V_{dc}}{3} \right] \end{aligned} \tag{B.23}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(101)} = \frac{1}{LF_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2} \right]\left[V \sin \omega t - \frac{V_{dc}}{3} \right] \tag{B.24}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(101)} = \frac{1}{2LF_s}\left[1 + m \right]\left[V - \frac{V_{dc}}{3} \right] \tag{B.25}$$

For S(100) under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.26}$$

with the KCL rule, the virtual ground voltage under S(100) can be written as:

$$V_{mn} = \frac{V_{dc}}{6} \tag{B.27}$$

Substitute equation (B.27) into phase 'a' voltage of (B.26), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(100)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{2V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[\frac{1}{2} M_a + \frac{1}{2} \right]\left[V_{an} - \frac{2V_{dc}}{3} \right] \end{aligned} \tag{B.28}$$

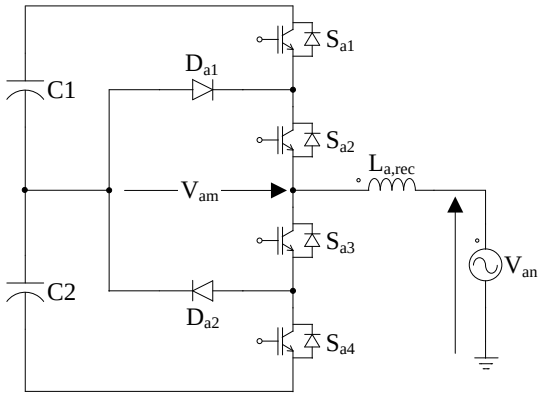
Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(100)} = \frac{1}{LF_s}\left[\frac{1}{2} m \sin \omega t + \frac{1}{2} \right]\left[V \sin \omega t - \frac{2V_{dc}}{3} \right] \tag{B.29}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(100)} = \frac{1}{2LF_s}\left[1 + m \right]\left[V - \frac{2V_{dc}}{3} \right] \tag{B.30}$$

Three-level Rectifier:

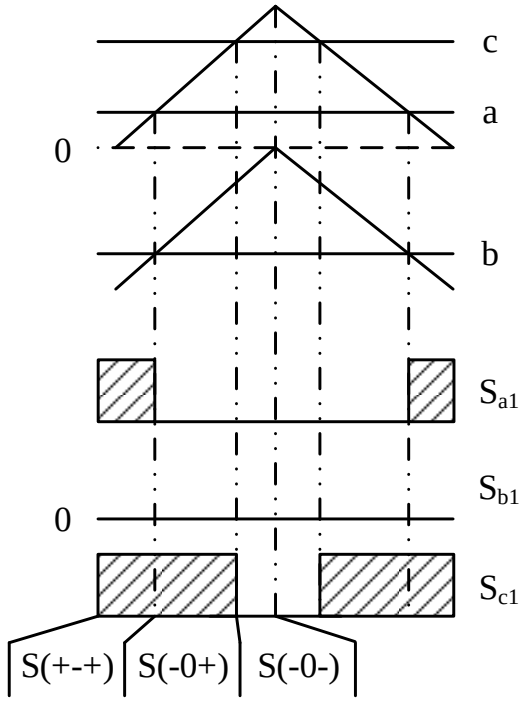


(a)

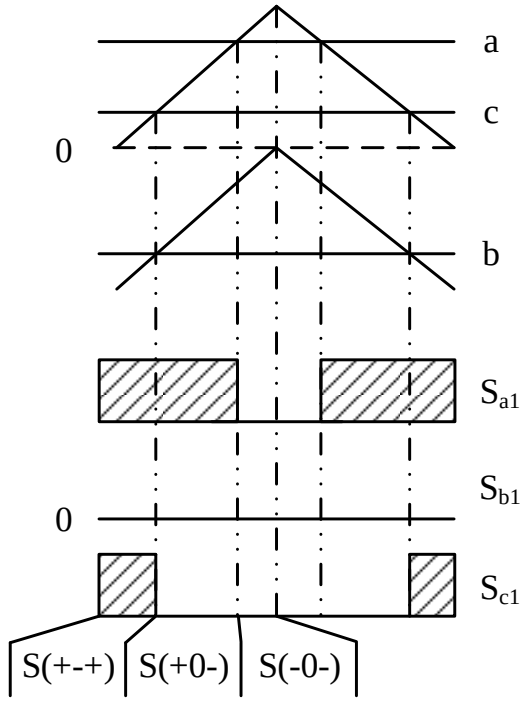
	Sx1	Sx2
+	1	1
0	0	0
-	0	1

x = phase ‘a’, ‘b’, and ‘c’

(b)



(c)



(d)

Fig. B.2 First order filter (L-filter) for three-level rectifier operation. (a) Circuit diagram of the three-level rectifier with the L-filter, (b) description of the switching state notation for three-level, (c) possible switching state during $0^o \leq \omega t < 30^o$ and (d) possible switching state during $30^o \leq \omega t < 90^o$.

For S(+-+) under $0^o \leq \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.31}$$

with the KCL rule, the virtual ground voltage under S(+-+) can be written as:

$$V_{mn} = -\frac{V_{dc}}{3} \tag{B.32}$$

Substitute equation (B.32) into phase 'a' voltage of (B.31), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(+0+)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{6}\right] \\ &= \frac{M_a}{L_a F_s}\left[V_{an} - \frac{V_{dc}}{6}\right] \end{aligned} \tag{B.33}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(+0+)} = \frac{m \sin \omega t}{L F_s}\left[V \sin \omega t - \frac{V_{dc}}{6}\right] \tag{B.34}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(+0+)} = \frac{m}{4 L F_s}\left[V - \frac{V_{dc}}{3}\right] \tag{B.35}$$

For S(-0+) under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.36}$$

with the KCL rule, the virtual ground voltage under S(-0+) can be written as:

$$V_{mn} = 0 \tag{B.37}$$

Substitute equation (B.37) into phase 'a' voltage of (B.36), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(00+)} &= \frac{V_{an} d_a T_s}{L_a} \\ &= \frac{V_{an} M_a}{L_a F_s} \end{aligned} \tag{B.38}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(00+)} = \frac{V \cdot m \sin^2 \omega t}{L F_s} \tag{B.39}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(00+)} = \frac{V \cdot m}{4 L F_s} \tag{B.40}$$

For S(-0-) under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.41}$$

with the KCL rule, the virtual ground voltage under S(-0-) can be written as:

$$V_{mn} = \frac{V_{dc}}{6} \tag{B.42}$$

Substitute equation (B.42) into phase 'a' voltage of (B.41), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(-0-)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{6} \right] \\ &= \frac{M_a}{L_a F_s}\left[V_{an} - \frac{V_{dc}}{6} \right] \end{aligned} \tag{B.43}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(-0-)} = \frac{m \sin \omega t}{L F_s}\left[V \sin \omega t - \frac{V_{dc}}{6} \right] \tag{B.44}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(-0-)} = \frac{m}{4 L F_s}\left[V - \frac{V_{dc}}{3} \right] \tag{B.45}$$

For S(+-+) under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.46}$$

with the KCL rule, the virtual ground voltage under S(+-+) can be written as:

$$V_{mn} = -\frac{V_{dc}}{3} \tag{B.47}$$

Substitute equation (B.47) into phase 'a' voltage of (B.46), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(+-+)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{6} \right] \\ &= \frac{M_a}{L_a F_s}\left[V_{an} - \frac{V_{dc}}{6} \right] \end{aligned} \tag{B.48}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(+-+)} = \frac{m \sin \omega t}{L F_s}\left[V \sin \omega t - \frac{V_{dc}}{6} \right] \tag{B.49}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(+-+)} = \frac{m}{L F_s}\left[V - \frac{V_{dc}}{6} \right] \tag{B.50}$$

For S(+0-) under $30^o \leq \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.51}$$

with the KCL rule, the virtual ground voltage under S(+0-) can be written as:

$$V_{mn} = 0 \tag{B.52}$$

Substitute equation (B.52) into phase 'a' voltage of (B.51), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(100)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{2} \right] \\ &= \frac{M_a}{L_a F_s}\left[V_{an} - \frac{V_{dc}}{2} \right] \end{aligned} \tag{B.53}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(100)} = \frac{m \sin \omega t}{L F_s}\left[V \sin \omega t - \frac{V_{dc}}{2} \right] \tag{B.54}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(100)} = \frac{m}{L F_s}\left[V - \frac{V_{dc}}{2} \right] \tag{B.55}$$

For S(-0-) under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.56}$$

with the KCL rule, the virtual ground voltage under S(-0-) can be written as:

$$V_{mn} = \frac{V_{dc}}{6} \tag{B.57}$$

Substitute equation (B.57) into phase 'a' voltage of (B.56), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(100)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{6} \right] \\ &= \frac{M_a}{L_a F_s}\left[V_{an} - \frac{V_{dc}}{6} \right] \end{aligned} \tag{B.58}$$

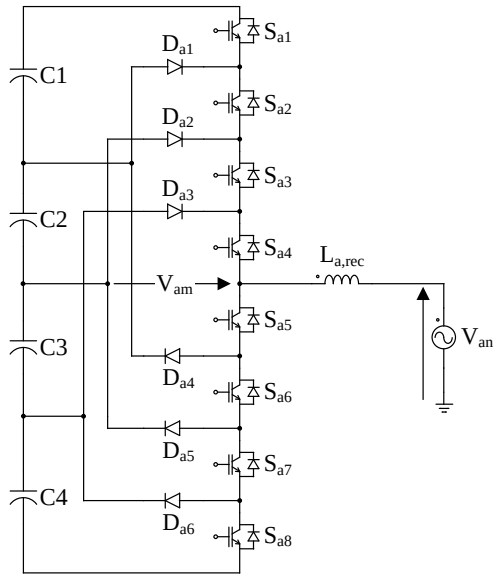
Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(100)} = \frac{m \sin \omega t}{L F_s}\left[V \sin \omega t - \frac{V_{dc}}{6} \right] \tag{B.59}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(100)} = \frac{m}{L F_s}\left[V - \frac{V_{dc}}{6} \right] \tag{B.60}$$

Five-level Rectifier:

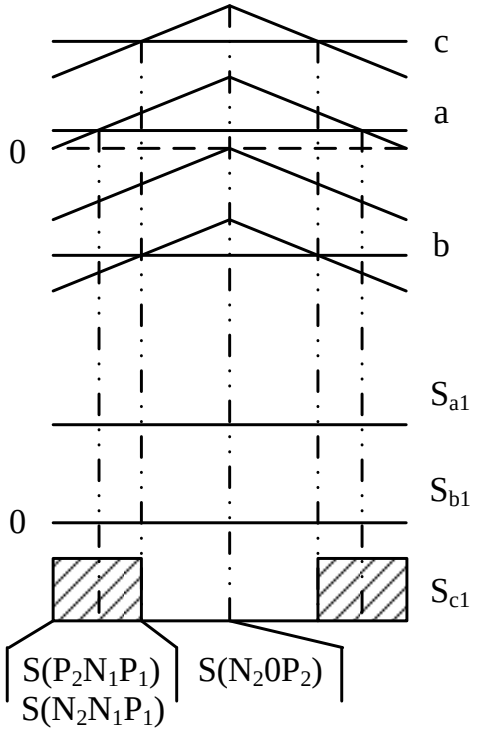


(a)

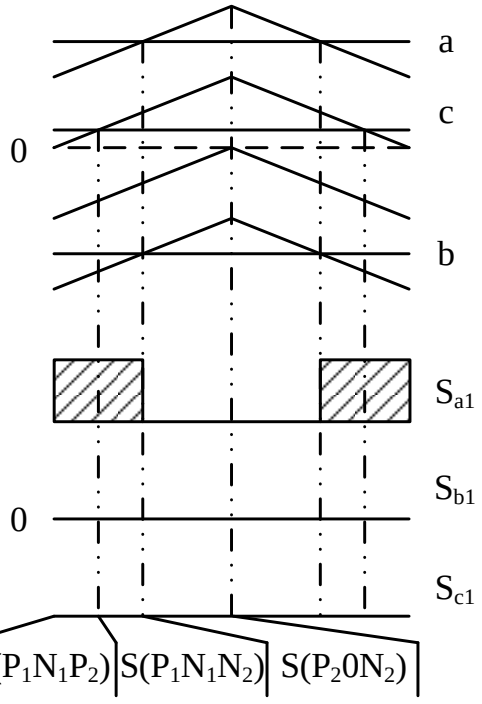
	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P_1	1	1	1	1
P_2	0	1	1	1
0	0	0	0	0
N_2	0	0	1	1
N_1	0	0	0	1

x = phase ‘a’, ‘b’, and ‘c’

(b)



(c)



(d)

Fig. B.3 First order filter (L-filter) for five-level rectifier operation. (a) Circuit diagram of the five-level rectifier with the L-filter, (b) description of the switching state notation for five-level, (c) possible switching state during $0^o \leq \omega t < 30^o$ and (d) possible switching state during $30^o \leq \omega t < 90^o$.

For $S(P_2N_1P_1)$ under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{4} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{4} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.61}$$

with the KCL rule, the virtual ground voltage under $S(P_2N_1P_1)$ can be written as:

$$V_{mn} = -\frac{V_{dc}}{6} \tag{B.62}$$

Substitute equation (B.62) into phase 'a' voltage of (B.61), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(P_2N_1P_1)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{12} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} - \frac{V_{dc}}{12} \right] \end{aligned} \tag{B.63}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(P_2N_1P_1)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t - \frac{V_{dc}}{12} \right] \tag{B.64}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(P_2N_1P_1)} = \frac{1}{2LF_s}\left[m - 1\right]\left[V - \frac{V_{dc}}{6} \right] \tag{B.65}$$

For $S(N_2N_1P_1)$ under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{4} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.66}$$

with the KCL rule, the virtual ground voltage under $S(N_2N_1P_1)$ can be written as:

$$V_{mn} = -\frac{V_{dc}}{12} \tag{B.67}$$

Substitute equation (B.67) into phase 'a' voltage of (B.66), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(N_2N_1P_1)} &= \frac{d_a T_s}{L_a}\left[V_{an} + \frac{V_{dc}}{12} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} + \frac{V_{dc}}{12} \right] \end{aligned} \tag{B.68}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(N_2N_1P_1)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t + \frac{V_{dc}}{12} \right] \tag{B.69}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(N_2N_1P_1)} = \frac{1}{2LF_s}\left[m - 1\right]\left[V + \frac{V_{dc}}{6} \right] \tag{B.70}$$

For $S(N_20P_2)$ under $0^o \le \omega t < 30^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{4} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.71}$$

with the KCL rule, the virtual ground voltage under $S(N_20P_2)$ can be written as:

$$V_{mn} = \frac{V_{dc}}{12} \tag{B.72}$$

Substitute equation (B.72) into phase 'a' voltage of (B.71), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(N_20P_2)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{12} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} - \frac{V_{dc}}{12} \right] \end{aligned} \tag{B.73}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(N_20P_2)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t - \frac{V_{dc}}{12} \right] \tag{B.74}$$

The maximum ripple current is occurred at $\omega t = 30^o$, one can obtain as:

$$\Delta i_{L,rec,S(N_20P_2)} = \frac{1}{2LF_s}\left[m - 1\right]\left[V - \frac{V_{dc}}{6} \right] \tag{B.75}$$

For $S(P_1N_1P_2)$ under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{4} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + \dfrac{V_{dc}}{4} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.76}$$

with the KCL rule, the virtual ground voltage under $S(P_1N_1P_2)$ can be written as:

$$V_{mn} = -\frac{V_{dc}}{6} \tag{B.77}$$

Substitute equation (B.77) into phase 'a' voltage of (B.76), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(P_1N_1P_2)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} - \frac{V_{dc}}{3} \right] \end{aligned} \tag{B.78}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(P_1N_1P_2)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t - \frac{V_{dc}}{3} \right] \tag{B.79}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(P_1N_1P_2)} = \frac{1}{LF_s}\left[2m - 1\right]\left[V - \frac{V_{dc}}{3} \right] \tag{B.80}$$

For $S(P_1N_1N_2)$ under $30^o \le \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{2} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{4} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.81}$$

with the KCL rule, the virtual ground voltage under $S(P_1N_1N_2)$ can be written as:

$$V_{mn} = -\frac{V_{dc}}{12} \tag{B.82}$$

Substitute equation (B.82) into phase 'a' voltage of (B.81), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(P_1N_1N_2)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{5V_{dc}}{12} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} - \frac{5V_{dc}}{12} \right] \end{aligned} \tag{B.83}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(P_1N_1N_2)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t - \frac{5V_{dc}}{12} \right] \tag{B.84}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(P_1N_1N_2)} = \frac{1}{LF_s}\left[2m - 1\right]\left[V - \frac{5V_{dc}}{12} \right] \tag{B.85}$$

For S(P_20N_2) under $30^o \leq \omega t < 90^o$

The grid phase voltage can represent as:

$$\begin{cases} V_{an} = L_a \dfrac{di_a}{dt} + \dfrac{V_{dc}}{4} + V_{mn} \\ V_{bn} = -L_b \dfrac{di_b}{dt} - \dfrac{V_{dc}}{2} + V_{mn} \\ V_{cn} = L_c \dfrac{di_c}{dt} + V_{mn} \\ i_a - i_b + i_c = 0 \end{cases} \tag{B.86}$$

with the KCL rule, the virtual ground voltage under S(P_20N_2) can be written as:

$$V_{mn} = \frac{V_{dc}}{12} \tag{B.87}$$

Substitute equation (B.87) into phase 'a' voltage of (B.86), the ripple current can be formulated as:

$$\begin{aligned} \Delta i_{La,rec,S(P_20N_2)} &= \frac{d_a T_s}{L_a}\left[V_{an} - \frac{V_{dc}}{3} \right] \\ &= \frac{1}{L_a F_s}\left[2M_a - 1\right]\left[V_{an} - \frac{V_{dc}}{3} \right] \end{aligned} \tag{B.88}$$

Calculate the ripple current expression into a general mathematical expression by expanding it into trigonometric form, we get:

$$\Delta i_{L,rec,S(P_20N_2)} = \frac{1}{LF_s}\left[2m\sin\omega t - 1\right]\left[V\sin\omega t - \frac{V_{dc}}{3} \right] \tag{B.89}$$

The maximum ripple current is occurred at $\omega t = 90^o$, one can obtain as:

$$\Delta i_{L,rec,S(P_20N_2)} = \frac{1}{LF_s}\left[2m - 1\right]\left[V - \frac{V_{dc}}{3} \right] \tag{B.90}$$

Author's Publications

Conference

[1] A. I. Maswood, O. H. P. Gabriel, and M. A. Rahman, "High power multilevel inverter with unity PF front-end rectifier," in *Transportation Electrification Conference and Expo (ITEC), 2012 IEEE*, 2012, pp. 1-5.

[2] O. H. P. Gabriel, A. I. Maswood, and A. Venkataraman, "Multiple-poles multilevel diode-clamped inverter (M^2DCI) topology for alternative multilevel converter," in *IPEC, 2012 Conference on Power & Energy*, 2012, pp. 497-502.

[3] H. R. Pinkymol, A. I. Maswood, O. H. P. Gabriel, and L. Ziyou, "Analysis of 3-level inverter scheme with DC-link voltage balancing using LS-PWM & SVM techniques," in *Renewable Energy Research and Applications (ICRERA), 2013 International Conference on*, 2013, pp. 1036-1041.

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on Industrial Technology (ICIT), 2015, Accepted for conference presentation in Seville, Spain.

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[1] A. I. Maswood, O. H. P. Gabriel, and E. Al Ammar, "Comparative study of multilevel inverters under unbalanced voltage in a single DC link," *Power Electronics, IET,* vol. 6, pp. 1530-1543, 2013.

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[3] O. H. P. Gabriel, A. I. Maswood and L. Ziyou, "Five-level multiple-pole PWM AC-AC converters with reduced components count," *Industry Electronics, IEEE Transactions on,* Accepted for Publication.

[4] O. H. P. Gabriel, A. I. Maswood, L. Ziyou and M. A. Chaitanya, "Grid Connected Three-Phase Multiple-Pole Multilevel Unity Power Factor Rectifier with Reduce Components Count," *Power Electronics, IET,* Will submit for review.

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U.S. Patent

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