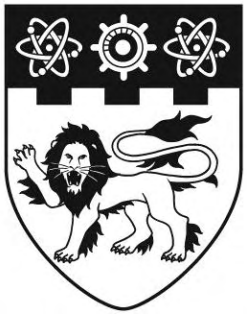

NANYANG TECHNOLOGICAL UNIVERSITY

NANOCRYSTAL FORMATION FOR NON-VOLATILE MEMORY APPLICATION

CHAN MEI YIN

SCHOOL OF MATERIALS SCIENCE AND ENGINEERING

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NANOCRYSTAL FORMATION FOR NON-VOLATILE MEMORY APPLICATION

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School of Materials Science and Engineering

A thesis submitted to the Nanyang Technological University
in fulfillment of the requirement for the degree of
Doctor Philosophy

2010

ABSTRACT

This dissertation focuses on the formation of nanocrystals and integration with high-k dielectrics to address the gate stack and voltage scaling issues for future generation flash memory. Several concepts for improved device performance were discussed, including the introduction of new materials, process development and novel device structures.

The first part of the work introduces a simple technique for the formation of Ge nanocrystals embedded in Lu_2O_3 high-k dielectric using pulsed laser deposition followed by rapid thermal annealing. The nanocrystal formation mechanism was discussed, which elucidates the low temperature formation of nanocrystals. The feasibility of tuning the nanocrystal density was further demonstrated with adequate size control. The size-dependent properties of nanocrystals were also examined, which shows the charge confinement effects in the small-size nanocrystals. The fabricated capacitor devices show promising potential for low voltage memory application, and a charge storage model was proposed. Further enhancement of the memory performance was demonstrated with the realization of a lanthanide-based graded high-k barrier structure, which shows simultaneous improvement in charge storage and retention.

The second part of the work explores a solution-based chemical synthesis approach to provide adequate control on the size, density and surface properties of the nanocrystals. A sonochemical reduction method was introduced for the synthesis of Ge nanocrystals, without the need of high temperature and pressure. A reduction of nanocrystal size and a more narrow size distribution was achieved, with effective surface passivation of the Ge nanocrystals. Self-assembly of Ge nanocrystals was further demonstrated by using functionalized substrate surfaces for chemical grafting of the nanocrystals. The fabrication of a colloidal nanocrystal / high-k dielectric charge storage memory device suggests a potential approach in overcoming the difficulties inherent in physical techniques for well-defined key device features.

The final part of the work introduces a carbon nanotube (CNT)-based alternative memory device architecture, with an enlarged memory window resulting from hybrid charge storage in Ge nanocrystal / high-k dielectric matrix and a large charge sensitivity of CNT channel. A comprehensive study on the trap properties highlights the important role of deep Ge nanocrystal traps for stable charge storage, which shows significant retention and endurance improvement. Further optimization of the device performance may lead to next generation nanoscale charge-based storage system for high density and low power memory applications.

ACKNOWLEDGEMENT

The success of this project cannot be achieved without the support and encouragement of many individuals.

First and foremost, I would especially like to thank my thesis supervisor, Associate Professor Lee Pooi See, for giving me the opportunity to undertake this interesting research experience. I am grateful for her invaluable guidance along the course of my research. The experience under her supervision has not only equipped me with technical knowledge, but also trained me to be a stronger person to face future challenges. My deepest appreciation also goes to Dr. Lap Chan, Dr. Ng Chee Mang and Dr. Vincent Ho from Chartered Semiconductor Manufacturing Ltd Singapore for providing a fruitful learning experience and support in my research work.

This piece of work would also not be possible without the support and assistance of many individuals from different departments. I would like to express my gratitude to Professor Cho Byung Joo, Professor Pey Kin Leong and Dr. Ramam Akippedi for providing me an opportunity to access the facilities in silicon nanodevice laboratory (SNDL), microfabrication laboratory (MFL) and Institute of Materials Research and Engineering (IMRE) for device fabrication. My appreciation is also extended to Assistant Professor Wang Junling from the School of Materials Science and Engineering (MSE) and Professor M. P. Srinivasan, for his support and advice on device characterization. I would also like to thank the staff of the laboratories from MSE, SNDL, MFL and IMRE, in particular Heryani, Mastura, Guo Jun, GangYih, Kwok Fai, Ling Ling, Siew Lang, Chee Tee and Emily for their technical support during the conduct of my experiments.

I would like to acknowledge my fellow seniors and research partners, Dr. Toh Suey Li, Dr. Ong Yi Ching, Dr. Yudi Setiawan, Peter Darmawan, Steve, Ya Ting, Assistant Professor Wong Lydia, Dr. Tan Tam Lyn, Dr. Zhang Tao, Allen, Donny, Eugene, Raymond, Yoga, Stella and Johnson, who have provided great assistance during my project execution. The discussions that I have engaged with them have yielded fruitful insights to my research project. During my time in MSE, I must also mention my laboratory mates, May, Yee Yan, Riko, Yu Hua, Kwan Wee, Chan Hoe, Yan Hua, Dr. Teh Lay Kuan, Dr. Ang Xiao Fang, Meng Keong, Derrick, Duen Yang, Phoebe, Jun Nie, Ee Ling and Vivian. It was all thanks to them that I was always not short of companionship and letting me have an enjoyable time in the laboratory amidst the pressure of my research.

Last but not least, I would like to thank my dear family and friends, for their support and encouragement throughout my studies. They are my pillar of strength that kept me going until I reach the finishing line.

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CHAPTER 1 INTRODUCTION

1.1 Background

The mainstream baseline memory technology today includes Static Random Access Memory (SRAM), Dynamic Random Access Memory (DRAM) and Flash Memory. A computer relies on SRAM and DRAM to supply data bits to the microprocessor. SRAM preserves data only while the power is continuously applied, while DRAM needs to be periodically refreshed even when the power remains applied, hence they are classified as volatile memory. Flash memory is a solid-state non-volatile memory with the data preserved even without power supply, which has found niches in solid-state hard disks, digital cameras and cellular phones. Among the three types of memories, SRAM has the advantage of fast read/write performance, DRAM shows high density capabilities, while Flash memory exhibits non-volatile characteristics. The driving force for new memory concepts is to be able to combine the benefits of these three types of memories in search for a new, 'universal' memory which exhibit non-volatility, high performance for high speed and low energy requirements, and high density.

Non-volatile memory (NVM) is quickly becoming an important function for System-on-a-chip (SoC) applications, which is dominated by NOR and NAND flash technologies. NOR flash technology is used for code and applications storage, which features eXecute In Place (XIP) that allows an application to be run directly from flash instead of reading the application code into system RAM. NOR delivers high read performance and is most cost effective in lower capacities – 1 to 4 Mbytes, but it suffers from extremely low write-and-erase performance. On the other hand, NAND architecture offers extremely high cell densities that translate to high storage capacity,

combined with fast write and erase speeds. However, there exists difficulty of using NAND with the need for flash management and special requirements for system interface. NAND technology is taking the lead in the memory density race today by providing multi-gigabit chips already in mass production, which is replacing hard drives in many consumer products, such as MP3 players, and becoming increasingly significant in laptops.

A flash memory cell is a metal-oxide-semiconductor field-effect-transistor (MOSFET) with a polysilicon floating gate sandwiched between a tunnel oxide and an inter-poly oxide to form a charge storage layer, as shown in Fig. 1.1.1. The floating gate flash memory is expected to face fundamental barrier between the 22 and 45nm process nodes[1] due to tunnelling oxide scaling limitations and storage node capacitive coupling.[1,2] Continuous scaling requires the reduction of gate length and write voltage, which is typically achieved by thinning the inter-poly and tunnel oxide. Tunnel oxide must be thick enough to assure retention but thin enough to allow ease of write/erase. Inter-poly dielectric must be thick enough to assure retention but thin enough to maintain an almost constant coupling ratio.

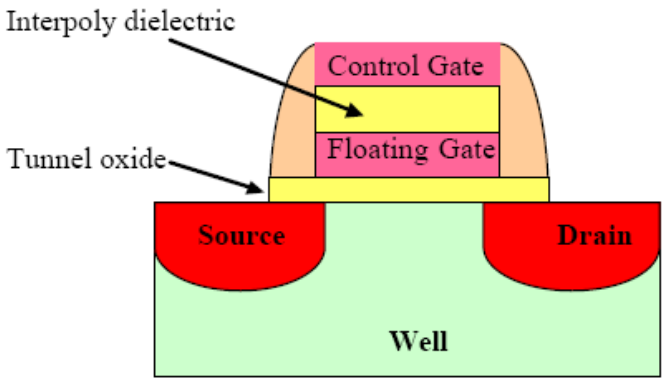


Fig. 1.1.1 Schematic diagram of a conventional Flash memory device with a MOSFET structure comprising a floating gate and control gate separated by an interpoly dielectric layer. The floating gate is generally a continuous polysilicon layer for storing charges.

Today's NAND Flash allows a tunnel oxide of 6-7nm. Next-generation flash cells required tunnel oxide to be further reduced to <6nm, which dramatically increases the tunnel current resulting in loss of the stored charge on the floating gate.[2,3] As shown in Fig. 1.1.2, each bit of the memory device is represented by only a few hundred to thousand electrons, the loss of one electron per day can result in the bit failure after a few years of storage.[3,4] The diminishing number of electrons poses significant restrictions on the device lifetime, thus resulting in reduced charge loss tolerance to less than ten electrons in 32nm technology node. Another significant scaling challenge involves maintaining adequate coupling of the control gate to the floating gate when the floating gate height reduced as the space between adjacent poly-Si gates shrink. Potential solutions to mitigate tunnel oxide scaling and coupling issue include the introduction of high-k dielectrics,[5] extension of the floating gate memory by charge trap memory devices by charge trap memory devices utilizing nitride layer or nanocrystals as charge storage elements[6-8] and the incorporation of strained silicon in flash devices.[3] Besides that, a number of non-charge-based memories are emerging, with new storage concepts including magnetic random access memory (MRAM),[9] ferreoelectric memory (FeRAM)[10] and phase change memory (PCRAM).[11]

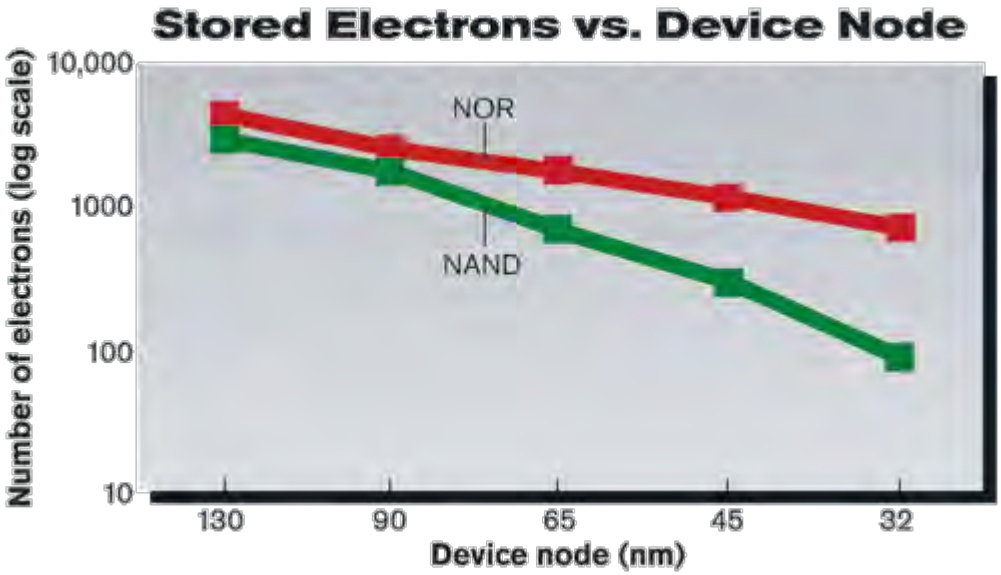


Fig. 1.1.2 The number of stored electrons for NOR and NAND Flash memory at different device technology node (reprinted from Ref [12]).[12]

Improving charge storage and retention are key enablers required for NVM scaling, and the most viable alternative today is the charge trap flash (CTF) memory with nanocrystal- and nitride-based storage. The discrete charge storage mitigates the vulnerability of charge loss through localized oxide defects, thus improving the device retention characteristics. Fig. 1.1.3 shows the schematic diagram of a floating gate memory device with continuous polysilicon floating gate and a nanocrystal memory device with an array of nanocrystals as the charge storage nodes. With the utilization of distributed and isolated nanocrystals, the impact of a single leakage path due to defect in the oxide is limited to charge stored in its proximity instead of leaking from the conducting floating gate. Hence the distributed nature of charge storage in nanocrystal memory makes it more robust to stress-induced leakage current (SILC). Due to a less sensitivity to gate oxide quality, a thinner tunneling oxide can be employed, which allows a faster write/erase speed and lower power operation accompanied with operating voltage scaling. Moreover, the discreteness of the charge

traps enables multibit-per-cell storage without going through multilevel approach, which poses stringent requirement on the threshold voltage control.[13,14]

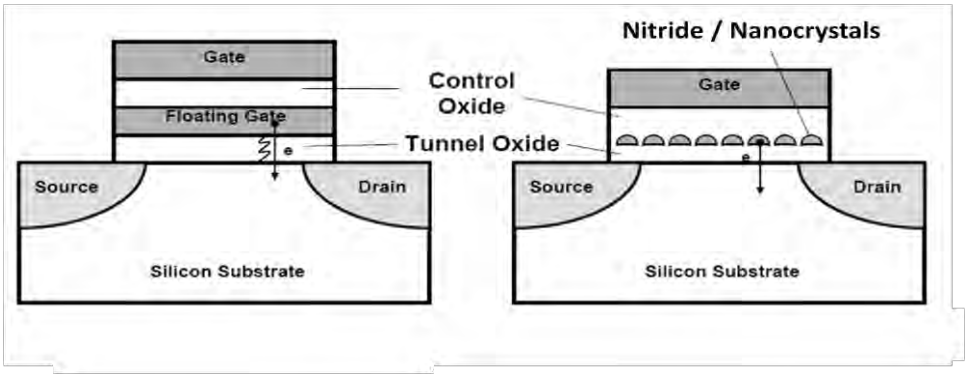


Fig. 1.1.3 Schematic of a memory cell with conventional floating gate and nitride / nanocrystals as discrete charge storage elements.

In terms of scaling limitations, nanocrystal memory has several advantages over nitride trap memory. First, compared to the atomic-size nitride traps, electron or hole energy states are energetically deeper in the nanocrystal potential wells.[15] The small conduction band discontinuity (ΔEc) of only 1.1eV at the Si_3N_4/SiO_2 interface results in poor retention and endurance properties due to charge leakage from its shallow trap sites.[16-18] Second, the ordering of trap sites is more controllable in nanocrystal memory,[19,20] while in nitride trap memory, trap sites are based on random distribution of dangling bonds, and charge storage is inhomogeneous in the memory structure. The volume charge trapping effect and over-erase phenomena due to hole trapping in the nitride valence band can cause severe distribution in the threshold voltage.[21] Third, nanocrystals have a large cross-section for charge trapping which leads to a larger trapping probability.[22] Furthermore, nanocrystal memory exhibits interesting potential for multibit storage application by utilizing Coulomb blockade effect, which is limited by tunneling between storage nodes.[23-25]

1.2 Motivation

The futuristic non-volatile storage memories demand for the need of new materials and memory concepts in approaching terabit storage density with high performance. The unique physical and chemical properties of nanocrystals arising from their nanometer size effect represent one of the key features motivating the study of nanocrystals for memory applications. In view of the attractive potential of nanocrystals as nanoscale functional components, this work seeks to explore their desirable attributes and opportunities for implementation and alleviate the scaling limitations of memory devices. When confined in the nanoscale, nanocrystals provide a means to limit the number of electrons employed due to Coulomb Blockade effect with reduced number of states and reduced capacitance. The concept of harnessing a single electron or just a few electrons for memory storage for the mitigation of defect-mediated charge loss is appealing. This work aims to exploit the advantage of charge confinement effect of nanocrystals for the realization of memory storage structures with extended capabilities.

In spite of the promising potential of nanocrystals for ideal data storage, there exist several challenges in the implementation of nanocrystal memories. One key issue is the process control requirements with regards to the properties, including size and size distribution, inter-crystallite spacing (lateral isolation), uniformity and aerial density. The main limitation for the fabrication methods today is the low threshold voltage shift related to limited gate surface coverage, and fluctuation of electrical characteristics due to the spread in dot size and density, which significantly affects the variation of the threshold voltage especially as the size of the memory cell decreases. This work seeks to establish the formation of Ge nanocrystals via a physical approach

using pulsed laser deposition technique and chemical approach using solution synthesis technique, with the aim of forming self-organized nanocrystals with distinct chemical composition, structure, size and density, which is applicable in different dielectric systems.

Although semiconductor nanocrystal-based memory is a potential candidate for future non-volatile memories, it suffers from weak electrostatic coupling and small memory window (threshold voltage shift). In addition, the trade-off between program/erase efficiency and data retention remains an important issue to be addressed. This motivates the search for new materials, with high-k dielectrics envisioned as a potential solution to obtain a compromise of the memory performance. In this work, different high-k materials are adopted as the tunnelling and blocking dielectric materials, with an emphasis on the lanthanide-based high-k dielectric. In particular, Lu_2O_3 is studied due to its favourable properties of thermodynamical stability, low crystallization temperature and low leakage current characteristics with a moderately high dielectric permittivity (~12).[26-28]

Lastly, an understanding of the operation of nanocrystal memories is required and the physical aspects with the underlying charge trapping mechanism would be studied. The challenges associated with the integration of the new materials and structures need to be addressed for reproducible and improved device characteristics.

1.3 Research Objectives and Scope

The main objective of this research is to study the integration of Ge nanocrystals with high-k dielectrics for memory application. The first approach involves the identification and selection of the nanocrystal and dielectric material system, focusing

on lanthanide-based high-k dielectric. The goal is to establish a pulsed laser deposition technique for well-controlled formation of Ge nanocrystals with desired size, density and dot separation for memory application. The nanocrystal formation mechanism is studied with the aim of developing an optimized process to form self-organized nanocrystals with tailored properties, i.e. uniform and small size nanocrystals with high areal density and sufficient intercrystallite separation.

The evaluation of Ge nanocrystal / high-k dielectric system for low voltage memory device would be carried out, which focuses on the role of nanocrystals on the charge trapping properties. Ultimately, in the search for an enhancement of memory properties by optimizing the program/erase and retention behaviour, an alternative concept is suggested using a dielectric modification approach. In addition, the charge confinement effects of nanocrystals would be explored to obtain a better understanding of the size-dependent electrical properties of the nanocrystals.

In order to achieve size-monodisperse nanocrystals with tailored size and density, a chemical approach is explored on a simple chemical reduction of precursor solution without the need of high temperature and pressure. Following that, integration strategies employing chemical functionalization of substrate surfaces is proposed for self-assembly and transfer of the colloidal synthesis methodology for memory device application.

Finally, an alternative memory concept is proposed for future high density memory device using a nanoscale device architecture with hybrid nanocrystal / high-k dielectric on advanced channel structure. The scope includes the integration of

nanocrystals with carbon nanotube (CNT) channel, with interest deriving from an improved electrostatic coupling effect associated with reduced channel width and large charge sensitivity of CNTs.

1.4 Organization of Report

Chapter 1 gives an overview on the background and development of NVM. The motivation of the formation of nanocrystals and the introduction of high-k dielectrics for memory application would also be introduced. In Chapter 2, a brief introduction on the operation behaviour of nanocrystal memories would be given, followed by the challenges current development of nanocrystal memories. In addition, the material selection and device design aspects would be discussed, followed by different techniques for the formation of nanocrystals. The experimental details on the technique utilized for nanocrystal formation and device fabrication would be described in Chapter 3. In Chapter 4, the formation and evolution of Ge nanocrystals by pulsed laser deposition technique is demonstrated, and the nanocrystal formation mechanism is discussed. Chapter 5 shows the application of the Ge nanocrystal / high-k dielectric system in memory capacitor device, as well as optimization strategies using a barrier modification approach for enhanced memory behaviour. The localized electrical properties and effect of dielectric matrix on the charge trapping properties are also discussed. In Chapter 6, a chemical approach for controlled synthesis and self-assembly of Ge nanocrystals is introduced for memory application. In Chapter 7, an alternative device architecture integrating the Ge nanocrystal / high-k dielectric material system to form a CNT-based memory is demonstrated. Finally, Chapter 8 summarizes the conclusion based on the results obtained outlines the recommendations for future work.

CHAPTER 2 LITERATURE REVIEW

2.1 Nanocrystal Memory Device Operations

The nanocrystal memory device utilizes a distributed film of nanocrystals as the floating gate for charge storage, which is sandwiched in between the bottom tunnel oxide and thick control oxide of the transistor structure. Fig. 2.1 shows the schematic diagram of a typical nanocrystal memory device and the corresponding band diagrams for electron injection (write cycle), storage (store) and removal (erasure) in the n-channel silicon field-effect transistor (FET).[23] During the write cycle, electrons tunnel from the channel inversion layer to the nanocrystals under a positive voltage application (i.e. forward biased wrt. source and drain), as shown in Fig. 2.1. Carriers are injected into the floating gate via Fowler-Nordheim (F-N) tunnelling or channel hot electron injection. During the erase process, electrons can tunnel from the nanocrystals to the substrate (or holes can tunnel from the substrate accumulation layer to the nanocrystals) under a negative voltage application, due to the lowered energy with respect to the control gate.

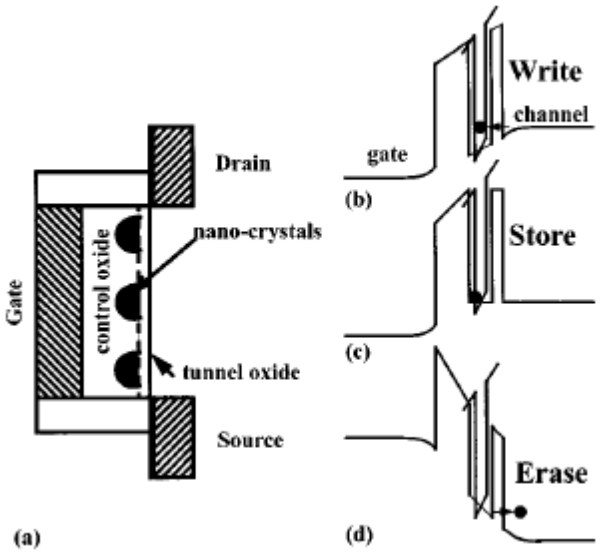


Fig. 2.1 A schematic cross section of a nanocrystal memory device (a) and the corresponding band diagram for electron (b) injection (c) storage and (d) removal from a nanocrystal proposed by Tiwari *et. al.* (reprinted from Ref [23]).[23]

The stored electrons in the nanocrystals effectively screen the gate charges, resulting in a threshold voltage shift due to the coupling of nanocrystals to the channel. The surface of a p-type substrate becomes less depleted with holes or less inverted with electrons, as a result of excess electrons in the nanocrystals. This reduces the conduction in the inversion layer, resulting in a threshold voltage shift towards more positive values. This results in a low current state, corresponding to a value of "0", upon reaching the charge threshold. On the other hand, the channel becomes less accumulated with holes as a result of electron emission from the nanocrystals or injection of holes into the nanocrystals. This results in a threshold voltage shift towards more negative values. Hence, the memory device goes back to the high current state, corresponding to a value of "1" when the residual charges is below a certain threshold level. In this way, each cell can hold one bit of information. The

effective threshold voltage of the memory device is determined by the amount of charge stored, with the threshold voltage shift, ΔV_T given by

$$\Delta V_T = \frac{npq}{\varepsilon_{ox}}\left(t_{cntl} + \frac{\varepsilon_{ox} d}{2\varepsilon_{Si}}\right) \tag{2.1}$$

where n is the nanocrystal density, p is the average number of electrons stored in a nanocrystal, q is the electronic charge, ε_{ox} and ε_{Si} represent the permittivity of the oxide and silicon respectively, d is the nanocrystal diameter, and t_{cntl} is the control oxide thickness.[23] For flash type memory operation, a large threshold voltage shift is required to obtain a large I_{on}/I_{off} ratio in terms of current sensing for low disturbance and fast switching. [23]

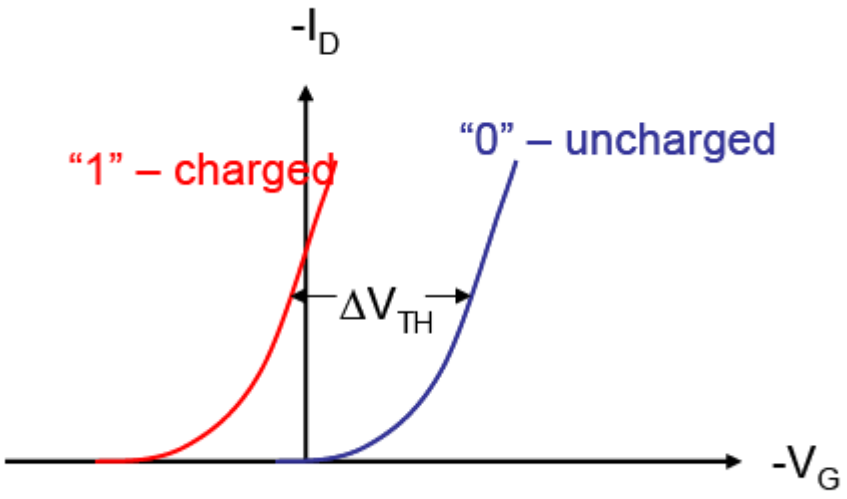


Fig. 2.2 Effect of charge storage on the threshold voltage of a n-channel memory device.

In the quiescent bias state under retention, leakage of the charge can occur either laterally by conduction between the nanocrystals or back-tunneling from the nanocrystals to the Si substrate.[29] The latter charge leakage can be reduced with the susceptibility to tunnel oxide defects mitigated by having a higher density, n, of

nanocrystals and a minimized number of electrons stored per nanocrystal, p for a given number density of electrons, np.[30] On the other hand, in order to prevent lateral charge conduction, a nanocrystal separation of about 5nm is necessary for reduced tunnelling probability and ensure sufficient electrical isolation.[30] Besides that, charge confinement effects or Coulomb blockade effects of nanocrystals could adversely affect the charge retention characteristics due to an increase in energy levels when multiple electrons are stored in the nanocrystals. With reduced nanocrystals size, the increase in energy levels becomes more significant. This can be calculated from the self capacitance of the nanocrystal given by

$$C= 2\pi\varepsilon_{ox}d \tag{2.2}$$

The increase in energy for a nanocrystal upon addition of the nth electron is given by

$$\Delta E_{n,n-1} = \frac{q^2}{2C}[n^2-(n-1)^2] = \frac{nq^2}{C} - \frac{q^2}{2C} \tag{2.3}$$

and the electrochemical potential change associated with the addition of each electron is given by

$$\Delta\mu = \Delta E_{n,n-1} - \Delta E_{n-1,n-2} = \frac{q^2}{C} \tag{2.4}$$

The small size requirement of nanocrystals for memory device application gives rise to a small self capacitance in atto farads (10^{-18}F), which results in a pronounced effect of the change in energy level. For example, an energy level of 0.5eV above the ground state is estimated for a nanocrystal of a diameter of ~5nm with five electrons stored. The increase in energy level adversely impacts the retention characteristics due to tunnelling mediated charge storage loss, which limits the amount of charge storage in the nanocrystal.

The optimal size and density of the nanocrystals can thus be estimated based on these considerations, with the assumption that nanocrystals of diameter d and a fixed edge-to-edge separation of s are arranged in a square lattice.[30,31] In order to mitigate lateral charge tunnelling between adjacent nanocrystals in the timescale of interest, thenanocrystal separation, s has to be above the threshold distance for tunnelling. Since the nanocrystal density is inversely proportional to $(d+s)^2$, the threshold voltage shift relation is given by

$$\Delta V_t \propto \frac{p}{(d+s)^2} \tag{2.5}$$

However, the effect of increased energy levels due to Coulomb Blockade effects poses limitation on the number of electron storage in a nanocrystal. Based on the data retention and read disturb criteria,

$$p \sim \frac{1}{\mu} \sim d \tag{2.6}$$

Hence, the threshold voltage shift can be written as

$$\Delta V_t \propto \frac{d}{(d+s)^2} \tag{2.7}$$

The distinct maximum of V_{th} could be obtained at d equal to s, which allows a large memory window to be achieved. The nanocrystal separation requirement of ~5nm gives an optimum nanocrystal diameter of 5nm. This in turn gives an optimal nanocrystal density of $10^{12}cm^{-2}$.[23] With sufficient electrical isolation of the nanocrystals, leakage primarily occurs by back-tunnelling from the nanocrystals to the substrate. This allows significant improvement in the charge retention characteristics associated with reduced parasitic tunnelling current.

2.2 Nanocrystal Memories – State of the Art and Issues

The first Si nanocrystal memory device with SiO_2 oxide barrier was demonstrated by Tiwari et. al.[23,32] Nanocrystal memory devices offer the advantages of improved retention, low power and fast program/erase operation, better endurance and immunity to soft errors. [33,34] Despite the promising device characteristics of Si nanocrystal-based memory devices, devices with SiO_2 tunneling barrier suffer from the trade-off between data retention and programming efficiency characteristics,[35] which poses limitation on the scaling of operation voltage. Hence recent efforts have focused on the replacement of SiO2 with high-k dielectrics to optimize the device performance.[36,37] This approach creates an asymmetry in charge transport through the gate dielectric in the programming and retention modes in order to maximize the $I_{G,\ Write/Erase}/I_{G,\ Retention}$ ratio.[38] In recent years, different candidate nanocrystal materials have also been explored as charge storage elements, including Ge nanocrystals,[39,40] SiGe nanocrystals,[41] metal[42,43] and dielectric nanocrystals.[44] Ge nanocrystals are considered as a strong candidate to replace Si nanocryststals as storage nodes due to its relatively small band gap compared to Si and compatibility with current complementary metal-oxide (CMOS) technology. With a smaller bandgap of Ge, the electrons face a smaller barrier to tunnel from the Si substrate into the nanocrystals during program/erase (P/E) mode. At the same time, and improved retention is enabled due to a higher confinement barrier of the charges.[45,46] Recently, the advantages of Ge over Si nanocrystal memory have been demonstrated by King et. al. in terms of the operating voltage and P/E time.[47] Due to the compatibility with standard CMOS process and relatively low P/E voltages, Ge nanocrystal memories are attractive candidate for embedded applications. Besides that, Ge nanocrystals exhibit advantages over Si with a higher carrier mobility of Ge and large excitonic

Bohr radius of ~18nm. Recently metal nanocrystals have also received considerable attention due to the advantage of an asymmetric electric field enhancement and selectable work function with deeper potential well for enhanced charge storage capacity, and an enhanced programming efficiency with large density of states. [41] However, metal nanocrystal memories suffers from several other issues, including degraded retention characteristics due to contamination problem and potential Fermi level pinning at the interfaces between metal nanocrystals and high-k dielectric.[15] Dielectric nanocrystals, on the other hand, are less favorable due to difficulties in controlling the defect-related traps of the dielectric material.[48]

Although nanocrystal memory offers attractive advantages over conventional memory, several issues remain before being implemented for mass production. The first issue is to establish nanocrystal fabrication techniques with the controllability of size, density and distribution to ensure cell-to-cell uniformity. In order to achieve tha highest possible nanocrystal density in excess of $10^{12}cm^{-2}$, adequate control of nanocrystal size and dot-to-dot separation of ~4-5nm is the key.[33,38] The approach of increasing the nanocrystal density enhances the risk for percolation between adjacent nanocrystals, which is detrimental for charge retention. The fabrication methods reported to date still face the controllability issue during the formation of nanocrystals. The variation in nanocrystal size and density in turn leads to fluctuations in device performance.[21,49] It has been demonstrated that the variation in the programmed states increases as the size of the memory cell decreases due to the non-uniformity of the size and density of the nanocrystals, which limits the application in high density and large-scale memory arrays.[33,36] The second issue is the voltage-time dilemma due to the trade-off between retention and programming efficiency, and the difficulty to

match the voltage and speed of memory to the logic devices. Furthermore, much work is needed to understand the underlying mechanisms responsible for charge trapping and size-dependent properties of nanocrystal memory devices. The contribution of highly confined electrons[38,50] and defect-related traps in the nanocrystals and nanocrystal/oxide interface on the charging behaviour needs to be determined. The ultimate limits of nanocrystal memory device are eventually determined by the ability to control and selectively enhance the nanocrystal-related traps over dielectric interface/defect-related traps.[50]

In order to improve nanocrystal memory device performance, recent work has focused on the utilization of high-k dielectrics to achieve a low operation voltage without sacrificing the retention behavior. Due to a smaller equivalent oxide thickness (EOT) and larger physical thickness, a high P/E tunnelling current can be obtained at low gate voltages. On the other hand, the off-state leakage current is reduced to lower levels under the retention mode.[51]The asymmetry of the barrier in P/E and retention mode results in faster P/E associated with an increased field sensitivity of the tunnel barrier, without sacrificing data non-volatility in the retention (low electric field) mode.[37,52] Recent high-k dielectric materials demonstrated for memory device applications include HfO_2,[36,46,53,54] ZrO_2,[55] Al_2O_3,[56] HfAlO,[41] and $LaAlO_3$.[57] However, high-k dielectric materials exhibit a trend of reduced energy band gap along with an increased dielectric constant, as shown in Fig.2.3 (a). HfO_2 is considered as a promising candidate as the first generation high-k dielectric material due to the high dielectric constant (25-30), large energy band gap (~5.6 eV) and high breakdown field (15-20 MV/cm). However, HfO_2 tends to crystallize at a low temperature ~500 ^oC, which leads to possible retention and reliability issues due to grain boundary

formation. Due to an improved thermal stability on Si expected from lanthanide-based high-k dielectrics, candidate dielectrics eg. La_2O_3, Lu_2O_3 and Gd_2O_3 are recently considered as the next generation high-k materials.

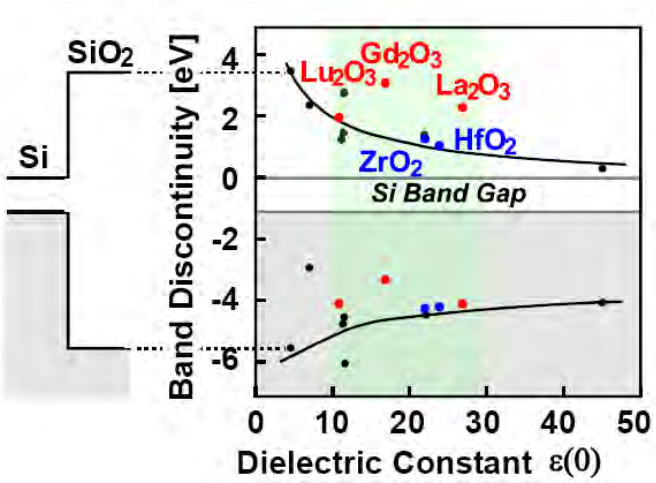


Fig 2.3 Band gap properties of different candidate high-k dielectrics with respect to the dielectric constant

2.3 Nanocrystal Fabrication Techniques and Growth Mechanism

The fabrication routes for the formation nanocrystals remain as a crucial scientific issue to be addressed before successful implementation in different potential applications. Different fabrication techniques for nanocrystal formation have been intensively investigated, including ion implantation followed by annealing,[29] [56,58] chemical vapour deposition (CVD),[59] co-sputtering followed by thermal annealing,[57] oxidation of SiGe, aerosol deposition[19,60] as well as colloidal suspension.[61]

The first three techniques require annealing at high temperatures, and it is difficult to control the size of the nanocrystals because the nucleation and enlargement cannot be independently controlled effectively during the annealing process.[62] Besides that, the ion implantation technique poses limitation on the minimum gate oxide thickness,[63] with possible degradation of the oxides (due to ion implantation damage), spatial

controllability problems,[64] and difficulty in obtaining the required amount of Si in the stack.[65] A well established way to obtain Si nanocrystals for application in nanocrystal memory is the CVD technique, due to its compatibility with standard integrated circuit technology and process tunability through the deposition parameters.[63] However the limited gate surface coverage of the nanocrystals deposited using low pressure CVD technique results in a low threshold voltage shift of the memory device. Besides that, this technique does not allow the flexibility for synthesizing different nanocrystal materials. Unlike SiH_4 that reacts on the SiO_2 surface, GeH_4 only decomposes on the Si surface but not on SiO_2 surface. Hence a two-step process is required for the the formation of Ge nanocrystals. An additional step is needed to for the nucleation of silicon islands which act as seeds on top of the SiO_2 surface for subsequent Ge nanocrystal growth.[61,62] On the other hand, the aerosol method has complications with size selection and particle delivery with the use of gas phase condensation.[66,67] In general, the physical fabrication techniques result in a relatively wide distribution of size and position of the nanocrystals. On the other hand, chemical synthesis of colloidal nanocrystals offers adequate control over the size and surface properties of the nanocrystals with narrow size distribution. It also allows a large scale production of nanocrystals, but it suffers from possible contamination issues due to associated chemicals.[68]This review focuses on the pulsed laser deposition technique as the physical approach and colloidal synthesis technique as the chemical approach for the formation of Ge nanocrystals.

2.3.1 Pulsed Laser Deposition Technique

Recently, successful growth of high quality dielectrics,[68] artificially structured materials,[69] and multicomponent thin films have been demonstrated using pulsed

laser deposition (PLD) technique. Self-assembly of nanostructures with a narrow size distribution was also achieved using PLD technique at low substrate temperatures (500-600 ^{o}C).[70] PLD is a process which involves the removal of atoms from the bulk material as a consequence of the interaction between an intense laser pulse and target material which vaporizes the material due to Coulomb explosion. A plasma plume constituting high energy neutrals, ions and electrons is subsequently developed and transferred onto the substrate surface, as shown in Fig. 2.4.[71,72] The main differences between PLD and other physical vapour deposition (PVD) methods are : (1) A high instantaneous deposition rate in orders of magnitude higher than other growth methods (typically ~2000 MLs^{-1}),[73] due to short bursts arrival of the depositing species in the order of 10–100 μs, and (2) a high kinetic energy of the generated plasma of the depositing species, as compared to and energy of ~1 eV for other thermally-grown films.[74]

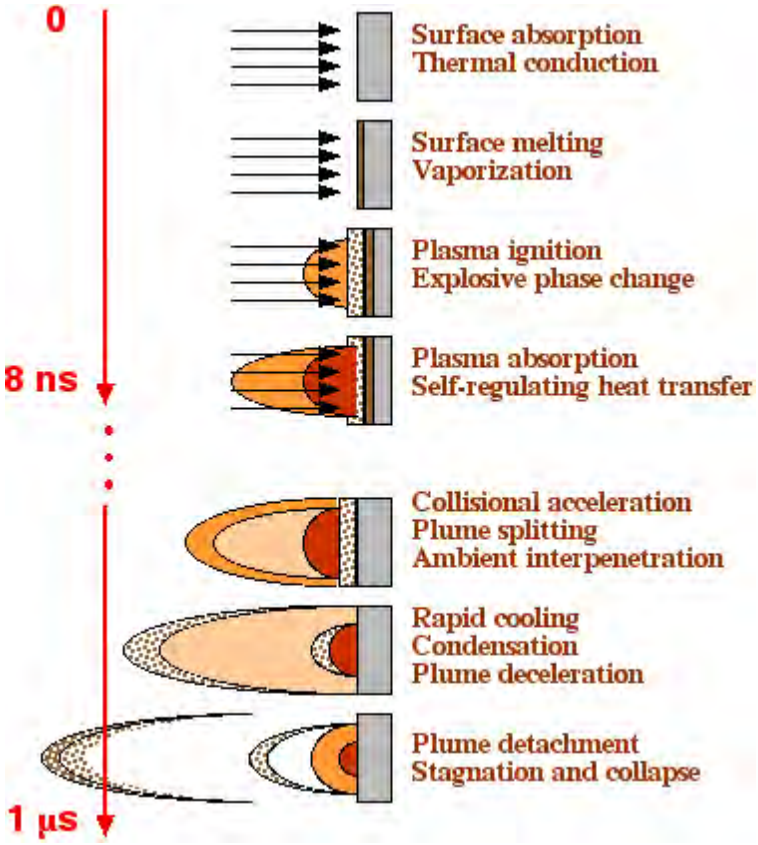


Fig. 2.4 Stages of laser ablation plume creation, expansion and condensation (reprinted from Ref [63]).[75]

The growth kinetics of PLD differs significantly from other PVD techniques as a consequence of high forward velocity of the plasma plume. This can be explained according to the classical nucleation theory. The balance between the volume free energy, ΔG_v and the surface energy, ΔG_s which acts as an energy barrier due to surface tension determines the formation of stable islands. Fig. 2.5 shows the total free energy of formation, ΔG governed by the equation,[74]

$$\Delta G = -\frac{4}{3}\pi\ r^3(n\Delta\mu) + 4\pi\ r^2\sigma \tag{2.8}$$

where n is the atom number density, $\mu = kT\ \ln S$ is the difference in chemical potential between the atoms with and without nucleation and σ is the surface tension.

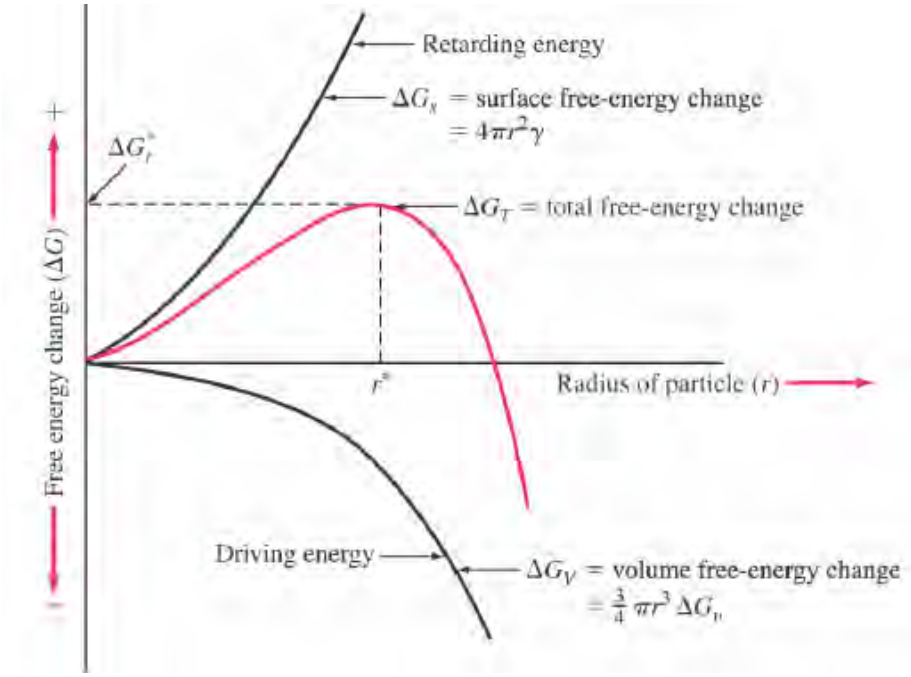


Fig. 2.5 The total free energy change determined from the balance between ΔG_v and ΔG_s, which provides the formation of stable nucleus above a critical radius of particle.

The critical free energy change needed to obtain a stable nuclei, ΔG* occurs at the critical radius point, when r = r*, beyond which the particles grow to a lower energy state. Taking the derivative of equation 2.8 with respect to r and equating to zero yields

$$r^* = \frac{-2\gamma}{\rho\Delta\mu} \tag{2.9}$$

And inserting this value of r^* in equation 2.8 yields

$$\Delta G^* = \frac{16\pi}{3}\frac{\gamma^3}{(\rho\Delta\mu)^2} \tag{2.10}$$

This shows that ΔG* is inversely proportional to the square of the change in chemical free energy per unit volume due to condensation, ΔG_v, which in turn depends on the supersaturation ratio, $S = P_v/P_s$

$$\Delta G_v = \frac{kT}{\Omega}\ln\frac{P_v}{P_s} \tag{2.10}$$

where Ω is the atomic volume, P_v is the vapour pressure of the saturated impinging flux, and P_s is the equilibrium pressure above the solid.

The nucleation rate during thin film deposition, N is proportional to the rate o impingement and density of nucleation site, N* which depends on ΔG*, as given by

$$N^* = n_s \exp\left(\frac{-\Delta G^*}{kT}\right) \tag{2.12}$$

where n_s is the maximum possible nucleation site density.

Hence a high density of stable nucleation sites requires large absolute values of ΔG_v. Due to the logarithmic dependence of ΔG_v on S, a significant increase in nucleation rate can only be realized when the vapor pressure of the impinging flux is orders of magnitude high than that of standard techniques. PLD techniques offer significant increase in nucleation rate associated with small critical radii, as a result of an extremely high saturation ratio due to rapid cooling of the depositing species. Hence the formation of uniformly distributed nanocrystals is expected from an enhanced mobility of the adatoms due to the large incident kinetic energy of the PLD plasma.

For a given saturation ratio, nuclei with size greater than r* will grow, while nuclei with radius smaller than r* will dissolve to lower the free energy. In the case of a continuous supply of precursor provided during the growth stage with the size of particles above r*, smaller particles grow faster since the free energy driving force is larger than larger particles. In the case of depleted precursor at the growth stage, the r* increases corresponding to a decrease in saturation ratio. Particles smaller than the new r* will dissolve, while particles larger than r* will grow, resulting in a broader size distribution. The growth of large particles at the expense of smaller particles is a consequence of Gibbs-Thomson effect. When supersaturation has decreased sufficiently at the later stage of nanocrystal growth, Ostwald ripening (coarsening) of nanocrystals occurs.[76] The evolution of the nanocrystals in coarsening regime follows the model for the diffusive decomposition of a supersaturated solid solution developed by Lifshitz and Slyozov,[77,78] where at time, t, the critical dimension, x_c, of the grain exhibits a $t^{1/3}$ power-law behavior. This gives a degree of supersaturation

that falls as $t^{-1/3}$ and the number of grains as t^{-1}. Arai *et al.*[79] have shown that if a cluster in a supersaturated solid grows by the diffusion process, the diameter of the cluster, d, increases by

$$d \propto (Dt)^{1/3} \tag{2.13}$$

$$D \propto \exp\left(\frac{-\Delta E}{kT}\right) \tag{2.14}$$

where t, D and ΔE are the time, diffusion constant and the activation energy, respectively. k is the Boltzmann constant and T is the temperature in Kelvin. Further broadening of the size distribution can also occur when two or more particles and/or nuclei aggregate together and grow into larger particles.

Most of the early reports on the synthesis of nanocrystalline materials by PLD have been performed in an inert gas environment that promotes clustering in the gas phase.[80] The formation of Ge nanoparticles embedded in a GeO_2 matrix has also been demonstrated using a reactive PLD technique, under a background pressure of reactive gas.[81] Recent works have demonstrated the formation of Ge[82,83] and metal nanocrystals[84] in vacuum environment with narrow size distribution. The observations suggest that the nanocrystals predominantly nucleate and grow at the substrate surface.[78,85,86] The growth of nanocrystals was further extended to the fabrication of nanocomposite films constituting nanocrystals embedded in amorphous dielectric matrix, including Ge-Al_2O_3,[87] Co-ZrO_2,[88] Au-Al_2O_3 [89] and Au-ZrO_2.[90-93] The formation of nanostructures occurs via quasi-three dimensional effective growth as a result of inhomogenous nucleation around the islands. The ionized species expanding in front of the plasma plume bombard the substrate prior arrival of the bulk species,

and the enhanced adatom mobility contributes to enhanced nucleation process.[90] It was shown that the granular thin films contain a more narrow size distribution of the immiscible nanoparticles very well defined with respect to the matrix as compared to the films obtained by other techniques, such as sputtering and ion implantation.[90] Two mechanisms of the particle growth including nucleation and particle coalescence have been observed, with their relative significance being different in different granular systems, yielding very different values of percolation threshold.[94] PLD technique allows the control of nanocrystal size by varying the laser fluence, and the competition between growth and sputtering processes leads to a self-regulation of the nanocrystal size that promotes a narrow size distribution with minimized coalescence.[94]

2.3.2 Colloidal Synthesis Technique

Colloidal chemical synthesis technique has been studied for the formation of monodisperse Ge nanocrystals with controlled particle size and surface properties. The nanocrystal growth process generally involves precipitation of nanocrystals from the solution followed by passivation of the nanocrystals with a capping layer. Different techniques have been employed for chemical synthesis of Ge nanocrystals, including reduction of $GeCl_4$ and R-$GeCl_3$ by Na dispersion in heptane[95,96] and Li naphthalenide,[94] oxidation and subsequent reduction of doped silica xerogel,[21] metathesis of Ge Zintl salts with GeCl4,[24] inverse micelles,[97-99] supercritical thermolysis[100] and tetraethylgermane (TEG) or diphenylgermane (DPG) decomposition in high temperature and pressure.[101] However, studies on the formation of Ge nanocrystals often indicate the need for high temperature and pressure to promote crystallization due to the strong covalent bonding properties of

Ge. Synthesis of Ge nanocrystals in ambient condition has been demonstrated using ultrasonic reduction method without the need for high temperature and pressure.[100,101] Ge nanocrystals were synthesized at room temperature based on the reduction of of precursor anhydrous $GeCl_4$ by metal hydride ($LiAlH_4$ and $NaBH_4$) or alkaline ($N_2H_4 \cdot H_2O$) reducing agent solution in an inert tetrahydrofuran (THF) solvent to avoid oxidation in air. The mechanism for the chemical reaction and crystallization of nanoparticles during the ultrasonic reduction (sonochemical process) is acoustic cavitation, which is an ultrasound-driven formation, growth and collapse of microbubbles.[100] An implosive collapse of the bubbles occurs as the size increases to the maximum threshold, resulting in rapid rupture of the chemical bonding of the reagents. As shown in Fig. 2.6, the formation of nanocrystals could occur at three possible reactions zones, including:

(a) Zone 1 – Gaseous region of cavitation bubbles containing permanent gas and vaporized mixture.

(b) Zone 2 – Gas-liquid transition region containing less volatile reaction components and surfactants

(c) Zone 3 – Bulk liquid phase

The crystallinity of the nanocrystals largely depends on the zone where the reactions occur. Within zone 1, bond breakage occurs when volatile solutes and solvent are exposed to extreme temperature and pressure upon cavitations. It was reported that crystallization of nanoparticles occur when the reaction takes place at the interface of the bubbles at zone 2. On the other hand, an amorphous product is formed if the

reaction takes place inside the bubble as a result of the high cooling rates which occur during the collapse of the bubbles.[101]

Fig. 2.6 Three zones of sonochemical reactions in the liquid medium (Reprinted from Ref [88]). [98]

2.4 Charge Transport Study of Nanocrystal Properties

Due to the promising potential of semiconductor nanocrystals in device applications, understanding the carrier transport and size-dependent electrical properties of the nanocrystals has become increasingly important. The electrical behavior and memory behavior is determined by the size and composition of the nanocrystals, which strongly dictates the changes in energy bandgap and density of states.[102] Conventional electrical measurement techniques using current-voltage measurements and capacitance-voltage techniques only provide the properties averaged over a macroscopic area. Proximal probe microscopic technique capable of simultaneous characterization of the structural and electronic properties with sub-nanometer resolution using scanning tunneling microscope (STM) offer great promise for the investigation of nanoscale devices. The measurement of electrical properties and electronic states of individual nanocrystals is enabled by the associated capability of probing local electronic structures with scanning tunneling microscopy (STS).[103]

Individual atoms of a surface can be resolved by STM under ideal circumstances, which allow the nanocrystals to be located in the topography mode. Current-voltage (I-V) and differential conductance-voltage (dI/dV) measurements of individual nanocrystals can be subsequently acquired in the STS configuration by positioning of the tip above a single nanocrystal to form a substrate/dot/tip double-barrier tunnel junction (DBTJ). As shown in Fig. 2.7, the tip/dot and dot/substrate barriers are represented by the capacitances $C_{tip/dot}$ and $C_{dot/sub}$ respectively..[35,104] The current $J_{tip/dot}$ and $J_{dot/sub}$ correspond to single electron tunneling.

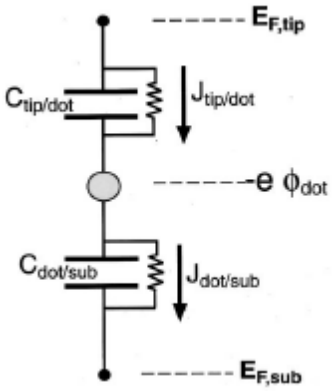


Fig. 2.7 Equivalent circuit corresponding to the double-barrier tunnel junction (DBTJ).(Reprinted from Ref [90])[105]

The electronic structure properties of the nanocrystals can be studied from the tunneling spectra. The spectra obtained by probing individual nanocrystals typically show a zero conductivity gap with dI/dV=0, which is related to the energies of the first conduction and first valence band level, which forms. the band gap of the nanocrystal.[106,107] An increase in the energy band gap values provides indication on size quantization of the electronic structure related to decreasing size of the nanocrystals. Resonant tunneling of electrons from the tip to the substrate via discrete unoccupied electron level (conduction band) of the nanocrystal[34,108] can also be observed from the onset of dI/dV > 0, as the tip Fermi level scans over the energy

level of the nanocrystal, as shown in Fig. 2.8. The resonant peaks featured from the tunneling spectra correspond to tunneling of carriers through discrete electron levels of the nanocrystal conduction band at positive substrate bias and levels of the valence band at negative bias. When more electrons get injected into the nanocrystals, Coulomb interactions between the injected electrons leads to additional contribution to the charging energy, which can be observed from the energy level spacing in the conduction and valence bands.[109]

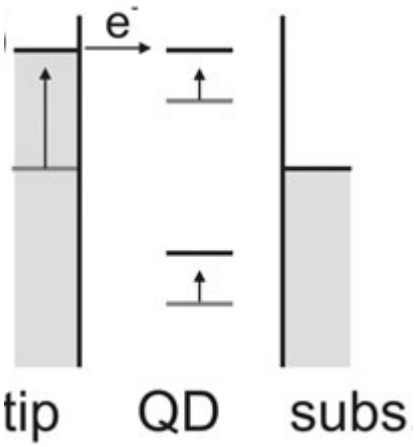


Fig. 2.8 Schematic illustration of the tunnelling of electron from the tip to substrate via unoccupied conduction level at positive substrate bias (Reprinted from Ref [94]). [110]

2.5 Optimization Strategies for Enhanced Memory Properties

Although charge trap memory devices utilizing nitride layer or nanocrystals provide solution for further scaling, the trade-off between data retention and P/E charactertistics remains an important issue. In this regard, different optimization strategies have been introduced to obtain a better trade-off characteristic. The first approach involves the manipulation of charge trap properties by introducing deep surface states at the nanocrystal surface to provide retention improvement and enlarged memory window.[111-113] The similar concept has been applied by forming an engineered transition layer with a graded dielectric layer formed between the Si

nanocrystals and SiO_2 matrix.[114-116] Recent advances have also demonstrated the enhancement of retention characteristics using a double tunnel junction memory with the charge leakage minimized by forming a layer of small size nanocrystals under an upper stack of nanocrystal charge storage layer. Further extension to multistacked nanocrystal memories allows for multilevel charge storage.[117] Large increase in storage densities>200 Gb is anticipated associated with the development of double nanocrystal layer technology, which allows further scaling to the 10nm generation, as shown in Fig. 2.9. Efforts on achieving adequate control on the nanocrystal properties have also been carried out using different templated self-assembly approach, including PS-PMMA diblock compolymer[118,119] and protein-mediated molecular chaperonin array[120] to manipulate the size and distribution of the nanocrystals.[114-116] The utilization of polymer-based materials provides a potential route for the formation of a uniform self-assembled array of nanocrystals. However, the nanocrystal size is limited by the pattern transfer from the pore diameter of 20nm, and the density is limited to the total pore density of ~ $6 \times 10^{10} cm^{-2}$ of the porous PS films.[121,122] Large-scale fabrication of high density arrays of nanocrystals with sizes below 20nm scale remains a challenge for this approach. On the other hand, the protein-mediated assembly allows a desirable nanocrystal size, which is determined by central cavity of the molecular lattice.[113] However, much research has to be done to control and manipulate the template in an efficient way.

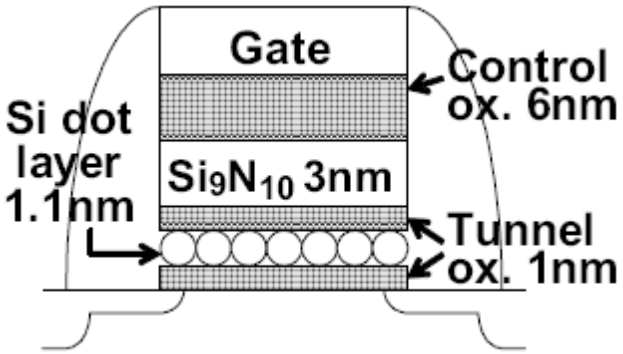


Fig. 2.9 A double tunnel layer technology introduced by Toshiba (Reprinted from Ref [98]). [116-118]

The second approach involves band gap engineering of the tunnel barrier such that the injection current density is enhanced at high electric fields, with the retention properties maintained at low electric fields.[123,124] The concept of VARIOT (variable oxide thickness) structure tunnel barrier was introduced to provide enhanced P/E efficiency[125] following the pioneering work from Baik et. al using $Si_3N_4/SiO_2/Si_3N_4$ barrier. Hence different layered barrier structure has been demonstrated, including tunnel oxide comprising SiO_2/HfO_2 bi-layer tunnel dielectric[126-129] and $Al_2O_3/HfO_2/Al_2O_3$ tri-layer tunnel oxide,[130] which provides improvement in the non-volatile memory characteristics. However, this approach requires the realization of a good interface quality between the multi-layer dielectric and the minimization of traps in the dielectric films to avoid performance degradation.

The introduction of advanced device architectures constitutes another approach for enhanced memory performance. A better electrostatic control can be achieved with the modification of channel structure, i.e the optimization of the channel W/L aspect ratio.[130,131] A better control of the Vt_h shift can be achieved by reducing the channel width and increasing the channel length.[132] Dramatically improved V_{th} window, P/E efficiency, retention and endurance characteristics has been demonstrated with the

introduction of a double gate structure[133] and FinFET architecture.[134] This is related to the effective suppression of short channel effects due to the gate-to-channel control from more than one side, which effectively improves the I_{on}/I_{off} ratio. Fig. 2.8 shows a double gate architecture with nanocrystals embedded in both side gate oxide layers. The body potential can be favorably modulated, as the electrons stored in the nanocrystals effectively prevent the emission of electrons from the nanocrystals on the other side. This in turn allows an improved retention and endurance with lower P/E voltage.

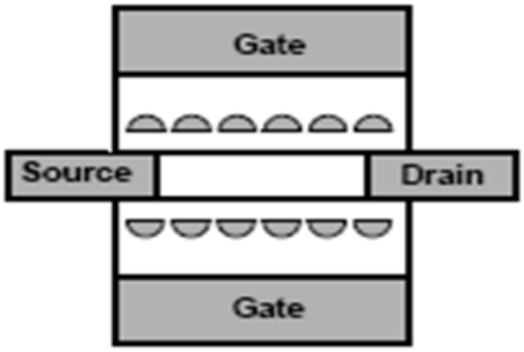


Fig. 2.10 A schematic cross section of a double gate nanocrystal memory device fabricated on a silicon on insulator (SOI) substrate.

However, the body thickness variation and process complexity results in process and device yield issues, which pose difficulties on the realization of the device architectures. The formation of monodisperse quasi-1D single-walled carbon nanotubes (CNTs) as the channel is an attractive solution to minimize body thickness variation of ultrathin semiconductor body on insulator in field effect transistor (FET) devices [135] The narrow channel width of the CNT provides an improved device electrostatics and minimized short channel effect of the device.[135] Significant hysteresis has been observed in the gate transfer characteristics of CNT-based memory devices, which is related to mobile ions [32] or charge traps within the oxide

layer [31], oxygen-related defects near the nanotube [136], nitride and nanoparticle-related trapping sites [54,137-139], and water molecules absorbed on the surface of the nanotubes [140]. Although the observed hysteresis opens up the possibility of memory device applications, there is lack of study on the trap properties and reliability, which significantly impacts the CNT memory behavior and device functionality. Different device architectures have been employed for CNT-based memory device fabrication, including top-gate and bottom-gate structures, with single nanotube, aligned arrays, or random networks of CNT channels. The top-gate structure allows efficient switching at low operation voltage, but the devices generally exhibit a relatively small V_{th} window, which remains a limitation for memory device performance [72]. On the other hand, bottom-gate devices generally require a relatively high operating voltage for the observation of a large memory window [9,141]. In order to obtain a large I_{on}/I_{off} ratio between the two logical states, "1" and "0", for flash memory device operation, it is important to study the charge transport and injection properties to achieve a large memory window and current rectification under low operation voltage. Several studies suggest that carrier transport in carbon nanotube field effect transistor CNTFET devices is dominated by Schottky tunneling barrier between the source/drain and channel.[135] Hence much work has been carried out on Schottky contact modification of CNTFET devices for carrier transport optimization. The two main approaches include the use of multiple gates for independent control of the source and drain contacts [142] and chemical doping of the nanotubes by adsorption of atoms or molecules [143]. The first approach requires adequate control on the patterning and alignment with multiple gates, while the second approach requires substantial bonding of the atoms/molecules on the CNT surface, which suffers from competing effects from atmospheric adsorbates. Further efforts are needed to obtain optimal

CNT memory device performance with a large memory window and low turn-on voltage without increasing the off-current.

2.6 Summary

In summary, this chapter introduces the background principles of nanocrystal memory device operation, which provides insights on the effect of nanocrystal size and density parameters on the device performance. Recent developments and existing challenges of nanocrystal memories have been reviewed, including the integration of high-k dielectrics for improved device performance. Studies on different techniques for the formation of nanocrystals were discussed, with an emphasis on the pulsed laser deposition and colloidal synthesis technique. Further understanding on the carrier transport property study of nanocrystals was highlighted, with STM characterization introduced as a useful tool for probing nanoscale electrical properties of the nanocrystals. Lastly, current efforts and strategies were highlighted, which provide the direction for enhancing the performance of nanocrystal memory devices.

CHAPTER 3 EXPERIMENTAL PROCEDURES

3.1 Material Selection and Device Design Considerations

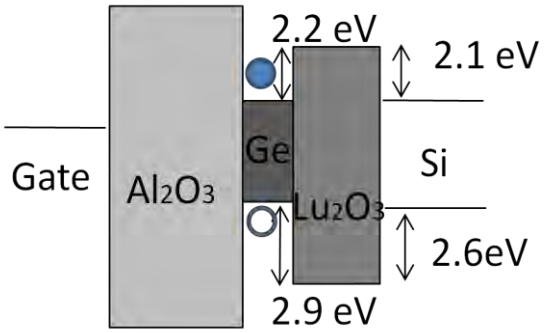
This work focuses on the integration of Ge nanocrystlas in lanthanide-based high-k dielectric, which is considered as the next generation high-k dielectric material.[144,145] The selection criteria for the high-k candidate material includes a large conduction band offset (CBO) and valence band offset (VBO) larger than 1.5 eV to meet the 10-year retention requirement, high dielectric constant, thermodynamic stability, high crystallization temperature and good interface properties with the Si substrate. In particular, Lu_2O_3 is adopted in this work due to its favourable properties with the highest lattice energy (13871 kJ/mol)[137] for better hygroscopic immunity and largest Gibbs free energy of formation, $\Delta_f G^o$ (1789.0 kJ/mol) among other lanthanide oxides,[146-148] as shown in Table 3.1

.

Table 3.1 Gibbs free energy of formation for different candidate gate oxide materials

Compound	***Gibbs Free Energy of Formation, $\Delta_f G^o$ (kJmol^{-1}) at 298K***
Lu_2O_3	-1789
SiO_2	-856.3
HfO_2	-1088.2
Al_2O_3	-1582.3
La_2O_3	-1705.8

The thermodynamical stability of the high-k dielectric is anticipated to provide a good quality interface, and facilitate the formation of stable Ge nanocrystals in the dielectric matrix. In terms of electrical properties, it has a relatively large bandgap (~5.8 eV) and conduction band offset (2.1 eV) among other candidate high-k dielectrics,[54,137,138,148] which is anticipated to give a low leakage current characteristic, besides having a moderately high dielectric permittivity. On the other hand, Al_2O_3 was chosen as the control dielectric to prevent the degradation of electrical properties due to moisture hygroscopic properties of Lu_2O_3. The high crystallization temperature and large band gap of properties of Al_2O_3 provide an effective blocking oxide, which is expected to reduce the charge leakage between the nanocrystals and control gate. The schematic illustration of the energy band diagram of the memory structure with Ge nanocrystals embedded in high-k dielectrics is shown in Fig. 3.1.1.



(a)

Fig. 3.1.1 Schematic energy band diagram of the Ge nanocrystal memory structure in this work.

Fig. 3.1.2 shows the illustration of band diagram during the operation of the Ge nanocrystal memory device with Lu_2O_3 high-k tunneling dielectric and Al_2O_3 control dielectric. The small electron barrier height of Lu_2O_3 allows an asymmetry in charge transport achieved between writing and retention state through different shape of the

barrier, i.e. triangle barrier in the write state and trapezoidal barrier in the retention state. Hence a lower write voltage is achieved with a low electron barrier height for F-N tunnelling, while the retention time is strongly limited by reduced direct tunnelling of charges through a thick barrier.

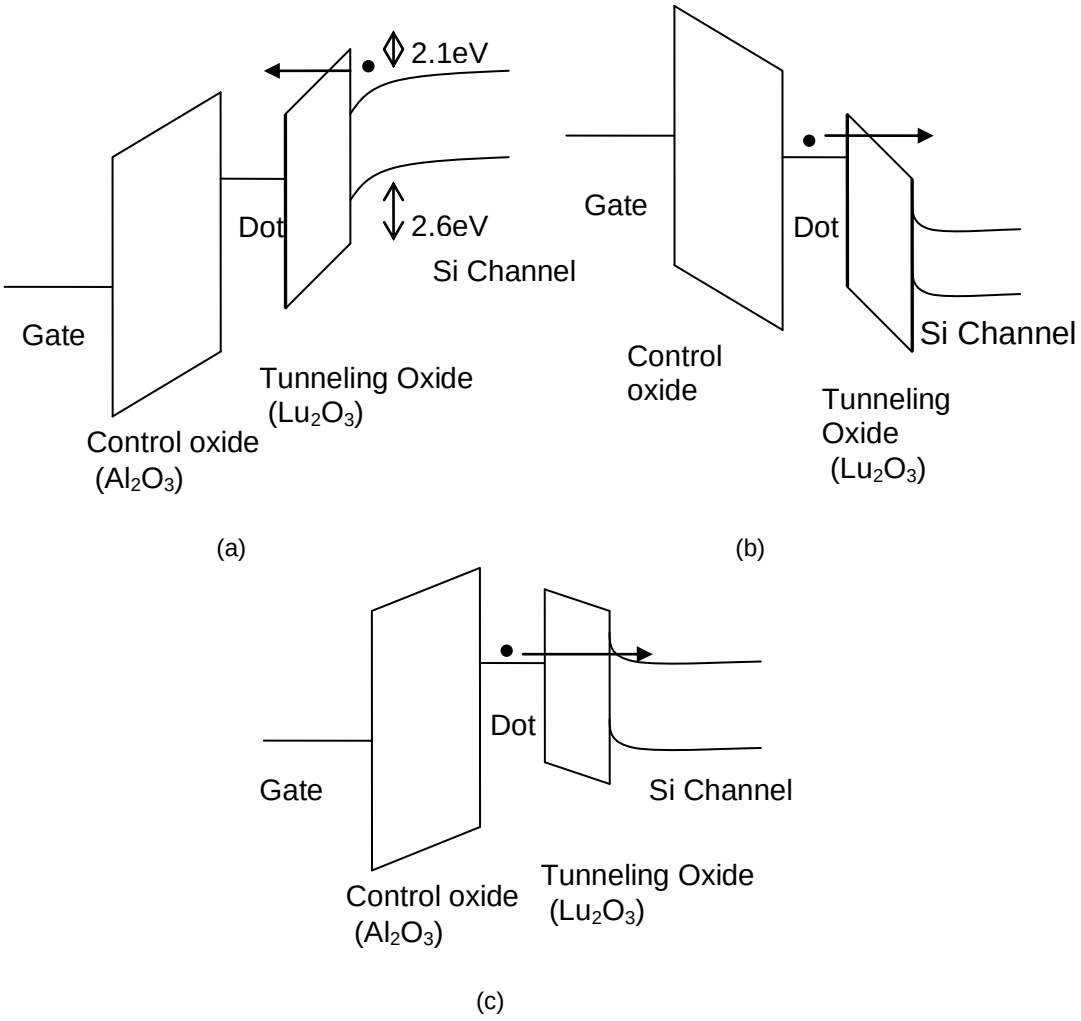


Fig. 3.1.2 Schematic band diagram of a nanocrystal memory structure with Lu_2O_3 as the tunneling dielectric and Al_2O_3 as the control dielectric under (a) write (positive applied bias) (b) erase (negative applied bias) and (c) retention state.

3.2 Formation of Ge Nanocrystals by Pulsed Laser Deposition and Characterization of Memory Capacitor Devices

In this work, a simple approach was utilized for the formation of nanocrystals embedded in amorphous Lu_2O_3 high-k dielectric matrix by the modification of the pulsed laser deposition (PLD) technique with a rotating target. A KrF excimer pulsed laser with a wavelength of 248 nm was used to ablate the target in an ultrahigh vacuum chamber. The laser energy density is approximately 1.5 J/cm^2, with the pulse repetition rate and pulse duration maintained at 5 Hz and 10 ns. Fig. 3.2.1 shows the schematic setup of the pulsed laser deposition system with pulses of laser light focused on the surface of the target for ablation and subsequent deposition of the target species on the substrate normal to the target surface.

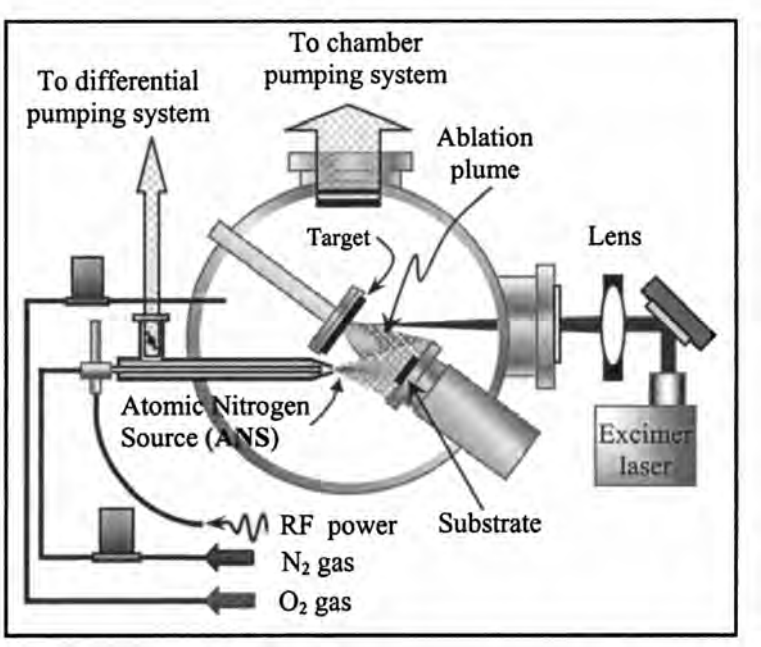


Fig. 3.2.1 Schematic diagram of the pulsed laser deposition system

The target to be laser ablated was first prepared from a high purity (99.999%) round Lu_2O_3 target (diameter D=25 mm) and a small Ge square wafer plate (about 3 mm in length). As shown in Fig. 3.2.2, the Ge plate was glued onto the surface of the Lu_2O_3

target using chemically non-reactive adhesive, making a two layer assembly with only physical, but not chemical, contact between them. During the PLD process, the center of the Lu_2O_3-Ge target assembly was set to spin slowly about its central axis and the laser beam vaporized the two component materials alternately. The Ge: Lu_2O_3 exposed area ratio during the laser ablation process is approximately 1:10.

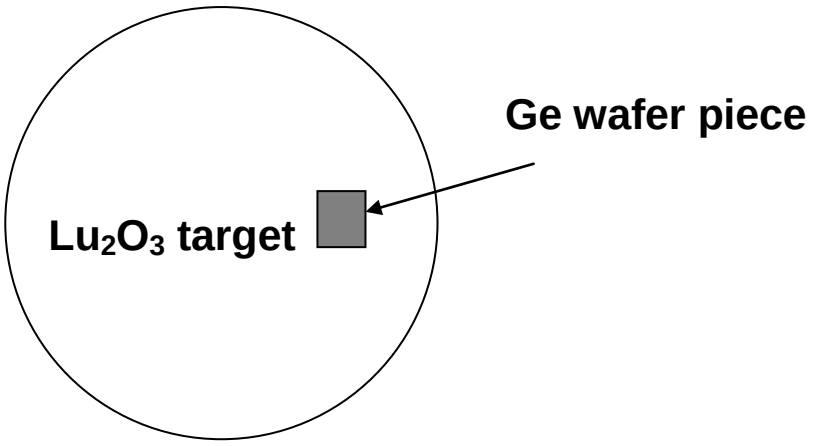


Fig. 3.2.2 Lu_2O_3-Ge target composite which allows the deposition of Ge species in Lu_2O_3 matrix by rotating the target for alternate ablation of Ge and Lu_2O_3.

The p-type (100) Si substrates were first cleaned using SC1 (10 H_2O: 1NH_4OH: 1H_2O_2) and SC2 (5H_2O: 1HCl: 1H_2O_2) pre-clean step, and then dipped in a 1% HF solution to remove the native oxide. The laser deposition was carried out in a high vacuum system (modified by Quasi-S Pte Ltd) with a background pressure of about 6×10^{-7} Torr with the target rotating at about 30 rounds/min and the substrate at room temperature. During the PLD process, for the tunneling oxide layer deposition, the target was kept stationary while allowing the laser to ablate the Lu_2O_3 for 2 minutes. Then, to form Ge nanocrystals embedded in Lu_2O_3 matrix, the target assembly was set to spin slowly about its central axis and the laser beam vaporized the two component materials alternately for 6 minutes. The deposition rate obtained from the fixed

process parameters is around 1.5 nm/min, which is expected to result in a final structure of ~3nm Lu_2O_3 tunneling oxide layer and ~9nm Ge/Lu_2O_3 layer. To form a trilayer structure for the memory device, an additional Al_2O_3 capping layer was deposited by ablating a round Al_2O_3 (99.999%) target (diameter *D*=25 mm) for 3 minutes to form ~5 nm control oxide layer. After deposition, the thin film was subjected to a rapid thermal annealing (RTA) treatment at 400°C for 60 s in nitrogen ambient. A control sample was also fabricated under the same conditions without the incorporation of Ge during deposition. The effect of varying deposition condition was further studied by modifying the target, with Ge: Lu_2O_3 exposed area ratio increased from 1:10 to 1:4.

The structural properties of the Ge nanocrystals embedded in the Lu_2O_3 matrix was examined using JEOL 2010 and JEOL 2100F microscope with 200kV accelerating voltage to capture high-resolution transmission electron microscopy (HRTEM) images. Atomic force microscopy (AFM) was also used to characterize the surface morphology of the films using Nanoscope Digital Instrument 3100.

Secondary ion mass spectroscopy (SIMS) depth profile analysis was carried out to investigate the elemental distribution of the films before and after annealing using a 1 keV Cs^+ was the primary ion source for sputtering and 25keV Ga^+ beam for analysis. SIMS is a key characterization tool commonly used to study dopant and impurity distributions in a sample. It operates using a focused primary ion beam (eg. O_2^+, Cs^+) for sputter erosion of the sample surface, resulting in the emission of secondary particles, constituting elemental ions, molecular ions and neutrals. The proper choice of primary ion beam is important in enhancing the sensitivity of SIMS, whereby O_2^+

ions are usually used for sputtering electropositive elements, while Cs^+ ions are usually used for sputtering negative ions from electronegative elements. The collected secondaty ions are than mass analyzed using a magnetic sector, quadrupole or time-of-flight mass spectrometer. The mass-to-charge spectrometry analysis gives information on the composition of the sample, with the isotope detection limit ranging from 1ppm to 1ppb.

The chemical composition of the thin films before and after anneal were studied by performing x-ray photoelectron spectroscopy (XPS) experiments. X-ray photoelectron spectroscopy (XPS), also known as electron spectroscopy for chemical analysis (ESCA), is a surface sensitive technique that provides both qualitative and quantitative surface chemical state information for the elements in the sample. XPS measurement is based on the photoelectric effect in which monochromated x-rays are irradiated onto the sample surface causing electrons to be emitted. The kinetic energy (E_k) of an emitted electron is given by:

$$E_k = h\nu - E_B - \phi \qquad (3.1)$$

where $h\nu$ is the energy of the x-ray (h is the Planck's constant and ν is the frequency of the x-ray), E_B is the binding energy and ϕ is the spectrometer workfunction. Fig. 3.2.3 shows the emission of a photoelectron ejected by an incident x-ray. By measuring E_k, the binding energy of the material can be determined based on Eq. (3.1). The element and its chemical states can thus be identified.

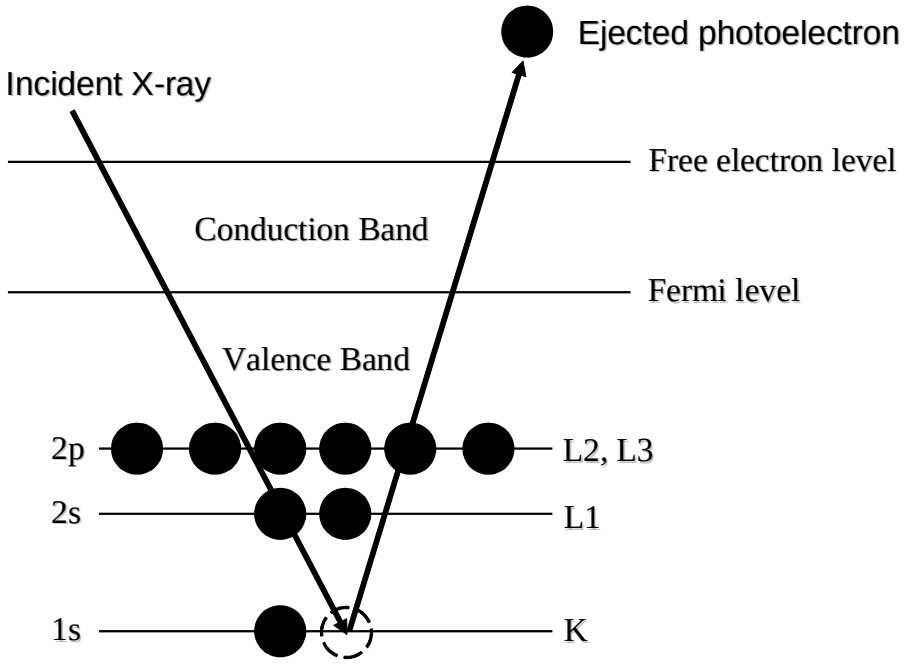


Fig. 3.2.3 Schematic illustration of an XPS emission process.

Since XPS is a surface sensitive technique capable of detecting ejected electrons from the top ten atomic layers of the sample, the analysis were performed on the films before capping layer deposition. Photoelectron spectra were collected using a PHI 5600 XPS system and Kratos Analytical AXIS HSi spectrometer with a monochromatized Al Kα X-ray source (1486.6 eV photons) at a take-off angle of 45^{o}. In order to obtain the chemical composition as a function of depth, depth profile measurement was performed using Ar^{+} ions at 0.5 keV energy on the as-deposited film. In order to eliminate crater wall effects, the measurement was acquired from a smaller region (300 x 1400 μm^2) in the centre of the sputter area (4 x 4 mm^2). Zalar rotation was used to minimize roughening of the samples caused by ion bombardment.

The surface atomic topography of the annealed sample was also characterized using scanning tunnelling microscope (STM) coupled to an ultra-high vacuum (UHV)

chamber at a pressure level of ~10^{-10} mbar. Under the topography mode, the sample surface was scanned at room temperature using a chemically treated tungsten tip at a sample bias voltage, V_s of +3 V and a set point tunnelling current of 0.1 nA. A feedback circuit was used to maintain a constant tunnelling current by adjusting the tip-surface separation distance. In order to allow sufficient tunnelling current detection, the measurement was performed on a thinner film stack with a tunnel barrier of ~2 nm and a nanocrystal layer of ~5 nm, as shown in Fig. 3.2.4. In order to study the localized electrical properties of the nanocrystals, current imaging tunnelling spectroscopy (CITS) technique was performed with the feedback circuit disabled after the preset tunnelling current was achieved, followed by bias voltage sweep to obtain the local current-voltage (I-V) characteristics. The IV characteristic at the scanned area (128x128 pixel) was mapped simultaneously during the topographic imaging, which allows the observation of local conductivity variation above the nanocrystals and dielectric regions. The I-V and differential conductance, dI/dV curves can be subsequently extracted from different locations of interest.

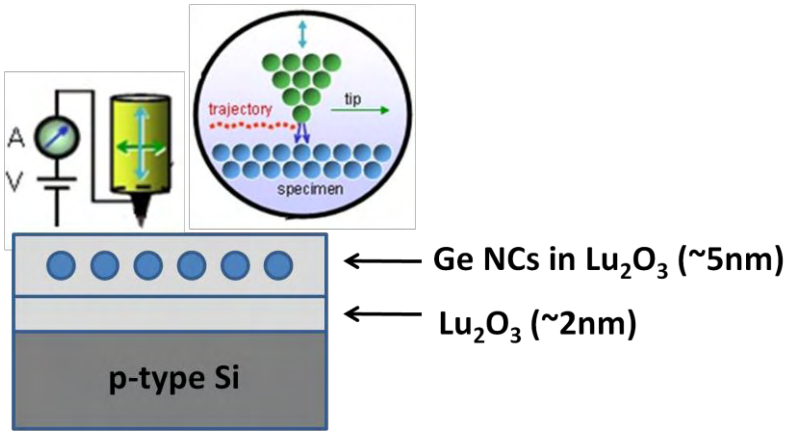


Fig. 3.2.4 STM measurement on the thin film stack with Ge nanocrystals embedded in Lu_2O_3, measured at a constant tunnelling current by adjusting the separation between sample surface and tungsten tip.

3.3 Study and Optimization on Ge Nanocrystal Memory Device Functionality

In the approach to achieve the formation of self-aligned graded barrier structure, a high anneal temperature of 800 ^{o}C was employed for thermally-induced intermixing of the oxide components. The dielectric film stack comprising ~3 nm Lu_2O_3 tunneling oxide layer, ~9 nm Lu_2O_3 Ge/Lu_2O_3 layer and ~5 nm Al_2O_3 capping layer deposited using PLD technique was subjected to RTA at 800 ^{o}C for 60s in N_2 ambient. Cross-sectional TEM, SIMS and Rutherford backscattering spectra (RBS) of the 800 ^{o}C annealed dielectric stack were used to characterize the formation of compositionally graded dielectric stack after the annealing treatment. The RBS spectra were obtained for the film compositional analysis using 650 keV He^{+} ions at a scattering angle of 65^{o} and an incident angle of 60^{o}.

Metal-insulator-semiconductor (MIS) memory capacitor structures were fabricated from the as-deposited, annealed samples and control sample without nanocrystals, as shown in Fig. 3.3.1. Au top electrodes were evaporated using a shadow mask technique, and backside Ohmic contact was formed after removing the native SiO_2 on the wafer backside with 1% diluted HF. Capacitance-voltage (C-V) and (C-t) measurements were performed at room temperature using HP4284A precision LCR meter under a measurement frequency of 100 kHz and test signal of 50 mV_{rms}, while current-voltage measurements (I-V) were performed using Keithley 4200-SCS semiconductor characterization system. The program/erase cycling (P/E) behavior was measured by applying +/-4V, 100ms gate voltage pulses followed by flatband voltage measurement up to 10^5 P/E cycles.

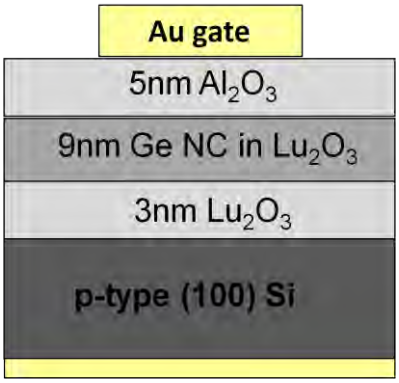


Fig. 3.3.1 Schematic illustration of the memory capacitor device with Ge nanocrystals embedded in Lu_2O_3 high-k dielectric.

In order to study the effect of dielectric matrix on the charge storage behaviour of the memory device, a dielectric film stack comprising Ge nanocrystals embedded in HfO_2 was deposited using PLD technique under the same conditions, followed by RTA at 400 ^oC and 800 ^oC for 60 s in N_2 ambient. XPS spectra of Ge 3d core level for the dielectric films after annealing at 400 ^oC and 800 ^oC were collected for chemical state analysis. MIS memory capacitor structures were fabricated from the samples after depositing ~8 nm HfO_2 control dielectric for C-V and I-V characterization, as shown in Fig. 3.3.2.

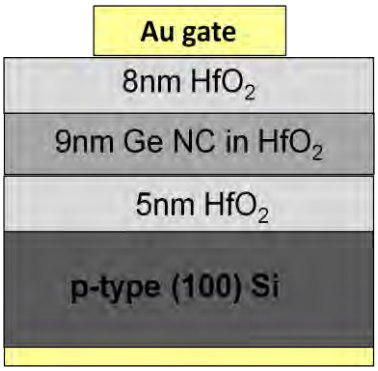


Fig. 3.3.2 Schematic illustration of the memory capacitor device with Ge nanocrystals embedded in HfO_2 high-k dielectric.

3.4 Self-Assembly and Chemical Synthesis of Ge Nanocrystals

The colloidal Ge nanocrystals were synthesized using a wet chemical reduction technique performed at room temperature and pressure in N_2 ambient. The synthesis mechanism is based on the reduction of germanium tetrachloride, $GeCl_4$ (99%) by hydrazine hydrate, $N_2H_4{\cdot}H_2O$ (64.5%) in an inert tertrahydrofuran, THF (99%) solvent. First, the $GeCl_4$ precursor was pipetted into a beaker with inert THF solvent to form the precursor solution. Next, reducing agent, $N_2H_4{\cdot}H_2O$ was pipetted into a three-necked flask uniformly mixed with THF solvent and octanol as the capping agent to form the reducing solution. The precursor solution was introduced drop-wise into the three-necked flask after powering up the ultrasonic bath. The process was allowed to proceed for 30 min to ensure complete reaction. Fig.3.4.1 shows the material resources and experiment set up for Ge colloid synthesis.

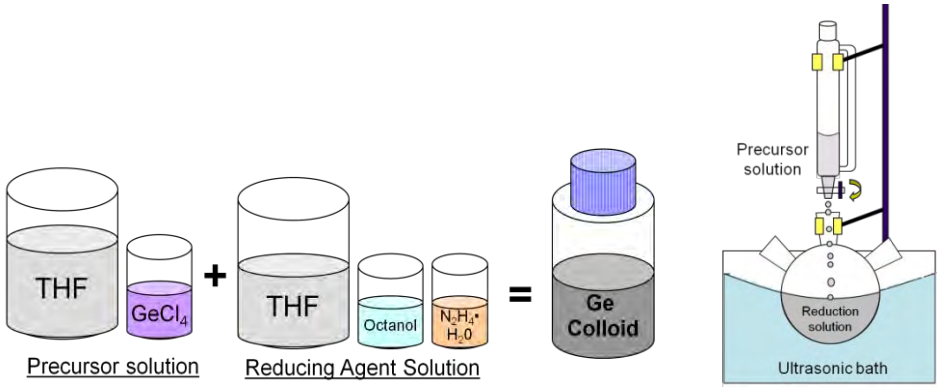


Fig. 3.4.1 Schematic illustration of the material preparation and equipment set up for colloidal Ge synthesis

Colloidal Ge solution with different concentration was synthesized by varying the volume of $GeCl_4$ and $N_2H_4{\cdot}H_2O$, while the volume of THF and octanol were remained constant. Table 3.2 shows the synthesis condition for different concentration of

colloidal solution. The chemical reaction involved in the reduction process is given by the equation

$$GeCl_4 + H_2N_4{\bullet}H_2O \rightarrow Ge + 4HCl + 2H_2O + N_2\uparrow \quad (3.2)$$

Table 3.2: Synthesis condition for different concentration of colloidal Ge solution

	Concentration of Ge Colloid	
	1.85mM	**1.1mM**
Part A: Precursor solution		
1. $GeCl_4$ (□l)	29.1	17.3
2. THF (ml)	100	100
Part B: Reducing agent solution		
1. $H_2N_4{\bullet}H_2O$ (□l)	36.3	21.6
2. Octanol (ml)	5	5
3. THF (ml)	30	30

P-type Si wafers with ~2 nm thermally grown oxide and 5nm atomic layer deposited HfO_2 were first prepared by immersing in SC1 solution (H_2O_2: NH_4OH: H_2O = 1:1:10) at 70 °C for 15 minutes to remove any organic contaminants and provide a hydroxylated surface for chemical functionalization. For chemical modification of the oxide surface, the substrates were blow-dried and immersed in absolute ethanol solution with 5% (3-aminopropyl) triethoxysilane (APTES) for 1 hour in the glove box. After that, the APTES-modified substrates were rinsed thoroughly with ethanol and de-ionized water (DI H_2O) to remove the loosely bound molecule successively before nitrogen blow-drying. The substrates were subsequently baked in vacuum oven at 120 ^oC for 30 minutes to complete the Si-O bond formation, as illustrated in Fig. 3.4.2.

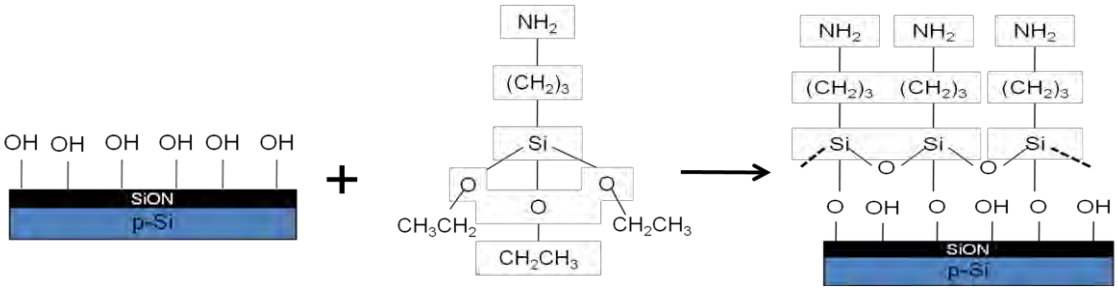


Fig. 3.4.2 Schematic illustration of amino-silanization process of the hydroxylated oxide surface.

The substrates with and without chemical modification were subsequently drop-casted with the colloidal solution of Ge nanocrystals and left in fumehood for 15 minutes to promote attachment of the nanocrystals. Lastly, the substrates were cleaned by successive rinsing with isopropanol (IPA) and DI H_2O to remove residuals followed by nitrogen blow dry.

The structural properties of the nanocrystals were studied using high-resolution transmission electron miscroscopy (HRTEM) by dipping the carbon-coated copper grid in the colloidal solution. The surface chemistry of the as-synthesized nanocrystals was further characterized using the fourier transform infrared (FTIR) spectroscopy technique. Attenuated Total Reflection, ATR-FTIR scan was performed from the wave number 600 to 4000 cm^{-1}. The attenuated energy of the evanescent wave due to the energy absorption from the sample is detected for the spectrum generation. Contact angle measurement was used to study successful silanization of the oxide surface using a FTA 100 series contact angle measurement system equipped with a charged coupled device (CCD) camera to determine the wettability of the surface. DI water was used as the spreading agent, and the shape of the liquid droplet on the oxide surface was described by the contact angle, i.e. the angle between the tangent line from the droplet and the solid surface. The chemical composition of the Ge

nanocrystals attached to the modified oxide substrates were investigated by performing XPS analysis on the oxide samples drop-casted with Ge colloidal solution. The chemical binding interaction between the colloidal Ge nanocrystals and the APTES-modified oxide surface was further studied by performing FTIR analysis. AFM was also used to characterize the morphology of the Ge nanocrystals deposited on the oxide surface before and after chemical treatment using Nanoscope Digital Instrument 3100.

For electrical characterization of the memory behaviour, metal-insulator-semiconductor (MIS) memory capacitor structures were fabricated from the samples with different concentration of colloidal Ge nanocrystal dispersed on the Si substrates with ~2 nm thermally grown SiO_2 as the tunnel oxide. ~10 nm Al_2O_3 was deposited after nanocrystal deposition using PLD technique to form the top control dielectric. Control sample was fabricated under the same condition except for the introduction of Ge nanocrystals. Au top electrodes were evaporated using a shadow mask technique, and backside contact was formed after native oxide removal. C-V measurements were performed at room temperature using HP4284A precision LCR meter at a frequency of 100 kHz to study the charge storage behaviour of the MIS capacitor devices.

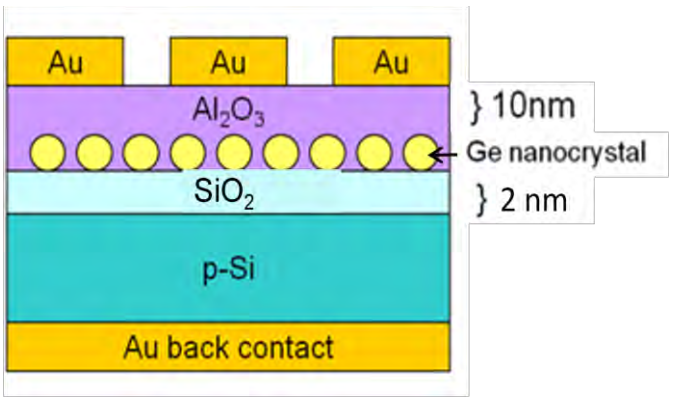


Fig. 3.4.3 Schematic illustration of the colloidal Ge nanocrystal memory capacitor device.

In order to demonstrate the feasibility of integrating the colloidal synthesis methodology and self-assembly technique with high-k gate dielectrics for memory device application, MIS memory capacitor devices were fabricated from the samples with colloidal Ge nanocrystal dispersed on the Si substrates with ~5 nm atomic layer deposited HfO_2 with and without APTES functionalization. ~10 nm HfO_2 was deposited after nanocrystal deposition using PLD technique to form the top control dielectric. After the formation of Au top and bottom electrodes, bi-directional C-V sweep measurements were performed at room temperature using HP4284A precision LCR meter at a frequency of 100 kHz.

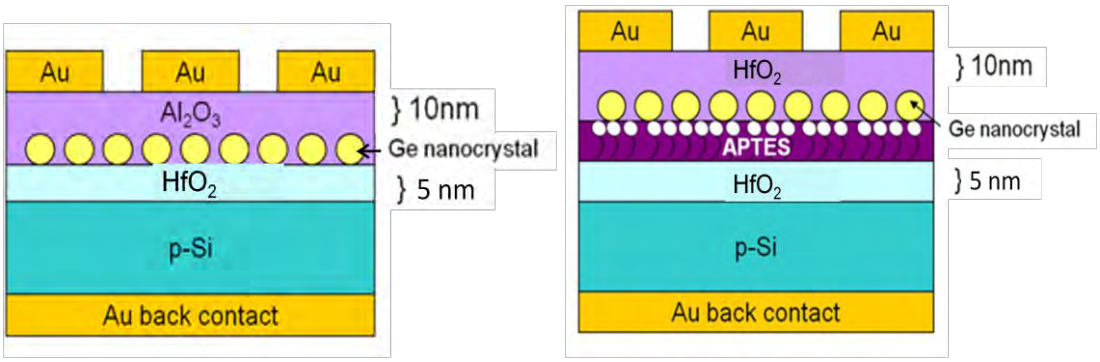


Fig. 3.4.4 Schematic illustration of the memory capacitor devices fabricated from the colloidal Ge nanocrystal deposited on the substrates with and without APTES functionalization.

3.5 CNT-based Ge Nanocrystal Memory

Single-walled carbon nanotubes (SWCNTs) were grown using chemical vapor deposition (CVD) technique using Co-MCM-41 catalysts to form narrow chirality distribution at 0.8 nm average diameter,[146] which allows a comprehensive study of

different devices with minimal deviation. (7,5) tubes are the main species identified in the CNT sample. Bottom gate carbon nanotube (CNT)-based transistor devices were built on heavily-doped p-type Si wafers with a surface resistivity of 0.01 Ωcm after standard Radio Corporation of America (RCA) clean followed by HF (1%) native oxide removal.

A 30-nm bottom HfO_2 high-k dielectric was grown on the substrates using atomic layer deposition (ALD) at 250^{o}C with hafnium tetrachloride ($HfCl_4$) as the metal source and H_2O as the oxygen source. In order to fabricate an additional charge trap layer with Ge nanocrystals, a 248 nm KrF pulsed laser with a fluence of 1.5 J/cm^2 and a frequency of 5 Hz was used to ablate the Ge-HfO_2 target assembly prepared from a high-purity (99.999%) round HfO_2 target (diameter D = 25 mm) and a small Ge square plate wafer (about 3 mm in length) in a two-layer assembly. The laser deposition was carried out with a background pressure of about 6 x 10^{-7} Torr and the target rotating at about 30 revolutions/min and the substrate at room temperature. The target assembly was set to spin slowly about its central axis and the laser beam vaporized the two component materials alternately for 8 min to form ~8 nm HfO_2 layer with embedded Ge nanocrystals. Next, the target was kept stationary to allow laser ablation of HfO_2 for 5 min to form a ~5nm thick tunnel oxide layer. After the deposition process, the dielectric film stack was subjected to rapid thermal annealing at 400^{o}C for 60 s in N_2 ambient. The 30 nm HfO_2 control sample grown by ALD was subjected to similar annealing conditions for comparison.

Cr (10 nm) / Au (100 nm) layers were sputtered on top of the dielectric film stack, and source / drain (S/D) pads were patterned using photolithography followed by

subsequent lift-off process. Purified CNTs dispersed in 1 wt% sodium dodecyl sulfate (SDS) H_2O solution with 0.01 mg/ml concentration were drop-casted onto the patterned substrates to form the channel connecting the S/D pads. After allowing the CNT solution to evaporate for 15 min, the substrates were rinsed with DI water and were blow dried with N_2. The distribution of CNTs on the substrates was characterized using AFM and the formation of Ge nanocrystals was studied using cross-sectional TEM characterization. The transistor and memory behavior was investigated by performing drain current (I_{ds}) vs. gate voltage (V_{gs}) measurements at temperatures from 298 K to 400 K using an HP4156C precision semiconductor parameter analyzer attached to a Temptronic temperature controller in both ambient and vacuum conditions. The charging behavior was further studied by performing I_{ds}-V_{gs} sweeps after applying electrical pulse stress on the device at increasing voltages. Charge retention behavior was investigated by monitoring the transient drain current, i.e. I_{ds}-t measurement after performing positive and negative bias charging of the device at temperatures from 298 K to 400 K. Device endurance characteristics were studied by performing several write and erase pulse cycle measurements at a pulse width of 1s followed by I_{ds}-V_{gs} sweeps for threshold voltage extraction at a current level of 1 nA.

CHAPTER 4 Formation and Evolution of Nanocrystals by Pulsed Laser Deposition Technique

4.1 Introduction

The formation of nanocrystals with controlled size, density and distribution which impacts the device characteristics is required for successful implementation of nanocrystal memory device. However, nanocrystal fabrication techniques reported to date have not address the issue of the fluctuations in electrical characteristics due to the spread in nanocrystal size and density from one device to the other. Thus, an understanding on the nanocrystal formation mechanism is essential to achieve the desired properties. This chapter focuses on a low thermal budget process to obtain adequate size control of nanocrystals, with less severe nanocrystal growth as compared to other high temperature nanocrystal fabrication techniquesIn this work, a simple approach was utilized for the formation of Ge nanocrystals embedded in lanthanide-based high-k dielectric using pulsed laser deposition followed by rapid thermal annealing in N_2 ambient. Structural characterization was carried out to study the nanocrystal formation mechanism, including transmission electron microscopy (HRTEM), secondary ion mass spectroscopy (SIMS) and x-ray photoelectron spectroscopy (XPS) analysis. The experimental results elucidate the role of chemical interaction between Ge oxides and the dielectric host matrix on the nanocrystal formation process during annealing. Further study on the variation of deposition parameter provides understanding on the factors affecting the nanocrystal properties, whereby the nanocrystal density is determined by the Ge content, and the size determined by the nucleation process during annealing. This offers extended possibilities for device optimization to achieve enhanced nanocrystal density with simultaneous control on size and spatial distribution. Size-dependent properties of the

nanocrystals and localized conductance modulation due to charge confinement of nanocrystals were also demonstrated by performing localized charge transport study.

4.2 TEM and SIMS Characterization

The evolution of Ge nanocrystals before and after anneal was characterized by HRTEM using JEOL microscope. Fig. 4.2.1 (a) shows the planar TEM image of the as-deposited film, with some dark contrast regions associated with the presence of nanoparticles in the oxide matrix. Small nanoparticles with 2-3 nm dimension and an areal density of 7 x 10^9 cm^{-2} were observed from the image. The nanoparticle size is close to the estimated critical size for nucleation of Ge nanocrystals about 2 nm.[148] However, lattice fringes are not clearly resolved in the dark areas, which could be related to the amorphous state or lattice instability in very small crystallites.[147] Fig. 4.2.1 (b) shows the planar TEM image of the film after post-deposition anneal (PDA) at 400 ^oC, with a large number of nanocrystals observed to precipitate densely in the amorphous Lu_2O_3 matrix. The annealing treatment resulted in an increased nanocrystal density of 7 x $10^{11}cm^{-2}$ and larger crystallites with a mean size of 6nm. This shows that the annealing treatment plays an important role on the formation of nanocrystals. The energy provided by annealing allows self-organization of the amorphous-like particles into more compact nanocrystals due to short-ranged diffusion of Ge atoms. The simultaneous increase in nanocrystal size and density achieved is favorable to ensure sufficient amount of charge storage for detectable threshold voltage shift of the memory device.[132] The nanocrystal size and density obtained is close to the optimal size and density requirements of ~5 nm and 10^{12} cm^{-2} anticipated for ideal non-volatile memory (NVM) operation.[149] In addition, the

nanocrystals were observed to be well-isolated by the amorphous high-k dielectric, which is important to limit charge tunnelling between crystallites.

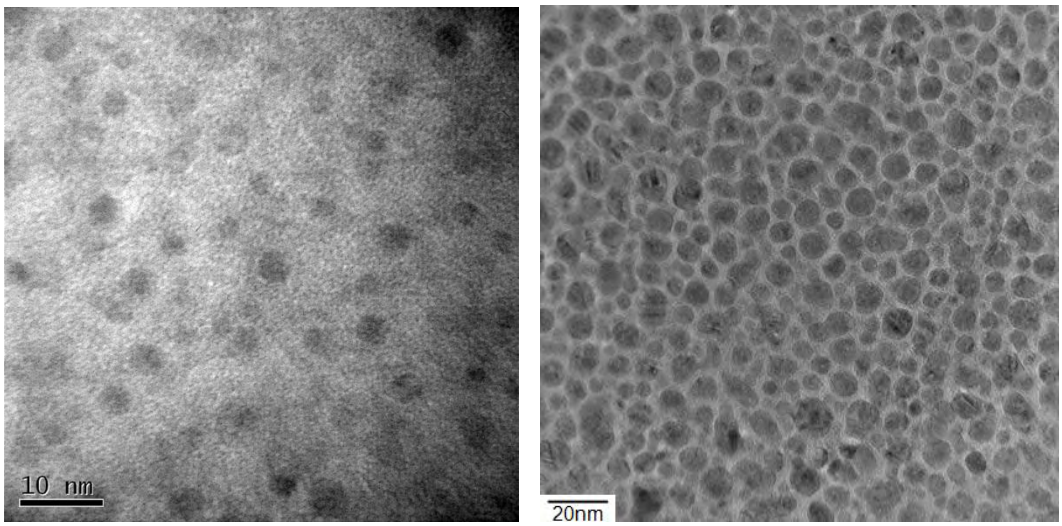


Fig 4.2.1 Planar TEM image of (a) as-deposited film and (b) 400 ^{o}C annealed film with Ge nanocrystals embedded in amorphous Lu_2O_3 dielectric matrix.

The structural properties of the Ge nanocrystals embedded in Lu_2O_3 matrix was examined from the cross-sectional TEM images in Fig. 4.2.2. Fig. 4.2.2 (a) shows that the Lu_2O_3 film remained amorphous after the PDA at 400 ^{o}C. The single crystalline nature of the Ge dots is evidenced from the observed lattice planes with an interplanar distance of ~0.33 nm in Fig. 4.2.2 (b), which correspond to the (111) lattice planes of bulk Ge in the diamond cubic phase. The shape of the nanocrystals is almost spherical which is favourable for NVM applications because the three-dimensional symmetry results in an effective charge confinement and physical stability from surface energy minimization.[150]

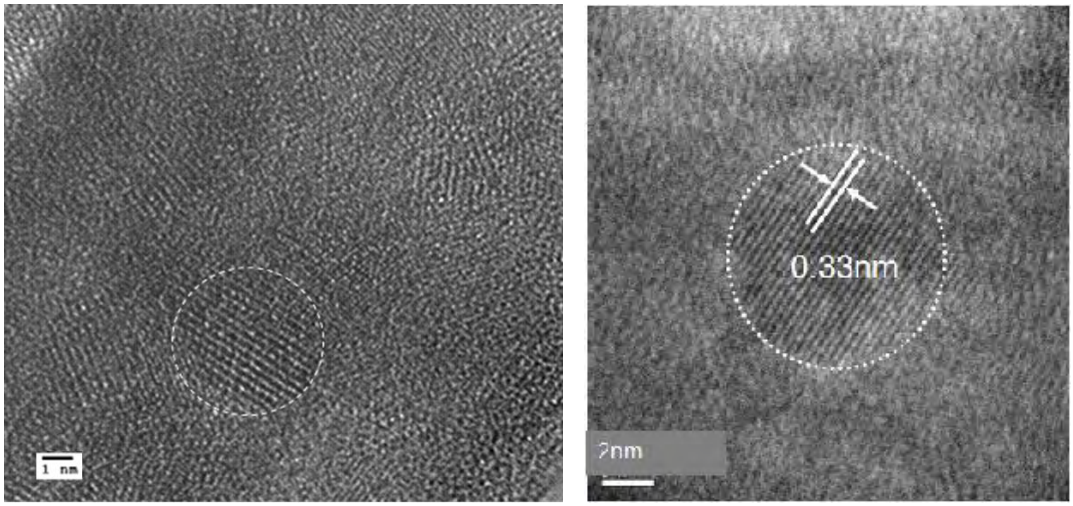


Fig 4.2.2 (a) Cross-sectional HRTEM image of the Ge nanocrystals embedded in amorphous Lu_2O_3 dielectric matrix and (b) HRTEM image of a single nanocrystal with lattice fringes observed.

Fig. 4.2.3 shows the SIMS depth profile of each element measured using a 1 keV Cs+ as the primary ion source for sputtering, plotted in the direction from the film surface to the Si substrate for the as-deposited and 400 ^{o}C annealed sample. Negligible changes were observed from the profiles after annealing, except for some slight difference in the slope of the falling edge for the Al and Ge profiles. However, the slight changes observed in the slope profiles does not provide indication on the in-diffusion of Al and Ge atoms, as tailing effects due to ion bombardment were expected to occur during the ion sputtering process.

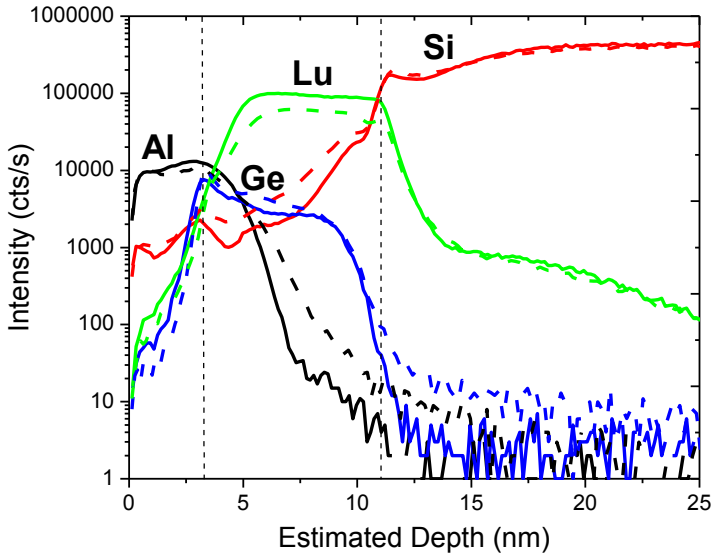


Fig 4.2.3 SIMS depth profiles of Al, Si, Ge and Lu measured as a function of depth into the Si substrate, with the solid lines plotted for the as-deposited film and dashed lines plotted for the 400°C annealed film.

The Ge atoms are well-distributed within the middle region of ~7 nm thick before and after anneal, in good agreement with the expected distribution, as illustrated in Fig. 4.2.4. In addition, both Ge profiles show the appearance of a small peak near the interface between the Lu_2O_3 and Al_2O_3 control dielectric. This suggests partial segregation and pile up of Ge atoms in the vicinity of the upper interface during the deposition process.

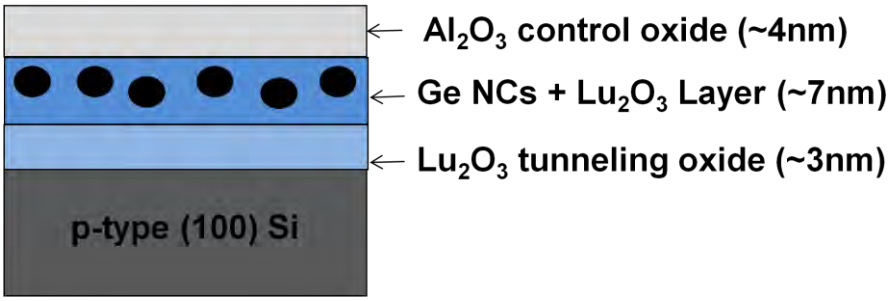


Fig 4.2.4 Schematic diagram of the high-k dielectric stack, illustrating the Ge nanocrystals distributed near the Lu_2O_3/Al_2O_3 interface due to segregation of Ge atoms during the deposition process.

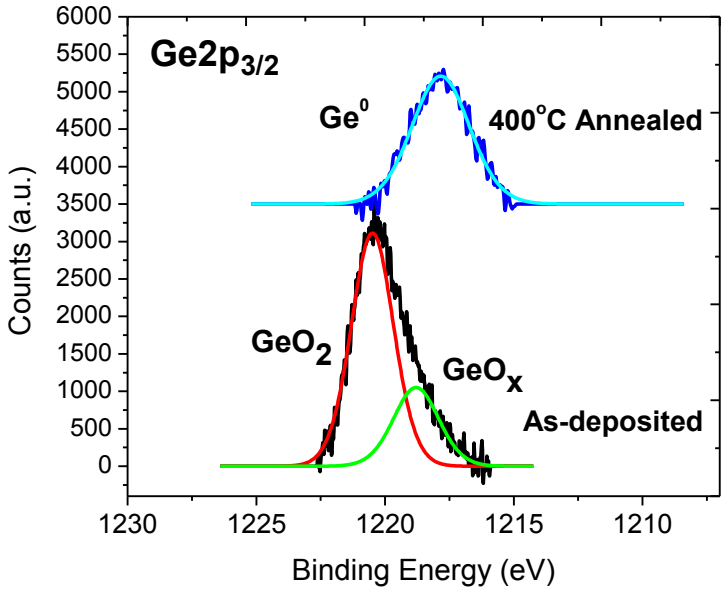
4.3 XPS Characterization

Fig. 4.3.1 (a) shows the XPS spectra of the films before and after the annealing treatment. As shown in Fig. 4.1.3 (a), the $Ge2p_{3/2}$ XPS spectra of the as-deposited sample indicates the existence of Ge in its oxidized state, with a fitted main peak at higher binding energy corresponding to GeO_2 (1220.5 eV) and a small lower binding energy peak for GeO_x (1218.8 eV). Based on the area enclosed by the peaks, quantitative analysis of the chemical state concentration obtained from the peak-fitted results indicates a large fraction of GeO_2 exists in the film. After the annealing treatment, the oxide peaks disappeared, with the Ge $2p_{3/2}$ peak shifted down to 1217.5eV, corresponding to the elemental state Ge. The results indicate a significant reduction of GeO_2 and suboxides leading to the creation of elemental Ge atoms upon annealing.

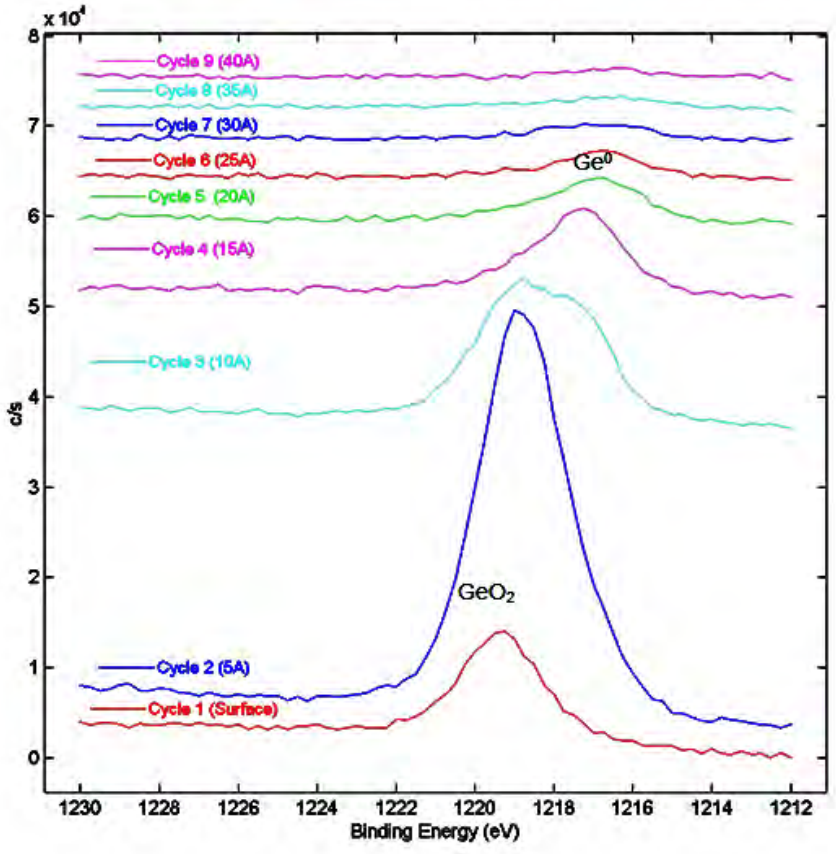
The incorporation of GeO_2 and suboxides has been observed in the films deposited by co-sputtering of Ge and SiO_2[26] as well as co-sputtering of Ge, HfO_2 and Al_2O_3 at ambient temperature.[151] Zhu et. al. also reported that Ge/Al_2O_3 thin films produced by pulsed laser deposition in vacuum environment resulted in Ge nanoparticles that are partly oxidized, with GeO_x structure formed at the interface between Ge and the Al_2O_3 matrix.[67] Besides that, the presence of GeO_x has also been observed from the Ge nanoparticles grown on HfO_2 by CVD and PVD due to the rapid oxidation of Ge atoms upon contact with the HfO_2 surface.[31,152] In the present work, it is plausible to assume that the Ge is partially oxidized during co-deposition with Lu_2O_3. This results in mixed composition in the film in the as-deposited state, constituting GeO_2, GeO_x,

Lu_2O_3 and sub-stoichiometric Lu oxides associated with oxygen deficiencies in the oxide matrix.

Fig. 4.3.1 (b) shows the XPS sputter depth profile analysis performed on the as-deposited film to provide information on the chemical state of Ge throughout the layer. It is found that the film consists of a sub-surface region with Ge existing in the oxide phase (GeO_2 and GeO_x), while the existence of elemental Ge phase was revealed in the bulk, after a few sputter cycles. However, the significantly lower integrated intensity of the Ge^0 peak compared to the GeO_2 and GeO_x peaks shows that Ge exists predominantly in the oxide phase throughout the film, with only a low concentration of elemental Ge present at larger depth. Table 4.1 shows the chemical state of Ge at different sputter depth in the film, and the atomic concentration obtained from by normalizing the relative spectral peak areas using sensitivity factors derived from standard materials in the database. It is observed that the deposited Ge species is concentrated in the near-surface region, dominated by GeO_2 and GeO_x, with very low levels of Ge existing in the bulk.



(a)



(b)

Fig 4.3.1 (a) Ge $2p_{3/2}$ core level XPS spectra of the film before and after N_2 anneal at 400°C and (b) Ge $2p_{3/2}$ stack plot with each spectrum obtained after each sputter cycle from the XPS depth profile measurement.

Table 4.1 Ge $2p_{3/2}$ binding energy and concentration as a function of depth in the film

Depth (Å)	Peak 1 Binding Energy (eV)	Peak 2 Binding Energy (eV)	% Ge in the film (%)
0	1219.5	1219.3	3.1
5	1218.9	1218.6	10.7
10	1218.9	1217	4.8
15	1218.3	1217.2	2.1
20	1217.1	-	1.5
25	1216.9	-	0.7
30	1217.1	-	0.5
35	1216.8	-	0.4
40	1216.6	-	0.2

The small amount of elemental Ge initially contained in the matrix can provide nuclei for the formation of nanocrystals, if the size is sufficiently larger than the critical size .[153,154] As shown in Fig. 4.3.2, for a given saturation ratio, nuclei with size greater than critical radius, r* will grow into nanocrystals, while nuclei with radius smaller than r* will dissolve to lower the free energy.

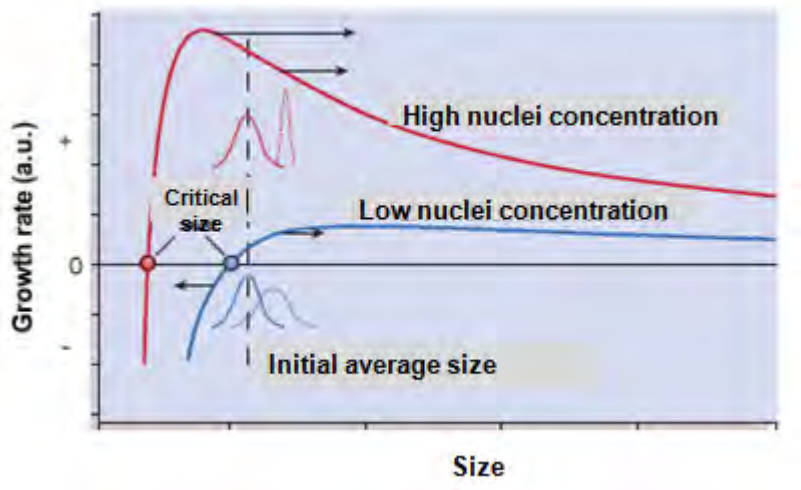


Fig 4.3.2 Schematic illustration of the growth process of the nanocrystals, with the critical nuclei size depending on the supersaturation ratio (Reprinted from Ref [142]). [155,156]

The critical radius size can be estimated based on Wulff's theorem.[157,158] By considering only {hkl} planes present in the polygon, the critical size r*{hkl} and Gibbs free energy for the formation of critical-sized crystallite ΔG* are given by

$$r_c^*\{hkl\} = 2v_c\gamma\{hkl\}/\Delta\mu \quad (4.1)$$

$$\Delta G^*\{hkl\} = 4\omega\gamma\{hkl\}3v_c^2/3\Delta\mu^2 \quad (4.2)$$

where v_c is the atomic volume (Ge: $v_c = 2.27 \times 10^{-23}$), $\gamma\{hkl\}$ is the surface energy density of the {hkl} plane and ω is a topological constant.

Since Ge{111} is the dominant plane in diamond structure nanocrystalline Ge, by inserting $\gamma\{111\} = 714$ erg/cm^2 and $\Delta\mu = 1.53 \times 10^{-13}$ erg at 300K into the equations, an estimated value of $r_c^*\{111\} = 10$Å and $\Delta G^*\{111\} = 3.35$ kJ/mol can be obtained.

This suggests likely nucleation of very small Ge precipitates close to the critical nuclei size in the initial deposit, which is in good agreement with the presence of small nanocrystal regions of ~2 nm observed from the planar TEM image in Fig. 4.2.1 (a).However, a large fraction of Ge is oxidized during the deposition process. The large amount of Ge oxides can dissolve in the Lu_2O_3 matrix, which is generally associated with a region free of nanocrystals in the TEM investigations.[157]As shown in Fig. 4.3.3, as the moving atoms bond together during the deposition process, nucleation proceeds when the atom cluster size, r is larger than the critical nuclei size, r*. On the other hand, elemental Ge clusters smaller than r* dissolve in the oxide matrix to lower the surface free energy. A large amount of Ge oxides are also incorporated and exist in the amorphous state in the Lu_2O_3 dielectric.

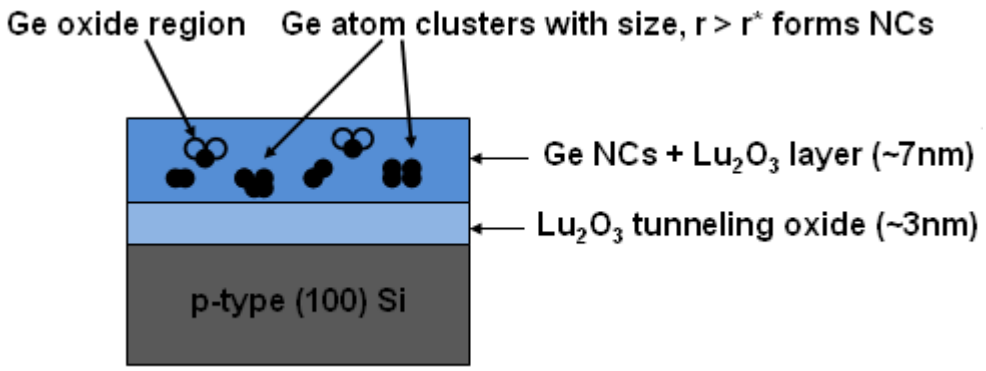


Fig 4.3.3 Schematic illustration of the nucleation of Ge nanocrystals during the deposition process.

Upon annealing at 400^{o}C, the Ge 2p spectrum shows a chemical shift of the oxidized Ge towards Ge^{0} state, suggesting the replacement of Ge-O bonds by Ge-Ge bonds. The significant dissociation of GeO_2 and GeO_x under a low annealing temperature of 400 ^{o}C is different from other reported works that require a high annealing temperature above 600 ^{o}C[159] and 700 ^{o}C[92] for the observations of reduction reaction. This can be explained from the thermodynamics perspectives, which involves a large negative Gibbs free energy change (ΔG) in the material system. This is likely to be related to a different reducing species involved in the reduction process originating from the sub-stoichiometric Lu oxides existing in the oxide matrix due to oxygen deficiencies. The possible reactions involved during the annealing treatment include:

$$GeO_2 + LuO_x \rightarrow Ge + Lu_2O_3$$

$$GeO_x + LuO_x \rightarrow Ge + Lu_2O_3$$

$$GeO_2 + GeO_x + LuO_x \rightarrow Ge + Lu_2O_3$$

The chemical stability of the reducing species involved in the material system potentially leads to pronounced reduction reaction, as compared to studies utilizing Si,[91] SiO_x,[90,92,94,160] Hf [92]and H_2[93] as the reducing species.

In order to study the chemical interactions involved, further studies on the chemical components in the films were evaluated from the Lu 4d, O1s and Si2p spectra in Fig. 4.3.4. The Lu4d spin-orbital doublet of the as-deposited film in Fig. 4.3.4 (a) consists of a peak at E_B~196.3 eV and 206.03 eV. The presence of stronger oxidation states of Lu is indicated by s slight simultaneous shift of the two peaks towards higher binding upon annealing. However, different oxidation states present in the matrix is difficult to be identified due to the small chemical shift (0.1 eV) exhibited by the Lu atom. The relative atomic concentration of each element quantified by integrating each peak and the O/Lu ratio of ~ 1.33 obtained from the as-deposited film indicates a small degree of non-stoichiometry. The oxygen deficiency in the dielectric matrix could act as possible source for the reduction reaction. The small chemical shift of the Lu4d peaks could be explained by further oxidation of sub-stoichiometric Lu oxides during annealing, whereby the sub-stoichiometric Lu oxides react with GeO_2 and GeO_x resulting in the formation of Ge and stoichiometric Lu_2O_3. As shown in Table 4.2, the standard Gibbs free energies of formation ($\Delta_f G^o$) at 298 K for GeO_2, GeO and Lu_2O_3 are -521.4, -273.2 and -1789.0 $kJmol^{-1}$ respectively.[93,161,162] As compared to other candidate gate oxide materials, Lu_2O_3 belongs to the rare earth oxide group, which has among the most negative $\Delta_f G^o$ of all the elements in the periodic table.[8,25,48]

Table 4.2 Gibbs free energy of formation for different oxide materials

Compound (Å)	**Gibbs Free Energy of Formation, $\Delta_f G^o$ ($kJmol^{-1}$) at 298K**
GeO2	-521.4
GeO	-273.2
Lu_2O_3	-1789.0
SiO_2	-856.3
HfO_2	-1088.2
Al_2O_3	-1582.3
La_2O_3	-1705.8

The significantly larger negative Gibbs free energy to form Lu_2O_3 provides a large negative ΔG involved in the reaction between sub-stoichiometric Lu oxides with GeO_2 and GeO_x to form Ge and stoichiometric Lu_2O_3. From the perspective of thermodynamics, GeO_2 and GeO_x are spontaneously reduced to Ge, while sub-stoichiometric Lu oxides are oxidized to Lu_2O_3. The significantly larger $\Delta_f G^o$ for Lu_2O_3 as compared to other oxides provides a large driving force and low activation energy for the reaction to proceed rapidly. Complete reduction of GeO_2 and GeO_x takes place, and the chemical stability of Ge in the Lu_2O_3 matrix successfully eliminates chemically unstable Ge oxides which potentially act as electrically defective interface states.

Fig. 4.3.4 (c) shows the O1s spectra collected from both the as-deposited and annealed sample, which can be resolved to different peaks due to different bonding states existing in the oxide matrix. A similar lower binding energy peak at ~530.3 eV obtained from the sample before and after anneal could be attributed to the O bonding

state in Lu_2O_3.[36,38,51,163] The higher binding energy broad peak could be related to the mixed oxide components existing in the Lu_2O_3 matrix, including silicate-like bonding,[50] sub-stochiometric Lu oxides as well as GeO_2 and GeO_x incorporated during the initial deposit. The existence of silicate-like bonding was shown from the Si2p spectra in Fig. 4.3.4 (c) for both the samples before and after anneal. Besides the fitted peak at 98.7 eV arising from the Si substrate, another peak component was observed at higher binding energy of 101.83 eV, which is correlated to the formation of Lu-O-Si bond at the interface.[164-167]

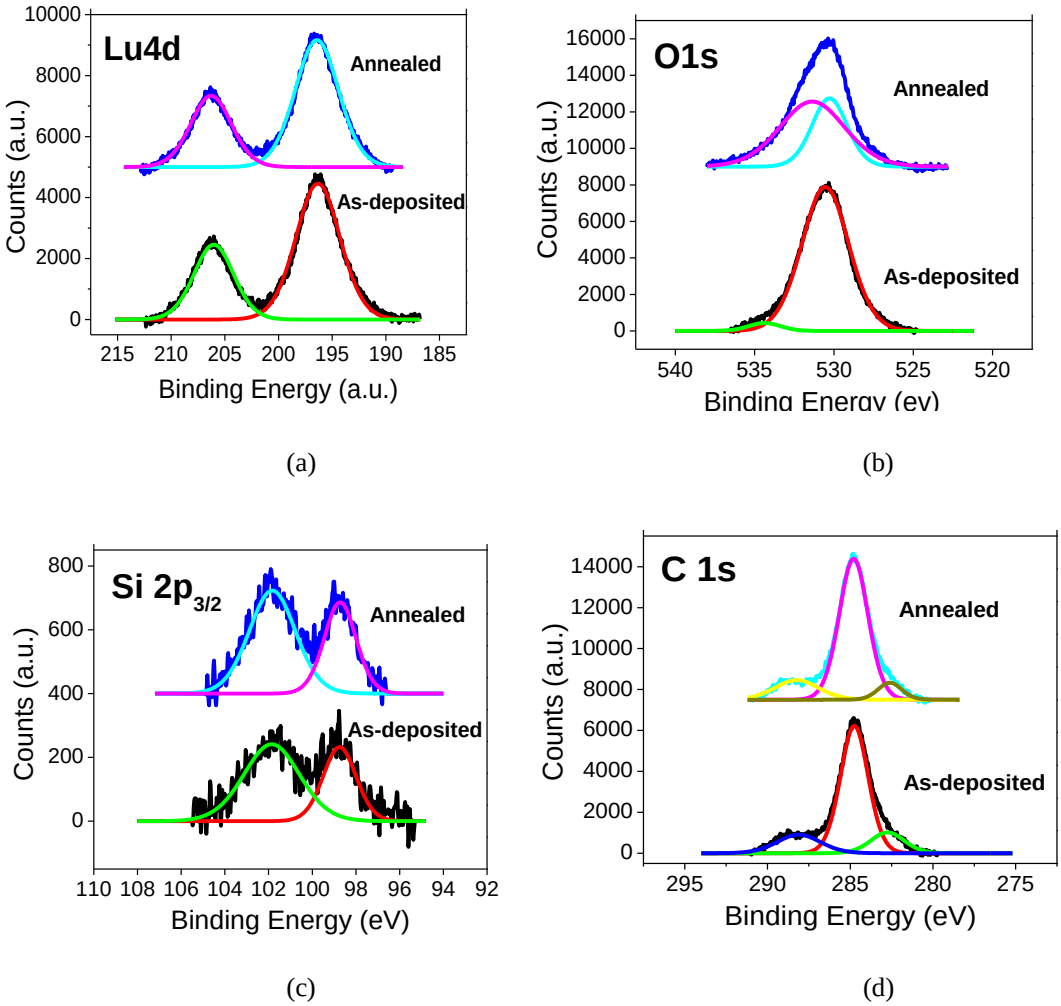


Fig. 4.3.4 (a) Lu 4d (b) O1s (c) $Si2p_{3/2}$ and (d) C1s core level XPS spectra of the film before and after N_2 anneal at 400°C.

Based on the structural and compositional analysis, the nanocrystal formation mechanism could be described from the thermodynamics point of view. The as-deposited film contains a large amount of excess Ge oxides and a small amount of elemental Ge, which forms a supersaturated solution. The high kinetic energy of plasma generated during the laser ablation process results in an enhanced adatom mobility during the deposition process, and some small crystallites are formed when the pre-existing Ge atoms diffuse and bond to existing nuclei forming stable clusters. During the annealing treatment, spontaneous dissociation of Ge oxides and suboxides occurs, leading to the creation of a large amount of elemental Ge atoms. The nanocrystal formation process primarily takes place with the precipitation of Ge nuclei corresponding to the reduction of Ge oxides upon annealing. This is evident from the densely distributed Ge nanocrystals observed from the plan-view TEM image of the annealed film, indicating a significant increased nucleation of Ge nanocrystals associated with the reduction process during the annealing treatment. The simultaneous increase in the average size and size distribution of the nanocrystals after annealing could be explained by short-ranged diffusion and nanocrystal growth from the precipitated nuclei. As shown in Fig. 4.3.5, the annealing treatment provides atomic mobility for diffusing Ge atoms to bond to the surface of precipitated nuclei and incorporate into the structure of the crystal lattice. The final size of the nanocrystals is determined by a combination of thermal decomposition and diffusion process contributing to the nanocrystal growth. Minimal coarsening effect was observed, as the low atom diffusivity limits the occurrence of Ostwald ripening process, whereby larger particles grow at the expense of smaller particles.[168]

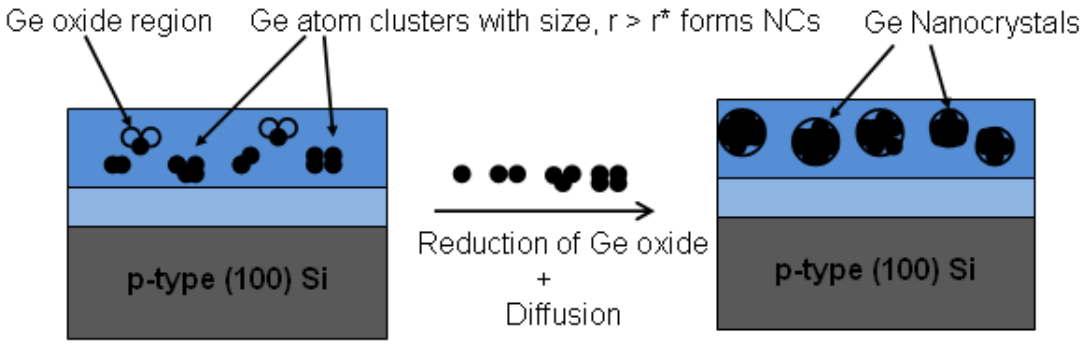
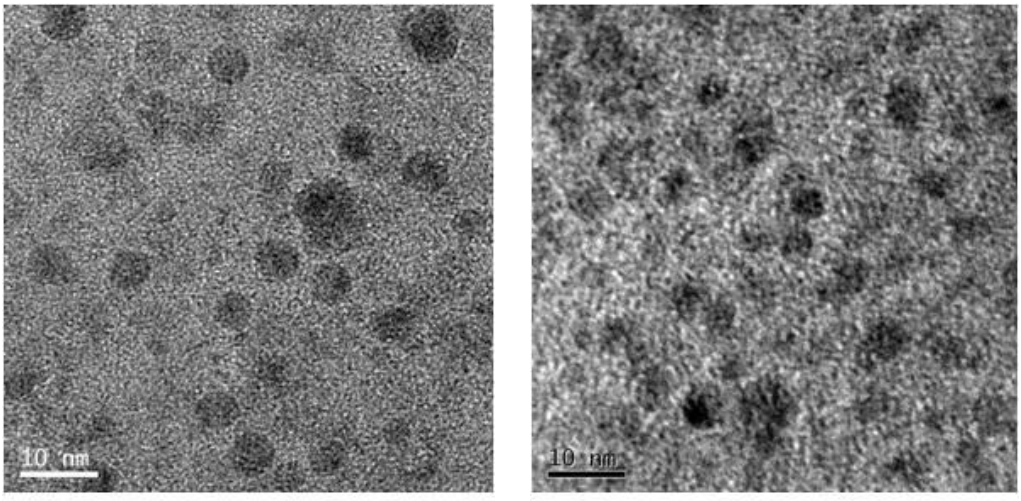


Fig. 4.3.5 The nucleation and growth process of Ge nanocrystals during the annealing treatment as a result of thermal decomposition and atomic diffusion

4.4 Effect of Varying Ge Content



(a) (b)

Fig. 4.4.1 Planar TEM image for the Ge nanocrystals embedded in Lu_2O_3 dielectric matrix deposited with a Ge:Lu_2O_3 target exposed area ratio of (a) 1:10 and (b) 1:4

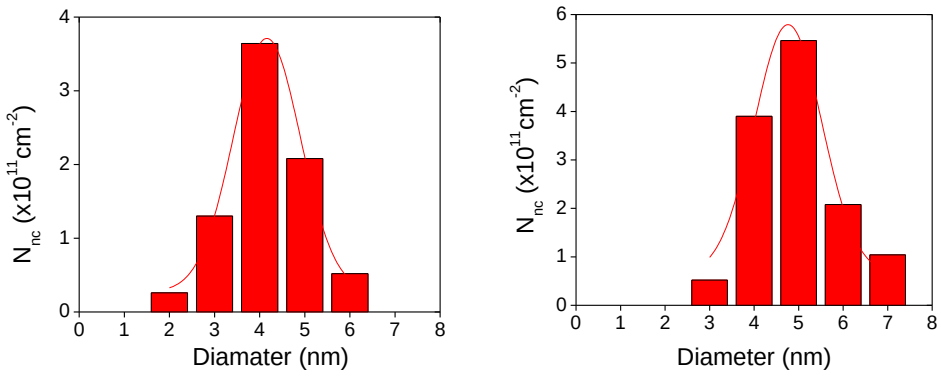


Fig. 4.4.2 Histograms of the Ge nanocrystals size distribution for the samples deposited with a Ge:Lu_2O_3 target exposed area ratio of (a) 1:10 and (b) 1:4

The effect of varying deposition condition was further studied by modifying the target, with Ge: Lu_2O_3 exposed area ratio increased from 1:10 to 1:4. Figure 4.4.1 shows the planar TEM images of the samples, with the estimated nanocrystal density increased from 7 x 10^{11}cm^{-2} to 1.6 x 10^{12} cm^{-2}, corresponding to an increased Ge content from 10% to 20%. Figure 4.4.2 shows the size distribution analysis of the samples estimated by considering 30 to 50 dots per sample, which could be approximated with a Gaussian fit. Similar size distribution of ~2 to 7 nm was obtained from both samples, with a slight increase in mean diameter from 4.2 nm to 4.8 nm for the sample with increased Ge content. However, Figure 4.4.1 shows the occurrence of nanocrystal coalescence in some regions, associated with a reduced average dot-to-dot spacing from 4.8 nm to 2.5 nm with increased Ge content.

Negligible enlargement in the nanocrystal size with increasing Ge content shows minimal Ostwald ripening of nanocrystals under the low anneal temperature of 400 ^{o}C. The uniform size distribution is anticipated from the nucleation of nanocrystals mediated by enhanced atomic mobility due to the high kinetic energy of incident particles generated from pulsed laser deposition process. The larger Ge: Lu_2O_3 exposed area ratio leads to an increased nanocrystal density with the nanocrystals maintained at similar size, which implies dominant formation of nanocrystals in the nucleation regime with controlled growth. This is in agreement with the nanocrystal formation mechanism suggested in the previous section, with significant contribution from the thermal decomposition of oxidized Ge. Due to dominant Ge nanocrystal formation resulting from the decomposition of Ge oxides and short-ranged diffusion of Ge atoms, adequate size control is obtained. On the other hand, the nucleation

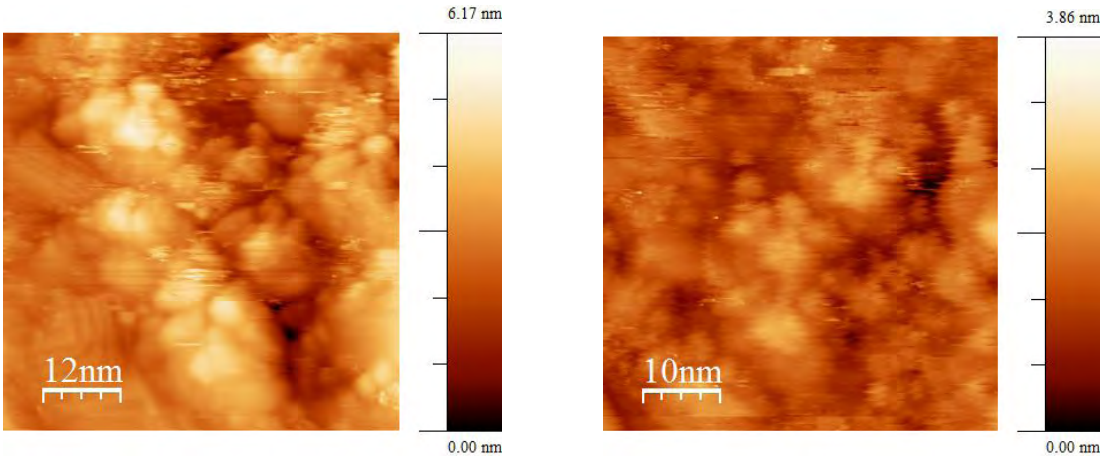
density is determined by the Ge content available for precipitation, which can be used to obtain an enhanced nanocrystal density.

The size control effect suggests the possibility to tune the nanocrystal density by increasing the Ge content, with the nanocrystals maintained at an optimum size of ~5nm. However, with the Ge content increased from 10% to 20%, nanocrystal coalescence was observed along with a reduced nanocrystal separation, which could be detrimental for electrical isolation of the stored charges. The inhomogeneous Ge content in the film and cluster formation during deposition resulted in coalescence of the nanocrystals at Ge-rich regions upon annealing. Based on the observations, it is possible to evaluate the optimum deposition condition to obtain the desired nanocrystal parameters. Although efforts have been focused on obtaining high density nanocrystals for enhanced charge storage, simultaneous control of size distribution and intercrystallite separation is important to ensure electrical isolation of the stored charges. An optimum nanocrystal density of 10^{12} cm^{-2} is anticipated to provide both an optimal nanocrystal size and separation of ~5 nm for memory operation.[169] Hence further work on tuning the Ge target exposed area ratio during deposition could provide an adaptive design of the nanocrystal memory with desired size, density and spatial distribution.

4.5 Probing on Nanocrystal Properties

Scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) techniques were employed to allow probing of the electrical properties of the nanocrystals at the nanoscale by correlating with the topographical images. Fig. 4.5.1

shows the STM topography images of the Ge nanocrystals embedded in Lu_2O_3 high-k dielectric with a total film thickness of ~7 nm after anneal. Nearly spherical nanocrystals with a size range of 3-8 nm were observed, in good agreement with the observations from TEM image. However, the observations of cluster formation with a size of ~9-17 nm suggest possible aggregation of the nanocrystals during the annealing treatment.



(a) (b)

Fig 4.5.1STM topography images of the Ge nanocrystals in Lu_2O_3 high-k dielectric with a scan size of (a) 60 nm x 60 nm and (b) 51 nm x 51 nm.

Scanning tunneling spectroscopy (STS) study was also carried out by acquiring current mapping images to study the electrical distribution of the film under different bias condition. A topographic image and corresponding current mapping images of the film are shown in Fig. 4.5.2. Under a positive substrate bias of +0.7 V, bright regions were observed from the locations with large clusters of the topography image. The observed current contrast provides an indication of electron injection from the tip into the nanocrystals, resulting in an enhanced current conduction observed from the clustered regions. With a larger applied bias of +1.3 V, an increased amount of small

bright spots appear, likely related to a larger voltage needed to overcome the larger barrier height for current injection into smaller nanocrystals embedded in the high-k dielectric. A reverse contrast was observed upon reversing the bias polarity, corresponding to hole injection from the tip into the nanocrystals. However, the current signal is significantly lower under negative substrate bias due to a reverse bias application of the sample configuration. Nevertheless, the observed current contrast shows bias-dependent charging effect, as a result of enhanced charge injection and subsequent charge confinement in the nanocrystals with increasing bias magnitude.

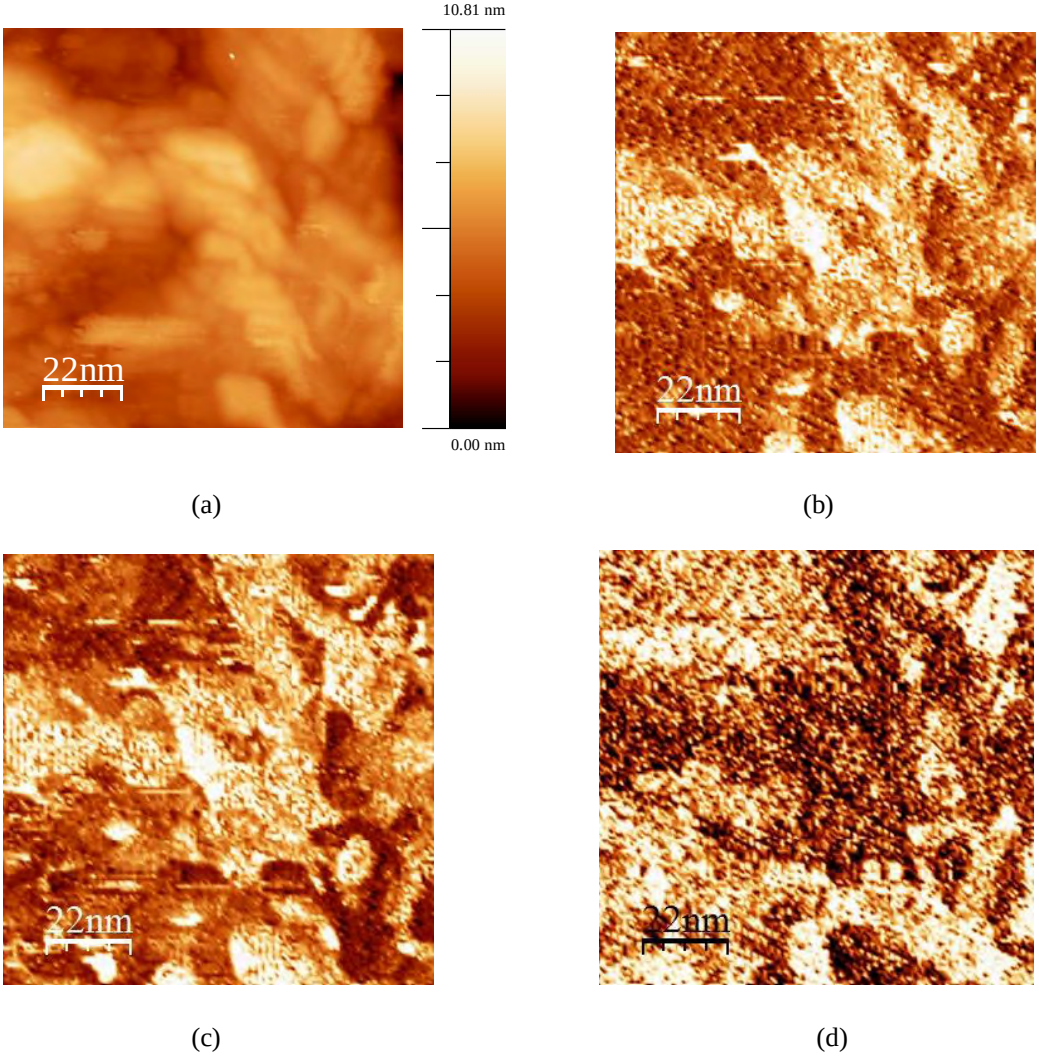


Fig 4.5.2(a) STM topography image and (b)-(d) corresponding current mapping images measured with a bias voltage of (b) +0.7V (c) +1.3V and (d) -1.3V applied to the substrate, and the tip grounded.

In order to probe the size-dependent properties and local current-voltage (I-V) behavior of the nanocrystals, scanning tunneling spectroscopy (STS) study was performed at different locations corresponding to the topographic image, as shown in Fig. 4.5.3. The I-V characteristics of the sample probed at different locations show rectifying behavior, which is consistent with the observations from comparable metal-insulator-semiconductor diodes with and without nanocrystals[170] and nanostructure Si / electrode heterojunction system.[166] The diode-like behavior originates from the p-n like junction properties formed at different interfaces in the system, which is strongly dependent on the electrode material properties. Schottky current transport behavior has been observed with p-type Si substrate as one of the electrode material. [23] The reverse bias current at negative substrate voltage is limited by minority carrier injection from the p-type Si substrate.

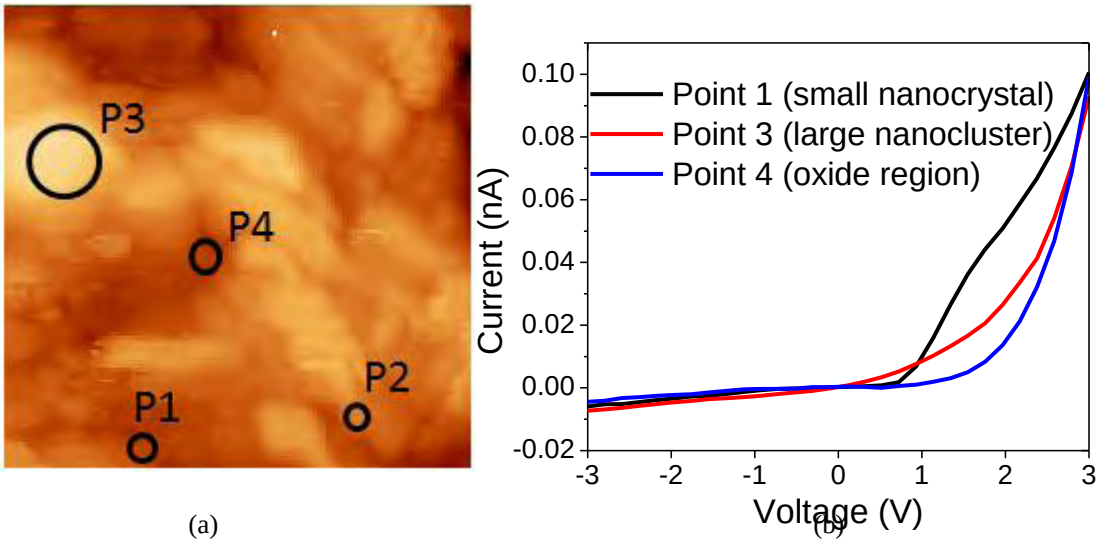


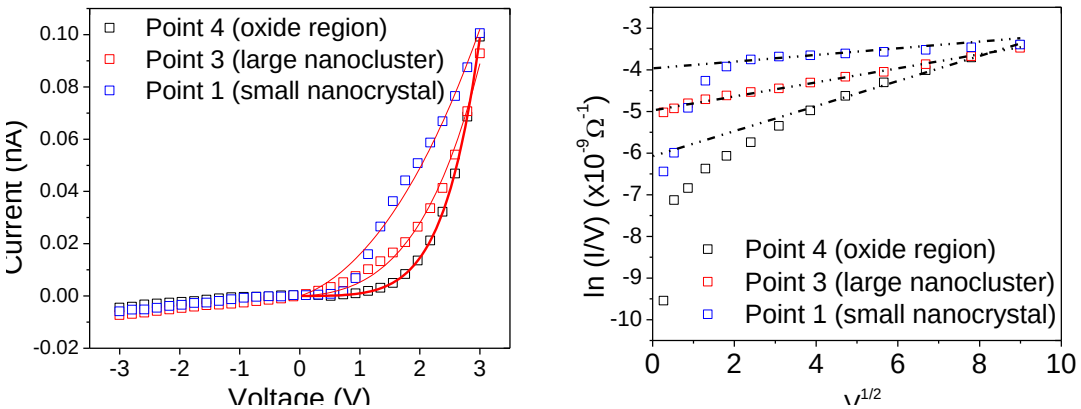
Fig 4.5.3(a) STM topography image and (b) corresponding local I-V characteristics extracted from different locations with and without nanocrystals from the image.

The current transport properties of the rectifying junctions were further examined in this study by further evaluating the I-V curves obtained from different regions. The observation of rectifying characteristics indicate diode-like reverse bias current characteristic. With this consideration, the I-V characteristics can be represented a serial combination of diode and resistor.[171] As shown in Fig. 4.5.4 (a), the forward bias I-V curves can be fitted to the Poole-Frenkel (P-F) model, given by the equation.[172]

$$I = I_0 V \exp\left(\frac{-q\Phi_B}{kT}\right)\exp\left(\frac{V}{V^*}\right)^{1/2} \qquad (V^*)^{1/2} = \frac{kT}{q}\left(\frac{q}{\pi\varepsilon_0\varepsilon d}\right)^{-1/2} \tag{4.3}$$

where I_0 is the pre-exponential factor, Φ_B is the trap energy, and ε is the dielectric constant. This suggests that under forward bias condition, majority voltage drops across the resistor resulting in electric field dependence of the oxide film resistivity, and the diode term becomes negligible. Fig. 4.5.4 (b) shows the field dependent P-F fit, with the forward bias characteristics, ln (I/V) plotted as a function of $V^{1/2}$ at room temperature. The reasonable linear fit of the curve observed from mid-to-high field regions for all location indicates dominant P-F hopping mechanism for the charge transport. Charge carriers hop between the trap states defined by the potential wells in the film stack. Different I-V characteristics were observed from the regions with nanocrystals (P1 and P3), with an enhancement in current conduction attributed to electric-field-induced charge transfer followed by charge confinement in the nanocrystals.[23] The zero-field conductivity value was obtained by extrapolated the forward bias conductivity extrapolated to zero bias voltage. A significantly higher

conductivity was observed from the oxide region with nanocrystals, which could be associated to a tunneling current assisted by the nanocrystals. The enhanced conductivity is more apparent for the small nanocrystal region, suggesting a more effective carrier confinement effect. In addition, the I-V characteristic of the small nanocrystal location shows larger deviation from the fitted curve especially in the low field region, which implies a different conduction mechanism due to trap-assisted tunneling contribution through the nanocrystal trapping centers.[23,173] These differences suggest that size of the nanocrystals play an important role in the properties of the junction constructed and carrier transport behavior. Thus, the tunnel barrier and trap energy states can be extracted by taking into account the geometric and charging effects in the transport mechanism.



(a) (b)

Fig 4.5.4 (a) I-V characteristics extracted from different locations with and without nanocrystals, with the curves fitted to the Poole-Frenkel equation and (b) The forward bias conductance ln (I/V) as a function of $V^{1/2}$, with the linearly fitted line extrapolated to the zero-field conductance.

Fig.4.5.5 shows the differential conductance, dI/dV curves extracted from the STS measurements. Remarkable features with conductance peaks were observed from the locations with small nanocrystals, P1 and P2. The observations show a signature of

resonant tunneling / charge transfer involving a small number of charge quanta between the electrodes and available states of the size-quantized nanocrystals.[23,136] Conductance peaks were observed under a voltage of ~1.2 V, which implies an increase in local density of states due to the onset of charge injection and subsequent confinement in the nanocrystals, which can be interpreted in terms of Coulomb effects.[25,174,175] No featured conductance peaks were observed from the regions with large clusters (P3) and reference location (P4), associated with current tunneling through a single tunnel barrier. In addition, zero-conductance gap was observed from the locations with small nanocrystals, P1 and P2, which provides information on the energy band gap of the nanocrystals. Threshold bias of ~0.3 eV was obtained under positive substrate bias, which corresponds to the conduction band minimum (CBM) values of the nanocrystals. On the other hand, a larger barrier height for hole tunneling was obtained under negative substrate bias, which corresponds to the valence band maximum (VBM) values of ~0.5 eV to 0.7 eV for an estimated nanocrystal size of 6nm and 5nm, respectively. This results in a zero-conductance gap width of ~0.8 to 1.0 eV, which agrees well with the increase in energy band gap from the Ge bulk of 0.66eV (CBM and VBM for bulk Ge is 0.28 eV and 0.41 eV) .[21,176-178] The band gap values of 0.8eV to 1.0eV is consistent with the theoretical prediction for an estimated nanocrystal size of 8 nm and 7 nm, respectively, which substantiates the nanocrystal size observed from the STM topography image. The observations support the size-dependent electronic properties of the nanocrystal, with the bandgap dictated and modulated by the nanocrystal size.[23,136]

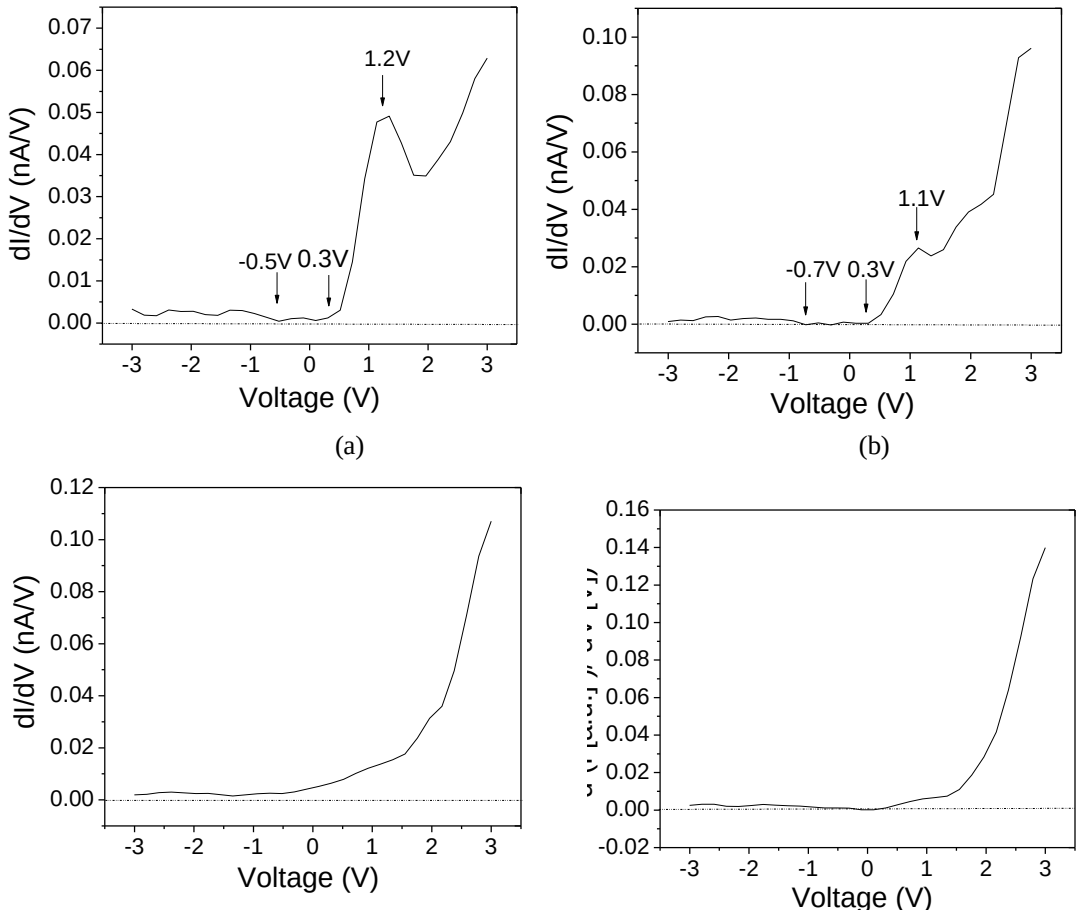


Fig 4.5.5 Differential conductance, dI/dV extracted from STS measurements extracted from the STM topography image at different locations (a) P1, corresponding to a nanocrystal size of ~6 nm (b) P2, corresponding to a nanocrystal size of ~5 nm (c) P3, corresponding to a large nanocluster size of ~20nm and (d) P4, corresponding to the reference oxide barrier without nanocrystals.

4.6 Summary

In summary, a low temperature technique for the formation of Ge nanocrystals was successfully demonstrated in this work. The nanocrystal formation mechanism was described with dominant thermodynamics contribution under the low annealing

temperature of 400 ^{o}C. Nucleation of Ge nanocrystals takes place predominantly through thermal decomposition of Ge oxides and suboxides followed by nanocrystal growth by short-ranged diffusion of Ge atoms. The low temperature reduction of Ge oxides and subsequent nanocrystal formation is realized by the large negative Gibbs free energy change (ΔG) involved in the material system. The feasibility of tuning the nanocrystal density was also demonstrated by increasing the Ge: Lu_2O_3 target exposed area ratio during deposition. The simple approach allows an increase in nanocrystal density with adequate size control obtained under the low anneal temperature. With an independent control of nanocrystal size and density, defined nanocrystal characteristics and structure design can be envisaged by further tuning of the Ge content during deposition. The unique property of the nanocrystals with size-dependent electrical behavior was also suggested from the localized charge transport study of the nanocrystals.

CHAPTER 5 Study and Optimization on Ge Nanocrystal Memory Capacitor Device Functionality

5.1 Introduction

Semiconductor nanocrystal-based memory provides improved scaling perspectives for future non-volatile memories. However, it suffers from weak electrostatic coupling and small memory window (threshold voltage shift).[179,180] In this regard, the implementation of different high-k dielectric materials has been explored for improved channel-control factor and retention characteristics.[167]

This chapter focuses on the introduction of lanthanide-based high-k dielectric in the Ge nanocrystal memory structure to enable low voltage operation and address the weak coupling issue of nanocrystal memory. Memory capacitor devices were fabricated for electrical characterization. Different charge storage mechanisms were proposed to explain the hysteresis behaviour that is related to the film structure and composition. Further enhancement of the memory performance with simultaneous improvement in charge storage and retention is demonstrated with the realization of a lanthanide-based graded high-k barrier structure enabled by thermally-induced intermixing of oxide components. Further studies on the effect of dielectric matrix suggest the important role of dielectric film structure and the nanocrystal-dielectric interface properties on the charge storage behaviour of the memory device.

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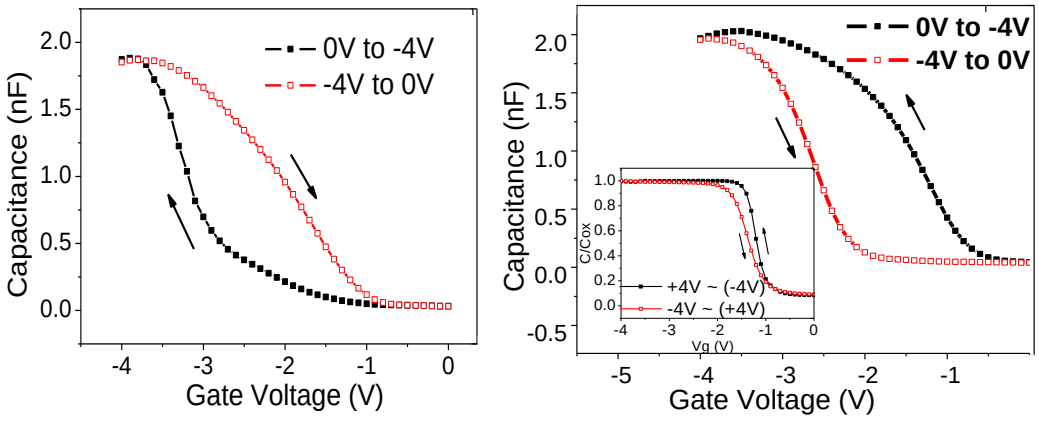
5.2 Charge Storage Capability and Charge Storage Behavior

5.2.1 Charge storage capability

The charge storage capability of the metal-insulator-semiconductor (MIS) memory capacitor devices fabricated from the samples with and without post-deposition anneal (PDA) was investigated by performing high frequency (100kHz) capacitance-voltage measurements. Fig. 5.2.1 shows the C-V hysteresis loops obtained from both samples by sweeping the gate voltage from the inversion region at 0V to accumulation region at -4V, and then swept back from the accumulation to inversion region. A significant difference was observed between the devices with and without PDA, with an opposite hysteresis loop direction obtained. The opposite hysteresis behaviour suggests the involvement of different mechanisms in the charge trapping process, which in general can be introduced by the mixed effects of injected charges stored in the nanocrystals and essential trap charges existing in the oxide or interface states.[181] The charge trapping in the nanocrystals may include the substrate injection mechanism[169], charge injection from the gate[182] and electron transfer from charged defects in the gate oxide.[136,183-186] Besides that, the drift of positively charged mobile ions contaminated in the gate oxide may also result in the hysteresis behaviour.[183,186,187]



(a) (b)

Fig. 5.2.1 High-frequency (100kHz) capacitance-voltage characteristics of the MIS devices (a) without and (b) with PDA at 400°C, with the inset showing the C-V curve of the control sample.

The anticlockwise hysteresis loop observed from the annealed device is generally attributed to the charge trapping effect of the nanocrystals via substrate injection mechanism, as illustrated in Fig. 5.2.1 (a). Fig. 5.2.1 (b) shows that when a positive voltage is applied to the gate, electrons can tunnel from the substrate inversion layer to the nanocrystals, resulting in a shift of the C-V curve towards positive voltages. When a negative voltage is applied to the gate, electrons can tunnel from the nanocrystals back to the substrate (and/or holes can tunnel from the substrate accumulation layer to the nanocrystals), resulting in a shift of the C-V curve towards negative voltages.[188-190] This is due to the screening of the gate charge by the stored charges in the nanocrystals, which effectively shifts the threshold voltage towards more positive or negative values, depending on the type of charges (electrons / holes) stored in the nanocrystals.[191,192] As shown in Fig. 5.2.1 (b), a significant charge storage effect was demonstrated with a large threshold voltage shift of ~1.3 V obtained from the annealed device. The large threshold voltage shift is favourable in obtaining a large I_{on} / I_{off} ratio for flash-type memory operation. Since no distortion in the C-V curves, e.g., flat step due to deep defect traps or large interface state density,

was observed,[191] the hysteresis effect can be related to the charging of the Ge nanocrystals or nanocrystal-related traps. The C-V curve of a control sample deposited under the same processing conditions without Ge incorporation exhibits a relatively smaller hysteresis (~0.2 V), likely related to the essential trapped charges existing in the oxide or interface states, with an interface state density, D_{it} of 2.66 x 10^{13} $cm^{-2}eV^{-1}$ estimated from the Lu_2O_3/Si interface using Terman equation.[193,194] Hence major charge storage effect from the device with Ge nanocrystals is attributed to the trapped charges in the nanocrystals, resulting in an enlarged hysteresis effect.

The stored charge density of the nanocrystals was estimated from the threshold voltage shift of the device, given by the following expression:[21]

$$\Delta V_{th} = \frac{qn}{\varepsilon_{ox}}\left(t_{cntl} + \frac{1}{2}\frac{\varepsilon_{ox}}{\varepsilon_{Si}} t_{well}\right) \tag{5.1}$$

where ΔV_{th} is the threshold voltage shift, t_{cntl} is the thickness of the control oxide under the gate, t_{well} is the linear dimension of the nanocrystal well, ε's are the permittivities, q is the magnitude of electronic charge, and n is the stored charge density. It should be noted that this equation is based on the general assumption that the charges are trapped in a sheet layer at well-defined distance from the gate electrode, which could introduce error in the charge estimation in the case that the trapped charges are scattered and not well-defined in a single layer. The number of trapped charges in the annealed device was estimated to be 7.0 x 10^{12} cm^{-2}. On the other hand, the areal density of the nanocrystals estimated from the TEM image is 7.0 x 10^{11} cm^{-2}, which gives an estimation of 10 charges per nanocrystal. This situation is different from the general

assumption that a single electron is stored in a nanocrystal, since the additional injection of carriers is limited by the large charging energy for small nanocrystals. [191] The Coulomb charging energy ($q^2/2C_{tt}$, where $C_{tt} = 2\pi\varepsilon oxd$ is the nanocrystal capacitance) of the nanocrystals with an average diameter of 9 nm in the present work was calculated to be 13 meV, which is less than the thermal energy of electrons (kT = 26 meV at room temperature).[193]Hence it is shown that Coulomb Blockade effect has no significant effect on the device at room temperature, and single electron charging effect can be ruled out in the memory operation.

It is generally assumed that the injected charges are stored dominantly in confined states in the nanocrystal conduction band.[167] However, other reports demonstrated that electrons are instead mostly stored in localized traps at the interface between the nanocrystals and the oxide or at the internal traps of the nanocrystals.[21] In addition, it has been shown that the role of traps at the interface and inside of the nanocrystals is responsible for the large memory window of semiconductor memories. The small density of states of the nanocrystals generally results in very small memory windows due to high conduction band / valence band edge of nanocrystals that limit the number of stored electrons.[195] Surface defect densities in the order of 10^{12} cm^{-2} has been reported for the interface of bulk Ge and SiO_2, which suggests that self-interstitial defects in the Ge nanocrystals may be responsible for the charge storage in nanocrystal memory devices.[141] The large memory window and trap density obtained from the present work suggests that charge storage is primarily attributed to the defects or deep traps originating from the internal or surface of the nanocrystals. The strained surface of nanocrystals could be a source of interfacial defects, and a substantially higher density of interface states could exist between the nanocrystals

and high-k dielectric as compared to thermally grown SiO_2. The charges injected into the nanocrystals first filled the empty states, where the trap level is deeper, and then fill the states where the level is shallower.[54,135,196]

On the other hand, Fig. 5.2.1 (a) shows a clockwise hysteresis obtained from the device without PDA with a similar magnitude in the flatband voltage shift of ~1V. The significant difference in the charge storage behaviour is related to the different composition and structural properties of the film before and after annealing. Based on the AFM, TEM and XPS analysis elucidated in Section 4.2 and 4.3, it can be deduced that the as-deposited film consists of a Ge-rich mixture with a large fraction of Ge oxides and a small amount of Ge precipitates.[197] Hence substantial amount of interface traps and structural defects eg. weakly bonded GeO_x, exists, which results in mixed charge trapping effects at the interface and defect states besides the excess Ge traps. With a larger amount of interface states and defects existing in the oxide before annealing, it is plausible to assume that the charge storage is dominated by defect-related charge trapping, whereby charge transfer process occurs between the excess Ge and Ge oxide traps as well as surrounding interface and defect states in the oxide matrix.[106] The large density of defects in the oxide prevents effective charge injection from the substrate and simultaneous charge injection from the gate, resulting in reverse hysteresis behaviour, as illustrated in Fig. 5.2.2 (c). Fig. 5.2.2 (d) shows the contribution of interface traps in the C-V characteristics which is apparent from the stretch-out in the C-V curve observed when the gate voltage was swept from inversion into the depletion region.

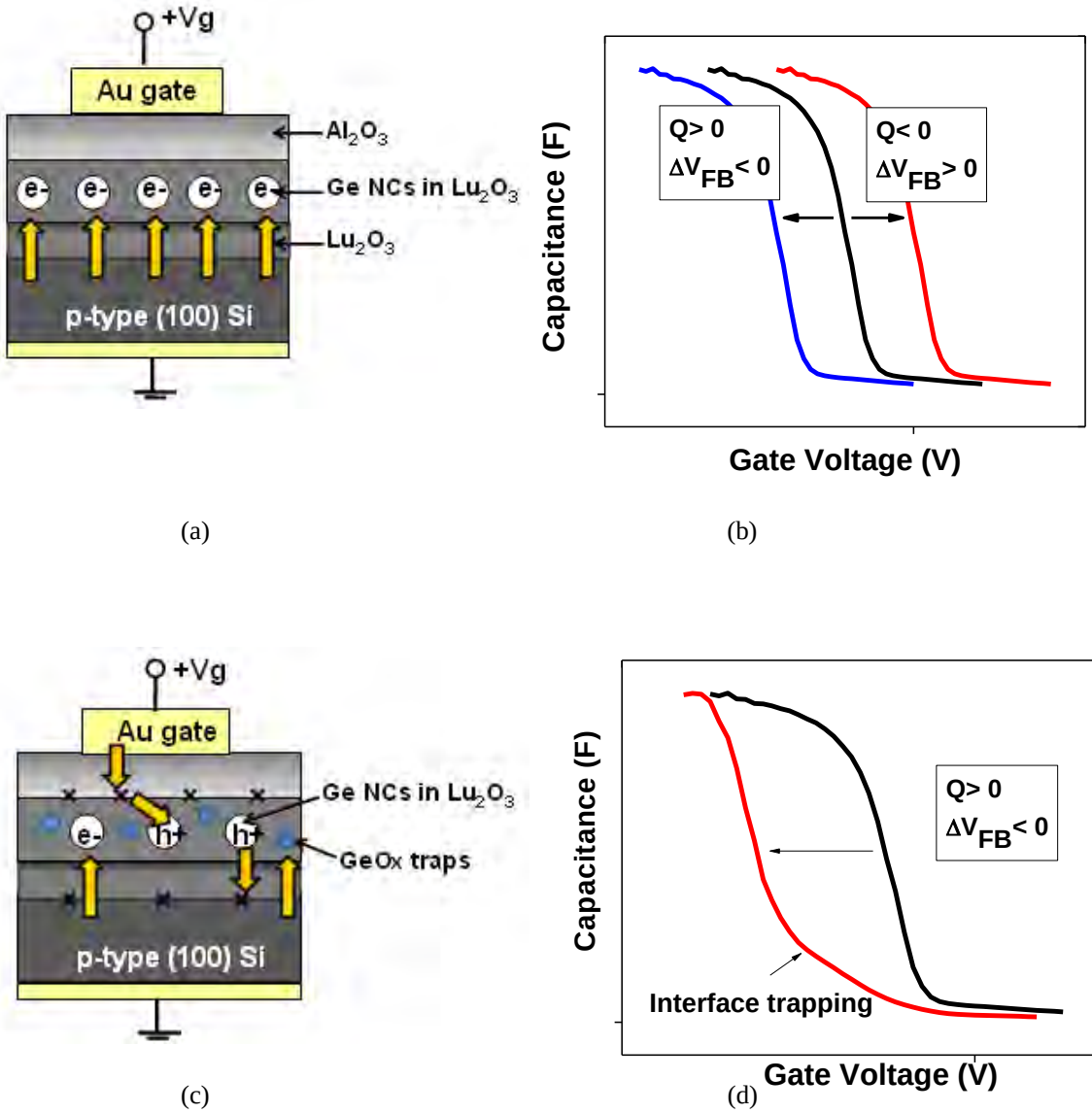


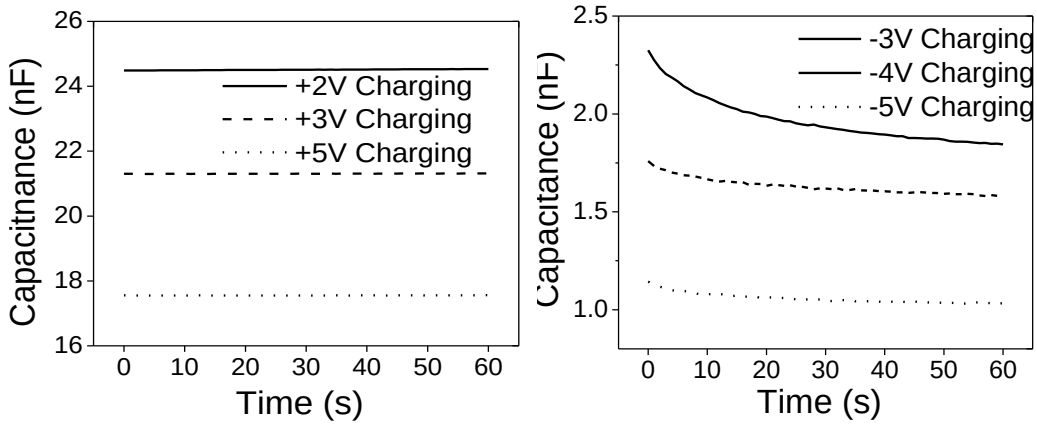
Fig. 5.2.2 (a) Charge storage model for the 400 °C annealed device and (b) the corresponding high-frequency capacitance-voltage characteristics with positive and negative flatband voltage shifts observed due to negative and positive charge trapping effect and (c) charge storage model for the as-deposited device and (d) the corresponding high-frequency capacitance-voltage characteristics with flatband voltage shift and stretch-out of capacitance-voltage curve due to the presence of interface traps.

5.2.2 Charging behavior and programming efficiency

The charging process of the annealed device was studied by monitoring the capacitance variation with time under constant positive or negative charging voltages. The stored charges in the nanocrystals obtained during the charging cycle would result in the screening of gate charge and a subsequent change in capacitance due to the contribution of electric field created by the dot charges.[198] Since the device in this work have a p-type substrate MIS structure, a positive voltage applied on the gate would trigger the device to be biased into the depletion / inversion region, while a negative applied voltage would trigger the device to be biased into the accumulation region. Hence under positive voltage charging, electrons (minority carriers) would be primarily attracted to the Si substrate-Lu_2O_3 interface and tunnel through the oxide into the Ge nanocrystals if effective charge injection occurs. With negative charges stored in the nanocrystals, the surface of the p-type substrate would become less depleted of holes or less inverted with electrons, resulting in an increase in overall gate capacitance. On the other hand, holes (majority carriers) injection into the nanocrystals could occur under negative voltage charging. With positive charges stored in the nanocrystals, the substrate surface would become less accumulated or more depleted with holes, resulting in an overall reduction of gate capacitance during the charging cycle.

Fig. 5.2.3 shows a capacitance-time (C-t) plot of the memory device with the gate voltage held at each charging voltage for 60 s. For both positive and negative charging voltages, the structure was not discharged prior to the application of a larger charging voltage. As shown in Fig.5.2.3 (a), negligible change in the capacitance value with time was observed under positive applied voltage up to a charging voltage

of +5 V, indicating negligible negative charge storage resulting from electron trapping in the nanocrystals. On the other hand, charging behaviour was already observed under a low negative charging voltage of -3 V. The reduction of gate capacitance observed during the charging cycle indicates effective charging of holes into the nanocrystals, with a saturation of charge storage reached after a holding time of 60 s. Further increase in the charging voltage to -4 V and -5 V resulted in only a slight reduction of the gate capacitance over time, indicating that the system was almost fully charged after -3 V charging for 60 s.



(a) (b)

Fig. 5.2.3 C-t plot of the memory capacitor device monitored under (a) positive and (b) negative charging voltages with a holding time of 60s.

The hole charging phenomena with negligible electron charging effect observed suggests that major charge storage of the memory device is due to hole contribution. The charging phenomenon is governed by the tunneling of holes from the substrate accumulation layer into the nanocrystals, with sufficiently thick control gate oxide that block subsequent carrier emission from the nanocrystals. The absence of electron trapping effect could be due to an ineffective electron injection into the nanocrystals and limited storage capacity for electrons in the nanocrystals. This could be due to the

existence of a high density of hole traps existing as electron donors, E_{TD} close to the valence band of the Ge nanocrystal (Fig. A5.1). The energy of the bottom (top) of the conduction (valence) band in the Ge nanocrystal region is above the energy level of the conduction (valence) band in the substrate. This results in higher charge loss rate due to the smaller tunneling barrier height for retention and smaller effective mass for electrons.[183] Hence electrons could not be retained stably in the conduction band of the nanocrystals without the existence of deep level traps, resulting in negligible electron charging effect due to tunneling out of electrons. On the other hand, it has been observed that holes exhibit more stable characteristics for charge retention,[141] which allows the holes to be captured and trapped easily in the nanocrystals.

Fig. 5.2.4 (a) shows the C-V characteristics before and after charging with sequentially increasing programming voltages from -2 V to -5 V under a step voltage of -0.5 V, with a holding time of 10 seconds for each programming voltage. The initial C-V curve obtained by sweeping from 0 V to -1.5 V before performing the charging measurements could be treated as the quasi-neutral condition (i.e. the uncharged condition) under a restricted bias sweep. A negligible shifting of the C-V curves was obtained under positive applied bias, indicating minimal electron charging effect. The C-V curves consistently shifted towards more negative gate voltages with increasing negative programming voltages as a larger amount of holes were injected and trapped in the nanocrystals. However, for programming voltages beyond -4 V, instead of having parallel negative shift of the C-V curves, a reduction in the accumulation capacitance value and a slight distortion of the C-V characteristic associated with the more stretched out curve was observed with increasing

programming voltages. It has been demonstrated that for the case of nanocrystals distributed throughout the oxide with a high concentration, charging and discharging of nanocrystals resulted in a modulation of the capacitance magnitude instead of the flatband voltage (V_{FB}) shift.[199-202] In the present work, initial V_{FB} shift associated with the parallel shift of the C-V curves occurred before the capacitance reduction was observed at higher programming voltages. Hence it is plausible to assume that the holes were initially injected into the nanocrystals resulting in the observed V_{FB} shift, and redistribution of charges from the nanocrystals to the surrounding traps occurred after the onset of charge saturation in the nanocrystals at a programming voltage of -4V, resulting in the capacitance reduction. Furthermore, the slight distortion of the C-V curves observed after stressing at higher voltages could be related to slow charge rearrangement instead of charge injection effects, which involves the tunneling out of the stored charges from the nanocrystals and subsequent charge transfer to the surrounding traps, likely to be interface and/or near-interface defects.[141] The observations suggest that the interface and near-interfacial oxide traps adversely affects the charging characteristics and overall electrical behaviour of the memory device.

In order to study the programming efficiency of the device, V_{FB} was extracted from each C-V curves. Fig. 5.2.4 (b) shows the magnitude of the shift in V_{FB} with respect to the quasi-neutral condition (ΔV_{FB}) plotted as a function of the programming voltage. A significant V_{FB} shift of 0.52 V was already observed under a low programming voltage of -2 V, indicating an effective charge injection into the nanocrystals. The V_{FB} shift increases with increasing programming voltages until a maximum V_{FB} shift of 1.32 V was obtained for programming voltages of -4 V and

beyond, corresponding to the saturation of charge storage. Hence an effective hole trapping phenomenon was demonstrated, with a large V_{FB} shift obtained under low operation voltages.

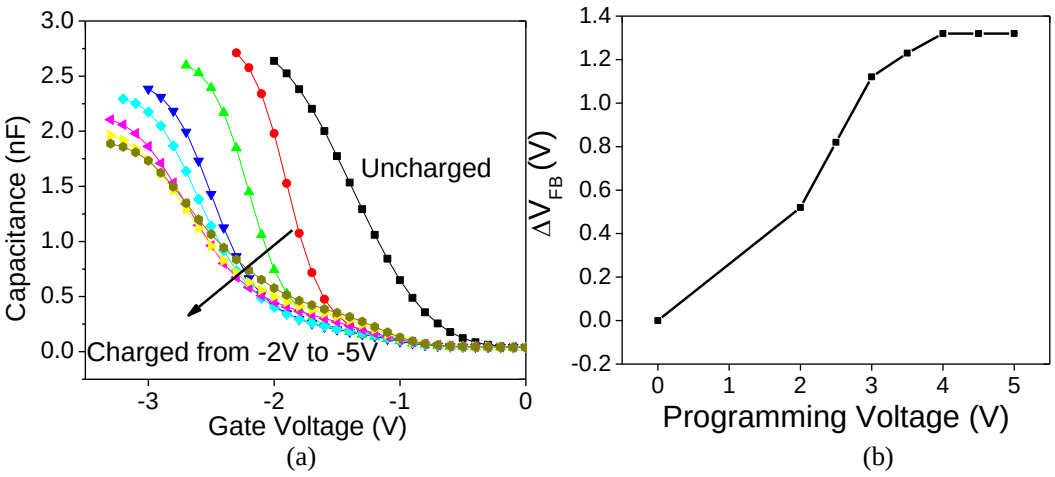
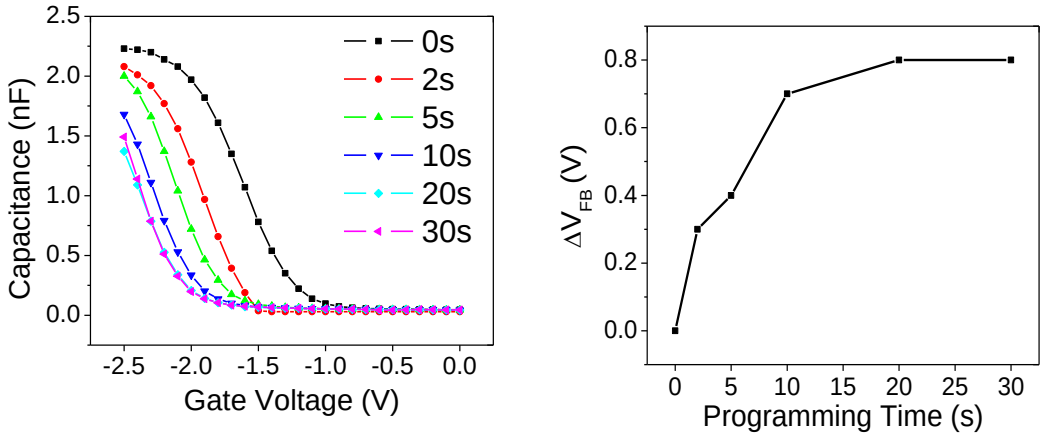


Fig. 5.2.4 C-V characteristics of the memory capacitor device obtained before and after applying sequential negative programming voltages with a stress time of 10s and (b) the corresponding flatband voltage shift as a function of programming voltages.

Fig. 5.2.5 shows the programming transient characteristics, with the C-V curves obtained before and after charging for different time, and the corresponding V_{FB} shifts plotted as a function of stress time under a programming voltage of -3 V. The results show the charge trapping kinetics with a significant V_{FB} shift of 0.3 V obtained after charging for 2 s. The V_{FB} shift increases with larger stress time and a maximum V_{FB} shift of 0.8 V was obtained for a programming time of 20 s and beyond.



(a) (b)

Fig. 5.2.5 (a) C-V characteristics of the memory capacitor device obtained before and after charging at -3V with different stress time and (b) The corresponding flatband voltage shift as a function of programming time.

5.2.3 Charge retention properties

Figure 5.2.6 shows the charge retention characteristics of the annealed memory capacitor device, with the normalized capacitance plotted as a function of discharging time. After charging the device under an applied bias of -3 V for 10 s, the capacitance was monitored over time under the flatband condition of the device at -1 V. The normalized capacitance in the C-t plot was calculated based on the formula $[C_{fb} – C(t)] / [C_{fb} – C(0)]$ where C_{fb} is the initial capacitance at -1V before performing the charging and discharging experiment, C(t) is the capacitance at measurement time t and C(0) is the initial capacitance at the start of the discharging experiment.[199] The onset of discharging process was only observed after a holding time of 100 s with no significant initial fast decay observed. 5% of initial stored charge was lost after a holding time of 1000 s, indicating a good stability of the programmed state expected from the charge decay behavior. The long term charge storage characteristic of the device is also shown in figure inset, with a gradual decrease of memory A retention

time of 10^4 s was measured for 25% charge storage loss, which is satisfactory as compared to devices with similar equivalent oxide thickness (EOT).[23] This shows that a small amount of leakage paths exist in the memory structure which provides effective charge trapping at the distributed storage nodes.

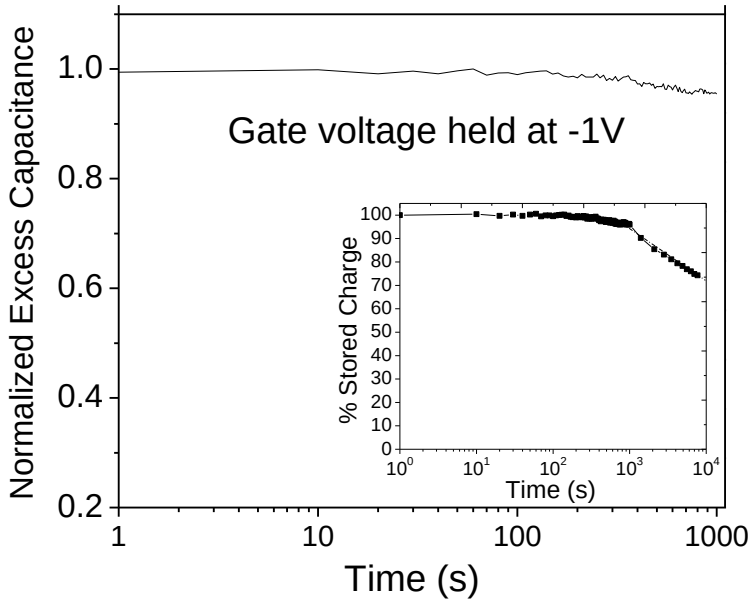


Fig. 5.2.6 Normalized charge decay characteristics of the 400°C annealed memory capacitor device after charging at -3V for 10secs.

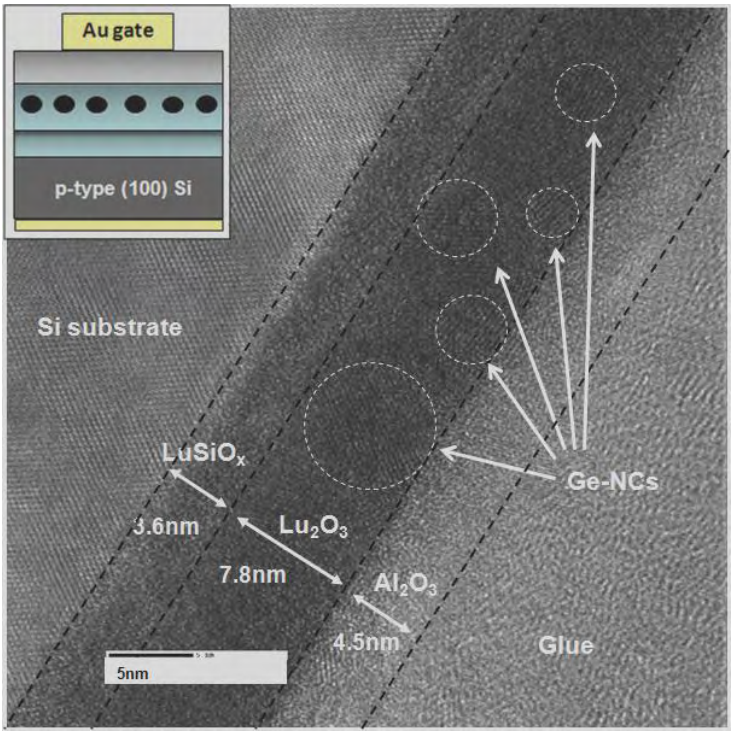
Charge leakage could occur either laterally by conduction between the nanocrystals or to the Si surface, with the former constrained by the tunnelling probability between nanocrystal islands, and the latter constrained by the quiescent bias state of the device which leaves the surface in depletion.[41] Initial fast decay characteristics have been observed by Kim et. al.[203] from the samples with nanocrystals that are not completely localized, and they further demonstrated slow capacitance decay characteristics with well-localized nanocrystals for the suppression of lateral charge transport. S. Huang et. al.[21] suggested that the long memory retention time is due to the build-up of opposing

electric field in the tunnel oxide, which hinders the discharge of remaining electrons in the nanocrystals. On the other hand, Shi et. al.[198,204] suggested that the long-term retention mode can be explained by the injected charges that are mainly stored in the deep traps and defects at the internal or surface of the nanocrystals instead of the conduction band. S. J. Baik et. al.[205] and C. M. Compagnoni et. al.[181] further modelled the discharging of nanocrystals based on deep level charge storage, which agrees with Shi's model. There are two possible discharging mechanisms for the loss of charges stored in the deep level traps, which involve the direct tunnelling of charges from the traps to the interface states in between the tunnel oxide and Si substrate, as well as the thermal de-trapping of electrons to the conduction band followed by back-tunnelling into the substrate.

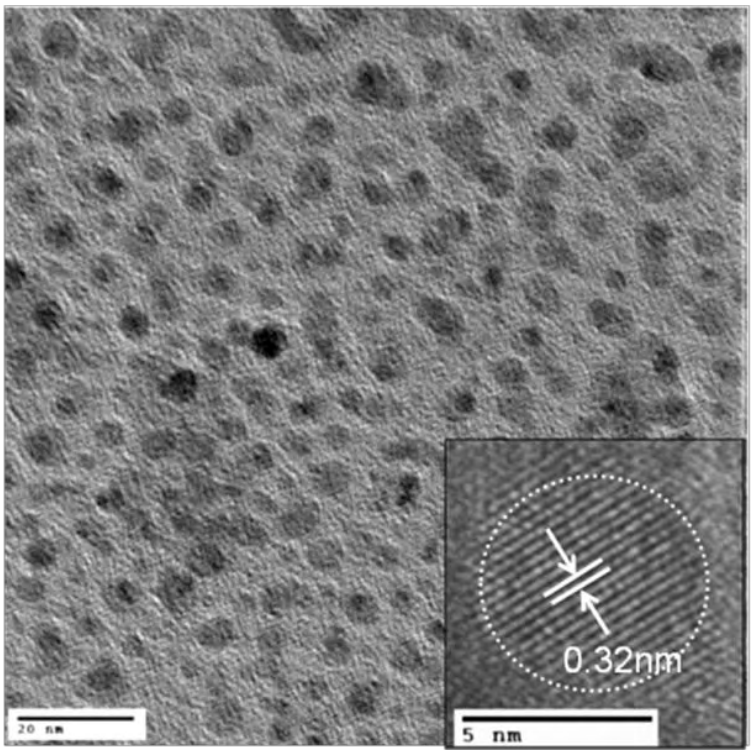
In the present work, good isolation of Ge nanocrystals in the amorphous Lu_2O_3 matrix effectively suppress initial fast decay characteristics due to lateral charge loss. In addition, a larger physical thickness of the high-k Lu_2O_3 tunnelling dielectric allows a reduction in direct tunnelling leakage compared to devices with the same EOT. The amorphous Lu_2O_3 could also play an important role in creating deeper trap energy levels at the nanocrystal/oxide interface for better retention. Carriers can be trapped at the internal and/or surface of the nanocrystals instead of the free band energy states, resulting in a larger potential barrier for tunnelling emission process. It is plausible to assume that the dominant charge loss process observed in this case is the back-tunneling of the trapped charges to the interface states at the Lu_2O_3/Si surface, as suggested by Shi et. al. Hence an improved retention is expected by reducing the interface states at the Lu_2O_3/Si surface with a good interfacial quality of the amorphous Lu_2O_3.

5.3 Optimization on Memory Structure

In order to achieve enhanced memory performance, a high temperature anneal process was adopted to induce intermixing of the oxide components for the realization of a self aligned graded barrier structure. Fig. 5.3.1 (a) shows the cross-sectional TEM image of the 800 ^{o}C annealed high-k dielectric stack, with Ge nanocrystals sandwiched between the Lu-based tunnel oxide and aluminium-based control oxide. The schematic illustration of the MIS capacitor device structure fabricated for memory characterization is shown in figure inset. Fig. 5.3.1 (b) shows the planar TEM image of the Ge nanocrystals embedded in the high-k dielectric after annealing at 800 ^{o}C. Nearly spherical-shaped nanocrystals with an areal density of 9 x 10^{11} cm^{-2} and size range of ~3-7 nm was observed in the amorphous Lu_2O_3 matrix. The lattice fringes of 0.32 nm shown in figure inset indicate single crystalline state of a (111) Ge nanocrystal of ~6 nm in diameter. No significant changes in the nanocrystal size and density was obtained upon high temperature anneal, although a small degree of coalescence was observed and associated with enhanced diffusion of Ge atoms.



(a)



(b)

Fig. 5.3.1 Cross-sectional TEM image of the Ge nanocrystals embedded in the amorphous $LuSiO_x$ / Lu_2O_3 / Al_2O_3 film stack after annealing at 800°C. Figure inset shows the schematic illustration of the device structure and (b) Planar TEM image of the Ge nanocrystals embedded in the film. Figure inset shows the high resolution image of a single crystalline Ge nanocrystal.

The elemental distribution of the films before and after 800 ^{o}C annealing was studied based on the SIMS depth profiles shown in Fig. 5.3.2. The Ge atoms were well-distributed within the middle region of 7nm thick before annealing, with a peak concentration near the interface with the Al_2O_3 control dielectric, which is in good agreement with the expected distribution of the deposition process. Partial segregation and redistribution of Ge was observed upon annealing at 800 ^{o}C. The Ge peak shows a strong broadening with a hump observed in the Al_2O_3 region, indicating out-diffusion of Ge into the Al_2O_3 capping layer. On the other hand, minimal in-diffusion was observed from the slope of the falling edge of Ge towards the substrate interface. The Si profile shows an incorporation of Si atoms into the high-k dielectric stack, suggesting plausible intermixing between Si and oxide components in the Lu_2O_3 high-k dielectric matrix.

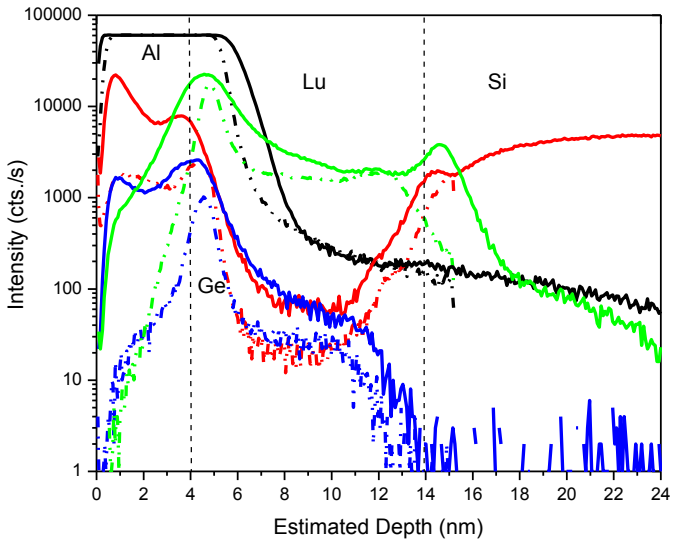


Fig. 5.3.2 SIMS depth profiles of Al, Si, Ge and Lu measured as a function depth into the Si substrate, with the solid lines plotted for the 800^{o}C annealed film and dashed lines for the as-deposited film.

Fig. 5.3.3 shows the RBS spectrum of the dielectric film stack annealed at 800 ^{o}C. Curve-fitting result reveals the formation of Lu-silicate and SiO_x interfacial layer after the annealing treatment. Hence a significant out-diffusion of Si from the substrate is resulted from the high temperature annealing. The diffusion process provides metallic Si nucleation sites which could facilitate the nucleation and growth process of Ge nanocrystals.[206] It has been reported that the incorporation of Si from the substrate into the dielectric significantly enhances the precipitation of Ge.[204] The diffusing Si atoms provide a larger source of reducing species besides the initially sub-stoichiometric Lu_2O_3 matrix, and the large diffusion kinetics results in a rapid displacement reaction for the precipitation of Ge nuclei and formation of SiO_x interfacial layer. Rapid nucleation and growth occurs with larger diffusion energy and atomic mobility provided for pronounced decomposition and self-organization. However, the high annealing temperature also results in enhanced diffusion of the Ge atoms leading to a reduction in Ge concentration from the middle layer which results in a competing process for the nucleation of Ge nanocrystals. The inter-diffusion of Si, Ge, Lu and Al atoms promotes the intermixing of oxide components that forms the resultant high-k barrier structure with graded composition. Concurrently, the formation of Ge nanocrystals remains dominant in the region near the Lu_2O_3/Al_2O_3interface due to a larger amount of excess Ge available for precipitation.

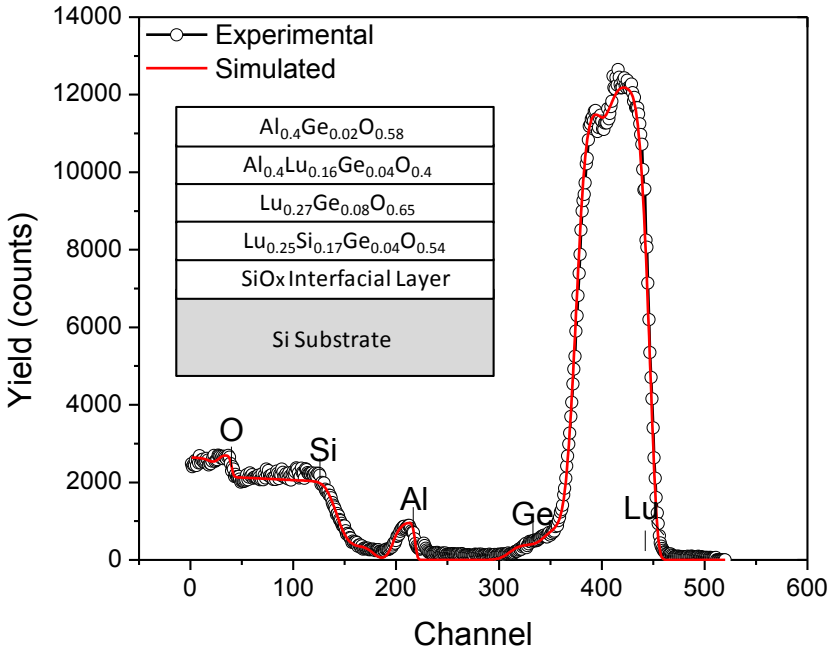
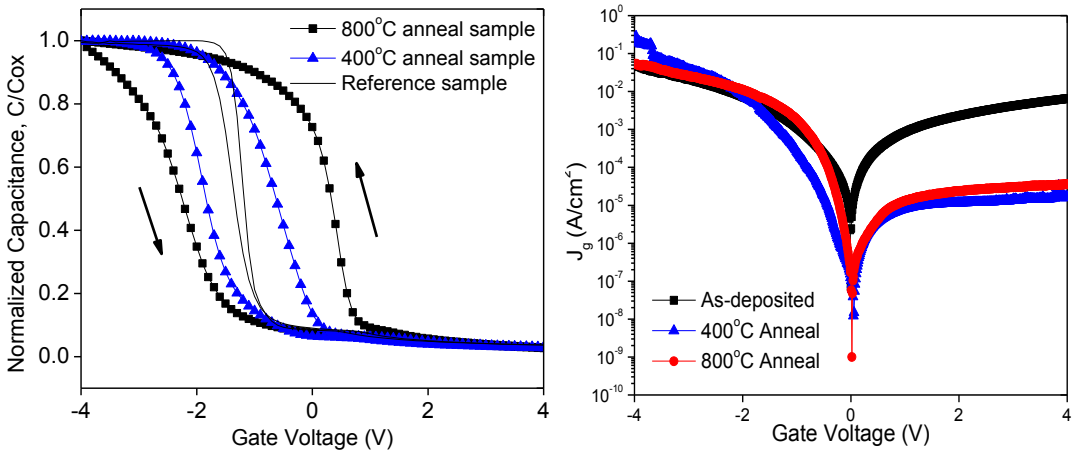


Fig. 5.3.3 RBS spectra for the 800°C annealed gate dielectric stack with the curve fitted using SIMNRA 6.03 for the evaluation of compositional depth distributions.

Fig. 5.3.4(a) shows the high-frequency (100kHz) C-V hysteresis loops obtained from the 400 °C and 800 °C annealed memory capacitor devices and the control device without nanocrystals. An enlarged memory window with a significant flatband voltage shift (ΔV_{FB}) of 2.7 V was obtained under a low operation voltage of +/-4 V, indicating an enhanced charge storage capability as compared to the ΔV_{FB} of 1.3 V for the 400 °C annealed device. The C-V curve of the reference sample without Ge incorporation exhibits a relatively small hysteresis (~0.2 V) related to essential trapped charges existing in the oxide or interface states. Hence major charge storage from the device with Ge nanocrystals is attributed to the trapped charges in the nanocrystals. Since no significant difference in nanocrystal size and density was observed between samples annealed at 400 °C and 800 °C, the improved memory behavior is associated to the modifications of the dielectric film stack composition after high temperature annealing. The intermixing of oxide components and enrichment of Si in the film results in the formation of a heterogeneous film stack,

leading to an enhanced charge trapping effect of the Ge nanocrystals associated with a larger memory window.[17] The graded barrier structure allows a more efficient programming due to modification of charge injection properties across a multi-dielectric stack structure.[207] In addition, a larger amount of charge trapping sites are available with additional contribution from different nature of trapping centers created between Ge and the surrounding Lu-based high-k dielectric matrix with gradual change in layer composition comprising $Lu_xSi_yO_z$, Lu_2O_3 and $Al_xLu_yO_z$. Fig. 5.3.4(b) shows the leakage current characteristics of the samples before and after annealing at 400 ^oC and 800 ^oC. The samples exhibit reduction in leakage current under inversion after annealing at 400 ^oC and 800 ^oC.



(a) (b)

Figure 5.3.4 (a) High-frequency (100kHz) capacitance-voltage (C-V) of the MIS memory capacitor device annealed at 400^{o}C and 800^{o}C plotted together with the reference curve without Ge and (b) Leakage current characteristics of the MIS memory capacitor device before and after annealed at 400^{o}C and 800^{o}C.

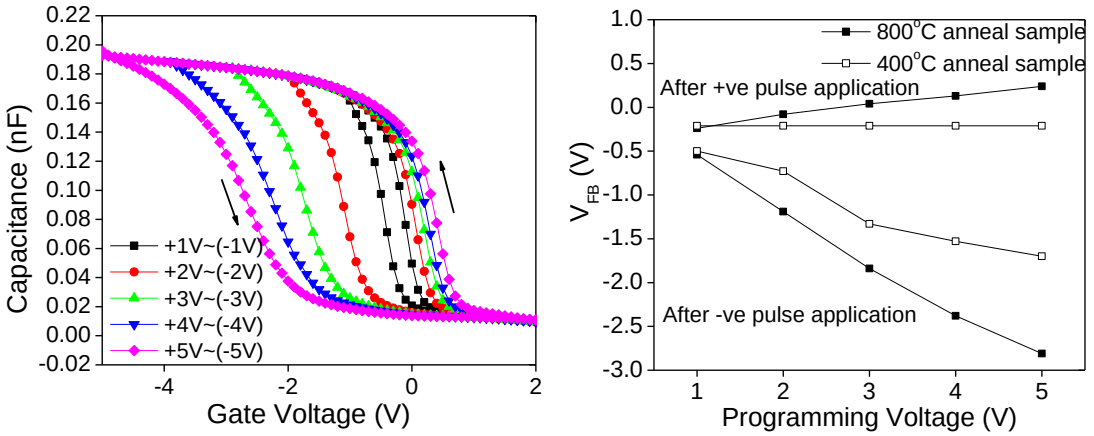
Table 5.3 shows the tabulated parameters extracted from the structural and electrical characterization of the samples. The samples exhibit reduction in leakage current under inversion after annealing at both 400 ^{o}C and 800 ^{o}C. A slight increase in leakage current under an accumulation bias of -1V was observed from the 800^{o}C annealed sample, likely related to a higher injection current with a smaller EOT and larger diffusion of Ge in the dielectric stack. A simultaneous EOT reduction was obtained upon 800 ^{o}C anneal despite an out-diffusion of Si into the film, suggesting the intermixing effect of Si, Ge, Lu and Al atoms on an overall increase in gate capacitance.

Table 5.3 Comparison of structural and electrical parameters of the MIS memory capacitor device before and after annealed at 400 ^{o}C and 800 ^{o}C.

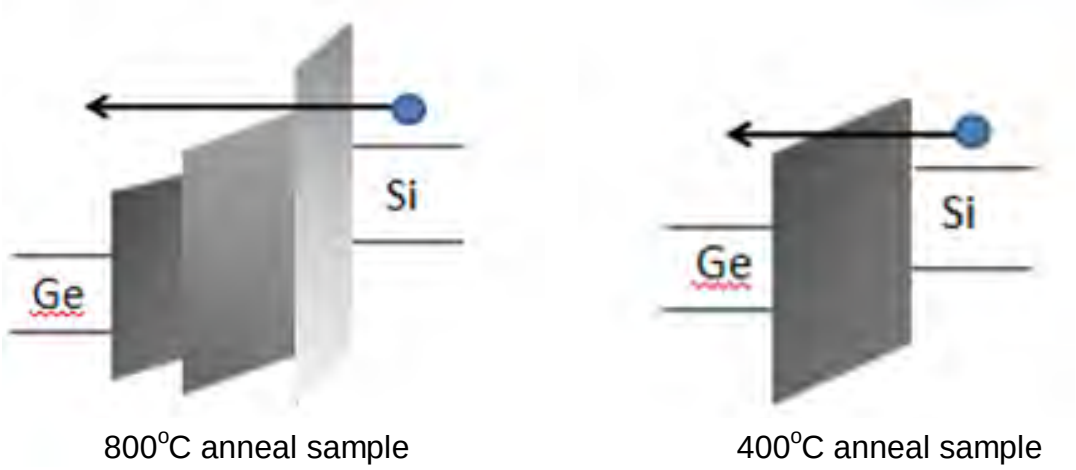
Sample	Size range (nm)	Density (cm^{-2})	ΔV_{fb} (V)	J_g @ -1V (A/cm^2)
As-deposited	2-3	7×10^{9}	-0.8	1.11×10^{-3}(EOT = 10.3nm)
400^{o}C anneal	3-9	7×10^{11}	1.3	2.63×10^{-4} (EOT = 9.8nm)
800^{o}C anneal	3-7	9×10^{11}	2.7	1.84×10^{-3} (EOT = 7nm)

The programming efficiency of the device was further investigated by performing C-V sweeps after applying varying pulse amplitude for 1s. Fig. 5.3.5 shows the C-V hysteresis loops with enlarged memory window obtained under increasing sweep amplitudes. The V_{FB} was extracted from the C-V curves and plotted as a function of the applied programming voltages in Fig.5.3.5 (b). Significant ΔV_{FB} from -0.96 V to -2.56 V was obtained from the 800 ^{o}C annealed sample with increasing negative programming voltages from -2 V to -5 V with respect to the initial C-V curve

obtained under a sweep range of +/-1 V before performing the charging measurements. A larger ΔV_{FB} from the 800 ^{o}C sample suggests a larger programming efficiency which could be related to the modification of charge injection properties across the graded barrier structure. Due to a large voltage drop over the low-k SiO_x barrier, the larger programming efficiency could be associated with strong direct tunneling current through the thin interfacial layer, as illustrated in the band diagram in Fig. 5.3.5 (c). On the other hand, the 400 ^{o}C sample experiences a smaller Fowler-Nordheim tunneling current through the single-layer Lu_2O_3 tunnel oxide.[35] In addition to a strong hole injection effect, progressive positive ΔV_{FB} was obtained under positive programming voltages indicating the occurrence of electron charging phenomena. This shows that both electron and hole injection are made possible by altering the gate stack structure for efficient write and erase, in contrast to the absence of electron injection for the 400 ^{o}C anneal sample. However, a smaller flatband voltage shift resulting from electron charging effect is related to smaller source for electron inversion and a higher electron emission rate of the structure. Further studies on the programming transient behaviour of the 800 ^{o}C annealed sample significant flatband voltage shift attained with 10 ms pulse width, with progressive shifting obtained from 10 ms to 10 s after negative bias programming application (see Fig. A5.2). This is comparable to other reported memory devices operating in the FN tunnelling regime.[4,5]



(a) (b)

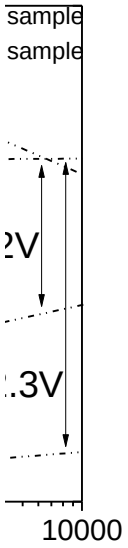


(c)

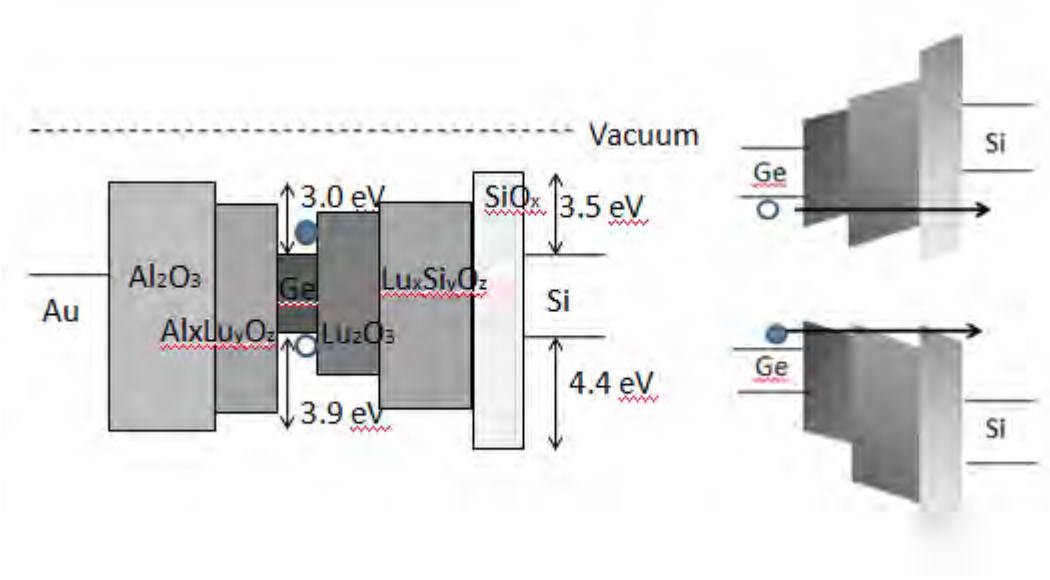
Figure 5.3.5 (a) C-V characteristics of the 800°C annealed MIS memory capacitor device after applying sequential increasing programming pulse voltages for 1s; (b) The flatband voltage shift as a function of programming voltages for the samples annealed at 400°C and 800°C and (c) Schematic illustration of the band diagram which shows different current injection behaviour through the graded tunnel barrier (800°C anneal sample) and single tunnel barrier (400°C anneal sample).

Retention characteristics of the 400 ^{o}C and 800 ^{o}C annealed memory capacitor devices are shown in 5.3.6 (a), after performing positive and negative stress voltages of +/-5 V for 10 seconds at room temperature. A gradual decrease of memory effect was observed for both samples, with a memory window of 1.2 V and 2.3 V retained for the 400 ^{o}C and 800 ^{o}C sample respectively, after a holding time of 10^4s. This shows that the 800 ^{o}C anneal sample allows a large voltage gap maintained to be easily current-sensed, with a measured retention time of 10^4 s for 25% charge storage loss. A faster charge storage loss was observed after applying positive stress voltage (i.e. negative charged state), further supporting the fact of higher electron loss rate due to a higher conduction band edge of the Ge nanocrystal above the conduction band minimum of the Si substrate.[208] On the other hand, a long retention time was observed from the positive charged state after negative stress voltage application. By considering solely the retention time of the trapped holes, a hole decay rate of 0.05 V / decade was estimated for the 800 ^{o}C anneal sample, implying a significant improvement in hole-based retention, as compared to a hole decay rate of 0.21V / decade estimated for the 400 ^{o}C anneal sample. The improved retention suggests a favorable band alignment of the layered dielectric stack for charge confinement, as depicted from the illustration of band profile in Fig. 5.3.6 (b). By assuming that the thick Al_2O_3 blocking oxide has negligible effect on the charge leakage, the energy band profile between the Ge nanocrystals and Si substrate is used to illustrate hole and electron tunneling through the stacked $SiO_x/Lu_xSi_yO_z/Lu_xO_y$ barrier under retention mode. Electron discharging through the multi-dielectric stack is possible due to a higher conduction band edge of Ge and the small potential barrier seen by the electrons to tunnel out into the Si substrate. The improved hole retention in the Ge nanocrystals is apparent due to a

large valence band offset combined with a large physical thickness of the dielectric stack barrier for effective hole confinement. Hence a small amount of hole discharge could only occur through thermal excitation followed by back-tunneling into the substrate conduction band and/or tunneling through the defects and interface states of the high-k dielectric stack. The program/erase cycling behavior of the 800 ^{o}C anneal sample is also shown in the inset of Figure 5.3.6 (a). Slight voltage shift of 0.1 V with minimal narrowing and degradation of the memory window was observed up to 10^5 write/erase cycles of +/-4 V, 100 ms gate disturbs. This shows stable charge trapping properties of the distributed nanocrystals and negligible creation of oxide defects under a low bias stress application.



(a)



(b)

Figure 5.3.6 (a) Retention characteristics of the 400°C and 800°C annealed memory capacitor device after applying positive and negative stress voltages of +/-5V for 10seconds at room temperature. Figure inset shows the endurance characteristics of the 800°C annealed device with pulse cycles of +/-4V applied for 100ms on the gate electrode. and (b) Schematic energy band diagram of the memory capacitor device structure comprising Ge nanocrystals sandwiched between $SiO_x/Lu_xSi_yO_z/Lu_2O_3$ tunnel dielectric and $Al_xLu_yO_z/Al_2O_3$ control dielectric stack under flatband condition; and illustration of electron (solid circle) and hole (open circle) discharging path through the tunnel dielectric stack under retention mode.

5.4 Effect of Dielectric Matrix and Trap Properties

The thermodynamic properties of Ge and dielectric host matrix play a role on the formation of stable Ge nanocrystals in the oxide matrix.[197] In order to study the effect of dielectric host material on the formation properties of Ge nanocrystals, XPS analysis was used to examine the chemical state of the films with Ge nanocrystals embedded in HfO_2 matrix. Fig. 5.4.1 shows the XPS spectra of Ge 3d core level for the dielectric films after annealing at 400 ^oC and 800 ^oC. The 400 ^oC annealed sample shows Ge 3d peak at 31.1 eV and 32.7 eV, corresponding to the formation of GeO_x and GeO_2 respectively. The oxidation of Ge has been attributed to the formation of Ge sub-oxides and Ge-O, Ge-Hf-O and Ge-Hf bonds at the Ge/HfO_2 interface.[209-211] It has been reported that Ge tends to form hafnium germinate when dispersed in HfO_2 matrix,[86,212,213] which leads to the creation of low quality GeO_x/$HfGeO_x$ trap states that could act as leakage path. A higher annealing temperature at 800^oC shows similar peaks at 30.8 eV and 32.6 eV indicative of oxidized Ge, without significant changes in chemical state composition. However, elemental state Ge is expected to exist in a lower concentration in the bulk of the film, which was not detected under the surface-sensitive analysis. The different chemical state composition observed with incomplete reduction of Ge oxides in the HfO_2 matrix could be related to a larger solubility of Ge in HfO_2 and lower chemical stability of Ge in the surrounding HfO_2 dielectric matrix.

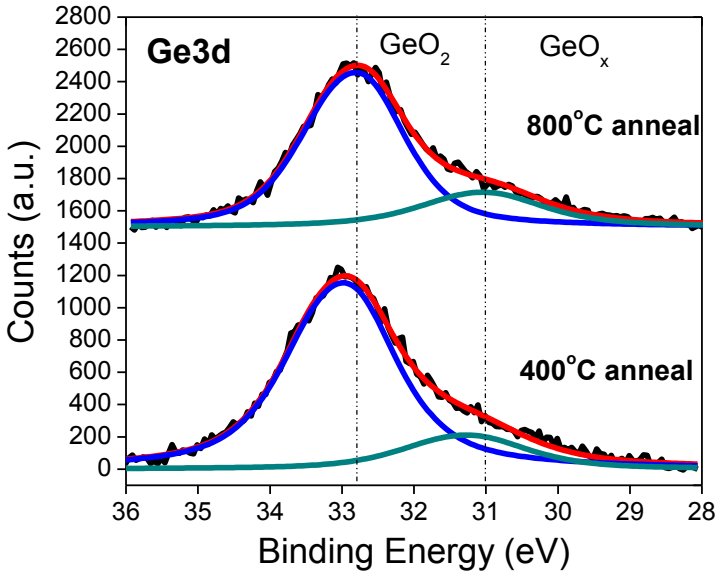
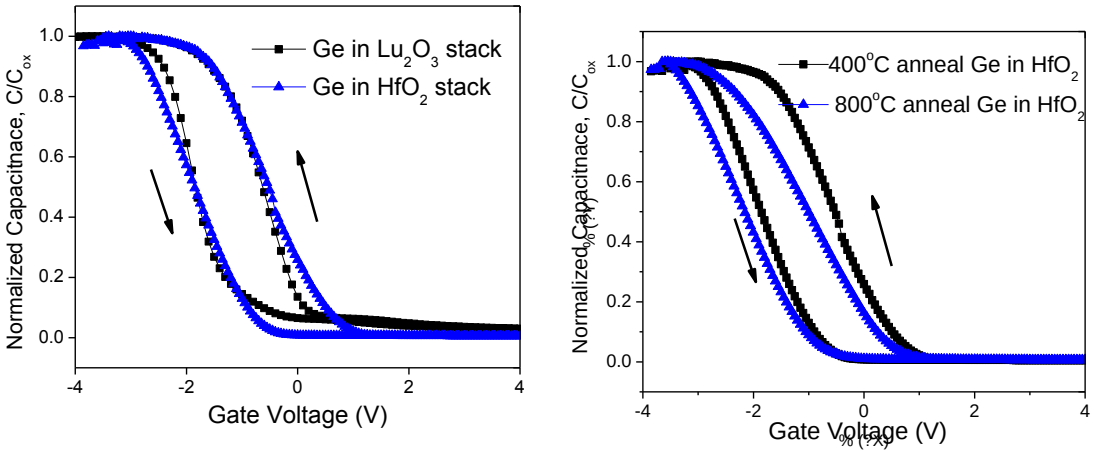


Fig 5.4.1 Ge 3d core level XPS spectra of the films with Ge nanocrystals embedded in HfO_2 dielectric after annealing at 400°C and 800°C.

The role of dielectric host matrix on the memory characteristics was further studied by performing high-frequency (100kHz) bi-directional C-V sweeps on the 400 °C and 800 °C annealed memory capacitor devices. Fig. 5.4.2 (a) shows the C-V comparison between the devices with Ge nanocrystals embedded in Lu_2O_3 and HfO_2 high-k dielectric after annealing at 400 °C. A similar ΔV_{FB} of ~1.3V was obtained from both samples, implying dominant contribution of nanocrystal-related charging effect on the memory behaviour for devices annealed at 400 °C. Upon annealing at 800 °C, instead of an enhancement of memory window as found in the Lu_2O_3 high-k dielectric, a degradation of the memory effect along with a gentler slope of the C-V curve was observed from the device with HfO_2 high-k dielectric matrix, as shown in Fig. 5.4.2 (b). This provides an indication of the role of interface states on the memory degradation of the device with HfO_2 high-k dielectric matrix annealed at 800 °C. Plausible diffusion and penetration of Ge nanocrystals into the tunneling oxide and

oxide/substrate interface during the high temperature anneal process resulted in the creation of interface states, leading to fast charge storage loss via the defect-related leakage paths.



(a) (b)

Fig 5.4.2 High-frequency (100kHz) C-V characteristics of the memory capacitor devices with (a) Ge nanocrystals embedded in Lu_2O_3 and HfO_2 high-k dielectric after annealing at 400°C and (b) Ge nanocrystals embedded in HfO_2 after annealing at 400°C and 800°C.

It has been reported that pure HfO_2 crystallizes at a low temperature of 500 °C, and the existence of Ge may decrease the crystallization temperature of the host matrix leading to localized crystallization.[86,209,213] The crystallization of HfO_2 dielectric matrix could facilitate diffusion of Ge nanocrystals. Due to the volume expansion upon crystallization, the formation of nanocrystalline regions results in the development of stress in the nanocrystal-matrix system.[214,215] Stress relaxation process requires diffusion of atoms (vacancies) away (towards) the developing crystalline phase.[216] The evolution of stress relief process during thermal annealing treatment has been reported to be governed by the diffusive flux of atoms away from the local nanocrystal growth region.[214] The formation of local crystallized region of HfO_2 promotes drives the diffusion of Ge atoms away from the Ge/HfO_2 interfaces for

stress relaxation and accommodate for the crystallization process. The diffusion of Ge nanocrystal throughout the dielectric introduces additional defect levels near the Si interface, which serve as interface charge traps.

This resulted in a large increase in gate leakage current after 800 ^{o}C anneal, as shown in Table 5.4. In addition, the incompletely reduced GeO_x in the film act as low quality trap states, which also contribute substantially to the increased gate leakage current. With the help of these trap states, the charges stored in the nanocrystals could easily tunnel back to the Si substrate via trap-assisted tunneling, resulting in the degradation of memory window observed.

Table 5.4 Comparison of the electrical parameters of the MIS memory capacitor devices with Ge nanocrystals embedded in Lu_2O_3 and HfO_2 high-k dielectric matrix annealed at 400 ^{o}C and 800 ^{o}C.

Sample	ΔV_{fb}(V)	Jg @ -1V (A/cm^2)
400^{o}C anneal Lu_2O_3	1.3	2.63 x 10^{-4} (EOT = 9.8nm)
800^{o}C anneal Lu_2O_3	2.7	1.84x 10^{-3} (EOT= 7nm)
400^{o}C anneal HfO_2	1.3	4.24 x 10^{-5} (EOT = 10.8nm)
800^{o}C anneal HfO_2	1.2	1.24 x 10^{-3} (EOT = 12.9nm)

5.5 Summary

In summary, this chapter presents the promising potential of a memory structure comprising Ge nanocrystals in lanthanide-based Lu_2O_3 for low voltage non-volatile memory applications. The introduction of high-k dielectrics allows a large ΔVth

(1.32V) achieved under low operating voltage (4V), which addresses the weak coupling issue of nanocrystal memory. A charge storage model was discussed for the memory structures with different trap properties, constituting Ge oxide-related defects and distributed Ge nanocrystals. A comparison with state-of-the-art nanocrystal memory devices demonstrates the advantage of large memory window obtained under low voltage operation of the memory structure, as shown in Table 5.5.

Table 5.5 Performance comparison of the Ge nanocrystal memory device with state-of-the-art devices.

	IBM[217]	UC Berkeley[79]	Atmel and CEA/LETI[88]	Samsung[218]	U. Texas, Austin[219-221]	NUS[222]	This work[223]
Voltage	3V	4V	10V	8V	8V	7V	4V
ΔVth	0.65 V	0.4V	3V	1V	1V-1.6V	1.5V	1.3V
Retention	1hr (85°C)	>1000min (RT)	2E4 (RT)	38 years (85°C)	1E4 (RT)	1E3 (85°C)	1E4 (RT)
Endurance	>1E9	>1E9	N/A	>1E6	1E4	>1E6	N/A
Remarks	Si NCs /SiO_2	Ge NCs /SiO_2	Pt NCs /SiO_2	Si NCs /NON	SiGe NCs /HfO_2	GeNCs /HfAlO	GeNCs /Lu_2O_3

Further barrier modification approach was investigated by thermally-induced intermixing of oxide components for the realization of a self-aligned lanthanide-based graded high-k barrier structure. Enhanced memory properties was achieved with a significantly enlarged memory window (2.7V) achieved under a low operation voltage (4V). The trade-off between program/erase efficiency and data retention was

addressed, with simultaneous improvement in charge storage and retention. Table 5.6 summarizes the comparison of the device performance with state-of-the-art engineered nanocrystal memory devices, which demonstrates combined advantage of large memory window, low operation voltage and data non-volatility.

Table 5.6 Performance comparison of the graded barrier nanocrystal memory device with state-of-the-art engineered devices.

	IBM[224]	U. Texas, Austin[225,226]	Max Planck Institute[227,228]	Samsung[229]	U. Cornell[230]	U. National Tsing Hua[231]	This work [232]
Voltage	6V	8V	8V	15V	8V	10V	4V
ΔVth	1.6V	1.6V	2.8 V	5.5V	1.5V	4.8V	2.7V
Retention	1E4 (RT)	1E4 (RT)	1E5(RT)	>1E5(RT)	1E4 (RT)	1E5 (RT)	1E4 (RT)
Endurance	>1E9	1E4	N/A	>1E5	N/A	N/A	>1E5
Remarks	Template-assisted assembly	Core shell SiGe NCs/HfO_2	Multilayer NCs	Pd NCs on SiO_2/HfO_2	Si NCs on SiO_2/HfO_2	Au NCs on $Al_2O_3/HfO_2/SiO_2$	Ge NCs /Lu_2O_3/ $LuSiO_x$

The study on the effect of high-k dielectric matrix shows significant role of the surrounding dielectric material on the chemical properties and stability of the Ge nanocrystals. Electrical characterization shows that the memory window is governed by the high-k dielectric properties, with more stable charge traps existing in the chemically stable amorphous Lu_2O_3 matrix. Hence the crystallization effect and chemical stability of the high-k dielectric matrix should be taken into account in the selection of nanocrystal and dielectric materials.

CHAPTER 6 Self-Assembled and Controlled Synthesis of Ge Nanocrystals based on Chemical Synthesis Method

6.1 Introduction

Physical techniques for the fabrication of nanocrystals generally require high temperature and expensive manufacturing processes which produce broad distribution of nanocrystal size and density. Chemical synthesis methodologies employing solution process may alleviate these problems by providing low temperature methodologies for the formation of mono-dispersed colloidal Ge nanocrystals.[231,232] Moreover, the solution-based synthesis offers numerous advantages such as chemical stability, control over nanocrystal surface termination, and provides a low cost, large area coverage and high yield assembly technique favorable for large scale electronic applications.[24,25,48] Although solution synthesis of nanocrystals is well developed, reports of procedures that result in the single crystals of nanometer size Ge crystals often indicate stringent need on high pressure and/or temperature to induce crystallization due to the strong covalent bonding. [233,234]

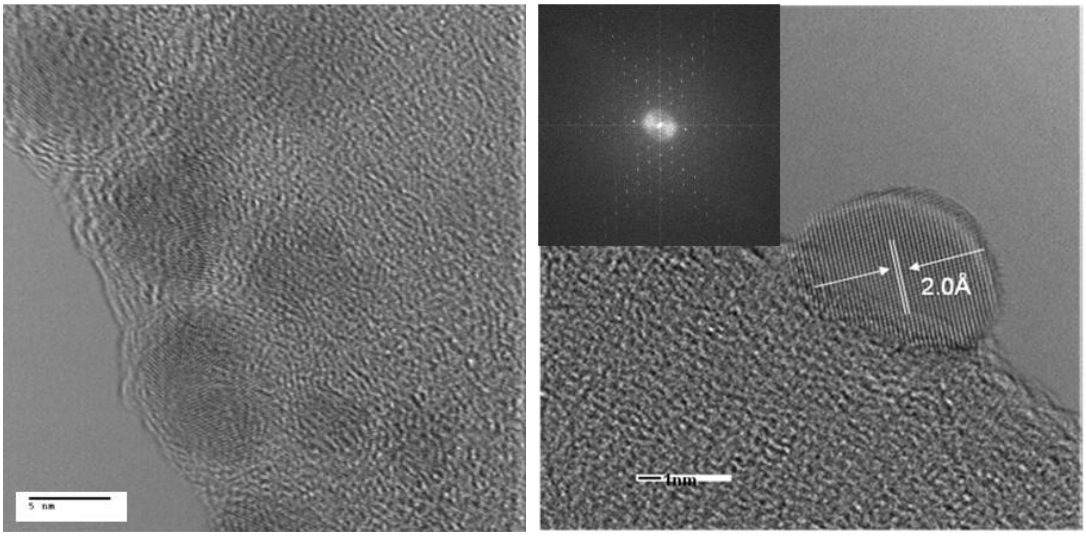
In this work, the motivation of adopting a solution-based chemical synthesis approach derives from the ability to provide adequate control on the nanocrystal size, density and surface properties. This approach uses a sonochemical reduction method for the synthesis of Ge nanocrystals, without the need of high temperature and pressure, whereby crystallization process could be induced by the acoustics energy provided by the ultrasonic reaction. In addition, it is possible to tailor the density and distribution of nanocrystals on different substrates by exploiting covalent interaction between the nanocrystals and functionalized substrate surfaces. The chemical grafting of

nanocrystals on oxide surfaces allows the transfer of the colloidal synthesis methodology for memory device application, with further possibility of exploring the size, density and surface effects on the electrical behaviour. The potential application of such architecture is demonstrated by the realization of memory device with significant charge storage.

6.2 Formation of Ge Nanocrystals

Figure 6.2.1 shows the transmission electron micrograph (TEM) image of the synthesized Ge nanocrystals prepared from 1.85 mM $GeCl_4$ precursor solution with 5 ml octanol. A size distribution of 5-7 nm with a mean diameter of 5 nm was obtained. Possible size control of the nanocrystals was attributed to tenable encapsulation of the nanocrystals by the octanol capping ligands leading to steric stabilization of the nanocrystals. The adsorption of octanol onto the surface of the particles provides repulsive force to screen the attractive interaction of particles that tend to cause agglomeration.[47,106] Figure 6.2.1(b) shows the high resolution TEM (HRTEM) image of a single Ge nanocrystal ~7 nm in diameter, with the observed lattice fringes indicating evident single crystalline state of the nanocrystal. The observed lattice planes with a d-spacing of 2.0 Å corresponds to the (220) lattice spacing of Ge, which shows that the diamond cubic structure of bulk Ge is retained in the nanoscale regime. The structure of the nanocrystal was further investigated from the constructed Far Fourier Transform (FFT) pattern shown in figure inset, which matches to the [110] zone axis of the diamond cubic Ge crystal structure. Reports have shown that high temperatures ~400 ^{o}C and high pressures of 200 atm are required to induce crystallization of Ge nanocrystals.[107,226] In this ultrasonic-mediated reduction

synthesis, the formation of Ge nanocrystals at room temperature could arise from the acoustic cavitation phenomena, with the crystallization process induced by the formation, growth and collapse of the bubbles in the THF solvent. The crystallinity of the final product is determined by the reaction site, whereby a good crystallinity is expected with the reactions occurring at the interface of the bubbles.[107,114,115]



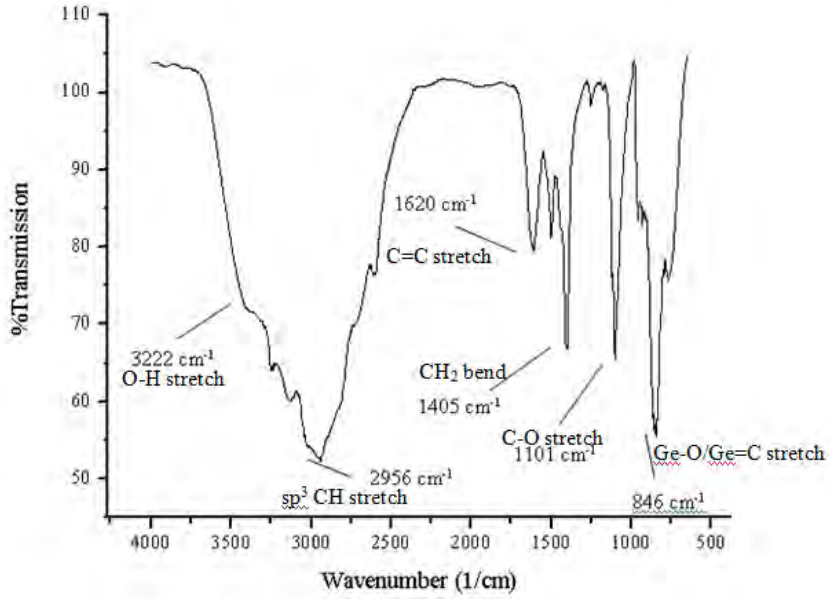
(a) (b)

Fig. 6.2.1 (a) TEM image of the octanol-stabilized Ge nanocrystals synthesized using 1.85mM $GeCl_4$ concentration and (b) HRTEM image of a single Ge nanocrystal, with the FFT image shown in figure inset.

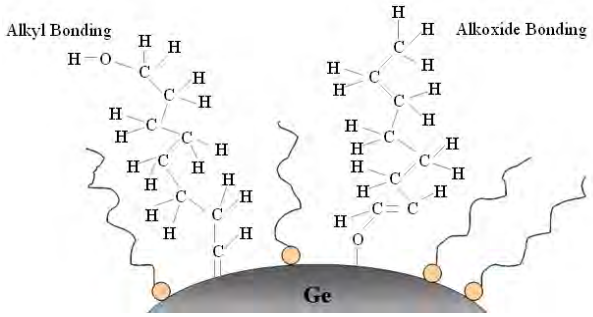
6.2.1 Effect of Capping Agent

The effect of octanol attachment on the colloidal Ge nanocrystals was investigated by performing Fourier Transform Infrared (FTIR) analysis on the Ge colloids deposited on the glass substrate, with the spectrum shown in Fig. 6.2.2 (a). The broad hydroxyl stretch at 3222 cm^{-1} and the Ge=C stretch at 846 cm^{-1} with the hydrocarbon related stretching at 2956 and 1405 cm^{-1} suggests possible reaction between Ge with a primary carbon of the octanol to form a structure with a terminal hydroxyl group. The alkyl bonding mechanism has been observed from the attachment of octanol on Ge nanocrystals from the previous reported work.[47,233-237] In addition, an alternative anchoring scheme could exist with the observations of the peak at 846 cm^{-1} related to

Ge-O stretch. A covalent alkoxide bonding formation is possible through the reaction of Ge and the octanol oxygen with elimination of the hydroxyl hydrogen. This is supported by the presence of C=C stretch seen at 1620 cm^{-1}. The FTIR results confirm that the Ge nanocrystal surface is chemisorbed by a hydrocarbon layer, and the detection of Ge=C and C=C bonds suggests two possible bonding mechanisms, as shown from the bonding scheme in Fig. 6.2.2 (b). With the formation of a strong bonding between the octanol capping ligand and the nanocrystals, the octanol provides an effective surface passivation to the nanocrystals for improved stability of the colloidal solution.



(a)

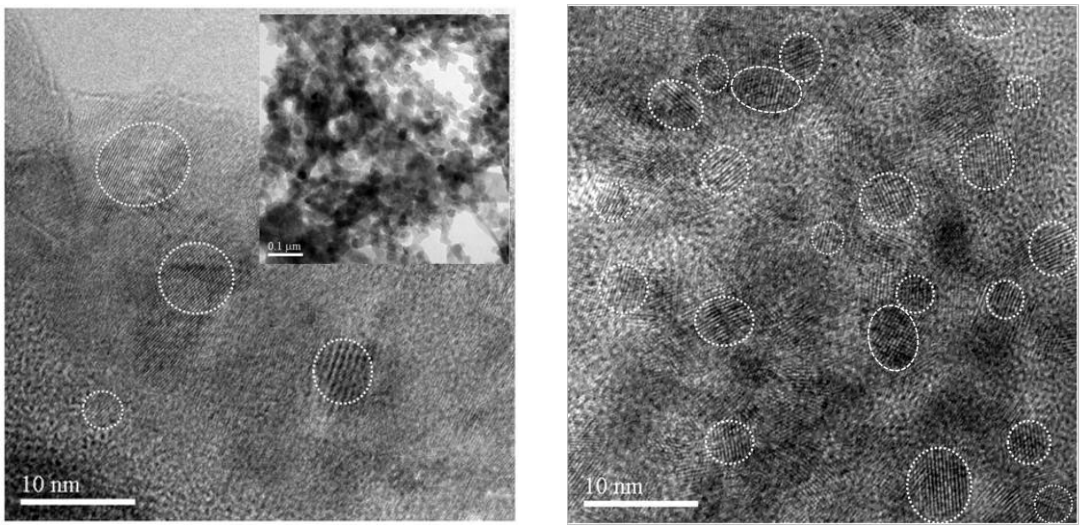


(b)

Fig. 6.2.2 (a) FTIR spectra of the Ge colloids and (b) possible bonding scheme between octanol and Ge.

6.2.2 Effect of Precursor Concentration

The effect of precursor concentration on the nanocrystal size and distribution was further studied by comparing the TEM images of the Ge nanocrystals synthesized using 1.85mM $GeCl_4$ and 1.1mM $GeCl_4$ precursor solution. Fig. 6.2.3 (a) shows a sparse distribution of nanocrystals observed from the sample synthesized using 1.85mM $GeCl_4$, with an average nanocrystal size of 5.5 ±1.6 nm. The low magnification image of the nanocrystals in figure inset shows severe agglomeration of nanocrystals, which forms a large amount of aggregates on the carbon-coated copper grid. On the other hand, the more uniform distribution of nanocrystals synthesized using 1.1mM $GeCl_4$ indicates an improved dispersion of the Ge nanocrystals associated with a lower concentration of precursor solution. An average nanocrystal size of 3.9 ±0.8 nm was obtained with a large surface coverage. The lower $GeCl_4$ concentration results in a slight reduction of nanocrystal size with a narrow size distribution and minimal agglomeration, although a small amount of nanocrystals aggregate together due to random attachment on the carbon-coated grid. This implies that the formation of Ge nanocrystals is not limited by the available nucleation sites provide by the reduction of $GeCl_4$, but rather the effective surface passivation of the nanocrystals by the octanol capping ligand. Insufficient stabilization of the nanocrystals is prone to aggregate formation due to the existence of Van der Waals force.



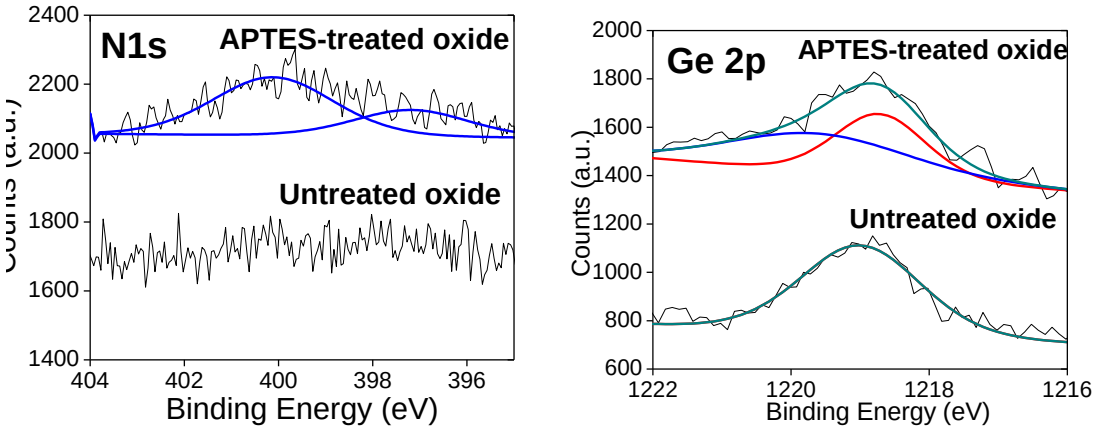
(a) (b)

Fig. 6.2.3 TEM image of the octanol-stabilized Ge nanocrystals synthesized using (a) 1.85mM $GeCl_4$ concentration with low magnification image shown in figure inset and (b) 1.1mM $GeCl_4$ concentration.

6.3 Substrate Functionalization and Self-Assembly of Ge Nanocrystals

The formation of (3-aminopropyl) triethoxysilane (APTES) self-assembled monolayer (SAM) on the oxide surfaces was indicated with a contact angle of 63.7° measured for the SiO_2 surface and 65.5^o measured for the HfO_2 surface upon silanization, which agrees with the contact angle measurement results for successfully modified surface.[238] In order to investigate the chemical composition of the Ge nanocrystals attached to the modified oxide substrate, x-ray photoelectron spectroscopy (XPS) analysis was performed on the HfO_2 samples drop-casted with Ge colloidal solution. The presence of N1s peaks detected from Fig. 6.3.1 (a) confirms the successful formation of APTES layer terminated with terminal amine groups, which is absent in the untreated oxide sample. The N1s spectrum reveals a lower binding energy peak at 397.2eV with a content of 30.3% and a higher binding energy peak at 400.1eV with a content of 69.7%. The first peak component at 397.2eV is related to the presence of free amine group from the APTES layer.[239,240] The higher binding energy peak at 400.1eV can be attributed to the N atoms in N=C bonding configuration, as reported

by Chowdhury.[119,227,228] This substantiates the chemical interaction between the $–NH_2$ group and octanol-capped Ge nanocrystals, leading to covalent attachment of the nanocrystals on the oxide surface via the linking group. The Ge 2p spectrum in Fig. 6.3.1 (b) shows an additional broad peak at 1219.6eV besides the peak at 1219eV upon APTES treatment of the oxide surface, which suggests chemical shift of the Ge 2p state due to interaction between the Ge colloids and the modified oxide surface.



(a) (b)

Fig 6.3.1 (a) N1s and (b) Ge 2p core level XPS spectra of the films with Ge nanocrystals deposited on the bare oxide and APTES-treated oxide surface.

The chemical binding interaction between the colloidal Ge nanocrystals and the APTES-modified oxide surface was further studied by performing FTIR analysis, as shown in Fig. 6.3.2. The role of the surface-terminated amine groups as the linkage group is further evidenced by a noticeable peak at $2319cm^{-1}$ corresponding to the N=C stretching vibration of the $–NH^+$=C- group which is absent in the reference sample without APTES modification. Successful formation of APTES self-assembled monolayer (SAM) on the oxide surface is further confirmed from the characteristic $1449cm^{-1}$ band attributable to $–N-CH_2$ bond present in APTES molecule .[240,241]

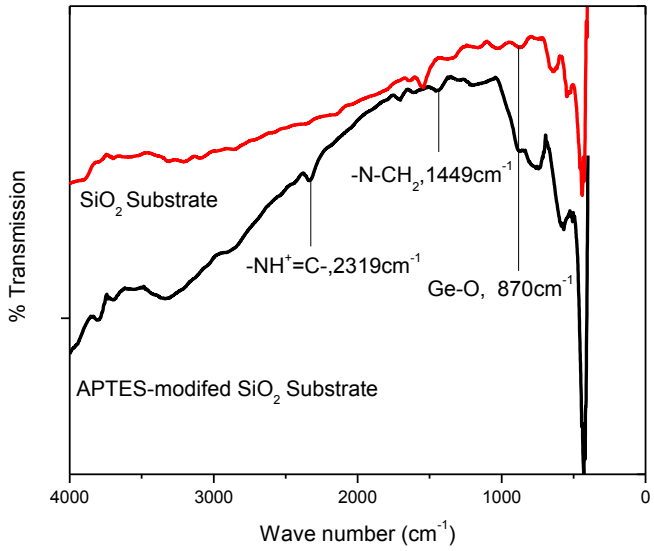


Fig 6.3.2 FTIR spectrum of the Ge colloids deposited on SiO_2 and APTES-modified oxide surface.

The N=C band observed from the APTES-modified oxide surface suggests possible bond interaction between the alkyl group from the octanol capped nanocrystals and the protonated amino-terminated monolayer on the oxide surface. The alkyl-terminated nanocrystals potentially attach to the surface-terminated $–NH_2$ groups from the APTES layer, taking advantage of the chemical functionalities for nanocrystal self-assembly. The possible bonding scheme of the nanocrystals on the APTES-modified oxide surface is shown in Fig. 6.3.3.

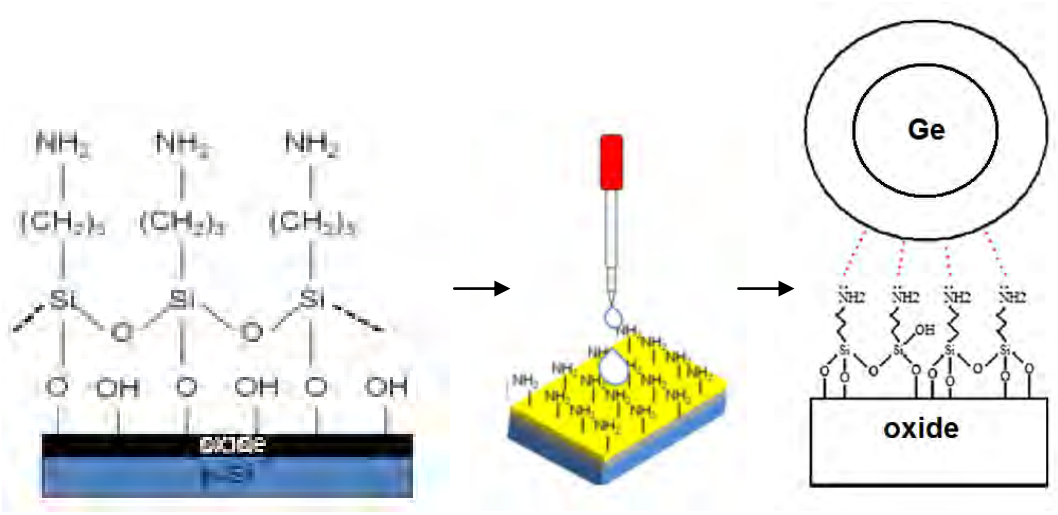
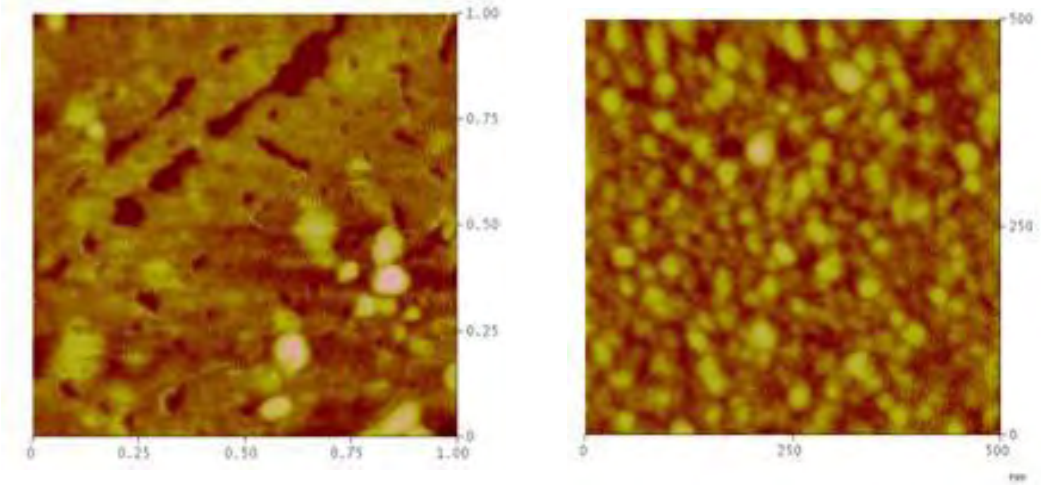


Fig 6.3.3 Schematic illustration of the APTES-modified oxide surface and subsequent drop-casting of Ge colloids, resulting in chemical binding interaction between the terminal $–NH_2$ group and the octanol-capped nanocrystal.

Fig. 6.3.4 shows the atomic force microscopy (AFM) images of the Ge nanocrystals deposited on the oxide surface before and after chemical treatment. The oxide surface without chemical treatment shows local clustering of the particles with a poor surface coverage, indicating non-uniform attachment of nanocrystal on the oxide surface. The formation of agglomerates can be explained by the attractive Van der Waals forces between the particles.[242] Fig. 6.3.4 (b) shows a more homogeneous distribution of Ge nanocrystals on the APTES-modified oxide surface, with a mean particle size of ~3nm estimated from the particle height, since the resolution in the vertical direction is not limited by the tip shape. This suggests that the amino-silanization of oxide surface plays an important role on the selective attachment of nanocrystals, whereby chemical grafting is favored due to possible bond interaction between the substrate and nanocrystals. The chemisorption process enhances the binding of nanocrystals on the oxide surface with a significantly improved areal density of ~6.7 x $10^{10}$$cm^{-2}$ estimated from the AFM image.



(a) (b)

Fig 6.3.4 (a) AFM images of the 1.8 mM concentration Ge nanocrystals deposited on the SiO_2 surface (a) before and (b) after APTES functionalization.

6.4 Charge Storage Capability and Charge Storage Behavior

6.4.1 Effect of Nanocrystal Properties

The charge storage behavior of the metal-oxide-semiconductor (MOS) capacitors fabricated from the samples with Ge nanocrystals sandwiched between as-grown SiO_2 tunnel oxide and Al_2O_3 control dielectric (fig. 6.4.1 inset) was studied by performing bi-directional capacitance-voltage (C-V) sweeps at a frequency of 100kHz. The control device was fabricated from the 2nm SiO_2 / 10nm Al_2O_3 dielectric stack without the incorporation of Ge nanocrystals. Fig. 6.4.1 shows the effect of different nanocrystal properties synthesized under different processing conditions on the memory behavior. It was found that the control device without Ge nanocrystals

exhibits hysteresis behavior of ~1.4V, likely related to the charge traps existing in the bulk dielectric film and/or at the SiO_2/Al_2O_3 interface. Similar hysteresis behavior was observed from the devices containing Ge nanocrystals synthesized under a $GeCl_4$ concentration of 1.85mM, with a rightward voltage shift observed from the device synthesized without octanol capping agent attributable to Ge-O dangling bonds that could act as electron traps. On the other hand, the device synthesized under a $GeCl_4$ concentration of 1.1mM displays a significantly enlarged flatband voltage shift, ΔV_{fb} of ~2.2V. The comparison of the memory properties indicates an important role of nanocrystal distribution for effective charge storage, which agrees with a more uniform distribution of nanocrystals with minimal agglomeration obtained under a lower concentration of precursor solution from the TEM analysis.

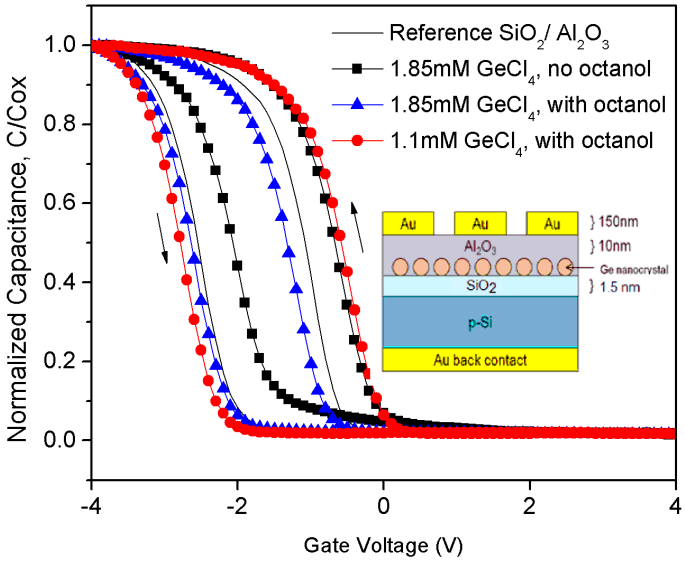


Fig 6.4.1 C-V hysteresis behaviour of the MOS capacitor devices with and without Ge nanocrystals synthesized under different processing conditions, and the device schematic illustrated in figure inset.

The ΔV_{fb} contributed from the Ge nanocrystals could be extracted from the ΔV_{fb} differences from the control device. As shown in Table 6.1, an effective ΔV_{fb} of 0.8V

obtained signifies a large charge storage density of 9.7 x $10^{12}$$cm^{-2}$ resulting from the nanocrystal contribution of the device synthesized using 1.1mM $GeCl_4$. This large amount of charge storage implies dominant contribution of the nanocrystal surface effect on the memory effect, with large amount of storage sites created at the interface between Ge and octanol capping ligand.

Table 6.1 Comparison of the flatband voltage shift and corresponding charge storage density for the devices synthesized under different processing conditions.

Sample	**ΔV_{fb} (V)**	**$q=C*\Delta V$ (C/cm^2)**
Reference SiO_2 / Al_2O_3	1.4	3.8 x 10^{12}
1.85mM $GeCl_4$, no octanol	1.3	2.9 x 10^{12}
1.85mM $GeCl_4$, with octanol	1.4	3.8 x 10^{12}
1.1mM $GeCl_4$, with octanol	2.2	1.35 x 10^{13}

6.4.2 Effect of Surface Functionalization

In order to demonstrate the feasibility of integrating the colloidal synthesis methodology and self-assembly technique with high-k gate dielectrics for memory device application, subsequent study on the memory behavior was carried out using HfO_2 as the high-k gate dielectric stack. After surface functionalization of the cleaned HfO_2 surface by the APTES SAM layer, the contact angle changes from 38.5^o to 65^o,

and this confirms the modification of the dielectric surface with terminal amino groups. The Ge colloids synthesized under the optimized condition with 1.1mM $GeCl_4$ concentration were used to provide a better distribution of nanocrystals on the HfO_2 tunneling dielectric, followed by encapsulation of the nanocrystals by HfO_2 blocking dielectric. The C-V hysteresis behavior of the MOS capacitor devices are shown in Fig. 6.4.2. The control device without Ge nanocrystals exhibits a small ΔV_{fb} of ~0.3V, related to pre-existing traps in the HfO_2 high-k dielectric.[115] A larger ΔV_{fb} of ~1.1V was obtained with the incorporation of Ge nanocrystals, indicating major charge storage contribution from the nanocrystal-related charge trapping sites.

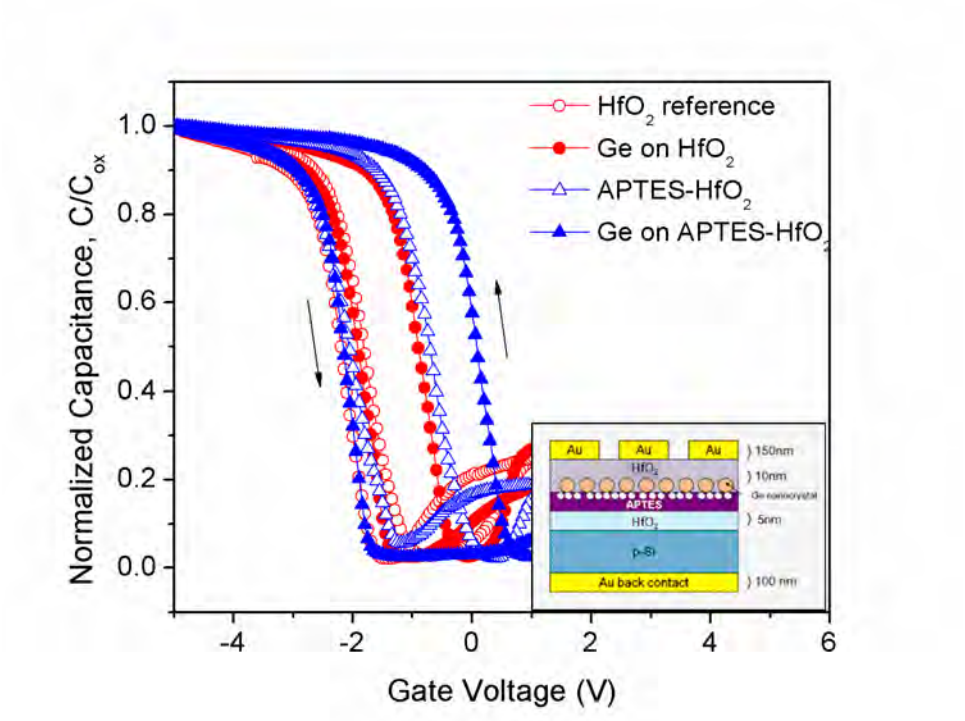
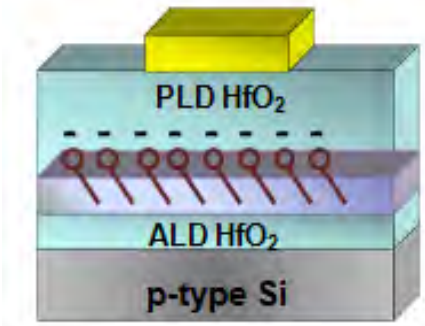


Fig 6.4.1 C-V hysteresis behaviour of the MOS capacitor devices with Ge nanocrystals synthesized from 1.1mM $GeCl_4$ deposited on HfO_2 high-k dielectric with and without APTES functionalization, , and the device schematic illustrated in figure inset.

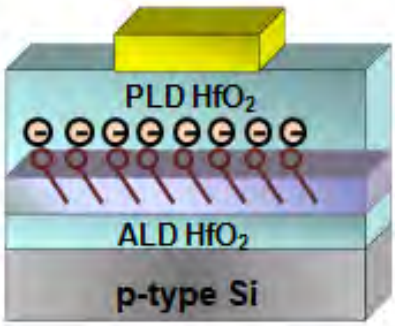
Distinct C-V hysteresis with a ΔV_{fb} of ~1.1V was also observed from the control device functionalized with APTES SAM layer, attributable to charge trapping effects of the organosilane molecules or the APTES/HfO_2 interface. Charge storage and pronounced hysteresis has been observed from different SAMs, including nitro-based molecules on metal surfaces,[114] nitrogen-related molecular defects in aminopropyl-seisesquioxine films,[240,241] F-terminated SAM[243,244] and APTES on thermally grown SiO_2.[245,246] Possible mechanisms for the hysteresis effect include the effect of mobile ions, carrier injection effect, ferroelectric-like model, interface charging and lateral electron hopping effect. In the present work, a distinct counterclockwise hysteresis observed associated with a positive ΔV_{fb} with respect to the HfO_2 sample without APTES modification indicates significant trapping of negative charges in the device. The observed counterclockwise hysteresis suggests the effect of carrier injection from the Si substrate into the charge trapping sites existing in the APTES and/or APTES/HfO_2 interface. The negative charge trapping effect is likely ascribed to the large electron affinity of the amine group and possible charge induced by the polarized organosilane molecules.[247] Due to absence of covalent binding between the NH_2 functional groups and the inorganic HfO_2 control dielectric deposited using pulsed laser deposition technique, electron trap sites originating from the amino groups and/or oxygen vacancy could exist at the APTES/HfO_2 interface. The dipole interaction between APTES and high-k dielectric could also contribute to the charge trapping effect between the APTES/HfO_2 interface.

The dispersion of Ge nanocrystals on the APTES functionalized HfO_2 evidently induces a larger ΔV_{fb} of ~2.2V, with a more positive V_{fb} shift ascribed to the trapping of electron charges. The presence of Ge nanocrystals provides confined electron trap

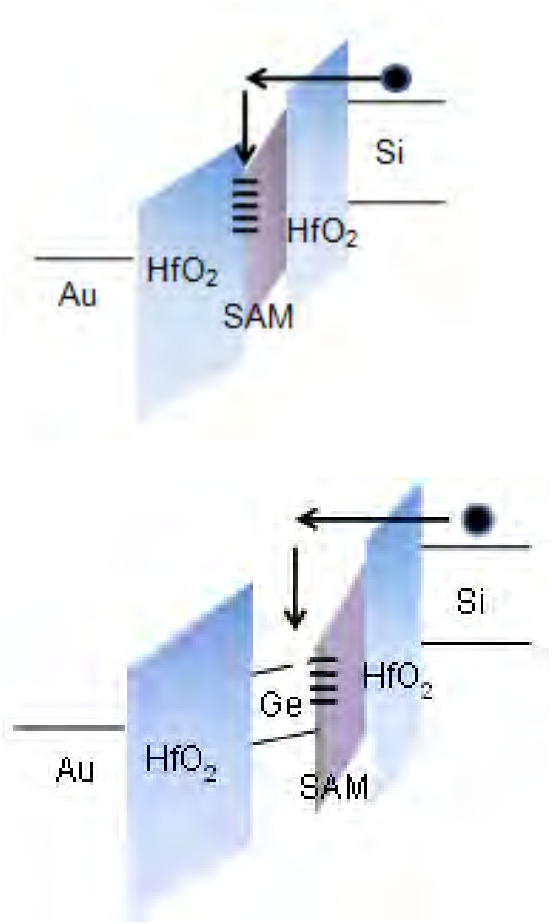
sites for more effective trapping of the electrons, thereby enlarging the memory window. Fig. 6.4.2 shows the trapping effect contributed by the APTES SAM layer and the enhanced charge storage effect assisted by SAM-induced charge injection into the Ge nanocrystal storage sites. Further characterization on the retention properties of the MOS capacitor devices shows good retention properties of the device with Ge nanocrystals deposited on APTES functionalized HfO_2 as compared to the unstable APTES charge retention (Fig A6.1). Further work on the minimization of charge trapping effects of the APTES SAM layer using a high vacuum low temperature anneal process is expected to provide an improved device performance associated with a better assembled nanocrystal layer on the modified dielectric surface.



(a)



(b)



(c) (d)

Fig 6.4.2 Schematic illustration of the charge trapping scheme of (a) HfO_2/APTES/HfO_2 device and (b) device with colloidal Ge nanocrystals deposited on the APTES-functionalized HfO_2 ; and the schematic energy band diagram showing possible charge injection into the (c) APTES/HfO_2 interface traps and (d) confined Ge nanocrystal trapping sites.

6.5 Summary

A solution-based chemical synthesis method for the formation of nanocrystals is demonstrated as an attractive low temperature process for large area and high density memory application. A reduction in nanocrystal size with a more narrow size distribution obtained from a lower concentration of precursor solution suggests the

feasibility of tuning the nanocrystal size and density, by ensuring effective surface passivation of the Ge nuclei with the octanol capping agent. Surface modification of SiO_2 and high-k dielectric layer with amino functional group is feasible to promote chemical grafting and uniform self-assembly of Ge nanocrysals. A larger memory effect was observed from the device upon immobilization on the functionalized dielectric layer, although further efforts on minimizing additional trapping effects from the SAM layer are required. The synthesis technique for tailoring the nanocrystal size and distribution, combined with adequate nanocrystal density control via the self-assembly methodology provides a potential approach to address the relationship between the memory performance and size, distribution and surface properties of the nanocrystals.

CHAPTER 7 CNT-based Ge Nanocrystal Memory

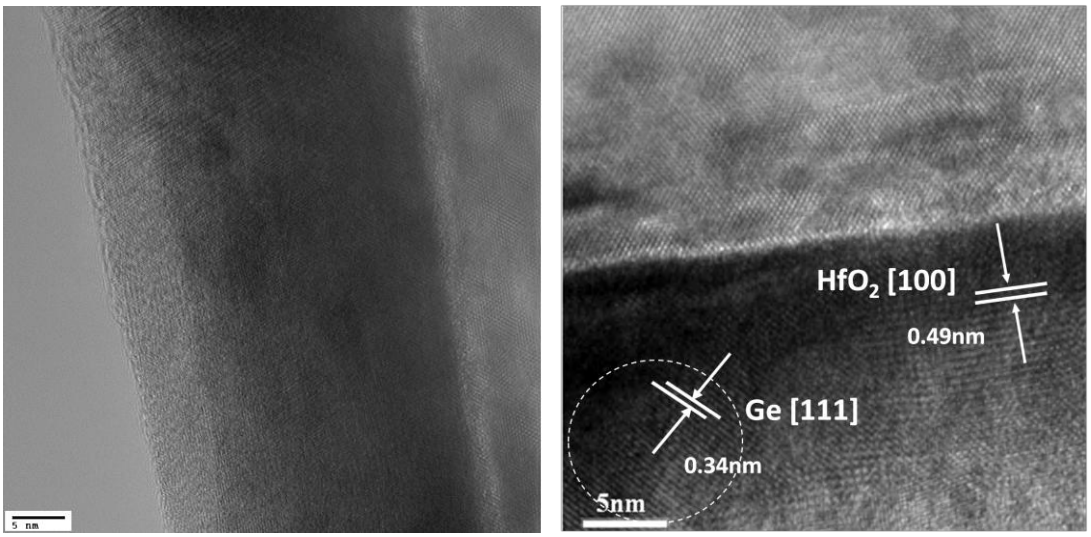
7.1 Introduction

Nanocrystal memories typically display small threshold voltage windows ΔV_T due to weak electrostatic coupling,[248,249] which could impose severe limitations to the current sensing circuit during data readout. Several methods have been proposed to improve the electrostatic control of the channel charge by increasing nanocrystal density[119] and size,[248] and alternatively by optimizing the aspect ratio of the cell channel W/L.[250]

In this chapter, CNT channel was adopted as alternative device architecture aimed to obtain enhanced threshold voltage shift associated with reduced channel width and large charge sensitivity of CNT.[251] Although significant hysteresis has been reported for CNT-based memory[167], there is lack of study on the trap properties and controllability. In order to obtain a large I_{on}/I_{off} ratio for flash memory operation, it is also important to study the charge transport and injection properties to ensure a large memory window and current rectification under low operation voltage. This work shows an effective tuning of the transport and memory behavior enabled using a hybrid memory device comprising Ge nanocrystals embedded in a HfO_2 high-k dielectric. Charge-induced modulation of the Schottky barrier leads to an effective increase in the read-out conductance ratio of two to three orders magnitude under low voltage operation, associated with a large memory window of ~5.3V. A more controllable and reliable memory effect was demonstrated from Temperature-dependent retention and endurance measurements demonstrate a more controllable and reliable memory effect due to stable charge storage in deep Ge nancrystal traps, as compared to shallow HfO_2 defect states.

7.2 Device Structure and Configuration

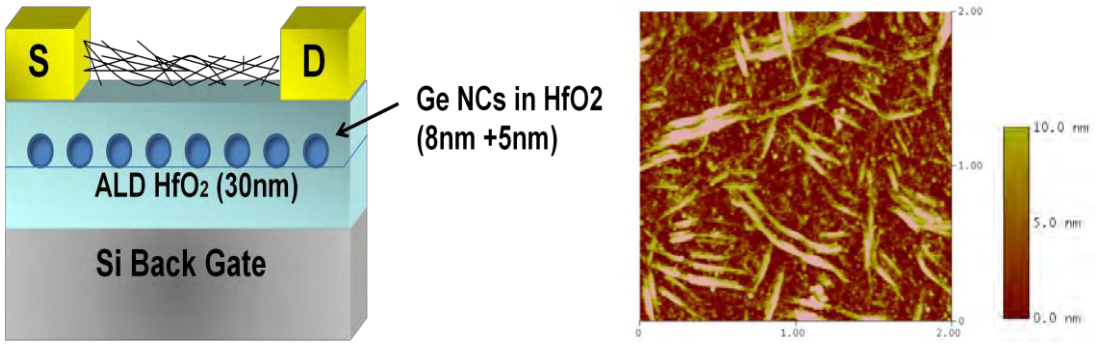
The structural properties of the HfO_2 film and Ge nanocrystals were examined from the cross-sectional TEM images in Fig. 7.2.1. Lattice fringes were observed from the 25nm thick HfO_2 film, indicating the formation of polycrystalline microstructure in between the amorphous zones. Fig. 7.2.1 (b) shows the HRTEM image of the sample with Ge nanocrystals embedded in the HfO_2 high-k dielectric. Nanocrystalline grains with lattice spacing, d of ~0.49nm and 0.34nm were observed, which can be attributed to [100] interplanar spacing of the HfO_2 in monoclinic phase and [111] interplanar spacing of the Ge nanocrystals respectively. This indicates the formation of Ge nanocrystals within the monoclinic HfO_2 during thermal annealing, which results in difficulties in distinguishing Ge nanocrystals from the HfO_2 grains.



(a) (b)

Fig. 7.2.1 Cross sectional TEM image of (a) 25nm thick HfO_2 film and (b) Ge-incorporated HfO_2 film after 400°C anneal with lattice fringes corresponding to HfO_2 and Ge.

Fig. 7.2.2(a) shows the schematic illustration of the back-gated CNT memory device with 10-µm source-drain channel length and 500-µm channel width. The CNT distribution on the substrates is shown from the AFM image of the CNT network in the region between the source-drain electrodes in Fig. 7.2.2 (b). Interconnected nanotube bundles were observed between the source-drain electrode gaps, which form a continuous pathway, acting as the channel in the FET configuration.



(a) (b)

Fig. 7.2.2 (a) Schematic illustration of the device structure with CNT network drop-cast on top of the HfO_2 high-k dielectric with embedded Ge nanocrystals, connected by patterned Au source and drain contact pads. (b) 2 x 2 µm AFM image of the CNT network dispersed between the Au electrode gaps.

7.3 Charge Transport and Charge Storage Characteristics

Room temperature drain current (I_{ds}) versus gate potential (V_{gs}) measurement of the CNTFET devices with Ge nanocrystals embedded in bottom HfO_2 high-k dielectric show good p-type FET behavior with a significant memory effect reflected in the reproducible hysteresis shown in Fig. 7.3.1. Out of 10 devices measured, a large threshold voltage shift of ~5.3 ± 0.5V was consistently obtained under a small gate voltage sweep range between -5V and 5V. This shift provides two distinct memory states (ON and OFF, represented as '1' and '0') with a read-out conductance ratio of 10^3, having a standard deviation of 16%. Since no difference in the electrical characteristics was observed under ambient and vacuum conditions, we can conclude

that the effect of the ambient environment and adsorbed water molecules on the memory behavior is negligible. Hence, the observed hysteresis is indicative of reversible charge injection between the CNT and underlying charge trapping sites in the high-k dielectric. The large memory window is attributed to a high density of charge trapping sites combined with high charge sensitivity of the nanotube due to an enhanced 3-D electric field, relative to a planar structure [249,252]. In addition, a well-defined current switching behavior obtained under a low operation voltage signifies a strong gate electrostatic coupling effect associated with the utilization of high-k dielectrics [253,254].

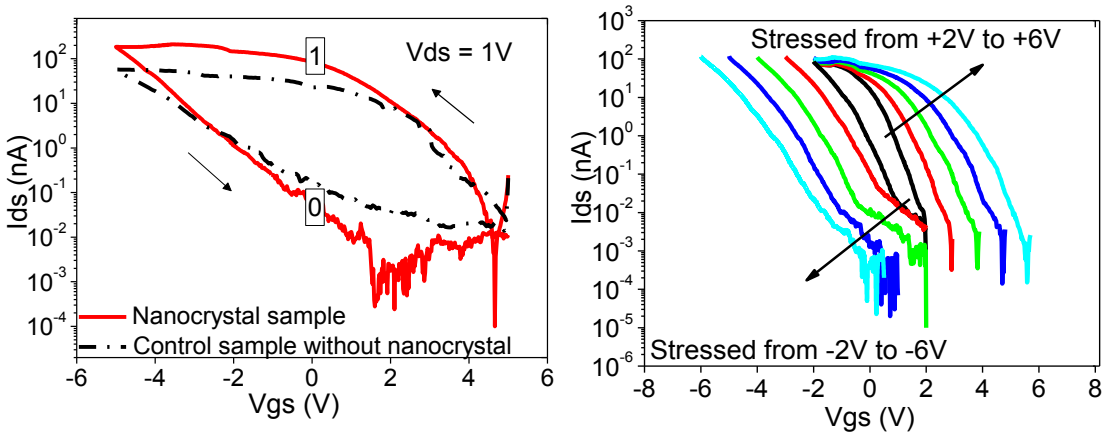
On the other hand, the control devices without Ge nanocrystals exhibit a slightly smaller hysteresis of ~5.0 ± 0.4V, with a smaller I_{ON}/I_{OFF} ratio of ~400 for memory read-out, having a standard deviation of 29%. It has been reported that hafnium-based oxide shows a large amount of V_{th} shift after stress bias application due to pre-existing traps , indicating possible charge storage in the HfO_2 dielectric trap states between the nanotube and Si gate of the control sample. The formation of nanocrystalline grains in the HfO_2 high-k dielectric could act as localized defects capable of trapping charges, resulting in the observed hysteresis. Although the integration of high-k dielectrics enables a low operation voltage due to strong gate coupling, the control devices exhibit a larger distribution of drain leakage current, pointing to an increased Schottky barrier transparency with the utilization of high-k dielectrics.

Since the measured gate leakage properties are of the same order of magnitude for both samples with and without nanocrystals (See Supplementary Data in Appendix,

Fig. S1), the better-controlled conductance states observed from the devices with Ge nanocrystals is attributed to the local electric field created by the trapped charges in the nanocrystals, leading to a suppressed gate-induced drain leakage (GIDL). With more consistent and narrowly distributed memory behavior of the devices with Ge nanocrystals, it is plausible to assume that the charges are preferentially stored in discrete nanocrystals / nanocrystal-related traps in addition to the dielectric trap states due to strong electrostatic interaction with the CNTs.

In order to study the charge trapping behavior, the threshold voltage (V_{th}) shifts were monitored from the I_{ds}-V_{gs} curves (Fig. 7.3.1b) after applying sequentially increasing write and erase back-gate pulses for one second without a simultaneous source-drain voltage. An initial 2 V bias sweep was measured before performing the charging measurements in order to obtain the quasi-neutral condition. An increasing number of electron and hole trapping events were observed from the progressive shifting of V_{th} towards more positive and negative voltages upon further charge injection with increasing positive and negative pulse voltages. The observed charging behavior agrees with reported simulation results, which show a linear variation of threshold voltage shift with the amount of charge if the charges are discrete and confined in a fixed position . This experimental observation provides further evidence that major charge storage occurs through efficient charge tunneling into the localized nanocrystals due to a larger capture cross section , although different types of traps could exist in the structure. Both the electron and hole charging behavior show a large V_{th} shift efficiency, which is significantly larger than the efficiency demonstrated from previously reported work utilizing oxide trap charging . The low driving fields

for write / erase of the memory, combined with the large V_{th} shift efficiency, offer a distinct advantage for low power and multilevel memory operation.



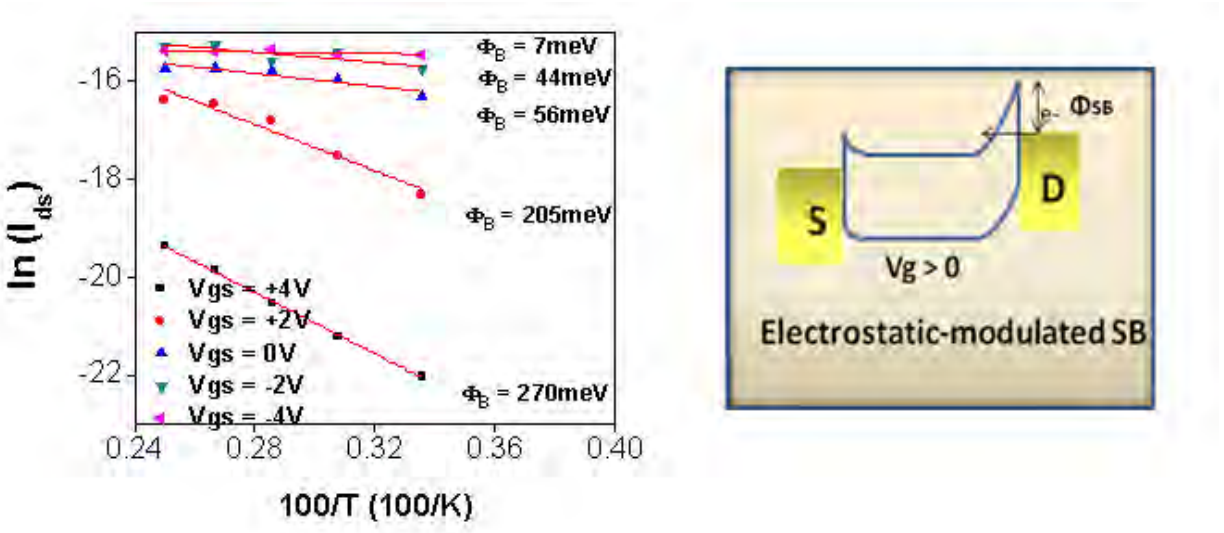
(a) (b)

Fig. 7.3.1 (a) Drain current (I_{ds}) vs. gate voltage (V_{gs}) curves for the CNT device with and without Ge nanocrystals in the HfO_2 bottom high-k gate dielectric, under a gate voltage sweep of +/-5 V and a drain voltage of V_{ds} = 1 V. ON (1) and OFF (0) states are defined at V_{gs} = 0 V. (b) I_{ds}-V_{gs} curves obtained at V_{ds} = 1 V after performing sequential increasing positive / negative gate voltage pulse from +/-2 V to +/-6 V for 1 s.

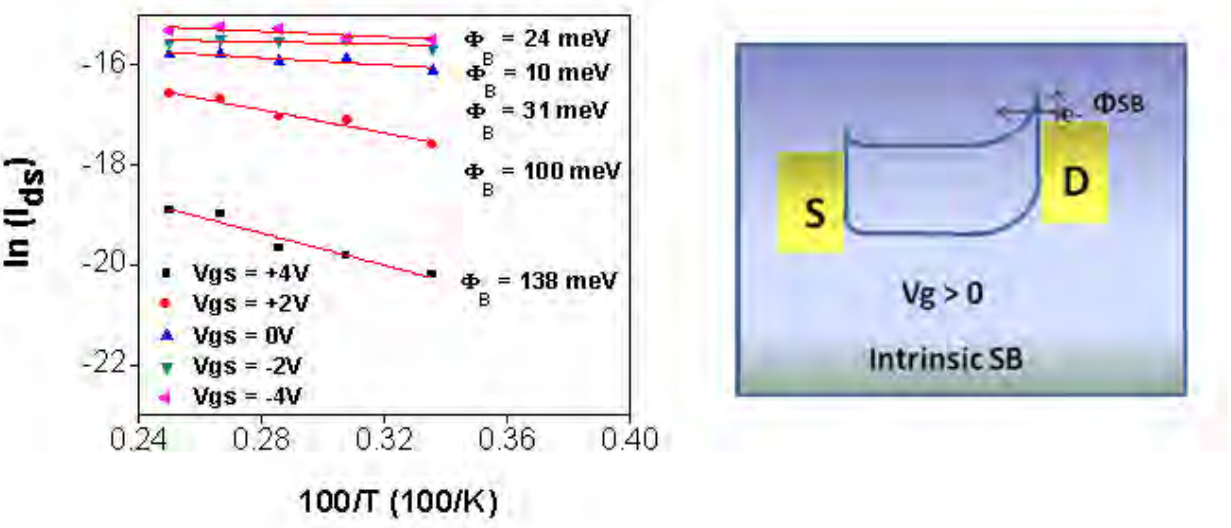
High temperature I_{ds}-V_{gs} measurements were performed on the devices with and without Ge nanocrystals in order to investigate their charge transport and trapping properties. In these experiments, a small, temperature-dependent hysteresis was observed (see Supplementary Data in Appendix, Fig. S2). The temperature-dependent Arrhenius plot of ln (I_{ds}) vs. 1/T in Fig. 7.3.2 displays a linear relation, indicative of Schottky barrier-modulated charge transport dominated by thermionic emission through the metal-CNT contacts. The Schottky barrier height, Φ_B (activation energy), was extracted in both devices from the slope of the linearly-fitted Arrhenius plot, with Vg varying from -4 V to +4 V. The extracted Φ_B for both devices exhibits an asymmetric behavior for electron and hole injection. The high work function Au electrode forms a low barrier contact for hole injection due to a favorable line up of the CNT valence band with the metal Fermi level, E_F. Under negative voltage

application, we obtained a low Φ_B of 7 – 56 meV and 10 – 31 meV for the nanocrystal sample and control sample, respectively, with a nearly ohmic contact for p-type operation.

In addition to the Schottky barrier height, the carrier conductance is also affected by the Schottky barrier width, which depends critically on the electrostatic environment Although the utilization of high-k dielectric allows an increased channel conductance by reducing the Schottky barrier width for increased transparency, the improved ON-current due to Schottky barrier thinning also tends to increase the OFF-current, which is detrimental for passive power optimization. In this case, despite a comparable Schottky barrier magnitude for the ON-state conduction obtained from both devices, the incorporation of Ge nanocrystals in the high-k dielectric results in an effective increase in Φ_B from 100 – 138 meV to 205 – 270 meV under positive voltage application in the OFF state. The experimental Φ_B value extracted from the control HfO_2 sample is close to the reported values of 80 -145 meV for a Au-CNT contact .



(a)

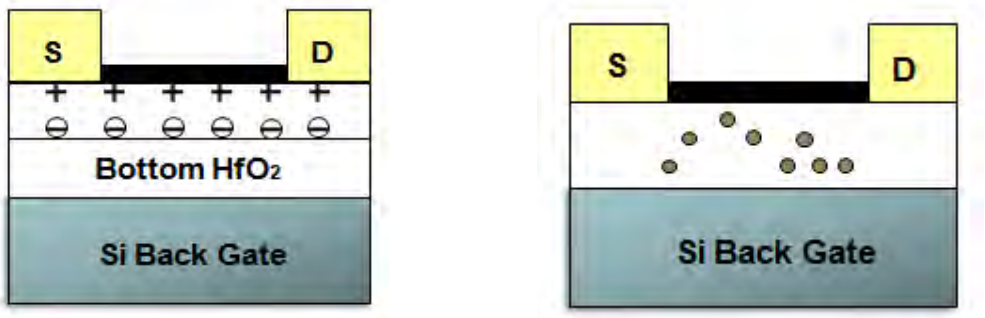


(b)

Fig. 7.3.2 Arrhenius plot (ln (I_{ds}) vs. 1/T) of the Au-contacted CNT device (a) with and (b) without the incorporation of Ge nanoparticles, measured at V_{ds} = 1 V. The corresponding band diagrams with and without local charge doping effect are also illustrated to explain the modulation of Schottky barrier height due to electrostatic charging effects.

This finding supports the notion that the suppressed excess OFF state leakage current with the incorporation of nanocrystals can be attributed to localized charge-induced effective tuning of the barrier height. The channel conductance is therefore limited by the additional potential barrier imposed by the charge stored in the nanocrystals which

effectively modulates the current transport utilizing a simple electrostatic doping approach. As illustrated in Fig. 7.3.3 (a), the trapped electrons in the nanocrystals create electric fields, which are higher in the contact regions due to fringing effects at the electrodes. The induced dipoles effectively increase the local metal work function, which provide a larger potential barrier that suppresses electron injection for improved OFF state properties. The electronic doping effect of the nanocrystals significantly modifies the local electric field and Fermi level alignment near the drain contact. This leads to effective tuning of Schottky barrier height, which provides favorable charge transport behavior due to an increased band asymmetry, with a large barrier for electron injection in the OFF state and a small barrier for hole injection in the ON state. On the other hand, minimal electrostatic doping effect is observed from the HfO_2 control sample due to random distribution of trapped charges in the dielectric, as shown in Fig. 7.3.3 (b).



(a) (b)

Fig. 7.3.3 Schematic illustration of the device structure with the distribution of trapped charges in (a) discrete Ge nanocrystals embedded in HfO_2 high-k dielectric and (b) random trapping sites in the control HfO_2 high-k dielectric.

7.4 Charge Retention and Trap Properties

Room temperature charge retention behavior of the CNT device with and without Ge nanocrystals is shown in Fig. 7.4.1 (a), with the drain current monitored at a read voltage of V_{gs} = 0 V and V_{ds} = 1 V. The measurements were taken after performing a

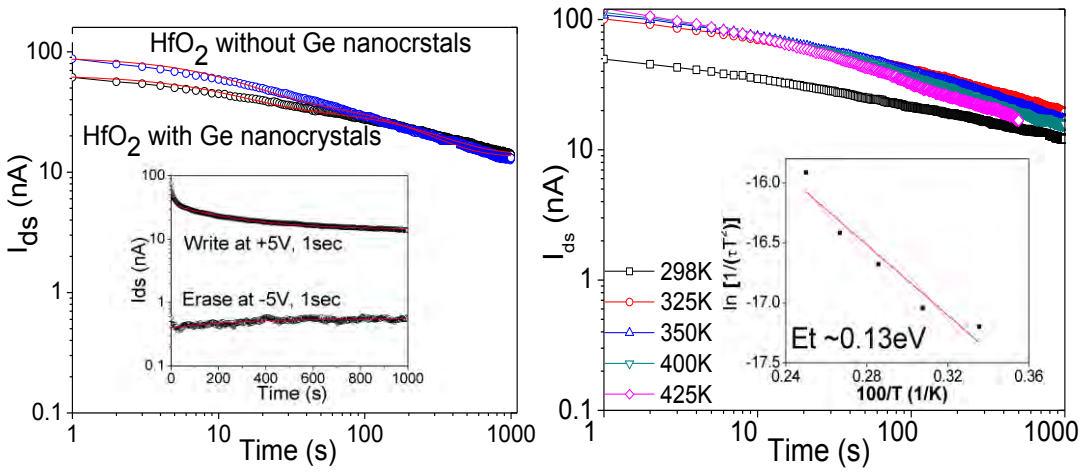
write operation under an applied voltage of +5 V for 1 s. The drain current transient curves of both devices can be fitted with the following double exponential decay equation suggested by Baik *et. al.* , accounting for multiple discharging events

$$I_d(t) = A_1[1-\exp(-\lambda_1 t)] + A_2[1-\exp(-\lambda_2 t)] \quad (7.1)$$

where A_1 and A_2 correspond to different trapping sites in the system, λ_1 and λ_2 represent the time constants that determine the charge decay rate. This decay behavior signifies that different discharging mechanisms are involved, leading to different discharging time constants. A similar λ_1 was extracted from both devices, likely related to minimal difference in interface properties of the devices which contribute to the discharging mechanism involving interface states. On the other hand, λ_2 value increase from 197s to 254s for the device with Ge nanocrystals, suggesting the contribution of nanocrystal traps to a suppressed charge decay rate. Variation in the nature of traps with different level states provides different tunneling components for the charge storage loss. To ensure good retention performance, deep trap energy is favorable, so that the stored charges do not de-trap easily due to thermal energy or electric field effects. A reduced charge loss rate for the sample with nanocrystals evidently illustrates the role of the hybrid charge trapping layer with additional deep trap sites provided by the Ge nanocrystals or nanocrystal / dielectric interface, which reduces the tunneling probability from the charge traps back to the CNT channel. On the other hand, trapped charges in randomly distributed HfO_2 defect states have a higher back-tunneling probability due to the shallow trap levels of vacancy-related defect states situated above the CNT band gap. The inset in Fig. 7.4.1 (a) shows the transient drain current of the device with nanocrystals after both write and erase operations. A more stable memory state was observed after the erase application at -5 V, indicating a smaller hole-tunneling component from the trap states, as compared to

electron de-trapping to the channel. Since different trap levels and discharging mechanisms may exist in the memory device, the trap energy was evaluated by performing high temperature measurements on the Ge nanocrystal sample after write operation.

Fig. 7.4.1 (b) shows the transient drain current measurement at high temperature. Different discharging time constants, τ, arbitrarily defined as the time corresponding to 75% of the charge storage loss were extracted and plotted as a function of temperature in figure inset. These measurements indicate a thermally-activated mechanism involved in the electron discharging process. By assuming a deep trap level discharging mechanism, as suggested by Baik *et al.*, a trap energy of E_t ~0.13 eV was extracted from the gradient of the linear fit of ln [1/ τT^2] vs. 1/T. The observed temperature-dependent behavior provides evidence that the discharging process is dominated by thermal activation (exponential dependence) coupled with direct tunneling (proportional to T^2) to the channel conduction band. This result is in line with our conjecture on the important role of traps in the charge storage of Ge nanocrystal memory devices.



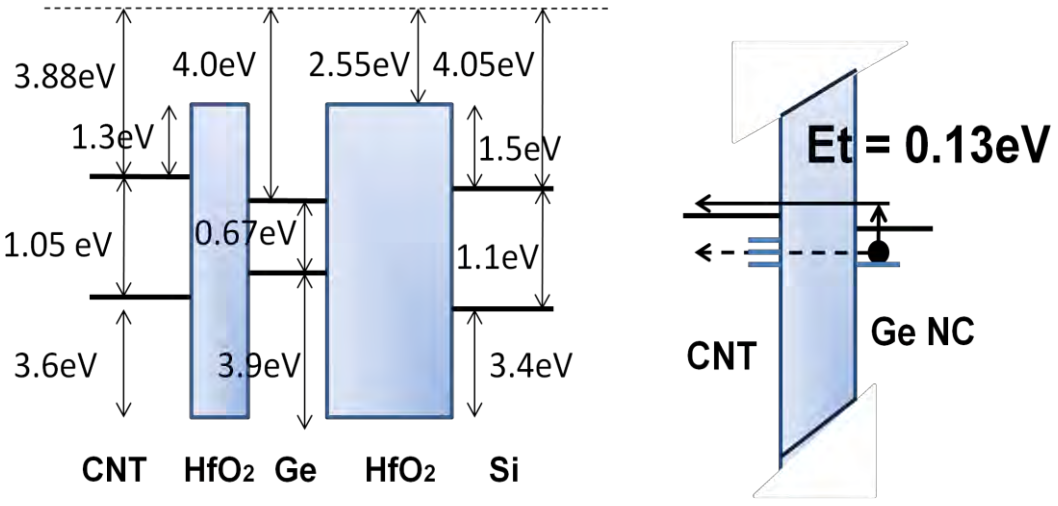
(a) (b)

Fig. 7.4.1 (a) Room temperature transient drain current characteristics of the device with and without Ge nanocrystals after performing a write operation at +5 V for 1 s. The inset shows the retention behavior of the device with Ge nanocrystals after performing both write and erase operations at +/-5 V for 1 s. (b) High temperature retention behavior of the device with Ge nanocrystals, with the inset showing the activation energy extracted from the plot of ln $[1/\tau T^2]$ vs. 1/T.

The energy band diagram of the CNT memory device structure with an additional potential well created by Ge nanocrystal is illustrated in Fig. 7.4.2 (a). By considering the conduction band level between the Ge nanocrystal and CNT channel, charges can be stored in the Ge potential well or in Ge / HfO_2 interface states, which lie below the conduction band edge of the CNT. A large band gap of ~1.05 eV was estimated for the CNTs with an average diameter of 0.8nm. The favorable band offset between the nanocrystal traps and CNT channel offers a large confinement barrier for improved charge retention, as compared to the fast de-trapping of charges from shallow HfO_2 defect states located ~0.7 to 1.2 eV below the HfO_2 conduction band.

The temperature-dependent discharging mechanism observed could be explained by thermal de-trapping of the electrons from the nanocrsytal-related traps to the nanocrystal conduction band, followed by direct tunneling into the conduction band of the channel, as suggested by Shi *et al.* . This process is shown in Fig. 7.4.2 (b). Another viable process during retention is direct tunneling from the traps into defect states at the dielectric / CNT interface, which accounts for the observation of multiple discharging events. The trap energy of E_t ~0.13 eV deduced from the retention behavior agrees with the trap energy level of Ge nanocrystals in SiO_2, assuming that those traps are related to the acceptor level of self-interstitial defects in Ge . Hence, further optimization focused on reducing the interface states between the HfO_2 and

the CNT channel by trap passivation as well as trap energy level engineering is expected to improve the charge retention behavior.



(a) (b)

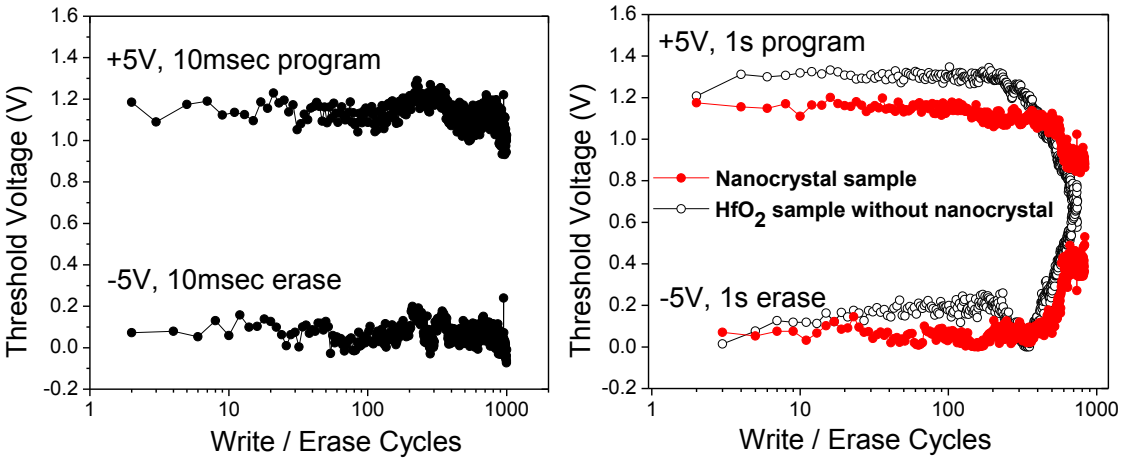
Fig. 7.4.2 (a) Schematic energy band diagram of the CNT memory device structure. (b) Energy band diagram under retention mode showing possible electron discharging paths from the trap states in the Ge nanocrystals.

7.5 Cycling Endurance Characteristics

The data endurance characteristics of the memory device with Ge nanocrystals was evaluated from the endurance cycling measurements after applying positive and negative 5V, 10msec gate pulses during programming and erasing (P/E) cycles, as shown in Fig. 7.4.5 (a). No degradation of the P/E threshold voltage window was observed up to 1000 cycles, indicating reproducibility of the threshold voltages with minimal gate disturb upon cycling. The reliability of the devices with and without Ge nanocrystals was further evaluated after applying positive and negative 5 V, 1 s gate pulses during P/E cycles, as shown in Fig. 7.4.5 (b). The P/E cycling measurements in this case are indicative of an accelerated stress cycle test with larger pulse duration for reduced test time and to ensure accurate read-out response in the bottom-gate operation. The onset of degradation in the threshold voltage window of the Ge

nanocrystal memory device was observed after 500 P/E cycles. This degradation is due to a reduced stability of the device after several stress cycles. Further study on the control device without Ge nanocrystals implies the loss of charge trapping efficiency upon stress cycling. Threshold voltage instability was evident after 200 P/E cycles followed by a rapid degradation of the P/E window, which converges after 700 cycles, indicating continuous charge leakage from HfO_2 traps. This leakage eventually leads to complete charge storage loss associated with the degraded memory functionality.

This result shows that the nature of the trapped charge in the defect states and interface trap density in the HfO_2 play a major role in the narrowing of the P/E window. The passage of tunneling current during P/E operation gradually increases the interface trap density, resulting in a larger loss of charge trapping efficiency due to increased leakage paths for tunneling of trapped charge back to the channel. In addition, charge build-up in the bulk of the dielectric due to accumulation of trapped charges also leads to degradation of the dielectric reliability. A better endurance characteristic observed from the nanocrystal sample confirms the significant role of discrete charge storage in isolated and confined nanocrystals, whereby the charges are more immune to stress-induced leakage current (SILC) due to localized oxide defects. The distributed charge storage in nanocrystal trap sites is less sensitive to the leakage paths as compared to trapped charge in random defect states which easily form percolation paths. Thus, the nanocrystal / high-k storage system provides a more precise control of the threshold voltage stability. An improved endurance behavior is expected from the nanocrystal memory device in a top-gated configuration with reduced parasitic capacitance, when short pulse duration is applied to evaluate the P/E cycling behavior.



(a) (b)

Fig. 7.5.1 Data endurance characteristics of (a) device with Ge nanocrystals cycled under P/E pulses of (+5V, 10msec) and (-5V, 10msec) applied to the bottom gate and (b) device with and without Ge nanocrystals cycled under P/E pulses of (+5V, 1sec) and (-5V, 1sec).

7.6 Summary

In summary, a CNT-based alternative memory device architecture is demonstrated with significantly enhanced memory window and large current rectification achieved under low operation voltage. This work demonstrates a new route for tailoring the charge trapping and transport behavior of CNTFET memory using charge interaction with the underlying Ge nanocrystals in HfO_2 high-k dielectric. An enlarged memory window was achieved by exploiting hybrid charge storage in Ge nanocrysatsl / high-k dielectric matrix and large charge sensitivity of CNT channel, which addresses the V_{th} window limitation of typical nanocrystal memory device. An effective increase in the read-out conductance ratio with the presence of nanocrystals points to a significant charge interaction between the nanocrystals and CNT as well as the CNT-electrode interface. A comprehensive understanding of the trap properties of devices with different trap nature demonstrates the essential role of localized charge storage in the

nanocrystals for controllable memory behavior. The retention improvement with the incorporation of Ge nanocrystals provides insights to tailor the trap energy level and band offsets for controlled memory stability. In addition, dominant charge storage in discrete nanocrystals leads to better endurance characteristics due to decreased sensitivity to localized oxide defects. This tailored conductance and memory behavior indicates promising potential for the hybrid nanocrystal / high-k dielectric structure in CNT-based memory device applications. Further optimization of device performance, for example, by properly defining CNT assembly and interface trap passivation, may lead to next generation nanoscale charge-based storage system for high density, low voltage and low power memory applications.

CHAPTER 8 CONCLUSION

8.1 Summary

This dissertion study is focused on the formation of nanocrystals and the exploration of high-k dielectric materials for memory device application. In order to satisfy higher requirements for future memory devices, different concepts were examined, including the search for appropriate gate dielectric material, process fabrication methodology and novel device structures.

Despite the vast array of literature on nanocrystals, the control of matter at nanometer dimension and the fundamentals on nanocrystal formation mechanism are yet to be understood fully. In Chapter 3, a low temperature technique for the formation of Ge nanocrystals was demonstrated using pulsed laser ablation technique. The nanocrystal density of 7 x $10^{11}$$cm^{-2}$ and larger crystallites with a mean size of 6nm is close to the optimal size and density requirements of ~5nm and $10^{12}$$cm^{-2}$ which significantly impacts the device characteristics. Our studies on the nanocrystal formation mechanism suggest an approach for independent control of nanocrystal size and density based on a thermodynamically driven process. Varying the Ge content during deposition affords direct control of the nanocrystal density for enhanced charge storage. This opens up possibility for realizing defined nanocrystal properties for device application which becomes increasingly important with diminishing number of stored electrons. The salient properties of nanocrystals were revealed using STM as a tool for nanoscale electrical characterization. The contribution of nanocrystal and geometric effects were demonstrated as the key parameters affecting the charge transport behaviour. Charge confinement effects observed in small nanocrystals reveal size-dependent transport behaviour, which lead to correlation between electronic and

microstructural properties. This provides implications that careful control of the nanocrystal diameter and internanocrystal separation can be potentially exploited for a bit per particle storage in future high density memory device.

In Chapter 4 and 5, the introduction of lanthanide-based Lu_2O_3 high-k dielectric in the Ge nanocrystal memory device was demonstrated, which provides a pathway for operating voltage scaling. Significant memory window of ~1.3V with sufficient retention was realized under a low operation voltage of 4V. The charge storage mechanism was ascribed to dominant role of traps at the internal nanocrystal or nanocrystal / dielectric interface, with and estimation of ~10 charges stored per nanocrystal. This is different from the few electrons charging signature observed from nanoscale STM characterization, which shows that the contribution of nanocrystal / dielectric interfaces could dominate the global behaviour of the memory device under large area characterization. The study on the effect of high-k dielectric indicates the control of various interfaces that are inherent for high-k dielectric as a key direction for material selection and memory performance optimization. The chemically stable amorphous Lu_2O_3 dielectric matrix plays an important role for the formation of stable charge trapping sites. In addition, a more versatile approach for enhancing the memory performance was demonstrated using a self-aligned graded lanthanide-based high-k barrier enabled by thermally-induced intermixing of the oxide components. Instead of using a multi-layer dielectric stack which requires good control of the interface quality, the self aligned graded barrier scheme provides process simplicity, with the memory window significantly enlarged from 1.3V to 2.7V. Simultaneous improvement in charge storage and retention was achieved, which addresses the trade-off between program/erase efficiency and data retention.

In order to control the charge storage properties of the nanocrystals, developing strategies to organize ordered assemblies of nanocrystals is the key for improving device performance. In order to move beyond the limitation of physical fabrication routes in tailoring the nanocrystal properties, the convergence of physical and chemical techniques was explored to aid in the development of controlled size and ordered arrangement of nanocrystals. In Chapter 6, a low temperature solution-based chemical method was demonstrated for the synthesis of nanometre-sized Ge nanocrystals without the need for stringent atmospheric conditions. Tenable control of the nanocrystal size was achieved with the encapsulation of the organic surfactant on the inorganic nanocrystal surface. Varying the precursor solution concentration affords further control of nanocrystal size and distribution. Strategies for organizing ordered self-assembly of the nanocrystals on oxide surface were further explored by exploiting self-assembled monolayers for chemical functionalization of the oxide surface. Successful amino-silanization of both SiO_2 and HfO_2 high-k dielectric surface were demonstrated, which provides a versatile approach for subsequent chemical grafting and assembly of the colloidal nanocrystals on the substrate surface. By employing the APTES/HfO_2 hybrid dielectric, a significantly enlarged memory window of ~2.2V was obtained as compared to the ΔV_{fb} of ~1.1V obtained from the device without functionalization. Combined with a physical elaboration process of high-k dielectric barrier, chemistry allows the control over device parameters by tailoring the nanocrystal assembly for the realization of solid-state device.

Finally, the opportunity for a three-dimensional hybrid nanostructure device was presented using CNTs as the channel element in the memory device architecture in Chapter 7. A significantly enlarged memory window of ~5.3V was achieved, which represents a promising approach to address the V_{th} window limitation of typical

nanocrystal memory device, associated with hybrid charge storage in Ge nanocrysatsl / high-k dielectric matrix and large charge sensitivity of CNT channel. Comparison on devices with different trap nature delineates the effect of different trap properties and signifies the importance of localized charge storage in the nanocrystals for controllable memory behavior with improved retention and endurance characteristics. Temperature-dependent charge transport studies highlight the electronic doping effect of nanocrystals for effective tuning of Schottky barrier height in CNTFET devices. The strong charge interaction between the nanocrystals and the CNTs presents significant impact for achieving enhanced charge storage and improved I_{on}/I_{off} ratio of CNT based memory device.

8.2 Future Prospects and Recommendations

In the long term, future memory devices require post-silicon innovations with new nano-devices based on different principles of physics, new materials and processes that offer the potential for ultimate density and performance.

8.2.1 Formation and Evolution of Nanocrystals by Pulsed Laser Deposition

The fundamental understanding and control of matter at nanoscale dimensions is imperative for controlled device performance with minimal threshold voltage variation resulting from the spread in nanocrystal size and density. Further work on the theoretical modelling the nanocrystal formation process is necessary to establish a fabrication route for the manipulation and formation of well-organized nanocrystals. Studies on the influence of substrate temperature also constitute another aspect in controlling the nanocrystal properties, which determines the free energy of free-atom clusters and diffusion coefficient during the growth process.

8.2.2 Study and Optimization on Ge Nanocrystal Memory Capacitor Device

Further characterization of spatial charge distribution using charge-pumping technique and trap energy level using deep level transient spectroscopy (DLTS) would be useful in-depth studies of the charge trapping mechanism. Localized charge transport study on nanocrystals fabricated with defined size and distribution would provide further insight on the charge trapping properties and size-dependent effects. The concept of barrier modification approach deserves further studies in order to improve the electron retention in addition to the hole retention behaviour. The engineering of trap energy by with the formation of surface-passivated / core-shell nanocrystals interface control constitutes another interesting direction to tune the charge trapping properties.

8.2.3 Self-Assembly and Chemical Synthesis of Colloidal Ge Nanocrystals

Size and ordered arrangement of the colloidal Ge nanocrystals with minimal aggregate formation are yet to be realized. The exploration of a more suitable capping ligand for improved stabilization and subsequent chemical bonding with the modified substrate may provide enhanced attachment of nanocrystals on the functionalized substrate. Thereafter, a layer-by-layer assembly technique can be pursued for ordering and multilayer self-assembly driven by electrostatic force. Once the mechanisms controlling the self-ordering phenomena are fully understood, the self-assembly technique can be exploited for the deposition of nanocrystals on a wide range of dielectric surfaces. Efforts on optimization of the memory device performance include the minimization of charge trapping effects of the APTES SAM layer, which is possible by optimization of the functionalization process and/or further treatment with a high vacuum low temperature anneal process.

8.2.4 CNT-based Ge Nanocrystal Memory

An improved device performance with minimized dielectric trap charging contribution from the CNT-based memory device is expected by utilizing a top-gated structure with uniform coverage of high-k dielectric and nanocrystal layer on the CNT channel. The device structure could also be extended to an asymmetric double-gate device architecture with enhanced gate electrostatic control, improved I_{on}/I_{off} ratio and V_{th} window. The successful realization of the device structure requires proper definition of CNT and nanocrystal assembly, which opens up possibility for multi-bit-per-cell memory operation. The hybrid nanostructure / high-k dielectric device architecture may ultimately lead to next generation nanoscale charge-based storage system for high density, low voltage and low power memory applications.

8.2.5 Outlook

The field of nanoscience promises exciting opportunities for building the future. In the mean time, many scientific challenges need to be addressed, including exquisite control over feature size and organization as well as the effect of interfaces. With the limitations being circumvented, the concept of combining bottom-up and top-down techniques using new materials and devices is expected to find use beyond the applications traditionally targeted by miniaturization efforts.

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APPENDIX

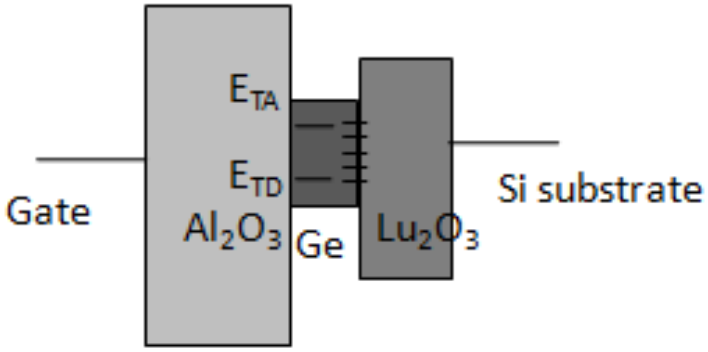


Fig. A5.1 Schematic band diagram of the Ge nanocrystal memory structure with Lu_2O_3 as the tunneling dielectric and Al_2O_3 as the control dielectric, illustrating nanocrystal trap states existing as electron acceptor, E_{TA} and electron donor, E_{TD} as well as defect traps at the nanocrystal/Lu_2O_3 interface.

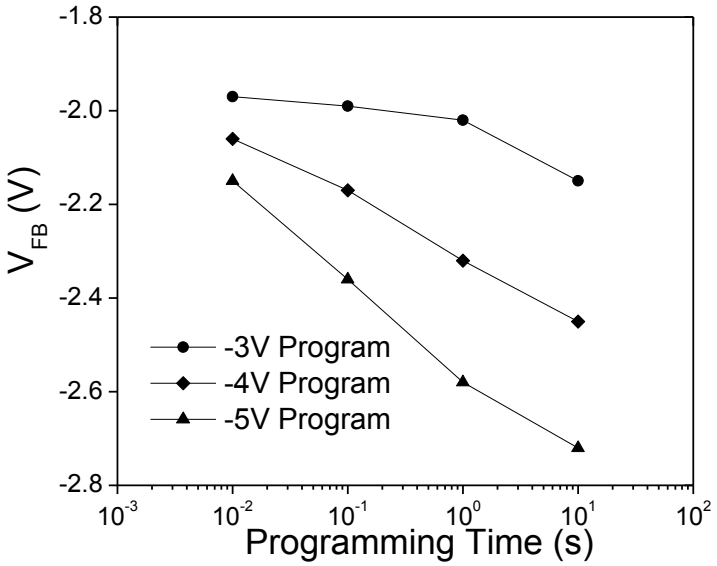


Fig. A5.2 Programming transient behavior of the 800 ^{o}C annealed sample with increasing negative bias application and pulse duration from 10 ms to 10 s.

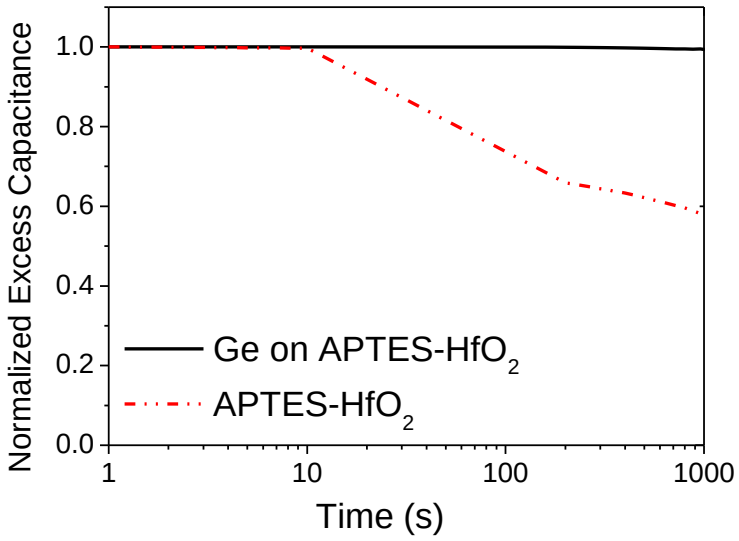


Fig. A6.1 Normalized charge decay characteristics of the MOS capacitor devices (a) with and (b) without Ge nanocrystals deposited on the HfO_2 dielectric functionalized with APTES SAM layer after charging at -5 V for 1s.

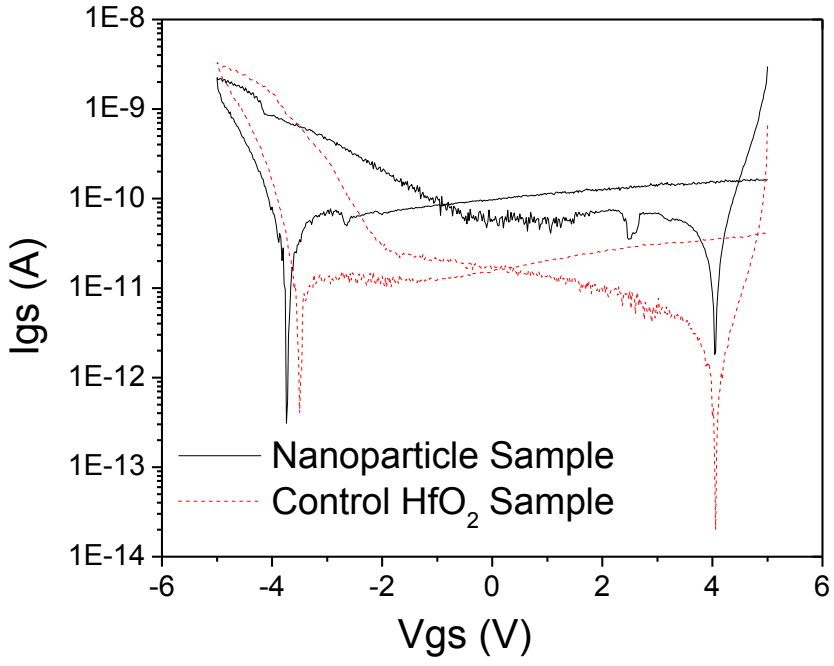
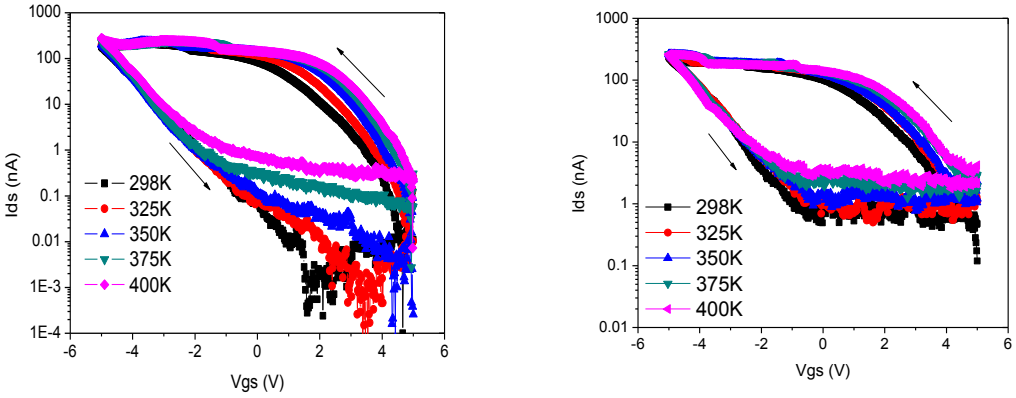


Fig. A7.1. Gate current (I_{gs}) vs. gate voltage (V_{gs}) curves for the CNT device with and without Ge nanocrystals in the HfO_2 bottom high-k gate dielectric, under a gate voltage sweep of +/-5 V and drain voltage of V_{ds} = 1 V.



(a) (b)

Fig. A7.2. High temperature I_{ds}-V_{gs} sweeps measured under temperatures from 298 K to 400 K for a) the device with incorporated Ge nanocrystals and b) the control sample without Ge nanocrystals.