

# Novel RF Front-End Design for Low Power UWB Applications

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# TABLE OF CONTENTS

ACKNOWLEDGMENTS . . . . .	i
TABLE OF CONTENTS . . . . .	iii
LIST OF FIGURES . . . . .	vi
LIST OF TABLES . . . . .	x
LIST OF SYMBOLS . . . . .	xi
ABSTRACT . . . . .	xii
<b>1 Introduction</b>	<b>1</b>
1.1 Motivation . . . . .	1
1.2 Objectives . . . . .	2
1.3 Major Contribution of the Thesis . . . . .	3
1.4 Organization of the Thesis . . . . .	4
<b>2 Introduction to Ultra-Wideband (UWB) Systems</b>	<b>6</b>
2.1 UWB Transceiver Architectures . . . . .	9
2.1.1 Impulse Radio UWB . . . . .	10
2.1.2 Multiband OFDM UWB–Receiver Architectures . . . . .	12
2.1.2.1 Direct-Conversion Receiver . . . . .	12
2.1.2.2 Heterodyne Architecture . . . . .	14
2.2 UWB Applications . . . . .	15
2.3 UWB Transceiver Design Challenges . . . . .	16
<b>3 Introduction to UWB Low-Noise Amplifier</b>	<b>18</b>
3.1 Broadband Amplifiers . . . . .	18
3.1.1 Tuned Amplifiers . . . . .	21

3.1.2	Shunt and Series Peaking . . . . .	23
3.1.3	Wideband Input Matching and Reactive Series Feedback . . . . .	25
3.1.4	Shunt-Shunt Feedback . . . . .	28
<b>4</b>	<b>Proposed Wideband Low-Noise Amplifier</b>	<b>34</b>
4.1	Circuit Design: Theory and Practice . . . . .	34
4.2	Wideband Amplifier Design . . . . .	41
4.2.1	Output Peaking Network . . . . .	41
4.2.2	Input Matching Network . . . . .	46
4.2.3	Noise Analysis . . . . .	48
4.2.4	Design Sensitivity to Process Variations . . . . .	51
4.3	Experimental Results . . . . .	53
<b>5</b>	<b>Introduction to Mixer Architecture</b>	<b>63</b>
5.1	Active Mixer . . . . .	63
5.2	Passive Mixer . . . . .	65
5.3	Non-Idealities of the Mixer . . . . .	68
5.3.1	Intermodulation Distortion . . . . .	68
5.3.2	Second-Order Intermodulation Distortion . . . . .	71
5.4	Noise in the Mixer . . . . .	77
<b>6</b>	<b>Proposed Integrated Wideband Receiver Front-End</b>	<b>80</b>
6.1	Theoretical Calculations of the Receiver Requirements . . . . .	81
6.1.1	Noise Figure Requirements . . . . .	81
6.1.2	Linearity Requirements . . . . .	81
6.2	UWB Front-End Architecture . . . . .	83
6.2.1	Single-to-Differential LNA with On-Chip Transformer . . . . .	84
6.2.2	Down-Conversion Mixer Architecture . . . . .	87
6.2.2.1	I/Q Mismatch . . . . .	97
6.3	Instrumentation Amplifier as Output Buffer . . . . .	100
6.4	Measurement Results . . . . .	101
6.5	Measurement Setups . . . . .	108
6.6	Summary . . . . .	111

<b>7 Conclusions and Recommendations</b>	<b>113</b>
7.1 Conclusions . . . . .	113
7.2 Recommendations . . . . .	115
<b>Author's Publications</b>	<b>116</b>
<b>Bibliography</b>	<b>117</b>

# List of Figures

2.1	Frequency allocation of MB-OFDM UWB channels. . . . .	7
2.2	UWB impulse radio. . . . .	10
2.3	An IR-UWB transceiver architecture for (a) transmitter and (b) receiver [1]. . . . .	11
2.4	All digital transmitter [1]. . . . .	12
2.5	Direct-conversion receiver architecture. . . . .	12
2.6	An example of MB-OFDM UWB receiver front-end. . . . .	14
2.7	Heterodyne receiver architecture. . . . .	14
3.1	Wideband two-stage amplifiers, (a) a source follower driving a common-source amplifier, (b) a source follower driving a common-gate amplifier, (c) a common-source amplifier drives a common-gate amplifier. . . . .	19
3.2	A resistive load cascode amplifier, biasing not shown. . . . .	20
3.3	(a) A single stage $LC$ tuned amplifier, (b) a cascode $LC$ tuned amplifier. Biasing not shown. . . . .	21
3.4	(a) A common-source amplifier with a shunt-peaking load, (b) equivalent circuit for the shunt-peaking amplifier. . . . .	23
3.5	Series peaking in a common-gate low noise amplifier with stagger compensation [2]. . . . .	24
3.6	Second-order low-pass ladder filter. . . . .	25
3.7	Fourth-order bandpass ladder filter. . . . .	26
3.8	(a) Matching network is used to achieve real value, (b) a simple solution is to simply terminate the matching network with a physical resistor, (c) a more elegant solution uses a feedback synthesized resistor input match. . . . .	27

3.9	(a) The complete input-matching requires a gate inductor $L_g$ to resonate with the capacitor $C_{gs}$ . (b) the equivalent circuit for the input match is a series $RLC$ circuit. . . . .	28
3.10	(a) Simplified schematic, and, (b) small-signal model of a shunt-shunt feedback amplifier. . . . .	29
3.11	$LC$ shunt-shunt feedback technique. . . . .	30
3.12	Transformer-feedback technique [3]. . . . .	31
3.13	An ultra-wideband amplifier using Chebyshev active filter [4]. . . . .	32
4.1	Common-source amplifier with output parasitic capacitance $C_p$ . . . . .	35
4.2	(a) Series inductive peaking circuit, (b) frequency response of the circuit (a) with and without $L$ , (c) complex poles location for maximum gain-flatness response, (d) shunt-series inductive peaking circuit, (e) frequency response of the shunt-series peaking circuit, (f) series-shunt-series peaking including a T-coil peaking network, (g) series-shunt-series peaking frequency response. . . . .	36
4.3	Transfer function of the equation (Eq. 4.6), plotted in MATLAB. . . . .	40
4.4	Transfer function of the peaking network (Figure 4.2(f)) using Cadence simulator. . . . .	40
4.5	(a) Common-source amplifier with symmetric T-coil peaking network, (b) and (c) simplified small-signal equivalent circuit of the T-coil peaking. . . . .	42
4.6	Group delay response of the T-coil network. . . . .	43
4.7	Amplitude response of the T-coil network vs. $k$ -factor at different frequencies. . . . .	44
4.8	Amplitude response of the T-coil network vs. frequency. . . . .	45
4.9	Wideband LNA using symmetrical center-tap inductor (biasing circuitry not shown). . . . .	46
4.10	Simulated frequency response of the LNA, in here $R = 0$ . The wideband LNA with/without feedback path is simulated for comparison, the 3 dB bandwidth is adjusted later. . . . .	47
4.11	Input impedance equivalent network of the LNA. . . . .	49

4.12	Simplified small-signal model of Fig. 4.5(a), noise contribution of $M_2$ is ignored. . . . .	49
4.13	Variations of normalized $R_n$ with three different currents vs. frequency. . . . .	51
4.14	Device variations effect on the noise figure performance. . . . .	54
4.15	Simulation stability of the wideband LNA, $\Delta$ . . . . .	55
4.16	Simulation stability of the wideband LNA, $K_f$ . . . . .	56
4.17	Contour plots of $\alpha$ variation (variation of the next stage parasitic capacitance) and its effect on the gain peaking vs. frequency. . . . .	57
4.18	Die micrograph of the wideband LNA. . . . .	58
4.19	Gain and input reflection coefficient of the LNA vs. frequency. . . . .	58
4.20	Measured and simulated S22 and S12 of the LNA vs. frequency. . . . .	59
4.21	Simulated IIP3 at 8 GHz. . . . .	60
4.22	Simulated and measured noise figure of the wideband LNA. . . . .	61
4.23	Measured quality factor of the inductors. . . . .	61
5.1	Current commuting active mixer. . . . .	64
5.2	Passive mixer structures. . . . .	65
5.3	Double balanced voltage-mode passive mixer [5]. . . . .	66
5.4	Double balanced current-mode passive mixer. . . . .	66
5.5	IIP3 versus $V_{gs}$ for a single transistor. . . . .	69
5.6	Distortion model for the unbalanced switching mixer in Fig. 5.2(a) [6]. . . . .	70
5.7	Nonlinearity in the RF. . . . .	72
5.8	RF and low-frequency intermodulation. . . . .	72
5.9	LO oscillator self-mixing. LO leakage to the RF port. . . . .	73
5.10	Self-mixing model in single balanced mixer [7]. . . . .	74
5.11	Time domain waveforms in a soft-switching single balanced mixer; applied sinusoid $LO(V_{LO})$ , output current $I_{out} = I_1 - I_2$ , and self-mixing function $sw(t)$ [7]. . . . .	75
5.12	Noise reduction technique in an active mixer [8]. . . . .	78
6.1	Simplified block diagram of the UWB front-end receiver . . . . .	84

6.2	Simplified schematic of the UWB single-to-differential LNA (biasing is not shown). . . . .	84
6.3	(a) Transformer model. (b) equivalent circuit model for coupled inductors. (c) equivalent circuit of (b) with load network transferred to the input. . . . .	86
6.4	S21 measurement of the transformer over a wide frequency range. . . . .	88
6.5	(a) Simplified schematic of the double-balanced down-conversion mixer, (b) & (c) Non-ideal LO switching and slope improvement . . . . .	89
6.6	Flicker noise comparison between different types of the mixers. . . . .	93
6.7	A single-balanced double-conversion mixer with offset voltage at gate. . . . .	96
6.8	I/Q receiver model with I/Q imbalance. . . . .	97
6.9	Instrumentation amplifier used for measurement setup. . . . .	100
6.10	Chip microphotograph of the wideband receiver. . . . .	102
6.11	Measured input reflection coefficient of the receiver. . . . .	103
6.12	Measured/Simulated conversion gain of the receiver at 8 GHz. . . . .	104
6.13	An example of measured IIP3 which shows the third-order interferer. . . . .	105
6.14	Measured IIP3 at 3.05 GHz frequency. . . . .	106
6.15	Measured IIP2 at 7.12 GHz frequency. . . . .	106
6.16	Measured isolation of the LO-RF and LO-IF ports. . . . .	107
6.17	Gain measurement setup. . . . .	109
6.18	Y-factor method in noise figure measurement setup. . . . .	111

# List of Tables

4.1	Component Values of the LNA . . . . .	54
4.2	Wideband LNA Performance Summary and Comparison . . . . .	62
6.1	Transformer Characteristics . . . . .	87
6.2	Performance Summary of the Receiver Front-end . . . . .	104
6.3	Performance Comparison Table . . . . .	108

# List of Symbols

$\tau$	time constant
$\omega$	resonance frequency
$k$	magnetic coupling coefficient
$\varphi$	phase degree
$\delta$	excess noise parameter
$\gamma$	excess noise parameter
$g_{d0}$	channel conductance
$r_g$	extra physical input resistance
$\varepsilon$	amplitude mismatch
$\theta$	phase mismatch
$F$	noise figure
$T$	temperature in Kelvin

# Abstract

The needs for short range and fine resolution communications systems has motivated researchers to replace the wire-line communications systems with ultra-wideband communications systems. The ultra-wideband radio technology introduces significant advantages for short-range communications systems. This technology operates in a wide bandwidth, which allows for gigabit data rates over short distances. Due to the low complexity of the ultra-wideband system and low transmit power, it benefits from low DC power consumption. However, with growing demands for wireless communications systems, the ultra-wideband communications systems are facing more challenging requirements. Since the ultra-wideband covers a wide range of frequency, it causes challenges in the design of building blocks, in particular receiver front-end. The scope of this dissertation is to design a novel and innovative RF front-end receiver for the ultra-wideband transceivers using CMOS technology.

A T-coil network can be implemented as a high order filter for bandwidth extension. This technique is incorporated into the design of the input matching and output peaking networks of a low-noise amplifier. The intrinsic parasitic capacitances within the transistors are exploited as a part of the wideband structure to extend the bandwidth. Using the proposed topology, a wideband low-noise amplifier with a bandwidth of 3–8 GHz, a maximum gain of 16.4 dB and noise figure of 2.9 dB (min) is achieved. The total power consumption of the wideband low-noise amplifier from the 1.8 V power supply is 3.9 mW. The prototype is fabricated in 0.18  $\mu\text{m}$  CMOS technology.

Furthermore, a two-stage down-conversion architecture for 3–8 GHz ultra-wideband receiver front-end is designed, which uses a local oscillator frequency equal to half of the input frequency. A single stage low power single-to-differential low-noise amplifier is designed to eliminate the need for an off-chip balun and increases the integration

level of the front-end receiver. Consecutively, the RF frequency is down-converted in two steps based on half-RF architecture to produce baseband signal. The proposed architecture introduces many advantages such as high linearity and good port-to-port isolation. The proposed technique is implemented in 0.18  $\mu\text{m}$  CMOS technology, which achieves a conversion gain of 36.1–32.4 dB and noise figure of 5.4–8.3 dB across the bandwidth.

# Chapter 1

## Introduction

### 1.1 Motivation

Ultra-wideband systems are a wireless technology, that are capable of transmitting data over a wide spectrum of frequency bands for short distances with very low power and high data rates. Back at 1960s, the ultra-wideband (UWB) came to be known for the operation of sending and receiving extremely short bursts of RF energy. It has outstanding ability for applications that requires precision distance or positioning measurement as well as high-speed wireless connectivity. The UWB technology delivers data rates in excess of 100 Mbps up to 1 Gbps. The UWB not only has the potential of carrying high data rate over a short distance, but also it can penetrate through doors and other obstacles. The key advantages of the UWB systems over narrowband systems are: high data rate due to the large bandwidth, low equipment cost, low power and immunity to multipath.

A significant difference between traditional radio transmission and the UWB radio transmission is that, traditional communications systems transmit data by varying the power level, frequency, and/or phase of a sinusoid wave. However, in the UWB radio, data is transmitted either as impulse radio (IR) or multiband orthogonal frequency division multiplex (OFDM). The IR UWB transmits data based on the transmission of very short pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. This technique results in lower-data rate and -design complexity

compared to the OFDM system. On the other hand, in the multiband OFDM technique each band with 528 MHz width encodes the data using quadrature phase shift keying (QPSK) modulation. Using this technique a data rate up to 480 Mb/s can be achieved. However, the design of this system is more challenging.

It is important that the operation of the UWB system should not cause harmful interferences, and at the same time this system must tolerate any undesirable interference signal. Regarding to the Federal Communications Commissions (FCC), the UWB signals occupy more than 500 MHz of the bandwidth in the 3.1 GHz–10.6 GHz band. The power spectral density (PSD) of the UWB transmitter measured in 1 MHz is limited to -41.3 dBm/MHz, to avoid interference with existing standard [9].

Due to the wideband requirements of the UWB RF front-end, it is very challenging to design the wideband RF front-end receiver. In most applications, it is desirable to obtain wideband on-chip input matching to a  $50 \Omega$  antenna/filter with good linearity, and low power consumption. In addition, gain flatness over the entire frequency range of interest is necessary to meet the design specifications. These properties are the cornerstones of the wideband receiver front-end, which can affect the total broadband communications systems characteristics. The scope of this dissertation is to design an innovative wideband RF front-end for the UWB receiver in the CMOS technology.

## 1.2 Objectives

The objectives of this thesis are summarized as follows:

- To design a low power low-noise amplifier in the CMOS technology.
- To introduce a simple but accurate lumped elements model for input/output matching of the low-noise amplifier.
- To propose a single-to-differential conversion technique to overcome the need for differential input signal and eliminate the bulky and lossy off-chip balun.

- To develop a low power quadrature mixer with high linearity and low-noise figure.
- To integrate the RF front-end in order to realize the UWB receiver front-end.

### 1.3 Major Contribution of the Thesis

A 3–8 GHz ultra-wideband receiver front-end for high data rate, short-range communications systems is designed and implemented. The major contribution in chapter 4, is to design and analyze a single stage wideband low-noise amplifier, which is used to cover a frequency range of 3–8 GHz frequency. In the proposed low-noise amplifier, a symmetric T-coil peaking network is utilized in order to achieve a wideband input matching and wideband output peaking response. In this low-noise amplifier the number of inductors are optimized to 3, in order to reduce the size and cost of the chip. The prototype of the single stage wideband low-noise amplifier is fabricated in a six-metal 0.18  $\mu\text{m}$  CMOS technology.

The proposed single stage low-noise amplifier is further improved with a single-to-differential architecture. The aim is to eliminate the bulky and lossy off-chip balun, in order to increase the circuit integration. Furthermore, in chapter 6 a two-stage down-conversion mixer is proposed, which is driven with a local oscillator frequency that is half of the input radio frequency. Since in this architecture, the local oscillator frequency is far from the input radio frequency, better isolation is obtained between port-to-port of the receiver compared to the direct conversion architecture. This technique results in reduction of non-ideal harmonics and consequently, improves the second- and third-order input intermodulation distortion. Also, this architecture reduces the total DC power requirement, due to the high level of integration. Finally, the single-to-differential low-noise amplifier is integrated with the two-stage down-conversion mixer to realize the ultra-wideband receiver front-end.

## 1.4 Organization of the Thesis

Chapter 2 is an introduction to the background and applications of the ultra-wideband systems. This chapter reviews different topologies applicable to the ultra-wideband systems, and introduces various architectures and challenges of these systems. Furthermore, the basic introduction of the RF receiver front-end will be reviewed.

Chapter 3 will briefly review some analog style amplifier designs, especially topologies that can provide high-frequency performance. In the microwave amplifiers, active elements such as transistors are treated as two-port device, which should be carefully matched to obtain the optimal performance. The classic tuning amplifier will be discussed, which is used to compensate the headroom problem in the cascode amplifiers. Furthermore, other tuning amplifiers associated with resonance filters are explained, to bridge the gap between the analog and RF amplifiers.

Chapter 4 presents the proposed low-noise amplifier circuit for the receiver front-end. Based on the bandwidth enhancement techniques, which are explained in details in this section, a wideband low-noise amplifier is resulted. In brief, shunt peaking is a form of bandwidth enhancement technique in which a one-port network is connected across the amplifier and load. The shunt peaking technique is then further developed into a shunt-shunt network, to achieve a wideband peaking network at the output of the low-noise amplifier. Similarly, the same technique is used for the input matching of the low-noise amplifier, to match the amplifier to the antenna over a wide range of frequency. Finally, the simulation and measurement results are presented to prove the feasibility of the circuit.

Chapter 5 provides an overview of the active and passive mixer circuit design. The advantages and disadvantages of the different mixer architectures are briefly described. The important characteristics of the mixer including conversion gain, noise figure, linearity and distortion are described in this section.

Chapter 6 presents the integrated low-noise amplifier with the two stage down-conversion mixer, to realize a wideband receiver front-end. The discussion on the circuit analysis, advantages and drawbacks of the proposed receiver front-end are included as well. The simulations and measurements results are discussed at the end of the chapter.

Chapter 7 summarizes the major contributions of this thesis and suggests future works to be developed.

# Chapter 2

## Introduction to Ultra-Wideband (UWB) Systems

Ultra-wideband (UWB) radio potentially offers higher communication speeds than traditional narrowband transceivers, which may be necessary in the near future to meet growing consumer demands for higher speed and better quality mobile links. In 1963 this standard was proposed by Ross [10]. Afterward, this technology was further defined by Federal Communications Commission (FCC) as any wireless scheme that transmits an extremely low-power signal at a fractional bandwidth of  $BW/f_c > 20\%$ , or more than 500MHz bandwidth, where  $BW$  is the communication bandwidth and  $f_c$  is the band center frequency. This prototype modulates data with binary phase shift keyed (BPSK) pulses over a wideband direct-conversion front-end, and samples the received signal for modulation. This standard found applications in imaging systems, high-speed wireless communications, and particularly in short-range high-speed data transmissions suitable for broadband networks [11], [12]. In 2002, the FCC allowed the UWB communications in the 3.1–10.6 GHz band having a -10 dB bandwidth greater than 500 MHz, and a maximum equivalent isotropic radiated power spectrum density of -41.3 dBm/MHz, to ensure negligible interference. The 3.1–10.6 GHz band is divided in 14 channels organized in five groups, as shown in Fig. 2.1. The 14 bands span the range of 3168 to 10560 MHz, and each band consists of 128 subchannels of 4.125 MHz each. Bands 1–3

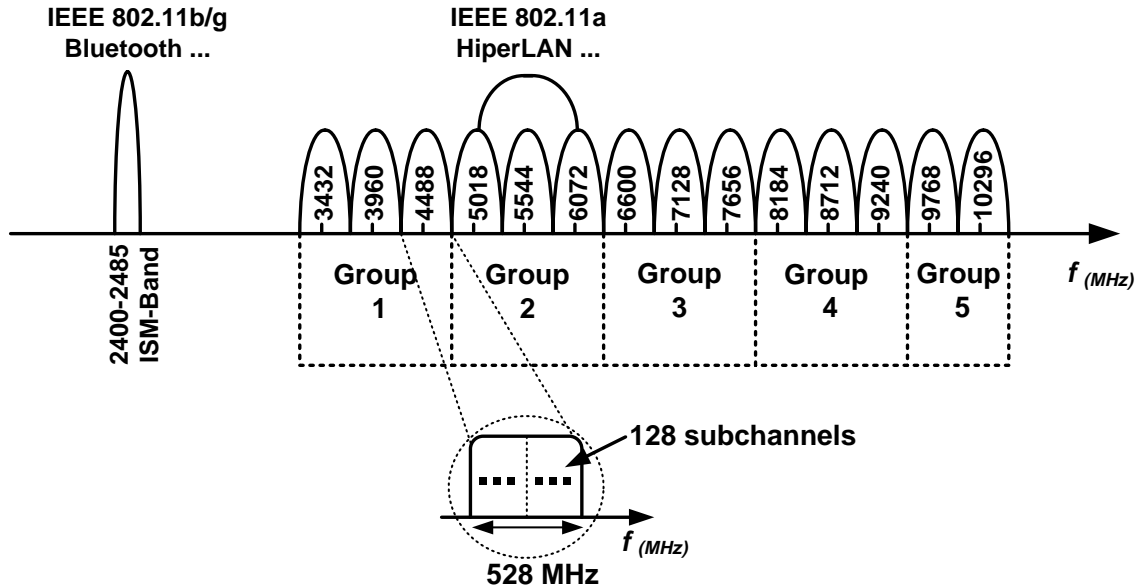


Figure 2.1: Frequency allocation of MB-OFDM UWB channels.

constitute “Group 1” and are mandatory for operation, whereas the remaining bands are envisioned for high-end products [13]. In this band (3.1–10.6 GHz) two proposals on the operation of the UWB devices are being considered. One employs BPSK, providing data rates from 28–1320 Mb/s within the transmission bands from 3.1 GHz to 4.85 GHz and from 6.2 GHz to 9.7 GHz [14]. The other uses the multi-band orthogonal frequency division multiplexing (MB-OFDM) approach, where information is encoded in 528 MHz wide channel using 122 quadrature phase shift key (QPSK) sub-carrier. The multiband OFDM alliance (MBOA) proposal for 802.15.3a uses OFDM modulation in a bandwidth of 528 MHz [14]. In contrast to IEEE 802.11a/g, MBOA employs only QPSK modulation in each sub-channel to allow low resolution in the baseband analog-to-digital (ADC) and digital-to-analog (DAC) converters. The unlicensed band is intended to enable applications such as; ground penetrating radars, imaging/surveillance systems, and wireless home video data links.

The advantage of the UWB systems over narrowband systems is that the UWB transceiver benefits from low complexity, low power, and multipath time resolution due

to the large bandwidth. A significant difference between traditional radio transmissions and UWB radio transmissions is that traditional communications systems transmit data by varying the power level, frequency, and/or phase of a sinusoidal wave. This means that a baseband signal is mixed with higher frequency carrier to a radio frequency within a desired channel for data transmission. For low data rate applications, impulse radio can be used, however for high data rate applications the MB-OFDM is employed. The impulse radio is based on the transmission of very short pulses by encoding the polarity of the pulses. In some cases, impulse transmitters are employed where the pulses do not modulate a carrier. Instead, the radio frequency emissions generated by the pulses are applied to an antenna, and the resonant frequency of the antenna determines the center frequency of the radiated emission. So the modulated signal is directly transmitted through the antenna to the air. This has greatly reduced the complexity of the transceiver architecture and RF front-end circuit design compared to the narrowband receivers. The frequency response characteristics of the antenna provides bandpass filtering, further affecting the shape of the radiated signal [15], [16]. As a result, the UWB systems benefit from simple modulation schemes, multiple access ability, and high data rates.

The main limitation of the UWB communications systems is the presence of strong in-band interference signals that degrade the receiver front-end performances. The overlap between the UWB and other standards is a major concern, which requires a high linear transceiver.

The IEEE 802.15 working group develops personal area network consensus standards for short distance wireless personal area networks (WPANs) [17], [9] and it is predicted that these systems will be capable of transmitting at higher data rate, up to 500 Mb/s with power consumption lesser than 1 mW [18]. The UWB technology is more attractive compared to a WiFi technology, IEEE 802.11b, with 11 Mb/s data rate that consumes a

200 mW power [19]. The UWB technology can improve the broadband networks, which can be used for the electronic home devices like camcorders, video games and high-definition TV (HDTV) connected to the wireless UWB devices. Other applications of the UWB include portable wall-penetrating radar, which is used for military application [20], surveillance systems, and radio frequency identification (RFID).

As part of IEEE P802.15, MB-OFDM with fast frequency hopping is proposed as a means of high-rate wireless communications in the UWB spectrum [21]. For this mode, the spectrum shown in Fig. 2.1 is divided into 528 MHz bands spanning from 3.1–8.2 GHz. The features of such a system must be obtained at moderate power consumption with minimum additional cost of the chip.

Two methods to implement the UWB systems are discussed below. Moreover, the challenges of the UWB systems design compared to the narrowband receivers are highlighted.

## 2.1 UWB Transceiver Architectures

The impulse radio UWB radios can be implemented either as multiband OFDM (MB-OFDM) or direct-sequence impulse radio (DS-IR). The IR system relies on a very short duration of the pulses with several gigahertz bandwidth. The main challenge facing the IR system, is the existence of the neighbor narrowband systems. Since IR receiver/transmitter systems are based on the short pulses, each narrowband signal with the same band from another system can fall on the IR fundamental band and disrupt the signal. A solution to this problem is to use a notch filter, however not only the design of a precise narrowband notch filter is very challenging, due to the difficulty in design of high quality factor inductors, but also the notch filter can degrade the useful signal. Therefore, IR systems need a very high linearity characteristic. The multiband OFDM on the other hand, can avoid this problem by switching from one band to the other band,

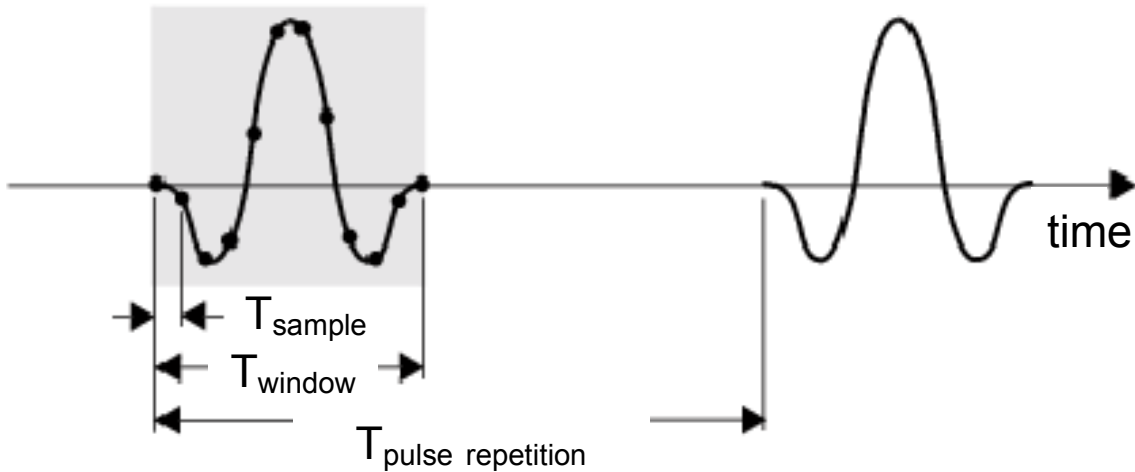


Figure 2.2: UWB impulse radio.

not to be affected by the other adjacent channels, which are used by the other systems. Besides, a MB-OFDM has the ability to provide the data rates up to 480 Mbps and above, over a short distance.

### 2.1.1 Impulse Radio UWB

The IR UWB radios communicate with short pulses or cycles on the order of nanoseconds, spreading their energy over a wide swath of bandwidth, as opposed to modulated sinusoids whose energy is localized around a single frequency. A sample pulse is shown in Fig. 2.2. The IR UWB transmits data based on the transmission of very short pulses with several gigahertz bandwidth. In some cases, impulse transmitters are employed where the pulse do not modulate a carrier. This technique results in lower-data rate and design complexity. However, the main challenge facing the IR system, is the existence of the narrow band systems. An example of the IR UWB transceiver is shown in Fig. 2.3(a), (b) [1], with on-off keying (OOK) modulation scheme for easy implementation and low power consumption. The transmitter is an all digital design, and a CMOS output buffer drives the antenna directly, which eliminates the need for an analog power amplifier. The receiver consists of an LNA and a clocked correlator. In order to reduce the

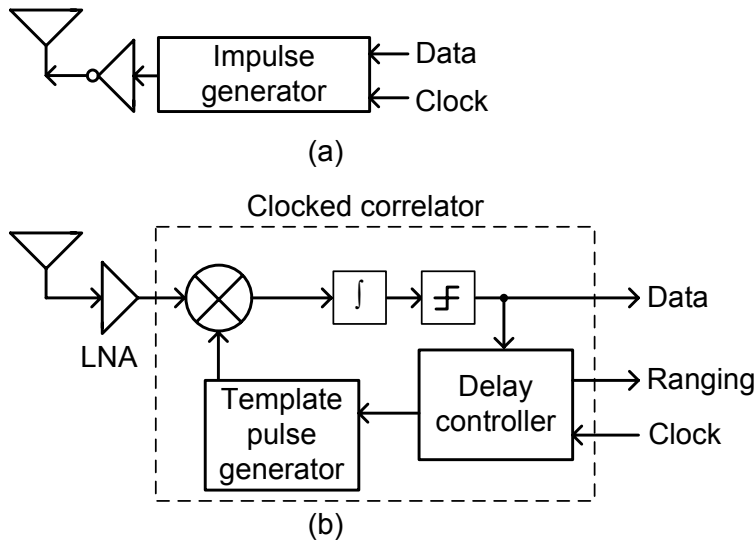


Figure 2.3: An IR-UWB transceiver architecture for (a) transmitter and (b) receiver [1].

power consumption, the LNA and correlator are operating intermittently. The clocked correlator consists of a mixer/integrator, comparator, template pulse generator, and delay controller. This is an example of power consumption reduction technique, which some of the algorithms are combined with analog domain implementation. In this architecture, the clocked correlator saves the area and power, which is normally required for an over-1-GHz ADC designed with conventional receiver architecture. The correlator converts the received RF signal to the baseband signal for further detection. When the received signal and the reference pulse are synchronized in phase, a peak emerges to complete the detection process. A transmitter with all digital block is shown in Fig. 2.4. The pulse trains with 2 ns width are modulated by input data with OOK modulation and the differential signal is provided to the antenna by the CMOS buffer. This transceiver is used for 1-Mb/s data communications, with a power consumption of 4.7 mW.

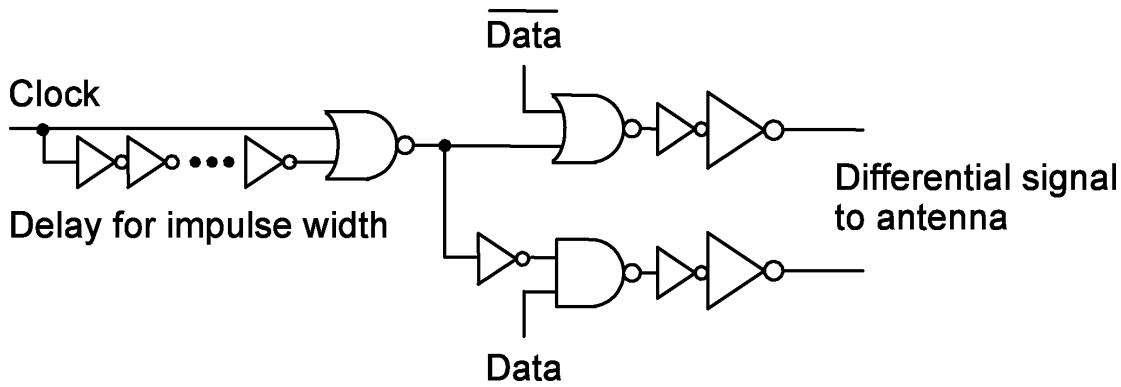


Figure 2.4: All digital transmitter [1].

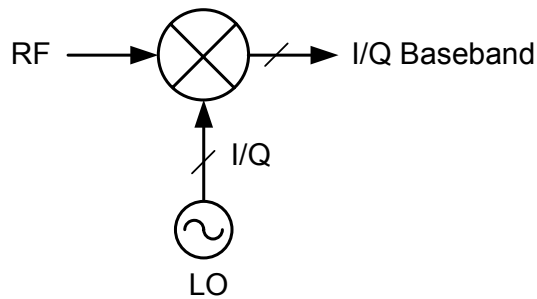


Figure 2.5: Direct-conversion receiver architecture.

## 2.1.2 Multiband OFDM UWB–Receiver Architectures

### 2.1.2.1 Direct-Conversion Receiver

The simplest way to down-convert the input RF signal to the baseband signal, is to use a LO frequency at the same frequency as RF frequency, known as direct-conversion technique, as shown in Fig. 2.5. This architecture allows for the highest level of integration, and offers the lowest cost between all architectures. It also avoids the need for image rejection filter, as the image is the signal itself. It is important to note that accurate quadrature balance in the receiver is still required in a direct-conversion receiver, to reduce the power level of the image. The image-rejection ratio in this architecture is determined by the phase/amplitude mismatch of the I/Q in quadrature oscillator. In addition, process variation adds to the phase and amplitude mismatch.

On the other hand, utilizing the direct-conversion receiver requires quadrature LO generation. Considering proper matching, and layout techniques, it is more difficult to keep the proper matching at high frequency compared to the low frequency. This is because at high frequency more parasitics appear at the LO and RF path. The LO generation is another challenge, particularly in the voltage control oscillator (VCO) circuit. The high power consumption, tuning-range frequency, and LO radiation of the VCO are few examples of the drawbacks in using direct-conversion technique. The other disadvantage associated with this technique is that LO signal, which is applied to the mixer circuit, has a tendency to leak toward the antenna. This radiated LO signal may interfere with other electrical devices within the radiation area of the antenna, such as, other radio or television receivers. So LO-to-RF coupling is problematic in this architecture. Moreover, flicker noise can be a problem, especially in the CMOS implementations. Low frequency noise of the switches in the mixer stage can be down-converted to the baseband and corrupt the signal. Fortunately, the wideband nature of the modulated signal can partially reduce the flicker noise problem. The other problem is the DC offset due to the self-mixing or mismatches, which is amplified by the large gain at the baseband chain. The DC offset is at the baseband, which is not easy to remove by a high pass filter (e.g., AC coupling).

A block diagram of MB-OFDM UWB receiver is shown in Fig. 2.6, which consist of an LNA followed by a correlator. This architecture is presented as a direct-conversion receiver. A preselect filter is placed right after the antenna [22], to reject the out-of-band signals, noise, and images thus passes only the desired UWB signal. After signal passes through the LNA, down-conversion mixer will convert the RF signal to the baseband. The low-pass filter (LPF) removes the adjacent signals, while the voltage gain amplifier (VGA) sets the level of the signal. After this, the analog-to-digital converter (ADC) performs the fast Fourier transform (FFT) to allow for digital signal processing, which is aimed for recovering the signal.

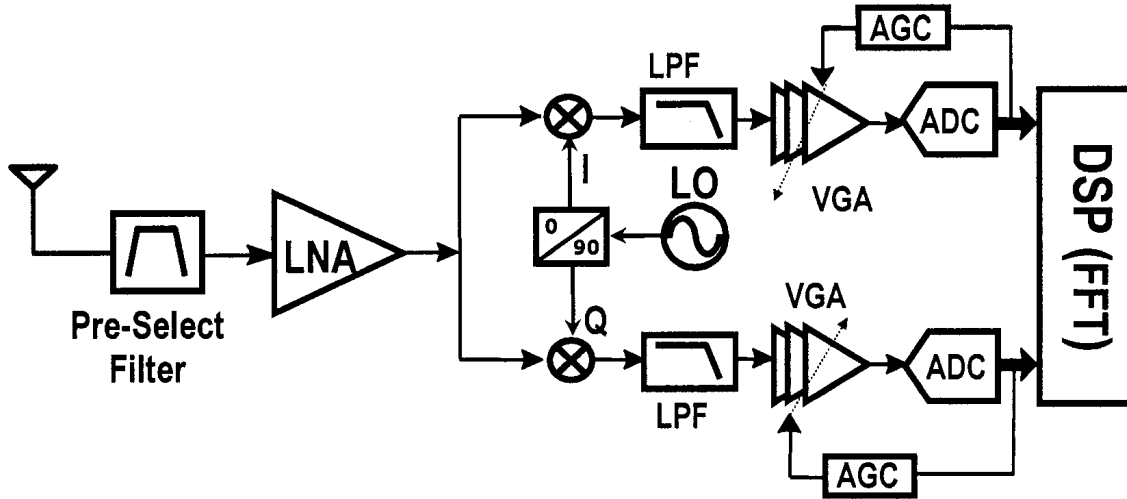


Figure 2.6: An example of MB-OFDM UWB receiver front-end.

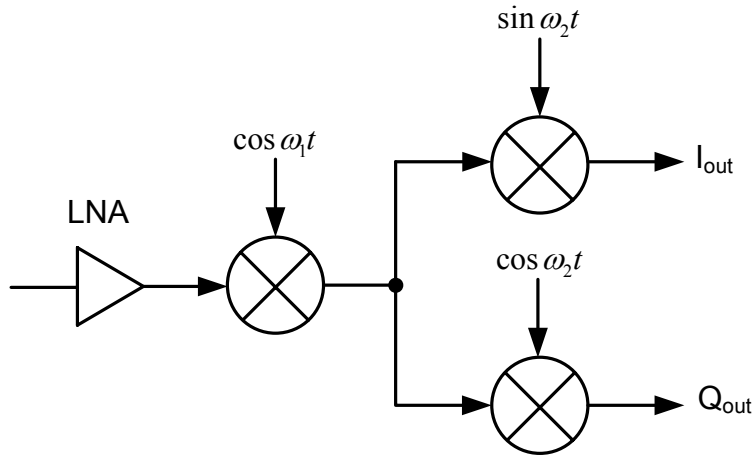


Figure 2.7: Heterodyne receiver architecture.

### 2.1.2.2 Heterodyne Architecture

The architecture of a heterodyne receiver is shown in Fig. 2.7. As it is shown, the down-conversion is performed into two steps. The main advantage of this architecture over the direct-conversion architecture is the use of low LO frequencies, resulting in relaxed layout routing in the quadrature circuit, especially VCO. The input frequency ( $f_{in}$ ) in the first mixer is down-converted to  $f_{in} - f_1$ , and then the result will be further down-converted to the baseband ( $f_{in} - (f_1 + f_2)$ ) in the second quadrature mixer. The first mixer is

drived with a single LO signal, which reduces the complexity of the receiver. The LO frequency planing for  $f_1$  and  $f_2$  can be a fraction of oscillator frequency  $f_{osc}$  such that  $f_1 = N \times f_{osc}$  and  $f_2 = f_{osc} \div M$ , where  $N$  and  $M$  are defined as ( $N = 1$  &  $M = 2$ ), ( $N = 2$  &  $M = 1$ ), and ( $N = M = 1$ ). For instance to operate at 6 GHz, three special cases of ( $N = 1$  &  $M = 2$ ), ( $N = 2$  &  $M = 1$ ), and ( $N = M = 1$ ) corresponding to  $f_{osc} = 4$  GHz,  $f_{osc} = 2$  GHz, and  $f_{osc} = 3$  GHz, respectively.

In the case when  $N = M = 1$ ,  $f_{osc} = f_{in}/2$  it obviates the need for frequency division and multiplication [23]. This frequency plan places the image signal nearby zero, which simplifies the design and routing of the LO signals. This technique is further discussed in chapter 6.

## 2.2 UWB Applications

The ultra-wideband technology has been around since the 1980s, but it has been mainly used for radar-based applications, because of the wideband nature of the signal that results in a very accurate timing information. However, due to the recent developments in high-speed switching technology, the UWB is becoming more attractive for low-cost consumer communications applications. In order to meet the low-cost requirement of product applications, MB-OFDM system is designed to minimize the transceiver architecture complexity. For the wireless systems it is very useful to send, 1) a lot of data, 2) very far, 3) very fast, 4) for many users and 5) all at once. Unfortunately, it is impossible to achieve all five attributes simultaneously. As explained above, the main differences between the UWB and the other narrowband or wideband systems is the bandwidth of the UWB systems, as defined by FCC is more than 25% of a center frequency. Clearly, this bandwidth is much greater than the bandwidth used by any current technology for communications systems. Also, the UWB is typically implemented in a carrierless fashion, on the other hand, conventional narrowband systems use RF carriers to convert the

signal on the frequency domain from baseband to the carrier frequency, where the system is allowed to operate.

The high data rates afforded by the UWB systems is suitable for the applications such as video distribution and/or video teleconferencing for, which the quality of the service is very important. Short-range wireless in general and ultra-wideband in particular, has a growing demand and capability for wireless data in portable devices at higher bandwidth, but lower in the cost and power consumption compared to the current available technologies. For the short-range operation, the average transmit power of pulses for duration of one nanosecond with a low duty cycle is very low. With an ultra-wideband spectrum bandwidth, the power spectral density of the UWB signals is extremely low, compared to the narrowband systems. This gives rise to the potential that the UWB systems can coexist with narrowband radio systems, operating in the same spectrum without causing undue interference. Also, the UWB operates with emission levels commensurate with common digital devices such as laptop computers, palm pilots, and pocket calculators.

## **2.3 UWB Transceiver Design Challenges**

Due to the stringent requirements of the UWB technology, there are challenges facing the design of the UWB RF front-end circuits, especially when it is implemented in the low cost CMOS technology. These challenges can be classified as: (a) distortion of the received signal, which can cause channel fading, (b) performance degradation due to the interference signals and narrowband jamming, (c) synchronization of very short pulses at the receiver. The challenges in (a) and (b) are discussed in this thesis. The concept of the synchronization of very short pulses is related to the impulse radio UWB, which means that the arrival time of the received signal should be synchronized.

The UWB technology is susceptible to in-band interference from existing bands such as those used by IEEE 802.11a radios. In other words, when receiving one channel,

signals in other channels enter the receiver and appear as blockers. The UWB antennas present designers with new opportunities and challenges such as; the UWB antenna must exhibit a nearly omni-directional radiation pattern for a wide range of frequencies, the wideband impedance match, and a linear phase response (i.e., flat group delay). Another important aspect in the UWB system design is that of the interface between the antenna and the RF front-end. The parasitic inductances and capacitances from interface can be absorbed into the filter/matching network between the antenna and circuit front-end, to reduce the parasitic affects. With analytical tools it is possible to examine the impact of the extracted matching network, so the impact on the wideband noise figure and gain can be analyzed. The UWB transmitted power level is required to be below that of the noise emission allowed for the electronic equipments to increase the sensitivity of the receiver.

Since the bandwidth of the UWB licensed by FCC is from 3.1–10.6 GHz, this implies that RF front-end including LNA and down-conversion mixer, should be able to process a bandwidth over a wide range of frequency. From circuit design point of view, it is important to realize that the design of the UWB transceivers have to overcome the following challenges; 1) the need for an LNA with a wideband input matching to a  $50 \Omega$  antenna, 2) gain flatness of the LNA; because the transmission and reception of the UWB pulse requires approximately constant group delay, 3) to design broadband receive/transmit switch at the antenna, 4) desensitization problem due to the WLAN interferences, and 5) a synthesizer with fast band hopping. For example, in a frequency-hopping direct-conversion receiver, imperfections and mismatches in the RF chain result in undesired signal, as well as a fixed noise at the hopping frequency. All these challenges need to be addressed in order to achieve a successful wideband transceiver design.

# Chapter 3

## Introduction to UWB Low-Noise Amplifier

### 3.1 Broadband Amplifiers

The cost and integration advantages of CMOS technology have motivated extensive studies in the high speed CMOS design for wireless applications. Recently, many wideband LNA designs in CMOS technology have been reported [4]–[24]. The wideband LNA designs can be classified as multi-band LNAs, distributed amplifiers (DA), and broadband noise canceling LNAs. Among wideband LNA designs, distributed and common-gate amplifiers suffer from high noise figure. Alternatively, the negative feedback amplifier topology provides wide bandwidth while reducing the gain of the circuit. Another important property of the negative feedback is the suppression of the nonlinearity. However, in the feedback circuits the stability may suffer if the loop gain is too high and the feedback becomes positive. Therefore, compensation techniques are required to eliminate the instability problem. In the noise canceling technique reported in [25], 5 inductors are used and the noise figure is 4.5–5.1 dB from 1.2–11.9 GHz with 20 mW power consumption, which makes it unattractive for low cost, low power applications. In [24], several narrowband amplifiers with different resonance frequencies are cascaded. Therefore, the resulting multistage amplifier provides a broadband response. This circuit required 8

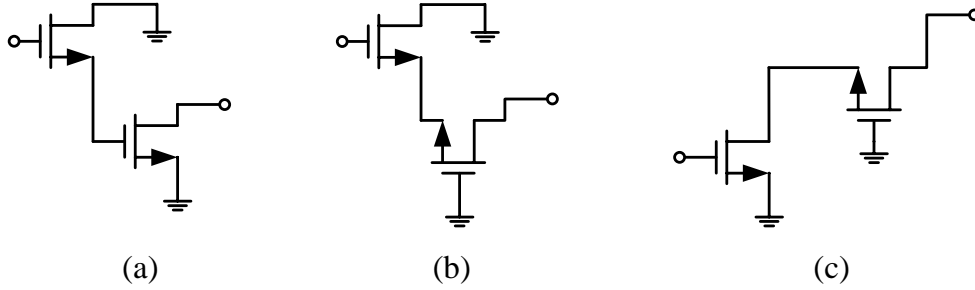


Figure 3.1: Wideband two-stage amplifiers, (a) a source follower driving a common-source amplifier, (b) a source follower driving a common-gate amplifier, (c) a common-source amplifier drives a common-gate amplifier.

inductors in a differential architecture and since many stages are cascaded it is prone to poor linearity and stability problems.

It is well known that the amplifier frequency response suffers from Miller feedback capacitance  $C_\mu$  and bandwidth is in tradeoff with the gain. Conventionally, the Miller effect can be reduced, as shown in Fig. 3.1. In Fig. 3.1(a), a source follower drives a common-source amplifier, thus lowering the source resistance seen by the Miller capacitor. In Fig. 3.1(b), a source follower drives a common-gate amplifier, increasing the input impedance of source follower amplifier without drastically altering the gain.

The third amplifier, shown in Fig. 3.1(c), is a cascade of a common-source and common-gate amplifier, which is widely known as cascode topology. This amplifier is simple and elegant as it provides both voltage and current gain. Since the devices can be stacked, the DC current is shared by the two stages, resulting in a low-power amplifier block. These schematics are the basic idea of the broadband amplifier design, now lets move on to a more detailed design. In the amplifier shown in Fig. 3.2, the voltage gain across the Miller capacitor can be made as small as desired by sizing the cascode transistor at the cost of loading amplifier with a non-dominant pole. In a well-balanced design, the dominant pole is due to the output capacitor,  $C_o$ , of the amplifier

$$\omega_{-3dB} = \frac{1}{R_L C_o} \quad (\text{Eq. 3.1})$$

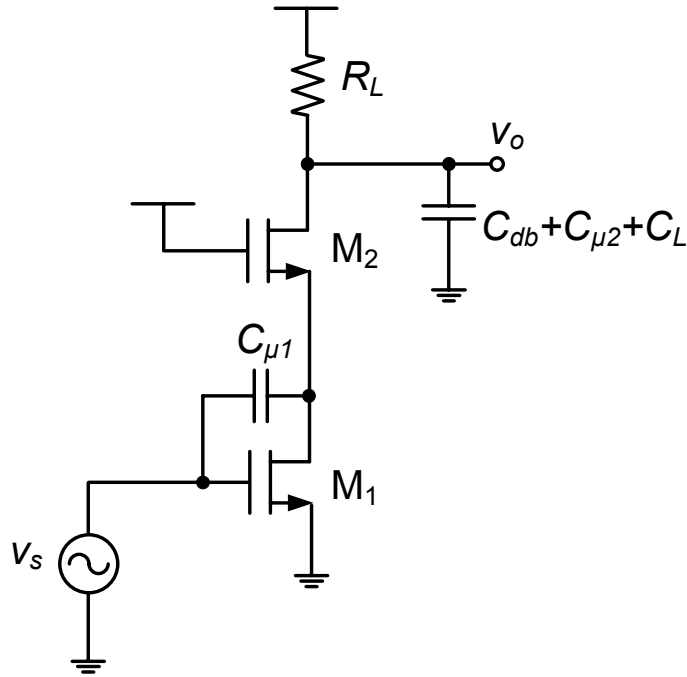


Figure 3.2: A resistive load cascode amplifier, biasing not shown.

where  $C_o = C_{\mu 2} + C_{db} + C_L$  and  $C_{\mu 2}$  is the Miller capacitor of  $M_2$ . The capacitor  $C_o$  is independent of the gain of the amplifier, since the gate terminal of  $M_2$  is fixed. The cascode boosts the gain of the amplifier by allowing a larger load resistance ( $g_m r_o^2$ ) for a given bandwidth. The gain-bandwidth product of the amplifier is then bounded by

$$A_v \times \omega_{-3dB} = \frac{g_m}{C_{\mu 2} + C_{db} + C_L} \approx \frac{g_m}{C_L} \quad (\text{Eq. 3.2})$$

In theory, this amplifier has a gain-bandwidth product approaching a significant fraction of the  $\omega_T$  of the device.

There are several problems with this amplifier. First, in terms of the gain, we have to pay with headroom since a larger load resistance  $R_L$  consumes larger DC headroom. This may lead to unreasonably high supply voltage. In most applications, we do not have control over the supply due to the intrinsic breakdown in a transistor. Higher  $f_T$  device also have lower breakdown voltage, leading to a natural limit to the gain of the amplifier. For example, 130 nm CMOS technology may limit the supply to 1.2 V. In

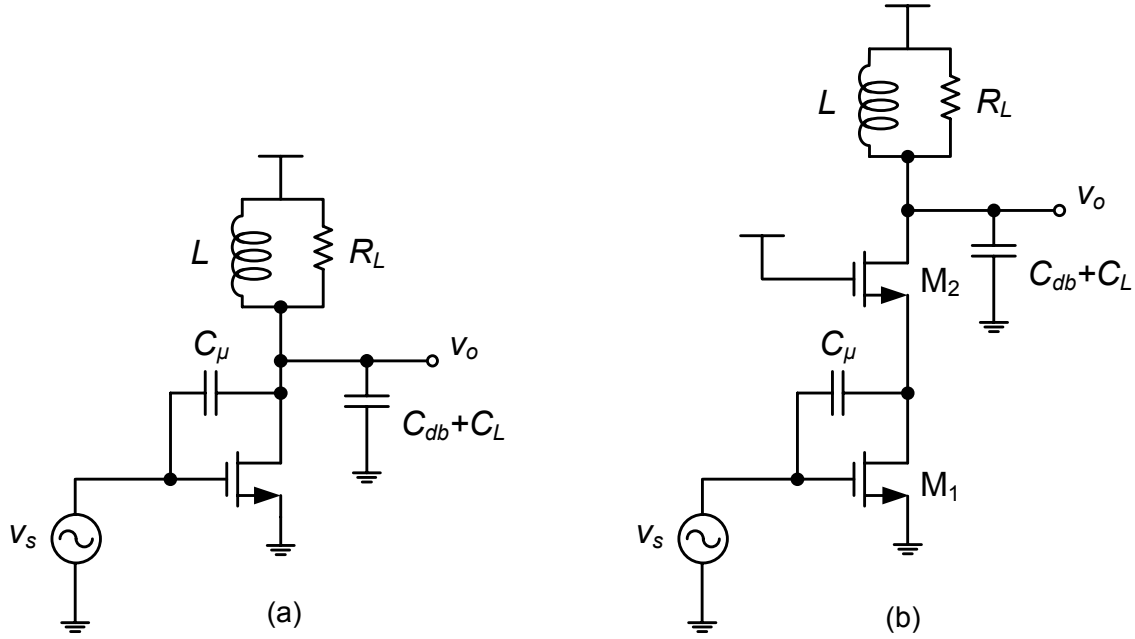


Figure 3.3: (a) A single stage  $LC$  tuned amplifier, (b) a cascode  $LC$  tuned amplifier. Biasing not shown.

the analog circuit, the voltage headroom is partially solved using active load. However, active load has several drawbacks. First it further limits the output swing of the amplifier, since the operation into triode region should be avoided for both the load and the cascode transconductance device. Furthermore, the non-linearity of the load degrades the linearity of the amplifier, leading to excess distortion.

### 3.1.1 Tuned Amplifiers

The  $RLC$  loaded amplifier shown in Fig. 3.3(a) solves several of the headroom problems of the circuit in Fig. 3.2. In Fig. 3.3(a), a single transconductance device drives a shunt  $RLC$  load, which results in

$$A_{v,max} = -g_m Z(j\omega) = \frac{-g_m}{Y(j\omega)} \quad (\text{Eq. 3.3})$$

In order to maximize the gain, we have to employ high- $Q$  inductors in the load and omit the resistor load  $R_L$ . Assuming the  $Q$ -factor is dominated by the inductor, the peak gain

is

$$A_{v,\max} \approx -g_m (R_{LP}) = -g_m Q_L \cdot \omega L \quad (\text{Eq. 3.4})$$

where  $R_{LP}$  is the equivalent parallel resistance of the inductor  $L$ . The gain is maximized at a fixed bias current and frequency is increased by maximizing the  $Q_L \times L$  product. So, in theory, there is no limit to the voltage gain of the amplifier as long as the quality factor  $Q_L$  can increase. Note that the parasitic capacitances of the circuit are resonated by the shunt inductor. In other word,  $L$  is chosen such that

$$LC_{eff}\omega^2 = 1 \quad (\text{Eq. 3.5})$$

where  $C_{eff} = C_{db} + (1 - |A_v^{-1}|)C_\mu + C_L$ . The ability of this circuit to tune out the parasitic capacitance is the major advantage of the tuned amplifier. The other important advantage of this circuit is that there is practically no  $DC$  voltage drop across the inductor, allowing very low-supply voltage operation. Another less obvious advantage is the improved voltage swing at the output of the amplifier. Usually the voltage swing is limited by the supply voltage and  $V_{DS,sat}$  of the amplifier. In this case though, the voltage can swing above the supply voltage, since the DC voltage drop across the inductor is zero. Beside the advantage of boosting output impedance and maximizing the  $Q$  of the load, cascode device in Fig. 3.3(b) solves the stability issue of the circuit.

It is interesting to note that the bandwidth of the amplifier is still determined by the time constant  $R_p C_{eff}$  at the load. The bandwidth is given by

$$BW = \frac{\omega_0}{Q} = \frac{\omega_0}{\omega_0 R_p C_{eff}} = \frac{1}{R_p C_{eff}} \quad (\text{Eq. 3.6})$$

where  $R_p = R_L || r_o || R_{LP}$  and  $R_{LP}$  is the parallel resistance of the inductor  $L$ . The ultimate sacrifice for the high-frequency operation in a tuned amplifier is that the amplifier is

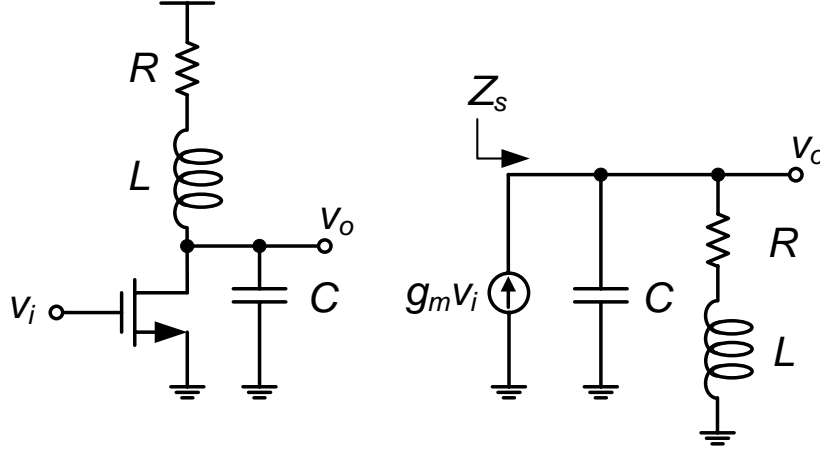


Figure 3.4: (a) A common-source amplifier with a shunt-peaking load, (b) equivalent circuit for the shunt-peaking amplifier.

narrowband. In fact, the larger is the  $Q$ -factor of the tank, the higher is the gain and the lower the bandwidth. To get some of the bandwidth back, it requires other techniques such as shunt peaking [26] and distributed amplifiers [27].

### 3.1.2 Shunt and Series Peaking

As shown in Fig. 3.4(a), in the simplest form, a load consisting of a resistor and an inductor in series lead to a zero in the transfer function. This can be used to cancel the pole of the transfer function and within a band of frequencies create a flat-frequency response. With reference to Fig. 3.4(b), one can get

$$Z(s) = (sL + R) \parallel \frac{1}{sC} = \frac{R(1 + s\frac{1}{R})}{1 + sRC + s^2LC} \quad (\text{Eq. 3.7})$$

This equation can be written in normalized form with  $m$  as the ratio of time constant

$$m = \frac{RC}{L/R} \quad (\text{Eq. 3.8})$$

letting  $\tau = L/R$  we have

$$Z(s) = \frac{R(1 + s\tau)}{1 + s\tau m + s^2\tau^2 m} \quad (\text{Eq. 3.9})$$

and by solving the above quadratic equation [28], the following equality is achieved

$$\frac{\omega}{\omega_1} = \sqrt{\left(1 + m - \frac{m^2}{2}\right) + \left(1 + m - \frac{m^2}{2}\right)^2 + m^2} \quad (\text{Eq. 3.10})$$

The maximum bandwidth obtainable occurs for  $m = \sqrt{2}$  or a bandwidth boost of 85% [26], [28]. This comes at the expense of 20% peaking. A good compromise value occurs for  $m = 2$ , which leads to only 3% peaking and a bandwidth of 82%. Finally, in a broadband application where a linear phase or flat delay response is desired, where  $m \approx 3.1$  with 57% bandwidth enhancement is selected. In this method, although the bandwidth is improved but peaking still is high.

Another example to obtain a wideband response is to use series peaking technique as shown in Fig. 3.5 [2]. Compared to a common-source (CS) LNA, a common-gate

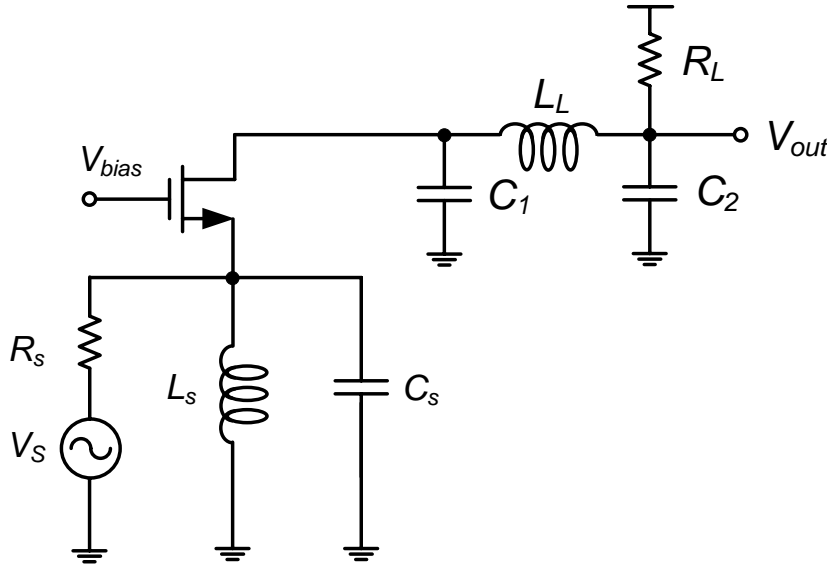


Figure 3.5: Series peaking in a common-gate low noise amplifier with stagger compensation [2].

(CG) LNA offers design simplicity, low power, and good linearity. In the common-gate LNA, the input match condition ( $g_m = 1/R_s$ ) keeps the size of the transistor small so the gate-source and gate-drain capacitances also remain small. As the value of  $R_s$  is

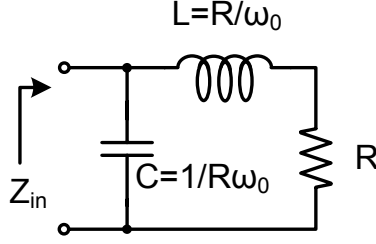


Figure 3.6: Second-order low-pass ladder filter.

fixed ( $50 \Omega$ ),  $R_L$  is necessarily large for high gain product. Because of high  $R_L$ , together with the total load capacitance  $C_2$ , sets a bandwidth constraint, which necessitates the use of techniques for the bandwidth extension. Thus, a low- $Q$  series-peaked inductor is utilized at the output for a broadband response. The capacitor  $C_s$  is tuned out by a source inductor  $L_s$  at the resonant frequency  $\omega_s = 1/\sqrt{L_s C_s}$ . Inductor  $L_s$  and capacitor  $C_s$  form a shunt parallel resonant network with  $Q = \omega_s C_s R_s / 2$  [2]. A low  $Q$  shunt network for the input suggests a possible broadband impedance match. The fundamental difference between the input matching networks is that the CS-LNA uses series resonant while the CG-LNA uses parallel resonant. By proper sizing the source inductor  $L_s$  and the input transistor ( $W/L$ ),  $\omega_s$  is optimized to meet the necessary specifications over the entire 3.1–10.6 GHz band.

### 3.1.3 Wideband Input Matching and Reactive Series Feedback

Since the input matching circuit can affect performance of the LNA, it is important to design a proper matching network in order to cover a wide range of frequency. Wideband impedance matching was first introduced by Bode [29] and Fano [30] to enhance the bandwidth of the antenna. Fano's method is a general solution to enhance the bandwidth of the narrowband circuits and it is possible to extend the bandwidth of the narrowband LNA.

Consider the second-order low-pass ladder filter as two port network in Fig. 3.6. Under the resonance condition, the input impedance of the network is real and equals to

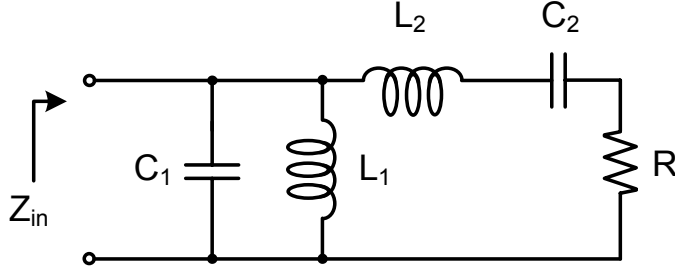


Figure 3.7: Fourth-order bandpass ladder filter.

*R*. Therefore, the values of  $L$  and  $C$  are calculated as

$$\begin{aligned} L &= \frac{R}{\omega_0} \\ C &= \frac{1}{\omega_0 R} \end{aligned} \quad (\text{Eq. 3.11})$$

Using the low-pass to bandpass transformation, the series inductor transformed to series  $LC$ , and shunt capacitor transforms to parallel  $LC$  network. Transforming the second-order filter in Fig. 3.6, results in a fourth-order filter, as shown in Fig. 3.7. The new value of the capacitors and inductors are determined as

$$L_1 = (\omega_2 - \omega_1)/C\omega_0^2 \approx \frac{R}{\omega_1} \quad (\text{Eq. 3.12})$$

$$C_1 = C/(\omega_2 - \omega_1) \approx \frac{1}{R\omega_2} \quad (\text{Eq. 3.13})$$

$$L_2 = L/(\omega_2 - \omega_1) \approx \frac{R}{\omega_2} \quad (\text{Eq. 3.14})$$

$$C_2 = (\omega_2 - \omega_1)/L\omega_0^2 \approx \frac{1}{R\omega_1} \quad (\text{Eq. 3.15})$$

where  $\omega_1$ ,  $\omega_2$ , and  $\omega_0$  are the low band, high band, and resonance frequency of the series and parallel devices, respectively. Therefore, the resulted bandpass network can be used as a wideband matching network, to design a wideband LNA.

Input matching network often must convert a predominantly imaginary load impedance to a real value. Consider the circuit shown in Fig. 3.8(a). At moderate frequencies the input is dominated by  $C_{gs}$ . We need to transform the input capacitance to a real load

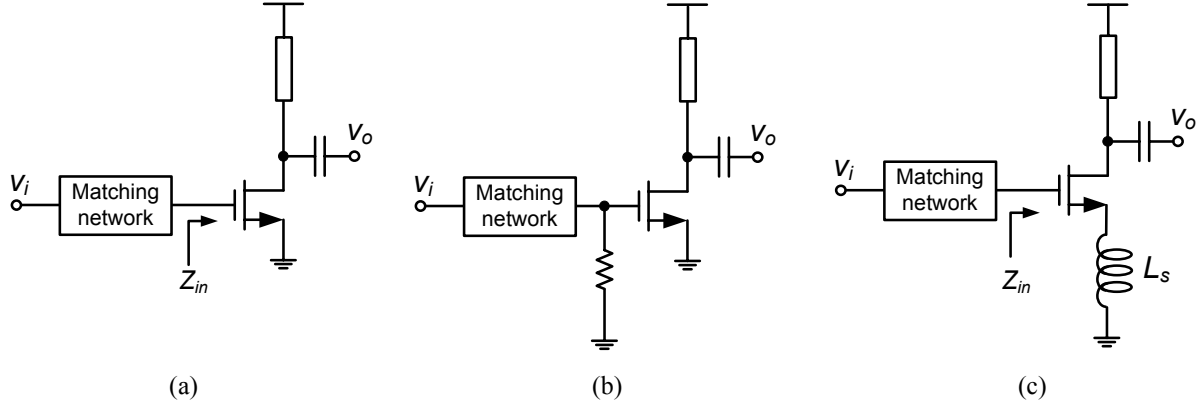


Figure 3.8: (a) Matching network is used to achieve real value, (b) a simple solution is to simply terminate the matching network with a physical resistor, (c) a more elegant solution uses a feedback synthesized resistor input match.

resistance. Any real MOS amplifier has a real component, which contributes to the input impedance. If the transistor layout has ample fingers to minimize the physical polysilicon gate resistance, the remaining gate-induced channel resistance is given by  $1/5g_m$  [26]. Thus the  $Q$ -factor of the input of the MOS transistor is given by

$$Q_{gate} \approx \frac{5g_m}{\omega C_{gs}} = 5 \frac{\omega_T}{\omega} \quad (\text{Eq. 3.16})$$

At moderate frequencies  $\omega \ll \omega_T$ , this is a high- $Q$  input impedance. If we resonate out this capacitor ( $C_{gs}$ ) with a shunt inductor, the resulting shunt resistance  $Q^2 R$  is too large to match to the low-source resistance. On the other hand, if we use a series inductor, the input resistance is simply the equivalent series resistance of the inductor  $R$ , too small to match. One explicit way is to add resistor to the gate, as shown in Fig. 3.8(b), but this method will add noise to the circuit. A more elegant solution is to add an inductor to the source of the amplifier, shown in Fig. 3.8(c). The action of this feedback produces a term, which in resonance becomes purely real as

$$\Re(Z_{in}) = R_{in} = \frac{g_m L_s}{C_{gs}} = \omega_T L_s \quad (\text{Eq. 3.17})$$

By controlling the value of the  $L_s$ , we can control the input impedance. We can also vary the  $\omega_T$  of the device by placing a capacitor in the shunt with  $C_{gs}$ .

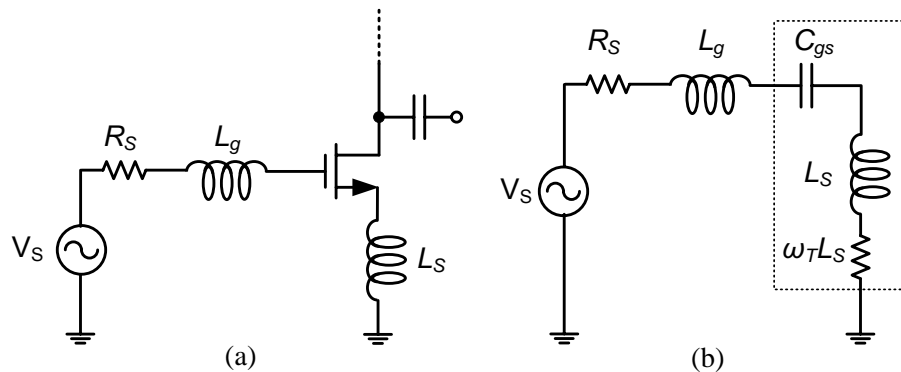


Figure 3.9: (a) The complete input-matching requires a gate inductor  $L_g$  to resonate with the capacitor  $C_{gs}$ . (b) the equivalent circuit for the input match is a series  $RLC$  circuit.

It is interesting to observe that the source impedance in effect drives a series  $RLC$  circuit, shown in Fig. 3.9(a) with equivalent circuit in Fig. 3.9(b). The inductively degenerated transistor in Fig. 3.9(b) follows the same concept in Fig. 3.7. The bandwidth of the matching stage of the inductively degenerated amplifier is set by the  $Q$ -factor of the input. Since the source impedance is fixed, there is little freedom in controlling the  $Q$ -factor of the input stage. But many applications require larger bandwidth. For example an ultra-wideband (UWB) amplifier needs a 3–8 GHz band. Therefore, this input matching is not suitable for a wideband input matching, and a filter with higher order is needed.

### 3.1.4 Shunt-Shunt Feedback

Consider a simplified resistive-feedback amplifier, as shown in Fig. 3.10(a). A simple single stage amplifier is designed with shunt-shunt feedback resistor,  $R_F$ . The equivalent small-signal model of the transimpedance amplifier is shown in Fig. 3.10(b), where  $g_m$  represents the transconductance of the transistor. Using the small-signal model in Fig. 3.10(b), the voltage gain of the amplifier can be derived as [31]

$$A_v = \frac{V_{OUT}}{V_{IN}} = - \left( g_m - \frac{1}{R_F} \right) (R_L \parallel R_F) \quad (\text{Eq. 3.18})$$

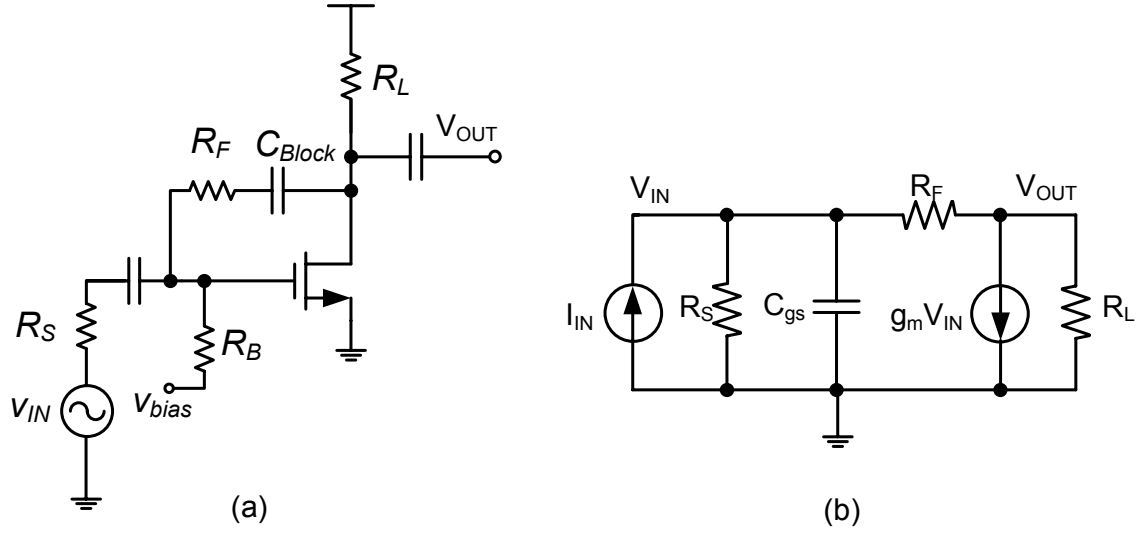


Figure 3.10: (a) Simplified schematic, and, (b) small-signal model of a shunt-shunt feedback amplifier.

Shunt-shunt feedback reduces the input impedance of the amplifier by a factor of  $(1 + af)$  and the input impedance of the amplifier is

$$R_{in} = \frac{R_S \parallel R_F}{1 + af} \approx \frac{R_S}{1 + af} \quad (\text{Eq. 3.19})$$

$$a = -(R_S \parallel R_F) g_m (R_L \parallel R_F) \quad (\text{Eq. 3.20})$$

$$f = -\frac{1}{R_F} \quad (\text{Eq. 3.21})$$

where  $a$  is the open-loop transimpedance gain,  $f$  is the feedback factor and  $R_F \gg R_S$ . For the input impedance matching,  $R_{in}$  should be equal to  $R_S/2$ , where in this case  $af$  is just below 1, which also ensures the stability condition. In order to achieve low noise figure in this architecture, high open-loop gain is required together with good input matching. The open-loop bandwidth also has to be high to achieve high linearity at high frequencies. The noise figure contribution of each noise source to the total output noise is calculated as [31]

$$NF \approx 1 + \frac{\gamma g_m}{R_S g_m} + \frac{1}{R_S R_L g_m^2} + \frac{4R_S}{R_F} \left( \frac{-1}{1 + \frac{R_S + R_F}{(1 + g_m R_S) R_L}} \right)^2 \quad (\text{Eq. 3.22})$$

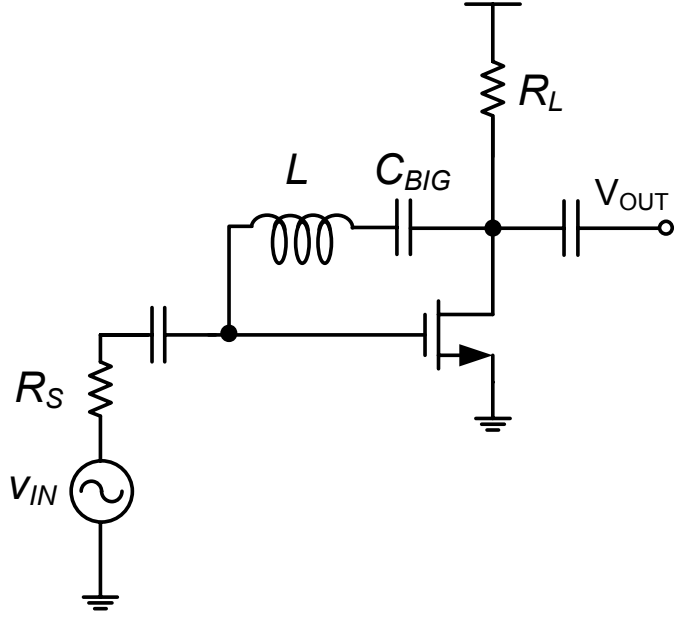


Figure 3.11:  $LC$  shunt-shunt feedback technique.

where  $\gamma g_m$  is the noise excess factor of the transistor. The calculation of (Eq. 3.22) shows that a large feedback resistor  $R_F$  reduces the noise figure contribution. A high  $R_F$  requires a high open-loop gain for input matching, which leads to high power consumption. Although, resistive feedback amplifier can achieve high gain and reasonably low noise figure, circuit techniques are required to improve the power consumption.

Another alternative approach to implement the shunt-shunt feedback is to use  $LC$  network instead of  $RC$  network, Fig. 3.11. This technique uses an inductor  $L$  to resonate out the gate-drain capacitor  $C_{gd}$  of the transistor to improve the reverse signal flow (coupling) from output to the input port. A severe drawback with this architecture is the size of the inductor and capacitor used for the feedback path. Normally, the value of the inductor should be very high to be able to resonate out the parasitic capacitor  $C_{gd}$ . Furthermore, a big value of  $C_{BIG}$  is required, which loads the drain and gate terminals of the transistor. This would reduce the forward gain through the transistor transconductance.

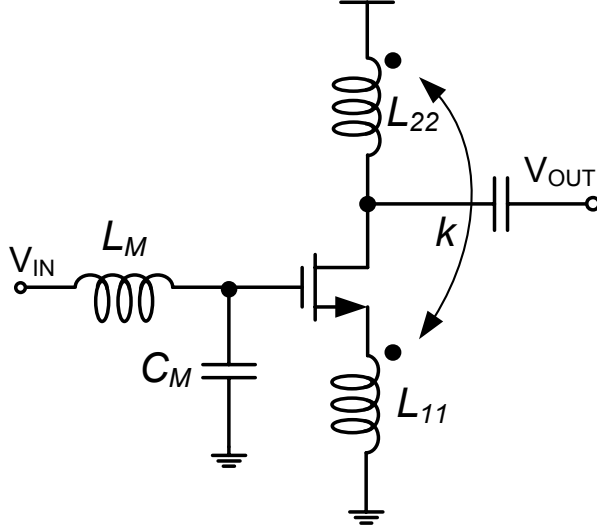


Figure 3.12: Transformer-feedback technique [3].

In [3], a transformer-feedback technique is proposed, which introduces magnetic coupling between drain and source inductors of a common-source transistor, as shown in Fig. 3.12. In this technique, a portion of the output signal is fed back through transformer, which effectively cancels the coupling from output to the input via Miller capacitor  $C_{gd}$  capacitor. The magnetic coupling between the input and output using transformer adds negative feedback. An increase in drain current lowers  $V_{OUT}$  or, equivalently, increases the ac voltage drop across  $L_{22}$  [3]. Therefore,  $V_{gs}$  decreases, which is a negative feedback. The transformer-feedback can be used as a wideband technique, which the bandwidth is restricted by the bandwidth of the transformer. For a given LNA design, the transformer turns ratio  $n$  is often constrained by linearity, gain, and noise specifications. In this design, the coupling coefficient  $k$  is the extra degree of freedom that can be adjusted to obtain desired bandwidth of the LNA. The architecture in Fig. 3.12 can be implemented differentially to reduce the effect of ground path parasitics and to increase common-mode rejection. Therefore the primary and secondary inductances are implemented as a differential transformer with magnetic coupling  $M$ . The input matching network is performed using  $L_M$  and  $C_M$  network, which  $L_M$  is implemented off-chip.

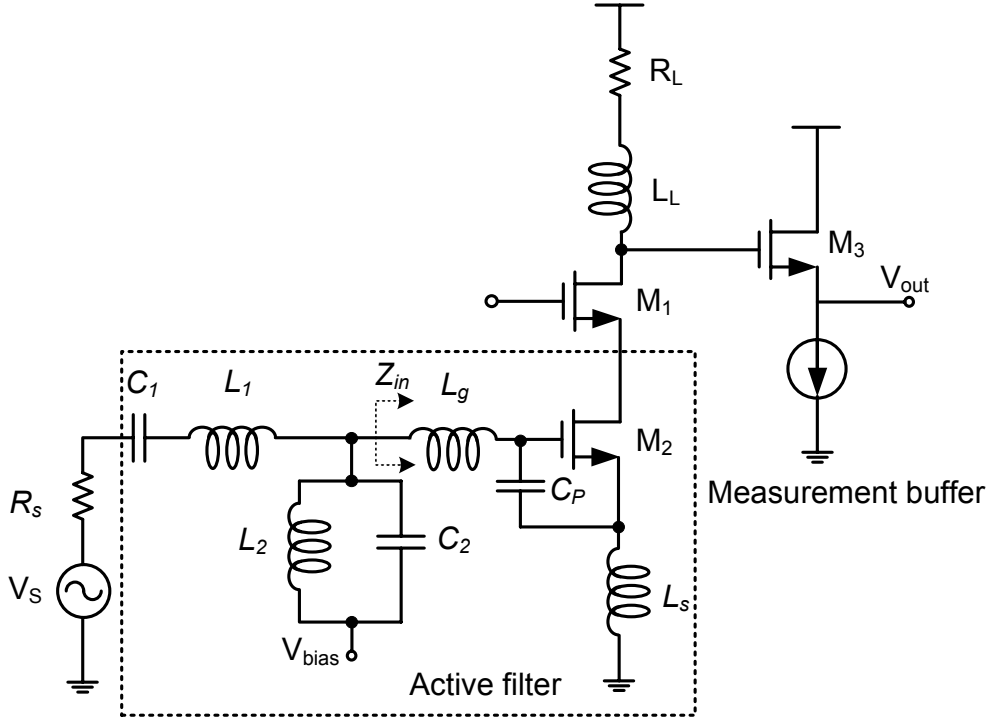


Figure 3.13: An ultra-wideband amplifier using Chebyshev active filter [4].

A broadband amplifier is shown in Fig. 3.13, which employs a three-section Chebyshev active filter at input. The series  $RLC$  network formed by the transconductance stage forms a third section of the filter, where  $R$  is the series resistance of  $L_s$  in the source of transistor and equals  $\omega_T L_s$ , shown before in Fig. 3.9(b). The bandwidth of the matching stage of the inductively degenerated amplifier in Fig. 3.13 is very depended on the  $Q$  factor of the input Chebyshev filter. The input impedance of the MOS transistor with inductive degeneration is achieved as [4]

$$Z_{in}(s) = \frac{1}{s(C_{gs} + C_p)} + s(L_s + L_g) + \omega_T L_s \quad (\text{Eq. 3.23})$$

where  $\omega_T = g_m/(C_{gs} + C_p) = g_m/C_t$ . This network is embedded in the Chebyshev structure to form the input matching network. The series resonance occurs between  $L_s$  and  $C_{gs} + C_p$ . The second series resonance, on the other hand, occurs between  $L_g$  and the equivalent capacitance resulting from the parallel combination of  $L_s$  and  $C_{gd}$  at

frequencies higher than the parallel resonance.

From noise analysis perspective, the noise contribution of the input network is due to the limited quality factor  $Q$  of the integrated inductors. The noise optimization relies on achieving the highest  $Q$  for a given inductance value. The need for high  $Q$  inductor to reduce the noise figure account as a drawback for the design. The noise contribution of the transistor  $M_1$  relies on the choice of its width for a given current bias. A minimum noise figure can be achieved once  $L_s$  and  $C_t$  resonate, and consequently a low noise figure over the entire amplifier bandwidth is obtained.

The voltage gain of the amplifier can be found by  $R_s/W(s)$ , where  $W(s)$  is the transfer function of the Chebyshev filter. The transfer function of the Chebyshev filter is unity in-band and tends to zero out-of-band. So the impedance looking into the amplifier is  $R_s$  in-band, and it is very high out-of-band. The overall gain is [4]

$$\frac{V_{out}}{V_{in}} = -\frac{g_m W(s)}{sC_t R_s} \cdot \frac{R_L \left(1 + \frac{sL_L}{R_L}\right)}{1 + sR_L C_{out} + s^2 L_L C_{out}}. \quad (\text{Eq. 3.24})$$

where  $R_L$  is the total resistance,  $L_L$  is the load inductance, and  $C_{out}$  is the total output parasitic capacitance at the drain of  $M_2$ . The shunt-peaking load is compensating the gain roll off, which in (Eq. 3.24) is set by  $L_L$ . The presence of parasitic capacitor  $C_{out}$  introduces spurious, which should be kept out-of-band.

The results observed from this design benefits from the use of a ladder-filter input matching network. This LNA achieves wide bandwidth and input matching from 3–10 GHz [4]. However, this wideband LNA needs too many components, specifically high  $Q$  inductors, to form the Chebyshev filter at the input. This drawback adds to the area and the cost of the design.

# Chapter 4

## Proposed Wideband Low-Noise Amplifier

One of the major challenges in wideband communications systems is the design of a wideband low-noise amplifier. As the first active component in the receiver chain, the LNA should offer sufficient gain and low noise to keep the overall receiver noise figure as low as possible. In most applications, it is desirable to obtain wideband on-chip input matching to a  $50\ \Omega$  antenna/filter, good linearity, and low power consumption. In addition, gain-flatness over the entire frequency range of interest is necessary to meet the design specifications. These properties are the cornerstones of the wideband LNA design, which affect the total broadband communication system characteristics.

This section introduces a T-coil network to achieve wideband input matching and wideband output response. In this technique the parasitic capacitors of the transistors and inherent mutual inductance of the inductors are taken as a part of the design [32]. In this design, 3 inductors are used, where 2 of the inductors are center-tap inductor, to implement a single-ended LNA.

### 4.1 Circuit Design: Theory and Practice

As mentioned in the last chapter, in [4] a Chebyshev type bandpass filter is used at the input of a common-source amplifier in order to provide good matching over a wide

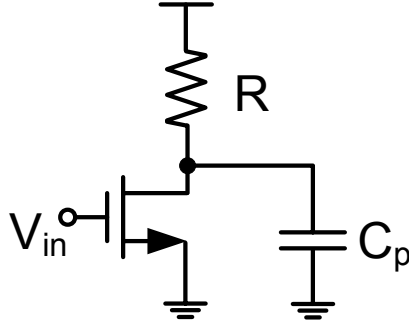


Figure 4.1: Common-source amplifier with output parasitic capacitance  $C_p$

bandwidth. These kind of filters necessitate the use of many components, which occupy a large area and reduce the circuits integration level. Furthermore, the loss associated with the components deteriorates the noise figure of the circuit. Therefore, techniques to alleviate these issues without degrading performance is required.

In general, when the LNA circuit is cascaded with the next stage, the interstage parasitic reactance attenuates the desired bandwidth of the LNA. For example, in Fig. 4.1 parasitic gate-source capacitance  $C_p$  of a mixer or buffer, reduces the circuit performances as it shunts with the output load  $R$  of the common-source amplifier. A dominant pole due to the parasitic  $C_p$  is created at the frequency of  $1/RC_p$ , which reduces the bandwidth. One way to compensate  $C_p$  is to insert an inductor in series with  $R$  at the output of the circuit in Fig. 4.1 to resonate out  $C_p$ . However, the existence of resistor  $R$  will require extra voltage headroom, which limits the allowable bias current. In the discussions below, different peaking techniques are introduced to improve the bandwidth. Shown in Fig. 4.2(a), a series inductor  $L$  across  $R$  and  $C$  is used to create a series peaking in the frequency response. The series inductor creates a second-order  $RLC$  resonant circuit with a resonance frequency of  $\omega_0=1/\sqrt{LC}$ . The transfer function of the circuit in Fig. 4.2(a) is the same with the case when  $R$  and  $C$  are swapped, since  $L$  is in series with  $C$

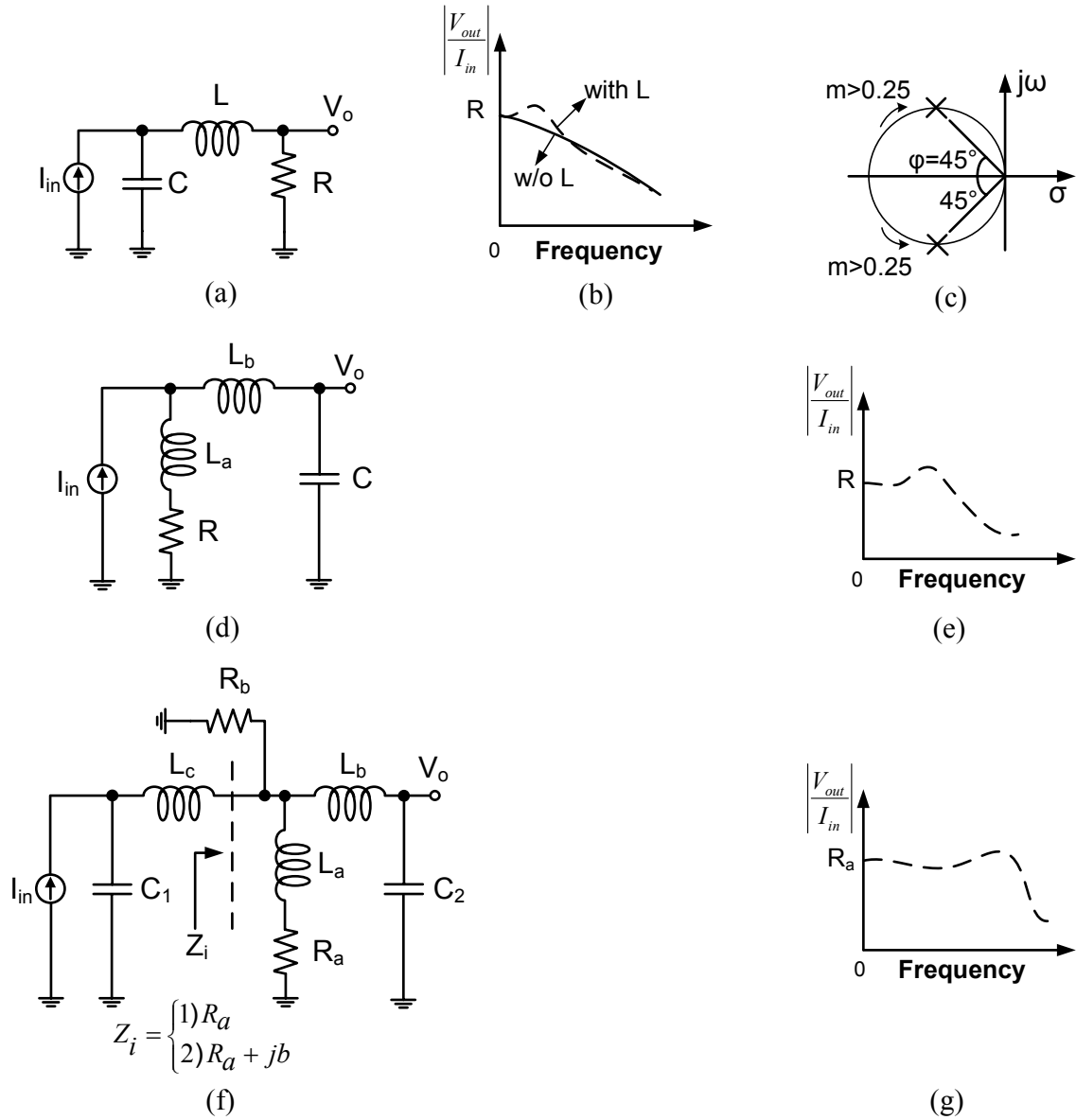


Figure 4.2: (a) Series inductive peaking circuit, (b) frequency response of the circuit (a) with and without  $L$ , (c) complex poles location for maximum gain-flatness response, (d) shunt-series inductive peaking circuit, (e) frequency response of the shunt-series peaking circuit, (f) series-shunt-series peaking including a T-coil peaking network, (g) series-shunt-series peaking frequency response.

in both cases. The transfer function of the series inductive peaking circuit is

$$H_1(s) = \frac{R}{s^2LC + sRC + 1} = \frac{1}{mR^2C^2} \cdot \frac{R}{s^2 + s/mRC + 1/mR^2C^2}. \quad (\text{Eq. 4.1})$$

where  $L = mR^2C$ ,  $m$  is a dimensionless parameter that defines the poles location and determines the overdamped response of the filter. From (Eq. 4.1), the complex conjugate poles are

$$s_{1,2} = -\frac{1}{2mRC} \pm j\sqrt{\frac{1}{mR^2C^2} - \frac{1}{4m^2R^2C^2}} = \frac{1}{2mRC} (-1 \pm j\sqrt{4m-1}). \quad (\text{Eq. 4.2})$$

From the frequency response shown in Fig. 4.2(b), the circuit including the series peaking inductor improves the bandwidth compared to the circuit without  $L$ . For this circuit with  $m = 0.25$  poles are equal to  $s_1 = s_2 = -2/RC$  near to the critically damped response. As the value of  $m$  increases ( $m > 0.25$ ) poles become complex conjugate and travel along the real axis toward the  $j\omega$  axis, as shown in Fig. 4.2(c). If we equate the standard 2<sup>nd</sup>-order Butterworth poles with (Eq. 4.2), the components values are calculated and maximum gain-flatness response is satisfied. As shown in Fig. 4.2(c), poles angle ( $\varphi$ ) should be equal to  $45^\circ$  from origin to get the maximum gain-flatness response [33].

The circuit in Fig. 4.2(a) with two reactance components represents one resonance frequency. The circuits with more than two reactance components have more than one resonance mode. A multi-resonance circuit can be utilized to cover a wider range of frequency than a single resonance circuit. For this reason, the resonance frequencies should be chosen properly to optimize the bandwidth of interest.

Now consider the circuit shown in Fig. 4.2(d). An inductor  $L_a$  in series with  $R$  adds a shunt peaking to the series peaking  $L_b$ , results in a shunt-series peaking circuit which improve the bandwidth. The frequency response of this circuit is shown in Fig. 4.2(e). The transfer function of the shunt-series peaking network is determined as

$$\begin{aligned} H_2(s) &= \frac{V_o}{I_{in}} = \frac{sL_a + R}{s^2C(L_a + L_b) + sCR + 1} \\ &= \frac{1}{C(L_a + L_b)} \cdot \frac{L_a(s + R/L_a)}{s^2 + sR/(L_a + L_b) + 1/C(L_a + L_b)}. \end{aligned} \quad (\text{Eq. 4.3})$$

where from denominator, the complex poles are

$$s_{1,2} = \frac{-R}{2(L_a + L_b)} \pm j \sqrt{\frac{1}{(L_a + L_b)C} - \left(\frac{R}{2(L_a + L_b)}\right)^2}. \quad (\text{Eq. 4.4})$$

The inductor  $L_a$  in series with  $R$  adds a real zero  $-R/L_a$  to the numerator of the transfer function in (Eq. 4.3). The addition of a zero improves the bandwidth but also peaks the response. To reduce the peaking issue in the frequency response of Fig. 4.2(e), the components values are equated to the standard  $2^{nd}$ -order polynomial normalized Butterworth system. For this reason, let us normalize the transfer function  $H_2(s)$  by putting  $R = 1$  and  $C = 1$  and then

$$L_a = m_1 R^2 C L_b = m_2 R^2 C, \quad m_2 < m_1 \quad (\text{Eq. 4.5})$$

where  $L_a$  and  $L_b$  are selected to get the maximum gain flatness. Note that in this work we are trying to keep an agreement between the bandwidth and the gain flatness.

Combining the circuits in Fig. 4.2(a) and Fig. 4.2(d), a series-shunt-series circuit which involves a T-coil network ( $L_{a-c}$ ) is resulted in Fig. 4.2(f). The parasitic capacitors  $C_1$  and  $C_2$  are separated by the T-coil network ( $L_{a-c}$ ). The transfer function of this circuit is the product of the transfer function in (Eq. 4.1) and (Eq. 4.3). For simplicity of the analysis,  $R_b$  is neglected (as  $R_b \gg R_a$ ) and two valid cases are assumed. The first case is when the input impedance  $Z_i = R_a$ , and the second case is when  $Z_i = R_a + jb$ . For the first case it can be seen intuitively that at low frequencies the inductors short the input to  $R_a$  while the capacitors are open. For higher frequencies  $Z_i$  contains the imaginary part  $jb$  due to the existence of the passive components. So the transfer function for the case 1 and 2 are consecutively as follow

case1:

$$H_1(s) = \frac{R_a/m_1 R_a^2 C_1^2}{s^2 + s/m_1 R_a C_1 + 1/m_1 R_a^2 C_1} \times \frac{m_1 (s + 1/m_1 R_a C_1)/C_2 (m_1 + m_2)}{s^2 + s/R_a C_2 (m_1 + m_2) + 1/R_a^2 C_2^2 (m_1 + m_2)}. \quad (\text{Eq. 4.6})$$

case2:

$$H'_1(s) = \frac{(R_a + jb)/m_1 (R_a + jb)^2 C_1^2}{s^2 + (s + 1/C_2 (R_a + jb))/(R_a + jb) (m_1 + m_2)} \times \frac{m_1 (s + 1/m_1 R_a C_1)/C_2 (m_1 + m_2)}{s^2 + (s + 1/C_2 (R_a + jb))/C_2 (R_a + jb) (m_1 + m_2)}. \quad (\text{Eq. 4.7})$$

The denominator of (Eq. 4.6), includes four poles given by

$$s_{1,2} = \frac{1}{2R_a C_1 m_1} (-1 \pm j\sqrt{4m_1 - 1}). \quad (\text{Eq. 4.8})$$

and

$$s_{3,4} = \frac{1}{2R_a C_2 (m_1 + m_2)} (-1 \pm j\sqrt{4(m_1 + m_2) - 1}). \quad (\text{Eq. 4.9})$$

In (Eq. 4.6), two left hand complex poles extend the bandwidth much further compared to the poles in (Eq. 4.3), because the circuit in Fig. 4.2(f) represents more than one resonance mode. Assuming  $C_2 > C_1$  so poles  $s_{1,2}$  are located at higher frequency than poles  $s_{3,4}$ . Fig. 4.2(g) illustrates the frequency response improvement of the circuit in Fig. 4.2(f). If we replace  $R_a$  in (Eq. 4.8) and (Eq. 4.9) by  $R_a + jb$ , the poles of (Eq. 4.7) are obtained. A similar circuit to Fig. 4.2(f) is presented in [2] which the transfer function of the circuit is normalized to find the relation between the components for maximum bandwidth. The circuit shown in Fig. 4.2(f) is analyzed based on the simple inductors without having any mutual coupling. In our analysis of the Fig. 4.2(f), 3 inductors are used while  $L_b$  is modeled as the mutual coupling between the inductors  $L_a$  and  $L_c$ . The series-shunt-series network can be isolated as long as the mutual coupling is modeled properly as an inductor. Since the mutual coupling is modeled as an inductor, the circuit can be further simplified. The final transfer function of Fig. 4.2(f) is a fourth-order equation. The transfer function of the circuit in Fig. 4.2(f) is plotted in MATLAB (Fig. 4.3) and compared with the simulation of the network in the Cadence simulator (Fig. 4.4) to prove the validity of the calculations. The similarity between these two plots

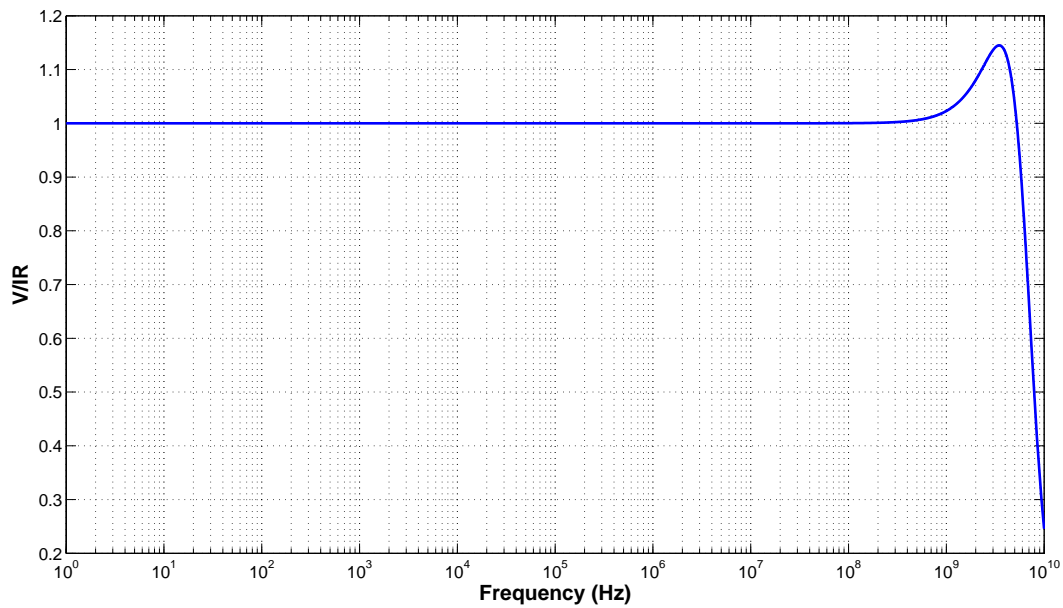


Figure 4.3: Transfer function of the equation (Eq. 4.6), plotted in MATLAB.

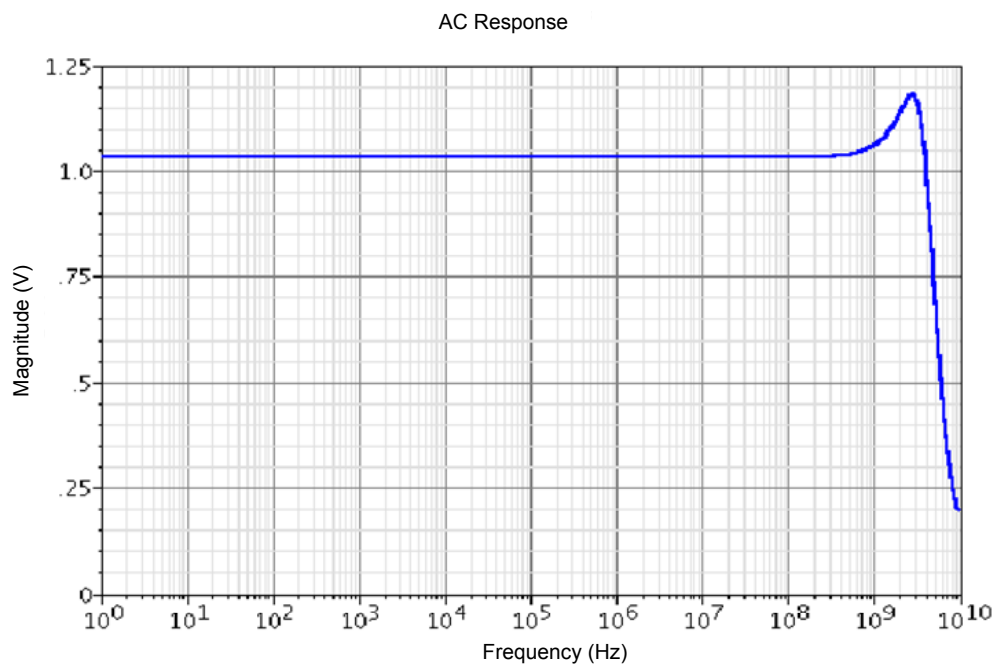


Figure 4.4: Transfer function of the peaking network (Figure 4.2(f)) using Cadence simulator.

confirms that the transfer function equation of 4.2(f) is correct. However, there are some discrepancies between graph of Fig. 4.3 and Fig. 4.4, which is due to the difference in

the modeling of the components in the MATLAB and Cadence simulator. The transfer function in Fig. 4.3 is normalized to  $50 \Omega$ , which is used to present the  $50 \Omega$  source.

## 4.2 Wideband Amplifier Design

In this section the series-shunt-series circuit in Fig. 4.2(f) is applied to a common-source amplifier to realize a wideband LNA design.

### 4.2.1 Output Peaking Network

The use of 3 inductors in Fig. 4.2(f) leads to difficulties in the layout. Fortunately, this issue can be resolved through implementation of a center-tap (CT) inductor. The circuit shown in Fig. 4.5(a) is a common-source amplifier incorporating the CT inductor with a magnetic coupling coefficient  $k$  between  $L_1$  and  $L_2$  to form the T-coil peaking network at the output network. The basic functionality of this T-coil network is similar to the circuit in Fig. 4.2(f) that was explained above. The CT inductor is employed to save die area and reduce the loss associated with the inductors. The CT inductor with the negative mutual coupling ( $-M$ ) leads to greater improvements compare to the circuit in Fig. 4.2(f).

In comparison with 3 separate inductors, the CT inductor in Fig. 4.5(a) introduces less parasitic components to the circuit. The equivalent small-signal model of the output peaking network is shown in Fig. 4.5(b). Since  $C_2 > C_1$  we assume that  $C_2 = (1 + \alpha)C/2$  and  $C_1 = (1 - \alpha)C/2$ , where  $0 < \alpha < 1$ . The CT inductor in this network has a symmetrical structure, hence  $L_1 = L_2 = L$ ,  $k = M/L$  and from here  $L_X = L_Y = L(k + 1)$  and  $L_Z = -kL$ . The mutual coupling between  $L_1$  and  $L_2$  as an extra term can be exploited to modify the bandwidth extension. For an on-chip CT inductor/transformer the  $k$ -factor is dependent to the number of layers and the stray of the capacitors between layer to layer. The  $k$ -factor is extracted from the inductor model given by the foundry.

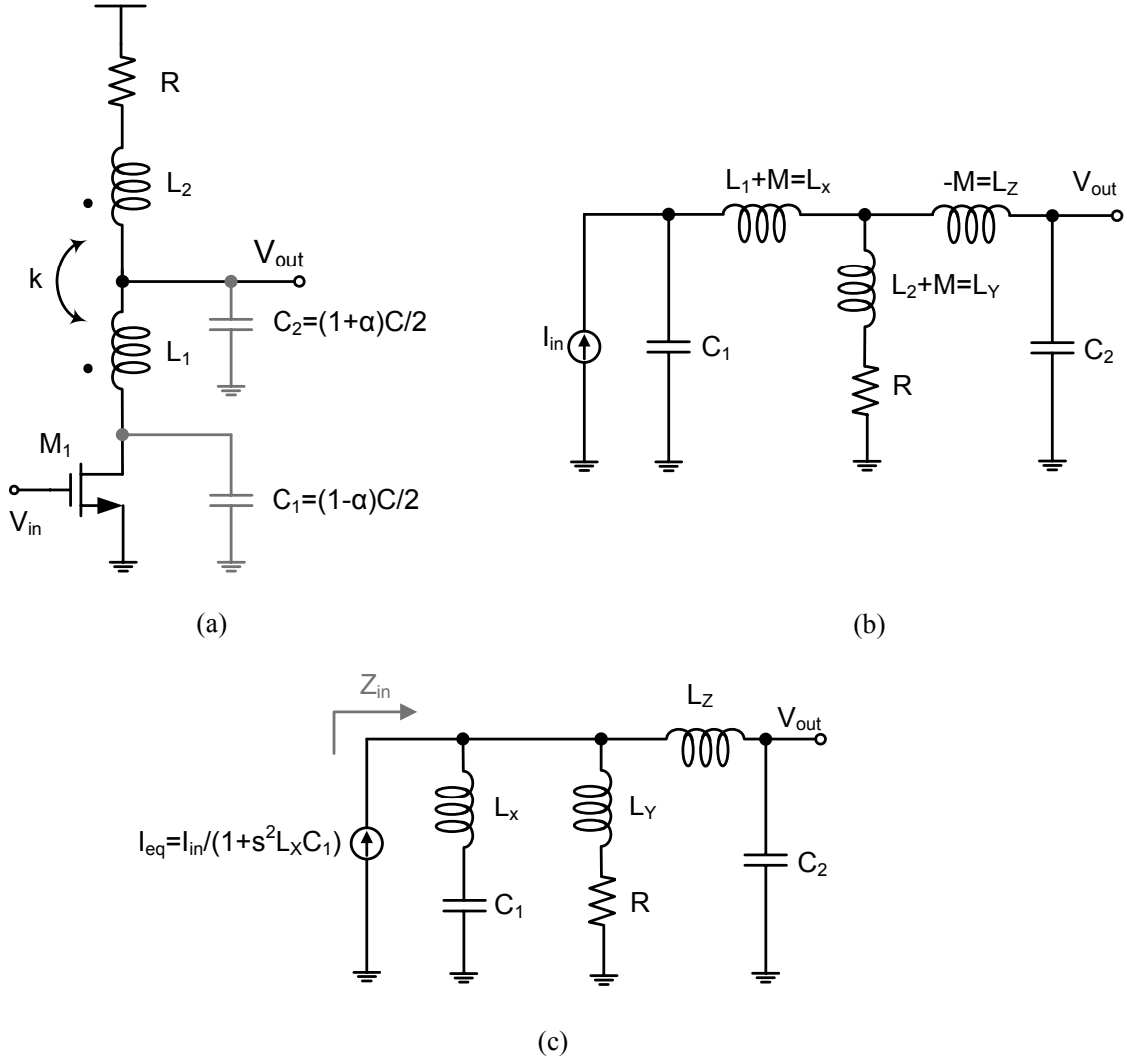


Figure 4.5: (a) Common-source amplifier with symmetric T-coil peaking network, (b) and (c) simplified small-signal equivalent circuit of the T-coil peaking.

The  $k$ -factor and mutual coupling inductance can be extracted from the impedance and admittance parameters:

$$M = \sqrt{(Y_{11}^{-1} - Z_{11}) \frac{Z_{22}}{\omega^2}}. \quad (\text{Eq. 4.10})$$

$$k(L_1, L_2) = \sqrt{\frac{(Y_{11}^{-1} - Z_{11}) Z_{22}}{\text{Im}(Z_{11}) \text{Im}(Z_{22})}}. \quad (\text{Eq. 4.11})$$

where  $\omega$  represents the resonance frequency of the CT inductor/transformer. In order to

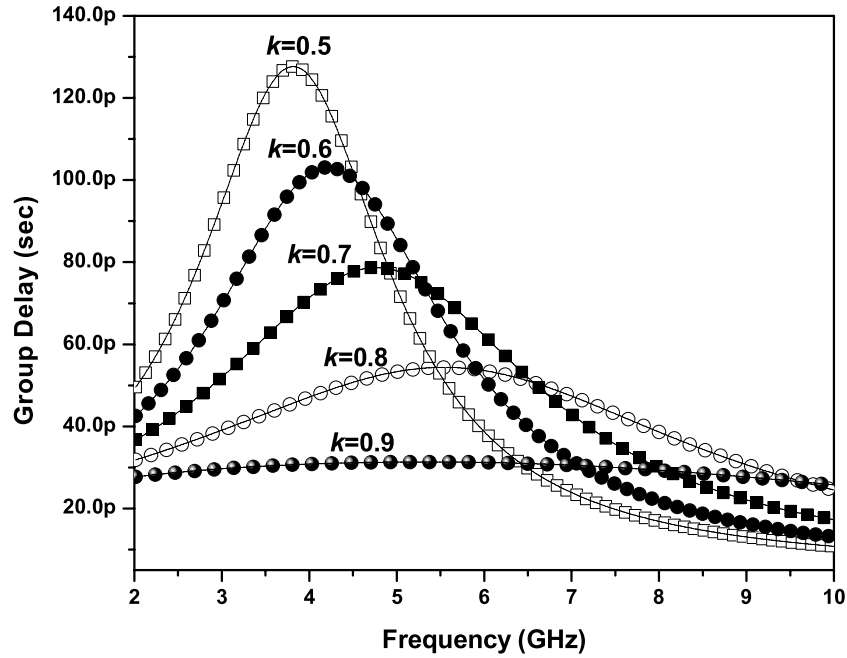


Figure 4.6: Group delay response of the T-coil network.

optimize the required gain-flatness over the entire bandwidth,  $k$ -factor should be determined precisely. For this reason, the relationship between group-delay and the  $k$ -factor of the T-coil network (Fig. 4.5(a)) is simulated in Fig. 4.6. Group-delay is a measure of the slope of the transmission phase response. The variations in group delay cause signal distortion, just as deviations from linear phase cause distortion. In this simulation the loss of the inductors are included into the circuit model to get more accurate results. As the  $k$ -factor increases, flatter group delay over wider bandwidth is resulted. In addition, the total attenuation of the symmetric T-coil network at different frequencies versus  $k$ -factor is plotted in Fig. 4.7. In practice, all symmetric T-coil networks have loss due to finite conductivity and/or lossy dielectric, which attenuates the signal. In order to calculate the loss or attenuation of the inductive network the parameters  $L$ ,  $C$ ,  $R$ , and  $G$  should be known. As the frequency increases, the attenuation of the T-coil network increases simultaneously. Therefore, a higher  $k$ -factor is required to reduce the attenuation especially at high frequencies. However, the design of a high  $k$ -factor CT inductor is not easy.

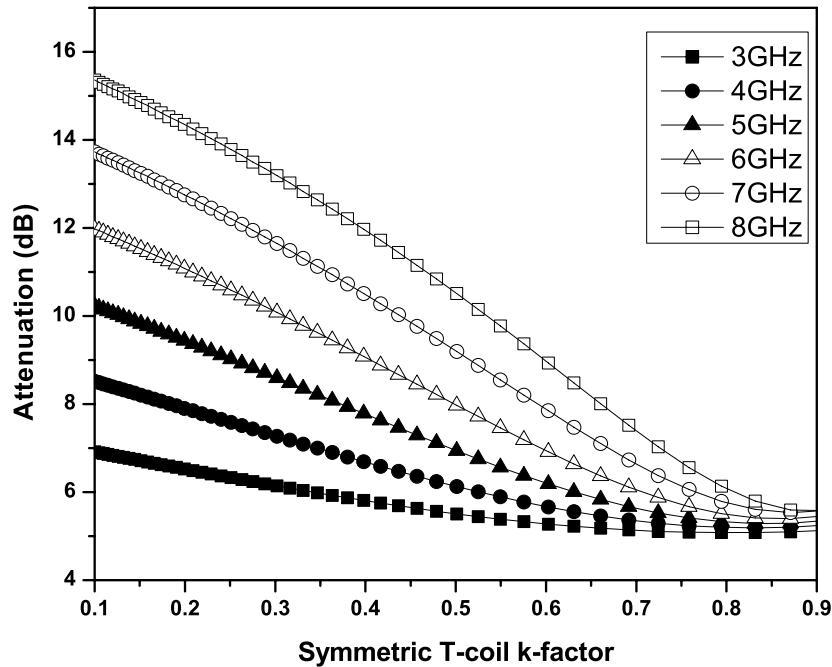


Figure 4.7: Amplitude response of the T-coil network vs.  $k$ -factor at different frequencies.

The reason is that the  $k$ -factor is limited by the parasitic capacitances and resistances of the inductor. To eliminate the nonideal characteristic of the inductor, stacked top metal layers are implemented while the center-to-center distance of the turn-to-turn winding should be reduced [34]. More importantly, if the parasitic capacitances of the output CT inductor become significant, more parasitic capacitances are added to  $C_1$ , which makes  $C_1$  comparable with  $C_2$ . This reduces the desirable bandwidth and makes the bandwidth extension technique inefficient. It is shown in the subsequent section that by increasing  $C_2/C_1$  ratio the bandwidth is further improved. Fig. 4.8 plots the attenuation of the output T-coil network versus frequency for  $k=0.5$  and  $0.9$ , respectively. The attenuation is more gradual for  $k=0.9$  and its deviation from 3 to 8 GHz is about 1.8 dB, which is flatter compared to the attenuation of  $k=0.5$ . Now, in order to prove the feasibility of the technique explained above, the T-coil peaking network is implemented in a cascode amplifier. Fig. 4.9 shows the complete single-ended cascode LNA with the CT inductor

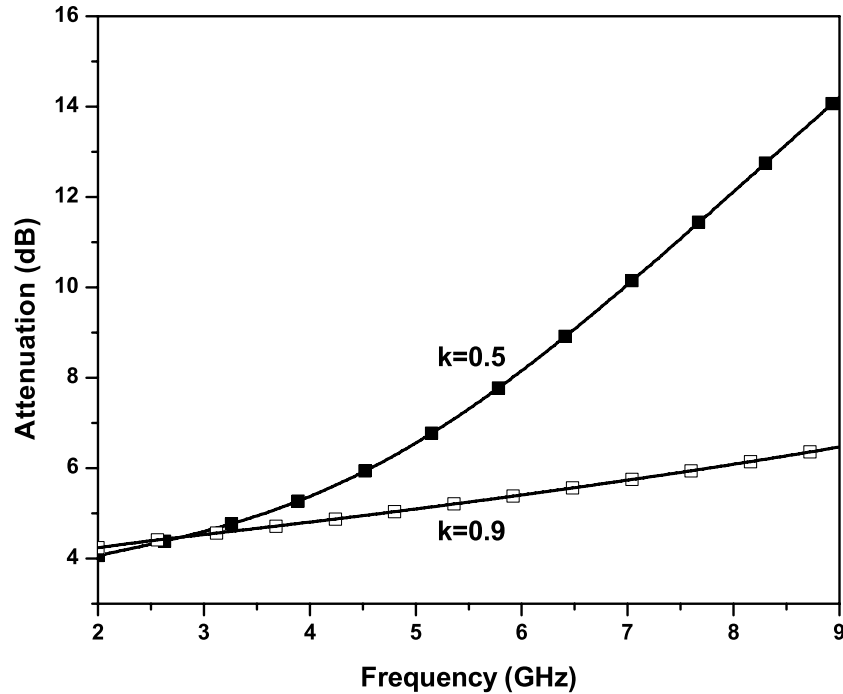


Figure 4.8: Amplitude response of the T-coil network vs. frequency.

at the input and the output of this circuit. An extra peaking inductor  $L_L$  is added into the output peaking network as a part of the load to prevent the gain roll-off and to improve the gain-flatness. A resistor  $R$  at the output load in series with  $L_L$  reduces the quality factor of this inductor, which extends the bandwidth of the LNA. However, the existence of  $R$  causes some drawbacks like peaking in the gain response and additional noise. In order to reduce the peaking in the gain response, a resistive-feedback path is connected across nodes “A” and “B”. In Fig. 4.10 the frequency response of the wide-band LNA with/without the feedback path is simulated. Clearly, the peaking issues are minimized due to the feedback path effect. That is,  $R_F$  moves the complex conjugate poles away from  $j\omega$  axis to get  $\varphi = 45^\circ$ . Therefore, proper selection of  $R_F$  value is critical to minimize the peaking in the frequency response. If the series parasitic resistance of the output inductors are high enough (low  $Q$  inductors),  $R$  can be removed from the output peaking circuit.

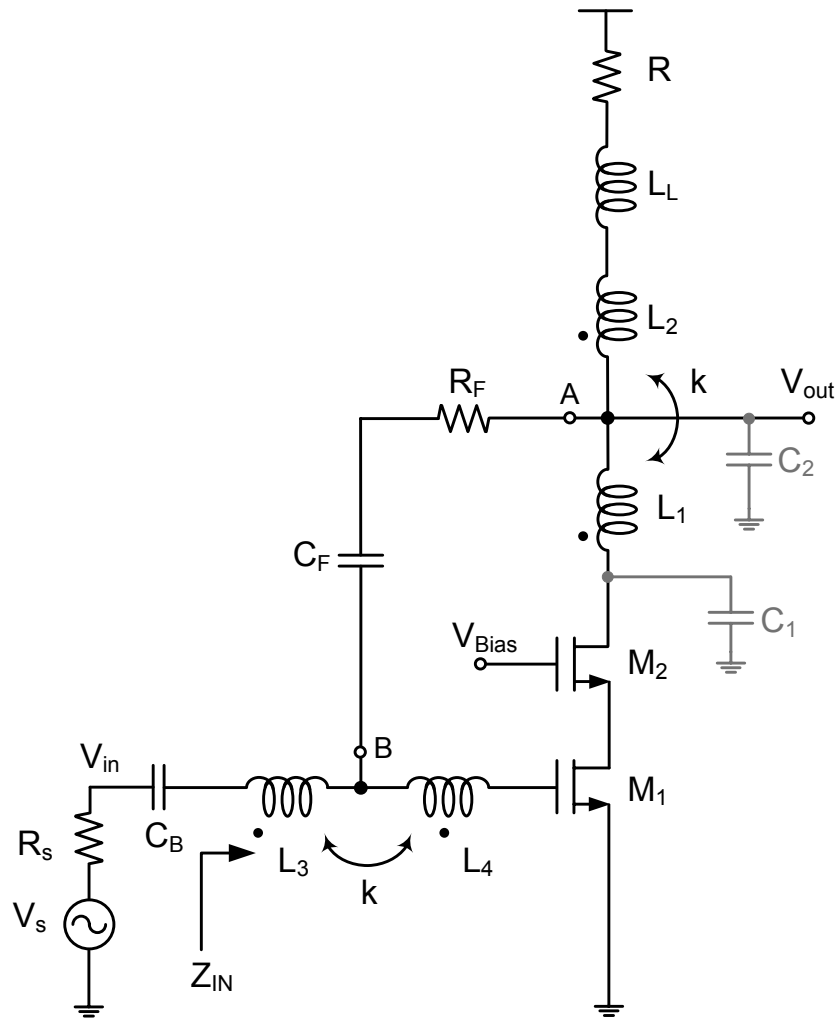


Figure 4.9: Wideband LNA using symmetrical center-tap inductor (biasing circuitry not shown).

### 4.2.2 Input Matching Network

Perhaps the most important reason for matching is to maximize the power transfer from a source to a load. In this part we would like to show how inductors and capacitors elements are used at impedance matching. Shown in Fig. 4.11 is the equivalent circuit model of the LNA input matching network. The input matching network is implemented using T-coil network, similar to the output peaking network. This technique helps to minimize the number of inductors at the input stage. The input impedance of this

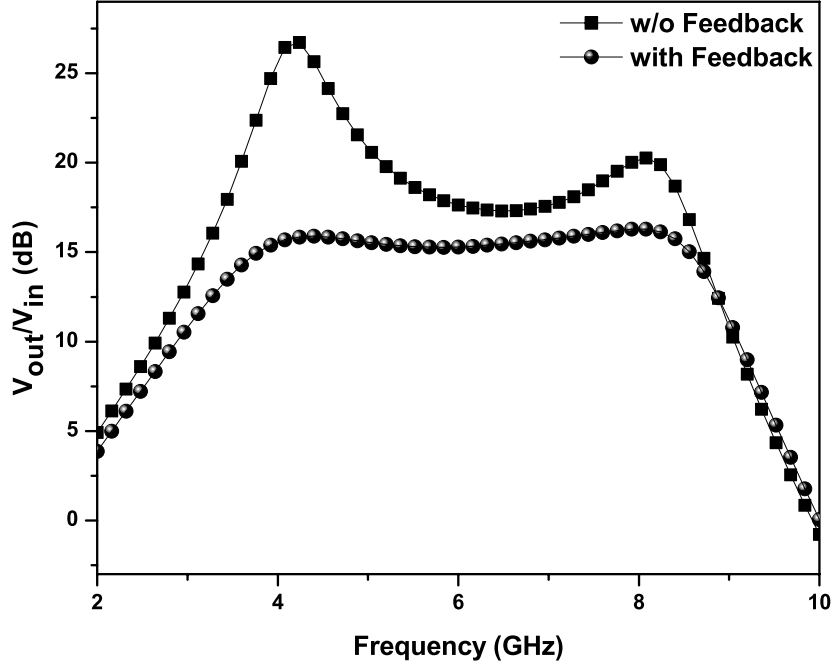


Figure 4.10: Simulated frequency response of the LNA, in here  $R = 0$ . The wideband LNA with/without feedback path is simulated for comparison, the 3 dB bandwidth is adjusted later.

circuit is expressed as

$$Z_{IN} = (sL_X + r_X) + \left[ sL_Z + \left( \frac{R_F}{1 - A_v} \right) \right] \parallel \left[ sL_Y + r_Y + \frac{1}{s(C_{gs} + C_\mu)} \right]. \quad (\text{Eq. 4.12})$$

where  $A_v$  is the open loop voltage of the amplifier,  $r_X$ ,  $r_Y$  are the loss associated with  $L_X$ ,  $L_Y$ , respectively and  $C_\mu$  is the Miller capacitor. The real part of (Eq. 4.12) is defined as  $R_s = \Re(Z_{IN})$  where  $\Re(Z_{IN})$  is directly dependent to  $R_F$ . Regardless of the loss associated with the inductors, the input resistance of the LNA is approximated by  $R_{in} = R_F / (1 - A_v)$ , which introduces a low input impedance and reduces the effect of input dominant pole

$$s_{in} = \frac{1}{R_{in}(C_B + C_{gs} + C_\mu)} = \frac{|A_v|}{R_F(C_B + C_{gs} + C_\mu)}. \quad (\text{Eq. 4.13})$$

where  $R_{in} \approx R_F / |A_v|$  if  $A_v \gg 1$ . The input matching network is implemented as bandpass filter. The tuning condition of the filter is dependent to the proper value of the components. For instance, the right selection of the blocking capacitor  $C_B$  is very

important because a large value of  $C_B$  adds to the overall parasitic capacitance at the input, affecting the overall bandwidth of the circuit. A small value on the other hand, has significant AC impedance that leads to the gain reduction.

The quality factor ( $Q$ ) of the input network is given by

$$Q_T = \frac{1/\omega_0 ((C_{gs} + C_\mu) || C_B)}{\left[ R_s + r_X + r_Y + \frac{\omega_0^2 (L(k+1))^2}{R_P} \right]}. \quad (\text{Eq. 4.14})$$

where resistor  $R_P = (R_F / (1 - A_v)) (1 + Q_{L_Z}^2)$  is the parallel equivalent resistance of the inductor  $L_Z$ , and  $\omega_0$  corresponds to the resonance frequency of the network as

$$\omega_0 = \frac{1}{\sqrt{((C_{gs} + C_\mu) || C_B) [L_X + (L_{Z'} || L_Y)]}}. \quad (\text{Eq. 4.15})$$

As  $k$ -factor of the input CT inductor increases, the attenuation reduces and the input network bandwidth increases. By tuning  $R_P$  in (Eq. 4.14),  $Q_T$  of the input network would be tuned and the desired input matching can be obtained. Note that the tradeoff between the input matching and the noise figure should be considered when the value of  $k$ -factor is selected. From (Eq. 4.15), it can be seen that the parasitic  $C_{gs} + C_\mu$  can be tuned out with proper selection of the components values.

### 4.2.3 Noise Analysis

There are many factors which may directly affect the NF of the proposed LNA design. The input impedance matching network, feedback resistor, biasing circuitry and drain current noise of the MOS device  $M_1$ , are the major contributors. In saturation, the drain current noise is mainly due to the drain current and is weakly dependent to drain voltage [35]. The output load resistance and the output buffer, which generally assumed to have insignificant noise contribution, also add to the NF. The parasitic components of the input CT inductor, which reduce  $Q_T$  of the matching network and channel length effect of the transistor  $M_1$  are inevitable issues. Therefore, careful design strategies are needed

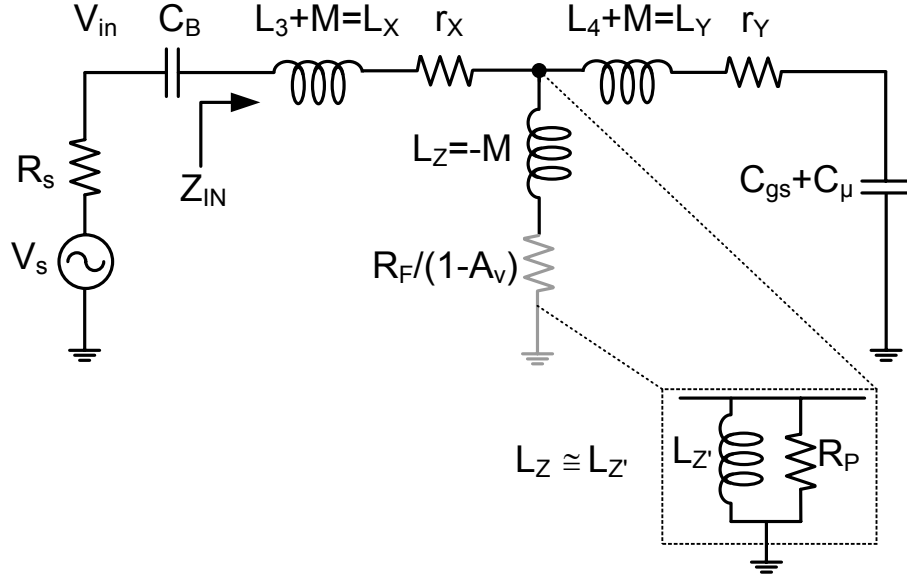


Figure 4.11: Input impedance equivalent network of the LNA.

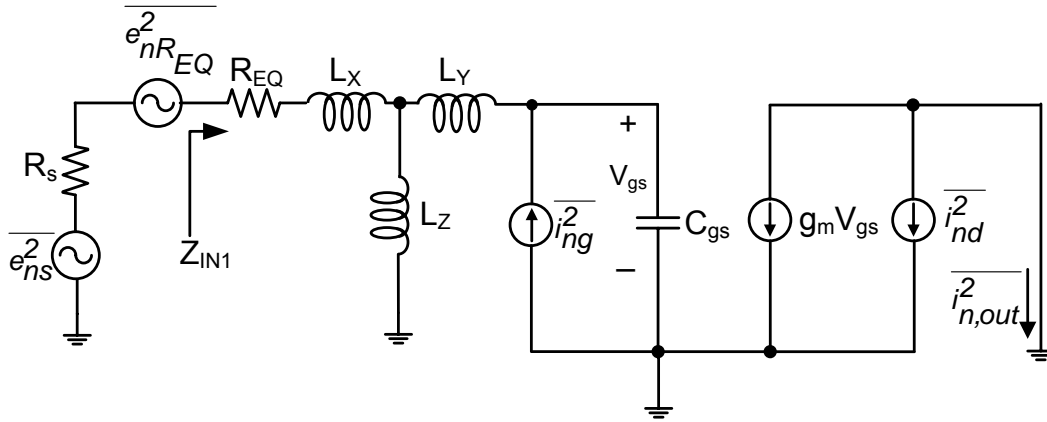


Figure 4.12: Simplified small-signal model of Fig. 4.5(a), noise contribution of  $M_2$  is ignored.

to overcome these issues. Since the noise contribution of the cascode transistor  $M_2$  is negligible, its noise effect is neglected [36].

The equivalent small signal noise model of the wideband LNA is shown in Fig. 4.12. Since the mutual coupling  $M$  between two halves of the inductors is noiseless, the effect of  $L_Z = -M$  is neglected in the NF calculations. By solving the small-signal model for  $Z_{IN1} = R_s$  at resonance and following the noise calculation method explained in [26], we

get

$$F = \frac{R}{R_s} \left( 1 + \frac{R}{R_s} \frac{\omega_0^2 R_s g_m \gamma}{\omega_{T_0}^2 \alpha} \chi \right). \quad (\text{Eq. 4.16})$$

where,

$$\chi = \frac{\delta \alpha^2}{5\gamma} [1 + Q_T^2] + 1 - 2|c| \sqrt{\frac{\delta \alpha^2}{5\gamma}}. \quad (\text{Eq. 4.17})$$

$$R = R_s + R_{EQ}, \quad \alpha = \frac{g_m}{g_{d0}}, \quad \omega_{T_0} = \frac{g_m}{C_{gs} + C_\mu}. \quad (\text{Eq. 4.18})$$

$$R_{EQ} = R_g + r_X + r_Y + \frac{(L_X \omega_0)^2}{R_F / 1 - A_v}. \quad (\text{Eq. 4.19})$$

where  $\delta \approx 1.33 - 4$ ,  $\gamma \approx 0.67 - 1.33$  are excess noise parameters,  $c \approx j0.4$  [36], and  $g_{d0}$  is the channel conductance at  $V_{DS} = 0$ . For the noise analysis, parasitic resistances of  $L_X$ ,  $L_Y$ , and gate resistance of the transistor  $M_1$  are lumped into  $R_{EQ}$ . In order to determine the NF contribution due to  $R_F$ , the open loop gain  $A_v$  is assumed to be consistent across the bandwidth. As discussed above, it is known that by tuning  $R_P$ , the  $Q_T$  of the input matching network can be tuned. From Eq. 4.17 and Eq. 4.16 it is clear that  $Q_T$  is directly related to the noise figure. It is concluded that by tuning the  $R_F$  resistor, which is directly related to the  $R_P$ , both noise figure and input matching network can be tuned, respectively. Therefore, by optimizing the input matching network the required noise figure is achievable. An increase in  $R_F$  reduces noise linearly. However, an increase in  $R_F$  pushes the input dominant pole in (Eq. 4.13) to a lower frequency. The NF can be lowered by choosing the right value of  $R_F$ , which alters  $Q_T$  in (Eq. 4.17). Given in (Eq. 4.18),  $\omega_{T_0}$  increases as the transconductance increases and consequently improves the NF. Any extra physical input resistance  $r_g$  adds an additional term of  $r_g/R_s$  to (Eq. 4.16). Since only one CT inductor is employed at the input of the LNA, less loss is contributed to the NF.

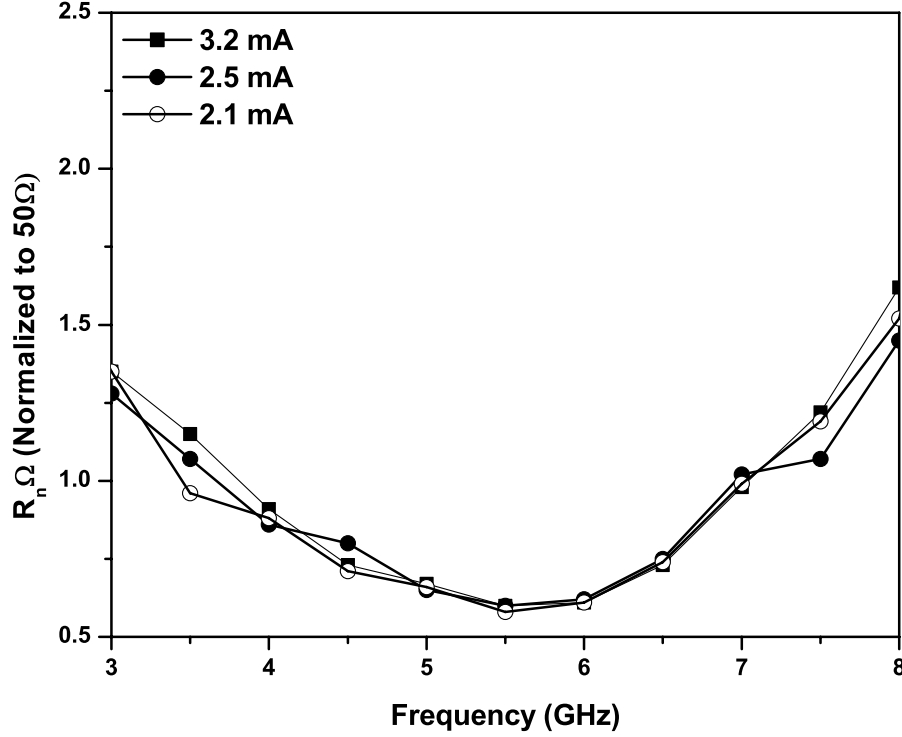


Figure 4.13: Variations of normalized  $R_n$  with three different currents vs. frequency.

#### 4.2.4 Design Sensitivity to Process Variations

Due to the frequency and process dependency of the components, variations in the design specifications are expected. In this part susceptibility of the LNA to these variations and its effect on the performances is briefly evaluated. For instance, mismatch between the components in the input matching network, frequency dependency of the components, modeling inaccuracy and manufacturing variations as technology scales, are the important parameters which increases the design sensitivity. In this wideband LNA, the gain, NF, and linearity specifications are constrained to be met with minimum power consumption. A key parameter that degrades the NF of the amplifier is the noise resistance  $R_n$  [37];

$$R_n = R_g + \frac{i_{dn}^2}{4kT} \left| \frac{1 + s(c_{gd} + c_{gs})R_g}{g_m - sC_{gd}} \right|^2 \quad (\text{Eq. 4.20})$$

where  $i_{dn}^2$  and  $R_g$  are the channel thermal noise and the gate resistance, respectively. Clearly, by reducing  $R_n$  the NF improves to some extent. In Fig. 4.13, the variation of the measured  $R_n$  versus frequency is plotted. The bias current is kept at less than 3.5 mA. Since the width ( $W$ ) of the device is inversely proportional to  $R_n$  [37], proper selection of  $W$  results in an optimum value of  $R_n$  that reduces the variation of the noise figure ( $\Delta NF$ ). However, the device size cannot be made arbitrarily larger to make  $R_n$  smaller because the parasitic  $C_{gs}$  increases as  $W$  increases. As shown, the variation of normalized  $R_n$  in this design is less than  $0.8 \Omega$  over a wide range of frequency at three different DC currents. It is noted that the variations of  $R_n$  is almost constant over the wide range of frequency. As a conclusion, since the variations of  $R_n$  are the same for 3 different currents, we cannot improve the NF necessarily from this point of view in this design.

The mismatch between the components degrades the gain and high frequency performances of the LNA. The focus in here is mainly on the sensitivity of the gain and noise figure to the parameters variations. Basically, with a higher power gain, a better NF performance can be resulted. On the other hand, this LNA is designed to be used with a mixer, and high gain LNA reduces the linearity of the whole design (LNA+Mixer). Therefore, LNA should meet the tradeoff between all the design characteristics. To gain more insights, we would calculate the voltage gain of the LNA. To derive the voltage gain of the amplifier, notice that  $R$ ,  $L_L$ , which are in series with  $L_2$ , and the parasitic  $C_1$  are neglected and  $L_1 = L_2 = L$ . The overall gain of the LNA is

$$\frac{v_{out}}{v_s} = \frac{-g_m}{sC_{gs}(R_s + Z_{IN})} \cdot \frac{(R_F \parallel sL)}{s^2L_ZC_2 + sC_2(R_F \parallel sL) + 1}. \quad (\text{Eq. 4.21})$$

where  $v_s = i_s R_s - v_{in}$  and assuming  $i_{d1} \approx i_{d2}$ , then the output current  $i_{d1}$  is equal to  $v_s \cdot g_m / sC_{gs}(R_s + Z_{IN})$ . Equation (Eq. 4.21) shows that the gain rolls-off if  $C_{gs}$  is large.

The impact of  $C_{gs}$  is reduced with higher  $f_T$  or reduction of the mismatch between the input matching components to guarantee that  $C_{gs}$  is resonated out over the frequency of interest. Moreover, the output capacitor  $C_2$  causes reduction in the voltage gain. The reduction in the voltage gain would increase the NF. These parameters should be considered to keep the agreement between the gain and NF performances.

Fig. 4.14 is plotted to show the sensitivity of the NF to 20% devices variations at 3.2 mA current consumption. As shown in the solid line plot, the worst case in the NF degradation is when  $W$  of the transistor  $M_1$  and  $L_{3,4}$  are increased (20%) and an extra pad capacitor is added to the circuit. This plot shows that the NF has a better performance at the frequencies lower than 5.5 GHz compared to the case when no variation is applied. This difference is due to the higher current from the larger device size. It should be noted that the frequency at which the minimum sensitivity to process variations in NF is observed (about 5.75 GHz from Fig. 4.14), is very close to the frequency at which the minimum value of  $R_n$  occurs (5.5 GHz in Fig. 4.13). However, the NF degrades at frequencies higher than 5.8 GHz due to the reduction in the gain and  $Q$ -factor of the inductors. The deterioration of the noise figure at higher frequencies is partially due to the gate resistance noise and gate induced noise (both are  $\propto f^2$ ) [36].

### 4.3 Experimental Results

In order to examine the stability condition of the LNA, the stability simulation is carried out as shown in Fig. 4.15 and Fig. 4.16. As these simulations shows, both stability conditions  $\Delta < 1$  and  $K_f > 1$  are met for a wide range of frequency.

From the discussion above, a wideband LNA with the bandwidth of 3.168–7.920 GHz is designed for the multiband OFDM standard. The components values are listed in Table 4.1. The size of  $M_1$  is selected properly to get low current consumption. From simulation, this wideband LNA provides a maximum gain of 20 dB with maximum NF of 2.9 dB

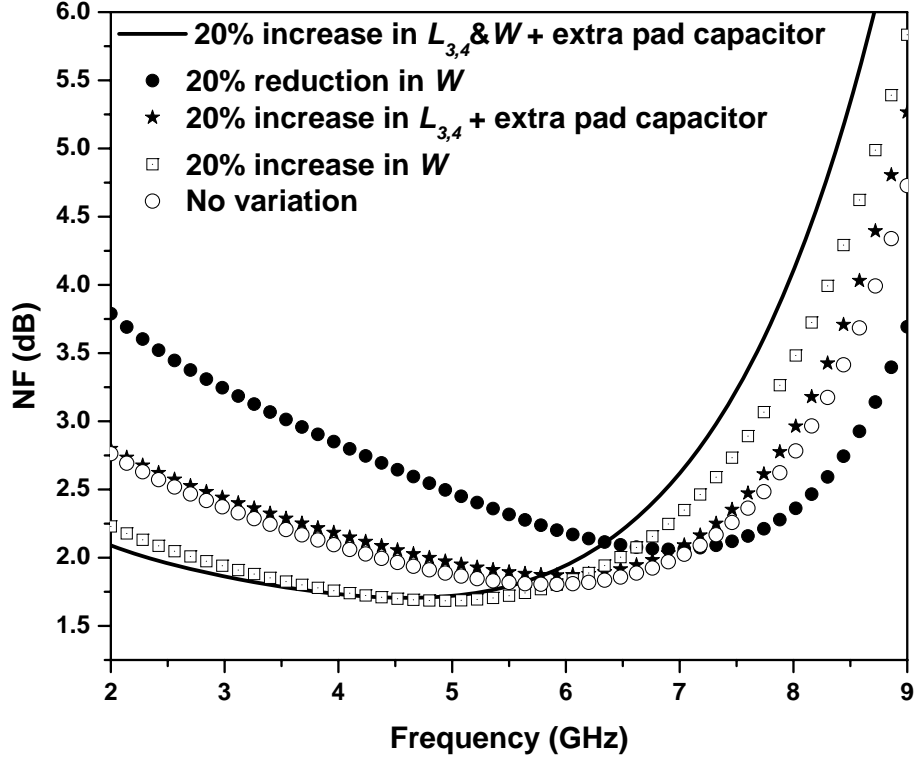


Figure 4.14: Device variations effect on the noise figure performance.

Table 4.1: Component Values of the LNA

$(W/L)_{M_1}$	$(W/L)_{M_2}$	$L_{1,2}^*$	$L_{3,4}^*$	$L_L$	$R_F$
120/0.18 $\mu\text{m}$	40/0.18 $\mu\text{m}$	9 nH	2.92 nH	1.31 nH	1.14 $k\Omega$

\*  $L_{1,2}$  and  $L_{3,4}$  are the center-tap inductor.

under 2.2 mA current consumption. Since the sum of series parasitic resistances of the output inductors  $L_L + L_{1,2}$  is high enough, which is about 55  $\Omega$  at 7 GHz,  $R$  in Fig. 4.9 was removed from the final design. This enables the transistors to have enough voltage headroom with the optimum device size which efficiently reduces the current consumption of the LNA. In addition, it improves the gain and the NF without extra current consumption.

By the size of the transistor  $M_1$ , the parasitic  $C_{gs}$  can be obtained. From the blocking capacitor  $C_B$  of 1 to 2 pF, the value of the input CT inductor is determined to get the

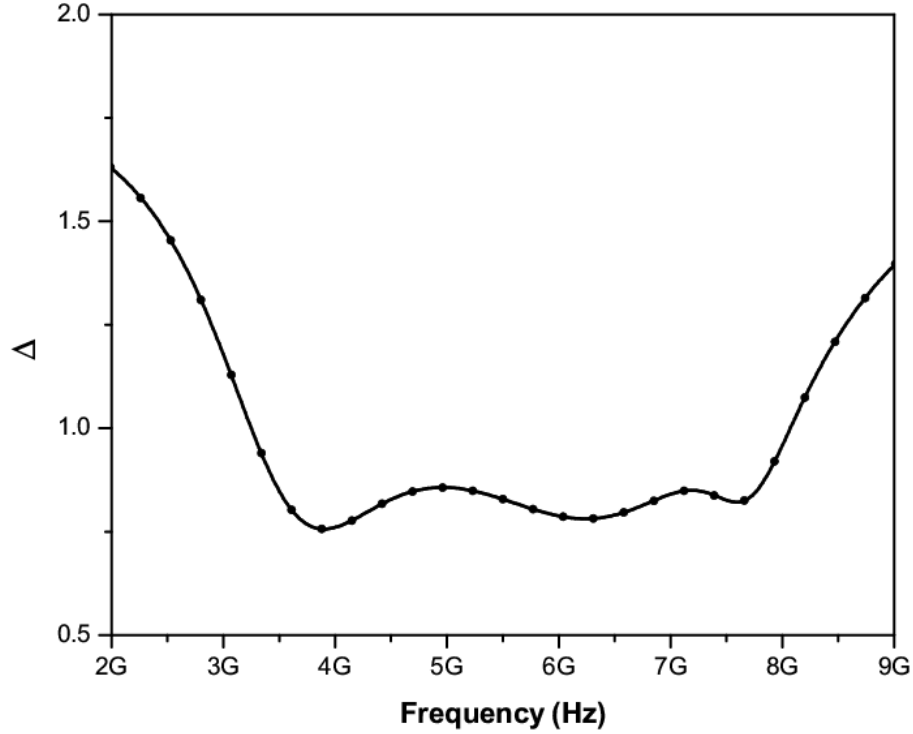


Figure 4.15: Simulation stability of the wideband LNA,  $\Delta$ .

desirable input matching. On the other hand, the size of  $M_2$  determines the parasitic capacitance  $C_1$  at the output network. The output response of Fig. 4.9 is simulated in Fig. 4.17 to show the different loading ( $C_2$ ) effects. As  $\alpha$  increases,  $C_1=(1-\alpha)C/2$  reduces and  $C_2=(1+\alpha)C/2$  increases. As shown in Fig. 4.17, with a reduction in  $C_1$  and an increase in  $C_2$ , the output T-coil network exhibits larger bandwidth with smaller peaking especially when  $C_2$  dominates ( $\alpha=0.9$ ). So the size of  $M_2$  is selected to be much smaller than the size of  $M_1$ , to decrease the parasitic  $C_1$  and to reduce the peaking in the response at high frequencies. Since this wideband LNA will be interfaced with a mixer in the UWB design, the input capacitance of the I/Q downconversion mixer should be taken into account as it determines the gain-flatness of the LNA. In this design, a current reuse buffer [38] is implemented to obtain  $50\ \Omega$  output matching for the measurement purposes. The loading effect of the buffer is determined to be about the same as the mixer

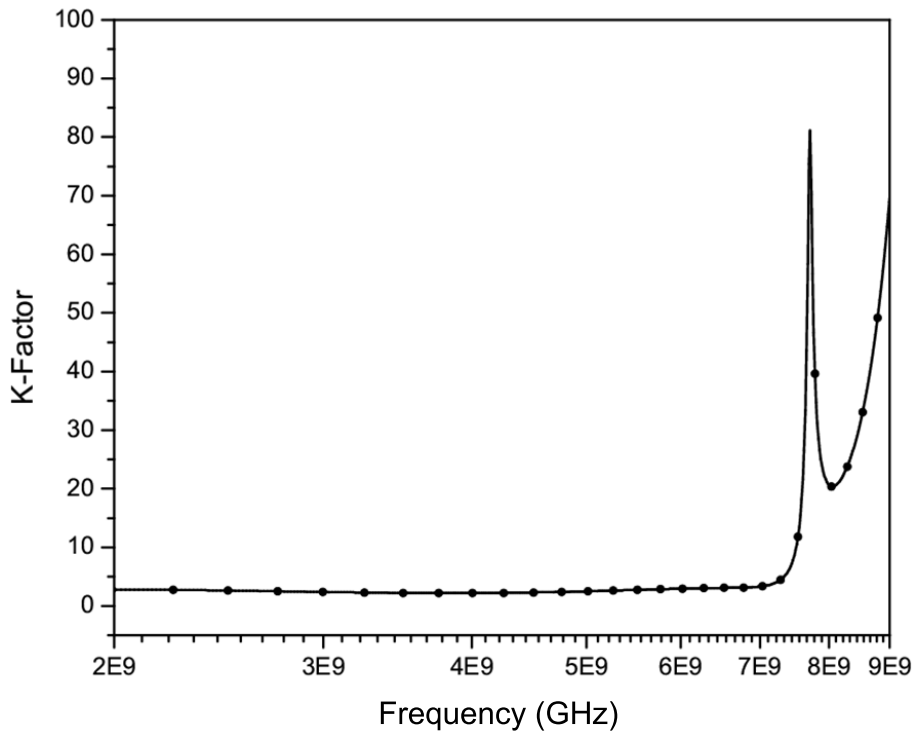


Figure 4.16: Simulation stability of the wideband LNA,  $K_f$ .

loading effect on the LNA stage. The prototype of the wideband LNA is fabricated in a six-metal 0.18  $\mu\text{m}$  CMOS technology. The die micrograph is shown in Fig. 4.18. The total die area including the output buffer is  $0.76 \times 0.81 \text{ mm}^2$ . The inductors are mounted on the pattern ground shield structure for better efficiency [39]. The empty spaces are covered with metal-filling to reduce the process variations effects. The transistors  $M_1$  and  $M_2$  are divided into six units to reduce the gate parasitic resistance. The simulated and measured results of the S-parameters are plotted in Fig. 4.19 and Fig. 4.20, respectively. The difference of the measured and simulated S11 could be due to process variations and pad capacitance. The measured gain has a maximum peak gain of 16.4 dB at 3.19 GHz frequency. The gain-flatness of 2.1 dB from 4 to 7.6 GHz frequency is obtained with 2.16 mA current consumption. The gain drops by 3.5 dB from the maximum peak gain at 7.6–8 GHz frequency. This drift can be corrected by adjusting the inductors in the subsequent silicon iteration. The measured input reflection coefficient is well below -

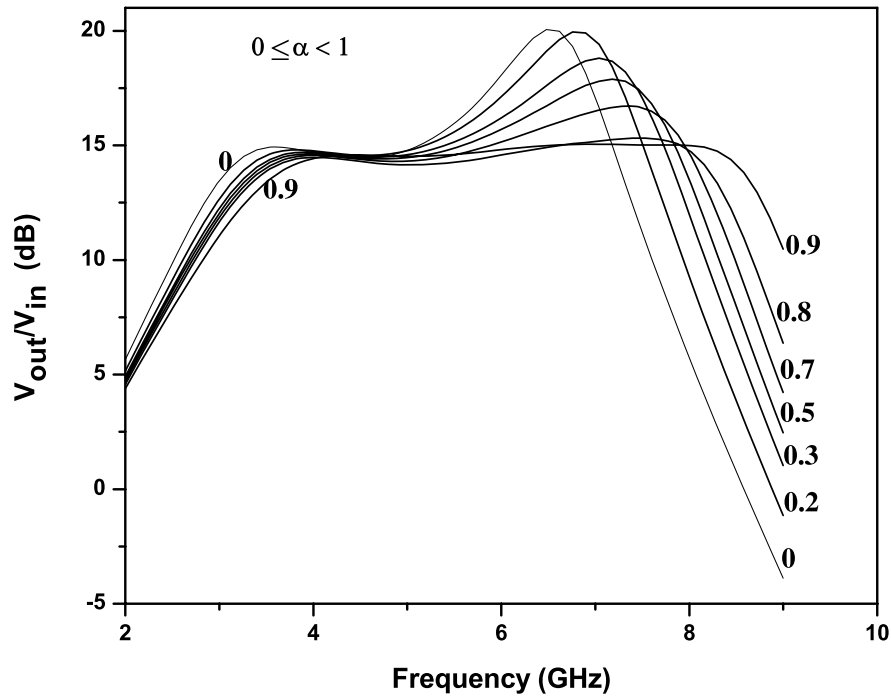


Figure 4.17: Contour plots of  $\alpha$  variation (variation of the next stage parasitic capacitance) and its effect on the gain peaking vs. frequency.

10 dB for the entire operating frequencies. As explained before, the output matching of the LNA is set by a current reuse buffer just for the test purposes. The comparison between the measured and simulated S22 and S12 is plotted in Fig. 4.20, respectively. The measured S22 is better than -10 dB from 3-6 GHz frequency. The measured S12 shows that there is a good isolation between output to the input of the LNA.

Two-tone test is used to simulate the IIP3 with 1 MHz frequency space between the tones. The third order input intercept point (IIP3) is simulated versus different frequencies. Fig. 4.21 plots an IIP3 of -9 dBm at 8 GHz frequency.

The simulated and measured NF over the bandwidth is shown in Fig. 4.22. Several dies were measured and mean value of the NF is plotted. The difference between the measured and simulated NF is owed to the process variations as explained before. A minimum NF of 2.7 dB is measured at 2.8 GHz and the NF at 3 GHz is 2.9 dB. The maximum NF is 4.66 dB at 7 GHz and it falls to 3.8 dB at 8 GHz frequency. From

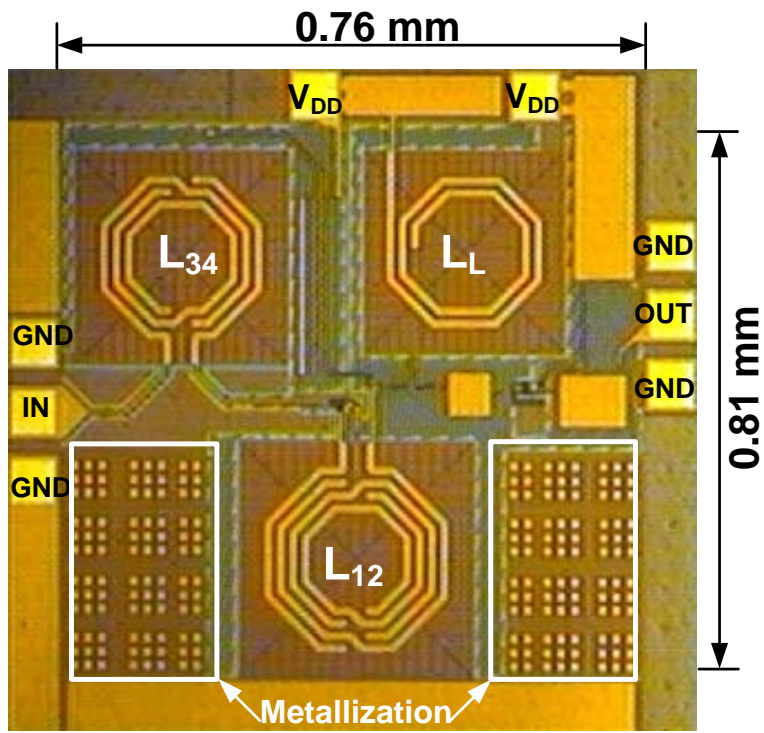


Figure 4.18: Die micrograph of the wideband LNA.

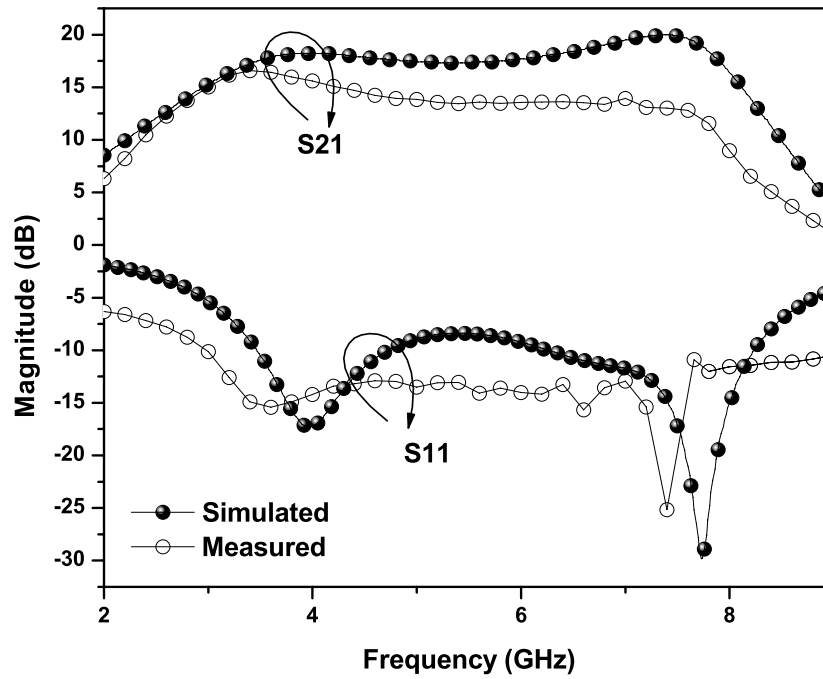


Figure 4.19: Gain and input reflection coefficient of the LNA vs. frequency.

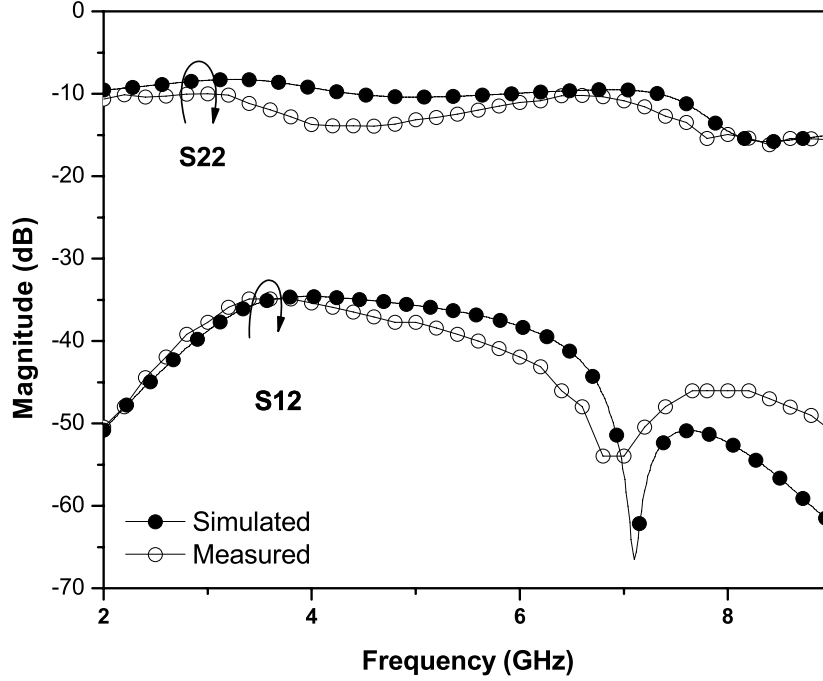


Figure 4.20: Measured and simulated S22 and S12 of the LNA vs. frequency.

another point of view, due to the on-chip parasitic components the quality factor of the inductors are reduced, which would reduce the noise figure performance proportionally. Fig. 4.23 depicts the measured quality factors of the input and the output inductors. The  $Q$ -factor of the input inductor effects the NF directly. The measured  $Q$ -factors are  $8 < Q_{L_L} < 11.8$ ,  $8.8 < Q_{L_{1,2}} < 10.7$ , and  $11.5 < Q_{L_{3,4}} < 13.9$  for 3–8 GHz frequency. A high  $Q$  inductor at the input is chosen for better NF, and lower  $Q$  inductors at the output were used for the gain-bandwidth trade-off. Table 4.2 indicates the performance comparisons of the proposed wideband LNA with prior works. A figure-of-merit ( $FOM$ ) is used here to compare the performance of different LNAs with similar functionality. The  $FOM$  in here evaluates the gain, -3 dB bandwidth, excess noise factor and power consumption of the LNA which is defined as [2]

$$FOM = \frac{|S_{21}| BW_{GHz}}{(F - 1) P_{mW}}. \quad (\text{Eq. 4.22})$$

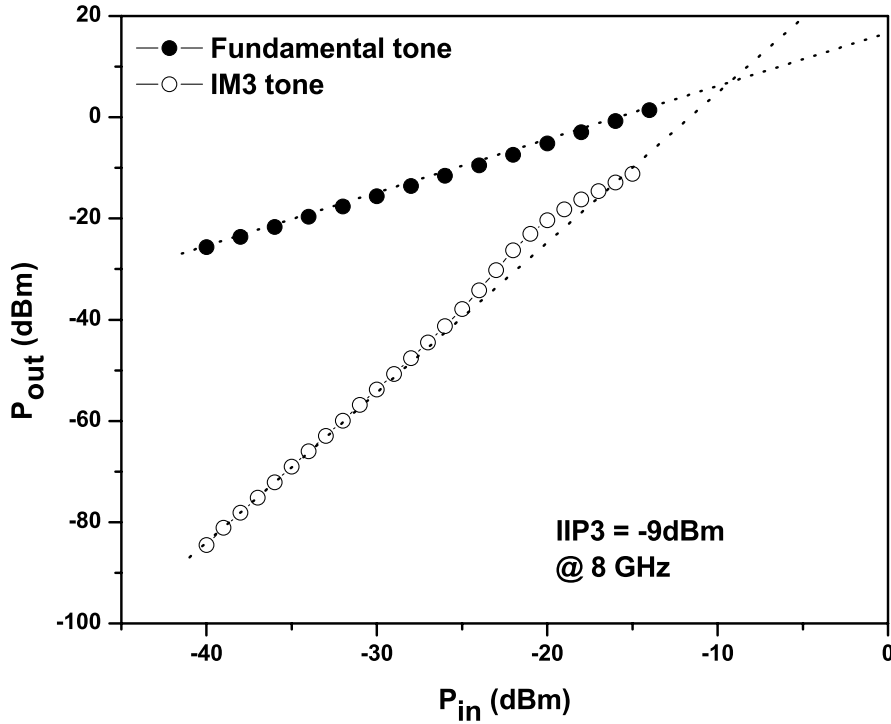


Figure 4.21: Simulated IIP3 at 8 GHz.

Based on the *FOM* calculated in Table. 4.2, the proposed wideband low-noise amplifier shows comparable performances to the other designs. In [48], the low power consumption at 1.2 V supply voltage and low noise figure performance are the reasons to have higher *FOM* compared to our proposed design.

As a summary, a technique to attain the wide bandwidth LNA is presented using 0.18  $\mu\text{m}$  CMOS technology. The introduced technique tunes-out the parasitic capacitances of the transistors over a wide bandwidth. The relations of the components in the standard form of the Butterworth filter are calculated to get the desired gain-flatness. The number of inductors are minimized to reduce the loss associated with them. Using this technique, a single stage wideband LNA is obtained with a low power consumption.

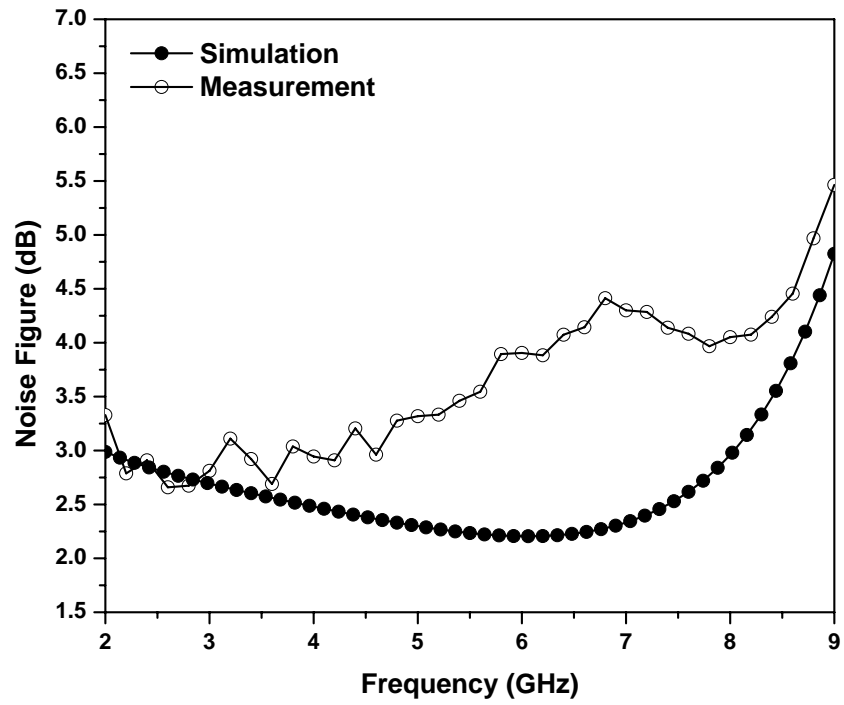


Figure 4.22: Simulated and measured noise figure of the wideband LNA.

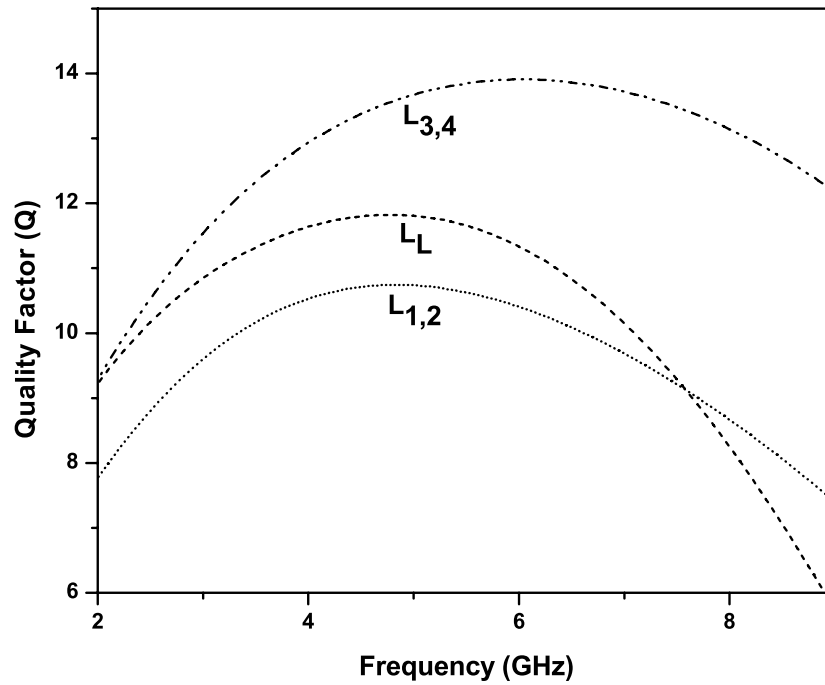


Figure 4.23: Measured quality factor of the inductors.

Table 4.2: Wideband LNA Performance Summary and Comparison

Reference	Technology	BW GHz	S11 dB	Gain <sub>max</sub> dB	NF dB	IIP3 dB	Power mW	Area mm <sup>2</sup>	FOM
<b>This Work</b>	0.18 $\mu$ m CMOS	<b>3–8</b>	<b>&lt;-10</b>	<b>16.4</b>	<b>2.9–4.66</b>	<b>-2.2</b> to <b>-9</b>	<b>3.9</b>	<b>0.62</b>	<b>4.4</b> to 8.9
[4] STD	0.18 $\mu$ m CMOS	2.3–9.2	<-9.9	9.3	4–8	-6.7 <sup>†</sup>	9	1.1	0.3 to 1.5
[4] TW	0.18 $\mu$ m CMOS	2.4–9.5	<-9.4	10.4	4.2–8	-8.8 <sup>†</sup>	9	1.1	0.49 to 1.6
[25]	0.18 $\mu$ m CMOS	3.1–10.6	<-11	9.7	4.5–5.1	-6.2	20	0.59	0.5 to 0.6
[2] LNA2	0.18 $\mu$ m CMOS	1.3–12.3	<-9	8.2	4.6–5.5	7.6-9.1	4.5	1	2.69 to 3.64
[40]	0.18 $\mu$ m SiGe	3–10	<-10	21	2.5–4.2	<-1 <sup>‡</sup>	30	1.8	1.6 to 3.4
[41]	0.18 $\mu$ m CMOS	0.4–10	<-10	12.4	4.4–6.5	-6	12	0.42	1 to 1.99
[42]	0.18 $\mu$ m CMOS	2.8–7.2	–	19.1	<3.8	-1 <sup>§</sup>	32	1.63	0.88
[43]	0.13 $\mu$ m CMOS	1.5–8.1	<-9	11.7	3.6–6	11.7 to 14.1	2.62 @1.3V	0.58	3.25 to 7.5
[44]	0.18 $\mu$ m SiGe/CMOS	0.1–11	<-12	8	2.9	-3.55	21.6	0.76	1.3
[45]	65 nm CMOS	0.2–5.2	–	15.6	<3.5	>0	14 @1.2V	0.009	1.7
[46]	0.18 $\mu$ m CMOS	0.048–1.2	-9	14 <sup>×</sup>	3 <sup>◇</sup>	3 <sup>◇</sup>	15.8 @2.2V	0.37	1.84
[47]	0.13 $\mu$ m CMOS	0.8–2.1	-8.5	14.5	2.6	+16	17.4 @1.5V	0.0992	0.48
[48]	0.13 $\mu$ m CMOS	3.1–10.6	<-9.9	16.5	2.07–2.93	-5.1 – -8.5 <sup>◇</sup>	9 @1.2V	0.87	5.78 to 9.1

\* at 3–8 GHz. <sup>†</sup> at 6 GHz. <sup>‡</sup> at 5.4 GHz, 5.6 GHz. <sup>◇</sup> at 4–8 GHz. <sup>§</sup> at 6 GHz. <sup>×</sup> power gain. <sup>◇</sup> at maximum gain.

# Chapter 5

## Introduction to Mixer Architecture

Mixers can be implemented using any nonlinear device such as diode, FET and bipolar transistors. Mixer design can be classified as passive and active structures. In the passive architecture, we wish to minimize the conversion loss, because low conversion loss generally guarantees low-noise operation. In microwave FET mixers, high gain is relatively easy to obtain, but it does not automatically guarantee that other aspects of performances will be good. Indeed, high mixer gain is often undesirable in receivers because it tends to increase the distortion of the entire receiver. Therefore, in most receiver applications, an active mixer is designed not to achieve the maximum possible gain, but to achieve a low-noise figure and modest gain.

### 5.1 Active Mixer

The CMOS active mixer (frequency multipliers) has many advantages over the passive type mixers. The active mixers can have broad bandwidth and provides conversion gain. The most well-known active mixer architecture is current commutating mixer shown in Fig. 5.1. This topology was introduced for the first time by Barrie Gilbert [49] in bipolar technology. Although other types of the mixers have been proposed, while most FET mixers structure have the LO and RF applied to the gate/source and IF is filtered from the drain. The time-varying transconductance is the dominant contributor to frequency

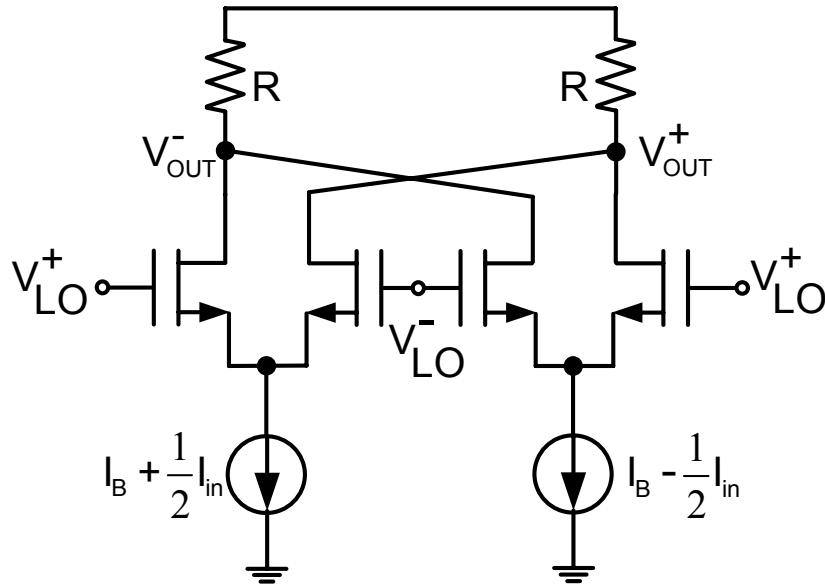


Figure 5.1: Current commutating active mixer.

conversion. In such mixers, the effect of gate-to-drain capacitance, gate-to-source capacitance and drain-to-source resistance are often detrimental and must be minimized. Since the time-varying transconductance is the primary contributor to mixing, it is important to maximize the range of the FET's transconductance variation. To maximize the transconductance variation, the FET must be biased close to its threshold voltage,  $V_t$ . Full saturation can be achieved by ensuring that the drain voltage  $V_d(t)$  under LO pumping remains at its dc value,  $V_{dd}$ . This condition is achieved by short circuiting the drain at the fundamental LO frequency and all LO harmonics. If the drain is effectively shorted, the LO current, which may have a fairly high peak value, can not cause any drain-to-source voltage variation. In this case the LO voltage across the gate-to-drain capacitance is minimal, so feedback is minimal and mixer is stable.

If the drain is not effectively shorted, the drain voltage varies with LO excitation. Then, the drain voltage is likely to drop, at the current peaks. If the voltage dips enough that the FET drops into its linear region, the peak transconductance also decreases. Similarly, the peak drain-to-source conductance increases, increasing the average output

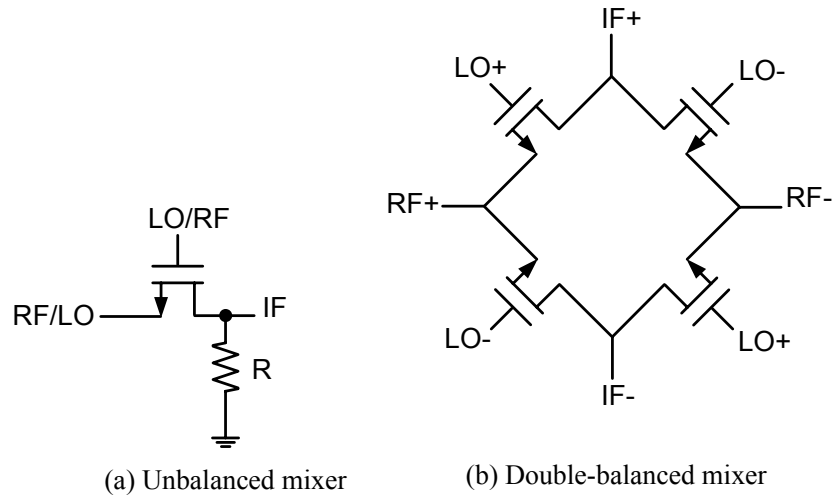


Figure 5.2: Passive mixer structures.

conductance, creating an additional loss mechanism. It is always best to bias the FET to attain the same drain voltage as it would require when used in an amplifier. A well-designed mixer is usually insensitive to small changes in dc drain voltage, but may be moderately sensitive to dc gate voltage.

## 5.2 Passive Mixer

The main advantage of the passive mixer is that it does not dissipate static power. More importantly, passive mixers have very low distortion, low  $1/f$  noise, and no shot noise. Since the high frequency noise is entirely thermal, the noise figure depends on the conversion loss. In Fig. 5.2 two examples of the FET passive mixers are shown. Since there is no current flowing thorough the switches, passive mixer tends to present a good linearity. Although, the switch resistance is non-linear but still their linearity performance is better than an active mixer. Passive mixers are divided into voltage-mode passive mixer [5], [50], Fig. 5.3, and current-mode passive mixer, Fig. 5.4. In the voltage-mode passive mixer, voltage is commutated using voltage switch. In addition, there is a substantial voltage swing across the switches, whereas the current-driven passive mixer

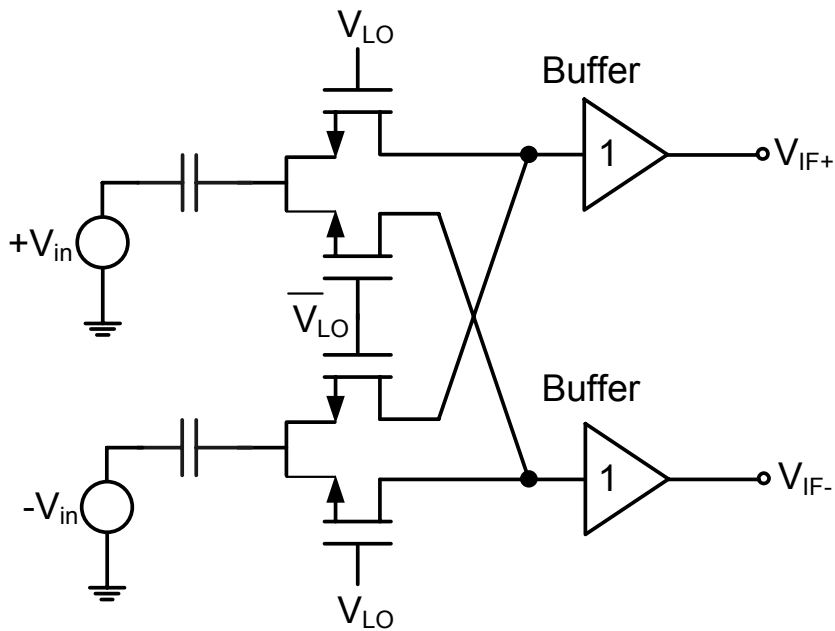


Figure 5.3: Double balanced voltage-mode passive mixer [5].

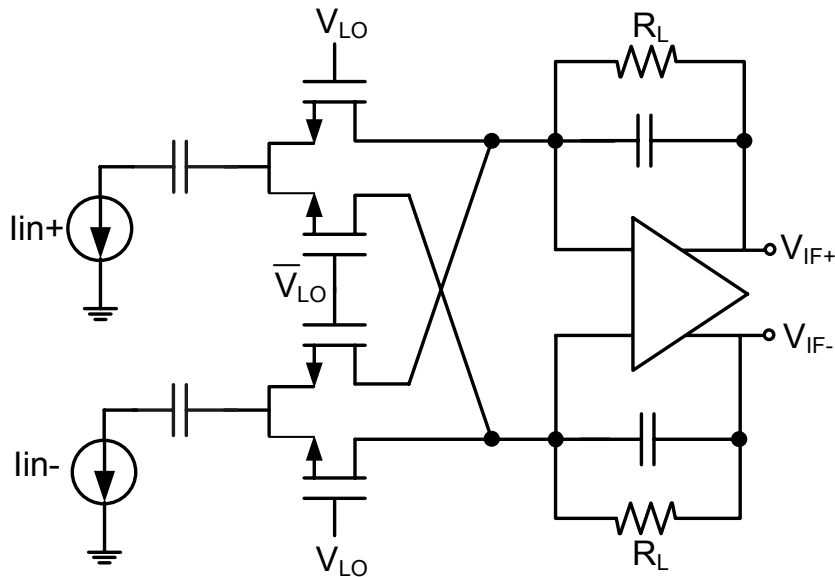


Figure 5.4: Double balanced current-mode passive mixer.

loaded with a transimpedance stage, have negligible signal swing across the switches, which further results in better linearity [51], [52]. In voltage-commutating passive mixer a buffer is needed after the switching transistors to drive the switch resistance and also

the input resistance of the stage following the mixer core. In contrast to the active mixer, in the current- and voltage-mode passive mixer, all the MOSFET switches are biased in triode region.

In Fig. 5.4, the RF transconductor transforms the RF output voltage of the LNA to a current. The conversion gain of this architecture assuming ideal LO square wave switching, is expressed as

$$CG = \frac{2}{\pi} g_m R_L \quad (\text{Eq. 5.1})$$

where  $g_m$  is the transconductance of RF stage in current-driver stage,  $R_L$  is the feedback resistor of the transimpedance amplifier. In practice, the real gain will be smaller due to the parasitic components at the common source of the switches of the mixer, and the output of the transconductance stage that shunts a part of the RF signal to ground. Therefore, it is important to be mindful of the device sizing, layout of the switching stage, and device matching in the transconductance stage.

In the passive mixer although the switches are non-linear, yet a better linearity compared to the active mixer can be achieved. The current-mode passive mixer has lower signal swing across the switches compared to the voltage-mode passive mixer, which increases the linearity performance of the current-mode passive mixer. The reason can be found in difference between loading stage in these two architectures.

Low frequency noise of the switches in the mixer design is a critical issue in many front-end receiver architectures, which can corrupt the output performance of the whole system. The flicker noise of the passive current-mode mixer is dominated by the transimpedance amplifier (TIA) stage. Any mismatch between devices in TIA adds to the total flicker noise of the mixer. Furthermore, the input parasitic capacitance of the mixer stage plays an important role in the noise contribution. A method to reduce the parasitic capacitance of the switches, is to reduce the device width. However if the device width

reduces, the ON-resistance of the device increases and the value of the ON-resistance becomes comparable to the output impedance of the driving stage. This causes the gain to reduce and the noise contribution to increase. On the other hand, this parasitic capacitance is much smaller in an active mixer, if the switches remain in the saturation region during the LO period.

## 5.3 Non-Idealities of the Mixer

### 5.3.1 Intermodulation Distortion

In short-channel CMOS transistors, the main source of distortion comes from the nonlinear behavior of the transconductance. Assuming the output transconductance is linear and the cross modulation between the transconductances is negligible. Then the ac current in a MOS transistor can be modeled as

$$i_{ds}(v_{gs}, v_{ds}) = g_m v_{gs} + g_{m2} v_{gs}^2 + g_{m3} v_{gs}^3 + \dots \quad (\text{Eq. 5.2})$$

The second-order transconductance  $g_{m2}$  equals to 0 A/V at  $v_{gs} = 0$ , and then increases before reaching a maximum value at a small overdrive voltage ( $V_{gs} - V_t$ ). Further increase in  $V_{gs}$  results in decreasing  $g_{m2}$ . As a result,  $g_{m3}$ , which is obtained by differentiating  $g_{m2}$  with respect to  $V_{gs}$ , decreases to zero at a very small overdrive voltage, i.e., when the transistor is operating in the moderate inversion region. Therefore, if the transistor is biased at this operating point, which is known as “sweep spot” [53], third-order harmonic distortion would tend to zero, which would result in infinite third-order output intercept point (OIP3), shown in Fig. 5.5.

Referring to the Fig. 5.2(a), when switching transistor is “on” it can be modeled as shown in Fig. 5.6. The transistor operates in the triode region and is replaced by a nonlinear resistor  $R_{on}$ . This is the primary source of intermodulation distortion. Note that arrow on the resistor symbol for  $R_{on}$  indicates the nonlinearity, not the time varying

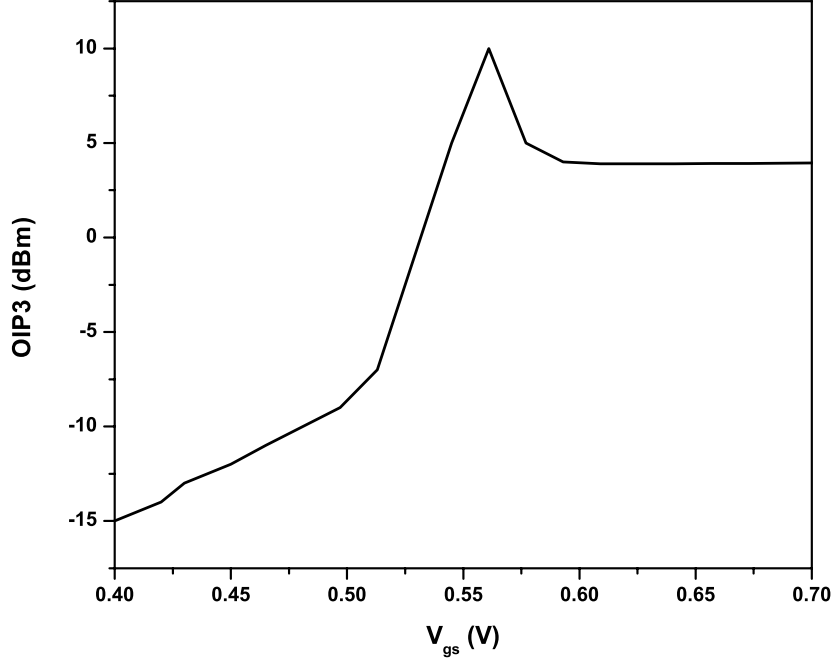


Figure 5.5: IIP3 versus  $V_{gs}$  for a single transistor.

resistor. The gate-to-source ( $C_{gs}$ ), gate-to-drain ( $C_{gd}$ ) and gate overlap capacitors are combined together and represented as  $C_g$ . In the low-frequency the distortion is mainly determined by the  $R_{on}$  of the transistor and distortion due to the parasitic capacitors  $C_{sb}$  and  $C_{db}$  is quite small. If we assume that LO is not switching, the mixer in Fig. 5.2(a) is represented as nonlinear time invariant (NLTI) system. Therefore, to derive distortion associated with  $R_{on}$ , we can use the equation for an MOS transistor biased in the triode region as

$$I_d = k(V_{gs} - V_t)V_{ds} - \frac{k}{2}V_{ds}^2 \quad (\text{Eq. 5.3})$$

where  $k = \mu C_{ox}(W/L_{eff})$ ,  $V_t$  is the threshold voltage, and  $L_{eff}$  is the effective length of the device. From (Eq. 5.3), we can see that  $I_d$  depends on  $V_{ds}^2$ , and this gives rise to distortion. Applying the Taylor series expansion, the third-order distortion in  $V_{if}$  is found as [6],

$$IM_3 = \frac{3}{8} \frac{1}{k(V_{GS} - V_t)^3 R} A_{rf}^2 \quad (\text{Eq. 5.4})$$

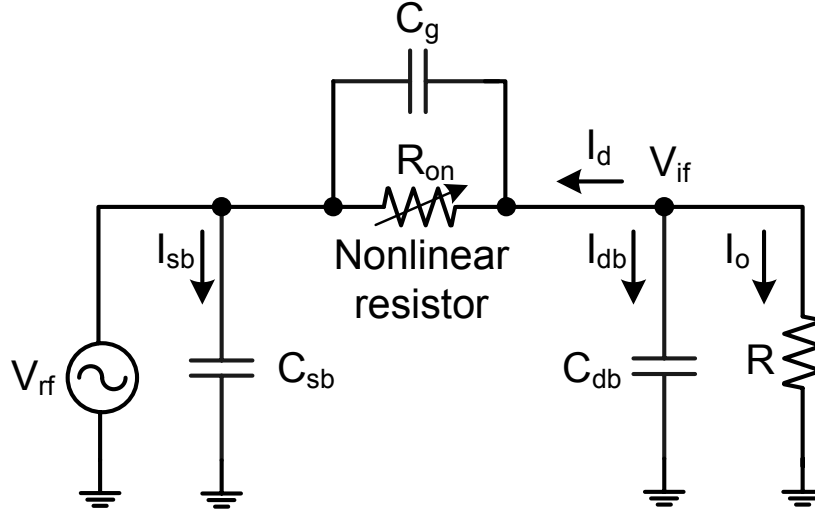


Figure 5.6: Distortion model for the unbalanced switching mixer in Fig. 5.2(a) [6].

where  $A_{rf}$  is the amplitude of the desired RF input to the mixer. This expression predicts the distortion in the switch for inputs with small signal levels and low frequency. Since the large signal is presented, (Eq. 5.4) does not predict the distortion in mixing operation, however, it illustrates design strategies for low distortion whether or not there is a large signal presented. The most important point from (Eq. 5.4), is that  $IM_3$  reduces with cube of the gate to source bias voltage. So, by applying large enough gate bias (or large LO drive for mixing operation), the third-order harmonic will reduce. Another important design strategy is to use large  $W/L$  ratios, however the bandwidth of the mixer decreases. At low frequency, if the gate bias ( $V_{gs} - V_{th}$ ) increases the distortion will reduce. The curve in Fig. 5.5 shows that for given different gate-to-source voltages ( $V_{gs}$ ) there is a point, which beyond that point increasing the bias voltage is not advantageous to the distortion reduction.

At high frequency, the reactive components coming from the junction capacitors contribute to third-order distortion and Volterra series must be used. To simplify the calculations, let's assume that the nonlinear capacitor  $C_{db}$  at the drain in Fig. 5.6 is replaced with a linear capacitor  $C$ , whose value is taken to be the value of  $C_{db}$  when  $V_{db} = 0$ , and

also assume that  $IM_3$  at low frequency is

$$IM_{3-LF} = \frac{3}{8} \frac{1}{k(V_{GS} - V_t)^3 R} A_{rf}^2$$

where

$$R \gg R_{on} \quad \frac{1}{j\omega_{rf}C} \gg R_{on} \quad \text{or} \quad \frac{1}{2\pi R_{on}C} \gg f_{rf} \quad (\text{Eq. 5.5})$$

Applying these assumptions to the model in Fig. 5.6, an expression for  $IM_3$  at high frequency due to interferers can be found as [6]

$$IM_3 = IM_{3-LF} \cdot \sqrt{1 + \left( \frac{RC\omega_{rf}}{3} \right)^2}. \quad (\text{Eq. 5.6})$$

Now, we consider the case when  $V_{lo}$  is switching. When  $V_{lo}$  is an ideal square wave, which means it has zero rise and fall time, the input voltage is multiplied by the Fourier representation of the LO square wave. The effect of the switching is simply shifting the frequency of the fundamental tone and the third-order products by  $f_{LO}$ . More details can be found in [6].

### 5.3.2 Second-Order Intermodulation Distortion

When two tones at  $\omega_{RF1}$  and  $\omega_{RF2}$  are presented at the RF input of the mixer, Fig. 5.7, the sum and difference of these two frequencies are generated as a result of nonlinearity in the RF input stage. Therefore, in the presence of duty-distortion in the LO, the offset frequency  $\omega_{RF2} - \omega_{RF1}$  can leak through following stage and fall in the output band.

A mechanisms which causes the second-order intermodulation ( $IM_2$ ) distortion in the mixer is known as RF-LO and LO-RF coupling, which is due to the parasitic coupling of the RF/LO frequency into LO/RF port [7], [54]. Lets first consider only offset from RF input. A low-frequency signal at frequency  $\omega_L$  at the RF input will mix with the RF

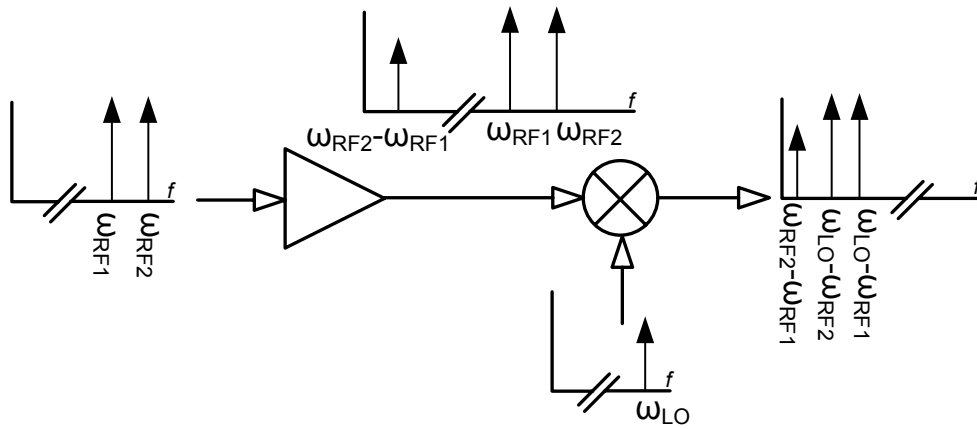


Figure 5.7: Nonlinearity in the RF.

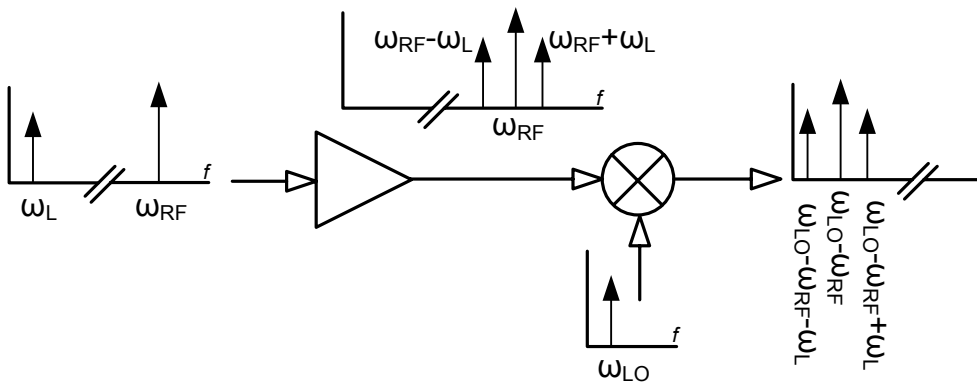


Figure 5.8: RF and low-frequency intermodulation.

signal at frequency  $\omega_{RF}$  in the presence of second-order distortion, and will create second RF tones at  $\omega_{RF} - \omega_L$  and  $\omega_{RF} + \omega_L$ . Both RF tones will mix with the local oscillator signal, generating the desired signal at  $\omega_{LO} - \omega_{RF}$  and the interferences at  $\omega_{LO} - \omega_{RF} \pm \omega_L$ , as shown in Fig. 5.8. As a result, the unwanted signal will mix down to the baseband and corrupts the baseband signal.

Leakage from LO port to the RF input creates intermodulation as shown in Fig. 5.9. The leaked LO signal on the RF port, is mixed with the LO signal, causing both the IF signal and a dc component appearing at the output. This will degrade the performance of the zero-IF receiver.

The other mechanism is due to the second-order nonlinearities in the active devices

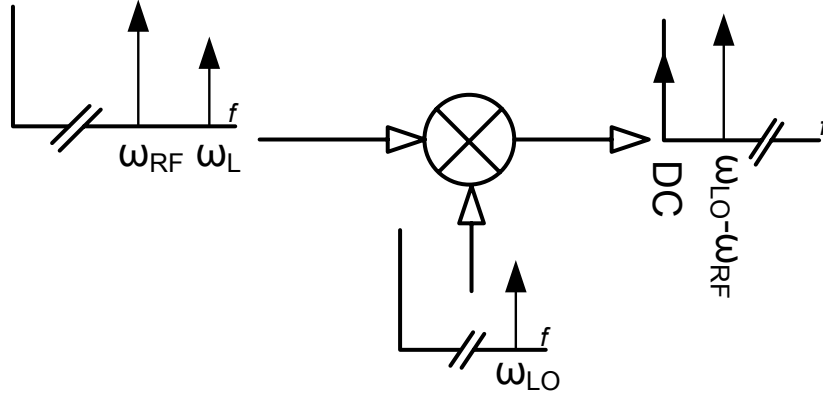


Figure 5.9: LO oscillator self-mixing. LO leakage to the RF port.

of the transconductor [55]. The low frequency intermodulation current at the output of the transconductor leaks to the output of the mixer without frequency conversion due to the duty-cycle distortion of the LO. This effect can be alleviated using a double-balanced topology if we assume that the devices in double-balanced structure are matched. Furthermore, the leakage due to the mismatch between the devices in the current switching stage is not easy to cancel. The second-order intermodulation products are generated due to the nonlinearity of the switching stage. The mismatch between two active devices contribute to the nonlinearity at low frequency. At high frequency on the other hand, the parasitic capacitance at common source of the RF input differential pair, increases the second-order intermodulation product. The parasitic capacitance introduces a limit to get a high second-order input intercept point (IIP2).

Considering a single balanced mixer in Fig. 5.10, and assuming a square-wave voltage applied at the switching pair, then the differential output current is equal to  $(I + g_{mRF}V_{in})$  for one half period and  $-(I + g_{mRF}V_{in})$  for the other half period. If the LO pulse has an exact 50% duty-cycle and assuming no mismatch between  $M_1$  and  $M_2$ , there would be no second-order term generated at the mixer output. Otherwise, if we consider the non-ideal case, the second-order intermodulation current at the output, neglecting the

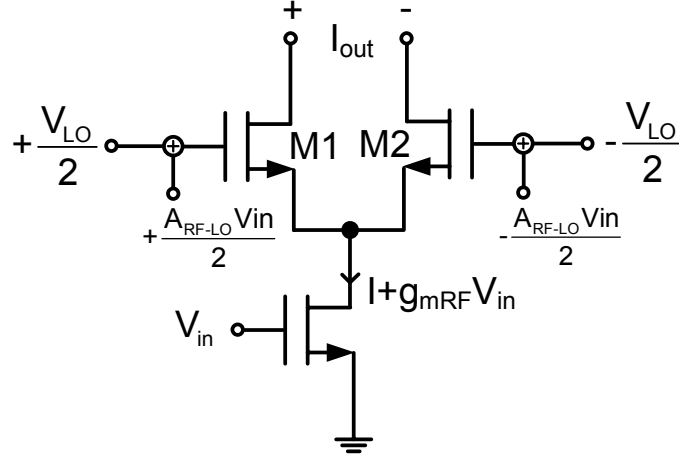


Figure 5.10: Self-mixing model in single balanced mixer [7].

high frequency components, is obtained by [7]

$$\begin{aligned}
 I_{IM2,out} &= \frac{g_{mRF} A_{RF-LO}}{V_L} V_{bk}^2 \times sw(t) \\
 V_{bk} &= A (\cos \omega_1 t + \cos \omega_2 t) \\
 I_{IM2,out} &= \frac{2g_{mRF} A_{RF-LO}}{\pi V_{pk}} A^2 \\
 &\times \left[ 1 + \cos(\omega_1 - \omega_2)t + \frac{1}{2} \cos 2(\omega_{LO} - \omega_1)t \right. \\
 &\left. + \frac{1}{2} \cos 2(\omega_{LO} - \omega_2)t + \cos(2\omega_{LO} - \omega_1 - \omega_2)t + \dots \right] \quad (\text{Eq. 5.7})
 \end{aligned}$$

where  $sw(t)$  is a square-wave function representing the LO waveform,  $V_{bk}$  is the blocker signal represented by a double sideband suppressed carrier (DSB-SC), and  $V_{LO}$  is a large amplitude sinusoid  $V_{LO} = V_{pk} \sin((2\pi/T_{LO})t)$  where  $V_{pk} \gg V_L$ . The square-wave function toggles between 0 and 1 with a duty cycle equal to  $2T_{sw}/T_{LO} = 2V_L/(\pi V_{pk})$ .  $V_{LO}$ ,  $I_{out}$ , and  $sw(t)$  are plotted in Fig. 5.11. From equation above, it is clear that the second term causes the intermodulation distortion, and the other spectral components can be easily filtered out. This equality shows that if there is a blocker at high frequency between LO frequency and received signal, both the received and intermodulation products would be available at IF.

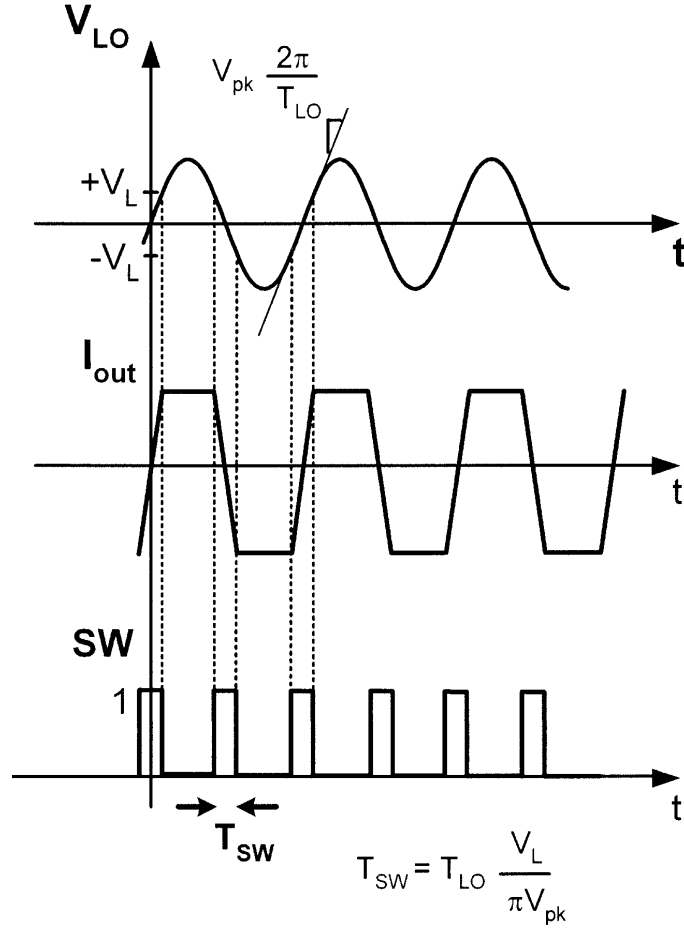


Figure 5.11: Time domain waveforms in a soft-switching single balanced mixer; applied sinusoid  $LO(V_{LO})$ , output current  $I_{out} = I_1 - I_2$ , and self-mixing function  $sw(t)$  [7].

From second-order input intercept point definition, the relation of the IIP2 to the LO amplitude and port-to-port coupling can be found as [7]

$$IIP2 (dBm) = 20 \log \left( \frac{2}{A_{RF-LO}} \right) + V_{pk} (dBm). \quad (\text{Eq. 5.8})$$

In order to increase the IIP2, the RF-to-LO coupling should be reduced and LO amplitude has to be increased. The coupling of the RF signal to the LO port of the mixer can create  $IM_2$  through modulating the resistance of the switches. In the direct conversion architecture, since the local oscillator is at the same frequency as the RF carrier, the potential exists for LO leakage to either mixer input or the antenna where radiation

may occur. The unintentionally transmitted LO signal may reflect back from an object nearby the transceiver, and be “re-received” consequently, which causing the self-mixing problem.

The  $IM_2$  of the input transconductance stage in the presence of the switch mismatch, can be harmful as well. The  $IM_2$  created by the transconductance stage can be up-converted around LO frequency in presence of the mismatch by the RF stage, and then down-convert to the baseband by the switching stage. Therefore, if a low-frequency signal is presented at the RF input, any available offset in the switching stage will allow this low-frequency signal to feed through to the mixer output.

Similar to (Eq. 5.2), considering the transfer characteristics of a nonlinear amplification circuit expressed by Taylor series expansion as [56],

$$v_{out}(t) = \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + \dots \quad (\text{Eq. 5.9})$$

where  $\alpha_1$  is the small-signal voltage gain,  $\alpha_2$  and  $\alpha_3$  are the second- and third-order distortion coefficients, respectively. For distortion analysis, assuming the interferer signal at RF input as

$$v_{in}(t) = A_m m(t) \cos[(\omega_c - \omega_0)t + \varphi_m(t)] \quad (\text{Eq. 5.10})$$

where  $A_m$  is the peak signal amplitude,  $m(t)$  is the modulating signal,  $\omega_c$  is the carrier frequency,  $\omega_0$  is the phase offset from carrier frequency, and  $\varphi_m$  is the time-varying phase signal. Now lets assume that our front-end design consists of an LNA followed by a quadrature mixer.

Let us represent the gains, second-/third-order distortion coefficients of the LNA and mixer by  $G_{LNA}$ ,  $G_{MIX}$ ,  $\alpha_{2LNA}$ ,  $\alpha_{3LNA}$ ,  $\alpha_{2MIX}$ , and  $\alpha_{3MIX}$ , respectively. The second-order distortion nonlinearity in the absence of distortion is calculated by applying the

signal in (Eq. 5.10) to (Eq. 5.9) and then the output of the mixer  $v_{out-Mix}$  is [57],

$$\begin{aligned}
 v_{out-Mix}(t) = & G_{LNA}G_{MIX}A_m m(t) \cos[\omega_0 + \varphi_m(t)] \\
 & + \frac{1}{2}\alpha_{2MIX}G_{LNA}^2 A_m^2 m^2(t) \\
 & + \frac{1}{2}\alpha_{2MIX}G_{LNA}^2 A_m^2 m^2(t) [\cos(2\omega_0 t + 2\varphi_m(t))]. \quad (\text{Eq. 5.11})
 \end{aligned}$$

If  $\omega_0$  is much larger than channel bandwidth, the second term  $0.5\alpha_{2MIX}G_{LNA}^2 A_m^2 m^2(t)$  generates in-band distortion. The first term and third term would be filtered-out by the low-pass filter following the mixer.

From above, it can be concluded that the presence of LO leakage at the input of RF circuit, degrades IIP2 of the receiver. Therefore, it is not only the mismatch in the circuit that should be taken care, but also the leakage from LO to RF should be minimized to improve the IIP2.

## 5.4 Noise in the Mixer

Mixer noise, particularly flicker ( $1/f$ ) noise in the CMOS mixers, can be troublesome when receiving narrowband wireless channels such as global system for mobile (GSM) communications systems. In [8], an extensive studies on the output noise of the active mixer, due to the flicker noise of the FET is done. The flicker noise of the FET is directly proportional to the dc current, which is commutated by the switching pair. As shown in Fig. 5.12, reduction in the current flowing through the switching stage would reduce the flicker noise. This method can be implemented by injecting a part of the current  $I_B$  into tail of the differential pair [8]. This technique reduces the flow of the current in the switching stage transistors. However, this method poses some drawbacks such as increase in white-noise level due to the additional current source plus linearity degradation. Another issue is the reduction of transconductance of the active differential FET switches, as their current is reduced.

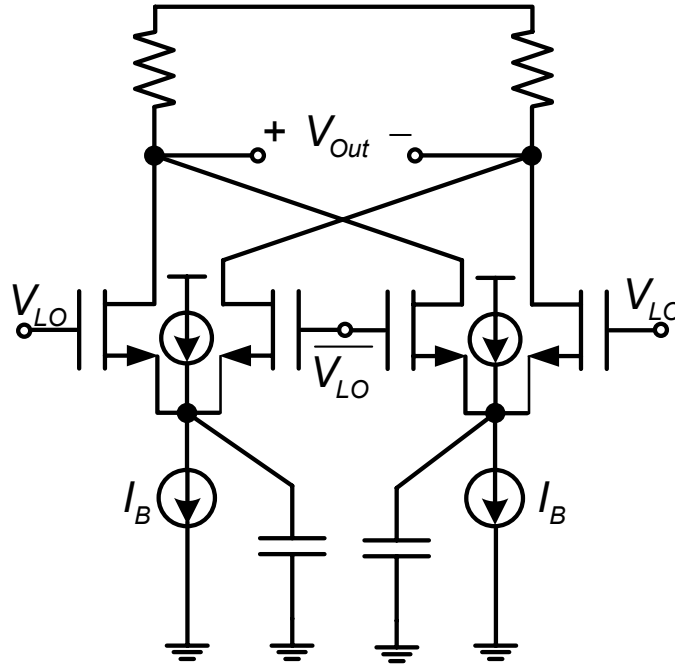


Figure 5.12: Noise reduction technique in an active mixer [8].

On the other hand, in a passive mixer, which operates without current commutating, results in a very low flicker noise at the output. Indeed, this mixer would only commutate the ac current. Since the mixer switches carry no DC current, they operate in the triode region and have to be driven with strong LO voltage. When LO is high, the triode FET switch directly connects the input transconductor to the output load through its ON resistance. Therefore, in order to minimize the loading-effect of the stage following the mixer, a current buffer is used after the mixer to isolate it from other stages, shown in Fig. 5.3. If voltage is desired instead of current at the output, a transresistance buffer should be designed.

In order to determine the noise of the passive mixer we have to take the output current buffer of the mixer into account. Consider a noise voltage at the frequency  $\omega_m$  in the input node of the current output buffer, Fig 5.3. Similar to the flicker noise, white noise of the load and buffer directly appears at the output. If FETs are used in the bias current

of the buffer, the flicker noise dominates the low-frequency of the buffer. Therefore, large FETs should be used in order to lower the flicker noise at the output.

In an active mixer, however, the flicker noise of the FET switches appears due to two different mechanisms [8]; direct mechanism, which is due to the commutated currents, and indirect mechanism, which is because of the parasitic capacitance at the tail of the differential pair, shown in Fig. 5.12. In the direct mechanism, the flicker noise is represented as time-varying offset voltage of the gate associated with the differential pair, having a constant rms value and a spectral density proportional to  $1/f$ . The offset voltage slowly modulates the commutation instant, which is located at the zero crossing of the LO waveform. This results in a train of noise pulses, which add to the ideal square-wave commutation waveform, and then flicker noise appears at the output. The analysis and expressions in [8] is used for a mixer with narrowband frequency.

Basically, if there is a leakage at the input RF signal  $f_{in}$ , the flicker noise appears at DC and  $2kf_{LO} \pm f_{in}$ . So, in a direct conversion architecture, where  $f_{in} = f_{LO}$  if there is a flicker noise at low frequency at the current source of the transconductance stage, it would be up-converted to the LO frequency. However, if there is a blocker at  $(2k - 1)f_{LO} + f_{in}$ , the dc commutating mechanism of the switches would transfer the flicker noise of the switches to the output [50]. This problem is not avoided in a broadband design, and the flicker noise can still appear at IF, if there is a blocker at  $f_{LO} + f_{RF}$ . Therefore, if the front-end receiver is broadband, large blockers at specific frequencies can create baseband flicker noise in both active and passive mixer. According to the mixer architecture, the affect of the flicker noise can be different. More details about the flicker noise in broadband circuits are given in [58].

# Chapter 6

## Proposed Integrated Wideband Receiver Front-End

The UWB front-end can be designed either as direct conversion technique or double conversion technique. So far many designs have been introduced which utilize the direct conversion receiver (DCR) architecture to implement the wideband receiver front-end [13], [59] and the problems with DCR (zero-IF) are also well understood [60]. In the UWB receiver front-end a blocking signal can simply get down-converted with the desired RF band to the baseband frequency. This blocking signal appears as low-frequency second-order distortion, which is generated due to the non-ideality of the receiver stage such as device/load mismatch in the mixer stage and RF self-mixing. A low linear receiver front-end would be more susceptible to the intermodulation products. Apparently, this issue in a wideband receiver is one of the drawbacks, which can severely suppress the front-end performances.

In the proposed double conversion architecture unlike the direct conversion technique, a half-RF architecture is utilized to alleviate the even-order distortion and LO leakage issues appeared in the DCR. This architecture, however, poses a number of drawbacks, which are described in this chapter.

## 6.1 Theoretical Calculations of the Receiver Requirements

The receiver front-end is designed based on a double down-conversion technique, which the first stage results in a half-RF, and second stage is a direct-conversion zero IF architecture. The key specifications for the proposed architecture are noise figure, input second- and third-order intercept point (IIP2 and IIP3), which are derived below. The specifications are calculated from the required signal-to-noise ratio, and the contribution of reciprocal mixing interferences from other bands.

### 6.1.1 Noise Figure Requirements

The total noise figure (NF) requirements of the receiver is calculated from input thermal noise (input noise of the receiver), noise due to the second-order nonlinearity products and noise due to front-end blocks in the receiver. It should be noted that noise from transmitter to the receiver part is ignored in this application since the receiver and the transmitter are not "ON" at the same time. The primary noise sources in the receiver front-end is mostly referred to the LNA and mixer. In addition, the loss associated with the preselect filter (1.1 dB) and TR (transmitter/receiver) switch (0.6 dB) are included in the NF calculation [9]. For a system operating at 480 Mb/s at 2 m, with signal-to-noise ratio (SNR) of 6 dB and a thermal noise power ( $P_{Nth} = 10 \log(k.T.B.10^3)$ ) of  $-86.77$  dBm, a NF equal to 6.2 dB is required, where  $k$  is Boltzman's constant,  $T$  is absolute temperature, and  $B$  is channel bandwidth (528 MHz). The strict sensitivity requirement of  $-73.2$  dBm to  $-80.5$  dBm is specified for information data rate of 480 Mb/s (at 2 m) to 110 Mb/s (at 10 m) [9].

### 6.1.2 Linearity Requirements

For the DCR system, the undesirable harmonics can fall in the RF frequency and reduce the system performance. The presence of other systems such as IEEE 802.11b/g, which

operate at 2.4 GHz-2.58 GHz frequency with the output power up to +30 dBm, lead to more challenging adjacent channel blocker rejection [22]. In addition, the in-band interferes from another UWB system should be considered to analyze the system linearity.

One source of the nonlinearity is second-order intermodulation IM2. From definitions, the IM2 products are created at; DC,  $f_1 + f_2$  and  $f_1 - f_2$ . The relationship between the power level of IM2 at  $f_1 \pm f_2$  (sensitivity  $P_{sens}$ ), interfere power at the input ( $P_{BLCK}$ ) and second-order intercept point (IIP2) is given as [61]:

$$IIP2_{REQ}(dBm) = 2P_{BLCK} - P_{sens} + SNR - 6 dB \quad (\text{Eq. 6.1})$$

where -6 dB represents the 25% IM2 products at  $f_1 \pm f_2$ . In the worst-case scenario where a WLAN system is placed at 0.2 m distance, an interferer can reach up to  $-3$  dBm. If the minimum sensitivity of the UWB receiver with 480 Mb/s is  $-73.2$  dBm with  $SNR = 6$  dB, a maximum IIP2 of  $+67.2$  dBm is required. Notice that the effect of pre-filtering is not taken into account. The required IIP2 can be lowered if the gain of the pre-filtering is considered. Assuming with an antenna filter, an out-of-band interferer can be attenuated by  $+20$  dB, which relaxes the required  $IIP_2$  down to  $27.2$  dBm.

One way to reduce the IM2 nonlinearity of the proposed receiver front-end, is to implement fully differential circuitry to reduce the generated common-mode due to the mismatch between devices. However, a fully differential structure may not be always possible for a stage like LNA in the UWB systems, since it is hard to design a low-loss wideband balun for wideband differential input signal. Therefore, other techniques like single-to-differential (SD) conversion could be used to eliminate the lossy balun in front of the receiver.

For third-order intermodulation (IM3), which are placed at  $2f_1 \pm f_2$  and  $2f_2 \pm f_1$ , if

two-tones are equal, then the required IIP3 is calculated as [62]

$$\begin{aligned} IIP3_{REQ} (dBm) &= \frac{1}{2} (2P_{int1} + P_{int2} - (P_{sens} - SNR)) \\ &= \frac{1}{2} (2P_{int1} + P_{int2} - P_{IM3} + Gain (dB)). \end{aligned} \quad (\text{Eq. 6.2})$$

where  $P_{int1}$  and  $P_{int2}$  are the received interference powers. For instance, if two interfere with power levels of  $-41$  dBm and  $-24$  dBm are received from an ISM band and a WLAN system respectively [22], the required IIP3 in this case with  $SNR = 6$  dB would be  $-9.7$  dBm, considering 110 Mb/s data rate.

Depending on the gain of the mixer, the linearity values could be even higher for different applications in the receiver front-end. The gain requirement of the front-end stage, is a trade-off between low-noise and linearity. For instance, the gain of the LNA should be high enough in order to get low NF, but not too high to corrupt the linearity requirements. In fact, the gain of the receiver can be compensated by a baseband filter or a variable-gain-amplifier (VGA) stage.

## 6.2 UWB Front-End Architecture

The proposed receiver architecture is based on a dual-conversion heterodyne technique, which enables for high system integration level and low power applications. A simplified block diagram of the receiver front-end is shown in Fig. 6.1. A SD LNA circuit is designed to avoid the lossy and costly balun in front of the receiver. As shown, after the LNA, a two-stage down-conversion mixer is designed to down-convert the wideband RF frequency to the baseband. Therefore, a 3–8 GHz RF frequency is down-converted to zero-IF at the baseband. The output buffers in Fig. 6.1 are integrated for the measurement purposes only. The differential output of the mixer is converted into a single I/Q, and drive an external  $50 \Omega$  load.

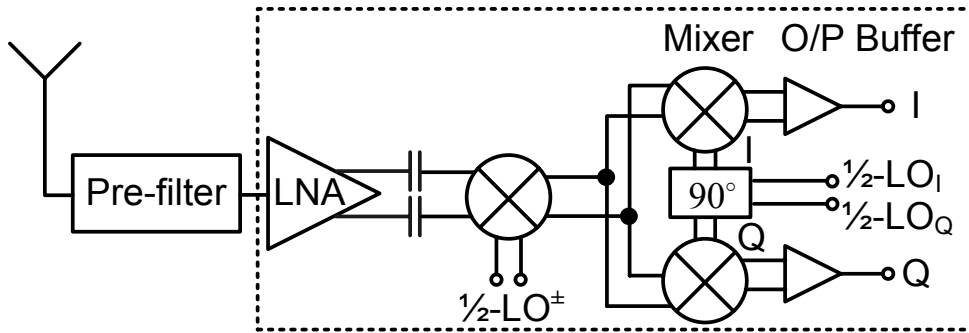


Figure 6.1: Simplified block diagram of the UWB front-end receiver

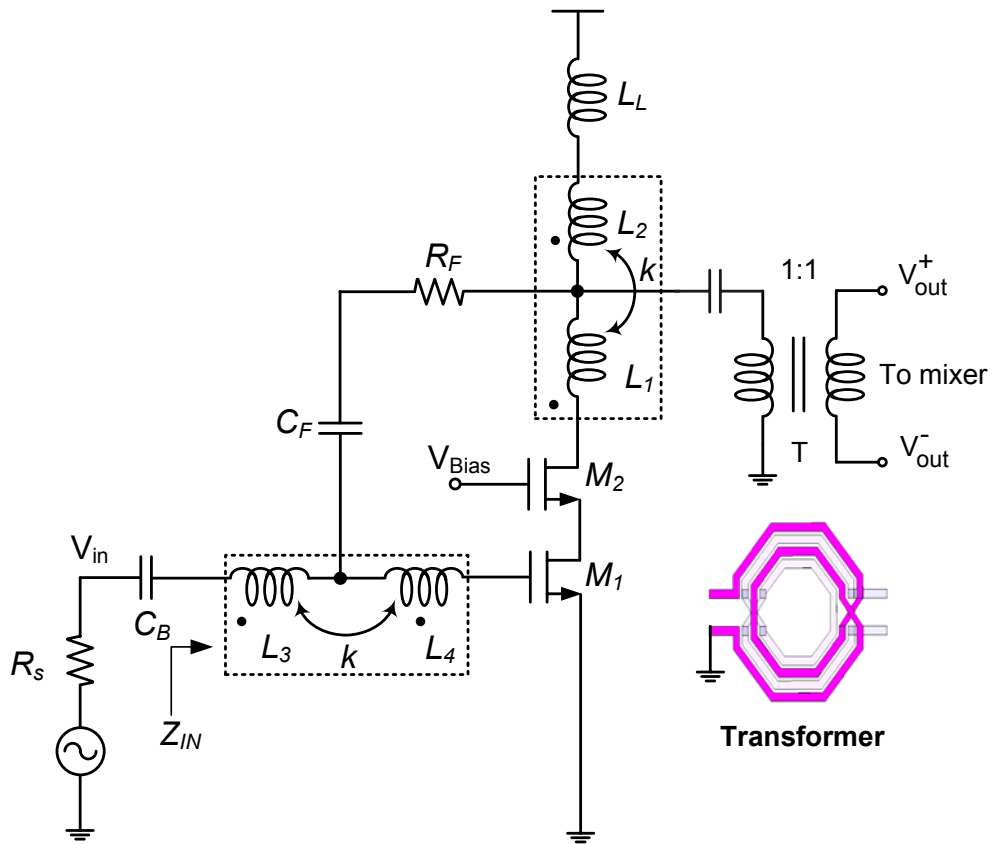


Figure 6.2: Simplified schematic of the UWB single-to-differential LNA (biasing is not shown).

### 6.2.1 Single-to-Differential LNA with On-Chip Transformer

In Fig. 6.2, a SD LNA using on-chip transformer is shown. The components values of the SD LNA are the same as the values mentioned in the table. 4.1. The SD LNA is used

with an output transformer load to provide differential output. The output transformer acts as AC-coupling, which attenuates the low frequency IM2 harmonics generated by the LNA. In addition, coupling capacitors were placed between LNA and mixer to remove any DC offsets from LNA. A very low current is consumed in this design, since only one stage is used to generate differential output. More details on the principle of the LNA can be found in [32]. The designed on-chip transformer, improves the integration level of the receiver, which avoid the use of off-chip lossy balun.

In comparison with microwave balun structure, which requires physical dimensions on the order of the signal wavelength, transformers have a relatively smaller size and wider bandwidth. Owing to the octagonal structure of the transformer, less loss is introduced. A symmetric winding style is implemented in the top metal layers to reduce the substrate capacitive loss. The appropriate number of turns  $n = 1$  is chosen for two reasons; to provide high quality factor ( $Q$ ) for better noise figure, and to prevent the LNA performances degradation.

Due to the bandpass and AC-coupling properties of the transformer, the low frequency IM2 components of the LNA are attenuated efficiently at the output of the transformer. Fig. 6.3(a) shows the transformer model used in this design. When two inductors are tightly coupled ( $k \approx 1$ ), then it is useful to view the coupled inductors as a perfect transformer with the parasitic components. The transformer is modeled with series resistances  $R_1$ ,  $R_2$ , parasitic capacitance of  $C_p$ , load capacitance  $C_L$  and mutual coupling ( $M$ ) between two inductors  $L_1$  and  $L_2$ , and  $I_{in}$ , which is the output current of the previous stage. Fig. 6.3(b) is an equivalent model of the circuit in Fig. 6.3(a) with an ideal transformer. The series resistances  $R_1$  and  $R_2$  are represented as

$$\begin{aligned} R_1 &= \frac{R_{p1}}{(1 + Q_1^2)} \\ R_2 &= \frac{R_{p2}}{(1 + Q_2^2)} \end{aligned} \quad (\text{Eq. 6.3})$$

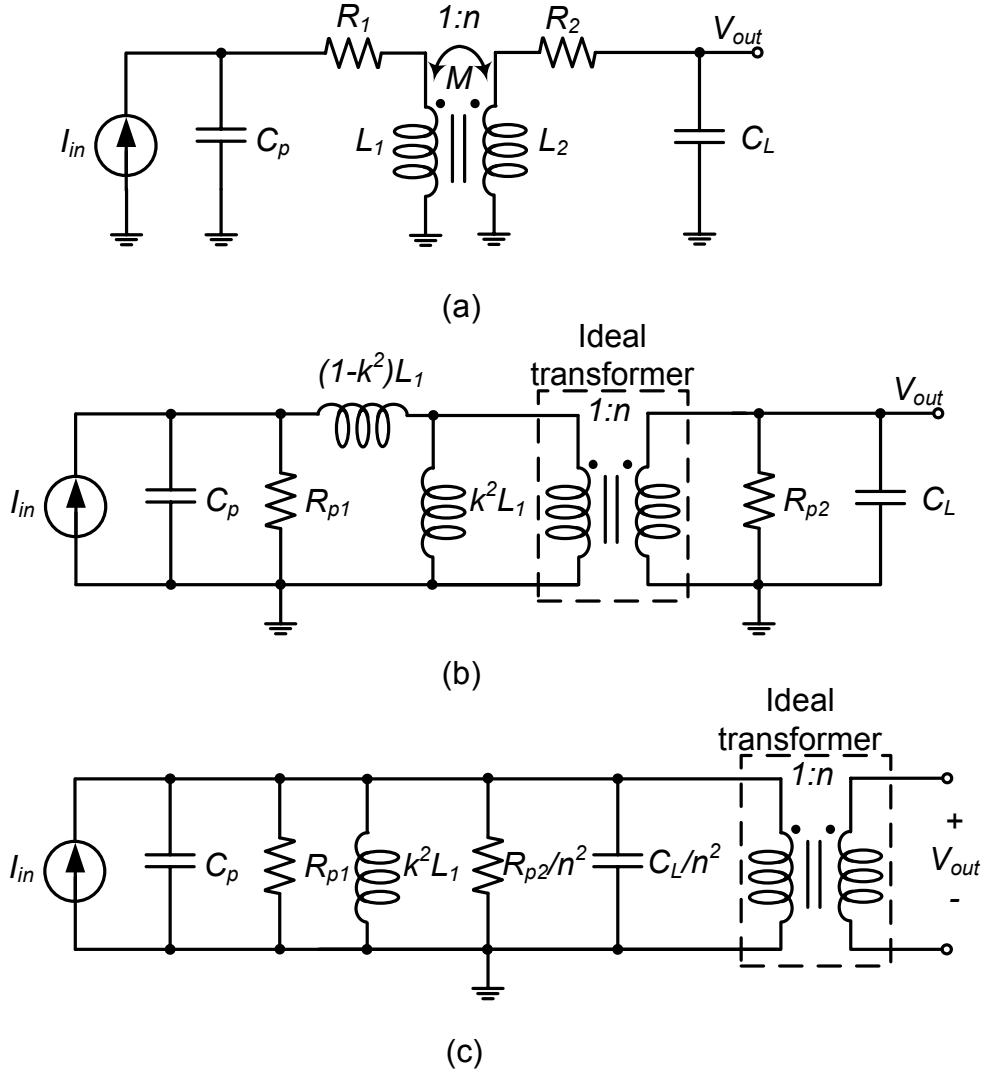


Figure 6.3: (a) Transformer model. (b) equivalent circuit model for coupled inductors. (c) equivalent circuit of (b) with load network transferred to the input.

where  $Q_1$  and  $Q_2$  are the quality factors of the primary and secondary of  $L_1$  and  $L_2$ . If we assume that  $k$  is very high and approximately equal to 1, then  $(1 - k^2)L_1$  is negligible, Fig. 6.3(c). Therefore, in resonance the voltage at secondary port is  $n^2$  times of the voltage at input port and  $V_{out}$  is

$$V_{out} = I_{in} \left( R_{p1} \parallel \frac{R_{p2}}{n^2} \right) n^2 \quad (\text{Eq. 6.4})$$

As the number of turns increases, the area occupied by the transformer increases

Table 6.1: Transformer Characteristics

Parameter	$Q_{p-max}$	$Q_{s-max}$	$L_p$	$L_s$	$f_{res-max}$	$k$
(1-10 GHz)	8 @ 8 GHz	13 @ 8 GHz	0.58 nH	0.68 nH	14 GHz	0.67–0.71

too, which causes an increase in the substrate capacitance and turn-to-turn capacitive coupling. Therefore, the resonance frequency of the transformer reduces. However, more turns induces stronger magnetic coupling, i.e., larger  $k$  factor. From layout design point of view, reduction in spacing between secondary and primary layers, improves the magnetic coupling between  $L_1$  and  $L_2$ , which leads to higher  $k$  factor. However, this space should not be kept as minimum as the technology limit. Because, as the secondary and primary layers get closer and closer, the coupling capacitors in between increase, and consequently resonance frequency drops drastically. Therefore, the geometrical parameters of the transformer should be selected with trade-offs.

Form above, a wideband transformer is designed with characteristics indicated in Table 6.1. Fig. 6.4 shows the S21 measurement over a wide range of frequency. The transformer was measured separately from 1–10 GHz, which shows a maximum primary inductor’s  $Q$  of 8 and secondary inductor’s  $Q$  of 13 at 8 GHz frequency.

### 6.2.2 Down-Conversion Mixer Architecture

In a CMOS down-conversion mixer DC offset and LO-RF feedthrough are the challenging issues, which can desensitize the mixer. Furthermore in the DCR, flicker noise is another issue, which appears at the output along with translated RF signal to the baseband frequency. The  $1/f$  noise in the mixer distort the signal, and degrades both the noise figure of the receiver and SNR. The  $1/f$  noise at the output of the mixer is partially originated from DC offset leakage due to the mismatch introduced by the switches. In the UWB systems, this issue is less disturbing than a narrowband system, since the baseband bandwidth is beyond  $1/f$  noise corner. However, this does not mean that  $1/f$

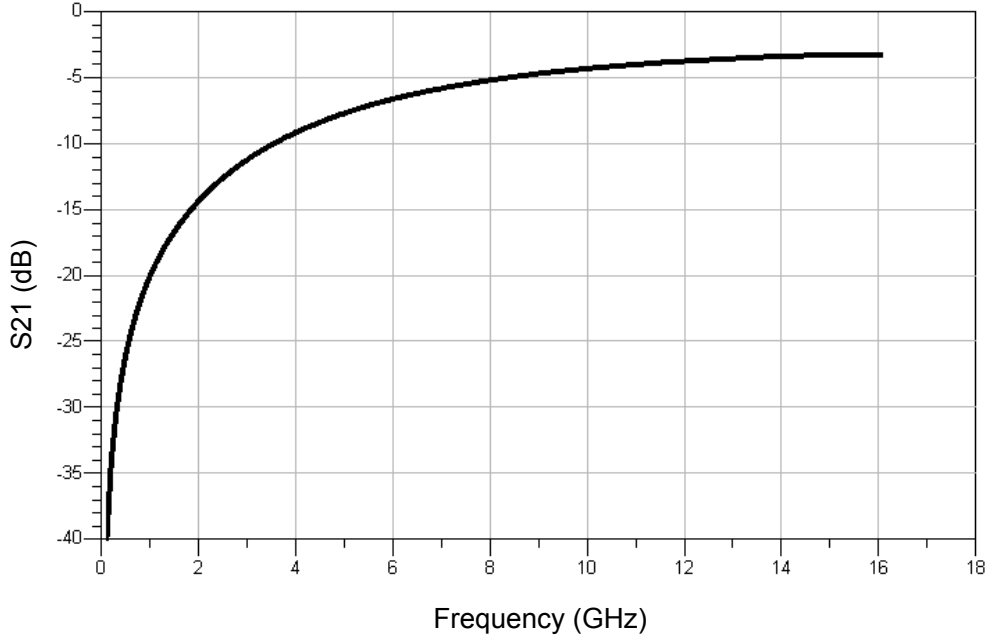


Figure 6.4: S21 measurement of the transformer over a wide frequency range.

noise can be ignored in the design of the UWB systems. The flicker noise can degrade the receiver's NF at low frequency. Due to the small size of the MOS transistors, the flicker noise can reach up to few MHz. The flicker noise of the switches down-converts to the baseband and corrupts the IF signal. In [58], it is discussed that if there is a blocker at  $(2k - 1)f_{LO} + f_{RF}$  in a zero IF system, the switch flicker noise would transfer to the baseband output.

A two-stage down-conversion mixing architecture is introduced in this work, which  $f_{LO} = f_{RF}/2$ , is chosen as subharmonic of the RF frequency. The proposed down-conversion mixer is shown in Fig. 6.5(a), and the down-conversion is performed in two-stage with the same LO frequency for both mixers. The first row of the transistors  $M_1 - M_2$  are the RF transconductance stage, which drive the switching transistors  $M_3 - M_6$ . The size of the switches are selected to obtain the proper noise figure and conversion gain of the mixer. The first switching stage down-converts the RF frequency to an intermediate frequency, and the second stage is similar to a direct conversion technique.

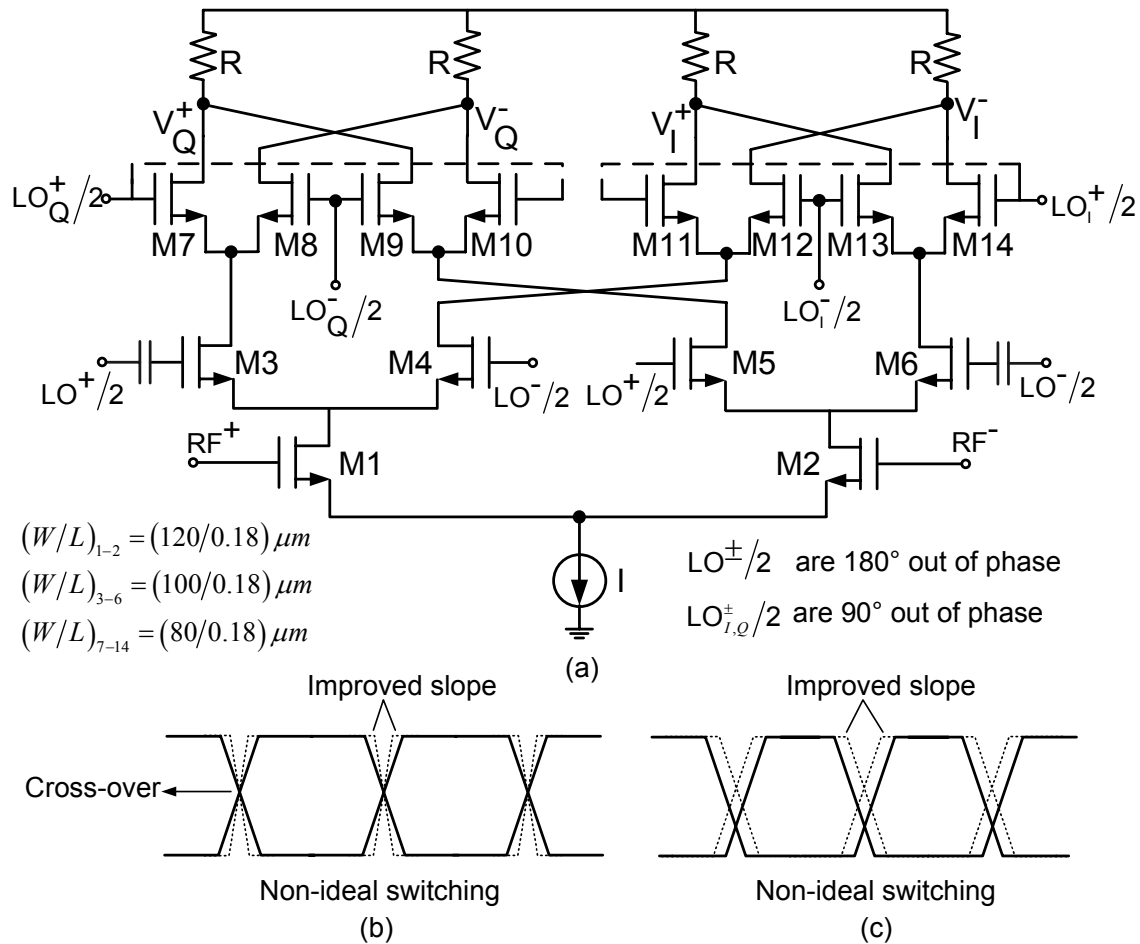


Figure 6.5: (a) Simplified schematic of the double-balanced down-conversion mixer, (b) & (c) Non-ideal LO switching and slope improvement

The second stage experiences the same issues as a conventional direct conversion receiver does, such as flicker noise. However, having a LO waveform with a large  $S \times T$  product, that is, low frequency LO with sharp transition will lower flicker noise of the switching stage, where  $S$  is the slope of the LO waveform at cross-over point, and  $T_{LO}$  is the LO period [8]. The  $1/2$ -LO signal is applied to the gate of the switching transistors stage to modulate the drain voltage of  $M_1 - M_2$ . The RF frequency is down-converted into  $1/2$ -RF frequency at the drains of  $M_3 - M_6$ . Therefore, the switching action of  $M_3 - M_6$  varies the drain-source voltage and transconductance ( $g_m$ ) to provide frequency conversion gain. The down-converted signal is translated into the baseband frequency by another  $1/2$ -LO

down-conversion stage using  $M_7 - M_{14}$  transistors. During the positive phase of 1/2-LO, current ( $I$ ) from the  $g_m$  stage are commutated through the drains of  $M_3$  and  $M_5$  to the Q-mixer quad  $M_7$  to  $M_{10}$ . During the negative phase of 1/2-LO,  $M_4$  and  $M_6$  commutate currents to the I-mixer quad  $M_{11}$  to  $M_{14}$ .

The magnitude of the  $1/f$  noise is dependent on the process used, size of the devices and topology of the design. Assuming the gate referred voltage of the switches as a slowly varying offset voltage associated with the switching pair. Due to the periodic behavior of LO frequency,  $\omega_{LO}$ , the voltage offset varies slowly and modulate the gate-referred noise. This modulation results in train of noise pulses, which adds to the square-wave modulation waveform, and appears as flicker noise at the output. The flicker noise at the output of the mixer appears due to two mechanisms; zero-crossing modulation (direct mechanism) and induced current in the tail capacitance ( $C_P$ ) (indirect mechanism) [8]. In a down-conversion mixer, the non-ideal properties of the switches causes non-ideal rise and fall time at the LO cross-over. As shown in Fig. 6.5(b), the LO slope at cross-over is reduced due to the imperfect characteristics of the switches and asymmetric layout routing. The idea in the half-RF mixer design is that  $1/f$  noise of the mixer is inversely proportional to  $S \times T_{LO}$ . So, since  $T_{LO}$  is large in this architecture, the  $1/f$  noise contribution to the output is small.

From system design point of view, a mixer that operates at lower frequency has advantages compared to a mixer that operates at higher frequency. The reason is the issues to generate high frequency LO signal. For the same architecture and technology, phase-noise performance of a voltage-controlled oscillator (VCO) at lower LO frequency is better than a VCO with higher LO frequency. For a VCO operating at higher frequency, larger transistor size is required to maintain the oscillation frequency ( $f_{osc}$ ). At higher  $f_{osc}$ , parasitic resistances/capacitances of the transistors and asymmetric routing of the layout, severely affect on the tuning range of the VCO. For the same topology, considering

the same phase noise performance, a VCO with higher  $f_{osc}$  consumes more power ( $P_{diss}$ ) than a VCO with lower  $f_{osc}$ . In a VCO which operates at lower frequency, the design of the output buffer is more relaxed. Consequently, a better figure-of-merit (FOM) can be achieved for a VCO operating at low frequency [63].

To investigate the mixer performance degradation due to the switching non-idealities, Fig. 6.5(b) plots non-ideal switching waveforms. As it is shown in solid line, the LO slope at cross-over is reduced due to the imperfect characteristics of the switches and asymmetric layout routing. One way to reduce the LO cross-over window is to increase the LO slope by increasing the LO-power, shown by dotted line in Fig. 6.5(b). This event helps to generate a sharp square-wave signal. The sharp square-wave signal can be generated using a frequency divider too, which redeems the noise of the switches. A larger LO-power forces the zero-crossing with a greater slope, which reduces the contribution of the direct noise [8]. However, if the high LO voltage forces the FET switches into deep triode region, the nonlinearity of the mixer deteriorates due to the nonlinear resistance of the switches.

Another issue that happens during the switching event is when the timing operation of the switches overlap each other, for instance when switch  $M_6$  is ON at  $LO^-$ , and  $M_5$  conducts for an interval time, while  $M_5$  is supposed to be OFF at this period. So, both  $M_6$  and  $M_5$  may conduct at the same time for a short period. In this case, a part of the current would be consumed by  $M_5$  due to the  $R_{ON}$  resistance of  $M_5$ . Therefore, the output conversion gain reduces. This issue can be originated from the mismatch between two switches. As a result, during this time flicker noise contribution increases.

As shown in Fig. 6.5(c), the non-ideal LO switching property due to the mismatch between threshold voltages of the switches (biasing voltage and device size mismatch), varies the duty cycle of the switches. Therefore, the ON-time of the transistor driven with  $LO^+$ , can be longer than its OFF-time, which causes the other transistor driven with

$LO^-$ , to have a shorter ON-time than OFF-time. Therefore, undesired components are generated at the differential output, which can cause the second-order intermodulation components (IM2). The ON and OFF times of the switches are determined by the bias voltage, and LO amplitude should be trimmed to reduce the undesired components due to the mismatch. Beside the threshold voltage mismatch, the coupling from LO to RF port can generate IM2. Generally, since the LO signal in the direct conversion technique is at the same frequency as the RF carrier, so LO signal can easily leak to the mixer input and result in time-varying dc offsets. Normally, the LO power is higher than RF power, which makes the LO to RF leakage more significant than RF to LO leakage. However, in half-RF architecture the local oscillator does not operate at the same frequency as RF carrier. This would eliminate the LO leakage to the RF port. Although the second LO is at the same frequency as the first IF, the self-mixing is relatively constant and can be canceled using the technique in [64]. Another advantage of this work is that the channel selection is realized with second LO (tunable), allowing the possibility of a programmable channel filtering.

In an architecture where the down-conversion is performed in two-stage, the flicker noise of the first stage may up-convert to the second stage and then to the IF frequency. In order to reduce the noise leakage from the first stage conversion to the output, the second stage is designed in double-balanced topology. By doing this, the LO-IF feedthrough would also be improved. The flicker noise of the mixer can be improved using PMOS transistors by increasing the length of the device, at the cost of bandwidth reduction.

Fig. 6.6, shows a flicker noise simulation comparison between two types of the mixer, which large  $S \times T_{LO}$  helps to lower the flicker noise as explained above. The conventional direct-conversion mixer shows much higher corner frequency than the proposed mixer. In general, since the baseband bandwidth in this application is very wide compared to many other narrowband designs, the corner frequency is higher than other narrowband

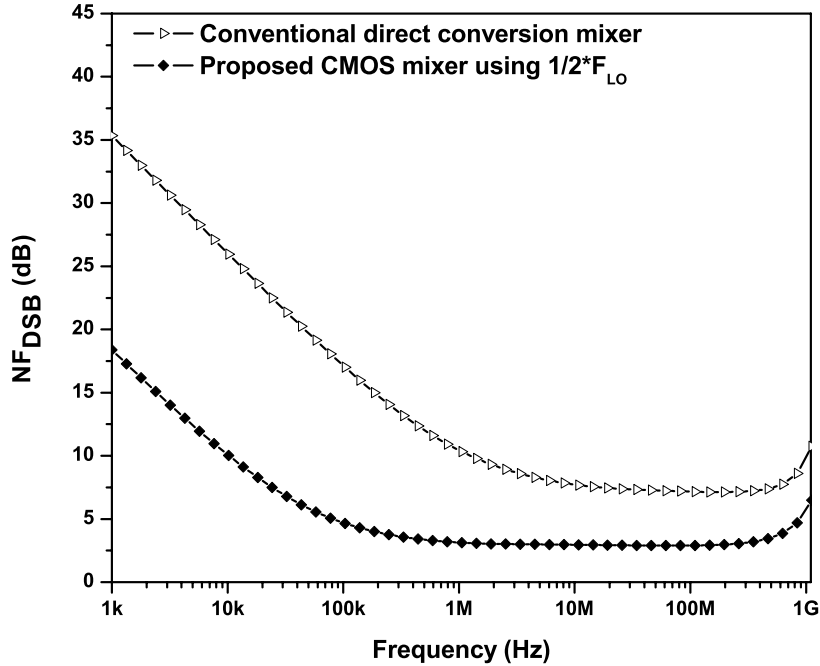


Figure 6.6: Flicker noise comparison between different types of the mixers.

applications. In the UWB application, since the baseband bandwidth is much wider than narrowband bandwidth, it is not possible to increase the size of the devices indefinitely for better flicker noise, because the baseband bandwidth reduces due to the parasitic capacitances.

A disadvantage of the proposed architecture is that  $I/Q$  mismatch causes the image of the signal to lie nearby zero. However, if the image experiences a high suppression by the antenna and RF front-end, the need for an exact image-reject filter will be obviated. Furthermore, the image at zero frequency can be filtered-out by coupling capacitors before the mixer. So the design of the image rejection filter can be more relaxed in this architecture compared to the other designs [65].

The isolation between the first and the second LO stage is finite, and thus a certain amount of LO signal from first/second stage leaks to the second/first stage. The LO leakage to the first and/or second stage due to the mismatch between two stages, produces a DC component at the output of the mixer. This phenomenon is called LO self mixing.

A DC offset cancellation technique can be used to remove the DC offset. The DC offset may be calibrated in different gain modes, which can be stored in a look-up table in a memory, or DC offset can be estimated by trimming the LNA input into a dummy load, which is stored in a memory. In the operation mode the DC offset value is fed to a subtractor in the analog baseband block to compensate the inherent DC offset based on operation gain.

In the proposed mixer, the required linearity and gain are set by proper selection of the load. For high linearity, the output impedance should be lower than the output impedance for high gain. For this design, the load is selected for reasonable gain and high linearity. Although an active load is more popular in the low voltage design and provides high gain-conversion, but it is at the expense of worse mismatch. The mismatch in the active load contributes more to the IM2 and DC offset, while resistive load has better mismatch. Moreover, the parasitic capacitance of the output active load create a low-pass filter with cut-off frequency of  $1/R_{load}C_{load}$  at the output load, which reduces the IF bandwidth, where  $C_{load}$  is the total parasitic capacitance at the output of the mixer. Hence, in order to improve the output bandwidth of the switching stage, the resistive output load is used instead of active output load.

Optimization of the mixer requires to adjust the LO-power and dc bias. The level of the LO-power is important to ensure that mixer reaches its peak linearity or “sweet spot”. To further investigate the linearity of the mixer, both nonlinearity of the transconductance and output conductance of a single transistor [66] are included in the drain-current in the Taylor-series expansion:

$$\begin{aligned}
 i_{ds}(v_{gs}, v_{ds}) = & g_{m1}(v_{gs}) + g_{ds1}v_{ds} + g_{m2}(v_{gs})^2 + g_{ds2}v_{ds}^2 + c_{m1}(v_{gs})v_{ds} \\
 & + g_{m3}(v_{gs})^3 + g_{ds3}v_{ds}^3 + c_{m2}(v_{gs})v_{ds}^2 + c_{m3}(v_{gs})^2v_{ds} + \dots
 \end{aligned} \tag{Eq. 6.5}$$

where  $c_{mx}$  is a cross-modulation term,  $g_{ds}$  is output conductance, and  $g_{mx}$  is the transconductance term. In (Eq. 6.5) the dependency of the  $i_{ds}$  with  $v_{gs}$ , and  $v_{ds}$  are shown, which

by reducing the dependency on  $v_{ds}$  higher linearity can be obtained. In Fig. 6.7,  $V_{OS}$  is the offset voltage source in series with the gate of the transistor, which is another source of the nonlinearity and IIP<sub>2</sub> reduction in the mixer. As mentioned in [67], in a conventional single-balanced down-conversion mixer the relation of the gate offset voltage to  $V_{IIP2}$  is

$$V_{IIP2} = 4(V_{GS} - V_{TH}) \frac{V_{P,LO}}{V_{OS}} \quad (\text{Eq. 6.6})$$

which  $V_{OS}$  is inversely proportional to the  $V_{IIP2}$  of the mixer. In order to achieve a high linearity, drain should be short-circuited at the unwanted mixing frequencies. Consequently the feedback path through  $c_{gd}$  is eliminated and undesired harmonics would not pass through  $c_{gd}$  to the gate. If  $v_{gs}$  of the switch increases further, the FET device drops into the linear region, as  $v_{ds}$  keeps reducing. As a result, the transconductance reduces, which reduces the output conversion gain. Concurrently,  $g_{ds}$  increases, which causes the average output conductance to increase. The increase in the output conductance introduces more source of nonlinearity.

The threshold mismatch between two transistors, which are laid-out side by side, introduces offset voltage  $V_{OS}$  in (Eq. 6.5). Therefore, IIP<sub>2</sub> can be improved further by increasing the LO-power or reducing the offset voltage. However, the LO-RF isolation may be affected by increasing the LO-power. A careful layout design helps to reduce the offset voltage due to the mismatch between devices, and subsequently higher IIP<sub>2</sub> is obtained. The IM<sub>2</sub> products of the LNA is strictly attenuated by the transformer, which adds to the advantages.

If we assume that the LO-power is large enough, and mixing function is observed by commutation of the RF transconductance with LO square-wave  $sq(\omega_{LO})$ , ignoring the



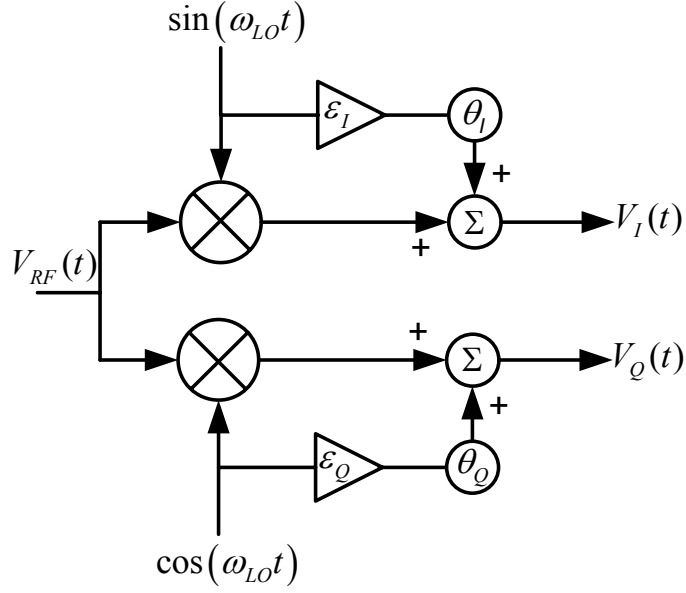


Figure 6.8: I/Q receiver model with I/Q imbalance.

where  $R$  is determined by the load resistance and  $R_{out,mixer}$  is the output impedance looking into drain of the switching stage when LO voltage is applied. The switching stage of the mixer is biased at  $V_{GS} - V_t = 0.25$  V to keep the switches in the saturation region, with total biasing current of 1.2 mA. Simulation results show that this bias voltage keeps an agreement between the linearity and noise figure as well. A further increase in the biasing voltage may cause the output voltage to be clipped, which reduces the conversion gain.

### 6.2.2.1 I/Q Mismatch

In practice, there are always mismatch in phase and amplitude between I and Q signals in the mixer, as modeled in Fig. 6.8. The I/Q imbalance is introduced by the local oscillator as amplitude mismatch  $\varepsilon$  and phase mismatch  $\theta$ . According to the model,

$$V_Q(t) = V_{RF}(t) \cdot \cos(\omega_{LO}t) + \varepsilon_Q \cdot \cos(\omega_{LO}t + \theta_Q). \quad (\text{Eq. 6.10})$$

$$V_I(t) = V_{RF}(t) \cdot \sin(\omega_{LO}t) + \varepsilon_I \cdot \sin(\omega_{LO}t + \theta_I). \quad (\text{Eq. 6.11})$$

we can rewrite (Eq. 6.10) and (Eq. 6.11) as

$$V_Q(t) = A \cos(\omega_{LO}t + \alpha). \quad (\text{Eq. 6.12})$$

$$V_I(t) = B \sin(\omega_{LO}t + \beta). \quad (\text{Eq. 6.13})$$

where

$$A = \sqrt{(V_{RF}(t) + \varepsilon_Q \cos(\theta_Q))^2 + (\varepsilon_Q \sin(\theta_Q))^2}. \quad (\text{Eq. 6.14})$$

$$\alpha = \tan^{-1} \left( \frac{\varepsilon_Q \sin(\theta_Q)}{V_{RF}(t) + \varepsilon_Q \cos(\theta_Q)} \right). \quad (\text{Eq. 6.15})$$

and

$$B = \sqrt{(V_{RF}(t) + \varepsilon_I \cos(\theta_I))^2 + (\varepsilon_I \sin(\theta_I))^2}. \quad (\text{Eq. 6.16})$$

$$\beta = \tan^{-1} \left( -\frac{V_{RF}(t) + \varepsilon_I \cos(\theta_I)}{\varepsilon_I \sin(\theta_I)} \right). \quad (\text{Eq. 6.17})$$

It should be noted that  $\varepsilon_I, \varepsilon_Q$  and  $\theta_I, \theta_Q$  in I and Q branches are independent and asymmetric, respectively. The first parts in (Eq. 6.10) and (Eq. 6.11) denote the down-converted signal and second terms are the frequency components created by the amplitude and phase mismatch. Equations (Eq. 6.12) and (Eq. 6.13) show that the outputs I and Q will be affected by the mismatch in the LO signal. In order to reduce the imbalance in the phase and amplitude in two branches, the following equalities should be satisfied,  $A = B$ ,  $\alpha - \beta = \pi/2$ , and  $V_Q(t) + V_I(t) = 0$ . Reduction in the mismatch would improve the performances especially second-order harmonic. To improve the mismatch in I and Q paths, long layout routing between stages should be prevented. The long layout routing simply adds loss and mismatch between two signals. Therefore, a unique symmetry between two paths is important. An I/Q calibration stage at baseband can improve the matching of the phase and gain in I/Q paths. Now, if we simplify (Eq. 6.5) and consider the second-order nonlinearity generated by the third-order nonlinearity

$$V_{out}(t) = \alpha_1 v_{in}(t) + \alpha_3 v_{in}^3(t) \quad (\text{Eq. 6.18})$$

where  $\alpha_1$  and  $\alpha_3$  are the small-signal voltage gain and third-order distortion coefficient. In order to find the second- and third-order intermodulation distortion due to the LO leakage, substituting (Eq. 6.10) in (Eq. 6.18), following the steps in [68] (Section 2, Desensitization and Blocking) and for simplicity let  $\theta_Q = 0$ , so the output voltage at  $Q$  side is given by

$$\begin{aligned}
V_{out}(t) &= \alpha_1 (V_{RF}(t) \cos(\omega_{LO}t) + \varepsilon_Q \cos(\omega_{LO}t + \theta_Q)) \\
&\quad + \alpha_3 (V_{RF}(t) \cos(\omega_{LO}t) + \varepsilon_Q \cos(\omega_{LO}t + \theta_Q))^3 \\
&= \dots + (\alpha_1 + 3\alpha_3\varepsilon_Q^2/2) (V_{RF}(t) \cos(\omega_{LO}t)) + \dots \\
&\quad + 3\alpha_3\varepsilon_Q \cos(\omega_{LO}t + \theta_Q)(V_{RF}(t) \cos(\omega_{LO}t))^2 + \dots.
\end{aligned} \tag{Eq. 6.19}$$

The term  $(\alpha_1 + 3\alpha_3\varepsilon_Q^2/2)$  reveals the second-order nonlinearity intermodulation at the output of the mixer. Therefore, the input level at each frequency over the amplitude of the output components at second-order nonlinearity is [68],

$$V_{IIP2} = \frac{\alpha_1 + 3\alpha_3\varepsilon_Q^2/2}{3\alpha_3\varepsilon_Q}. \tag{Eq. 6.20}$$

For the I side the same calculation is applied to get the second-order nonlinearity. So the impact of the mismatch, which clearly affects the IIP2 should be considered. It should be noted that this model can be further completed by considering the effect of I and Q on each other, which would make the analysis more complicated.

From [68], the input referred voltage intercept point for third-order two tone-intermodulation is given by

$$V_{IIP3} = \sqrt{\frac{4\alpha_1}{\alpha_3}}. \tag{Eq. 6.21}$$

If we plug (Eq. 6.21) into (Eq. 6.20), and let  $\alpha_1 = \alpha_3 \cdot V_{IIP3}^2/4$  then the relationship between IIP2 and IIP3 is obtained as follows

$$V_{IIP2} = \frac{V_{IIP3}^2}{12\varepsilon_Q} + \frac{\varepsilon_Q}{2} \simeq \frac{V_{IIP3}^2}{12\varepsilon_Q}. \tag{Eq. 6.22}$$

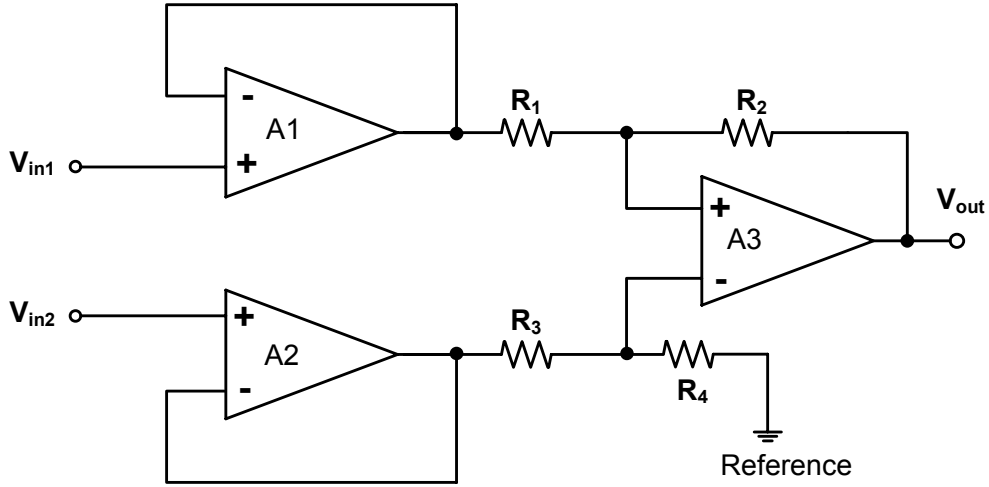


Figure 6.9: Instrumentation amplifier used for measurement setup.

where this approximation is valid for small values of  $\varepsilon_Q$ . This expression leads us to a conclusion that, IIP2 of the mixer in presence of LO leakage is directly proportional to IIP3. Therefore, an improvement in IIP3 reduces the second-order distortion, and improves IIP2, respectively. Another important point in (Eq. 6.22), is the reverse relation of the LO leakage to the IIP2. In this work, this concept is developed to improve IIP2 and IIP3 without extra circuit implementation. Although, much delicate circuit implementations are needed for much better IIP2 and IIP3 performances.

### 6.3 Instrumentation Amplifier as Output Buffer

An instrumentation amplifier, as shown in Fig. 6.9, is a closed-loop gain block that has a differential input and an output that is single-ended with respect to a reference terminal. Most commonly, the input impedances of the input terminals are balanced and have high values. High input impedance is necessary to avoid loading the previous stage. As for opamps ( $A1 - A3$ ), output impedance is very low, nominally only a few milli-ohms, at low frequencies. An instrumentation amplifier (inst-amp) employs an internal feedback resistor network that is isolated from its input signal terminals.

The inst-amp must be able to handle very low input voltages, and must be low noise. Furthermore, an instrumentation amplifier must provide sufficient bandwidth for the particular applications. Initially, the front-end receiver is designed for a 250 MHz bandwidth. Since typical unity gain bandwidth for an opamp fall between 500 kHz and 4 MHz, the bandwidth and gain performance trade-off is achieved easily, but at higher bandwidth it becomes much more of an issue.

The circuit in Fig. 6.9 shows a 3-opamp in one inst-amp block. If  $R_1 = R_3$  and  $R_2 = R_4$ , then

$$V_{out} = (V_{in2} - V_{in1}) \left( \frac{R_2}{R_1} \right). \quad (\text{Eq. 6.23})$$

This circuit provides an inst-amp function, amplifying differential signal while rejecting those that are common mode. In addition, it provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The designed inst-amp will match the output of the receiver front-end to a  $50 \Omega$  output, which is the impedance of the probe used for measurement.

## 6.4 Measurement Results

The wideband receiver front-end is fabricated in  $0.18 \mu\text{m}$  CMOS technology, shown in Fig. 6.10, which occupies an area of  $0.84 \times 1.06 \text{ mm}^2$ . A low frequency power-combiner at the output converts the differential output into a single-ended signal for measurement. A quadrature LO is applied off-chip using a signal-generator, which is directed to a wideband balun and  $90^\circ$  hybrid coupler. From measurement results, the LNA consumes a total current of  $I_{LNA} = 2.45 \text{ mA}$  from a  $1.8 \text{ V}$  supply voltage. The proposed mixer is designed to operate at  $1.8 \text{ V}$ , however in order to obtain better results due to the headroom issues, the operating point can be increased up to  $V_{DD2} = 2.2 \text{ V}$ . The measured

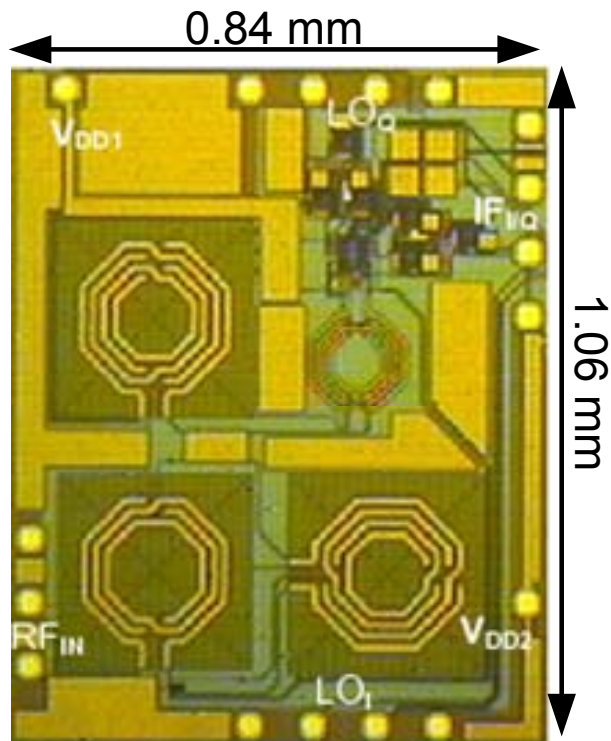


Figure 6.10: Chip microphotograph of the wideband receiver.

input return loss ( $S_{11}$ ) is plotted in Fig. 6.11, showing a reasonable input matching from 3–8 GHz, which satisfies the requirements. The fluctuation of the graph is expected from measurement setup. In order to make sure that the measurement is valid, all the tests are repeated for 10 chips. Due to the process variations, there are small differences between the performances of one chip to the other chip.

The conversion gain (CG) of the receiver is measured and simulated at the output of an on-chip unity-gain buffer, shown in Fig. 6.12. The peak gain is about 39.2 dB. The frequency response of the receiver can be improved with a wider-band baseband filter for higher data rate. The measured 3-dB bandwidth is shown, which is lower than in the simulation. The on-chip parasitic capacitances of the inst-amp create a low-pass filter with the output load of the front-end receiver, and have reduced the bandwidth of the design. For this reason, a bandwidth of 190 MHz is achieved. Therefore, the unity-gain

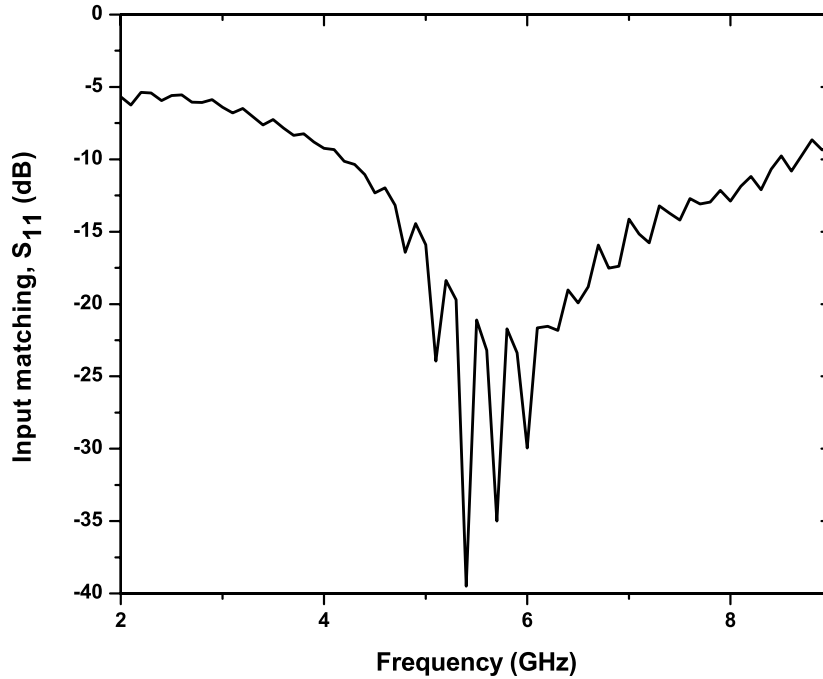


Figure 6.11: Measured input reflection coefficient of the receiver.

buffer should be designed with much wider bandwidth. Note that this inst-amp is used for measurement purposes, it would be replaced with a channel select filter in a complete receiver. The measured bandwidth can be improved by using an off-chip low-noise low-frequency inst-amp to reduce the on-chip parasitics. From a separate measurement, conversion gain ripple at different frequencies from 3–8 GHz is about 2.5 dB. In order to evaluate whether the circuit can handle large input signals, two-tone test was carried out. For the third-order intermodulation test, two signals with the same amplitude spaced with 10 MHz frequency, were applied to the RF port for 3–8 GHz. Similarly, for the second-order intermodulation test, two-tone were used to measure IIP2. The second-order intermodulation test was simulated at the output of the mixer separately, which shows  $IIP2_{max} > 48$  dBm. The measured IIP2's at different frequencies are listed in Table 6.2. For instance two tones representative of interferences at 7.02 GHz and 7.03 GHz with LO frequency of 3.57 GHz and RF frequency of 7.12 GHz were applied, which results in

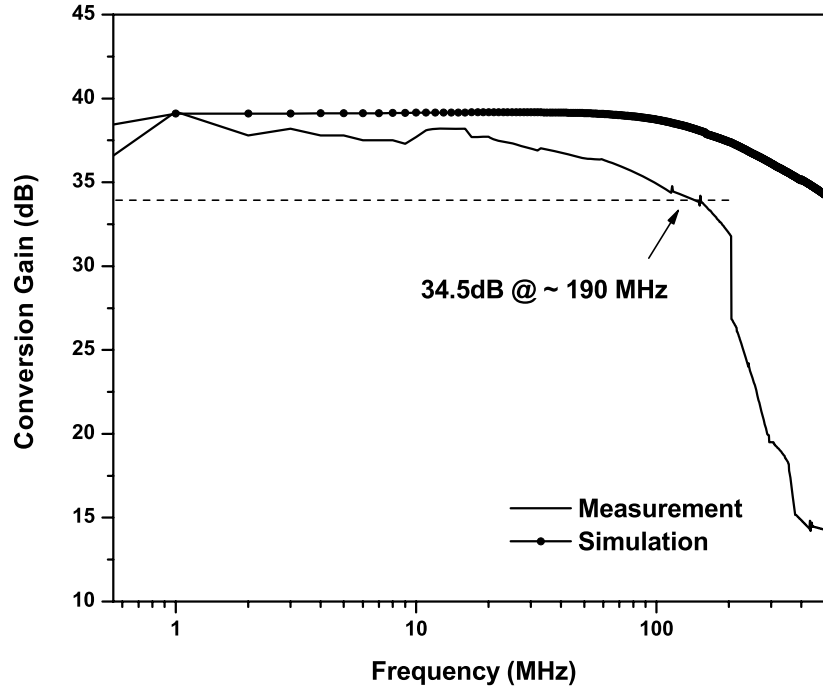


Figure 6.12: Measured/Simulated conversion gain of the receiver at 8 GHz.

Table 6.2: Performance Summary of the Receiver Front-end

RF Freq.* (GHz)	Gain <sub>max</sub> (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	P1 dB
3.43	32.4	0	33	8.3	-11
4.48	36.1	-2.5	28	5.4	-14
6.6	34	0	29	7.1	-12.1
7.12	34.54	+3.5	30	6	-10.5
7.65	34.8	+3.8	27	7	-10.8

\* The LO frequency is selected half of the RF frequency.

second-order intermodulation at 10 MHz. The measured IIP2 is 30 dB for this particular second-order intermodulation tone. Since the off-chip components can have different effects from frequency to frequency, a small phase or magnitude imbalance in the RF or LO input baluns and hybrid coupler easily dominates the IIP2 measurements. Therefore, it is important to make sure that these devices have the lowest phase imbalance at

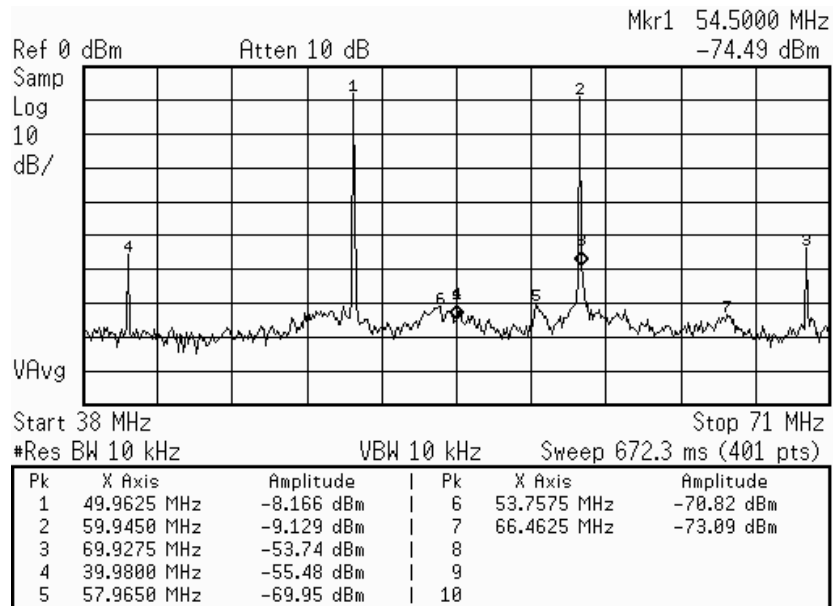


Figure 6.13: An example of measured IIP3 which shows the third-order intermodulation product.

their operating frequency. Generally, wideband off-chip baluns have high loss and phase imbalance. In order to guarantee the accuracy of the measurement, all losses of the cables and balun were considered during the measurement. In addition, the output unity-gain buffer can degrade the IIP2 performance too. In Fig. 6.13 and Fig. 6.14 the graph and measured third-order intermodulation are shown at 3.05 GHz frequency, for instance. Two-tones are applied at 3.05 GHz and 3.06 GHz respectively, while LO is at 1.5 GHz frequency. The 1 dB difference between two fundamental tones at  $49.96 \approx 50$  MHz and  $59.94 \approx 60$  MHz, in Fig. 6.13 (screen captured graph), maybe due to the unbalanced off-chip wideband balun at LO port. The phase and amplitude imbalance of the balun may cause distortion in the measurement, particularly at 1.5 GHz frequency, since the available wideband off-chip balun is calibrated from 2–4 GHz, which is used for LO signal. The measured second-order intermodulation of the UWB front-end receiver at 7.12 GHz is plotted in Fig. 6.15.

Table 6.2 summarizes some performances of the circuit. The measured LO-RF and LO-IF isolation is plotted in Fig. 6.16. The LO-IF isolation is not very high since the

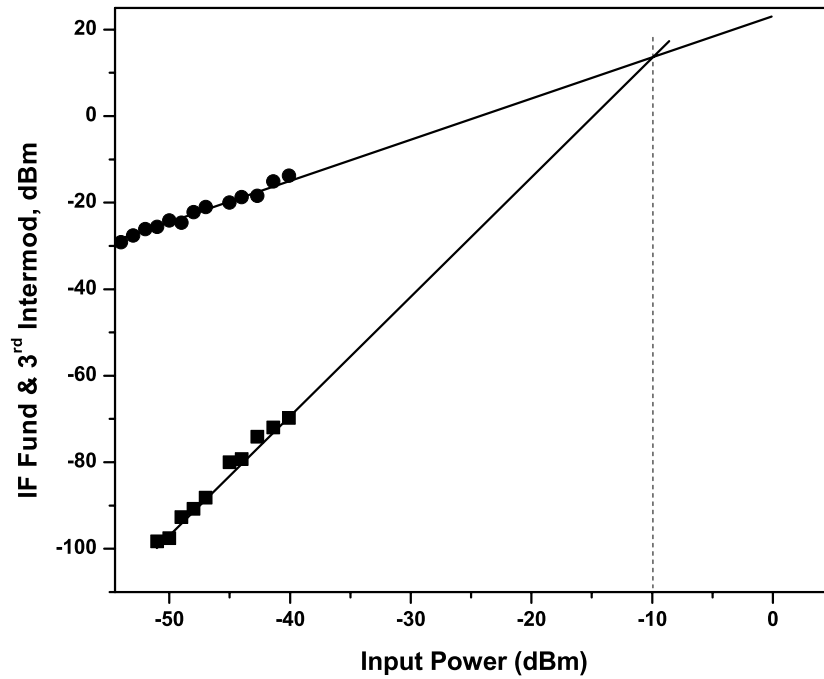


Figure 6.14: Measured IIP3 at 3.05 GHz frequency.

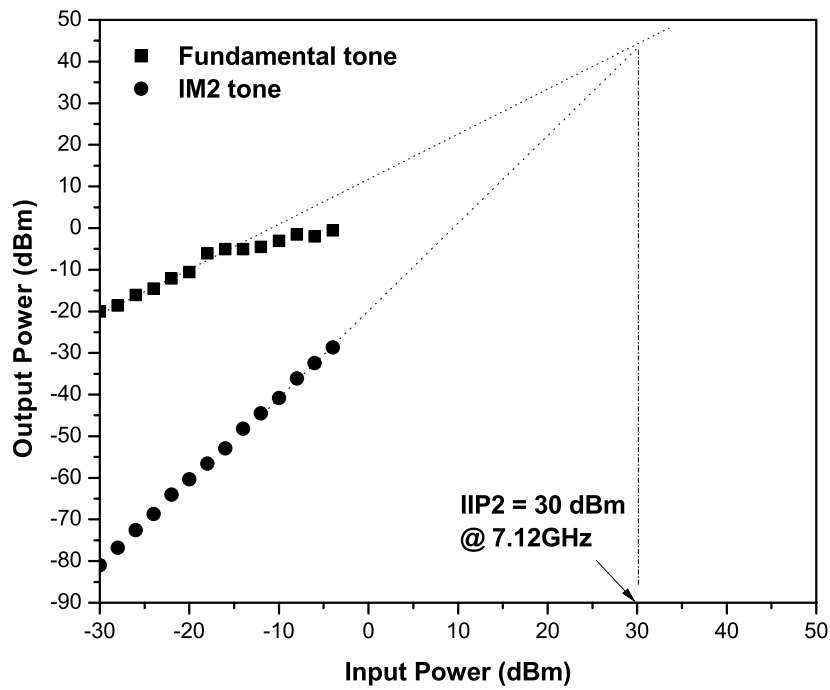


Figure 6.15: Measured IIP2 at 7.12 GHz frequency.

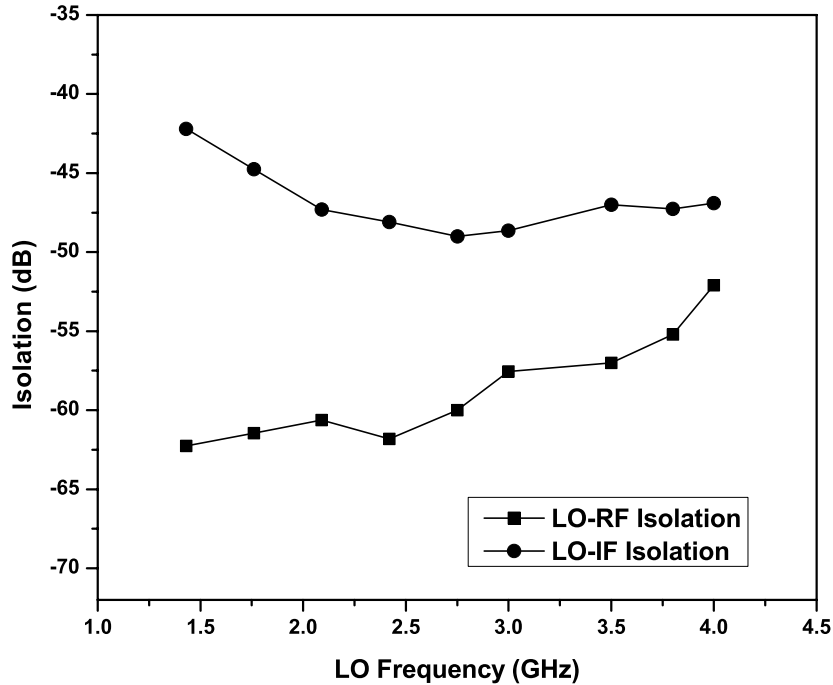


Figure 6.16: Measured isolation of the LO-RF and LO-IF ports.

first mixer produces an IF equal to the LO frequency. With a high isolation between LO-RF port, a maximum value of IIP2 is achievable [69], and less unwanted signals are presented at the output.

In order to measure the noise figure and flicker noise corner frequency, if possible, a wideband low-noise voltage amplifier with a known gain and a bandwidth wider than 500 MHz should be used to boost the front-end noise above the noise floor of the spectrum analyzer, to reduce the measurement uncertainties. Due to the spectrum analyzer limitations, the flicker noise frequency is extrapolated based on the readings on the spectrum analyzer. The noise figure is measured at different frequencies with a constant IF, which is recorded in Table 6.2. Furthermore, the noise figure is also measured at other IF frequencies up to 120 MHz. Since the input matching at 3.4 GHz is poor, the noise figure, at this frequency is higher than other frequencies, shown in Table. 6.2. The input 1-dB compression point shown in Table. 6.2 is measured at different frequencies.

Table 6.3: Performance Comparison Table

Ref.	BW (GHz)	Gain <sub>max</sub> (dB)	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	Power (mW)	Tech. <sup>×</sup> ( $\mu\text{m}$ )	FOM	Size $\text{mm}^2$
This work	3–8	36.1	>-2.5 <sup>+</sup>	<+33	5.4–8.3	8*	0.18	16.2–7	0.89
[70]	3–10	15.5	>-6.6	–	5.2–5.4	14.8	0.13	3.7–3.5	1.5
[71]	3–10	29.1	-13.5	–	4.9–8.8	33	0.13	2.8–0.92	2.4
[72]	3.1–8	23.2	>-3	<+46	5.2–7.3	18	0.18	1.7–0.9	1.7
[73]	3–5	37	-22	–	3.6–4.1	51	0.13	2.1–1.76	6.6 <sup>Ψ</sup>

<sup>×</sup> All the references use CMOS technology. <sup>+</sup> The lowest IIP3 is -10 dB at 3 GHz.

\* The power consumption including output buffer is 50.4 mW. <sup>Ψ</sup> The whole transceiver.

Two single tones are applied at  $f_{RF}$  and  $f_{LO}$ , respectively. The input amplitude of the RF signal is swept, and the output power of the receiver is measured accordingly. The measured gain compression of the output versus RF input power is plotted to find 1-dB compression point. The performance of the proposed front-end receiver is compared to the other references in Table 6.3. The  $FOM$  in here evaluates the gain, -3 dB bandwidth, excess noise factor and power consumption of the receiver, which is defined as [2]:

$$FOM = \frac{|Gain_{max}| BW_{GHz}}{(NF - 1) P_{mW}}. \quad (\text{Eq. 6.24})$$

Due to low power consumption and high gain, this work shows higher  $FOM$  compared to the other designs.

## 6.5 Measurement Setups

The gain measurement structure of the whole receiver front-end is shown in Fig. 6.17. Note that for an accurate measurement, shorter cables are preferred over long cables due to their lower losses. The gain of the device under test (DUT) is found as

$$Gain_{receiver} = Gain_{total} - Gain_{buffer} - Gain_{cable-loss} - Gain_{combiner-loss}. \quad (\text{Eq. 6.25})$$

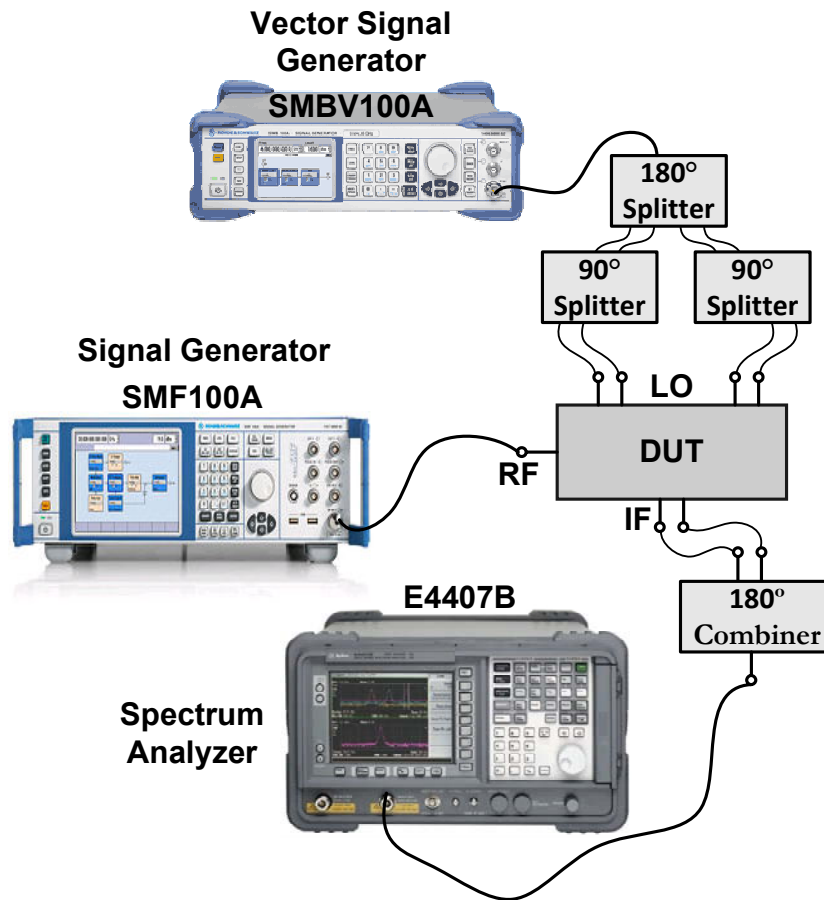


Figure 6.17: Gain measurement setup.

For the noise figure measurement, there are three methods namely as; Gain method, Y-factor method, and the noise figure meter method. The gain method involves more measurement steps as well as calculations, but under certain conditions, they turn out to be more accurate. From definition, noise is due to two effects. One is the interference that comes to the input RF system in the form of signals that differ from the desired one. The second is due to the random fluctuation of carriers in the RF system (LNA, mixer, receiver, and etc). This effect is a result of Brownian motion [74] of the electrons in device, which is equal to  $kT\Delta F$ , where  $k = 1.38 \times 10^{-23}$  Joules/ $K$ ,  $T$  is temperature in Kelvin and  $\Delta F$  is the noise bandwidth (HZ). At room temperature (290  $K$ ), the noise power density is -174 dBm/Hz. Therefore, from following equation the noise figure is

calculated [68]

$$NF_{Gain-method} = P_{Nout} - (-174dBm/Hz + 10 \log(BW) + Gain) \quad (\text{Eq. 6.26})$$

where “ $BW$ ” is the bandwidth of the output channel, “Gain” refers to the system gain, and “ $P_{Nout}$ ” is the measured total output noise power. In order to use this method, the gain of the DUT should be predetermined. To measure the  $P_{Nout}$ , the input of the DUT is terminated with the  $50 \Omega$  impedance, and then the output noise power density is measured with the spectrum analyzer.

In the Y-factor method, which is a popular method for the noise figure measurement, a noise source with known ENR (Excess Noise Ratio) is needed. The setup and noise source calibration for the Y-factor method measurement are shown in Fig. 6.18. The ENR accuracy of the noise source contributes heavily to the accuracy of the noise figure measurement. The ENR values are provided by the manufacturer under matching condition. Consequently, any mismatch introduces significant ENR inaccuracies. The noise figure in this method is measured by

$$NF_{Y-method} = 10 \log \left( \frac{10^{(ENR/10)}}{10^{(Y/10)} - 1} \right) \quad (\text{Eq. 6.27})$$

Since the noise power is proportional to the noise temperature, it can be written as;

$$Y = \frac{T^{ON}}{T^{OFF}} \quad (\text{Eq. 6.28})$$

where Y is the ratio of the output noise power density when the noise source is on and off.

In the last method, the noise figure meter generates a pulse signal to drive a noise source, which is applied to the DUT. The output of the DUT is then measured with the noise figure analyzer. Since the input noise and signal-to-noise ratio of the noise source is known to the analyzer, the noise figure of the DUT can be calculated internally and displayed.

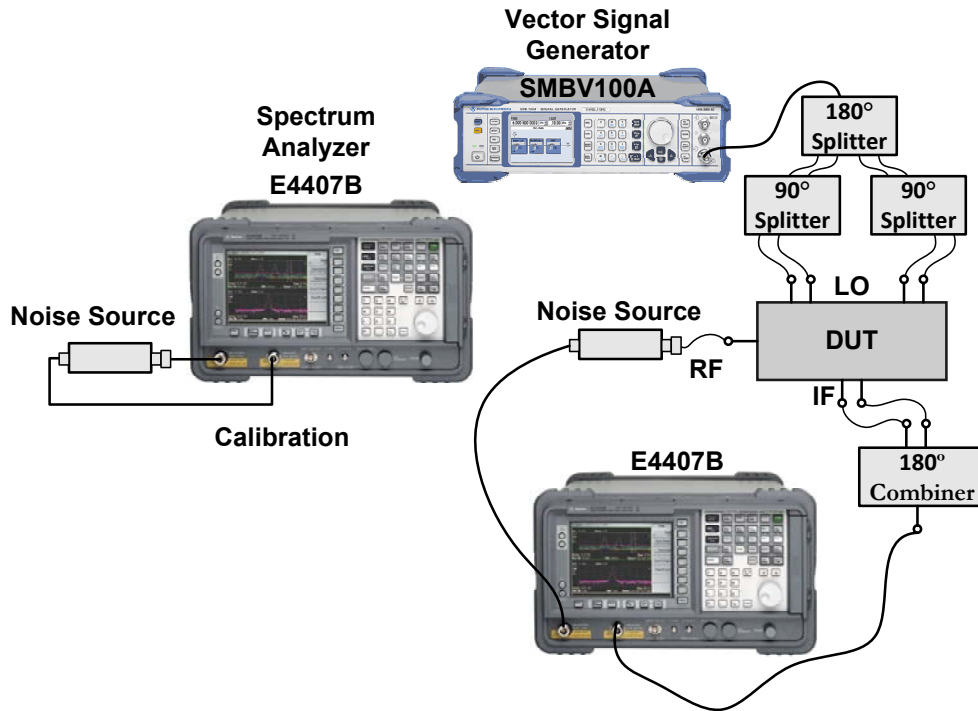


Figure 6.18: Y-factor method in noise figure measurement setup.

In the receiver front-end measurement, the noise figure was measured both by the gain method and Y-factor method. However, since in the Y-factor method an accurate wideband noise source at low frequency is hard to find, we mostly relied on the gain-method for the noise figure measurement.

## 6.6 Summary

A half-RF technique is employed in the design of a 3–8 GHz receiver front-end. The single stage low power single-to-differential LNA eliminated the need for an off-chip balun and increases the integrity level of the front-end receiver. Using the proposed technique, a good linearity and IIP2 was achieved by the receiver front-end. The reduction in flicker noise helps to improve the lower frequency noise figure, which is discussed above. A good LO-RF isolation restricts the leakage of the unwanted signals to the RF port,

which reduces the second-order harmonic distortion, without the need for extra circuit implementation.

# Chapter 7

## Conclusions and Recommendations

### 7.1 Conclusions

The high demands for fourth-generation wireless communications systems, especially UWB systems, has attracted the researchers. Nowadays, the UWB systems are more attractive due to their low complexity, high data rate, low power consumption, and robustness to interference. The most important characteristic of the UWB is the capability of operating in low power regime (transmit power of -41.3 dBm). The UWB wireless standard allows the system to operate at very low signal-to-noise ratios with high bandwidth. This means that the UWB system is able to achieve high data rate with relatively low transmit power, which is desirable for low power applications.

Several wideband low-noise amplifier architectures, as well as their advantages and disadvantages are discussed. After reviewing the conventional wideband amplifiers, it is found that a new architecture is needed to reduce the number of components (particularly inductors), to increase the level of integration, and to be suitable for low-cost standard CMOS technology. Therefore, a novel approach is proposed based on the T-coil peaking network. Comprehensive analysis to design the T-coil peaking network is explored, which allows the designers to know the steps of the multi-resonance network implementation. The trade-offs and susceptibility of the low-noise amplifier to the process variations in a wide range of frequency are explained. The proposed architecture is applied in the

design of a single stage LNA at 3–8 GHz frequency, to realize the wideband LNA. The proposed LNA is fabricated in 0.18  $\mu\text{m}$  CMOS technology, and it is tested on-wafer. The wideband LNA has a maximum gain of 16.4 dB, and achieves a NF of 2.9–4.66 dB, while consumes 2.16 mA from the 1.8 V power supply.

Based on the knowledge of the passive and active mixers, it is concluded to use an active mixer for the wideband receiver front-end, to achieve high gain and low-noise characteristics. The challenges to design a proper mixer are explored, and the issues facing the direct-conversion receiver architecture are explained. The possible solution without paying for extra circuit implementation and power consumption is proposed. Unlike the conventional direct-conversion architecture, a two-stage down-conversion mixer topology is utilized in the receiver front-end to relax some issues regarding the direct-conversion architecture. This architecture alleviates the leakage problem at LO frequency at the input of the LNA (RF input). A simple analysis on the nonlinearity intermodulations of the mixer is performed. This analysis shows that, as the proposed technique reduces the coupling between the ports, the nonlinearity intermodulations are reduced. Consequently, higher linearity and IIP2 are obtained.

Finally, the proposed single stage LNA with single-ended output is further improved to a differential output architecture without consuming extra current consumption, to make it compatible for integration with the proposed mixer. The wideband single-to-differential LNA is integrated with the two stage down-conversion mixer to down-convert the RF frequency to the baseband. The whole receiver front-end is fabricated in 0.18  $\mu\text{m}$  CMOS technology, and tested on wafer. It consumes less than 8 mW power, excluding testing buffer, from a 1.8 V power supply. The measured NF is 5.4–8.3 dB from 3–8 GHz frequency, with a maximum gain of 36.1 dB.

## 7.2 Recommendations

The design of the receiver front-end will not be complete without wideband phase-locked loop (PLL) circuit. The use of half-RF frequency for the LO, makes the design of the PLL more relaxed and reduces the power consumption. The next step for this work is to design a wideband PLL, which is very challenging and it should cover a wide range of frequency.

In addition, there are other blocks, which need to be explored further, such as a high speed and resolution analog-to-digital converter, wideband synthesizer, and wideband baseband filter. Since a wideband frequency is covered in the UWB system, high robustness to interference, low-complexity receiver/transmitter and low energy consumption are the important concepts to develop for future research. Finally, the integration of all these building blocks is very important to make all the blocks compatible.

# Author's Publications

1. **A. Meamar**, C. C. Boon, M. A. Do, and K. S. Yeo, "A 3–8 GHz low-noise CMOS amplifier," *Microwave and Wireless Components Letters, IEEE*, vol. 19, pp. 245–247, April 2009.
2. **A. Meamar**, C. C. Boon, D. M. Anh, and Y. K. Seng, "A Wideband Low Power Low-Noise Amplifier in CMOS Technology," *IEEE Transactions on Circuits and Systems I: Reg. Papers*, vol. 57, pp. 773–782, April 2010.
3. **A. Meamar**, C. C. Boon, Shi Xiaomeng, Lim Wei Meng, Do Manh Anh, and Y. K. Seng, "A Single-Ended Ultra-Wideband Receiver Front-End Employing Two-Stage Down-Conversion Mixer," *Accepted in ISCAS 2011, International Symposium on Circuit and Systems*.

# Bibliography

- [1] T. Terada, S. Yoshizumi, M. Muqsith, *et al.*, “A CMOS ultra-wideband impulse radio transceiver for 1-Mb/s data communications and  $\pm 2.5$ -cm range finding,” *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 891–898, 2006.
- [2] S. Shekhar, J. Walling, and D. Allstot, “Bandwidth extension techniques for CMOS amplifiers,” *IEEE J. Solid-State Circuits*, vol. 41, pp. 2424–2439, Nov. 2006.
- [3] D. Cassan and J. Long, “A 1-V transformer-feedback low-noise amplifier for 5-GHz wireless LAN in 0.18- $\mu$ m CMOS,” *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 427–435, 2003.
- [4] A. Bevilacqua and A. Niknejad, “An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers,” *IEEE J. Solid-State Circuits*, vol. 39, pp. 2259–2268, Dec. 2004.
- [5] J. Crols and M. Steyaert, “A 1.5 GHz highly linear CMOS downconversion mixer,” *IEEE J. Solid-State Circuits*, vol. 30, pp. 736–742, Jul 1995.
- [6] C. Keys, *Low-distortion mixers for RF communications*. PhD thesis, University of California, Berkeley, 1994.
- [7] D. Manstretta, M. Brandolini, F. Svelto, *et al.*, “Second-order intermodulation mechanisms in CMOS downconverters,” *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 394–406, 2003.

- [8] H. Darabi and A. Abidi, "Noise in RF-CMOS mixers: a simple physical model," *IEEE J. Solid-State Circuits*, vol. 35, pp. 15–25, Jan 2000.
- [9] A. Batra, J. Balakrishnan, G. Aiello, *et al.*, "Design of a multiband OFDM system for realistic UWB channel environments," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 2123–2138, Sept. 2004.
- [10] G. Ross, *The transient analysis of multiple beam feed networks for array systems*. PhD thesis, Ph.D. dissertation, Polytechnic Institute of Brooklyn, Brooklyn, NY, 1963.
- [11] S. Roy, J. Foerster, V. Somayazulu, *et al.*, "Ultrawideband radio design: the promise of high-speed, short-range wireless connectivity," *Proceedings of the IEEE*, vol. 92, no. 2, pp. 295–311, 2004.
- [12] R. Scholtz, R. Weaver, E. Homier, *et al.*, "UWB radio deployment challenges," *The 11th IEEE International Symposium on Personal, Indoor and Mobile Radio Communications. PIMRC.*, vol. 1, 2000.
- [13] B. Razavi, T. Aytur, C. Lam, *et al.*, "A UWB CMOS Transceiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555–2562, 2005.
- [14] A. Batra, J. Balakrishnan, A. Dabak, *et al.*, "Multi-band OFDM physical layer proposal for IEEE 802.15 task group 3a," *IEEE P802.15-03/268r1-TG3a*, pp. 365–368, 2004.
- [15] G. Aiello, G. Rogerson, D. Commun, *et al.*, "Ultra-wideband wireless systems," *IEEE Microwave Magazine*, vol. 4, no. 2, pp. 36–47, 2003.
- [16] E. Kwerel, J. Williams, U. S. F. C. C. O. of Plans, and Policy, *A Proposal for a Rapid Transition to Market Allocation of Spectrum*. Federal Communications Commission, Office of Plans and Policy, 2002.

- [17] J. Foerster, "IEEE P802. 15 working group for wireless personal area networks (WPANs), channel modeling subcommittee report-final," 2003.
- [18] S. Stroh, "Ultra-wideband: Multimedia unplugged," *IEEE Spectrum*, vol. 40, no. 9, pp. 23–27, 2003.
- [19] G. Chien, W. Feng, Y. Hsu, *et al.*, "A 2.4 GHz CMOS transceiver and baseband processor chipset for 802.11 b wireless LAN application," *Digest of International Solid-State Circuits Conference, ISSCC.*, pp. 358–499, 2003.
- [20] W. Jones, "No place to hide [radar devices]," *IEEE Spectrum*, vol. 42, no. 11, pp. 20–21, 2005.
- [21] A. Batra, J. Balakrishnan, G. Aiello, *et al.*, "Design of a multiband OFDM system for realistic UWB channel environments," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, no. 9 Part 1, pp. 2123–2138, 2004.
- [22] R. Roovers, D. Leenaerts, Bergervoet, *et al.*, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2563–2572, 2005.
- [23] B. Razavi, "A 5.2-GHz CMOS receiver with 62-dB image rejection," *IEEE J. Solid-State Circuits*, vol. 36, no. 5, pp. 810–815, 2001.
- [24] Shuzuo Lou, Hui Zheng, and Luong, H.C., "A 1.5-V CMOS receiver front-end for 9-band MB-OFDM UWB system," *IEEE Custom Integrated Circuits Conference*, pp. 801–804, Sept. 2006.
- [25] C. Liao and S. Liu, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE J. Solid-State Circuits*, vol. 42, pp. 329–339, Sept. 2007.

- [26] T. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge University Press Cambridge, 1998.
- [27] A. Yazdi, D. Lin, and P. Heydari, "A 1.8 V three-stage 25GHz 3dB-BW differential non-uniform downsized distributed amplifier," in *Solid-State Circuits Conference, IEEE ISSCC Dig. Tech. Papers*, pp. 156–590, 2005.
- [28] S. Mohan, M. Hershenson, S. Boyd, *et al.*, "Bandwidth extension in CMOS with optimized on-chip inductors," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 346–355, 2000.
- [29] H. Bode, *Network analysis and feedback amplifier design*. Van Nostrand Reinhold, 1956.
- [30] R. Fano, "Theoretical limitations on the broadband matching of arbitrary impedances," *Journal of the Franklin Institute*, vol. 249, no. 1, pp. 57–83, 1950.
- [31] B. Perumana, J.-H. Zhan, S. Taylor, *et al.*, "Resistive-Feedback CMOS Low-Noise Amplifiers for Multiband Applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, pp. 1218–1225, May 2008.
- [32] A. Meaamar, C. C. Boon, M. A. Do, *et al.*, "A 3–8 GHz low-noise CMOS amplifier," *Microwave and Wireless Components Letters, IEEE*, vol. 19, pp. 245–247, April 2009.
- [33] D. Feucht, *Handbook of Analog Circuit Design*. San Diego, CA: Academic, ch. 8., 1990.
- [34] J. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1382, 2000.

- [35] Y. Cui, G. Niu, and S. Taylor, "On the relations between Y- and H-noise representations in MOSFETs and importance of noise source correlation," *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, p. 4, Jan. 2006.
- [36] A. Scholten, L. Tiemeijer, R. van Langevelde, *et al.*, "Noise modeling for RF CMOS circuit simulation," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 618–632, 2003.
- [37] G. Banerjee, K. Soumyanath, and D. Allstot, "Desensitized CMOS low-noise amplifiers," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 55, pp. 752–765, April 2008.
- [38] J. Zhan and S. Taylor, "A 5GHz resistive-feedback CMOS LNA for low-cost multi-standard applications," *IEEE ISSCC Dig. Tech. Papers*, pp. 721–730, 2006.
- [39] C. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF ICs," *IEEE J. Solid-State Circuits*, vol. 33, pp. 743–752, May 1998.
- [40] A. Ismail and A. Abidi, "A 3-10 GHz low-noise amplifier with wideband LC-ladder matching network," *IEEE J. Solid-State Circuits*, vol. 39, pp. 2269–2277, April 2004.
- [41] K.-H. Chen, J.-H. Lu, B.-J. Chen, *et al.*, "An ultra-wide-band 0.4-10 GHz LNA in 0.18- $\mu\text{m}$  CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, pp. 217–221, March 2007.
- [42] Y.-J. Chen and Y.-I. Huang, "Development of integrated broad-band CMOS low-noise amplifiers," *IEEE Trans. Circuits and Sys. I: Regular Papers*, vol. 54, pp. 2120–2127, Oct. 2007.
- [43] H. Zhang, X. Fan, and E. Sinencio, "A low-power, linearized, ultra-wideband LNA design technique," *IEEE J. Solid-State Circuits*, vol. 44, pp. 320–330, Feb. 2009.

- [44] P. Heydari, "Design and analysis of a performance-optimized CMOS UWB distributed LNA," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1892–1905, Sept. 2007.
- [45] S. Blaakmeer, E. Klumperink, D. Leenaerts, *et al.*, "Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1341–1350, June 2008.
- [46] D. Im, I. Nam, H.-T. Kim, *et al.*, "A Wideband CMOS low noise amplifier employing noise and IM2 distortion cancellation for a digital TV tuner," *IEEE J. Solid-State Circuits*, vol. 44, pp. 686–698, March 2009.
- [47] W.-H. Chen, G. Liu, B. Zdravko, and others., "A highly linear broadband CMOS LNA employing noise and distortion cancellation," *IEEE J. Solid-State Circuits*, vol. 43, pp. 1164–1176, May 2008.
- [48] M. Reiha and J. Long, "A 1.2 V reactive-feedback 3.1-10.6 GHz low-noise amplifier in 0.13- $\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuits*, vol. 42, pp. 1023–1033, June 2007.
- [49] B. Gilbert, "A precise four-quadrant multiplier with subnanosecond response," *IEEE J. Solid-State Circuits*, vol. 12, no. 4, pp. 358 – 499, 2002.
- [50] S. Chehrazi, R. Bagheri, and A. Abidi, "Noise in passive FET mixers: a simple physical model," in *Proc. of Custom Integrated Circuits Conference*, pp. 375–378, 2004.
- [51] E. Sacchi, I. Bietti, S. Erba, *et al.*, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Proc. of Custom Integrated Circuits Conference*, pp. 459–462, Citeseer, 2003.
- [52] M. Valla, G. Montagna, R. Castello, *et al.*, "A 72-mW CMOS 802.11 a Direct Conversion Front-End With 3.5-dB NF and 200-kHz Noise Corner," *IEEE J. Solid-State Circuits*, vol. 40, no. 4, pp. 970–977, 2005.

- [53] B. Toole, C. Plett, and M. Cloutier, "RF circuit implications of moderate inversion enhanced linear region in MOSFETs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 51, no. 2, pp. 319–328, 2004.
- [54] L. Sheng, J. Jensen, and L. Larson, "A wide-bandwidth Si/SiGe HBT direct conversion sub-harmonic mixer/downconverter," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 9, pp. 1329–1337, 2000.
- [55] S. Laursen, "Second order distortion in CMOS direct conversion receivers for GSM," in *Proceedings of 25th European Solid-State Circuits Conference*, pp. 342–345, 1999.
- [56] W. Sansen, "Distortion in Elementary Transistor Circuits," *IEEE Transaction on Circuit and Systems-II: Analog and Digital Signal Processing*, vol. 46, no. 3, pp. 315–325, 1999.
- [57] I. Elahi, K. Muhammad, and P. Balsara, "IIP2 and DC offsets in the presence of leakage at LO frequency," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 8, pp. 647–651, 2006.
- [58] S. Chehrazi, A. Mirzaei, and A. Abidi, "Noise in Current-Commutating Passive FET Mixers," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, pp. 332–344, Feb. 2010.
- [59] C. Sandner, S. Derksen, D. Draxelmayr, *et al.*, "A WiMedia/MBOA-Compliant CMOS RF Transceiver for UWB," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2787–2794, Dec. 2006.
- [60] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, pp. 428–435, Jun 1997.

- [61] E. Bautista, B. Bastani, and J. Heck, "A high IIP2 downconversion mixer using dynamic matching," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1934–1941, 2002.
- [62] Y. Li, C. Wu, A. Sangiovanni-Vincentelli, and J. Rabaey, "Design and optimization of an mb-ofdm ultra-wideband receiver front-end," *ICCSC08 Proceedings*, pp. 502–506, 2008.
- [63] K. W. Tang, S. Leung, N. Tieu, *et al.*, "Frequency Scaling and Topology Comparison of Millimeter-wave CMOS VCOs," in *IEEE Compound Semiconductor Integrated Circuit Symposium, CSICS.*, pp. 55–58, Nov. 2006.
- [64] J. Cavers and M. Liao, "Adaptive compensation for imbalance and offset losses in direct conversion transceivers," *IEEE Transactions on Vehicular Technology*, vol. 42, pp. 581–588, Nov. 1993.
- [65] D. Kaczman, M. Shah, M. Alam, *et al.*, "A SingleChip 10-Band WCDMA/HSDPA 4-Band GSM/EDGE saw-less CMOS Receiver With DigRF 3G Interface and +90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, pp. 718–739, March 2009.
- [66] S. Kang, B. Choi, and B. Kim, "Linearity analysis of CMOS for RF application," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, no. 3, pp. 972–977, 2003.
- [67] "EE215C lecture series, UCLA."
- [68] B. Razavi, *RF microelectronics*. Prentice Hall PTR Upper Saddle River, NJ, 1998.
- [69] S. Chehrazi, A. Mirzaei, and A. Abidi, "Second-Order Intermodulation in Current-Commutating Passive FET Mixers," *IEEE Trans. Circuits Syst. I: Regular Papers*, vol. 56, pp. 2556–2568, Dec. 2009.

- [70] A. Safarian, L. Zhou, and P. Heydari, "A Distributed RF Front-End for UWB Receivers," in *Custom Integrated Circuits Conference, CICC, IEEE*, pp. 805–808, sept. 2006.
- [71] B. Shi and M. Chia, "A CMOS ESD-protected RF front-end for UWB receiver," in *in Proc. of European Solid State Conference.*, pp. 252 –255, sept. 2009.
- [72] G. Cusmai, M. Brandolini, P. Rossi, *et al.*, "A 0.18- $\mu\text{m}$  CMOS Selective Receiver Front-End for UWB Applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 8, pp. 1764–1771, 2006.
- [73] C. Sandner, S. Derksen, D. Draxelmayr, *et al.*, "A WiMedia/MBOA-Compliant CMOS RF Transceiver for UWB," *IEEE J. Solid-State Circuits*, vol. 41, pp. 2787–2794, Dec. 2006.
- [74] A. Einstein, *Investigations on the Theory of Brownian Movement*. New York: Dover, 1956.