A 16 mW 1 GS/s 49.6 dB SNDR TI-SAR ADC for Software Defined Radio in 65 nm CMOS

Lei Qiu, Kai Tang, Yuanjin Zheng, *Senior Member, IEEE*, Liter Siek, *Senior Member, IEEE*, Yan Zhu, *Member, IEEE* and Seng-Pan U, *Fellow, IEEE*

***Abstract*—This paper presents a 10-bit 1 GS/s 4-channel time-interleaved (TI) successive approximation register (SAR) analog-to-digital converter (ADC). To suppress the time skew, the full rate master clock based sampling technique is adopted. The effect of sampling switch mismatches on time skew is addressed. The measured time skew spurs caused by the sampling switch mismatches are around -52~ -55 dB at Nyquist input. Then, a tap-interpolating fractional delay (TIFD) filters based digital background time skew calibration technique is proposed. Also, a full analysis of the effects of the various parameters on the time-skew-generated spur levels is presented, which indicates that the time skew error level is related to the length of calibration filters, calibration range and bandwidth penalty. The sub-channel ADC exploits a 250 MS/s SAR ADC with a low cost high-speed sub-radix-2 searching technique. The reference interference of non-binary TI ADCs is discussed and tolerated by the sub-radix-2 searching scheme. The proposed adders based encoding circuit is optimized with lower propagation delay to meet high-speed requirements. The prototype was fabricated in a 65 nm CMOS technology. The measurement results show that the ADC achieves an SNDR of 49.6 dB with a power of 15.95 mW and a figure of merit (FoM) of 63 fJ/conversion-step when operating at 1 GS/s and 458.1 MHz Nyquist input. The ADC core achieves an area of 0.158 mm^2.**

***Index Terms*— digital background calibration, SAR ADCs, sub-radix-2, time-interleaved, time skew.**

I. Introduction

THE scaling of CMOS technology has fuelled the emergence of high performance analog-to-digital converters (ADCs) with lower power consumption and smaller silicon area [1]-[6]. The power and area efficient high-performance ADCs, instead of traditional ADCs with hundreds of milliwatts power consumption [7]-[11], facilitate software defined radio (SDR) and wideband communication implementations. Also, portable testing instruments (e.g., portable oscilloscopes, spectrum analyzers) could be further developed by leveraging such low-power high performance ADCs.

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It is known that pipelined ADCs are suitable for implementations with high-resolution and high speed sampling at gigahertz frequencies [12]-[15]. However, to achieve low power consumption, power efficient amplifiers are needed. Some techniques were reported [15]-[19] to overcome the design challenges (low intrinsic device gain and low power supply). However, the calibration techniques introduce complicated circuits requiring additional silicon area and power consumption [15]. SAR ADCs are power and area efficient [1]-[6]. However, due to the serial comparison nature and accuracy requirement for each comparison cycle, the sampling rates of prior high speed SAR ADCs [1], [20], [21] are limited. Complex arithmetical units based sub-radix-2 algorithm has been discussed in [32], [35]. They were not suitable for high speed implementations due to the long SAR logic loop propagation delay. To achieve higher sampling rate with SAR architecture, time-interleaved (TI) SAR ADCs were presented [5], [9]-[11], [22]-[24]. However, the power and area overhead in terms of clock distribution increase heavily. The power efficiency of a 24-way TI SAR ADC in [24] was improved as compared with traditional TI ADCs [9]-[11]. However, the time-interleaving overhead of clock distribution is still non-negligible. Another 8-way TI SAR ADC [22] consumes large area of 0.78 mm^2 with off-chip timing calibration, with one flash ADC degrading the system power efficient. The state-of-the-art TI SAR ADC [23] with fully digital background time skew calibration utilized the differentiating FIR filter to estimate and compensate the timing offset, which consumes large power and has large bandwidth penalty.

In this work, we present a 1 GS/s 10-bit four-channel time-interleaved SAR ADC consuming only 15.95mW power and 0.158 mm^2 core area [40]. To constrict the time skews in a small range, a time skew suppressed sampling technique with full rate clock for TI ADCs is utilized and the mismatch of sampling switches is considered. To further compensate the time skew, a tap-interpolating fractional delay (TIFD) FIR correction filter based calibration technique is proposed, which consumes less computation units and drops less bandwidth in digital domain. A full analysis of parameter effect on time skew spurs is presented, which indicates that the time skew error level is related to the length of calibration filters (interpolation filter and fractional delay filter), calibration range and bandwidth penalty. Additionally, the reference interference in redundant TI SAR ADC is addressed. This work implements a high-speed sub-radix-2 searching technique, with only adder based encoding scheme for SAR ADCs. The proposed adders

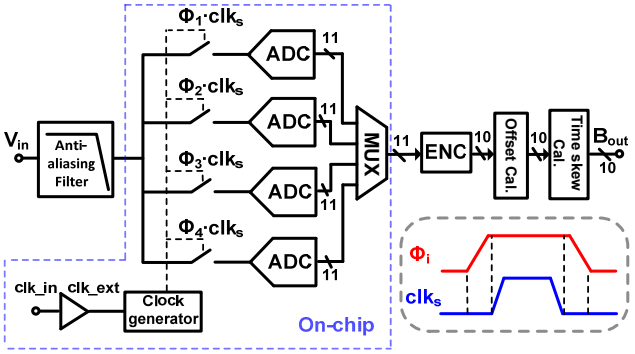


Fig. 1. Proposed architecture of the four-channel TI-ADC with sampling rate at 1 GS/s.

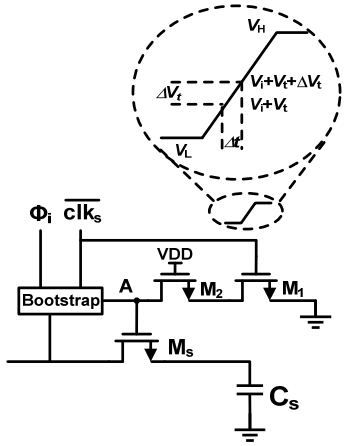


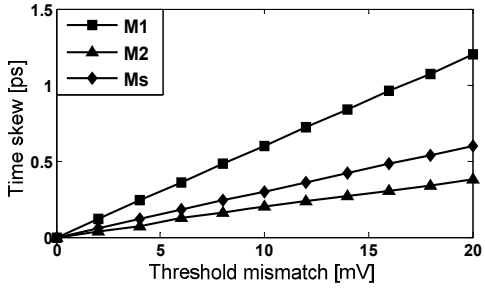
Fig. 2. Effect of threshold mismatch on time skew.

based encoding circuit is optimized with lower propagation delay to meet high-speed requirement.

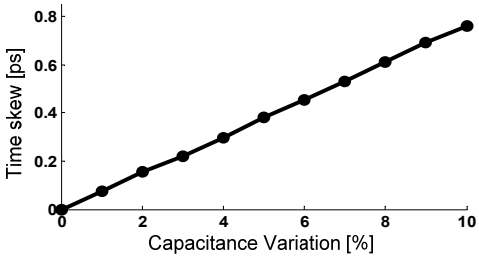
The paper is organized as follows. Section II introduces the proposed TI SAR ADC architecture, including sampling scheme, sub-radix-2 high speed sub-SAR ADC and the proposed digital background time skew calibration technique. The detailed circuit implementations are described in Section III. Section IV shows the measurement results. Finally, the conclusion is drawn in Section V.

II. Proposed TI-ADC Architecture

The overall ADC architecture is shown in Fig. 1, which consists of four sub-SAR ADCs operating at 250 MS/s with total 1 GS/s [40]. An anti-aliasing filter, which is implemented off-chip, is inserted in front of the ADC to filter noise and interference out of the band of interest. To reduce the time skew, the sampling instant of each channel is only determined by the falling edge of the 1 GS/s master clock clk_s, while the corresponding TI clock signals Φ_i (i=1, 2, 3, 4) are used to perform the channel selection [13]. In sub-ADCs, one redundant bit is implemented in the proposed sub-radix-2 searching technique. After multiplexing, the digital outputs are decimated by a factor of 45 for testing purpose. The selection of decimation factor should equal $n{\cdot}M$+1 to ensure the decimated output rotating equally across all interleaved channels. Variable n is an integer and the M is the number of channels. The decimated outputs of ADC are followed by an encoding circuit



(a)



(b)

Fig. 3. The relation between time skew and (a) offset of transistors M_1, M_2 and Ms (b) capacitance variation at node A.

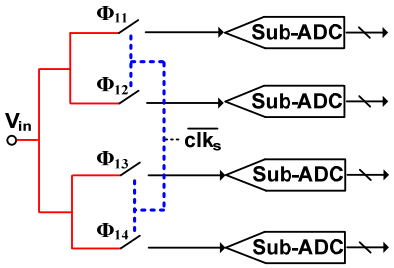


Fig. 4. Layout guidance of input and clock signal for the four-channel TI ADC.

(ENC) to encode the outputs from 11-bit to 10-bit. The offset errors are extracted and compensated by averaging and accumulation in digital domain [7].

A. Sampling Network

Although each channel is sampled by the same clock signal clk_s, there are still some time skew error sources, including threshold mismatches of the sampling switches (transistor M_1, M_2, Ms in Fig. 2) and size mismatches after fabrication. The effect of threshold mismatch of transistor M_1 is explained in Fig. 2. The time skew Δt can be derived as

$$\Delta t = \frac{t_{fall}}{V_H - V_L}\Delta V_t , \quad (1)$$

where t_{fall} is the falling (rising) time of the clock. From (1), it can be concluded that making the falling edge sharper and reducing threshold mismatch ΔV_t of transistor M_1 could decrease the time skew. To reduce threshold mismatches of sampling switches (transistor M_1, M_2, Ms) shown in Fig. 2, the size of sampling switch could be increased properly according to [36], which states that the standard deviation of threshold mismatch is

$$\sigma_{\Delta V_t} = \frac{A_{V_t}}{\sqrt{WL}} , \quad (2)$$

where A_{Vt} is the matching constant. To evaluate the effect of process variation on time skew, we set the falling time of clk_s as 70 ps, the size of M_1 and M_2 as 4 μm/60 nm and the size of the Ms as 15 μm/60 nm. The simulation results of threshold mismatch and capacitance mismatch at node A (Fig. 2) versus time skew are illustrated in Fig. 3, where M_1 has a more significant effect on time skew. The time skew is proportional to the capacitance variation at node A. To suppress the error caused by unmatched routing, the routing of clock signal clk_s and input signal V_{in} are illustrated in Fig. 4. The "binary tree" connection is utilized to guarantee the routings of clk_s and V_{in} to each channel identical. Assuming that the time skew error is treated as Gaussian distributed variable, the relation between SNDR and time skew standard deviation σ_t with given input frequency f_{in} is [37]

$$SNDR = 20\log\frac{1}{2\pi f_{in}\sigma_t} - 10\log\left(\frac{M-1}{M}\right), \tag{3}$$

Therefore, to satisfy an SNDR of 60 dB at a 500 MHz input frequency, the time skew deviation σ_t between channels should be less than 0.37 ps, which is difficult to achieve without additional calibration even with perfect matching layout.

B. TIFD Filters based Time Skew Calibration

Fractional delay filters (FDF) [27], [28] could be utilized to compensate the time skew error in digital domain. Supposing T is the overall ADC sampling period, and $T_d=\alpha T$ represents the fractional delay, where α is the normalized fractional delay. Because of the presented time skew suppressed sampling technique, the range of fractional delay in this design could be constrained into [-0.002T, +0.002T]. The calibration of time skew is divided into two parts: detection and correction. The time skew detection technique in [29] is employed, which compares the mean value (by accumulation and average) of the multiplication of signals $x_m(n)$ (m=0, 1, 2, …, M-1) in two adjacent channels to detect the polarity of time skew error $p(t_m)$ and updates the coefficients of fractional delay FIR filter $F(a_m)$ adaptively as shown in Fig. 5 [40]. For time skew correction, the proposed fractional delay FIR filter architecture is shown in Fig. 6, where only the second-channel (m=1) is illustrated and the length of FIR correction filter is 2N+1 (N=2, 4, …) (N=2 in Fig. 6). The α indicates the time error to be calibrated. C =[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, $c_{2,0}$, $c_{2,1}$, $c_{3,0}$, $c_{3,1}$, $c_{4,0}$, $c_{4,1}$] are the coefficients of fractional delay filters. $I_{m,m+1}(n)$ is the interpolation filter (IF) to generate the interpolated tap between channel m and channel m+1. The input of the IF is the sampled raw data from the all sub-channels.

To update the coefficients of the fractional delay filters with the detected time skew error α, the coefficients are approximated by first-order polynomials of α (shown in Fig. 6). The approximation error is

$$e(\omega,\alpha) = F(\omega,\alpha) - D(\omega,\alpha), \tag{4}$$

where

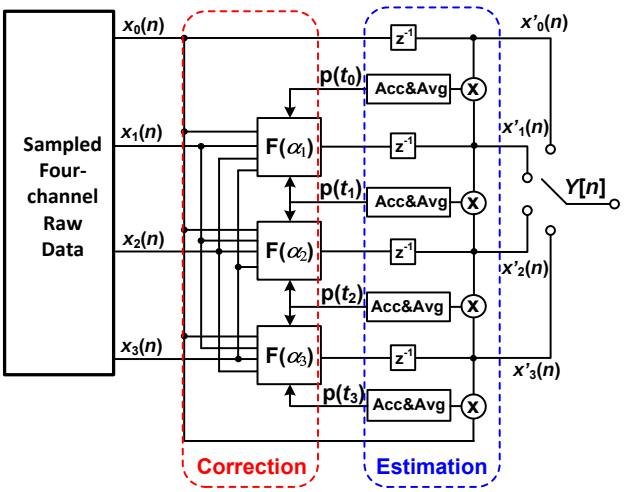


Fig. 5. The calibration architecture for the time skew error.

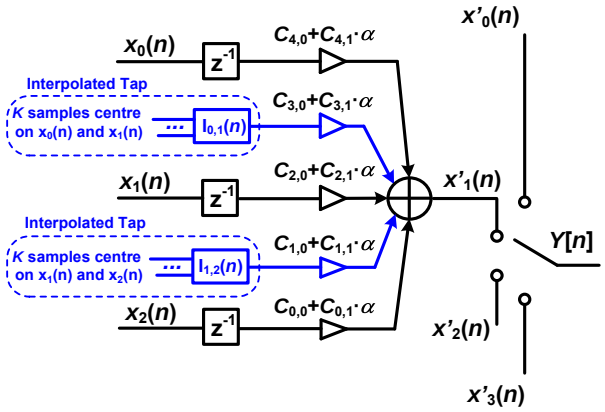


Fig. 6. The structure of FIR correction filter of a sub-channel with N=2 and M=4.

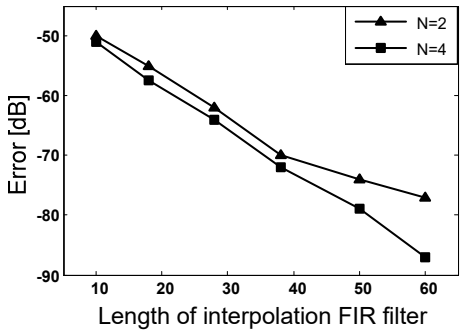


Fig. 7. Error level versus the length of interpolation FIR filters (Bandwidth penalty=5%, calibration range is [-0.002T, 0.002T]).

$$F(\omega,\alpha) = \sum_{n=0}^{N}(c_{2n,0}+\alpha c_{2n,1})e^{-j\omega(n+\frac{K-N}{2})T} + \sum_{n=0}^{N-1}(c_{2n+1,0}+\alpha c_{2n+1,1})\sum_{k=0}^{K-1}e^{-j\omega(k+n)T} \tag{5}$$

and

$$D(\omega,a) = e^{-j\omega(\alpha+\frac{K}{2})T}. \tag{6}$$

$F(\omega,\alpha)$ and $D(\omega,\alpha)$ are the transfer function of the TIFD filter and the ideal fractional delay function, respectively. Variable K (K=2, 4, …) is the length of IF. For the ideal fractional delay

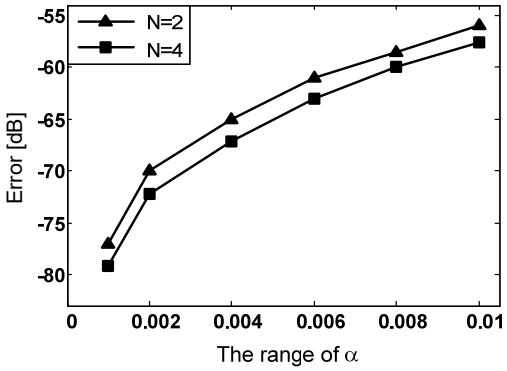


Fig. 8. Error level versus the range of fractional delay α (Bandwidth penalty=5%, length of IF=38-tap).

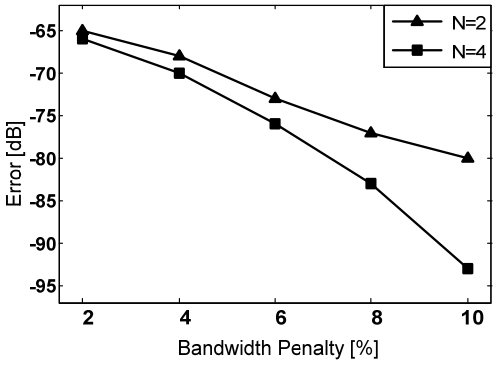


Fig. 9. Error level versus the bandwidth penalty. (Length of IF=38-tap, calibration range is [-0.002T, 0.002T]).

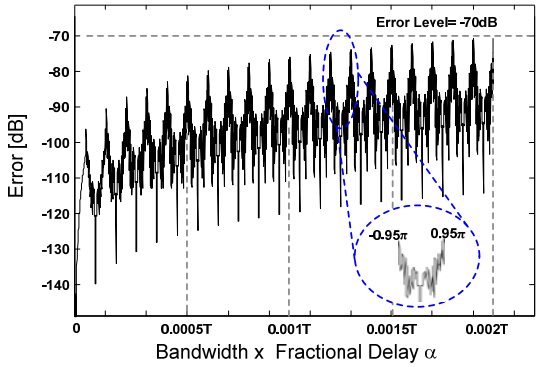


Fig. 10. Optimized error level versus bandwidth x fractional delay. (Length of IF=38-tap, length of FDF=5-tap, Bandwidth penalty=5%, calibration range is [-0.002T, 0.002T]).

filter, α and $K/2$ are the fractional (time skew) and integral delay (middle-tap of IF) respectively. The coefficients of FDF $C_{n,m}=[c_{0,0}, c_{0,1}, c_{1,0}, c_{1,1}, \ldots, c_{2N,0}, c_{2N,1}]$, whose length is $4N+2$, are to be optimized. The transfer function $F(\omega,\alpha)$ of the FIR filter can be rewritten as [43]

$$F(\omega,a)=C_{n,m}\cdot(c(\omega,a)-js(\omega,a))^{\mathrm{T}} \tag{7}$$

where

$$c(\omega)=[\cos(\frac{K-2}{2}\omega), a\cos(\frac{K-2}{2}\omega), \sum_{k=0}^{K-1}\cos(k\omega), a\sum_{k=0}^{K-1}\cos(k\omega), \ldots$$
$$\sum_{k=0}^{K-1}\cos((k+N-1)\omega), a\sum_{k=0}^{K-1}\cos((k+N-1)\omega), \cos((\frac{K}{2}-1+N)\omega),$$
$$a\cos((\frac{K}{2}-1+N)\omega)]$$

TABLE I PERFORMANCE COMPARISON OF DIGITAL CALIBRATION

	Filter Length (taps)	Bandwidth Penalty	Error (dB)	Adaptive	Cal. Range
[25]	60	10%	-72	No	0.15T
[26]	75+30	33%	-72	Yes	-
[23]	-	9.25%	-70	No	-
This work	**38+5**	**5%**	**-70**	**Yes**	**0.002T**

and

$$s(\omega)=[\sin(\frac{K-2}{2}\omega), a\sin(\frac{K-2}{2}\omega), \sum_{k=0}^{K-1}\sin(k\omega), a\sum_{k=0}^{K-1}\sin(k\omega), \ldots$$
$$\sum_{k=0}^{K-1}\sin((k+N-1)\omega), a\sum_{k=0}^{K-1}\sin((k+N-1)\omega), \sin((\frac{K}{2}-1+N)\omega),$$
$$a\sin((\frac{K}{2}-1+N)\omega)]$$

The error level of the proposed TIFD filters based time skew calibration technique is related to four parameters, which are the length of IF, the length of FDF, calibration range and bandwidth penalty. Fig. 7 shows the error level versus different lengths of IF. As the length of IF increases, the error level could be achieved by 5-tap (N=2) FDF is limited to be -80 dB. If a 9-tap (N=4) FDF is chosen, the error level could be suppressed to be -90 dB. The error level versus calibration range is illustrated in Fig. 8. It indicates that with smaller the targeted calibration range, the error level could be less. Fig. 9 shows the relation between error level and bandwidth penalty. As the bandwidth penalty increases, the error level could be suppressed significantly. Similar with the scenario in Fig. 7, the error level is limited to be around -80 dB when 5-tap FDF is selected. In this work, the lengths of IF and FDF are set to be 38-tap and 5-tap respectively. And a calibration range of +/-0.002T with 5% bandwidth penalty is selected. The optimization results is shown in Fig. 10. It shows that a -70dB error level could be achieved. The advantage of the proposed calibration technique is that it can achieve background time skew error calibration with shorter tap fractional delay filters and less bandwidth penalty compared to [25] and [26]. Since the tap-interpolation is adopted in fractional correction filter design, it equivalently doubles the Nyquist band. Therefore, a smaller bandwidth penalty could be achieved. To save calibration cost, multiplier-less realization of digital filters [39] is employed. For instance, a 38-tap interpolation filter could be realized by using only 55 adders. The word-length of all the optimized coefficients is 12-bit. As shown in Table I, with 38-tap interpolation filter and 5-tap TIFD filter, a -70dB error level could be obtained with only 5% bandwidth scarified. The coefficients optimization of the 38-tap IF is depicted in Appendix.

C. High Speed Custom Weighted Sub-Radix-2 SAR ADC

To design a 10-bit SAR ADC using conventional binary weighted DAC array, it requires ten conversion cycles with each cycle satisfying the same settling accuracy requirement as

$$V_{\mathrm{ref}}\cdot e^{-t/\tau} < V_{\mathrm{ref}}/2^{M+1}, \tag{8}$$

where M is the resolution of ADC, τ is the RC time constant of DAC settling. It means the required settling time for 10-bit

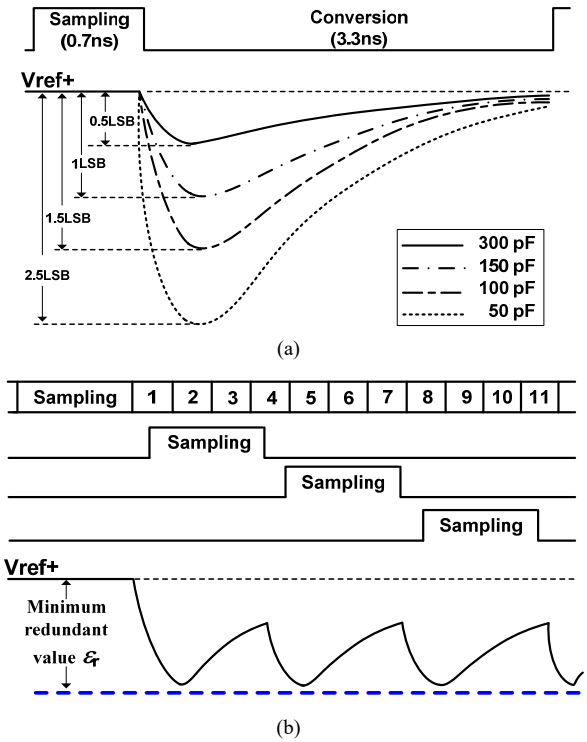


Fig. 11. Reference voltage settling. (a) In single-channel SAR ADC with different decoupling capacitance. (b) In a 4-channel time-interleaved SAR ADC.

resolution is $t > 7.6\tau$. Otherwise, the comparison error occurs. With presence of the custom weighted sub-radix-2 DAC [34], the settling accuracy requirements for the MSBs are significantly relieved. Taking a 4% redundancy range as an example, the required settling time is

$$V_{\text{ref}} \cdot e^{-t/\tau} < 4\% \cdot V_{\text{ref}} \Rightarrow t > 3.2\tau \tag{9}$$

Therefore, the settling time of DAC could be shorter. Due to the large capacitance of MSB branches, the significant drop of reference voltage also can be covered by proper sub-radix-2 weights setting. For a DAC array with a 0.25 pF capacitance and a conversion time of 3.3 ns, it can be seen in Fig. 11(a) that to satisfy the precision requirement of reference voltage recovering in single-channel SAR ADC, the decoupling capacitance C_{dc} between positive and negative of reference voltage should be around 300 pF. With the presence of sub-radix-2 searching, the size of decoupling capacitor could be significantly reduced. Fig. 11(b) shows the reference voltage settling in TI SAR ADC. Since all the sub-channels share the same reference voltage, the conversion phase of any channel will be interrupted by the other channels. The worst case happens at sampling and MSB settling of other channels. The analysis of reference interference on TI SAR ADCs has been addressed in [42]. The reference error caused by sampling and MSB settling could easily influence the conversion of other channels. To tolerate the shared reference voltage interference, the minimum redundant value ε_r should be larger than the maximum reference voltage ripple (shown in Fig. 11(b)), which means

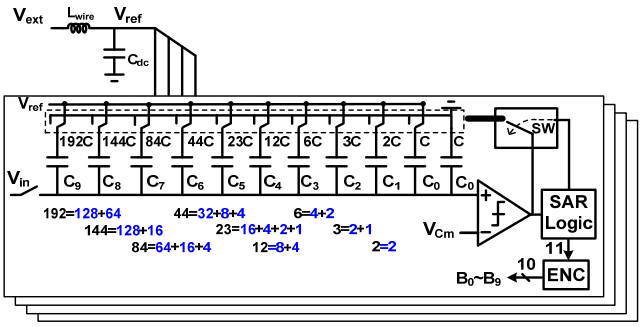
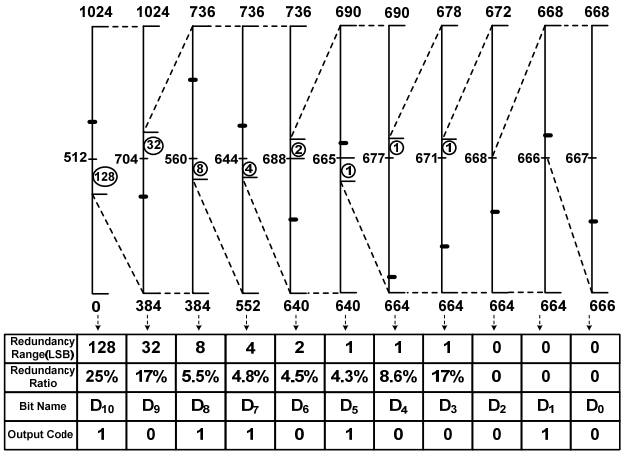


Fig. 12. The sub-radix-2 high speed SAR ADC architecture, where only single-end is shown.



Redundancy Range(LSB)	128	32	8	4	2	1	1	1	0	0	0
Redundancy Ratio	25%	17%	5.5%	4.8%	4.5%	4.3%	8.6%	17%	0	0	0
Bit Name	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Output Code	1	0	1	1	0	1	0	0	0	1	0

Fig. 13. Illustration of the sub-radix-2 algorithm operation with 666.5 LSB input.

$$\frac{C_{DAC}}{C_{\text{dc}}} < \varepsilon_r \,. \tag{10}$$

The redundant value ε_r should cover the sampling phase of all the sub-channels.

In the time-interleaved SAR ADC, the sub-radix-2 weights are embedded into DAC array directly [34], resulting in high speed conversions. The architecture of the sub-radix-2 SAR ADC is shown in Fig. 12. The off-chip reference voltage V_{ext} goes through the bonding wire L_{wire} and is decoupled by C_{dc} to generate V_{ref}. For sub-SAR ADC successive approximation, 11 conversion cycles are needed including one redundant bit. The sub-radix-2 weights D_{10}~D_0 are

$$\begin{aligned} D_{10} &= 2^9 - d_1 \\ D_9 &= 2^8 + \frac{d_1}{2} - d_2 \\ D_8 &= 2^7 + \frac{d_1}{2^2} + \frac{d_2}{2} - d_3 \\ &\cdots\cdots \\ D_0 &= 2^{-1} + \frac{d_1}{2^{10}} + \frac{d_2}{2^9} + \ldots + \frac{d_{10}}{2} - d_{11} \end{aligned} \quad , \tag{11}$$

which are 384, 288, 168, 88, 6, 24, 12, 6, 4, 2, 1 [34]. The redundancy ratios of the all the cycles are set to be larger than 4% to tolerate errors caused by the incomplete settling of the control switches. The last two redundant values are set to 1

TABLE II TIME ALLOCATION FOR ONE SAR CONVERSION

	Each cycle	Number of cycles
DAC settling time	100 ps	10
Logic delay	50 ps	11
Comparison time	150 ps	11
Sampling	700 ps	
Total	3.9 ns	

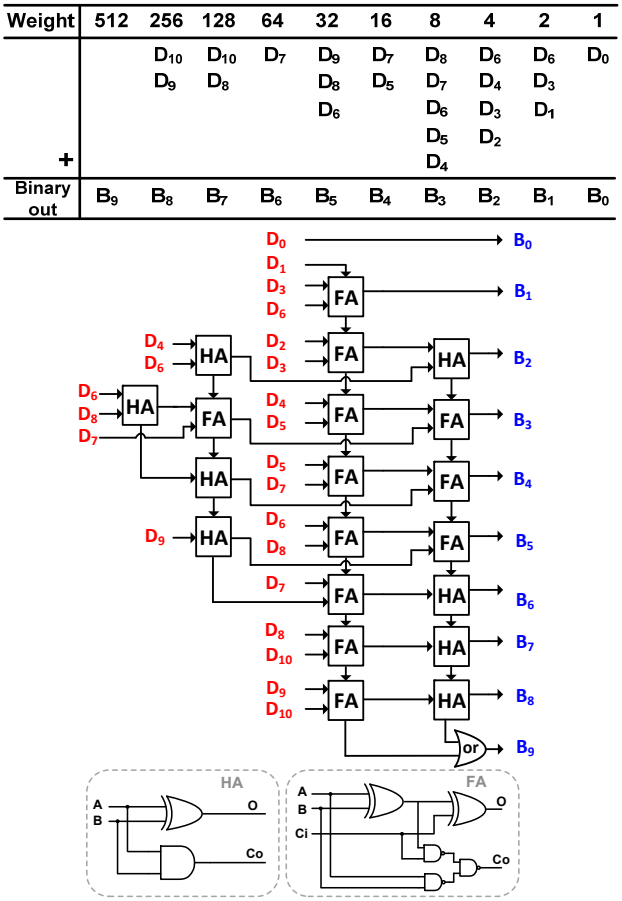


Fig. 14. Mapping table and schematic of encoding circuit from D_i (i=0~10) to B_j (j=0~9).

LSBs to adjust the number of unit capacitors as integers to facilitate the floor planning of the DAC array. In Fig. 13, the sub-radix-2 algorithm is illustrated with a 666.5 LSBs input. The numbers in circles are the redundant values of each cycle. With the different constraints of error tolerance range, the redundant value of each cycle and the number of redundant cycles could be properly changed. The total settling time requirement is shortened from 76τ (7.6τ x 10 cycles) to 35.2τ (3.2τ x 11 cycles) by using the proposed sub-radix-2 algorithm. The time allocation for one SAR conversion is depicted in Table II.

To convert the redundant ADC output codes to binary codes, the adder based encoding circuit illustrated in Fig. 14 is adopted. D_{10}~D_0 represent the redundant outputs and B_9~B_0 represent the binary codes. The encoding operation is realized

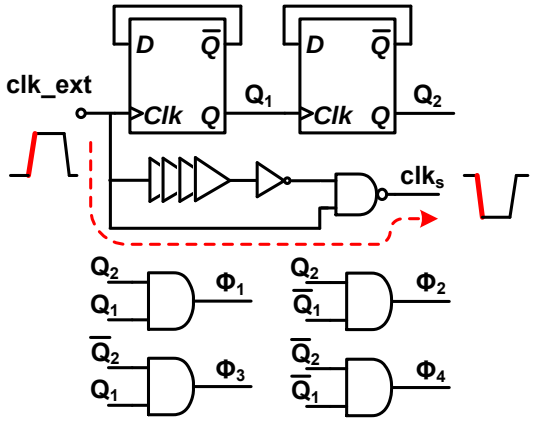


Fig. 15. Schematic of internal clock generator.

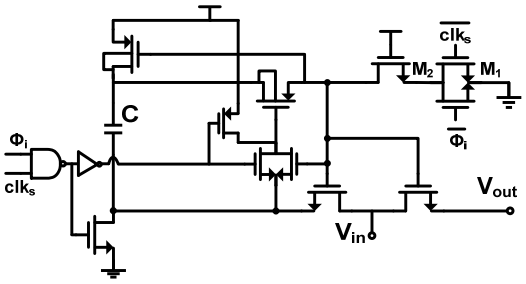


Fig. 16. Schematic of sampling switch.

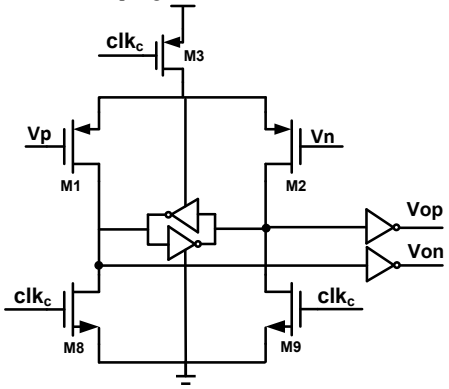


Fig. 17. Schematic of comparator circuit.

by adders instead of multiplier based FIR filters [33]. Compared with [20], no subtraction and extra unit capacitors are required. Although the hardware overhead (12 full adders (FA), 8 half adders (HA), 1 OR gate) is as same as the encoding circuit in [34], the propagation delay is significantly improved. In the improved encoding circuit shown in Fig. 14, the delay of worst case includes 4 HAs and 5 FAs, which is from D_1 (eg. toggling from 0 to 1) to B_9. However, the delay of from D_1 to B_9 in the encoding circuit in [34] could include up to 5 HAs and 11 FAs. The encoding circuit are built with only adders (FA) and half adders (HA), resulting in low power consumption.

III. CIRCUITS DESIGN

A. Internal Clock Generator

To suppress the time skew in TI SAR ADCs, a clock signal with Nyquist sampling rate is needed. The schematic of internal

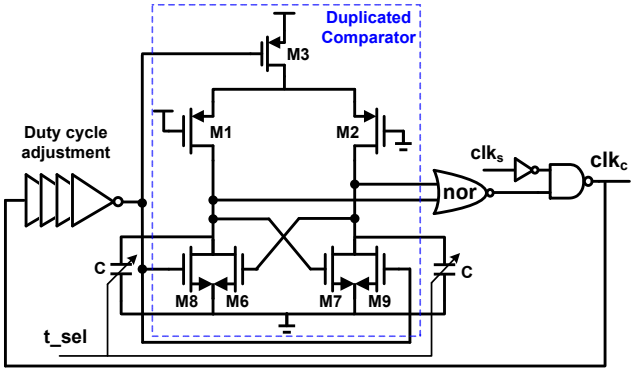


Fig. 18. Schematic of local synchronous timing generator.

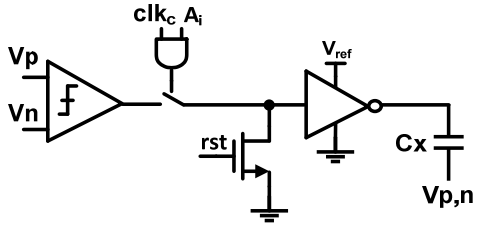


Fig. 19. Schematic of control logic circuit.

clock generator is shown in Fig. 15, where *clk_ext* is the external clock input. Signal Q_1 and Q_2 are generated by divide-by-2 and divide-by-4, respectively. The signal clk_s is obtained from *clk_ext* with duty cycle changed. When clk_s is high, one of four sub-channels operates in sampling phase. Using Q_1 and Q_2, the Φ_i (i=1, 2, 3, 4) can be generated through AND gates. In this design, the rising edge of the buffered *clk_ext* goes through only one NAND gate to generate the falling edge of clk_s, introducing less additional jitter through internal clock path. The power supply for clk_s generation is separated from other logic circuit to reduce power supply noise interference. The schematic of bootstrapped switch for proposed sampling technique is drawn in Fig. 16. Φ_i is the control signal mentioned before. When Φ_i is high, the corresponding bootstrapped switch is activated. clk_s is the full rate sampling clock, dominating the sampling instant.

B. Single Channel SAR ADC

The monotonic DAC switching [31] is adopted for sub-ADC. The schematic of dynamic comparator is shown in Fig. 17. The PMOS transistors are adopted as the input pair. When *clk_c* is high, the comparator is in reset phase. It enters comparison phase when *clk_c* is low. Two inverters follow the *Vop* and *Von* to prevent hysteresis effect caused by the following latch circuit. The programmable synchronous timing generator providing local timing with process corner sensing function is shown in Fig. 18. The generator is an oscillation circuit with an enable signal clk_s. When clk_s is low, the oscillation loop is activated. A duplicated dynamic comparator is inserted into the loop to sense the process variation of regeneration time. *t_sel* is to tune the load capacitance of the comparator, which means changing the period of clk_c. The duty cycle adjustment block is used to change the duty cycle of clk_c to balance the duration of comparison and DAC settling. The proposed dynamic control logic shortens the delay between comparator output and DAC array, which just equals to the

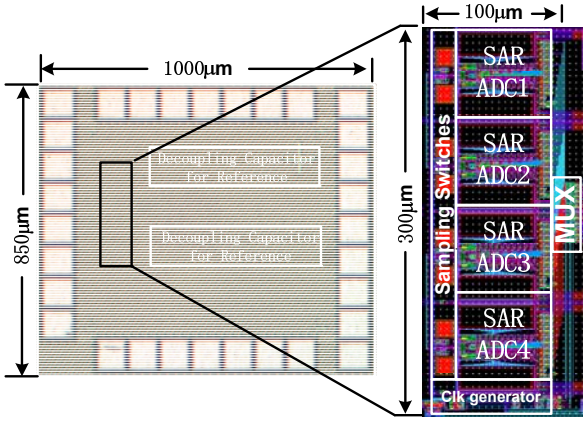


Fig. 20. Chip micrograph and layout.

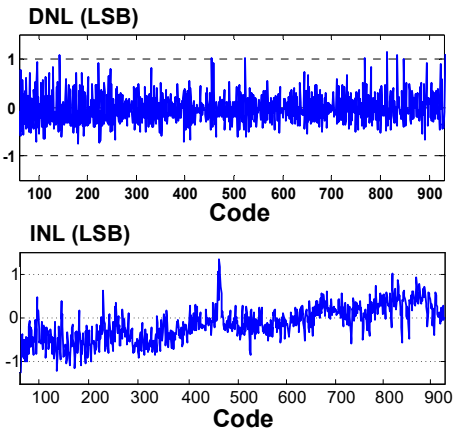


Fig. 21. Measurement results of DNL & INL.

delay of one transmission gate and an inverter. The schematic of DAC control logic is shown in Fig. 19. In the sampling phase, the reset signal *rst* is high, and all the unit capacitors in DAC array are connected to V_{ref}. During the conversion phase, the DAC array is controlled by *clk_c* under certain state A_i. The control logic is controlled by a state machine based shift register. The unit capacitor is realized with five stacked metal layer.

IV. Measurement Results

The ADC chip is fabricated in a 1P9M 65 nm CMOS process with low-V_{th} option. The die photo is shown in Fig. 20, and the ADC core occupied 0.158 mm^2. Instead of using power hungry reference buffer, a decoupling capacitor C_{dc} of 100 pF, which occupies 0.09 mm^2, is used to guarantee a sufficient error coverable range for the successive approximation comparisons. The measurement is conducted in room temperature. The power consumption is 7.95 mW (excluding off-chip time skew calibration) at 1.2V power supply when operating at 1 GS/s, with each sub-channel SAR ADC consuming 1.85 mW, and 0.4 mW for the internal clock generation and multiplexing. The encoding (ENC) block is designed off-chip, of which the estimated power is 0.15 mW and its area is 110 μm^2. The offset mismatch and background time skew calibration are done off-chip, of which the estimated power consumption is 8 mW and area is 0.038 mm^2 with 39600 gate count. The capacitance

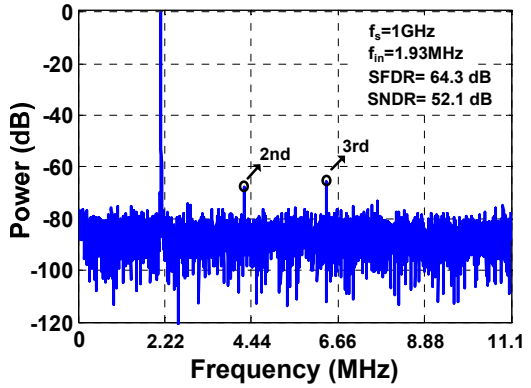
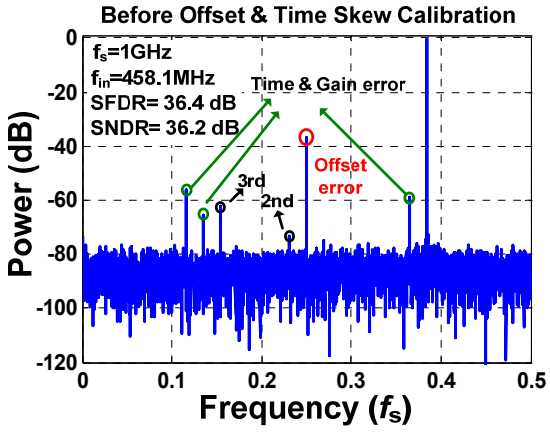
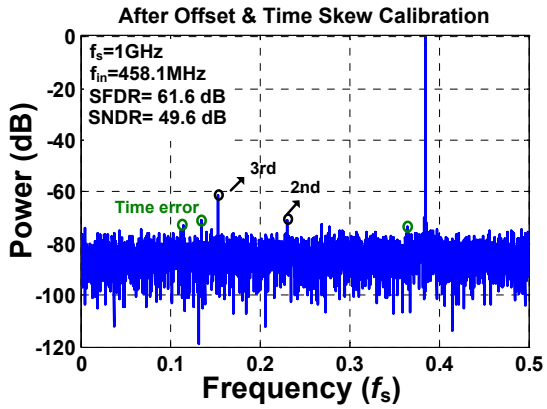


Fig. 22. Measured 8192-point FFT (digital output is decimated by 45) with f_{in}=1.9 MHz.



(a)



(b)

Fig. 23. Measured 8192-point FFT (digital output is decimated by 45) with f_{in}=458.1 MHz before and after offset and time skew calibration.

TABLE III SUMMARY OF THREE TESTED CHIPS

Chip sample	Time error (SFDR @458.1 MHz)	Offset error (Average)	Gain error (Average)
No.1	52.1 dB	26mV	0.0008
No.2	55.3 dB	17mV	0.0005
No.3	53.4 dB	28mV	0.0006

of each single-end input sampling DAC array is 240 fF (512C,

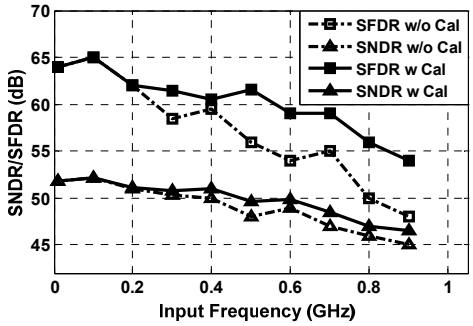


Fig. 24. SFDR and SNDR before and after time skew calibration versus input frequency at f_s=1 GHz and V_{dd}=1.2 V.

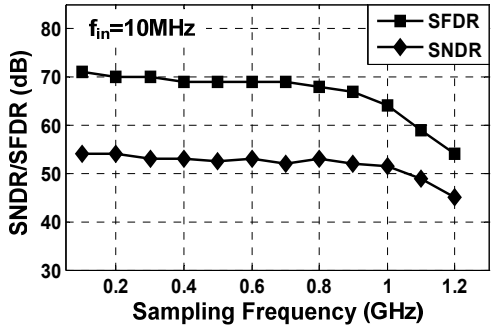


Fig. 25. SFDR and SNDR versus sampling frequency at f_{in}=10 MHz and V_{dd}=1.2 V.

TABLE IV OPTIMIZED FILTER COEFFICIENTS

$C_{n,m}$	m=0	m=1
n=0	-3.5e-7 (0)	0.2675
n=1	4.1e-6 (0)	-1.4925
n=2	1	-7.3e-13 (0)
n=3	4.1e-6 (0)	1.4925
n=4	-3.5e-7 (0)	-0.2675

each unit capacitor C of 0.47 fF) excluding parasitic capacitance. To reduce the effect of parasitic inductor of bonding wire, double input pads are used with the parasitic capacitance of 2 pF. The impedance of input is matched to be 50 Ω on board, resulting in a 3 GHz input bandwidth. In this design, the differential input range is 2.0 V_{p-p} at 1.2 V supply.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are shown in Fig. 21. The peak DNL is +1.2/-0.7 LSBs and peak INL is +1.3/-1.2 LSBs. Fig. 22 shows the measured output spectrum of 1.9 MHz. The SNDR is 52.1 dB, which is limited by large measured input-referred noise of comparator. Before offset calibration, the SNDR and SFDR are degraded mainly by offset mismatch. It is found that the gain mismatch is small enough with negligible effect on the SNDR and SFDR. Without time skew calibration, the SFDR caused by time error at 458.1 MHz input is around 52~55 dB (0.6ps *rms* equivalently) with *W/L* of M_2 (Fig. 16) being around 4 um/60 nm. The summary of measurement for the three sample chips is listed in Table III. In Fig. 23, after offset and time skew calibration, the measured SFDR at a 458.1 MHz input are improved to 61.6 dB (harmonic dominated), with all the time skew spurs less than -70 dB. The corresponding effective

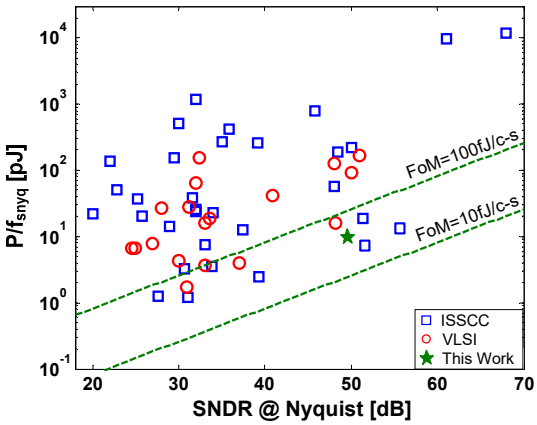


Fig. 26 Energy per conversion for all ADCs with published at ISSCC and VLSI conferences from 1997 to 2016.

number of bit (ENOB) is 7.96 bits at Nyquist input frequency. The length of time skew correction filter and interpolation filter are set as 5 and 38 respectively, which calibrate the time skew spurs to be lower than -70 dB. The coefficients of correction filter are listed in Table IV. Assuming the first channel as the reference channel, the measured time skew of other 3 channels in one chip are -0.6 ps, 0.1 ps and -1.5 ps. The iterative time step T_{step} is set to 0.1 ps. Fig. 24 shows the SFDR and SNDR (before and after time skew calibration) versus input frequency from 10 MHz to 900 MHz. Fig. 25 depicts the SFDR and SNDR versus sampling frequency at 10 MHz input frequency. Compared with the state-of-the-art ADCs (Table V), the proposed ADC achieves a low FoM value of 36.7 fJ/conversion-step (63 fJ/conversion-step with time skew compensation) and a die size of 0.03 mm^2 (0.158 mm^2 including time skew calibration and decoupling capacitors). In term of energy per conversion, this work achieves 15.9 pJ per conversion. A comparison with the prior state-of-the-arts ADCs faster than 1 GS/s published at ISSCC and VLSI conference from 1997 to 2016 [38] is shown in Fig. 26.

TABLE VI
THE COEFFICIENTS OF INTERPOLATION FILTER

n	IF(z)	*n*	IF(z)	*n*	IF(z)
0	0.00375	13	-0.05225	26	0.03500
1	-0.00500	14	0.06600	27	0.02900
2	0.00650	15	-0.08725	28	-0.02450
3	-0.00800	16	0.12475	29	0.02050
4	0.00975	17	-0.21075	30	-0.01725
5	-0.01200	18	0.63600	31	0.01425
6	0.01425	19	0.63600	32	-0.01200
7	-0.01725	20	-0.21075	33	0.00975
8	0.02050	21	0.12475	34	-0.00800
9	-0.02450	22	-0.08725	35	0.00650
10	0.02900	23	0.06600	36	-0.00500
11	-0.03500	24	-0.05225	37	0.00375
12	0.04225	25	0.04225		

V. CONCLUSION

A test chip of a four-channel 10-bit SAR ADC with sampling rate up to 1 GS/s, adopting time skew suppressed sampling technique, is presented. By utilizing the power and area efficient sub-radix-2 high speed sub-SAR ADCs, the TI-ADC achieves a low power consumption (15.95 mW) at 1GS/s and small silicon area of 0.158mm^2 including time skew calibration and decoupling capacitors. Moreover, the remaining time skew error could be compensated readily to be lower than -70 dB by TIFD filters based digital background time skew calibration. The custom designed sub-radix-2 DAC array improves the error tolerance capability during the conversion. Additionally, the adders based encoding logic provides a power and area efficient error-tolerant SAR ADC architecture.

VI. APPENDIX

The appendix describes the optimization of coefficients of

TABLE V COMPARISON OF STATE-OF-THE-ART GHZ ADCS

	ISSCC 2016[41]	JSSC 2013[15]	JSSC 2014[13]	ISSCC 2013[5]	ISSCC 2014[23]	ISSCC 2014[22]	This Work	
Architecture	TI-SAR	Pipe-line	Pipe-line	TI-SAR	TI-SAR	TI-SAR	TI-SAR	
Time skew calibration	Off-chip	Off-chip	No	No	On-chip	Off-chip	No	Off-chip
Technology (nm)	40	65	65	40	40	65	65	
Supply voltage(V)	1.1	1.0	1.0	1.2	1.1	1.0	1.2	
Power (mW)	18.4(1)	19.0	7.1	10.8	93	18.9	7.95	15.95(2)
Fs (GS/s)	2.6	0.8	1.0	0.9	1.6	1.0	1.0	
Resolution(bit)	10	10	9	9	9	10	10	
SNDR@ Nyquist(dB)	50.6	52.2	47.7	51.2	48.0	51.4	48.3	49.6
FoM (fJ/con-step)	25.6(1)	71.4	35.6	40.5	283	62.3	36.7	63(2)
Active Area (mm^2)	0.825(1)	0.18	0.1	0.038	0.83	0.78	0.03	0.158(2)(3)

(1) Digital calibration is not included.
(2) Including estimated power and active area used for the offset and time skew calibrations.
(3) Decoupling capacitors are included.

IF. The approximation error is

$$e_{IF}(\omega) = F_{IF}(\omega) - D_{IF}(\omega), \quad (12)$$

where

$$F_{IF}(\omega) = \sum_{k=1}^{K} c_k \cdot e^{-j\omega kT} \quad (13)$$

and

$$D_{IF}(\omega) = e^{-j\omega(\frac{1}{2}+\frac{K}{2})T}. \quad (14)$$

$F_{IF}(\omega)$ and $D_{IF}(\omega)$ are the approximation function and the ideal half delay, respectively. Variable K (K=2, 4, …) is the length of interpolation FIR filter. The coefficients c_k (k=1, 2, … K) are to be optimized. The min-max criterion is adopted to optimize the coefficients of IF, and the optimization problem is solved by standard SOCP (second-order cone programming) solver [43]. The coefficients of the 38-tap IF is listed in Table VI. The coefficients are symmetric about the two central taps (tap-18 and tap-19). The word-length of the coefficients is 12-bit.

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Dr. U authored and co-authored 140+ publications, 4 books in Springer and China Science Press in the area of VHF SC filters, Analog Baseband for Multi-standard wireless transceivers and Very High-Speed TI ADCs. He co-holds 9 US patents. Dr. U received ~30 research & academic/teaching awards and is co-recipient of 2014 ESSCIRC Best Paper Award. He is also the advisor for ~30 various international student paper award recipients, e.g. SSCS Pre-doc Achievement Award, ISSCC Silk-Road Award, A-SSCC Student Design Contest, IEEE DAC/ISSCC Student Design Contest, ISCAS, MWSCAS, PRIME and etc. Dr. U as the Macau founding Chairman received The 2012 IEEE SSCS Outstanding Chapter Award. Both at the 1st time from Macau, he received the Science & Technology (S&T) Innovation Award of Ho Leung Ho Lee Foundation in 2010, and also The State S&T Progress Award in 2011. He also received both the 2012 and 2014 Macau S&T Invention and Progress Awards. In recognition of his contribution in academic research & industrial development, he was awarded by Macau SAR Re government the Honorary Title of Value in 2010. He was also elected as the "Scientific Chinese of the Year 2012".

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