Experimental characterization and modeling of the contact resistance of Cu–Cu bonded interconnects

H. L. Leong, C. L. Gan, R. I. Made, C. V. Thompson, K. L. Pey et al.

Citation: J. Appl. Phys. **105**, 033514 (2009); doi: 10.1063/1.3074503
View online: http://dx.doi.org/10.1063/1.3074503
View Table of Contents: http://jap.aip.org/resource/1/JAPIAU/v105/i3
Published by the American Institute of Physics.

Experimental characterization and modeling of the contact resistance of Cu–Cu bonded interconnects

H. L. Leong,[1] C. L. Gan,[1,a)] R. I. Made,[1] C. V. Thompson,[2,b)] K. L. Pey,[3,c)] and H. Y. Li[4]
[1]*School of Materials Science and Engineering, Nanyang Technological University, Singapore 639798, Singapore and Advanced Materials for Micro- and Nano-Systems, Singapore-MIT Alliance, 4 Engineering Drive 3, Singapore 117576, Singapore*
[2]*Department of Materials Science and Engineering, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139, USA*
[3]*School of Electrical and Electronics Engineering, Nanyang Technological University, Singapore 639798, Singapore*
[4]*Institute of Microelectronics, 11 Science Park Road, Singapore Science Park II, Singapore 117685, Singapore*

(Received 28 April 2008; accepted 19 December 2008; published online 9 February 2009)

The effects of the surface roughness and applied loads on the specific electrical contact resistance of three-dimensional Cu–Cu bonded interconnects have been quantitatively investigated. Wafer-level thermocompression bonding was carried out on bonded Cu layers with either different surface roughness at a certain load or with similar surface roughness at different applied loads. Experimental results show that as the surface roughness of the Cu bonding layer increases or as the bonding load decreases, the specific contact resistance of the bonded interconnects increases. A model is presented which quantifies the relationship between the specific contact resistance and the true contact area (which is a function of the surface roughness and applied load). Through the true contact area, the integrity of a bonded interface may be predicted from the electrical measurement of the contact resistance. © *2009 American Institute of Physics*. [DOI: 10.1063/1.3074503]

I. INTRODUCTION

Three-dimensional (3D) integrated circuits (ICs) have been investigated as a technology that will extend Moore's law.[1] Thermocompression bonding of copper interconnects on silicon wafers is an attractive option for realizing 3D ICs due to copper's ability to function *both* as a mechanical adhesive and as an electrical contact between wafers. Currently, most of the reported findings on Cu-bonded 3D ICs have focused on the development of a suitable fabrication process flow, as well as on the characterization of the Cu–Cu bond quality from a mechanical perspective, as characterized through bond strengths or dicing yield measurements.[2–6] However, to implement a 3D architecture for circuit applications, electrical characterizations such as the contact resistance of the Cu–Cu bonded interconnects must be made and understood.

The electrical contact resistance between surfaces is important in many fields of science and engineering, such as microswitches in microelectromechanical systems,[7,8] flip-chip bonding in microelectronics packaging,[9,10] and the head-disk interface of magnetic rigid disks.[11] Electrical contact resistance models have been proposed in the 1960s by Greenwood[12] and Holm.[13] They developed analytical expressions for the constriction resistance due to individual or clusters of circular contact areas. However, when the contact size is smaller than the mean free path of electrons, ballistic transport will have to be considered.[14,15] A general analytical relation for size-dependent electrical contact resistance of contacts that considers both the diffusive and ballistic components as asymptotic limits has also been proposed.[16]

The effects of surface roughness and load on the electrical contact resistance of aluminum have been experimentally studied by Crinon and Evans.[17] On the other hand, Kogut and Komvopoulos[18] carried out numerical analysis on the dependence of electrical contact resistance on load, surface roughness, and apparent area. Jang and Barber[19] developed an electrical contact resistance model that takes into consideration the statistical size and spatial distribution of contact spots. Currently, there are a few reports on the experimental characterization of the electrical resistance of Cu–Cu bonded structures, but none explains the impact of process parameters for fabrication of 3D ICs on the electrical measurements.[20–22] In this paper, the effects of prebond surface roughness of the Cu bonding layers and the applied load of the bonding process on the specific contact resistance of Cu–Cu bonded interconnects are correlated. An electrical contact resistance model, based on the true contact area model using contact theory,[23] is also presented and shown to correctly predict the contact resistance of Cu–Cu bonded interconnects observed in experiments over a range of process variables.

II. EXPERIMENTS

A schematic of the four-point contact resistance measurement test structure and its electrical connections is shown in Fig. 1. Figure 2 shows a side view schematic of the contact resistance test structure. The top and bottom wafers

a)Electronic mail: clgan@ntu.edu.sg.
b)Also at Advanced Materials for Micro- and Nano-Systems, Singapore-MIT Alliance.
c)Also at Advanced Materials for Micro- and Nano-Systems, Singapore-MIT Alliance.

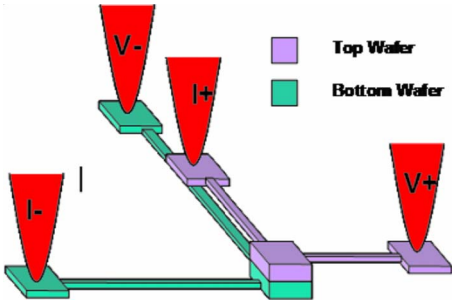

FIG. 1. (Color online) Schematic of the contact resistance test structure.

were fabricated separately using standard Cu damascene processes, and the oxide surrounding the Cu bond pads was recessed to facilitate contact between the two bonding layers. The oxide recess was created using either a dry or a wet etch to achieve different degrees of surface roughness on the Cu bond pads. The surface roughness of the Cu bonding layer was determined using atomic force microscopy (AFM) before bonding. A method has been previously developed and published for extracting the surface roughness parameters, namely, the radii of curvature of individual asperities R_i, the standard deviation of summit heights σ_s, and the density of asperities η, from AFM profile measurements.[23] In this method, profiles were taken randomly from the Cu bond pad surfaces with a scan size of 1×1 μm^2 and a scanning interval of ~5 nm. To ensure that these small-area characterizations were representative of the surface as a whole, a minimum of six scans per surface were taken and the average values were used in subsequent analyses. Data from the AFM scans were then analyzed using a MATLAB algorithm[23] that generates 3D topographical maps in which a direct estimation of R, σ_s, and η can be obtained.

The wafers were cleaned with acetic acid to remove the Cu oxide before bonding. From the process parameters, the thickness of the Cu bonding layers on the top and bottom wafers was estimated to be about 4 kÅ and 1 μm, respectively, and the thickness of the Al pads on both wafers was about 7.5 kÅ. The 200 mm diameter wafers were optically aligned using an EVG 640 Aligner. The alignment marks fabricated on both the front side and backside of the wafers were aligned to one another. The top wafer was placed face-down first and the position of the alignment marks on the front side was recorded. The bottom wafer was then placed faceup and the alignment marks on the backside were adjusted to the positions recorded for the top wafer.

After alignment, the wafers were clamped together in a bond chuck but separated by three 30 μm thick metal flaps.

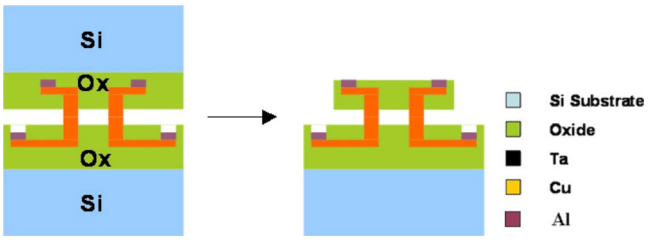

FIG. 2. (Color online) Side view schematics of the test structure.

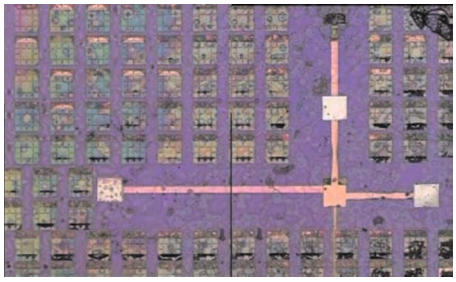

FIG. 3. (Color online) Planar optical view of the test structure after the delayering.

The bond chuck was then transferred to a bonding chamber (EVG 520), and the chamber was subjected to three N_2 pump-purge cycles to reduce the ambient oxygen content. Next, the chamber was pumped down to $\sim5\times10^{-4}$ mbar and a preprogrammed piston load, which ranged from 6 to 10 kN, was applied. The temperature was then ramped to 400 °C and the wafers were held together for 30 min. The piston load was subsequently removed and the wafers were annealed at 400 °C under the same chamber pressure for another 30 min.

The Si substrate of the top wafer was then back ground mechanically from a thickness of 700 to about 200 μm. The remaining Si and oxide layers were subsequently removed using plasma etching to expose the Al pads for probing. Figure 3 shows a planar optical view of the bonded wafers after the delayering.

The contact resistance measurements were carried out on a wafer-level probe station using the four-point probe method.[20] The contact resistance R_c can thus be given by

$$R_c = \frac{V_+ - V_-}{I}, \tag{1}$$

where V_+ and V_- are the measured voltages on the top and bottom pads, respectively, while a current sweep I from -50 to 50 mA is driven from the top to the bottom pad. The contact resistance measurements were carried out using a Keithley 2400 to source the current and a HP 34401A for the voltage measurements. The accuracies of the current stress and voltage readings are ±86 μA and ±3.2 μV, respectively. The error from an individual measurement is thus $\sim0.4\%$ and the variation between measurements is about 0.3%.

The specific contact resistance ρ_c can be obtained from

$$\rho_c = R_c A_n, \tag{2}$$

where A_n is the nominal bonded area (i.e., the area of the bond pad). Note that the top and bottom metal layers belong to different wafers and the bond pad size was either 50×50 or 100×100 μm^2 in these experiments.

III. EXPERIMENTAL RESULTS

The contact resistance of the test structures was measured and the specific contact resistances are plotted against the total surface roughness, as shown in Fig. 4(a). The specific contact resistance measurements show significant scattering about the average value. The reason for this spread in

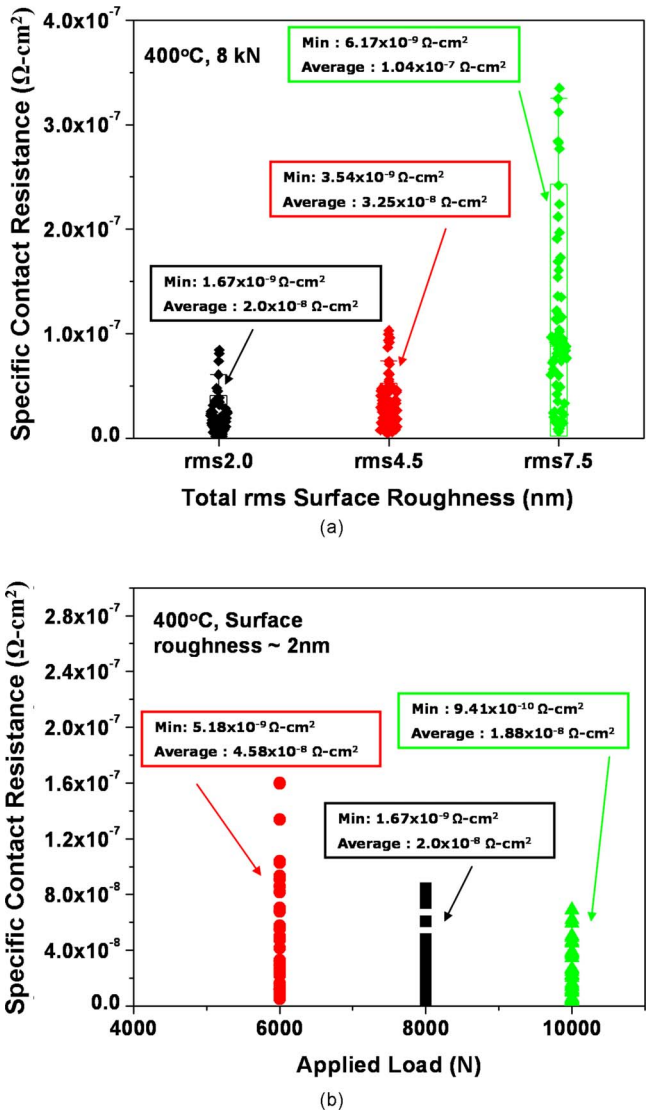

FIG. 4. (Color online) Experimental measurements of specific contact resistances of Cu bonded interfaces (a) for different total surface roughness (2, 4.5, and 7.5 nm) and (b) for different applied loads (6, 8, and 10 kN). Wafers were bonded at 400 °C.

values could be variations in the true contact area between structures due to processes such as dishing and back grinding, resulting from bonding nonuniformity of patterned wafers.[23,24] Nonetheless, the results show that as the total surface roughness increases from about 2 to 4.5 and 7.5 nm, the average specific contact resistance increases from 2.0×10^{-8} to 3.25×10^{-8} and 1.04×10^{-7} Ω cm^2, respectively.

The effects of the applied load on the contact resistances were also investigated and a plot of specific contact resistances versus applied load is shown in Fig. 4(b). The wafers were bonded with an applied load of 6, 8, or 10 kN. The total surface roughness of the prebond surfaces was kept at about 2 nm in each case to improve the yield from the bonding process. Results show that as the applied load increases, the measured average specific contact resistance decreases due to the increase in the true contact area.

IV. CONTACT RESISTANCE MODEL

The contact between two rough surfaces can be modeled as the contact of an equivalent rough surface to a perfectly flat plane.[25,26] From a contact mechanics perspective, as illustrated in Fig. 5(a), the surface asperities are not completely flattened during bonding and only a fraction of the asperities are in contact with the opposite surface. This can be visualized as a distribution of contact spots between the two surfaces, as illustrated in Fig. 5(b). The contact resistance can be assumed to be the equivalent resistance of all the contact spots at the bonded interface. It is proposed that the prebond surface roughness of the Cu bonding layers and the applied load of the bonding process, which characterize the true contact area,[23] are also the main factors affecting the value of the contact resistance of the bond interfaces.

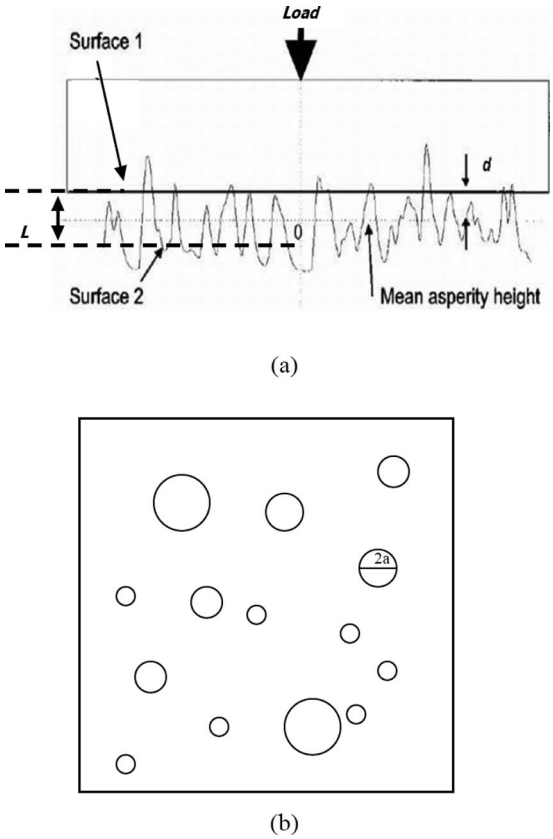

FIG. 5. Schematics of (a) a flat plane in contact with an equivalent rough plane and (b) the corresponding model of contact spots between the two planes.

The constriction resistance of an individual asperity between the classical and ballistic electronic conduction regimes can be expressed as[15,16,27]

$$R_a = \Gamma(K)\frac{\rho}{2a} + \frac{4\rho l}{3\pi a^2}, \tag{3}$$

where ρ is the resistivity of the bonded material, a is the contact radius of a contacting asperity, and l is the electron mean free path, which in this case is that of Cu and has a value of 38.7 nm.[27] $K = l/a$ is the Knudsen ratio and $\Gamma(K)$ is a function decreasing from 1 to 0.694 as l/a increases from 0 to ∞.[13,27]

In our proposed contact resistance model, the contact resistance of a bonded interface is assumed to be equivalent to the parallel resistance of all contacting asperities. This can be written as

$$R_C = \frac{1}{\sum_{i-1}^{N_c} \left(\Gamma(K_i) \frac{\rho}{2a_i} + \frac{4\rho l}{3\pi a_i^2} \right)^{-1}}, \tag{4}$$

where a_i is the contact radius of each contacting asperity and N_c is the total number of asperities that are in contact at the nominal bond area.

Assuming a Gaussian distribution of the asperity peak height,[23]

$$N_c = \eta A_n \int_{d/\sigma_s}^{\infty} \phi(x) dx, \tag{5}$$

where η is the area density of asperities, A_n is the nominal contact area, x is the asperity height normalized by the standard deviation, d is the distance between mean planes of the two contacting surfaces, and $\phi(x)$ is the standardized Gaussian height distribution scaled to make its standard deviation unity.

The contact area of each asperity is approximated by the following relation:[23]

$$A_a(z) = \pi a^2 \approx 2\pi R(z-d), \tag{6}$$

where R is the radius of curvature of the asperity and z is the asperity height. Thus, the contact radius of each contacting asperity is

$$a_i = \sqrt{2R_i(z_i - d)}. \tag{7}$$

To calculate a_i, d has to be obtained first by solving[23]

$$L_t = 3(2)^{1+x/2} \eta A_n \pi \bar{R}^{1-x/2} Y \left(\frac{0.2}{\varepsilon} \right) \sigma_s^{1+x/2} \times \int_{d/\sigma_s}^{\infty} \left(x - \frac{d}{\sigma_s} \right) \phi(x) dx, \tag{8}$$

where L_t is the applied load during bonding, $\bar{R}$ is the average radius of curvature of the asperities, σ_S is the deviation of the asperity height distribution, and Y, ε, and x are the yield stress, yield strain, and strain hardening index of the bonded material, respectively. With the values of L_t, A_n, and the surface roughness parameters known, a value for d/σ_s is obtained such that the equality of Eq. (8) is satisfied. This d value is subsequently substituted back into Eq. (7) to calculate the contact radius of each contacting asperity.

Hence, a theoretical estimate of the contact resistance R_C for a Cu–Cu bonded interface can be obtained from Eq. (4) using the calculated values of N_c and a_i, which are dependent on the applied load and surface roughness of the prebond Cu layers.[23]

V. DISCUSSION

From Eq. (4), the contact resistance model's predictions for the specific contact resistances at 2, 4.5, and 7.5 nm rms surface roughness are about 3.68×10^{-9}, 5.67×10^{-9}, and 7.36×10^{-9} Ω cm^2, respectively. The prediction is about 5–15 times smaller than that of the average experimental values but is fairly close to the minimum measured value in each case: 1.67×10^{-9}, 3.54×10^{-9}, and 6.17×10^{-9} Ω cm^2,

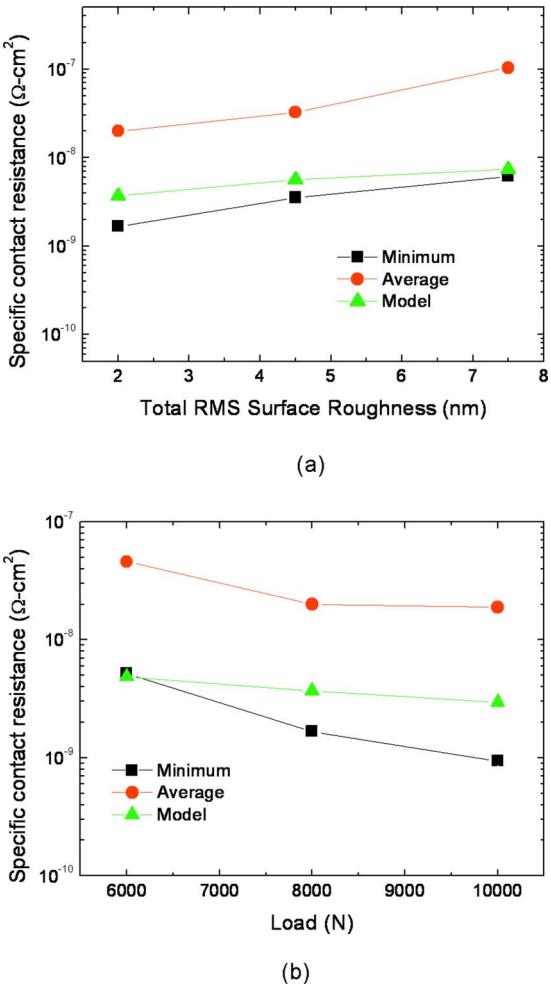

FIG. 6. (Color online) Model prediction of specific contact resistances of Cu bonded interfaces (a) for different total surface roughness (2, 4.5, and 7.5 nm) and (b) for different applied loads (6, 8, and 10 kN). Wafers are assumed to be bonded at 400 °C.

respectively [Fig. 6(a)]. The model did not provide a lower bound on the experimental data as it assumes a Gaussian distribution of asperity heights over the whole wafer surface. Thus in reality, the actual distribution of the asperity heights over the whole wafer surface could result in some bonded pads having a larger true contact area, leading to a lower measured contact resistance than the theoretical value. Moreover, the theoretical contact resistance is calculated under the ideal case of bonding between rough surfaces and does not yet account for actual process variations such as dishing. It has been reported that dishing occurs for patterned structures and this would reduce the true contact area[23] (because of fewer contacting asperities) and thus lead to a higher measured average contact resistance.

Similarly, wafers that were bonded with an increasing applied load have a decreasing specific contact resistance, as shown in Fig. 6(b). As in the previous analysis, the model's prediction is about an order of magnitude lower than the average measured value but is in the range of the minimum measured value in each case.

An electrical contact resistance-bonding map, as a function of applied load and surface roughness, can be plotted based on Eq. (4), as shown in Fig. 7, which is based on each

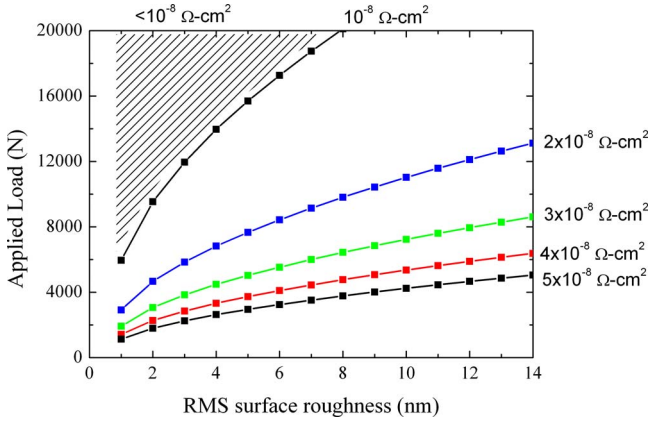

FIG. 7. (Color online) An electrical contact resistance-bonding map which depicts the specific contact resistance as a function of applied load and rms surface roughness. The wafers are assumed to be bonded at 300 °C with a nominal area of 0.02 m^2.

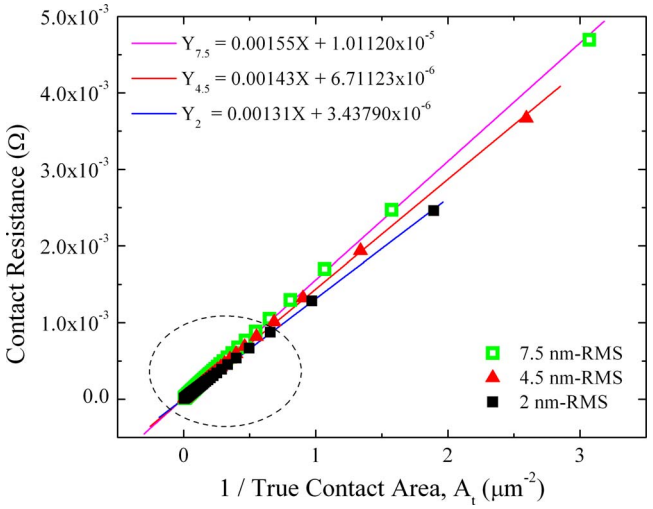

FIG. 8. (Color online) Graph of the contact resistance vs the inverse true contact area. The wafers are assumed to be bonded over a range of applied loads from 100 N to 50 kN at 300 °C with a nominal area of 0.006 m^2. The highlighted region indicates cases where the wafers are bonded under large loads.

AFM measurement assuming a total nominal contact area of 0.02 m^2. Typically, a measured specific contact resistance is on the order of 10^{-8} $\Omega\ cm^2$. The trend lines of specific contact resistance values from 10^{-8} to 5×10^{-8} $\Omega\ cm^2$ are calculated for each bonding and surface condition and represent arbitrarily defined boundary conditions. This electrical map allows the estimate of the specific contact resistance for a given wafer surface roughness and applied load, or for a given surface roughness, the applied load that is required to attain a certain value of specific contact resistance.

Based on the contact area model given in Refs. 23 and 24, the true contact area between two bonded surfaces is

$$A_t = 2\eta A_n \pi \bar{R}\sigma_s \int_{d/\sigma_s}^{\infty} \left(x - \frac{d}{\sigma_s}\right)\phi(x)dx. \tag{9}$$

The contact resistance can be related to the true contact area instead of the nominal bond area, as shown previously in Eq. (2) by

$$R_C = \frac{\rho_c'}{A_t}, \tag{10}$$

where ρ_c' is the *effective* specific contact resistance. Figure 8 shows the inverse relationship of the true contact area with the contact resistance for different surface roughness. For each measured surface roughness, the electrical contact resistance and true contact area are calculated using Eqs. (4) and (10), respectively, for a range of applied loads from 100 N to 50 kN. It is observed that the effective specific contact resistance is independent of the applied load, which is not the case for the specific contact resistance, and increases from 1.31×10^{-11} to 1.43×10^{-11} and 1.55×10^{-11} $\Omega\ cm^2$ with surface roughness of 2, 4.5, and 7.5 nm, respectively.

It has been demonstrated that the true contact area increases with decreasing surface roughness or increasing load,[23] resulting in the dependence of the specific contact resistance on the applied load and surface roughness, as shown in the electrical contact resistance-bonding map in Fig. 7. From the models, the decrease in contact resistance with an increase in applied load during bonding is due to a larger true contact area. Furthermore, this increase in the true contact area is the result of a significant increase in the number of contacting asperities, more than an increase in the contacting asperity radius. On the other hand, the specific contact resistance is observed to be less sensitive to the surface roughness. This is because at sufficiently high applied loads during bonding, large true contact areas can be obtained regardless of surface roughness, as indicated in the highlighted region in Fig. 8.

Hence the true contact area, which is a function of the surface roughness and the applied load, directly affects the contact resistance of bonded interfaces. Furthermore, the mechanical quality of the bond interface has been shown to depend on the true contact area as well.[23,28] This means that through the electrical measurement of the contact resistance of bonded interconnects, the bond strengths of thermocompression-bonded wafers can be evaluated without the need of destructive testing such as razor blade or four-point-bend tests. A high applied load and low surface roughness will lead to strong bonds between wafers and ensure optimal electrical performance of the bonded interconnects.

VI. CONCLUSION

Our experimental results show that for a given load, the contact resistances are higher for bonded interfaces with higher prebond Cu surface roughness than those with smoother surfaces. In addition, for approximately the same prebond Cu surface roughness, a higher applied load leads to lower contact resistances (due to a larger true contact area) and vice versa. In each experiment, the measured data has a significant spread about the average value. This is attributed to the nonuniform distribution of the true contact area as well as the nonuniformity of the bonding process. It also highlights the importance of proper design of the fabrication process, in particular, minimization of the Cu surface roughness, to obtain optimal results.

An electrical model has also been developed to predict the contact resistance of a bonded interface, taking into ac-

count the number of contacting asperities and asperity contact radius (which affects the true contact area too), which are functions of the applied load and surface roughness. Comparisons between the modeling and experimental results show that the theoretical estimate is in the range of the minimum measured value in each set of experiments, but is about an order of magnitude lower than the average value. This is because the model represents a situation in which bonding is affected only by the surface roughness and does not account for other larger-area process-related nonuniformities. Nevertheless, the electrical contact resistance model allows estimation of the mechanical strengths of the bonded interfaces (through measurement of the true contact area) via nondestructive electrical characterization of the bonded pads.

ACKNOWLEDGMENTS

This research was supported by the Singapore-MIT Alliance (SMA). The authors would like to acknowledge S. K. Hong (Tezzarron Semiconductor) for useful discussions.

[1]International Technology Roadmap for Semiconductors (ITRS), http://www.itrs.net/.
[2]R. Tadepalli, "Characterization and Requirements for Cu–Cu Bonds for Three-Dimensional Integrated Circuits," Ph.D. thesis, MIT, 2007.
[3]A. Shigetou, N. Hosoda, T. Itoh, and T. Suga, 51st Electronic Components & Technology Conference (IEEE, New York, 2001), p. 755.
[4]K. N. Chen, C. S. Tan, A. Fan, and R. Reif, Electrochem. Solid-State Lett. **7**, G14 (2004).
[5]K. N. Chen, C. S. Tan, A. Fan, and R. Reif, J. Electron. Mater. **34**, 1464 (2005).
[6]K. N. Chen, A. Fan, and R. Reif, J. Mater. Sci. **37**, 3441 (2002).
[7]D. Hyman and M. Mehregany, IEEE Trans. Compon. Packag. Technol. **22**, 357 (1999).
[8]H.-S. Lee, C. H. Leung, J. Shi, S.-C. Chang, S. Lorincz, and I. Nedelescu, J. Microelectromech. Syst. **11**, 147 (2002).
[9]F. G. Shi, A. Mikrajuddin, S. Chungpaiboonpatana, K. Okuyama, C. Davidson, and J. M. Adams, Mater. Sci. Semicond. Process. **2**, 263 (1999).
[10]K. W. Oh and C. H. Ahn, IEEE Trans. Adv. Packag. **22**, 586 (1999).
[11]S. Wang and K. Komvopoulos, ASME J. Tribol. **122**, 246 (2000).
[12]J. A. Greenwood, Br. J. Appl. Phys. **17**, 1621 (1966).
[13]R. Holm, *Electrical Contacts, Theory and Applications* (Springer-Verlag, Berlin, 1967).
[14]Y. V. Sharvin, Sov. Phys. JETP **21**, 655 (1965).
[15]G. Wexler, Proc. Phys. Soc. London **89**, 927 (1966).
[16]A. Mikrajuddin, F. G. Shi, H. K. Kim, and K. Okuyama, Mater. Sci. Semicond. Process. **2**, 321 (1999).
[17]E. Crinon and J. T. Evans, Mater. Sci. Eng., A **242**, 121 (1998).
[18]L. Kogut and K. Komvopoulos, J. Appl. Phys. **94**, 3153 (2003).
[19]Y. H. Jang and J. R. Barber, J. Appl. Phys. **94**, 7215 (2003).
[20]K. N. Chen, A. Fan, C. S. Tan, and R. Reif, IEEE Electron Device Lett. **25**, 10 (2004).
[21]K. N. Chen, S. H. Lee, P. S. Andry, C. K. Tsang, A. W. Topol, Y. M. Lin, J. Q. Lu, A. M. Young, M. Leong, and W. Haensch, 2006 International Electron Devices Meeting (IEEE, New York, 2006), p. 101.
[22]B. Swinnen, W. Ruythooren, P. De Moor, L. Bogarets, L. Carbonell, K. De Munck, B. Eyckens, S. Stoukatch, D. Sabuncuolu Tezcan, Z. Tokei, J. Van Aelst, and E. Beyne, 2006 International Electron Devices Meeting (IEEE, New York, 2006), p. 105.
[23]H. L. Leong, C. L. Gan, C. V. Thompson, K. L. Pey, and H. Y. Li, J. Appl. Phys. **102**, 103510 (2007).
[24]H. L. Leong, "Quantitative Analysis of the Mechanical and Electrical Properties of Cu–Cu Bonds for Three-Dimensional Integrated Circuits (3D ICs)," Ph.D. thesis, Nanyang Technological University, 2007.
[25]K. Willner, *Contact Mechanics III* (Computational Mechanics Publication Ltd., Southampton, 1997), p. 13.
[26]K. L. Johnson, *Contact Mechanics* (Cambridge University Press, Cambridge, England, 1985).
[27]R. S. Timsit, IEEE Trans. Compon. Packag. Technol. **29**, 727 (2006).
[28]H. L. Leong, C. L. Gan, C. V. Thompson, K. L. Pey, and H. Y. Li, Materials Research Society Symposium Proceedings, Warrendale, PA, 2007, Vol. 1036E.