Design and Analysis of a K-band Wideband VCO with Robust Start-up and Frequency Boost

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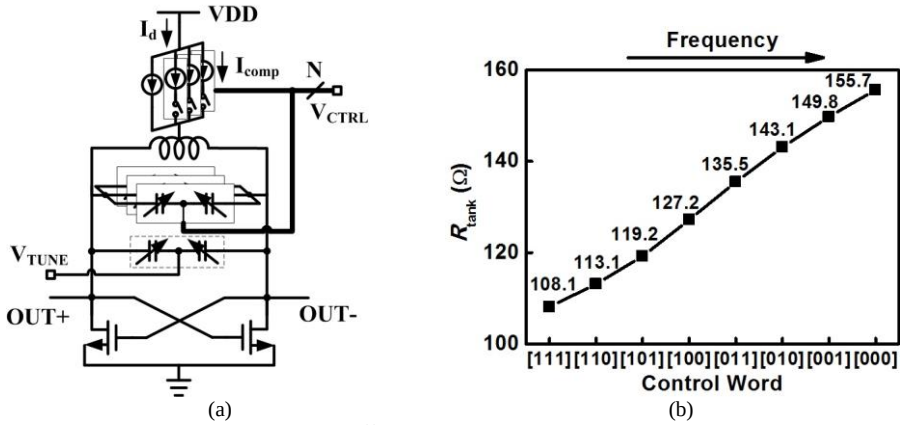
***Abstract*—This paper presents a K-band differential voltage-controlled oscillator (VCO) with robust start-up. A hybrid technique that combines open-loop digitally-controlled tail current with switchable auxiliary cross-coupled pairs (ACCPs) is proposed to ensure robust start-up for wideband operation. Compared with prior close-loop current controlling method, the proposed technique does not suffer from phase noise degradation. Furthermore, by evenly distributing the ACCPs, transistors with smaller size are allowed to achieve the same start-up condition, which leads to frequency boost and phase noise improvement. Implemented in 0.18μm CMOS technology, the VCO achieves a wide frequency tuning range of 21.4 - 26.29 GHz (20.5%) and a low phase noise of -108.8 dBc/Hz at 1 MHz offset from 25.8 GHz carrier frequency. At 1.1 V power supply, the power consumption of the core circuit is 7.9 - 11.4 mW across the entire output frequency range.**

***Index Terms*—K-band, CMOS VCO, wideband, start-up, evenly distributed auxiliary cross-coupled pairs.**

I. INTRODUCTION

To provide local oscillator (LO) signal to a heterodyne transceivers, VCO should be designed carefully with appropriate trade-offs among phase noise, tuning range, and power dissipation. Nevertheless, all the specifications make sense only on the premise that the VCO can reliably start up across all the process corners. Because of the potentially large process variation, designing a VCO with robust start-up is critical and challenging, especially for wideband applications [1-6]. Much effort has been made in recent years to achieve the goal. In [2]-[4], the reliable start-up is realized by introducing continuous feedback. The main functional blocks in the loop are peak detector (PD) and level comparator whose output constantly adjusts the tail current to guarantee robust start-up. Similarly, [5][6] use discrete feedback schemes, which comprises of a PD and digital state machine to digitally control the binary-weighted tail current. However, these works with close-loop schemes suffer from two major drawbacks. Firstly, as the control signal is applied directly on the bias of the tail current, any noise from the control circuit would translate to VCO phase noise. Secondly, the extra building blocks give rise to penalty in power consumption and chip area.

In order to address the aforementioned issues, a novel differential VCO with robust start-up is proposed by using the open-loop digitally-controlled tail current combined with switchable auxiliary cross-coupled pairs (ACCPs). The digitally-controlled tail current and ACCPs collectively provide transconductance (G_m) enhancement to compensate loss of the resonator and ensure robust start-up. To minimize the loading effect induced by ACCPs, a novel scheme of evenly-distributed ACCPs (denoted as ED-ACCPs hereinafter) is developed and analyzed, which boosts the loss compensation



(a) (b)

Fig.1 (a) VCO topology (b) tank resistance at resonance versus different control word

capability and therefore results in frequency boost and phase noise improvement. Fabricated in 0.18μm CMOS technology, the VCO achieves reliable start-up with a superior phase noise and a wide tuning range of 20.5%.

In section II, the issue of LC tank parallel resistance variation is first presented and the start-up condition is discussed. Then, the hybrid technique is proposed and the merits of the evenly-distributed ACCPs are theoretically analyzed in terms of loss compensation capability and impact on oscillation frequency. The detailed design of the VCO is shown in section III. The measurement results and conclusion are presented in section IV and V.

II. Analysis and Design Considerations of VCO with Robust Start-up

A. Discussion of VCO tank variation and start-up condition

In order to mitigate power supply pulling effect, the topology of PMOS tail current on the top along with NMOS-only cross-coupled pair is adopted in the proposed VCO design, as depicted in Fig. 1 (a). The overall band of interest is divided into 8 sub-bands by means of varactor switching. In this way, the VCO gain (k_{VCO}) is reduced to achieve better phase noise in PLL. However, as capacitance is switched into or out of the LC tank to tune the frequency, the equivalent parallel tank resistance (R_{tank}) at resonance will vary. For typical high-Q inductor and varactor, R_{tank} is expressed as

$$R_{tank} = \frac{L}{CR_{Ls} + CR_{Cs}} \tag{1}$$

where L, C, R_{Ls}, R_{Cs} represent tank inductance, capacitance, series resistance of inductor and varactor, respectively. To tune the oscillation frequency downward, the capacitance C needs to increase in square. As oscillation frequency falls, R_{Ls} decreases because it is dominated by skin effect and eddy current induced losses. Such variation is, however, comparably subtle at sub-MMW frequency. Hence, the increase in C outweighs the decrease in R_{Ls}, which leads to a net increase of the first term in the denominator of (1). Additionally, in practice, the relative rise in C is greater than the relative fall in R_{Cs} [7]. In aggregate, R_{tank} is proportional to oscillation frequency. As shown in Fig.1 (b), R_{tank} at highest band is nearly 1.5 times larger than the one at lowest band.

The cross-coupled pair in VCO periodically converts DC power into RF power to compensate the energy loss caused by R_{tank}. At start-up, (2) should be satisfied

$$1/G_m < R_{tank}, \quad (2)$$

where G_m is the transconductance of cross-coupled transistors. As a rule of thumb, the actual G_m should be three times larger than the minimum value given by (2). However, this imposes a strict requirement for wideband VCO design. For MOSFET operating in the saturation region, in first order, its G_m is derived as

$$G_m = \sqrt{\mu_0 C_{ox}(W/L) I_d} \quad (3)$$

where μ_0 is the device carrier mobility, C_{ox} is the oxide unit capacitance, W/L is transistor aspect ratio and I_d is the drain current flowing through it. In order to strike a balance between power consumption and oscillation frequency, a hybrid technique of I_d enhancement and switchable ACCPs is proposed for robust start-up. Each factor contributes equally to the G_m enhancement. The I_d enhancement is realized by an open-loop digitally-controlled tail current and is consequently free from the abovementioned issues in [2]-[6]. For ACCPs, a novel design technique is employed, featuring better compensation capability and intrinsically smaller loading effect. Considering that a large varactor array is normally used to achieve wide tuning range, a long inductor route is inevitably introduced. Conventionally, all the ACCPs are simply placed at common nodes (such scheme is denoted as CN-ACCPs hereinafter) as illustrated in Fig. 2(a). Taking advantage of the nature of the long inductor route, the scheme of evenly-distributed ACCPs is proposed in Fig. 2(b). In both schemes, the core inductor is the traditional high-Q octagonal inductor. To compare VCO's performance based on the two schemes, detailed analysis is carried out as follows.

B. Analysis of ACCPs' capability on loss compensation

The common-node ACCPs would adversely results in long interconnection between the ACCPs and inductor route, and also between the two transistors forming the ACCPs. The lossy interconnection generates parasitic resistance and inductance, which reduces the negative conductance the ACCPs can provide. On the other hand, in terms of loss compensation, the evenly-distributed ACCPs is also more efficient than common-node ACCPs, even assuming those interconnections have negligible impact. To validate the above discussion, the inductor route is modeled as multiple repetitive lumped RLC units as shown in Fig. 2 (c), where L_r is the unit route inductance, C_{var} is the varactor capacitance, R_r and R_{var} are the series resistance of inductor route and varactor respectively. In addition, all the loss related to the inductor route including electromagnetic loss is absorbed into R_L. As the network is composed of N-stage cascaded units, the ABCD matrix of each unit is extracted. The ABCD parameters are obtained from (4a)-4(d),

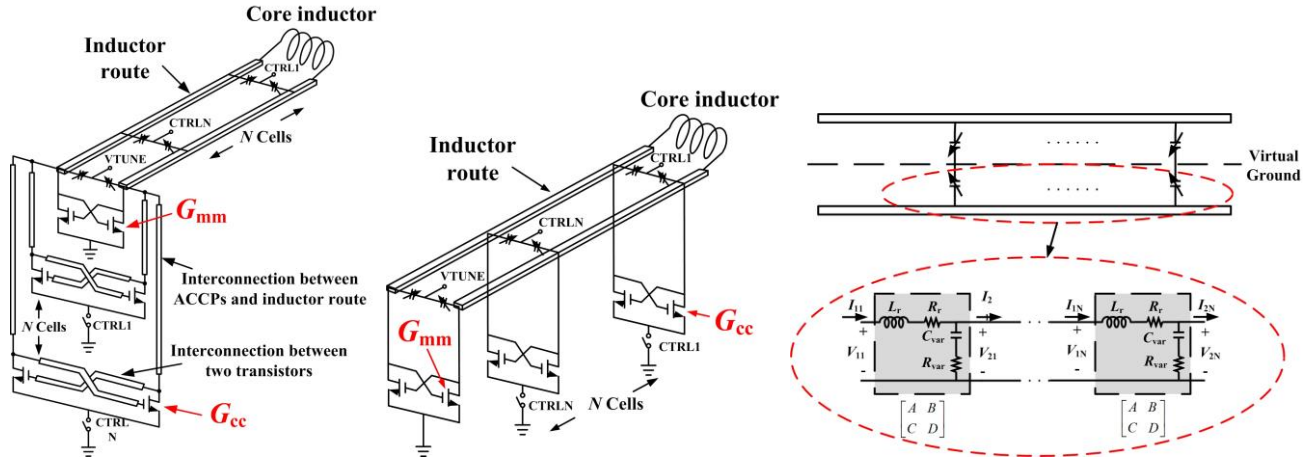


Fig. 2. (a) Scheme of common-node ACCPs (b) scheme of evenly-distributed ACCPs (c) lumped element model of inductor route.

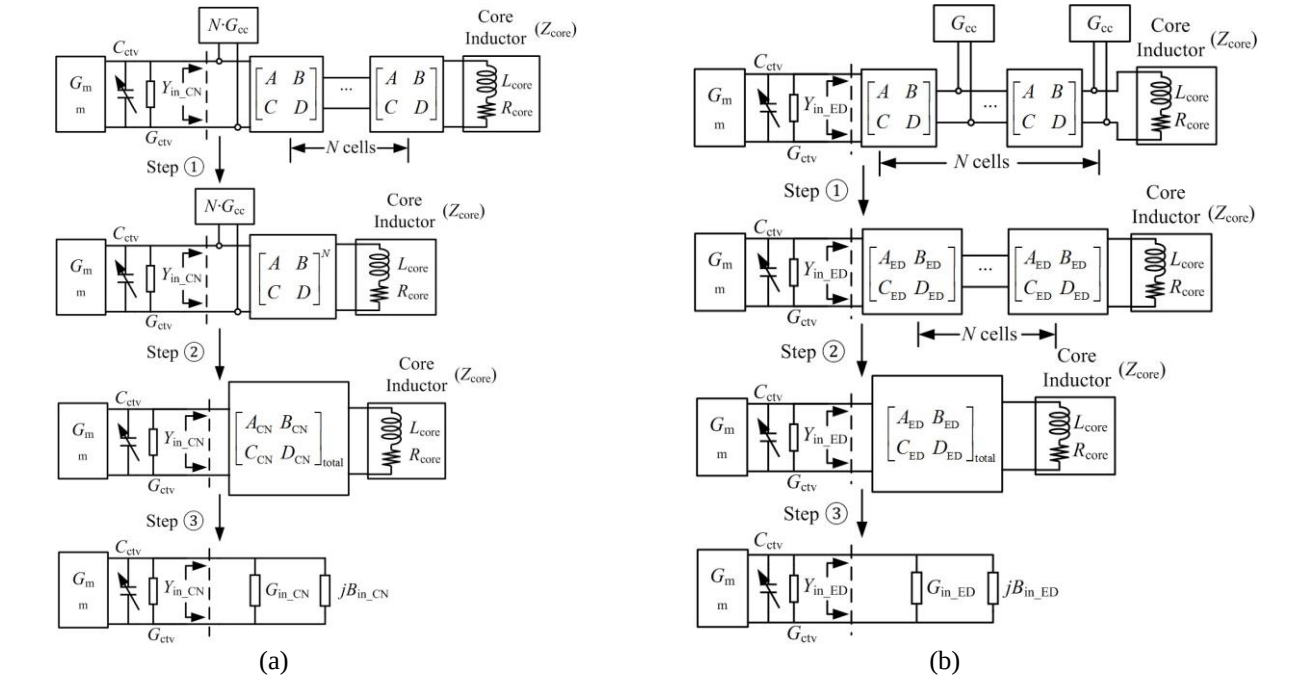


Fig. 3. Graphic interpretation for parameters extraction procedure of (a) common-node ACCPs (b) evenly-distributed ACCPs.

TABLE I

DERIVATION PROCEDURE FOR THE TWO SCHEMES

	Common-node ACCPs	Evenly-distributed ACCPs
Step ①	N-stage $ABCD$ matrices form a single-stage $ABCD_N$ matrix given by (5a);	Each $ABCD$ matrix absorbs the one-port network G_{cc} located at its port 2 to generate N-stage $ABCD_{ED}$ matrices given by (5b);
Step ②	The $ABCD_N$ matrix absorbs the one-port network $N{\cdot}G_{cc}$ located at its port 1 to generate $ABCD_{CN\_total}$ matrix given by (6a);	N-stage $ABCD_{ED}$ matrices form a single-stage $ABCD_{ED\_total}$ matrix given by (6b);
Step ③	Y_{in_CN} is derived with port 2 of $ABCD_{CN\_total}$ matrix terminated by Z_{core} (impedance of the core inductor) given by (7a).	Y_{in_ED} is derived with port 2 of $ABCD_{ED\_total}$ matrix terminated by Z_{core} (impedance of the core inductor) given by (7b).

$$A=\left.\frac{V_1}{V_2}\right|_{I_2=0}=\frac{j\omega L_r+\dfrac{1}{j\omega C_{var}}+R_r+R_{var}}{\dfrac{1}{j\omega C_{var}}+R_{var}}=\frac{j(Q_rR_r-Q_{var}R_{var})+R_r+R_{var}}{-jQ_{var}R_{var}+R_{var}} \tag{4a}$$

$$B=\left.\frac{V_1}{I_2}\right|_{V_2=0}=j\omega L_r+R_r=jQ_rR_r+R_r \tag{4b}$$

$$C=\left.\frac{I_1}{V_2}\right|_{I_2=0}=\frac{1}{\dfrac{1}{j\omega C_{var}}+R_{var}}=\frac{1}{jQ_{var}R_{var}+R_{var}} \tag{4c}$$

TABLE II
PARAMETERS IN LUMPED ELEMENT MODEL

N	G_{cc} (mS)	R_r (Ω)	Q_r	R_{var} (Ω)	Q_{var}	R_{core} (Ω)	Q_{core}
7	-1.2 (Nominal) -0.81 (Worst) -1.72 (Best)	0.1, 0.3	10-15	7	20-25	2	18

$$D = \left.\frac{I_1}{I_2}\right|_{V_2=0} = 1 \quad \text{(4d)}$$

where the reactance of the unit inductor and varactor is represented by its series quality factor Q_r and Q_{var} respectively. The graphical interpretation for the parameters extraction procedure of the two schemes is exhibited in Fig. 3, literal description is shown in Table I and the required equations are listed as follows.

$$ABCD_N = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^N \quad \text{(5a)}$$

$$ABCD_{CN\_total} = \begin{bmatrix} ABCD_N(1,1) & ABCD_N(1,2) \\ ABCD_N(2,1) + N \cdot G_{cc} ABCD_N(1,1) & ABCD_N(2,2) + N \cdot G_{cc} ABCD_N(1,2) \end{bmatrix} \quad \text{(6a)}$$

$$Y_{in\_CN} = \frac{Z_{core} ABCD_{CN\_total}(2,1) + ABCD_{CN\_total}(2,2)}{Z_{core} ABCD_{CN\_total}(1,1) + ABCD_{CN\_total}(1,2)} \quad \text{(7a)}$$

$$ABCD_{ED} = \begin{bmatrix} A + G_{cc}B & B \\ C + G_{cc}D & D \end{bmatrix} \quad \text{(5b)}$$

$$ABCD_{ED\_total} = \begin{bmatrix} A + G_{cc}B & B \\ C + G_{cc}D & D \end{bmatrix}^N \quad \text{(6b)}$$

$$Y_{in\_ED} = \frac{Z_{core} ABCD_{ED\_total}(2,1) + ABCD_{ED\_total}(2,2)}{Z_{core} ABCD_{ED\_total}(1,1) + ABCD_{ED\_total}(1,2)} \quad \text{(7b)}$$

Here, the only distinction between the two schemes is the location of G_{cc} which stands for the negative conductance delivered by a single ACCP. G_{mm} is the negative conductance provided by the main cross-coupled pair, and C_{ctv} and G_{ctv} are the continuous-tuning varactor capacitance and its series conductance. The core inductor impedance Z_{core} is represented by inductance L_{core} series with resistance R_{core}. It is further expressed as $Z_{core} = R_{core} + jQ_{core}R_{core}$ for computation, in which Q_{core} is its series quality factor. All these passive elements are of typical values extracted from EM simulation and are listed in Table II. Q_{core} is generally higher than Q_r because shielding techniques for quality factor enhancement can be applied to core inductor but is unavailable to the inductor route. To take PVT variation into consideration, G_{cc} is simulated under various operating conditions, where the process corners are typical, FNFP (fast NMOS fast PMOS), SNSP (slow NMOS slow PMOS), FNSP (fast NMOS slow PMOS) and SNFP (slow NMOS fast PMOS), the supply voltage (V_{DD}) is 1V, 1.1V, 1.2V, the ambient temperature (T) is -30°C, 27°C, 85°C. The simulation results show that the nominal G_{cc} is -1.2mS when corner = typical, V_{DD} = 1.1V and T = 27°C, the worst G_{cc} is -0.81mS under conditions of corner = SNSP, V_{DD} = 1V and T = -30°C, the best Gcc is -0.81mS under conditions of corner = FNFP, V_{DD} = 1.2V and T = -30°C.

Excluding the common parts G_{mm}, C_{ctv} and G_{ctv} in both schemes, only the rest of the network needs to be investigated. The

smaller input conductance G_{in} (real part of Y_{in}) indicates a more efficient loss compensation scheme. By applying the parameters in Table II to (4) and following the steps introduced in Fig. 3, input conductance G_{in_CN} of common-node ACCPs and G_{in_ED} of evenly-distributed ACCPs are computed and plotted in Fig. 4. To investigate the results further, the variables Q_r and Q_{var} are swept within a reasonable range for K-band application. Serving as references, the upper surfaces $G_{in\_wo\_ACCPs}$ in Fig. 4 (a) - (f) represent the input conductance without using ACCPs. As seen, both G_{in_CN} and G_{in_ED} are always smaller than $G_{in\_wo\_ACCPs}$, whereas surface of G_{in_ED} is always lower than that of G_{in_CN}. In addition, when R_L equals to 0.1 Ω, the surfaces of G_{in_CN} and G_{in_ED} are almost overlapped. This can be explained that as these ACCPs becomes spatially closer, evenly-distributed ACCPs is essentially similar to common-node ACCPs. Fig. 4 proves that with the same total negative conductance, evenly-distributed ACCPs achieves more efficient compensation. Also, evenly-distributed ACCPs guarantee a negative G_{in} under all circumstances, indicating that VCO can always start up regardless of PVT variation. Furthermore, on the premise of $G_{cc} \propto (W/L)^{0.5}$ and under nominal conditions, to achieve the same G_{in}, the required single evenly-distributed ACCP aspect ratio $(W/L)_{ED\_req}$ normalized by the one of common-node ACCP is calculated and shown in Fig. 5. As can be seen, to satisfy the same start-up condition, the required size of each ACCP is smaller when evenly-distributed ACCPs scheme is adopted. This leads to twofold benefits: (1) significant reduction in ACCPs parasitic capacitance and therefore boost in oscillation frequency and tuning range, (2) decrease in phase noise. The phase noise improvement lies in two aspects[8][9]. Firstly, the cross-coupled pair exhibits time-variant parasitic capacitance which proportionally contributes to AM-to-PM phase noise degradation. Secondly, noise from cross-coupled transistor and current source modulates high-order harmonics generated from non-linearity of cross-coupled transistors and results in phase degradation. Such effect can be alleviated by increasing transition frequency f_t and gate overdrive voltage V_{gs}-V_t and these quantities can be increased by decreasing the device width of the switching devices. On the other hand, since the inductor route is generally long for wideband VCO with large array of varactors [10][11], it will unavoidably entail large parasitic inductance and resistance in the same order of the core inductor for MMW application. Comparing Fig. 4(b) with Fig. 4(a) and Fig. 5(b) with Fig. 5(a), it is clear that the proposed evenly-distributed ACCPs will be much more effective when the inductor route is longer.

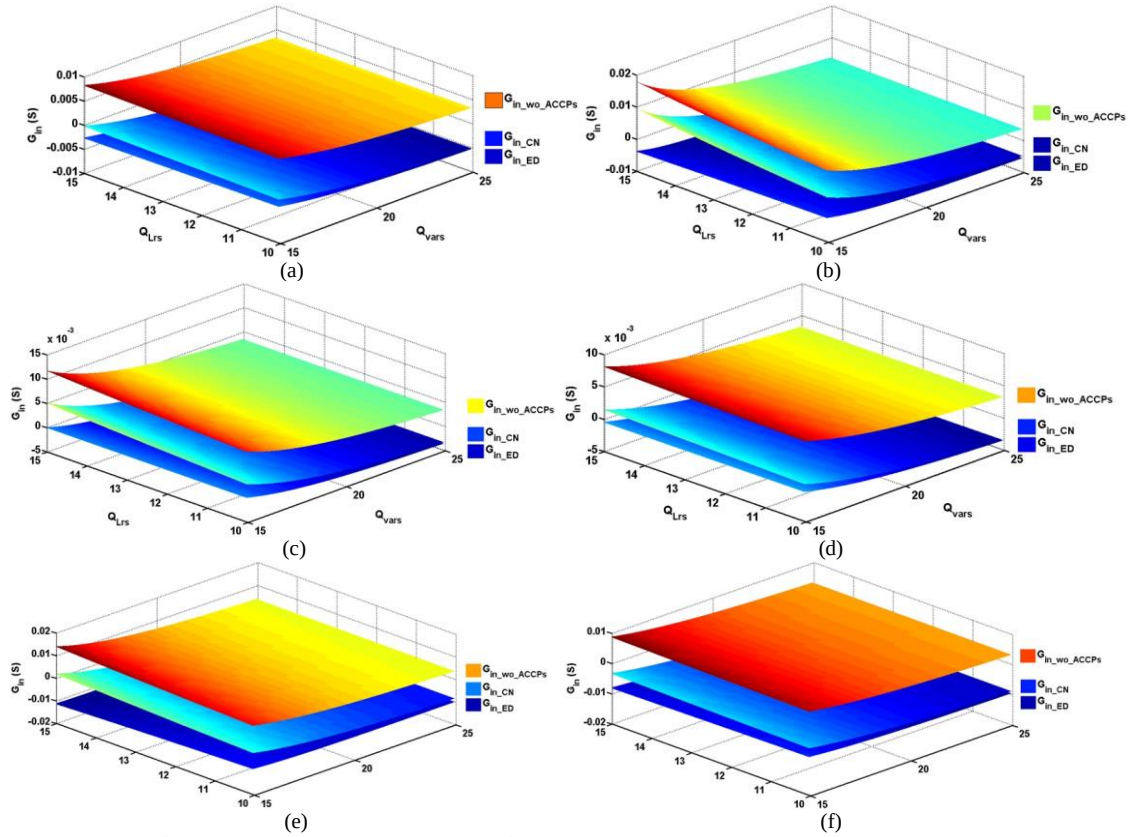


Fig. 4. Computation results of G_{in} when G_{cc} = -1.2 mS, (a) R_r = 0.3Ω (b) R_r = 0.1Ω; G_{cc} = -0.81 mS, (c) R_r = 0.3Ω (d) R_r = 0.1Ω; G_{cc} = -1.72 mS, (e) R_r = 0.3Ω (f) R_r = 0.1Ω.

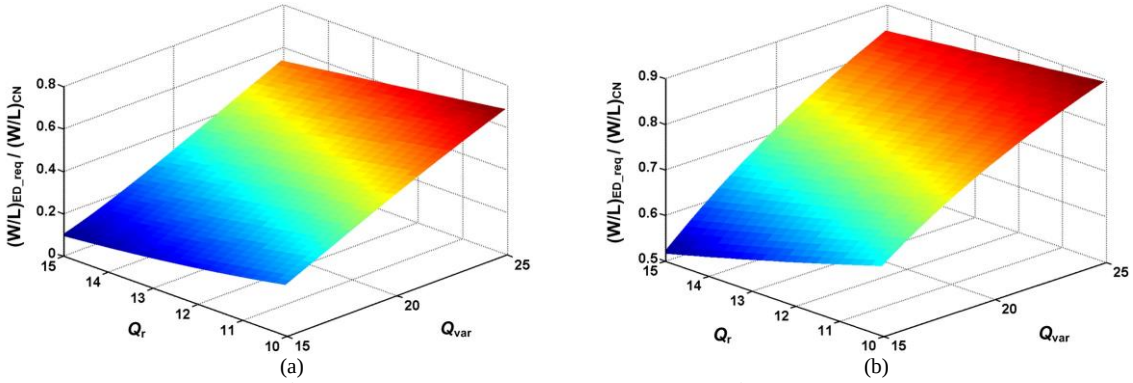


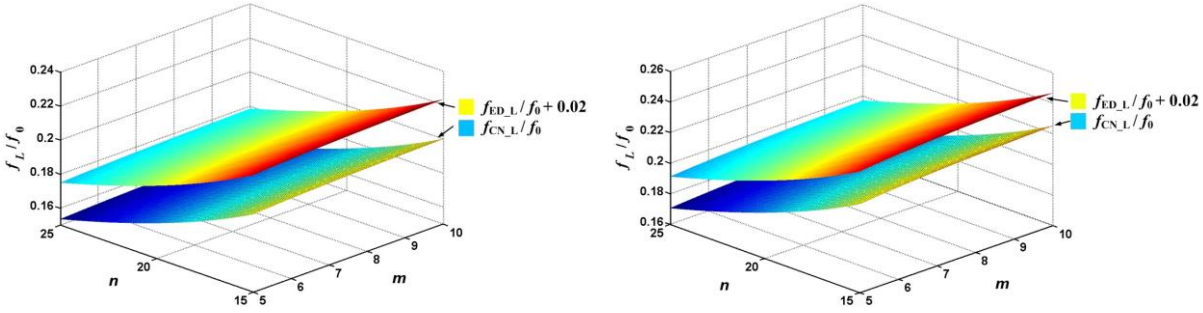
Fig. 5. Required single ACCP aspect ratio of evenly-distributed ACCPs normalized by the one of common-node ACCPs to achieve the same G_{in} when (a) G_{cc} = -1.2 mS, R_r = 0.3Ω (b) G_{cc} = -1.2 mS, R_r = 0.1Ω

C. Analysis of impact on oscillation frequency

Besides being benefited from the less capacitive loading due to the higher loss compensation capability, the structure of evenly-distributed ACCPs intrinsically leads to higher oscillation frequency. For simplicity but without loss of generality, a special case of N = 1 is used for mathematical analysis. Then the simplified LC tank models of the two schemes are constructed as shown in Fig. 6. C_f is the composite of the continuous-tuning varactor capacitance and parasitic capacitance of the main cross-coupled pair. C_c stands for the parasitic capacitance of a single ACCP. Both tanks are of fourth-order and all of the components are assumed to be ideal for simplicity. There exists two possible oscillation frequencies, namely, low frequency (f_L) and high frequency (f_H) for each scheme, and they are solved in (8).

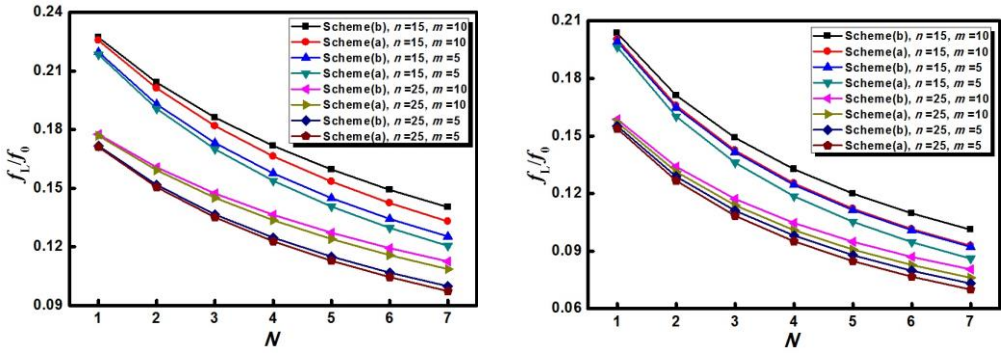
(a) (b)

Fig. 6. Schematic of the forth-order LC tank for (a) common-node ACCPs and (b) evenly-distributed ACCPs.



(a) (b)

Fig.7. Calculated low oscillation mode frequency for fourth-order LC tank (a) k = 0.15 (b) k = 0.5.



(a) (b)

Fig.8. Simulation results of low oscillation mode frequency (a) k = 0.15 (b) k = 0.5.

$$f_{CN\_L,H}=\frac{1}{2\pi}\cdot\sqrt{\frac{1}{2(L_r\|L_{core})C_{var}}+\frac{1}{2L_r(C_c+C_f)}\mp\sqrt{\frac{1}{4(L_r\|L_{core})^2C_{var}^2}+\frac{L_{core}-L_r}{2L_r^2L_{core}(C_c+C_f)C_{var}}+\frac{1}{4L_r^2(C_c+C_f)^2}}} \quad (8a)$$

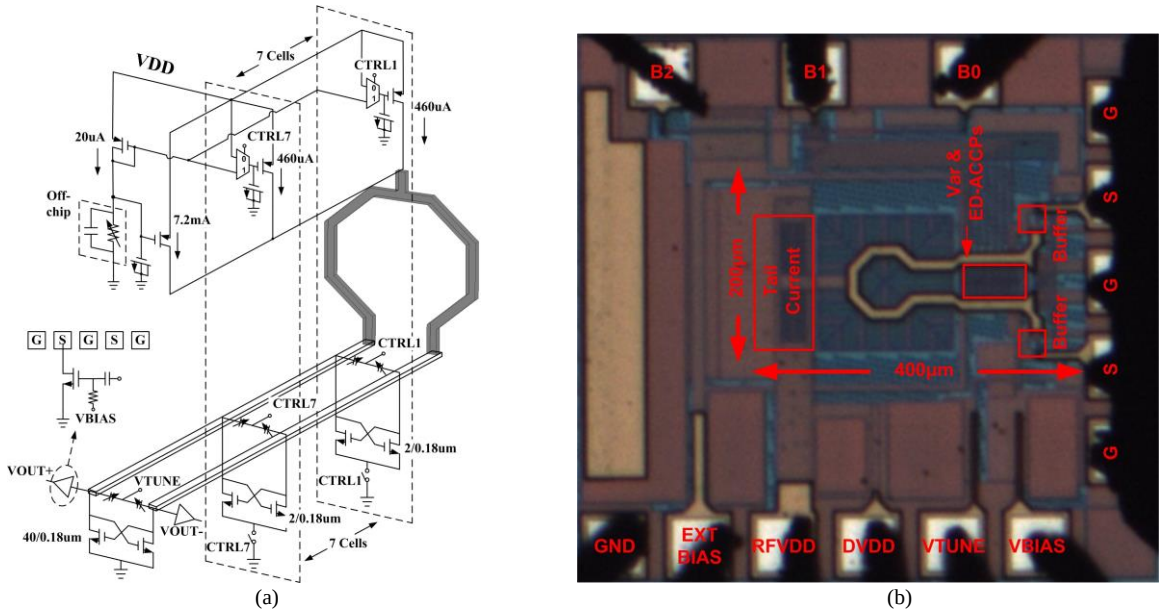
$$f_{ED\_L,H}=\frac{1}{2\pi}\cdot\sqrt{\frac{1}{2(L_r\|L_{core})(C_c+C_{var})}+\frac{1}{2L_rC_f}\mp\sqrt{\frac{1}{4(L_r\|L_{core})^2(C_c+C_{var})^2}+\frac{L_{core}-L_r}{2L_r^2L_{core}C_f(C_c+C_{var})}+\frac{1}{4L_r^2C_f^2}}} \quad (8b)$$

Assuming $L_r = k\cdot L_{core}$ and $C_f = m\cdot C_{var} = n\cdot C_c$, (8) is further expressed as (9) in terms of k, m, n and f_0 which equals to $1/[2\pi\cdot(L_{core}\cdot C_c)^{-0.5}]$.

$$f_{CN\_L,H}=\sqrt{\frac{(k+1)m}{2kn}+\frac{1}{2k(1+n)}\mp\sqrt{\left[\frac{(k+1)m}{2kn}\right]^2+\left[\frac{1}{2k(1+n)}\right]^2+\frac{(1-k)m}{2k^2n(1+n)}}}\cdot f_0 \quad (9a)$$

$$f_{ED\_L,H}=\sqrt{\frac{(k+1)m}{2k(m+n)}+\frac{1}{2kn}\mp\sqrt{\left[\frac{(k+1)m}{2k(m+n)}\right]^2+\left[\frac{1}{2kn}\right]^2+\frac{(1-k)m}{2k^2n(m+n)}}}\cdot f_0 \quad (9b)$$

By varying m from 5 to 10 and n from 15 to 25, the low oscillation frequency normalized by f_0 is depicted in Fig. 7. With C_c = 4 fF and L_{core} = 150 pH, f_0 is 205 GHz. For high oscillation mode, f_H greatly exceeds the f_{max} of 0.18μm CMOS technology. As a consequence, the high oscillation mode cannot be sustained and the VCO tends to operate in the low frequency mode. Due to close proximity of the two surfaces in Fig. 7, an offset of 0.02 is added on f_{ED_L}/f_0 for the sake of clarity. By zooming in Fig. 7(a) and (b), the actual distances by which the surface of evenly-distributed ACCPs surmounts that of common-node ACCPs are about 0.002 and 0.0035 respectively, corresponding to 410 MHz and 720 MHz frequency



(a) (b)

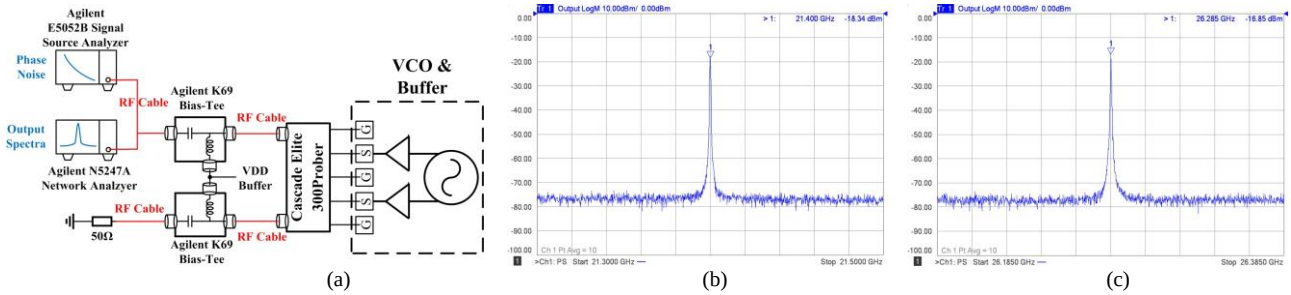
Fig. 9. (a) Schematic (b) micrograph of the proposed K-band VCO.

improvement after de-normalization. Moreover, since the order of the LC tank equals to $2N + 2$, it is extremely difficult to obtain the analytical solution of oscillation frequency for case of $N > 1$. Therefore the circuit simulation is performed, as the results are shown in Fig. 8 with several combinations of k, n and m. As shown, the oscillation frequency of evenly-distributed ACCPs is always higher than that of common-node ACCPs. It is noticeable that the frequency improvement is more significant for larger N, which is a very useful advantage in wideband MMW VCO.

III. Circuit Implementation

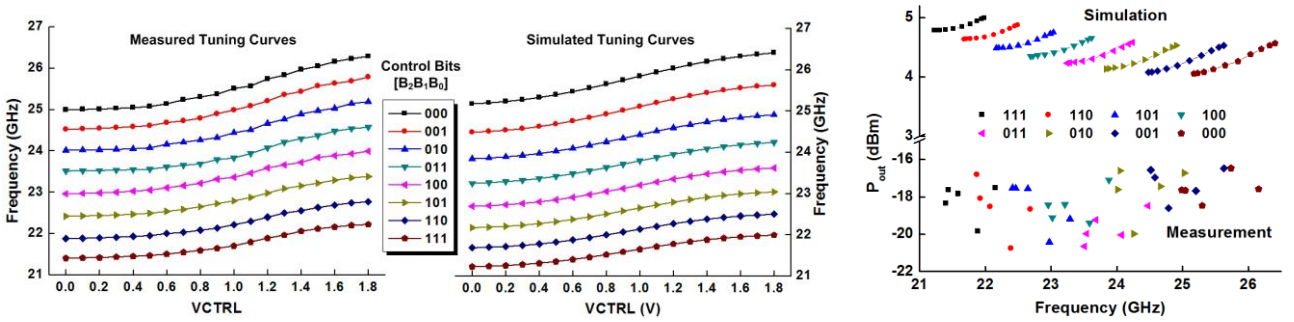
Based on the above analysis, the schematic of the proposed K-band VCO is shown in Fig. 9 (a). An array of open-loop digitally-controlled tail current is constructed using long-channel PMOS transistors to reduce flicker noise. Large MOSFET capacitors are added on the gate of the current sources to further suppress the bias-induced noise. The function of band switching is realized by using NMOS varactors, one of which with large size is used for continuous tuning and the other seven identical smaller ones are for discrete band switching. These varactors are placed symmetrically and evenly along the inductor route. To reduce the number of pads, all the control bits are generated by a binary-to-thermometer decoder.

Once the passive LC network is determined, R_{tank} is simulated and plotted in Fig. 1 (b). All the data are obtained at $V_{tune} = 1$ V where R_{tank} is at the middle point of the in-band variation. Accordingly, the size of the main and auxiliary cross-coupled pairs is determined to satisfy $3/g_m < R_{tank}$ for reliable start-up across the whole frequency as shown in Fig. 9(a). Each switchable ACCP is sized 2 μm / 0.18 μm, which provides a g_m of 800 μS. As to the choice of number of frequency bands (N), if N is too small, the tuning range of each band will be large, which will increase K_{vco} and degrade phase noise. Nevertheless, as N increases, the required minimum varactor capacitance for band switching decreases, whose accuracy will be greatly affected by process variation. Moreover, such small capacitance would be easily overwhelmed by any parasitics. All these undesired scenarios may cause frequency discontinuity after fabrication. Hence, $N = 7$ is selected as a trade-off



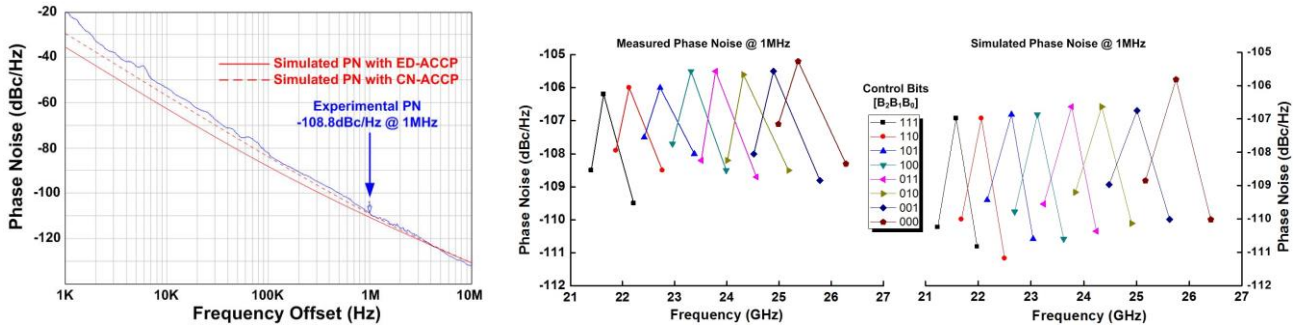
(a) (b) (c)

Fig. 10. (a) Measurement fixture (b) output power spectra of the VCO at lowest operating frequency (c) highest operating frequency



(a) (b) (c)

Fig. 11. (a) Measured tuning curves (b) simulated tuning curves (c) simulated and measured output power.



(a) (b) (c)

Fig. 12. (a) Measured phase noise at 25.8GHz and simulated phase noise with evenly-distributed ACCPs and common-node ACCPs (b) measured phase noise spots at 1MHz offset (c) simulated phase noise spots at 1MHz offset.

between frequency continuity and VCO gain. In addition, the difference in capacitance C_{on} and C_{off} of the ACCPs while working in saturation and cut-off region should be taken into account to maintain frequency continuity. The outputs of the core VCO are ac coupled to differential open-drained output buffers for testing.

IV. Measurement Results and Discussions

This work is fabricated in 1P6M 0.18μm GlobalFoundries CMOS technology. The chip micrograph is shown in Fig. 9 (b). The total chip area is 0.6 × 0.7 mm^2, of which 0.2 × 0.4 mm^2 is occupied by the core circuit. The measurement fixture is depicted in Fig. 10 (a). The output spectra at the lowest and highest carrier frequency are presented in Fig. 10 (b) and (c) separately.

TABLE III

PERFORMANCE COMPARISONS WITH STATE-OF-THE-ART K-BAND VCOS

Ref.	CMOS Process	Freq. (GHz)	Tuning Range	Tuning Voltage (V)	Tuning Sensitivity (GHz/V)	V_{DD} (V)	P_{dc} (mW)	Phase Noise (dBc/Hz)	[a] *FoM* (dBc/Hz)	[b] FoM_T (dBc/Hz)	[c] $FoM_{T/V}$ (dBc/Hz)
[12]	0.18 µm	24.27	2.2%	N.A	N.A	0.65	7.8	-100.3 @ 1M	-178.8	-171.7	N.A
[13]	0.18 µm	29.75	8.4%	-1.8 - 1.8	1.74	1	2.7	-106.8 @ 1M	-191.9	-190.5	-179.4
[14]	90 nm	20.7	4.8%	0 - 1.3	0.77	1.3	3	-113.0 @ 1M	-194.6	-188.2	-185.9
[15]	0.18 µm	24.5	16.8%	0 - 2.8	1.36	1.7	1.7	-95.5 @ 1M	-180.3	-184.1	-175.2
[16]	0.13 µm	28.15	6.7%	0 - 2.4	0.79	1.2	14.4	-112.9 @ 1M	-190.9	-187.4	-179.8
[17]	0.13 µm	26.3	23.6%	-1.5 - 1.5	2.07	1.2	36.5	-96.2 @ 3M	-159.5	-167.0	-157.5
[18]	0.18 µm	26.91	4.8%	0 - 3.3	0.39	1.8	17.7	-115.0 @ 1M	-191	-184.5	-174.1
[19]	0.18 µm	21.89	5.1%	N.A	N.A	0.6	3.5	-109.8 @ 1M	-190.9	-185.1	N.A
[20]	0.18 µm	21.35	2.8%	-1 - 1.5	0.24	2.4	9.6	-105.9 @ 1M	-182.6	-171.6	-163.6
[21]	0.13 µm	22.85	1.3%	N.A	N.A	1	10	-109.5 @ 1M	-186.7	-169.1	N.A
[22]	0.18 µm	19.88	2.6%	0 - 1.8	0.28	1.8	32	-111.0 @ 1M	-181.9	-170.1	-165.0
This Work	**0.18 µm**	**23.85**	**20.5%**	**0 - 1.8**	**0.45-0.72**	**1.1**	**7.9 - 11.4**	**-108.8@ 1M**	**-186.5**	**-192.7**	**-187.6**

[a] $FoM = L\{\Delta f\} - 20\log(f_0/\Delta f) + 10\log(P_{dc}/1\text{mW})$ [b] $FoM_T = FoM - 20\log(TR/0.1)$ [c] $FoM_{T/V} = FoM_T - 20\log(1\text{V}/\Delta V_t)$

The measured tuning range is from 21.4 GHz to 26.29 GHz with tuning voltage (ΔV_t) from 0 to 1.8 V and the measured and simulated oscillation frequency curves are plotted in Fig. 11 (a) and (b), respectively. The oscillation frequency has sufficient overlap between adjacent bands. Fig. 11(c) shows the simulated and measured VCO output power (P_{out}), where the simulated P_{out} was directly obtained at the output node of VCO core, while measured P_{out} was captured from the network analyzer without calibrating out loss induced by internal buffer, probe, balun and cables. Fig. 12 (a) shows the VCO phase noise curve at 25.8 GHz carrier frequency with low phase noise of -108.8 dBc/Hz at 1 MHz offset. Also the simulated and measured phase noise curves at 25.8 GHz carrier frequency are attached in Fig. 12 (a). It is clear that by using scheme of evenly-distributed ACCPs, VCO achieves better phase noise than that with common-node ACCPs, which verifies the aforementioned analysis. The measured phase noise at 1MHz offset versus carrier frequency is plotted in Fig. 12 (b), which features a best phase noise of -109.5dBc/Hz and a worst phase noise of -105.2 dBc/Hz. This shows good agreement with simulation results in Fig. 12 (c).

The overall core circuit excluding output buffer draws current of 7.2 to 10.4 mA with a step of 460 uA for each band at 1.1 V supply. The DC current consumption of differential output buffers with off-chip Bias-Tee is 9.2 mA at 1.5 V supply. The key performance of the VCO is summarized and compared with other relevant works in Table III. The figure of merit $FoM_{T/V}$ is proposed in [23] and is utilized as a metric of the VCO's tuning capability.

Compared to other state-of-the-art works [2]-[6], this VCO with robust start-up achieves a superior phase noise and tuning range without using complicated functional circuits.

V. CONCLUSION

Based on accurate modeling and analysis, an effective method to realize a VCO with robust start-up is proposed. The open-loop digitally-controlled tail current and switchable auxiliary cross-coupled pairs are introduced to ensure robust start-up across a wide frequency range. By evenly distributing the auxiliary cross-coupled pairs along the long inductor route, a high efficiency loss compensation and boost on oscillation frequency is achieved. A phase noise of -108.8 dBc/Hz at 1MHz and a wide tuning range of 21.4 GHz to 26.29 GHz are accomplished. At 1.1 V supply, the VCO core consumes 7.9 to 11.4

mW across the tuning range. Benefited from the proposed technique, this work accomplishes the best FoM_T and $FoM_{T/V}$ among prior state-of-the-art works.

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