NANYANG TECHNOLOGICAL UNIVERSITY

INVESTIGATION OF RESISTIVE SWITCHING AND CONDUCTION MECHANISMS IN OXIDE-BASED RRAM DEVICE FOR EMERGING NONVOLATILE MEMORY APPLICATIONS

FANG ZHENG

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

NANYANG TECHNOLOGICAL UNIVERSITY

2013

INVESTIGATION OF RESISTIVE SWITCHING AND CONDUCTION MECHANISMS IN OXIDE-BASED RRAM DEVICE FOR EMERGING NONVOLATILE MEMORY APPLICATIONS

FANG ZHENG

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

A thesis submitted to Nanyang Technological University

in partial fulfilment of the requirement for the degree of

Doctor of Philosophy

2013

Acknowledgement

First and foremost, I am deeply indebted to my supervisors Prof. Yu Hong Yu and A/P Fan Weijun, for their valuable guidance, consistent support and encouragement throughout the course of my graduate study at Nanyang Technological University, Singapore. From the start of my graduate course, Prof. Yu has been inspirational and is the role model of a hardworking and creative researcher. Scientific, technological and ethical standard of the two professors' are the ones I aspire to. I consider myself privileged to have the opportunity to work with such outstanding and motivated professors.

I would like to express my sincere gratitude to my co-supervisors Dr. Navab Singh, Institute of Microelectronics (IME), Singapore, Prof. Ghibaudo Gerard, Institut de Microélectronique Electromagnétisme et Photonique (IMEP), France and Dr. Barbara de Salvo, Laboratoire d'électronique des technologies de l'information (LETI), France, for their guidance during the course of this thesis work.

I also would like to express my appreciation to Dr. Li Xiang, IME, Dr. Wang Xinpeng, IME, Dr. Jan Chroboczek, IMEP, Dr. Xu Yong, IMEP, Dr. Julien Buckley, LETI, Dr. Carlo Cagli, LETI, for their valuable discussion on my research work.

I would like to take this opportunity to thank Nanyang Technological University, Singapore, for providing a research scholarship and research facilities. And I am also grateful for the research facilities support by Institute of Microelectronics, Singapore. More than that, I would like to thank France Embassy in Singapore for the financial support of the exchange study in IMEP/LETI, Grenoble, France, under Merlion Project.

Many thanks go to the members of the CMOS group, Dr. Liu Wenjun, Mr. Wu Ling, Mr. Sun Yuan, Mr. Wang Zhongrui, Mr. Tran Xuan Anh, for their support and sharing knowledge with me. I would also like to thank Prof. Kang Jinfeng, Mr. Gao Bin, Ms. Wu Xing, Mr. Li Yicen, Mr. Qin Hailang for their technical discussion and support.

Special thanks go to the technical staffs in Nanyang Nanofabrication Center (N2FC), Semiconductor Characterization Lab, Nanoelectronic Lab in NTU and clean rooms in IME. I am indebted to many friends who assisted me in the fulfilment of this research.

I dedicate this dissertation to my dear family, my parents and my wife. Many thanks to their unconditional love, without their support, patience and love through my life, I would not be able to reach this far.

Table of Contents

Acknowledgement I

Table of Contents III

Summary VII

List of Figures X

List of Tables XIX

Chapter 1 Introduction 1

1.1 Background 1

1.2 Objectives 3

1.3 Scope of Research and Approaches 4

1.4 Major Contributions of the Thesis 5

1.5 Organization of the Thesis 7

Chapter 2 Literature Review 9

2.1 Introduction 9

2.2 Nonvolatile Memory and Emerging Memory Technologies 9

2.3 Resistive Random Access Memory Device 14

2.4 Classification of device operation 17

2.5 Resistive Switching Mechanisms 19

2.5.1Thermal Effect 20

2.5.2 Electrochemical Metallization (Programmable Metallization) 24

2.5.3 Valence Change Systems (Anion Migration Induced) 28

2.5 Metal-Oxide Based Material Stacks for RRAM 35

2.7 Summary 38

Chapter 3 Experiments 39

3.1 Introduction 39

3.2 Device fabrication techniques 39

3.3 Fabrication Process Flow 42

3.4 Physical Characterization Tools 45

3.5 Electrical characterization 53

3.5.1 Equipment used for characterization 53

3.5.2 Resistive switching measurement 55

3.5.3 Retention measurement 57

3.5.4 AC switching measurement 59

3.5.5 Low frequency noise measurement 60

3.6 Summary 62

Chapter 4 Resistive Switching Mechanism Investigation and Temperature Instability Study in Oxide-based RRAM 63

4.1 Introduction 63

4.2 Physical Analysis 64

4.2.1 XPS Results of the Oxidized Film 64

4.2.2 Cross-Section TEM and EDX analysis 66

4.3 Resistive Switching in HfO_x-Based RRAM Cell 67

4.4 Temperature Effect on Resistive Switching 70

4.5 Retention Characteristic of Fabricated Cells 73

4.6 Multi-level switching 77

4.7 Summary 80

Chapter 5 Current Conduction Mechanism Investigation in Oxide-Based RRAM 82

5.1 Introduction 82

5.2 Device under test 83

5.3 DC current conduction mechanism investigation 84

5.4 Low frequency noise background 91

5.5 LFN analysis on oxide-based RRAM cell 94

5.6 Noise fluctuation model for LRS 100

5.7 Current conduction model for filament type RS cell 103

5.8 Summary 111

Chapter 6 Oxide-Based RRAM Device Performance Improvement by Material Optimization 113

6.1 Introduction 113

6.2 Design of experiment 114

6.3 Forming free in multilayer device 117

6.3 Uniformity improvement of operation parameters in both cycle to cycle and device to device regime 120

6.4 Chemical insight of forming free behavior in multilayer device 128

6.5 Summary 132

Chapter 7 Conclusion and Recommendations 133

7.1 Conclusion 133

7.2 Recommendations and Future Work 135

Bibliography 137

Author’s Publications 159

Summary

This thesis introduces fabrication and physical as well as electrical characterizations of oxide-based resistive random access memory (RRAM) which has been recently explored as one of the most promising nonvolatile memory technology. The objective of this thesis focus on the device fabrication and investigation of underlying physics of resistive switching mechanism and current conduction mechanism indifferent resistance states in oxide-based RRAM, in order to improve device performance for the implementation and integration of memory cell in CMOS circuits.

High performance resistive switching device has been demonstrated based on TiN/HfO_x/Pt structure, and its switching and retention behaviors under voltage and temperature bias have been studied. The resistive switching behavior can be explained by the formation and rupture of oxygen vacancies related conduction filament. It is found that at high temperature, transition voltage of set/reset process decreases probably due to an effectively lowered potential barrier for oxygen vacancy formation and recovery plus higher oxygen mobility; high resistance state (HRS) leakage increases that leads to a smaller on/off window, which may be due to the higher density of oxygen vacancies giving rise to the trap-assisted tunneling current. In terms of retention stability, temperature plays a more important role than voltage bias; room temperature retention time can be extrapolated from accelerated temperature measurement. Multi-level resistive switching can be achieved by proper control of compliance current or reset stop voltage,

however, it may not sustain at high temperature due to an increased leakage current at HRS.

To have better understanding of resistive switching phenomena, current conduction mechanism has been investigated via both DC and low frequency noise analysis. It is confirmed that for low resistance state (LRS), current conduction is localized without any area dependence; whereas for HRS, it is nearly uniform leakage current that scales reciprocally with device area. A model consisting of two parallel resistances from conduction filament and uniform leakage current has been proposed to represent the current conduction in filament type switching memory cell. It is found that in low resistance regime, filament resistance dominates current conduction as well as noise behavior which varies nearly to the square of the resistance variable; while in high resistance regime, uniform oxide leakage dominates, which results in a roughly constant noise level that related to device areas. Based on this, a noise model is proposed for this type of switching cell, and the simulation curve fits experiment data well. Further, a filament conduction noise model has been suggested for LRS, allowing estimation of filament carrier concentration that is found in the metallic range.

Based on the understanding of switching mechanism and current conduction, device with multilayer oxides is used to tackle the uniformity issue faced in RRAM device operation. Compared with single layer control device, resistance switching parameters uniformity has been significantly improved in $HfO_x/TiO_x/HfO_x/TiO_x$ multilayer structure for both cycle-to-cycle in one device and device-to-device. Compact set/reset voltage distribution,

reduced reset current as well as tight HRS resistance distribution has been observed in multilayer device. More than that, forming process is not necessary in such device owing to the lowered fresh resistance caused by Ti induced defects in oxides. Physical analysis using transmission electron microscope (TEM) - electron energy loss spectroscopy (EELS) is carried out to probe the chemical origin of multilayer forming free device. It is suggested that doping effect of Ti diffused in HfO_x and confinement of filament between multilayer oxides leads to the improvement in stability and uniformity.

In a summary, high performance oxide-based RRAM device has been demonstrated on standard CMOS fabrication platform. Resistive switching and current conduction mechanism has been investigated via various physical and electrical characterization. Excellent uniformity and forming free has been achieved by switching material optimization.

List of Figures

Figure 2.1 Schematic of a floating gate Flash memory cell [18] 10

Figure 2.2 Schematic of the OUM vertical phase-change memory element: Amorphization of this region stops the low-resistive current path and results in an overall large resistance. [28] 12

Figure 2.3 Simplified structure of an conventional MRAM cell [29] 13

Figure 2.4 A typical metal–insulator–metal capacitor structure of RRAM device cell.... 15

Figure 2.5 Conceptual diagram for ideal 3D NVM stacking structure utilizing stackable peripheral circuits [41] 16

Figure 2.6 The two basic operation schemes of resistance switching memory cells. (a) unipolar switching and (b) bipolar switching. cc denotes compliance current. Dashed lines indicate that the real voltage level at the system will differ from the control voltage because of the cc in action. Please note that the I-V of real systems may deviate considerably for both operation schemes. [43] 17

Figure 2.7 Classification of the resistive switching effects which are considered for nonvolatile memory applications. [43] 19

Figure 2.8 Unipolar I-V curves of a Pt/NiO/Pt stack with a NiO film thickness of 50nm [51]. Initial forming and a few cycles of set and reset processes are indicated, where current compliance is applied to forming and set processes. 21

Figure 2.9 Schematics of the initial state as well as forming, reset and set process. After forming, conductive paths are formed between electrodes, and it is believed to be ruptured near metal / oxide interface 22

Figure 2.10 Typical current-voltage characteristic of a Ag/Ag-Ge-Se/Pt electrochemical metallization cell. The insets A to D show the different stages of the switching procedure. [56] 25

Figure 2.11 Optical microscopy image of a Ag dendrite grown from the (-)Au electrode towards (+)Ag electrode within a As_2S_3 thin film on a glass substrate. [57] 26

Figure 2.12 (a) Sketched cross-section of bipolar switching oxide cells indicating the virtual cathode after forming process (b) highly conductive LRS (set) state (c) highly resistive HRS (reset) state. 31

Figure 2.13 Active electrode interface of the oxide dual-layer memory concept. [63] (a) Sketch of the potential barrier for initial, programmed (reset) and erased (set) memory cell. (b) Cell characteristic as a function of tunneling oxide thickness and scaling of the current with tunneling oxide thickness. (c) Simulated evolution of the oxygen vacancy profile with time during reset 34

Figure 3.1 Basic capacitor structure of RRAM cell in this work with TiN and Pt as electrodes. Probing positions during measurement are also indicated. 41

Figure 3.2 Basic mask layout for top electrode patterning with different dimensions 41

Figure 3.3 Baseline flowchart of MIM capacitor structure fabrication 42

Figure 3.4 Schematic illustration of an ellipsometer measurement setup [95] 46

Figure 3.5 Image of LEO 1550 Gemini SEM used in this work 47

Figure 3.6 SEM image of poor quality platinum film deposited at the initial phase of this project 48

Figure 3.7 TEM image of an under etched contact hole, which causes a large contact resistance 49

Figure 3.8 Schematic diagram of AFM operation principle [98] 50

Figure 3.9 An example of EDX scan plot that reveals the spatial distribution of elements in an Pt/HfO_x/TiN RRAM cell.. 51

Figure 3.10 Simplified schematic illustration of how XPS works [100] 52

Figure 3.11 Equipment used in electrical characterization (a) Keithley 4200 Semiconductor Characterization System (b) SUSS 200mm probe station system (c) Agilent 81110A pulse generation unit 54

Figure 3.12 Typical DC bipolar resistive switching current-voltage characteristics of HfOx based RRAM device with TiN as top electrode and Pt as bottom electrode 55

Figure 3.13 New operating scheme proposed by Chen *et al.* using CSM for forming and set and VSM for reset to improve device switching uniformity [103] 57

Figure 3.14 Data retention measurement (a) constant voltage stress measurement (b) retention measurement with short period bias applied only at certain recording time points... 58

Figure 3.15 Schematic waveforms of two pulses of widths 50ns and 20ns measured at half peak voltage point with rising and falling time of 10ns. 59

Figure 3.16 (a) Schematic of 3PMNS low frequency noise measurement setup (b) Simplified schematic of the programmable biasing amplifier [109]. 61

Figure 4.1 XPS Hf 4*f* scan of HfO_x as-deposited film with oxidation time of 5 and 20 minutes respectively, binding energy (BE) peaks at 17.1eV and 18.6 eV show the as prepared Hf thin film has been fully oxidized. (Calibrated with C 1*s*)............................ 65

Figure 4.2 HRTEM image of the TiN/HfO_x/Pt memory cell, an interfacial layer of TiO_xN_y is identified.. 66

Figure 4.3 EDX spectrum of elemental spatial profile showing oxygen tends to be attracted by TiN. Inset indicates the direction of profile. 67

Figure 4.4 The switching characteristics of 100 repetitive DC sweeping current-voltage of the HfO_x based ReRAM after a forming process at room temperature. 68

Figure 4.5 Switching endurance of 500 cycles in DC sweeping mode at room temperature. Resistance values are taken at 0.5V for both HRS and LRS 69

Figure 4.6 The schematics of set and reset processes. During set, oxygen ions move away from its lattice by applied electric field and form the conduction path with oxygen vacancies. During reset, oxygen ions move back to recombine with the vacancies and then conduction path disappears. 70

Figure 4.7 Comparison of resistive switching at both 25°C and 100°C. (inset shows schematic high temperature HRS leakage current (TAT) increases). At high temperature, trap concentration inside dielectric increases, which gives rise to TAT current. Therefore, the On/Off ratio decreases at high temperature. 71

Figure 4.8 Retention behavior at both room and high temperature at the voltage of 0.5V. It shows a clear current level different between room temperature and high temperature, while for both cases, retention is stable over the 1000s period. 72

Figure 4.9 Set (V_{set}) and reset (V_{reset}) voltages decrease with increasing temperature. Data points show the average values of 10 set/reset voltages of DC sweeps at each temperature. 73

Figure 4.10 Resistance variation ($|\Delta R/R_{t=0}|$) of HRS at different stress conditions and temperatures. It shows $|\Delta R/R_{t=0}|$ (original resistance is defined as the resistance prior to

stressing) does not vary much, which is negligible as compared with memory window of ~100 times. 74

Figure 4.11 Measured HRS retention times as a function of temperature. The exponential dependence of the retention time with temperature is observed, which is consistent with formula derivation. 76

Figure 4.12 Multi-level switching with different reset stop voltages from -2V to -3.5V. Besides LRS, four levels of resistance can be achieved by proper control of voltage. 77

Figure 4.13 Multi-level switching under different compliance currents from 5mA to 50mA. Besides HRS, three levels of resistance can be achieved by proper control of compliance current. 78

Figure 4.14 Multi-level switching disappears at high temperature (60°C). This may be due to higher leakage current at high temperature, which is equivalent to a lowered HRS resistance. Inset shows the multi-level switching at room temperature 79

Figure 4.15 Schematic set / reset transition indicating diffusion in reset process 80

Figure 5.1 Schematic of the memory cell (DUT) used in current conduction mechanism investigation via both DC and LFN analysis. TiN and Pt are used as top and bottom electrode respectively and 10nm of HfO_x is used as resistive switching layer. 83

Figure 5.2 Typical bipolar resistive switching curve for HfO_x RRAM device used for current conduction investigation 84

Figure 5.3 Logarithmic plot of I-V curve for current conduction model fitting of HRS and LRS. Slope of one is observed for the entire LRS and small voltage bias of HRS, slope is close to 2 for HRS at large bias. 85

Figure 5.4 Temperature dependent resistance plot with activation energy fitting. 87

Figure 5.5 Current voltage curves for the fresh state of devices with different areas. It clearly shows four current levels in accordance with device areas. 88

Figure 5.6 (a) Current voltage curves of HRS states for different areas. It shows clearly four current levels in accordance with device areas. (b) Normalized current density with device areas indicating area scaling property of HRS current... 89

Figure 5.7 Current voltage curves of LRS states for different areas showing no area dependence and a linear relationship on the biasing voltage... 90

Figure 5.8 Resistance versus device area plot for fresh, HRS and LRS. For both fresh and HRS state, resistance shows a reciprocal scaling effect with respect of device areas; while for LRS, there is no dependence on device areas. 91

Figure 5.9 Normalized PSD plot for (a) Fresh (b) HRS (c) LRS states under small bias. The noise PSD is independent of bias conditions for all three states. 95

Figure 5.10 Illustration of breakdown of RRAM device applying large voltage bias without current compliance... 96

Figure 5.11 (a) Measured noise PSD of the fresh state for devices L10 to L100. (b) Area normalization on fresh PSD spectrum results in a similar noise level for all devices...... 97

Figure 5.12 (a) Measured noise PSD of the HRS state for devices L10 to L100. (b) Area normalization on HRS PSD spectrum results in a similar noise level for all devices. 98

Figure 5.13 (a) Measured noise PSD of LRS state for device L10 to L100..................... 99

Figure 5.14 Schematic of filament conduction noise model for LRS, the outer shell indicates interface trap region that will affect the conduction current........................... 101

Figure 5.15 Calculated carrier concentration with commonly accepted parameter values of filament radius (5nm to 10nm) and interface trap density (10^{10} to $10^{11}cm^{-2}eV^{-1}$) at room temperature. 102

Figure 5.16 Multi-level resistive switching in oxide-based RRAM device produced by different reset stop voltage. More levels could be achieved by carefully control measurement conditions... 104

Figure 5.17 Schematic illustration of resistance change in the memory cell. Between highly conductive LRS (top left) and highly resistive HRS (bottom left), there are intermediate resistance levels caused by reduced or partial ruptured conduction filament. 105

Figure 5.18 Normalized LFN power spectral density measured at different resistance states from a set of five L10 devices... 106

Figure 5.19 (a) PSD versus resistance plot of L10 device at 100Hz and model fitting. (b) Model fitting of PSD versus resistance plot at different frequencies 107

Figure 5.20 Normalized noise versus resistance plot of devices with four different areas and model fitting 111

Figure 6.1 High resolution TEM pictures of (a) single layer device, revealing an oxide thickness of 10nm (b) multilayer device indicating four layers of oxides between top and bottom electrodes and a total dielectric thickness of around 10 to 12nm...................... 115

Figure 6.2 EDX spatial profile of multilayer device. Two Hf and O peaks and two Ti peaks with one merging into TiN electrode signal observed, indicating four layers of oxides sandwiched in between electrodes.. 116

Figure 6.3 (a) Forming and set / reset process for single layer HfO_x control device. The conductive paths need to be formed before bipolar resistive switching cycles. The forming voltage is as large as 1.95V, which is about 0.5V larger than that of set voltage. (b) Initial set / reset process in multilayer device. No forming is needed for such devices. The voltage of first forming sweep is similar to the following set voltage and fresh resistance is also similar to that of HRS state. 118

Figure 6.4 Distribution of forming voltage for SL device and first set voltage for ML device, which shows and average difference of 0.3 to 0.5V... 120

Figure 6.5 Operation parameter comparison of 500 DC switching cycles from a single device. (a) Set voltage of SL and ML device, showing a similar distribution profile and range, with standard deviation improvement from 0.19 in SL to 0.14 in ML device. (b) Reset voltage distribution, obvious improvement can be seen in ML device, and standard deviation reduces from 0.41 to 0.12.. 121

Figure 6.6 Resistance distributions of 500 DC cycles from one device each of SL and ML structure. Inset is the LRS / HRS resistance versus cycle number plot. HRS distribution of around two orders in SL reduces to only about two times in ML device. 122

Figure 6.7 (a) Set voltage distribution (b) Reset voltage distribution of 100 switching cycles of 10 devices selected on an 8 inch wafer. For floating box chart, the top and bottom whiskers indicate 90% and 10% distribution and the box represents 75% to 25% range. 50% point is indicated as the bar inside the box and the mean value is represented as the dot inside the box.. 124

Figure 6.8 Maximum reset current of 100 switching cycles from 10 devices each from SL and ML structures. Compare to SL, ML device shows a tighter reset current distribution as well as lower amplitude. 125

Figure 6.9 HRS / LRS resistance distribution of 100 switching cycles from 10 devices each with SL and ML structures. LRS distribution is similar, while HRS distribution reduces from more than two orders in SL to only about three times for 10 devices in ML structure.. 126

Figure 6.10 Electric pulse switching of multilayer RRAM device. It shows an increasing trend in voltage amplitude as pulse width reduced. Switching speed as fast as 5ns has been demonstrated with set voltage of +2.1V and reset voltage of -3V. 127

Figure 6.11 EELS results of the fresh multilayer oxides RRAM device, showing N K-edge at 401eV, Ti $L_{3,2}$-edge at 453eV, as well as O K-edge at 532eV. The sharp rise of Ti $L_{3,2}$ edge can been seen in every oxide layer, indicating Ti diffused into both HfO_x layers. The point to point distance is 3.0 Å in the EELS line scan. N K-edge can be clearly observed in the TiN top electrode layer, while no signal in the multiple oxide layers. Oxygen atoms counts clearly show up in every oxide layer, while zero count in the TiN top electrode layer. [153] 129

Figure 6.12 Energy-loss near-edge structure (ELNES) of the TiN top electrode, first HfO_x layer, and second HfO_x layer shown in Figure 6.11, respectively. The different Ti states are labeled. The peak shifts towards a lower energy which indicates a change of the Ti ionic state. Ti in both HfO_x layers show the same onset slope shift which is ~ 1eV. [153] 131

List of Tables

Table 1 List of resistance switching materials for RRAM devices reported in the literatures [66]. 36

Table 2 Summary and comparison of device performance among several promising metal oxide based RRAM cells. 37

Chapter 1 Introduction

1.1 Background

Semiconductor industry has experienced an inconceivable growth in the past four decades. Microelectronic products has followed Gordon Moore's prediction in 1965 [1] that the number of devices which can be integrated on a chip of fixed area will double every 12 months (later amended to doubling every 18 to 24 months), better known as Moore's Law. This simple prediction unleashed a powerful economic cycle of investment followed by enhanced products that brought about new and varied applications motivating yet more investment. Thus, Moore's Law has become the driving force behind dramatic reduction in unit cost over the past few decades for memory, enabling products of ever higher density and ultimately putting enormous amount of memory in the hands of the consumer at much reduced cost.

Aggressive scaling of the semiconductor memory cells and the dramatic increase in the memory array size demand a high density, low cost, and low power consumption cell structure. DRAM dominates the volatile random access memory markets, and it is difficult to continually scale a DRAM cell with a large capacitor. Due to their short retention time of only up to a few seconds [2], it requires frequent refreshing and thus results in large power consumption even in idle state. On the other hand, Flash memory does not require refreshing, consumes less power and may achieve high array density

with stacked floating gate structure, thus explaining its success in becoming the ubiquitous nonvolatile memory in the market. Until now, Flash technology had served well for economic nonvolatile memory developments because of the scalable underlying physics, materials and fabrications [3]. However, conventional memory scaling is expected to come up against technical and physical limits in the very near future. Further scaling of both NOR and NAND Flash is projected to slow down due to a few major challenges as described in the following [4]. First of all, it is theoretically impossible to fabricate defect free tunnel oxide. And there is no way to further thin down tunnel oxide without impairing data retention for the current technology [5]. Secondly, beyond 40nm node, an effective gate coupling ratio (GCR) cannot be achieved without new innovation [6]. There are also specific issues like short channel effect when tunnel oxide stops scaling for NOR or crosstalk between adjacent cells for NAND, as well as few electron storage with scaling down of memory cell. As a result, it is necessary to identify emerging memory technologies to obtain electrical accessibility, high speed, high density, low power, as well as CMOS compatibility.

A number of alternatives to contemporary Flash memory have been extensively studied to obtain a more powerful and functional nonvolatile memory. Memory concepts that have been pursued recently range from spin-based memories (magnetoresistive random access memories, or MRAM in short, and related ideas), in which a magnetic field is involved in the resistive switching, to phase-change RAM (PCRAM), in which thermal processes control a phase transition in the switching material from the amorphous to the crystalline state. Yet another class of resistive switching phenomenon is based on the

electrically induced change of the resistance of a metal-insulator-metal (MIM) memory cell, usually referred to as resistive random access memory (RRAM or ReRAM in short). Papers at the IEDM Conference in 2007 suggested for the first time that RRAM exhibits lower programming current than PCRAM or MRAM without sacrificing programming speed, retention or endurance [7]. Furthermore, in IEDM 2008, high performance RRAM device were presented by H. Y. Lee, et al., [8] with low operation power (<3V, <0.1mA), more than 10^6 cycles of read/write and retention of 10 years at 85 ℃. With time goes, development of RRAM has drawn great attention in the electron device research.

1.2 Objectives

Resistive random access memory has emerged as one of the most promising candidates for future nonvolatile memories or universal memories [9]. Since 1960s [10], large number of materials have been explored for use as RRAM [9, 11-15]. Although most of these materials can be switched between two or more distinct resistance states by applying suitable voltage or current stress, the switching mechanism however, is believed to vary from material to material and is not fully understood. This research work aims to study the underlying physics of oxide-based RRAM switching behavior as well as current conduction mechanism in different resistance states and to optimize device performance for the implementation and integration of RRAM in CMOS circuits.

The objectives are detailed as follows:

(1) To fabricate and investigate oxide-based RRAM devices with both physical and electrical analysis. And to correlate results from both analyses.

(2) To clarify the oxide-based RRAM switching behaviours and its physical mechanisms, with the aim to understand: the formation process and the characteristics of oxygen vacancies and its impact to carrier transportation; as well as the impact of interface/surface of the oxide/electrode materials on the RRAM switching behaviours.

(3) To explore and verify qualitative or quantitative physical models for the resistive switching behaviours. These models would then be able to help serve as a guiding principle to design high-performance RRAM devices.

(4) To investigate current conduction in different states in order to better understand the switching behavior.

(5) To design and realize high performance RRAM devices (with low operating voltage, fast programming / erasing speed, high endurance, stable retention and good uniformity).

1.3 Scope of Research and Approaches

The scope of research in this work includes:

(1) Preparation of HfO_x based RRAM cell with various fabrication conditions and physical parameters for electrical and physical characterization.

(2) Physical characterization of HfO_x based RRAM cells, including morphology study (SEM, cross-sectional high resolution TEM), elemental composition analyses (X-ray

photoelectron spectroscopy, Energy-dispersive X-ray spectroscopy, electron energy loss spectroscopy), etc.

(3) Electrical investigation of memory behaviors including forming process, switching characteristics, transition voltages (set / reset voltage), and retention behaviors.

(4) Study of temperature influence on switching characteristics so as to get a better understanding of switching mechanism.

(5) Investigation of bias-temperature instability on device retention behaviors.

(6) Current conduction investigation of different resistance states with low frequency noise analysis.

(7) Device performance improvement with material-oriented optimization.

1.4 Major Contributions of the Thesis

This work mainly focuses on fabrication and characterization of the resistive switching behaviors of HfO_x based RRAM memory cells. High performance devices based on TiN / HfO_x/ Pt structure has been demonstrated and its resistive switching and retention under voltage and temperature bias have been investigated. The switching phenomena can be explained as formation and rupture of oxygen vacancies related conduction filaments [16]. It is observed that with increasing temperature, 1) high resistance state (HRS) leakage increases, which may be due to higher density of oxygen vacancy related defects giving rise to the trap-assisted tunneling current; 2) set/reset voltage decreases, which may be due to an effectively lowered potential barrier for oxygen vacancy formation and

recovery and high oxygen ion mobility; 3) multi-bit switching at room temperature may not be retained at high temperature due to high leakage of HRS at high temperatures.

To further investigate on the current conduction mechanism, low frequency noise (LFN) analysis has been implemented on devices with different dimensions. Together with direct current (DC) voltage characteristics, it is confirmed that, for the LRS, current conduction is localized without an area dependence, whereas, for the HRS, it is a uniform leakage current throughout the whole device area. A LFN model is proposed for the filamentary low resistance state based on the carrier number fluctuation approach, allowing electrical analysis of filament characteristics and the surrounding trap concentration. In addition, current conduction of different resistance states has been studied with LFN analysis. A model consisting of two parallel resistances from conductive filament and uniform leakage oxide is proposed to represent the conduction in filamentary switching RRAM cell. It is found that in the low resistance regime, filament resistance dominates current conduction and noise behavior which varies nearly to the square of resistance variable; while in the high resistance regime, uniform oxide leakage is the major source of conduction, it gives a nearly constant noise level.

With the information of filament type switching in HfOx based RRAM cell, device performance has been improved with multilayer structure of switching dielectrics. Significantly improved uniformity of the device parameters (for cycle-to-cycle within the same device, and device-to-device) such as set voltage, reset voltage / current, and on & off state resistance distribution are successfully demonstrated on HfO_x/TiO_x multilayer

based resistive switching devices, as compared with HfO_x based single layer devices. In addition, such multilayer devices are free from forming process, which is greatly beneficial from the viewpoint of RRAM circuit operation. To probe the chemical origin of the forming free behavior in such device, detailed physical analysis is applied. It is believed that both the Ti doping effect and the confinement of conduction filament within different dielectrics layers contribute to the improvement.

1.5 Organization of the Thesis

This thesis consists of seven chapters: Chapter 1 introduces the background of RRAM developments, objectives of this research work, scopes and contributions of the report.

Chapter 2 presents the literature survey on resistive switching phenomenon and classification of switching mechanisms. A few commonly accepted mechanisms are discussed in details.

Device fabrication process flow and description of tools used for physical and electrical characterization tools and techniques are presented in Chapter 3.

Chapter 4 focuses on the investigation of resistive switching mechanism. This chapter describes the voltage bias and temperature instability of resistive switching and data

retention. A qualitative model of resistive switching in HfO_x based RRAM device will also be presented.

Current conduction is studied in detail with low frequency noise analysis in Chapter 5. A conduction model consisting of two parallel resistances from the filament and uniform leakage oxide is proposed to represent the conduction in filamentary switching RRAM, as well as a LFN model is depicted for LRS quantitatively.

Chapter 6 demonstrates forming free RRAM devices with excellent uniformity by implementing multilayer dielectric structure. Tight operation parameter distribution has been achieved in HfO_x / TiO_x multilayer structure and the resistive switching uniformity has been significantly improved. Physical analysis is applied to probe the origin of forming free behavior in such device.

Summary and conclusions of resistive switching in oxide based RRAM devices as well as suggestions and recommendations for future studies are detailed in Chapter 7.

Chapter 2 Literature Review

2.1 Introduction

This chapter provides an overview of development of RRAM as nonvolatile memory, which had been reported in the literature. A few emerging memory technologies are introduced briefly. Classification of switching behavior is described, and a few dominant switching mechanisms are discussed.

2.2 Nonvolatile Memory and Emerging Memory Technologies

There are two major types of memories in today's semiconductor markets, namely volatile and nonvolatile. The former loses any data as soon as the power supply is turned off, therefore, it requiring constant power to be applied for the device to remain operational. The most common volatile memory is random access memory (RAM). In comparison, the later memory retains its data even when the power to the system or device is turned off. Data retention is typically measured in terms of years while stimulating operation at high temperatures. The most important nonvolatile memory is Flash memory, based on the concept of floating gate. Flash memory was first proposed

by Kahng and Sze in 1967 [17]. A typical Flash nonvolatile memory device is similar to a MOS transistor that has a source, a drain, an access (a control gate), and a floating gate. Compared with standard MOSFET the difference lies in the floating gate, which is electrically isolated, or "floating" as shown in Figure 2.1.

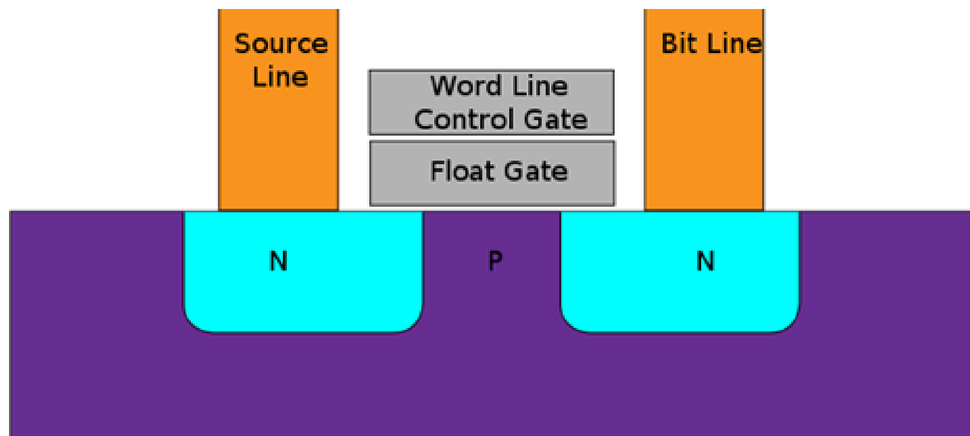


Figure 2.1 Schematic of a floating gate Flash memory cell [18]

In the last decade, the expansion of portable electronic system market has been sustained by the availability of nonvolatile memory, the key technology being Flash. However, further scaling of both NOR and NAND Flash is projected to slow down due to a few scientific and technological challenges. First one is the tunnel oxide, which cannot be further thinned down without impairing data retention. Moreover, as the device scales down, the number of electrons that can be stored on the floating gate and present in the device channel decreases to a very low level. Negative effects such as random telegraph noise arising from trapping processes are expected to cause reading errors and threshold

voltage instability as few electrons are involved in the scaled devices [19]. On the other hand, the requirements on data retention become even more challenging. Going beyond 40nm node, the maximum acceptable leakage over a ten years period should be less than 10 electrons per cell [20]. All these difficulties, arising from fundamental limitation of the charge storage concept, are calling for emerging non-volatile memory technologies at the nanoscale.

Various alternative memory concepts have been explored in the last few decades. Memories based on switchable resistors are considered promising. One of them is the phase change memory (PCM). first proposed by J.F. Dewald and S.R. Ovshinsky who, in the 1960's, reported the observation of a reversible memory switching in chalcogenide materials [21]. Chalcogenides are semiconductor glasses that are made from elements belonging to group VI of the periodic table, many of them had shown desired material properties for possible usage in PCM application [22-25].

Figure 2.2 shows the schematic of vertical OUM (Ovonic Unified Memory) PCM memory element in the so-called Lance-like structure. It has a sandwiched configuration with several functional layers. The active phase-change material ($Ge_2Sb_2Te_5$ – GST) is placed between a top metal electrode and a resistive bottom electrode (also called heater). During programming, current flows vertically through the PCM cell from the bottom

electrode to the top electrode. The narrow heater to GST contact concentrates current flowing through and results in local heating of active GST in a semispherical volume where phase change between amorphous and crystalline phase occurs. The two phases of chalcogenide are quite different in resistances, which represents '0' and '1' for data storage respectively. Physical scaling limitation does not seem to pose any problems for phase change mechanism at least down to 5nm [26]. However, PCM cell requires very large current density to initiate phase change; the high power consumption is one of its major drawbacks [27], especially in today's ultra large scale integration (ULSI) circuit, where power density is one of the major concerns.

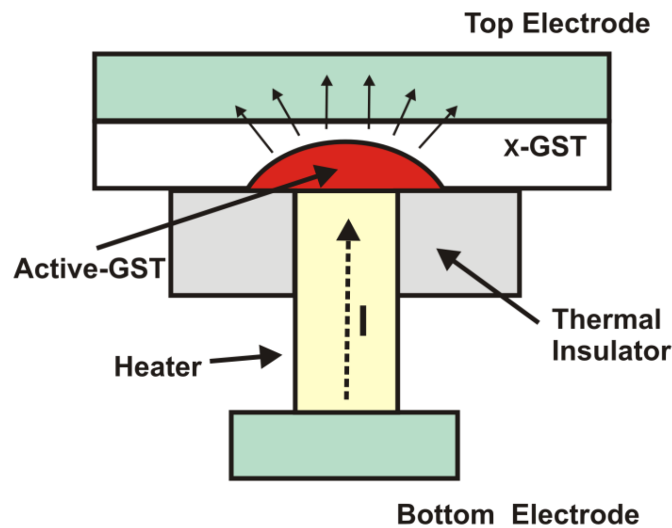


Figure 2.2 Schematic of the OUM vertical phase-change memory element: Amorphization of this region stops the low-resistive current path and results in an overall large resistance. [28]

Another nonvolatile memory technology developed since 1990s is MRAM, short form of magnetoresistive random access memory. Unlike other RAM chip technologies which

stores data as electric charge or current flows, MRAM keeps information by magnetic storage elements. The elements are formed from two magnetic plates and separated by a thin insulating layer as shown below in Figure 2.3. One of the two plates is a permanent magnet set to a particular polarity; the other's field can be changed according to external field.

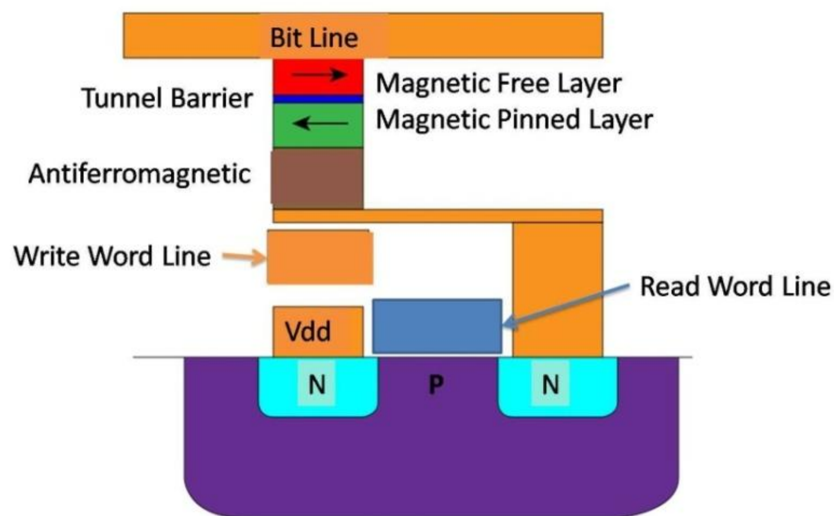


Figure 2.3 Simplified structure of an conventional MRAM cell [29]

Data is written to the cells using a variety of means that are related to current induced magnetic field. Reading is accomplished by measuring the electrical resistance of the cell. Due to magnetic tunnel effect, the electrical resistance changes with the orientation of the field in the two plates. By measuring the resulting current, the resistance of any particular cell can be determined. Typically, if the two plates have the same polarity this is considered as '1'; if the two plates are of opposite polarity the resistance is higher and

recognized as '0'. In the early stage of MRAM development, it requires an external magnetic field to toggle the resistance state, giving rise to very high current and thus resulting in scaling issues [30]. However, recent research revealed the spin transfer torque RAM (STT RAM) as an attractive solution to overcome the high power consumption issue in older MRAM cells. On top of that, STT RAM has a good scalability down to $6F^2$ cell size [31-32].

Besides these memory technologies, another promising candidate is the resistive random access memory (RRAM). It has drawn great attention and been developed by many companies and institutes [33-36] due to its potential of becoming next generation NVM or universal memory.

2.3 Resistive Random Access Memory Device

In 1962, the hysteresis of current-voltage (I-V) characteristics was reported by Hickmott in metal-insulator-metal (MIM) structure of $Al/Al_2O_3/Al$ for the first time [10]. It was discovered that the resistance changes as a result of applied electric field. Subsequently, resistive switching had been reported in other binary metal oxides [37-38]. This first period of high research activity lasted up to the mid-1980s [15]. The current wave of

resistive switching for memory exploration started in the late 1990s, triggered by Asamitsu et al. [39], Kozicki et al. [40] and Beck et al. [11].

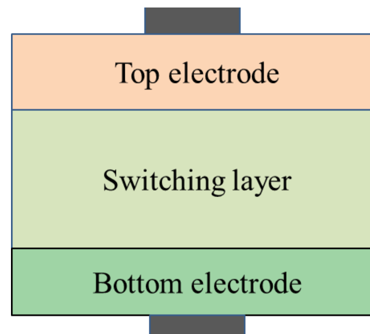


Figure 2.4 A typical metal–insulator–metal capacitor structure of RRAM device cell

RRAM memory cell has a simple MIM structure, as illustrated in Figure 2.4. Electrode materials may be same or different for top and bottom, and switching layer varies from a large range of materials [30]. Transition event from high resistance state (HRS) to low resistance state (LRS) is referred to as "set" process. The reverse transition from LRS to HRS is referred to as "reset" process. In many cases, the fresh samples have very large resistance that requires a much higher voltage stress to trigger resistive switching for subsequent cycle, this process is called "forming" process.

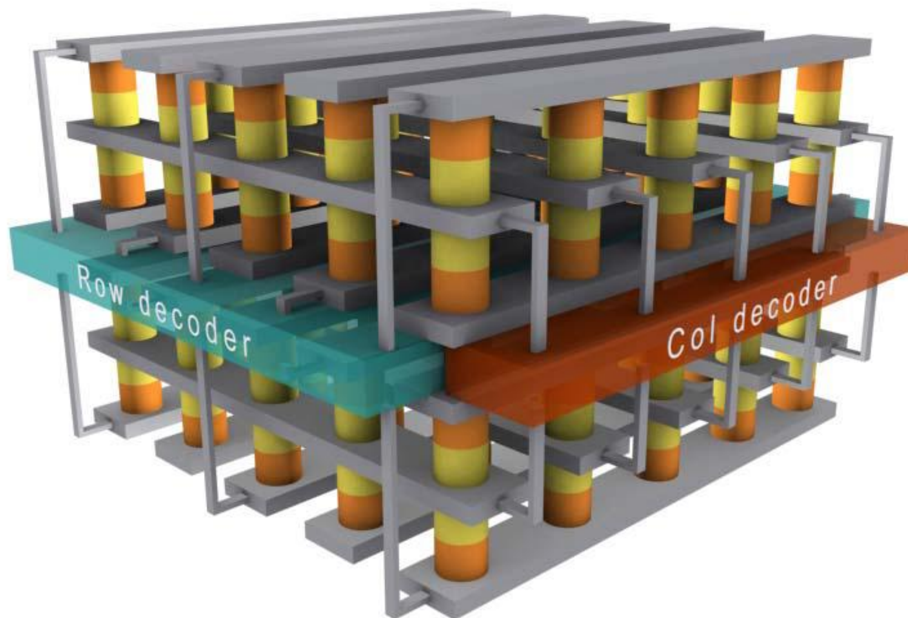


Figure 2.5 Conceptual diagram for ideal 3D NVM stacking structure utilizing stackable peripheral circuits [41]

Because of its simple sandwiched structure, it is possible to construct highly scalable cross-point and multilayer stackable structure with proper selection device [42]. Figure 2.5 is the conceptual diagram for ideal 3D stacking structure proposed by Samsung in IEDM 2008. Other than potential ultra high integration density, RRAM has advantages of nonvolatility, high speed, low power consumption, high scalability, as well as CMOS compatibility and will be discussed in detail in this work.

2.4 Classification of device operation

A commonly used classification of resistive switching is based on operation polarities, by which resistive switching can be classified into two types: unipolar or bipolar. The typical I-V curves of the two types of resistive switching are shown below.

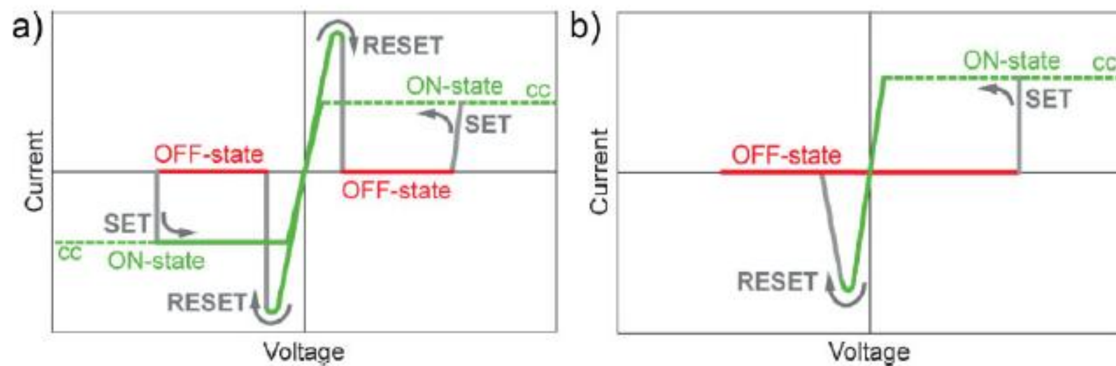


Figure 2.6 The two basic operation schemes of resistance switching memory cells. (a) unipolar switching and (b) bipolar switching. cc denotes compliance current. Dashed lines indicate that the real voltage level at the system will differ from the control voltage because of the cc in action. Please note that the I-V of real systems may deviate considerably for both operation schemes. [43]

In unipolar switching, the switching direction depends on the amplitude of the applied voltage but not the polarity [44]. An as-prepared memory cell is usually in a very high resistance state and is put into LRS by forming to trigger switching behavior. The cell in LRS can then be switched to HRS by applying a threshold voltage (reset voltage). Subsequently, switching from HRS to LRS can also be achieved by applying a voltage (set voltage). To avoid hard breakdown of the device, it is recommended to provide

current compliance via a semiconductor parameter analyzer or more practically by the selection transistor/diode or simply a series resistor in the circuit. The set voltage is always higher than the reset voltage, and the reset current is always higher than the compliance current during set process.

Bipolar resistive switching shows directional switching dependence on the polarity of the applied voltage. The set operation occurs on one polarity of the voltage or current with or without current compliance, the reset process requires the opposite polarity. Usually a forming process is required to initiate the bipolar switching behavior, but it may not be necessary for some cases. The MIM structure needs to have some asymmetry, such as different electrode materials or a dedicated voltage polarity during the initial electroforming step, in order to show bipolar switching behavior.

There are also systems that have been reported such that the operation conditions can be changed between unipolar and bipolar, and they have been named nonpolar [45]. To a certain extent, nonpolar is also a special case of unipolar switching.

2.5 Resistive Switching Mechanisms

Up to now, a wide variety of physical phenomena are known, which can in principle lead to nonvolatile resistive switching memory effects (Figure 2.7). Although the physical driving force of all these resistive switching is electrically induced, they are quite different from one another.

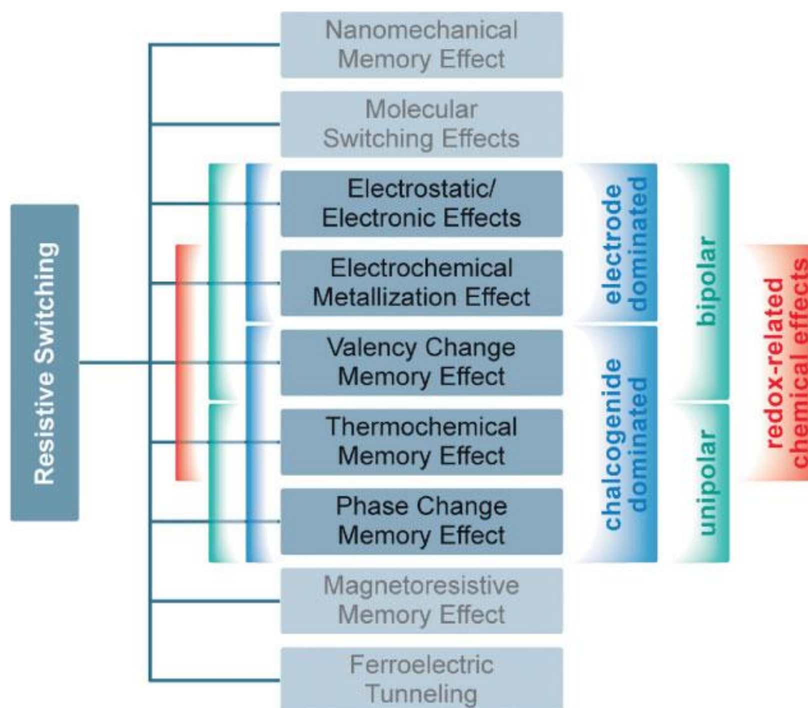


Figure 2.7 Classification of the resistive switching effects which are considered for nonvolatile memory applications. [43]

Figure 2.7 summaries nearly all resistive switching effects which are considered for nonvolatile memory application. Among these effects, mechanical forces can be utilized

in nanomechanical memory. Molecular structure changing induced resistance change may become memory device facilitating a single molecule [46]. Electrostatic and electronic effects are discussed as the possible origin of resistive switching in the literature. Alternation of ferroelectric polarization direction may be utilized to change tunnel current [47]. Phase change memory that has been developed recently relies on the temperature induced change between amorphous and crystalline phase. Redox-related chemical effects are also of great interest in resistive switching explanation. For commonly defined RRAM, it usually refers to the categories of thermochemical memory effects, electrochemical metallization effects, and valency change memory effects. Several well accepted switching mechanisms for these types of RRAM are to be discussed in details in the following part.

2.5.1Thermal Effect

One of the well-known switching mechanisms is based on thermal effect, or thermochemical memory (TCM) effect. A typical resistive switching explained by thermal effect shows a unipolar operation. The most remarkable candidate material among many is NiO, first reported about in the 1960s [38] and now has been developed by many research groups [11, 48-50]. Figure 2.8 shows a typical semi log current-voltage characteristic of NiO thin film RRAM with Pt electrodes.

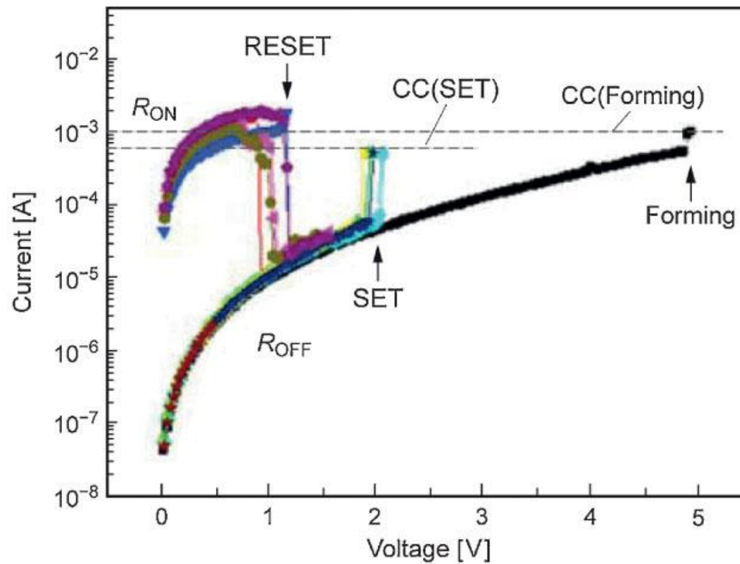


Figure 2.8 Unipolar I-V curves of a Pt/NiO/Pt stack with a NiO film thickness of 50nm [51]. Initial forming and a few cycles of set and reset processes are indicated, where current compliance is applied to forming and set processes.

As schematically depicted in Figure 2.9, resistive switching is initiated by a voltage-induced partial dielectric breakdown, after which device resistance is modified by Joule heating through a discharged filament. Within the first sweep, the cell exhibits a sudden current increase at a forming voltage (current increase is limited by a preset compliance). Subsequently, the system can be switched between two resistance states, HRS and LRS. During set process, because of the compliance current, only a weak conduction filament with controlled resistance is formed. In the reset process, this conduction filament is ruptured thermally because of high power density generated locally, similar to a traditional household fuse but on the nanoscale. Hence, this switching mechanism is also referred to as fuse / antifuse type.

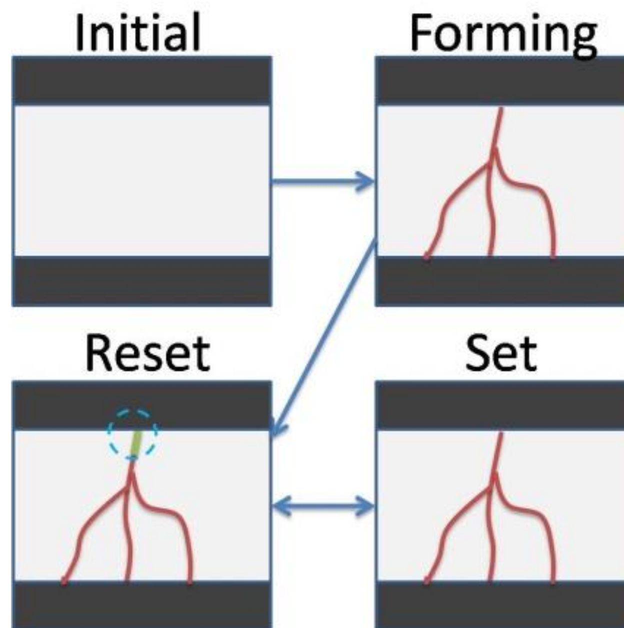


Figure 2.9 Schematics of the initial state as well as forming, reset and set process. After forming, conductive paths are formed between electrodes, and it is believed to be ruptured near metal / oxide interface

Electrical breakdown can be realized on all materials with proper electric field above a certain magnitude, and this breakdown is typically induced by a thermal runaway [52]. When an electric field (E) is applied on the insulating material, the residual conductivity (σ) leads to generation of Joule heating locally. This energy is released in the form of temperature increase and heat conduction according to,

$$\sigma E^2 = C_V \frac{\partial T}{\partial t} - \nabla \cdot (\kappa \nabla T) \tag{2.1}$$

where C_V is the specific heat per unit volume and κ is the thermal conductivity. The runaway process is caused by the conductivity change that has an exponential dependence on the temperature which is true in all insulating and semiconducting materials,

$$\sigma \sim e^{(-\frac{W_A}{kT})} \quad (2.2)$$

In this expression, W_A denotes the activation energy of the conductivity, usually caused by the temperature dependence of the carrier concentration.

The localized thermal runaway at first produces a threshold switching in which a temporary LRS is generated. If the stimulation persists, oxygen atoms drifts out of this local high temperature region and this transition state may have a structural change, which is filament formation [43]. Until here, a permanent LRS is completed, which is now a memory switching.

Direct visualization of conductive filament has been reported in Pt / TiO_2 / Pt RRAM device with the conducting nanofilament formed with magneli phase of Ti_nO_{2n-1} [53]. Evidence from recent studies involving high-resolution transmission electron microscopy (HRTEM) and electron energy loss spectroscopy (EELS) of NiO memory cells suggest that the filamentary conducting paths form in the grain boundaries [54]. Planar device

with CuO as switching layer was used for investigation by Fujiwara et al. [55] It was found that filament-like structure formation occurred between Pt electrodes during forming process. It was also shown that if this filament-like structure is cut with a focused ion beam, device switches back to high resistance. However, there are still some ongoing debates if the LRS of a MIM is caused by a single filament as indicated by an electrode area independent LRS resistance or multiple filamentary current paths, which are randomly distributed [43].

2.5.2 Electrochemical Metallization (Programmable Metallization)

Electrochemical metallization system (ECM) is also known as programmable metallization cell (PMC) or conductive bridging (CB) cell or solid-electrolyte (SE) cell in the literature. Resistive switching in this kind of cells is realized by an electrochemical metal deposition and dissolution. Figure 2.10 schematically shows the basic principle of operation in an ECM memory cell with typical current-voltage characteristics.

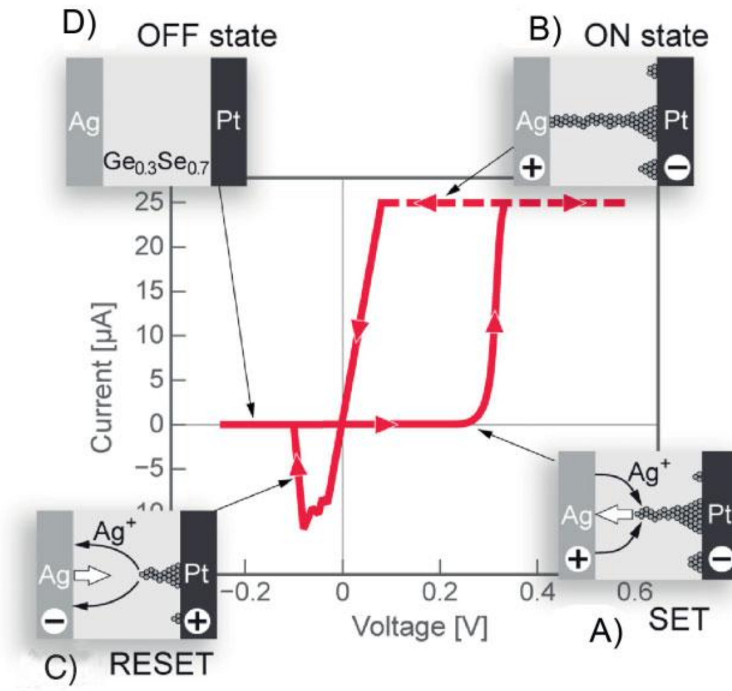


Figure 2.10 Typical current-voltage characteristic of a Ag/Ag-Ge-Se/Pt electrochemical metallization cell. The insets A to D show the different stages of the switching procedure. [56]

An ECM memory cell consists of three layers with their respective functions. One is an electrochemical-active metal electrode, such as Ag, Cu or Ni, which provides metal cations for bridge formation. Another is an electrochemical-inert counter electrode, such as Pt, Ir, W or Au, which blocks further chemical reaction. And lastly, a layer of solid-electrolyte sandwiched between two electrodes. In 1976, Hirose first reported switching behavior induced by silver dendrite formation and annihilation in As-photodoped amorphous As_2S_3 of a MIM system with lateral structure (Figure 2.11 shows lateral structure image from optical microscope) [57]. About twenty years later, Kozicki et al. successfully developed the vertical MIM configuration using GeSe as the ion conductor

and applied this idea to be used for nonvolatile memory [40]. Recently, tiny device down to 20nm has been demonstrated in the literature [58].

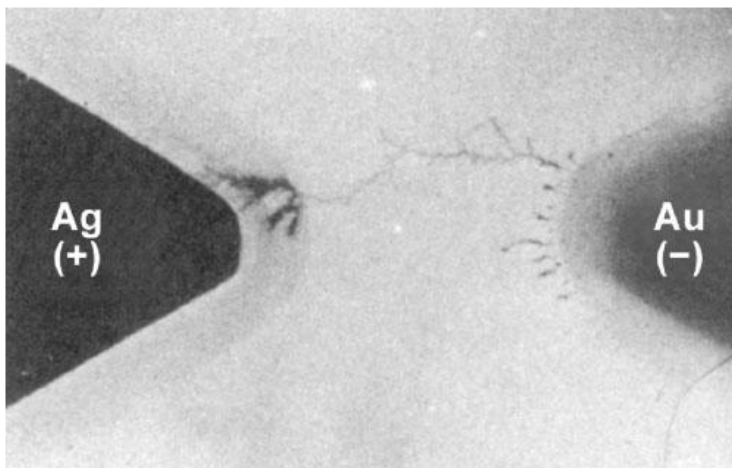


Figure 2.11 Optical microscopy image of a Ag dendrite grown from the (-)Au electrode towards (+)Ag electrode within a As_2S_3 thin film on a glass substrate. [57]

In ECM cells, resistance changes due to metal cations migration and accumulation. When a sufficiently positive bias voltage is applied to the active electrode, metal cations move towards the cathode in the force of electric field and are reduced there. Accumulated metal atoms form a bridge that propagates towards active electrode, once in contact with the anode, the device is turned on. The overall set process involves the following steps[43]:

i. Dissolution of active anode M according to reaction

$M \rightarrow M^{z+} + ze^-$

where M^{z+} represents the metal cations in the solid electrolyte thin film;

ii. Migration of M^{z+} cations across the solid-electrolyte thin film under the action of high electric field towards the inert cathode;

iii. Reduction and electrocrystallization of M on the surface of the inert electrode according to the cathodic deposition reaction

$M^{z+} + ze^{-} \rightarrow M$

As electric field is applied on the active electrode, electrocrystallization process (step iii.) is enhanced in the direction towards anode as indicated in Figure 2.10 inset A. At this time, the metal filament has grown enough to contact the active electrode; the device is switched to LRS. This low resistance can be retained after removing the electrical bias. Only when a sufficient voltage bias with opposite polarity is applied on the active electrode, this bridge then dissolves starting from the anode contact side and eventually annihilates the filament. After this, the cell is reset back to HRS state. It is worth noting that in the initial transition of reset process, there are two currents in parallel, one is an electrical current through the metallic bridge, and the other is an electrochemical current (also called Faradaic current) which dissolves the metal filament [43].

The most frequently studied ECM systems involve Ag and Cu as electrochemically active metals and phase separated amorphous selenides and sulfides as well as various oxides, acting as solid electrolytes [15]. In the past years, ECM devices has developed rapidly, switching in the nanoseconds range and on / off ratio of larger than five orders of magnitude have been demonstrated [59].

2.5.3 Valence Change Systems (Anion Migration Induced)

There are still many other switching cells that do not depend on active electrode metal penetration into dielectrics. First report of such system seems as early as 1960s in Nb / NbO films [60].

Various explanations from electronic and / or ionic mechanisms had been proposed for such devices in the literature. Several possible mechanisms for resistive switching are based on purely electronic effects. Simmons et al. suggested the charge-trap model [37] a few decades ago. In this model, charges are injected by Fowler–Nordheim tunneling at high electric fields and trapped as defects or metal nanoparticles within the insulator subsequently. Trapped charges can change the resistance of the MIM structure by modifying the electrostatic barrier, similarly to that of gate – channel resistance in the Flash FET. Another explanation of purely electronic effects happens in a strongly correlated electron system. Electronic charge injection acts like doping to induce an insulator-metal-transition (IMT) that alters system resistance as in perovskite-type oxides.

In contrast to the pure electronic effect switching, more convincing models based on anion transport especially oxygen vacancies induced resistance change had grown in the

literatures during recent years [16]. In many transition metal oxide materials, oxygen ion defects, typically oxygen vacancies are much more mobile than cations.

Enrichment or depletion of oxygen vacancies affects the valence state of the transition metal cations and may in turn lead to a considerable change in the electronic conductivity. Because of the generic character of the valence change in this class of resistive switching, it is referred to as valence change memory (VCM).

Based on the geometrical localization of switching event, there are two fundamentally different switching types within VCM, one is filamentary switching and the other is area distributed switching. In the first case, LRS conduction current is localized in a small filament range, obviously the LRS resistance is independent of the electrode area, while in the latter case, the resistance change is more or less homogeneous over the whole area, and hence, the LRS resistance is proportional to the electrode area. Only in the view point of device scaling, filament type is favored since operation window increases as cells scale down.

For filament type, switching procedures can be described as the following: oxygen ion defects (typically oxygen vacancies) are mobile in the oxide, with the presence of high

electric field, they migrate towards the cathode. If the ion exchange reaction is blocked by the cathode during electroforming process, an oxygen-deficient region starts to build and propagate towards the anode. The deficiency in ions is adapted by metal cations with cathode emitted electrons. Once transition metal cations with reduced valence states are formed, they generally turn the oxide into a highly conductive phase, which is sometimes referred to as the “virtual cathode”. When this virtual cathode approaches or almost touches the anode, the resistance of the system drops dramatically and the electroforming or set process is considered complete. In contrary to some reports in the literature, oxygen vacancies accumulate under the cathode, not under the anode. It can be explained like this: as oxygen vacancies are donors, the region in which they accumulate are n-type doped, the electric field decreases significantly in this region because of increased conductivity, leading to a decreased oxygen vacancy motion. As a consequence, the oxygen vacancies accumulate in the virtual cathode region that propagates towards the anode. Once the electroforming is completed, bipolar switching takes place through local redox reactions between the virtual cathode and the anode, by forming and breaking the conductive contact as illustrated in Figure 2.12.

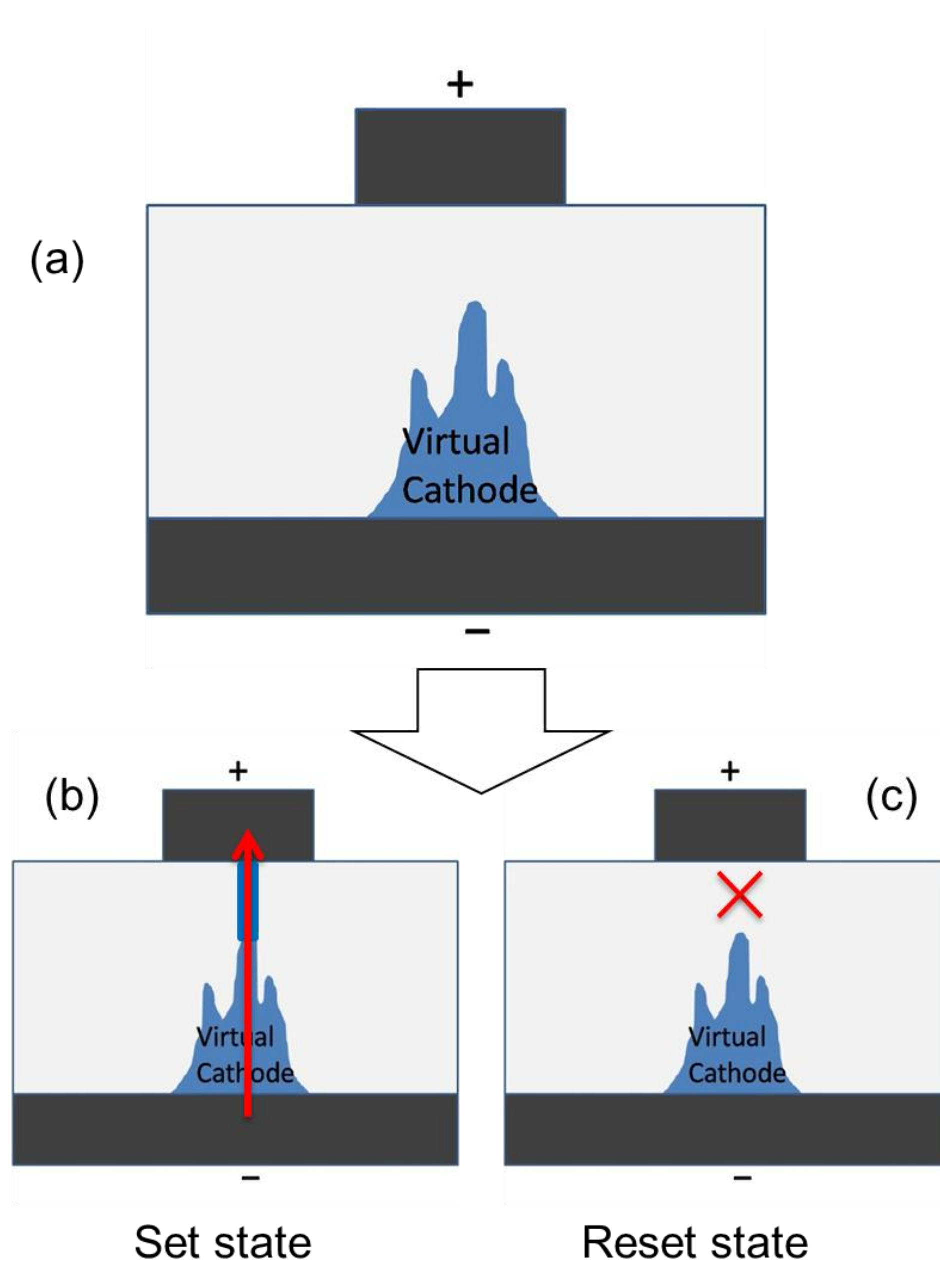


Figure 2.12 (a) Sketched cross-section of bipolar switching oxide cells indicating the virtual cathode after forming process (b) highly conductive LRS (set) state (c) highly resistive HRS (reset) state.

Since this is single filament switching, the LRS resistance is independent of the electrode area. Also, it has been reported that if the active electrode is cut into several parts after forming and switching, only one part of the cell shows resistive switching behavior while other parts exhibit very high resistance that is similar to fresh devices [61]. This is a clear evidence of single filament switching behavior after forming. For large electrode area, the on / off ratio is relatively small. This may be due to the fact that only a very small portion of the whole area is turned into conduction path and the remaining area contributes to a parallel resistance. As a consequence, the on / off ratio improves significantly with scaling on the basis that HRS is proportional to the electrode area. In this view, filamentary switching type shows excellent scaling prospects. However, the controllability of the filament formation and rupture may be an important issue.

Besides filamentary-type switching, there are also some other reports in the literature about resistive switching showing electrode area dependent LRS resistance. A so-called homogeneous interface-type resistive switching had been reported by Sawa [62], which was observed in different conductive oxide and metal electrode stacks. For this type of switching cells, the device resistance scales with area and the change of resistance is attributed to modification of Schottky-barrier at the interface homogeneously distributed over the entire electrode area, which is induced by the electric field.

Meyer et al. presented another remarkable design of resistive switching cells with well-controlled parameters in 2008 [63]. In their design, it introduced an additional tunneling oxide (TO) between electrode and conductive metal oxide (CMO). Resistive switching in this kind of cells is attributed to the modulation of potential barrier height of tunneling oxide by electric field induced oxygen ion transfer between the conductive oxide and the insulating tunneling oxide as sketched in Figure 2.13 (a). The resistive switching in the memory cell can be understood in terms of a variation of the space charge in the tunneling oxide which is due to oxygen ions from conductive metal oxide layer, resulting in a corresponding variation of tunneling barrier. When a proper positive voltage is applied, oxygen ions are attracted from the adjacent region of the CMO into the TO resulting in an increase of effective tunnel barrier height and thus, the resistance of the cell increases. In contrary, a negative voltage repels oxygen ions from the TO, reducing tunnel barrier height, leading to a high conductive state.

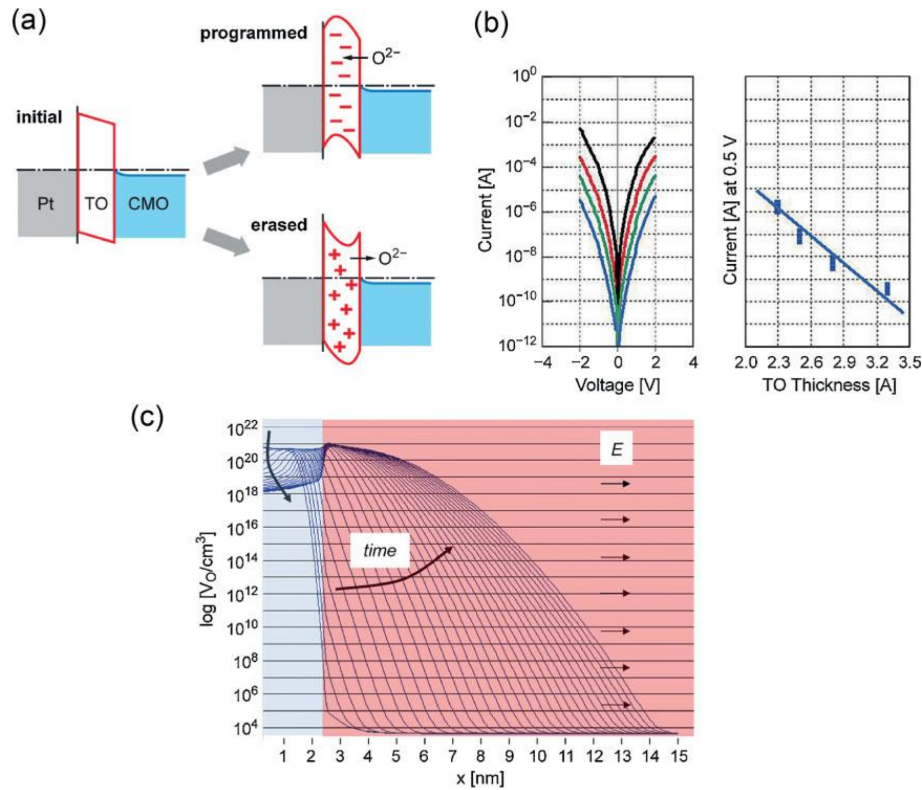


Figure 2.13 Active electrode interface of the oxide dual-layer memory concept. [63] (a) Sketch of the potential barrier for initial, programmed (reset) and erased (set) memory cell. (b) Cell characteristic as a function of tunneling oxide thickness and scaling of the current with tunneling oxide thickness. (c) Simulated evolution of the oxygen vacancy profile with time during reset.

Excellent scaling of the read and write current proportional to the electrode area and an exponential dependence of the current on the barrier thickness (Figure 2.13 (b)) indicates a homogeneous interface-type switching rather than a filamentary switching mechanism in this design. Simulation is implemented to calculate the oxygen motion across the interface in more details. Figure 2.13 (c) shows the simulated evolution of the oxygen vacancies profile during set process.

Although the interface-type resistive switching cells described above show improved device homogeneity and well-behaved scaling properties compared to filament-type switching cell, it cannot be concluded that the movement of ions and electrons occurs completely homogeneously over the whole device area. In contrast to the assumption of a homogeneous charge transport, it had been reported for PCMO [64] as well for Nb-doped STO [65] that the conductivity of these materials is strongly inhomogeneous. Due to the statistical distribution of these inhomogeneous conductive sites on the nanoscale, the properties of the above mentioned devices may scale with the area for device dimensions in micrometer range, but may differ in the nanometer range. Thus, scaling experiments down to nanometer scale have to be performed for clarification.

2.5 Metal-Oxide Based Material Stacks for RRAM

Resistive switching phenomena have been observed in a large variety of material stacks for MIM structure. Research activities have been carried out among universities, research institutes as well as industries. Table 1 below summarizes resistive switching materials reported in the literatures.

Table 1 List of resistance switching materials for RRAM devices reported in the literatures [66].

Binary Metal Oxide	HfO_x, ZrO_x, TaO_x, NiO_x, NbO_x, TiO_x, CuO_x, AlO_x, MnO_x, WO_x,, VO_x, MgO_x …
Perovskite	PCMO($Pr_{0.7}Ca_{0.3}MnO_3$), LCMO($La_{1-x}Ca_xMnO_3$), BSCFO($Ba_{0.5}Sr_{0.5}Co_{0.8}Fe_{0.2}O_{3-\xi}$), YBCO($YBa_2Cu_3O_{7-x}$), (Ba,Sr)$TiO_3$(Cr,Nb-doped), $SrZrO_3$(Cr,V-doped), (La,Sr)MnO_3, $Sr_{1-x}La_xTiO_3$, $La_{1-x}Sr_xFeO_3$, $La_{1-x}Sr_xCoO$, $SrFeO_{2.7}$, $LaCoO_3$, $RuSr_2GdCu_2O_3$, $YBa_2Cu_3O_7$, $SrTiO_3$, $SrZrO_3$…
Others	Ge_xSe_{1-x}(Ag,Cu,Te-doped), Ag_2S, Cu_2S, CdS, ZnS,CeO_2, SiO_2, …

Other than those materials listed in the above table, there are also other material systems (eg. organic materials) showing resistive switching. However, considering CMOS platform compatibility, only a few promising candidates are considered for memory chip development. Among them, binary transition metal oxide takes a leading step in the selection due to their simple composition and availability in CMOS platforms. Research efforts have been made in several metal oxides, Table 2 summarizes the device performance of various RRAM cells.

Table 2 Summary and comparison of device performance among several promising metal oxide based RRAM cells.

Switching Layer	Thickness	Electrodes	Current	Voltage	Speed Endurance	Retention	Mode	Ref
HfO_2	5-20nm	Ni-TiN	<0.2mA (lowest Ic)	<1.5V (lowest Ic)	$>10^4$ (bipolar)' 10^3 (unipolar)	>20hrs @ 150C	both bipolar and unipolar	[67]
HfO_2	5-10nm	Ti-TiN	<0.3mA	<1V	(SET/RESET: 5ns/1ns 1T1R)	$>5\times10^4$s @ 85C	bipolar	[8]
HfO_2	30nm	Si-Ni	<2.5mA	<4V	(SET/RESET: 500ns/100ns)	$>10^4$s @ 85C	Unipolar	[68]
HfOx/TiOx/HfOx/TiOx	4/2/4/2nm	Pt-TiN	<1mA	<1.5V	>500 (DC)	N.A.	bipolar	[69]
ZrOx/HfOx	NS/3nm	Pt	N.A.	N.A.	N.A.	N.A.	bipolar	[70]
SiO_x/HfSiON	2.5nm	Si-NiSi	<0.2mA	<4V	>50 (DC)	$>10^4$s @ 150C	both bipolar and unipolar	[71]
HfO_2/Al_2O_3	4.2nm	Si-Ni	<1mA	<1.5V	$>10^6$ (SET/RESET: 10ns/30ns)	$>7\times10^3$s @ 120C	unipolar	[72]
NbO	40nm	Pt-Pt	<10mA	<4V	>150 (DC)	N.A.	unipolar	[73]
Ta2O5/TaOx	5/20nm	Pt-Pt	<0.1mA	<2.5V	>106 (SET/RESET: 10µs/10µs)	N.A.	bipolar	[74]
Ti/TiO2	5/20nm	TiN-TiN	<1mA	<1.5V	NS	N.A.	bipolar	[75]
Ti/HfO2	10/5nm	TiN-TiN	<1mA	<2V	>4×104 (SET/RESET: 0.5ms/0.5ms)	>3×104s @ 200C	bipolar	[76]
WOx	46nm	W-Pt	<5mA	<1.2V	>107 (SET/RESET: 10µs/10µs)	N.A.	bipolar	[77]
ZrO2	19nm	Pt-Ti	<25µA (single level)	<3V	$>4\times10^3$	26400s (150C) 11000s (175C) 470s (200C)	bipolar	[78]
NiO	35nm	W-Au	<4mA	<1.5V	>200 (DC)	$>3\times10^6$s @ 125C	unipolar	[79]
TaO_x	~40nm	Pt-Pt	<0.1A	<2.5V	N.A.	N.A.	bipolar with Ta_2O_5 layer	[80]
TiO:Gd	40nm	Pt-W	<15mA	<1.5V	N.A.	N.A.	unipolar	[81]
TiO_2	60nm	Pt-Pt	<10mA	N.A.	$>4\times10^3$	N.A.	bipolar	[82]
ZnO:La	200nm	Pt-Si	<20mA	<3V	>150 (DC)	$>10^6$s	bipolar	[83]
ZnO, NiO/ZnO or WO_3/ZnO	50, 50/50 or 50/50nm	Pt-Au	<10mA	<2V	N.A.	N.A.	unipolar	[73]
$Zn_{0.98}Cu_{0.02}O$	80nm	ITO-Ag	<20mA	<15V	N.A.	$>10^3$s	both bipolar and unipolar	[84]
$ZrO_2/Cu/ZrO_2$	20/3/20nm	Pt-Cu	<70mA	<2.5V	N.A.	N.A.	unipolar	[85]

2.7 Summary

As Flash memory approaches scaling limitations in the near future, several emerging memory technologies are briefly discussed here. An overview of the development of resistive random access memory is presented in details. Based on operation scheme, it is divided into unipolar and bipolar devices. Three possible switching mechanisms are introduced, although the physics behind these mechanisms are still under debate. In order to better understand resistive switching phenomena and improve device performances, more detailed physical and electrical analyses are needed.

Chapter 3 Experiments

3.1 Introduction

In order to study resistive switching behavior and investigate current conduction mechanism in oxide-based RRAM devices, memory cells mainly with HfO_x dielectrics are fabricated. Both physical and electrical characterizations are performed on these devices. This chapter describes fabrication process, electrical measurement methods as well as physical analysis tools used.

3.2 Device fabrication techniques

Basic RRAM device cell has a simple metal - insulator - metal capacitor structure; fabrication of metal oxide-based memory device can be done with conventional CMOS semiconductor fabrication process. The most common deposition technique of the switching oxide layer is sputtering of metal followed by oxygen annealing or reactive sputtering in oxygen ambient [86]. Other deposition methods are also utilized in the literature, including atomic layer deposition (ALD) [8, 13], metal organic chemical vapor deposition (MOCVD) [87], pulsed laser deposition (PLD) [88] and sol-gel spin on [89-90]. Some papers also report resistive switching in self-assembly NiO nanowire [49, 91] or ZnO nanorod structures [92]. The thickness of the oxide usually ranges from a few nanometers to about 100nm. For the most cases, the substrate used is silicon, which is the

most common material for integrated circuits. However, there are some other efforts to fabricate memory cell on transparent substrate like glass [93] or flexible substrate like polymer sheet [90, 94], for some special applications, e.g. inexpensive flexible lightweight portable electronics.

In this study, resistive switching devices with HfO_x as the dielectric are fabricated. TiN and Pt are used as the top and bottom electrode respectively. All fabrication processes are done in the ---Nanyang Nanofabrication Centre (N2FC) Clean Room 1 (CR1) and Clean Room (CR2) and clean rooms in Institute of Microelectronics.

Figure 3.1 shows the basic capacitor structure of the RRAM cell, and Figure 3.2 shows the simple mask design for top electrode definition with different dimensions. For quick run devices, only one mask is used to define top electrode and probing position is indicated in Figure 3.1. There are also three masks cross-bar structure devices and samples with passivation glass design, for which the fabrication details are not shown here.

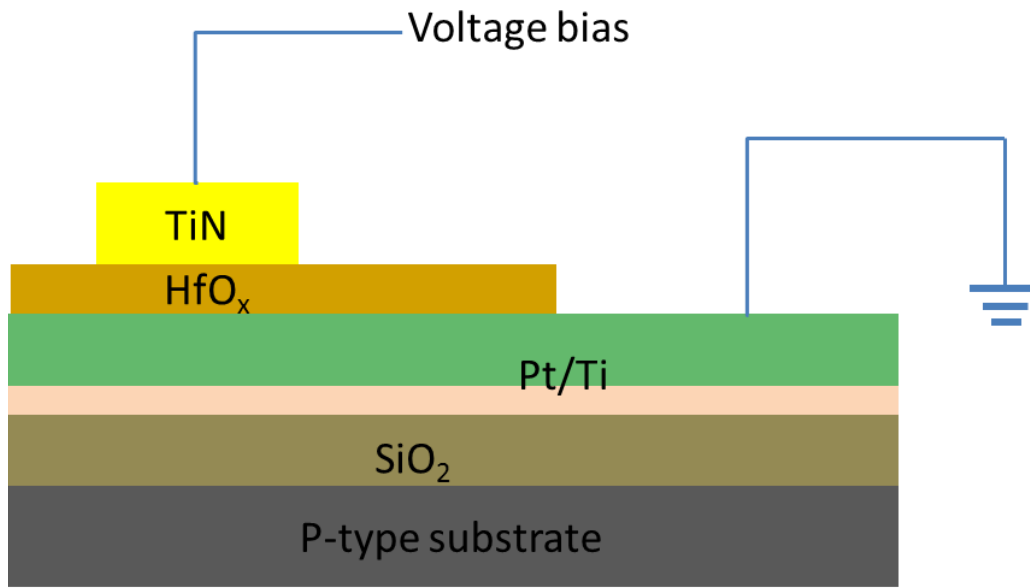


Figure 3.1 Basic capacitor structure of RRAM cell in this work with TiN and Pt as electrodes. Probing positions during measurement are also indicated.

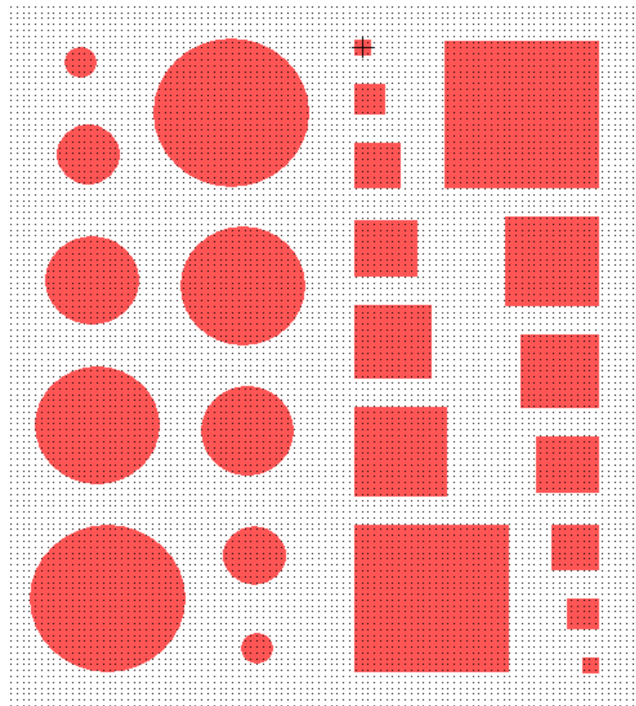


Figure 3.2 Basic mask layout for top electrode patterning with different dimensions

3.3 Fabrication Process Flow

Since this is CMOS compatible fabrication, processes are mostly done with conventional CMOS fabrication tools. Process flow of the basic capacitor fabrication is shown in the following chart and discussed in details below.

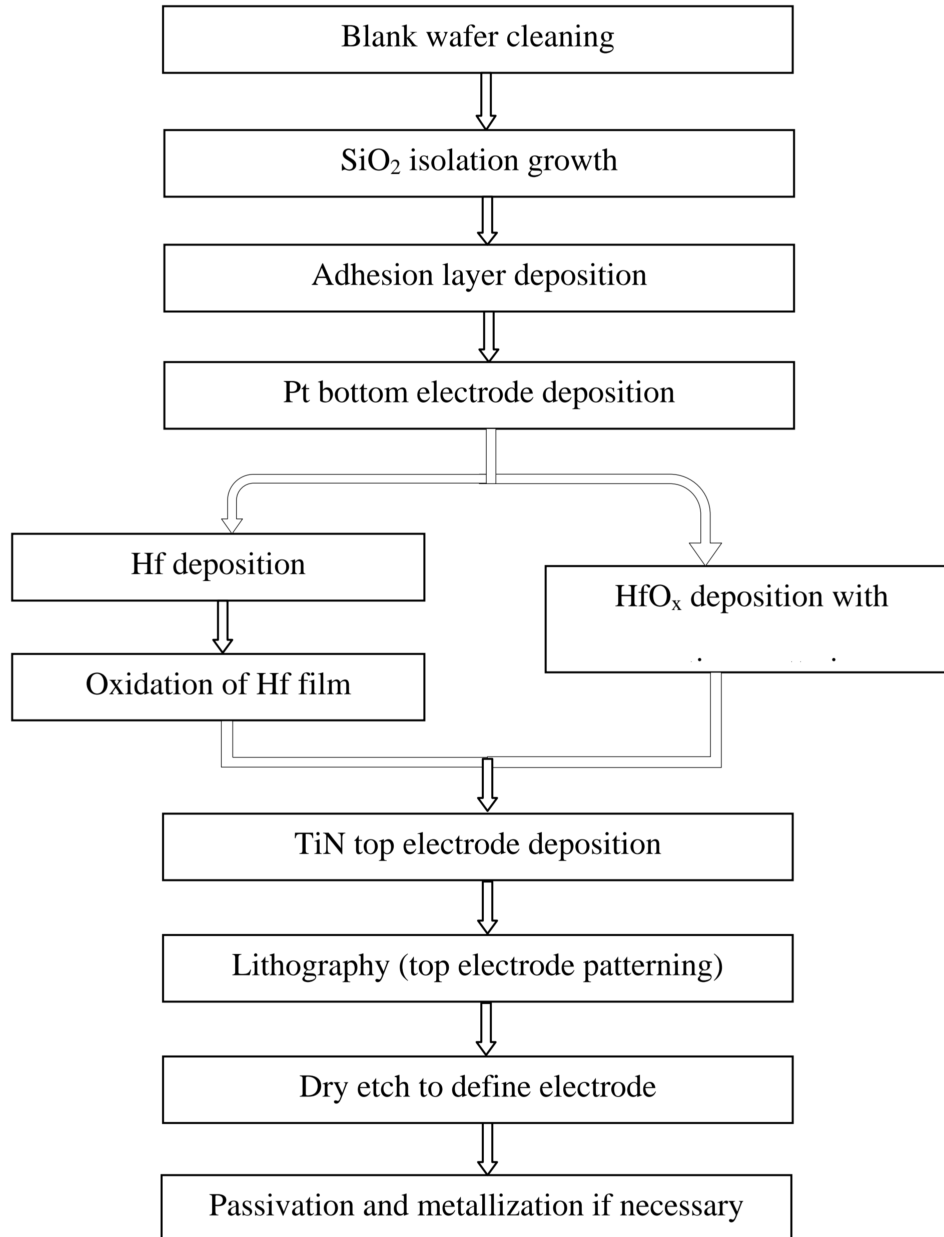


Figure 3.3 Baseline flowchart of MIM capacitor structure fabrication

i. Blank wafer cleaning: standard RCA cleaning is used for wafer cleaning. Two sequential cleaning solutions, NH_4OH- H_2O_2-H_2O (called standard cleaning 1 (SC-1), a composition of 1: 1: 5 to 1: 2: 7 at 70 to 80 ^oC) and HC1-H_2O_2-H_2O(called standard cleaning 2 (SC-2), a composition of 1: 1: 6 to 1: 2: 8 at 70 to 80 ^oC), is used to remove particles, organic and metal contaminations.

ii. Isolation field oxide growth: a thick layer of 500nm SiO_2 is grown on the blank wafer by wet oxidation in the furnace. It is used to isolate the capacitor devices from substrate.

   - The thickness is controlled by oxidation time and inspection is done with ellipsometer.
   - Since this layer is to isolate device from substrate, requirement on thickness is not critical.

iii. Adhesion layer and bottom electrode deposition: a thin layer of ~30nm Ti is deposited by sputtering or ebeam evaporation to improve adhesion between SiO_2 and Pt electrode, as pure Pt layer directly deposited on SiO_2 may peel off. After that, a 100nm Pt layer is deposited as the bottom electrode by sputtering or ebeam evaporation.

iv. HfO_x deposition by oxidation: A thin Hf film is deposited by sputtering with different thickness in a high vacuum base pressure at room temperature. Then sample is

oxidized in the oxygen ambient in alloy furnace, at different temperatures ranging from 450°C to 800°C and for different time durations of 5 to 20 minutes. Rapid thermal process (RTP) with oxygen ambient is also tested.

v. Top electrode deposition: a 100nm thick TiN is deposited by reactive sputtering in Clusterline 200 with a high vacuum base pressure of 10^{-8} mbar and a Ti to N ratio of ~ 2:1.

vi. Lithography steps include: i) mask cleaning in acetone and IPA (isopropyl alcohol), and then baking to evaporate residue water droplets; ii) photoresist (PR) spin coating (PR5214); iii) pre-bake at 105°C for 105 seconds; iv) exposure under UV light; v) develop in AZ developer for 60 seconds; vi) post bake at 110°C for 10 minutes to harden the PR for etching.

- The above describes the way to use the PR positively for etching. It is possible to use it as a negative PR for lift-off process, when the metal electrode material is difficult to be etched, e.g. Ni, Pt. In such case, fabrication process flow is a bit different.

vii. Dry etching and photoresist strip: A chlorine based dry etching recipe is used to etch the TiN in a metal etcher to define top electrode patterns. Etching time is proportional to the thickness of the metal. Etching stop time is determined with end point detection plus a 15 to 20 percent over etch in the machine to ensure total removal of the metal electrode in the designed area.

viii. After top electrode patterning, device is ready for electrical characterizations. However, to prevent device from external contamination or oxidation, it is sometimes necessary to have passivation after all processes. This is done by covering the wafer with PECVD dielectrics (silicon oxide / nitride or both), open contact hole, and then metallization to form measurement pads.

After device fabrication, various physical and electrical characterization techniques are used to study the resistive switching in HfO_x-based RRAM devices, and the detailed results will be presented and analyzed in the following chapters.

3.4 Physical Characterization Tools

During device fabrication, it sometimes requires inspections before or after some steps. And to better understand the resistive switching behavior in HfO_x-based RRAM devices, it is necessary to know the microscopic nature of the material. For these purposes, several physical characterization tools frequently used in the project are introduced.

- Spectroscopic Ellipsometer: It is an optical tool designed for investigation of the dielectric properties (complex refractive index or dielectric function) of thin films. Figure 3.4 is the schematic illustration of an ellipsometer measurement setup. It is a very sensitive measurement technique and provides incomparable capabilities for thin film metrology. It is commonly used to characterize film thickness for single layer or

complex multilayer stacks with an excellent accuracy. In this work, it is mainly used to measure the thickness of HfO_x film through iterative fitting of optical functions and film thickness. And the value is further calibrated with TEM examination that will be introduced later.

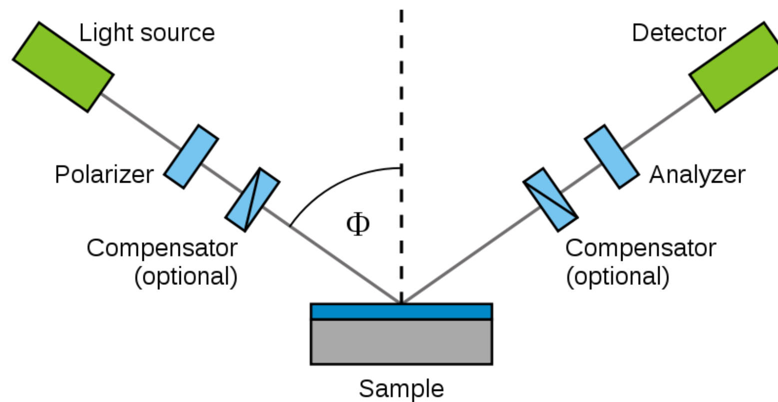


Figure 3.4 Schematic illustration of an ellipsometer measurement setup [95]

- Surface profile measuring system: This is another tool used for film thickness measurement as well as some critical dimension inspection. It works with a tiny diamond stylus (in contact with the sample surface vertically) that moves laterally across the samples surface over a specific distance. The surface profile is plotted directly with vertical stylus displacement as a function of position without any modeling [96]. It has a vertical measurement resolution around 10nm. As its resolution is not so high and sputtering deposition is nearly proportional to process time, it is practical to deposit a thick film and take the average deposition rate. For example in this project, switching oxide layer used is at the range of around 10nm,

while for profiler measurement, a thick oxide of more than 500nm is deposited and take the average deposition rate to be used for thin oxide.

- Scanning electron microscope (SEM): It works by scanning the sample surface with a high-energy electron beam in a raster scan pattern. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography and other properties. In this work, SEM is used to check the surface morphology of the deposited films. It is also used to measure thin film thickness with cross-section configuration.

Figure 3.5 Image of LEO 1550 Gemini SEM used in this work

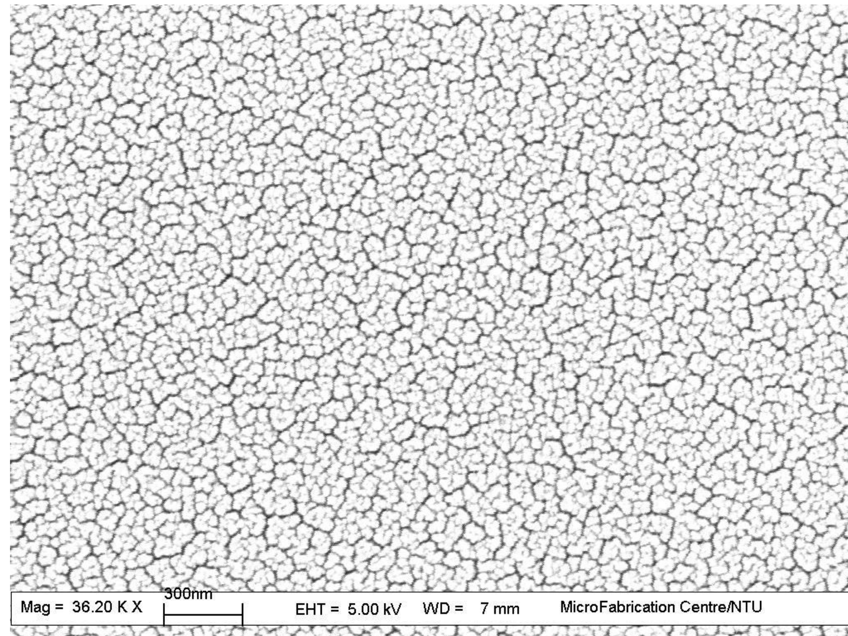


Figure 3.6 SEM image of poor quality platinum film deposited at the initial phase of this project

- Transmission electron microscope (TEM): It is a microscopy technique whereby a beam of electrons is transmitted through an ultra thin specimen, interacting with the specimen as it passes through. An image is formed with interaction of the electrons transmitted through the specimen. The image is magnified and focused onto an imaging device [97]. The TEM is capable of imaging at a significantly higher resolution than an optical microscope; it also has a higher resolution than SEM. This enables the examination of specimen details as small as a single column of atoms and such features make the TEM a powerful analysis tool in a range of scientific fields, especially in the semiconductor industry. In this work, TEM is used to image the cross-section morphology of the MIM structure.

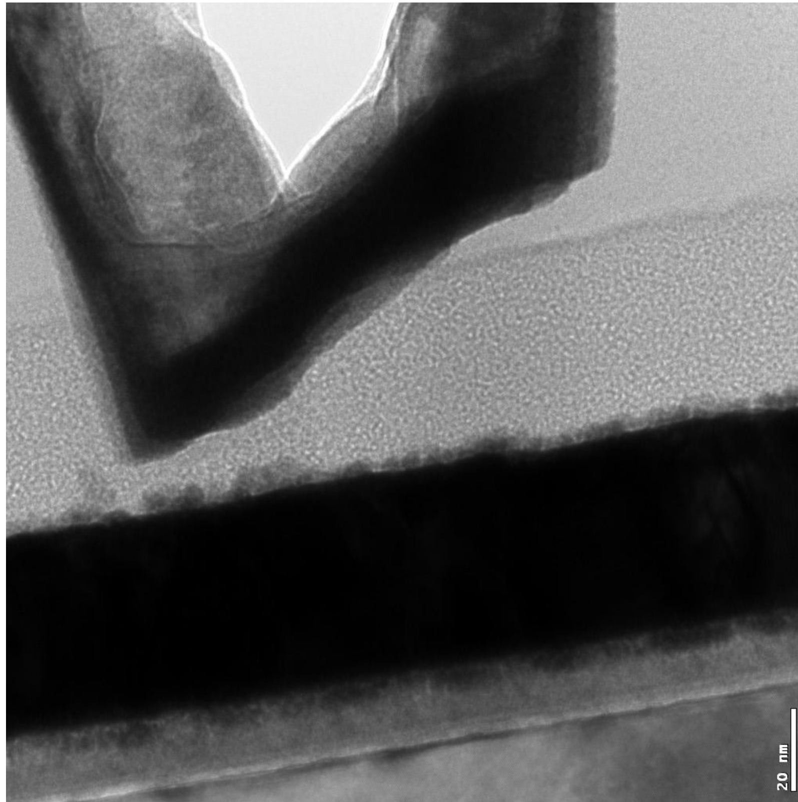


Figure 3.7 TEM image of an under etched contact hole, which causes a large contact resistance

- Atomic force microscopy (AFM): It is a very high resolution type of scanning probe microscopy used to plot surface roughness at nanoscale. The AFM consists of a tiny cantilever with a sharp tip at its end used to scan the surface of the sample. The cantilever is typically made of silicon or silicon nitride with a tip on the order of nanometers. During surface scan, the tip is brought into proximity of the sample. Atomic forces between the tip and the sample lead to a deflection of the cantilever [98]. Typically, this deflection is measured using a laser spot reflected from the top surface of the cantilever into an array of photodiodes. The collected signals are

processed with electronic circuits and the surface information is plotted. AFM is used to characterize surface roughness of the thin films in this work.

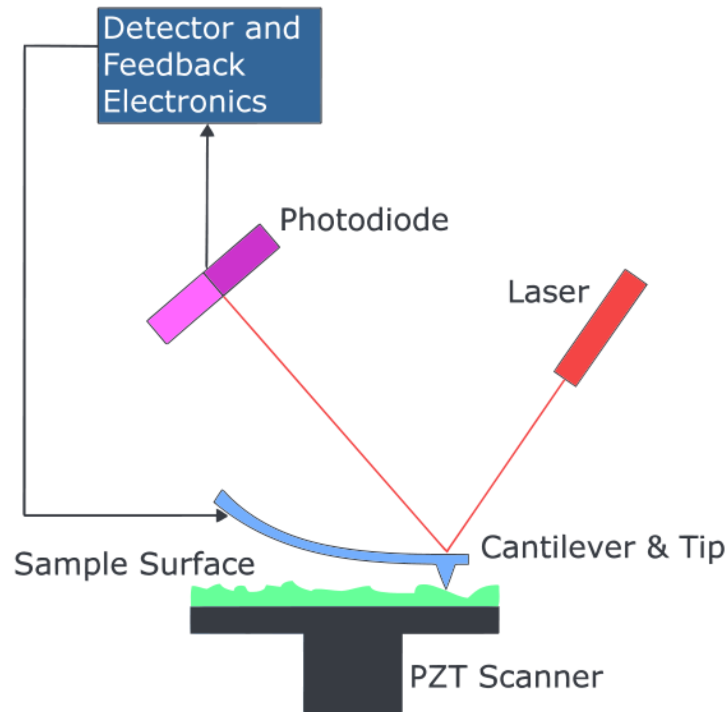


Figure 3.8 Schematic diagram of AFM operation principle [98]

- Energy dispersive X-ray spectroscopy (EDX/EDS): It is an analytical technique used for elemental analysis or chemical characterization of a sample. It relies on the investigation of a sample through interactions between electromagnetic radiation and matter, analyzing x-rays emitted by the matter in response to being hit with charged particles. Its characterization capabilities are due in large part to the fundamental principle that each element has a unique atomic structure allowing x-rays that are characteristic of an element's atomic structure to be identified uniquely from each

other [99]. In this work, EDX is used to show the elemental spatial profile of the MIM capacitor during TEM characterization.

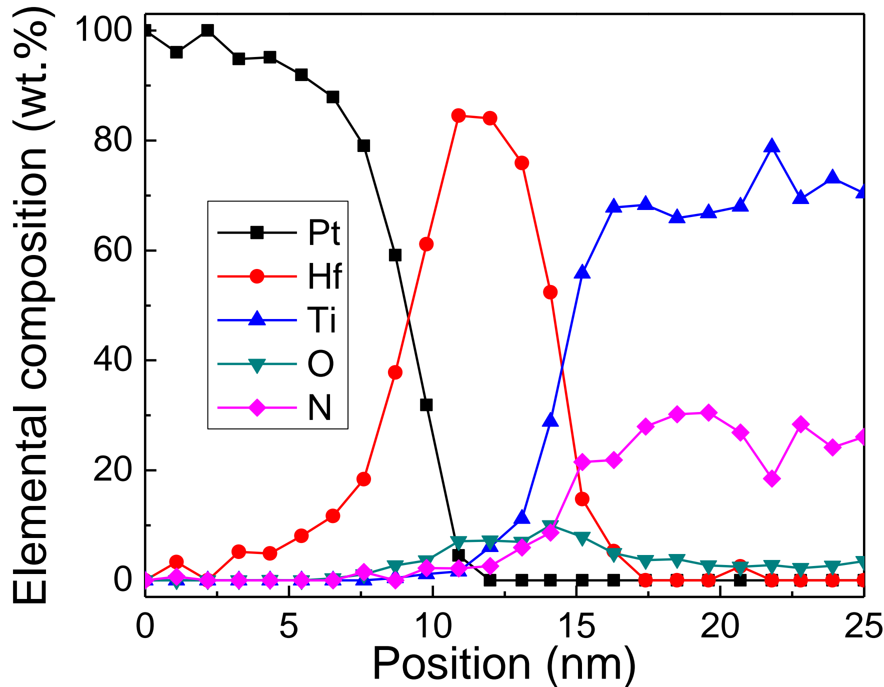


Figure 3.9 An example of EDX scan plot that reveals the spatial distribution of elements in an Pt/HfO$_x$/TiN RRAM cell

- X-ray Photoelectron Spectroscopy (XPS) is a quantitative spectroscopic technique that measures the elemental composition, empirical formula, chemical state and electronic state of the elements that exist within a material. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy (KE) and number of electrons that escape from the top 1 to 10 nm of the material being analyzed [100]. In this work, the valence state of hafnium in the

hafnia film is confirmed by the XPS signal peaks position, and hafnium to oxygen ratio is identified by analyzing of XPS signal curve. Details of XPS results are shown in Chapter 4.

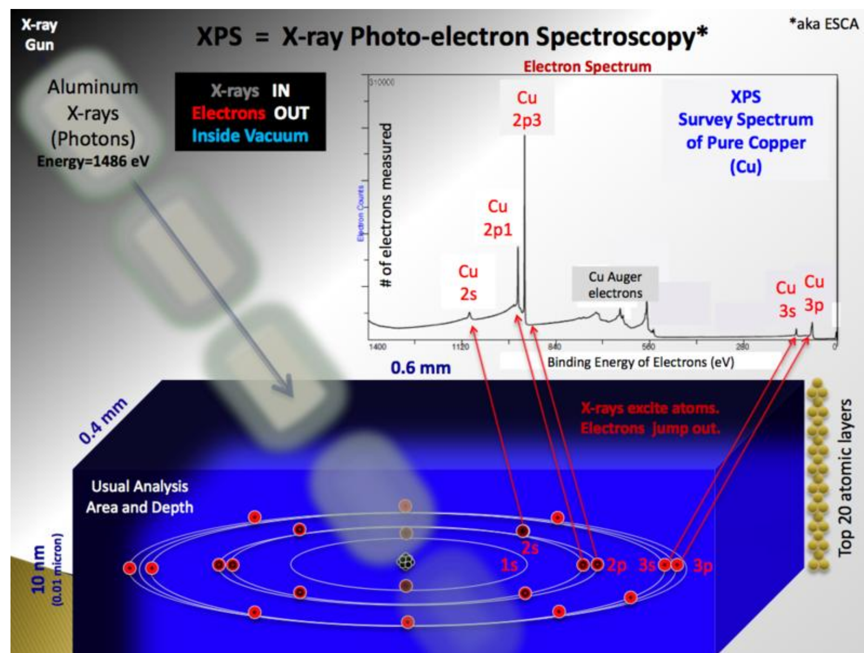


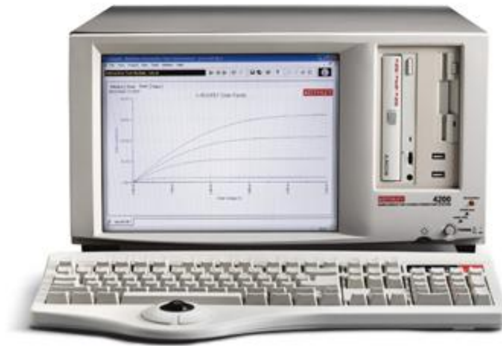
Figure 3.10 Simplified schematic illustration of how XPS works [100]

3.5 Electrical characterization

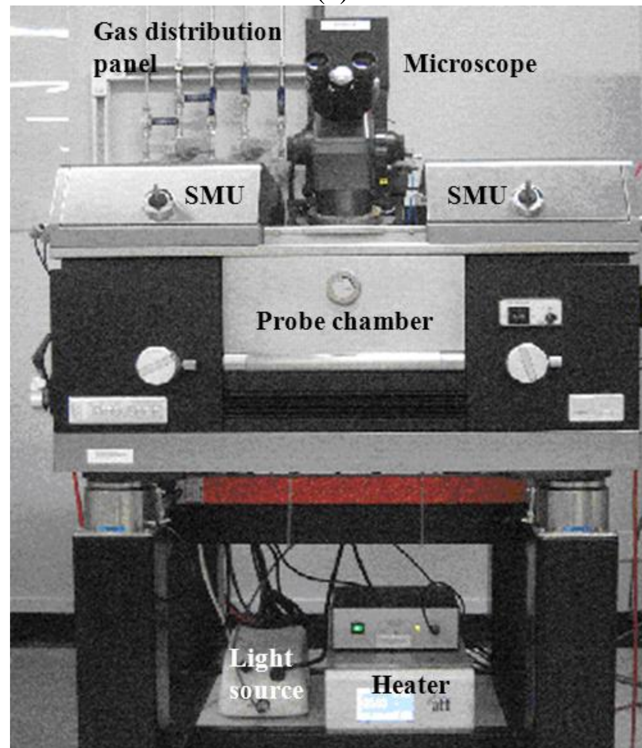
3.5.1 Equipment used for characterization

In order to study the resistive switching behavior and verify the performance of oxide-based RRAM devices, electrical characterization is carried out mainly on a Keithley 4200 Semiconductor Characterization System (SCS) connected to a SUSS 200mm manual probe station setup. For fast switching, an Agilent 81110A pulse generator (Figure 3.11 (c)) is used to provide short pulse down to the nanoseconds range. And an oscilloscope is usually connected to check the input and output waveforms.

The Keithley 4200 SCS as shown in Figure 3.11 (a) is the most frequently used electrical parameter analyzer in this project. It performs lab grade DC device characterization with advanced features such as real-time plotting, sub-femtoamp resolution and analysis with high precision. Its embedded PC with windows operating system and mass storage enables self-documentation and point-and-click interface, which speeds and simplifies the process of data collection. There are four high resolution source measurement units (SMU) that can be connected to probe heads in the SUSS probe station system via tri-axial cables with low current leakage. The SUSS probe station serves as a platform for device biasing and all related electrical measurement. The station setup consists of several components as indicated in Figure 3.11 (b): a gas distribution panel, an optical microscope for observation, a manual probe chamber with SMU connections, a vibration absorbent table, a light source and an electronic heater for temperature control.



(a)



(b)

(c)

Figure 3.11 Equipment used in electrical characterization (a) Keithley 4200 Semiconductor Characterization System (b) SUSS 200mm probe station system (c) Agilent 81110A pulse generation unit

3.5.2 Resistive switching measurement

In the chapter of literature review, resistive switching behavior (RS) is classified into two modes, unipolar and bipolar. HfOx based RRAM device with TiN as top electrode and Pt as bottom electrode shows mostly bipolar switching as shown in Figure 3.12. The most common measurement method is voltage-sweep controlled switching. In this method, a gradually changing voltage bias with constants steps is applied to the top electrode and the bottom electrode is grounded. This is called voltage sweep mode (VSM). During voltage sweep, the resistance changes from HRS to LRS and vice versa.

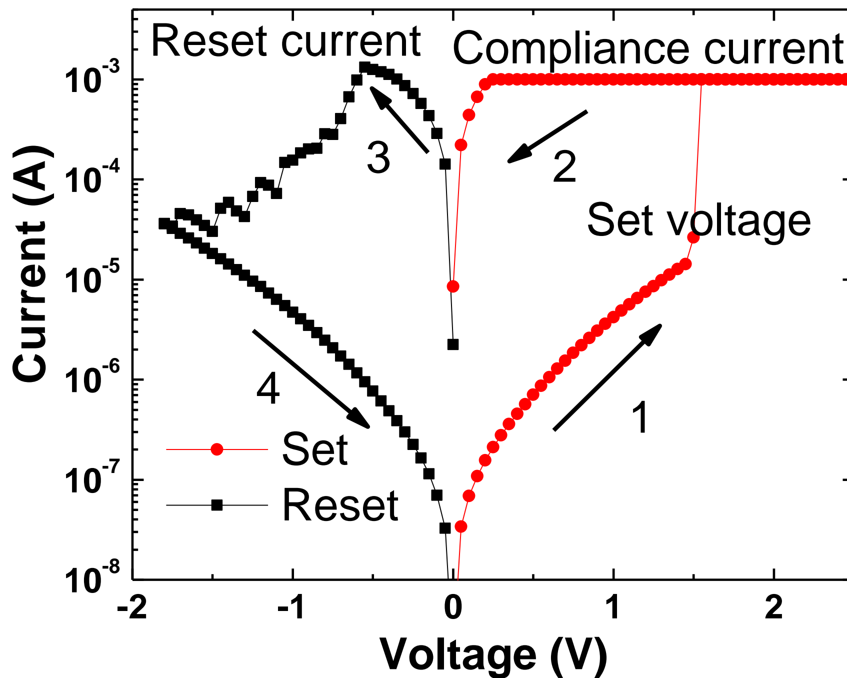


Figure 3.12 Typical DC bipolar resistive switching current-voltage characteristics of HfOx based RRAM device with TiN as top electrode and Pt as bottom electrode

As indicated in Figure 3.12, during positive voltage sweep 1 (set process), current suddenly jumps at 1.5V. This is defined as the set voltage. To avoid permanent breakdown of the device, compliance current is set at 1mA in this example. The LRS is maintained even after voltage bias is removed. While during the negative sweep 3, the current starts to drop at -0.55V. This peak value of the current is defined as the reset current and the voltage point is defined as the reset voltage. However, in some other cases, the reset voltage is defined as the point where LRS resistance increases to a certain level, e.g. 10 times of the original value. The forming process measurement is very similar to that of set and may be just different in terms of compliance current level. It is not separately discussed here.

In most bipolar VSM switching, an abrupt current jump during the set / forming process is observed. Although the current seems to be limited by the compliance in the figure, the actual transit voltage / current might be much high due to the discharge of parasitic capacitance [101]. To aim for suppression of the overshoot current during transition and inspired by current driven electroforming reported by Nauenheim *et al.* [102], current sweep mode (CSM) is proposed to improve switching uniformity [103-104]. This measurement technique is also implemented in the project. However, it does not work so well for most of the devices used in this work. There are still obvious overshoot that results in a much higher reset current than compliance value. It is worth noting that to implement CSM directly in large scale memory array is technically challenging due to the limit of pulse current operation mode in CMOS circuits. Optimization of the RRAM

cell or circuit is required, such as integration with a control transistor or a series resistor [105-106].

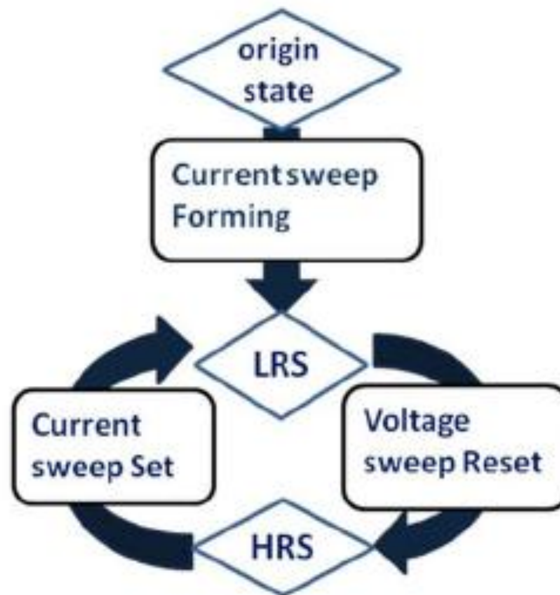


Figure 3.13 New operating scheme proposed by Chen *et al.* using CSM for forming and set and VSM for reset to improve device switching uniformity [103]

3.5.3 Retention measurement

Data retention is referred to the ability of the memory cell to retain its state over a long period regardless of whether the power is on or off. It is an important specification of nonvolatile memory. In general, a minimum of 10-year data retention time is required for a commercial memory chip. As it is impossible to measure retention over such a long time, it is more practically to estimate or project retention based on accelerated stressing data and Arrhenius plot. Retention measurement in this work is mostly done with a constant voltage stress as shown in Figure 3.14 (a). It is also possible to measure data

retention by applying bias only at the time point when reading resistance as in Figure 3.14 (b) leaving the device unstressed for the rest of the time. Temperature accelerated retention measurement is also used, which is to be discussed in a later chapter.

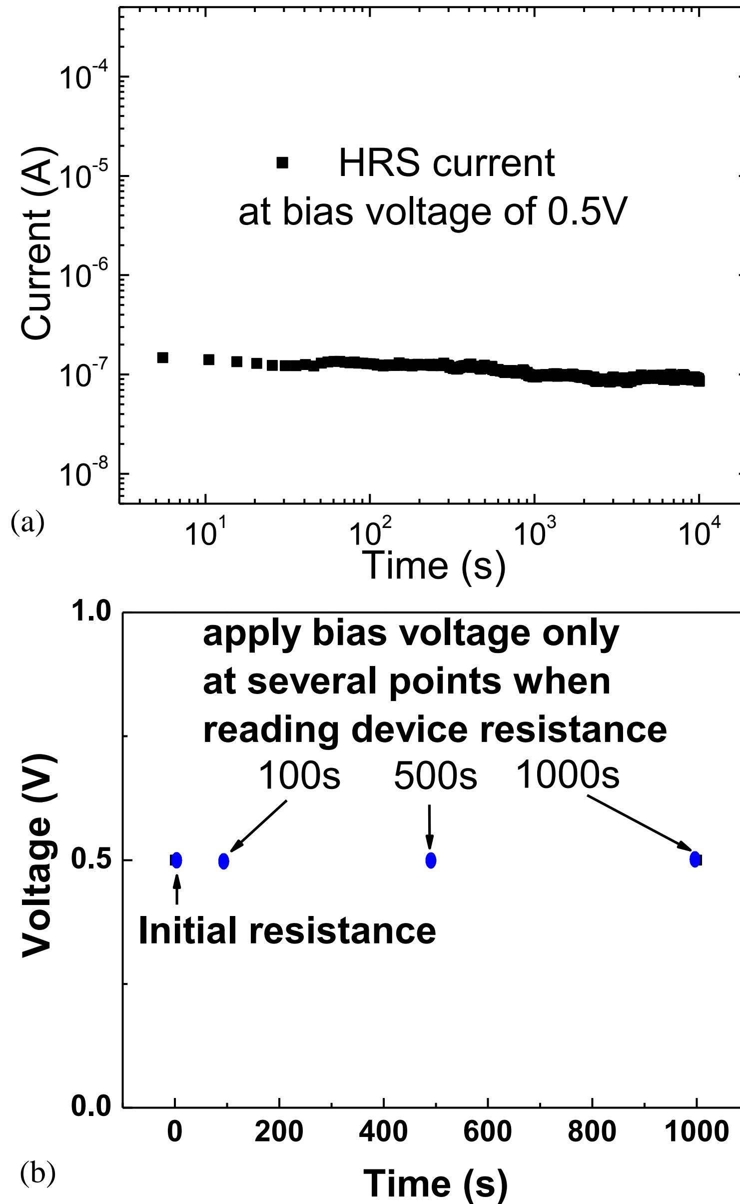


Figure 3.14 Data retention measurement (a) constant voltage stress measurement (b) retention measurement with short period bias applied only at certain recording time points

3.5.4 AC switching measurement

Oxide-based RRAM is developed for next generation nonvolatile memory applications. Programming / erasing speed is also one of the important specifications. Compared to Flash memory with programming speed in the milliseconds range, RRAM operates at a much faster speed down to nanoseconds. To test switching speed of the fabricated cells, AC resistive switching (pulse measurement) is implemented with an Agilent pulse generator. Figure 3.15 shows the waveforms of two pulses of widths 50ns and 20ns respectively measured at mid-height with rising and fall time of 10ns. Similar to DC switching, an electrical pulse is applied to the top electrode of the device with the bottom electrode grounded.

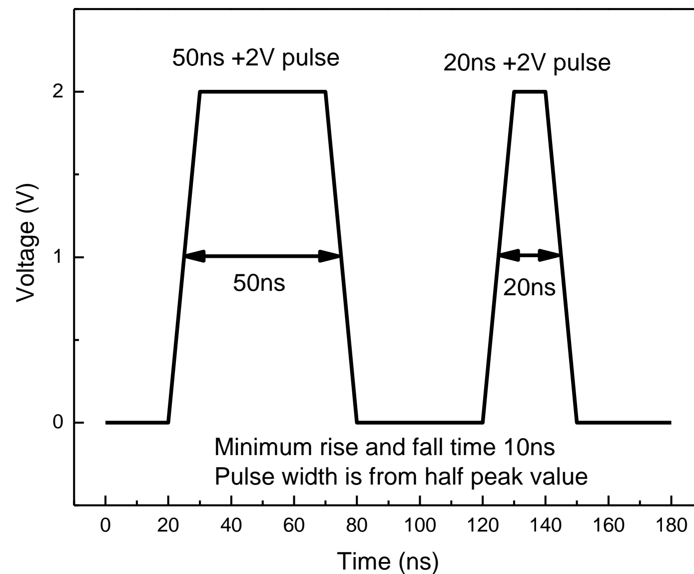
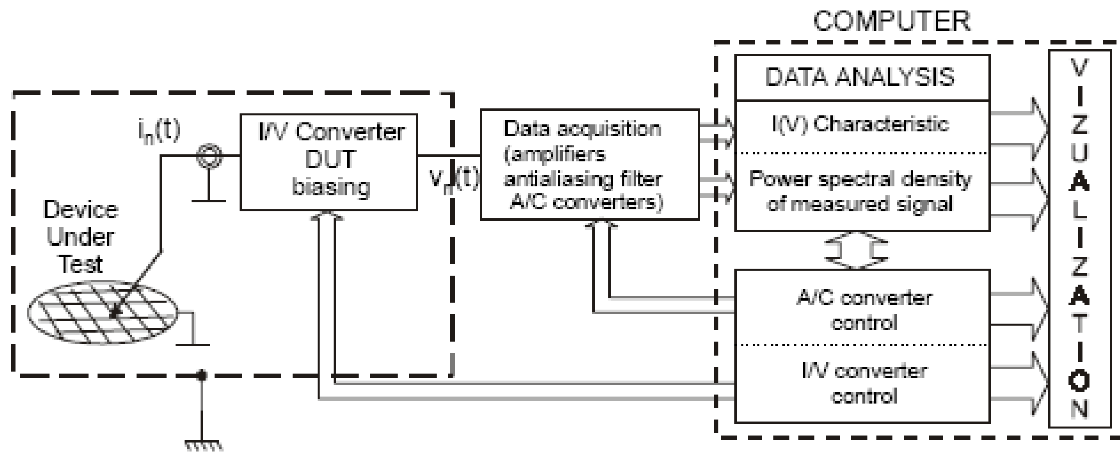


Figure 3.15 Schematic waveforms of two pulses of widths 50ns and 20ns measured at half peak voltage point with rising and falling time of 10ns.

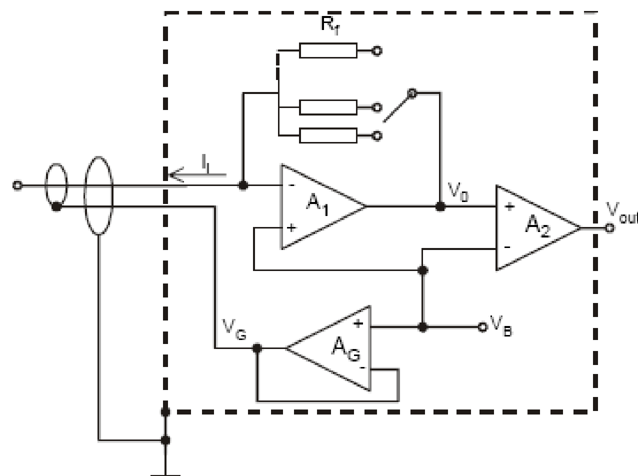
3.5.5 Low frequency noise measurement

The low frequency noise (LFN) has been the research topic for the MOSFET device since the past. As the LFN signal increases with respect to the reciprocal of the device area [107], it is drawing more attention as continuous scaling down of the critical dimensions. It has been recognized as a capable tool to characterize the current conduction mechanism and fluctuation sources in any electronic devices. As the RRAM device is to be used in ultra-high density nonvolatile memory, it is expected that LFN analysis can provide useful information about the conduction mechanism as well as defect characteristics.

With that in mind, LFN measurement is carried out on the memory devices fabricated. A wafer-level, computer-assisted system, programmable point probe noise measuring system (3PMNS) is used for LFN analysis [108]. Figure 3.16 (a) shows the schematic of the 3PMNS noise measurement setup. The computer-controlled current / voltage converter (I/V converter) whose input can be remotely biased is referred as a programmable biasing amplifier (PBA). A simplified version of PBA is shown in Figure 3.16 (b). PBA features computer-controlled gain and input bias, which allows developing program for automatic or keyboard-controlled LFN measurement on various electronic devices. The simplicity of the novel instrument makes the data collection not only easier and faster but also extremely flexible.



(a)



(b)

Figure 3.16 (a) Schematic of 3PMNS low frequency noise measurement setup (b) Simplified schematic of the programmable biasing amplifier [109].

3.6 Summary

Fabrication process flow of oxide-based RRAM devices has been presented in this chapter. Various physical characterization tools used during and after fabrication have also been introduced. Electrical measurement methodologies including resistive switching, data retention and low frequency noise analysis are discussed. Equipment or system setup for each electrical characterization test has also been described.

Chapter 4 Resistive Switching Mechanism Investigation and Temperature Instability Study in Oxide-based RRAM

4.1 Introduction

Since late 1990s, RRAM has been actively researched both in industry and academia as one of the most promising candidates for next generation nonvolatile memory or universal memory [9, 15]. Resistive switching behavior of various transition metal oxides (TMO) and complex oxides, including NiO_x, TiO_x, WO_x, ZnO_x, CuO_x, SrTiO, LaCaMnO, etc. have been reported [9, 12-14, 30, 62, 86, 89, 92, 110-112]. Due to simple composition, TMO has attracted greater attention as RRAM materials.

In recent years, many ideal characteristics including high programming speed (down to nanoseconds), long data retention period of more than 10 years, low power consumption, high integration density and continued scalability have been demonstrated in numerous RRAM devices. And among them, HfO_x based RRAM device has displayed outstanding performance as presented in IEDM 2008 [8]. However, precise predictions of device performance are still not possible, as many details of the switching mechanism behind the reported phenomena are still unknown [30], which is a key challenge of this technology.

To better understand the underlying physics, resistive switching behavior of HfO_x based RRAM device is being thoroughly investigated in this chapter. Stable bipolar switching has been observed in the fabricated cells with good endurance and retention. Bias temperature instability testing is being implemented to study the voltage and temperature effects on both (a) the switching and retention [50, 113-114], and (b) multilevel switching phenomena.

4.2 Physical Analysis

The device under test uses a thermal oxidized HfO_x as the resistive switching layer, TiN and Pt as the top and bottom electrode, respectively. Device fabrication process is described in Chapter 3.

4.2.1 XPS Results of the Oxidized Film

The chemical composition of the prepared resistive switching layer after oxidation is analyzed by XPS. Thin Hf film of ~8nm being deposited by DC sputtering is oxidized in furnace at 450°C for different periods of 5 to 20 minutes. Two samples with 5 min and 20 min oxidation time are sent for XPS measurement. Hf 4*f* scan shows two peaks at binding energies of 17.1eV and 18.6eV indicating that both films have been fully oxidized even within short oxidation time. The composition analysis from XPS also shows a hafnium to oxygen ratio of 1:2. This confirms the as prepared Hf film to be fully oxidized prior to TiN top electrode deposition.

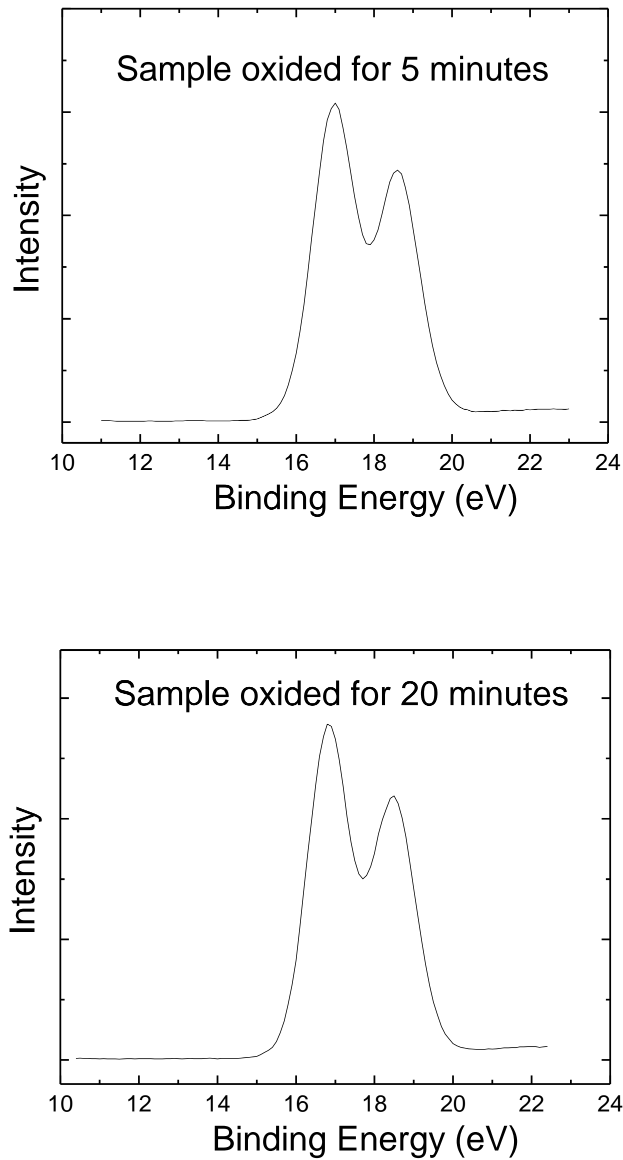


Figure 4.1 XPS Hf 4*f* scan of HfO_x as-deposited film with oxidation time of 5 and 20 minutes respectively, binding energy (BE) peaks at 17.1eV and 18.6 eV show the as prepared Hf thin film has been fully oxidized. (Calibrated with C 1*s*)

4.2.2 Cross-Section TEM and EDX analysis

High resolution transmission electron microscope (HRTEM) is used to check the morphology of the prepared samples. Figure 4.2 below shows the cross-sectional image of the TiN/HfO_x/Pt memory cell. The thickness of HfO_x is approximately 8nm, and an interfacial layer (IL) of TiO_xN_y (~ 1 to 2nm) is identified between the HfO_x and top electrode (TiN), which may be due to the strong attraction of oxygen ions towards Ti [115].

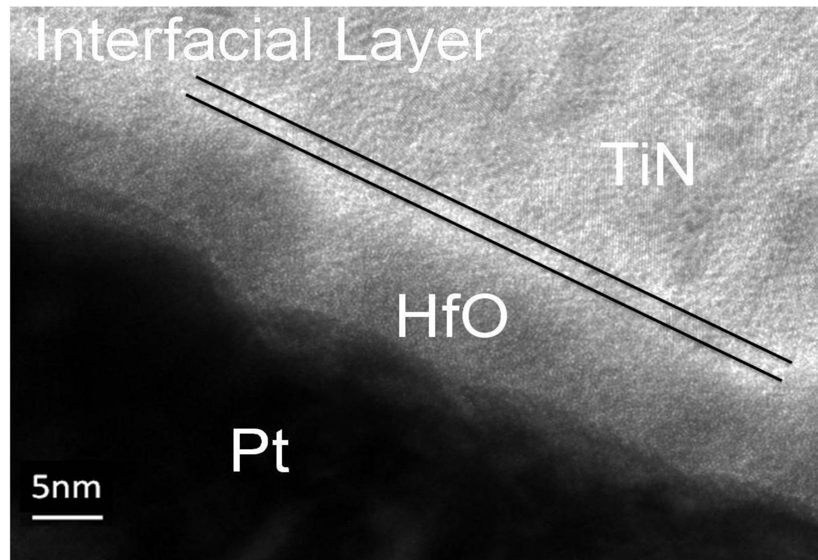


Figure 4.2 HRTEM image of the TiN/HfO_x/Pt memory cell, an interfacial layer of TiO_xN_y is identified

This interfacial layer formation is further confirmed with EDX spectrum profile as shown in Figure 4.3. The oxygen profile trends towards the TiN side, indicating that the HfO_x layer in the device region possibly becomes oxygen deficient due to the formation of

TiO_xN_y. It is believed that this IL layer may serve as an oxygen reservoir for resistive switching.

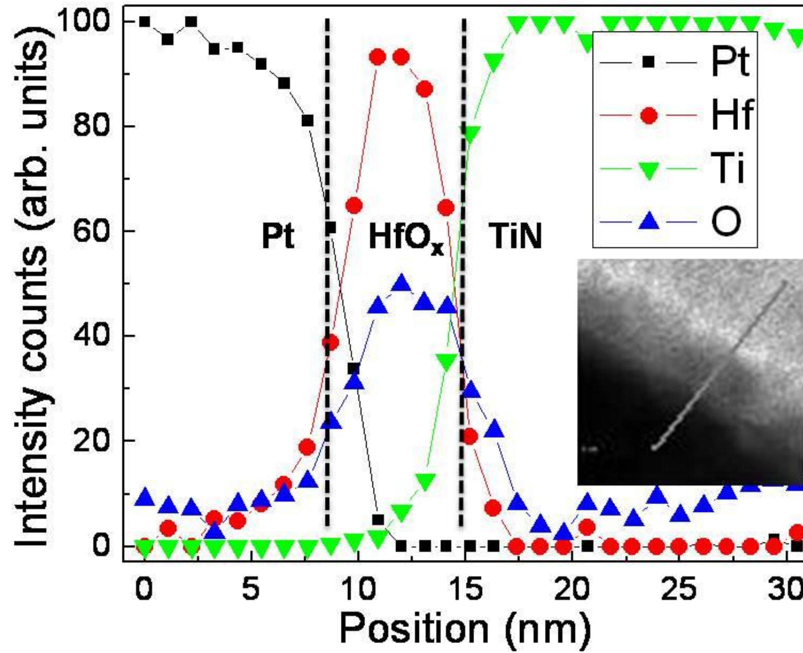


Figure 4.3 EDX spectrum of elemental spatial profile showing oxygen tends to be attracted by TiN. Inset indicates the direction of profile.

4.3 Resistive Switching in HfO_x-Based RRAM Cell

Polarity dependent bipolar resistive switching phenomenon is observed in the fabricated RRAM cells. Figure 4.4 shows the current-voltage (I-V) characteristics of 100 repetitive DC sweeps after forming at room temperature. Sweeping directions have been marked in the figure.

1. 0V→3V: With an increasing positive voltage bias, the current suddenly increases at a set voltage (~1.4V), indicating a transition from high resistance state (HRS) to low resistance state (LRS).
2. 3V→0V: With a voltage dropped from 3V to 0V. The resistance state remains unchanged, indicating that the resistance state can be maintained.
3. 0V→-4V: A reverse voltage bias is applied and resistance of the cell is reset back to HRS.
4. -4V→0V: When the voltage bias is reduced to 0V, no change of resistance state is being observed.

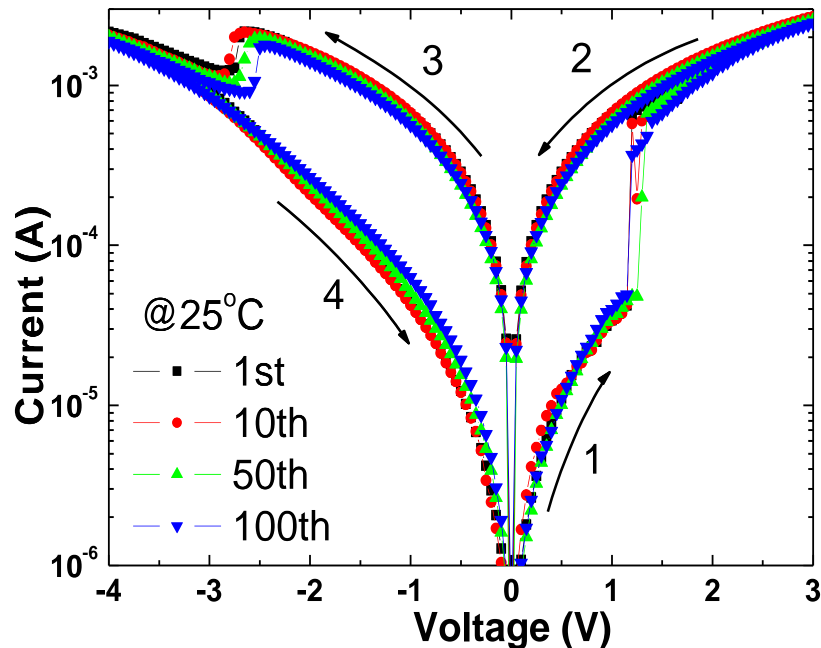


Figure 4.4 The switching characteristics of 100 repetitive DC sweeping current-voltage of the HfO_x based ReRAM after a forming process at room temperature.

For the fabricated RRAM devices, a good endurance has been demonstrated, an on / off ratio of more than ten times is maintained after 500 DC cycles as shown in Figure 4.5.

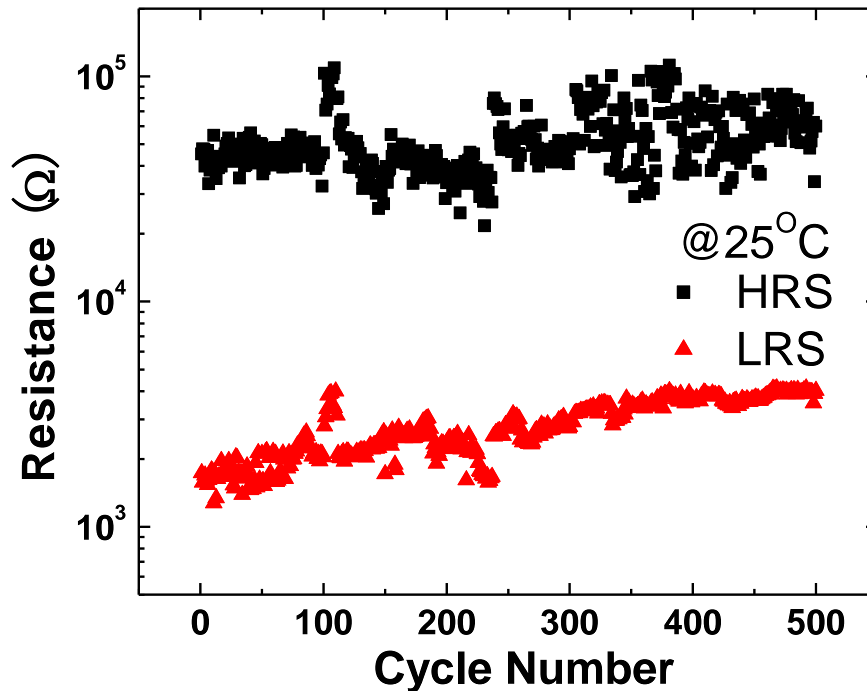


Figure 4.5 Switching endurance of 500 cycles in DC sweeping mode at room temperature. Resistance values are taken at 0.5V for both HRS and LRS

The resistive switching phenomenon can be explained by the formation and rupture of oxygen vacancies related conduction filaments [16]. In detail, the set process can be liken to a percolation effect which forces oxygen ions to be depleted from the oxide, thus forming a conduction path with oxygen vacancies (V_o). This process is similar to dielectric soft breakdown. Correspondingly, the reset process depletes electrons from the vacancies and recovers them with oxygen ions from TiO_xN_y interfacial layer or interstitials. The schematic set/reset process is shown in the figure below.

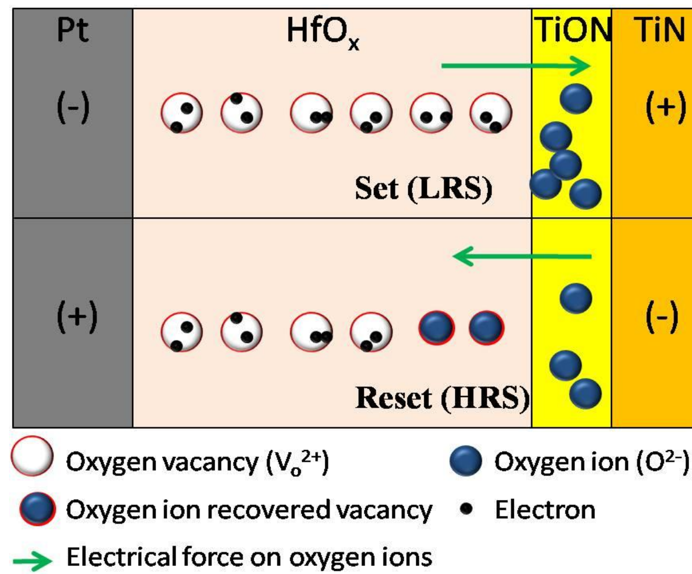


Figure 4.6 The schematics of set and reset processes. During set, oxygen ions move away from its lattice by applied electric field and form the conduction path with oxygen vacancies. During reset, oxygen ions move back to recombine with the vacancies and then conduction path disappears.

4.4 Temperature Effect on Resistive Switching

To better understand the resistive switching behavior in TiN/HfO_x/Pt device, resistive switching at both room temperature and high temperature (100°C) are being compared in Figure 4.7. It is clearly observed that HRS current increases under both polarities with temperature, which can be explained by the schematics as inset of this figure.

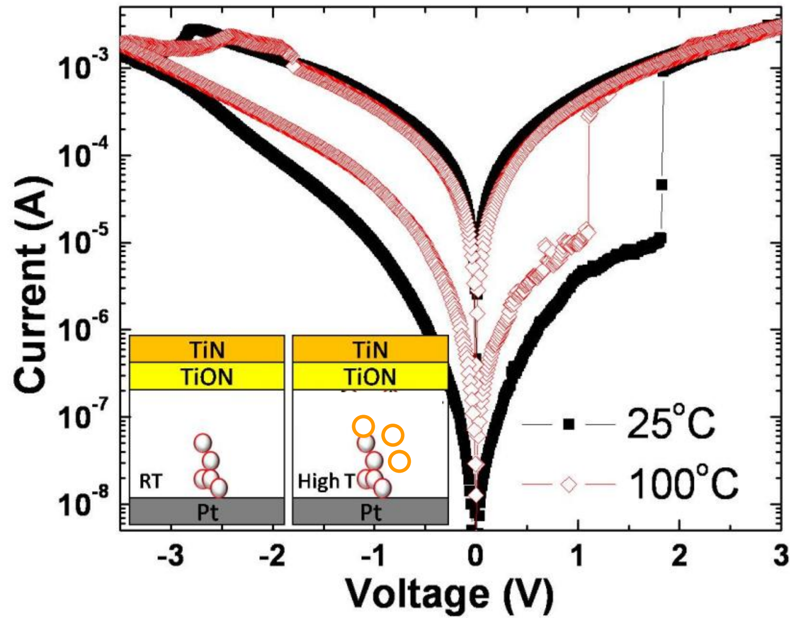


Figure 4.7 Comparison of resistive switching at both 25°C and 100°C. (inset shows schematic high temperature HRS leakage current (TAT) increases). At high temperature, trap concentration inside dielectric increases, which gives rise to TAT current. Therefore, the On/Off ratio decreases at high temperature.

When device is reset to HRS, the conduction filament is believed to be broken near the metal dielectric interface at the top electrode, cutting off the current. According to crystal defect theory [116], the probability (p) of oxygen ions to overcome the potential barrier and create vacancies can be expressed as

$$p \approx \nu \exp(-E / k_B T) \tag{4.1}$$

where E is potential barrier height, T is temperature. Thus, with the increase of temperature, the probability of defect formation increases. It could also be described as follows: with increasing temperature, thermal vibration of oxygen ions becomes stronger,

which means the base energy is higher, thus the potential barrier is equivalently lowered. As a result, more oxygen vacancies are being generated. The increased V_o–related traps inside the dielectrics would therefore increase the trap-assisted tunneling (TAT) leakage [115, 117]. Consequently, a smaller on/off ratio would also be observed, as illustrated in Figure 4.8. For both room and high temperature, retention are stable during the 1000s measurement.

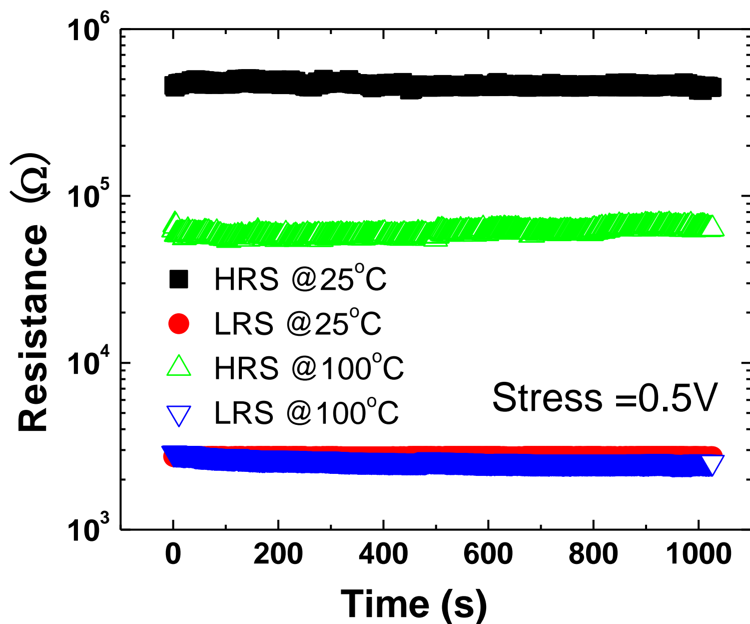


Figure 4.8 Retention behavior at both room and high temperature at the voltage of 0.5V. It shows a clear current level different between room temperature and high temperature, while for both cases, retention is stable over the 1000s period.

Furthermore, as temperature increases, the probability of oxygen vacancies generation increases based on crystal defect theory, which is equivalent to the oxygen vacancy formation energy barrier lowering in both within the oxide (for set process) and

interfacial layer (for reset process). In addition, oxygen ion mobility will increase with higher temperature [63]. Thus it is believed that owing to these two factors, a reduced electrical field is required to create/rupture the filament for set/reset process [118]. Hence the set and reset voltages are expected to decrease with increasing temperature, which can be confirmed in Figure 4.9. Note that during the measurement, 10 cycles of DC sweep are applied at each temperature point.

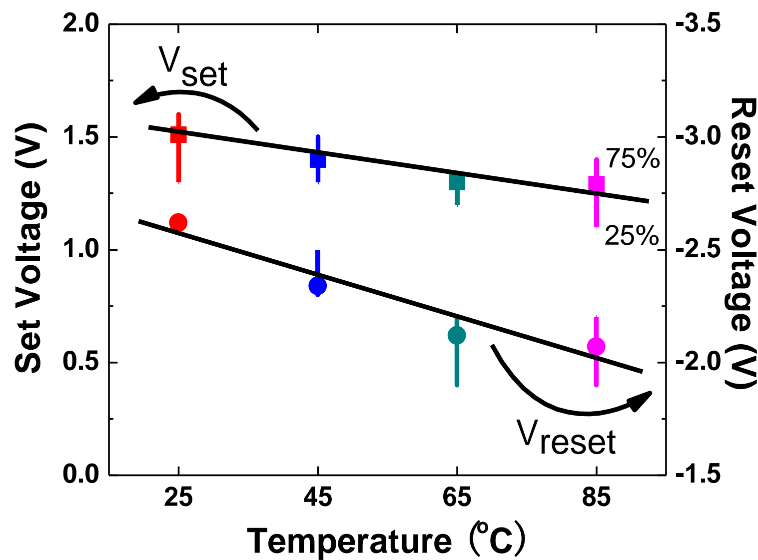


Figure 4.9 Set (V_{set}) and reset (V_{reset}) voltages decrease with increasing temperature. Data points show the average values of 10 set/reset voltages of DC sweeps at each temperature.

4.5 Retention Characteristic of Fabricated Cells

Data retention is an important parameter of NVM, where temperature usually plays an important role. Hence, bias temperature instability of prepared memory cells is being investigated. Electrical stress of 0.1V to 0.8V at both room temperature and high

temperature on the reliability of RRAM devices is studied in Figure 4.10. The HRS resistance variation after different periods of stress ($|\Delta R/R_{t=0}|$, where $R_{t=0}$ stands for the resistance prior to stressing) is used to evaluate the degradation of ReRAM. It can be observed that the variation at room temperature is much smaller as compared to high temperature case for all stressing conditions. The resistance variation at high temperature is less than 60% and is almost independent of stressing condition. This variation will not degrade the reliability (retention) of ReRAM, as shown in Figure 4.10. Possible reasons may be due to small stressing voltage (smaller than V_{set}) and short stressing time.

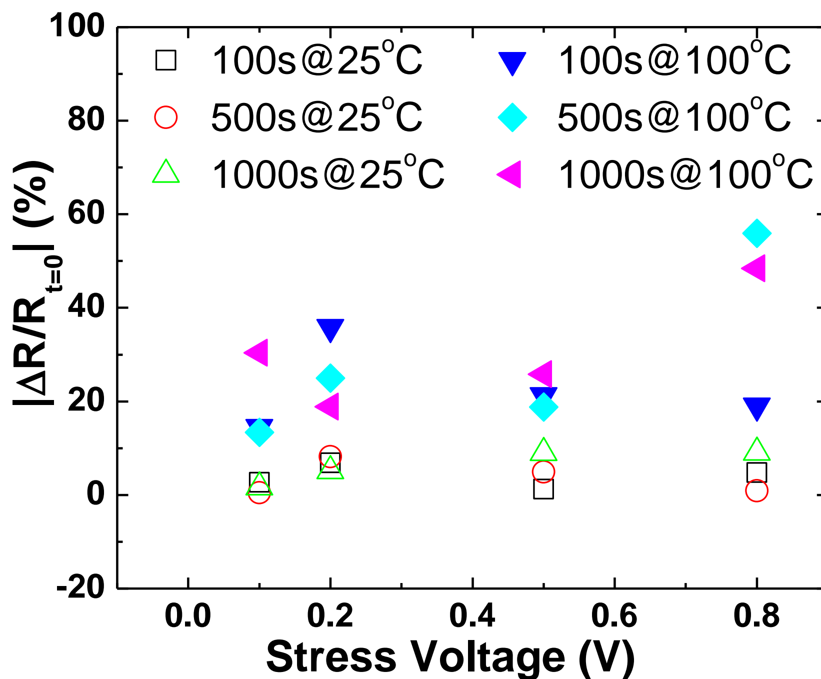


Figure 4.10 Resistance variation ($|\Delta R/R_{t=0}|$) of HRS at different stress conditions and temperatures. It shows $|\Delta R/R_{t=0}|$ (original resistance is defined as the resistance prior to stressing) does not vary much, which is negligible as compared with memory window of ~100 times.

It has been widely accepted that the formation and rupture of conductive filaments (CF) consisting of oxygen vacancies (V_o) are responsible for the switching between HRS and LRS. The generation and diffusion of a new V_o will cause the significant reduction of HRS resistance, inducing a sharp current increase and lead to HRS retention failure [119-120]. Based on the crystal defect theory and probability theory, the expected HRS retention time can be expressed as following:

$$F(t) = 1 - (1-p)^{\frac{nt}{t_0}} \tag{4.2}$$

$$p = \exp\left(-E_a/k_B T\right) \tag{4.3}$$

$$t_E = \frac{t_0}{n|\ln(1-p)|} \approx \frac{t_0}{np} \tag{4.4}$$

$$\therefore \ln t_E \propto \frac{1}{T} \tag{4.5}$$

where $F(t)$ is failure probability, p is V_o generation probability, E_a is activation energy related to the formation of V_o, t_E is expected time of HRS retention, n is number of possible places for V_o generation and t_0 is vibration period for lattice oxygen atom.

From this model, the natural logarithm of expected HRS retention time is inversely proportional to temperature, which is consistent with reported literatures [119, 121-123]. It is verified with measurement results as shown in Figure 4.11. In this figure, each data point is a logarithm average value of ten measurement results, where observed exponential dependence of HRS retention time on temperature is consistent with the previous formula derivation. Other than that, the slope is found to be 2580.22, and the

activation energy extracted is 0.22eV which is related to the formation energy of V_o generation.

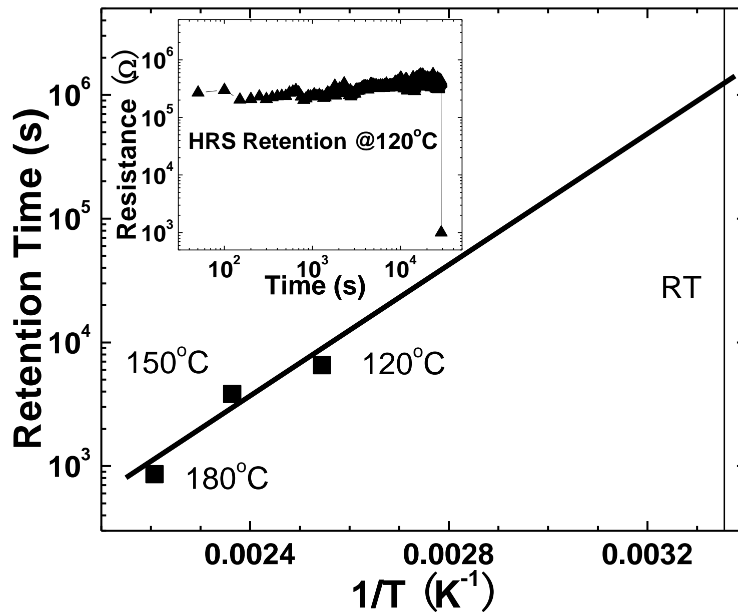


Figure 4.11 Measured HRS retention times as a function of temperature. The exponential dependence of the retention time with temperature is observed, which is consistent with formula derivation.

For RRAM devices fabricated in this study, LRS retention is considered consistently stable, hence only HRS retention is being investigated, and moreover, retention failure occurs in HRS. However, for real device development, both HRS and LRS should be studied in detail and also the intermediate states for multilevel storage. Such research effort can be found in the literatures [113, 119-120].

4.6 Multi-level switching

By a proper control of the measurement conditions, HfO_x based RRAM devices exhibit multi-level operating potential, which can further increase the memory capacity. This feature makes RRAM better candidate for the next generation nonvolatile memory. There are two possible ways to enable multi-level switching as shown in Figure 4.12 and Figure 4.13 by either using different reset stop voltage or different compliance level as reported in the literatures [8, 124-125].

In Figure 4.12, the reset voltage sweep stops at different value of -2V, -2.5V, -3V and -3.5V, which results in different HRS values. This may be due to the incomplete recovery of oxygen ions with vacancies, and it reveals that some of the oxygen ions may need higher voltage to enable the recovery process with vacancies.

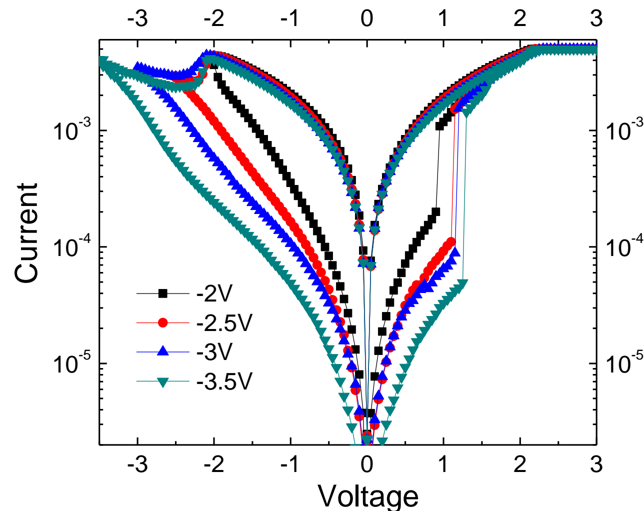


Figure 4.12 Multi-level switching with different reset stop voltages from -2V to -3.5V. Besides LRS, four levels of resistance can be achieved by proper control of voltage.

Another method is by setting different compliance current as shown in Figure 4.13. The compliance level limits the degree of breakdown during set process, hence giving different LRS resistance values, which indicates that the compliance current may affect the number or size of the conduction paths [126].

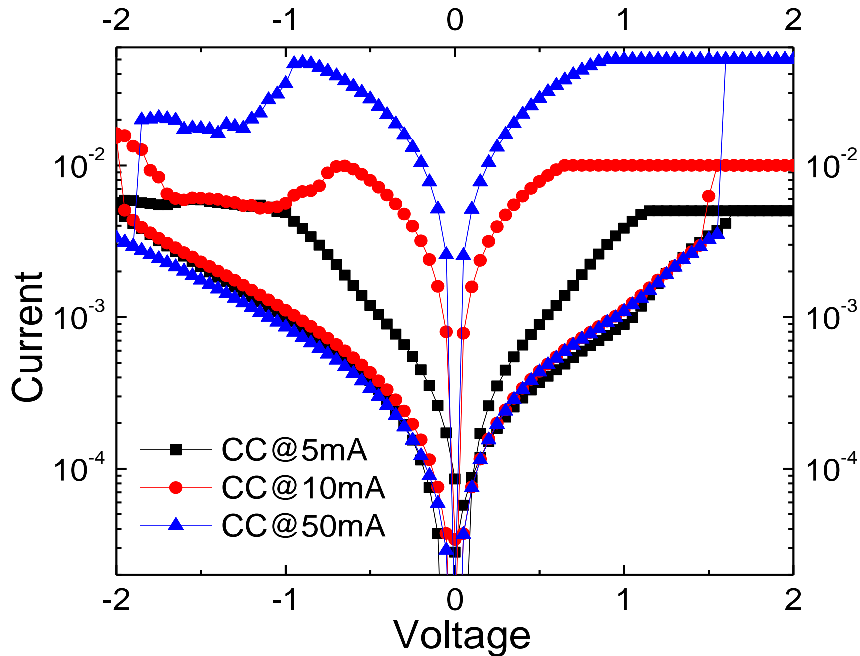


Figure 4.13 Multi-level switching under different compliance currents from 5mA to 50mA. Besides HRS, three levels of resistance can be achieved by proper control of compliance current.

However, at high temperature, due to the higher leakage at HRS as mentioned previously, the multi-level switching might not be retained as shown in Figure 4.14. These temperature dependent switching properties might pose a challenge to the commercialization of binary oxide based RRAM devices. Material-oriented solutions

should be applied to improve the conditions by controlling the formation / rupture of conduction filaments as well as thermal stability of switching layer.

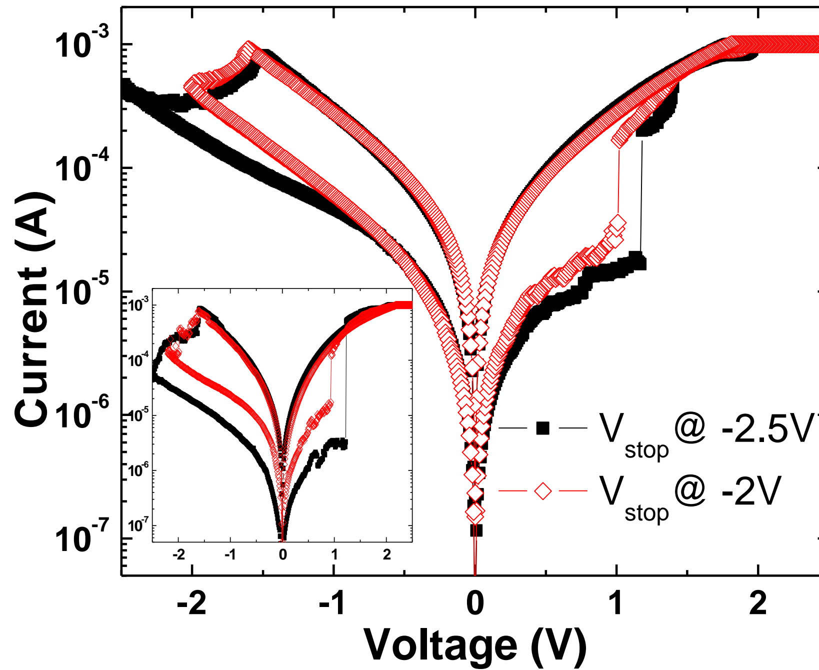


Figure 4.14 Multi-level switching disappears at high temperature (60°C). This may be due to higher leakage current at high temperature, which is equivalent to a lowered HRS resistance. Inset shows the multi-level switching at room temperature.

In Figure 4.12 and Figure 4.14, it is observed that the transition between LRS and HRS (reset process) is much broader when compared to its opposite (set process) [114], which is more abrupt. The V_o related conduction filament is used to explain the resistive switching mechanism of HfO_x-based RRAM. For set process, it is believed that electric field can cause the oxygen ions to be removed from its original lattice point, which would further lead to immediate V_o related filament formation at once without involving the

oxygen ion diffusion. Thus we observe the abrupt leakage jump from HRS to LRS. While for reset process, it involves the diffusion process of oxygen ion from interfacial layer or interstitial site to its desired position. Due to the diffusion process of oxygen ions, it might not be possible to recombine all the V_o in one time. Thus, the transition from LRS to HRS could be broader.

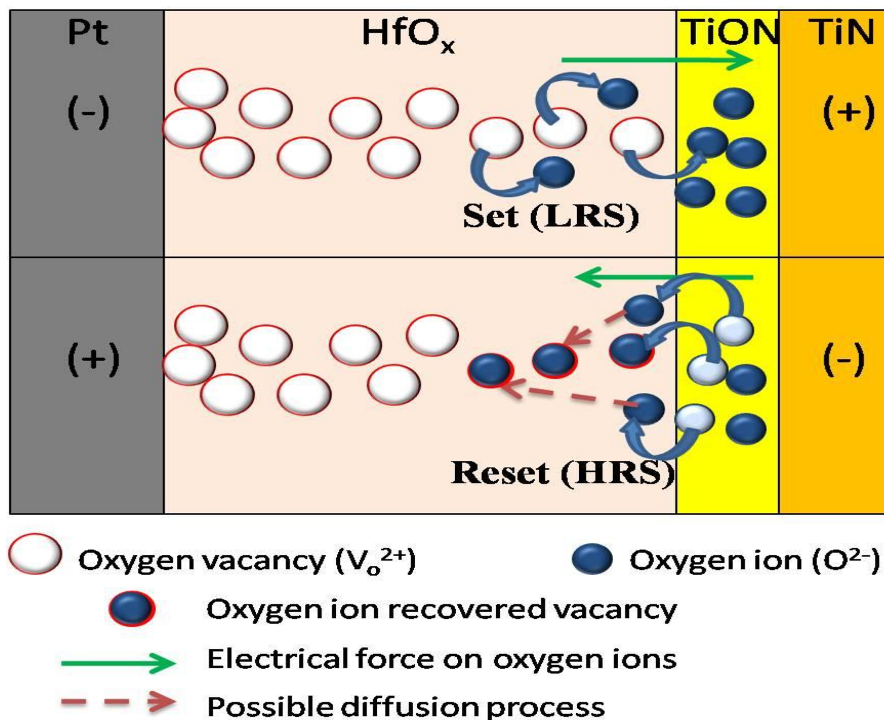


Figure 4.15 Schematic set / reset transition indicating diffusion in reset process

4.7 Summary

The resistive switching behavior and thermal instability in HfO_x-based RRAM cell is being studied in this chapter. Important findings are summarized as following:

- Bipolar resistive switching phenomenon with good endurance is observed in the fabricated RRAM cells. This can be explained by formation and rupture of oxygen vacancies related conduction filament.
- At high temperature, the probability of oxygen vacancy formation increases, giving rise to the trap-assist tunneling leakage, hence memory window decreases with increasing temperature.
- Temperature effect plays a more important role on HRS resistance degradation as compared to electrical bias. HRS resistance failure can be related to oxygen vacancy generation, hence the expected retention time at room temperature can be extrapolated from Arrhenius plot.
- Multi-level switching is observed in the fabricated cells with different reset stop voltage or different compliance current. However, multilevel switching might not be retainable at high temperature.

Chapter 5 Current Conduction Mechanism Investigation in Oxide-Based RRAM

5.1 Introduction

Transition metal oxide materials have been extensively studied in the recent years for future generation nonvolatile memory application owing to its promising performance and CMOS compatibility [8-9]. Switching mechanism in this type of Resistive Random Access Memory devices is proposed to be related to local oxygen vacancy filament formation and rupture by redox reaction [16, 48], which has been discussed in detail in the previous chapter. However, the current conduction mechanisms in different resistance states are still under debate despite its importance to understand the RRAM switching properties and power consumption [127].

The low frequency noise (LFN) measurement is a powerful tool to characterize the current conduction mechanism and fluctuation sources in any electronic devices [107]. Since the LFN increases reciprocally with device area, it has received wide attention especially in aggressively scaled devices [107, 128]. For RRAM devices, LFN characteristics are expected to provide useful information about conduction and fluctuation mechanisms as well as defect characteristics [129-132]. In this chapter, current conduction mechanism is investigated with DC and LFN analysis on HfO_x based RRAM devices of various dimensions.

5.2 Device under test

HfO_x-based RRAM devices used for this study are fabricated using the standard CMOS platform technology on 8 inch Si wafers. A 20 nm thick Ti layer and a 50 nm thick Pt layers are deposited by E-beam evaporation as the adhesion layer and the bottom electrode, respectively. Then 10 nm HfO_x and 50 nm TiN layers are deposited by reactive sputtering with proper annealing conditions as the switching layer and top electrode respectively. Devices are then patterned with traditional lithography and dry etched into square shapes with dimensions from 10×10 μm^2 to 100×100 μm^2. Post metal dielectric is used to cover the wafer preventing devices from further possible damages after fabrication.

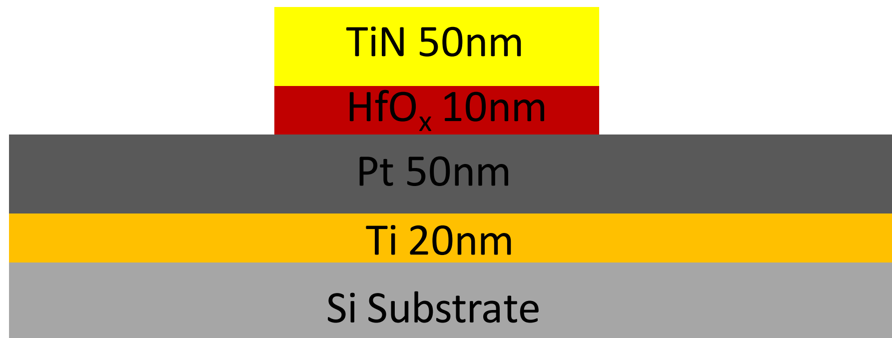


Figure 5.1 Schematic of the memory cell (DUT) used in current conduction mechanism investigation via both DC and LFN analysis. TiN and Pt are used as top and bottom electrode respectively and 10nm of HfO_x is used as resistive switching layer.

In this part of the work, a group of measurements are taken on four types of square devices with dimensions of 10um, 20um, 50um and 100um (for clarity, denoted as L10, L20, L50 and L100 respectively). To avoid one device representing the measurement

results, which might be non-typical, for each area, at least 3 devices are used, and for each device, three states of fresh, HRS and LRS are measured with five different biases.

5.3 DC current conduction mechanism investigation

Devices used for conduction study exhibit polarity dependent bipolar resistive switching behavior and a typical transition curve is show below:

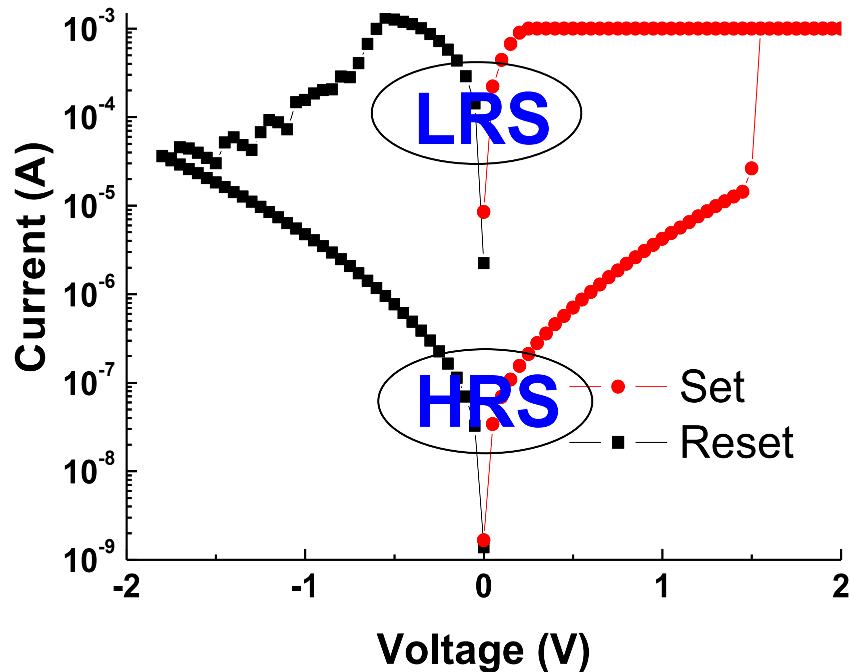


Figure 5.2 Typical bipolar resistive switching curve for HfO_x RRAM device used for current conduction investigation

To analyze the current conduction mechanism in different states, the respective I-V curve is plotted with logarithmic axes in Figure 5.3. From I-V fitting with a slope of 1 in the

upper part of this figure, it indicates the ohmic / metallic conduction nature of LRS. However, for HRS, slope equals to one at very small bias and around two at higher voltage. It exhibits non-ohmic behavior with non-linear I-V slope, which may be due to electron hopping conduction.

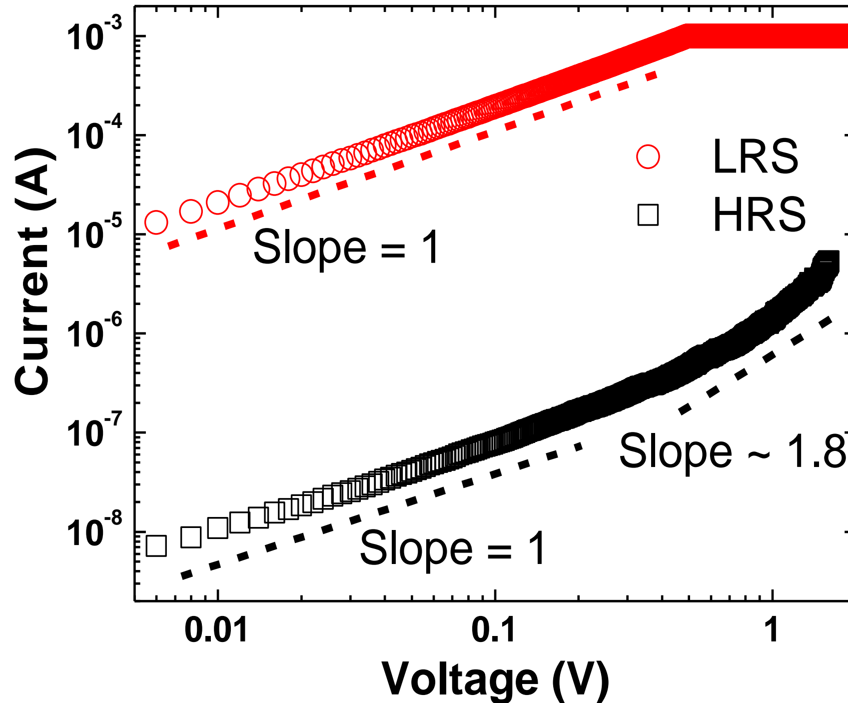


Figure 5.3 Logarithmic plot of I-V curve for current conduction model fitting of HRS and LRS. Slope of one is observed for the entire LRS and small voltage bias of HRS, slope is close to 2 for HRS at large bias.

To get further information, LRS and HRS resistances are measured at various temperatures as shown in Figure 5.4. This measurement confirms the ohmic / metallic conduction nature of LRS with temperature independency. While for HRS, a thermal

activation energy of around 40 meV in the high temperature resistance measurement confirms electron hopping conduction [133]. As a result, the on current of LRS should be independent of device area, while on the contrary the off leakage current of HRS and fresh state should be scalable with device area as reported in the literature [8, 134]. It should be noted here that this resistance change with temperature is not to be confused with Figure 4.8 in Chapter 4. Resistance values here are measured at different temperatures without switching each time, that means, RRAM cell is reset to HRS and then measure resistance for a few times at different temperatures. However, in Figure 4.8, RRAM device is switched at each temperature and then resistance is measured. That is to say the resistance change here is due to semiconductor like conduction, while in Figure 4.8, it is due to the change of switching kinetics. Of course, there is some impact of conduction related resistance decrease in Figure 4.8, but this portion is much less than the resistance change due to switching kinetics if we compare the amplitude of change in resistance levels of these two figures.

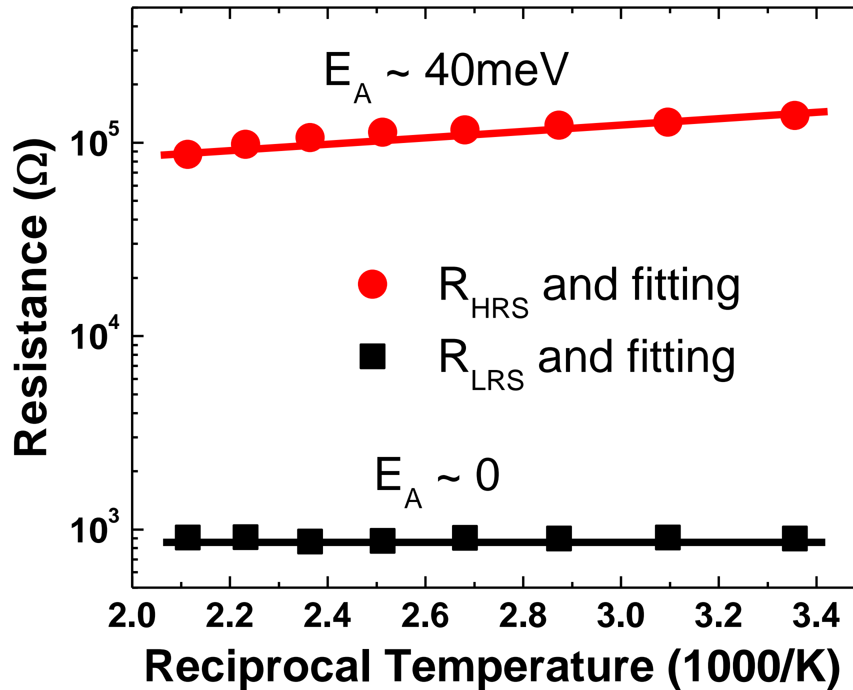


Figure 5.4 Temperature dependent resistance plot with activation energy fitting.

To compare DC current levels in devices with different areas, small bias voltage sweep is applied in the fresh state, HRS and LRS. A voltage below transition threshold is used to avoid resistive switching during measurement. Figure 5.5 shows I-V curve for the fresh state of 4 devices with different areas. All these curves are non-linear (not shown in linear scale here), which indicates kind of hopping or thermally activated current transport with dependence on the area. It is the oxide leakage current since no stress has been applied yet.

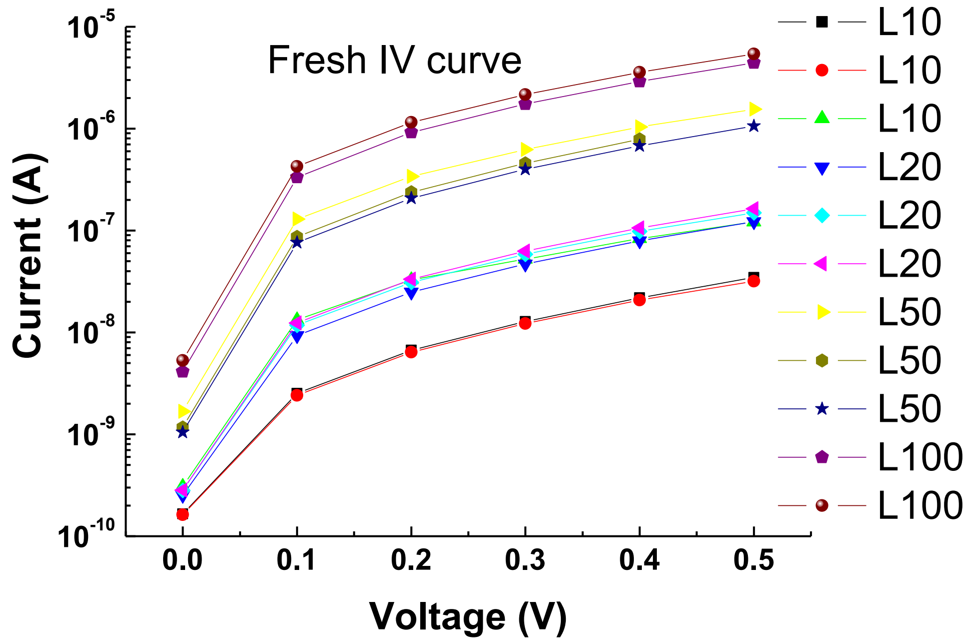


Figure 5.5 Current voltage curves for the fresh state of devices with different areas. It clearly shows four current levels in accordance with device areas.

The HRS I-V curves are presented in Figure 5.6. Figure 5.6 (a) is the I-V curve for all devices. It is similar to those of the fresh state, i.e. area dependent and not linear. The amplitude is also similar; it indicates roughly complete recovery of the conduction filament after reset process. After normalization with area, all curves overlaps with each other. This indicates that the HRS current is more or less uniformly distributed over the whole device area.

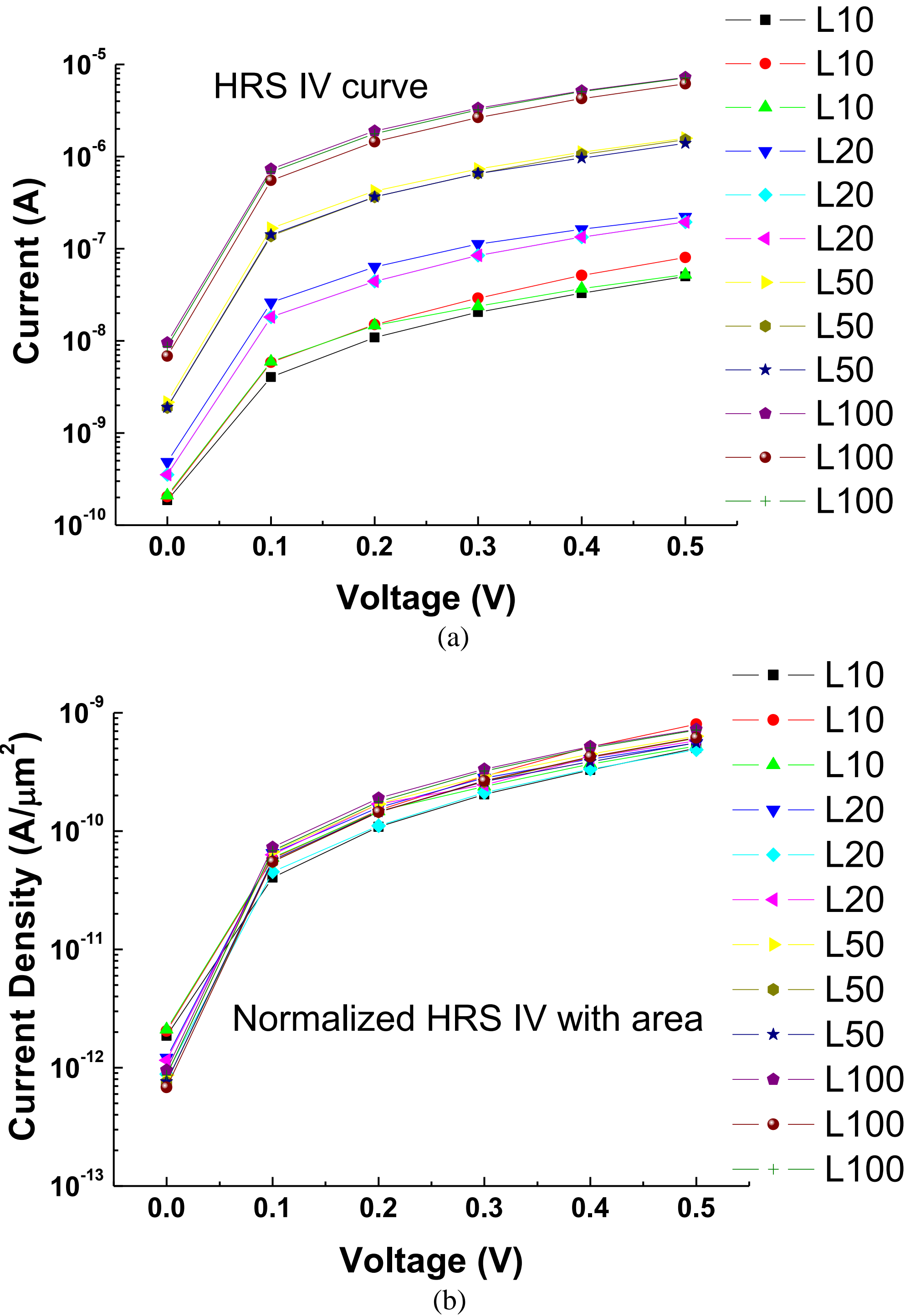


Figure 5.6 (a) Current voltage curves of HRS states for different areas. It shows clearly four current levels in accordance with device areas. (b) Normalized current density with device areas indicating area scaling property of HRS current.

The LRS I-V characteristics are shown in Figure 5.7. Without any normalization, all curves are at similar level, the current level is related to the compliance setting, which limits the degree of conduction to some extent. It means the current in LRS does not depend on the area of device, which is consistent with filament conduction. Moreover, all currents show a linear dependence on the bias voltage (not shown in linear-axis plot here), which is the ohmic conduction behavior.

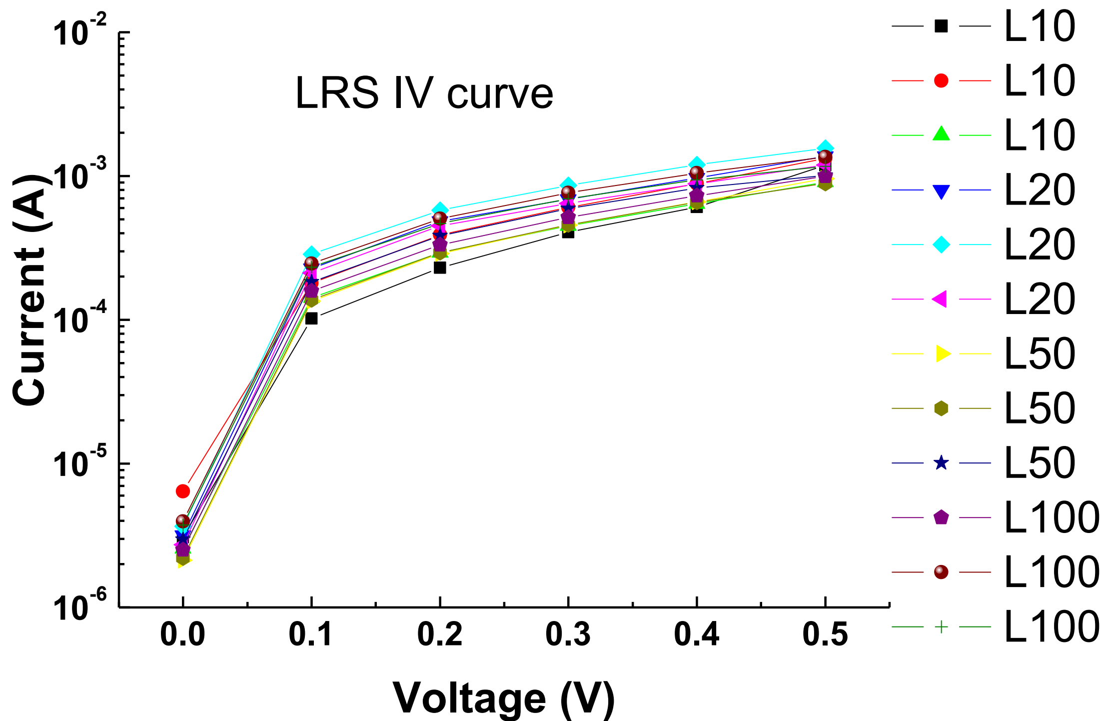


Figure 5.7 Current voltage curves of LRS states for different areas showing no area dependence and a linear relationship on the biasing voltage.

To get a clearer picture of the resistance levels at different states with device area scaling, Figure 5.8 is plotted. It shows that the resistance scales linearly with device area in fresh

and HRS states with log-log axis, while the resistance keeps nearly constant at all device area points in LRS, similar to those reported in the literatures [8, 134].

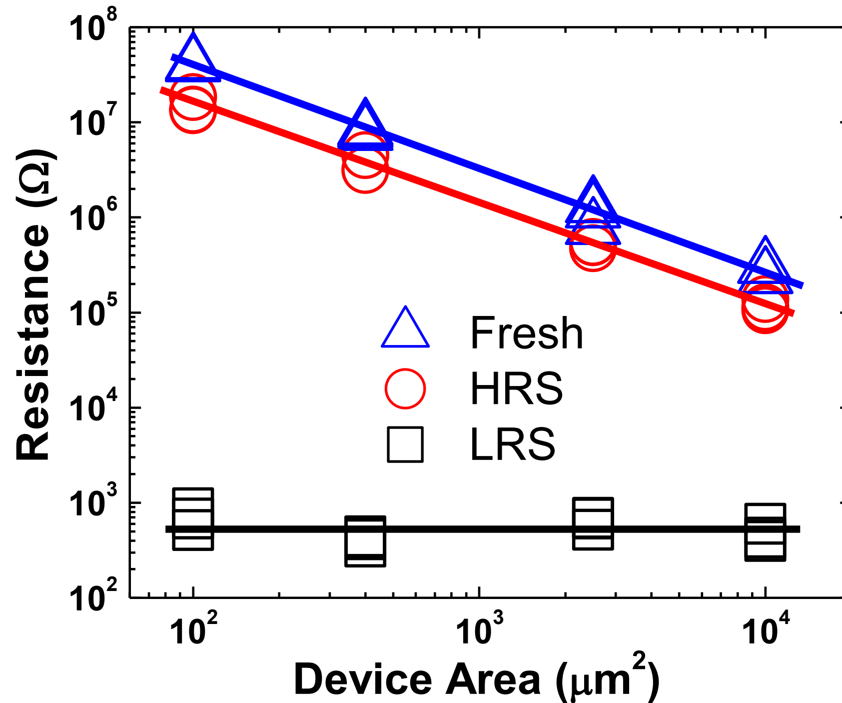


Figure 5.8 Resistance versus device area plot for fresh, HRS and LRS. For both fresh and HRS state, resistance shows a reciprocal scaling effect with respect of device areas; while for LRS, there is no dependence on device areas.

5.4 Low frequency noise background

Currents and voltages in an electronic circuit are perturbed from their given values due to interference of noise. The desired signal becomes difficult to distinguish when the noise power is significant in relation to the signal power. This is why noise has to be minimized in the electronic systems. One could categorize noise into two major forms, external sources and internal random fluctuations in the electronic transport process. External

noise comes from adjacent circuits, AC power lines, radio transmitters, etc., which may disturb the system in use. The major interest of noise study is from internal noise, it is the true noise from the system itself. Due to its random nature, this kind of noise cannot be completely eliminated and therefore limits the accuracy of measurement and sets a lower limit on how small the signals that can be detected and processed in an electronic circuit. Thus, noise is a fundamental problem in science and engineering, important to understand, characterize and consider in order to minimize its effects and estimate the accuracy of detected signals [135].

True noise in an electronic device is random, spontaneous perturbation from electronic conduction of the device itself. A common and powerful method to characterize and describe noise is by converting the problem from the time domain to the frequency domain by Fourier transformation. The noise analysis has been implemented in MOSFET devices for a long time and it sheds light on the current transport as well as traps information like density or distribution in the device. It can similarly be applied to RRAM cells for current transport and traps studies.

The excess noise above the well-known thermal noise and shot noise that shows up at low frequencies is the so-called low frequency noise. Other names are *1/f* noise or flicker noise. It is the common name for fluctuations with a power spectral density (PSD) propotional to $1/f^{\gamma}$ with γ close to 1, usually in the range 0.7 – 1.3. The PSD for $1/f$ noise takes the general form:

$$S_I = \frac{KI^\beta}{f^\gamma} \quad (5.1)$$

where K is a constant and β is a current exponent. $1/f$ fluctuations in the conductance have been observed in the low-frequency part of the spectrum (10^{-5} to 10^{7} Hz) in most conducting materials and a wide variety of semiconductor devices [136-139].

There are essentially two physical mechanisms behind any fluctuations in the current: carrier number fluctuations and mobility fluctuations. Generation-recombination noise from a large number of traps (number fluctuations) can produce $1/f$ noise if the time constant of traps are distributed as [140]:

$$g(\tau) = \frac{1}{\ln(\tau_2/\tau_1)} \text{ for } \tau_1 < \tau < \tau_2,\ g(\tau) = 0 \text{ otherwise.} \quad (5.2)$$

Some remarks are necessary about the addition of g-r noise spectra. First, it is assumed that the g-r noise from the traps can simply be added. This is true if the traps are isolated and do not interact [141]. Secondly, the traps are assumed to couple in the same way to the output current.

The other mechanism that can give $1/f$ noise is mobility fluctuations. It was first described by Hooge with the following empirical formula for the resistance fluctuations [142]:

$$\frac{S_R}{R^2} = \frac{\alpha_H}{fN} \quad (5.3)$$

The dimensionless parameter α_H, referred to as the Hooge parameter, was first suggested to be constant and equal to 2×10^{-3}. Later, it was found that α_H depends on the crystal quality. In the case of oxide-based RRAM device, it is believed that low frequency noise is attributed to carrier number fluctuation caused by trapping / de-trapping from defects in the oxide.

5.5 LFN analysis on oxide-based RRAM cell

Noise measurement is carried out on the three different states, fresh, HRS and LRS, and current normalized power spectral density (PSD) is plotted in Figure 5.9 under different bias conditions. It is seen that for all three states, PSD slopes are close to 1, which confirms the 1/f noise nature for the oxide-based RRAM devices. It can also be seen from the figure that the noise PSD is independent of bias conditions, which means it is an intrinsic characteristic of the current conduction.

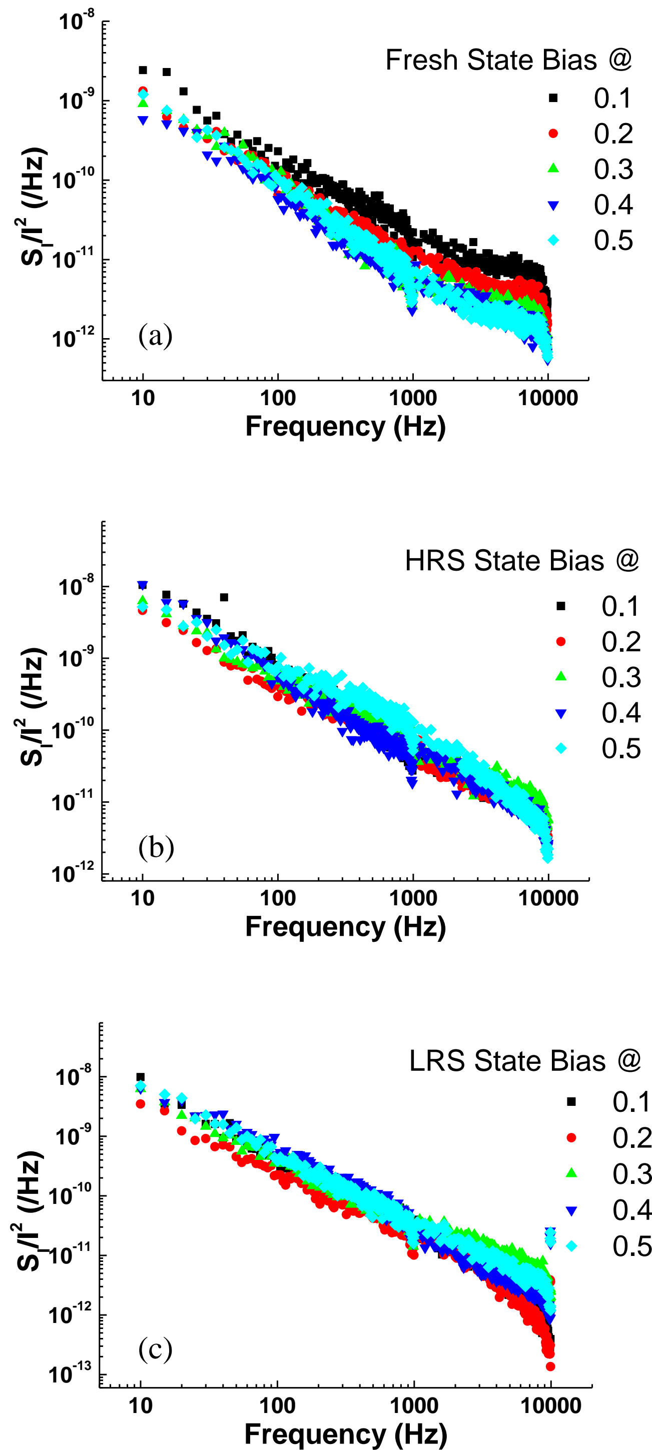


Figure 5.9 Normalized PSD plot for (a) Fresh (b) HRS (c) LRS states under small bias. The noise PSD is independent of bias conditions for all three states.

Bias of up to 0.5V is applied on LRS during noise measurement. This is to avoid further breakdown of the device (usually not recoverable), as for LRS it may reach compliance current (1mA) at a low voltage of around 0.6-0.7V. If the voltage bias is increased for noise measurement without compliance, it will cause further breakdown damage to the device as shown in the figure below. For this concern, only up to 0.5V biasing is used for noise measurement on scaling effect.

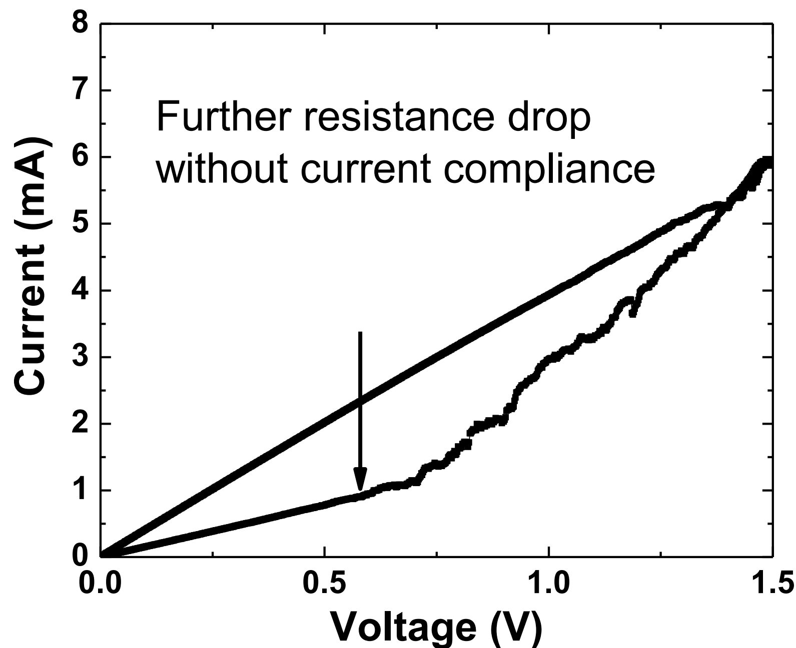
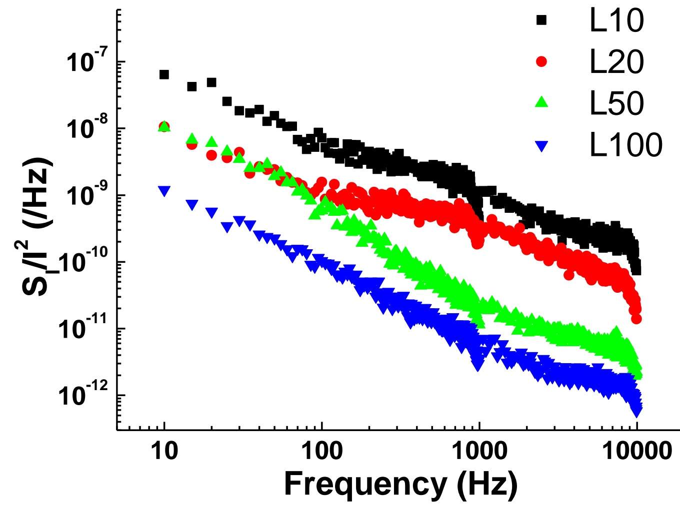
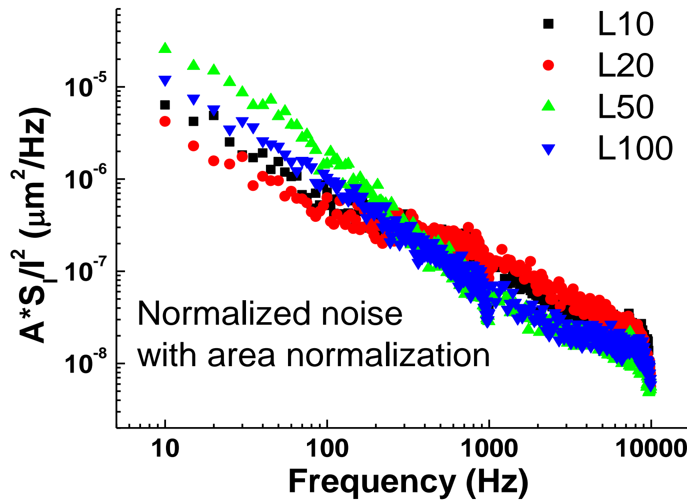


Figure 5.10 Illustration of breakdown of RRAM device applying large voltage bias without current compliance

LFN analysis of devices with different areas is compared in all three states - fresh, HRS and LRS in the following.



(a)

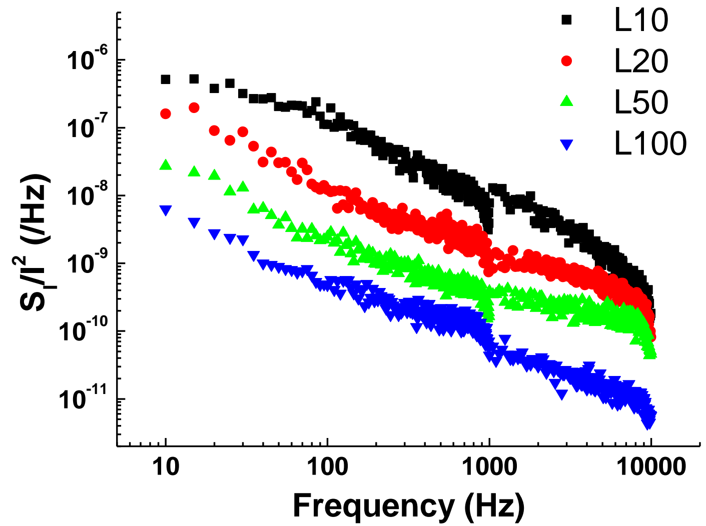


(b)

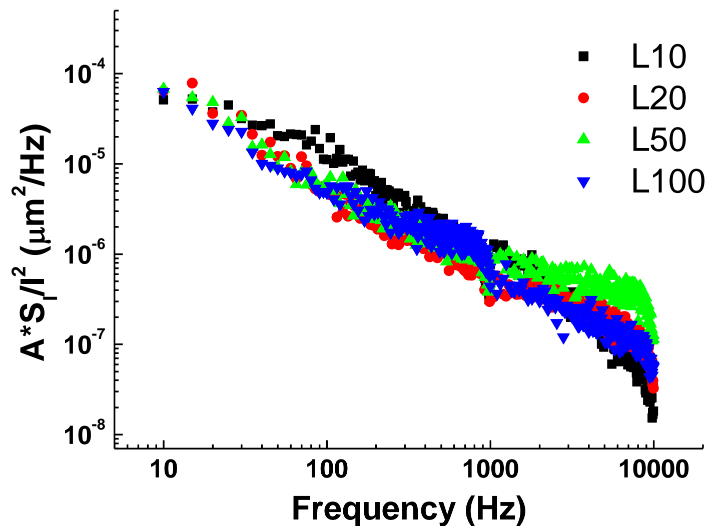
Figure 5.11 (a) Measured noise PSD of the fresh state for devices L10 to L100. (b) Area normalization on fresh PSD spectrum results in a similar noise level for all devices.

Figure 5.11 is the PSD spectrum of the fresh state for devices L10 to L100. It is seen that in Figure 5.11 (a) noise PSD scales reciprocally with the area (similar to the observation

in CMOS devices). To compare L10 with L100, a PSD level difference of around two orders of magnitude is observed. However, after normalizing with the device area, the four PSD curves fall into a similar level, as illustrated in Figure 5.11 (b).



(a)



(b)

Figure 5.12 (a) Measured noise PSD of the HRS state for devices L10 to L100. (b) Area normalization on HRS PSD spectrum results in a similar noise level for all devices.

Similar to that of fresh state, the HRS noise spectrum also shows a device area scaling effect as plotted in Figure 5.12 (a). Normalized current noise spectrum of L10 and L100 differs in about two orders. By multiplying the device area, all four PSD falls into a similar level as shown in Figure 5.12 (b). It is worth noting that the PSD for the HRS is at a slightly higher level than that of fresh state. One possible reason may be the effect of some residual tiny filament fragments formed during resistive switching cycles.

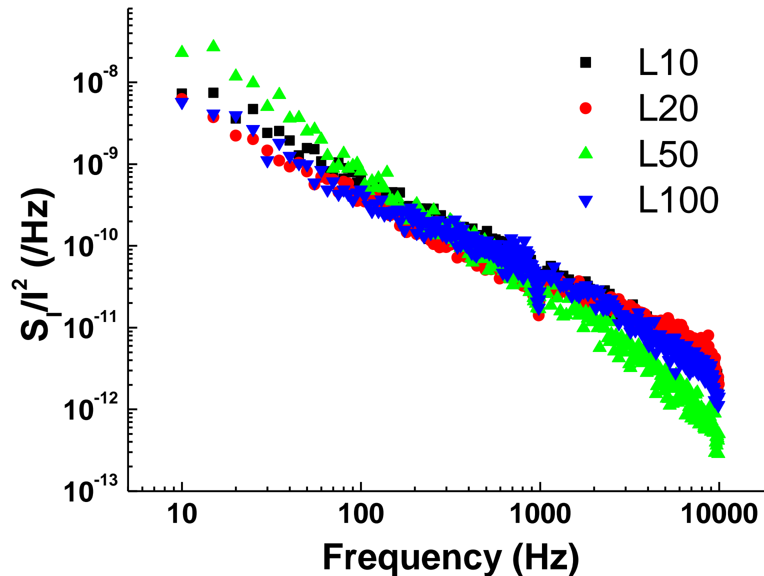


Figure 5.13 (a) Measured noise PSD of LRS state for device L10 to L100.

Unlike fresh or HRS, LRS current conduction is localized within the conduction filament. Thus, the LFN spectrum is expected to be independent of device areas. LFN study on devices with different areas is compared in Figure 5.13. It is can be seen that LFN PSD is similar for all four devices with various areas, which is consistent with the localized current conduction model in LRS.

5.6 Noise fluctuation model for LRS

It is commonly believed that the LRS conduction is due to the formation of filament involving oxygen vacancy related defects, although the "real" configuration of the conduction filament remains unclear [15, 62]. The localized current conduction in our device is confirmed by both DC current characteristics and LFN measurements. Therefore, the LFN in LRS can be modeled as a tiny filament or a nanowire as depicted in Figure 5.14. In this model, it is assumed that the LFN is produced by trapping/detrapping of electrons into/from traps surrounding the conduction nanowire [143]. Therefore, the traps are necessarily located in the dielectric surrounding the nanowire, that is the interface traps in HfO_2. In this figure, L is the length of the filament, which is the thickness of the sample, *r* is the radius of the conduction filament, and, the interface trap region that will affect the conduction current is indicated by the outer shell around the filament. Carriers in the conduction filament moving into and out of traps surrounding the isolated nanowire should give rise to fluctuation in the LRS conductance and, so, in LRS current.

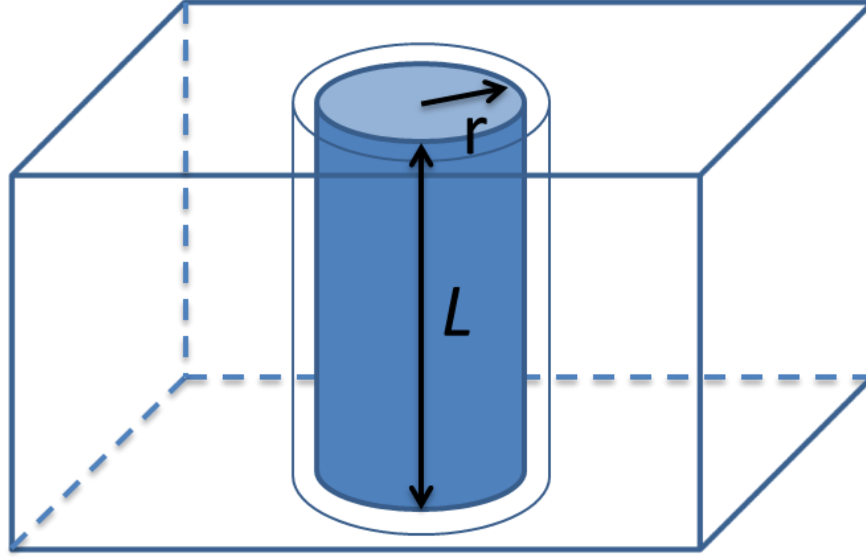


Figure 5.14 Schematic of filament conduction noise model for LRS, the outer shell indicates interface trap region that will affect the conduction current

With this configuration of an isolated nanowire surrounded by a dielectric, the normalized noise PSD in the LRS can be expressed in terms of the carrier number fluctuation theory [144]:

$$\frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{N_{it}\, kT 2\pi r L}{N^2 f} \tag{5.4}$$

where N_{it} is the interface trap density in HfO_x and N is the total carrier number in the filament with a carrier concentration n_0, and $N = n_0 \pi r^2 L$. Substituting carrier number expression into the above equation gives:

$$\frac{S_I}{I^2} = \frac{S_N}{N^2} = \frac{2N_{it}\, kT}{L\pi r^3 {n_0}^2 f} \tag{5.5}$$

Given an approximate filament radius of 5 to 10nm [143] and an empirical interface trap density in HfO_2 of 10^{10} to $10^{11}cm^{-2}eV^{-1}$ [145], the carrier concentration in the filament is plotted in Figure 5.15.

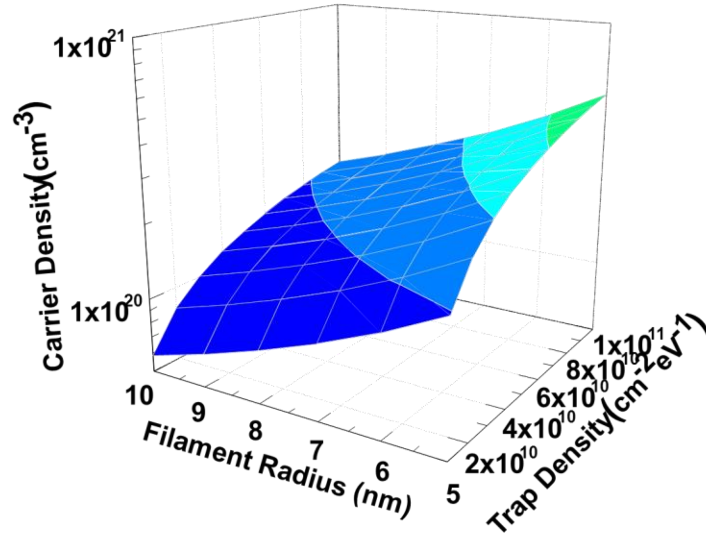


Figure 5.15 Calculated carrier concentration with commonly accepted parameter values of filament radius (5nm to 10nm) and interface trap density (10^{10} to $10^{11}cm^{-2}eV^{-1}$) at room temperature.

It can be seen that the carrier concentration is estimated to be around 10^{20} cm^{-3}. This carrier concentration corresponds to a metallic type of filament conduction, in good agreement with previous findings[112].

Other than carrier concentration estimation, the conductance of the filament can be roughly written as:

$$G = \frac{qn_0\mu\pi r^2}{L} \tag{5.6}$$

Take a few commonly accepted values to substitute into the equation, it gives an estimation on the carrier number and mobility:

- $N_{it} = 10^{10} cm^{-3}, r = 3nm$ ➔ $n_0 = 3.548 \times 10^{20} cm^{-3}$, $\mu = 168.2\, cm^2/V \cdot s$
- $N_{it} = 10^{10} cm^{-3}, r = 5nm$ ➔ $n_0 = 1.649 \times 10^{20} cm^{-3}$, $\mu = 130.3\, cm^2/V \cdot s$
- $N_{it} = 10^{11} cm^{-3}, r = 3nm$ ➔ $n_0 = 1.122 \times 10^{21} cm^{-3}$, $\mu = 53.2\, cm^2/V \cdot s$
- $N_{it} = 10^{11} cm^{-3}, r = 5nm$ ➔ $n_0 = 5.214 \times 10^{20} cm^{-3}$, $\mu = 41.2\, cm^2/V \cdot s$

If it is assumed to be a pure Hf metal filament inside, it takes $\rho = 33.1\mu\Omega \cdot cm$ and with an approximate LRS resistance of 400Ω, it gives the radius of filament:

$$R = \rho \frac{L}{A} = \frac{\rho L}{\pi r^2} \Rightarrow r = 1.623nm \qquad (5.7)$$

and assume electron concentration is equal to atom density of Hf metal, it gives $m_0 = 4.489 \times 10^{22} cm^{-3}$. With these values, and expression of noise, trap concentration in HfO_x is calculated as $2.545 \times 10^{21} cm^{-3}$. This value is not in a reasonable range and also the radius would be too small [143, 146-147]. It suggests a filament that is not pure Hf metal, it might be certain kind of oxygen deficient oxides which is highly conductive as reported in the literature [15].

5.7 Current conduction model for filament type RS cell

During DC resistive switching measurement, by properly controlling the reset stop voltage, different resistance levels could be achieved as illustrated in Figure 5.16.

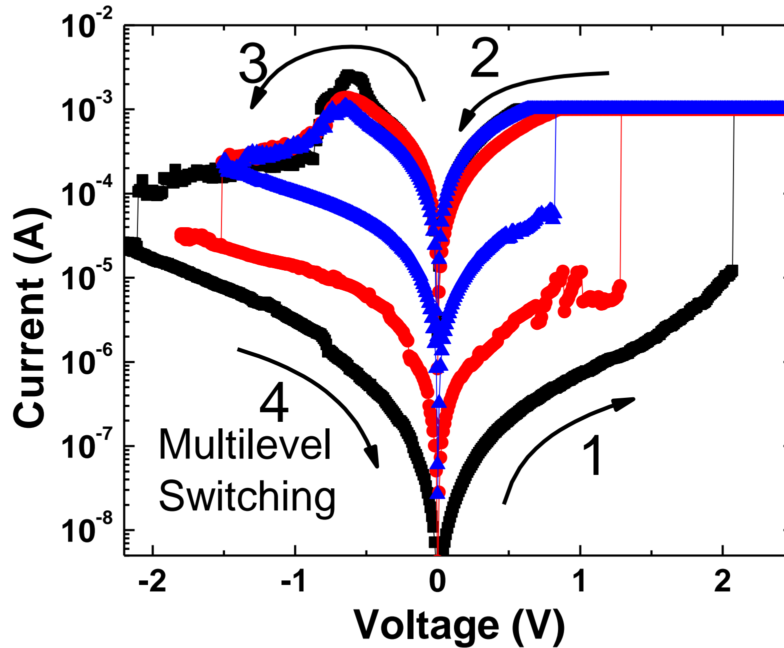


Figure 5.16 Multi-level resistive switching in oxide-based RRAM device produced by different reset stop voltage. More levels could be achieved by carefully control measurement conditions

It is commonly accepted that for HfO_x based RRAM, resistive switching is caused by oxygen vacancies related conductive filament (CF) formation and rupture as discussed in the previous chapters [16, 115]. Figure 5.17 is the schematic representation of resistance evolution from high conductive LRS to highly resistive HRS in the filament type switching device. It also illustrates intermediate resistance levels formed by reduction of filament size or partial rupture of filament. With this configuration, current conduction in the cell can be modeled into two parts. One is the highly conductive filament region; the other is the uniform leakage oxide region. The total resistance of the device is the parallel

combination of the filament resistance R_F and the uniform resistance R_U and can be expressed as:

$$R_t = (\frac{1}{R_F} + \frac{1}{R_U})^{-1} \text{ or } G_t = G_F + G_U \tag{5.8}$$

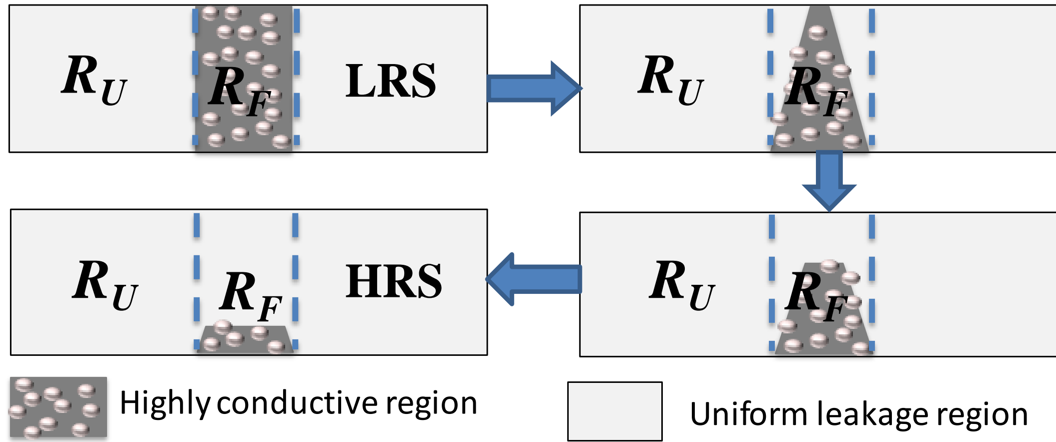


Figure 5.17 Schematic illustration of resistance change in the memory cell. Between highly conductive LRS (top left) and highly resistive HRS (bottom left), there are intermediate resistance levels caused by reduced or partial ruptured conduction filament.

When the CF is formed, R_F will be much smaller than R_U, total resistance equals nearly to R_F. Thinning or partial rupture of conductive filament reduces the filament conductivity and gives rise to the total resistance which will in turn result in intermediate resistance levels. When the CF is totally ruptured, device resistance approaches to the value of uniform oxide resistance R_U and the amplitude of leakage current is proportional to device area.

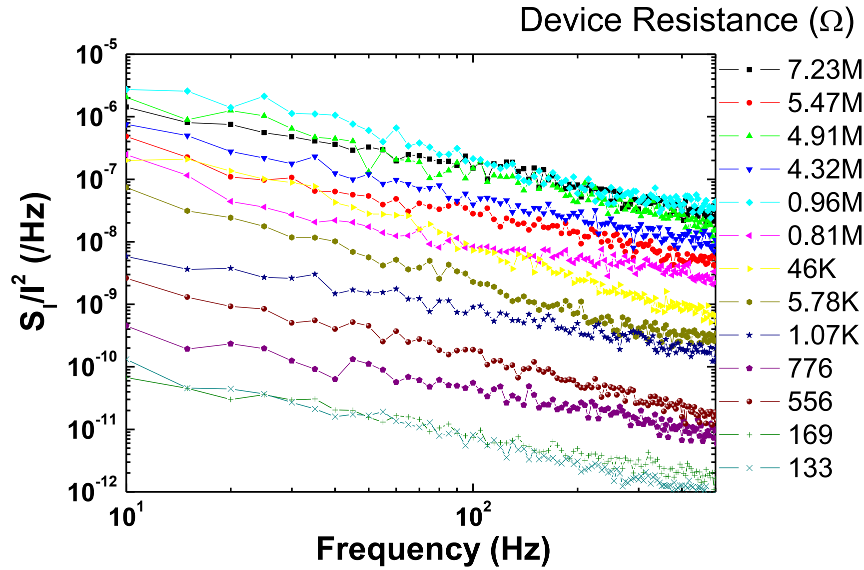
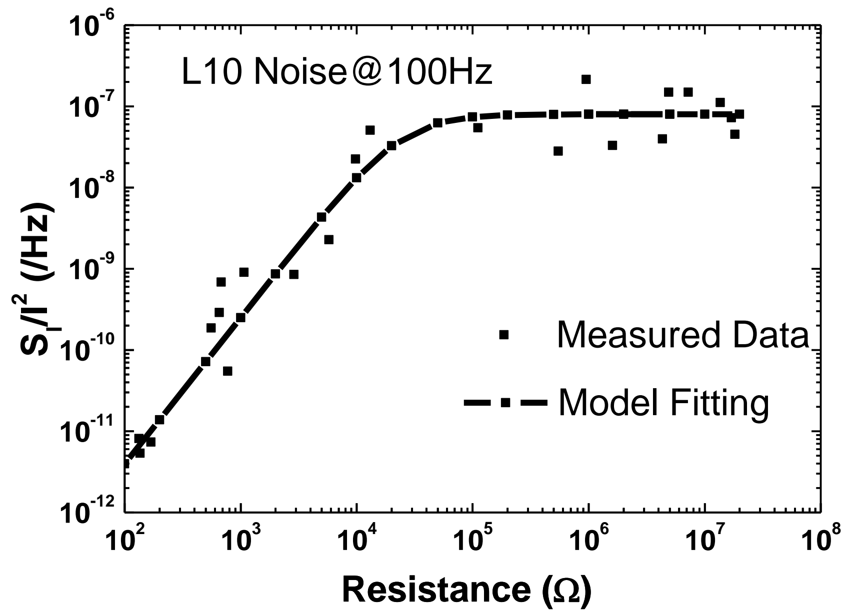


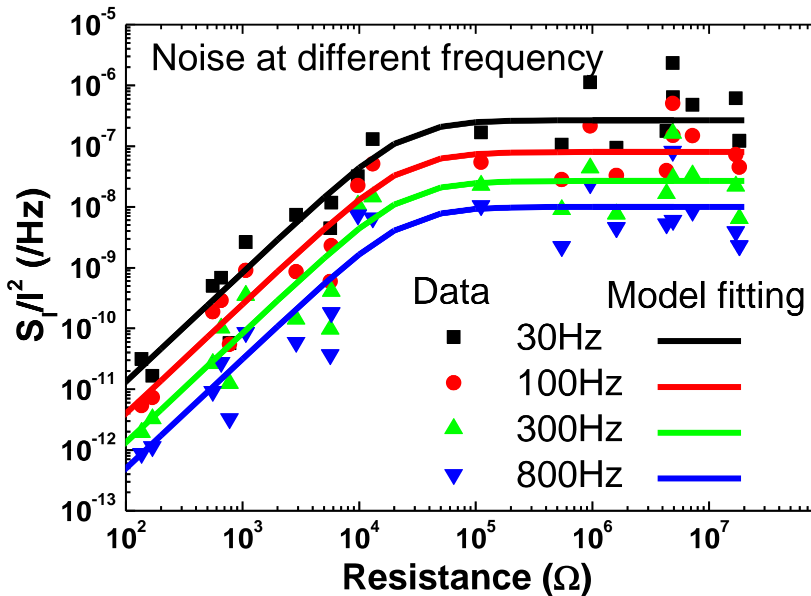
Figure 5.18 Normalized LFN power spectral density measured at different resistance states from a set of five L10 devices.

This conduction model is supported with LFN analysis by measuring power spectral density (PSD) at different resistance states. Typical *1/f* noise is observed in such devices without noticeable electrical bias dependence [148]. In the low resistance regime, the CF is formed and current conduction as well as LFN behavior is dominated by this highly conductive region, which varies with changing resistance. When the filament vanishes, the total resistance increases and the uniform conduction oxide region contributes more and more. Thus, noise behavior will be dominated by R_U, which is approximately a constant value. It can been seen from Figure 5.18 that at low resistance values, normalized PSD level increases with higher resistance; however, after the device resistance reaches a certain value, the noise spectrum is relatively constant for all the

resistance values above that. To better observe this trend, normalized PSD is plotted versus device resistance in Figure 5.19.



(a)



(b)

Figure 5.19 (a) PSD versus resistance plot of L10 device at 100Hz and model fitting. (b) Model fitting of PSD versus resistance plot at different frequencies

This noise spectrum trend can be explained like this: in the low resistance regime, CF is formed and current conduction as well as LFN behavior is dominated by this highly conductive region, which varies with changing resistance; as filament starts vanishing, total resistance increases and the uniform conduction oxide region contributes more and more, noise behavior will be dominated by R_U, which is approximately a constant value. Start from Equ. (5.8), the following can be derived:

$$\delta G_t = \delta G_F + \delta G_U \tag{5.9}$$

Then the LFN PSD can be expressed as:

$$S_{G_t} = S_{G_F} + S_{G_U} \tag{5.10}$$

$$\frac{S_{Gt}}{{G_t}^2} = \frac{S_{G_F}}{{G_F}^2} \cdot \frac{{G_F}^2}{{G_t}^2} + \frac{S_{G_U}}{{G_U}^2} \cdot \frac{{G_U}^2}{{G_t}^2} \tag{5.11}$$

i.e. $$\frac{S_I}{I^2} = \frac{S_{Gt}}{{G_t}^2} = \frac{S_{Rt}}{{R_t}^2} = \frac{S_{R_F}}{{R_F}^2} \cdot \frac{{R_t}^2}{{R_F}^2} + \frac{S_{R_U}}{{R_U}^2} \cdot \frac{{R_t}^2}{{R_U}^2} \tag{5.12}$$

Seen from (5.12), at low R_t, $R_U >> R_F$, so $R_t \approx R_F$ and

$$\frac{S_{Rt}}{R_t^2} \approx \frac{S_{R_F}}{R_F^2} \tag{5.13}$$

At high R_t, $R_F >> R_U$, so $R_t \approx R_U$, and

$$\frac{S_{Rt}}{R_t^2} \approx \frac{S_{R_U}}{R_U^2} \tag{5.14}$$

So the overall noise can also be approximated as:

$$\frac{S_I}{I^2}=\frac{S_{Gt}}{G_t^{\ 2}}=\frac{S_{Rt}}{R_t^2}\approx\left[\left(\frac{S_{R_F}}{R_F^2}\right)^{-1}+\left(\frac{S_{R_U}}{R_U^2}\right)^{-1}\right]^{-1} \tag{5.15}$$

It should be noted here for resistance approximations, R_U>>R_F means R_U should be at least 10 times of the value of R_F. Moreover, it assumes that at low R_t, R_U>>R_F, which is only true when device area is much larger than conductive filament size (this is the case in this study with device dimension in micrometers). If cell scales down to nanometer range, this approximation may not hold. And also to assume a uniform leakage oxide for high resistance, it requires a nearly complete recovery of conductive filament to give a high resistance close to that of fresh resistance.

In Figure 5.19 (a), normalized noise PSD S_I/I^2 of device L10 at 100Hz versus resistance R_t is plotted and fitted with approximation Equ. (5.15). It is seen that in the low resistance regime, S_I/I^2 increases as a power law of resistance while keeps nearly constant at high resistance regime. As so, Equ. (5.12) can be re-written as:

$$\frac{S_I}{I^2}=\frac{S_{Gt}}{G_t^{\ 2}}=\frac{S_{Rt}}{R_t^{\ 2}}=\frac{A_F}{f}\cdot\frac{R_t^{\ 2}}{R_F^{\ 2}}+\frac{B_U}{f}\cdot\frac{R_t^{\ 2}}{R_U^{\ 2}} \tag{5.16}$$

where PSD expression A_F for filament noise varies as $R_t^{1.79}$ according to the fitting and PSD expression B_U for uniform leakage oxide is at constant noise level of around 8×10^{-8} /Hz at 100Hz. This power variation relationship has also been reported similarly in the literature by S. B. Lee, et. al. [131]. It is presented in the letter that according to percolation theory: $S^R/R^2 \propto R^w \ at\ p > p_c$, where p_c is the percolation threshold. And

the w value measured in their work is 1.8 ± 0.3, which is related to the current distribution in the percolation network. In addition to that, Joule heating and associated thermal dissipation processes as well as possible movement of ions may also affect the current flow [131].

Based on these values, normalized PSD at different frequencies are also plotted and fitted in Figure 5.19 (b) at four frequency points of a set of devices with approximation equation, it fits all fours lines quite well. Of course, there is some scattering of data points around the fitted line, likely due to experimental uncertainties or to variability related to oxygen vacancy defects which are hard to control.

Since in the low resistance regime conduction is mainly from the CF, noise spectrum will depends on the properties of the CF rather than the device area. On the other hand, the high resistance noise is mainly related to the area of the device. To explicitly include the area dependence of LFN model, the expression for overall noise PSD can be modified as follows:

$$\frac{S_I}{I^2} = \frac{S_{Gt}}{{G_t}^2} = \frac{S_{Rt}}{{R_t}^2} = \frac{A_F}{f} \cdot \frac{{R_t}^2}{{R_F}^2} + \frac{K_U}{WLf} \cdot \frac{{R_t}^2}{{R_U}^2} \tag{5.17}$$

where K_U is the PSD expression for uniform leakage oxide without area effect, W is the width and L is the length of the device area.

To verify this expression, PSD of four different device areas are measured on L10, L20, L50 and L100, respectively. As can be seen from Figure 5.20, the model accounts very well for both variations of noise PSD with different resistance states and device areas, emphasizing the physical consistency of this approach.

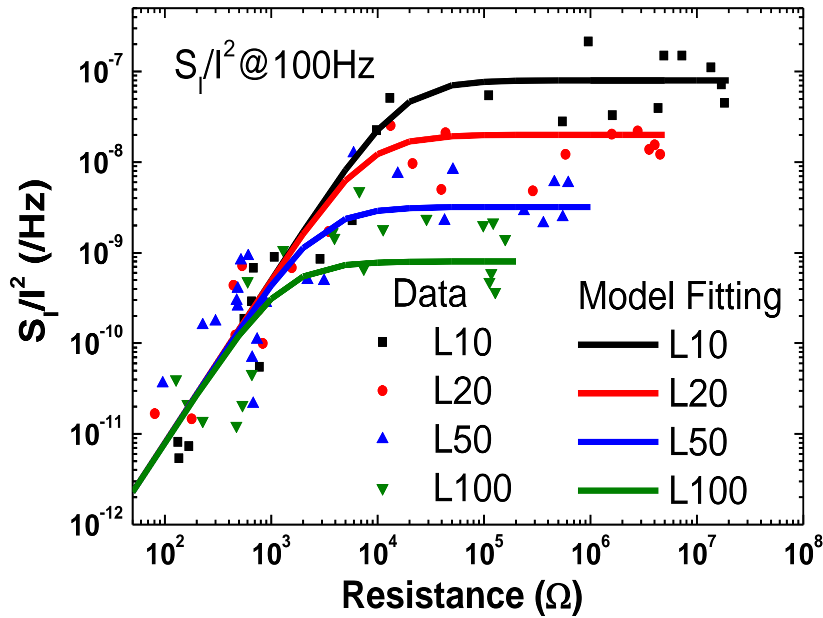


Figure 5.20 Normalized noise versus resistance plot of devices with four different areas and model fitting

5.8 Summary

Current conduction mechanism in oxide-based RRAM device has been investigated with DC measurement and LFN analysis in this chapter. It is confirmed that for LRS, current conduction is localized without area dependence, whereas, for HRS, uniform leakage

current scales with device area. Moreover, LFN analysis has been implemented on the HfO_x based RRAM devices with different resistance levels to investigate the current conduction mechanism. It is found that the cell could be treated as two parallel resistances of conductive filament and uniform leakage oxide. In the low resistance regime, the filament resistance dominates current conduction as well as LFN behavior, where noise PSD varies to the power of the filament resistance. While in the high resistance regime, the uniform oxide dominates, which results in a roughly constant noise level.

Based on the analysis, an ungated nanowire or filament conduction fluctuation noise model has been proposed for LRS, allowing estimation of filament carrier concentration that is found to be in a reasonable metallic conduction range. Further, a noise model is proposed for this type of switching cell, and the simulated curve fits experimental data quite well.

Chapter 6 Oxide-Based RRAM Device Performance Improvement by Material Optimization

6.1 Introduction

As one of the most promising next generation nonvolatile memory candidates to replace transistor-based flash memory, resistive random access memory (RRAM) has been extensively studied since 1990s owing to its high scalability, fast switching speed and ease of fabrication [9, 43]. One of the transition metal oxides, HfO_x, has recently been reported with high performance for resistive switching [8] and its switching mechanism has been attributed to a model based on the local conduction filament [16, 115]. Despite recent advancements in the performance of RRAM devices, for aiming at mass production one of the most challenging tasks is to address the concern of the broad dispersion of switching parameters (i.e. uniformity on cycle to cycle within one device, and device to device) that are generally observed in the RRAM cells. The non-uniform device parameters (including set voltage, reset voltage / current and on & off state resistance), which is believed to be mainly due to the randomness of local filament formation and rupture, shall negatively affect the programming / erasing or read operation of the RRAM cells, and make them un-repeatable. On the other hand, for the reported high performance RRAM devices, a forming process [62] is generally required

to initialize the switching behavior, which might add complexity to the RRAM circuit operation due to the high voltage needed for forming.

To tackle these concerns on the device uniformity, several methodologies have been reported, including ion doping or using different material stacks [11-13, 30, 59]. In this chapter, a forming free RRAM cell with significantly improved uniformity as compared to the reported literatures, achieved using HfO_x/TiO_x multilayer (ML) dielectrics as the switching material is discussed. Both Ti doping into HfO_x effect and the confinement of conduction filament between multi-layers are believed to be responsible for the improvement.

6.2 Design of experiment

Same as previous chapters, HfOx based RRAM devices are used in this study. 20 nm Ti adhesion layer and 50 nm Pt bottom electrode are first deposited on 8-inch silicon substrate by electron beam evaporation. Then, ~ 4 nm HfO_x is deposited by reactive sputtering in argon and oxygen ambient, ~ 2 nm of TiO_x is prepared by oxidation of Ti film. These two processes are repeated to produce the final four-layer oxide structure of HfO_x / TiO_x / HfO_x / TiO_x. After 50 nm TiN top electrode is deposited with reactive sputtering and patterned with traditional lithography, dry etch is done to finish the square-shape devices. The control sample of single layer (SL) oxide is in the meanwhile prepared with 10 nm reactive sputtering HfO_x and keeping all other processes the same.

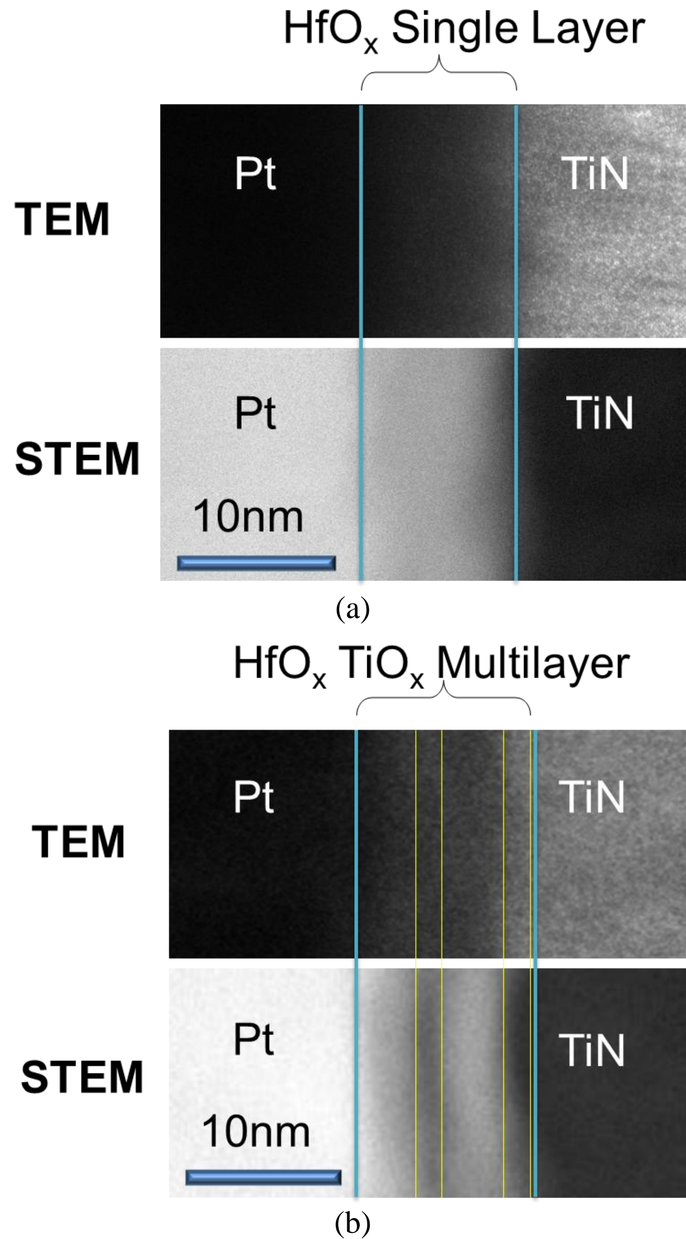


Figure 6.1 High resolution TEM pictures of (a) single layer device, revealing an oxide thickness of 10nm (b) multilayer device indicating four layers of oxides between top and bottom electrodes and a total dielectric thickness of around 10 to 12nm.

Micro morphologies are studied with high resolution cross-sectional transmission electron microscopy (TEM) for both single layer control device and multilayer device in Figure 6.1. In the control device TEM picture Figure 6.1 (a), shows an oxide thickness of 10nm, which is commonly used in this work. While for the multilayer device in Figure 6.1 (b), it reveals four layers of oxides between top and bottom electrodes with a total thickness of around 10 to 12nm. It is slightly thicker than the control device, which is due to the consideration that TiO_x is more conductive than HfO_x.

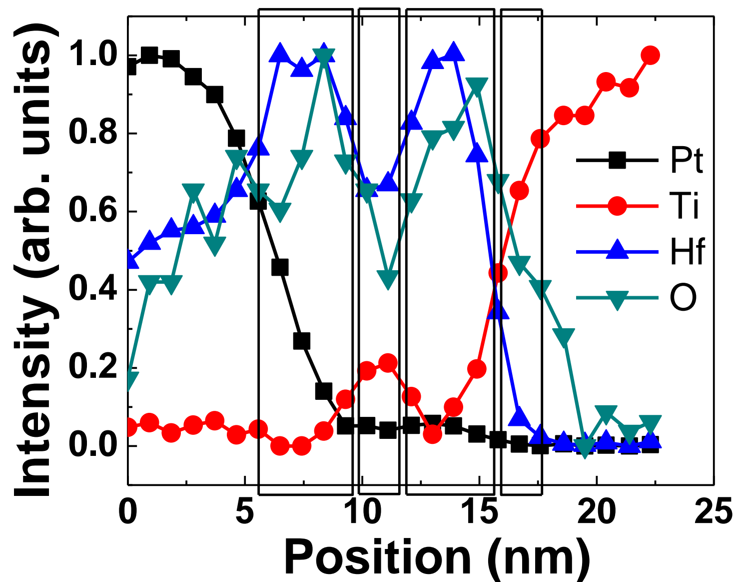


Figure 6.2 EDX spatial profile of multilayer device. Two Hf and O peaks and two Ti peaks with one merging into TiN electrode signal observed, indicating four layers of oxides sandwiched in between electrodes.

To get further information on the multilayer oxide composition, energy-dispersive X-ray (EDX) spatial profile is presented in Figure 6.2. It can be seen that between Pt (black line

with square symbols) and TiN electrodes (red line with round symbols), there are two peaks of Hf and O, and also there are two peaks of Ti, while the right one merges with Ti signal from electrode TiN. These peaks indicating two layers of HfO_x and TiO_x placed alternatively between two electrodes.

6.3 Forming free in multilayer device

It is believed that the sandwiched TiO_x layers may serve three-fold purposes: Firstly the TiO_x layers may attract oxygen from HfO_x layers during fabrication process, so to create oxygen vacancies related defects [149] within the dielectric. This is possibly the reason that makes the device forming free as discussed later. Secondly, during resistive switching, the TiO_x layers may also serve as oxygen reservoir to recover conduction filament created by set process. Thirdly, Ti may also diffuse into HfO_x as the doping atoms to stabilize the filament formation [111]. Electrical characterization of memory devices used to present the performance improvement are carried out using Keithley 4200 SCS and the data collected are mainly from 100 μm^2 devices.

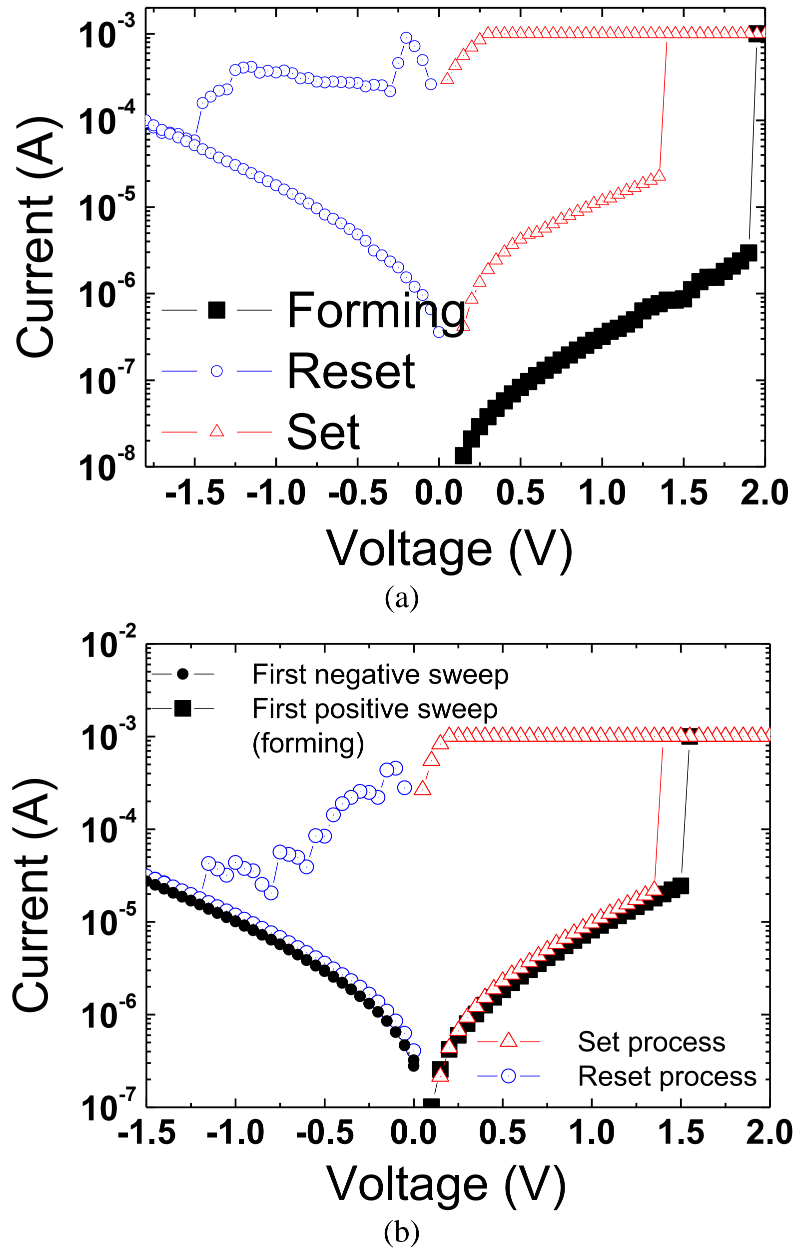


Figure 6.3 (a) Forming and set / reset process for single layer HfO_x control device. The conductive paths need to be formed before bipolar resistive switching cycles. The forming voltage is as large as 1.95V, which is about 0.5V larger than that of set voltage. (b) Initial set / reset process in multilayer device. No forming is needed for such devices. The voltage of first forming sweep is similar to the following set voltage and fresh resistance is also similar to that of HRS state.

Figure 6.3 (a) illustrates the typical forming, set and reset process of the SL device. As the fresh resistance is usually much higher than that of reset HRS state, it requires a forming voltage larger than set voltage to initiate bipolar resistive switching. In the case of the device plotted in this figure, the forming voltage is about 0.5V larger than set voltage. However, in the ML device of Figure 6.3 (b), it is seen that the HRS resistance is comparable to the fresh state without electrical forming. Moreover, the first set voltage or so-called forming voltage is also comparable to or sometimes even lower than the subsequent set voltage (data not shown here). Combine these points, it means the conventional forming process is not necessary for such ML devices. As stated earlier, this may be attributed to the defects created by Ti attraction of oxygen, which increases the leakage current in fresh state that gives an effectively lower resistance, making it closer to HRS state. Hence in such a manner, their breakdown voltages become similar.

Statistical data of the forming voltage for the SL device and first set voltage for the ML device are shown in Figure 6.4. As can be seen from the figure, there is an average difference of 0.3V to 0.5V between the SL and ML devices. The average set voltage of the SL and ML devices are comparable, while the first set transition voltage as well as the fresh resistance of ML are lower than those of SL devices.

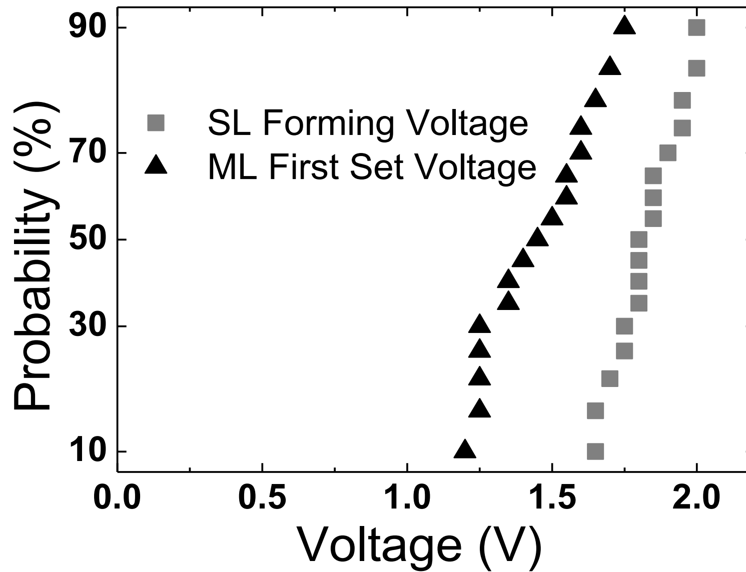
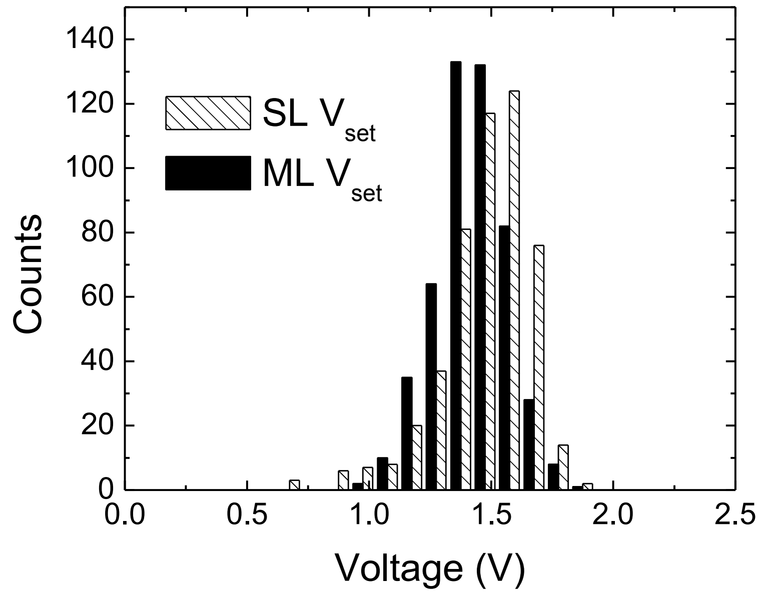


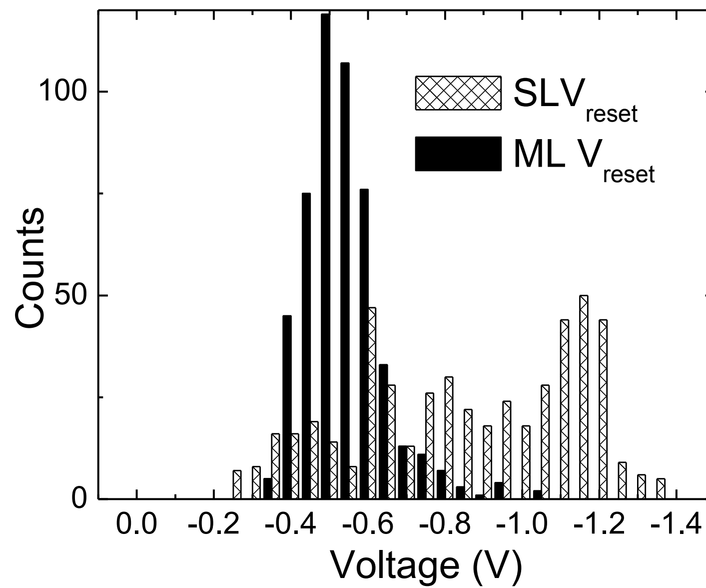
Figure 6.4 Distribution of forming voltage for SL device and first set voltage for ML device, which shows and average difference of 0.3 to 0.5V.

6.3 Uniformity improvement of operation parameters in both cycle to cycle and device to device regime

As mentioned in the previous part of this chapter, TiO_x layers inserted in the dielectric serves as oxygen reservoirs for the reset process and Ti ions also attribute to doping effect of stabilizing conductive filament formation [7]. Two layers of HfO_x can also confine filament formation during set process [150]. Combine these effects, the resistive switching of ML device is expected to be much better controlled than SL. In this part, operation parameters are compared for SL and ML from both cycle to cycle and device to device to demonstrate uniformity improvement in the ML devices.



(a)



(b)

Figure 6.5 Operation parameter comparison of 500 DC switching cycles from a single device. (a) Set voltage of SL and ML device, showing a similar distribution profile and range, with standard deviation improvement from 0.19 in SL to 0.14 in ML device. (b) Reset voltage distribution, obvious improvement can be seen in ML device, and standard deviation reduces from 0.41 to 0.12.

Single device resistive switching voltage of 500 DC cycles for both SL and ML based devices are compared in Figure 6.5. It is seen that for set voltage distribution, there is no significant difference between the SL and ML structure for a single device. The average set voltage is 1.47V for SL and 1.42V for ML, with standard deviation improvement from 0.18 in SL to 0.14 in ML. Since the reset process of bipolar switching is usually gradual, in contrast to the abrupt transition of the set process, the voltage at which resistance reaches a critical level (eg. 20kΩ in this work) is defined as reset voltage here. In Figure 6.5 (b), an improvement of more than two times in reset voltage distribution can be seen for ML device; the standard deviation reduces from 0.41 in SL to 0.12 in ML structure.

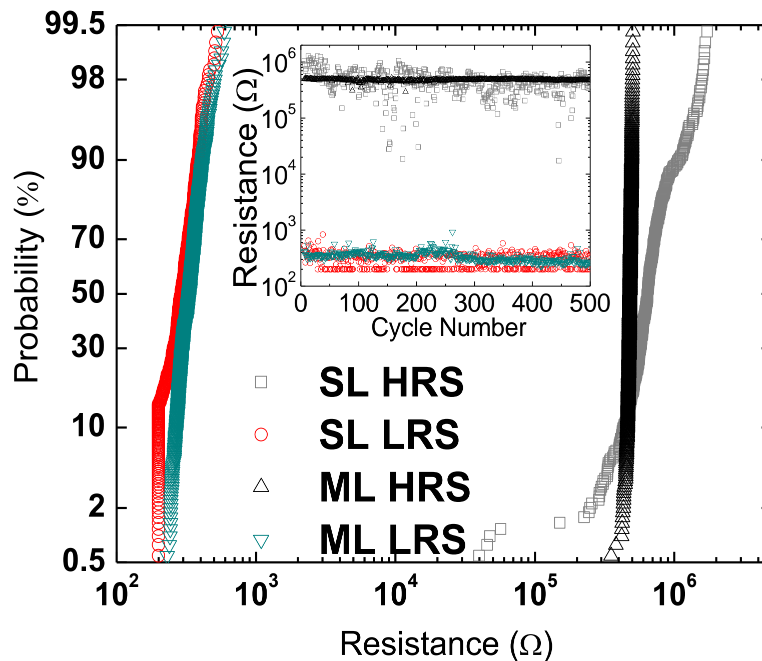
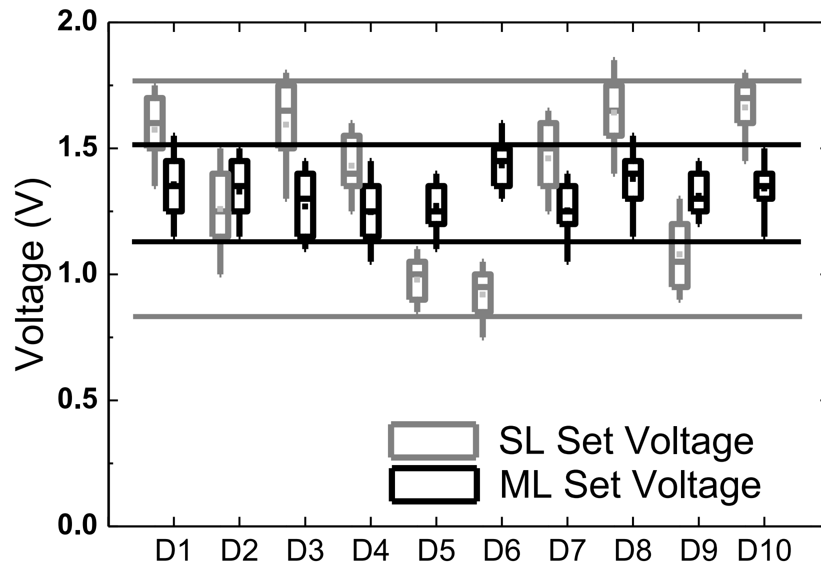


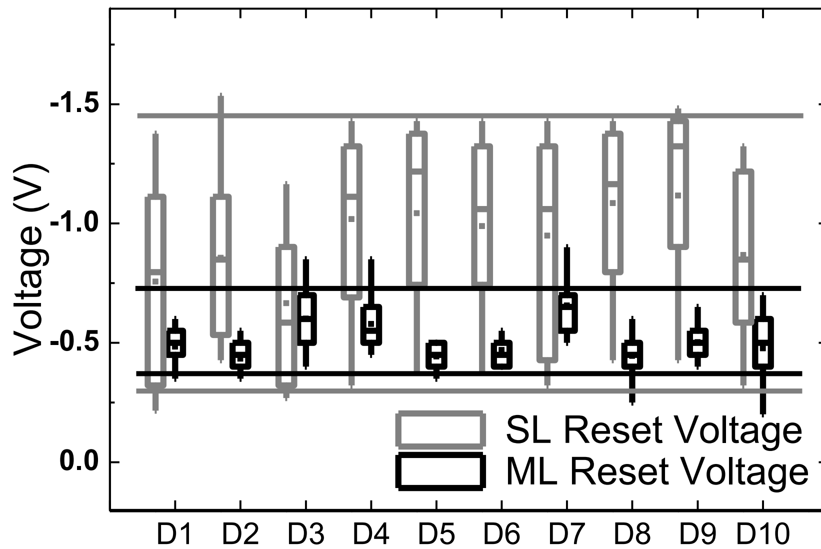
Figure 6.6 Resistance distributions of 500 DC cycles from one device each of SL and ML structure. Inset is the LRS / HRS resistance versus cycle number plot. HRS distribution of around two orders in SL reduces to only about two times in ML device.

In Figure 6.6, the on / off resistance distributions from 500 DC switching cycles is plotted. HRS distribution within two times of variation is achieved in the ML device compared to that of around two orders in the SL device. The LRS distribution is similar for both devices, which is usually limited by compliance current. It is worth noting that some of SL LRS resistance values (red circle symbol) reach compliance current at reading voltage, this means the actual resistance is smaller than those plotted in the figure, which will make the LRS distribution a bit larger. The inset of this figure is the resistance versus cycle number plot. For both the SL and ML devices, there is no severe degradation of memory window after 500 switching cycles.

To further characterize the device to device variation of the two structures (SL and ML), 100 switching cycles from 10 randomly selected devices on the 8-inch wafer are summarized in Figure 6.7. For the floating box chart, the top and bottom whiskers indicate 90% and 10% distribution respectively and the box represents 75% to 25% range. 50% point is indicated as the bar inside the box and the mean value is represented as the dot inside the box. Though the set voltage distribution for one single device is similar for two structures as presented in Figure 6.5 (a), device to device dispersion is improved from ~1 V in SL devices to ~0.4 V in ML devices. Similarly, as shown in Figure 6.7 (b), the device to device reset voltage variation reduced to more than a half for ML devices (from ~ 1.2 V to ~ 0.4 V).



(a)



(b)

Figure 6.7 (a) Set voltage distribution (b) Reset voltage distribution of 100 switching cycles of 10 devices selected on an 8 inch wafer. For floating box chart, the top and bottom whiskers indicate 90% and 10% distribution and the box represents 75% to 25% range. 50% point is indicated as the bar inside the box and the mean value is represented as the dot inside the box

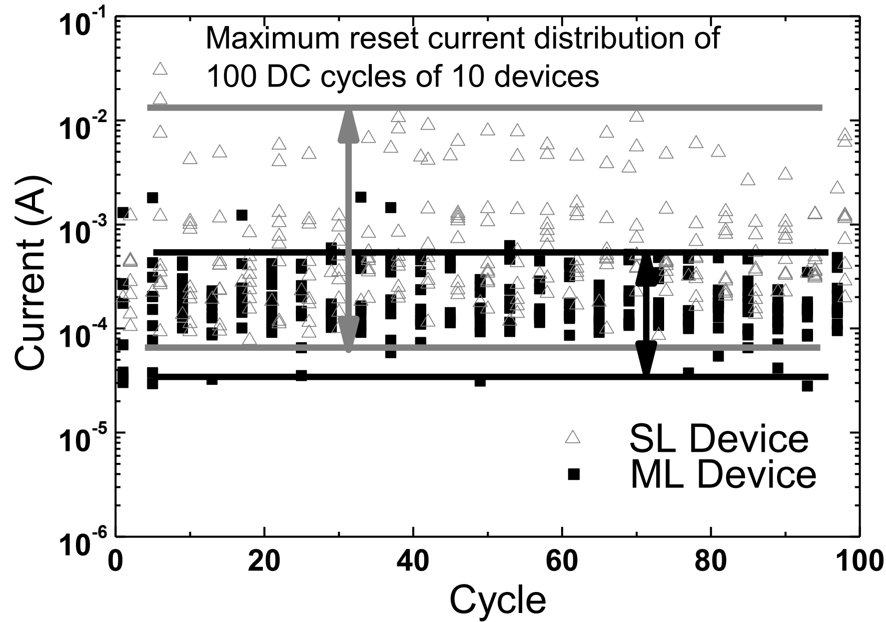


Figure 6.8 Maximum reset current of 100 switching cycles from 10 devices each from SL and ML structures. Compare to SL, ML device shows a tighter reset current distribution as well as lower amplitude.

Besides transition voltage, reset current is also one of the important parameters to evaluate device performance in RRAM as it is directly related to the power consumption, which is a major concern in integrated circuit chips nowadays [151-152]. In Figure 6.8, maximum reset current is also plotted for 100 switching cycles from 10 devices each with SL and ML structures. Current as high as 10mA can be seen in SL device and the median value is about 1mA. However, in ML device, the maximum reset current median value drops to around 200 μA, this may be attributed to the Ti assisted filament recovery during reset process. It is reported that reset current might be reduced with lower compliance current to a certain level, however, it does not work well here. This can be probably

attributed to the parasitic capacitance discharging during set process current overshoot [101, 106].

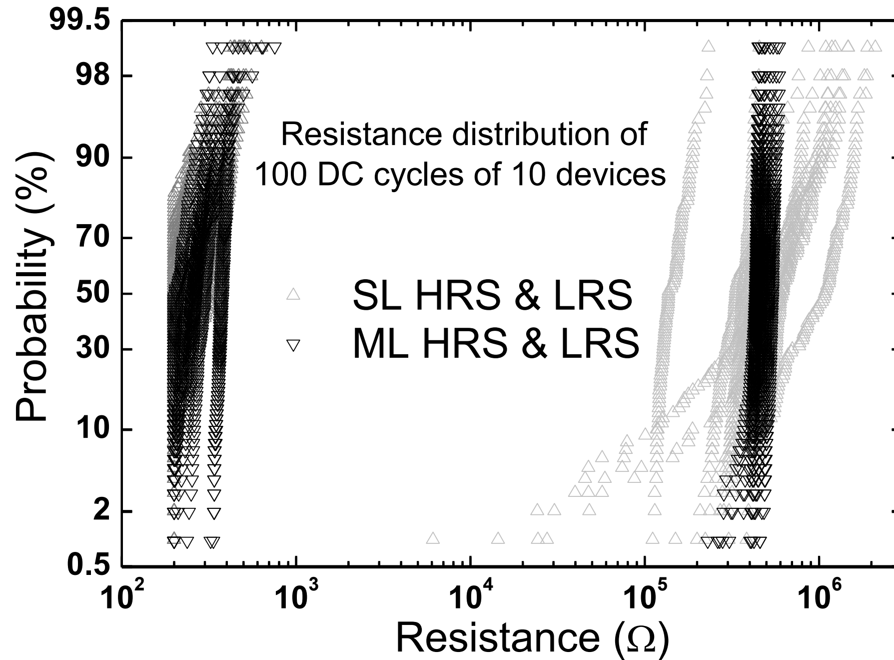


Figure 6.9 HRS / LRS resistance distribution of 100 switching cycles from 10 devices each with SL and ML structures. LRS distribution is similar, while HRS distribution reduces from more than two orders in SL to only about three times for 10 devices in ML structure.

HRS and LRS resistance probability is also plotted in Figure 6.9. Similar to the single device, LRS distribution is close for SL and ML. However, HRS resistance distributions for ML are much more compact than SL. Dispersion of more than two orders in SL reduces to only about three times in 10 devices with ML structure.

Although electrical measurement is mainly carried out in DC bias conditions, short electrical pulse is also used to test the switching speed of the fabricated device as shown

in Figure 6.10. An increasing trend can be seen in the amplitude of voltage with reducing of pulse width. Switching speed as fast as 5ns has been demonstrated in multilayer RRAM device with set voltage at +2.1V and reset voltage at -3V.

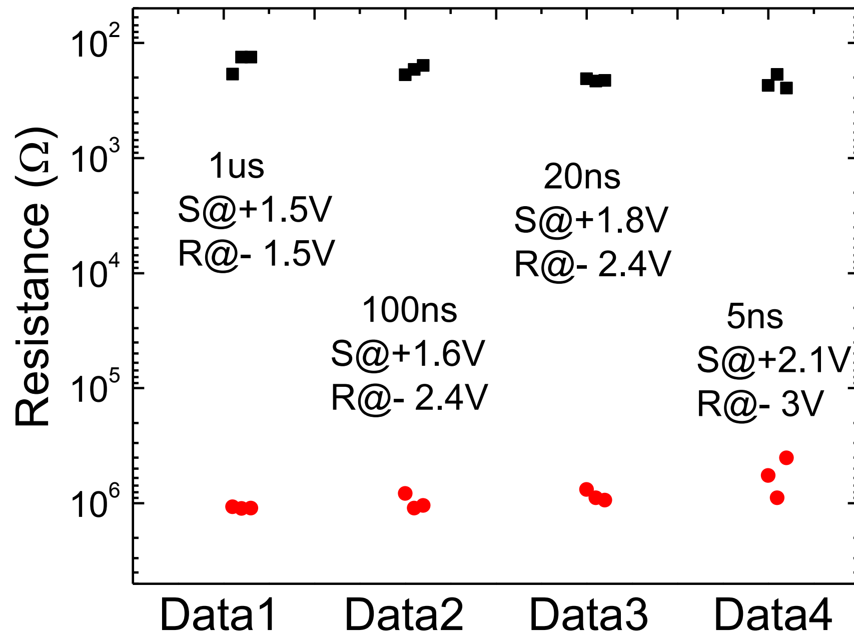


Figure 6.10 Electric pulse switching of multilayer RRAM device. It shows an increasing trend in voltage amplitude as pulse width reduced. Switching speed as fast as 5ns has been demonstrated with set voltage of +2.1V and reset voltage of -3V.

As discussed previously, formation and rupture of local conduction filament with the assistance of REDOX reaction is widely accepted to explain the bipolar resistive switching behavior [15]. In the ML structure reported in this work, during the formation of TiO_x layer, the TiO_x attracts oxygen from HfO_x to create oxygen vacancy related defects that weakens the strength of the dielectric [69], which leads to the reduction of the

resistance of fresh oxide and the first switching voltage (forming), as compared to the SL HfO_x based devices. In the meanwhile, Ti may diffuse into HfO_x to serve as dopants, which may result in a lower oxygen vacancies formation energy [111]. During reset process, this thin TiO_x layer may serve as oxygen reservoir to recover the conductive path, which makes the process more effective. In addition, confinement of filament between two HfO_x layers may also contribute to the improvement of the switching parameter dispersions [150].

6.4 Chemical insight of forming free behavior in multilayer device

In the filament type resistive switching memory cell, usually an initial forming process is required to form a percolation path as conductive filament in the oxide to enable subsequent bipolar / unipolar switching. For a virgin oxide, this voltage can be very high that may cause permanent breakdown of dielectric or affect endurance of the memory cell. Moreover, an extra step is needed before memory chip operation; it adds complexity to the peripheral circuit design. Therefore, it is desirable if the forming and successive set voltages are similar and low in amplitude for stable RRAM operations. HfO_x / TiO_x multilayer device has shown such lowered forming voltage and highly uniform electrical behavior, and hence, an in-depth physical analysis is carried out to probe the chemical origin of multilayer forming free RRAM device together with X. Wu *et al.* [153]. Advanced nano-scale characterization tool such as TEM along with electron energy loss

spectroscopy (EELS) is used to characterize the physical properties of the multilayer device cell. These findings may shed light on the future memory cell design for mass production of RRAM.

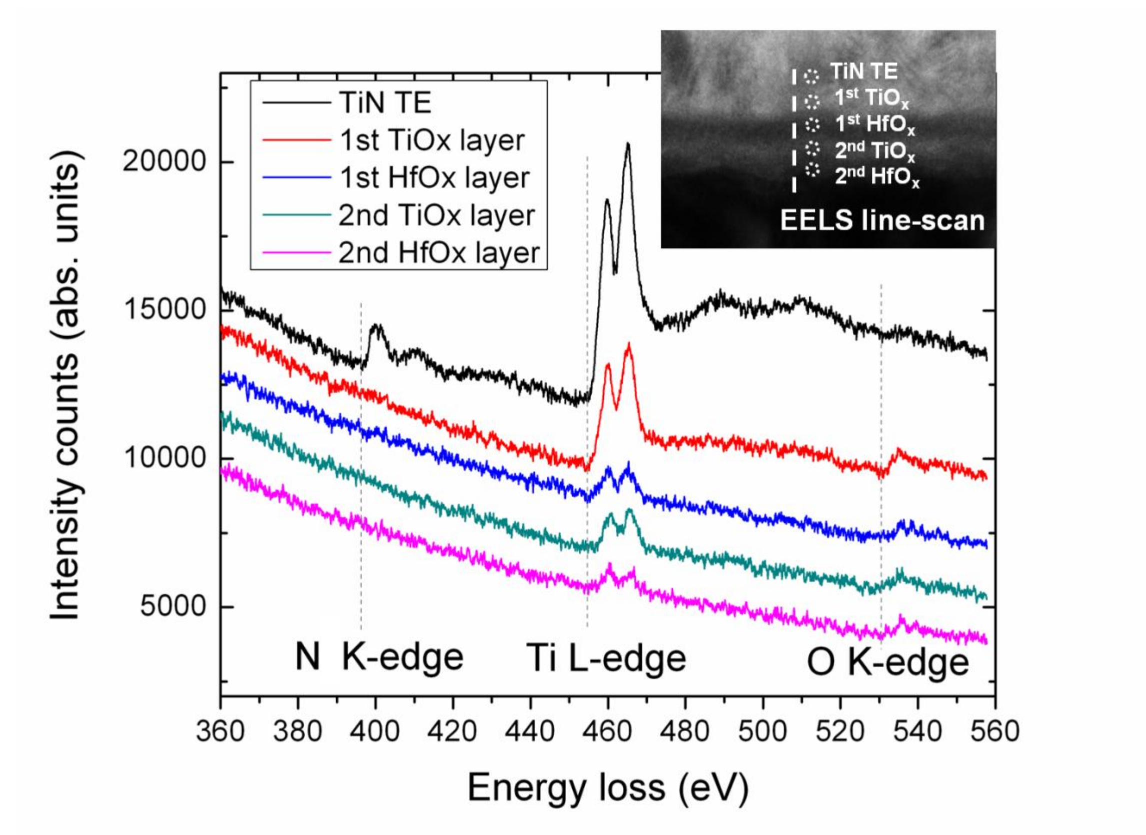


Figure 6.11 EELS results of the fresh multilayer oxides RRAM device, showing N K-edge at 401eV, Ti $L_{3,2}$-edge at 453eV, as well as O K-edge at 532eV. The sharp rise of Ti $L_{3,2}$ edge can been seen in every oxide layer, indicating Ti diffused into both HfO_x layers. The point to point distance is 3.0 Å in the EELS line scan. N K-edge can be clearly observed in the TiN top electrode layer, while no signal in the multiple oxide layers. Oxygen atoms counts clearly show up in every oxide layer, while zero count in the TiN top electrode layer. [153]

To investigate the elemental distribution information in the multilayer RRAM device, EELS measurements are performed using an FEI Titan TEM, operated at 300 kV in scanning TEM (STEM) mode. The STEM probe size is set to be approximately 1.3 Å in diameter, and the point-to-point distance is 3.0 Å in the line scan. Figure 6.11 shows the EELS results of the N K-edge, Ti $L_{3,2}$-edge, as well as the O K-edge on a fresh multilayer RRAM device. The N K-edge can be clearly observed in the TiN TE layer, while no such signal exists in the multiple oxide layers. Oxygen signal clearly shows up in every oxide layer, while zero O-count exists in the TiN TE layer. The key observation is that a sharp rise in the Ti $L_{3,2}$-edge is seen in every oxide layer, indicating that the Ti ions actually diffused / migrated into both the HfO_x layers. It has been reported that implanted Ti ions can improve resistive switching properties in ZrO_2-based RRAM device [154]. TiO_x layer in this study may produce similar effects by aforementioned doping and oxygen attraction.

Figure 6.12 illustrates the energy-loss near-edge structure (ELNES) at the TiN TE layer, the first TiO_x / HfO_x layer, and the second TiO_x / HfO_x layer, for the same region shown previously in Figure 6.11. Note that the ELNES is commonly used to elucidate the bonding and localized electronic structure; in this approach, the detailed shape of the EELS edge is studied, as it is a function of the local density of electron states [155-157]. In general, the $L_{3,2}$ edges of the 3d transition metal contains information about the valence state, coordination and site symmetry of the central atom. The L_3 edge originates from electron transitions from the inner $2p_{3/2}$ orbitals to empty 3d orbitals of the metal and the L_2 edge originates from $2p_{1/2} \rightarrow 3d$ electron transitions. The relative intensity and energy position of these L_3 and L_2 lines are strongly dependent on the d-band occupancy

and therefore on the valence state of the transition element [155-156]. In the case of Ti compounds, the near-edge structures found in the $L_{3,2}$ edges mainly reflect the covalent bonding states resulting from direct and/or indirect interactions between Ti and surrounding atoms. It will be shown here how the chemical bonding and site symmetry of the Ti and O and the valence state of titanium influence the shape of the Ti $L_{3,2}$.

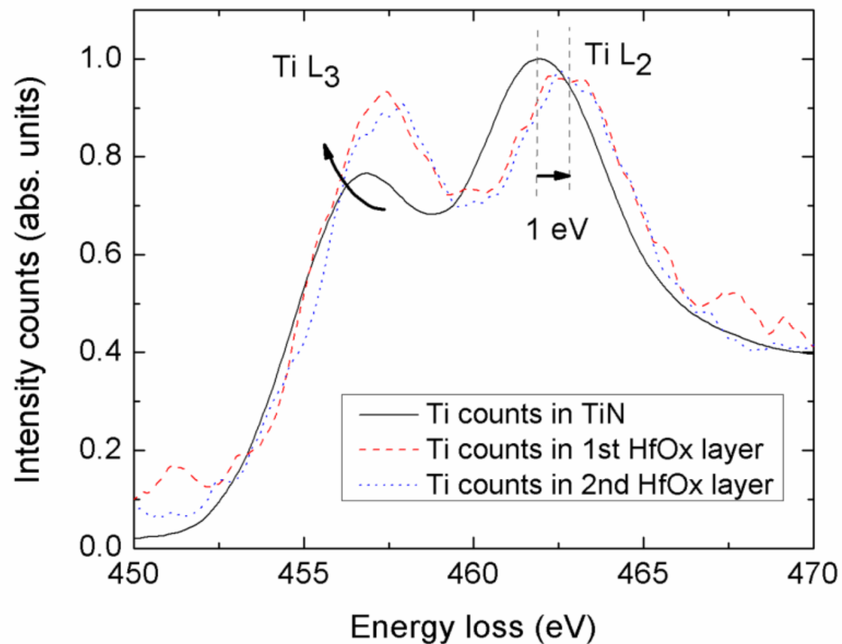


Figure 6.12 Energy-loss near-edge structure (ELNES) of the TiN top electrode, first HfO_x layer, and second HfO_x layer shown in Figure 6.11, respectively. The different Ti states are labeled. The peak shifts towards a lower energy which indicates a change of the Ti ionic state. Ti in both HfO_x layers show the same onset slope shift which is ~ 1eV. [153]

In this figure, for the TiN TE in all the measured samples, the Ti L_3-edge onset is at 453eV. In both HfO_x layers, a shift of the L_2 line to higher energy by 1.0eV is clearly visible for the EELS spectra taken from the particle edge with also an increase in L3 line

intensity. Based on these findings, Ti in the HfO_x has a higher valence state than Ti in the TiN gate. It also reveals an increase from Ti^{4+} to Ti^{3+}. Ti atoms here attract electrons rather than losing electrons. When an oxygen vacancy is formed, it is electron depleted and can easily trap electrons [16]. Hence, Ti prefers to diffuse into oxygen vacancy rather than hafnium vacancy. This Ti-guided conductive filament growth along oxygen vacancy reduces the randomness of the filament formation and rupture process, leading to improvement of stability and uniformity of RRAM device [153].

6.5 Summary

In this chapter, forming free RRAM cells with $HfO_x/TiO_x/HfO_x/TiO_x$ multilayer structure is demonstrated. The resistive switching uniformity is significantly improved (both cycle-to-cycle uniformity in one device and device-to-device uniformity). Compact set / reset voltage distribution, reduced reset current as well as tight HRS resistance distribution in 500 cycles for a single device and 100 cycles for ten devices is achieved.

Physical analysis using TEM-EELS has been carried out on such device, it suggests that Ti diffusion into HfO_x is the chemical origin for the observed forming free behavior. And a combination of Ti-guided filament formation in HfO_x and confinement of filament between layers is attributed to the suppression of parameter dispersion.

Chapter 7 Conclusion and Recommendations

7.1 Conclusion

High performance RRAM device has been demonstrated in this work with binary transition metal oxide as switching layer. The resistive switching mechanism can be described in terms of formation and rupture of oxygen vacancies related conductive filament. Temperature effect on switching is studies, with elevated temperature, set and reset voltages decreases due to higher oxygen ion mobility and lowered defects formation energy barrier. More than that, trap-assist tunneling current increases at high temperature, which results in a smaller memory window due to higher leakage current of HRS. In terms of retention, temperature plays a more critical role than voltage bias from biased temperature instability test. By proper control operation conditions, multi-level resistance switching can be achieved to enable multi-bit storage in a cell. However, it is worth noting that at high temperature, this might be affected due to higher leakage at HRS.

To get a clear picture of current conduction mechanism in different states, which is important to understand the oxide-based RRAM switching properties and power consumption, both DC and low frequency noise analysis is implemented. It is confirmed that for low resistance state, current conduction is localized without area dependence, whereas, for fully recovered high resistance state, uniform leakage current scales with device area. The current conduction in the cell could be treated as two parallel resistances

of conduction filament and uniform leakage oxide. In the low resistance regime, filament resistance dominates current conduction as well as LFN behavior, which varies to the power of filament resistance. While in the high resistance regime, uniform oxide dominates, which results in a roughly constant noise level. Based on this, a noise model is propose for this type of switching cell, and the prediction curve fits experimental data quite well. Further, a filament conduction noise model has proposed for LRS, allowing estimation of filament carrier concentration found in the metallic range.

Based on the understanding of switching mechanism and current conduction, device with multilayer structure is used to tackle the uniformity issue faced in RRAM device operation. Compared to single layer control device, resistive switching uniformity has been significantly improved in HfO_x / TiO_x / HfO_x / TiO_x multilayer structure for both cycle-to-cycle uniformity in one device and device-to-device. Compact set / reset voltage distribution, reduced reset current as well as tight HRS resistance distribution in 500 cycles for a single device and 100 cycles in ten devices are achieved. Further to that, fresh resistance in such multilayer device is dragged down to the level of HRS during switching, and forming voltage is similar to that of set, in another way of saying these devices are forming free. Physical analysis using TEM-EELS is carried out to probe the chemical origin of multilayer forming free device. It is suggest that doping effect of Ti diffused in HfO_x and confinement of filament between multilayer oxides leads to the improvement in stability and uniformity of multilayer device.

7.2 Recommendations and Future Work

In spite of the research work presented here, there are still many open questions about the resistive switching behavior in HfO_x or oxide-based RRAM device.

From the theoretical point of view, the actual switching mechanism is still not fully understood. As mentioned in this thesis, oxygen vacancies play an important role in the filament switching; local redox reaction is involved during resistance change. The detailed chemical process should be clarified for further study. The physical properties of HfO_x as the main switching layer are also important. For example, the oxygen diffusivity, the electron mobility, etc., should be evaluated to describe the resistive switching precisely and thereafter to build proper model that can serve as guidance for memory construction.

The nature of conduction paths in HfO_x should be clarified for better understanding of current conduction in oxide-based RRAM. There are two possible approaches. One way is to fabricate device with ultra small dimensions down to a few tens to a few nanometers range. With in-situ TEM biasing, it may reveal the microscopic structure change when resistive switching happens. Together with EELS analysis on different states during TEM observation, it may provide detailed chemical information to facilitate understanding of resistance switching process. Another approach is by utilizing X-ray photoelectron spectroscopy or Raman spectroscopy with very small incident beam diameter. Due to the interference by the signals from surrounding oxide, conventional spectroscopy is difficult

to obtain the information of the localized conduction filament. Nanometer-resolution spectroscopy could be helpful to probe directly to the conduction paths to shed light on the electronic structure.

Besides memory cell study, to aim at ultra-high density nonvolatile memory applications, several other issues need to be considered. Topics like but not limited to selection device, stackable integration scheme, reliable electrode contact, etc., would all be research areas for oxide-based RRAM.

Bibliography

[1] G. Moore, "Progress in digital integrated electronics," in *Technical Digest - International Electron Devices Meeting, IEDM*, 1975, p. 11.

[2] *Dynamic random-access memory*. Available: http://en.wikipedia.org/wiki/DRAM

[3] "ITRS 2006 Update," in *International Technology Roadmap for Semiconductors*, 2006.

[4] C. Y. Lu, K. Y. Hsieh, and R. Liu, "Future challenges of flash memory technologies," *Microelectronic Engineering,* vol. 86, pp. 283-286, 2009.

[5] A. L. Lacaita and D. J.Wouters. "Phase-Change Memories", *physica status solidi (a),* vol. 205, pp. 2281-2297, 2008.

[6] H. Yu, Y. Sun, N. Singh, G. Q. Lo, and D. L. Kwong, "Perspective of flash memory realized on vertical Si nanowires," *Microelectronics Reliability,* vol. 52, pp. 651-661, 2012.

[7] K. Tsunoda, K. Kinoshita, H. Noshiro, Y. Yamazaki, T. Iizuka, Y. Ito, A. Takahashi, A. Okano, Y. Sato, T. Fukano, M. Aoki, and Y. Sugiyama, "Low power and high speed switching of Ti-doped NiO ReRAM under the unipolar voltage source of less than 3 V," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2007, pp. 767-770.

[8] H. Y. Lee, P. S. Chen, T. Y. Wu, Y. S. Chen, C. C. Wang, P. J. Tzeng, C. H. Lin, F. Chen, C. H. Lien, and M. J. Tsai, "Low power and high speed bipolar switching with a thin reactive ti buffer layer in robust HfO_2 based RRAM," in

Technical Digest - International Electron Devices Meeting, IEDM, 2008, pp. 297-300.

[9] I. G. Baek, D. C. Kim, M. J. Lee, H. J. Kim, E. K. Yim, M. S. Lee, J. E. Lee, S. E. Ahn, S. Seo, J. H. Lee, J. C. Park, Y. K. Cha, S. O. Park, H. S. Kim, I. K. Yoo, U. I. Chung, J. T. Moon, and B. I. Ryu, "Multi-layer cross-point binary oxide resistive memory (OxRRAM) for post-NAND storage application," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2005, pp. 750-753.

[10] T. W. Hickmott, "Low-frequency negative resistance in thin anodic oxide films," *Journal of Applied Physics,* vol. 33, pp. 2669-2682, 1962.

[11] A. Beck, J. G. Bednorz, C. Gerber, C. Rossel, and D. Widmer, "Reproducible switching effect in thin oxide films for memory applications," *Applied Physics Letters,* vol. 77, pp. 139-141, 2000.

[12] I. G. Baek, M. S. Lee, S. Seo, M. J. Lee, D. H. Seo, D. S. Suh, J. C. Park, S. O. Park, H. S. Kim, I. K. Yoo, U. I. Chung, and J. T. Moon, "Highly scalable nonvolatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulses," in *Electron Devices Meeting, 2004. IEDM Technical Digest. IEEE International*, 2004, pp. 587-590.

[13] B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg, and S. Tiedke, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition," *Journal of Applied Physics,* vol. 98, pp. 033715-10, 2005.

[14] H. Sim, H. Choi, D. Lee, M. Chang, D. Choi, Y. Son, E. H. Lee, W. Kim, Y. Park, I. K. Yoo, and H. Hwang, "Excellent resistance switching characteristics of

Pt/$SrTiO_3$ schottky junction for multi-bit nonvolatile memory application," 2005, pp. 758-761.

[15] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature Materials,* vol. 6, pp. 833-840, 2007.

[16] N. Xu, B. Gao, L. F. Liu, B. Sun, X. Y. Liu, R. Q. Han, J. F. Kang, and B. Yu, "A unified physical model of switching behavior in oxide-based RRAM," in *Digest of Technical Papers - Symposium on VLSI Technology*, 2008, pp. 100-101.

[17] K. Kahng and S. M. Sze, "A floating gate and its application to memory devices," *Electron Devices, IEEE Transactions on,* vol. 14, pp. 629-629, 1967.

[18] *Flash memory*. Available: http://en.wikipedia.org/wiki/Flash_memory

[19] H. Kurata, K. Otsuga, A. Kotabe, S. Kajiyama, T. Osabe, Y. Sasago, S. Narumi, K. Tokami, S. Kamohara, and O. Tsuchiya, "The impact of random telegraph signals on the scaling of multilevel flash memories," in *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, 2006, pp. 112-113.

[20] Y. Shin, "Non-volatile memory technologies for beyond 2010," in *Symposium on VLSI Circuits*, 2005, pp. 156-159.

[21] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Physical Review Letters,* vol. 21, pp. 1450-1453, 1968.

[22] J. H. Yi, Y. H. Ha, J. H. Park, B. J. Kuh, H. Horii, Y. T. Kim, S. O. Park, Y. N. Hwang, S. H. Lee, S. J. Ahn, S. Y. Lee, J. S. Hong, K. H. Lee, N. I. Lee, H. K. Kang, U. I. Chung, and J. T. Moon, "Novel Cell Structure of PRAM with thin metal layer inserted GeSbTe," in *Technical Digest - International Electron Devices Meeting*, 2003, pp. 901-904.

[23] Y. Ling, Y. Lin, L. Lai, B. Iao, Y. Lai, J. Feng, T. A. Tang, B. Cai, and B. Chen, "A novel edge contact type cell for phase change RAM using N-doped GeSbTe films," in *International Conference on Solid-State and Integrated Circuits Technology Proceedings (ICSICT)* 2004, pp. 707-710.

[24] A. V. Kolobov, P. Fons, J. Tominaga, A. I. Frenkel, A. L. Ankuoinov, S. N. Yannopoulos, K. S. Andrikopoulos, and T. Uruga, "Why phase-change media are fast and stable: A new approach to an old problem," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* vol. 44, pp. 3345-3349, 2005.

[25] S. Lee, Y. J. Song, Y. N. Hwang, S. H. Lee, J. H. Park, K. C. Ryoo, S. J. Ahn, C. W. Jeong, J. H. Oh, J. M. Shin, F. Yeung, W. C. Jeong, Y. T. Kim, J. B. Park, K. H. Koh, G. T. Jeong, H. S. Jeong, and K. Kim, "Effect of the Bottom Electrode Contact (BEC) on the phase transformation of N_2 doped $Ge_2Sb_2Te_5$ (N-GST) in a Phase-change Random Access Memory," 2005, pp. 373-378.

[26] D. Wright, M.M.Aziz, M.Armand, S.Senkander, and W.Yu, "Can we reach Tbit/sq.in. storage densities with Phase-Change media ?," in *European Phase Change Ovonic Science symposium*, 2004.

[27] D. H. Kang, D. H. Ahn, M. H. Kwon, H. S. Kwon, K. B. Kim, K. S. Lee, and B. K. Cheong, "Lower voltage operation of a phase change memory device with a highly resistive TiON layer," *Japanese Journal of Applied Physics, Part 1: Regular Papers and Short Notes and Review Papers,* vol. 43, pp. 5243-5244, 2004.

[28] A. L. Lacaita and D. J. Wouters, "Phase-change memories," *physica status solidi (a),* vol. 205, pp. 2281-2297, 2008.

[29] *Magnetoresistive Random Access Memory*. Available: http://en.wikipedia.org/wiki/Magnetoresistive_Random_Access_Memory

[30] "Emerging Research Devices," in *International Technology Roadmap for Semiconductors*, 2007.

[31] W. J. Gallagher, D. Abraham, S. Assefa, S. L. Brown, J. DeBrosse, M. Gaidis, E. Galligan, E. Gow, B. Hughes, J. Hummel, S. Kanakasabapathy, C. Kaiser, M. Lamorey, T. Maffit, K. Milkove, L. Yu, J. Nowak, P. Rice, M. Samant, E. O'Sullivan, S. S. P. Parkin, R. Robertazzi, P. Trouilloud, D. Worledge, G. Wright, and Y. See-Hun, "Recent advances in MRAM technology," in *VLSI Technology, 2005. (VLSI-TSA-Tech). 2005 IEEE VLSI-TSA International Symposium on*, 2005, pp. 72-73.

[32] W. Zhao, S. Chaudhuri, C. Accoto, J.-O. Klein, D. Ravelosona, C. Chappert, and P. Mazoyer, "High Density Spin-Transfer Torque (STT)-MRAM Based on Cross-Point Architecture," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1-4.

[33] S. T. Hsu and W.-W. Zhuang, "Electrically programmable resistance cross point memory structure," 2003.

[34] M.-S. Lee and I.-G. Baek, "Methods of programming non-volatile memory devices including transition metal oxide layer as data storage material layer and devices so operated," 2006.

[35] H. L. Lung, "High density chalcogenide memory cells," U.S. Patent 7067865, 2006.

[36] K. A. Campbell, J. T. Moore, and T. L. Gilton, "Single-polarity programmable resistance-variable memory element," U.S. Patent 6867996, 2005.

[37] J. G. Simmons and R. R. Verderber, "New conduction and reversible memory phenomena in thin insulating films," *Proc. R. Soc. London, Ser. A,* vol. 301, pp. 77-102, 1967.

[38] J. F. Gibbons and W. E. Beadle, "Switching properties of thin Nio films," *Solid State Electronics,* vol. 7, pp. 785-790, 1964.

[39] A. Asamitsu, Y. Tomioka, H. Kuwahara, and Y. Tokura, "Current switching of resistive states in magnetoresistive manganites," *Nature,* vol. 388, pp. 50-52, 1997.

[40] M. N. Kozicki, M. Yun, L. Hilt, and A. Singh, "Applications of programmable resistance changes in metal-doped chalcogenides," *Pennington NJ USA: Electrochem. Soc,* vol. 298-309, 1999.

[41] M. J. Lee, C. B. Lee, S. Kim, H. Yin, J. Park, S. E. Ahn, B. S. Kang, K. H. Kim, G. Stefanovich, I. Song, S. W. Kim, J. H. Lee, S. J. Chung, Y. H. Kim, C. S. Lee, J. B. Park, I. G. Baek, C. J. Kim, and Y. Park, "Stack friendly all-oxide 3D RRAM using GaInZnO peripheral TFT realized over glass substrates," in *Electron Devices Meeting, 2008. IEDM 2008. IEEE International*, 2008, pp. 1-4.

[42] J. Shin, I. Kim, K. P. Biju, M. Jo, J. Park, J. Lee, S. Jung, W. Lee, S. Kim, S. Park, and H. Hwang, "TiO_2-based metal-insulator-metal selection device for bipolar resistive random access memory cross-point application," *Journal of Applied Physics,* vol. 109, pp. 033712-033712-4, 2011.

[43] R. Waser, R. Dittmann, C. Staikov, and K. Szot, "Redox-based resistive switching memories nanoionic mechanisms, prospects, and challenges," *Advanced Materials,* vol. 21, pp. 2632-2663, 2009.

[44] D. S. Jeong, H. Schroeder, and R. Waser, "Coexistence of bipolar and unipolar resistive switching behaviors in a Pt TiO_2 Pt stack," *Electrochemical and Solid-State Letters,* vol. 10, pp. G51-G53, 2007.

[45] H. Akinaga, H. Shima, F. Takano, I. H. Inoue, and H. Takagi, "Resistive switching effect in metal/insulator/metal heterostructures and its application for non-volatile memory," *IEEJ Transactions on Electrical and Electronic Engineering,* vol. 2, pp. 453-457, 2007.

[46] E. Lörtscher, J. W. Ciszek, J. Tour, and H. Riel, "Reversible and controllable switching of a single-molecule junction," *Small,* vol. 2, pp. 973-977, 2006.

[47] E. Y. Tsymbal and H. Kohlstedt, "Tunneling across a ferroelectric," *Science,* vol. 313, pp. 181-183, 2006.

[48] D. C. Kim, S. Seo, S. E. Ahn, D. S. Suh, M. J. Lee, B. H. Park, I. K. Yoo, I. G. Baek, H. J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U. I. Chung, J. T. Moon, and B. I. Ryu, "Electrical observations of filamentary conductions for the resistive memory switching in NiO films," *Applied Physics Letters,* vol. 88, 2006.

[49] S. I. Kim, J. H. Lee, Y. W. Chang, S. S. Hwang, and K. H. Yoo, "Reversible resistive switching behaviors in NiO nanowires," *Applied Physics Letters,* vol. 93, 2008.

[50] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, S. Spiga, C. Wiemer, M. Perego, and M. Fanciulli, "Conductive-filament switching analysis and self-accelerated

thermal dissolution model for reset in NiO-based RRAM," in *Technical Digest - International Electron Devices Meeting, IEDM* 2007, pp. 775-778.

[51] J. B. Yun, S. Kim, S. Seo, M. J. Lee, D. C. Kim, S. E. Ahn, Y. Park, J. Kim, and H. Shin, *Phys Status Solidi (RRL),* vol. 7, p. 280, 2007.

[52] J. J. O'Dwyer, *The Theory of Electrical Conduction and Breakdown in Solid Dielectrics,* 1973.

[53] D.-H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X.-S. Li, G.-S. Park, B. Lee, S. Han, M. Kim, and C. S. Hwang, "Atomic structure of conducting nanofilaments in TiO_2 resistive switching memory," *Nat Nano,* vol. 5, pp. 148-153, 2010.

[54] G. S. Park, X. S. Li, D. C. Kim, R. J. Jung, M. J. Lee, and S. Seo, "Observation of electric-field induced Ni filament channels in polycrystalline NiO_x film," *Applied Physics Letters,* vol. 91, 2007.

[55] K. Fujiwara, unpublished|.

[56] C. Schindler, M. Meier, R. Waser, and M. N. Kozicki, "Resistive switching in Ag-Ge-Se with extremely low write currents," in *Proceedings Non-Volatile Memory Technology Symposium, NVMTS*, 2007, pp. 82-85.

[57] Y. Hirose and H. Hirose, "Polarity-dependent memory switching and behavior of Ag dendrite in Ag-photodoped amorphous As_2S_3 films," *Journal of Applied Physics,* vol. 47, pp. 2767-2772, 1976.

[58] K. Terabe, T. Hasegawa, T. Nakayama, and M. Aono, "Quantized conductance atomic switch," *Nature,* vol. 433, pp. 47-50, 2005.

[59] T. Sakamoto, H. Sunamura, H. Kawaura, T. Hasegawa, T. Nakayama, and M. Aonob, "Nanometer-scale switches using copper sulfide," *Applied Physics Letters,* vol. 82, pp. 3032-3034, 2003.

[60] W. R. Hiatt and T. W. Hickmott, "Bistable switching in niobium oxide diodes," *Applied Physics Letters,* vol. 6, pp. 106-108, 1965.

[61] Z. Li, M. D. Pickett, D. Stewart, D. A. A. Ohlberg, X. Li, W. Wu, W. Robinett, and R. S. Williams, "Experimental demonstration of a defect-tolerant nanocrossbar demultiplexer," *Nanotechnology,* vol. 19, 2008.

[62] A. Sawa, "Resistive switching in transition metal oxides," *Materials Today,* vol. 11, pp. 28-36, 2008.

[63] R. Meyer, L. Schloss, J. Brewer, R. Lambertson, W. Kinney, J. Sanchez, and D. Rinerson, "Oxide dual-layer memory element for scalable non-volatile cross-point memory technology," in *Proceedings - 2008 9th Annual Non-Volatile Memory Technology Symposium, NVMTS 2008*, 2008.

[64] A. Ignatiev, N. J. Wu, X. Chen, S. Q. Liu, C. Papagianni, and J. Strozier, "Resistance switching in perovskite thin films," *Physica Status Solidi (B) Basic Research,* vol. 243, pp. 2089-2097, 2006.

[65] R. Muenstermann, R. Dittmann, K. Szot, S. Mi, C. L. Jia, P. Meuffels, and R. Waser, "Realization of regular arrays of nanoscale resistive switching blocks in thin films of Nb-doped $SrTiO_3$," *Applied Physics Letters,* vol. 93, 2008.

[66] Y. Nishi, "Challenges and opportunities for future non-volatile memory technology," *Current Applied Physics,* vol. 11, pp. e101-e103, 2011.

[67] Y. Y. Chen, G. Pourtois, X. P. Wang, C. Adelmann, L. Goux, B. Govoreanu, L. Pantisano, S. Kubicek, L. Altimime, M. Jurczak, J. A. Kittl, G. Groeseneken, and D. J. Wouters, "Switching by Ni Filaments in a HfO_2 Matrix: A New Pathway to Improved Unipolar Switching RRAM," in *Proc. IEEE Int. Memory Workshop*, 2011, pp. 1-4.

[68] T.-H. Hou, K.-L. Lin, J. Shieh, J.-H. Lin, C.-T. Chou, and Y.-J. Lee, "Evolution of RESET current and filament morphology in low-power HfO_2 unipolar resistive switching memory," *Applied Physics Letters,* vol. 98, p. 103511, 2011.

[69] Z. Fang, H. Y. Yu, X. Li, N. Singh, G. Q. Lo, and D. L. Kwong, "$HfO_x/TiO_x/HfO_x/TiO_x$ Multilayer-Based Forming-Free RRAM Devices With Excellent Uniformity," *Electron Device Letters, IEEE,* vol. 32, pp. 566-568, 2011.

[70] D. Lee, J. Lee, M. Jo, J. Park, M. Siddik, and H. Hwang, "Noise-Analysis-Based Model of Filamentary Switching ReRAM With ZrO_x/HfO_x Stacks," *Electron Device Letters, IEEE,* vol. 32, pp. 964-966, 2011.

[71] N. Raghavan, W. Liu, X. Li, X. Wu, M. Bosman, and K. L. Pey, "Filamentation Mechanism of Resistive Switching in Fully Silicided High-κ Gate Stacks," *Electron Device Letters, IEEE,* vol. 32, pp. 455-457, 2011.

[72] X. A. Tran, B. Gao, J. F. Kang, X. Wu, L. Wu, Z. Fang, Z. R. Wang, K. L. Pey, Y. C. Yeo, A. Y. Du, M. Liu, B. Y. Nguyen, M. F. Li, and H. Y. Yu, "Self-rectifying and forming-free unipolar HfO_x based-high performance RRAM built by fab-avaialbe materials," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 31.2.1-31.2.4.

[73] K. Jung, Y. Kim, Y. S. Park, W. Jung, J. Choi, B. Park, H. Kim, W. Kim, J. Hong, and H. Im, "Unipolar resistive switching in insulating niobium oxide film and probing electroforming induced metallic components," *Journal of Applied Physics,* vol. 109, p. 054511, 2011.

[74] C. B. Lee, D. S. Lee, A. Benayad, S. R. Lee, M. Chang, M.-J. Lee, J. Hur, C. J. Kim, and U.-I. Chung, "Highly Uniform Switching of Tantalum Embedded Amorphous Oxide Using Self-Compliance Bipolar Resistive Switching," *Electron Device Letters, IEEE,* vol. 32, pp. 399-401, 2011.

[75] J.-K. Lee, J.-W. Lee, J. Park, S.-W. Chung, J. S. Roh, S.-J. Hong, I.-w. Cho, H.-I. Kwon, and J.-H. Lee, "Extraction of trap location and energy from random telegraph noise in amorphous TiO_x resistance random access memories," *Applied Physics Letters,* vol. 98, p. 143502, 2011.

[76] Y.-S. Chen, H.-Y. Lee, P.-S. Chen, P.-Y. Gu, W.-H. Liu, W.-S. Chen, Y.-Y. Hsu, C.-H. Tsai, F. Chen, M.-J. Tsai, and C. Lien, "Good Endurance and Memory Window for Ti/HfO_x Pillar RRAM at 50-nm Scale by Optimal Encapsulation Layer," *Electron Device Letters, IEEE,* vol. 32, pp. 390-392, 2011.

[77] S. Kim, K. P. Biju, M. Jo, S. Jung, J. Park, J. Lee, W. Lee, J. Shin, S. Park, and H. Hwang, "Effect of Scaling WO_x-Based RRAMs on Their Resistive Switching Characteristics," *Electron Device Letters, IEEE,* vol. 32, pp. 671-673, 2011.

[78] M.-C. Wu, Y.-W. Lin, W.-Y. Jang, C.-H. Lin, and T.-Y. Tseng, "Low-Power and Highly Reliable Multilevel Operation in ZrO_2 1T1R RRAM," *Electron Device Letters, IEEE,* vol. 32, pp. 1026-1028, 2011.

[79] C. Dumas, D. Deleruyelle, A. Demolliens, C. Muller, S. Spiga, E. Cianci, M. Fanciulli, I. Tortorelli, and R. Bez, "Resistive switching characteristics of NiO films deposited on top of W or Cu pillar bottom electrodes," *Thin Solid Films,* vol. 519, pp. 3798-3803, 2011.

[80] H. K. Yoo, S. B. Lee, J. S. Lee, S. H. Chang, M. J. Yoon, Y. S. Kim, B. S. Kang, M. J. Lee, C. J. Kim, B. Kahng, and T. W. Noh, "Conversion from unipolar to bipolar resistance switching by inserting Ta_2O_5 layer in Pt/TaO_x/Pt cells," *Applied Physics Letters,* vol. 98, p. 183507, 2011.

[81] L. F. Liu, Y. S. Chen, J. F. Kang, Y. Wang, D. D. Han, X. Y. Liu, and X. Zhang, "Unipolar resistive switching and mechanism in Gd-doped-TiO_2-based resistive switching memory devices," *Semiconductor Science and Technology,* vol. 26, p. 115009, 2011.

[82] H. K. Gun, H. L. Jong, Y. S. Jun, J. S. Seul, H. Y. Jung, J. Y. Kyung, H. L. Min, M. K. Kyung, D. L. Hyung, W. R. Seung, J. P. Tae, and S. H. Cheol, "Improved endurance of resistive switching TiO_2 thin film by hourglass shaped Magnéli filaments," *Applied Physics Letters,* vol. 98, p. 262901, 2011.

[83] M. H. Tang, Z. Q. Zeng, J. C. Li, Z. P. Wang, X. L. Xu, G. Y. Wang, L. B. Zhang, S. B. Yang, Y. G. Xiao, and B. Jiang, "Resistive switching behavior of La-doped ZnO films for nonvolatile memory applications," *Solid-State Electronics,* vol. 63, pp. 100-104, 2011.

[84] Q. Xu, Z. Wen, and D. Wu, "Bipolar and unipolar resistive switching in $Zn_{0.98}Cu_{0.02}O$ films," *Journal of Physics D: Applied Physics,* vol. 44, p. 335104, 2011.

[85] Y. Li, S. Long, H. Lv, Q. Liu, W. Wang, Q. Wang, Z. Huo, Y. Wang, S. Zhang, S. Liu, and M. Liu, "Reset Instability in Cu/ZrO_2:Cu/Pt RRAM Device," *Electron Device Letters, IEEE,* vol. 32, pp. 363-365, 2011.

[86] C. H. Ho, E. K. Lai, M. D. Lee, C. L. Pan, Y. D. Yao, K. Y. Hsieh, R. Liu, and C. Y. Lu, "A Highly Reliable Self-Aligned Graded Oxide WOx Resistance Memory: Conduction Mechanisms and Reliability," in *VLSI Technology, 2007 IEEE Symposium on*, 2007, pp. 228-229.

[87] K. C. Min, M. Kim, Y. H. You, S. S. Lee, Y. K. Lee, T. M. Chung, C. G. Kim, J. H. Hwang, K. S. An, N. S. Lee, and Y. Kim, "NiO thin films by MOCVD of $Ni(dmamb)_2$ and their resistance switching phenomena," *Surface and Coatings Technology,* vol. 201, pp. 9252-9255, 2007.

[88] H. Lina, Q. Bingjun, and L. Litian, "Bistable resistive switching of pulsed laser deposited polycrystalline $La_{0.67}Sr_{0.33}MnO_3$ films," in *Solid-State and Integrated-Circuit Technology, 2008. ICSICT 2008. 9th International Conference on*, 2008, pp. 936-939.

[89] T. Zhang, Z. Su, H. Chen, L. Ding, and W. Zhang, "Resistance switching properties of sol-gel derived $La_{0.67}Ca_{0.33}MnO_3$ thin films on F-doped SnO_2 conducting glass," *Applied Physics Letters,* vol. 93, pp. 172104-3, 2008.

[90] N. Gergel-Hackett, B. Hamadani, B. Dunlap, J. Suehle, C. Richter, C. Hacker, and D. Gundlach, "A Flexible Solution-Processed Memristor," *Electron Device Letters, IEEE,* vol. 30, pp. 706-708, 2009.

[91] K. Oka, T. Yanagida, K. Nagashima, H. Tanaka, and T. Kawai, "Nonvolatile bipolar resistive memory switching in single crystalline nio heterostructured

nanowires," *Journal of the American Chemical Society,* vol. 131, pp. 3434-3435, 2009.

[92] W. Y. Chang, C. A. Lin, J. H. He, and T. B. Wu, "Resistive switching behaviors of ZnO nanorod layers," *Applied Physics Letters,* vol. 96, 2010.

[93] J. W. Seo, J.-W. Park, K. S. Lim, J.-H. Yang, and S. J. Kang, "Transparent resistive random access memory and its characteristics for nonvolatile resistive switching," *Applied Physics Letters,* vol. 93, pp. 223505-3, 2008.

[94] S. Kim and Y.-K. Choi, "Resistive switching of aluminum oxide for flexible memory," *Applied Physics Letters,* vol. 92, pp. 223508-3, 2008.

[95] *Ellipsometry*. Available: http://en.wikipedia.org/wiki/Ellipsometry

[96] *Profilometer*. Available: http://en.wikipedia.org/wiki/Profilometer

[97] *Transmission electron microscopy*. Available: http://en.wikipedia.org/wiki/Transmission_electron_microscopy

[98] *Atomic force microscopy*. Available: http://en.wikipedia.org/wiki/Atomic_force_microscope

[99] *Energy-dispersive X-ray spectroscopy*. Available: http://en.wikipedia.org/wiki/Energy-dispersive_X-ray_spectroscopy

[100] *X-ray photoelectron spectroscopy*. Available: http://en.wikipedia.org/wiki/X-ray_photoelectron_spectroscopy

[101] K. Kinoshita, K. Tsunoda, Y. Sato, H. Noshiro, S. Yagaki, M. Aoki, and Y. Sugiyama, "Reduction in the reset current in a resistive random access memory consisting of NiO_x brought about by reducing a parasitic capacitance," *Applied Physics Letters,* vol. 93, pp. 033506-3, 2008.

[102] C. Nauenheim, C. Kuegeler, A. Ruediger, and R. Waser, "Investigation of the electroforming process in resistively switching TiO_2 nanocrosspoint junctions," *Applied Physics Letters,* vol. 96, pp. 122902-3, 2010.

[103] B. Chen, B. Gao, S. W. Sheng, L. F. Liu, X. Y. Liu, Y. S. Chen, Y. Wang, R. Q. Han, B. Yu, and J. F. Kang, "A Novel Operation Scheme for Oxide-Based Resistive-Switching Memory Devices to Achieve Controlled Switching Behaviors," *Electron Device Letters, IEEE,* vol. 32, pp. 282-284, 2011.

[104] W. Lian, H. Lv, Q. Liu, S. Long, W. Wang, Y. Wang, Y. Li, S. Zhang, Y. Dai, J. Chen, and M. Liu, "Improved resistive switching uniformity in Cu/HfO_2/Pt devices by using current sweeping mode," *IEEE Electron Device Letters,* vol. 32, pp. 1053-1055, 2011.

[105] Y. Hosoi, Y. Tamai, T. Ohnishi, K. Ishihara, T. Shibuya, Y. Inoue, S. Yamazaki, T. Nakano, S. Ohnishi, N. Awaya, H. Inoue, H. Shima, H. Akinaga, H. Takagi, H. Akoh, and Y. Tokura, "High Speed Unipolar Switching Resistance RAM (RRAM) Technology," in *Electron Devices Meeting, 2006. IEDM '06. International*, 2006, pp. 1-4.

[106] H. J. Wan, P. Zhou, L. Ye, Y. Y. Lin, T. A. Tang, H. M. Wu, and M. H. Chi, "In Situ Observation of Compliance-Current Overshoot and Its Effect on Resistive Switching," *Electron Device Letters, IEEE,* vol. 31, pp. 246-248, 2010.

[107] G. Ghibaudo and T. Boutchacha, "Electrical noise and RTS fluctuations in advanced CMOS devices," *Microelectronics Reliability,* vol. 42, pp. 573-582, 2002.

[108] "3PNMS is fabricated at Grenoble by Synergie-Concept Groups, 38240 Meylan, France."

[109] A. Szewczyk, L. Spiralski, G. Ghibaudo, G. Reimbold, and J. A. Chroboczek, "Programmable system for low frequency noise measurements in microelectronics devices contacted by point probes," presented at the the XVII IMEKO World Congress, Dubrovnik/Croatia, 2003.

[110] H. B. Lv, M. Yin, X. F. Fu, Y. L. Song, L. Tang, P. Zhou, C. H. Zhao, T. A. Tang, B. A. Chen, and Y. Y. Lin, "Resistive Memory Switching of CuO Films for a Nonvolatile Memory Application," *Electron Device Letters, IEEE,* vol. 29, pp. 309-311, 2008.

[111] H. Zhang, B. Gao, B. Sun, G. Chen, L. Zeng, L. Liu, X. Liu, J. Lu, R. Han, J. Kang, and B. Yu, "Ionic doping effect in ZrO_2 resistive switching memory," *Applied Physics Letters,* vol. 96, p. 123502, 2010.

[112] Z. B. Yan, S. Z. Li, K. F. Wang, and J. M. Liu, "Unipolar resistive switching effect in $YMn_{1-\delta}O_3$ thin films," *Applied Physics Letters,* vol. 96, 2010.

[113] D. Ielmini, "Modeling the Universal Set/Reset Characteristics of Bipolar RRAM by Field- and Temperature-Driven Filament Growth," *Electron Devices, IEEE Transactions on,* vol. 58, pp. 4309-4317, 2011.

[114] S. Larentis, F. Nardi, S. Balatti, D. Ielmini, and D. C. Gilmer, "Bipolar-Switching Model of RRAM by Field- and Temperature-Activated Ion Migration," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1-4.

[115] Z. Fang, H. Y. Yu, W. J. Liu, Z. R. Wang, X. A. Tran, B. Gao, and J. F. Kang, "Temperature instability of resistive switching on HfO_x-based RRAM devices," *IEEE Electron Device Letters,* vol. 31, pp. 476-478, 2010.

[116] C. Kittel, "Introduction to Solid State Physics," 8th ed, 2005, pp. 585-591.

[117] D. Ielmini, "Filamentary-switching model in RRAM for time, energy and scaling projections," in *Electron Devices Meeting (IEDM), 2011 IEEE International*, 2011, pp. 17.2.1-17.2.4.

[118] U. Russo, D. Ielmini, C. Cagli, A. L. Lacaita, S. Spiga, C. Wiemer, M. Perego, and M. Fanciulli, "Conductive-filament switching analysis and self-accelerated thermal dissolution model for reset in NiO-based RRAM," in *Electron Devices Meeting, 2007. IEDM 2007. IEEE International*, 2007, pp. 775-778.

[119] B. Gao, J. F. Kang, H. W. Zhang, B. Sun, B. Chen, L. F. Liu, X. Y. Liu, R. Q. Han, Y. Y. Wang, B. Yu, Z. Fang, H. Y. Yu, and D. L. Kwong, "Oxide-based RRAM: Physical based retention projection," in *Solid-State Device Research Conference (ESSDERC), 2010 Proceedings of the European*, 2010, pp. 392-395.

[120] B. Gao, H. Zhang, B. Chen, L. Liu, X. Liu, R. Han, J. Kang, Z. Fang, H. Yu, B. Yu, and D.-L. Kwong, "Modeling of Retention Failure Behavior in Bipolar Oxide-Based Resistive Switching Memory," *Electron Device Letters, IEEE,* vol. 32, pp. 276-278, 2011.

[121] D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, "Trade-off between data retention and reset in NiO RRAMS," in *Reliability Physics Symposium (IRPS), 2010 IEEE International*, 2010, pp. 620-626.

[122] D. Ielmini, F. Nardi, C. Cagli, and A. L. Lacaita, "Size-Dependent Retention Time in NiO-Based Resistive-Switching Memories," *Electron Device Letters, IEEE,* vol. 31, pp. 353-355, 2010.

[123] L. Zhang, Y.-Y. Hsu, F. Chen, T. , H.-Y. Lee, Y.-S. Chen, W.-S. Chen, P.-Y. Gu, W.-H. Liu, S.-M. Wang, C.-H. Tsai, R. Huang, and M.-J. Tsai, "Experimental investigation of the reliability issue of RRAM based on high resistance state conduction," *Nanotechnology,* vol. 22, p. 254016, 2011.

[124] S. Yu, Y. Wu, Y. Chai, J. Provine, and H. S. P. Wong, "Characterization of switching parameters and multilevel capability in HfO_x/AlO_x bi-layer RRAM devices," in *VLSI Technology, Systems and Applications (VLSI-TSA), 2011 International Symposium on*, 2011, pp. 1-2.

[125] J. F. Kang, B. Gao, B. Chen, L. F. Liu, X. Y. Liu, H. Y. Yu, Z. R. Wang, and B. Yu, "Oxide-Based RRAM: A Novel Defect-Engineering-Based Implementation for Multilevel Data Storage," in *Memory Workshop (IMW), 2012 4th IEEE International*, 2012, pp. 1-4.

[126] S. C. Chae, J. S. Lee, S. Kim, S. B. Lee, S. H. Chang, C. Liu, B. Kahng, H. Shin, D. W. Kim, C. U. Jung, S. Seo, M. J. Lee, and T. W. Noh, "Random circuit breaker network model for unipolar resistance switching," *Advanced Materials,* vol. 20, pp. 1154-1159, 2008.

[127] Y. Nishi and J. Jameson, "Challenge of nanoelectronic materials and devices toward new nonvolatile memories," in *International Conference on Solid-State and Integrated Circuits Technology Proceedings, ICSICT* 2008, pp. 892-896.

[128] S. Machlup, "Noise in semiconductors: Spectrum of a two-parameter random signal," *Journal of Applied Physics,* vol. 25, pp. 341-343, 1954.

[129] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada, "Effect of bottom electrode of ReRAM with Ta_2O_5/TiO_2 stack on RTN and retention," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2009, pp. 775-778.

[130] L. Jung-Kyu, J. Hu Young, C. In-Tak, L. Jeong Yong, C. Sung-Yool, K. Hyuck-In, and L. Jong-Ho, "Conduction and Low-Frequency Noise Analysis in Al/α-TiOx/Al Bipolar Switching Resistance Random Access Memory Devices," *Electron Device Letters, IEEE,* vol. 31, pp. 603-605, 2010.

[131] S. B. Lee, S. Park, J. S. Lee, S. C. Chae, S. H. Chang, M. H. Jung, Y. Jo, B. Kahng, B. S. Kang, M. J. Lee, and T. W. Noh, "Large *1/f* noise of unipolar resistance switching and its percolating nature," *Applied Physics Letters,* vol. 95, pp. 122112-122112-3, 2009.

[132] M. Terai, Y. Sakotsubo, Y. Saito, S. Kotsuji, and H. Hada, "Memory-State Dependence of Random Telegraph Noise of Ta_2O_5/TiO_2 Stack ReRAM," *Electron Device Letters, IEEE,* vol. 31, pp. 1302-1304, 2010.

[133] D. Muñoz Ramo, A. L. Shluger, J. L. Gavartin, and G. Bersuker, "Theoretical prediction of intrinsic self-trapping of electrons and holes in monoclinic HfO_2," *Physical Review Letters,* vol. 99, 2007.

[134] F. T. Chen, H.-Y. Lee, Y.-S. Chen, P.-S. Chen, P. Gu, C.-W. Chen, Y.-Y. Hsu, W.-H. Liu, W.-S. Chen, M.-J. Tsai, S.-C. Lo, and M.-W. Lai, "Size dependence of $TiN/HfO_2/Ti$ MIM ReRAM resistance states: Model and experimental results," *Current Applied Physics,* vol. 10, pp. e75-e78, 2010.

[135] M. V. Haartman and M. Östling, *Low-frequency noise in advanced MOS devices*: Springer, 2007.

[136] A. Van Der Ziel and E. R. Chenette, "Noise in Solid State Devices," in *Advances in Electronics and Electron Physics*. vol. Volume 46, L. Marton, Ed., ed: Academic Press, 1978, pp. 313-383.

[137] P. Dutta and P. M. Horn, "Low-frequency fluctuations in solids: *1/f* noise," *Reviews of Modern Physics,* vol. 53, pp. 497-516, 1981.

[138] F. N. Hooge, T. G. M. Kleinpenning, and L. K. J. Vandamme, "Experimental studies on *1/f* noise," *Reports on Progress in Physics,* vol. 44, pp. 479-532, 1981.

[139] M. B. Weissman, "*1/f* noise and other slow, nonexponential kinetics in condensed matter," *Reviews of Modern Physics,* vol. 60, pp. 537-571, 1988.

[140] M. Surdin, "Fluctuations in the thermionic current and the 'flicker effect'," *J. Phys. Radium,* vol. 10, pp. 188-189, 1939.

[141] F. N. Hooge, "*1/f* noise sources," *Electron Devices, IEEE Transactions on,* vol. 41, pp. 1926-1935, 1994.

[142] F. N. Hooge, "*1/f* noise is no surface effect," *Physics Letters A,* vol. 29, pp. 139-140, 1969.

[143] D. Ielmini, F. Nardi, and C. Cagli, "Resistance-dependent amplitude of random telegraph-signal noise in resistive switching memories," *Applied Physics Letters,* vol. 96, 2010.

[144] J. W. Lee, D. Jang, G. T. Kim, M. Mouis, and G. Ghibaudo, "Analysis of charge sensitivity and low frequency noise limitation in silicon nanowire sensors," *Journal of Applied Physics,* vol. 107, 2010.

[145] R. Degraeve, A. Kerber, P. Roussel, E. Cartier, T. Kauerauf, L. Pantisano, and G. Groeseneken, "Effect of bulk trap density on HfO_2 reliability and yield," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2003, pp. 935-938.

[146] C. Cagli, F. Nardi, and D. Ielmini, "Modeling of Set/Reset Operations in NiO-Based Resistive-Switching Memory Devices," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 1712-1720, 2009.

[147] U. Russo, D. Ielmini, C. Cagli, and A. L. Lacaita, "Self-Accelerated Thermal Dissolution Model for Reset Programming in Unipolar Resistive-Switching Memory (RRAM) Devices," *Electron Devices, IEEE Transactions on,* vol. 56, pp. 193-200, 2009.

[148] Z. Fang, H. Y. Yu, J. A. Chroboczek, G. Ghibaudo, J. Buckley, B. De Salvo, X. Li, and D. L. Kwong, "Low-Frequency Noise in Oxide-Based TiN/HfO_x/Pt Resistive Random Access Memory Cells," *Electron Devices, IEEE Transactions on,* vol. PP, pp. 1-4, 2012.

[149] H. Y. Lee, Y. S. Chen, P. S. Chen, T. Y. Wu, F. Chen, C. C. Wang, P. J. Tzeng, M. J. Tsai, and C. Lien, "Low-power and nanosecond switching in robust hafnium oxide resistive memory with a thin Ti cap," *IEEE Electron Device Letters,* vol. 31, pp. 44-46, 2010.

[150] J. Yoon, H. Choi, D. Lee, J. B. Park, J. Lee, D. J. Seong, Y. Ju, M. Chang, S. Jung, and H. Hwang, "Excellent switching uniformity of Cu-doped MoO_x/GdO_x bilayer for nonvolatile memory applications," *IEEE Electron Device Letters,* vol. 30, pp. 457-459, 2009.

[151] B. S. Amrutur and M. Horowitz, "Techniques to reduce power in fast wide memories [CMOS SRAMs]," in *Low Power Electronics, 1994. Digest of Technical Papers., IEEE Symposium*, 1994, pp. 92-93.

[152] M. Borah, M. J. Irwin, and R. M. Owens, "Minimizing power consumption of static CMOS circuits by transistor sizing and input reordering," in *VLSI Design, 1995., Proceedings of the 8th International Conference on*, 1995, pp. 294-298.

[153] X. Wu, Z. Fang, K. Li, M. Bosman, N. Raghavan, X. Li, H. Y. Yu, N. Singh, G. Q. Lo, X. X. Zhang, and K. L. Pey, "Chemical insight into origin of forming-free resistive random-access memory devices," *Applied Physics Letters,* vol. 99, pp. 133504-133504-3, 2011.

[154] L. Qi, L. Shibing, W. Wei, Z. Qingyun, Z. Sen, C. Junning, and L. Ming, "Improvement of Resistive Switching Properties in ZrO_2-Based ReRAM With Implanted Ti Ions," *Electron Device Letters, IEEE,* vol. 30, pp. 1335-1337, 2009.

[155] L. A. Grunes, R. D. Leapman, C. N. Wilker, R. Hoffmann, and A. B. Kunz, "Oxygen K near-edge fine structure: An electron-energy-loss investigation with comparisons to new theory for selected 3d transition-metal oxides," *Physical Review B,* vol. 25, pp. 7157-7173, 1982.

[156] G. A. Botton, C. C. Appel, A. Horsewell, and W. M. Stobbs, "Quantification of the EELS near-edge structures do study Mn doping in oxides," *Journal of Microscopy,* vol. 180, pp. 211-216, 1995.

[157] R. F. Klie and N. D. Browning, "Atomic scale characterization of oxygen vacancy segregation at $SrTiO_3$ grain boundaries," *Applied Physics Letters,* vol. 77, pp. 3737-3739, 2000.

Author's Publications

Journal Publications:

1. **Z. Fang,** X. P. Wang, X. Li, Z. X. Chen, A. Kamath, G. Q. Lo and D. L. Kwong, "Fully CMOS-Compatible 1T1R Integration of Vertical Nanopillar GAA Transistor and Oxide Based RRAM Cell for High Density Nonvolatile Memory Application", *IEEE Transactions on Electron Devices,* vol 60, page 1108 - 1113, 2013.

2. **Z. Fang,** H.Y. Yu, W. J. Fan, G. Ghibaudo, J. Buckley, B. de Salvo, X. Li, X. P. Wang, G. Q. Lo, D. L. Kwong, "Current Conduction Model for Oxide-Based Resistive Random Access Memory Verified by Low Frequency Noise Analysis", *IEEE Transactions on Electron Devices,* vol 60, no 3, page 1272 - 1275, 2013.

3. **Z. Fang**, H.Y. Yu, J.A. Chroboczek, G. Ghibaudo, J. Buckley, B. de Salvo, X. Li, D.L. Kwong, "Low Frequency Noise in Oxide-Based (TiN/HfO_x/Pt) Resistive Random Access Memory Cells", *IEEE Transactions on Electron Devices,* vol 59, no 3, page 850-853, 2012.

4. **Z. Fang,** H. Y. Yu, X. Li, N. Singh, G.Q. Lo, D.L. Kwong, “$HfO_x/TiO_x/HfO_x/TiO_x$ Multilayer Based Forming Free RRAM Devices with Excellent Uniformity”, *IEEE Electron Device Letters*, vol 32, page 566-568, 2011.

5. **Z. Fang**, H.Y. Yu, W.J. Liu, Z.R. Wang, X.A. Tran, B. Gao, J.F. Kang, “Temperature Instability of Resistive Switching on HfO_x-Based RRAM Devices”, *IEEE Electron Device Letters*, vol 31, page 476-478, 2010.

Conference Publications:

1. **Z. Fang**, X. P. Wang, X. Li, Z. X. Chen, A. Kamath, G. Q. Lo and D. L. Kwong, “Fully CMOS Compatible Vertical Nanopillar Transistor Based 1T1R Integration of Resistive Random Access Memory with Excellent Switching Properties”, IEEE International Nanoelectronics Conference, Jan 2013.

2. **Z. Fang**, X. P. Wang, G. Q. Lo, D. L. Kwong, “Conduction Investigation in Oxide-based Resistive Random Access Memory with Low Frequency Noise Analysis”, Non-Volatile Memory Technology Symposium (NVMTS 2012), Nov 2012.

3. **Z. Fang**, X. Li, X. P. Wang, G. Q. Lo, "Area Dependent Low Frequency Noise in Metal Oxide Based Resistive Random Access Memory", International Conference on Information and Electronics Engineering, Oct 2012.

4. **Z Fang**, H Y Yu, X Li, N Singh, D L Kwong, "Current Conduction Mechanism Investigation in Oxide-Based RRAM Via Low Frequency Noise Analysis", International Conference of Young Research on Advanced Materials, Jul 2012.

5. **Z. Fang,** Z. R. Wang, H. Y. Yu, "Device Uniformity Improvement of Oxide-based (HfO_2) RRAM with Multilayer Switching Dielectrics", *International Conference on Nanoscience & Technology*, Sep 2011.

6. **Z. Fang**, H. Y. Yu, X. Li, N. Singh, G.Q. Lo, D.L. Kwong, "Oxide-based RRAM Device Performance Improvement by Material Optimization", *International Conference on Electrical and Communication Engineering*, Sep 2011.

7. **Z. Fang**, H. Y. Yu, X. Li, N. Singh, G.Q. Lo, D.L. Kwong, "Forming free RRAM devices with improved uniformity prepared by multilayer structure", *International Conference on Materials for Advanced Technologies,* Jun 2011.

8. **Z. Fang,** H.Y. Yu, W.J. Liu, N. Singh, Patrick G.Q. Lo, "Resistive RAM Based on HfO_x and Its Temperature Instability Study", *International Conference on Electrical and Communication Engineering*, August 2010.

9. **Z. Fang**, H.Y. Yu, W. J. Liu, K.L. Pey, X. Li, L. Wu, Z.R. Wang, Patrick G.Q. Lo, B.Gao, J. F. Kang, "Bias Temperature Instability of Binary Oxide Based (HfO_x) ReRAM", *International Reliability Physics Symposium*, May 2010.

10. **Z. Fang**, H. Y. Yu, X. Li, K. L. Pey, W. J. Liu, "High Performance HfO_x –Based Resistive RAM Devices and Its Temperature Dependent Switching", *International Symposium on Integrated Circuits,* Dec 2009.

As Contributing Author:

1. S. Yu, B. Gao, **Z. Fang**, H. Y. Yu, J. F. Kang, and H.-S. P. Wong, "A low energy oxide-based electronic synaptic device for neuromorphic visual system with tolerance to device variation", Advanced Materials, Jan 2013, doi: 10.1002/adma.201203680.

2. X. P. Wang, **Z. Fang**, X. Li, B. Chen, B. Gao, J. F. Kang, Z. X. Chen, A. Kamath, N. S. Shen, N. Singh, G. Q. Lo and D. L. Kwong, "Highly Compact 1T-1R Architecture ($4F^2$ Footprint) involving Fully CMOS Compatible Vertical GAA Nano-Pillar Transistors and Oxide-Based RRAM Cells Exhibiting Excellent NVM Properties and Ultra-Low Power Operation", *IEEE International Electron Devices Meeting (IEDM)*, Dec 2012.

3. S. Yu, B. Gao, **Z. Fang**, H. Y. Yu, J. F. Kang, and H.-S. Wong, "A Neuromorphic Visual System Using RRAM Synaptic Devices with Sub-pJ Energy and Tolerance to Variability: Experimental Characterization and Large-Scale Modeling", *IEEE International Electron Devices Meeting (IEDM)*, Dec 2012.

4. W. J. Liu, X. W. Sun, Z. R. Wang, X.A. Tran, **Z. Fang**, F. Wang, L. Wu, J. Wei, and H. L. Zhu, H. Y. Yu, "Vth shift in Single Layer Graphene field Effect Transistors

and its correlation with Raman inspection", *IEEE Transactions on Device and Materials Reliability*, vol 12, page 478-481, Jun 2012.

5. Z. R. Wang, H. Y. Yu, X. A. Tran, **Z. Fang**, J. H. Wang, and H. B. Su, “Transport properties of HfO_{2-x} based resistive-switching memories”, *Physical Review B*, vol 85, 195322, May 2012.

6. Z. R. Wang, L. Wu, **Z. Fang**, X.A. Tran, W. Liu, H.Y. Yu, “Highly uniform, self-compliance and forming free RRAM based on ALD HfO2 with Ge Doping”, *IEEE Transactions on Electron Devices,* vol 59, page 1203-1208, Apr 2012.

7. X.A. Tran, W. Zhu, B. Gao, J. F. Kang, W. J. Liu, **Z. Fang**, Z. R. Wang, B.Y. Nguyen, M.F. Li, and H.Y. Yu, “A Self-Rectifying HfO_x-Based Unipolar RRAM With NiSi Electrode”, *IEEE Electron Device Letters*, vol 33, page 585-587, Apr 2012.

8. Z. R. Wang, V. Tjoa, L. Wu, W.J. Liu, **Z. Fang**, X.A. Tran, J. Wei, W. G. Zhu and H.Y. Yu, “Mechanism of Different Switching Directions in Graphene Oxide Based RRAM”, *Journal of the Electrochemical Society*, vol 159 Issue 6 pages K177-K182, Apr 2012.

9. W. J. Liu, X. W. Sun, **Z. Fang**, Z. R. Wang, X. A. Tran, F. Wang, L.Wu, G. I. Ng, J. F. Zhang, J.Wei, H. L. Zhu, and H. Y. Yu, "Positive Bias-Induced V_{th} Instability in Graphene Field Effect Transistors", *IEEE Electron Device Letters*, vol.33, page 339-341, Mar 2012.

10. X.A. Tran, B. Gao, J.F. Kang, X. Wu, L. Wu, **Z. Fang**, Z.R. Wang, K.L. Pey, Y.C. Yeo, A.Y. Du, B.Y. Nguyen, M.F. Li, H.Y. Yu, "Self-Rectifying and Forming-Free Unipolar HfO*x* Based High Performance RRAM Built by Fab-Avaialbe Materials", *IEEE International Electron Devices Meeting (IEDM)*, Dec 2011.

11. B. Chen, Y. Lu, B. Gao, Y.H. Fu, F.F. Zhang, P. Huang, Y.S. Chen, L.F. Liu, X.Y. Liu, J.F. Kang, Y.Y. Wang, **Z. Fang**, H.Y. Yu, X. Li, N. Singh, G. Q. Lo, D. L. Kwong, "Physical Mechanisms of Endurance Degradation in TMO-RRAM", *IEEE International Electron Devices Meeting (IEDM)*, Dec 2011.

12. C. Cagli, J. Buckley, V. Jousseaume, T. Cabout, A. Salaun, H. Grampeix, J. F. Nodin,H. Feldis, A. Persico, J. Cluzel, P. Lorenzi,L. Massari,R. Rao, F. Irrera, F. Aussenac, C. Carabasse, M. Coue, P. Calka, E. Martinez, L. Perniola, P. Blaise, **Z. Fang**, H.Y. Yu, G. Ghibaudo, D. Deleruyelle, M. Bocquet, C. Müller, A. Padovani, O. Pirrotta, L. Vandelli, L. Larcher, G. Reimbold, B. de Salvo, "Experimental and Theoretical Study of Electrode Effects in HfO2 based RRAM", *IEEE International Electron Devices Meeting (IEDM)*, Dec 2011.

13. X. Wu, **Z. Fang**, K. Li, M. Bosman, X. Li, H. Y. Yu, N. Singh, G. Q. Lo, X. X. Zhang, K. L. Pey, "Chemical insight into origin of forming-free resistive random-access memory devices", *Applied Physics Letters*, vol **99**, 133504 (2011).

14. X.A. Tran, B. Gao, J.F. Kang, L. Wu, Z.R. Wang, **Z. Fang**, K.L. Pey, Y.C. Yeo, A.Y. Du, B.Y. Nguyen, M.F. Li and H.Y. Yu, "High Performance Unipolar AlO_y/HfO_x/Ni based RRAM Compatible with Si Diodes for 3D Application", in *Digest of Technical Papers - Symposium on VLSI Technology*, Jun 2011.

15. X.A. Tran, H.Y. Yu, Y.C. Yeo, L. Wu, W.J. Liu, Z.R. Wang, **Z. Fang**, K.L. Pey, X.W. Sun, A.Y. Du, B.Y. Nguyen, M.F. Li, "A High Yield HfO*x* Based Unipolar Resistive RAM Employing Ni Electrode Compatible with Si-Diode Selector for Cross-Bar Integration", *IEEE Electron Device Letters*, page 396-398, Mar 2011.

16. B. Gao, H. W. Zhang, B. Chen, L. F. Liu, X. Y. Liu, R. Q. Han, J. F. Kang, **Z. Fang**, H. Y. Yu, B. Yu, D. L. Kwong, "Modeling of Retention Failure Behavior in Oxide-based Resistive Switching Memory", *IEEE Electron Device Letters*, page 276-278, Mar 2011.

17. B. Gao, J. F. Kang, H. W. Zhang, B. Sun, B. Chen, L. F. Liu, X. Y. Liu, R. Q. Han, Y. Y. Wang, B. Yu, **Z. Fang**, H. Y. Yu, D. L. Kwong, "Oxide-based RRAM:

Physical based retention projection", *Solid-State Device Research Conference (ESSDERC),* page 392-395, 2010