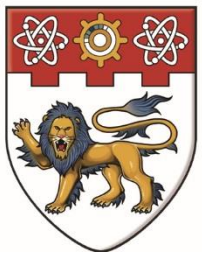

NANYANG TECHNOLOGICAL UNIVERSITY

COMPACT TRANSFORMER BASED POWER COMBINATION TECHNIQUES FOR MILLIMETER-WAVE CMOS POWER AMPLIFIERS

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SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

2016

Compact Transformer Based Power Combination Techniques for Millimeter-wave CMOS Power Amplifiers

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A thesis submitted to the Nanyang Technological University in partial fulfillment of the requirement for the degree of Doctor of Philosophy

2016

Acknowledgments

During all these years in Nanyang Technological University, I always appreciate who give me chances to pursue PhD degree in this research topic. It is a tough road in this journey but it is lucky for me to have reliable supervisors, friendly colleagues and supportive family members all the time. Nanyang Technological University also provides researchers with superb facilities and services.

First of all, I would like to dedicate my deep gratitude to my supervisor, Professor Kong Zhi Hui who opened the door of integrated circuit design to me. There have been a lot of memorable moments of discussing projects, troubleshooting and providing me her opinion about this research topic. As a supervisor, she gave me strong support and sought resources to facilitate our work. It is her patience, trust and guidance that lead me to go through all the difficulties encountered. With no doubt, her professionalism has inspired me and the experience of being her student would benefit my future career.

I also appreciate my co-supervisor Professor Yeo Kiat Seng, Dr. Ma Kaixue and Professor Siek Liter for their precious research suggestions. They selflessly shared their years of academic and industrial experience with me during the time in Centre of Excellence in IC Design (VIRTUS). Their

concentrated work altitudes prompted me to pursue the extreme performance of CMOS RF amplifiers.

In design verification step, research associate Yang wanlan and Lim Weimeng spared no efforts in collaborating with me. Their expert measurement setup guaranteed the fabricated chips are tested properly.

Certainly, for a student majored in integrated circuit design, supports from industry and government are also very important. Globalfoundries has liberally provided their well-developed semiconductor technologies for our experiments. Singapore EDB also awarded scholarships to our IC design students. I sincerely want to thank these aforementioned agencies.

Many thanks to this thesis reviewers for your precious opinion.

My last acknowledge belongs to my dear parents and my wife. They always support me with their care and love.

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Abstract

The strong demand on miniaturization of wireless communication systems has propelled the development of radio-frequency (RF) component integration in semiconductors. In the realm of millimeter-wave (mm-wave), the V-band centred at 60 GHz has been demonstrated to be the most promising frequency range for short range communication applications such as high data rate transfer systems. In fact, silicon-based 60 GHz chipsets with integrated power-amplifiers (PA) have become an economical choice for high density integration. As an indispensable building block in RF-front-end, compact PAs are highly sought after especially for low cost and high volume production. This dissertation presents novel designs of compact PAs using series, hybrid and parallel power-combining transformer techniques based on 65 nm low-power CMOS technology for V-band applications.

In the first design, a special shielding technique is incorporated into a series combining transformer for diminishing phase and amplitude discrepancies of the combined waves in differential drive PA. A new layout configuration of high quality factor (Q) inductor integrated with CMOS transistor source is demonstrated. To characterize this circuit topology, admittance matrix condensation algorithm is proposed, validated and then used for seeking the optimum inductance range. Following that, the nonlinearity of CMOS transistor with inductive source degeneration (ISD) is studied using

Volterra kernels in mm-wave frequency range. Based on these techniques, the fabricated PA has a compact size of 693×652 μm^2. Comparing to the state-of-the-art, the measured gain is above 10 dB at a wide bandwidth of 41-61 GHz. It is also capable of delivering high saturated power of 15.2 dBm at V-band.

The second differential PA utilizes an innovative concentric winding technique to realize differential 2-way parallel splitting and 4-way hybrid combining transformers with compact size. The implementation strategies of the hybrid combining transformer are acquired by investigating its coupling effect. When the combiner is connected with active devices, its nonlinear behaviors are studied. Using this winding technique, the area consumption of passive matching networks is largely saved and hence the chip area can be more efficiently used in a multi-stage PA architecture. During design phase of cascading stages, the active device is analyzed with transformer matching topology for wideband stability and gain flatness. With a compact size of 0.32 μm^2, the implemented PA in measurement achieves a high gain of 26.6 dB and delivers a high output power of 19.7 dBm at 60 GHz. The according 3-dB bandwidth covers a wide range of 51 GHz to 67 GHz. This PA also demonstrates the best performance in terms of gain-bandwidth product and figure of merit among the most advanced V-band CMOS PAs.

Finally, a balun for power-combining is devised on the proposed principle of concentric winding for realizing high power density in a single-ended PA. This configuration concurrently accomplishes balanced-unbalanced conversion

and parallel power splitting/combining. To calculate its power combination efficiency under the circumstance of input/output wave components with various phases and amplitudes, a computation method has been developed accordingly. Using the proposed power combining balun, the designed PA occupying only 0.10 μm^2 chip core area achieves the highest power density of 269.15 mW/mm^2 among the state-of-the-art 60 GHz CMOS PAs.

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Chapter 1: Introduction

1.1 Motivation

The utilization of frequency resources is based on the fact that radio-waves with different frequencies are not equally attenuated by atmosphere. Millimeter-wave transmission in air is of low loss at frequencies around Ka, W bands [1]-[3]. Due to this characteristic, these frequencies are mostly exploited for long range applications such as satellite communication, surveillance, remote sensing, navigation systems and military radar.

At V-band, the electromagnetic wave is of high attenuation in air and the radio range is relatively short. Therefore, the RF front-end operating at this un-licensed band is more appealing for multi-gigabit data transfer [4]-[8] and secure communications [9]. In IEEE 802.11ad standard for High Rate Wireless Personal Area Networks [10], the carrier frequency is around 60 GHz for supporting high data rate around 5 GB/s. Its potential applications include fixed/mobile network backhaul, fiber extensions/metro networking, enhancing network paths, LAN-to-LAN connections and radio local area networks (RLANs).

In such communication systems, RF PA enlarges the transmitter's radio range by increasing the power level of a signals to be propagated. High

performance PA with compact size is very attractive for low-cost RF front-end fabrication. The wireless system's performance in terms of linearity, effective range and reliability is also highly attributed to the PA design. Therefore, it is of utmost importance to realize compact mm-wave PAs with sufficient gain, output power etc. When the mm-wave PA ICs are studied on the whole, it can be found that the integrated semiconductor device plays a decisive role in PA performance. Several semiconductor devices including GaAs pHEMT / mHEMT, GaN, CMOS, BiCMOS and InP HEMT have been widely applied in mm-wave PA fabrication. Each technology possesses its own strength and weakness for PA implementation.

In general, the PAs in GaN and GaAs processes have demonstrated superb output power and efficiency up to W band [11]-[15]. GaAs pHEMT is a most common III-V semiconductor device in high output power ICs. For GaAs pHEMT PAs produced by MMIC commercial vendors such as TriQuint, Mimix and Avago, the circuit topology is composed by multiple stages and amplification paths [16]-[18]. Benefiting from high break down voltage, GaN PAs demonstrate both high output power and high *PAE* in mm-wave bands [19]-[22]. If the operating frequency becomes the primary design constraint, power amplifiers using InP HEMT and GaAs mHEMT device may challenge working frequency up to 0.5 THz [23][24]. Compared to the above III-V group devices, BiCMOS and CMOS are more suitable for low-power circuit in high

density integration [25]-[30]. In these silicon-based technologies, the baseband part may be designed with RF circuits including PA.

In a practical PA design, choosing semiconductor device is more than comparing the advantages and disadvantages of physical devices. The propagation characteristics of radio waves should be taken account as well. For long radio range applications such as satellite and radar, radio waves may need to be transmitted into a receiver in remote aerospace. In this case, above watt-level output power is desirable for antenna radiation and the propagated radio waves should avoid enduring high-rate absorption by air. For this reason, PAs in GaN and GaAs are prevalent for Ka and W band usages. In comparison, the communication range of V-band products for multi-gigabits data transfer is generally within a kilometer. Moreover, the majority of ICs for consumer electronics are fabricated in silicon process. As a result, it is possible and appealing to have SiGe and CMOS System-on-Chip (SOC) solutions at low cost. To achieve this aim, low power supply and breakdown voltages of silicon-based devices become a bottleneck for PA design. Due to this background and motivation, V-band PAs in silicon have recently drawn substantial research attention. The research status of mm-wave PAs on silicon substrates are compared in the following paragraphs.

As the gate length of CMOS transistor is scaled down to tens of nanometers, this progress has stimulated the development of CMOS RF front-ends operating at mm-wave band [31][32]. Since CMOS transistor can only

endure low bias voltage, it is considerably difficult to achieve high output power PA in this process. Therefore, if the target output power is fixed, more currents would be required for General Purpose (GP) CMOS PA than its GaN and GaAs counterparts. The fabrication of low-power (LP) CMOS is similar to that of GP CMOS but the former draws less dc current in the condition of the same transistor size. Currently, it has been reported that CMOS PA can operate at frequency more than 100 GHz [33]. As GP or LP CMOS process has been highly commercialized, multiple metal layers are available for chip layout. By taking this advantage, it is more convenient for GP/LP CMOS PA to adopt compact matching topologies such as coupling inductors as compared to pHEMT and GaN PAs.

Silicon on insulator (SOI) process has been developed for the purpose of ameliorating the performance of CMOS. In this technology, a resistive oxide layer is inserted under the transistor structure [34]. As a result, parasitics introduced by lossy silicon substrate are significantly reduced [35]. Currently, the cut-off frequency (f_t) and max-oscillation frequency (f_{max}) of 45 nm CMOS transistor in SOI are 0.35 THz and 0.3 THz respectively [36]. Since less parasitic is induced in this technology, it is desirable to design PA with higher *PAE* [37]. However, floating body effect of CMOS SOI may become a problem for its SOC applications. Besides, its fabrication cost is much higher than GP and LP CMOS as it has not been fully commercialized.

SiGe Heterojunction Bipolar transistor (BiCMOS) is another economical choice for making silicon-based PA IC. In this process, the BJT device can be integrated to satisfy the requirement of fast switching circuit parts. Meanwhile, CMOS transistor may still be available for other densely integrated function blocks [38]. As BJT is capable of enduring higher dc voltage supply and current than CMOS transistor, this characteristic is desirable for increasing PA output power level. Currently, the f_t of the advanced BiCMOS device is 0.3 THz while its f_{max} is 0.35 THz [39].

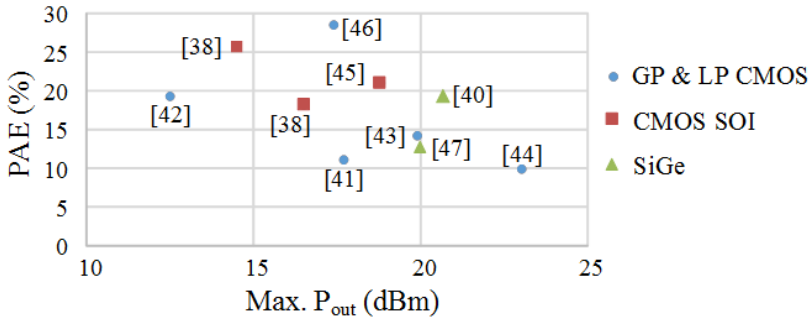


Fig. 1 *PAE* versus P_{sat} of 60 GHz PAs in silicon.

In Fig. 1, high performance 60 GHz PAs in the aforementioned silicon based technologies are selected and compared in terms of their *PAE* and saturated output power (P_{sat}). Most of these high output PAs use power combination techniques as the power delivered by one transistor is rather limited at mm-wave frequencies. Among them, the SOI and CMOS PAs have demonstrated slightly better results in *PAE*. In [46], the high *PAE* result is mainly because of RF CMOS scaling down to 45 nm and hence this transistor is capable of providing high gain and efficiency than other semiconductor devices.

With comparable *PAE* record, the transistor gate-length of the CMOS SOI PA is still 65 nm. Currently, most of high power 60 GHz PAs in silicon are fabricated using commercial BiCMOS and GP CMOS technologies. The reported output power level of SiGe PA reaches 20 dBm approximately [40]. In comparison, the reported output power delivered by GP & LP CMOS PA is around 23 dBm with large dc current around 1.7 A [44].

GaN field-effect transistor (FET) in SiC substrate can be biased at high dc voltage because of its robustness to breakdown effect. This technology can greatly level up the maximum output power of RF PAs [48]. Presently, the compatibility of this technology need to be further improved for the possibility of SOC. The most advanced GaN PA is reported to operate at 94 GHz [49]. Compared with circuits in the other kinds of group IV semiconductor, GaN IC is of bulky size due to low density integration. As discussed, this technology is promising in long range communication system requiring large dc power. Consequently, GaN device is seldom investigated for applications in 60 GHz PA. However, the P_{sat} of GaN PA can still keep an extraordinary high level of 31 dBm with 20% *PAE* even at 91 GHz [50].

As stated above, different technologies for mm-wave IC fabrication have been compared in several aspects including their usages, process limitations and performances in PA design. For this research, the potential application is aimed at consumer market of high data rate transfer. On the one hand, V-band around 60 GHz is the interested frequency of such communication systems. The

transmitter radio range is generally less than a kilometer and Silicon-based technologies have the potential of delivering sufficient output power. On the other hand, GP and LP CMOS are prevalent in fabricating all kinds of ICs inside consumer electronics. As it would be of low cost to fabricate analog, digital and RF parts in the same process, general purpose or low-power CMOS becomes the most appealing and economical choice. Moreover, these two CMOS technologies have been highly commercialized by foundries including TSMC, Globalfoundries (GF), STM, UMC etc. The process reliability and uniformity would guarantee yield even in mass production. From the above investigation and analysis, V-band PA research in GP and LP CMOS is promising in short range communication system for high data rate transfer.

1.2 Objectives

For mm-wave PA in GP or LP CMOS, there are several design challenges from the nature of semiconductor device.

The first challenge is the transistors' gain roll-off effect as the operating frequency increases. This phenomenon is obvious in mm-wave band as demonstrated in Fig. 2. The maximum stable gain (*MSG*) of Globalfoundries 65nm LP CMOS transistor in class A bias condition is plotted versus frequency. Below 6.5 GHz, the transistor may provide more than 20 dB gain in the case that it is perfectly matched by lossless passive networks. However, only 10 dB

gain can be extracted from the same transistor at 60 GHz. To achieve the same power gain level, the cascading stages inside a 60 GHz PA may be twice as many as that of a 6.5 GHz PA. Accordingly, the circuit topology of 60 GHz integrated PA is more complicated. For transmitter, the expected total gain of the PA can be estimated from the difference between the output power of the mixer and the input power of the antenna. The reported mixer output power level ranges from -5 to -2 dBm [51]-[53], whereas the antenna input power is highly related to communication link budget [54].

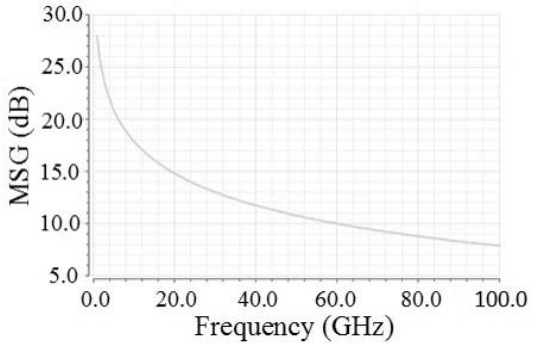


Fig. 2 *MSG* versus frequency of a LP CMOS transistor with 50 μm gate-width.

The limited gain level of CMOS transistor also deters design of high drain efficiency nonlinear PA in mm-wave band. It is because high drain efficiency and power added efficiency are not always simultaneously achieved in PA. Mathematically, *PAE* is expressed as

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} = \frac{P_{out}}{P_{dc}}\left(1 - \frac{1}{G}\right) \tag{1.1}$$

By this definition, the *PAE* is related to input power or power gain. Even if the ratio of P_{out} to P_{dc} is high, the final *PAE* could still be low because of a low gain level.

In classification of class A, B, AB, C, E, F … PA, the efficiency concept is examined from the view of drain efficiency as demonstrated in Fig. 3 and table I.

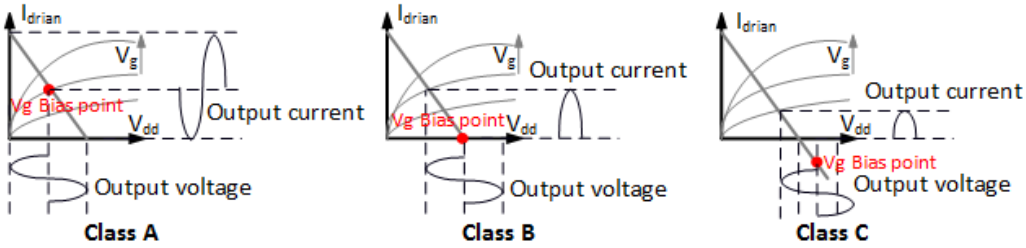


Fig. 3 Class A, B, C PA operation in theory

Table I

AMPLIFIER CLASSES OVERVIEW

Amplifier Classes	Conduction Angle	Drain Efficiency in theory
Class A	2π	50 %
Class AB	π to 2π	50% to 75 %
Class B	π	75 %
Class C	Less than π	75 % to 100%
Class D to T	Switching Mode	100%

From class A to C amplifiers, the drain efficiency is increased when less conduction angle is allowed for the output ac current. The required input voltage swing is not fully concerned by this classification. In a practical nonlinear PA design, the gate bias voltage of transistor is close to or even below the threshold voltage. Compared with linear PA delivering the same output

voltage swing, higher input ac voltage is needed for nonlinear one because of less gain. At 6.5 GHz and 60 GHz, the simulated maximum gain of GF's LP 50 μm gate-width transistor is plotted versus gate bias in Fig. 4. These two curves also indicate that nonlinear PAs in this process would induce lower power gain than linear ones especially at mm-wave band. As the *MSG* of this transistor operating in class B mode has already been very low at 60 GHz, any further degradation of power gain would become the main obstacle to designing nonlinear PAs with high *PAE*. If high drain efficiency and *PAE* needs to be simultaneously achieved by nonlinear PAs at mm-wave band, a possible solution is to further scale down the gate-length of CMOS transistor. Currently, most of the reported V-band PAs in 65 nm or 90 nm CMOS are set at class A operation mode for better *PAE* result [41]-[44]. Therefore, this research would mainly focus on improving the performances of linear mm-wave PA fabricated in this 65 nm LP CMOS.

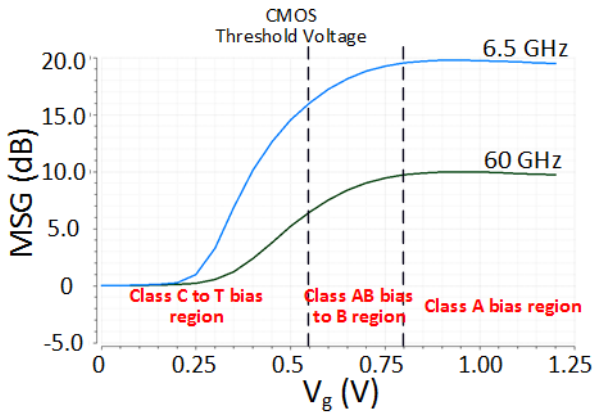
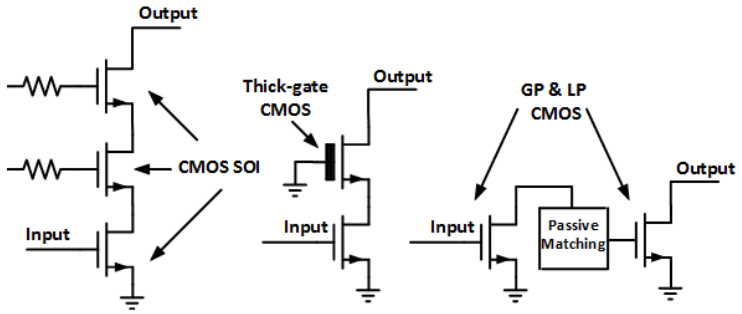


Fig. 4 *MSG* versus gate bias V_g at 6.5 GHz and 60 GHz.

For class A PA design, losses caused by signal transmission and imperfect matching decrease the gain level drawn from a single stage. Cascode [55][56], stacked FET devices [57]-[61] or cascading stages may be applied to strengthen the overall power gain as illustrated in Fig. 5.



(a) (b) (c)

Fig. 5 (a) Stacking CMOS SOI device; (b) Cascode with thick-gate CMOS; (c) Cascading stages.

Compared with GP/LP CMOS process, SOI and thick-gate technologies have not been fully commercialized and are costlier in fabrication. The advantage of cascode or staked FET configurations is obvious that it saves chip space for passive matching components. However, this amplification scheme is not preferred in GP/LP CMOS PA. It is because the top transistors would endure high gate-body voltage. For high RF output power operation, the dc voltage at gate can easily break GP or LP CMOS device down. Cascading common sourced (CS) transistors is of less requirements on semiconductor device. This topology is suitable for GP and LP CMOS PA design. In cascading amplifier, matching CMOS transistor needs extra inductive components to

enhance gain. In practical design, these inductive components can be distributed transmission line, planar inductors and transformers. As cascading stages increases, more chip area would be required. Accordingly, one important concern in this research is how to save the size of matching components for cascading amplifier.

The second design challenge of CMOS PA comes from the limited output power delivered at mm-wave band. The power-frequency limit of semiconductor device causes the decline of output power versus frequency [62]. Moreover, low bias voltage due to CMOS transistor gate-length scaling down is undesirable for making high output power PA. In a typical 60 GHz communication link budget [63][64], the antenna gain and PA output power can be traded off for satisfying receiver sensitivity. The PA output power, P_t in dBm is estimated by

$$P_t = P_r - G_t - G_r + 20\log\frac{\lambda}{4\pi d} \tag{1.2}$$

Where d and λ denote the communication range and the wavelength of the transmitted signals. To realize 10 m communication range for in-door applications, the free space loss item 20log(λ /4 π d) is about -88 dB. The minimum input power P_r is subject to receiver sensitivity of around -47 dBm [65]. The transmitter and receiver antenna gain, G_t and G_r respectively for 60 GHz applications is at level of 15 dBi [54][66]. From the above, the desirable PA output power should be more than 11 dBm at least. Higher PA output power

would be helpful for improving system bit error rate (BER) or communication range. In order to generate enough power for radiation, the total gate-width of transistors in the final stage should be sized accordingly. If only one transistor in the final stage is employed to satisfy high output power requirement, both gain level and *PAE* of this stage would be suffered. For this reason, it is essential to investigate power combining techniques. In CMOS mm-wave PAs, Several power combining techniques based on Wilkinson combiner [43][44], transformer [41][42][46][67]-[69], dual-radial architecture [70] and direct current combiner [71] have been adopted.

As demonstrated in Fig. 6, Wilkinson power combiner uses coplanar waveguide (CPW) or microstrip for interconnection and matching components. When more than two unit amplifiers (UA) are planned, Wilkinson combiners can also be cascaded. The resistor in this diagram is to improve matching and odd-mode rejection. On the whole, the horizontal size of Wilkinson combiner approximates $\lambda/4$ wave length and therefore it generally consumes bulky area in CMOS. In [43], the Wilkinson combiner in the final stage occupies about one third of the total chip area. In the PA reported in [44], this combiner covers nearly 50% of the overall chip area.

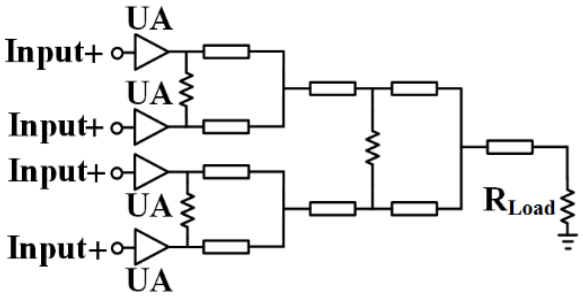


Fig. 6 Wilkinson combiner

For dual radial configure demonstrated in Fig. 7, the power splitting and combining networks are vertically overlapped to save area [70]. Although the area of power division networks may be reduced, there would be an additional power combination accomplished by the drive stage. Compared with other kind of power distribution schemes, this power combination is not necessary. As a result, more interconnection loss is induced and leads to power gain degradation.

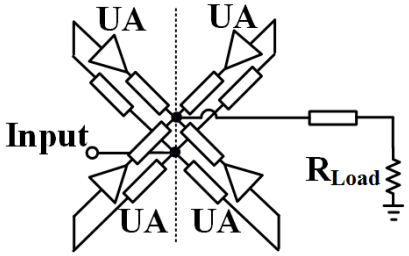


Fig. 7 Dual-radial power splitting and combining architecture

The balanced PA architecture is used to ameliorate I/O's backward reflection coefficient within wide bandwidth. As shown in Fig. 8, quadrature couplers such as Lange type are indispensable I/O components since they make the two waves reflected back from UAs present 180° phase differences. Between the two couplers, UAs can be cascaded to increase the overall gain. At

Q band, such a balanced PA in CMOS demonstrates above -10 dB backward reflection coefficient at the I/O ports [72]. At W band, another balanced CMOS PA has achieved 12 dBm P_{sat} with I/O's backward reflection coefficient below -15 dB at 37.8 % bandwidth [73]. As silicon substrate is rather lossy, it is hard to maintain low insertion loss with 90 degree coupler. Moreover, certain 90 degree coupler such as Lange type consist of narrow microstrip transmission lines. This layout requirement further reduces PA gain and power.

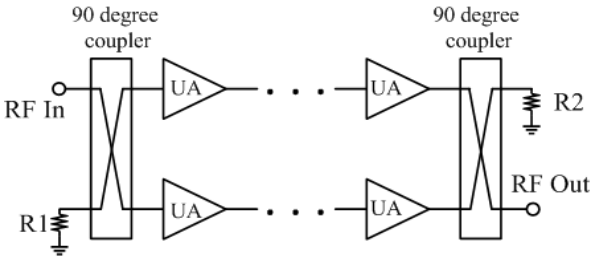


Fig. 8 Balanced PA architecture.

Direct combination is actually a kind of current addition technique. This combiner uses transmission lines with equal wave length as shown in Fig. 9. Similar to Wilkinson combiner, the size of direct combiner also approximates λ/4 wave length. Therefore, both the 2-way and 4-way direct power combiner reported in [71] nearly take up half of the chip core area. If the number of unit amplifier further increases, it would be hard to maintain in-phase wave addition at the load in layout design.

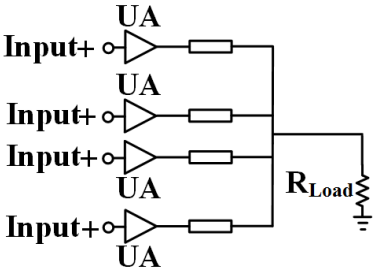


Fig. 9 Direct current combiner

In power combining transformer design, the transmission lines in coupling are folded into a spiral to compress its layout size. As illustrated in Fig.10 (a), the winded transmission lines can be placed far away from its ac ground. In this way, the corresponding inductance of transmission lines is enhanced. Compare with other transistor matching methods, the length of transmission line can be saved by using transformer configuration. Moreover, transformer in the final stage can accomplish transistor matching, impedance conversion and power combining simultaneously. For the above reasons, power combining transformers are of great advantages in size than other techniques. It has been a most attractive and practical solution for realizing compact integrated PA. By the classification method put forward by Kyu Hwan An etc. in [74], the transformer combination has been categorized to series and parallel types. The series combining transformer illustrated in Fig.10 (b) adds ac voltages out from UA pairs. In Fig. 10 (c), the parallel combining transformer sums up the coupled current.

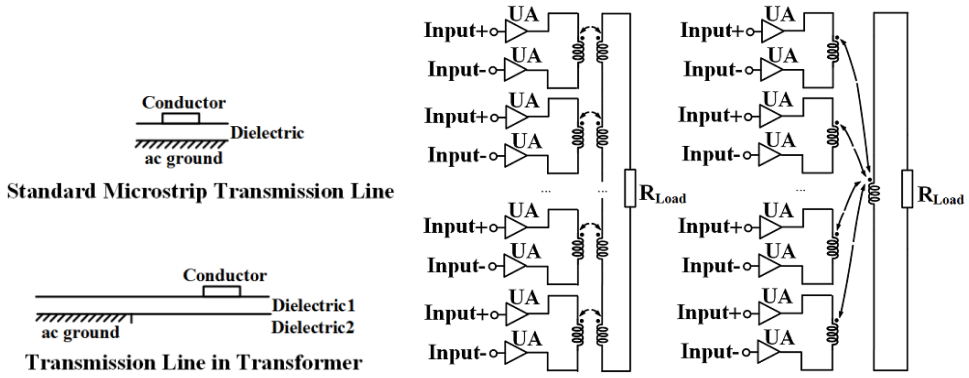


Fig. 10 (a) AC ground placement of transmission lines; (b) Series combining transformer; (c) Parallel combining transformer.

By examining the series and parallel combining transformers developed, it can be found that there is considerable unused area left. In addition, a lot of chip space is occupied by the interconnects. These clues imply that power combining transformer still has the margin of reducing size and hence levelling up its power density in silicon. As power combiner is generally the bulkiest component in mm-wave integrated PAs, this prospects are highly desirable for the purpose of saving IC fabrication cost and increasing yield. For the most advanced V-band CMOS PAs with high output power delivered by various multiple way combiners [41][43][44][68][71], their chip sizes are ranged from 0.83 to 1.88 mm^2. Based on the above investigations, it is of possibility to reduce the sizes of PAs by half with comparable or better performances. To achieve this goal, novel combining transformers with compact size would be proposed, implemented and verified in this CMOS PA research.

During design and implementation of novel transformers, the output waves to be combined are with various amplitudes and phases due to parasitic capacitors. The amplitude and phase status play an important role in affecting combination efficiency. Therefore, another primary task of this research is to source, investigate and ameliorate the phase and amplitude differences / imbalances for better transformer combination efficiency.

Finally, the CMOS transistor is potentially unstable at mm-wave band for PA design. It is because the capacitances between transistor gate and drain would enable coupling between input and output port. One method of solving stability problem is to insert additional resistors at transistor input as reported in [75]. However, this resistive part would inevitably absorb RF power and hence reduce PA gain and output power. Another method reported in [76]-[78] is to use neutralization capacitances. This configuration is only applicable to stabilize transistor pairs excited by differential signals. Besides, the matching design for unit amplifier is sensitive to the value of the cross connected neutralization capacitors. Inductive source degeneration (ISD) can be compatible with both differential and single-end mode operation and has been applied in LNA design operating at a few GHz [79]. To use ISD in mm-wave PA design, dc current capacity, integration compatibility and source inductance selection need to be taken into account in this research. Moreover, the linear and nonlinear behaviors of CMOS transistor with ISD would be thoroughly investigated in mm-wave band.

In summary, the efforts of this research are to maximize the performances of class A V-band PA in 65 nm LP CMOS. After comparing different methods of power combination, innovations on power combining transformer would be a primary task for reducing combiner size. During this exploration, one important concern is to source, characterize and ameliorate the waves to be combined with various phases and amplitudes. In unit amplifier stabilization, ISD technique into CMOS transistor can be a widely applicable solution. But so far, its characteristics and practical implementation strategies have not been comprehensively reported and studied for mm-wave PA design. All these design aspects need to be explored in this research.

1.3 Major contributions of the Thesis

In this thesis, novel techniques for compact and high performance mm-wave CMOS PAs are introduced, analysed and tested. During these PA designs, original analysis methods and algorithms are developed to characterize and optimize integration of passive and active devices. These techniques and methods are detailed in three 65 nm LP CMOS PA using innovative series, hybrid and parallel power combining transformers / baluns. Specifically, the contributions are introduced in the aspects of PA architectural planning, passive and active device design as follow.

During topology planning in architecture, all the cascaded stages inside the three PAs are arranged along loop-like shape. In this way, all the integrated components would make best use of chip area on the whole.

For the sake of characterizing active and passive device together, equivalent single-ended model conversion from multi-port differential transformer is introduced. By this method, multiple port transformers in connection with unit amplifiers become analyzable. The stability, bandwidth and matching of active together with passive device are then discussed.

In passive device design for CMOS PA:

1. Series power combining with X-shape patterned ground shielding are proposed for power division/combination in the first differential PA. With this special ground shielding, phase and amplitude differences of the waves to be combined are diminished within wide bandwidth. The inductive and capacitive coupling behavior of this series combining transformer is described by simplified lumped element model;
2. Within the second differential CMOS PA, 2-way parallel splitting transformer and 4-way hybrid combining transformer are devised to achieve high output power and compact combiner size. By maximally utilizing available transformer area and metal layers, the idea of concentric winding method has been put forward and implemented in these two compact transformers. Since both large power and high gain put pressure in valuable chip area, this winding technique can also give

a better tradeoff to integrate drive stages offering high total gain. The design strategies of hybrid combining transformer are acquired by studying its internal coupling effects and nonlinear behaviors with the active device. These analysis results are well applied in optimizing transformer layout and metal layer assignment for better efficiency.

3. In the third CMOS PA, baluns with power splitting/combining function are explored. This balun is also based on concentric parallel combining technique. As this configuration is able to accomplish unbalance-balance conversion and power combination simultaneously, the overall PA size can be greatly reduced while the power density is increased accordingly. For solving the problem of combination efficiency in the presence of layout parasitic components and asymmetry, computation method is derived from S-parameters. It can conveniently calculate the power combination efficiency of multi-port combiners with various phase and amplitude status. Such method can be widely used in characterizing in-phase or differential drive combiners.

In active device design for CMOS PA:

1. A new layout configuration of distributed high *Q* inductor integrated in the source of CMOS transistor is demonstrated for the first time. This layout is highly compatible with CMOS technology. It is also capable of enduring high dc current to PA transistor's drain. For optimizing the

dimensions of source inductor, its *Q* values are compared in the condition of different metal layer options and trace width;

2. The linear behaviors of CMOS transistor with ISD in mm-wave band are studied by the proposed admittance matrix condensation. This matrix condensation algorithm can be widely used in circuit symbolic derivation or numerical calculation. By using this method to characterize the lump element model, it is proved that ISD can enhance transistor stability and maintain transistors' stable gain when proper inductance value is selected. This ISD technique also benefits passive matching component design as impedance turn ratio of the external load to unit amplifiers are alleviated;
3. This thesis also presents nonlinear analysis steps of CMOS transistor with ISD in mm-wave frequency domain. The Volterra series is used to calculate the second and third order harmonic distortion in mild nonlinearity when CMOS transistor is biased at saturation region. The analytical outcome accords well with Spectre simulation results. The linear and nonlinear analysis of CMOS transistor with ISD provides a comprehensive solution for choosing the appropriate source inductance range.

1.4 Organization of the Thesis

Chapter 2 presents the differential mm-wave PA based on series combining transformer with special X-patterned ground shielding. After introducing PA fundamentals, this chapter continues with the elementary part in this PA design, CMOS transistor with inductive source degeneration. Its small signal feature is characterized by lump-element model. The algorithm of admittance matrix condensation is developed to solve such a complex circuit topology. Next, the large signal performances of CMOS transistor with ISD is studied by Volterra analysis. Then the architecture and transformers for the first differential CMOS mm-wave PA are discussed especially the power splitting/combining transformer design with X-shape pattern-ground shielding. In the end of this chapter, the implementation and measurement results of this differential mm-wave PA in 65 nm LP CMOS are detailed.

In chapter 3, design and analysis methodologies for making compact, wideband, high gain and output CMOS mm-wave PA using hybrid combining transformer are introduced. This chapter starts from architecture arrangement of transformer-based PA on the whole. In the next, the method of representing multi-port differential transformer by its equivalent single-ended model is provided for the convenience of analyzing PA stabilization and wideband matching strategies. Then the novel differential 2-way parallel dividing transformer and 4-way hybrid combining transformer are proposed for compact PA size. Particularly, the coupling model of the 4-way hybrid combining transformer is investigated for practical layout design guidance. Finally,

experiment results of the second differential CMOS PA in 65 nm LP CMOS are provided.

Chapter 4 elaborates the innovative parallel combining balun applied in single-ended V-band LP CMOS PA for high power density. In the beginning of this chapter, the concept and configuration of parallel combining balun is expounded. Then the computation solution for power combination efficiency is derived in the condition of input/output wave components with various phases and amplitudes. Afterwards, the architecture and implementation of the third single-ended mm-wave PA using the proposed balun is demonstrated. The measurement results of the fabricated PA in 65 nm LP CMOS is given in the end of this chapter.

Chapter 5 concludes this thesis and prospects the future research of mm-wave CMOS PA.

Chapter 2: Series Power Combination in CMOS

2.1 Fundamental of RF Power Amplifier

The basic function of RF/mm-wave PA is to enhance transmitter's output power for antenna radiation. In the level of hybrid integrated PA design or transistor matching, this building block can be represented by a two-port network in fig. 11. When a fully integrated PA is considered as a whole for system analysis, RF PA can be illustrated by deleting input and output matching networks in this figure since they have been integrated inside the chip. In this situation, Z_S and Z_L equal to Z_S' and Z_L' accordingly.

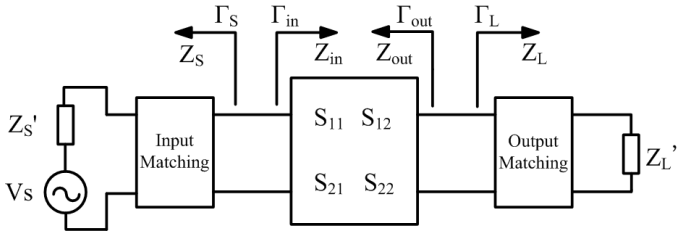


Fig. 11 RF/mm-wave PA represented by a two-port network

The four reflection coefficients Γ_{in}, Γ_{out}, Γ_S and Γ_L are defined as

$$\Gamma_{in} = \frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\Gamma_L} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \tag{2.1}$$

$$\Gamma_{out} = \frac{S_{22} - \Delta\Gamma_S}{1 - S_{11}\Gamma_S} = S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \tag{2.2}$$

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.3}$$

$$\Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0} \tag{2.4}$$

Where Δ equals $S_{11}S_{22}$-$S_{12}S_{21}$ and Z_0 is characteristic impedance [80].

The power gains are defined in terms of transducer, operation and available power gain denoted as G_T, G_p and G_a respectively. G_T represents the load power P_L over the available power P_{avs} from source.

$$G_T = \frac{1-|\Gamma_S|^2}{|1-\Gamma_{in}\Gamma_S|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{22}\Gamma_L|^2} \tag{2.5}$$

Operation power gain G_p is expressed by the power absorbed by load over the power actually injected into the networks. It means that how much gain can be obtained by adding the two-port network.

$$G_p = \frac{1}{1-|\Gamma_{in}|^2}|S_{21}|^2\frac{1-|\Gamma_L|^2}{|1-\Gamma_{22}\Gamma_L|^2} \tag{2.6}$$

Available power gain G_a is derived from the ratio of maximum power at the load to the source available power. It represents the potential gain that can be achieved when both input and output are in conjugate matching. In this ideal condition, G_t, G_p and G_a are all equivalent [81].

$$G_a = \frac{1-|\Gamma_S|^2}{|1-S_{11}\Gamma_S|^2}|S_{21}|^2\frac{1}{1-|\Gamma_{out}|^2} \tag{2.7}$$

In the case $|\Gamma_{in}|$ or $|\Gamma_{out}|$ is more than 1, the two-port network oscillates rather than amplifies signals. Rollett stability fact K is introduced to determine

the oscillation risk of a two-port networks. The criteria of unconditional stable status should meet the following two expressions [82].

$$K>1 \text{ and } |\Delta|<1, \text{ where } K=\frac{1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2}{2|S_{12}S_{21}|} \tag{2.8}$$

For a more concise expression, another stability parameter μ is alternatively developed in [83] as

$$\mu=\frac{1-|S_{11}|^2}{|S_{22}-S_{11}^{*}\Delta|+|S_{12}S_{21}|} \tag{2.9}$$

As input power increases, the fluctuations of voltages and currents may be proportional to bias. In this situation, certain specifications for PA in large signal operation are *PAE*, P_{1dB}, P_{sat}, HD_n, IM_n.

The growth of input signal level will cause gain compression until it reaches zero. Meanwhile, the PA gradually reaches the maximum output power P_{sat}. P_{1dB} denotes the points when large signal gain is 1 dB lower than small signal gain. HD_n is short for harmonic distortion where n (n>1) represents the order number of a harmonic. If $V_{out,1,0}$ and $V_{out,n,0}$ express the voltage magnitude of the fundamental and n-th harmonic respectively, the HD_n is obtained by

$$HD_n=\frac{|V_{out,n,0}|}{|V_{out,1,0}|} \tag{2.10}$$

Similarly, IM_n means the n-th order inter-modulation voltage over the fundament output voltage. The second and third order inter-modulation distortions are expressed as

$$IM_2 = \frac{\left|V_{out,1,\pm 1}\right|}{\left|V_{out,1,0}\right|} \tag{2.11}$$

$$IM_3 = \frac{\left|V_{out,2,\pm 1}\right|}{\left|V_{out,1,0}\right|} \tag{2.12}$$

2.2 CMOS Transistor with Inductive Source Degeneration

The CMOS transistor itself is of high instability at mm-wave frequencies. When ISD is applied in CMOS transistor for mm-wave PA design, three implementation details should be taken care. Firstly, the quality factor value of inductor should be as high as possible to reduce dc power dissipation. Secondly, since the matching components like transmission lines or transformers at the input/output of unit amplifier would largely occupy the areas nearby, the placement of this additional inductor should be better not to introduce too much interferences. Finally, its trace width should be wide enough to sustain high dc current density. Different from LNA design with low source current, the dc current flowing through a PA may be rather considerable. If the trace width of a dc path is not enough, severe electro-migration effect is a potential risk for PA.

The proposed source degeneration inductor integrated with CMOS transistor is illustrated in Fig. 12. Through vertical vias in dense placement, all source fingers are connected to a common thick metal layer M8 away from CMOS metal contact. Compared with layers M1-M7, M8 is made of thick

metal with high conductivity and can endure about 4 times more current. For design reference of drain bias path in 65 nm LP CMOS, dc current limit per unit width of metal layers is demonstrated in Table II. The data is estimated at the condition of 100 °C and 100 000 power-on-hours. In the circumstance of short line connection, the current limit in table II is roughly tripled when trace length is less than 10 μm. For 200 μm gate-width LP CMOS transistor biased at 0.8 V drain voltage, the total dc current is around 42.5 mA. To compactly implement source inductor, M7 and M8 are preferred metal layer options.

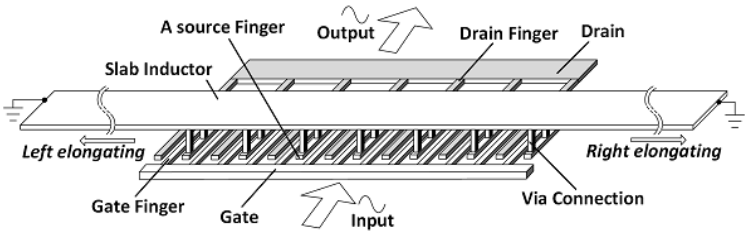


Fig. 12 Proposed ISD Structure in Layout.

Table II

METAL CURRENT LIMIT OF THE 65 NM LP CMOS TECHNOLOGY (100°C)

	M1	M2	M3	M4	M5	M6	M7	M8	M9
Current Limit (mA/μm)	1.7	2.2	2.2	2.2	2.2	2.2	9.2	>9.2	2.3

The high *Q* ISD is formed by elongating the slab inductor in the side direction according to the value desired. Since transistors used for PA generally consist of multiple fingers, the slab inductor can be designed symmetrical to the centre for balanced dc current distribution. Accordingly, the total dc current limit of slab inductor is doubled. In this condition, the inductance for each

source terminal can be roughly estimated by paralleling the left and right slab inductor.

In Fig. 13, the *Q* values for various trace width are computed at 60 GHz by EM simulations. The results of slab inductor designed in other metal layers are also provided for comparison. Although *Q* can be enhanced by widening the trace width of slab inductor, it will also bring more parasitic capacitance between source to gate or drain. It also puts more demands on chip area as trace width increases. Therefore, the width should be kept as small as possible while an acceptable *Q* is maintained. By Fig 13, slab inductor would be of higher *Q* in M8 than in other metal staking options. The corresponding *Q* is more than 11.2 because slab inductor in M8 would be of low series resistance and overlapping capacitance to the ground plane. In this figure, it can also be found that a small peak *Q* value exists when thick metal layer M8 is of 3.5 um width. This dimension is just about the distance between transistor gain and drain with 2um gate-width fingers. Such a slab inductor can sustain around 64.4 mA dc current which is sufficient to satisfy current density requirements.

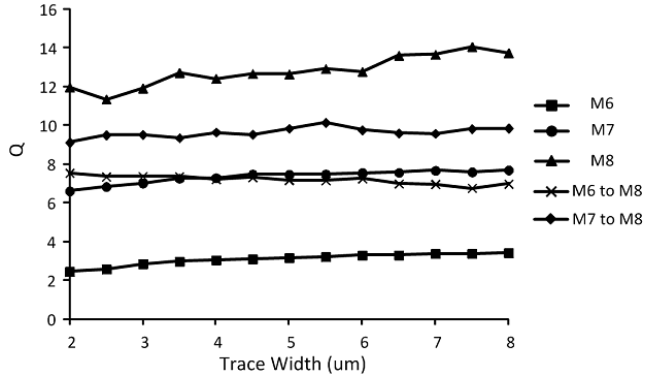


Fig. 13 *Q* values of slab inductor with various trace width at 60 GHz

In this configuration, the wave propagation direction is in line with both gate and drain terminals and perpendicular to the vertical source connections. On the one hand, the coupling between the source and gate/drain is physically reduced by this wave direction. On the other hand, this slab inductor would almost not affect the transformer matching in either input or output port. Moreover, this configuration can easily be integrated in a single-end or differential power amplifier.

In this PA design, the transistor is biased at saturation region, the dominant elements play key roles in transistor model are shown in Fig. 14. This lump element model would be used to characterize both the linear and nonlinear behaviors of LP CMOS transistor with ISD.

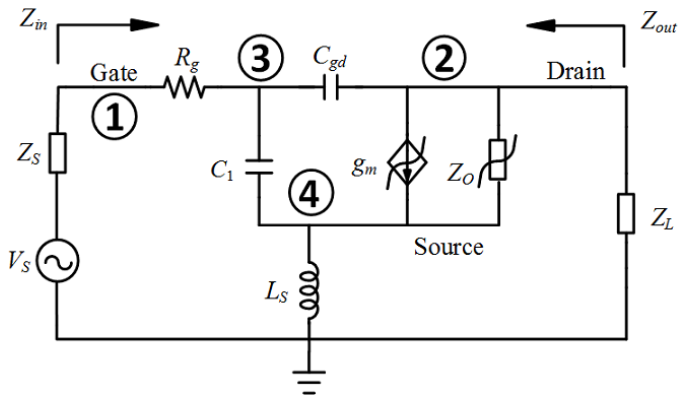


Fig. 14 Simplified lumped element model of LP CMOS transistor with ISD.

In this model, C_1 express the total equivalent capacitors between transistor gate and source. R_g is the gate resistance which is comparable to the source impedance Z_S. It cannot be ignored when large gate-width transistor is matched

to passive networks in mm-wave frequency range. Z_O is the channel conductance between drain and source. Z_O and g_m are modeled as nonlinear impedance and transconductance respectively to describe the main sources of nonlinearity in LP CMOS transistor. In higher order harmonic analysis using Volterral series, nonlinear current is supposed to be excited from the fundamental signals by these nonlinear components. These transistor parameters can be extracted by SPECTRE simulator.

In this active device model, the gate capacitances C_{gd} between gate and drain is of vital importance for PA stability status. It is because this element enables capacitive coupling between input and output as operating frequency increases. In another word, it explains the Miller effect which may cause active device oscillatory in mm-wave frequency. If this capacitance is removed from the active device model, there would be of no instability problem caused. However, this capacitor C_{gd} also greatly increases the difficulty of analyzing the whole active device as it cannot be treated as a unilateral model anymore. In this case, Miller approximation is not accurate enough to characterize this mm-wave circuit. In order to handle such kinds of complex circuit topology, a theorem named as admittance matrix condensation is motivated, introduced and derived for analyzing the model in Fig. 14.

2.3 Admittance Matrix Condensation

Matrix is a fundamental tool in circuit analysis. For characterizing various kinds of circuit and system, impedance, admittance, scattering and transmission matrix have been defined [80]. Among them, admittance matrix is widely used in analyzing multi-port networks as it can be directly derived from circuit topology or schematic.

As the internal nodes of a circuit schematic increases, the corresponding matrix dimension would also be enlarged. Therefore, high dimension admittance matrix representing a complex schematic increases difficulty in deriving symbolic equations or calculating specific responses for I/O ports. However, a number of classical circuit design theories and techniques are on the basis of port-to-port parameters such as amplifier stability, gain etc. In order to reduce matrix dimension, pivotal condensation can be applied in admittance analysis. However, this method can only derive equivalent matrix from $N\times N$ to $(N\text{-}1)\times(N\text{-}1)$ dimension [84]. For a circuit with M I/O ports and N internal nodes, the iteration times of pivot condensation would be $N\text{-}M$. Therefore, this iteration for high scale matrix condensation is not suitable for symbolic calculation and also needs multiple steps in circuit analytical computation.

For port-to-port analysis, the proposed admittance matrix condensation can transform $N\times N$ admittance matrix representing a circuit topology to its equivalent $M\times M$ form ($N>M$) without multiple iteration as shown in Fig. 15. In symbolic computation of circuit topologies even with complex internal connection, the proposed algorithm can conveniently give the condensed

admittance matrix. In numerical computation, this method is capable of converting high dimension admittance matrix for calculating the concerned *I*-*V* relationship. As stated, one application of admittance matrix condensation is to optimize the active device part in mm-wave amplifier.

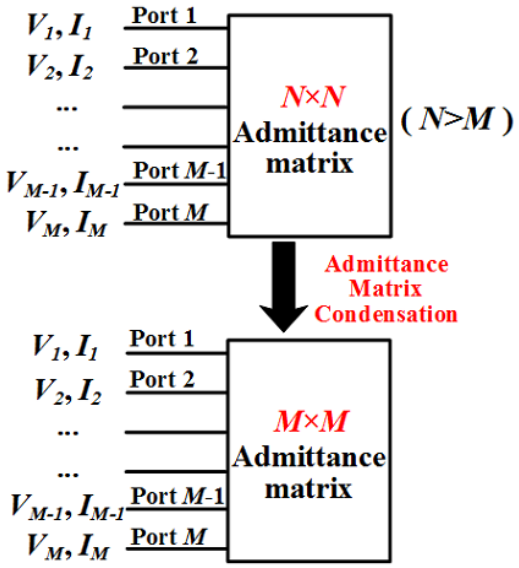


Fig. 15 Admittance matrix condensation from $N\times N$ to $M\times M$ dimension ($N>M$).

The admittance matrix can be directly used for solving *I*-*V* equation of $[I]=[Y][V]$. In the first step of admittance matrix condensation, the original elements are firstly sequenced according to the node number associated to circuit topology ($N>M$) as

$$[Y]=\begin{bmatrix} y_{1,1} & \cdots & y_{1,M} & y_{1,M+1} & \cdots & y_{1,N} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ y_{M,1} & \cdots & y_{M,M} & y_{M,M+1} & \cdots & y_{M,N} \\ y_{M+1,1} & \cdots & y_{M+1,M} & y_{M+1,M+1} & \cdots & y_{M+1,N} \\ \vdots & \ddots & \vdots & \vdots & \ddots & \vdots \\ y_{N,1} & \cdots & y_{N,M} & y_{N,M+1} & \cdots & y_{N,N} \end{bmatrix} \tag{2.13}$$

For better demonstration of admittance matrix condensation, the nodes related to the concerned ports are numbered from 1 to M while the unconcerned nodes are numbered from M+1 to N in (2.14). For I-V relationship in (2.13), the matrix product result of [Y][V] should confirm Kirchhoff's current law. For circuit internal nodes, there would be no external current injected physically. Therefore, the current addition result of internal nodes inside a circuit topology should be zero for i_{M+1} to i_N. This condensation is to obtain the equivalent port-to-port admittance elements when circuit internal voltages from v_{M+1} to v_N are not the key concern.

$$\begin{bmatrix} \begin{bmatrix} i_1 \\ \vdots \\ i_M \end{bmatrix} \\ \begin{bmatrix} i_{M+1} \\ \vdots \\ i_N \end{bmatrix} \end{bmatrix} = \begin{bmatrix} \begin{bmatrix} y_{1,1} & \cdots & y_{1,M} \\ \vdots & \ddots & \vdots \\ y_{M,1} & \cdots & y_{M,M} \end{bmatrix} & \begin{bmatrix} y_{1,M+1} & \cdots & y_{1,N} \\ \vdots & \ddots & \vdots \\ y_{M,M+1} & \cdots & y_{M,N} \end{bmatrix} \\ \begin{bmatrix} y_{M+1,1} & \cdots & y_{M+1,M} \\ \vdots & \ddots & \vdots \\ y_{N,1} & \cdots & y_{N,M} \end{bmatrix} & \begin{bmatrix} y_{M+1,M+1} & \cdots & y_{M+1,N} \\ \vdots & \ddots & \vdots \\ y_{N,M+1} & \cdots & y_{N,N} \end{bmatrix} \end{bmatrix} \begin{bmatrix} \begin{bmatrix} v_1 \\ \vdots \\ v_M \end{bmatrix} \\ \begin{bmatrix} v_{M+1} \\ \vdots \\ v_N \end{bmatrix} \end{bmatrix} \tag{2.14}$$

The above matrix can be alternatively represented by submatrix divided in (2.14) as

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_1 & Y_2 \\ Y_3 & Y_4 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.15}$$

For circuit internal nodes, there would be no external current injected physically. Therefore, i_{M+1} to i_N equals zero. The product of M+1 to N rows in [Y] with [V] gives

$$[Y_4][V_2] = -[Y_3][V_1]$$

$$\begin{bmatrix} y_{M+1,M+1} & \cdots & y_{M+1,N} \\ \vdots & \ddots & \vdots \\ y_{N,M+1} & \cdots & y_{N,N} \end{bmatrix} \begin{bmatrix} v_{M+1} \\ \vdots \\ v_N \end{bmatrix} = -v_1 \begin{bmatrix} y_{M+1,1} \\ \vdots \\ y_{N,1} \end{bmatrix} -\ldots- v_M \begin{bmatrix} y_{M+1,M} \\ \vdots \\ y_{N,M} \end{bmatrix} \tag{2.16}$$

The internal node voltage inside a circuit are solved by using Cramer law to $[Y_4]$

$$v_{i+M}\left(i=1,\ldots,N-M\right)=\sum_{m=1}^{M}(-1)^i\frac{\left|Y_{4(i,m)}\right|}{\left|Y_4\right|}v_m\ ,\left|Y_4\right|\neq 0 \tag{2.17}$$

$[Y_{4(i,\ m)}]$ is obtained by substituting the i column of $[Y_4]$ by the m column of $[Y_3]$ and then interchange the replaced i column sequence to the first one. Applying the results of (2.17) in $[I_1]$ calculation leads to

$$[I_1]=[Y_1 \quad Y_2][V]=[Y'][V_1] \tag{2.18}$$

$$[Y']=\frac{1}{\left|Y_4\right|}\begin{bmatrix} (-1)^0 y_{1,1}\left|Y_4\right|+\sum_{i=1}^{N-M}(-1)^i y_{1,i+M}\left|Y_{4(i,1)}\right| & \cdots & (-1)^0 y_{1,M}\left|Y_4\right|+\sum_{i=1}^{N-M}(-1)^i y_{1,i+M}\left|Y_{4(i,M)}\right| \\ \vdots & \ddots & \vdots \\ (-1)^0 y_{M,1}\left|Y_4\right|+\sum_{i=1}^{N-M}(-1)^i y_{M,i+M}\left|Y_{4(i,1)}\right| & \cdots & (-1)^0 y_{M,M}\left|Y_4\right|+\sum_{i=1}^{N-M}(-1)^i y_{M,i+M}\left|Y_{4(i,M)}\right| \end{bmatrix}$$

(2.19)

The elements $y'_{m,n}$ (n=1,…,M) of $[Y']$ in (2.19) is then expressed as

$$y'_{m,n}=\frac{1}{\left|Y_4\right|}\left[(-1)^0 y_{m,n}\left|Y_4\right|+\sum_{i=1}^{N-M}(-1)^i y_{\mathrm{m},i+M}\left|Y_{4(i,n)}\right|\right] \tag{2.20}$$

From (2.20), $y'_{m,n}$, is derived from element $y_{m,n}$ in $[Y_1]$, the m row in $[Y_2]$, the n column in $[Y_3]$ and the whole $[Y_4]$. The above four items for solving each

$y'_{m,n}$ constitute submatrix $[A_{m,n}]$ with $(N\text{-}M+1)\times(N\text{-}M+1)$ dimension out of $[Y]$. The elements in $[A_{m,n}]$ are detailed as

$$a_{j,k} = \begin{cases} y_{m,n}\,(j=1,k=1); \\ y_{m,(k-1)+M}\,(j=1,k=2,...,N-M+1); \\ y_{(j-1)+M,n}\,(j=2,...,N-M+1,k=1); \\ y_{(j-1)+M,(k-1)+M}\,(j,k=2,...,N-M+1); \end{cases} \tag{2.21}$$

For $[A_{m,n}]$, $|Y_4|$ (k=1) and $|Y_{4(k-1,\ m)}|$ (k=2,..,N-M+1) are minors of $|A_{m,n}|$ when it is expanded by its first row.

$$\left|A_{m,n}\right| = (-1)^{1+1} y_{m,n} \left|Y_4\right| + \sum_{k=2}^{N-M+1} (-1)^{1+(N-M+1)} y_{m,(k-1)+M} \left|Y_{4(k-1,n)}\right| \tag{2.22}$$

By (2.19) and (2.21), the admittance element in the condensed matrix for port-to-port circuit analysis is concisely represented as

$$y'_{m,n} = \frac{\left|A_{m,n}\right|}{\left|Y_4\right|},\ \left|Y_4\right| \neq 0 \tag{2.23}$$

The complete matrix condensation procedure is then concluded as

1. The nodes associated with ports are firstly numbered;

2. By connection relationship of circuit topology, the original $N\times N$ admittance matrix without condensation can be directly written according to Kirchhoff's Current Law;

3. Using (2.23), the condensed $M\times M$ admittance matrix is obtained from the $N\times N$ one.

Example

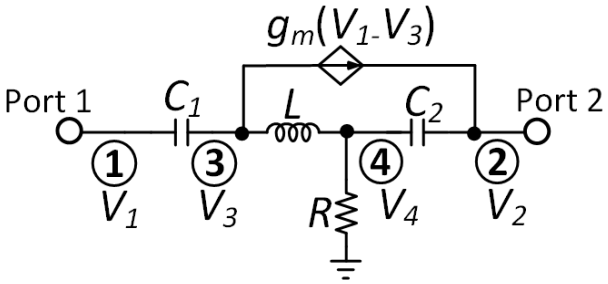


Fig. 16 An example of circuit topology to be solved by admittance matrix condensation. (R=5.0 Ω, g_m=0.1 S, C_1=10.0 fF, C_2=100.0 fF, L=10.0 pH)

In this circuit topology, the cross connected transconductance between node ② and ③ complicates the analysis. This model cannot be directly solved from input to output and hence admittance condensation method is necessary.

By using the proposed theorem, the condensed admittance matrix of circuit topology in Fig. 16 can be conveniently solved. In the first step, the circuit nodes associated with port 1 and port 2 are sequenced preferentially. The characteristics at port 1 and port 2 are the mostly concerned and hence the associated nodes are numbered as ① and ②. The left circuit internal nodes are numbered as ③ and ④;

In the second step, the original admittance matrix is obtained from physical connection relationships in circuit topology;

$$[Y]=\left[\begin{array}{cc|cc} sC_1 & 0 & -sC_1 & 0 \\ -g_m & sC_2 & g_m & -sC_2 \\ \hline -sC_1+g_m & 0 & sC_1+1/sL-g_m & -1/sL \\ 0 & -sC_2 & -1/sL & sC_2+1/sL+1/R \end{array}\right] \tag{2.24}$$

In the final step, the equivalent condensed admittance matrix is immediately written by (2.23).

$$y'_{1,1} = \frac{\begin{vmatrix} sC_1 & -sC_1 & 0 \\ -sC_1 + g_m & sC_1 + 1/sL - g_m & -1/sL \\ 0 & -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}}{\begin{vmatrix} sC_1 + 1/sL - g_m & -1/sL \\ -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}} \tag{2.25}$$

$$y'_{1,2} = \frac{\begin{vmatrix} 0 & -sC_1 & 0 \\ 0 & sC_1 + 1/sL - g_m & -1/sL \\ -sC_2 & -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}}{\begin{vmatrix} sC_1 + 1/sL - g_m & -1/sL \\ -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}} \tag{2.26}$$

$$y'_{2,1} = \frac{\begin{vmatrix} -g_m & g_m & -sC_2 \\ -sC_1 + g_m & sC_1 + 1/sL - g_m & -1/sL \\ 0 & -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}}{\begin{vmatrix} sC_1 + 1/sL - g_m & -1/sL \\ -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}} \tag{2.27}$$

$$y'_{2,2} = \frac{\begin{vmatrix} sC_2 & g_m & -sC_2 \\ 0 & sC_1 + 1/sL - g_m & -1/sL \\ -sC_2 & -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}}{\begin{vmatrix} sC_1 + 1/sL - g_m & -1/sL \\ -1/sL & sC_2 + 1/sL + 1/R \end{vmatrix}} \tag{2.28}$$

For verification of this symbolic expression, the condensed Y parameters in Fig. 16 are computed by (2.25) to (2.28) at 100 GHz.

$$[Y'] = \begin{bmatrix} \text{-0.006064 + 0.006830i} & \text{0.002498 + 0.001120i} \\ \text{-0.124034 - 0.055643i} & \text{0.013198 + 0.097652i} \end{bmatrix} \tag{2.29}$$

In comparison, the results obtained by commercial circuit simulator is denoted as $[Y'_c]$. The results indicate that the proposed condensation method is

able to give equivalent port-to-port admittances. In commercial software, symbolic expression of the condensed admittance matrix can never be obtained.

$$[Y'_c] = \begin{bmatrix} -0.006+0.007i & 0.002+0.001i \\ -0.124-0.056i & 0.013+0.098i \end{bmatrix} \quad (2.30)$$

In comparison, both symbolic and numerical results of the equivalent port-to-port admittance are available with the aid of admittance matrix condensation. Moreover, this method can also be used to analyse other kinds of circuit topologies.

2.4 Linear Analysis of CMOS transistors with ISD

In the proposed mm-wave amplifier, inductive source degeneration is applied in CMOS transistors to increase stability. In small signal analysis, the nonlinearity of Z_O and g_m are not considered. Then this active device is characterized by the lumped element model in Fig. 17. In this model, two nodes are associated with I/Os sequenced as ① ② and the other two are circuit internal nodes numbered as ③ ④. The capacitance between gate and drain causes instability and this cross coupled connection increases the analysis complexity. For characterizing the circuit topology, 4×4 admittance matrix is required. Condensation of the 4×4 admittance matrix to its equivalent 2×2 one would facilitate application of the classical two-port theories for amplifier

design . From the circuit topology in Fig. 17, the 4×4 admittance matrix is written in (2.31) as

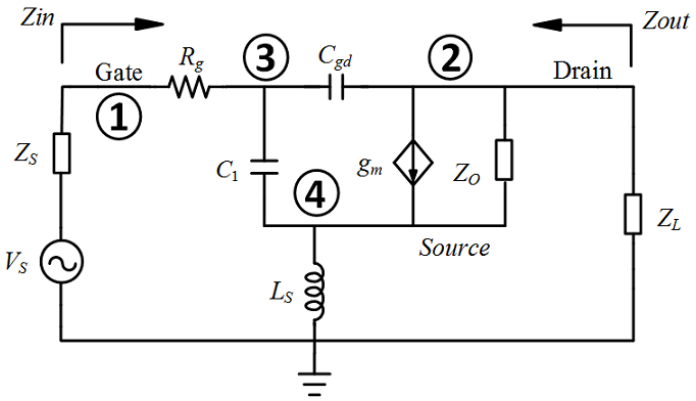


Fig. 17 Simplified first order lumped element model of LP CMOS transistor with ISD

$$[Y]=\left[\begin{array}{cc|cc} y_{1,1} & 0 & -1/R_g & 0 \\ 0 & y_{2,2} & g_m - sC_{gd} & -g_m - 1/Z_0 \\ \hline -1/R_g & -sC_{gd} & y_{3,3} & -sC_1 \\ 0 & -Z_0 & -g_m - sC_1 & y_{4,4} \end{array}\right] \tag{2.31}$$

$$y_{1,1} = 1/R_g \tag{2.32}$$

$$y_{2,2} = 1/Z_0 + sC_{gd} \tag{2.33}$$

$$y_{3,3} = 1/R_g + s\left(C_1 + C_{gd}\right) \tag{2.34}$$

$$y_{4,4} = g_m + 1/Z_0 + 1/\left(sL_S\right) + sC_1 \tag{2.35}$$

In 2.31, Z_O represents $sC_{ds}+1/R_{ds}$. Applying the results of (2.23) into (2.31), the condensed two port admittance matrix can be directly derived as follows

$$[Y']=\begin{bmatrix} y'_{1,1} & y'_{1,2} \\ y'_{2,1} & y'_{2,2} \end{bmatrix} \tag{2.36}$$

$$\Delta = y_{3,3}y_{4,4} - sC_1\left(g_m + sC_1\right) \tag{2.37}$$

$$y'_{1,1} = \frac{\begin{vmatrix} y_{1,1} & -1/R_g & 0 \\ -1/R_g & y_{3,3} & -sC_1 \\ 0 & -g_m - sC_1 & y_{4,4} \end{vmatrix}}{\Delta} = y_{1,1} - \frac{y_{4,4}}{{R_g}^2\Delta} \tag{2.38}$$

$$y'_{1,2} = \frac{\begin{vmatrix} 0 & -1/R_g & 0 \\ -sC_{gd} & y_{3,3} & -sC_1 \\ -Z_0 & -g_m - sC_1 & y_{4,4} \end{vmatrix}}{\Delta} = -\frac{sC_{gd}y_{4,4} + sC_1/Z_0}{R_g\Delta} \tag{2.39}$$

$$y'_{2,1} = \frac{\begin{vmatrix} 0 & g_m - sC_{gd} & -g_m - 1/Z_0 \\ -1/R_g & y_{3,3} & -sC_1 \\ 0 & -g_m - sC_1 & y_{4,4} \end{vmatrix}}{\Delta} = \frac{y_{4,4}\left(g_m - sC_{gd}\right) - \left(g_m + 1/Z_0\right)\left(g_m + sC_1\right)}{R_g\Delta}$$

(2.40)

$$y'_{2,2} = \frac{\begin{vmatrix} y_{2,2} & g_m - sC_{gd} & -g_m - 1/Z_0 \\ -sC_{gd} & y_{3,3} & -sC_1 \\ -Z_0 & -g_m - sC_1 & y_{4,4} \end{vmatrix}}{\Delta}$$

$$= y_{2,2} + \frac{\left(g_m - sC_{gd}\right)\left[sC_{gd}y_{4,4} + sC_1/Z_0\right] + \left(g_m + 1/Z_0\right)\left[sC_{gd}\left(g_m + sC_1\right) + y_{3,3}/Z_0\right]}{\Delta} \tag{2.41}$$

For amplifier design, the input and out impedances (Z_{in} and Z_{out}) are the most concerned parameters for matching. At microwave or mm-wave frequencies, transistor may even provide negative gain without external matching components. To maximize power gain, matching designed is highly

related to Z_{in} and Z_{out}. With the results in (2.36), Z_{in} and Z_{out} are conveniently obtained by using the general formulas of two-port networks as

$$Z_{in} = \left(y'_{1,1} - \frac{y'_{1,2}\, y'_{2,1}}{Y_L + y'_{2,2}} \right)^{-1} \tag{2.42}$$

$$Z_{out} = \left(y'_{2,2} - \frac{y'_{1,2}\, y'_{2,1}}{Y_S + y'_{1,1}} \right)^{-1} \tag{2.43}$$

The maximum stable gain (*MSG*) and stability criterion of classical two-port networks can also be immediately calculated by using elements in the condensed matrix [*Y*'].

$$K = \frac{2Re\left(y'_{1,1}\right)Re\left(y'_{2,2}\right) - Re\left(y'_{1,2}\, y'_{2,1}\right)}{\left|y'_{1,2}\, y'_{2,1}\right|} \tag{2.44}$$

$$MSG = \frac{y'_{2,1}}{y'_{1,2}} \tag{2.45}$$

From (2.42) to (2.44), the classical two-port theories are conveniently applied in a particular schematic analysis with the help of admittance matrix condensation. The condensed [*Y*'] representing the circuit topology in Fig. 17 are plotted in Fig. 18. The computation results of admittance matrix condensation exactly match the curve by commercial circuit simulator. By the result of $y'_{1,2}$, L_S would gradually change its sign of real part from negative to positive. ISD also increases the absolute value of $y'_{2,1}$ real part. Simultaneously, its imaginary part is decreased in a less gradient compared with the real part curve of $y'_{2,1}$.

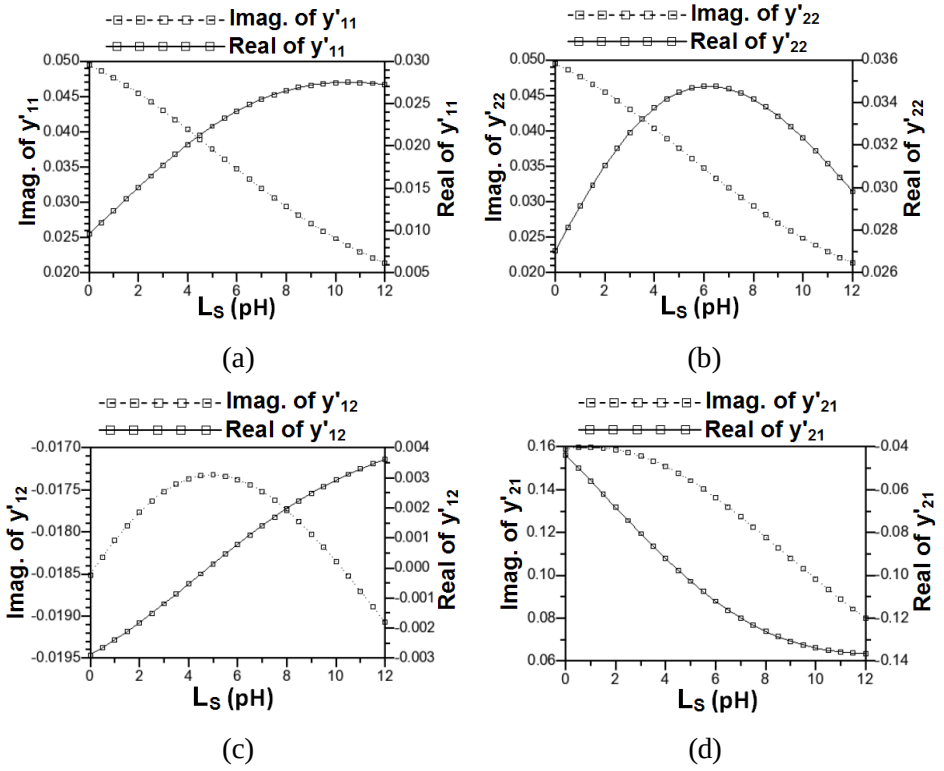


Fig. 18 (a) Real and imaginary part of y'_{11}; (b) Real and imaginary part of y'_{22}; (c) Real and imaginary part of y'_{12}; (d) Real and imaginary part of y'_{21}.

In Fig. 19, $|y'_{2,1}|$, $|y'_{1,2}|$ and *MSG* are plotted in the condition of varied L_S. It is noticeable that L_S ranging from 0 pH to 5 pH will slightly increases $|y'_{2,1}|$ while decreases $|y'_{1,2}|$ simultaneously. In another word, forward transmission and reverse isolation are ameliorated by ISD at mm-wave band. For this reason, source inductance of 4 pH to 6 pH is preferred in this design and the *MSG* can be improved up to 0.6 dB.

Without admittance matrix condensation, the analysis of a circuit topology requires a case-by-case derivation and even may be rather troublesome. For solving Z_{out} by definition, the current flowing through g_m, Z_O and C_{gd} should be

calculated one by one and then added up. The voltage at node ② are required to be computed in response to V_S in advance of solving Z_{out}. All these parameters need to be solved for the purpose of deriving only one parameter Z_{out}. Moreover, certain expression like *MSG* is hard to derive in (2.45).

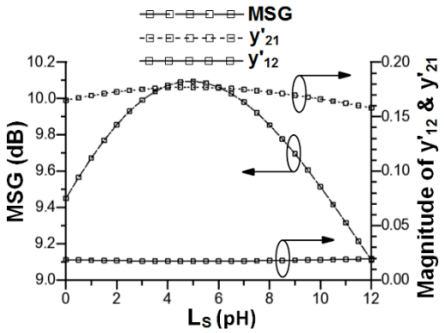


Fig. 19 *MSG*, Magnitude of y'_{12} and y'_{21} versus L_S at 60 GHz.

The result of *K* versus L_S is also plotted in Fig. 20. The stability factor *K* increases as L_S does. The active device part becomes absolute stable when *K* is above 1. Although source inductance of 10 pH is capable of making the two-port networks absolute stable, the *MSG* would also be degraded. When the value of L_S exceeds 6 pH, stability factor *K* is improved at the price of *MSG* greatly reduced.

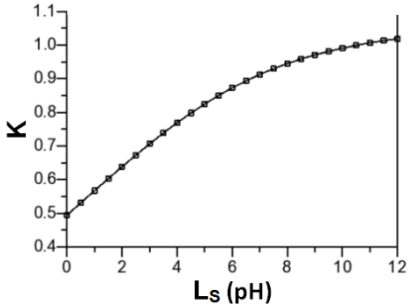
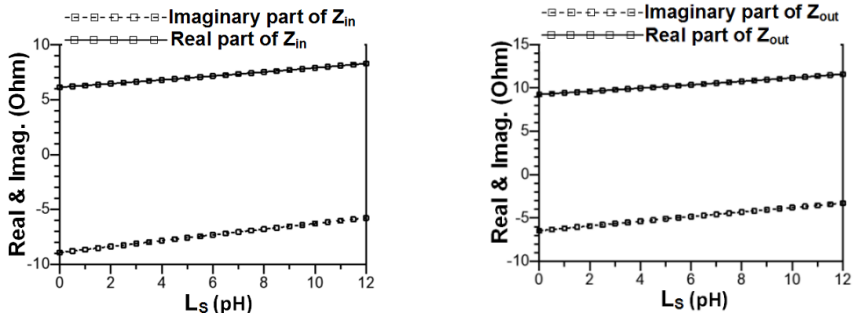


Fig. 20 *K* versus L_S at 60 GHz.

For passive component matching, Z_{in} and Z_{out} of transistors are key parameters. The real and imaginary parts of Z_{in} and Z_{out} are shown in Fig. 21. ISD increases the real part of Z_{in} and Z_{out} while slightly decreases the absolute of their imaginary part. In Fig. 21 (a), the real part of Z_S is close to 6 Ω for conjugate matching without ISD. However, this design target is undesirable for external matching circuits for two reasons. On the one hand, such a low value needs external matching networks with high impedance turn ratio in real part. It would be difficult to realize this aim practically and still maintain low transition loss in silicon substrate. On the other hand, the design target is of high oscillation risk without additional stabilization methods. As a result, the selections of Z_S are unavoidable to make more trade-offs between matching and stability without ISD. This case is similar for Z_L in output matching. As the source inductance L_S increases, the impedance alteration in the real part of Z_{in} and Z_{out} eases the requirements for passive circuits in impedance turn ratio. Meanwhile, the stability of the active device increases as well. In this way, better matching and stability can be achieved by ISD technique.



(a) (b)

Fig. 21 (a) Real and imaginary parts of Z_{in}. (b) Real and imaginary parts of Z_{out}

2.5 Nonlinearity Analysis of Inductive Source Degeneration

The nonlinearity behaviour of CMOS transistor with ISD can be analysed with the aid of Volterra series. This method has been used to characterize nonlinear circuit operating at only a few gigahertz in [85]-[88] but yet mm-wave. For providing a comprehensive ISD design reference, second and third harmonic distortions of the proposed configuration are computed. In Volterra theory, the output response of ac signal into a system can be regarded as superposition of *n*-th order harmonics in frequency domain. Nonlinearity current sources are added into small signal model for computation of higher order voltages and currents. In this design case, the drain ac current can be expressed as a function by v_{gs} and v_{ds}. It is expended in Taylor series as follows.

$$i_{ds}(v_{gs}, v_{ds}) = \frac{\partial i_D}{\partial v_{GS}} v_{gs} + \frac{1}{2}\frac{\partial^2 i_D}{\partial v_{GS}^2} v_{gs}^2 + \frac{1}{6}\frac{\partial^3 i_D}{\partial v_{GS}^3} v_{gs}^3$$

$$+ \frac{\partial i_D}{\partial v_{DS}} v_{ds} + \frac{1}{2}\frac{\partial^2 i_D}{\partial v_{DS}^2} v_{ds}^2 + \frac{1}{6}\frac{\partial^3 i_D}{\partial v_{DS}^3} v_{ds}^3$$

$$+ \frac{\partial i_D}{\partial v_{GS}\partial v_{DS}} v_{gs} + \frac{1}{2}\frac{\partial^3 i_D}{\partial v_{GS}^2\partial v_{DS}} v_{gs}^2 v_{ds} + \frac{1}{2}\frac{\partial^3 i_D}{\partial v_{GS}\partial v_{DS}^2} v_{gs} v_{ds}^2$$

$$= g_m v_{gs} + K_{2gm} v_{gs}^2 + K_{3gm} v_{gs}^3$$

$$+ g_o v_{ds} + K_{2go} v_{ds}^2 + K_{3go} v_{ds}^3$$

$$+ K_{2gm\&go} v_{gs} v_{ds} + K_{3gm2\&go} v_{gs}^2 v_{ds} + K_{3gm\&go2} v_{gs} v_{ds}^2 \qquad (2.46)$$

g_m, K_{2gm}, K_{3gm}, g_o, K_{2go}, K_{3go}, $K_{2gm\&go}$, $K_{3gm2\&go}$, $K_{3gm\&go2}$ are dc bias dependant parameters and all of them are indispensable for Volterra analysis at mm-wave frequency range. In order to obtain good linearity and efficiency, the Taylor series are extracted at saturation region with 0.8 V V_{GS} and 1.2 V V_{DS}. It has been known that Volterra method is only suitable for characterizing weak nonlinear behavior. In this design, as long as the peak voltage value of the input signal at gate is smaller than 0.5 V, the influence caused by other capacitance variation is negligible compared to the nonlinearity effect of transconductance and channel impedance. This amplitude range of input peak voltage has been beyond the breakdown voltage limit of LP CMOS transistor and hence it is sufficient for making a practical calculation. Once the nodal voltages in lower order model are solved, the results are then available for higher order current sources calculation using Volterra Kernels. The expressions for the second and third order nonlinear current sources i_{NL2} and i_{NL3} are obtained by the following equations:

$$i_{NL2}(v_{gs,1}, v_{ds,1}) = \frac{1}{2} K_{2gm} v_{gs,1}^2 + \frac{1}{2} K_{2go} v_{ds,1}^2 + \frac{1}{2} K_{2gm\&go} v_{gs,1} v_{ds,1} \tag{2.47}$$

$$\begin{aligned} i_{NL3}(v_{gs,1}, v_{gs,2}, v_{ds,1}, v_{ds,2}) &= K_{2gm} v_{gs,1} v_{gs,2} + \frac{1}{4} K_{3gm} v_{gs,1}^3 \\ &+ K_{2go} v_{ds,1} v_{ds,2} + \frac{1}{4} K_{3go} v_{ds,1}^3 + \frac{1}{2} K_{2gm\&go} \left(v_{gs,1} v_{ds,2} + v_{gs,2} v_{ds,1} \right) \\ &+ \frac{1}{4} K_{3gm2\&go} v_{gs,1}^2 v_{ds,1} + \frac{1}{4} K_{3gm\&go2} v_{gs,1} v_{ds,1}^2 \end{aligned} \tag{2.48}$$

$v_{gs,1}/v_{ds,1}$ and $v_{gs,2}/v_{ds,2}$ denote the first order and second order GS/DS voltage respectively. The corresponding second and third order circuit topologies are similar as illustrated in Fig. 22. In small signal model, Z_S, Z_L and Z_O are complex impedance. When applied at higher order model, their imaginary part should be modified according to the harmonic frequency. By substituting elements s, Z_S, Z_L and Z_O in matrix (2.31) with $2s/3s$, Z_{S2}/Z_{S3}, Z_{L2}/Z_{L3} and Z_{O2}/Z_{O3}, the according second/third order nodal matrix is expressed by $[A_{NL2}]/[A_{NL3}]$ in (2.51)/(2.53). The nonlinear current sources i_{NL2}/i_{NL3} in Fig. 22 is taken into account by matrix $[I_{NL2}]/[I_{NL3}]$ as follows.

$$I_{NL2} = [0 \quad i_{NL2} \quad 0 \quad -i_{NL2}]^T \tag{2.49}$$

$$I_{NL3} = [0 \quad i_{NL3} \quad 0 \quad -i_{NL3}]^T \tag{2.50}$$

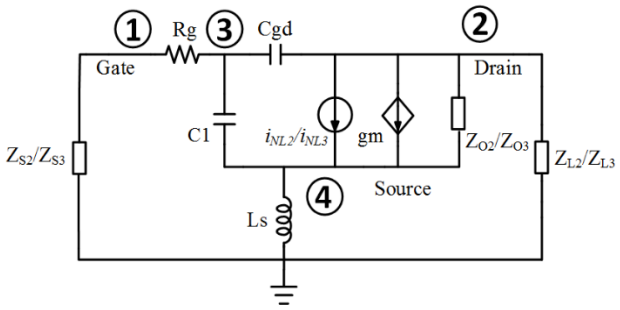


Fig. 22 Schematic for the Second and third order nonlinearity analysis.

For the second order harmonic, the complete nonlinearity equation is expressed as

$$[I_{NL2}] = [A_{NL2}][V_{NL2}] \tag{2.51}$$

$$\begin{bmatrix} 0 \\ i_{NL2} \\ 0 \\ -i_{NL2} \end{bmatrix} = \begin{bmatrix} 1/R_g + 1/Z_{S2} & 0 & -1/R_g & 0 \\ 0 & 1/Z_{02} + 2sC_{gd} + 1/Z_{L2} & g_m - 2sC_{gd} & -g_m - 1/Z_{02} \\ -1/R_g & -2sC_{gd} & 1/R_g + 2s\left(C_1 + C_{gd}\right) & -2sC_1 \\ 0 & -Z_{02} & -g_m - 2sC_1 & g_m + 1/Z_{02} + 1/\left(2sL_S\right) + 2sC_1 \end{bmatrix} \begin{bmatrix} v_{1NL2} \\ v_{2NL2} \\ v_{3NL2} \\ v_{4NL2} \end{bmatrix} \tag{2.52}$$

For the third order harmonic, the nonlinearity equation can be constructed in a similar way as

$$[I_{NL3}] = [A_{NL3}][V_{NL3}] \tag{2.53}$$

$$\begin{bmatrix} 0 \\ i_{NL3} \\ 0 \\ -i_{NL3} \end{bmatrix} = \begin{bmatrix} 1/R_g + 1/Z_{S3} & 0 & -1/R_g & 0 \\ 0 & 1/Z_{03} + 3sC_{gd} + 1/Z_{L3} & g_m - 3sC_{gd} & -g_m - 1/Z_{03} \\ -1/R_g & -3sC_{gd} & 1/R_g + 3s\left(C_1 + C_{gd}\right) & -3sC_1 \\ 0 & -Z_{03} & -g_m - 3sC_1 & g_m + 1/Z_{03} + 1/\left(3sL_S\right) + 3sC_1 \end{bmatrix} \begin{bmatrix} v_{1NL3} \\ v_{2NL3} \\ v_{3NL3} \\ v_{4NL3} \end{bmatrix} \tag{2.54}$$

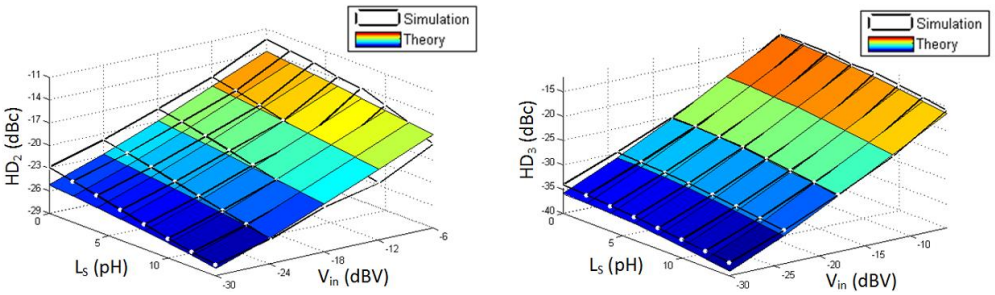
With linear drain voltage v_{2L1}, the second and third order harmonic distortion (HD_2 and HD_3) can then be calculated by (2.55) and (2.56).

$$HD_2 = \frac{\begin{vmatrix} 1/R_g + 1/Z_{S2} & 0 & -1/R_g & 0 \\ 0 & i_{NL2} & g_m - 2sC_{gd} & -g_m - 1/Z_{02} \\ -1/R_g & -i_{NL2} & 1/R_g + 2s\left(C_1 + C_{gd}\right) & -2sC_1 \\ 0 & 0 & -g_m - 2sC_1 & g_m + 1/Z_{02} + 1/\left(2sL_S\right) + 2sC_1 \end{vmatrix}}{|A_{NL2}|v_{2L1}} \tag{2.55}$$

$$HD_3 = \frac{\begin{vmatrix} 1/R_g + 1/Z_{S3} & 0 & -1/R_g & 0 \\ 0 & i_{NL3} & g_m - 3sC_{gd} & -g_m - 1/Z_{03} \\ -1/R_g & -i_{NL3} & 1/R_g + 3s\left(C_1 + C_{gd}\right) & -3sC_1 \\ 0 & 0 & -g_m - 3sC_1 & g_m + 1/Z_{03} + 1/\left(3sL_S\right) + 3sC_1 \end{vmatrix}}{|A_{NL3}|v_{2L1}} \tag{2.56}$$

In Fig. 23, both theoretical and simulation results of HD_2 and HD_3 are contoured at 60 GHz. ISD technique reduces HD_2 and HD_3 simultaneously

even at 60 GHz. It can also be observed that HD_3 increases more significantly than HD_2 when the input is excited by higher level voltages, which accurately reflects the internal mechanism of a transistor. In mild nonlinear region, *Ls* can boost linearity more effectively with larger input power. For 5 pH source inductor with V_{in} equals to -12 dB, HD_2 and HD_3 are reduced by about 2 dBc and 1.5 dBc theoretically.



(a) (b)

Fig. 23 (a) L_S, V_{in} versus HD_2 at 60 GHz. (b) L_S, V_{in} versus HD_3 at 60 GHz.

As L_S ranged from 0 pH to 12 pH, the simulated output power P_{sat} and peak *PAE* are also plotted in Fig. 24 for design reference. When L_S equals to 5 pH, the P_{sat} and *PAE* are 14.9 dBm and 35.8 % respectively in the condition of lossless matching. Such P_{sat} and *PAE* results are very close to that of an active device without ISD, which are 15.2 dBm and 38.6 % correspondingly.

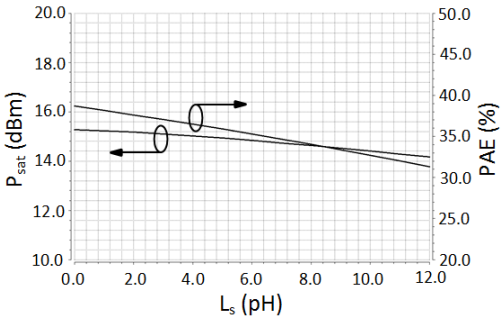


Fig. 24 Ideal Simulated P_{sat} and *PAE* versus L_S valued from 0 pH to 12.0 pH.

2.6 Architecture of CMOS Power Amplifier with Series combining Transformer

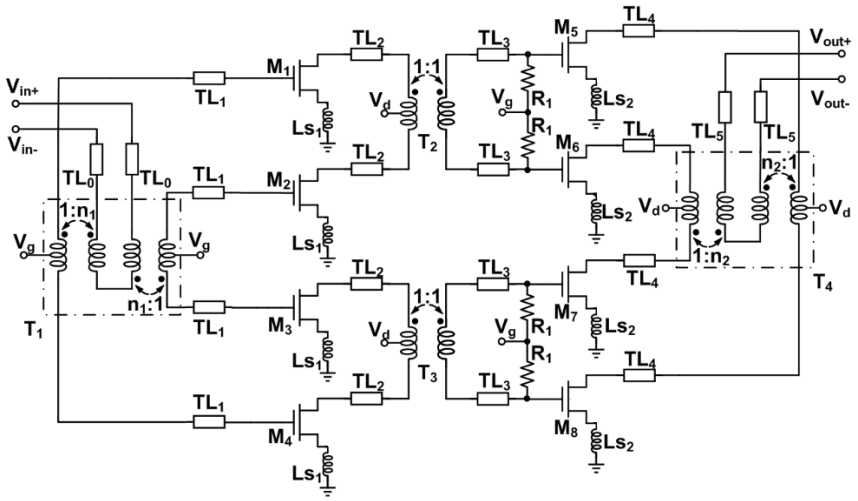


Fig. 25 Schematic of millimeter-wave CMOS PA using ISD technique and series combining transformer.

The architecture of mm-wave CMOS PA using ISD technique and series combining transformer is shown in Fig. 25. This differential PA is composed of two stages matched by transformers. Both in schematic or layout, the circuit maintains symmetry in horizontal plane. In the first stage, the gate-width of each transistor is 140 μm. The active devices of the second stage consist of 200 μm gate-width CMOS transistors. As discussed in the previous chapter, 5 pH L_{S1} and L_{S2} is applied for reducing impedance turn ratio, facilitating matching and offering better linearity in this design.

In this architecture diagram, T_1 and T_4 are series transformers that can realize impedance matching and power splitting / combining concurrently. In T_1 / T_4, the four terminals in connection with CMOS transistors form two differential pairs. These two differential ports are in series power splitting / combining way. In an ideal case, the external source and load are 100 Ω. Therefore, the impedance turn ratio of the external to the internal can be still as high as 8:1 and 5:1 for T_1 and T_4 respectively. In [55], the inductive coupling is mainly concerned in transformer analysis. In this amplifier design, both capacitive and inductive coupling play important roles in matching which would be examined in detail. T_2 and T_3 are two identical 1:1 transformers that interconnect the two stages and present the desired impedances to the active devices.

All drain bias V_d is fed through center taps of transformers. This bias pattern saves large areas for making bulky RF chocks such as inductors and capacitors. TL*n* (*n*=1, 2, 3, 4) represents the additional transmission lines for interconnections. The gate bias of the second stage is fed through a large resistor valued 4k Ω for simplifying structures of T_2 and T_3.

The selection of the sizes of active devices is based on the targeted output power of the PA. The design guidelines for the active device size selection are listed as follows:

1) The total target output power P_{out} in dBm is set as the starting point of active device selection;

2) According to PA architecture, the number of active devices n in the final stage determines how much power should be delivered out by each one;

3) The loss L_T in dB caused by passive matching and I/O connections increases the desirable output power level of each active device;

4) As the actual fabricated device would draw less dc current than that in simulation, which accounts for output power reduction. Therefore, it is recommended to define a correction coefficient α as the ratio of typically measured dc current over its simulated value;

5) With α compensation, the output power of each active device in the final stage should be above (P_{out}-10lg(n)+L_T-10lgα) dBm in the design phase (P_{out}≈15.0 dBm, n=4, L_T≈2.5 dB and α≈0.6 for the final stage of this PA design in GF 65 nm LP CMOS);

6) Then the active device size should satisfy the above output power requirement. Its corresponding input power becomes the reference to choose drive stage size. The procedure is repeated from step 1 to step 5. The overall PA design sequence is from the final stage to the first stage.

2.7 Input and Output Series Combining Transformers

In practical signal transition inside a transformer, both inductive and capacitive coupling actually exist. When the capacitive coupling is made to be

insignificant, the width of both primary and secondary loops need to be narrowed for improving *Q* of the winding inductors. However, this design principle is not applicable for high turn ratio transformer design as it may bring superfluous leakage inductance that is undesirable for matching. Moreover, the limited trace width is hard to endure high dc current for PA bias. In this design, the impedance matching and power splitting rely upon both capacitive and inductive coupling. The proposed transformer structure is applied in T_1 and T_4 sharing the same configuration, as illustrated in Fig. 26. A special X-shape ground shielding is inserted to reduce phase and amplitude differences of wave transition between the two secondary and primary loops. It also provides an extra degree of freedom in adjusting turn ratio.

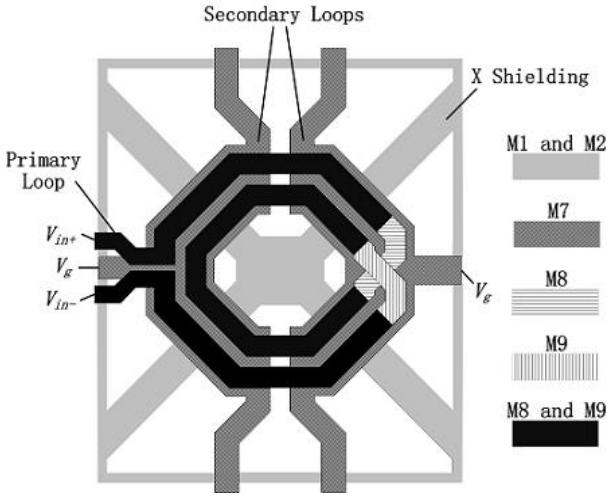


Fig. 26 Layout of proposed series splitting / combining transformer.

In T_1, V_{in+} and V_{in-} are injected into the transformer by the primary loop. Two secondary loops are in bilateral symmetry and the input power from the

primary loop is divided into four output ports. When only the left or right portion of transformer is considered, half of the primary and one secondary loop are coupled through windings with turn ratio estimated as *N/2*. The ac current directions in the secondary two loops are in reverse. On the whole, the primary couple the left and right part in a series way because it sums up the ac voltage level coupled from secondary loops. This series coupling can maximize the turn ratio of primary over secondary which is estimated as two times of *N/2*. As the winding trace length of the primary is much longer than that of the secondary, the topmost thick metal M8 and M9 are stacked to reduce conduction loss. In the intersection part, M8 and M9 are physically separated to form an air bridge. The secondary loops are made of board metal trace to further enlarge turn ratio *N/2*. As most part of primary traces are physically placed over the secondary loops, this configuration would provide capacitive coupling paths.

The center taps of secondary loops can be used to bias transistor gate in the first stage. Likewise, V_d is feed into T_4 by the same side points and wide winding trace is helpful for minimizing heat generated in parasitic series resistors. This series combining transformer can be analyzed the by lumped element model in Fig. 27. The model extracts the dominant components to investigate the internal mechanism of coupling between the primary and secondary loops. In this case, TL1 are modeled as inductors L_1 and they can be

considered along with the load terminated at secondary loops as Z_L' for concise expressions mathematically.

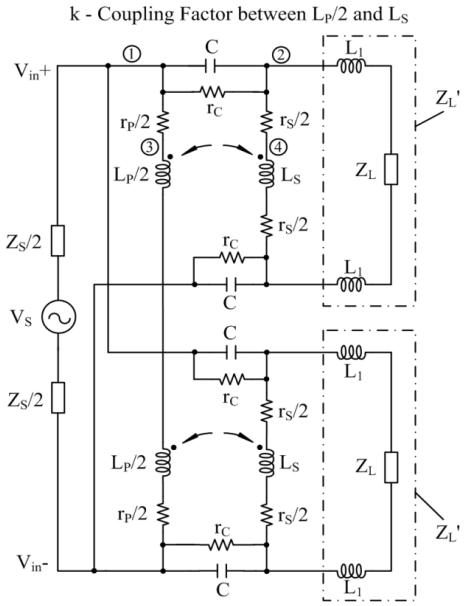


Fig. 27 Lumped element model of series combining transformer.

Solving this model, V_1 is equals to V_{in+} and the voltage at point 2 can be expressed as

$$V_2 = V_1 \frac{g_3\left(g_1 N^2 + g_2\right) + g_1 g_2 N}{\left(g_1 N^2 + g_2\right)\left(g_2 + g_3 + g_L\right) - g_2^{\,2}} \tag{2.57}$$

$$N = L_P / L_S \tag{2.58}$$

$$g_1 = 1/\left(r_P + jwL_P(1-k)\right) \tag{2.59}$$

$$g_2 = 1/\left(r_S + jwL_S(1-k)\right) \tag{2.60}$$

$$g_3 = 1/(2r_C) + jwC/2 \tag{2.61}$$

$$g_S = 1/Z_S \tag{2.62}$$

$$g_L = 1/Z_L' \tag{2.63}$$

The currents between 1-4 nodes are solved by

$$I_{12} = V_1 \frac{g_1 g_3 \left[\left(N^2 - N \right) g_2 + N^2 g_L \right] + g_2 g_3 g_L}{\left(g_1 N^2 + g_2 \right)\left(g_2 + g_3 + g_L \right) - g_2{}^2} \tag{2.64}$$

$$I_{13} = V_1 \frac{g_1 g_2 \left[(1 - N) g_3 + g_L \right]}{\left(g_1 N^2 + g_2 \right)\left(g_2 + g_3 + g_L \right) - g_2{}^2} \tag{2.65}$$

$$I_{24} = V_1 \frac{g_1 g_2 N \left[(N - 1) g_3 - g_L \right]}{\left(g_1 N^2 + g_2 \right)\left(g_2 + g_3 + g_L \right) - g_2{}^2} \tag{2.66}$$

In this series combining transformer, N is more than 4 for satisfying turn ratio requirements. From (2.65) and (2.66), I_{24} are N times of I_{13} in magnitude which explains the major loss caused by inductive components. The efficiency of the transformer from primary to one secondary loop, differential input and output impedance are found to be

$$\eta = \frac{g_L \left[g_3 \left(g_1 N^2 + g_2 \right) + g_1 g_2 N \right]^2}{g_S \left[\left(g_1 N^2 + g_2 \right)\left(g_2 + g_3 + g_L \right) - g_2{}^2 \right]^2} \tag{2.67}$$

$$Z_{in} = \frac{2\left(g_1 N^2 + g_2 \right)\left(g_2 + g_3 + g_L \right) - 2 g_2{}^2}{g_1 g_2 g_3 (N - 1)^2 + g_1 g_2 g_L + g_1 g_3 g_L N^2 + g_2 g_3 g_L} \tag{2.68}$$

$$Z_{out} = \frac{2\left(g_1 N^2 + g_2 \right)\left(g_1 + g_3 + g_S \right) - 2 g_1{}^2 N^2}{g_1 g_2 g_3 (N - 1)^2 + g_1 g_2 g_S N^2 + g_1 g_3 g_S N^2 + g_2 g_3 g_S} \tag{2.69}$$

Supposing an extreme case when k is equal to 1 with pure real g_S and g_L, V_2 and efficiency η would be pulled down as N increase. The magnitude of I_{12}

is decreased as well because of less capacitive coupling current. The lowest reflection condition is achieved when $Z_{in}=Z_S^*$ and $Z_{out}=Z_L'^*$.

During transformer implementation, the X-shape ground shielding is placed under the secondary loops to diminish phase and amplitude differences. As illustrated in Fig. 26, the primary loop is physically blocked from this shielding by the secondary loops. As a result, this shielding will lower secondary loop inductance L_S more significantly than primary loop inductance L_P, which would be helpful for realizing high turn ratio. The simulation results of T_1 with and without X-shape shielding are shown in Fig. 28.

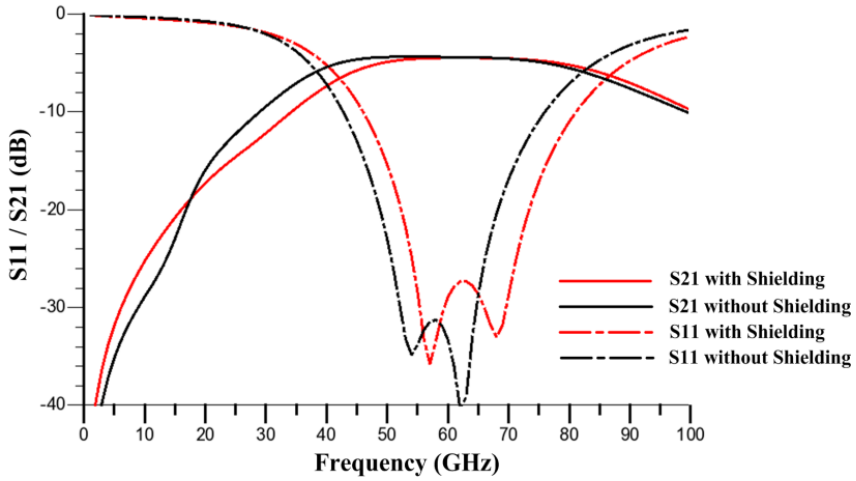


Fig. 28 S_{21} and S_{11} of series combining transformer with and without X-shape shielding.

In Fig. 28, S_{11} is forward reflection coefficient at the differential input port of primary loop and S_{21} is forward transmission coefficient from primary to only one secondary loop. The insertion loss of transformer with X-shielding is around 1.4 dB at 60 GHz, exhibiting 0.2 dB higher than the case without it. The

1dB bandwidth of S_{21} covers 40 GHz to 80 GHz regardless shielding conditions. With X-shielding, the turn ratio is boosted from 4.36 to 5.03 at 60 GHz.

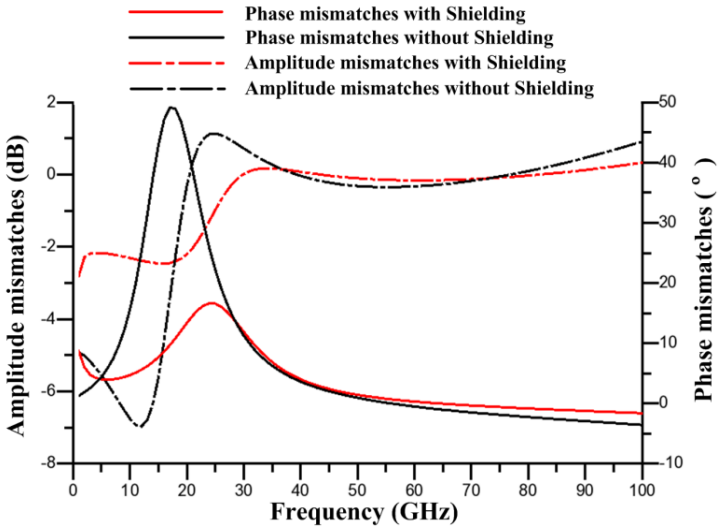


Fig. 29 Amplitude and phase differences with and without X-shape Shielding.

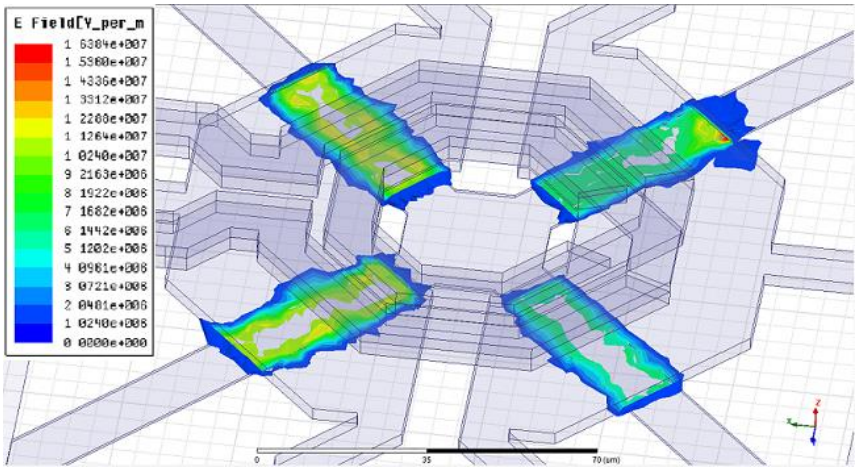


Fig. 30 E-field between secondary loops and the X-shape ground shielding in series combining transformer.

Amplitude and phase differences represent the variations of wave transition between the primary and two secondary loops. In Fig. 29, it can be found that X-shape shielding effectively reduces phase and amplitude

differences in the whole frequency domain. It mainly attributes to providing a common ground reference in the center of this transformer as illustrated in Fig. 30. With the help of the special shielding, phase differences are less than ±1 degree at 53 - 84 GHz and amplitude differences are controlled to be less than 0.15 dB at 31GHz – 91 GHz.

2.8 Measurement Results of CMOS PA with Series Combining Transformer

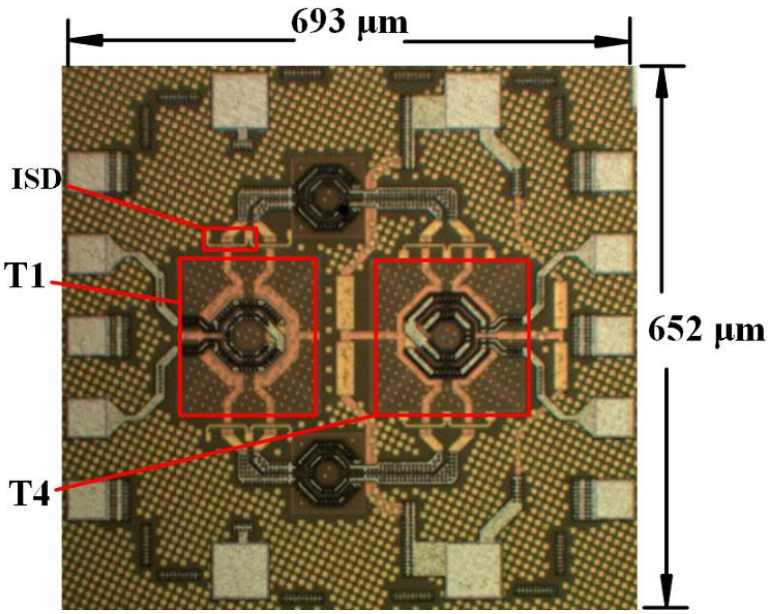


Fig. 31 Photograph of series combining mm-wave PA with ISD in 65 nm CMOS.

This mm-wave PA with series splitting/combining transformer was fabricated in GF's 65 nm LP CMOS technology. All MOSFETs integrated inside are 2.6 nm thin-oxide devices. With transistors' V_t around 0.55 V, the

supply voltages of this PA are set to be 0.8 V V_g and 1.2 V V_d. Fig. 31 shows the photograph of the overall transformer coupled PA using ISD technique. Including two sets of GSGSG I/O pads and four power supply pads, the entire chip only consumes 693×652 μm^2 in area, while the dimension of T_1 and T_4 is about 160×150 μm^2. ISD are compactly implemented in both drive and final stages. The performances of the PA were characterized by Microtech Elite 300 probe station and Agilent PNA-X that can test differential circuits up to 67 GHz. The instruments were de-embedded by open-through calibration methods and the PA is terminated with 100 Ω differential source and load.

In Fig. 32, the data of S-parameter measurement basically agrees well with simulation with a little frequency shifting. The gain of this two-stage PA is above 10 dB from 41 GHz to 61 GHz (40% bandwidth). S_{11} and S_{22} also indicate that the I/O ports are wideband matched. At 60 GHz, this PA achieves 11.3 dB gain, about 2.1 dB lower than simulation. In practical chip implementation, there are three main aspects which cause the differences between measurement and simulation results. First of all, CMOS transistor modelling is an approximation of the physical devices as described by process data sheet, which inevitably introduces certain deviations. The accuracy of passive device EM modelling is also constrained by commercial simulators. Secondly, additional transmission lines connecting transformers T_1 or T_4 to PA I/O would incur extra loss and signal phase shifts. Finally, the I/O pad configuration induces parasitic capacitance which is proportional to the pad

area. Therefore, the parasitic capacitance would shift the S-parameters curves towards lower frequencies. But even in the presence of the above non-ideal design aspects, the measured curves are only shifted by 8 % in frequency which demonstrates the robustness of the proposed PA techniques.

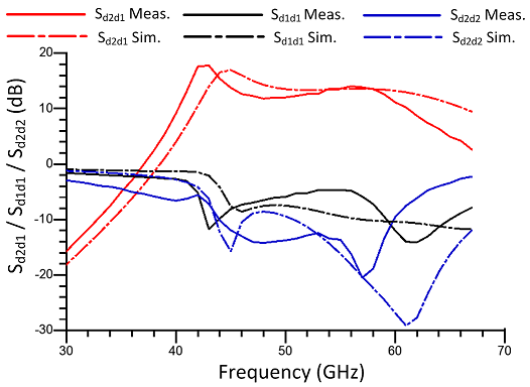


Fig. 32 Measured and simulated S-parameter under 0.8 V V_g and 1.2V V_d

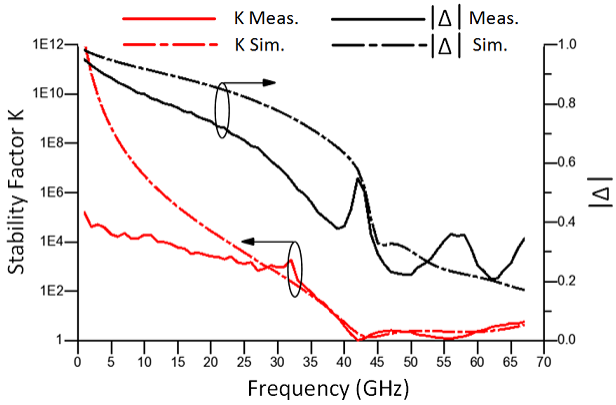


Fig. 33 Stability factor K and $|\Delta|=|S_{11}S_{22}-S_{12}S_{21}|$.

In Fig. 33, the PA is unconditional stable for satisfying conditions of $K>1$ and $|\Delta|<1$. The series combining transformers largely suppress wave propagations below 40 GHz and hence guarantee stability. At higher frequencies, transistors were stabilized by the proposed ISD technique.

The *CMRR* can be calculated by Equation (2.70) from four-port S-parameter measurement results. Fig. 34 demonstrates that the measured and simulated *CMRR*. The designed PA achieved *CMRR* better than 26 dB at 41 - 61 GHz.

$$CMRR = 20\log_{10}\left(\frac{\left|S_{21}+S_{43}-S_{23}-S_{41}\right|}{\left|S_{21}+S_{43}+S_{23}+S_{41}\right|}\right) \tag{2.70}$$

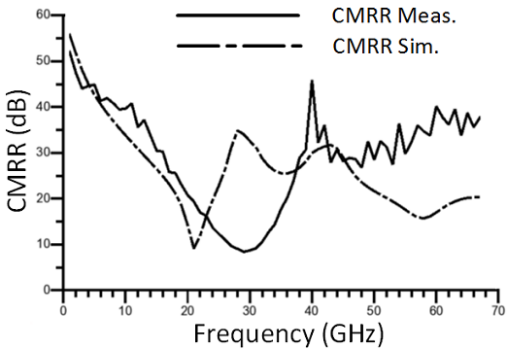
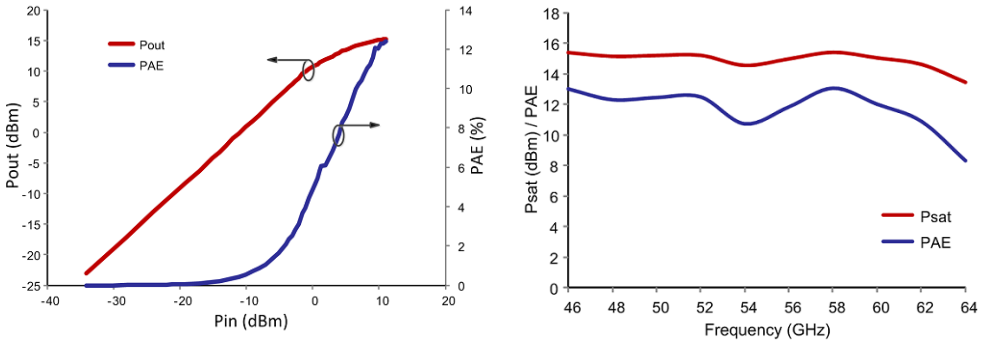


Fig. 34 Simulation and measurement results of *CMRR*.

The large signal test results are illustrated in Fig. 35. At 60 GHz, the output referred 1dB compression point is 11.9 dBm and it can deliver 15.2 dBm P_{sat} with peak *PAE* of 12.4%. At other frequency points, the PA achieves its maximum output power 15.4 dBm at 46 GHz and 58 GHz with 13.0% *PAE*.

In Table III, this V-band common sourced PA draws high gain from per-stage among the state-of-the-art which indicates that CMOS transformer with ISD can ease matching and enhance stable gain level. Compared to PAs with output power above 15 dBm, this chip is of high *PAE* and maintains a very compact size.



(a) (b)

Fig. 35 (a) P_{out} and *PAE* versus P_{in} at 60 GHz; (b)P_{out} and *PAE* from 46 GHz to 64 GHz.

Table III

COMPARISON OF MILLIMETER WAVE CMOS PAS

Ref.	CMOS Tech.	Freq. (GHz)	Area (mm^2)	Gain (dB)	Gain Per-stage @60GHz(dB)	P_{1dB} (dBm)	P_{sat} (dBm)	*PAE*	Topology
[90]	65 nm LP	44-60	0.39*	8.3	4.15	9.7	11	7.1	2-stage CS
[91]	65 nm LP	53-68	0.462	15.5	7.8	11.5	18.1	3.6	2-stage CC
[78]	65 nm GP	58-65	0.053	15.8	5.3	2.5	11.5	11	3-stage CS
[42]	90 nm NA	58-66	0.15	15	5.0	10.2	12.5	19.3	3-stage CS
[68]	65 nm LP	58-64	2.25*	20	5.0	13.5	15.6	6.6	4-stage CS
[92]	65 nm GP	53-73	0.268	13.2	4.4	13.0	13.4	8.7	3-stage CS
[93]	65 nm GP	56-63	0.357*	9.4	4.7	13.7	14.9	16.2	3-stage CS
[89]	65 nm GP	58-64	0.366*	14.9	5.0	10.7	11.3	9.4	3-stage CS+CC
[94]	45 nm LP	50-67	0.384*	6.0	3.0	11.0	13.8	7.0	2-stage PP
[95]	65 nm GP	56-62	1.20*	20	4.0	12.5	16	6.6	5-stage CS
This PA	**65 nm LP**	**41-61**	**0.250 0.449***	**11.3**	**5.6**	**11.9**	**15.2**	**12.4**	**2-stage CS**

*: Area of pads included; CS: common source; CC: cascode, PP: push pull;

In summary of this PA, transistor based ISD configuration is proposed in design of CS CMOS PA for mm-wave band applications. The method of realizing high *Q* inductor in the source of CMOS transistor is presented. In advance of solving its circuit topology, the theorem of admittance matrix condensation for port-to-port analysis is derived. This algorithm is then conveniently applied in characterizing the linear model of the active device part.

To choose the optimal source inductances for better stability, *MSG* and linearity, the above results are then synthetically considered with nonlinearity analysis. In passive device design, 2-way series combining transformer is investigated by lumped element model when both capacitive and inductive coupling are taken into account. By applying X-shape pattern ground shielding in transformer, the phase and amplitude differences are diminished. Moreover, the turn ratio of primary to secondary loops can be further enlarged. Finally, an mm-wave PA using the proposed ISD technique and series combining transformer is implemented in 65 nm LP CMOS. At 41 - 61 GHz, its measured differential drive gain is above 10 dB while the *CMRR* is more than 26 dB. At 60 GHz, this differential PA demonstrates high gain from each stage at V-band. The P_{1dB} and P_{sat} achieve 11.9 dBm and 15.2 dBm respectively with 12.4% peak *PAE*.

Chapter 3: Hybrid Power Combination in CMOS

3.1 High Performance CMOS PA Design Considerations

The design of class A power amplifier needs to take account a series of tradeoffs for high overall performances. In particular, PA specifications including gain, bandwidth, chip size, output power and efficiency etc. have been the primary concerns. In a practical PA design, these targets would actually affect each other and their relationship can be summarized in Fig 36.

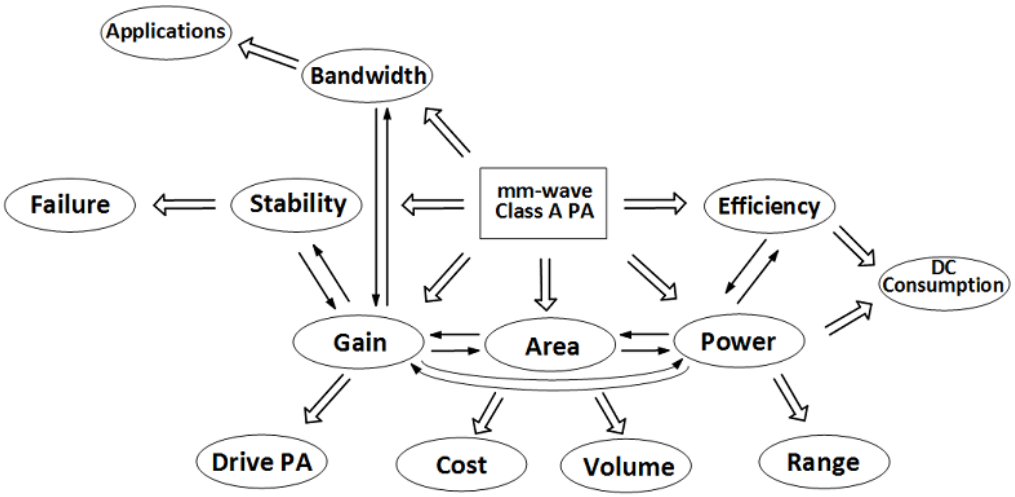


Fig. 36 Design considerations of class A mm-wave PA with high performances.

As wave propagation in air is of high attenuation at V band, higher output power would be helpful for increasing the radio range of transmitter**.** However, the design target of high output power may limit PA efficiency and need more chip area for combiner integration. It is because higher output power level

basically requires more transistor gate-width size. There are two solutions for handling transistors with large total gate-width. One solution is to increase the number of transistor unit but each one of less gate-width. This method would complicate the configuration of power combiner. As a result, the combiner would become bulkier. For example, the final stage of power amplifier reported in [96] consists of thirty-two transistor units. Generally, eight and sixteen transistor units are easier to be realized [44][97]. Another solution is to employ less transistor unit but each one with larger gate-width size. Although the passive matching topologies can be simplified in this way, it is hard to maintain gain level and power added efficiency. In PA applications, both power and efficiency are crucial for the total dc power consumption. Therefore, the output power is directly related to the trade-offs among transistor unit design, dc consumption, chip area, efficiency, final-stage gain and radio range.

For large output PA, high total gain also becomes another important specification. If the input power from mixer or VGA is insufficient, large output power cannot be obtained in the designed PA without additional drive [98]. In order to increase the gain level of PA in GP or LP CMOS with low breakdown gate voltage, cascading is the most practical way. However, more chip space is required by cascading more stages which also complicates the PA architecture. Therefore, both large power and high gain put pressure on design of passive matching circuit in valuable chip area. For semiconductor ICs, its fabrication volume and cost are mainly subject to chip area.

In high gain condition, the PA stability should be taken care as the potential oscillation risk may cause chip failure. In the previous section, the amplifier stability at operating band has been improved by ISD technique. Another difficulty in high gain PA design is to offer gain flatness within wide bandwidth as a number of passive and active devices would be cascaded. Therefore, all those mutual constraints should be concerned for making an mm-wave class A PA with high overall performances.

3.2 High Performance PA Solutions and Architecture

To realize outstanding overall performances, several techniques are proposed in a compact, high gain, large power and wideband CMOS PA design. In Fig. 37, the architecture of differential V-band CMOS PA is illustrated. In this design, a four stage CS amplification scheme is adopted to achieve high total gain level. The input and output placement of UA1 (or UA2) and UA4 are in the opposite directions vertically. On the whole, all components including UAs and matching components form a loop-like configuration to fully use available area. In this way, the space utilization between the left and right side are well balanced. If all UAs are horizontally placed in the same direction, the overall circuit layout is prone to resembling a triangular-like shape in layout [99]-[101]. Isolation region for decoupling amplification stages at the left and right sides is provided in the center of this configuration.

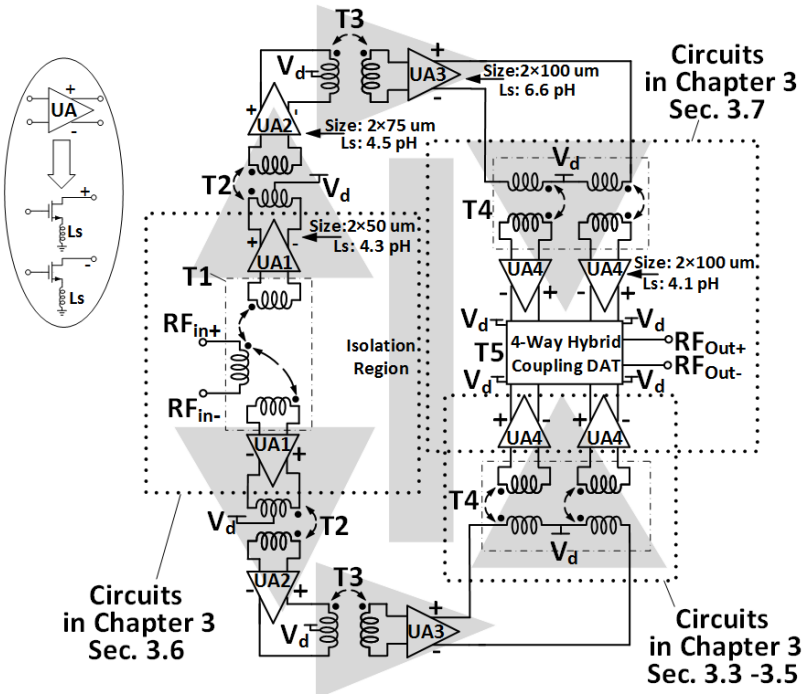


Fig. 37 The proposed architecture of differential V-band transformer-based CMOS PA.

Table IV

UA PARAMETERS W/ AND W/O ISD AT 60 GHZ

		Without ISD		With ISD		
Stage	Device Size (um)	*MSG* (dB)	μ	Inductance (pH)	*MSG* (dB)	μ
UA1	50×2	10.5	0.74	4.3	10.5	0.86
UA2	75×2	10.2	0.65	4.5	10.4	0.79
UA3	100×2	10.1	0.57	6.6	10.4	0.77
UA4	100×2	10.1	0.57	4.1	10.3	0.69

μ: Edwards's stability parameter.

For stability and bandwidth consideration, CMOS transistor with ISD would be investigated with matching transformers. Within each stage, the active devices consist of ISD-embedded 65 nm CMOS transistors operating in pseudo-differential mode. Table IV demonstrates the design parameters of UAs

with and without ISD technique. It indicates that the stable region in Γ_L plane is enlarged by ISD while the potential stable gain level of active device is maintained or slightly boosted as discussed.

In the passive device design, all matching networks are realized by transformer configurations for compact size. It is because transformer can accomplish impedance matching, interconnection and power distribution simultaneously. These transformers are sequenced from T1 to T5 in Fig. 37. In the first stage, the differential input signal is divided by a parallel transformer. Then 1:1 transformers are implemented for inter-stage matching between UA1s, UA2s and UA3s. Next, four UA4 blocks are driven by two UA3s with the aid of series power splitters. In the final stage, a novel 4-way hybrid combining transformer is used for generating high output power.

Among these transformers, T1 and T4 also divide power from one input to two outputs by parallel and series splitting respectively. In the final stage, T5 is responsible for combining output power from all unit amplifiers to the external load. By the above arrangement, T1, T4 and T5 function as matching and power division / combination networks simultaneously for size reduction. For the sake of compressing the size of passive components as much as possible, concentric winding method would be proposed in design of differential 2-way parallel splitting transformer and 4-way hybrid combining transformer. By using this innovative winding technique, it gives a better tradeoff to integrate more drive stages. Therefore, the goals of high gain, high power and compact

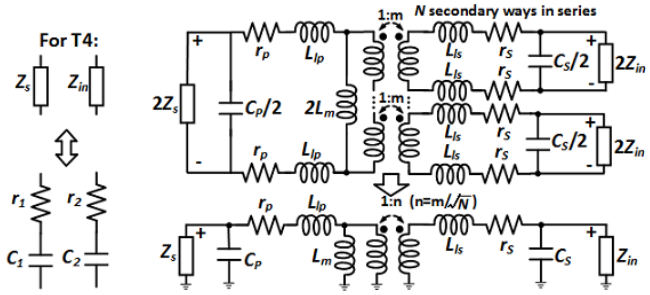
size can be achieved simultaneously. Moreover, the implementation strategies of hybrid combining transformer would be acquired by analyzing its coupling effect. When the combiner is connected with active device, the nonlinear behaviors are also studied.

In power supply design, all drain bias V_d is fed through the virtual ground points of transformers and no bulky RF choke circuit is added. The gate bias V_g of transistors is fed through large resistors for simplifying transformer structures.

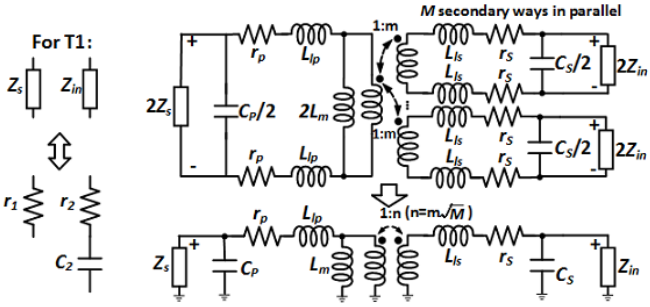
In the following sections of this chapter, this PA would be detailed according to the sequences denoted in Fig. 37.

3.3 Stability Analysis of ISD-Embedded CMOS Transistor and Input Matching Transformer

In architecture design, parallel splitter T1 and series splitter T4 are with one input and two output ports. In these two transformer modeling, the distributed parasitic capacitances can be simplified by C_p and C_s instead [12][42]. Such differential transformers with multiple ports are hard to be analyzed with the active device. To make T1 and T4 analyzable, their equivalent single-ended modeling method is illustrated in Fig. 38 when parameter deviations between ports in series / parallel are not the key concern.



(a)



(b)

Fig. 38 (a) Transformation from multi-port in series differential connection to equivalent single-ended model; (b) Transformation from multi-port in parallel differential connection to equivalent single-ended model.

In this simplified series and parallel transformer model, $2Z_S$ can either represent the differential output impedance of the drive stage in Fig. 38 (a) or the external source impedance in Fig. 38 (b). Z_{in} in this model is the input impedance of the next stage. $2L_m$, $2L_{lp}$ and $2L_{ls}$ demonstrate the mutual coupling inductance, primary winding leakage inductance and secondary winding leakage inductance of the transformer. $2r_p$ / $2r_s$ and $0.5C_p$ / $0.5C_s$ are the parasitic winding resistor and capacitor. In the equivalent single-ended model, the coupled primary and secondary loops should not change the original *I-V* relationship as it is in the differential model. In series transformer, the

secondary N loops would divide the voltage level coupled from the primary loop. In parallel transformer, the coupled current from the primary loop is shared by the secondary ones. These two relationships would be reflected by turn ratio 1:n after single-ended conversion. For reducing the number of secondary ports, the turn ratio can be alternatively represented by $m/\sqrt{N}$ for series transformer and $m\sqrt{M}$ for parallel type. The parasitic capacitances and mutual inductances are then modeled as C_p, C_s and L_m instead.

By the above transformation, the characteristics of both active device and multi-port transformer can be considered together by their equivalent single-ended model. As an example of stability and matching analysis when both active device and passive transformer are taken into account, the unit amplifier of the final stage UA4 are investigated with series transformer T4 in Fig. 39.

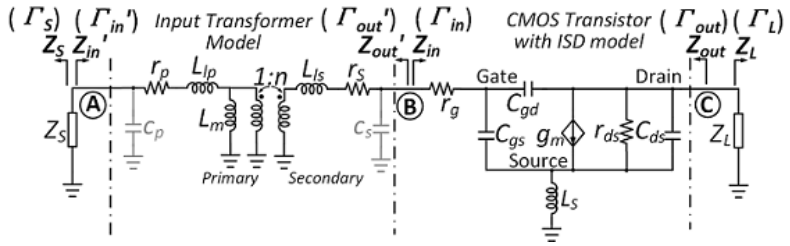


Fig. 39 Lumped-element model of input transformer with Transistor-based ISD (Transistor-based ISD model: L_S=4.1 pH, r_g=2.8 Ω, C_{gs}=65.8 fF, C_{gd}=25.6 fF, C_{ds}=28.8 fF, g_m=0.096 S, r_{ds}= 60.7 Ω; Input transformer model: r_1=8.0 Ω, C_1 =159.0 fF, L_m=17.2 pH, L_{lp}=8.0 pH, L_{ls}=15.1 pH, Cp=63.6 fF, C_S=45.6 fF, m= 1.13, n= 0.8, r_P=1.0 Ω and r_S=1.0 Ω)

For the active device part, the Z parameters of the CMOS transistor with ISD is derived as

$$Z_{BC} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} =$$

$$\begin{bmatrix} \dfrac{\dfrac{1}{sC_{gs}}\left(\dfrac{1}{sC_{gd}} + r_{ds} \| \dfrac{1}{sC_{ds}}\right)}{\Delta} + r_g + sL_S & \dfrac{\dfrac{1}{sC_{gs}}\left(r_{ds} \| \dfrac{1}{sC_{ds}}\right)}{\Delta} + sL_S \\ \dfrac{\left(r_{ds} \| \dfrac{1}{sC_{ds}}\right)\left(\dfrac{1}{sC_{gs}} - g_m \dfrac{1}{s^2 C_{gs} C_{gd}}\right)}{\Delta} + sL_S & \dfrac{\left(r_{ds} \| \dfrac{1}{sC_{ds}}\right)\left(\dfrac{1}{sC_{gs}} + \dfrac{1}{sC_{gd}}\right)}{\Delta} + sL_S \end{bmatrix} \tag{3.1}$$

$$\Delta = g_m \frac{1}{s^2 C_{gs} C_{gd}} + \frac{1}{sC_{gs}} + \frac{1}{sC_{gd}} + \left(r_{ds} \| \frac{1}{sC_{ds}}\right) \tag{3.2}$$

$$s = jw = j2\pi f \tag{3.3}$$

When the active device is connected with passive matching networks and load impedance, Γ parameters can easily represent all the possible impedances seen at Fig. 39's B and C nodes as

$$Z_{in} = Z_{11} - \frac{Z_{12} Z_{21}}{Z_{22} + Z_0 \left[(1+\Gamma_L)/(1-\Gamma_L)\right]} \tag{3.4}$$

$$Z_{out} = Z_{22} - \frac{Z_{12} Z_{21}}{Z_{11} + Z_0 \left[(1+\Gamma_{out}')/(1-\Gamma_{out}')\right]} \tag{3.5}$$

$\mathrm{Re}(Z_{in})>=0$ and $\mathrm{Re}(Z_{out})>=0$ are another straightforward criterion for conditional stability judgment derived from [82]. The two-port network is stable in the condition that input and output impedance remain positive with a passive termination. When $\mathrm{Re}(Z_{in})\geq 0$ and $\mathrm{Re}(Z_{out})\geqslant 0$ are satisfied for all $|\Gamma_L|<1$ and $|\Gamma_S|<1$, this criteria becomes unconditional stability condition.

By (3.4) and (3.5), Z_{in} and Z_{out} normalized with Z_0 can either be directly contoured in smith chart or plotted by converting them to reflection coefficients

Γ_{in} and Γ_{out}. In this PA design, 100 μm gate-width CMOS transistors with 4.1 pH L_S are applied in the final stage. The input / output coefficients Γ_{in} / Γ_{out} of this device are plotted by Fig. 40 in the condition of $|\Gamma_L| \rightarrow 1$ / $|\Gamma_{out}'| \rightarrow 1$. Comparing the circles with and without ISD, Γ_{in} and Γ_{out} are shifted towards the inside of $|\Gamma_{in}|=1$ and $|\Gamma_{out}|=1$ region by ISD at 51 GHz and 60 GHz. In view of input and output impedances, ISD stabilizes CMOS transistor by increasing their real parts. If L_S are further increased to 12.0 pH, all $|\Gamma_{in}|$ and $|\Gamma_{out}|$ are shifted inside the unit magnitude region and the device becomes absolute stable at 60 GHz. The transistor integrated is not fully stabilized by ISD for keeping a relative high maximum available gain.

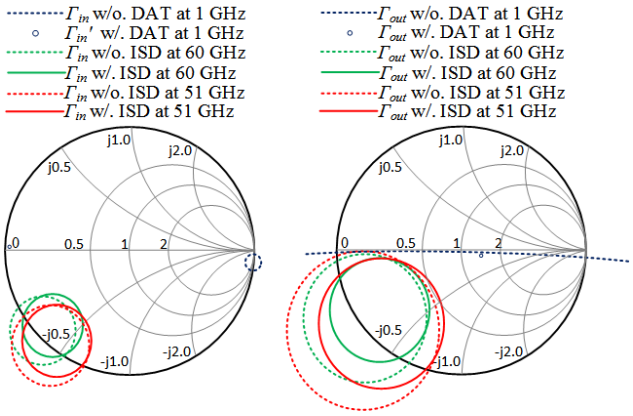


Fig. 40 (a) Z_{in} region with /without ISD at 53 GHz and 60 GHz; Z_{in} / Z_{in}' region without / with input transformer at 1 GHz. (b) Z_{out} region with / without ISD at 1 GHz, 53 GHz and 60 GHz; Z_{out} region with / without input transformer at 1 GHz.

At 1 GHz, ISD almost does not move Z_{in} and Z_{out} circles since slab inductor is a frequency dependent device. With series transformer T4 matched

to the input of ISD-embedded transistor, Z_{in}' and Z_{out}' in Fig. 39's model are expressed as

$$Z_{in}' = \frac{1}{sC_p} \left\| \left(r_p + sL_{lp} + sL_m \left\| \left(\frac{1}{n^2} \left(sL_{ls} + r_s + \frac{1}{sC_s} \| Z_{in} \right) \right) \right) \right. \tag{3.6}$$

$$Z_{out}' = \frac{1}{sC_s} \left\| \left(r_s + sL_{ls} + n^2 \left(sL_m \left\| \left(sL_{lp} + r_p + \frac{1}{sC_p} \| Z_S \right) \right) \right) \right. \tag{3.7}$$

For low frequencies away from operating band, the combination of mutual inductance L_m, parasitic resistor r_p and r_s play key roles in transistor stabilization as illustrated in Fig. 41.

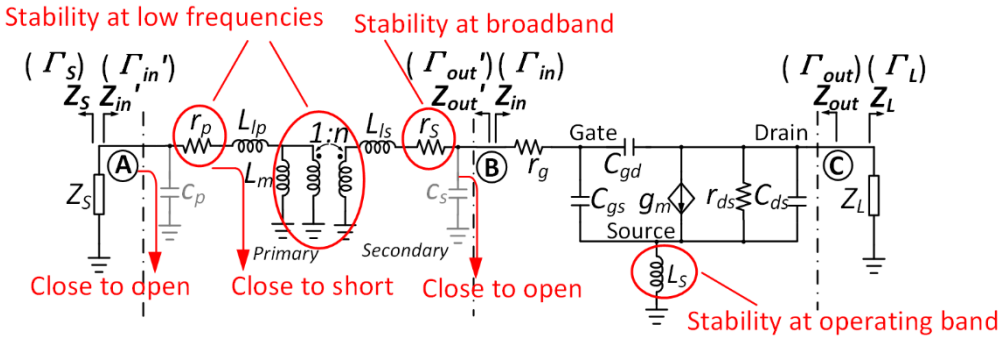


Fig. 41 Transformer in response to signal excitation at different wave band.

In matching design at mm-wave band, the function of L_m in T4 is to resonate out paralleled capacitive components in signal transition path to ground. At low frequencies such as 1 GHz, capacitances C_p and C_s are close to open while L_m, L_{lp} and L_{ls} are close to short in response to a small s. Since L_m is in parallel with input impedance seen by secondary loops, Z_{in}' would be of a rather low magnitude regardless Z_{in}. When f is varied from 60 GHz to 1 GHz, r_p

would become a dominant item in Z_{in}' as sL_m is diminished by 60 times. As a result, even a small series resistor r_P may contribute a positive real part for Z_{in}'. Contouring $|Z_{in}|$ and $|Z_{out}'|$ in the condition of $|\Gamma_L| \rightarrow 1$ and $|\Gamma_S| \rightarrow 1$ with different phases, their regions are shrunk to the tiny dotted area with positive real part in smith chart as demonstrated in Fig. 40. Therefore, the instability of active device at low frequencies is secured by parasitic series resistor of matching transformer. The parasitic resistor r_s of the secondary loop is directly connected with the input of the active device. It is capable of stabilizing active device within wide bandwidth.

In Fig. 42, the stability factor is plotted in the condition of active device with / without ISD and input matching transformer. With input matching transformer T4, the active device become absolute stable at low frequencies. Below 33 GHz, the K value of the combined configuration is more than 5. Thanks to ISD technique and input transformer, the overall two-port network is absolute stable at almost all the frequencies interested. Even the lowest K value point (0.97 at 63 GHz) is rather close to 1.

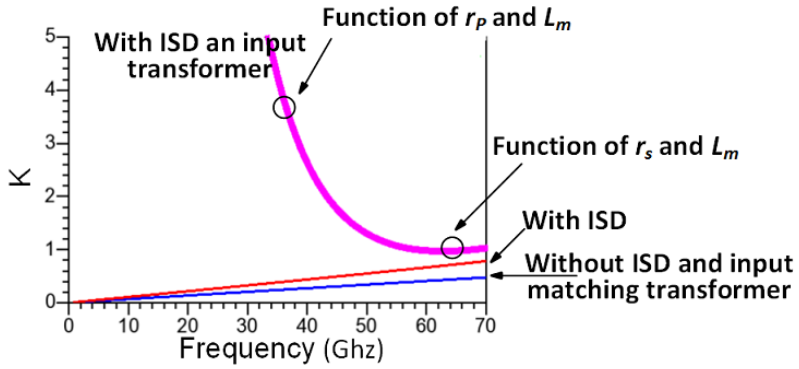


Fig. 42 Stability factor K with /without ISD and input matching transformer.

3.4 Bandwidth Analysis of CMOS Transistor with ISD

The bandwidth of mm-wave PA is related to both active device matching and signal transition in passive components. In [102][103], the discussion is mainly about the transformer design part. As a matter of fact, the impact of active device to amplifier bandwidth should also considered. To characterize the active device matching by external passive device, the quality factor of the input and output impedance is defined by the imaginary part over its real part for bandwidth analysis.

$$Q_{in} = \frac{Im(Z_{in})}{Re(Z_{in})} \tag{3.8}$$

$$Q_{out} = \frac{Im(Z_{out})}{Re(Z_{out})} \tag{3.9}$$

It is noticeable that the concept of Q_{in} and Q_{out} are different from quality factor Q for inductor winding. The definition of Q is to estimate the ratio of winding inductance to parasitic resistance. In this analysis, Q_{in} and Q_{out} only care about the characteristics at I/O port seen from B and C nodes in Fig. 41. The Q_{in} values of LP CMOS transistor with 50 μm, 100 μm and 200 μm gate-width are demonstrated in Fig. 43. For the final stage design, the Q_{in} is also compared in the case of 100 μm transistor with / without ISD. Another stabilization technique called neutralization capacitor reported in [78] is also in

comparison. This technique needs cross connected capacitors between differential input and output. In Fig. 43, ISD and neutralization capacitor techniques are compared in the condition of achieving same stability factor.

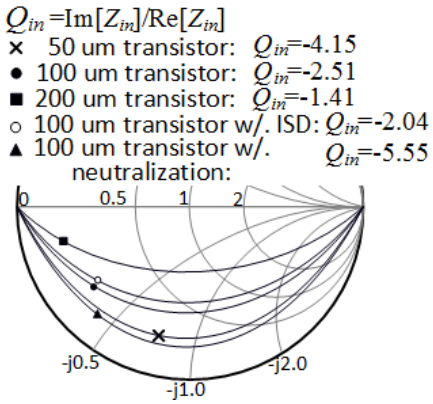


Fig. 43 Q_{in} of transistor with 50 μm, 100 μm and 200 μm gate width, Q_{in} of 100 μm transistor with ISD, Q_{in} of 100 μm transistor with neutralization.

If additional stabilization method has not been introduced into transistors, the total gate-width of unit amplifier is a significant parameter determining Q_{in}. CMOS Transistor with 50 μm gate-width demonstrates the highest $|Q_{in}|$. As the transistor size increases, the $|Q_{in}|$ would be decreased as well. When the LP CMOS transistor is enlarged to 200 μm, the $|Q_{in}|$ would be as low as 1.41.

The different stabilization technique is then compared in the condition of transistor size fixed. For 100 μm gate-width transistor, ISD decreases $|Q_{in}|$ from 2.51 to 2.04 by increasing $Re(Z_{in})$ and slightly reducing $|Im(Z_{in})|$. Consequently, passive matching networks with lower $|Q_{out}'|$ would also be applicable. When neutralization capacitors are used, the $|Q_{in}|$ would be as high as 5.55. Correspondingly, the external components connected to the input of active

device should possess higher $|Q_{out}'|$ in ideal matching. For matching active device at the output, the conclusions are similar the above. The results of $|Q_{out}|$ are not shown for figure clarity.

Since Z_{out}' of the passive networks should exhibit inductive for matching the capacitive active device, forward transmission loss would be induced at frequencies deviating the optimally matched point. Consequently, the bandwidth may be limited. When transformer insertion loss is not considered, the external matching components presented to active device input can be simply viewed as a series or parallel matching topology. In Fig. 44, the active device is demonstrated by capacitor C_{in} in series with resistor R_{in}. In reference to node B in Fig. 39, external inductance in parallel or series with source resistance represents input matching networks for active device.

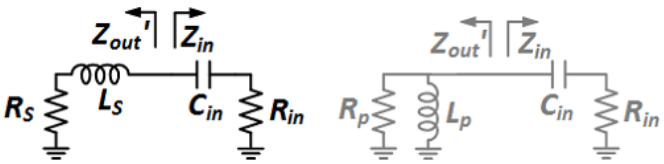


Fig. 44 Simplified active device input matching by external inductance in parallel or series with source resistance.

The forward transmission coefficients T_s and T_p corresponding to external series and parallel matching topology are define as

$$T_S = 20\log\left(\sqrt{1-\left|\frac{R_{in}+1/sC_{in}-R_S-sL_S}{R_{in}+1/sC_{in}+R_S+sL_S}\right|^2}\right) \tag{3.10}$$

$$T_P = 20\log\left(\sqrt{1-\left|\frac{R_{in}+1/sC_{in}-R_p sL_p/\left(R_p+sL_p\right)}{R_{in}+1/sC_{in}+R_p sL_p/\left(R_p+sL_p\right)}\right|^2}\right) \tag{3.11}$$

To satisfy conjugate matching at the specific frequency f_0, the desired R_s, L_s, R_p and L_p presented by passive matching networks are found to be

$$s_0 = j2\pi f_0 \tag{3.12}$$

$$|Q_{in}| = \frac{1}{|s_0| C_{in} R_{in}} \tag{3.13}$$

$$R_s = R_{in} \tag{3.14}$$

$$L_s = \frac{1}{|s_0|^2 C_{in}} = R_{in}\frac{|Q_{in}|}{|s_0|} \tag{3.15}$$

$$R_p = \frac{1}{Re\left[s_0 C_{in}/\left(R_{in}s_0 C_{in}-1\right)\right]} = \frac{1+R_{in}^{\ 2}C_{in}^{\ 2}|s_0|^2}{R_{in}C_{in}^{\ 2}|s_0|^2} = R_{in}\left(1+|Q_{in}|^2\right) \tag{3.16}$$

$$L_p = -\frac{1}{sIm\left[s_0 C_{in}/\left(R_{in}s_0 C_{in}-1\right)\right]} = \frac{1+R_{in}^{\ 2}C_{in}^{\ 2}|s_0|^2}{|s_0|^2 C_{in}} = L_s\left(1+\frac{1}{|Q_{in}|^2}\right) = R_{in}\frac{|Q_{in}|}{|s_0|}\left(1+\frac{1}{|Q_{in}|^2}\right)$$

(3.17)

Using the results of (3.12) to (3.17) to express forward transmission coefficients, T_s and T_p become the function of just s and $|Q_{in}|$ as follow

$$T_S = 20\log\left(\sqrt{1-\left|\frac{|Q_{in}|\left(|s_0|^2-s^2\right)}{|Q_{in}|\left(|s_0|^2+s^2\right)+2ss_0}\right|^2}\right) \tag{3.18}$$

$$T_P = 20\log\left(\sqrt{1-\left|\frac{2|Q_{in}|ss_0 + s^2\left(1-|Q_{in}|-|Q_{in}|^3\right)+s_0{}^2|Q_{in}|^2}{2|Q_{in}|ss_0 + s^2\left(1+|Q_{in}|+|Q_{in}|^3\right)+s_0{}^2|Q_{in}|^2}\right|^2}\right) \tag{3.19}$$

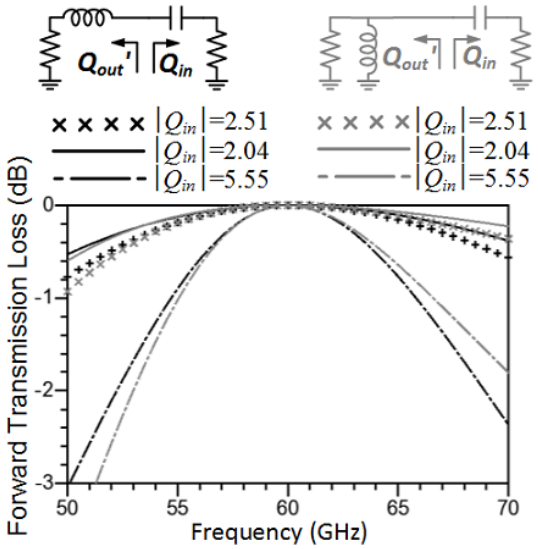


Fig. 45 Forward transmission coefficients T_s and T_p.

In Fig. 45, the results of (3.18) and (3.19) with different $|Q_{in}|$ are plotted. At the whole frequency range, the curve flatness of forward transmission coefficient is ameliorated after ISD is introduced into 100 μm gate-width CMOS transistor. Compared with capacitive neutralization achieving the same stability, ISD technique provides less forward transmission loss at frequencies deviating the optimal matching point. In another word, less gain unevenness would be induced at the input of active device.

3.5 Matching Analysis of Transformer and Active Device

The gain level obtained from active device matched by transformer is mainly subject to two design aspects. On the one hand, impedance matching between transformer and CMOS transistor with ISD largely decides how much gain can be available. On the other hand, the signal transition in passive device and transmission loss at the input of active device cause gain degradation. When both aspects are considered, the matching can also be investigated by the model in Fig. 39. The *Z* parameters between A-B nodes are derived as

$$Z_{AB} = \begin{bmatrix} Z_{11}' & Z_{12}' \\ Z_{21}' & Z_{22}' \end{bmatrix} \tag{3.20}$$

$$Z_{11}' = \frac{1}{sC_p\Delta'}\left\{sL_m\left[n^2\left(r_p + sL_{lp}\right) + r_s + sL_{ls} + \frac{1}{sC_s}\right] + \left(r_p + sL_{lp}\right)\left(\frac{1}{sC_s} + r_s + sL_{ls}\right)\right\} \tag{3.21}$$

$$Z_{12}' = Z_{21}' = \frac{nL_m}{sC_pC_s\Delta'} \tag{3.22}$$

$$Z_{22}' = \frac{1}{sC_s\Delta'}\left\{sL_m\left[n^2\left(r_p + sL_{lp}\right) + r_s + sL_{ls} + \frac{n^2}{sC_p}\right] + \left(r_s + sL_{ls}\right)\left(\frac{1}{sC_p} + r_p + sL_{lp}\right)\right\} \tag{3.23}$$

$$\Delta' = sL_m\left[n^2\left(r_p + sL_{lp}\right) + r_s + sL_{ls} + \frac{n^2}{sC_p} + \frac{1}{sC_s}\right] + \left(r_s + sL_{ls} + \frac{1}{sC_s}\right)\left[n^2\left(r_p + sL_{lp}\right) + \frac{n^2}{sC_p}\right]$$

(3.24)

In the condition of transformer connected to the input of CMOS transistor with ISD, the extractable gain level is mainly decided by transformer output

matching impedance Z_{out}'. Z_{out}' can be conveniently calculated by applying the elements in (3.20) into the equation below.

$$Z_{out}' = Z_{22}' - \frac{Z_{12}' Z_{21}'}{Z_{11}' + Z_S} \tag{3.25}$$

The Z_{out}' presented by T4 from 1 GHz to 67 GHz is demonstrated in Fig. 46. It is designed inside various equal gain circles at 51 GHz, 60 GHz and 67 GHz. Due to transistor gain's roll-off effect, it is easier to extract higher gain at low frequencies. For this design, the active device may offer higher gain at 51 GHz if it is ideally matched. This potential gain unevenness should be compensated by the aforementioned forward transmission loss and signal transition loss of transformer.

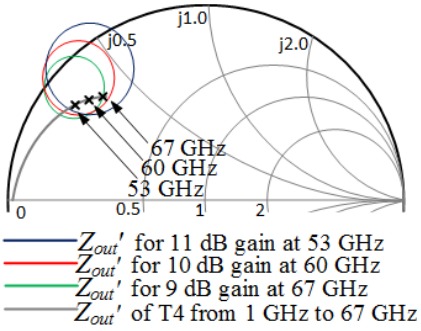


Fig. 46 Available gain circles of UA4 at 51 GHz, 60 GHz and 67 GHz; Z_{out}' curve presented by T4 from 1 GHz to 70 GHz.

In (3.26), the *Z* parameters between A-C planes in Fig. 39 are derived so as to calculate the gain level after compensation.

$$Z_{AC}=\begin{bmatrix} Z_{C11} & Z_{C12} \\ Z_{C21} & Z_{C22} \end{bmatrix}=\begin{bmatrix} Z_{11}'-\dfrac{Z_{12}'Z_{21}'}{Z_{11}+Z_{22}'} & \dfrac{Z_{12}Z_{12}'}{Z_{11}+Z_{22}'} \\ \dfrac{Z_{21}Z_{21}'}{Z_{11}+Z_{22}'} & Z_{22}-\dfrac{Z_{12}Z_{21}}{Z_{11}+Z_{22}'} \end{bmatrix} \tag{3.26}$$

Then the transducer gain G_T, operation gain G_P and available gain G_A for this two-port network are particularly derived to characterize transformer matching to CMOS transistor with ISD. The relationship between Z parameters and circuit topology is illustrated in Fig 47.

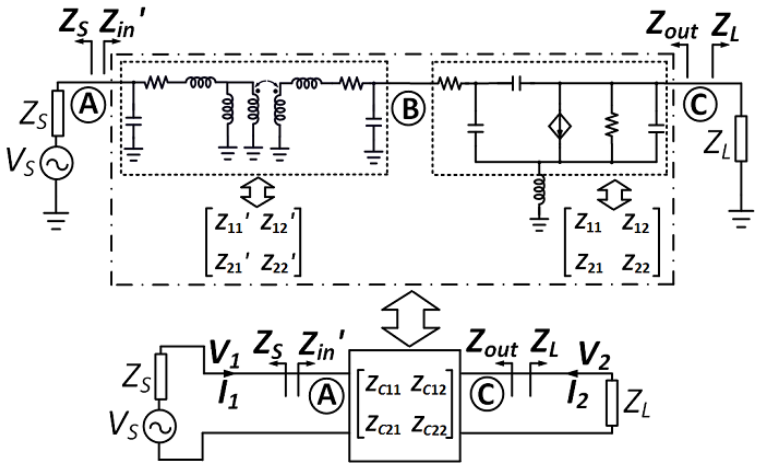


Fig. 47 The relationship between Z parameters and circuit topology.

The V_1, V_2, I_1 and I_2 in Fig. 47 are solved to be

$$V_1=Vs\frac{Z_{C11}(Z_L+Z_{C22})-Z_{C12}Z_{C21}}{(Z_S+Z_{C11})(Z_L+Z_{C22})-Z_{C12}Z_{C21}} \tag{3.27}$$

$$V_2=Vs\frac{Z_LZ_{C21}}{(Z_S+Z_{C11})(Z_L+Z_{C22})-Z_{C12}Z_{C21}} \tag{3.28}$$

$$I_1=Vs\frac{Z_L+Z_{C22}}{(Z_S+Z_{C11})(Z_L+Z_{C22})-Z_{C12}Z_{C21}} \tag{3.29}$$

$$I_2 = Vs\frac{Z_{C21}}{(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}} \tag{3.30}$$

The maximum available source power P_{av}, power injected into this two-port network P_{in}, power delivered to the load P_L and the maximum power P_{Lmax} at load with output conjugated matching can then be expressed as

$$P_{av} = \frac{Vs^2}{4Re(Zs)} \tag{3.31}$$

$$P_{in} = \frac{\left|Vs(Z_L + Z_{C22})\right|^2}{Re\left(Z_{C11} - \frac{Z_{C12}Z_{C21}}{Z_L + Z_{C22}}\right)\left|(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}\right|^2} \tag{3.32}$$

$$P_L = \left|Vs\frac{Z_{C21}}{(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}}\right|^2 Re(Z_L) \tag{3.33}$$

$$P_{Lmax} = \left|Vs\frac{Z_{C21}}{(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}}\right|^2 Re\left(\left(Z_{C22} - \frac{Z_{C12}Z_{C21}}{Z_S + Z_{C11}}\right)^*\right) \tag{3.34}$$

The transducer gain G_T, operation gain G_P and available gain G_A can then be computable by

$$G_T = \frac{P_L}{P_{av}} = \frac{4Re(Z_L)Re(Zs)\left|Z_{C21}\right|^2}{\left|(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}\right|^2} \tag{3.35}$$

$$G_P = \frac{P_L}{P_{in}} = \frac{Re(Z_L)\left|Z_{C21}\right|^2}{\left|Z_L + Z_{C22}\right|^2} Re\left(Z_{C11} - \frac{Z_{C12}Z_{C21}}{Z_L + Z_{C22}}\right) \tag{3.35}$$

$$G_A = \frac{P_{Lmax}}{P_{av}} = \frac{4Re(Zs)\left|Z_{C21}\right|^2}{\left|(Z_S + Z_{C11})(Z_L + Z_{C22}) - Z_{C12}Z_{C21}\right|^2} Re\left(Z_{C22} - \frac{Z_{C12}Z_{C21}}{Z_S + Z_{C11}}\right) \tag{3.35}$$

Since the PA overall gain level is accumulated by the four stages, the operation gains of these stage are computed for gain flatness adjustment as illustrated in Fig. 48. The overall PA gain flatness can be easily estimated by adding these gain components together. Using this method to compensate the gain roll-off effect, the transformers are optimized stage by stage for presenting less forward transmission and transformer insertion loss at higher frequencies. Then the gain flatness of the overall PA is tuned for wideband response.

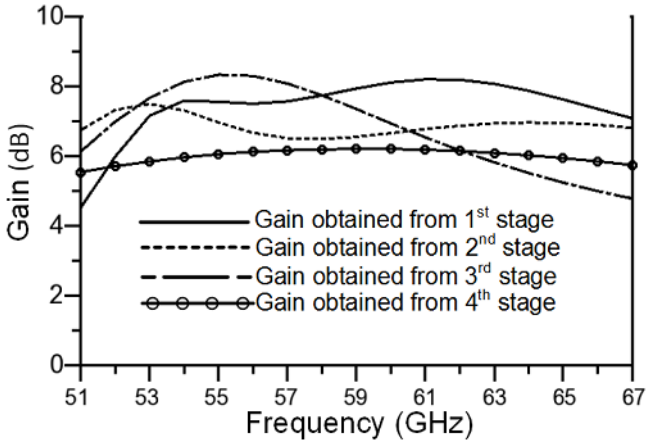


Fig. 48 Computed operation gain of the four stages.

3.6. Concentric Winding in differential Paralleling Splitting

For the conventional 2-way parallel splitting transformers in Fig. 49 (a), two winding centers are required for making secondary loops [67][104]. In order to compress the size of differential 2-way parallel splitting transformer, two secondary loops are winded around one center as illustrated in Fig. 49 (b). Due to high turn ratio of external source impedance to that of active device, the

primary loop is winded with two turns while only one turn is applied in secondary loop design. The proposed power splitter is simply represented by a configuration consisting of multiple coupling inductors. Each part of primary loop couples the input power into two secondary ones by current division and hence the two differential outputs are paralleled.

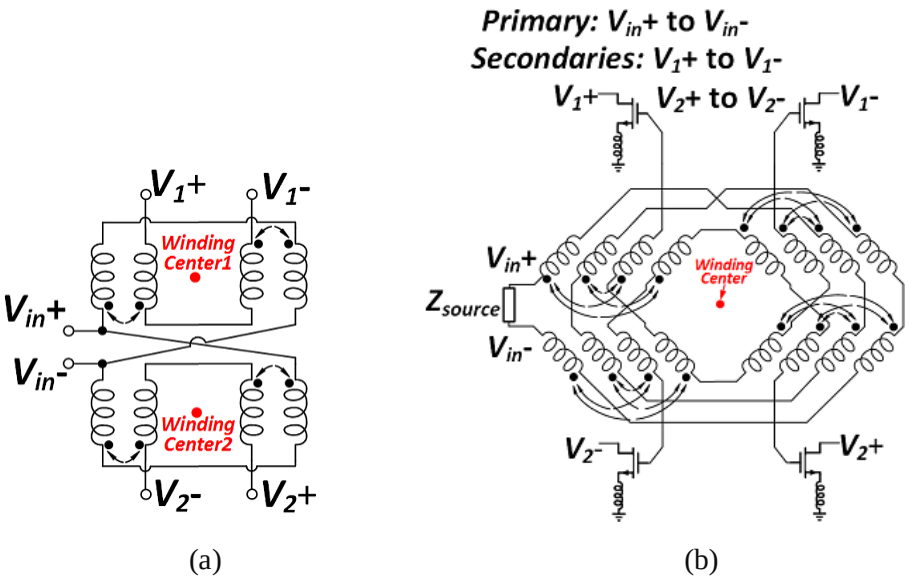


Fig. 49 (a) Conventional 2-way parallel splitting transformer diagram; (b) Diagram of the proposed concentric 2-way parallel splitting transformer T1.

In physical implementation as shown in in Fig. 50, each secondary loop is winded along halves of two octagon paths around a common geometry center. The traces of T1 are mainly implemented by M7 and M9 while M8 is used for jumper wires. By this concentric winding method, the size of T1 can be comparable to a transformer without power division function.

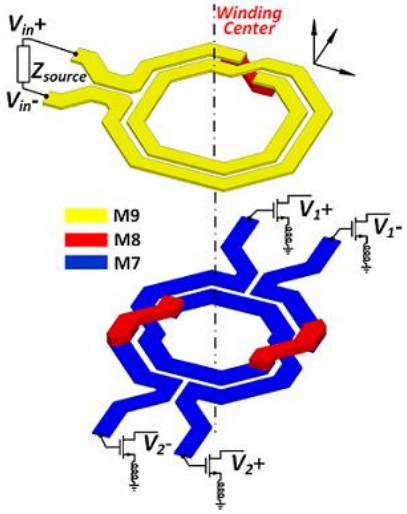


Fig. 50 Physical implementation of concentric parallel splitting transformer T1.

In Fig. 51, the simulated insertion loss of way 1 and way 2 in T1 are plotted. On the whole, this transformer is designed to be with lower insertion loss above 60 GHz. This design strategy is to compensate the gain roll-off effect of active device in the first stage as stated. At 60 GHz, the insertion loss of way 1 is 1.17 dB while it is about 1.36 dB for way 2. The isolation between way 1 and way 2 is more than 7.03 dB from 50 GHz to 70 GHz.

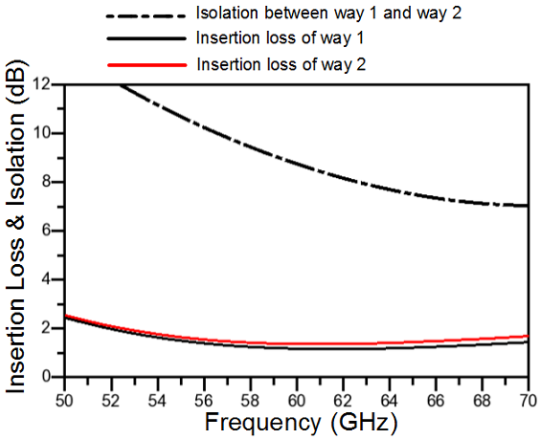
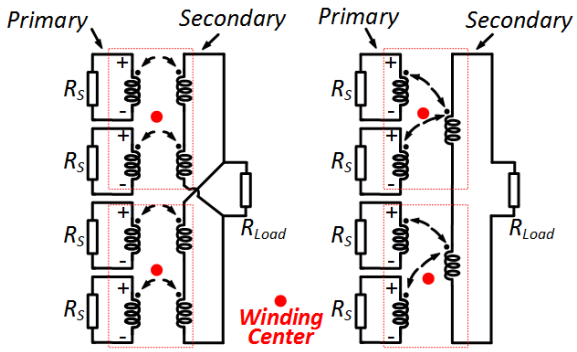


Fig. 51 Simulated insertion loss of way 1 and way 2 in T1.

3.7. Concentric Winding in Differential 4-way Hybrid Combining Transformer Design

The 4-way power combiner T5 is also devised in the concept of concentric winding for size reduction. For the conventional 4-way transformers based on parallel-series or series-parallel combining, the implementation is mostly accomplished by duplicating dual-way combiners physically [41][68][105]-[108]. As illustrated in Fig. 52, these two kinds of power combining transformer consist of two identical sub-transformers. Accordingly, such device size is bulky and comparable to transformers relying on parallel or series combining solely.



(a) (b)

Fig. 52 (a) Conventional differential 4-way series-parallel combining transformer diagram; (b) Conventional differential 4-way parallel-series combining transformer diagram.

To reduce the size of power combiner, a novel differential 4-way hybrid combining transformer T5 is proposed and illustrated in Fig. 53. This

configuration can also be inspired by the winding topology in Fig. 49. (b). If each secondary loop can be further split in the center point, additional two ways would be available for power division or combination. According to this design principle, way 1 and way 2 originate from the same winding loop in the differential parallel splitting transformer. Similar to the case in T1, these two ways are paralleled by way 3 and way 4 in T5. When input waves are only injected into way 1 and way 2 (or way 3 and way 4), the secondary winding trace would add up the coupled voltage. Therefore, both parallel and series power combining are achieved simultaneously. Compared with series, parallel, series-parallel and parallel-series combining transformers, all the primary and secondary loops of T5 are winded around one common geometry center. The proposed configuration would greatly save chip area for winding power combining transformer.

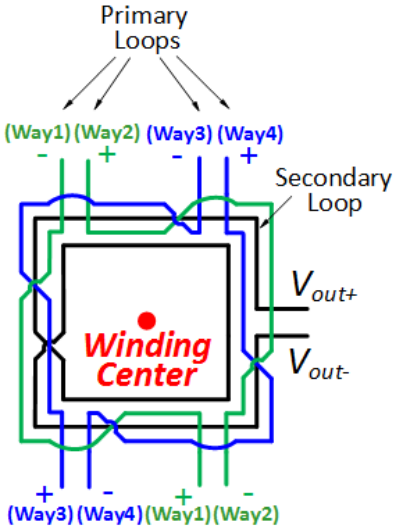


Fig. 53. The proposed winding diagram of novel 4-way hybrid combining transformer.

In the first step of implementing T5, the metal layer selection for winding traces is based on ideal inductive coupling assumption. The impedance turn ratio T of one input referred to the output is estimated by physical winding ratio of inductors. For an arbitrary ideal combining transformer with N ways in series combination by M paralleled duplications, T is theoretically found to be

$$T = \frac{Re(Z_p)}{Re(Z_s)} = \frac{n^2 M^2}{N^2} \tag{3.36}$$

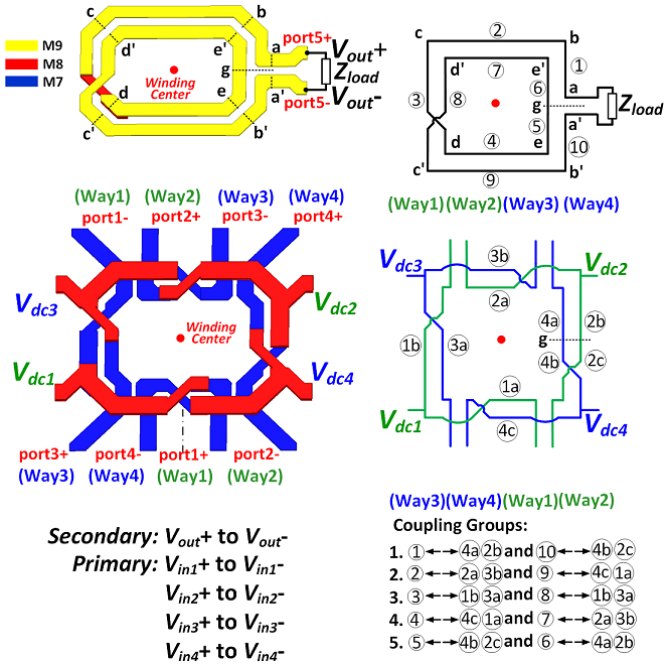
Z_p and Z_s demonstrate impedances terminated in primary and secondary loop. n is the winding ratio of a primary loop over the secondary loop. The ratio of current flowing through a primary loop to that of the secondary loop is roughly estimated by

$$\frac{I_p}{I_s} = \frac{N}{nM} \tag{3.37}$$

For this 4-way hybrid coupling transformer with 2 series way by 2 parallel multiplication, the optimal load impedance for the active device is around 26.3+j25.1 Ω according to simulation. When the secondary loop in T5 is with 2 turns, this winding scheme would theoretically transfer the input impedance seen by each UA4 to one fourth of output load 100 Ω. Correspondingly, the ac current ratio is estimated as 2:1. The efficiency of transformer is directly related to the dc power dissipated in inductors and the ratio of power converting to heat by parasitic resistor r_p and r_s in winding loops are estimated by

$$\frac{P_p}{P_s} = N \times M \times \frac{r_p}{r_s} \times \left(\frac{N}{nM}\right)^2 = \frac{r_p}{r_s}\frac{N^3}{n^2 M} \tag{3.38}$$

r_p and r_s are mainly caused by metal loss. When the items of the overall dissipated power P_p and P_s are minimized, the efficiency can be improved. By (3.38), power dissipation in primary loops is the dominant item when compared to that in secondary loops. To achieve good efficiency, high conductivity metal M7 and M8 with ultra-low metal loss are preferred for making primary loops. The secondary loop is made by metal M9 with relative lower conductivity. With this metal selection, the practical winding of T5 is illustrated in Fig. 54. (a).



(a) (b)

Fig. 54 (a) Physical configuration of 4-way hybrid combining T5; (b) Coupling diagram of the proposed 4-way hybrid combining transformer T5.

For better power combination performances, the effect of capacitive coupling is then investigated so as to make further strategies of implementing

T5. In Fig. 54. (b), the secondary loop is split into ten sections sequenced from ① to ⑩ while the primary loops are recognized as two or three sections divided by dc injection taps and secondary virtual ground point ‘g’. Between any two primary and secondary sections in coupling, the capacitive coupling between each primary and secondary section is described by the cross coupled capacitances C_{c1} and C_{c2}. In the model shown in Fig. 55, both capacitive and inductive coupling components are included. C_{gs} and C_{gp} represent the parasitic capacitance between winding traces to ac ground.

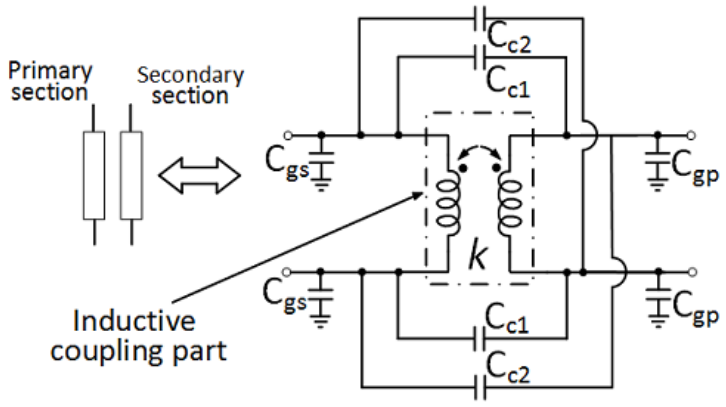


Fig. 55 Capacitive and inductive coupling model between each primary and secondary sections.

The analysis of the overall T5 model begins with studying the sections grouped in Fig. 54. (b). As an example, secondary sections ② and ⑨ together with primary sections 1a, 2a, 3b and 4c are analyzed in Fig. 56. Checking the currents i_1 and i_1' flowing through capacitors C_{c1} in this figure, it can be found that they are of equal magnitude but opposite signs. This relationship is also valid for other current pairs denoted as i_j and i_j' (j=1 , 2 , ..., 8). It means that

the total currents out of *b* point by capacitive coupling are equal to those flowing into *b'* through C_{c1} and C_{c2}.

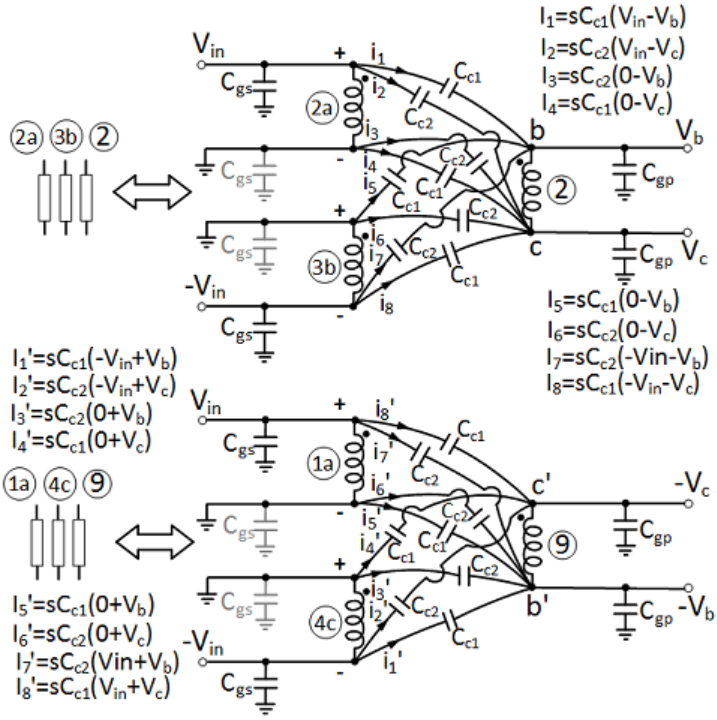


Fig. 56 Capacitive coupling among secondary sections ② and ⑨ together with primary sections 1a, 2a, 3b and 4c (Inductive coupling is not shown for figure clarity).

By summing up the currents of i_1, i_3, i_5 and i_7, the effective capacitance of C_{c1} and C_{c2} between *b* and *b'* points is then expressed as $(C_{c1}+C_{c2})+V_{in}(C_{c2}-C_{c1})/2V_b$. For the sake of concise expression, C_{c1} and C_{c2} approximate to C_c with the assumption that coupling effect is of little variation between any two terminals in Fig. 55. Then the effective capacitance between *b* and *b'* can be further simplified as $2C_c$. Applying this method to analyze other node pairs in Fig. 56, all the cross coupled capacitances are alternatively modeled by $2C_c$, C_{e1} as C_{e2} in Fig. 57.

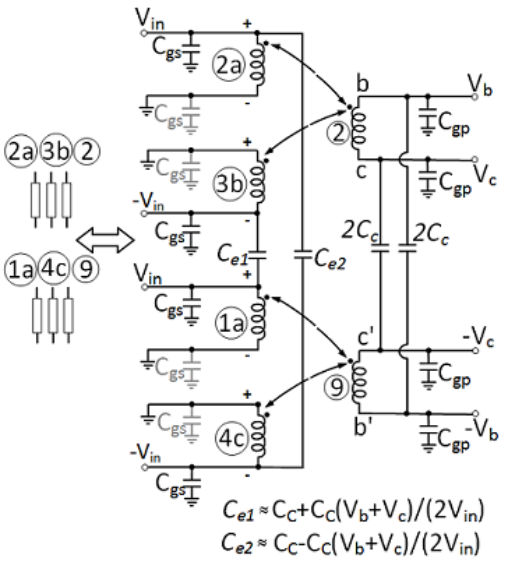


Fig. 57 Simplified coupling model of secondary sections ② and ⑨ together with primary sections 1a, 2a, 3b and 4c.

Once equivalent capacitors for the rest coupling groups in Fig. 54 are calculated, the lumped element model T5 would be available as demonstrated in in Fig. 58. Due to secondary currents in symmetry to virtual ground, I_{1a} is theoretically equal to I_{3b} by inductive coupling which gives the equation of $Z_{1a} = Z_{3b}$. Therefore, T5 is tended to offer identical input impedance for differential port 1 and port 3. For port 2 and port 4, it is also of the same case. The input impedance differences between port 1 and port 2 can be sourced in this model. Along the secondary loops, capacitors C_{gp}, C_{c1} and C_{c2} lead to inconsistent current distribution between I_0 to I_5 because of leakage currents flowing through C_{p1} to C_{p5}. In the primary part, C_{c1} and C_{c2} differentiate capacitances C_{13}, C_{31}, C_{24} and C_{42}. Comparatively, the primary parasitic capacitor C_{gs} is not as crucial as C_{gp}, C_{c1} and C_{c2} in differential operation mode.

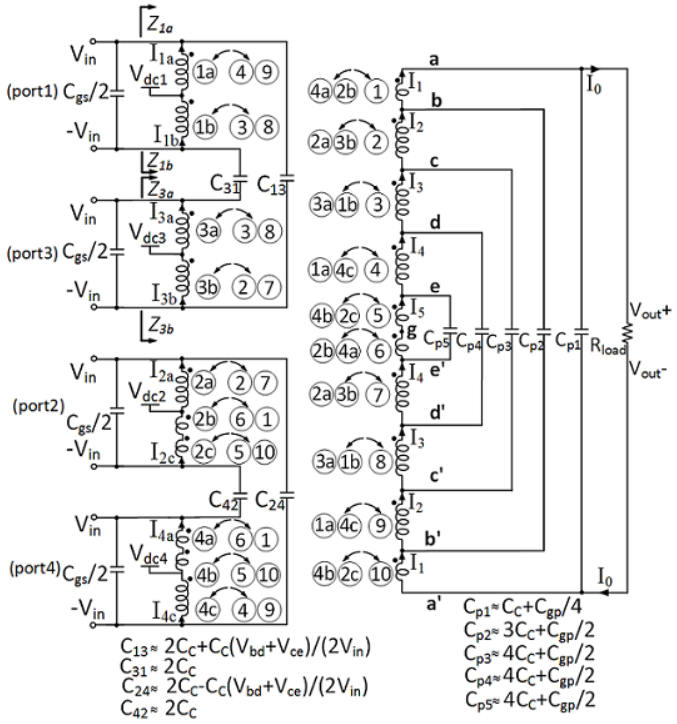


Fig. 58 Lumped element model of the 4-way hybrid combining transformer T5.

Applying the above analysis results in T5 physical configuration design, the key notes are summarized as follows:

1) For minimizing current discrepancies between I_0 to I_5 caused by C_{gp}, the ground plane should be placed as far as possible to sections in coupling. In this design, the distance is set to be more than 20 μm as illustrated in Fig. 59;

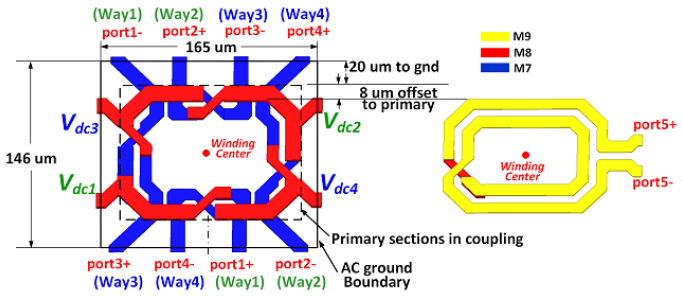
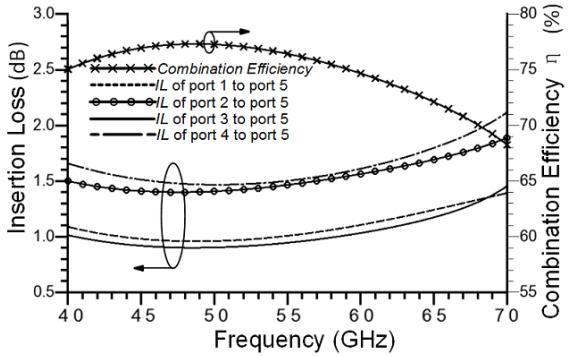


Fig. 59 Key design aspects of the proposed 4-way hybrid combining transformer T5.

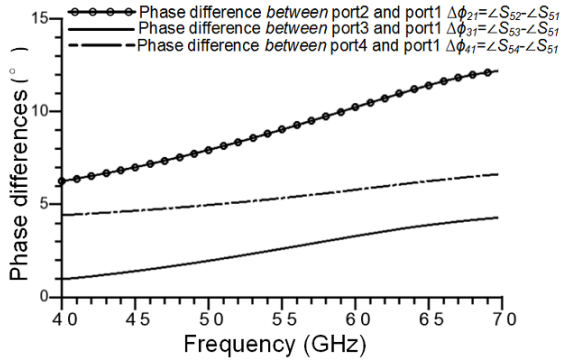
2) In order to reduce C_c in T5, the primary and secondary loops are not vertically overlapped but with certain offsets in trace placement;

3) As C_{gp} is more important than C_{gs}, the secondary loops can be winded in smaller dimensions than primary ones.

With these design guide, the physical sizes of combiner are further optimized by full-wave EM simulator Ansys HFSS. Its dimension in 65 nm CMOS is 165×146 μm^2. The simulated insertion loss and phase differences of the four differential ports are shown in Fig. 60 respectively.



(a)



(b)

Fig. 60 (a) *IL* of the four differential ports and the overall power combination η; (b) Phase differences between port1 to other ports.

From 40 GHz to 70 GHz, the simulated insertion loss of port 1 to port 4 is less than 1.89 dB and the phase differences are smaller than 12.4 degree. At 60 GHz, the insertion loss and phase differences are within 1.6 dB and 10.2 degree respectively. The *PAE* of the final stage is simulated when the output of 100 μm gate-width CMOS transistors with ISD is matched by T5 as demonstrated in the figure below.

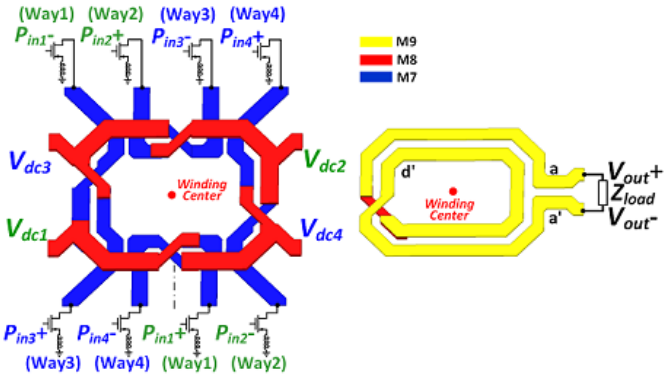


Fig. 61 Differential 4-way hybrid combining transformer T5 terminated by LP CMOS transistor with ISD.

With the above insertion loss and phase differences taken account, the *PAE* and power gain may also be affected by nonlinear behavior of active device. This determines how much power would be injected into T5. Firstly, the output power delivered by each unit amplifier may be reduced by deviations of input impedance to the optimal load. In Fig. 62, the simulated input impedances seen by the four primary ports are very close to the optimal load at 60 GHz. The differential impedance 26.7+j26.5 Ω seen by port 1 is closest to the optimal

load impedance. By comparing these input impedances with equivalent power contours, the power degradation caused by impedance variation to the maximum point is no more than 0.2 dB.

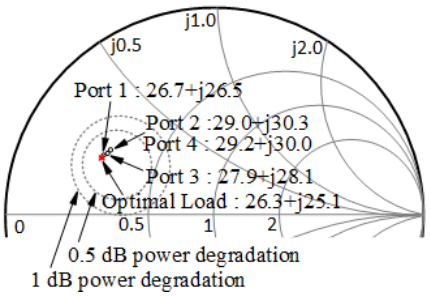


Fig. 62 Optimal load impedance, load impedance circles with 0.5 dB and 1 dB power degradation, input impedances seen by the four primary different ports at 60 GHz.

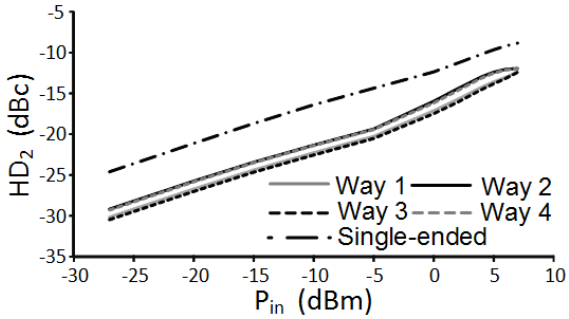


Fig. 63 HD_2 of way1 to way 4 at the inputs of secondary loops at 60 GHz.

Another nonlinear loss comes from ac ground shift for unit amplifiers within a differential pair, which induces even order harmonics. As illustrated in the model of Fig. 58, the impedance seen by each amplifier in a differential pair may not be identical because of capacitive coupling and layout asymmetry. In physical implementation, the position of center taps for dc injection should be tuned for suppressing harmonics. For ideal differential circuits, the second order harmonic distortion (HD_2) is supposed to be infinite. Therefore, the

second order harmonic distortion can be used to adjust virtual ground position. In this design, the tuned HD_2 of way 1 to way 4 are at least 2.8 dB better than that of single-ended amplifier as illustrated in Fig. 63.

With the above two nonlinear loss taken account, the *PAE* of the four differential pairs without power combination is plotted in Fig. 64. Compared with differential amplifier pair matched by ideal LC networks, the impedances presented by T5 offer slightly lower *PAE* when the input power (P_{in}) is more than 5 dBm. Including all of the aforementioned nonlinear and combination loss, the simulated results of *PAE* and power gain of the active device with T5 are also plotted in Fig. 64. The four differential pairs after power combination by T5 demonstrate 27.4 % *PAE*, 7.2 dB power gain with 13 dBm total input power. From the simulation results in Fig. 60 to Fig. 64, insertion loss, phase differences, input impedances and HD_2 show that way 1 is of better consistency to way 3 as analyzed by the model in Fig. 58.

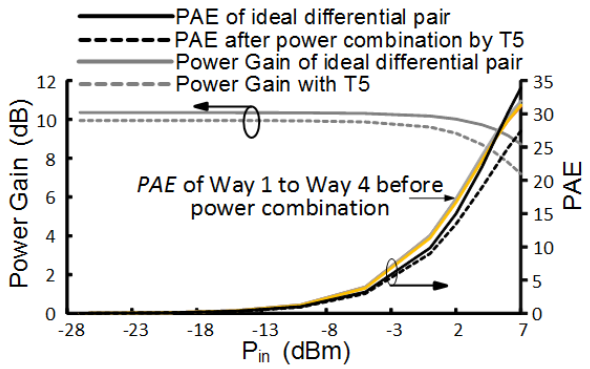


Fig. 64 *PAE* and power gain of an ideally LC-matched differential pair, *PAE* of the four differential pairs without power combination, *PAE* and power gain of the four differential pairs after power combination by T5 at 60 GHz.

3.8. Experimental Results of the Proposed Differential PA using the Novel Hybrid Combining Transformer

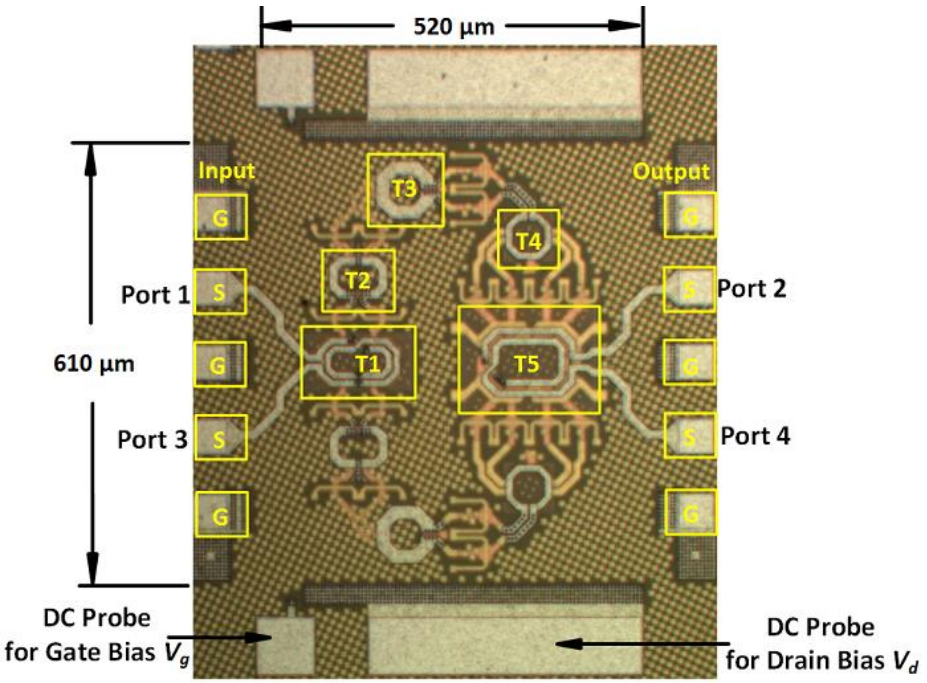


Fig. 65 Chip photograph of the fabricated differential CMOS PA.

The proposed differential mm-wave PA using novel 4-way hybrid combining transformer was fabricated in GF's 65 nm LP CMOS technology as shown in Fig. 65. The external probe voltages of this PA is firstly biased at 1.0 V V_g and 1.2 V V_d. This PA only consumes 520×610 µm^2 core area, while the dimensions of parallel splitting transformer T1 and hybrid combining transformer T5 are about 150×105 µm^2 and 165×146 µm^2 respectively. ISD are compactly implemented in all drive and final stages. The characterization of the

chip was similar to the first differential PA by CASCADE probe station, Agilent PNA-X and VNA.

In S-parameters measurement, the result agrees well with simulation as illustrated in Fig. 66. Two peak gain points are observed at 52.3 GHz and 60.0 GHz at the level of 26.8 dB and 26.6 dB accordingly. The 3-dB bandwidth of this PA covers 51 GHz - 67 GHz. The measured S_{22} is less than -7.1 dB at 51.6 - 67.0 GHz. The minimum value of S_{22} is -13.2 dB at 52.3 GHz and -17.2 dB at 62.0 GHz. The reverse isolation S_{12} is below -45 dB at the whole frequency range. At 60 GHz, the S_{11} of the proposed PA is about -6.0 dB.

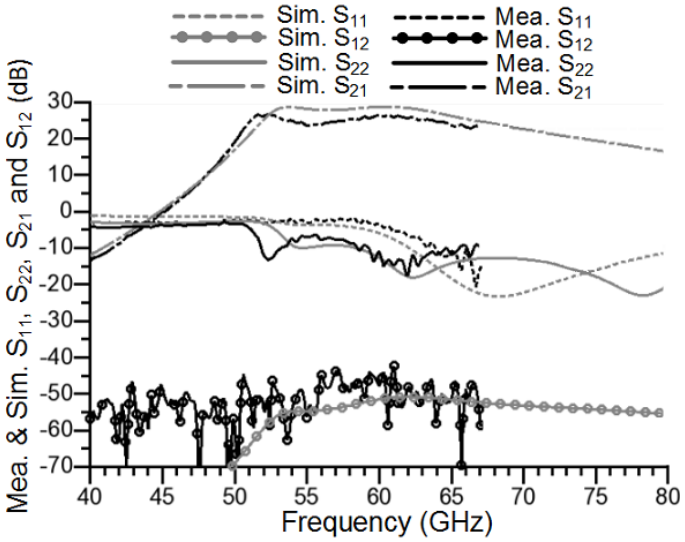
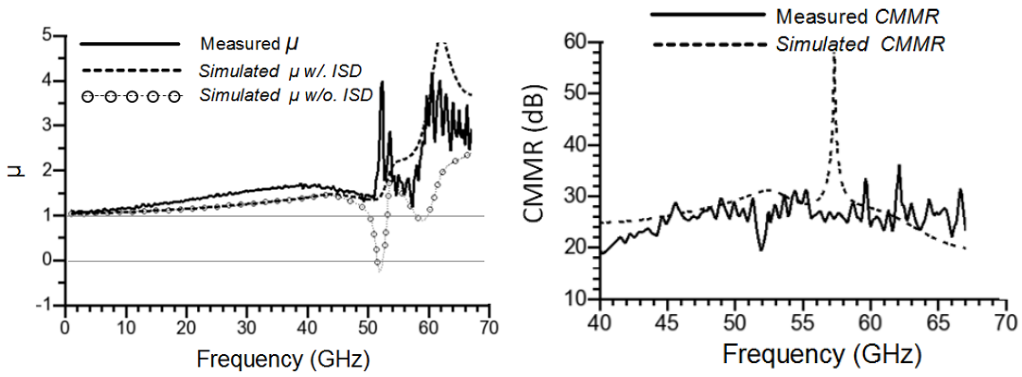


Fig. 66 S-parameter measurement and simulation results of the fabricated CMOS PA .

Across all band tested, the PA is unconditional stable for satisfying the condition of μ>1 as shown in Fig. 67 (a). If ISD is removed from CMOS transistors in circuit simulation, the whole PA would become oscillatory with center frequency at 51.8 GHz. The simulated and measured *CMRR* are shown

in Fig. 67 (b). The simulated peak value at 57.5 GHz is obtained as a result of a collective coincidental rejection of common-mode gain by the transformers of multiple stages at this exact frequency point. Therefore, deviations due to process variations during chip fabrication may easily influence this peak point. In fact, emphasis should be placed on the average *CMRR* level over the entire frequency range as this is the more important and useful parameter, which is of ultimate concern for this PA design. As a whole, this designed PA achieved *CMRR* better than 19.4 dB at 51 - 67 GHz.

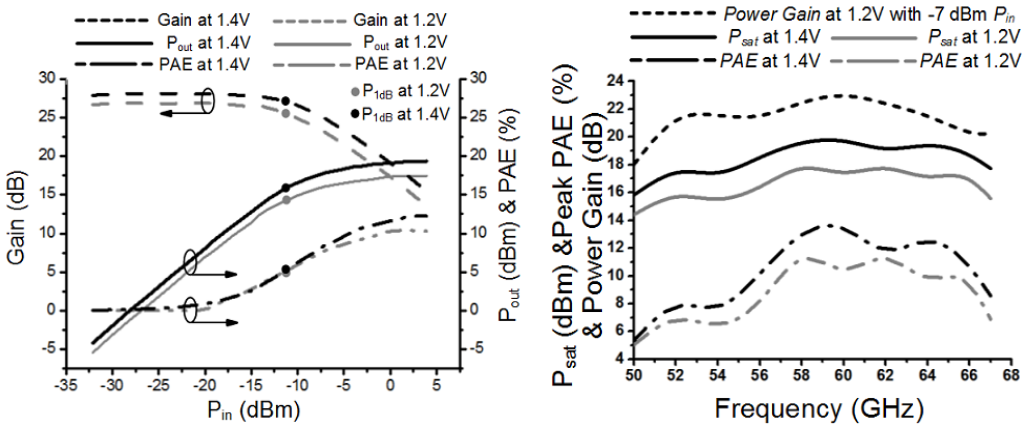


(a) (b)

Fig. 67 (a) Simulated and measured stability parameter μ; (b) Simulation and measurement results of *CMRR*.

In large signal measurement, the PA is able to deliver 17.5 dBm P_{sat} with 10.3% *PAE* at 60 GHz as plotted in Fig. 68. The output referred 1 dB and 3 dB compression points reach 14.3 dBm and 15.8 dBm correspondingly. In Fig. 68 (b), the highest P_{sat} is 17.7 dBm measured at both 58 GHz and 62 GHz with 11.2% *PAE*. With -7 dBm input power, the 3-dB bandwidth of power gain covers 50.6 GHz to 67.0 GHz. Compared with the first PA, the second PA

requires much lower drive power. To generate 17.0 dBm RF output, only -2 dBm drive power is needed. Therefore, only one PA can easily meet gain and power requirements of V band communication link.



(a) (b)

Fig. 68 (a) Measured Power gain, P_{1dB}, P_{out} and *PAE* vs P_{in} at 60 GHz. (b) P_{sat} and peak *PAE* versus frequency.

To estimate the lifetime of this PA with 1.2 V and 1.4 V bias, measurement is based on the method proposed in [46][109]. Both the dc and input power are set at high level to accelerate chip failure and the lifetime is estimated by extrapolation. The measurement results of dc current and output power in the condition of V_d bias probe voltage ranged from 2.0 V to 1.7 V are shown in Fig. 69. The RF stress corresponding to 17 dBm output power is around 0.8 V. The lifetime of the overall PA is estimated to 174.6 power-on hours (POH) at 1.4 V and 12388.3 POH at 1.2 V.

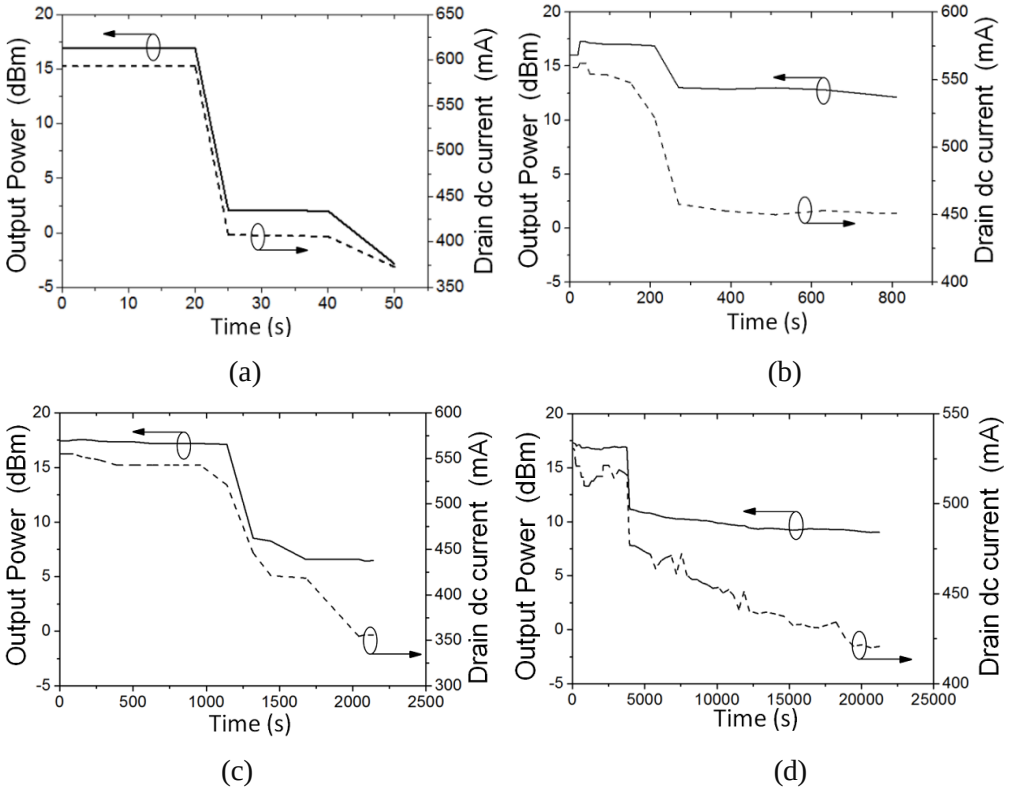


Fig. 69 dc current and output power tested in the condition of V_d bias probe with different voltages: (a) PA under 2.0 V bias; (b) PA under 1.9 V bias; (c) PA under 1.8 V bias; (d) PA under 1.7 V bias.

In table V, the performances of the designed mm-wave PA are compared with the state-of-the-arts. The standard ITRS FOM for evaluating PA performance has been defined in [110][111] as

$$\text{ITRS } FOM_{\text{PA}}=P_{out}\times Gain\times PAE\times f^2 \tag{3.39}$$

Using the proposed techniques, this differential PA in 65 nm LP CMOS is of high performances in several aspects among the most advanced. It simultaneously achieves high gain, high power, high power density and wideband. Therefore, the ITRS FOM of this PA is even comparable to ones

fabricated in 45 nm CMOS or SOI technology. Moreover, the PA still maintains a compact size with the above performances. As it provides high gain level within wide bandwidth, the 3-dB gain bandwidth is at the top of state-of-the-art as well. For the power combiner part, it is of the smallest size and each way occupies chip area less than one order of magnitude compared to other configurations.

Table V

THE MOST ADVANCED MM-WAVE CMOS PAS

Ref.	Tech. (nm)	Freq. (GHz)	Mode	V_d (V)	Gain (dB)	BW (GHz)	P_{1dB} (dBm)	P_{sat} (dBm)	Area (mm^2)	*PAE*	P_{sat}/ Core Area (mW/mm^2)	GBWP (dB·GHz)	FOM ($W•GHz^2$)
[43]	90NA	60	4CS	1.2	20.6	7*	18.2	19.9	1.76	14.2	55.5	144.2	5735.8
[55]	90NA	60	3CC	3.0	26.6	16	14.5	18.0	0.64	12.2	98.6	425.6	12666.7
[70]	90LP	60	3CS	1.2	15.7	5.8	14.7	18.5	0.385	10.2	183.88	91.06	965.8
[91]	90LP	60.5	2CC	1.2	14.3	15	11.0	16.6	0.461	4.9	98.94	214.5	220.7
[42]	90NA	61	3CS	1.2	15	5*	10.2	12.5	0.15	19.3	118.6	75.0	403.8
[78]	65GP	60	3CS	1.0	16.0	8.5	5.0	11.5	0.05	15.2	265.0	136.0	307.7
[112]	65GP	60	3CS	1.0	20.3	12*	15.0	18.6	0.28	15.1	258.73	243.6	4219.7
[41]	65GP	60	3CC	1.0	19.2	10	15.4	17.7	0.83	11.1	70.94	192.2	1957.2
[90]	65LP	60	2CS	1.2	8.3	16	9.7	11	0.28*	7.1	44.96	132.8	21.8
[68]	65LP	61	4CS	1.2	20	5*	13.5	15.6	1.15*	6.6	31.57	100.0	891.7
[113]	65GP	61	3CS	1.0	30.0	7.0	6.8	10.6	0.06	7.7	208.8	210.0	3289.7
[44]	65LP	64	3CS	1.2	16.3	25.1	19.4	23.2	1.88*	10.0	111.13	409.3	3650.6
[61]	45†	35	2SF	4.8	19.4	13	21.0	27.2	4.16	10.7	126.2	252.2	5991.3
[59]	45†	41	1SF	5.0	8.9	10.0	21.0*	21.6	0.30	25.1	481.8	89.0	473.4
[114]	45†	45	1SF	5.1	>18	-	-	24.3	-	14.6	-	-	5020.9
[60]	45†	47	2SF	4.8	24.9	9.5*	-	20.1	0.18	15.4	568.5	236.6	10757.6
[115]	45LP	60	2CC	2.0	20.0	10.0	11.2	14.5	0.04	14.4	704.6	200.0	1461.0
[46]	40NA	60	3CS	1.0	21.2	4.0*	14.0	17.4	0.074	28.5	742.6	84.8	7432.7
[69]	40GP	60	3PP	1.8	22.4	-	13.9	16.4	0.081	23.0	538.9	-	6281.0
[116]	40NA	60	4CS	1.2	29.0	5.6*	17.0	22.6	2.16	7.0	84.2	162.4	36425.1
[107]	40NA	78.5	2CS	0.9	18.1	15.2	17.8	20.9	0.19	22.3	647.5	275.1	10915.5
This PA	**65LP**	**60**	**4CS**	**1.2**	**26.6**	**16**	**14.3**	**17.5**	**0.32**	**10.3**	**175.73**	**425.6**	**9531.0**
This PA	**65LP**	**60**	**4CS**	**1.4**	**28.0**	**13.9**	**16.0**	**19.7**	**0.32**	**13.4**	**291.39**	**389.2**	**28405.8**

* Estimated value from paper cited. BW is abbreviation of 3-dB bandwidth estimated by S-parameters.

†: SOI;

+N (1, 2, 3, 4.): number of stages; CS: common source; CC: cascode; PP: push-pull; SF: stacked-FET

In summary of this chapter, a compact mm-wave differential CMOS PA with wideband, large output power and high gain performances is achieved in

commercial LP CMOS process. In PA architecture planning, the loop-like circuit topology for cascading four CS stages is introduced. The solutions for realizing compact PA with high performances are discussed. During design of amplification stages, the method of converting differential transformer model to its equivalent single-ended form is provided in advance. Then the CMOS transistor with ISD can be taken into account with multi-port transformers in the design aspects of stability, bandwidth and matching. In the passive transformer design, concentric winding technique is firstly proposed to implement innovative 2-way parallel splitting and 4-way hybrid combining transformer in compact size. Specifically, the physical design strategies of hybrid combining transformer are acquired by studying its coupling behavior and nonlinearity with the active device. In measurement, this differential mm-wave PA in GF 65 nm LP CMOS achieves more than 23.8 dB gain at 51 - 67 GHz and 19.7 dBm P_{sat} with 13.4% *PAE* at 60 GHz. With a compact size of 520×610 μm^2, this V-band PA provides high ITRS FOM, $P_{sat}/_{Core\ Area}$ and 3-dB bandwidth. Although the aforementioned techniques are demonstrated in 65nm LP CMOS, it can also be applied in other silicon-based processes such as SiGe BiCMOS or SOI.

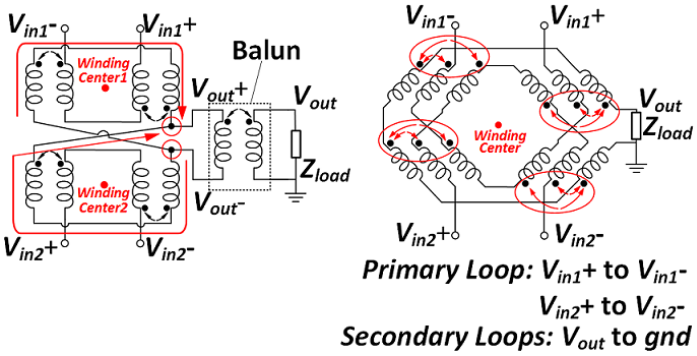
Chapter 4: Parallel Power Combination in CMOS

4.1 Concentric Winding Technique in Parallel Combining Balun

As mentioned in chapter 2 and 3, one problem of PA design using in-phase power combiners is that the features of multiple input ways to the output are hard to be identical. Even if schematic keeps symmetry, the parasitic and asymmetry in layout inevitably induces differences between the multiple inputs. These differences would be reflected by amplitude and phase status of the input /output wave components. These differences could be a major source for power degradation using in-phase combiners [41][99][104]. However, the corresponding calculation method of power combination efficiency has not been studied so far.

In single-ended transformer PAs, additional baluns in I/O ports may be required for unbalance-balance conversion [55][68]. This additional device requires additional area and brings extra loss. For transformers / baluns applied in signal-ended PA, the power combination efficiency with various phase and amplitude wave components at input / output port is a more complicated problem. It is because the waves with 180° phase differences injected into two ports in differential operation may actually not achieve in-phase status at the output port. In this case, the two wave components are not ideally unbalanced within the differential pair of transformer / balan. If the number of input differential pairs is more than two, the waves to be combined at the output would consist of

components from in-phase and unbalanced input ports. All these differences and non-ideal internal unbalance are hard to be numerically characterized by the lump element model. Currently, their impact to power combination efficiency has not been investigated and available for PA design reference. This chapter would focus on solving this practical power combination problem during design and implementation of a single-ended mm-wave CMOS PA based on novel parallel combining balun for achieving high power density in LP CMOS.



(a) (b)

Fig. 70 (a) Current summation in ideal conventional parallel combining transformer and balun; (b) Current summation in the proposed concentric parallel combining balun.

In this single-ended PA design, the proposed parallel combining balun also takes the advantage of concentric winding technique for compact size. In the winding diagram of this parallel combining balun illustrated in Fig 70 (b), each section of the secondary loop would couple the signal from two primary sections as denoted by red in this figure. Similar to the parallel splitting transformer in section 3.6, the current addition requirement for parallel combining is simultaneously satisfied when signals are coupled from primary to secondary loops. For single-

ended applications, the external source and load are 50 Ω. Compared with the impedance transformation in differential PA, the turn ratio from the external to circuit internal is about reduced by half in single-end PA. Therefore, only one turn is enough for winding the secondary loop.

The physical implementation of the proposed power combining balun is demonstrated in Fig. 71. The primary and secondary traces are implemented by M7 to M9 in 65 nm LP CMOS. Each secondary way is winded along halves of two octagon paths while M7 is used for jumper wires. This configuration can be either be used as power division or combination networks. Moreover, the center taps in the primary loops are available for dc feed.

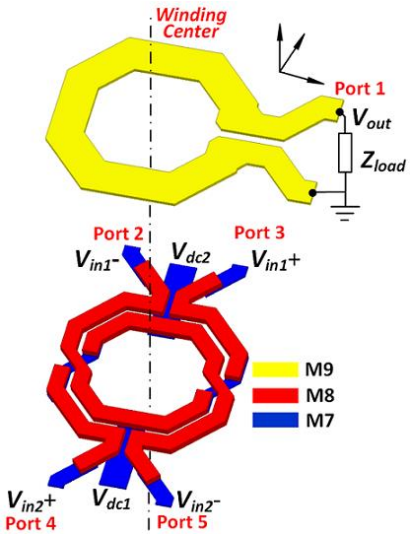


Fig. 71 Physical implementation of the proposed parallel combining balun.

During physical design, parasitic resistance, parasitic capacitance and layout asymmetry inevitably exist in the configuration of parallel combining balun, which are major sources of imperfect phase and amplitude status. With the parasitic taken

into account [68][117]-[119], the parallel combining balun is examined by the model in Fig. 72. In the aspects of the parasitic, the main factors lead to amplitude difference and phase difference / non-ideal internal unbalance are concluded as

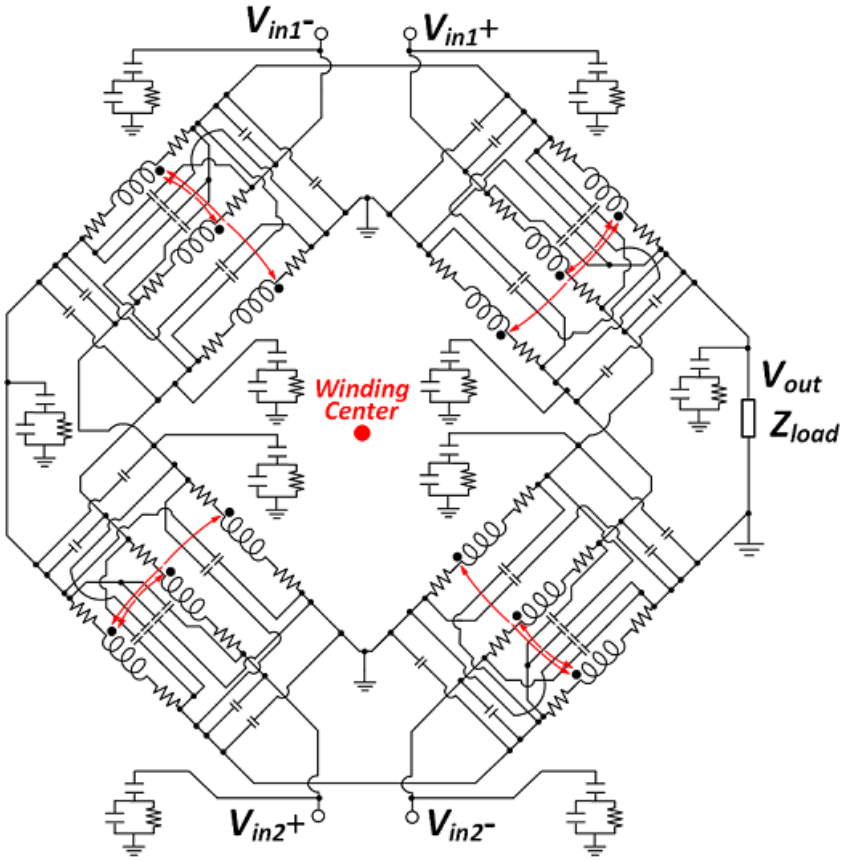


Fig. 72 Lumped element model of the proposed parallel combining balun.

1) The ground parasitic capacitance and resistance along the primary and secondary sections create the leakage current paths to ground. Therefore, the current distribution in the two primary loops are not entirely identical;

2) The mutual coupling capacitances between primary and secondary sections provide additional signal transition paths. Therefore, the current coupled through

the inductive path from primary to secondary loop are also different for the four sections.

In the aspects of layout asymmetry, amplitude difference and phase difference / non-ideal internal unbalance are sourced from physical implementation of the proposed parallel combining balun as follows.

1) For the four input port, the jumper wire can hardly be in symmetry. Consequently, the coupling factor, winding inductance and even parasitic components are of slight different values for the four sections of primary and secondary loops;

2) The output portion of the secondary loop determines that the left and right part of a transformer-based configuration cannot maintain fully symmetry as well. The results of this effect are similar to the above point.

For the above reasons, the lumped element model for studying the differences and internal non-ideal imbalances becomes rather convoluted and it would be hard to calculate the exact value of power combination efficiency in this way.

4.2. Power Combination Calculation Using S-parameters

In practical PA design, scatting matrix is more convenient to precisely describe the characteristics of the five ports. It is because it treats the internal mechanism of multi-port networks as black box and only concerns about the

characteristics of input / output ports. The S-parameters are generally obtained by circuit simulator or test equipment when in-phase input signals are injected into power combination networks. The S_{1m} (m= 2, 3, …, n-1, n) represents the forward transmission coefficients of the multiple-port networks in Fig. 73.

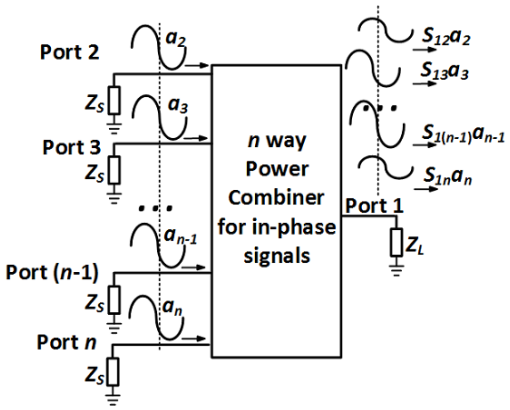


Fig. 73 n way power combination for in-phase input signals.

For an ideal binary combiner with n input ways, the according S_{1m} in dB should be $-3\times\log_2 n$. The type of power combiners can be regarded as two groups, namely in-phase signal combiner and differential drive combiner. Their ideal condition of S_{1m} phases are different. For in-phase power combiner with equal incident power wave at input ports, the overall power combination efficiency can be directly calculated by superposition of output S_{1m} components with different amplitude and phase.

$$\eta_{in-phase} = \left|S_{12} + S_{13} + \ldots + S_{1(n-1)} + S_{1n}\right| = \left|\left|S_{12}\right|e^{j\angle S_{12}} + \left|S_{13}\right|e^{j\angle S_{13}} + \ldots + \left|S_{1(n-1)}\right|e^{j\angle S_{1(n-1)}} + \left|S_{1n}\right|e^{\angle S_{1n}}\right| \quad (4.1)$$

By summing up real part and imaginary part of the items in (4.1) separately, the power combination can be derived as

$$\eta_{in-phase} = \sqrt{\left(\sum_{m=2}^{n}|S_{1m}|\cos\angle S_{1m}\right)^2 + \left(\sum_{m=2}^{n}|S_{1m}|\sin\angle S_{1m}\right)^2} = \sqrt{\sum_{m=2}^{n}\sum_{k=2}^{n}|S_{1m}||S_{1k}|\cos\left(\angle S_{1m} - \angle S_{1k}\right)} \quad (4.2)$$

To obtain good power combination efficiency using in-phase combiners, phase differences should be close to $2\pi i$ (i=integer) by (4.2). As long as the outcome of $\cos(\angle S_{1m} - \angle S_{1k})$ is still positive, the magnitude of forward transmission coefficient should be as high as possible.

For the proposed parallel combining balun, the simulated S-parameter S_{1m} of this five-port network are demonstrated in Fig 74.

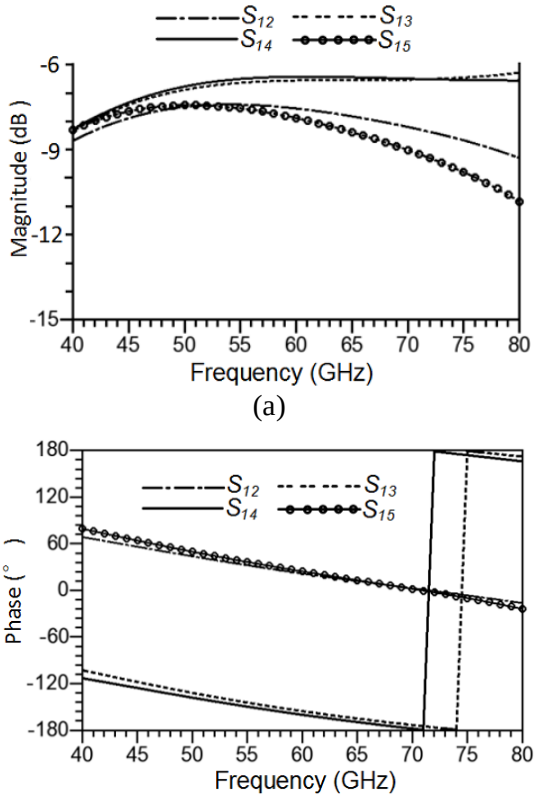


Fig. 74 (a) Magnitude in dB of the S-parameters; (b) Phase in degree of the S-parameters.

However, the input ports of coupling inductor configurations need to be driven by differential signals in pair. If in-phase signals are injected into this parallel combining balun, most of power would be canceled at the output by (4.2). The power combination efficiency of the proposed parallel combining balun is calculated when differential waves are excited at the four input ports. Their phases at port 2 and port 5 are ideally of 180 degree differences compared to those at port 3 and port 4. As passive combiner is linear device, such changes at the input cause linear phase shift in the output wave components as demonstrated in Fig. 75.

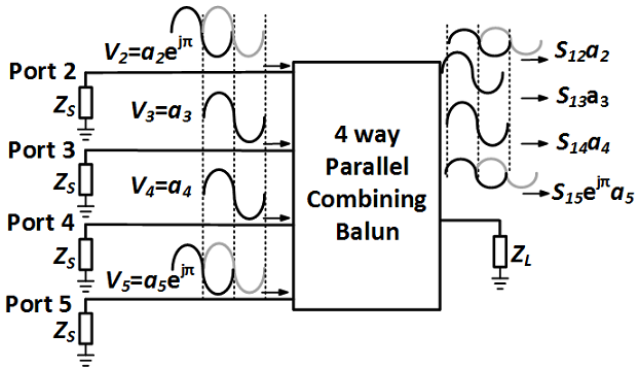


Fig. 75 Power combination for the proposed 4-way parallel combining balun.

Then the power combination efficiency of the parallel combining balun is solved by superposition of the components that are derived in (4.3). In Fig. 76, the phase differences and phase unbalances denoted in equation (4.3) are plotted. From 50 GHz to 70 GHz, all of them are smaller than 6.2 degree.

$$\eta_{Balun} = \left|S_{12}e^{j\pi} + S_{13} + S_{14} + S_{15}e^{j\pi}\right|$$

$$= \sqrt{\begin{array}{l}|S_{12}|^2 + |S_{13}|^2 + |S_{14}|^2 + |S_{15}|^2 - 2|S_{12}||S_{13}|\cos(\angle S_{12} - \angle S_{13}) - 2|S_{12}||S_{14}|\cos(\angle S_{12} - \angle S_{14}) + 2|S_{12}||S_{15}|\cos(\angle S_{12} - \angle S_{15}) \\ +2|S_{13}||S_{14}|\cos(\angle S_{13} - \angle S_{14}) - 2|S_{13}||S_{15}|\cos(\angle S_{13} - \angle S_{15}) - 2|S_{14}||S_{15}|\cos(\angle S_{14} - \angle S_{15})\end{array}} \quad (4.3)$$

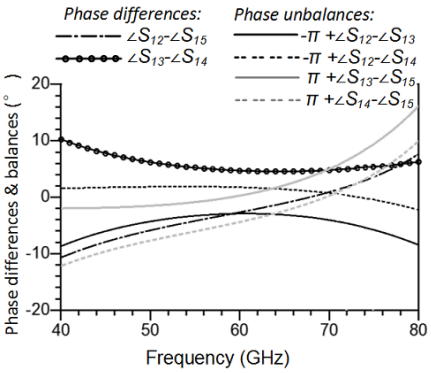


Fig. 76 Phase differences between ports with in-phase signals, phase unbalances between ports with differential signals.

The calculated overall power combination efficiency of the proposed 4-way parallel combining balun is above 57.5 % at 50 GHz - 70 GHz as shown in Fig. 77. It achieves 77.5 % efficiency at 62 GHz. Using the proposed calculation method to investigate the robustness of this balun to input phase deviations, the combination efficiency is also computed in the condition that the four input ports are not driven by ideal differential signal pairs. When one input way is of 30° phase deviation, the combination efficiency is dropped by just 1.7 to 2.6 % at 62 GHz. With 60° phase deviation, this efficiency is further reduced to the value between 68.4% and 70.7 %.

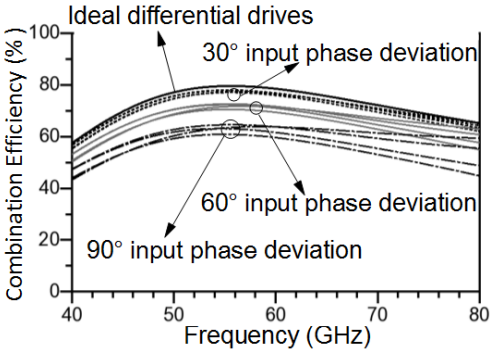


Fig. 77 Combination efficiency of the proposed power combining balun with ideal differential drives, one input with 30° /60° / 90° phase deviation.

4.3. Single-ended V-band CMOS PA Design using Parallel Splitting / Combining Balun

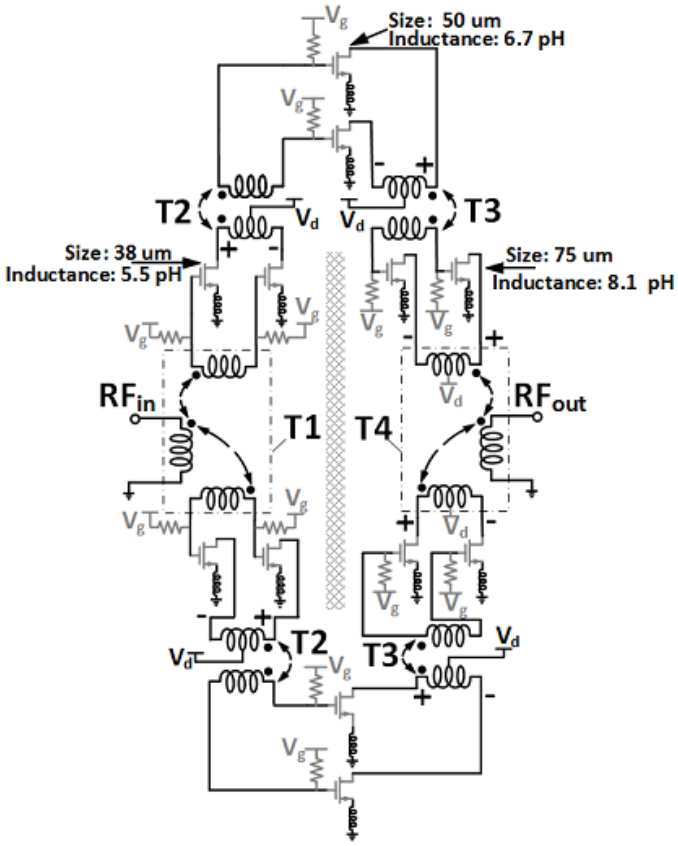


Fig. 78 The architecture topology of the proposed single-ended V-band CMOS PA.

For demonstrating the application of novel power combining balun, an architecture of single-ended V-band CMOS PA is proposed for high power density design as shown in Fig. 78. On the whole, three common source stages are cascaded. All integrated components are arranged along a loop-like topology to

maximize usages of all the occupied chip area. Within the active device of each stage, inductive source degeneration is added to stabilize LP CMOS transistors. For the passive matching part, the power combining balun T4 is applied in the final stage as discussed. Besides T4, T1 also shares the same configuration that can unbalance and divide the input signal. The inter-stage matching and interconnection are accomplished by 1:1 transformers T2 and T3. All gate bias is fed trough large resistors while transistor drain is connected to center taps of transformer and balun.

4.4. Experimental Results of the Single-ended V-band PA

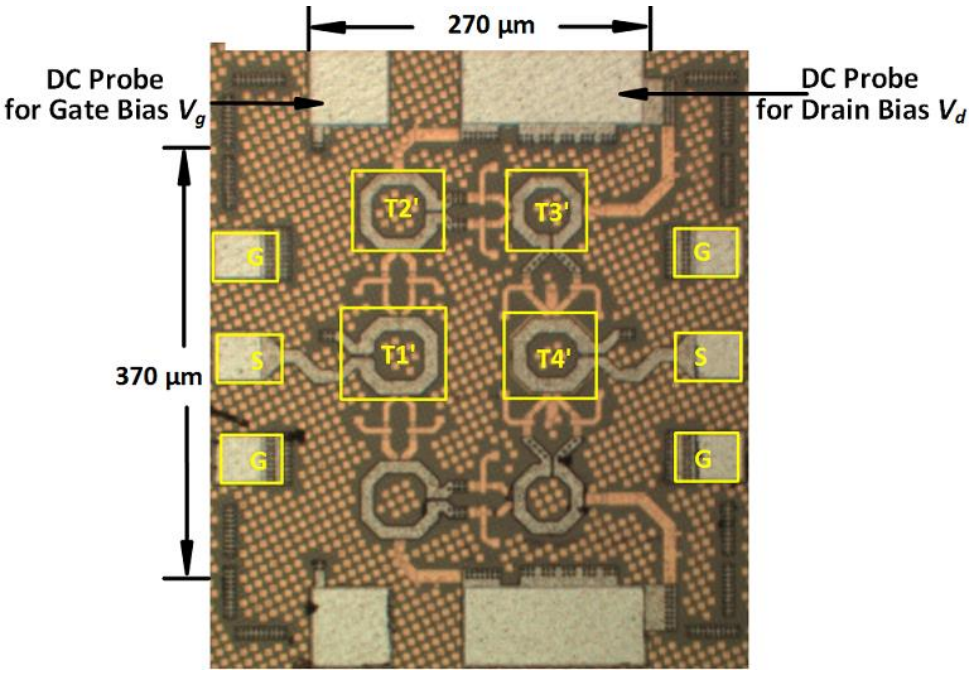
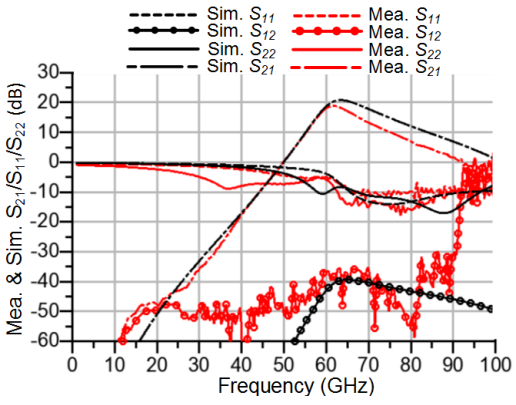


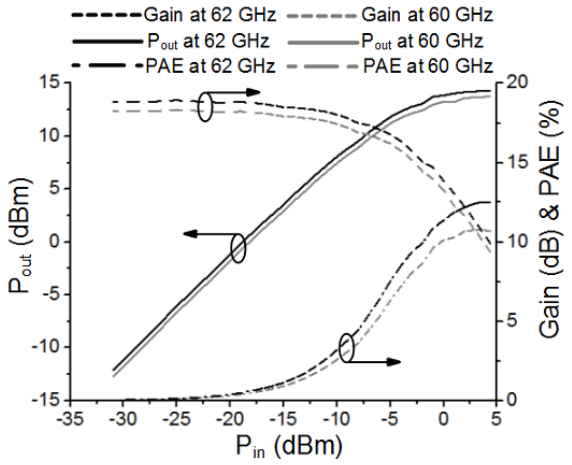
Fig. 79 Chip photograph of the fabricated V-band single-ended CMOS PA

With the proposed parallel combining balun, the V-band PA was fabricated in GF's 65 nm LP CMOS technology. In Fig. 79, the chip core only consumes 270×370 μm^2 area, while the dimensions of T1 and T4 are about 110×110 μm^2 and 95×95 μm^2 respectively. In measurement, Agilent PNA-X can support single-ended circuit test up to 110 GHz. The PA is terminated with 50 Ω source and load.

The probe voltages are biased at 1.0 V V_g and 1.2 V V_d. The measured S-parameters show that the PA can offer 18.9 dB gain at 62 GHz. The according 3-dB bandwidth is 58.3-66.6 GHz as shown in Fig. 80 (a). In power measurement, the output referred P_{1dB} and P_{sat} at 62 GHz are 8.8 dBm and 14.3 dBm respectively, as illustrated in Fig. 80 (b). At 60 GHz, the P_{1dB} is 8.3 dBm while P_{sat} is 13.8 dBm. The peak *PAE* at 60 GHz and 62 GHz is 10.7 % and 12.5 % correspondingly. In table VI, this single-ended V-band PA in LP process is of compact size and achieves high power density $P_{sat}/_{Core\ Area}$ of 269.15 mW/mm^2 among the advanced 65 nm CMOS PAs.



(a)



(b)

Fig. 80 (a) Simulated and measured S-parameters of the single-ended V-band PA; (b) The measured large signal gain, P_{out} and PAE vs P_{in} at 60 GHz and 62 GHz.

Table VI

COMPARISON TABLE OF THE STATE-OF-THE-ART

Ref.	Tech. (nm)	Freq. (GHz)	Mode	Supply Voltage (V)	Gain (dB)	P_{1dB} (dBm)	P_{sat} (dBm)	Area (mm^2)	*PAE*	P_{sat}/ Core Area (mW/mm^2)
[78]	65 GP	60	Sing.+3CS	1.0	16.0	5.0	11.5	0.05	15.2	265.0
[112]	65 GP	60	Sing.+3CS	1.0	20.3	15.0	18.6	0.28	15.1	258.73
[41]	65 GP	60	Diff.+3CC	1.0	19.2	15.4	17.7	0.83	11.1	70.94
[90]	65 LP	60	Sing.+2CS	1.2	8.3	9.7	11	0.28*	7.1	44.96
[68]	65 LP	61	Sing.+4CS	1.2	20	13.5	15.6	1.15*	6.6	31.57
[113]	65 GP	61	Sing.+3CS	1.0	30.0	6.8	10.6	0.06	7.7	208.8
[44]	65 LP	64	Sing.+3CS	1.2	16.3	19.4	23.2	1.88*	10.0	111.13
This Work	**65 LP**	**62**	**Sing.+3CS**	**1.2**	**18.9**	**8.8**	**14.3**	**0.10**	**12.5**	**269.15**

* Estimated value from paper cited.

+*N* (1, 2, 3, 4.): number of stages; CS: common source; CC: cascode

In summary of chapter, a novel parallel combining balun based on concentric winding technique is proposed and then applied in a single-ended V-band PA design for high power density in LP CMOS. By this balun, the parallel combining and unbalance-balance conversion are simultaneously accomplished by concentric winded inductors for compact combiner size. In balun practical implementation,

the amplitude difference and phase difference / non-ideal internal unbalance are sourced from parasitic components and asymmetry in layout. To accurately calculate power combination efficiency of combiners with in-phase or differential input signals, computation method based on S-parameters are derived. This method is then applied in efficiency calculation of the proposed parallel combination balun. Finally, a single-ended PA is designed in GF 65 nm LP CMOS process to demonstrate the application of novel power combining balun. This PA has a compact size of 270×370 μm^2 and can offer 18.9 dB gain, 14.3 dBm P_{sat} at 62 GHz. Among the most advanced V-band CMOS PAs in 65 nm CMOS, this PA in LP process is of highest power density. The power density of single-ended PA can be further improved by increasing transistor size.

Chapter 5: Conclusion and Recommendations

5.1. Conclusions

In this thesis, power combination techniques for compact transformers are thoroughly explored and analyzed for mm-wave PA designs. After investigating the features of semiconductor devices and current power combining methods, novel series, hybrid and parallel combining transformer / balun are devised, implemented and verified by three V-band PAs in 65 nm LP CMOS.

The first differential PA is based upon series combining transformer. The ISD technique is introduced to stabilize CMOS transistor at mm-wave band. The layout of its source inductor is specially optimized for mm-wave PA design. For characterizing complex circuit topologies like CMOS transistor with ISD, an algorithm named as admittance matrix condensation is derived and then applied in linear analysis of this PA. This algorithm can also be conveniently used in symbolic derivation and numerical calculation of other kinds of circuits. The nonlinear behavior of CMOS transistor with ISD is also studied using Volterra series at mm-wave band. These linear and nonlinear analysis give comprehensive design reference of the optimal source inductance range. In passive transformer design for this PA, an X-shape patterned ground shielding

is introduced into series transformer to reduce phase and amplitude differences. With the proposed series combining transformer, the fabricated differential PA demonstrates above 10 dB gain and 26 dB *CMRR* at 41 - 61 GHz. At 60 GHz, the measured P_{1dB}, P_{sat} and peak *PAE* are 11.9 dBm, 15.2 dBm and 12.4 % correspondingly. It only consumes 0.25 μm^2 core area in 65 nm LP CMOS.

In the second differential PA design using novel differential 4-way hybrid combining transformer, the architecture and solutions for high gain, high power and wideband performances are proposed in the beginning. By developing a method of converting differential transformer model to its equivalent single-ended form, the passive devices can be analyzed with active device for PA stability and matching within wide bandwidth. As a key solution for compact PA size, concentric winding is innovated and applied in design of differential 2-way parallel splitting transformer and 4-way hybrid combiner transformer. These two configurations save considerable chip space in comparison with the conventional transformers. The design of 4-way differential hybrid combining transformer are particularly investigated for its physical implementation. With these analysis and techniques, the second differential mm-wave PA is also realized in 65 nm LP CMOS by Globalfoundries. The designed PA is able to provide 26.6 gain at 60 GHz and covers 16 GHz bandwidth. It achieves 17.7 / 19.7 dBm output power under 1.2 V / 1.4 V probe voltage while the peak *PAE* is 11.2% / 13.4% respectively. In 520×610 μm^2 core area, this CMOS PA in LP process offers high ITRS FOM, power density and wide bandwidth.

In the last single-ended PA design, a novel configuration named as power combining balun is devised for high power density in LP CMOS. For reducing the size of single-ended PA using parallel power combining, concentric winding technique is also applied in the proposed power combining balun. After examining the possible causes for amplitude difference and phase difference / non-ideal internal unbalance, the method of computing power combination efficiency is derived. This method can also be used to characterize various kinds of combiners injected by waves with different phase and amplitude. With the proposed parallel combining balun, the fabricated three-stage V-band CMOS PA in 65 nm LP CMOS has achieved 18.1 dB and 18.9 dB gain at 60 GHz and 62 GHz correspondingly. Occupying just 0.10 μm^2 area, this PA is capable of delivering 14.3 dBm P_{sat} with 12.5 % *PAE* in measurement. The power density is as high as 269.15 mW/ mm^2.

The specifications of all the above PAs are sufficient to support communication system for V-band short-range and high-data-rate communication applications as discussed in the first chapter. Benefitting from high delivered power with margins, adopting these PAs gives freedoms to choose lower gain antenna with smaller size. Another option is to keep antenna specifications and achieve wider communication range by using the developed PAs. According to gain requirement of the typical link budget, only one PA module based on the second or third prototype is enough to drive antenna. For the first prototype, two PAs may be cascaded to strengthen total gain to support high output power operation when

input power out from mixer to PA is at the level of around -2 dBm [53]. Moreover, the sizes of all the proposed PAs are rather appealing for system implementation. Among the reported high power V-band 65 nm or 90 nm CMOS PAs using combiners with more than four ways, the dimensions of the developed PAs are reduced to 27% compared with the average. Meanwhile, wide bandwidth, large power, high power density performances have also been realized by the proposed PA design techniques.

5.2. Recommendations for Further Research

In future work, the author will look into adopting nonlinear PA architectures into mm-wave PA design. As discussed in chapter 2, the maximum drain efficiency of class A/B PA is limited to 50% / 78.5%. For the consideration of *PAE*, the designed PAs introduced in this thesis are in class A operation because of the *MSG* limitation of 65 nm LP CMOS. As CMOS transistor scaling down, the high drain efficiency and *PAE* nonlinear mm-wave PA in silicon would become a practical and attracting research area. Ideally, the *PAE* of a single-stage class E / F PA may approach 100% in the condition transistor gain is large enough. For example, mm-wave class F PA based on harmonics rejection would be a possible solution for high *PAE*. However, lossy substrate and matching components may be challenges of implementing mm-wave nonlinear PA. Another research concern can be mm-wave amplifier

linearity design. To achieve this goal, certain auxiliary components such as digital circuits need to be designed.

The author would also explore other RF components such as mixer, switch and antenna design. The goal is to integrate PA towards RF SOC solutions. In such a system level design, the reliability of integration is a primary concern since malfunction in any building block may degrade the overall performances or fail a chip. Another consideration is how to properly plan these blocks for high performance while maintaining low power consumption.

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[1] J.-A. Han, Z.-H. Kong, K.-X. Ma and K.-S. Yeo, "A 26.8 dB Gain 19.7 dBm CMOS Power Amplifier Using 4-way Hybrid Coupling Combiner," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 1, pp. 43–45, Jan. 2015.

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