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ELECTROMIGRATION STUDY OF THROUGH SILICON VIA (TSV)

SUBMITTED

BY

TAN YEOW CHONG

SCHOOL OF ELECTRICAL & ELECTRONIC ENGINEERING

A thesis submitted to
Nanyang Technological University
in partial fulfilment of the
requirements for the
Degree Master of Engineering (Research)
(Electrical & Electronic Engineering)
Nanyang Technological University
Year 2010

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Abstract

In the continuous drive for smaller chips (Moore's Law) and heterogeneous semiconductor applications, traditional processing and packaging technologies may not be able to support this trend. 3-D IC can offer a greater packing density in the same footprint as 2-D miniaturizing is reaching its physical limit.

Through Silicon Via (TSV) is one of the most promising and key enabling technology for 3-D IC. However, TSV technology puts high demands on the process module and integration. This brings about reliability issues ranging from process related such as void-free filling and scalloping of sidewalls to thermo-mechanical stress/strain induced defects during both operation and manufacturing. Numerous thermo-mechanical analyses have been reported and reliability test experiments are carried out.

In contrast with the extensive study of thermo-mechanical analyses on TSV, electromigration (EM) study of TSV is rarely reported. Recently, it is found that the driving forces for EM is not solely the current density, but temperature gradient and its resulting thermo-mechanical stress are as significant as the current density in affecting the EM of an interconnect. In view of the high thermo-mechanical stress in the TSV as has been well studied, it is worthwhile to look at the EM performance of TSV as well.

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This work is to study the EM performance of TSV in Silicon interposer application. Finite Element (FE) modeling and simulation employing ANSYS is carried out. Established models successfully applied in the area of EM in ULSI interconnects where Atomic Flux Divergence (AFD) is used as a merit of EM performance will be adopted.

Our simulation results show that both the thermal and stress migration are the dominant contributing factors to the resultant AFD in TSV instead of the current density. The value of maximum AFD is also found to be dependent on the process technology, and exhibits asymmetric behavior in simulations if different process is used between the top and bottom metallization of a TSV. Modeling is also done for 2 different coverage patterns of top metallization: (i) the metal line covers the via completely, and (ii) the metal line only extends to the centre of the via, covering half of the via. The simulation results for the latter model shows that a possible second EM failure site of sufficiently high AFD exists and worse EM performance is obtained as compared to the first model. The second possible EM failure site is further confirmed through dynamic simulation of void growth for the second model.

A new method of resistance measurement based on the Kelvin Double Bridge has been proposed. Comparison has been made with different common resistance measurement methods and calculations using examples show that the proposed method can be superior by being very accurate and sensitive, especially when the surrounding horizontal interconnects are more resistive than the vertical interconnect in a multi-layer structure.

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An in-house EM tester has also been designed and built for the purpose of future TSV EM tests. The in-house tester is capable of sourcing high currents up to 3A, with the ability to isolate and "short" over a failed device belonging to a daisy-chain, thus allowing continuously testing on the "surviving" TSVs, thereby rendering better accuracy in lifetime measurement due to the larger number of time-to-failure data for individual TSV and increased throughput of each test.

Lastly, some guidelines are proposed for future EM test structure design by considering all the conclusions made in different aspects of study in this work.

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Acknowledgement

I will like to express gratitude for my supervisor, Associate Professor Tan Cher Ming, for his valuable guidance and insight for this project. He has shared his extensive experience in the EM reliability field during numerous discussions and meetings. Without him, this project will not be possible.

Secondly, I wish to show appreciation to the collaborating IME team, especially my co-supervisor, Dr Zhang Xiaowu. Special mention also goes to Dr Yu Daquan, for arranging and attending the monthly meetings and responding swiftly to any queries regarding the project. Mr Chai Tai Chong also offers suggestions and valuable inputs to the project direction.

Next, I am thankful for being awarded the scholarship from Singapore Economic Development Board (EDB) and Systems on Silicon Manufacturing Co. (SSMC) to pursue a higher degree under the Joint Industry Postgraduate Program.

I am also glad to have met some good company and treasures the valuable discussions with my fellow research students Dr Hou Yuejin, Dr Li Wei, He FeiFei, Fu Chunmiao, and Xu Mingjie. Some have contributed greatly to the technical aspect, while others have been great fun to be with. Next, I thank the lab staff for their assistance in logistics.

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Lastly, I am grateful to my wife and my family, for their support and understanding despite the busy schedule of the project. I would not have made it without them.

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Chapter 1 Background

1.1 Importance of Reliability

In the world today, designing products with optimized performance at reasonable cost and yield is no longer sufficient. Reliability of the product is also important to customers and reputation of the product allows an edge over others with the stiff competition in today's manufacturing industry.

Designing reliability in the early stages also offer advantages such as shortened time to market and higher yield can be achieved, which is a very critical subject of interest in manufacturing. However, reliability assessment using experimental setup can be expensive with limited resources such as time and financial costs. It has long been acknowledged that modeling and simulation is an essential part in product development for the purpose of predicting the product's reliability prior to production. Results of a recent questionnaire and survey performed targeting 140 industrial TCAD (Technology Computer Aided Design) users show an estimated 30-40% reduction in both cost and time for the technology development, and the savings are observed to be increasing from 2007 onwards [1].

Reliability modeling is a key factor to shorten development cycle time and ensure the performance of the product within the specifications [2]. In the recent 2009 ITRS Edition "Modeling and Simulation" chapter, a sub-chapter of reliability modeling has been newly included to recognize its role in the increasing

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importance for more robust reliability margins, in addition to the purpose of achieving better device performance traditionally.

The world today is mainly driven by high technology products comprising of integrated circuits (IC). These microelectonics based products accompany the advancement of humankind and are used in everyday's activities where failures resulting from unreliability can have consequences and impacts of varying seriousness. In a simple case, compensation under warranty and monetary losses from the affected company's stocks are not unheard of; but loss of human lives can happen in cases when the pacemaker fails in a heart patient or a catastrophic plane crash due to electronic failure for example.

Interconnects are an essential constituent of integrated circuits and they occupy a significant part of the total die area. It has been reported that the continuous scaling down has the biggest potential negative impact on device reliability [3]. With increasing complexity in integrated circuits, the individual components must become increasingly more reliable if the reliability of the whole system is to be acceptable [4].

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1.2 Trend in IC Packaging

1.2.1 Introduction

For several decades, the semiconductor industry has focused on reducing the minimum feature size to improve device performance and increase density. The well-known Moore's Law [5] states that "The number of transistors incorporated in a chip will approximately double every 24 months." To date, the industry has been using this as a guideline for their research and development, resulting in smaller and faster chips with more functionality.

In the continuous drive for smaller chips and heterogeneous semiconductor applications, traditional processing and packaging technologies may not be able to support this trend [6, 7]. Scaling has resulted in shorter gate delay and increased device density, but the same performance enhancement does not apply to interconnects. Even if the process challenges, material issues, and reliability problems accompanied with scaling of both device and interconnects were overcome, interconnect scaling will still degrade interconnect delay. In Figure 1, it can be seen clearly that there is no significant benefit and even degradation in terms of overall speed beyond 0.25µ technology for Cu/low-k ULSI where interconnect delay starts to dominate overall device gate delay. Furthermore, miniaturization also places the interconnects closer to each other, thus interconnect crosstalk is increased significantly. Reverse scaling of the interconnects have been investigated to reduce RC delay, but the self-inductance in global signal interconnects has to be considered at device operation of gigahertz clock frequencies [8].

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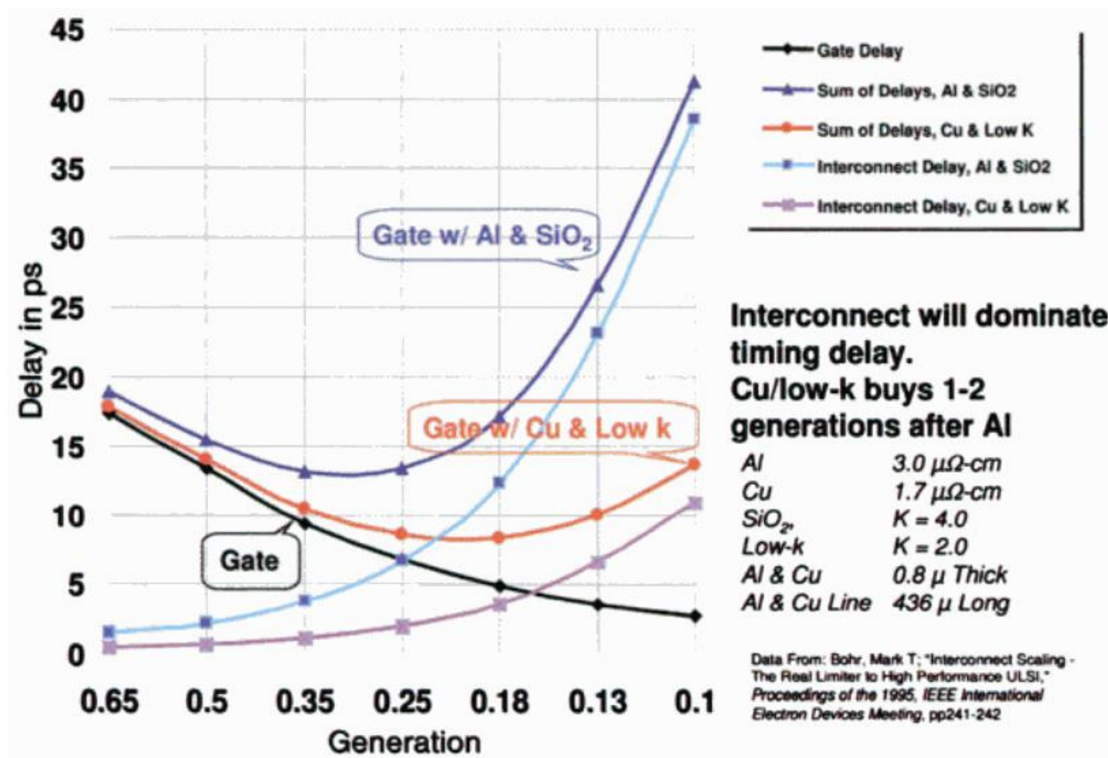

Figure 1. Interconnect delay vs IC node. [9]

In view of the problems accompanying the semiconductor technology node advancement, the industry have looked into other ways of increasing chip density, such as novel packaging methods. 3-D IC can offer a greater packing density in the same footprint as 2-D scaling is reaching its physical limit. With 3D stacking, the shortened chip-to-chip routing speeds up communication to a certain extent compared to a 2-D board solution. Traditional implementations of 3-D architecture include stacked dies, package on package technology, and flip chip packaging. Typical representations of these technologies are shown in Figure 2. However, these technologies are associated with the use of wire bonding, limited heterogeneous application, substrate warpage and increase in package height [10]. Overall, these technologies can alleviate some of the challenges faced in 2-D miniaturizing, but there is still a certain degree of inflexibility with regards to the

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placement and I/O count of the wirebonds which are typically limited to the chip peripherals. Furthermore, the parasitics associated with the interconnects are only reduced from that of 2D architecture, but not minimized.

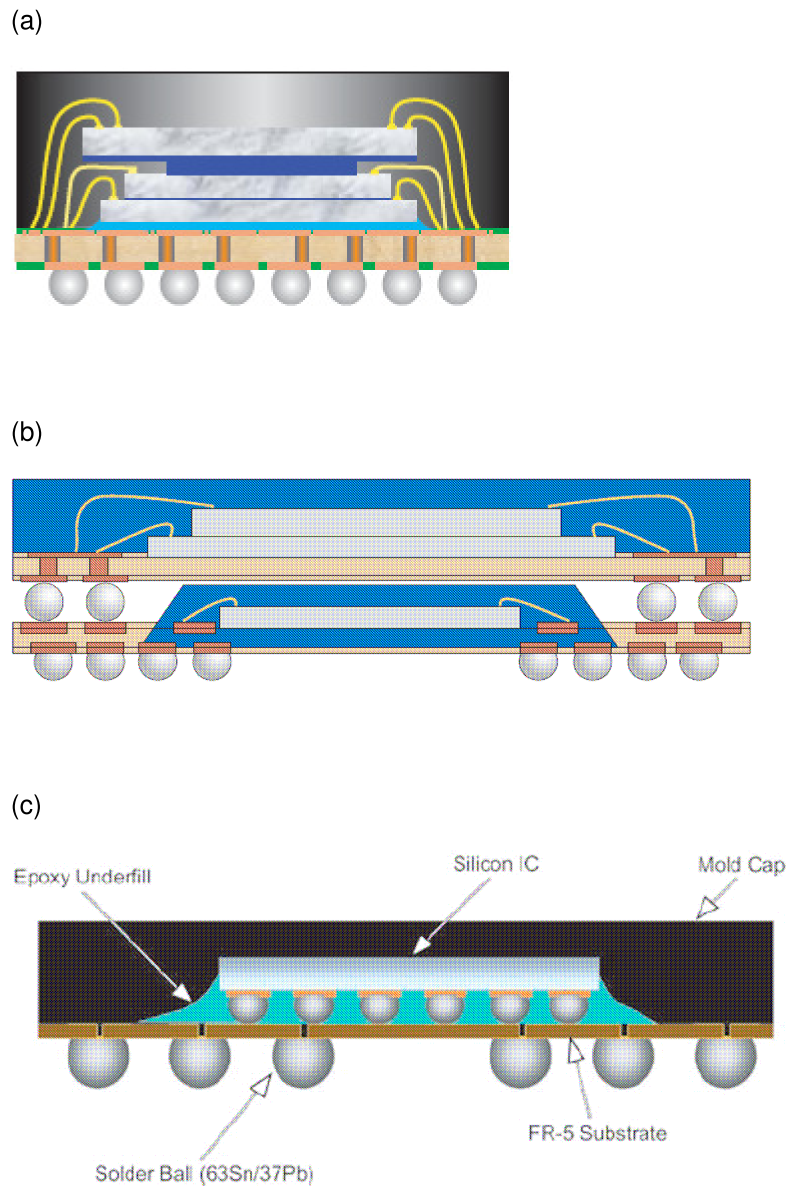

Figure 2. Typical representations of: (a) Stacked die chip-scale package, (b) Package-on-Package, and (c) Flip-chip. (Pictures courtesy of Amkor Technology)

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1.2.2 "True" 3D Integration – Through Silicon Via (TSV)

It has been regarded that the traditional 3-D implementations as mentioned in the previous section is strictly "3D Packaging" [11]. Recently, 3D integration is hotly pursued by the semiconductor industry. TSV is one of the most promising and key enabling technology for 3-D IC [12]. It can be the ultimate solution to overcome the challenges faced by traditional 3-D implementations. Unlike "3D Packaging" in which a signal has to travel over longer interconnects, TSV allows a *direct vertical* connection between die, resulting in even faster data rate and reduced power consumption. This is termed as "3D integration".

Traditional wirebonding connections for "3D Packaging" are limited to the periphery of the chips and the resolution of wire bonders can further limit the I/O density. Also, it can be seen from Figure 2 that spacers are often necessary if the higher level chip is bigger or same in size as the lower level chip, thus further increasing the overall height and packaging costs However, these issues are not applicable to a 3D architecture using TSV solution. With TSVs, the interconnections are no longer limited to the chip's periphery and these interconnections are only as short as the thinned down chip.

3D integration also allows for heterogeneous chip interconnection [13, 14], whereby thinned wafers of different specific functions including mixed signal and/or mixed technology designs are aligned and vertically interconnected to realize a functional system. The different layers which can be of different substrate materials are made very thin, and the TSVs can be placed to allow for shortest interconnection between functions. As seen in Figure 3, the TSV array is

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capable of very attractive form factor compared to traditional wire-bonding and/or chip stacking techniques.

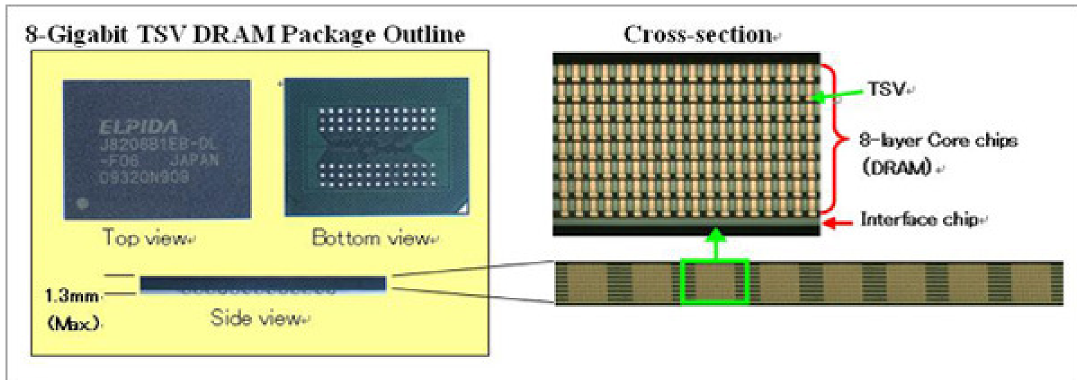

Figure 3. Cu-TSV Multi-Layer 8-Gigabit DRAM. [15]

There is also considerable interest for TSV application as interposers for chip-to-board interface. The package level interconnection density of traditional substrates are not able to keep up with the increase in chip interconnection density [12]. A silicon interposer with TSVs can act as a redistribution layer between the relatively fine-pitched on chip pads and the relatively larger-pitched pads on the substrate [16]. Besides having better electrical performance when using TSVs as described previously, better matching of the coefficient of thermal expansion (CTE) between a silicon carrier with TSVs and the chip can also help reduce the thermal and mechanical challenges of matching ICs of dense interconnects with a PCB of standard or advanced area-array pitches [17]. Figure 4 shows a representation of such a Si interposer with TSVs.

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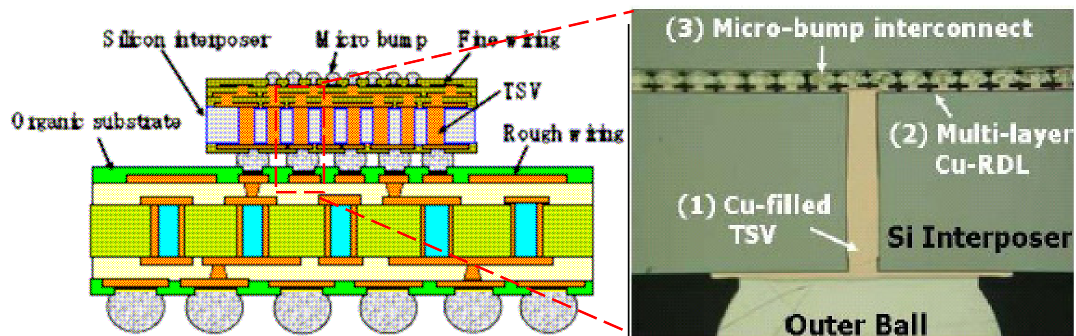

Figure 4. Silicon interposer with TSVs: (a) Schematic [18], (b) Micrograph [19].

1.3 Motivation

It has been shown that TSV has a lot to offer and thus the industry is moving towards commercializing this technology [20-22]. Nevertheless, TSV technology puts high demands on the process module and integration [23, 24]. This brings about reliability issues ranging from process related such as void-free filling and scalloping of sidewalls to thermo-mechanical stress/strain induced defects during both operation and manufacturing. As such, there is a huge amount of work done on the reliability of TSVs, especially in the area of thermo-mechanical reliability.

The presence of defects might aid in the EM process of vacancies accumulation and voids formation during subsequent operation. This may be even more evident in the relatively more complex TSV structure. However, there is a lack of reported and published work for electromigration (EM) in TSV up to date.

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Besides the thermo-mechanical aspect of reliability, EM has always been important and remains to be a major reliability issue in integrated circuit chip level interconnection. EM is a phenomenon where mass transport occurs in metallic conductor through diffusion under application of current. The mass transport causes local accumulation and/or depletion of the metallic conductor material, which can induce parametric or even functional failure.

While thermo-mechanical analyses on TSV is rather extensive, EM study of TSV is rarely reported due possibly the belief that EM is not important for TSVs as they are much larger than the adjacent metallizations as compred to a typical Cu/low-k line via structure. As a result, the current density in TSV is so much smaller than that in the lines connected to it, and it is believed EM will occur in the lines first before TSV starts to suffer from EM failure. Recently, it is found that the driving forces for EM is not solely the current density, but temperature gradient and its resulting thermo-mechanical stress are as significant as the current density in affecting the EM of an interconnect. In view of the high thermo-mechanical stress in the TSV as has been well studied, it is worthwhile to look at the EM performance of TSV as well.

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1.4 Scope and Contribution

This work is collaborated with Institute of Microelectronics (IME) Singapore, A*STAR. The main purpose is to study the EM performance of TSV in their Silicon interposer application for chip-to-board interface. An EM study by just performing experiments will be difficult and costly as resources are very limited. Therefore, simulation and modeling will be employed first to identify possible locations suffering from EM damage.

The objective of this work is to study the effect of EM on TSV and the dependence of EM severity on TSV structure design using simulations. With the insights gained from performing EM simulations, an EM test structure for the studied TSV for Si interposer application will be proposed. IME has included this proposed structure in the EM test portion of their planned reliability test chip which includes various other test structures such as piezo-resistive stress sensors, die crack sensors, surface insulation comb and triple track structures etc.

To the best of the author's knowledge, study of EM in TSV is very rarely reported. Thus this work can be a starting point for future research in this specialized area. Experimental data has not been included in this work as samples have not yet been obtained. However, this thesis will discuss some potential problems with proposed solutions that may be encountered during EM testing of the TSVs. An in-house EM tester has been designed and built which will be described in this thesis.

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Chapter 2 Literature Review

2.1 Reliability of TSV

The reliability of interconnects have been discussed in Chapter 1 and its importance cannot be further stressed. It is noted that TSV is an enabling technology to form z-axis interconnects for the adoption of 3D integration. As with all new interconnection technologies which are accompanied by extensive reliability studies, there is also much work done on the reliability of TSV. This section will cover some of the work done on the TSV reliability, with special emphasis on the thermo-mechanical challenges and issues in TSV.

2.1.1 Thermo-mechanical Reliability

In a copper-filled TSV, the surrounding materials include the barrier metal, the oxide insulation, BCB and the silicon bulk. A lot of thermo-mechanical modeling have been done due to the potential reliability concern caused by coefficient of thermal expansion (CTE) mismatches, especially the huge difference of CTEs (>5x) between the Cu TSV and its surrounding Si body. As a result of the mismatch, the induced stress/strain under thermal loading can cause delamination at the interface between the TSV and Si.

Ranganathan et al. [25] studied and evaluated experimentally on the impact of sidewall roughness and scalloping. Using electrical leakage current as a merit, it was shown that a hybrid Si etching process to reduce the sidewall roughness

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exhibits better electrical leakage characteristics. They also reported high thermo-mechanical stress at the corners of the via (see Figure 5) and that higher leakage current is measured when the temperature during measurements is increased.

Jürgen Wolf et al. [26] used FE simulations to predict the thermo-mechanical stress and provide first reliability estimations. In their model, they recreated the impact on both stress and strain of each individual process step. They identified some regions of interest which have high equivalent stress and equivalent plastic strain. It was concluded that the stress and strain has a strong dependence on process temperature and that it is advantageous in this aspect to have a low temperature process. Ramm et al. [27] reported similar findings at the same time and also investigated using Cu and W as different material for the TSV filler. They highlighted the thermo-mechanical advantage in the bulk of the TSV when using W instead of Cu as material for TSV filler due to much better matching of CTE (<2x) with Si. Moving away from the bulk of the TSV, however, there is an inverse effect of CTE mismatch at the interface between the via and Cu metallization. They concluded that experimental verifications are needed before a decision can be made on which is the more critical area, and adjust the process correspondingly.

Selvanayagam et al. [28] studied the impacts of thermal mismatch in TSV arrayed silicon interposer. In their work, they considered two cases consisting of local mismatch arising from individual TSV and global mismatch from the interposer. They reported the high stress/strain compounded with any process imperfections can result in mechanical failure. The increased in copper content for silicon

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interposer containing TSVs also cause an increase in the interposer's effective CTE. This can result in a further mismatch between the interposer and chip.

Lu et al. [29] observed stress-free points after studying the stress distribution and its interaction in TSV arrays. He suggested that by properly arranging the array, the area of "keep-away-zones" (see Figure 6) with stress high enough to damage devices can be optimized, and yet retaining the same TSV density.

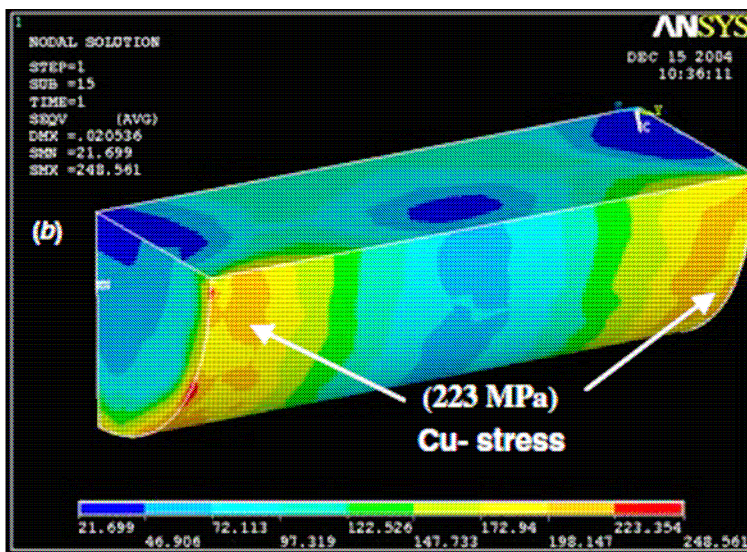

Figure 5. High thermomechanical stresses concentrated at the top and bottom regions of the via. [25]

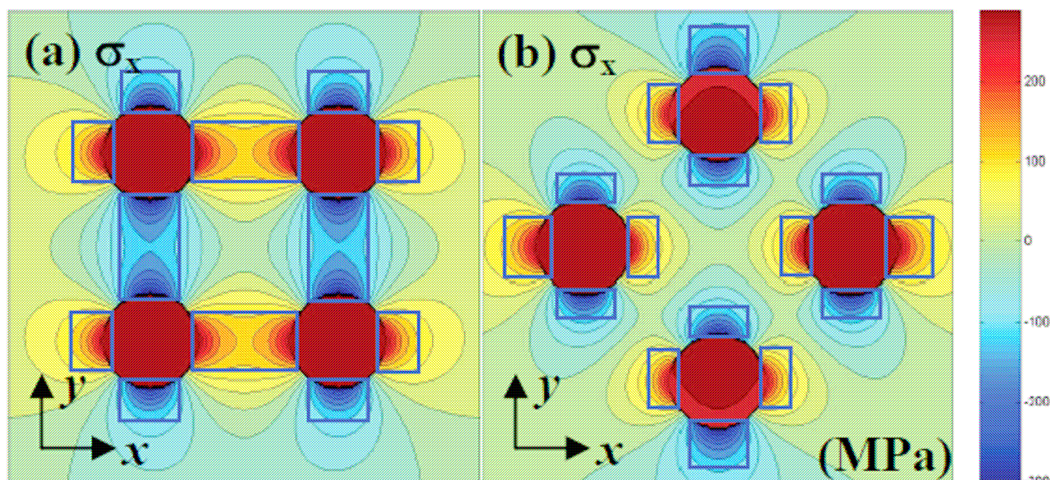

Figure 6. Different array arrangement resulting in reduction of area occupied by high stress "keep-away-zones" which are highlighted in blue box. [29]

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2.1.2 Mechanical Reliability

During chip-stacking in 3D integration, the process of mechanical bonding between inter-layer Au bumps and intra-layer Cu TSV can damage the TSV or cause the die to crack. Tanaka et al. [30] carried out simulations and similar experiments and emphasize that the loading force be properly applied in order to avoid such damage. They reported that even though high shear stress is generated at the edge between Cu TSV and Au bump, this stress rapidly decreases inside the silicon chip. Experimental verification confirmed and demonstrated that the Cu TSV should be able to withstand the mechanical shock under typical bonding conditions.

From the literature review, both thermo-mechanical and mechanical aspect of TSV reliability are well studied and a lot of work is concerning the thermo-mechanical issues in the TSV. However, there is a lack of reported work in the aspect of EM reliability. It is also worthwhile to note that most of the published reliability studies on TSV are based heavily on finite element analysis (FEA) and simulations. This may be due to some difficulties of carrying out expensive experiments on actual samples, especially when the technology is still not mature. In comparison, performing simulations allow for flexibility of studying a variety of factors and a particular field of interest as well demonstrated in the various works. In the reviewed literature, finite element analysis (FEA) is a very common simulation tool for TSV reliability study. Therefore, this work will also concentrate on using simulations to study the reliability of the IME fabricated TSV in Si interposer.

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2.2 Electromigration in ULSI Interconnect

2.2.1 Introduction

Electromigration (EM) has always been important in integrated circuit chip level interconnection and remains to be a major reliability issue. EM is a phenomenon where mass transport occurs in metallic conductor under application of current. This phenomenon is best observed under accelerated conditions where the metallic conductor is stressed with high current density and high temperature. Because an interconnet's EM lifetime under normal operating conditions has to be 10 or more years [31], EM tests are typically conducted under these accelerated conditions to obtain accelerated lifetime data in a reasonable time and estimate meaningful field operation lifetime through statistical analysis and extrapolation. These accelerated lifetime testing experiments generally involve the resistance monitoring of the device under test (DUT), through which the test structure is considered to have failed when its resistance increases to a predetermined value.

In Chapter 1, it was established that the move towards 3D integration with TSVs is inevitable and there is a need to look into its EM issue as with all new interconnect technologies. Due to the lack of reported work on EM in TSVs, we will limit our discussion and find relevance from what is learnt in the EM study for ULSI interconnects. From literature, the stressing current density ranges from 10^4A/cm^2 to 10^6A/cm^2, depending on the material of the interconnect under test such as Al interconnect, Cu interconnect, and PbSn solder joint etc [31, 32]. Caution is also taken to limit the stressing temperature such that the local temperature which includes joule heating within the interconnect, does not increase the DUT

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resistance significantly arising from the temperautre dependence of the interconnect resistance. Otherwise, "false" failure can result if the failure criterion is too stringent. In the extreme case of temperature high enough to exceed the melting point of the interconnect material, failure observed will be due to undesired failure mechanism yielding erroneous results. As such, a reasonably good estimation can usually be obtained from performing iterations of thermal-electric simulations at different test temperature.

2.2.2 EM induced Failure

EM induced mass transport causes localized accumulation of atoms or vacancies, resulting in hillocks and voids formation respectively. Figure 7 shows a schematic and micrographs of a void and a hillock. Hillocks can result in short circuit between adjacent interconnects while voids in the interconnects cause increased resistance and can even result in open circuit. Increased resistance in interconnects decrease circuit performance and may be flag off as parametric failure, even though open circuit condition has not been reached. On the other hand, short circuit caused by hillocks and open circuit in the event of severe voiding respectively will result in functional failure.

The more prominent electromigration related failure mode in current processing technology is failure due to formation and accumulation of voids instead of short circuit failure mode due to formation of hillocks [31]. This is attributed to the presence of harder layers like the top passivation layer and surrounding metallic barrier layer in modern Cu DD process which can suppresses hillocks formation

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[33]. Also, the shrinking line width probably makes it easier for voids to reach a critical size large enough to cause EM failure [31].

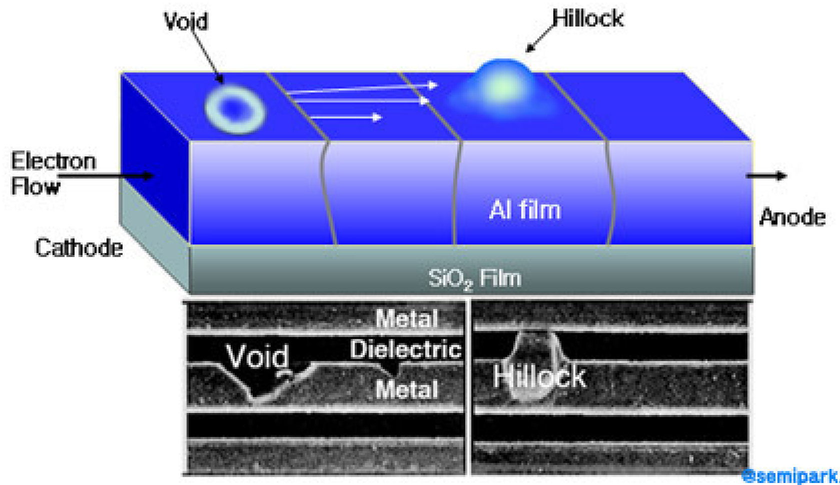

Figure 7. Void and Hillock. [34]

2.2.3 Theoretical Description and Modeling Physics of EM in modern ULSI Cu Interconnects

Since the earliest works on EM by Fiks [35] and Huntington and Grone [36], the theory of EM and its model has been refined. The mass transport in EM is now attributed to the interaction among various driving forces (the driving force approach), which results in atomic flux (AF) and divergence (AFD). The dominant driving forces that are considered in EM modeling for Cu include electron wind force induced migration (EWM), temperature gradient induced migration (TM), and thermo-mechanical stress gradient induced migration (SM) [31, 37].

Electron wind force (EWF) represents the force experienced by metal ions in the conductor due to momentum exchange between these ions and moving electrons in

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the electron flow direction. The EWF experienced in a thin film metallization is especially large, due to high current density in the small cross-section. Huntington and Grone studied and theorized the existence of electron wind force where they observed marker motion of light transverse scratches in gold wires, which always occurs towards the cathode and appears to be proportional to the current density [36].

The contribution of thermal effects to EM has to be recognized because there is very low atomic mobility at very low temperature [32]. Temperature gradient can cause mass transport as atoms tend to move from a high temperature region to a low temperature region. Thermal gradient can arise in the metallization due to joule heating in the presence of electrical current and also the non-uniformity of physical shape, structure and inhomogeneous surrounding material. With current crowding at abrupt changes in the structure such as meanders and corners, EM is enhanced due to the higher EWM at these current crowding locations. The situation can worsen as voids start to grow, which results in higher current crowding and simultaneous joule heating reinforcing each other at the vicinity of voids [38]. The non-uniform interconnect structure such as line-via and the inhomogeneous material can also act as source of thermal gradient because of the larger Cu plug acting as a heat sink with surrounding materials of different heat conductivity.

Thermo-mechanical stress stems from the thermal mismatch of the metallization material with its surrounding materials. The non-uniform thermal distribution in the test structure induces a thermo-mechanical stress gradient when it is subjected

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to raised temperature in EM test conditions. It has been reported that the presence of this stress significantly shortens the EM lifetime [39, 40].

Atomic fluxes due to these various driving forces can occur in the interconnect as described above, especially where there is structural and material inhomogenity and discontinuity. Net mass transport occurs only when the resultant divergences is non-zero [32]. When the resultant AFD is positive, mass depletion will be observed; whereas mass accumulation is defined by negative AFD. S. Rzepka et al. and Dalleau et al. pioneered the work to combine these 3 driving forces and used them in finite element (FE) models to evaluate EM reliability [37, 41]. Tan et al. [31, 42] manifested this approach and brought to attention that both TM and SM are at least as significant, if not more than EWM, which was traditionally considered to be the sole driving force for EM. In their work, they compiled experimental evidence from reported literature and verify their calculation and simulation to show that TM and SM were mistakenly considered to be just a supporting role to modify EWM, but are in fact potential driving forces during EM [43].

Detailed formulation of the divergences is reproduced below. Equations (1) – (3) represent the AF due to EWM, TM and SM respectively; and equations (4) – (6) represent the AFD due to EWM, TM and SM respectively. Various works have validated this model with experimental observations showing that AFD simulations can predict EM failure locations in ULSI interconnects accurately [42, 44].

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$$J_A = \frac{N}{k_B T} Z^* e \rho D_0 \exp\left(-\frac{E_A}{k_B T}\right)\vec{j} \tag{1}$$

$$J_{th} = -\frac{NQ^* D_0}{k_B T^2} \exp\left(-\frac{E_A}{k_B T}\right)\nabla T \tag{2}$$

$$J_S = \frac{N\Omega D_0}{k_B T} \exp\left(-\frac{E_A}{k_B T}\right)\nabla \sigma_H \tag{3}$$

$$div(J_A) = \left(\frac{E_A}{k_B T^2} - \frac{1}{T} + \alpha \frac{\rho_0}{\rho}\right) J_A \nabla T \tag{4}$$

$$div(J_{th}) = \left(\frac{E_A}{k_B T^2} - \frac{3}{T} + \alpha \frac{\rho_0}{\rho}\right) J_{th} \nabla T + \frac{NQ^* D_0}{3 k_B{}^3 T^3} j^2 \rho^2 e^2 \exp\left(-\frac{E_A}{k_B T}\right) \tag{5}$$

$$\begin{aligned} div(J_S) = {} & \left(\frac{E_A}{k_B T^2} - \frac{1}{T}\right) J_S \nabla T + \frac{2E\alpha_l N\Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right)\left(\frac{1}{T} - \alpha \frac{\rho_0}{\rho}\right)\nabla T^2 \\ & + \frac{2E\alpha_l N\Omega D_0}{3(1-\nu)k_B T} \exp\left(-\frac{E_A}{k_B T}\right) \frac{j^2 \rho^2 e^2}{3 k_B{}^2 T} \end{aligned} \tag{6}$$

where, N is the atomic density,

k_B is the Boltzman constant,

T is the local temperature,

Z^* is the effective charge number,

e is the fundamental electronic charge,

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ρ is the temperature dependent electrical resistivity given as $\rho = \rho_0 [1 + \alpha (T - T_0)]$, and α is the temperature coefficient of resistivity, ρ_0 is the electrical resistivity at temperature T_0,

D_0 is the prefactor of the self-diffusion coefficient,

E_A is the activation energy for the self-diffusion,

j is the local current density,

Q^* is the heat of transport,

Ω is the atomic volume ($\Omega = 1/N$),

σ_H is the local hydrostatic stress given as $\sigma_H = \frac{1}{3}(\sigma_{11} + \sigma_{22} + \sigma_{33})$

E is the Young's Modulus,

α_l is the thermal expansion coefficient (CTE),

ν is the Poisson ratio,

of the interconnect material.

It has been derived theoretically that EM lifetime is inversely proportional to the AFD [45] and thus the magnitude of AFD represents how fast or slow that mass transport is occurring. Practically, the site of maximum positive AFD is assumed to be the location of void nucleation at the onset of EM and the void grows irreversibly.

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2.2.4 Finite Element (FE) Modeling

The use of advanced computing hardware and software is a great aid to the understanding and predicting of many physical phenomena. Finite element analysis (FEA) software allows structures to be realistically modeled and their corresponding behavior under specified boundary conditions can be simulated.

In many engineering problems, the physical phenomenal associated can be described with differential equations, but these equations are complex to solve. A numerical technique to find approximate solutions of partial differential equations (PDE) and integral equations is the finite element method. This method necessitates the sub-division of the continuous domain describing the problem into a mesh consisting of discrete elements and nodes, simplifying the PDE into a system of ordinary differential equations, which are then numerically integrated using standard techniques.

He et al. noted the inadequacy of various 2D-based modeling and simulation tools for the purpose of EM reliability [46]. This is mainly due to the incorrect over-reliance on just current density as the sole driving force for EM, and also inaccurate assumption of ignoring the coupling of stress evolution from the interconnect's surrounding. It has been reviewed in Section 2.2.3 that thermo-mechanical stress gradient is the most significant driving force for EM. From these reasons, together with the complexity of TSV structure, there is thus a need for 3D modeling to allow us to better model the complicated EM physics. In this research, ANSYS® is used to solve for the interactions among the various driving forces described in the previous section. ANSYS® is a very popular FEA software

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with multi-physics capability and is used extensively by both the industry and research community. Many works dealing with EM also employ ANSYS® for simulation.

ANSYS® has a vast library of element types. Each element type has a degree of freedom set, which constitute the primary nodal unknowns to be determined by the analysis [47]. Therefore, a suitable element type has to be chosen for different discipline of study applicable to the engineering problem such that its degrees of freedom (DOF) are sufficient to characterize the model's response.

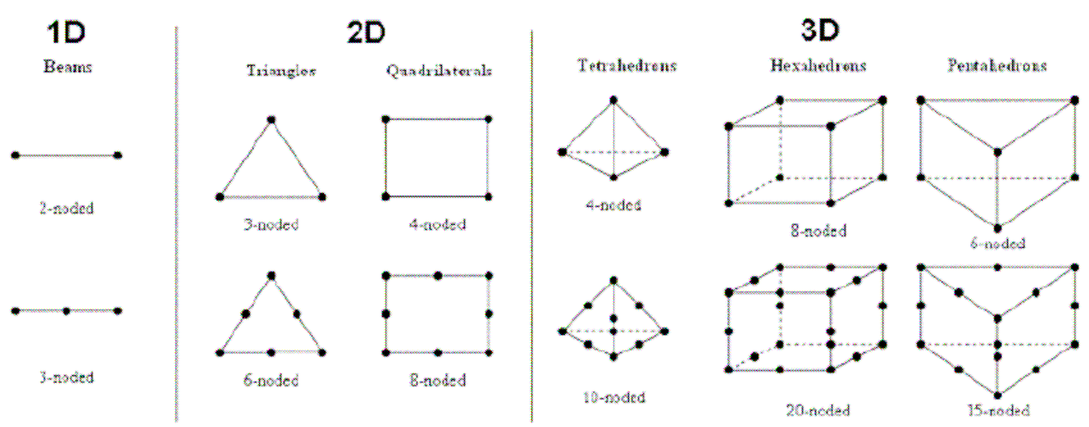

Figure 8. Basic elements in ANSYS. [47]

There are different element shapes for different element types, and some element types can have multiple options. Elements that have midside nodes in addition of the corner nodes are known as quadratic elements whereas those without midside nodes are linear elements. In general, besides choosing the element type based on their degrees of freedom, the choice of model such as 2D/3D; linear/quadratic; tetra/hexa; are as important. Using higher order elements ie. quadratic instead of linear elements yield the most accurate results in some applications, but are very

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computationally expensive [48]. Similarly, the higher the mesh density, the more computing resource and/or time will be needed to reach the solution. However, it is important to note that having more elements in a mesh will allow for more available nodes in calculating the response of interest and subsequently, reaching a more precise solution. It is common practice to perform an empirical pre-study on the mesh size sensitivity whereby a suitable mesh size is chosen when further mesh size reductions add no benefit to the solution under the same loading conditions [49].

2.2.5 EM Test Structure

It is important for EM test structures to be designed as close as possible to the actual structure. A test structure which is significantly different from reality may alter the actual failure mechanism, resulting in "false" information. An IC in today's technology consists of a few layers and a multilevel interconnection system. To draw relevant reliability data, line-via type structures are often used instead of single level planar type such as the Blech [50], NIST [51] and SWEAT [52] test structures. The Blech EM test structure (see Figure 9a) is typically used for "edge displacement" experiments where migration is observed and EM drift velocity can be determined. The NIST EM test structure in Figure 9(b) shows a straight metal strip with Kelvin type connections available for accurate resistance measurement. The careful design of the actual length of metal strip and placement of pads allow for good temperature profile control. In the SWEAT EM test structure (see Figure 9c), a series of alternating wide and tapering narrow regions is designed such that high temperature gradient and current density can be

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generated in the transition regions. This results in a highly accelerated EM test where EM lifetime results can be obtained in a relatively short time.

While there are several pitfalls associated with the SWEAT test structure and method reviewed by Tan and Yeo [53], the Blech test structure is still good for use when the study is to determine EM drift velocity; whilst the NIST test structure is strictly used to study various aspects of EM on just the line itself [54]. However, for observation of EM failure modes in a multilevel interconnection system such as TSV for 3D integration, we shall limit our discussion to the multi-level type of test structure.

Figure 9(d) shows an example of such a line-via test structure most widely used today. They are differentiated between “M1 testing”, where the electron flow is downstream stressing the M1 test line; and “M2 testing”, where the electron flow is upstream stressing the M2 test line [31]. In addition, the “dummy” lines on the opposite level of the line under test of each corresponding test type are often made short to observe the “Blech Effect” [50, 55], minimizing the occurrence of failure in these lines. “Blech Effect” is so termed due to the work by Blech and his co-workers which he proposed and quantified that a threshold-length product relating the current density and conductor length, where EM mass transport will cease. In particular, at a given EM stress condition, there exists a threshold conductor length, the “Blech Length”, where the backflow flux due to stress or concentration gradient is large enough to balance the opposing mass transport flux due to electric field. It also coincides with the observation of why there is little or no EM transport observed at low current density. The “Blech Effect”, also known as the

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"short length effect", explains the purpose of having "dummy lines" in the respective EM test structures.

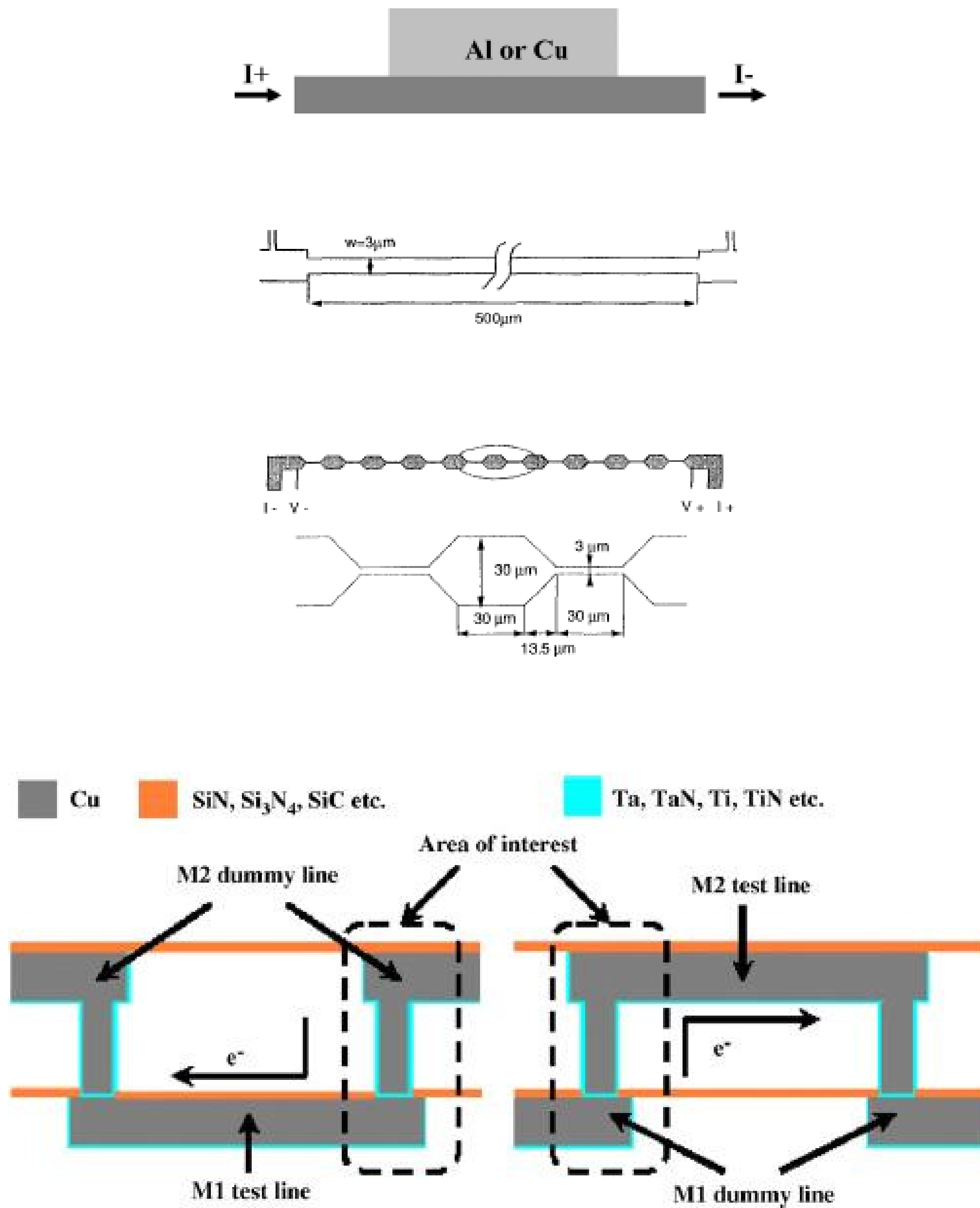

Figure 9. Schematics of (a) Blech (vertical plane view), (b) NIST (top view), (c) SWEAT (top view), and (d) M1(downstream) and M2(upstream) test structure. [31, 52]

A variation from the single test structures is the daisy-chain type of test structure. It consists of multiple DUTs in series in a single daisy-chain. Therefore, the

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current that flows through each DUT is the same in magnitude. The main feature of a daisy-chain type of EM test structure is that both "upstream" and "downstream" stressing are carried out simultaneously, as the electron flow is opposite in direction between each adjacent DUT. However, caution must be exercised when analyzing the reliability data because there may be a bimodal failure distribution due to the alternating direction of current flow in adjacent DUTs in the chain and detailed physical failure analysis has to be carried out. Alternatively, the daisy-chain type can be fabricated such that the layer of line not under test is designed to be significantly shorter than the layer of line under test to observe the "Blech Effect". In this way, the daisy-chain type of test structure can be used for just M1 or M2 testing.

In EM tests using daisy-chain type of test structure, the resistance measured includes all the DUTs in the chain. There is a practice of assuming that majority of the resistance increase is due to the DUT suffering from the worst EM damage. This is also known as the "weakest link model". The disadvantage of practicing such method is that it may be difficult to determine the location of EM failure, and also in identifying the failure mode if the failures are sensitive to current polarity. As such, detailed post mortem or advanced techniques such as using OBRICH (optical beam induced resistance change) has to be carried out to locate the physical failure and also confirm the assumption of adopting the "weakest link model". Furthermore, the remaining DUTs except the failed DUT will have to be deconvoluted from the lifetime data through statistical means. Also, the pitfall in such an assumption is that an apparent increase in the daisy-chain's resistance as measured up to the failure criterion could be due to the sum of much smaller

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resistance increase of multiple TSVs. This will result in obtaining a severe underestimation of time to failure.

A work-around to increase the data from the same population size is by having dedicated voltage taps to monitor the resistance across individual DUTs. The failure can also be easily isolated by comparing the individual voltage (resistance since current is the same due to series connection) in this manner. In the case where the EM lifetime distribution is bimodal, particularly when due to current polarity, the failure data can be easily separated from each current direction and methods have been developed to achieve respective data relevant to each mode [56]. Furthermore, isolation of the failed DUT allows the possibility of finding a way to bypass such a failed DUT so that stressing can be continued on the surviving DUTs.

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Chapter 3 Modeling

3.1 EM Test Vehicle Design

This project is a collaboration with IME-Singapore, A*STAR. One of the early objectives that were set up is to provide EM reliability assessment to their TSV in interposer technology. For EM reliability study, actual experimental results are desired to constitute a more comprehensive study.

However, EM study by just performing experiments will be difficult and costly since resources are very limited. Thus, modeling and simulations can be done first to decide the possible area of study, and also complement the future experimental data. Furthermore, established models have been successfully applied and verified in the area of EM in ULSI interconnects (see Section 2.2.3).

Preliminary simulations were performed to identify locations of high current crowding and extensive review of past work concerning EM in Cu interconnects was done. It was noted that the test structure should mimic the actual fabricated device closely for an accurate reflection of its EM reliability during EM testing. However, it is preferable to have some degree of variation included in the study so as to further enhance understanding, in addition of the assessment.

In literature, it was reported that thermo-mechanical stress is a huge contributing factor driving EM and it will be of great interest to look into this. Unfortunately,

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actual in-situ stress distribution is difficult and almost impossible to measure. Therefore, we seek to find a straight forward method to vary the thermal gradient, indirectly altering the thermo-mechanical stress while keeping other variables constant such as dimensions of the structure for fair comparison. This will be illustrated in Section 4.

After discussion with the fabrication team in IME, it was decided to have a daisy-chain of 10 TSVs comprising of alternate short/long length of top metallization coverage. The reason for having a difference in the length is to effectively vary the thermo-mechanical stress distribution in adjacent metal lines. It is planned to carry out a packaged EM test in an oven. A schematic of the EM test vehicle portion is depicted in Figure 10. Constant current will be forced between the ends of the chain with multiple supply vias to split the supply current, minimizing the occurrence of premature failure of vias other than the TSVs under test. Voltage taps are available between each adjacent TSVs under test so that readings across each via can be made. In view of the fab's process capabilities, the TSV structure and its physical dimensions is described in Figure 11.

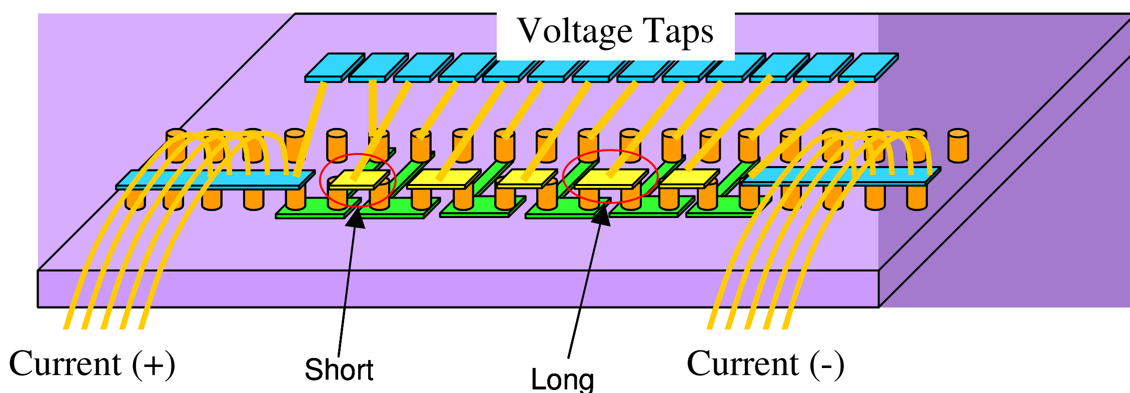

Figure 10. EM Test Vehicle Design. (Diagram courtesy of Dr Daquan Yu, IME-Singapore, A*STAR)

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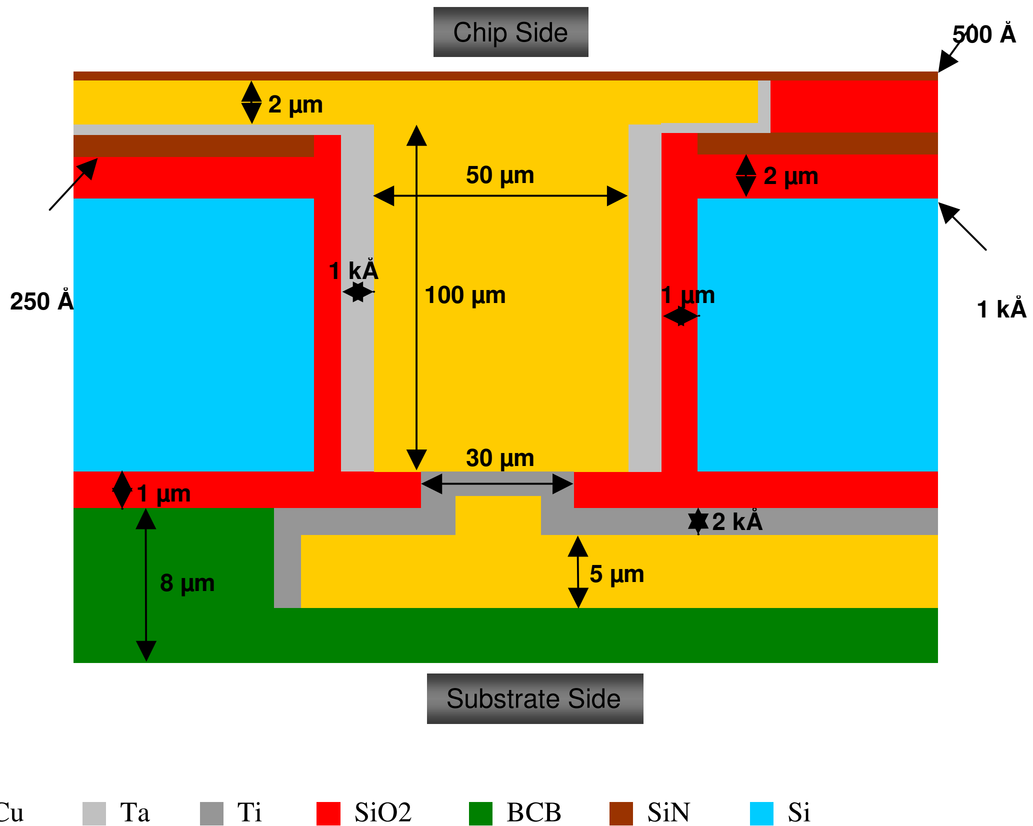
3.2 Model Description

3.2.1 Simulation Analysis



Cu Ta Ti SiO2 BCB SiN Si

Figure 11. Schematic of TSV in Si interposer from IME.

An FE model is built on an actual TSV structure in interposer to be fabricated by IME-Singapore, A*STAR. Material used for die-attach to the substrate (not shown in Figure 11) is to be epoxy. The relevant properties of the material modeling is shown in Table 1. Modeling is performed only on half the actual structure by virtue of the plane symmetry of the cross-section.

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Simulation involves two coupled-field analyses using ANSYS® consisting of, (i) direct coupled-field thermal-electric analysis, and (ii) coupling the thermal result from previous analysis to perform structural-thermal analysis. The boundary conditions are as follows. In the first analysis, the bottom surface of the substrate is held at 200°C with uniform current density of 1.5MA/cm^2 and 0.6MA/cm^2 for top and bottom metallization respectively. The difference in the uniform current density under the same current magnitude as the boundary condition is due to the different cross-section area of the metallization as shown in Figure 11. The second stage is performed with load transfer coupled analysis where the nodal temperature solution from the first analysis is then applied as body load as initial condition to solve for structural-thermal analysis. In this analysis, the corresponding boundary conditions are set as such. Substrate bottom is assumed to have zero displacement and only in-plane displacements are allowed for the 4 vertical sides. The stress free temperature (SFT) of the interposer is assumed to be 125°C [6, 28] for initial condition in both analyses. User sub-routines were developed to compute the necessary constituents such as divergences of stress and temperature gradients from simulation results in order to achieve the total resultant AFD in the model. Section 2.2.3 describes the AFD modeling equations and Figure 12 shows a flow chart for the simulation described above.

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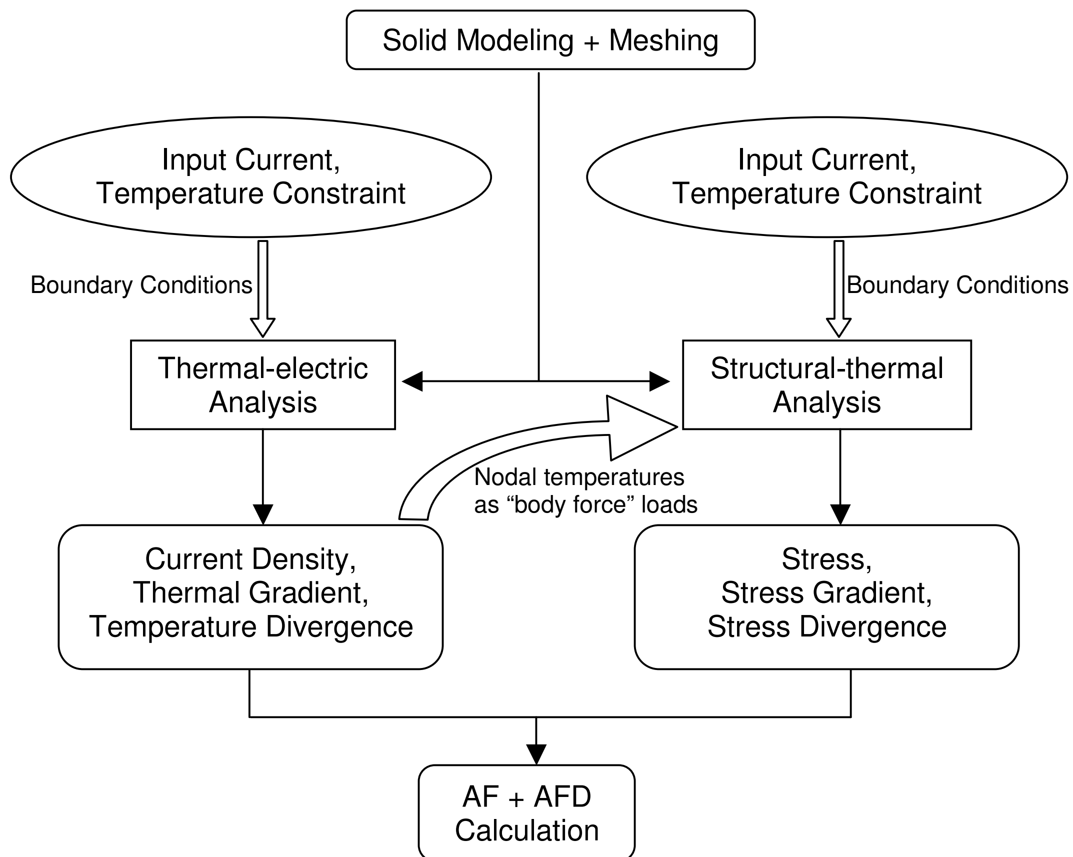

Figure 12. Flowchart for EM simulation.

Material	E (GPa)	CTE (ppm/°C)	Poisson Ratio
Cu	110	18	0.34
Ta	186	6.3	0.34
Ti	116	9.4	0.36
SiO_2	71.4	0.68	0.16
SiN	220	3.2	0.27
Si	130	2.6	0.28
BCB	2.9	50	0.33
Epoxy	3.6	46.2	0.37

Table 1. Material Properties used for simulations. [6, 57-60]

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3.2.2 Element Type Selection

Considering the complexity of the model, 3D 8-node hexahedral element is used for the analysis. Preliminary simulations are also run to achieve a suitably fine mesh density such that convergence of the results is achieved.

Solid69 element is found to be suitable for thermal-electric analysis with the appropriate DOFs; and solid45 element which possesses structural-thermal DOFs is used correspondingly for the thermo-mechanical second stage. Besides possessing the appropriate degrees of freedom for the corresponding analysis, these 2 element types also have both tetrahedral and hexahedral options. Generally, meshing with tetrahedrons is easier and faster compared to hexahedrons. Tetrahedrons can be used to mesh most solid volumes fuss free, unlike hexahedrons, where only regularly shaped rectangular volumes can be meshed. However, it has been reported in literature [47, 48] that linear tetrahedral elements are not recommended for mechanical analysis, in particular, when stress results are needed. In view of the thermo-mechanical simulation in our analysis, extra effort is made to divide the model into regular volumes so that a reasonable mesh containing hexahedral elements can be obtained. Figure 13 and Figure 14 show the mesh structure used in the simulations.

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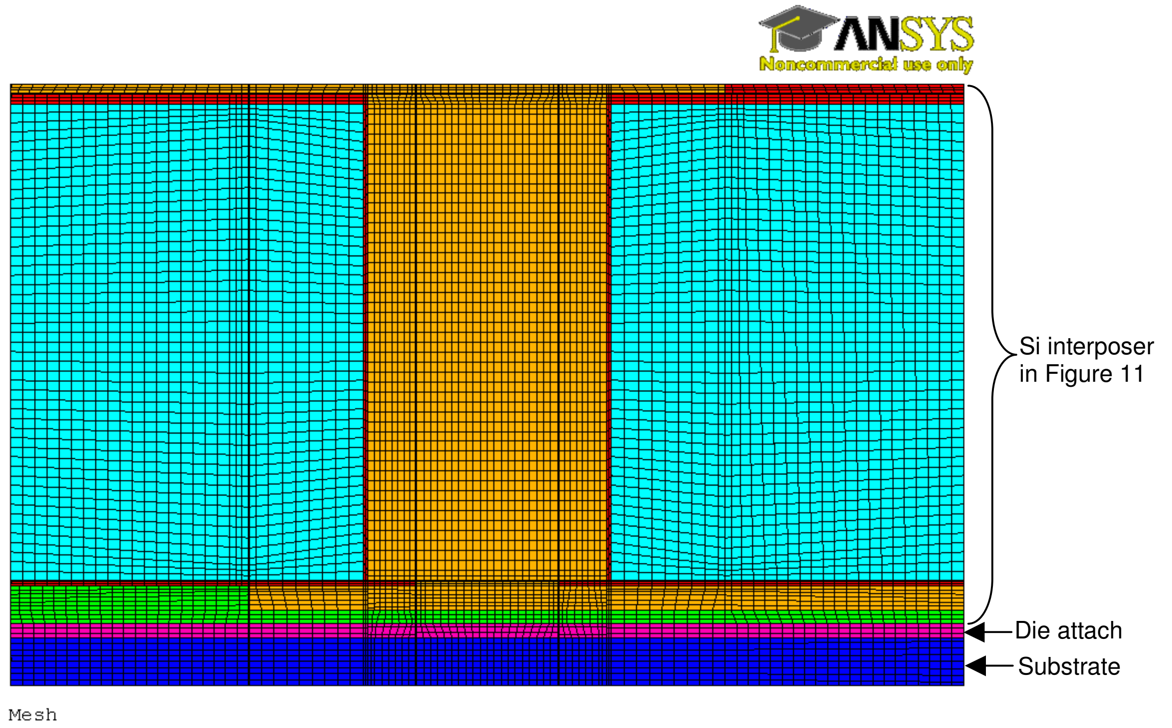

Figure 13. Mesh of the TSV in Si interposer.

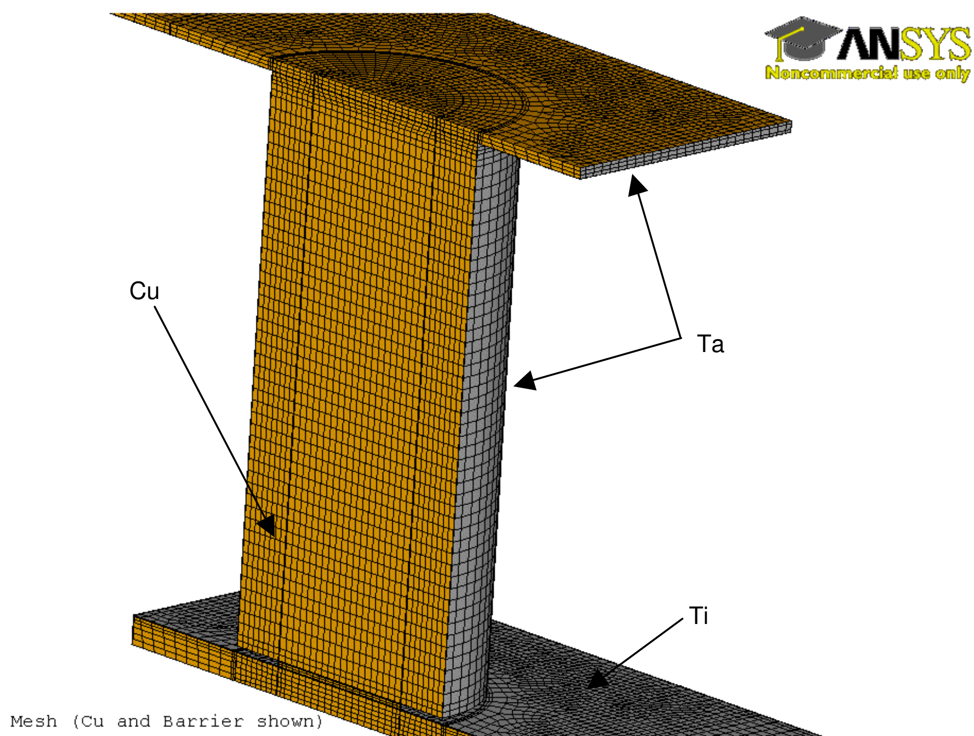

Figure 14. Mesh showing Cu and Barrier.

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3.2.3 Mesh Convergence Check

To avoid local stress excursion/singularity due to inappropriate mesh density, mesh convergence testing is carried out for the model. Iterations of stress simulations under the same boundary conditions are performed and both stress and temperature at the critical corner of the via is recorded. With each iteration, the mesh density is increased and stress contours are observed to be continuous with the contours varying in a smooth manner between adjacent elements. Figure 15 shows that the recorded parameters are observed to converge at the chosen mesh density. The stress values shown in the plot are absolute magnitudes because negative stresses are obtained. This is due to the temperature from the simulation results is higher than SFT (125°C). It is also noteworthy to mention here that as the temperature approaches SFT, the stress is also observed to decrease because stress at SFT is ideally zero. From this pre-study of mesh-sensitivity, a minimum element size of 1.5 µm will be used for further simulations throughout this work.

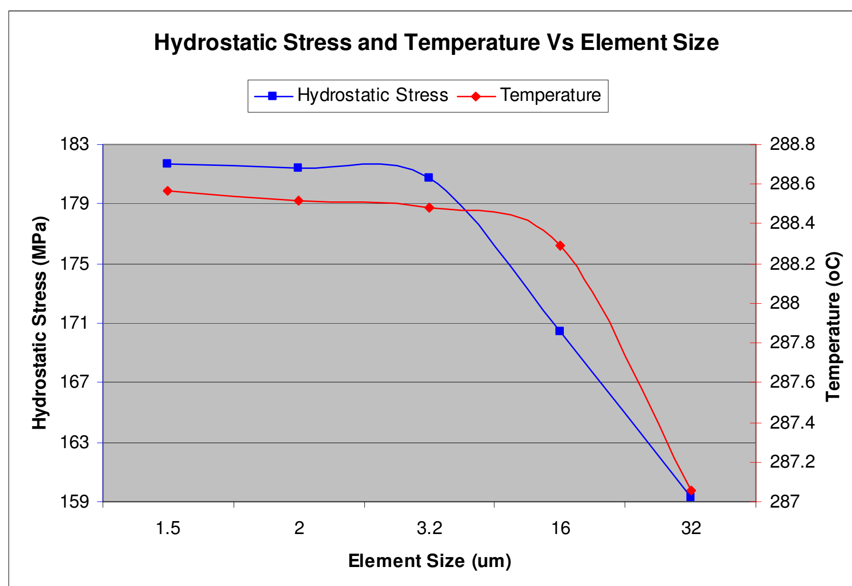

Figure 15. Hydrostatic stress and Temperature vs element size.

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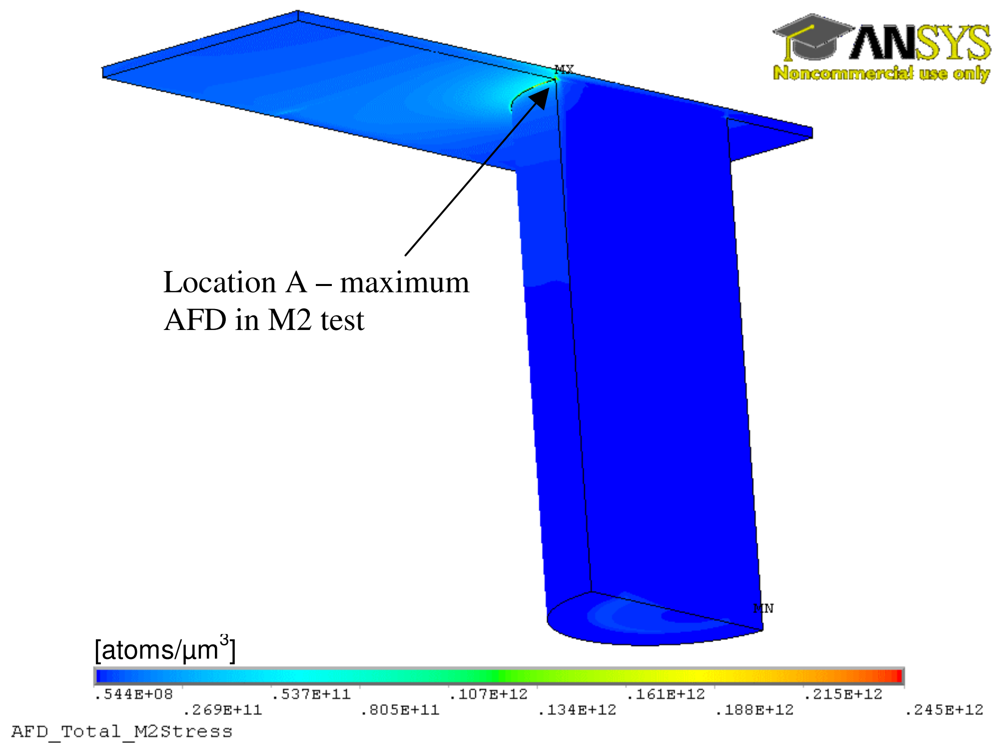
Chapter 4 Simulation Results and Discussions

4.1 Effect of Heat Sink Placement

4.1.1 Model 1

(a)



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(b)

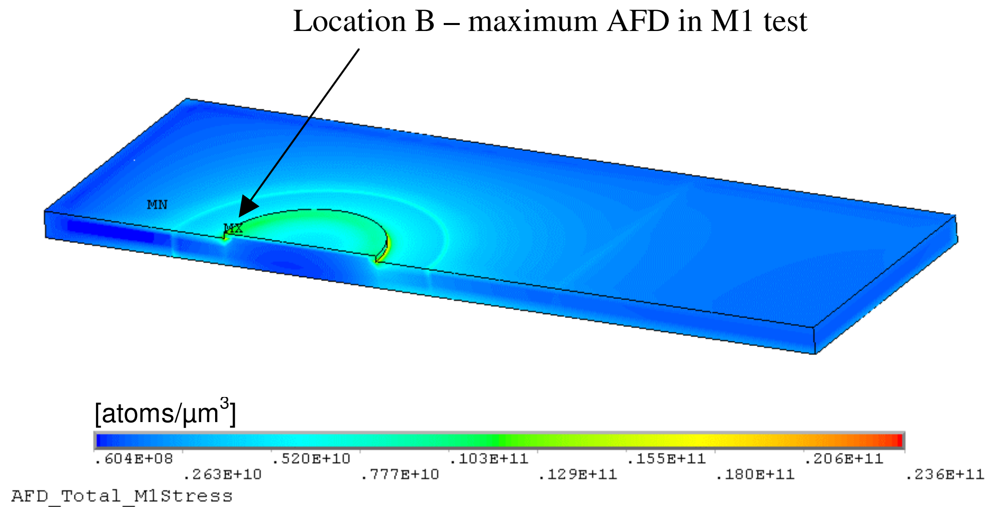

Figure 16. Plot of resultant AFD: for (a) M2 Test, (b) M1 Test in atoms/µm3 for Model 1.

Model 1 refers to the original TSV structure as shown in Figure 13. Figure 16(a) and (b) shows the simulated AFD for M2 test and M1 test for Model 1 respectively. Location A shows the maximum AFD in M2 test; whereas Location B is the maximum AFD for M1 test.

It is observed that EM is more severe in M2 test than M1 test based on the values of total AFDs at locations A and B as shown in Figure 16. This asymmetrical behavior can be attributed to the difference in process technology and geometrical difference between the top and bottom metallization. Further analyses later will show that the current crowding, thermal and stress gradient are indeed different between the top and bottom metallization.

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The individual contribution of the 3 driving forces in the conventional AFD formulation are also extracted and summarized in Table 2. One can see from Table 2 that SM contributes to more than 85% to the total AFD as compared to just 8% contribution from the EWM at the locations of maximum AFD. Several works have reported that high localized stress/strain is recorded at these corners where the via meets the pad through both thermo-mechanical simulations and X-ray diffraction experiments under temperature cycling [26, 28, 61, 62]. The presence of these high localized stress/strain is thus expected to have an adverse effect on the EM performance of TSV.

	AFD Contribution (%)		
	EWM	TM	SM
M2 Test	7.5	4.3	88.2
M1 Test	8	3.5	88.5

Table 2. Breakdown of resultant AFD contributions from 3 driving forces at local maximum.

Since SM is heavily dependent on the stress gradient generated by the coupled thermo-mechanical stress, reducing the thermal gradient can lower the total AFD at these high AFD locations, enhancing the EM performance of TSV. This will be explored and explained with results from Model 2 in the next section.

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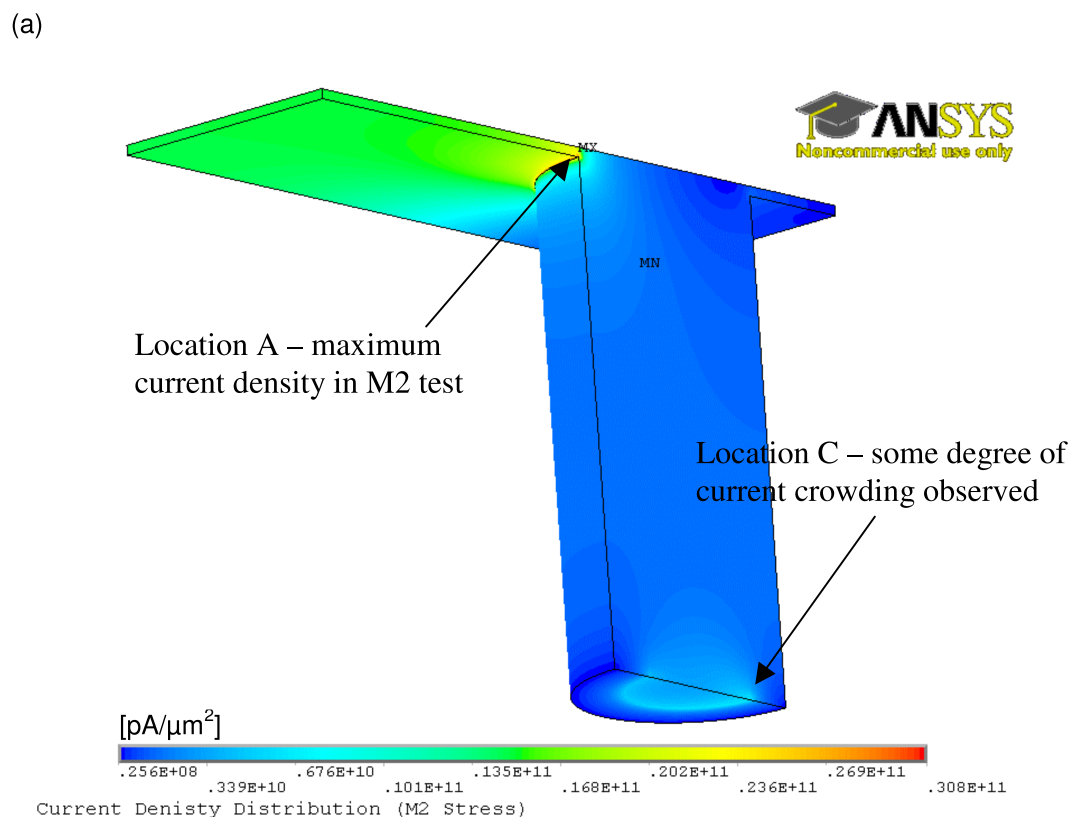
Figure 17(a) and (b) shows the current density distribution for M2 stress and M1 stress respectively. It can be seen clearly that there is severe current crowding where there is a sharp change in the path of current flow. There is also some current crowding at Location C in Figure 17(a). This corresponds to the location where the pad opening of the bottom metallization is. Due to the smaller opening of the bottom metal pad with respect to the bottom diameter of the via, the current flow is more constricted towards the middle of the via bottom.

(a)



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(b)

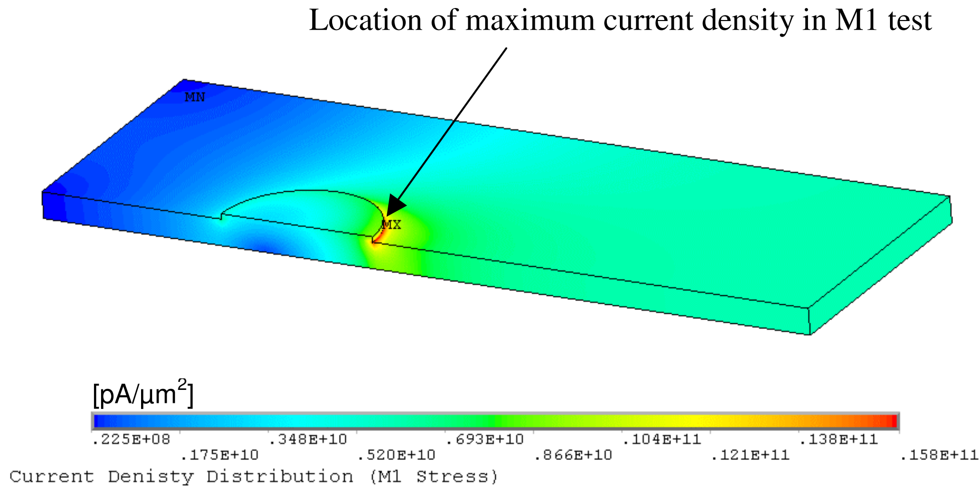

Figure 17. Current density distribution: for (a) M2 Test, (b) M1 Test in pA/µm2 for Model 1.

The magnitude of the current density at the maximum current crowding location is also higher in M2 stress (see Figure 17a) than in M1 stress (see Figure 17b). This is because of the difference in geometrical dimension between the top metallization and the bottom metallization as shown in Figure 11. Assuming current continuity, the same magnitude of current flow will see a higher current density for a smaller cross-sectional area. The top metallization has a cross section less than half of the bottom metallization. This accounts for the higher current density which leads to higher current crowding at corners.

It is also observed that temperature changes most rapidly at the locations of current crowding in Figure 18. This observation is probably due to the fact that current

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crowding at these corners causes severe localized joule heating and act as "mini" heat source. As copper is a good heat conductor, high thermal gradient results in these locations of localized heating.

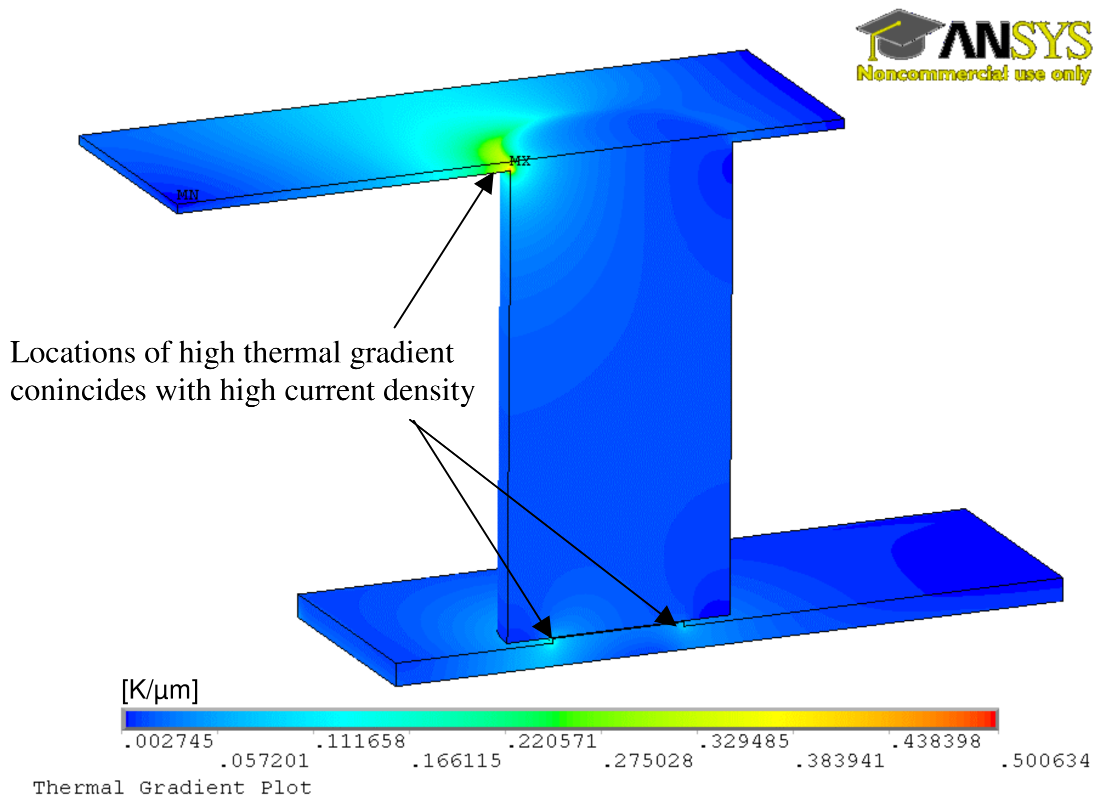

Figure 18. Plot of Thermal Gradient in K/μm for Model 1.

4.1.2 Model 2

It has been mentioned previously that from the analysis of the simulation in Model 1, the breakdown of contributions to maximum AFD amongst the 3 driving forces shows that SM is the dominant factor. Since SM is very dependent on the thermal gradient induced thermo-mechanical stress, we should be able to reduce the maximum AFD by reducing the thermal gradient at these high AFD sites. As a simplified example, the original model is modified to have its die attach and heat sink on the top side of the TSVs. This is to simulate flipping of the silicon

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interposer between the chip side and the substrate side. In so doing, the thermal and stress gradients is significantly different from the previous model as will be shown below.

The AFD plots for this modification are shown in Figure 19. The value of the total AFD at similar locations of maximum AFD in this model is tabulated for comparison with the previous model. Table 3 shows that the maximum AFD for both M2 and M1 tests decrease significantly from its previous values. This means that any effort to relieving thermo-mechanical stress in the TSV offers important benefits. A better EM performance can be obtained and higher thermo-mechanical reliability can be achieved at the same time. Even though lowering the current density can reduce AFD because of the lowered EWM contribution, its effect is far less than that of reducing the thermo-mechanical stress due to its low significance. Therefore, reducing thermo-mechanical stress early in the design will be the key approach for improving EM performance, especially when the tighter limits are imposed on current density due to miniaturization, design or power requirements.

	AFD (atoms/μm^3.s)		Decrease
	Model 1	Model 2	
M2 Test	0.245E12	0.173E11	14x
M1 Test	0.236E11	0.256E10	9.2x

Table 3. Comparison of AFD at local maximum with heat sink at opposite side.

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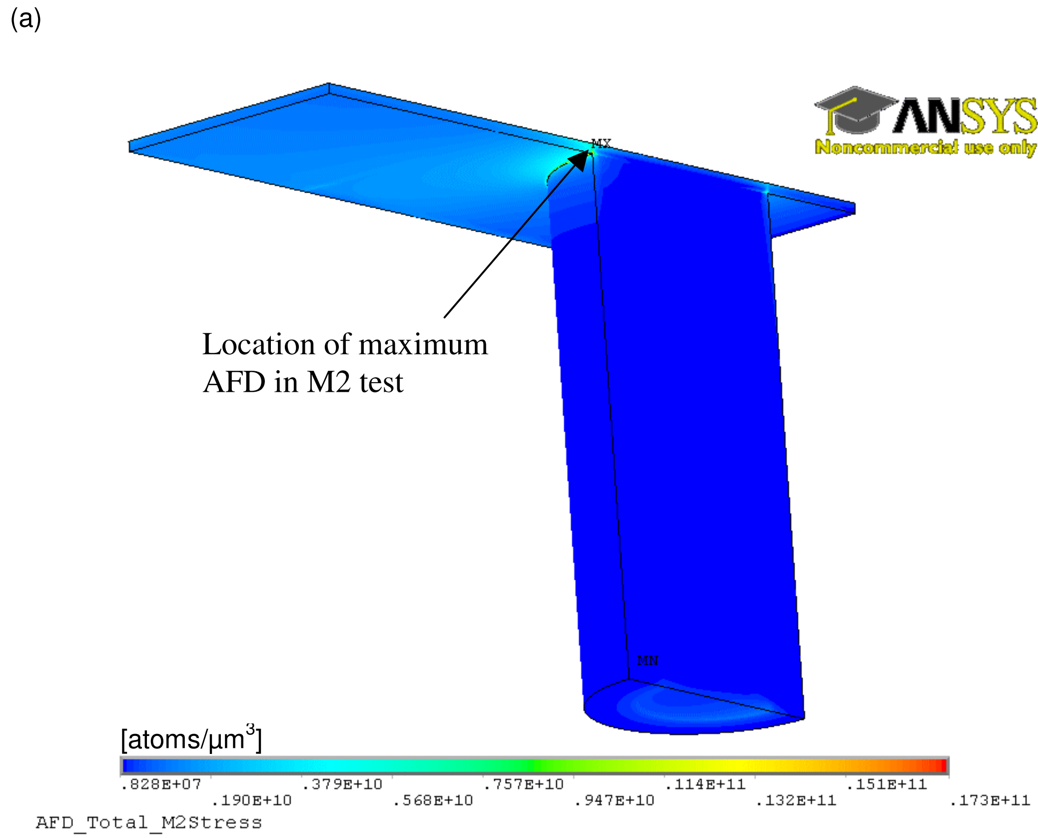
(a)



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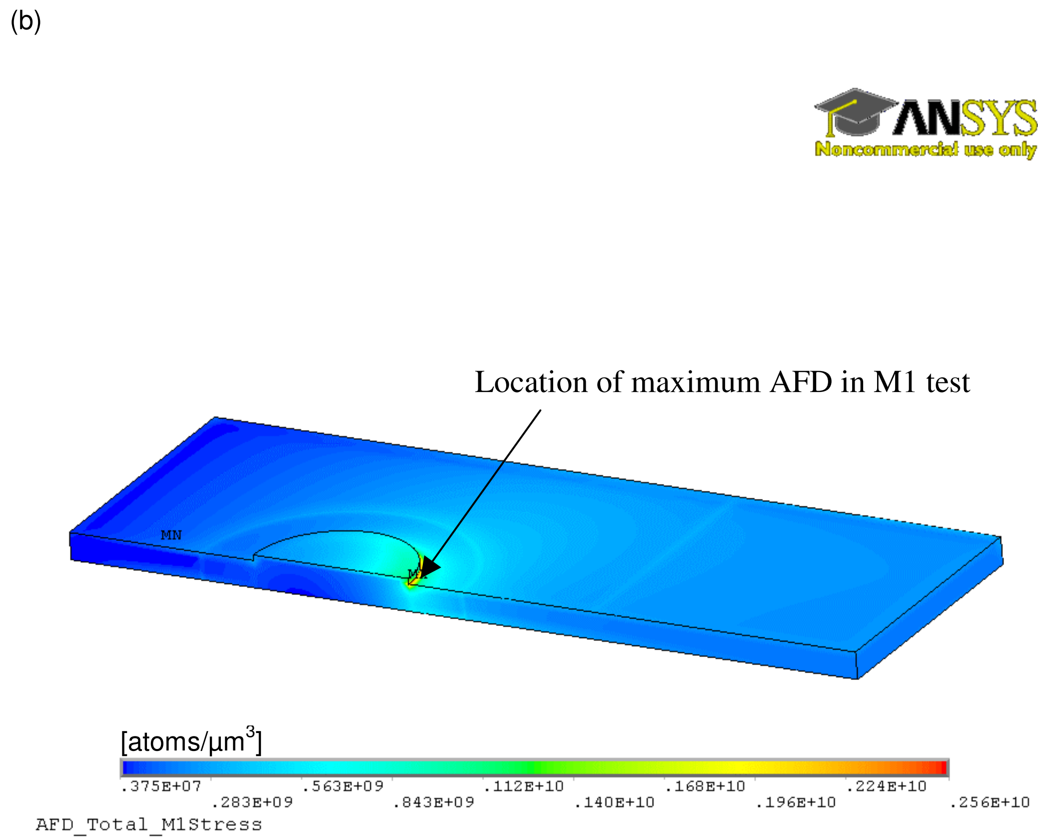

Figure 19. Plot of resultant AFD: for (a) M2 Test, (b) M1 Test for in atoms/µm3 for Model 2.

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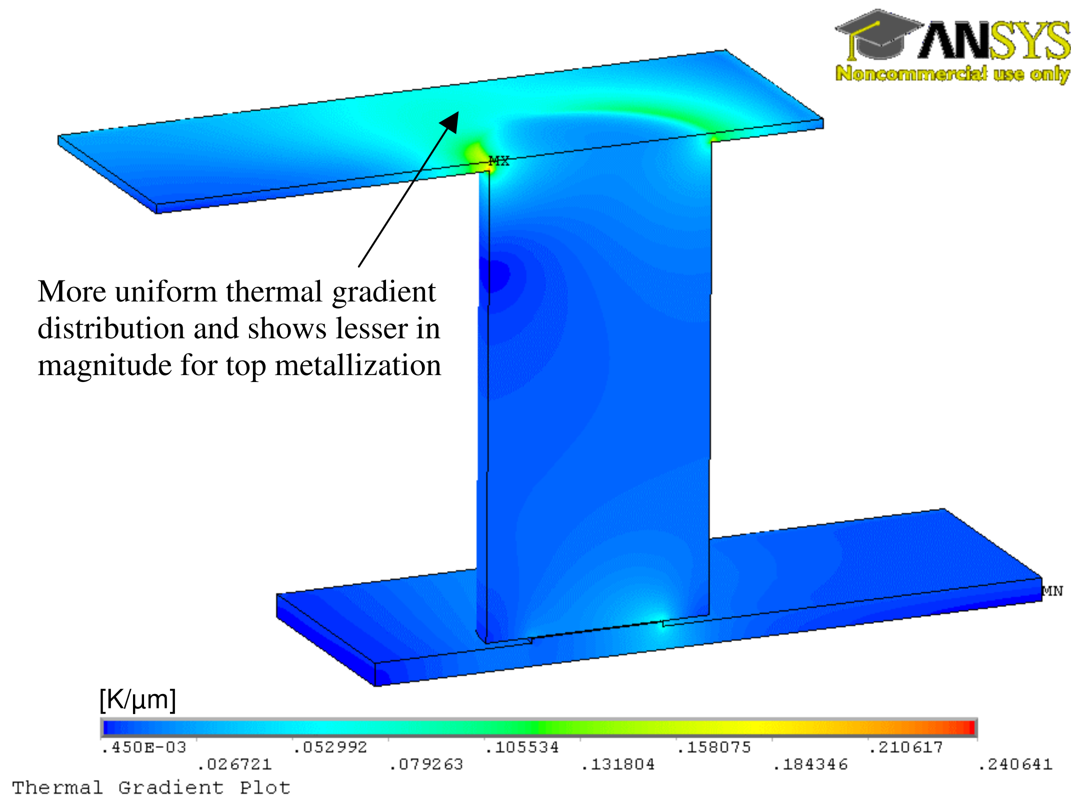

Figure 20. Plot of Thermal Gradient in K/µm for Model 2.

Figure 20 shows the thermal gradient plot after the interposer is "flipped" between the chip side and the substrate side. Compared to Figure 18, the maximum thermal gradient is reduced by half from the previous model. Also, the corresponding distribution on the top side of the top metallization shows better uniformity. This may be due to the better heat dissipation because the heat sink is now on the side of the top metallization as opposed to the previous model where the heat sink is on the side of the bottom metallization.

Figure 21 and Figure 22 shows the von mises stress and hydrostatic stress prior to and after "flipping" the interposer respectively. It is observed that high equivalent stress exists at the corners of the via, consistent with the literature [26, 28, 61, 62].

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Ideally, the interconnect will be free from stress and strain at SFT whereby tensile or compressive stress will exist in metallization at temperatures below or above the SFT respectively. The negative value in Figure 22 represents compressive stress as the test temperature is higher than the stress free temperature. Both von mises stress and hydrostatic stress exhibit significant improvement in Model 2 compared to Model 1. This reiterates that relieving thermo-mechanical stress in the TSV can help improve both EM and thermo-mechanical reliability at the same time.

In Figure 23, the negative radial stress represents the compressive force felt by copper as it expands more than the surrounding silicon under temperature stress which is higher than SFT. In the same manner, Figure 24 also indicates largely compressive stress is experienced. The distribution contours are also intuitive due to the direction of the principal stress of axial stress and radial stress respectively, where uneven magnitudes are felt in the same cross-sectional plane. In reported literature, Liu et al. [62] has performed thermo-mechanical simulations and plotted similar stress distributions which the magnitudes and distributions in this work here concurs. They reported experimental verification with XRD measurements by developing a method to correlate their simulation results and experimental measurements. Part (a) of each respective figures show the stress plots obtained using the model in this work; whereas Part (b) are taken from the above-mentioned literature. For fair comparison, similar simulation conditions as the reported work are used to obtain Figure 23 and Figure 24 , where the SFT is 50°C and the thermo-mechanical stress is recorded at temperature loading of 300°C. The consistency of the results between the two different models from both works may serve as a preliminary verification of the model used here.

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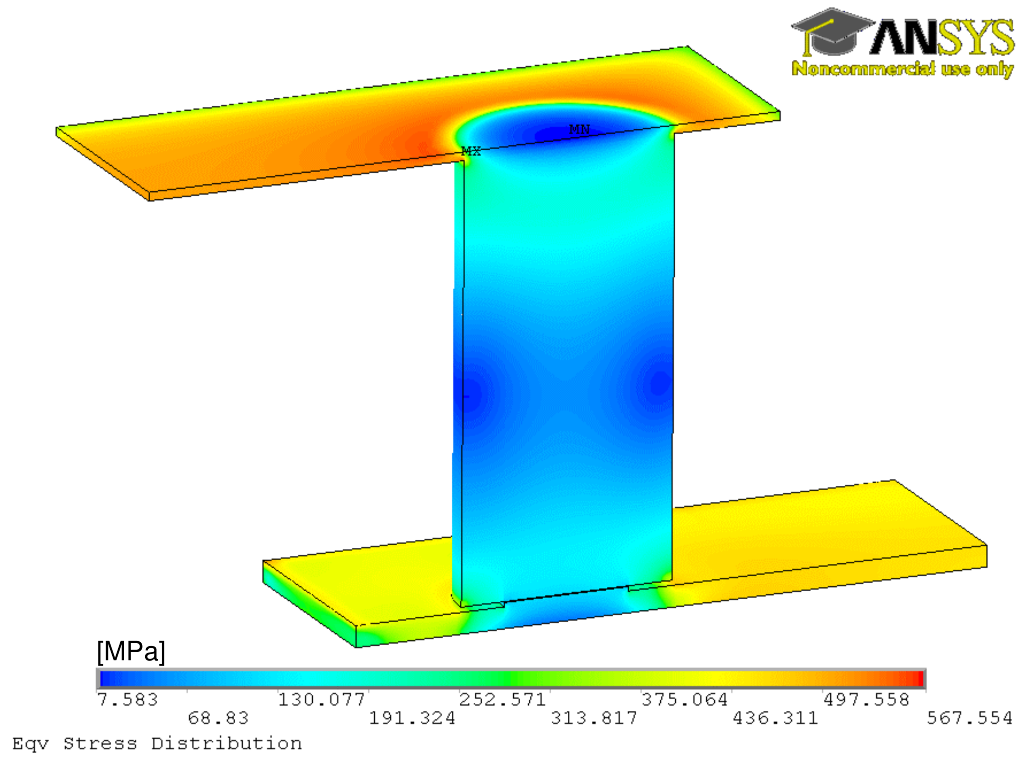
(a)



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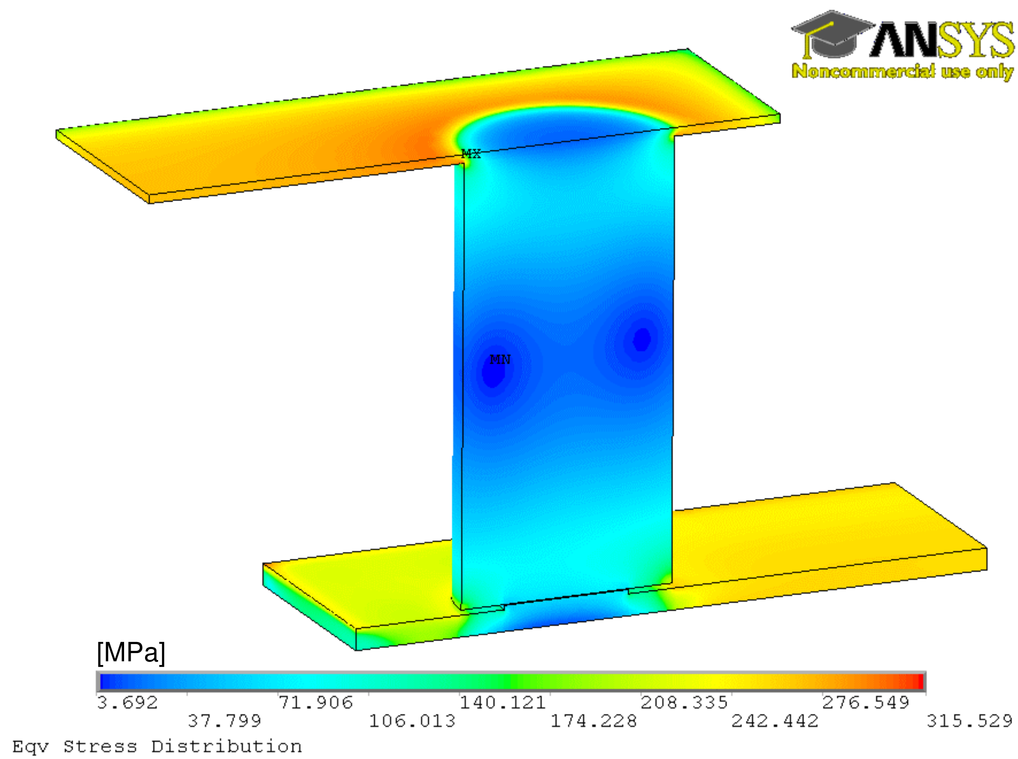

Figure 21. Plot of Von Mises Stress: for (a) Model 1, (b) Model 2 in MPa.

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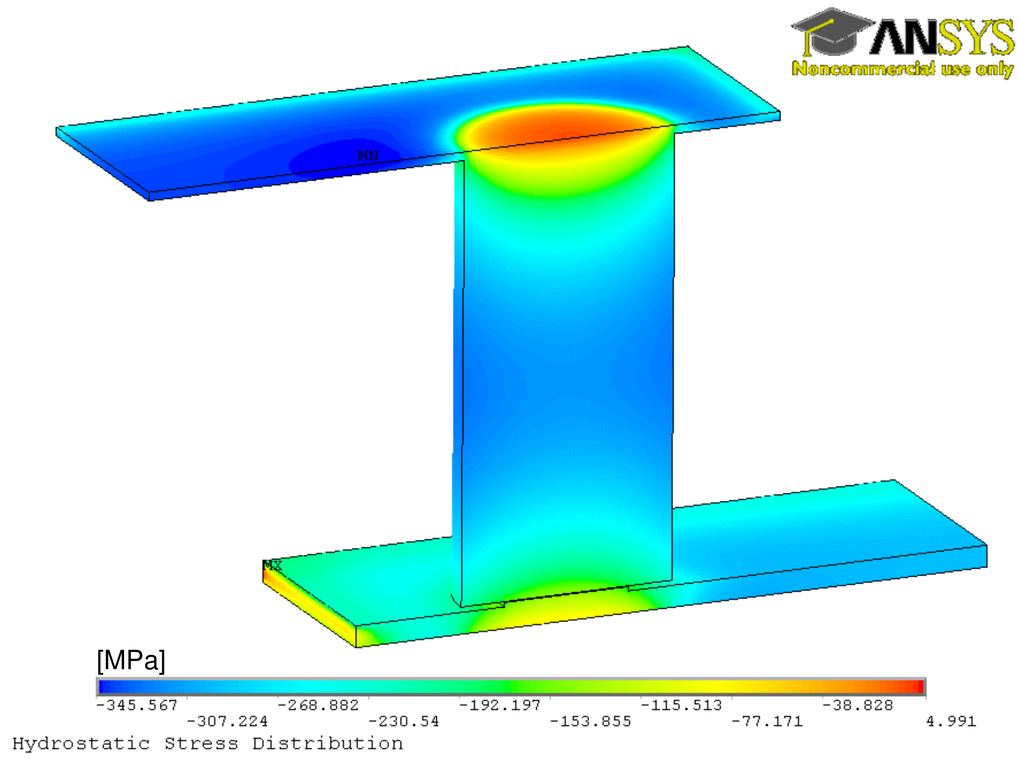
(a)



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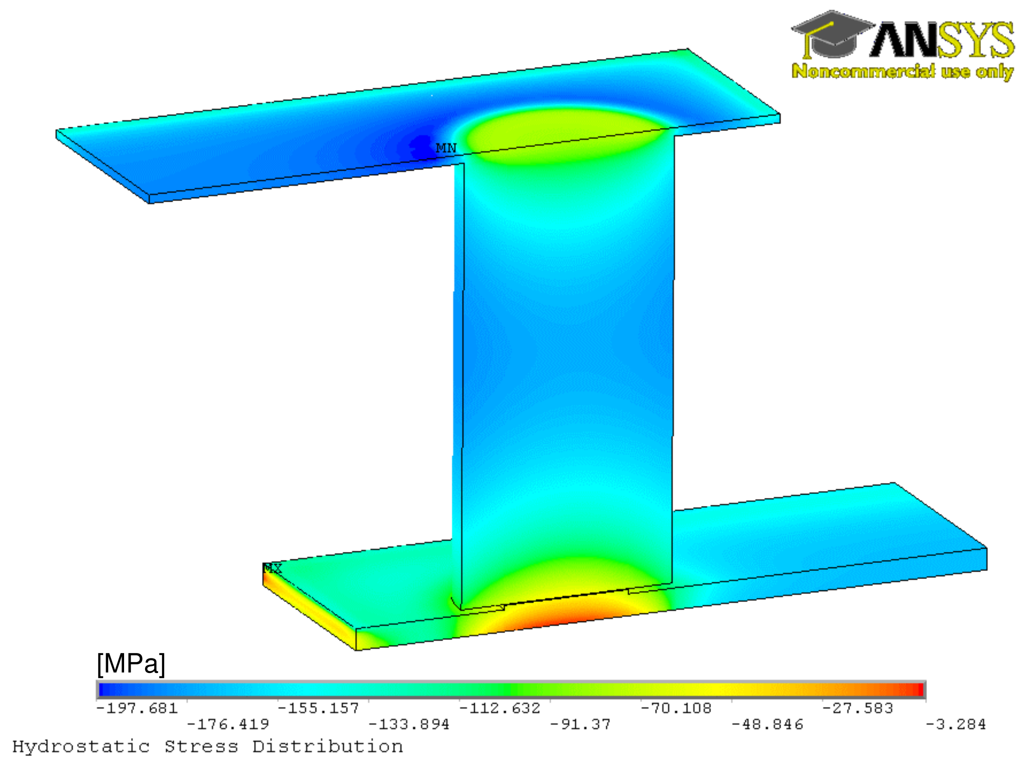

Figure 22. Plot of Hydrostatic Stress: for (a) Model 1, (b) Model 2 in MPa.

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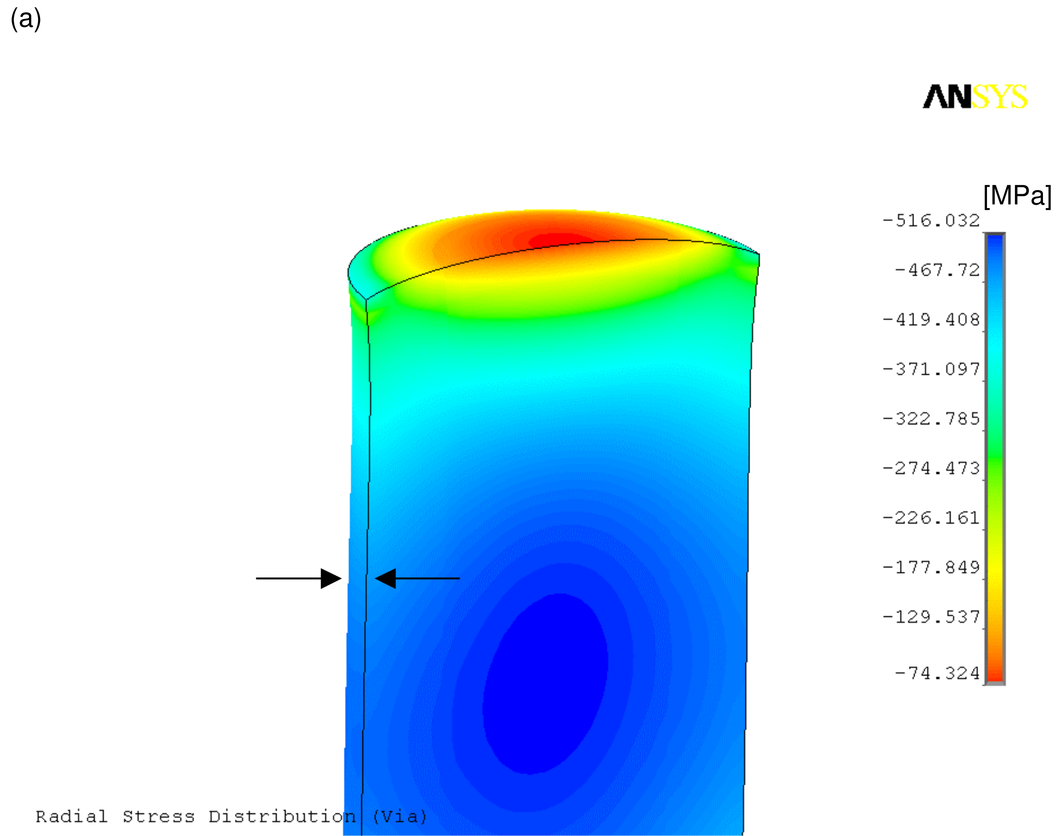
(a)



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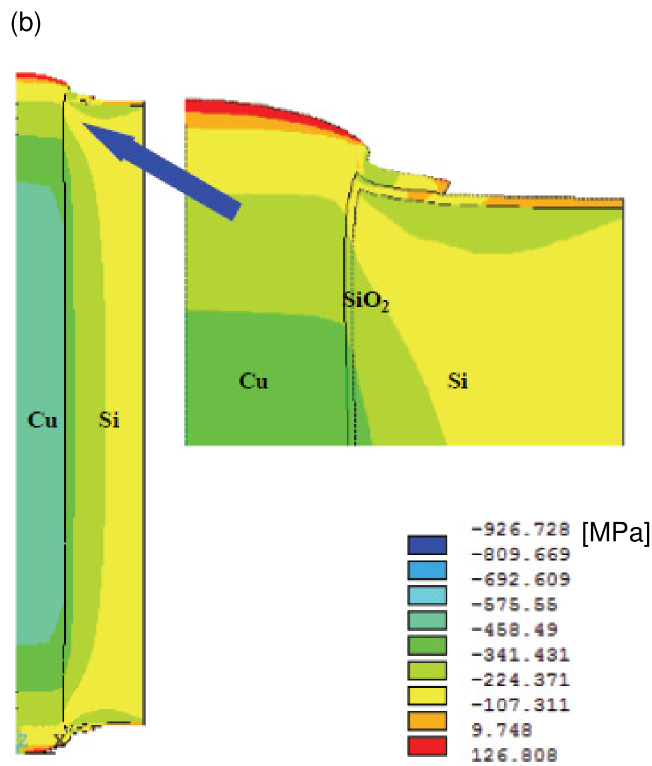

Figure 23. Plot of Radial Stress in MPa for (a) the current model in this work, and (b) reported literature [62] at 300°C. (deformation scale factor x 50)

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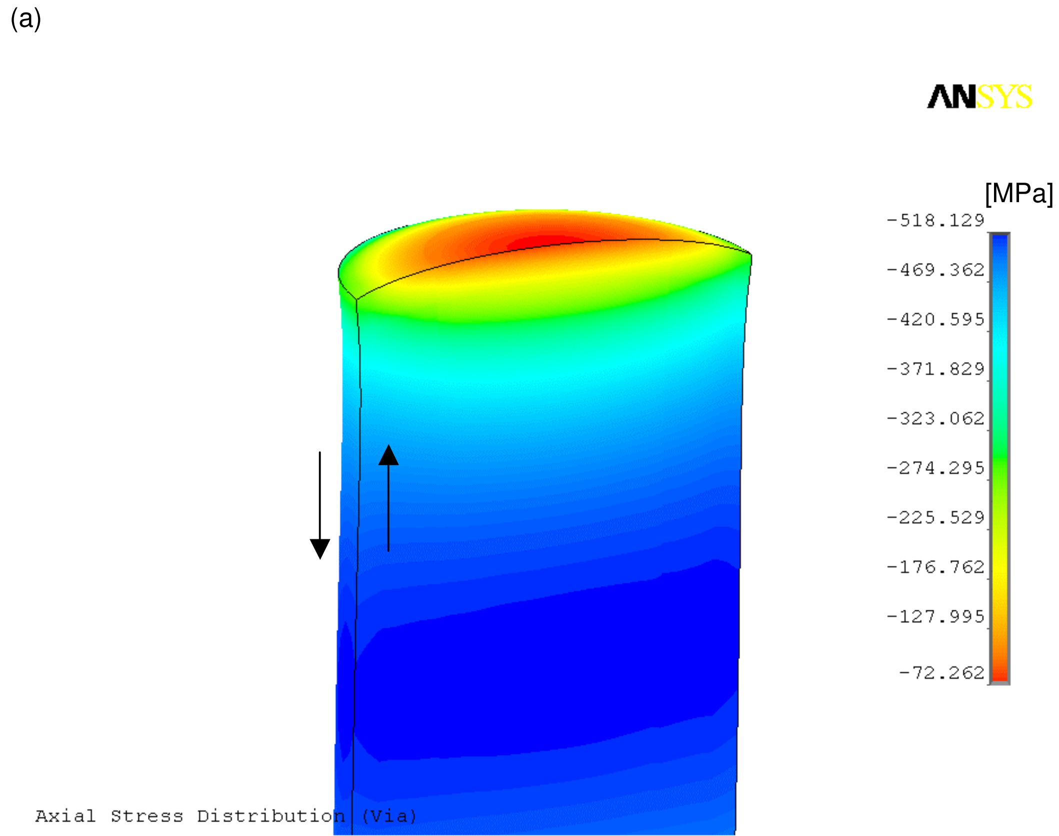
(a)



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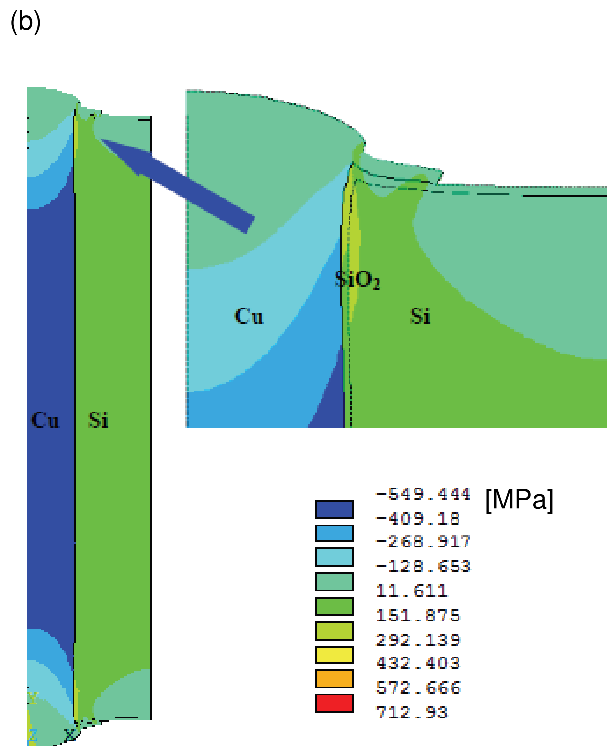

Figure 24. Plot of Axial Stress in MPa for (a) the current model in this work, and (b) reported literature [62] at 300°C. (deformation scale factor x 50)

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4.2 Effect of Coverage Pattern

4.2.1 Model 3

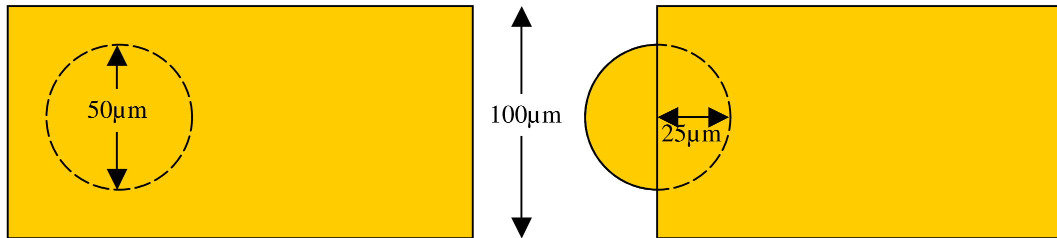

Figure 25. Top metallization coverage pattern of Model 1 & 2 vs Model 3.

The same TSV structure is also simulated with a different coverage pattern for the top metallization. Figure 25 compares the original top coverage pattern where the metal line covers the via completely against one where the metal line covers only half the via. The die attach and heat sink is on the top side in this model for merits of comparison with Model 2. Results of the AFD simulation are shown in Figure 26.

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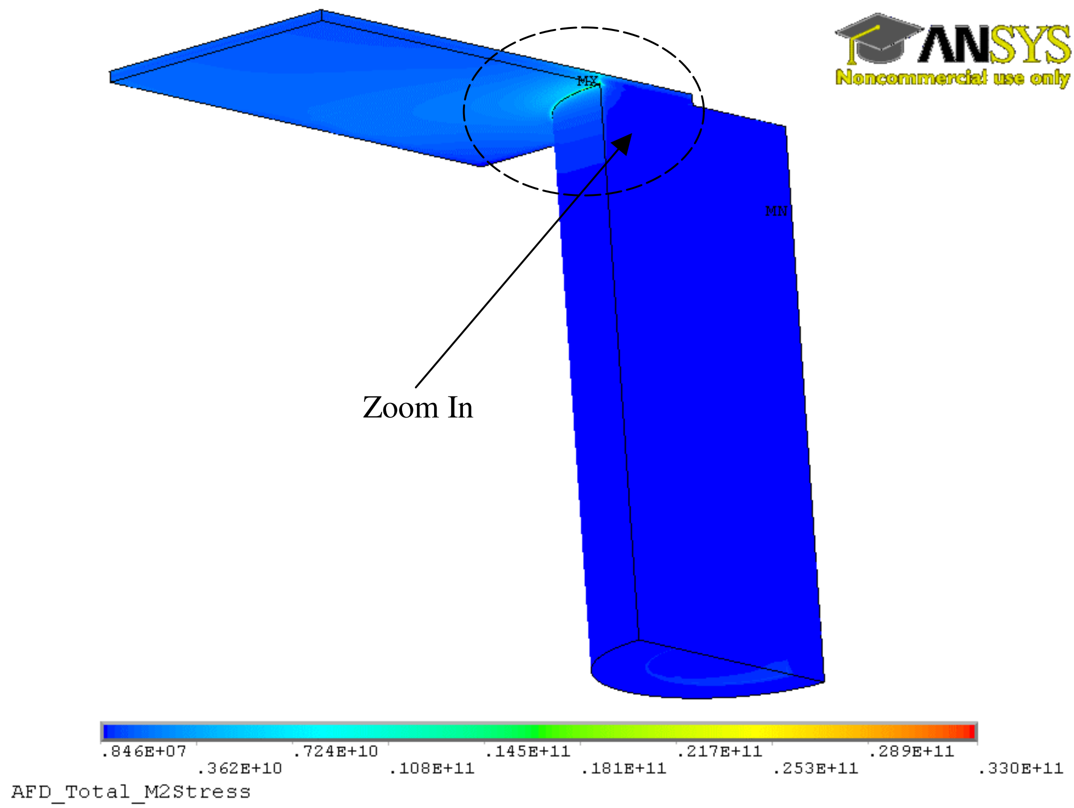
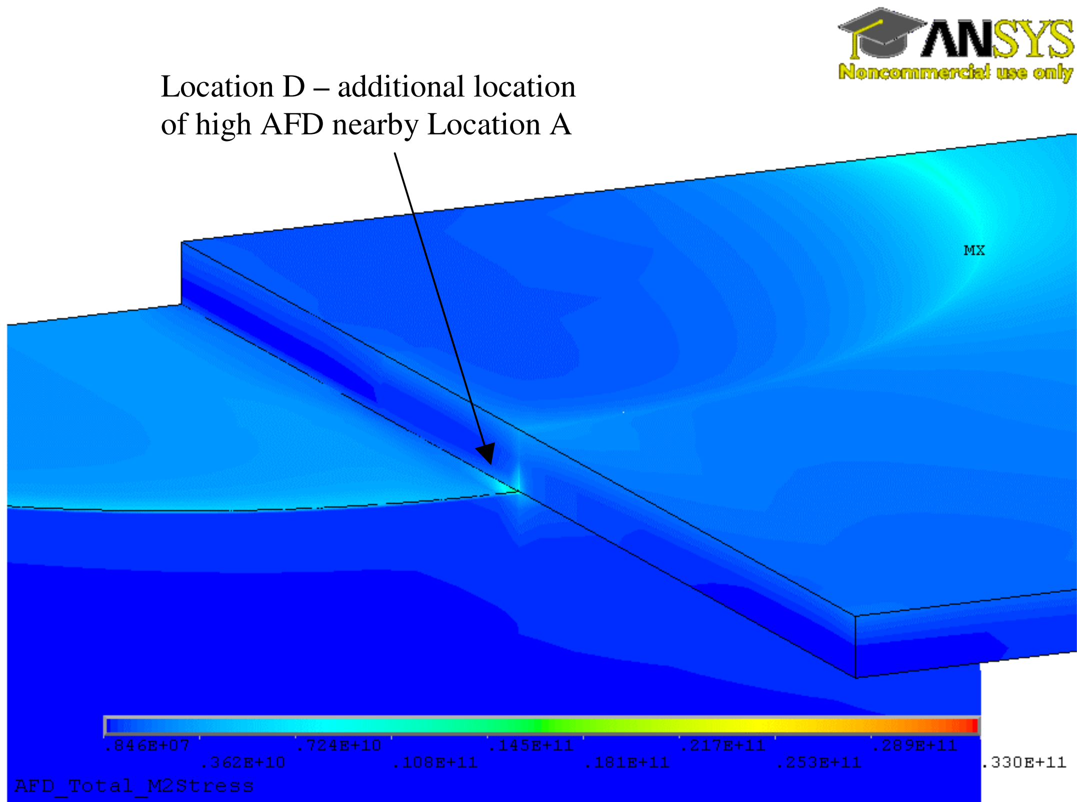
(a)





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(b)

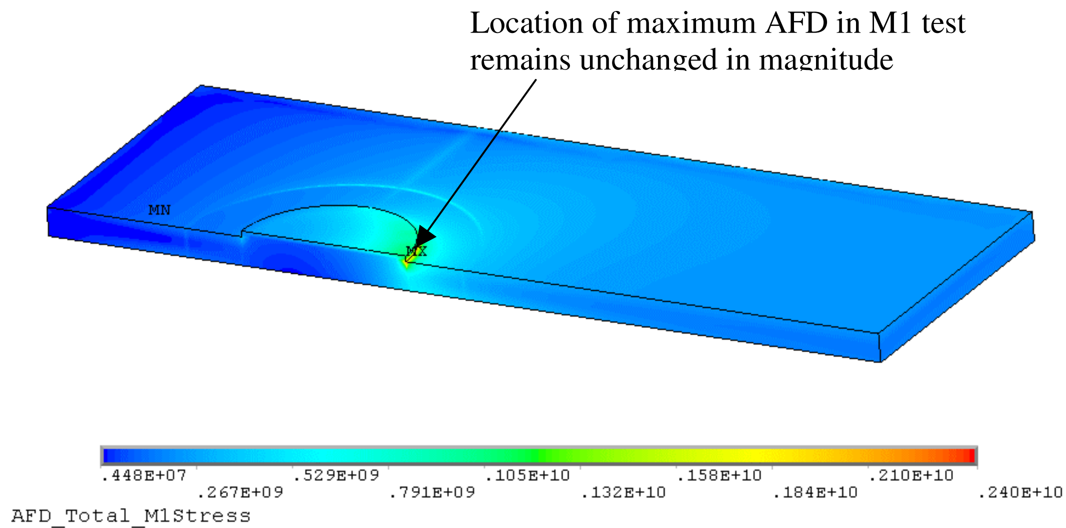

Figure 26. Plot of resultant AFD: for (a) M2 Stress, (b) M1 Stress for Model 3.

The maximum AFD for M1 stress in this model is found to be of the same order and similar location compared to Model 2; whereas the maximum AFD for M2 stress is almost twice of that earlier at the same maximum location. Furthermore, we can also see that a possible second EM failure site (location D) behind location A exists, and high AFD occurs at this location D which is the interface between the end of the line and the via. A dynamic simulation of void growth which is similar to ref [37, 59], further confirms the notion that the AFD at this location is sufficiently high to allow simultaneous growing of voids. This has a major implication: The competing and simultaneous growth of voids in the same vicinity may result in sooner catastrophic open circuit failure. Due to a higher AFD value

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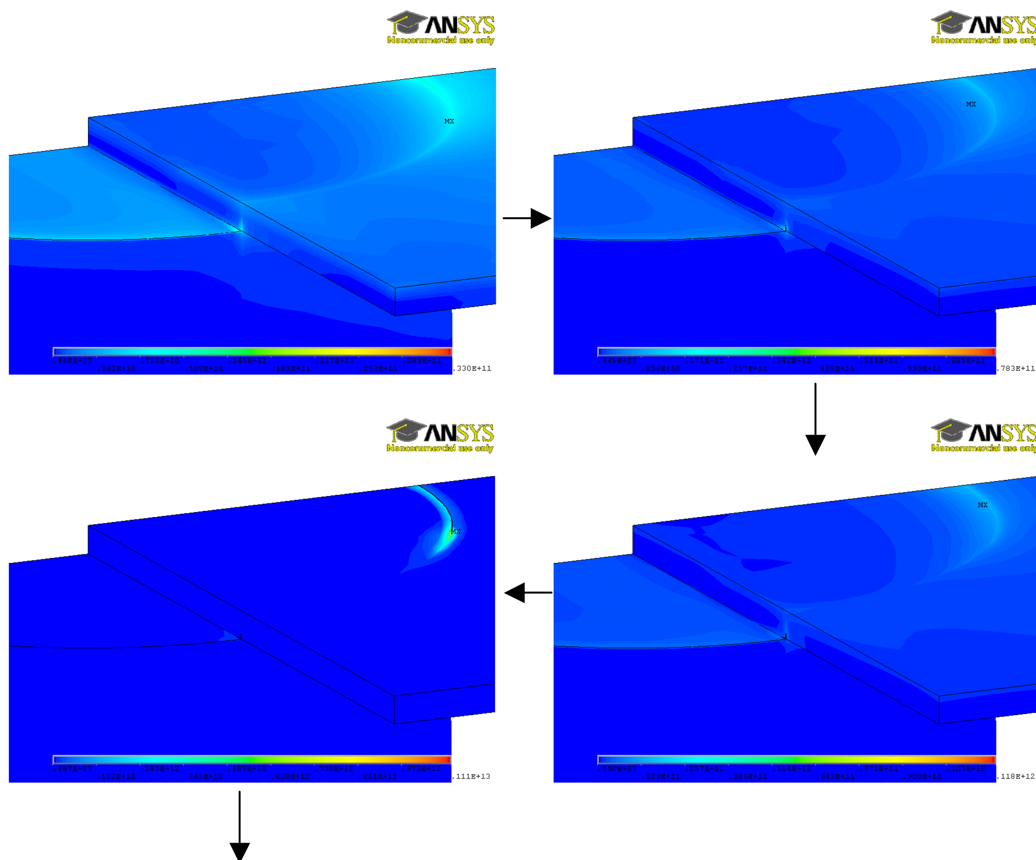
at location A and the near vicinity existence of additional location D, a worse EM performance can be expected for Model 3.

The dynamic simulation used is described in detail here. A separate user developed routine has been written to delete selected elements of highest AFD value in the TSV structure. Following that, the AFD of the modified TSV structure is recalculated. In this way, a pseudo void evolution condition is achieved when the steps are repeated in an iterative manner. Due to the extremely high mesh density used, the number of elements to be deleted in each loop is set arbitrarily to 50. Figure 27 clearly shows that onset of voids at location D which eventually grows towards location A and vice versa. Figure 28 shows a closer view of the void growth.



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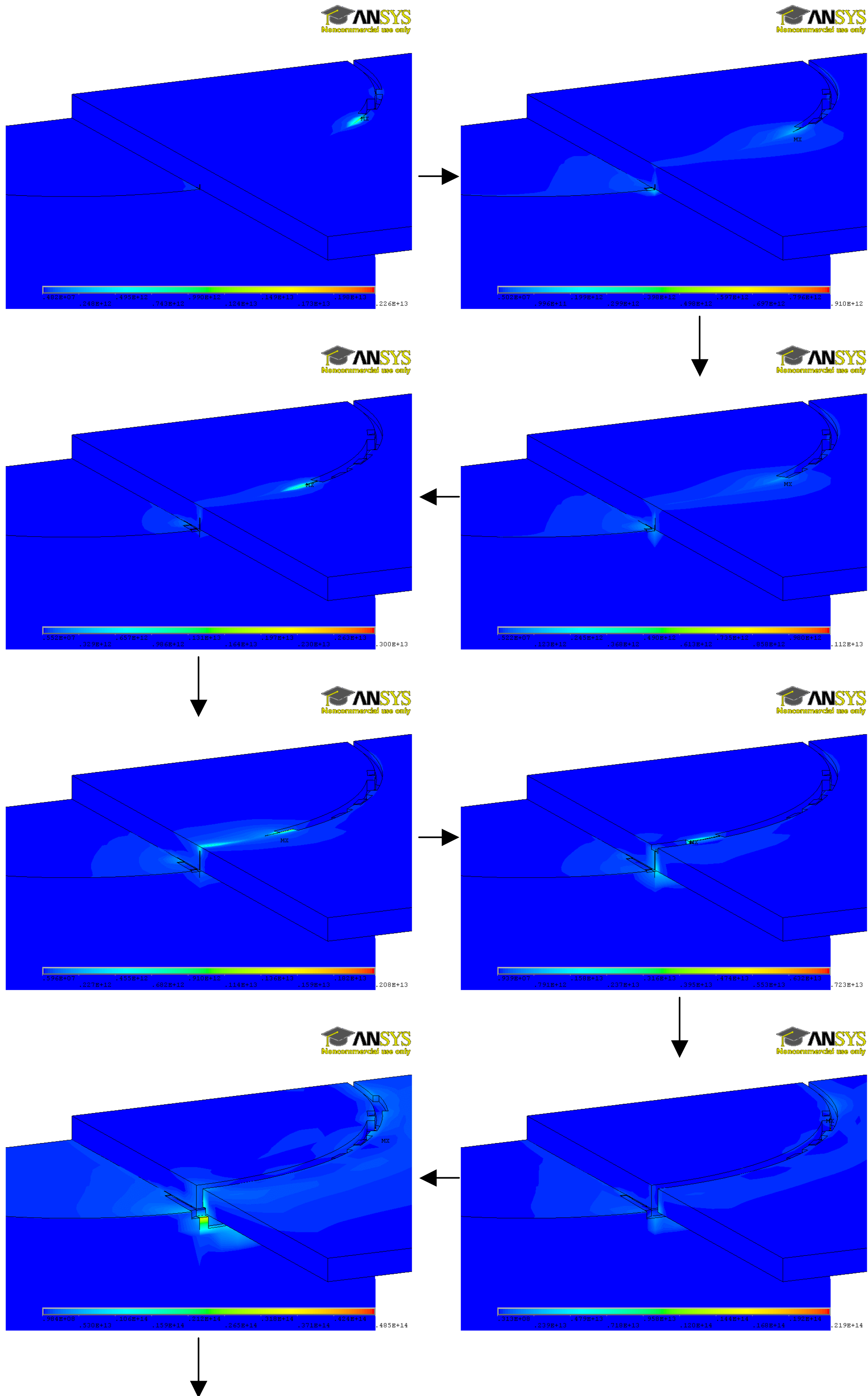

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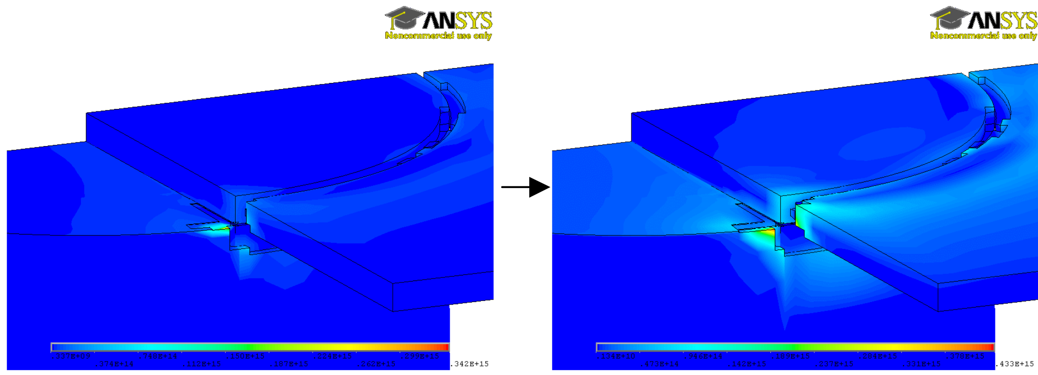

Figure 27. Iterations of the dynamic simulation.

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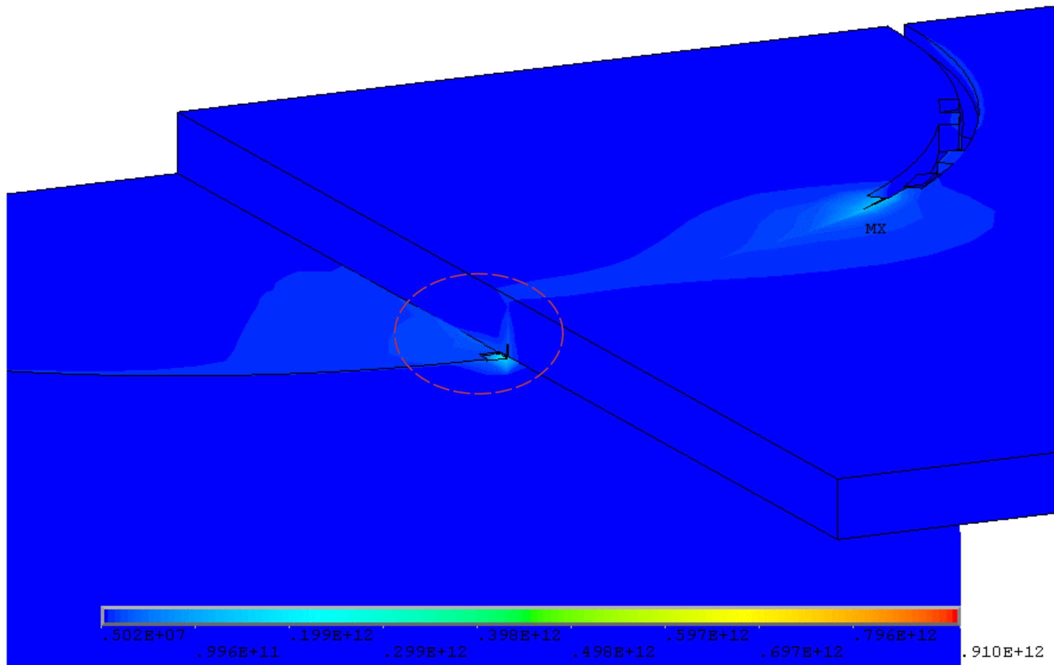
(a)



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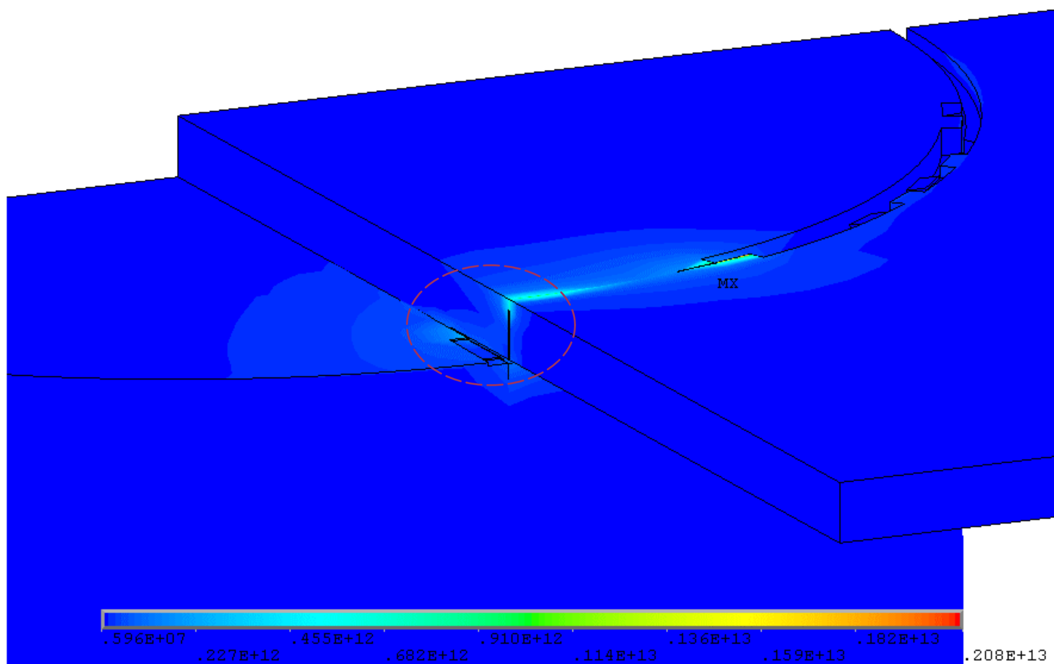

Figure 28. Void growth after (a) 5th loop of iteration, (b) 8th loop of iteration.

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In Section 4.1, it is found empirically that thermo-mechanical stress is the dominant factor (see Table 2) for EM in the studied TSV application. By reducing the thermal gradient at high AFD locations, the AFD is also observed to reduce significantly (see Table 3). Therefore, efforts to improve thermo-mechanical reliability of TSVs through reducing the thermo-mechanical stress can aid in improving its EM reliability.

It is also shown through simulations that the AFD can be very different due to the different metallization scheme and the geometrical dimensions. The simulations show that most failures may be observed only on the top side of the interposer, at the corner where the metallization meets the TSV. This exhibits a strong asymmetrical behavior in terms of EM experimental failure between top side and bottom side.

The effect of metallization coverage is studied in Section 4.2 using a case where the top metallization extends to cover half the via. Worse EM performance is observed in this case, as compared to one that covers the via fully. An additional location of sufficiently high AFD is found to be in the vicinity of predicted EM location. Further simulations show that voids can grow concurrently and meet to merge, resulting in a earlier failure. This implies that a novel coverage pattern can be found to optimize the EM performance of a TSV structure.

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Chapter 5 Proposed Experimental Methodology

It is desired to have some experimental data to complement the simulation results and achieve a better understanding of the underlying physics of EM in TSVs. As such, the project is closely worked together with IME-Singapore, A*STAR to include proposed EM test structures in their reliability test chip design for 3D chipstacks. However, resources are limited and the fabrication technology is not yet mature. The test structures are already planned into the production run, but yield is still low and no good samples are achieved yet. This is made worse due to the fact that the test chip is highly complicated, containing many other test structures ranging from piezo-resistive stress sensors, die crack sensors, surface insulation comb and triple track structures etc.

With experimental verification in mind, some groundwork for future EM tests on this chip have been laid down. An in-house EM tester control block has been designed and built, customized for carrying out EM experiments on the test chip. Various resistance monitoring methods are discussed and a new method is also proposed.

5.1 Resistance measurement methods

5.1.1 Introduction

To assess the electromigration reliability of different types of interconnects experimentally, EM tests are conducted that generally involve resistance monitoring of DUT under high temperature and current stress conditions, where

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the test structure is considered to have failed when its resistance change reaches a predetermined value. This section will discuss some of the resistance measuring methods employed and reported.

Unlike other interconnect technologies such as aluminum, copper damascene, and solder bumps, there is no established global standard of TSV EM experimental technology. The established EM test standards usually describe the use of Four-probe measurement technique to accurately monitor and measure the resistance during EM stressing. In the TSV discussed here, the resistance of the via is calculated to be as much as 20 times smaller compared to the resistance of the top metallization, or 4 times smaller when compared to the bottom metallization; assuming a length of 200 μm for the surrounding metallization. In the particular context of resistance measurement, a very sensitive method has to be employed in order to detect any small change of resistance due to EM damage. An example of solder bump EM testing will be illustrated here because similar to TSV, solder bump also have very low resistance as compared to adjacent metallizations which will be further detailed in the next paragraph. Furthermore, EM testing methodologies for solder bump interconnect is relatively mature compared to the lack of reported work for TSV EM tests.

A typical individual solder bump interconnection has a relatively low resistance of 5-20 mΩ compared to the resistance of external wiring connections to the pads above and below the bump, which is generally of a few tenths of an ohm to over 1 ohm [63]. These wirings may also degrade during the course of the solder EM stress test. As such, any small resistance change of the solder bump due to EM

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will be easily masked due to the increase in the resistance of the wirings as will be seen in the example in Section 5.1.5. As a result of this "noise", measurement of the actual bump resistance change is challenging but such measurement is essential to assess the amount of damage in the bump. Figure 29 shows a schematic of an EM test structure in a daisy chain configuration for solder bumps. The current flow and the structure of such a daisy chain type configuration is similar to the designed TSV EM test structure.

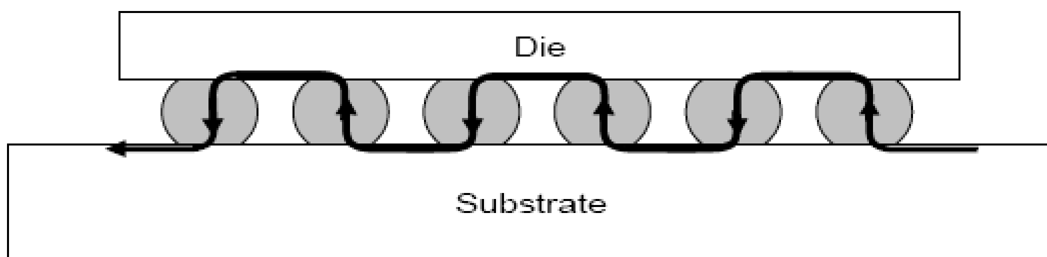

Figure 29. Daisy chain EM test structure for solder bumps. [63]

In the following sections, two commonly used resistance monitoring methods for the solder bump will be examined, and a new method based on the Kelvin Double Bridge [64] will be proposed. The effectiveness of the resistance monitoring methods will be discussed. The pros and cons of each method will also be described.

5.1.2 The Four-probe Measurement Technique

Four-probe measurement technique is very well established and has been used by both industrial and the research community for solder bump resistance measurement. It provides a fast and simple non-destructive method for resistance measurement. By using a separate pair of lead for forced current and voltage

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sense, the accuracy of the measurement can be increased since contact resistance of the probe to solder and the resistance of the wiring can be excluded in the measurement results. However, this method is sensitive to any resistance increase due to, for example, temperature variation on the DUT by possible oven temperature fluctuation.

5.1.3 The Wheatstone Bridge Method

Some reported that the Wheatstone Bridge method can successfully detect early failures and EM damage in solder bumps with high sensitivity [65, 66]. They showed that the Wheatstone Bridge configuration can eliminate the error due to temperature fluctuation present in the Four-probe measurement method. This is because the temperature effect on resistance change will cancel out each other when the bump and external wiring are located on both arms in the unknown legs as shown in Figure 30(a), where R_a and R_b are representing 2 solder bumps or equal number of bumps on each arm in daisy chain, and R_M and R_N represents the ratio arms of the bridge circuit. The high sensitivity of this method is attributed to the fact that measurement of the unknown resistance is based on the ratio of the known resistances in the ratio arms with the bridge in near-balance condition. Therefore, any change in the DUT will result in further voltage imbalance across the 2 legs, which can then be easily detected with a high resolution galvanometer.

5.1.4 The Kelvin Double Bridge Method

However, the interconnect between the 2 adjacent solder bumps in the daisy chain represented by dashed lines in Figure 30(a) introduces additional resistance, and its

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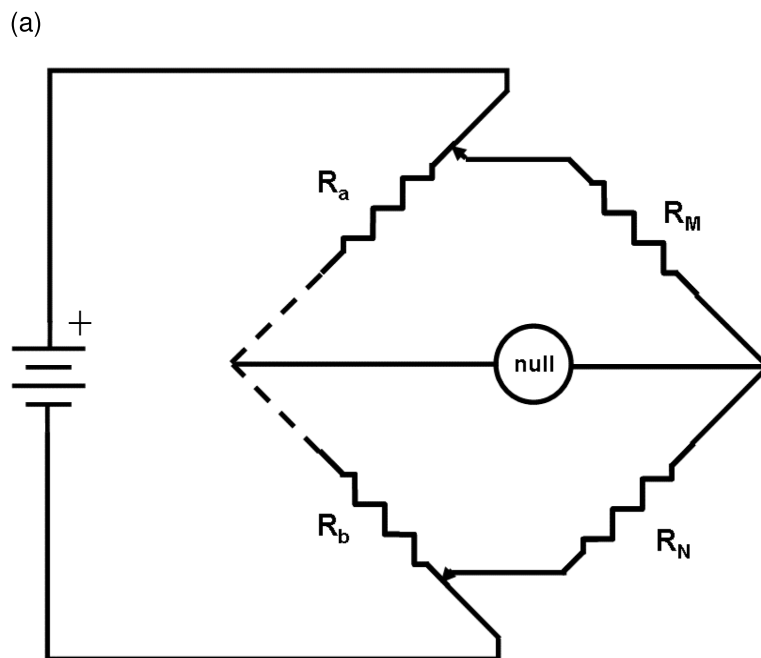
corresponding EM damage can potentially mask the EM damage of the solder bumps with the Wheatstone Bridge method. We propose to use the Kelvin Double Bridge as a more accurate assessment of EM damage during EM tests. The Kelvin Double Bridge depicted in Figure 30(b) will be able to cancel out the effect of the interconnect resistance between the 2 solder bumps, provided that the interconnect is limited between R_a and R_b. As seen in the original balance equation [64] of the Kelvin Double Bridge which is reproduced in Eq. 7 for this application, any terms involving the resistance of the interconnect between adjacent solder bumps represented by dashed lines will cancel out if the ratios R_m / R_n and R_M / R_N are the same.

$$\frac{R_b}{R_a} = \frac{R_{interconnect}}{R_a}\left(\frac{R_m}{R_m + R_n + R_{interconnect}}\right)\left(\frac{R_N}{R_M} - \frac{R_n}{R_m}\right) + \frac{R_N}{R_M} \qquad (7)$$

here $R_{interonnect}$ is the resistance of the interconnect segment between two solder bumps.

(a)



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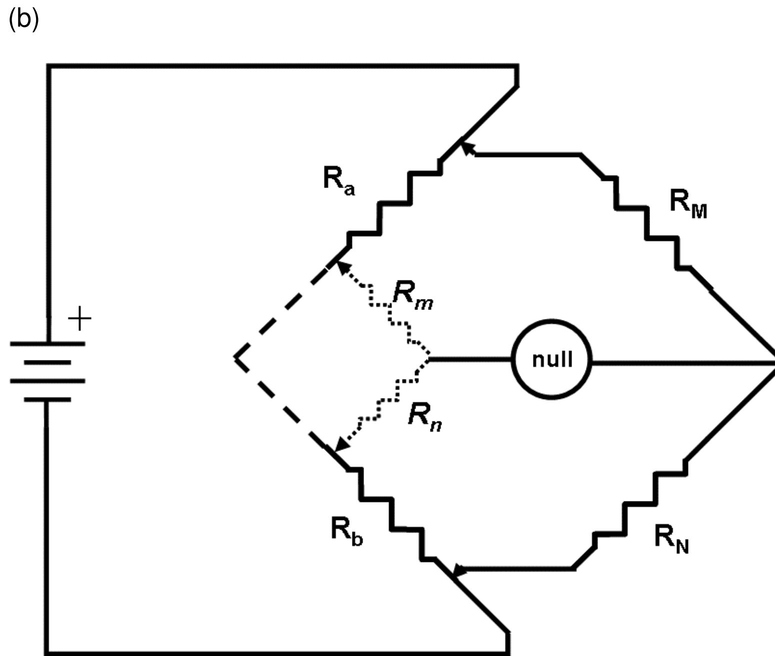

Figure 30. (a) Wheatstone Bridge [64], (b) Kelvin Double Bridge [64].

For both bridge methods, it is advisable to use resistors of small manufacturing tolerance and good long-term stability. Although the bridge methods are able to reduce the interconnect noise due to temperature fluctuation as explained earlier, the high temperature stress in EM tests may cause significant thermal degradation to the resistors and cause permanent drift from its resistance value. One can thus consider wire-wound type resistors if the cost is justifiable.

Due to the mathematical principle of the bridge methods, a very high measurement accuracy can be obtained from using resistors that meet the above criterion together with a high resolution galvanometer.

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5.1.5 Comparison of the Resistance Monitoring Methods

To compare the above-mentioned three different monitoring methods, we compute the error in measuring the increase in resistance (ΔR) for each method with the following assumptions and scenario as example.

1. A 10% resistance increase in solder bump as EM failure criteria
2. A modest estimate of 0.5mΩ EM damage in the Cu interconnect.
3. A temperature increase of 0.1°C on DUT due to oven temperature fluctuation.

Material properties are shown in Table 4

Material	Resistance	TCR (10^{-3} K^{-}
100µm cubic eutectic PbSn solder	~1mΩ	4.5 [67]
100µm long Cu interconnect with 1µm x 0.2µm cross-section	~10Ω [32]	4.3 [68]

Table 4. Components and its electrical characterization.

Table 5 shows the computed errors from the three methods, and the % error is defined as

$$\%Error = \frac{\Delta R_{Total} - 0.1}{0.1} \times 100\% \qquad (2)$$

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This error serves as a measure of the inaccuracy arising from considering the "parasitic" resistance and the assumptions stated above, versus the actual assumed damage on the solder bump which is 0.1mΩ.

ΔR_{Total} is the total increase in the measured resistance. In the case of four-probe method, ΔR_{Total} consists of the resistance increases from oven temperature fluctuation and Joule heating in addition to the assumed EM damages in both the line and the solder bump. An example of ΔR for the Four-probe method is computed as follows.

$$\begin{aligned} \Delta R_{Four-probe} &= (Oven\ Temperature\ Fluctuation) \\ &\times \begin{bmatrix} (TCR_{solder} \times R_{solder}) \\ +(TCR_{interconnect} \times R_{interconnect}) \end{bmatrix} \\ &= 0.1 \times [(4.5E-03 \times 1.1) + (4.3E-03 \times 10000.5)] \\ &= 4.3 \end{aligned} \tag{3}$$

For the case of the Wheatstone Bridge, the effect of temperature fluctuation on resistance will be eliminated when the method of voltage balancing is used. For the Kelvin Double Bridge, only the assumed damage on the solder bump will be included.

It is clear from Table 5 that the Four-probe method yield a highly inaccurate result. Although the Wheatstone Bridge can eliminate the error due to temperature fluctuation, it still measures the resistance degradation in both the interconnect and solder bump. In comparison, only the Kelvin Double Bridge is able to measure the actual bump resistance.

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Measurement Method	Assumed EM		Computed ΔR (mΩ) due to temperature	Total ΔR (mΩ)	% Error
	Bump	Interconnect			
Four-probe	0.1	0.5	4.3	4.9	4800
Wheatstone	0.1	0.5	0	0.6	500
Kelvin double	0.1	0	0	0.1	0

Table 5. Error on resistance increase using different monitoring methods.

5.1.6 Advantages and Limitations of the different methods

While Kelvin Double Bridge produces the best result, its cost and complexity is the highest as compared to the widely adopted Four-probe measurement. However, the bridge's complexity can be reduced to a certain extent by fabricating its components such as the arms resistors in a packaged IC. On the other hand, although the Four-probe method is the simplest, its high degree of inaccuracy as illustrated in the previous section may not be sufficient in measuring low resistance DUT, such as that in solder bump and TSV EM tests.

Both the bridge methods have the merit of eliminating inaccuracies arising from even the slightest oven temperature fluctuation. As such, low cost ovens may be used without adversely affecting the measurement results. The complexity associated with the bridge methods is thus compensated with the ability to use cheaper ovens.

In EM tests concerning daisy chain of vias or solder bumps, the interconnect between adjacent DUTs in the chain are sometimes fabricated so that the lines will not fail before the DUT itself. Different methods such as having short

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interconnects observing "Blech effect" [50] or having thick and wide lines so that the interconnects are made "invincible" have been employed. However, such a structure could alter the current density and thermo-mechanical stress distribution in the interconnect line as well as the solder bump, and move the EM failure site away from the potential failure location of the bump in an actual device, rendering different failure modes from that in actual field performance which is undesirable for accelerated testing. With the Kelvin Double Bridge method, any resistance increase in the interconnects becomes irrelevant.

As each resistance measurement method has its pros and cons, it is important to consider one's requirements before deciding on the method employed.

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5.2 Proposed Experimental Setup

An in-house EM tester control block has been designed and built, customized for carrying out EM experiments on the test chip. Although commercial EM testers have a lot of benefits such as dedicated true current source for each DUT, compatibility with variety of test structures, built-in data logging and analysis, integrated oven, etc. Unfortunately, common EM testers may be ill-suited for our application due to cost issues and lack of feature such as ability to incorporate various resistance monitoring methods and source very high current.

To build our own EM tester, it is important to understand the requirements for our experiments. For EM testing, it is essential to have the same stress current flowing through all the DUT for valid reliability data. The resistance across each DUT needs to be continuously monitored, such that a device is deemed to have failed when its resistance increases by a pre-determined percentage. The method employed to measure resistance for the tester designed in this early prototype will be based on the traditional Four-probe measurement method. This is so as to keep the design as simple as possible at this stage. Future improvements can be made by just modifying the tester program to incorporate other measurement methods described in Section 5.1. Some of the requirements and solutions to difficulties encountered in designing the in-house EM tester will also be described together with the prototype built.

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5.2.1 Problems Encountered and The Approach Taken

Stressing current needed not readily available

To achieve EM data in reasonable amount of time, it is common practice to have a stressing current density in the order of 10^6A/cm^2 for Cu interconnects. Referring to Figure 11, the top metallization has a smaller cross-section area of 100 µm width by 2 µm thick as compared to the 100 µm width by 5 µm thick cross-section of the bottom metallization. Overstressing the current density may result in an alternative failure mechanism which is undesirable for our purpose of study, so the input current is calculated based on the highest uniform current density, ie. in the top metallization. Calculations reveal that an input current of 3A is needed to achieve a uniform current density of 1.5MA/cm^2 for the top metallization. This translates to a uniform current density of 0.6MA/cm^2 for the bottom metallization. Commercial EM testers such as the widely used Qualitau offer up to 1A; whilst the Aetrium in our lab only offer up to 200mA respectively. The Keithley SMU (Source Measurement Unit) model 2602A is capable of sourcing 3A per channel (A or B) suits this aspect. Other SMU (NI LabVIEW compatible) can also be used, where the amount of source current for the tester is only limited to the SMU chosen.

Data Acquisitions and Logging

To program the SMU and record the resistance data obtained, a PC with NI (National Instruments) LabVIEW will be used. A VI (virtual instruments), which is a program developed using LabVIEW, is written to interface with the SMU will perform continuous data acquisitions over the period of the EM test.

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Number of samples that can be tested limited by single current source

From the statistical point of view, EM reliability data usually contains 15 or more samples. Commercial testers have the capability of running such a sample population or more in parallel with the availability of dedicated current source for each DUT. As the choice of SMU is limited to only those with 3A specification, the tester design must be such that a minimum number of the expensive SMU will be used and yet obtain reasonable amount of throughput. A daisy-chain type of EM test structure will be suitable in this case because only a single current source is needed when connected to the series of DUT in the daisy chain; with each DUT seeing the same amount of stressing current.

Resistance data is needed for each TSV in the daisy-chain

There are 2 channels available in the SMU with 1 channel used as 3A current source. Without having to PC interface with additional voltmeters, the other channel left on the SMU can be used to measure voltage. However, there needs to be some kind of a control circuit to switch across each TSV in the daisy-chain at regular intervals. A control circuit consisting of a microcontroller (MCU) and multiplexers (MUX) is designed and programmed to interface with the same VI so that resistance across individual TSVs in the daisy-chain can be obtained using a single channel. The MUX used are analog type since voltage readings are not of digital (1s or 0s) nature. The interfacing with this control circuit is also interfaced with the PC using the same VI.

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Non-termination of test in the event of failure

In the event of a failed TSV characterized by a specific % increase in its resistance, stressing has to be stopped for the failed TSV(s); whilst continued on the "surviving" TSVs in the daisy-chain so as to maximize the data samples from a single test. For this reason, dedicated relays are added to act as a "jumper" for individual TSV in case of failure or open-circuit, shunting the stressing current so that the remaining TSVs can be tested until test termination. These relays are controlled by the micro-controller and implemented in the same VI.

The schematic design of the in-house EM tester is shown in Figure 31.

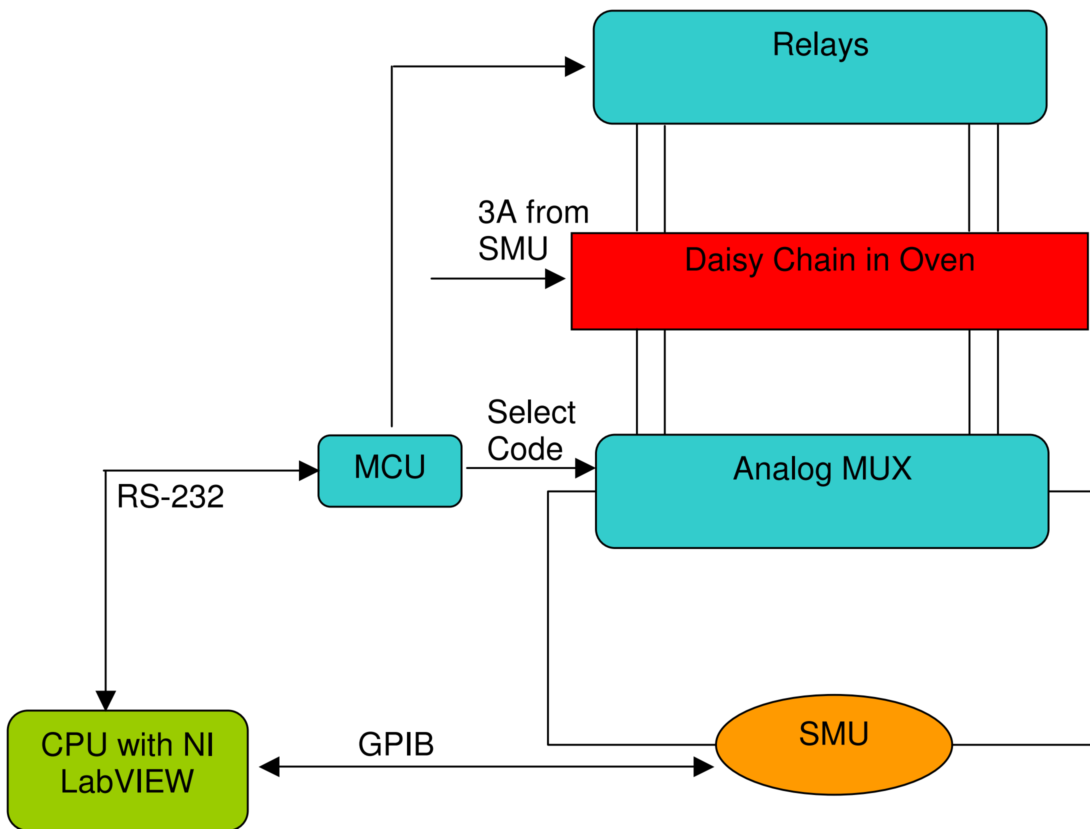

Figure 31. Schematic diagram of designed tester.

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5.2.2 Electrical Implementation

With the above considerations, the electrical design of the control circuit block is shown in Figure 32. Connections for VDD, GND, crystal etc. are omitted from this schematic to maintain simplicity. The same goes for connections from MCU to RS-232 (DB-9 type) and MCU to PPI (Programmable Peripheral Interface). These connections are of standard type application and can be found in their datasheet and also ref [69-72] . A PPI is used to increase the number of I/O ports so as to "future proof" the tester such that additional functionality can be easily added on. It must be noted that a MAX232 or equivalent must be included which functions as a driver/receiver between the high level EIA-232 voltage for the serial port and 5V TTL/CMOS level for the MCU.

The remaining connections shown in the schematic are specific pertaining to the program written in this work, but can vary so long as consistency is maintained between the hardware and the code. The bottom half of Figure 32 shows the connections between the relay, MUX the TSV in the daisy-chain to fulfill the function described in Section 5.2.1. 555s are used to supply enough current for driving the relays. "Kick-back" diodes and by-pass capacitors are also added to ensure a robust design. Since DC power supply is used to power all the components in the circuit, thus there is no need for external voltage regulators and supply filters.

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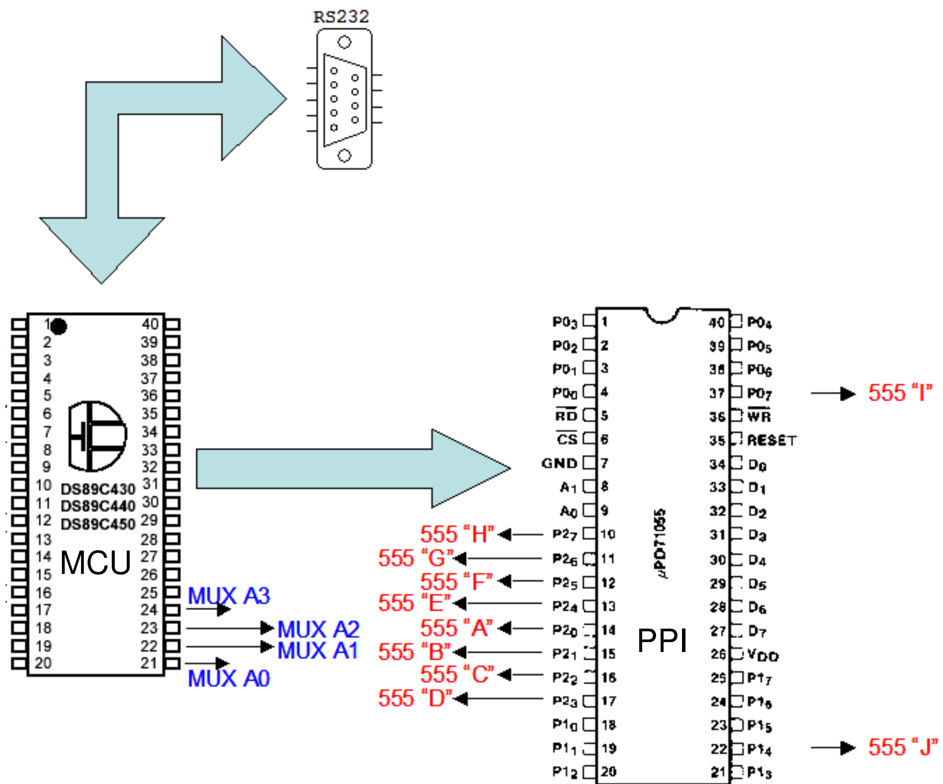

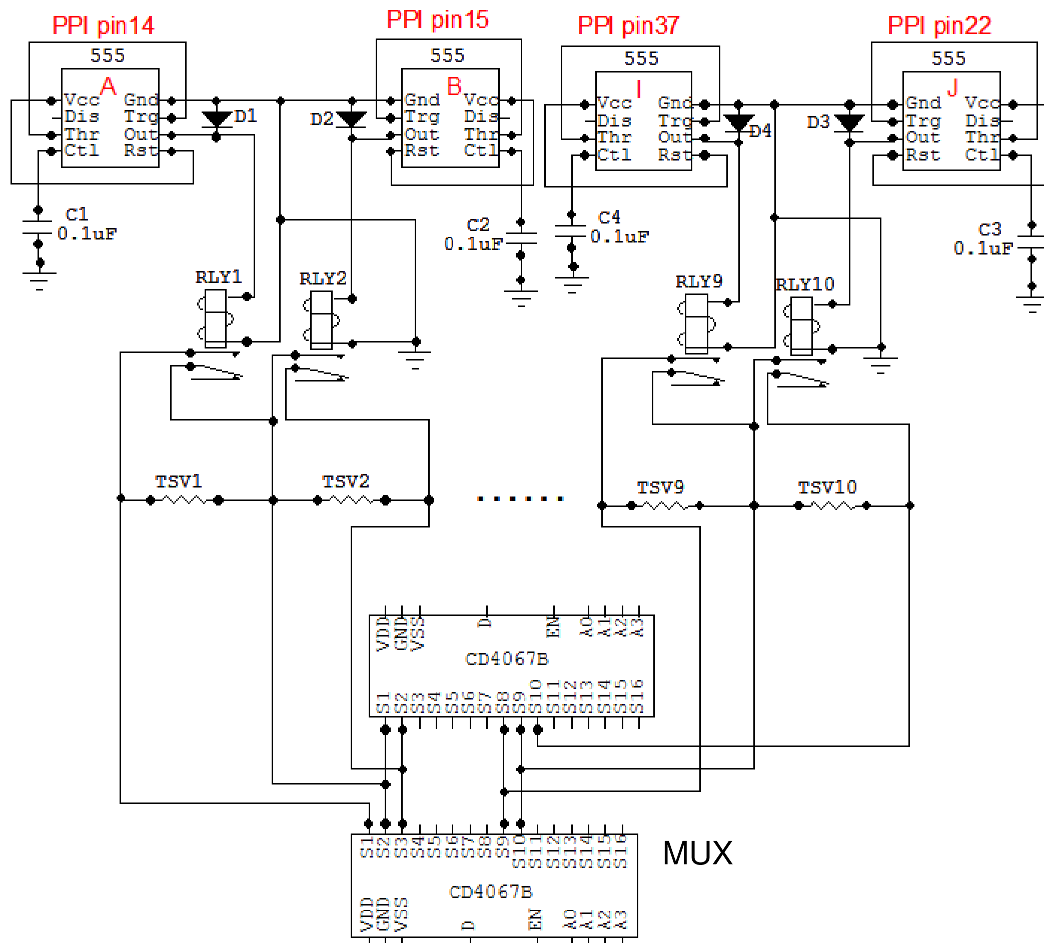

Figure 32. Circuit schematic of control block.

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5.2.3 Software Implementation

LabVIEW VI

Figure 33 shows the front panel, which is the user interface; and Figure 34 shows the block diagram, which resembles a flowchart. The front panel imitates a real physical instrument with some notable additions. Besides having controls to setup the mode of source and measurement, there are also indicators for values read out. Before running the VI, correct addressing have to be selected for the GPIB port and RS-232 serial port. There are plots labeled A to J for each of the 10 TSVs in the daisy-chain.

The block diagram utilizes a flowchart style of programming which LabVIEW converts to programming code in the background. The execution of this program will be in running sequence (i) to (x). In (i), the SMU and RS-232 is initialized and set-up. After the SMU is configured, (ii) enables and turns on each channel of the SMU. (iii) is a while loop which will acquire the data across a TSV in the daisy-chain for each iteration until test termination and (iv) sets the loop execution rate to once per second. (v) behaves like a shift register, producing “A” to “J” for each iteration written to the serial port in (vi). Resistance values are then obtained in (vii) by dividing voltage by current and ready to be written into a spreadsheet file (see “Write To Measurement File” icon). (viii) is a case structure consisting of 10 cases, 1 for each TSV in the daisy-chain. In each case, the resistance value for a specific TSV will be logged into its respective spreadsheet file. This value is plotted real-time in the respective graphs on the front panel. Also in each case, the resistance is compared with a pre-determined value of the failure criterion. The output of the comparison is carried into (ix), where it will determine the value

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written to the serial port. The implementation of (ix) is as such because the 4 most significant bits will inform the MCU to turn on the relay. For example, when the comparison is true for the third TSV ie. TSV “C” has failed, 0000 0011 will be written instead of 1000 0011 (binary for ‘C’). The 4 least significant bits, which are used as select code for the MUX, remains unchanged regardless of failure or surviving. The MCU will check the serial data read and the corresponding relay is switched on when serial read is less than 1000 0000. Termination of the EM test exits the while loop, then (x) turns off both SMU channels and closes both GPIB and serial communication.

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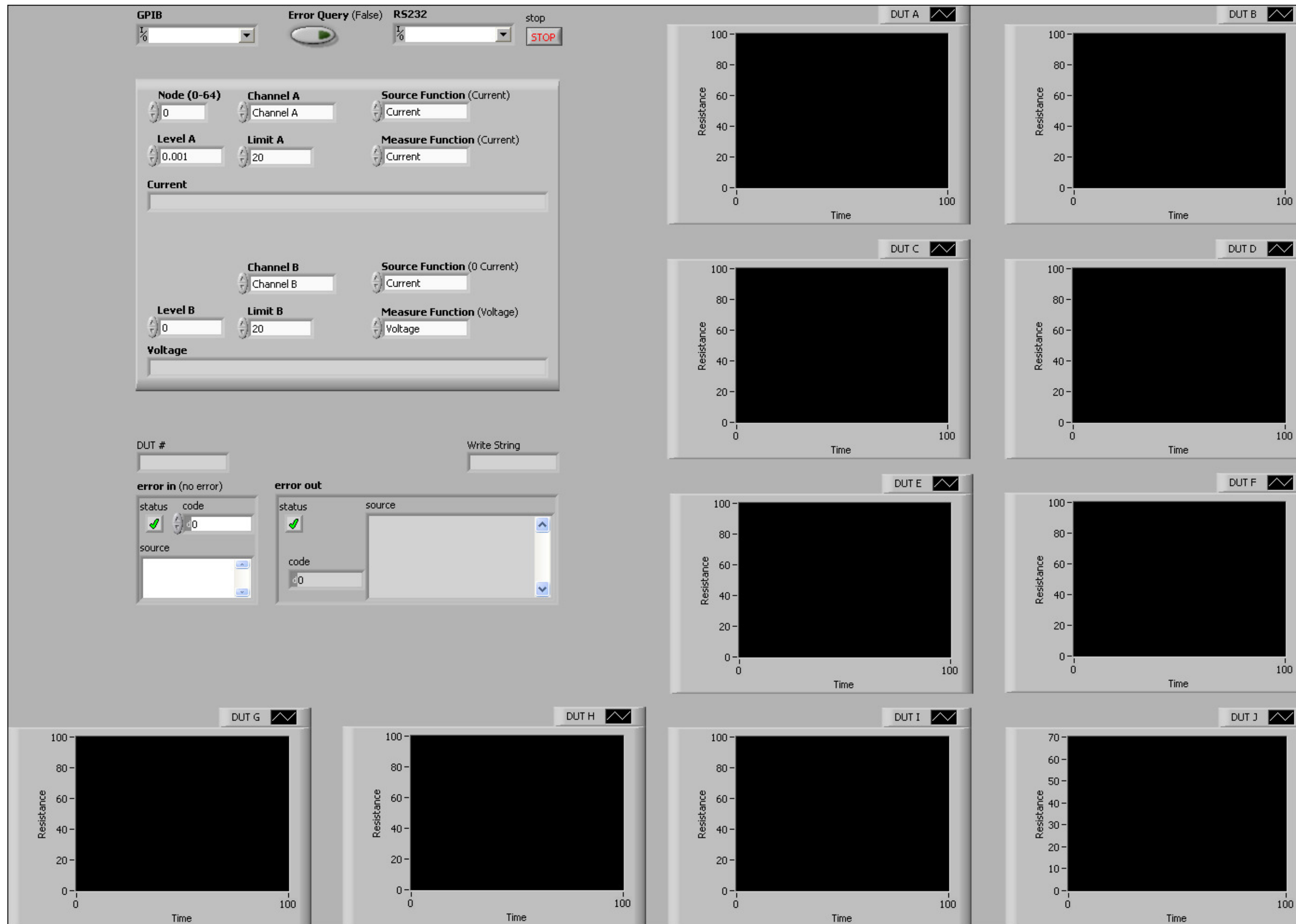

Figure 33. Front Panel of designed VI.

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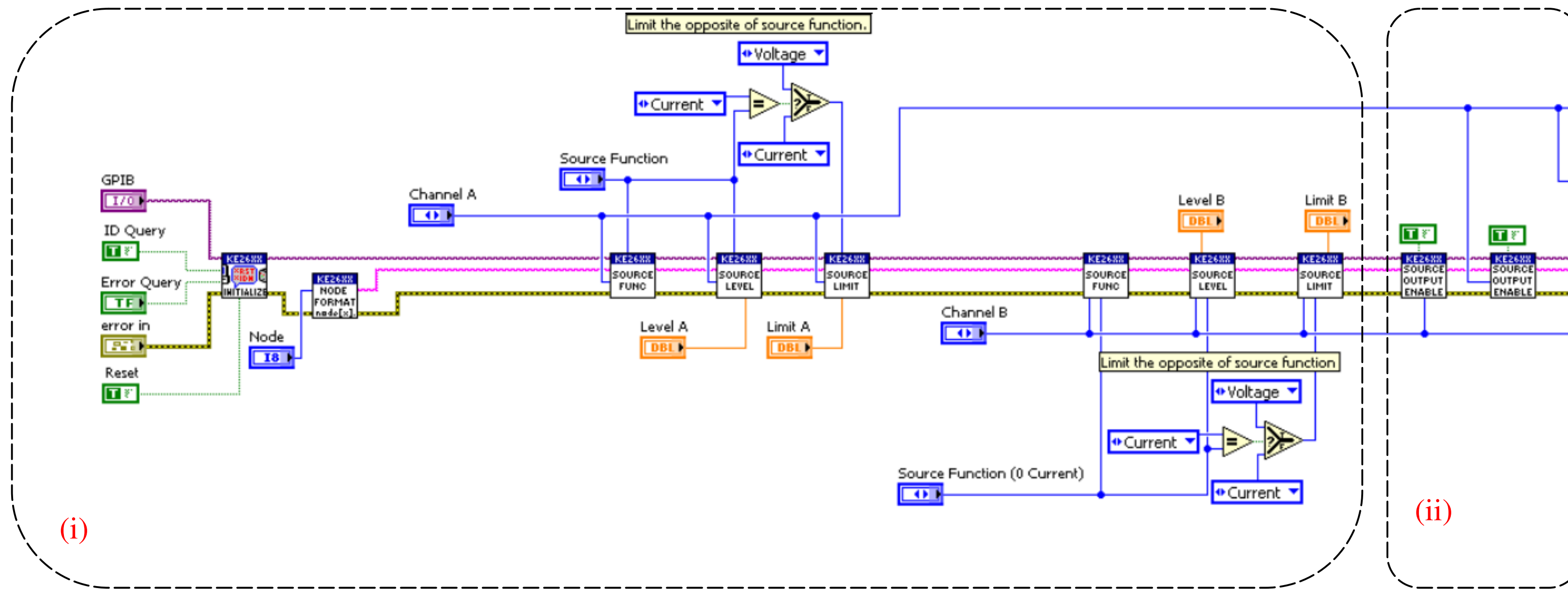

Figure 34. Block diagram.

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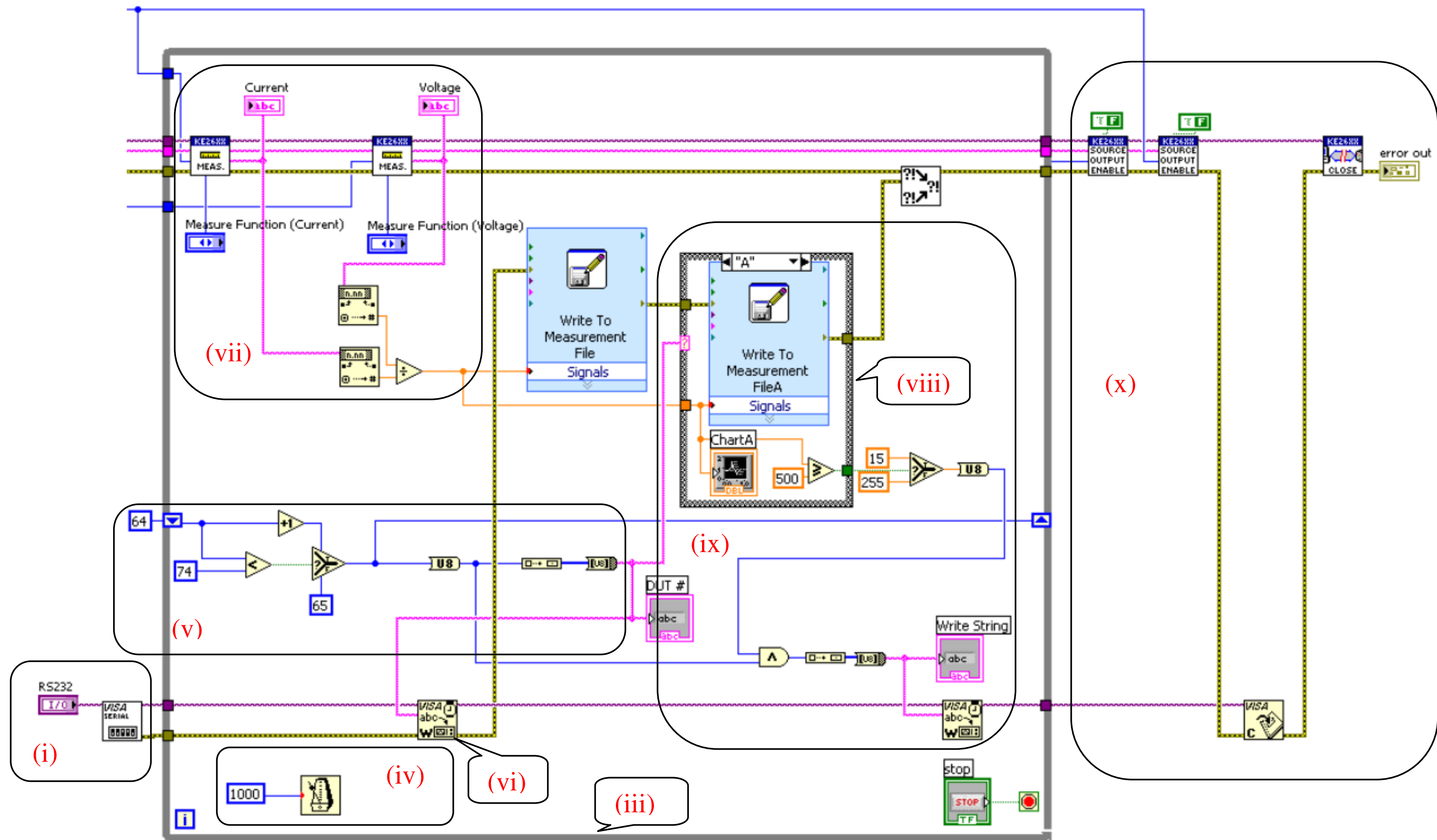

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MCU programmed using C

The MCU is loaded with a lightweight C program and the code can be found in Appendix A. The pseudo code is shown below.

Initialise MCU Port 2 to 0

Initialise all PPI output to 1 //Turn off all relays

Declare variable "labview" of char type

While (true)

a. "labview" = serial read
b. if "labview" < 0x40
    a. switch ("labview")
        i. case 0x01: PPI Port C Bit0 = 0 and break //Turn on Relay A
        ii. case 0x02: PPI Port C Bit1 = 0 and break //Turn on Relay B
        iii. case 0x03: PPI Port C Bit2 = 0 and break //Turn on Relay C
        iv. case 0x04: PPI Port C Bit3 = 0 and break //Turn on Relay D
        v. case 0x05: PPI Port C Bit4 = 0 and break //Turn on Relay E
        vi. case 0x06: PPI Port C Bit5 = 0 and break //Turn on Relay F
        vii. case 0x07: PPI Port C Bit6 = 0 and break //Turn on Relay G

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viii. case 0x08: PPI Port C Bit7 = 0 and break //Turn on Relay H

ix. case 0x09: PPI Port A Bit7 = 0 and break //Turn on Relay I

x. case 0x0A: PPI Port B Bit4 = 0 and break //Turn on Relay J

c. else Port 2 = labview

The 4 least significant bits of the MCU Port 2 is used for the MUX select code, which is determined from the LabVIEW VI. A case structure is also implemented in the event of failure, again notified by the VI, whereby the relay corresponding to the failed TSV will be turned on.

A photo of the actual build up is shown in Figure 35.

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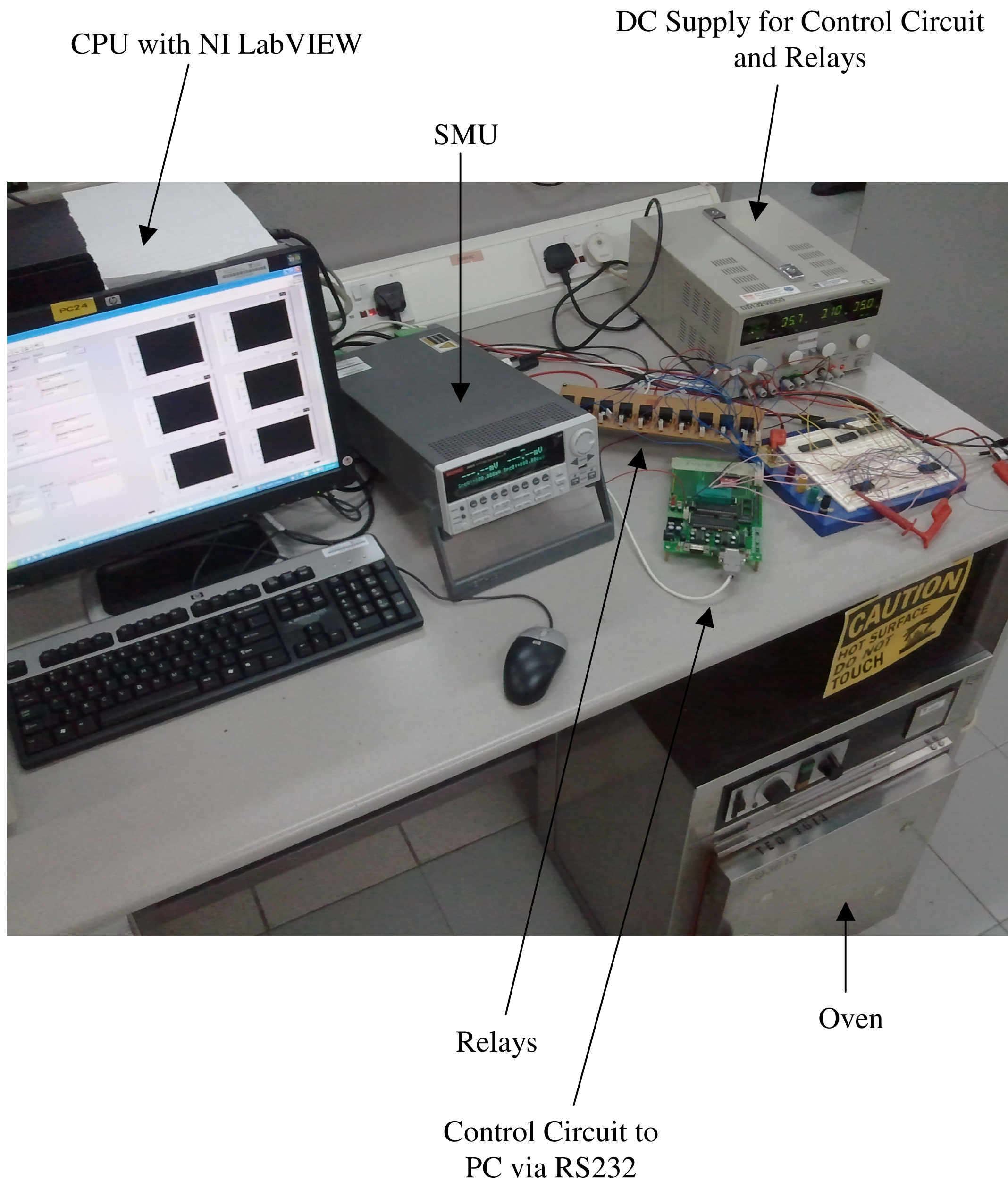

Figure 35. Photograph of in-house EM tester showing different components.

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5.3 Considerations for Revised Test Structures

Through the process of designing and building the in-house EM tester, certain guidelines can be drawn out in terms of plan for future EM test structures. The conclusions drawn from Section 5.1 can also be applied here and this section will describe some of the considerations proposed.

Let R_a and R_b shown in Figure 30 (b) be 2 adjacent TSVs in a daisy-chain, with 2 connections out from M2 line to R_m and R_n ; and 2 connections out from M1 to R_M and R_N . A top-view schematic of such a design is shown in Figure 36. There are some points to be noted when considering such a design.

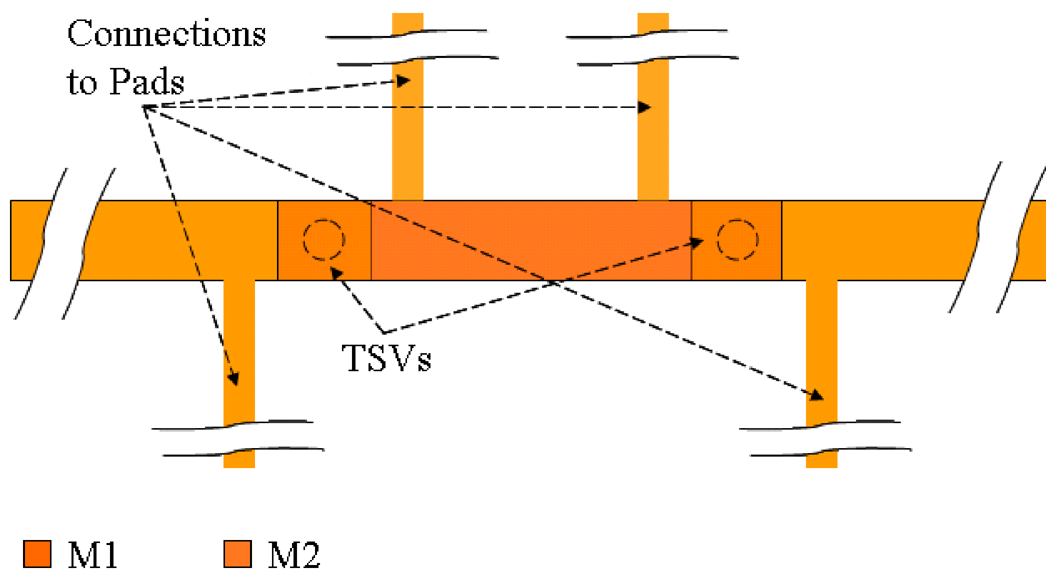

Figure 36. Top view of proposed test structure.

In Section 5.1, it was understood that one of the main advantages of using the proposed Kelvin Double Bridge method is that any EM damage on the interconnect limited to between the 2 adjacent DUT, which can potentially mask

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the actual damage near the DUT, will be yielded irrelevant in terms of resistance extraction. As the M2 line in the actual TSV sample (Si interposer) is significantly thinner than the M1 line, it may be assumed that M2 is more critical than M1 in this case. Therefore, the choice of M2 to have connections out for R_m and R_n is a logical one.

As shown in Figure 36, the connections out for pad are narrow and perpendicular to the chain to reduce heat-sinking effects [54]. It should also be mentioned here that these connections must be placed as close to the TSV as possible, but some simulations may have to be performed to confirm any influence such as significant changes in the thermal profile affecting the AFD at the predicted failure site considerably. The voltage taps must be long to avoid possible "replenishing" effects to voiding location from the pad at the other end of voltage tap [73]. Future work can include further simulations to evaluate the extent of EM damage in the voltage taps respective to the failed TSV because the stressing current will then flow through these taps in the event of failure. It may be possible to optimize the placement and design of the voltage taps so that any EM damage in these taps will be minimized and they will not fail before test termination.

Besides allowing for external Kelvin Double Bridge configuration, this test structure also allows for the flexibility of using the traditional Four-probe method in the in-house EM tester. Therefore, future experiments can be performed to compare the different resistance measurement methods.

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Chapter 6 Future Work

It is shown in this work that EM can indeed occur in TSVs and it is worthwhile to look into this important aspect for a more complete reliability study. Simulations have been performed and some important conclusions have been drawn. However, this work is just a starting point in this direction of research and some initial groundwork for experimental verifications have been laid. It is therefore hoped that further research will be carried out in this area especially with suitable EM reliability data. This is especially so for the resistance measuring method proposed in Chapter 5. It will be interesting to compare, for example, the difference in EM lifetime data using the different resistance measuring methods.

As there has been very little reported works on EM study in TSVs, its importance is still rather understated. The simulations verified with experimental evidence can help better understand the physics of EM in TSVs. Physical failure analysis on failed samples can be carried out to verify the location of the voids vs the maximum AFD location. Data analysis from the EM tests can also bring more insight to the dominance of one failure mechanism, if there are any. Void evolution may also be studied experimentally to see the effect of metallization coverage and if there is any effect on say, early failure for example. The study on the impact of metallization coverage may also be extended to include various degree of coverage.

Although the scope of this work limits itself to fully filled copper TSVs for interposer application, future study can be performed on other TSV variations such

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as TSVs with polymer sidewall lining, “hybrid TSV” of polymer filled core with metal sidewall, and annular shape TSVs. For example, having a partially Cu filled TSV yield several advantages such as reduced electroplating time and stress due to the significant decrease in Cu content compared to surrounding Si. Using a “softer” polymer as the core can also help relax the stress in the Cu sidewall. However, there may be some trade-off in terms of EM performance with regards to the benefit gained discussed above. This is because the relative thinner layer of Cu in these TSVs can see a significant increase in localized current crowding density and severe thermal and stress gradient may result. As have been shown in this work, it is the thermo-mechanical stress gradient which is the dominant contribution to high AFD. EM failure mode can shift further into the via itself as it is also easier for the voids in the thin sidewall to grow to a critical size for EM failure.

As a reliability study concerns itself with an extension of quality in the time dimension, the relationship between AFD and EM lifetime can also be developed further so that meaningful prediction of time to failure can be estimated from the simulated AFD values.

Although the in-house EM tester should be capable of performing EM experiments on the future samples, it can be further developed to add more functionality. For example, the different resistance monitoring methods discussed in Section 5 can be integrated into the EM tester program, as it is designed to use Four-probe measurement at this stage. Although the prototype built and shown in Figure 35 consists of a mixture of test boards and veroboards as it is in the early stage, the

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whole circuit can be put into a PCB design eventually. The bridge circuit for resistance monitoring may also be designed in an IC chip. LabVIEW, being a powerful tool can allow improvements to be made to the current prototype, such as interfacing LabVIEW with precision equipment to record temperature measurements during EM tests.

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Chapter 7 Conclusion

EM modeling has been done on TSV in Si interposer using FEA. It is found that thermo-mechanical stress is the dominant factor for EM in the studied TSV application. By reducing the thermal gradient at high AFD locations, the AFD is shown to reduce significantly. As such, efforts to improve thermo-mechanical reliability of TSVs through reducing the thermo-mechanical stress can also aid in improving its EM reliability.

Next, it is shown through simulations that the AFD can be very different due to the different metallization scheme and the geometrical dimensions. The simulations show that most failures may be observed only on the top side of the interposer, at the corner where the metallization meets the TSV. This exhibits a strong asymmetrical behavior in terms of EM experimental failure between top side and bottom side.

Worse EM performance can also be expected for metallization that extends to cover half the via, as compared to one that covers the via fully. An additional location of sufficiently high AFD is found to be in the vicinity of predicted EM location. Further simulations show that voids can grow concurrently and meet to merge, resulting in a earlier failure. This implies that a novel coverage pattern can be found to optimize the EM performance of a TSV structure.

Experimental verifications have being planned for the future and some aspects of the TSV specific EM test have been presented. For resistance monitoring

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methods, the advantages and drawbacks of each method are explored qualitatively. A new method based on the Kelvin Double Bridge is proposed to further increase the sensitivity of resistance measurement. An in-house EM tester for the planned samples is also designed and built.

Lastly, some guidelines have been proposed for designing future EM test structures by considering the different lessons learnt and presented in this work. It is worthwhile to re-iterate here that due care must be taken for the placement and design of voltage taps to avoid possible inaccurate result. The reasons for such caution are as mentioned earlier, and this is even more so if the predicted EM location is near to the voltage taps. The first design of test structures are already in the process of fabrication, and experiments are expected to be carried out in due course.

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Appendix A – C program loaded into MCU flash

```
#include <DS89C4xx.H>
#include <absacc.h>
#define PortA 0x4000                    //PPI PortA address
#define PortB 0X4001                    //PPI PortB address
#define PortC 0X4002                    //PPI PortC address
#define Control_Register 0x4003         //PPI Control Register address

void delay(int time)                    //time delay
{
        int i,j;
        for(i=0;i<time;i++)
        for(j=0;j<1200;j++);
}

unsigned char rx(void)
{
        while (RI_0 ==0);               //check RI until set
        RI_0=0;
        return(SBUF0);
}

main (void)
{
char labview;

delay(5000);                    //wait for PPI to reset, PPI reset slower than MCU

XBYTE[Control_Register] = 0x80;         //initialise PPI all ports output
XBYTE[PortA] = 0xFF;                    //turn off relays
XBYTE[PortB] = 0xFF;                    //turn off relays
XBYTE[PortC] = 0xFF;                    //turn off relays
```

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```
SCON0=0x52;                    //initialize serial 4800 BR; 8 Bit; NP
TMOD=0x21;
TH1=0xFA;
TR1=1;

P2=0;                          //multiplexer select code initialise to zero

      while(1)
      {

      labview=rx();                  //receive from labview via rs232

      if (labview < 0x40)
      {
            switch(labview)
            {
                  case 0x01 : XBYTE[Control_Register]=0x00; break;   //turn
                  on relay 1, relay 1 @ PortC bit 0
                  case 0x02 : XBYTE[Control_Register]=0x02; break;  //turn
                  on relay 2, relay 2 @ PortC bit 1
                  case 0x03 : XBYTE[Control_Register]=0x04; break;  //turn
                  on relay 3, relay 3 @ PortC bit 2
                  case 0x04 : XBYTE[Control_Register]=0x06; break;  //turn
                  on relay 4, relay 4 @ PortC bit 3
                  case 0x05 : XBYTE[Control_Register]=0x08; break;  //turn
                  on relay 5, relay 5 @ PortC bit 4
                  case 0x06 : XBYTE[Control_Register]=0x0A; break;  //turn
                  on relay 6, relay 6 @ PortC bit 5
                  case 0x07 : XBYTE[Control_Register]=0x0C; break;  //turn
                  on relay 7, relay 7 @ PortC bit 6
                  case 0x08 : XBYTE[Control_Register]=0x0E; break;  //turn
                  on relay 8, relay 8 @ PortC bit 7
                  case 0x09 : XBYTE[PortA]=0; break;  //turn on relay 9,
                  relay 9 @ PortA bit 7
```

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```
                    case 0x0A : XBYTE[PortB]=0; break;  //turn on relay 10,
                    relay 10 @ PortB bit 4
                }
            }

        P2=labview;     //send labview data to multiplexor select

        }
}
```

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