A Digital Time Skew Calibration Technique for Time-Interleaved ADCs

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***Abstract*— In this paper, a digital time skew calibration technique for time-interleaved (TI) ADCs is presented. The time skew calibration for TI-ADCs in analog domain suffers from limited correction accuracy and additional jitter. And the proposed digital time skew calibration method estimates the polarity of the time skew through correlation of adjacent channels and corrects the time error by adopting adaptive fractional delay filters iteratively. Simulation results show that, in a 4-channel 1GS/s 12-bit TI-ADC system, the SFDR can be improved to 78dB by 5-order FIR filters within a calibration range of [-0.005/f_s, +0.005/f_s].**

I. Introduction

Time-interleaved (TI) analog-to-digital converters (ADCs) are crucial for high-speed and high-resolution ADCs design [1-4]. A block diagram of M-channel TI-ADCs is presented in Fig. 1. The input signal is sampled by a multi-phase clock with frequency f_s/M and multiplexed in digital domain with a digital clock with frequency f_s. The sampling rate of the TI-ADCs could be increased proportionally with the number of channels. However, there are mismatches between channels owing to PVT variation, such as offset mismatch, gain mismatch, time skew and bandwidth mismatches, leading to performance degradation in terms of linearity. These mismatch calibrations can be categorized into foreground [5-7] and background [8-13] calibrations. Generally, the background calibration techniques are preferred as it does not interrupt normal operation of TI-ADCs and could track environmental variation (e.g. temperature, process aging). Numerous approaches have been published to solve the mismatches in time-interleaved ADCs [2-13]. Time skew correction in analog domain may induce additional jitter, and the obtained precision is limited. Traditional time skew correction in digital domain suffers from long tap FIR filters, which is power hungry and increases the latency for ADCs with high sampling rates.

In this paper, a time skew calibration technique, which operates fully in digital domain, including estimation and correction, is proposed. The presented calibration technique achieves >75dB SFDR with only 5-tap adaptive fractional delay filters. The remainder of the paper is divided into four sections. Section II gives a brief introduction of mismatches in TI-ADCs. In Section III, the proposed calibration method is described. Section IV shows the design example and simulation results, and finally conclusion is drawn in Section V.

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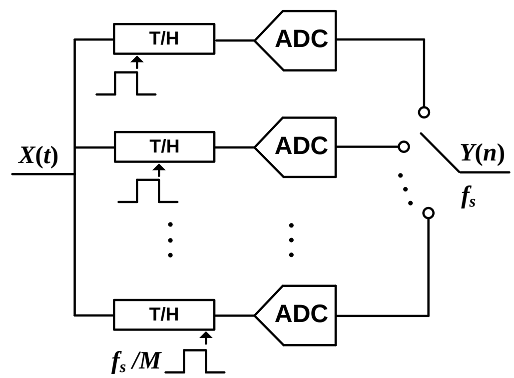


Fig. 1. The structure of time-interleaved ADCs.

II. Mismatches Sources in TI-ADCs

The mismatch model of the M-channel TI-ADCs is shown in Fig. 2, which includes bandwidth mismatch $g'_M(\omega)$, offset mismatch b_M, gain mismatch a_M and the time skew Δt_M normalized by T_s. Detailed discussion of mismatches effects could be found in [6-7]. For the normal calibration priority, offset mismatch is compensated first, then follows the gain mismatch calibration, bandwidth mismatch and lastly, the time skew, which can be calibrated with different techniques [2-13]. Offset mismatch and gain mismatch can be calibrated easily [14-15]. The analysis of bandwidth mismatch and a filter bank based calibration technique was presented in [16]. The time skew could be compensated by post digital processing with long-tap FIR filters [14]. However, the coefficient multipliers increase computational complexity and silicon area. In [6], a digital filter bank with optimized coefficients was adopted to compensate all the mismatches in TI-ADCs, but time skew mismatches are obtained through off-line measurement. Similar to [8], a multi-channel filter based calibration method presented in [5] ignored the time skew estimation. The time skew calibration methods reported in [4], [7], [9], [11] corrected the time skew error by tuning the delay of clock signal. However, the tuning accuracy is process limited and the jitter performance of clock signal may

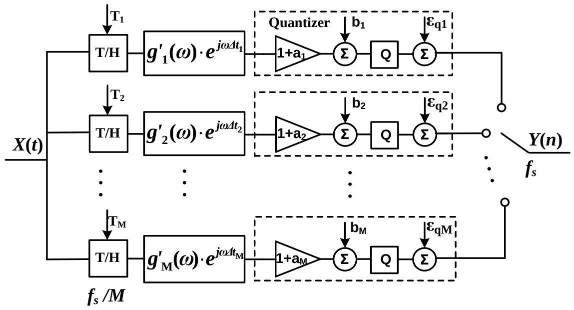


Fig. 2. The model of *M*-channel time-interleaved ADCs, including bandwidth mismatch, offset mismatch, gain mismatch and time skew.

be degraded.

III. Proposed Calibration Technique for TI-ADCs

A. Digital fractional delay filter design

In this section, the design of digital fractional delay filter is proposed. Supposing T as clock period, and $T_d=\alpha T$ is the fractional delay time, where α is the delay parameter. Prior works [17], [18] on fractional delay filter optimized the filter coefficients in entire delay range -0.5< α <0.5, which results in polynomial approximation with order larger than 2 in order to achieve expected linearity. For time skew calibration, the range of α is usually within -0.02< α <0.02 [11]. Optimization for α in a small range reduces the order of polynomial approximation and FIR filter length, and equivalently, reducing hardware overhead and power consumption. The ideal transfer function of a filter with delay $(\alpha+\beta)T$ is given by

$$D(\omega,a)=e^{-j\omega(\alpha+\beta)T}, \tag{1}$$

where α is the fractional delay and β is the integer delay. Here, the coefficients of FIR filter are approximated by the linear polynomial of fractional delay α. Therefore, the transfer function of the FIR filter is

$$F(\omega,a)=\sum_{n=0}^{N-1}(c_{n,0}+\alpha c_{n,1})e^{-j\omega nT}, \tag{2}$$

where N is the number of tap. The difference between ideal transfer function and the real transfer function, namely, the approximation error, is given by

$$e(\omega,\alpha)=F(\omega,a)-D(\omega,a)\ . \tag{3}$$

The approximation error should be minimized by using certain criterion. The FIR filter coefficients $C_{n,m}$=[$c_{0,0}$, $c_{0,1}$, $c_{1,0}$, $c_{1,1}$, …, $c_{N-1,0}$, $c_{N-1,1}$], whose length is $2N$, are to be optimized. The transfer function of $F(\omega,\alpha)$ can be rewritten as

$$F(\omega,a)=C_{n,m}\cdot(c(\omega)-js(\omega))^{\mathrm{T}},$$

where $\boldsymbol{c}(\omega)$=[1, 1, cos(ω), cos(ω),…, cos((N-1)ω), cos((N-1)ω)], and $\boldsymbol{s}(\omega)$=[0, 0, sin(ω), sin(ω),…, sin((N-1)ω), sin((N-1)ω)]. To minimize the approximation error, the following min-max problem need be solved:

$$\min_{C_{n,m}}\{\max|e(\omega,\alpha)|\},\qquad \omega\in\Omega,\ \alpha\in A, \tag{4}$$

where $C_{n,m}$ contains all the filter coefficients to be optimized. Ω and A are the frequency band and time delay range of optimization respectively. The objective in (3) can be written as

$$\begin{aligned}&|e(\omega,\alpha)|\\&=|F(\omega,\alpha)-D(\omega,\alpha)|\\&=\left\|\begin{bmatrix}R^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha)\\ I^F(\omega,\alpha)\,C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha)\end{bmatrix}\right\|_2\\&=[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\end{aligned}$$

where

$$\begin{aligned}&R^D(\omega,\alpha)=[D(\omega,\alpha)]_R,\ I^D(\omega,\alpha)=[D(\omega,\alpha)]_I\\&R^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_R\\&I^F(\omega,\alpha)=[(c(\omega)-js(\omega))]_I\\&R^{FD}(\omega,\alpha)=R^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-R^D(\omega,\alpha)\\&I^{FD}(\omega,\alpha)=I^F(\omega,\alpha)C_{n,m}{}^{\mathrm{T}}-I^D(\omega,\alpha)\end{aligned}$$

Here $[\cdot]_R$ and $[\cdot]_I$ represent the real and imaginary parts of a complex number or vector respectively. Therefore, the min-max problem can be reformulated as

$$\begin{aligned}&\min_{C_{n,m}}\quad \delta\\&\text{subject to}\quad \delta-[R^{FD}(\omega,\alpha)^2+I^{FD}(\omega,\alpha)^2]^{1/2}\geq 0\,.\end{aligned} \tag{5}$$

And the above optimization problem within a certain range of frequency ω and fractional delay value α could be solved by a standard SOCP solver [19], which is

$$\begin{aligned}&\min_{x}\quad c\cdot x\\&\text{subject to}\quad c\cdot x\geq\|Fx-d\|_2,\end{aligned} \tag{6}$$

where c=[1, zeros(1,2N)], $x=[\delta,\ C_{n,m}]^{\mathrm{T}}$, F=[0, $R^{\mathrm{F}}(\omega_i,a_j)$; 0, $I^{\mathrm{F}}(\omega_i,a_j)$], $d=[R^{\mathrm{D}}(\omega_i,a_j),\ I^{\mathrm{D}}(\omega_i,a_j)]^{\mathrm{T}}$, i=0, 1,…, I, j=0, 1,…, J. And I and J are the number of frequency points and fractional delay points for computation respectively.

B. Time skew calibration for TI-ADCs

The block diagram of a 4-channel TI-ADC depicting the proposed calibration technique is shown in Fig. 3. The calibration structure is a close-loop iterative system. The proposed calibration scheme has no stringent requirement on the reference input. Setting the first sub-channel as the reference channel, the delay of other 3 channels are tunable through variable fractional delay filters $F(\alpha_m)$ (m=1, 2, 3). The time skew estimation approach in [7] is adopted, and multiplication is conducted between every two adjacent channels, then the output value $p(t_m)$ (m=0, 1, 2, 3) of the accumulator and average unit is the approximation of the mean value $E_N[M]$. Then, every two adjacent $E_N[M]$ are compared. The delay parameter $\alpha_{m,m+1}$ of the delay filter $F(\alpha_{m,m+1})$ add or subtract one time step t_{step} according to the $E_N[M]$ comparison result. The convergence of the close loop system has been proven in [7]. Fig. 4 depicts an

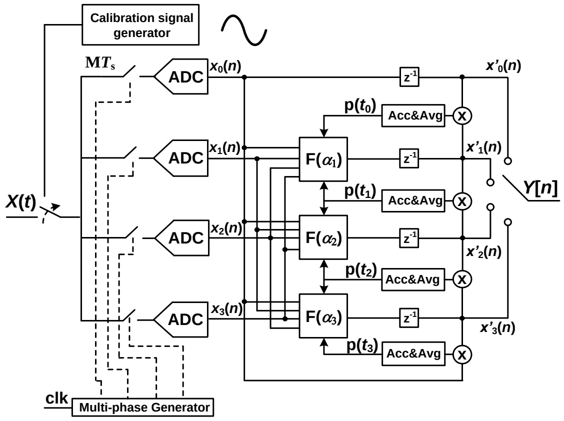


Fig. 3. The proposed calibration architecture.

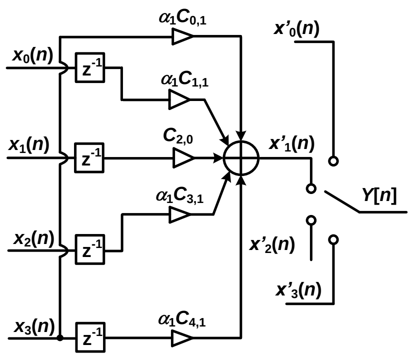
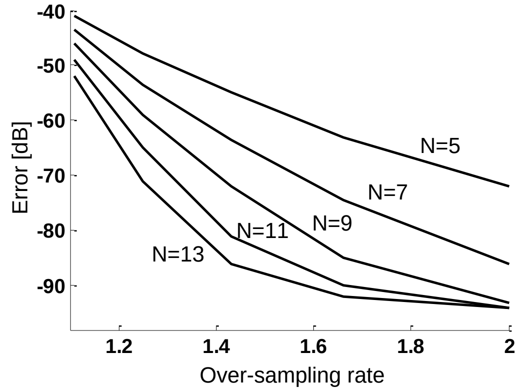


Fig. 4. Implementation structure for $F(\alpha_1)$ with 5-tap FIR filter with coefficient using linear polynomial of fractional delay α_1.

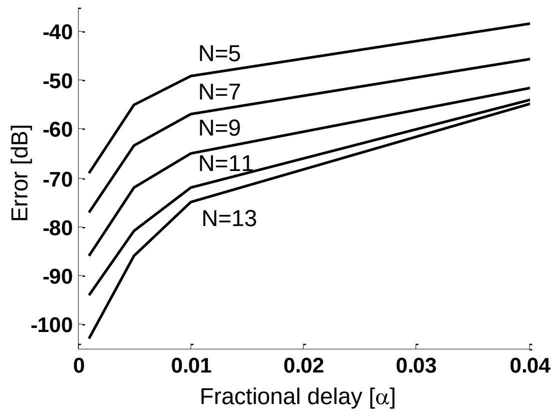
implementation structure of a 5-tap fractional delay FIR filter. The coefficients use linear polynomial approximation. The α_m in Fig. 4 represents the time skew of $x_1(n)$. Since the range of fractional delay for time skew calibration is comparatively small, 20ps time skew for 1GS/s ADC system is reasonable. Therefore, the linearity could be calibrated to be 80dB by using the proposed short-tap FIR filter calibration technique. The number of taps of the fractional FIR filter is not necessarily long and 5~13 taps are reasonable for most implementations. The relations of over-sampling rate, fractional delay, number of taps N and error suppression are illustrated in Fig. 5.

IV. Simulation Results

In this section, a 4-channel 1GS/s 12-bit TI-ADC system is designed to demonstrate the proposed calibration technique. The over sampling rate is 1.6. The fractional delay range for optimization is α=[-0.005, 0.005]. Using the SOCP solver, the optimization result for a 5-tap fractional FIR filter is shown in Fig. 6. And the corresponding optimized coefficients of FIR filter are listed in Table I. The small coefficients are set to 0. The input signal for calibration $x(t)$ $=\sin(2\pi f_{i1}t)+\sin(2\pi f_{i2}t)+\sin(2\pi f_{i3}t)+\sin(2\pi f_{i4}t)$, f_{i1}=63.5MHz, f_{i2}=133.8MHz, f_{i3}=204.1MHz, f_{i4}=235.3MHz. The reference channel is channel 1. Setting the time skew of the other three channels to [Δt_1, Δt_2, Δt_3] = [2ps, -3ps, 5ps]. The tuning time step is 0.1ps. The number of samples needed to accumulate and average N is set to 20,000. The 1024-point fast Fourier



(a)



(b)

Fig. 5 (a) Error level versus over sampling rate with different N and a=[-0.005, 0.005]. (b) Error level versus fractional delay range with different N and oversampling rate=1.4.

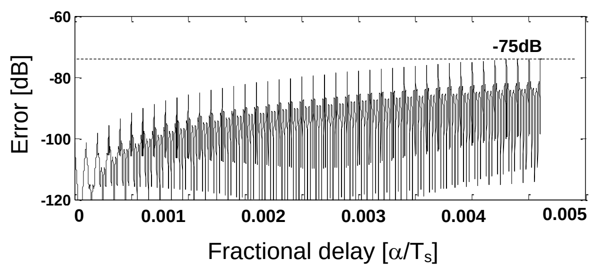
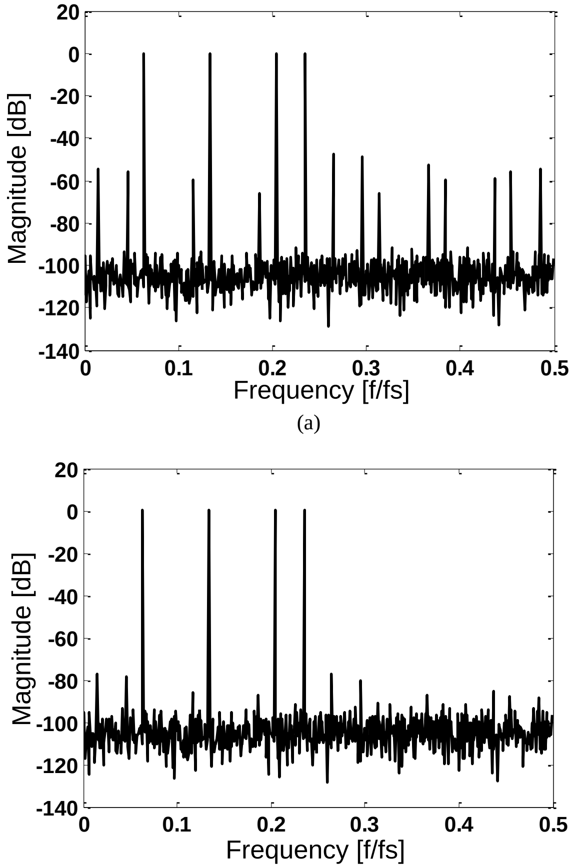


Fig. 6. Convergence of the optimized time delay values.

TABLE I
Optimized Filter Coefficients

$C_{n,m}$	m=0	m=1
n=0	-5.6e-7 (0)	0.1453
n=1	6.3 e-6 (0)	-0.7602
n=2	1	-1.3e-13 (0)
n=3	6.3 e-6 (0)	0.7602
n=4	-5.6e-7 (0)	-0.1453

transform (FFT) of output signal before calibration is shown in Fig. 7(a), while Fig. 7 (b) shows the FFT of output signal after calibration. It can be seen from Fig. 7(b) that the SFDR can be improved from 48dB to 78dB. The convergence process of calibration is presented in Fig. 8, which shows the calibration is terminated after iterating about 20 times and the optimized time delay value is [α_1, α_2, α_3]= [1.9ps, -3.1ps, 5.0ps].



(a)

(b)

Fig. 7. Calibration results. (a) Before calibration. (b) After calibration.

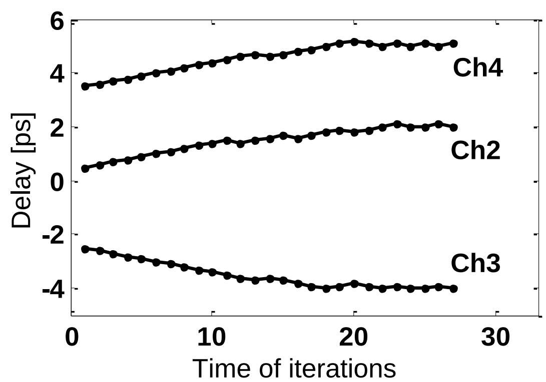


Fig. 8. Convergence process.

V. CONCLUSION

In this paper, an adaptive fractional delay FIR filter based calibration technique for *M*-channel TI-ADCs is proposed. Compared with previous published techniques, it provides a fully digital time skew calibration technique with less computational complexity. And the variable delay filter could also be extended to high order approximation for better accuracy. In addition, the calibration technique is extendable to TI-ADCs with more channels.

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