

Design of High-Speed Low-Power Clock and Data Recovery Circuit

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STATEMENT OF ORIGINALITY

I hereby certify that the content of this thesis is the result of work done by me and has not been submitted for higher degree to any other university or institution.

Date

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ABSTRACT

In this thesis, the design of fully integrated high-speed low-power clock and data recovery (CDR) circuits in complementary metal-oxide-semiconductor (CMOS) devices for synchronous optical network (SONET) applications has been explored.

The majority of the backbone optical communication systems are based on the SONET standards. The “SONET OC-192 Specifications” have been defined for *10-Gb/s* optical communication applications in order to evaluate the jitter performance of the designs.

Despite the aggressive device scaling in CMOS technology, the CDR circuits that are realized in CMOS processes still face significant high-frequency design and speed constraints. When it comes to complying with the stringent jitter requirements posed by the OC-192 standards, CMOS circuits have to *work harder* than their GaAs or SiGe counterparts to overcome the limitations due to the high-frequency parasitics. Extensive research work must be carried out at all fronts related to the CMOS CDRs in order to obtain a total solution to the problems currently faced by the designers.

To contribute to the pool of these solutions, we have proposed several modifications and methods in this thesis. Before going into the detailed discussion, we should note that all the design work presented here is done on the phase-locked loop (PLL)-based CDR architectures and their building blocks.

A 10-GHz voltage-controlled oscillator (VCO) is designed and fabricated in Chartered Semiconductor Manufacturing (CHRT) Foundry's 0.18- μm Analog/RF CMOS 2-poly 6-metal process. The active chip area is 280 μm x 250 μm . The phase noise is measured to be -95 dBc/Hz at 1-MHz offset. The below-3mW power consumption, excluding the buffers, indicates that our design is suitable for low-voltage and low-power SONET applications.

The effect of the supply voltage scaling on the tuning voltage of the VCO is also investigated. A wide tuning range of 2.2 GHz is obtained for 1.8-V supply, whereas this range has reduced to 300 MHz for 1.5 V. This variable VCO tuning range is useful for improving the jitter performance of the overall CDR by providing immunity against the ripples on the VCO control line.

Another critical block in the CDR system is the phase detector (PD). Two methods are proposed, one in circuit level and the other in architectural dimension, in order to make use of the available technology in the best way possible.

The first method involves a modification to the existing D-flip-flops (DFF) such that very high switching speeds can be achieved using the 0.18- μm CMOS devices. Currently, the maximum operation frequency for conventional DFFs in the above-mentioned technology is not exceeding 6 GHz. On the other hand, with our proposed DFF, one can easily achieve 10 GHz with reasonable power consumption. Furthermore, the improvement in the DFF speed directly enhances the PD performance since the main building block of a sequential PD is the DFF. The output voltage swing of 500 mV with a 1.4-V-dc of the *conventional* DFF is too low to

facilitate the proper operation of the devices that are connected to these output terminals, whereas the modified DFF outputs have a wide swing of 1.5 V with a dc average settling at 900 mV. This wide swing is achieved with a 10 mW increase in the power consumption compared to the conventional DFF, which is worth for such convenience in this technology.

The second method describes a novel *dual-rate PD* that can be used in both half-rate and full-rate CDR systems. Additionally, the design retimes the data without an external decision circuit and hence it minimizes the systematic offset. With its total power consumption of 30 mW from a 1.8-V supply, this PD has one of the best power efficiency among the existing PDs. To the best of our knowledge, this is the only PD architecture with *dual-rate* operation capability.

Another issue that bothers the designers is the existence of the loop filter components that hinder the implementation of the *fully integrated* PLL-based CDRs. We have proposed a modified loop filter topology to tackle this problem. The filter capacitor can be selected to be as small as 20 pF so that it can be implemented on-chip using our filter topology.

In order to investigate the collective contributions of the proposed modifications, a fully integrated 10-Gb/s CDR circuit is designed and fabricated in CHRT 0.18- μm CMOS process. Analytical evaluation of the loop parameters indicates that the CDR can successfully satisfy the jitter requirements of the OC-192 standard. The small chip size of 560 μm x 780 μm , low phase noise of the recovered clock of -112.7 dBc/Hz at 1-MHz offset, and low-power consumption of 70 mW from a 1.8-V supply further

enhance the importance of the design as an attractive solution to the 10-Gb/s applications.

Finally, the half-rate PD circuit is also tested in a fully integrated half-rate CDR design example in CHRT 0.18- μm CMOS process. The post layout simulations and the measurement results indicate that the design satisfies the jitter requirements with a phase noise of -114 dBc/Hz at 1-MHz frequency offset. It consumes 85 mW from 1.8-V supply voltage and occupies a silicon space of 820 μm x 840 μm .

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TABLE OF CONTENTS

STATEMENT OF ORIGINALITY	i
ABSTRACT	ii
ACKNOWLEDGMENTS	vi
TABLE OF CONTENTS	vii
LIST OF FIGURES	xi
LIST OF TABLES	xv
CHAPTER 1	1
Introduction	1
1.1 Motivation	1
1.2 Objectives	4
1.3 Major Contributions of the Thesis.....	4
1.4 Organization of the Thesis	6
CHAPTER 2	9
Background	9
2.1 Overview of an Optical Receiver System	9
2.2 Properties of Random Data Formats	11
2.3 Open-Loop and Closed-Loop CDRs	14
2.4 System Parameters	15
2.4.1 Jitter Definitions	15
2.4.2 Jitter Specifications for the OC-192 CDR.....	16
2.5 Summary	19
CHAPTER 3	20
PLL Fundamentals	20

3.1 What is a PLL?	21
3.2 Charge-Pump PLLs and the Transfer Function.....	22
3.3 Locking Behaviour of the CP PLL.....	27
3.3.1 Capture Range	28
3.3.2 Tracking Range	29
3.4 Summary	29
CHAPTER 4	31
10-GHz Integrated Voltage-Controlled Oscillator	31
4.1 Oscillator Fundamentals.....	31
4.2 Ring Oscillators.....	33
4.3 LC Oscillators.....	35
4.3.1 LC Resonators	36
4.3.2 Negative- G_m Oscillators	38
4.4 10-GHz VCO Design	40
4.4.1 Effect of Supply Voltage Variation on VCO Tuning Range.....	44
4.4.2 Measurement Results	48
4.5 Summary	51
CHAPTER 5	52
Phase Detectors.....	52
5.1 Linear Phase Detectors.....	53
5.2 Binary Phase Detectors.....	55
5.3 Half-rate Linear Phase Detectors	57
5.4 Half-rate Binary Phase Detector.....	59
5.5 Summary	61

CHAPTER 6	63
Techniques to Improve the Phase Detector Performance	63
6.1 Hogge PD with Improved Flip-Flop	63
6.1.1 Circuit Design.....	63
6.1.2 Simulation Results and Comparison	67
6.2 Dual-Rate Linear PD	71
6.2.1 Half-Rate Linear PD Architecture.....	71
6.2.2 Proposed PD in a Full-Rate CDR Configuration	75
6.2.3 High-Frequency Circuit Design Techniques.....	77
6.2.4 Simulation Results for the Dual-Rate PD.....	78
6.3 Summary	81
CHAPTER 7	83
A Fully Integrated 10-Gb/s CMOS Clock and Data Recovery Circuit.....	83
7.1 CDR Architecture.....	84
7.2 Building Blocks.....	85
7.2.1 Phase Detector and Charge Pump	85
7.2.2 Integrated Loop Filter.....	88
7.2.3 10-GHz VCO.....	92
7.3 Jitter Analysis of the Designed CDR.....	93
7.3.1 Jitter Transfer Function	93
7.3.2 Jitter Generation	97
7.3.3 Jitter Tolerance	100
7.4 Measurement Results	102
7.5 Summary	108

CHAPTER 8	109
A Fully Integrated Half-Rate 10-Gb/s CDR	109
8.1 Half-Rate CDR Architecture	109
8.2 The Quadrature VCO with 5-GHz Operating Frequency.....	110
8.2.1 QVCO Measurement Results and Comparison.....	115
8.3 Half-Rate CDR Simulation and Measurement Results	117
8.4 Jitter Performance of the Half-Rate CDR	122
8.5 Summary	124
CHAPTER 9	125
Conclusion & Recommendations	125
9.1 Conclusion.....	125
9.2 Recommendations	127
BIBLIOGRAPHY	130
AUTHOR'S PUBLICATIONS	137

LIST OF FIGURES

Figure 2.1. A typical 10-Gb/s SONET receiver architecture.	10
Figure 2.2. NRZ and RZ data formats.....	12
Figure 2.3. The fastest 10-Gb/s data waveform in NRZ format.....	13
Figure 2.4. Optimum sampling point for a data signal.....	16
Figure 2.5. Jitter in a clock signal.....	16
Figure 2.6. Jitter transfer specification for the OC-192 standard.....	17
Figure 2.7. SONET mask for jitter tolerance requirement.	18
Figure 3.1. Simple PLL topology.	21
Figure 3.2. Charge-pump PLL architecture.....	23
Figure 3.3. The PFD, charge-pump, and simple loop filter combination.....	23
Figure 3.4. The output of the PFD with a charge-pump circuit [11].....	24
Figure 3.5. Linear model of the charge-pump PLL.....	25
Figure 3.6. Loop filter after the addition of the stabilizing resistor R_p and the ripple filtering C_{px}	27
Figure 4.1. Feedback oscillator.	32
Figure 4.2. (a) LC tank, (b) Series L-R connection, (c) Parallel L-R connection, (d) Parallel RLC tank.	36
Figure 4.3. (a) Negative resistance cross-coupled pair and (b) its small-signal equivalent.	38
Figure 4.4. (a) Basic cross-coupled LC oscillator, (b) A Cross-coupled voltage-controlled oscillator.	39
Figure 4.5. Complementary cross-coupled VCO.	40
Figure 4.6. Typical varactor characteristic.....	44

Figure 4.7. Varactor behaviour under two different supply voltages.....	45
Figure 4.8. Double-loop CDR architecture in [21].	46
Figure 4.9. Simulating the supply voltage reduction.....	47
Figure 4.10. Spectrum analyzer plot of the VCO output.....	48
Figure 4.11. Chip micrograph of the 10-GHz VCO.....	49
Figure 4.12. VCO tuning range for different supply voltages.....	49
Figure 5.1. Hogge phase detector and its waveforms.....	53
Figure 5.2. PD waveforms in phase-locked condition.	54
Figure 5.3. Alexander PD and its waveforms for the two cases.....	56
Figure 5.4. Half-rate linear PD with its waveforms [22].....	58
Figure 5.5. (a) A half-rate binary PD, (b) A DETFF sampling the <i>Data</i> by <i>CLK</i> , (c) S_0 samples discarded for late and early <i>CLK</i> , (d) Detecting the absence of data transition [23].	60
Figure 6.1. Hogge PD block diagram.....	64
Figure 6.2. Conventional current-steering DFF core.....	65
Figure 6.3. Modified DFF for high-speed Hogge PD.	66
Figure 6.4. Dynamic XOR gate.....	67
Figure 6.5. The waveforms for the Hogge PD with conventional DFFs.....	68
Figure 6.6. The waveforms for the Hogge PD with fast DFFs.	69
Figure 6.7. Net phase difference vs. time for the two PDs.....	70
Figure 6.8. Double-edge-triggered D-flip-flop (DETFF).....	72
Figure 6.9. Failure of half-rate PD with single-phase clock signals.	73
Figure 6.10. Proposed half-rate PD architecture and its timing diagram.	74
Figure 6.11. The PD and its waveforms in a full-rate CDR configuration.	76
Figure 6.12. 2:1 Multiplexer.....	78

Figure 6.13. PD output for 10-Gb/s random data after pre-layout simulation.	79
Figure 6.14. PD output for 10-Gb/s random data after post-layout simulation.....	79
Figure 6.15. Layout of the proposed PD.	81
Figure 7.1. Typical CDR architecture.	84
Figure 7.2. Hogge PD with fast DFF.....	85
Figure 7.3. The recovered data for a typical 10-Gb/s input.....	86
Figure 7.4. Charge pump circuit.....	87
Figure 7.5. Loop filter, type-II 2 nd -order.	89
Figure 7.6. Integrated loop filter.....	89
Figure 7.7. Linear model of the CDR.....	90
Figure 7.8. Locking characteristics of the loop.	92
Figure 7.9. The recovered clock output at 10 GHz.	93
Figure 7.10. Magnitude of the transfer function response.....	96
Figure 7.11. Zoom to jitter peaking region of the transfer characteristics.	96
Figure 7.12. The position of the clock and data edges (a) optical sampling point (no jitter) and (b) with jittered data input.....	100
Figure 7.13. Calculated jitter tolerance and SONET mask.	102
Figure 7.14. Full-rate integrated CDR micrograph.	103
Figure 7.15. The probing station for measurements.....	106
Figure 7.16. Measured phase noise of the full-rate CDR.	106
Figure 8.1. Half-rate CDR architecture.	109
Figure 8.2. Quadrature VCO for 5-GHz clock signal generation.....	111
Figure 8.3. QVCO layout.	113
Figure 8.4. QVCO outputs.	113
Figure 8.5. QVCO simulated phase noise.	114

Figure 8.6. QVCO chip photograph.	115
Figure 8.7. QVCO measured phase noise.	116
Figure 8.8. Half-rate CDR chip photograph.....	117
Figure 8.9. Locking characteristics of the loop.	118
Figure 8.10. The 10-Gb/s recovered data output from the half-rate PD.....	119
Figure 8.11. Half-rate CDR recovered clock simulated phase noise.	120
Figure 8.12. Half-rate CDR recovered clock measured phase noise.....	121
Figure 8.13. Half-rate CDR recovered clock spectrum at 5 GHz.	121

LIST OF TABLES

Table 4.1. The effect of parasitics on the VCO design.	43
Table 4.2. Performance comparison of the fabricated VCO with the existing designs.	50
Table 6.1. Comparison of existing designs with the proposed PD.....	80
Table 7.1. Calculated jitter tolerance vs. SONET mask requirements.....	101
Table 7.2. Summary and comparison of the CDR performances.....	107
Table 8.1. QVCO device parameters.....	112
Table 8.2. Simulated QVCO performance and comparison.....	116
Table 8.3. CDR comparison with the existing designs.	123

CHAPTER 1

Introduction

1.1 Motivation

The continuous increase of the data transport over the Internet has boosted the demand for high-speed communication networks in order to accommodate the bandwidth requirement that is doubling every 12 months [1]. To facilitate the high-bandwidth data transfer, the standards for 2.5-Gb/s to 10-Gb/s serial links have been addressed and the next generation of optical networks such as 40-Gb/s systems is being explored [2]. High-speed data signals are transferred through optical fibers that offer the highest bandwidth and the lowest loss when compared to the other media such as copper wire and coaxial cables. At the end of these long transmission lines is the *optoelectronic* transceiver circuit that either regenerates the data signal and forwards it to the next optical fiber node or processes the data for the end user. After the data carrying light, which travels over the optical fiber, is converted to electric signals by a photodiode circuit, the rest of the data processing is done in the electronic section of the transceiver. Unfortunately, the bandwidth and the speed of the solid-state devices are much lower than the optical section and hence the electronic interface has been the bottleneck in designing high-speed optical systems [2].

The majority of the backbone optical communication systems are based on the synchronous optical network (SONET) standard [3]. Based on the integer multiples of 51.85 Mb/s, SONET defines a hierarchy that allows different data rates to be multiplexed. As a result of this classification the *SONET OC-192* standard has been

specified for *10-Gb/s* optical communication. OC-192 has the capability of connecting lower data rate ring networks and hence drastically reducing the complexity of the network. Video conferencing and asynchronous transfer mode (ATM)-based services such as local area network (LAN) connections are among the other services that can be provided using OC-192 systems.

The most critical block in an optical receiver unit is the clock and data recovery (CDR) circuit. As a result of the above-mentioned bandwidth-speed challenges and the additional issues related to the nonreturn-to-zero (NRZ) data format employed in the optical transceivers, the design of the CDR has been one of the most challenging parts of the overall system design. In an optoelectronic receiver, the CDR circuit is required to extract the clock signal from the incoming random data stream in NRZ format that is corrupted by noise and interference due to the physical medium and the circuit components.

PLL-based CDRs provide superior performance compared to their inductor-capacitor (LC) and surface acoustic wave (SAW) resonator counterparts since they provide clock signal extraction in the absence of spectral component at the baud rate, and the wide range of frequency tuning makes the PLL a flexible choice in terms of process and temperature variations [4]. Although most of the building blocks of a PLL-based CDR can be integrated on a single chip, the large passive components still remain as exceptions and hence the obstacles for a fully integrated CDR implementation.

The first generation OC-192 systems, which were released to the market in the 90s, relied exclusively on GaAs-based technologies that had low level of integration but

provided high performance in combination with the discrete components. The transistor speed of these technologies with typical f_T and f_{MAX} values of 60-70 GHz were superior when compared to the silicon-based processes at that time.

Recently, significant improvement has been reported in the silicon technologies. Several foundries have announced SiGe HBT f_T and f_{MAX} values higher than 70 GHz over the last three years [5], [6]. These processes offer very fast bipolar transistors for the analog portion and submicron level CMOS devices for the digital circuits. The number of fabrication masks for the BiCMOS process is higher than that of a CMOS process. Furthermore, the digital circuits fabricated using these BiCMOS processes cannot operate as fast as those that are fabricated in a standard CMOS process [3]. A small number of foundries offering BiCMOS process add to its shortcomings and forces the system-on-chip designers to look for an alternative to this rather costly technology.

Aggressive scaling in device dimensions has improved the speed of MOSFETs and resulted in the production of NMOS transistors in the 0.15- μm and 0.13- μm generations with f_T values approaching 80 GHz. It is predicted that f_T will exceed 120 GHz for 0.1- μm devices. Lower fabrication cost, high yield, and higher level of integration make CMOS technologies more cost-efficient than their SiGe and GaAs counterparts. Additional features like supply voltage scalability and availability of multiple metal layers for the implementation of high-quality passive devices strengthen their positions in the market and provide the capability of integrating the analog and the digital sections on the same chip. Such integration reduces the number of packages and decreases the circuit board area.

The lack of accurate device models in CMOS technologies for exceptionally high operation frequencies such as 10 GHz is another challenge that the CDR designers are facing.

1.2 Objectives

This research is focused on the design of the fully integrated low-voltage low-power *clock and data recovery* circuits in CMOS technology along with the investigation of new circuit techniques and system-level solutions that can improve the performance of the optical transceivers. The CDR designs target the 10-Gb/s SONET OC-192 standard that has found a wide application area with the increase in the Internet traffic throughout the world.

The possible modifications for each building block of the CDR unit are to be determined in order to address the high-frequency design challenges. Achieving low power consumption is another matter of concern as it has a direct impact on the packaging. A complete transceiver with all the vital building blocks can easily consume 1 to 2 W of power. Therefore, apart from bringing this figure down, the power consumption of the CDR should be kept as low as possible so as not to exceed the power budget.

1.3 Major Contributions of the Thesis

In this research, two CDR units are designed for SONET OC-192 10-Gb/s data rate application. The circuits are implemented in Chartered Semiconductor Manufacturing Foundry's 0.18- μm CMOS process and tested using a probing station that is capable of

on-wafer measurements. Each circuit incorporates unique high-frequency design techniques and system-level novelties.

One of the CDRs is a full-rate design with an emphasis on its fully integrated feature that comes as a result of a modification done in the loop filter block. The circuit phase noise is -112.7 dBc/Hz at 1-MHz offset, leading to low jitter and good jitter tolerance performance. The analytically calculated jitter generation is less than 0.1 ps-rms (root-mean-square) and the jitter tolerance mask is satisfied with a wide margin (0.72 UI at 4-MHz jitter frequency). The active chip area is $560 \mu\text{m} \times 780 \mu\text{m}$. The power consumption of this design is less than 55 mW excluding the output buffers (70 mW with buffers). With such small size and low power consumption, this circuit is a feasible alternative to the expensive GaAs and SiGe counterparts that are currently in the market.

It is not always wise to push for the marginal limits of the process when the system specifications and the requirements of the standards are stringent, and when there is limited space for trade-off. Therefore, the half-rate architecture and its advantages are investigated in the second CDR design. The crucial block in a half-rate design is the half-rate phase detector (PD) that is operating with full-rate data signal (10 Gb/s) and a half-rate clock signal (5 GHz). Unlike application-specific half-rate PDs reported so far, we have introduced a dual-rate PD that can be employed in both full-rate and half-rate CDR architectures. The simulated performance of the PD exhibits reasonable power consumption of 30 mW from a 1.8-V supply and a small chip area of $130 \mu\text{m} \times 160 \mu\text{m}$.

A close look to the PLL analysis and a new loop filter topology are among the major achievements in this research as well. The improved loop filter employed in our CDR designs occupies a remarkably small chip area because the filter capacitance is in the range of 10 to 20 pF and it does not require external components. The impact of using this filter topology on the loop dynamics and the jitter performance are also demonstrated as part of this research.

The effects of reducing the bias voltage of the VCO on the voltage gain and the tuning range of the VCO are determined. By reducing the supply voltage from the nominal 1.8 V to 1.5 V, the VCO gain can be brought down to 300 MHz/V from 2.2 GHz/V. Lower gain will result in fewer ripples on the control voltage of the VCO. This finding leads us to the possibility of merging the frequency locking aid with the data recovery core of the CDR. The findings of this particular research is crucial not only for the jitter performance of the CDR unit but also for the system designers who aim to simplify the process of the frequency acquisition and the data recovery without jeopardizing the system performance.

1.4 Organization of the Thesis

Chapter 1 provides an introduction to the SONET systems, the basic concepts about the design of high-speed clock and data recovery circuits, and an outline of the thesis.

Chapter 2 gives the background on the optical receiver system. It further elaborates on the random data types and compares the open-loop and the closed-loop CDR systems. The jitter requirements of the OC-192 standard are given in conjunction with the

definitions of the important system parameters such as the jitter transfer, jitter generation, and the jitter tolerance.

Chapter 3 takes a closer look at the PLL design since the CDR performance totally relies on that of the PLL. Fundamental loop equations are summarized and their implications on the CDR designs are discussed. As we will refer to these topics throughout the thesis, the main parameters of the PLLs, such as the stability, natural frequency, and the damping factor are described. Subsequently, the locking behaviour of the PLLs and the definitions of the capture range and tracking range are briefly discussed.

In Chapter 4, after a brief description of the oscillator circuits and different types of oscillators, circuit design techniques are introduced for a 10-GHz VCO. This VCO is to be used with the rest of the building blocks in a CDR implementation, therefore, a prototype has been fabricated and the measurement results are presented in this chapter. The effect of the supply voltage scaling on the tuning range of the VCO is investigated and its impact on a possible CDR application is further analyzed.

Chapter 5 presents a literature review of the popular phase detector designs. The pros and cons of each topology and the design challenges associated with them are also elaborated. It is important to have low jitter and high-speed PDs for the SONET OC-192 applications. Based on the comparison; the suitable topologies to satisfy the jitter requirements of the overall CDR unit are selected among the available PD designs.

In Chapter 6, we describe our proposed techniques to improve the performance of the phase detectors in OC-192 applications. While the first proposal tackles the issues related to full-rate PDs at the circuit level, the second technique introduces an architectural solution to the half-rate PD implementations. The dual-rate operation capability is also investigated.

Chapter 7 presents the full-rate CDR design targeting the OC-192 applications. The impact of the modifications and the improvements in both circuit topology and system architecture is illustrated throughout the chapter. A new loop filter topology is also highlighted in this chapter. The compact size of this filter facilitates the realization of the fully integrated CDR system. The jitter performance of the CDR is analyzed and it is shown that the jitter requirements are satisfied with safe margins.

Chapter 8 revisits the half-rate PD design and describes a half-rate CDR system that incorporates this PD circuit. The advantages of employing half-rate architecture in some applications are highlighted. Additional to the above-mentioned circuits, the design of a quadrature VCO is described. Since this VCO provides the clock signal to the half-rate PD, its operation frequency and phase noise performance are investigated. The simulation and measurement results are presented for the quadrature VCO and the overall CDR design.

Chapter 9 wraps up the thesis with conclusion and recommendations that could help the designers in their pursuit for improved CDR designs in the future.

CHAPTER 2

Background

2.1 Overview of an Optical Receiver System

Optical communication (OC) systems are designed to address the challenge of carrying large volumes of data across long distance with minimum loss. Optical fibers exhibit the highest bandwidth compared to various transmission media such as copper and coaxial cable and hence they are capable of transmitting high-speed data over long distance with minimum cost. However, the data signal still experiences distortion as it travels through the fiber, mostly due to the fiber dispersion [3]. This distortion further degrades the data *eye opening* by introducing intersymbol interference (ISI) and reduces the signal amplitude.

In order to maintain the communication between the transmitter and the end-user amid the noise and fiber loss, extensive research has been carried out to provide an efficient solution in the optical domain. New approaches that are advocating the *all-optical* data recovery have yet to address the optical limitations so that these solutions can be implemented down to the end-user level [1]. Until then, we will continue to rely on the special blocks called *repeaters* to restore the distorted signal in the optical fiber. Repeaters are the electrical interfaces between two optical fiber networks that first convert the laser modulated optical pulses into electrical current, perform clock signal extraction and data recovery, convert this *regenerated* data signal into optical pulses, and finally, forward it to the next optical fiber.

A similar electronic interface can be employed at the receiver end as well. Instead of forwarding the recovered data to the optical network, the end-user interface processes it at the subsequent electrical blocks. As the electronic interface is the only means to ensure that the long distance data transmission has a low bit-error-rate (BER), its signal-to-noise ratio (SNR) must be sufficiently high.

A typical SONET OC-192 receiver architecture is shown in Fig. 2.1 [7]. It employs a photodiode to detect and convert the incoming high-speed optical pulses of a single channel into electrical current pulses. A low-noise high-bandwidth transimpedance amplifier (TIA) converts these pulses into a voltage value and a low-pass filter gets rid of the high-frequency noise components in the data stream. In general the TIA-Filter output voltage swing is not high enough to operate the succeeding blocks. Therefore, an automatic gain control (AGC) amplifier provides additional amplification and compensates for the variations in the signal power.

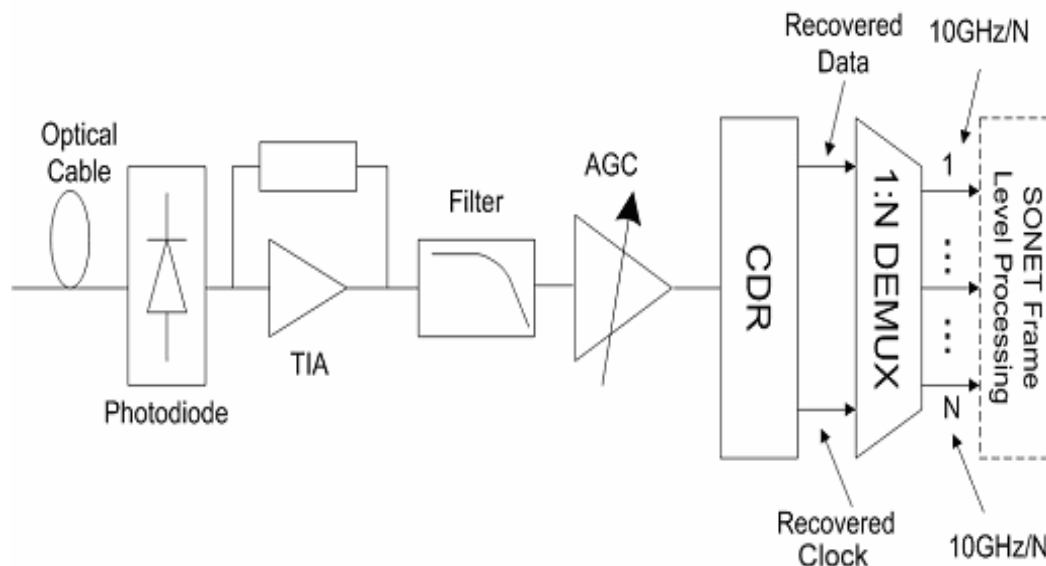


Figure 2.1. A typical 10-Gb/s SONET receiver architecture.

In order to maintain the synchronization between the transmitter and the receiver, the data signal should be recovered using the same clock signal. This operation is performed in the clock and data recovery block. Upon acquiring lock to the exact clock signal, the distorted data is recovered and passed to the demultiplexer (DEMUX) for further data processing in an environment that is running at a frequency lower than that of the original clock signal. Typical DEMUX ratios are 1:4, 1:8, and 1:16, depending on the lower speed channel configurations.

2.2 Properties of Random Data Formats

In a baseband communication system, the original analog waveform is sampled using *natural sampling* to obtain the *pulse amplitude modulation* (PAM) data where the amplitude of the samples follow the original data. In order to make these samples suitable for transmission through a digital system, they are quantized and encoded into a digital word. This procedure is called *pulse code modulation* (PCM). The digital word is a set of binary digits that needs to be converted into electrical pulses so as to transmit them through a communication channel. Since the data signal travels a long distance over the communication media, it will be distorted.

On the other hand, the receiver has to detect if there is a pulse at a given time slot or not with minimum error. It can be shown that the likelihood of detecting a pulse correctly is directly proportional to the pulse width as the pulse width represents its energy, i.e., the wider the pulse, the higher the pulse energy and hence the better detection capability for the receiver [8].

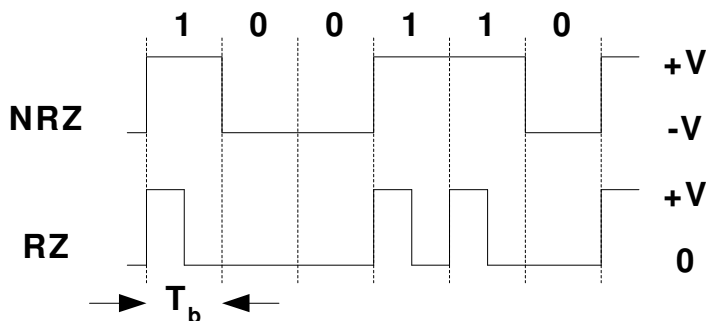


Figure 2.2. NRZ and RZ data formats

Of the four major groups of data formats (Nonreturn-to-Zero (NRZ), Return-to-Zero (RZ), Phase Encoded, and Multilevel Binary), NRZ format is the choice in high-speed optical communication applications to maximize the data rate within a given channel bandwidth when compared to RZ type. Fig. 2.2 shows an example of the two data formats. For NRZ data, each bit has duration of T_b (i.e., bit period) corresponds to a bit rate of $r_b = \frac{1}{T_b}$; whereas in RZ data format the signal reaches zero between consecutive bits and it is possible to treat the RZ as an NRZ data sequence with a bit rate of $1/(2T_b)$. This RZ data requires twice the bandwidth of NRZ data to transmit the same bit sequence. Therefore, RZ data is not commonly used in optical communication systems where the efficient use of bandwidth for high-volume data traffic over the optical fiber is the primary concern. Furthermore, the NRZ format surpasses the other formats for its simplicity, ease of detection, and resistance to negative effects of the noise.

More complex multilevel data formats are not suitable for high bit rate optical communications because they impose stringent constraints on the laser source driver circuit to achieve the desired modulation and satisfy the jitter requirements [9]-[12].

Unfortunately, not all the features of the NRZ format ease the circuit designers' burden:

The NRZ signal may *apparently* stop transition from logic '1' to '0' or vice versa when there are long consecutive '1's or '0's. These are the most challenging periods for the CDR unit during the transmission where it must maintain the operation frequency and it should not be carried away by the frequency-drifting effects such as the charge leakage at the passive components and the parasitics.

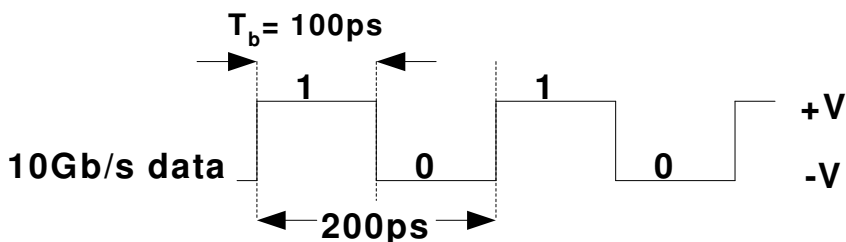


Figure 2.3. The fastest 10-Gb/s data waveform in NRZ format.

Another interesting phenomenon that significantly influences the choice of the CDR architecture and its performance is that the NRZ signal does not have a frequency component at its bit-rate equivalent.

As shown in Fig. 2.3, at its highest data transition rate, which is formed by consecutive 'one's and 'zero's, a 10-Gb/s signal has 100-ps bit duration for each bit (remember the definition of bit rate: $r_b = 1/T_b$). Therefore, this sequence has a period of 200ps , which is equivalent to a 5-GHz signal. Extracting the clock frequency of 10 GHz from a 5-GHz random data signal is not straightforward and requires nonlinear operations in the CDR unit.

2.3 Open-Loop and Closed-Loop CDRs

The basic communication system applications have demonstrated that the existence of a spectral component in a received signal makes it possible to extract the clock signal by simply passing the signal through a bandpass filter [8]. Depending on the required sharpness of the filter response, i.e., the filter quality factor (Q), the filter can be implemented using an LC resonator tank or a SAW structure.

While LC or SAW-based open-loop CDR circuits offer fast acquisition and low jitter in the recovered clock, they operate at a fixed frequency and provide no output in the absence of data transitions. This is particularly problematic in the case of consecutive identical digits. The CDR circuit assumes that the data flow has stopped and it ceases the process of clock and data recovery, resulting in the drifting of the recovered clock.

The lack of the spectral component at the clock frequency, which is the case in SONET systems that operate with the NRZ data format, is another matter of concern because the optical receiver must perform some nonlinear operation before the SAW or the LC resonator can take charge of the data recovery. Furthermore, these open-loop systems cannot make use of any feedback to adjust their outputs when there are temperature, process, and supply variations [13]. The manual tuning of the long sequence of repeaters to compensate for these variations and the inherent -but unknown- group delay of the system [14] will not be practical, if not impossible. Another drawback is that neither LC nor SAW-based CDR circuits are practically realizable in monolithic form due to their bulky size and technology constraints that limit the implementation of high- Q on-chip passive devices [4].

Contrary to the fixed-frequency open-loop systems, the PLL-based closed-loop architectures provide superior performance for the clock and data recovery. They provide comparatively wide tuning range. They are capable of extracting -and maintaining lock onto- the clock signal in the absence of input data transitions and can be easily integrated on a chip. The wide tuning range of the VCO can also compensate for the frequency drifts that are caused by the process and temperature variations. Unfortunately, since the loop bandwidth of the PLL-based CDR is small, the frequency acquisition can take longer time than the open loop systems. Nevertheless, the recovery time, in general, is not a big concern for the CDR systems and it remains within the specified limits.

2.4 System Parameters

2.4.1 Jitter Definitions

Asynchronous networks may communicate with each other using different data rates and clock frequencies at the expense of some data loss or extra buffering activity. On the other hand, being a synchronous system, the SONET OC-192 applications are highly sensitive to the timing issues and they cannot tolerate a frequency discrepancy between the transmitter and the receiver. Moreover, the amount of the phase difference is equally important since the data signals must be sampled at the mid point of each bit in order to satisfy the optimum sampling condition with minimum probability of error (Fig. 2.4). The digital communication standards specify certain limits to these phase differences in the circuits and this is where the concept of jitter comes into the picture. Although one can list several definitions of it [9], *jitter* can simply be defined as the abrupt and unwanted variations in the timings of the signal transitions.

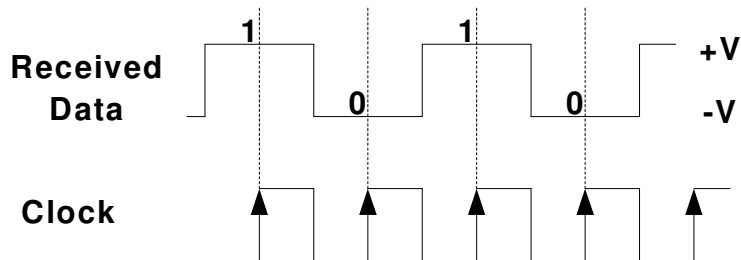


Figure 2.4. Optimum sampling point for a data signal

Jitter plays a key role in determining the CDR performance. It can be expressed in terms of either *unit intervals (UI)*, where one cycle of the clock signal is one unit interval (1UI=1-bit period); or *absolute time* in picoseconds. As shown in Fig. 2.5, the variations in the zero crossings of the clock signal can degrade the intersymbol interference performance of the system and lead to detection errors.

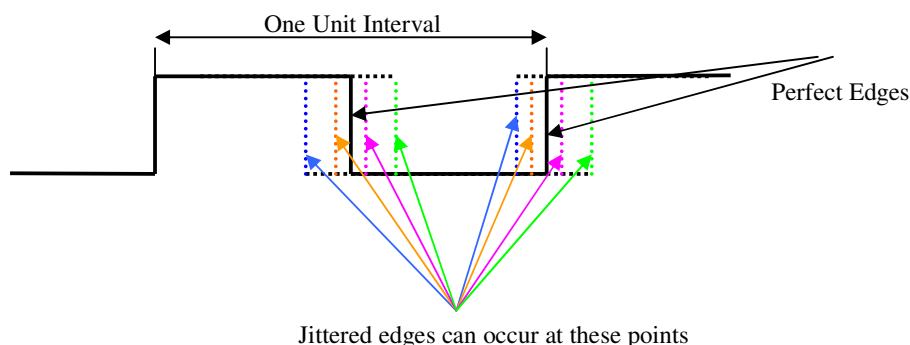


Figure 2.5. Jitter in a clock signal.

2.4.2 Jitter Specifications for the OC-192 CDR

The CDR jitter characteristics that are critical to SONET optical receiver design are *Jitter Generation, Jitter Transfer, and Jitter Tolerance*.

The *jitter generation* is the process whereby jitter appears at the output port of a digital equipment in the absence of an applied jitter at the input [10]. This jitter is produced by the sub-blocks of the CDR. The jitter generation is limited to 10 ps_{p-p} (peak-to-peak) or 1 ps-rms for 10-Gb/s applications.

The *jitter transfer* is the relationship between the jitter that is applied to the input port and the jitter appearing at the output port. It has two components: *jitter peaking* and *jitter bandwidth* [10]. Jitter transfer requirement for the OC-192 is shown in Fig. 2.6. The jitter bandwidth and the jitter peaking should be less than 120 kHz and ± 0.1 dB, respectively.

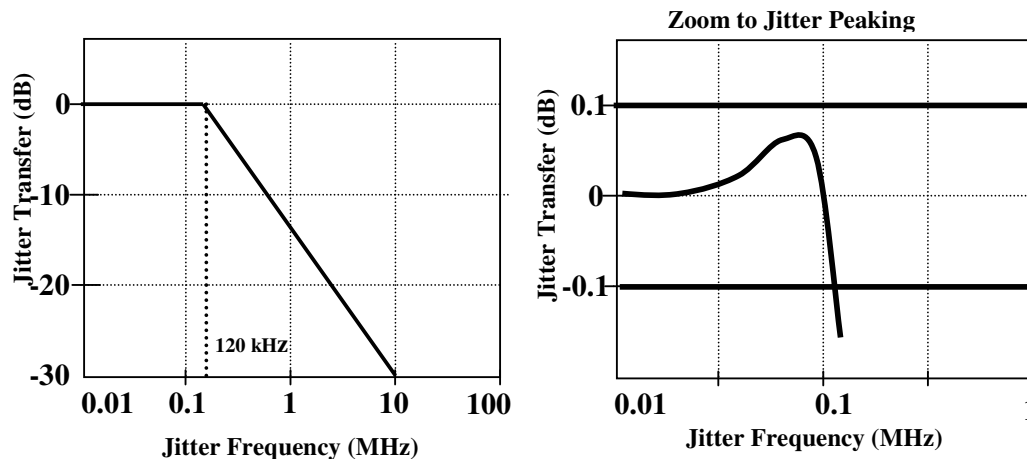


Figure 2.6. Jitter transfer specification for the OC-192 standard.

There seems to be some kind of conflicting requirements between the jitter generation and the jitter transfer specifications. Achieving a low jitter generation with a jitter bandwidth of 120 kHz is very difficult. The small bandwidth does not ease the burden of the CDR unit in removing the out-of-band noise above 120 kHz, and the CDR design is further complicated to minimize the noise generated by the internal blocks. Additionally, the jitter peaking requirement demands careful attention to the poles and zeros of the system [11]. In fact, the narrow bandwidth requirement can only be justified for long series of repeaters that are cascaded to each other. The jitter generated by a single block will be added to the succeeding blocks; therefore, if the jitter bandwidth does not remain below the specified value, the jitter will be accumulated through the chain of the repeaters. These repeaters are the reason for the low jitter peaking requirement as well: The above-mentioned peaking specification is

enforced to keep the contribution of each block so low that the contribution of the overall peaking remains at the minimum level.

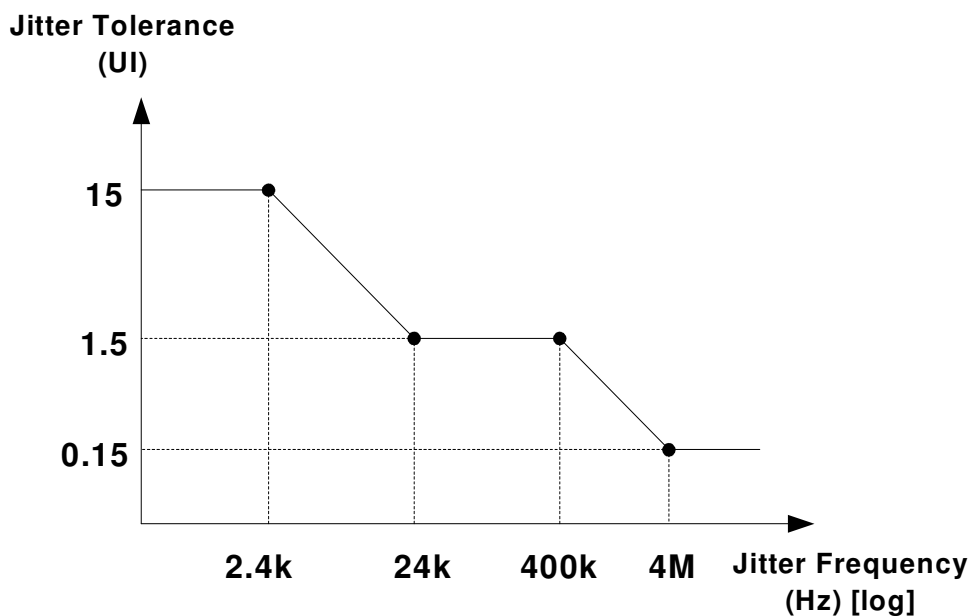


Figure 2.7. SONET mask for jitter tolerance requirement.

The *jitter tolerance* is the ability of the CDR unit to retrieve the data and retime it when the signal is highly jittered. The tolerance value is measured as the maximum amplitude of the peak-to-peak sinusoidal jitter at a given jitter frequency that results in a 1-dB power penalty at the output. During the measurement, the signal at the input port is modulated with a sinusoidal signal to produce jitter at different frequencies.

Requirements on the input jitter tolerance are specified in terms of compliance with a jitter mask that represents a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency that results in a 1-dB power penalty when the input signal is modulated [12]. Fig. 2.7 shows the jitter tolerance mask defined by Bellcore for OC-192. A CDR device under test must exhibit

a jitter tolerance characteristic such that its jitter tolerance plot will stay above this SONET mask.

2.5 Summary

In this chapter, a brief overview of the optical receiver system, major data formats that are used for the optical fiber communication, and the SONET requirements that are to be satisfied in order to achieve a successful CDR design are presented.

The definition and the importance of the various parameters are also discussed. It should be noted that one cannot play with only one parameter to excel his design since all of them are linked to each other in many ways. In fact, it is a matter of trade-off or compromise to achieve a certain level of satisfactory results. The fundamentals of the PLL systems and their impact on the CDR design will be discussed in the following chapters.

CHAPTER 3

PLL Fundamentals

Throughout this thesis, we will focus on the closed-loop CDR structures, and certain terms such as loop gain and loop bandwidth will be occasionally used; therefore, a brief overview of the PLLs is essential.

The PLLs have been widely used in areas such as communications, digital systems, microprocessor applications, wireless systems, and disk drive control circuits. With the advent of the submicron silicon technologies in the last 15 years, most of the building blocks of a PLL can be integrated into a single chip, something that was not possible when the first examples of the PLLs emerged in 1930s. Although the operation principles of the PLLs are well documented and are more or less the same since the invention of its concept, different applications focus on different aspects of a PLL circuit and demand certain parameters to be satisfied, posing a variety of challenges to the designers. For example, both the clock recovery circuit of an optical receiver and the frequency synthesizer of a mobile phone employ PLLs, but the design of the building blocks of each PLL and the required experience are significantly different.

In this chapter the fundamental concepts about the PLL systems and their impact on the CDR design will be discussed. Since the scope here is the operation of the overall system, the description of the building blocks here will be concise and mostly from the system designer's point of view. The detailed descriptions will be given in the subsequent chapters. It should be noted that although the clock and data recovery

systems deal with random input signals; for simplicity, we make the assumption that the input signals to the PLL are periodic for the most part of this chapter.

3.1 What is a PLL?

A phase-locked loop is basically a nonlinear feedback system that compares the input phase with the output phase [11]. At the core of the PLL is the phase detector along with the VCO. The PD compares the phases of the input signal and that of the VCO and provides an output V_{CTRL} , indicating that the VCO should increase or decrease its oscillation frequency in order to acquire -or maintain- the lock in the system. V_{CTRL} is adversely affected by the switching activity in the PD. In order to circumvent this problem, a loop filter is added between the PD and the VCO, completing the simple PLL structure as shown in Fig. 3.1. ϕ_{IN} and ϕ_{OUT} here denote the total phases of the input and output, respectively.

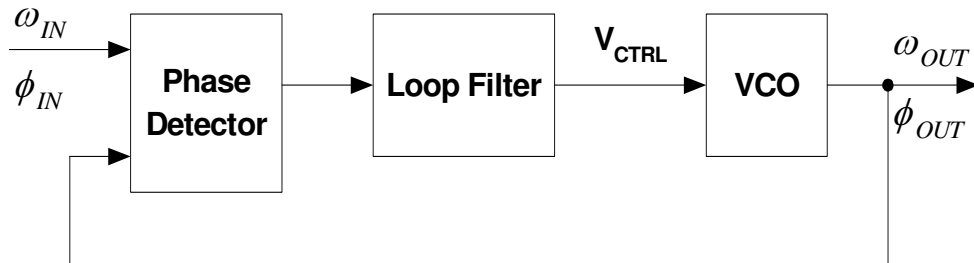


Figure 3.1. Simple PLL topology.

The operation of the PLL is based on the well-known phase-frequency relationships:

$$\omega(t) = \frac{d\phi}{dt} \quad (3.1)$$

and

$$\phi(t) = \phi(0) + \int \omega \cdot dt \quad (3.2)$$

where $\omega(t)$ and $\phi(t)$ represent the radian frequency -expressed in rad/s- and the phase, respectively. $\phi(0)$ is the initial phase and it will be ignored for the rest of the analysis for the sake of simplicity.

3.2 Charge-Pump PLLs and the Transfer Function

Conventional Type-I PLLs have been the early examples of the synchronization circuits [15]. Because of their limitations, they hardly find way to the integrated circuit applications. Fortunately, addition of a charge-pump circuit to the simple PLL structure proves very useful in monolithic implementations such as that of a CDR. The charge-pump, which will be described in detail in the subsequent chapters, is a switching circuit that pumps current to the loop filter or draws current from the filter according to the information provided by the phase detector.

The charge-pump variant of the PLL has initially targeted the applications where frequency acquisition is the crucial performance parameter of the system, such as the frequency synthesizers that are used in the mobile/cellular communication transceivers. As its features provide significant flexibility in the system design, the charge-pump PLL is widely used in the optical communication nowadays.

A charge-pump PLL can be constructed as shown in Fig. 3.2. The PFD block produces Up (UP) and Down (DN) signals according to its periodic inputs CK1 and CK2. The UP denotes the case when the CK1 is leading CK2 or CK1 is faster than CK2. The DN case is the opposite of this situation. When the two inputs are equal in phase and frequency, both outputs go to logic '0' indicating a 'neutral' (N) state. The PFD block

is designed such that the two outputs can never give logic '1' output at the same time [11], [16], and [17]. These features result in the name, *three-state PFD*, i.e., UP, DN, and N states.

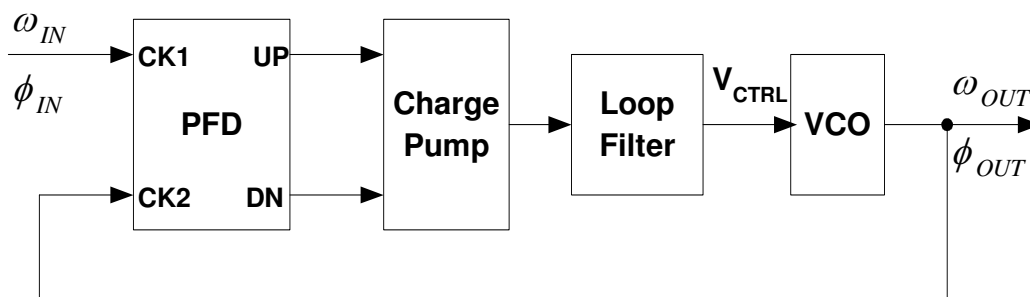


Figure 3.2. Charge-pump PLL architecture.

The digital outputs of the PFD block are translated into a current value in the charge pump and passed through the loop filter to obtain the control voltage that is necessary to tune the VCO circuit to acquire the phase/frequency lock.

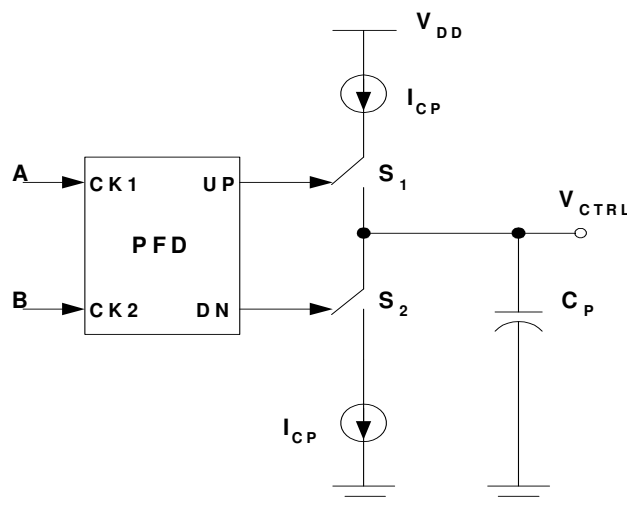


Figure 3.3. The PFD, charge-pump, and simple loop filter combination.

The combination of the PFD and the CP along with a simple loop filter is shown in Fig. 3.3. The switch S_1 closes when the PFD indicates 'UP' and S_2 closes when PFD output is 'DN'. They control the current flow into or out of the loop filter. The

capacitor C_P is employed to filter out the ripples that are produced by the switches in the charge pump and the logic gates in the PFD from the output V_{CTRL} . The output waveforms are depicted in Fig. 3.4.

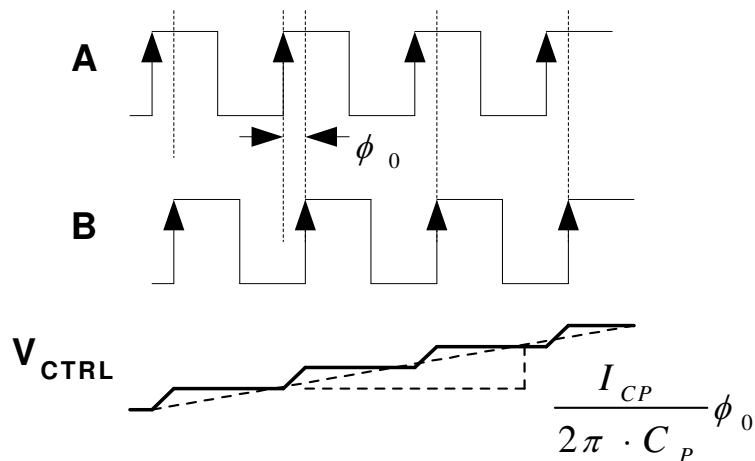


Figure 3.4. The output of the PFD with a charge-pump circuit [11].

Due to the switching activity, the charge-pump PLL exhibits discrete time behaviour and hence the loop does not obey the linear, time-invariant network principles in the strict sense. In general, the principles of the simple transfer function analysis cannot be applied to this nonlinear time-varying system. Fortunately, in many applications, including the CDRs, the loop bandwidth is much smaller than the input signal frequency and hence the discrete intervals exhibit very small changes in one input cycle, and the system can then be assumed to be continuous when averaged over many cycles [17].

The configuration in Fig.3.3 is used to derive the transfer function of the PFD-CP-LPF combination. The phase error is represented by the average error current in s-domain

$$I_d(s) = I_{CP} \cdot \frac{\phi_0(s)}{2\pi} \quad (3.3)$$

from which we can approximate the voltage appearing at the loop filter output to be

$$V_{CTRL}(s) = I_d(s) \cdot Z_{LPF}(s) = \frac{I_{CP}}{2\pi \cdot s C_P} \cdot \phi_0(s) \quad (3.4)$$

The transfer function will then be

$$\frac{V_{CTRL}(s)}{\phi_0(s)} = \frac{I_{CP}}{2\pi \cdot C_P} \cdot \frac{1}{s} \quad (3.5)$$

Based on the foregoing analysis and assumptions, we are ready to construct a linear model of the charge-pump PLL and complete the analysis of the system (Fig. 3.5). The VCO is modeled here as the integrator; recall from (3.2) that the phase can be represented as the integration of the frequency. K_{VCO} -expressed in rad/s/V- is the oscillator gain. We should note that when the loop is not locked, the nonlinear effects make it impossible to derive a transfer function. Therefore, the transfer functions are valid only for the case when the loop is locked.

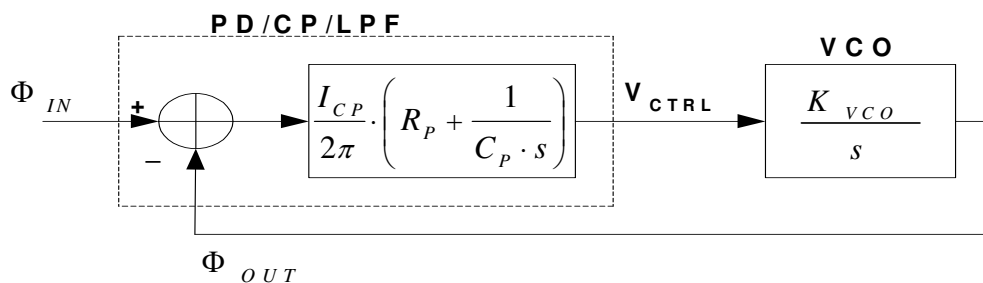


Figure 3.5. Linear model of the charge-pump PLL.

Furthermore, the simple loop filter needs some modification so as to stabilize the loop. It is obvious from (3.5) that when the PFD/CP/LPF block is combined with a VCO, the open-loop transfer function will have two poles at the origin, resulting in two imaginary poles for the closed-loop transfer function [11] and hence the stability problem. A series resistor is added to the filter capacitor to introduce a ‘zero’ to the

transfer function in order to minimize the risk of the unwanted oscillations. With the addition of a zero, the $Z(s)$ in (3.4) will be

$$Z(s) = R_p + \frac{1}{C_p \cdot s} \quad (3.6)$$

Similar to a Type-I PLL, the gain of the feedback path is equal to unity and hence the finalized open-loop transfer function is

$$\frac{\Phi_{OUT}}{\Phi_{IN}}(s)|_{OPEN} = \frac{I_{CP}}{2\pi} \left(R_p + \frac{1}{C_p \cdot s} \right) \cdot \frac{K_{VCO}}{s} \quad (3.7)$$

The uncompensated loop gain has one more pole than that of the Type-I PLL; therefore, this topology is called Type-II PLL for the double poles at the origin. The calculation of the closed-loop function is straightforward:

$$H(s) = \frac{\Phi_{OUT}}{\Phi_{IN}}(s)|_{CLOSED} = \frac{\frac{I_{CP}}{2\pi} \cdot K_{VCO} \cdot \left(\frac{R_p \cdot C_p \cdot s + 1}{C_p} \right)}{s^2 + \left(\frac{I_P}{2\pi} \cdot K_{VCO} \cdot R_p \right) \cdot s + \frac{I_P}{2\pi \cdot C_p} \cdot K_{VCO}} \quad (3.8)$$

Using the control theory notation $H(s) = \frac{\omega_n^2}{s^2 + 2\zeta \cdot \omega_n \cdot s + \omega_n^2}$, we can derive the natural frequency ω_n and the damping factor ζ as

$$\omega_n = \sqrt{\frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot C_p}} \quad (3.9)$$

and

$$\zeta = \frac{R_p}{2} \cdot \sqrt{\frac{I_{CP}}{2\pi} \cdot K_{VCO} \cdot C_p} \quad (3.10)$$

respectively.

The modification of the loop filter to curb the stability problem comes with a price of increased ripples that usually prove unacceptable for many applications. When the CP pumps a current of I_{CP} into the loop filter, the resistor R_P will generate a voltage jump of $\Delta V_{CP} = I_{CP} \cdot R_P$, which will then charge the filter capacitor. After the charge pump activity is over, the capacitor will be discharged over the VCO control line. The ripples can degrade the spectrum purity of the VCO output and result in jitter in the system. Additional filtering is required in such cases; therefore, another capacitor is connected in parallel to the series resistor-capacitor pair. In order not to disturb the loop dynamics, the 2nd capacitor size is chosen about 5 to 10 times smaller than C_P [16]. The finalized structure of the loop filter is shown in Fig. 3.6.

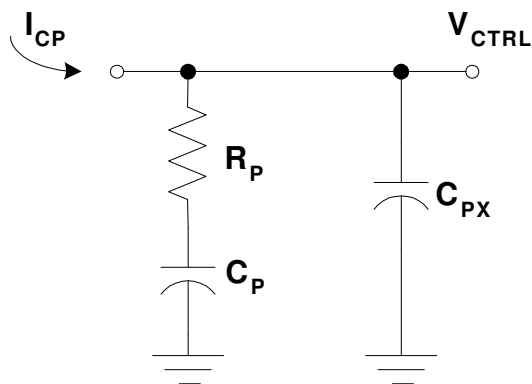


Figure 3.6. Loop filter after the addition of the stabilizing resistor R_P and the ripple filtering C_{PX} .

3.3 Locking Behaviour of the CP PLL

Contrary to the classical systems that make use of PLLs such as frequency synthesizers in the mobile communication systems, the CDR circuits do not impose stringent requirements on the settling time of the synchronization unit. The nonlinear analysis of the overall PLL along with its locking behaviour is well taken care of in [18].

Therefore, instead of a detailed transient response analysis of the PLL, we will briefly give the basic definitions of the locking behaviour of the system that are applicable to the CDR applications.

The research papers that are published on the CDR design will usually mention two terms regarding the acquisition behaviour of the system [19]-[23]. We will discuss them in the subsequent sections.

3.3.1 Capture Range

Probably, the most crucial of the above-mentioned terms is the *capture range* for a CDR design. The capture range, which is also called *acquisition range* or *pull-in range*, will determine the number of design iterations and hence the number of fabrication runs that one will have to meet the exact operation frequency with a reasonable margin. This margin is necessary to prevent the temperature and process variations from offsetting the design performance.

Capture range is the frequency interval that a PLL circuit can acquire lock onto the clock frequency once the system is turned on. In general, the VCO will be oscillating at its free running frequency ω_{FR} at start-up. The frequency difference between the data signal and the VCO output will then be $\Delta\omega = |\omega_{IN} - \omega_{FR}|$. The maximum amount of $\Delta\omega$ within which the system can achieve lock is the capture range for that PLL.

The capture range depends mostly on the loop filter bandwidth. The wider the bandwidth is, the wider the capture range will be. We should note that the bandwidth cannot be made large indefinitely as it will violate the PLL stability criteria [17] and fail to filter the high-frequency noise. With the increasing bandwidth, the linear time invariant approximations and the formulas derived so far will not hold, either. Therefore, some reasonable trade-offs are made and innovative circuit design techniques have to be employed to achieve a feasible performance.

3.3.2 Tracking Range

Once the PLL is locked, the circuit has to maintain the lock. With the ripples coming from the charge pump or due to the sudden changes in the data signal characteristics, it is not always possible for the circuit to tolerate the frequency jumps. The amount of frequency variations that a PLL can handle at locked state determines the *tracking range*. The circuit can accommodate small changes and have sufficient time to respond to them. Unfortunately, the abrupt and large jumps will usually drive the PLL out of lock. If the variation falls within the acquisition range, it is still possible to acquire lock. Otherwise the circuit can never re-lock unless it is backed by a frequency acquisition aid.

3.4 Summary

A detailed analysis for the Type-II PLL is carried out. This will help us understand the challenges in the design of the PLL-based, closed-loop CDRs that we have focused on in this thesis.

Fundamental loop equations are reviewed and their implications on the CDR designs are discussed. The main parameters of the PLLs, such as the natural frequency and the damping factor are obtained. Subsequently, the locking behaviour of the PLLs and the definitions of the capture range and tracking range are briefly discussed.

It is observed that conventional Type-II PLLs with conventional loop filter structure have to employ bulky passive components in order to satisfy the jitter requirements. Therefore, some circuit level and architectural modifications are necessary in order to achieve the jitter compliance and the monolithic integration of the CDR at the same time.

CHAPTER 4

10-GHz Integrated Voltage-Controlled Oscillator

After the PLL analysis in previous chapters, it is time to go into the details of the PLL-based CDR designs. It is not a far-fetched claim that the design of each block in the CDR system is equally important and it requires careful design steps to be taken. However, the conventional approaches to the problems that are encountered while designing CMOS CDRs do not provide cutting-edge solutions to the issues at hand. Either at the system level or the circuit level, the designers have to push the limits of the conventional methods to obtain innovative solutions.

In order to get the best performance out of a 0.18- μm CMOS process we have explored several circuit design techniques and tested their effectiveness in physical implementations wherever possible. The first block that we start our exploration is the VCO block. After a brief set of definitions of different types of VCOs, our findings and their impact on the overall CDR system will be presented.

4.1 Oscillator Fundamentals

An oscillator is a nonlinear device that makes use of the concept of positive feedback to amplify the inherent noise and to generate a periodic output. One possible feedback topology that is used in oscillators is shown in Fig. 4.1.

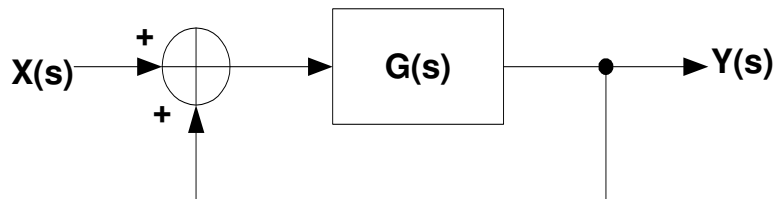


Figure 4.1. Feedback oscillator.

The transfer function for this configuration can be obtained as

$$\frac{Y(s)}{X(s)} = \frac{G(s)}{1 - G(s)} \quad (4.1)$$

where the feedback path has unity gain and the forward loop gain is denoted as $G(s)$ in s -domain. Note the positive feedback in the loop. We have mentioned the lack of the external input for an oscillator circuit at the beginning of this discussion, but to help us understand the principles of oscillation, we have included the input $X(s)$ in Fig. 4.1.

In order to produce oscillation at a specific frequency ω_0 , two conditions –also known as *Barkhausen's Criteria*- have to be satisfied:

1. The open loop gain is at least equal to unity. ($|G(j\omega_0)| \geq 1$)
2. The *total* phase shift around the loop is 0° or 360° . ($\angle G(j\omega_0) = 0^\circ$ or $\angle G(j\omega_0) = 360^\circ$)

We should also note that Barkhausen's criteria are necessary but not sufficient to start (or sustain) an oscillation for some circuit topologies. Careful study of the stability should be carried out to determine the possibility of an unreliable or unpredictable oscillation for those circuits [25]. Nevertheless, assuming that these conditions are met at only one frequency, to ensure a smooth start-up for the oscillation, the circuit

usually requires a ‘kick’ that will trigger the amplifier $G(s)$ to induce sufficient gain through feedback. Fortunately, the switch-on noise of the power supply, or the random noise generated by the devices can provide that.

In CDR applications, an oscillator that is capable of oscillating in various frequencies depending on a control voltage V_{CTRL} is more useful than a fixed frequency counterpart. This tunable variant of the oscillator is better known as the voltage-controlled oscillator (VCO). The relationship between the output frequency and the control voltage of a VCO is given as:

$$\omega_{OUT} = \omega_{FR} + K_{VCO} \cdot V_{CTRL} \quad (4.2)$$

where ω_{FR} is the free running frequency, expressed in rad/s. Currently there are two major topologies of VCOs in use:

1. Ring Oscillators
2. LC Oscillators

4.2 Ring Oscillators

Ring oscillators are formed by cascading a number of gain stages in a loop formation or a ring shape. In order for a ring oscillator to maintain the oscillation at a certain frequency, Barkhausen’s criteria must be satisfied. For the single-ended designs, an odd number of gain stages is required whereas for the differential ring oscillators, this number should be 2 or its integer multiples [24].

The oscillation frequency of a ring oscillator mostly depends on the delay that is introduced by each stage in the loop. By simply adjusting this delay, a voltage

controlled ring oscillator can be realized. Changing the load resistor of the gain stages, applying positive feedback to the gain stage outputs [11], or delay variation by interpolation [14], [22] are among the various techniques that are employed for delay variation.

The intermediate stages in a ring oscillator can deliver clock signals with equal frequencies and equally spaced phases. This feature of the ring oscillator makes it very attractive for multiphase-clocked applications such as half-rate CDRs [22], [23]. The wide tuning range that can be achieved from a ring structure is also helpful for the first-time fabrications where the designers do not have sufficient information on the process and the temperature variations. Unpredicted frequency shifts can be compensated using a ring VCO with a wide tuning range.

Unfortunately, the ring oscillators tend to have higher phase noise than their LC counterparts because of their high number of active and passive devices in the signal path [11], [26]. Furthermore, the ring oscillator phase noise varies with the control voltage, resulting in uneven jitter performance for a CDR system [23]. And the speed limitation resulting from the loading effect of the cascaded gain stages prevents the designers from using ring topology for high-frequency CDR applications. Particularly when the operation frequency approaches the process boundaries, the ring structure proves not practical: Maximum oscillation frequency for a three-stage differential ring oscillator in 0.18- μm CMOS technology is reported to be no more than 7 GHz [22]. The 10-GHz clock requirement for our full-rate CDR design necessitates the LC topology.

4.3 LC Oscillators

The early CDR and other PLL implementations that are mainly operating at low frequencies have led to the use of ring oscillators [27]-[30] -a perfect candidate for monolithic integration- as they didn't require bulky passive components such as capacitors or inductors. The wide tuning range of the ring oscillators is another factor that have made them popular for the *first-time fabrication trials* where achieving the desired operation frequency amid unpredicted process and temperature variations is somewhat more important than the other performance parameters such as phase noise, spectral purity, and power consumption. However, the high phase noise of the ring oscillators and the ever-increasing operation frequencies demand a better alternative in today's communication systems.

The use of the LC resonators with the active devices facilitates the design of oscillators that are exhibiting superior phase noise performance and output voltage swings. The active device can ideally compensate for the resonator tank loss and deliver the lost energy when the tank voltage is at its maximum so as not to cause any phase distortion [31]. This behaviour is far away from that of a ring oscillator where first of all, there is not a high-Q resonator; and second, the energy resulting from the feedback connection is delivered at the wrong time, i.e., at the zero-crossings of the output voltage, resulting in high phase noise [32].

Another feature of the LC configurations is that they can produce circuits with very high operation frequencies contrary to the ring oscillators that suffer from the inherent delay from each gain stage in the loop. Maintaining the oscillation with minimum number of stages so as to increase the frequency proves very difficult particularly for

our frequency of interest where the 0.18- μm CMOS process operates at the edge of its performance boundaries.

Having opted for the LC oscillators for our CDR design, it is instructive to review fundamental properties of the LC resonators before investigating the improvements that can enhance their performance in a CDR system.

4.3.1 LC Resonators

At the core of an LC oscillator is the parallel combination of a resonator tank that is formed by an inductor and a capacitor. This parallel combination is shown in Fig. 4.2.(a). The resistor R_S at the inductor branch is due to the parasitic resistance of the inductor coil, where the quality factor Q of the inductor is defined as $\frac{\omega \cdot L_S}{R_S}$. For monolithic implementations, the Q value ranges from 3 to 10, depending on the frequency of operation.

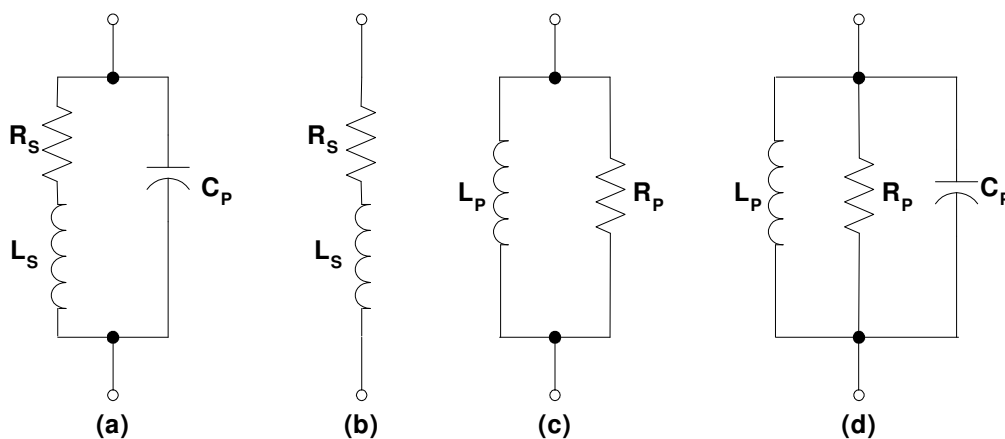


Figure 4.2. (a) LC tank, (b) Series L-R connection, (c) Parallel L-R connection, (d) Parallel RLC tank.

The conversion of the series L-R to a parallel form is for the ease of analysis and design insight. Since the two configurations are equivalent, the parallel inductor L_P can be calculated as

$$L_P = L_S \cdot \left(1 + \frac{R_S^2}{L_S^2 \cdot \omega^2} \right) \quad (4.3)$$

The second term in the parenthesis is equal to $1/Q^2$ and hence, assuming $Q \gg 1$,

$$L_P \approx L_S \quad (4.4)$$

Similarly the parallel resistor can be obtained as

$$R_P = \frac{L_S \cdot L_P \cdot \omega^2}{R_S} \approx \frac{\omega^2 \cdot L_S^2}{R_S} \approx Q^2 \cdot R_S \quad (4.5)$$

When we analyze the tank circuit shown in Fig. 4.2.(d), we observe that the reactive components of the tank will be equal at resonance frequency ω_{res} :

$$j \cdot \omega_{res} \cdot L_P = \frac{1}{j \cdot \omega_{res} \cdot C_P} \quad (4.6)$$

The oscillation frequency in rad/s can be written as

$$\omega_{OSC} = \omega_{res} = \frac{1}{\sqrt{L \cdot C}} \quad (4.7)$$

Since the reactive components of the total tank impedance are of opposite signs, they will ‘cancel’ each other at resonance, resulting in a simple resistor R_P as the effective impedance of the tank. Therefore, the addition of an active device is inevitable to compensate for this resistive loss at the resonator tank.

As long as Barkhausen’s criteria are satisfied, numerous versions of this resonator and the active device pair combination can be built to realize an oscillator. Well-known examples include Colpitts oscillator, Pierce oscillator, and their variants [25]. On the

other hand, few of the LC oscillators will be suitable for the monolithic implementations since the space limitations and the size of the passive components in the resonator usually have stringent trade-off conditions.

4.3.2 Negative- G_m Oscillators

The parallel tank structure shown in Fig. 4.2.(d) suffers from a resistive loss due to R_p .

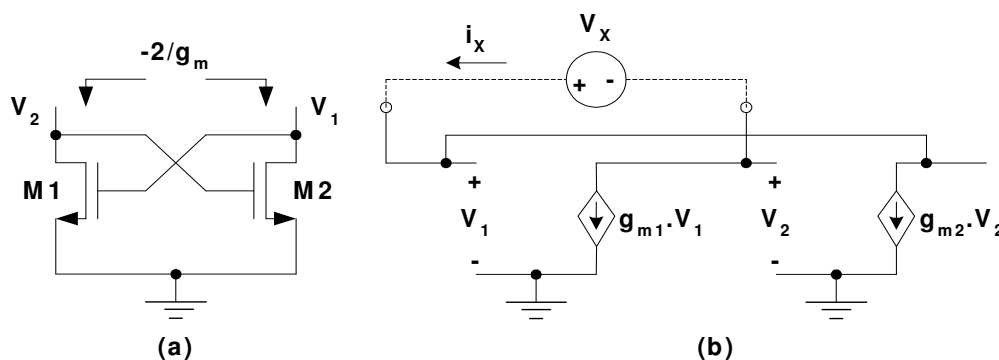


Figure 4.3. (a) Negative resistance cross-coupled pair and (b) its small-signal equivalent.

If this loss can be compensated by any means, the oscillation can be sustained and a well-defined voltage at the oscillator output is obtained. One circuit that can generate a negative resistance is illustrated in Fig. 4.3. Using the small signal equivalent circuit, we can calculate the resistance between the terminals V_1 and V_2 . V_X and i_X in Fig. 4.3.(b) are the test voltage and current, respectively. Thus, we get

$$i_X = g_{m2} \cdot V_2 = -g_{m1} \cdot V_1 \quad (4.8)$$

$$V_1 = -\frac{i_X}{g_{m1}} \quad (4.9)$$

$$V_2 = \frac{i_X}{g_{m2}} \quad (4.10)$$

The test voltage can be expressed in terms of the terminal voltages as

$$V_X = V_1 - V_2 \quad (4.11)$$

Finally, in order to find the resistance, we first assume that the two MOS devices exhibit the same transconductance: $g_{m1} = g_{m2} = g_m$ and calculate the ratio V_X/i_X as

$$\frac{V_X}{i_X} = \frac{V_1 - V_2}{i_X} = -\frac{\frac{i_X}{g_{m1}} - \frac{i_X}{g_{m2}}}{i_X} = -\left(\frac{1}{g_{m1}} + \frac{1}{g_{m2}}\right) = -\frac{2}{g_m} \quad (4.12)$$

When combined with a resonator RLC tank, this structure forms the very basic form of the cross-coupled LC oscillator topology (Fig. 4.4.(a)). Due to the negative resistance obtained in this configuration, these circuits are also called ‘negative- g_m oscillators’.

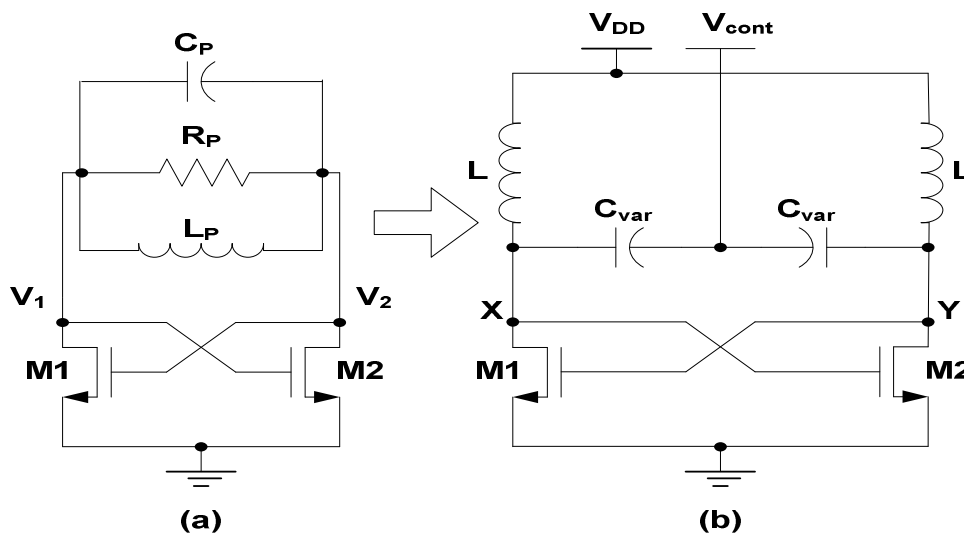


Figure 4.4. (a) Basic cross-coupled LC oscillator, (b) A Cross-coupled voltage-controlled oscillator.

The equation (4.7) reveals that the oscillation frequency can be tuned by varying either the inductor or the capacitor values in the tank [11]. Unfortunately, due to the complex nature of the on-chip inductors, modifying the inductor dimensions is not practical for the purpose of frequency tuning and hence the capacitors have become the crucial components for varying the frequency.

The oscillators are tuned using variable capacitors that are also known as *varactors*. The varactors can be realized by either reverse-biased *pn-junction* diodes or the MOS capacitors that are simply formed by shorting the drain and source terminals of a MOS transistor. The capacitance of a varactor can be changed by simply increasing or decreasing the voltage potential across its terminals. With the addition of the varactor and the supply biasing, the oscillator in Fig. 4.4.(a) can be redrawn as shown in Fig. 4.4.(b). Since the negative resistance is still provided by the cross coupled pair, the operation principles for this new configuration are still the same as those of the former.

4.4 10-GHz VCO Design

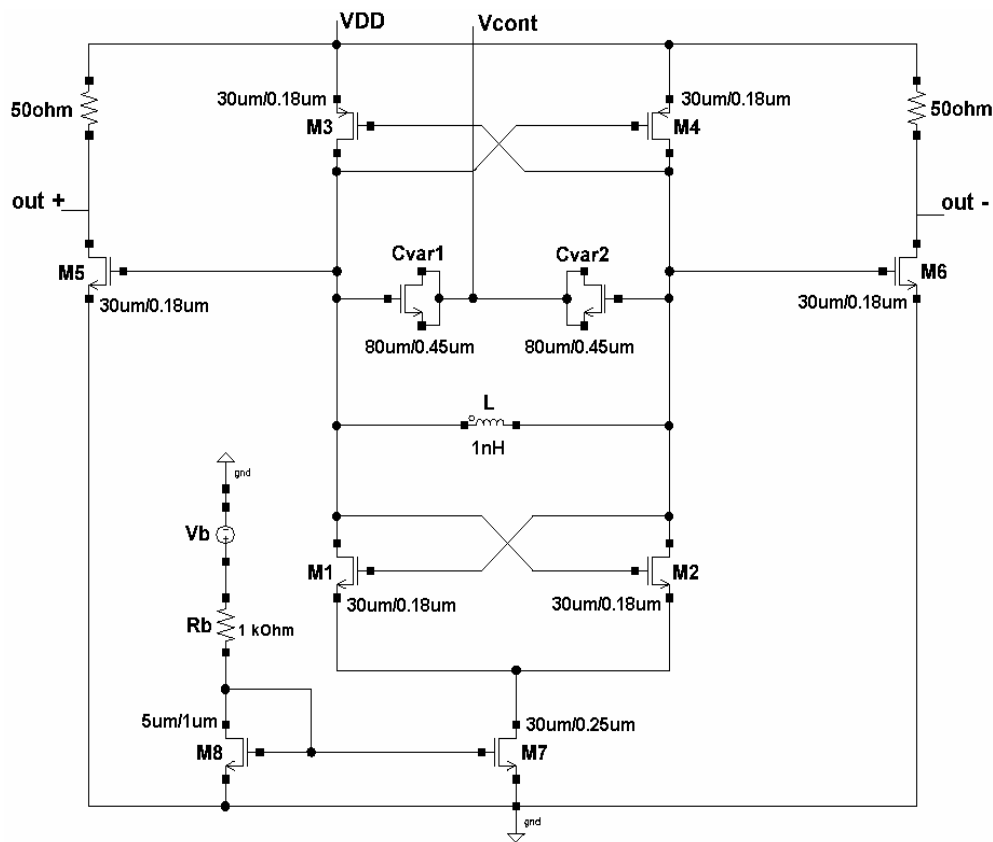


Figure 4.5. Complementary cross-coupled VCO.

An improved version of the simple cross-coupled oscillator is designed to further investigate the impact of the VCO on a CDR system. The schematic of the circuit with the device dimensions is shown in Fig. 4.5.

This is a *complementary cross-coupled VCO* where the fixed capacitors are replaced with the MOS varactors to perform frequency tuning and a complementary PMOS pair is added to reinforce the negative resistance. The PMOS pair also improves the symmetry between the rise and fall times of the waveforms at the drain terminals of M1 and M2, which is essential to reduce the upconversion flicker noise [11], [31].

This circuit can be viewed as two identical Colpitts oscillators that are cross-coupled together. Each of them utilizes the other as an active impedance transformer and as part of its feedback loop. At the expense of reduced maximum oscillation frequency due to higher parasitics around the tank, this topology provides better noise suppression and a well-controlled output swing when compared to the simple cross-coupled VCO counterpart [31]. The devices M5 and M6 form the buffer with the 50- Ω resistors to facilitate the on-wafer measurement. The current mirror (M7-M8) is added to the VCO to supply a stable biasing current and to prevent the supply voltage variations that can modulate the VCO output voltage [11].

The varactors C_{var1} and C_{var2} are implemented using NMOS transistors with shorted drain and source terminals. The tank capacitor includes the variable capacitances (C_{var1-2}), the parasitic capacitance of the on-chip inductors, and the parasitic capacitance at the gate and drain terminals of the MOSFETs [M1-M6].

The VCO circuit is fully differential and symmetric to reduce the cross talk and other parasitic effects. Knowing that the parasitic capacitance of a component increases with its size, we have used small aspect ratios for the cross-coupled pair and the buffer transistors.

The VCO design at such a high frequency requires several techniques to be applied so that one can obtain a working prototype in minimum number of fabrication iterations. Although the device models that are provided by the foundry take the parasitic effects into account to some extent, their accuracy is inversely proportional with the operation frequency. Additionally, not only the devices introduce parasitic capacitance; the metal interconnects and the test pads also degrade the performance. Therefore, the layout and the circuit level simulations have to be used interchangeably to tune both of these domains.

We start by *roughly* determining the inductor and the capacitor values for an oscillation frequency of 10 GHz using (4.7). The inductor is around 1nH whereas the total capacitor value is calculated to be 300 fF. The varactor contributes 120 to 200 fF of this value, which is sufficient to obtain a tuning range of 2 GHz.

The preliminary layout is drawn and the parasitic extraction is performed. The information obtained from this extraction is used to construct the post-layout simulation environment. The post-layout schematic gives us valuable insights about the circuit behaviour with the parasitics. We observe that the oscillation frequency shifts to 8.3 GHz with a slight degradation of the phase noise. For the *fabricated* VCO to oscillate at 10 GHz, we have to design the circuit targeting a higher frequency, i.e.,

around 12 GHz. While we keep the inductance constant, we change the varactor capacitance and finalize the device dimensions as shown in Fig. 4.5.

Table 4.1. The effect of parasitics on the VCO design.

	Primitive Design	Finalized Design	
	Post-Layout	Post-Layout	Measurement
	Simulation	Simulation	
Max. frequency (GHz)	8.3	10.8	10.5
Phase noise (dBc/Hz)/ frequency offset	-102/1MHz	-100.2/1MHz	-95/1MHz
Tuning range (GHz)	2	2.5	2.2
Voltage supply (V)	1.8	1.8	1.8
Power consumption w/o buffers (mW)	2.55	2.4	2.52
Technology	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS

Table 4.1 illustrates the results obtained in the design cycle. The discrepancy between the measurement results and the post-layout simulations clearly demonstrate that using the layout-parasitic extraction in the intermediate stages of the design considerably helps us estimate the effect of parasitics.

The ‘primitive design’ in Table 4.1 refers to the case where the circuit is configured for 10-GHz oscillation without taking the layout parasitics into account, relying only on the device models. As a result, the post layout simulation indicates a huge discrepancy from the targeted frequency. On the other hand, when the frequency shift is compensated for in the design stage by adjusting the LC tank, the post-layout

simulation of this ‘finalized design’ and the measurement results indicate a reasonably close match.

4.4.1 Effect of Supply Voltage Variation on VCO Tuning Range

In a complementary cross-coupled VCO, one of the varactor terminals is connected to the control voltage V_{cont} and the other is connected to the output node V_{out} . For a fixed V_{cont} input, V_{out} changes with the oscillating output waveform but it nevertheless maintains an average value along with a *dc* component. The difference between this average value and V_{cont} determines the capacitance of the varactor.

A typical *voltage vs. capacitance* characteristic of an NMOS varactor is shown in Fig. 4.6. The voltage across the varactor depends on not only the control voltage but also the supply voltage.

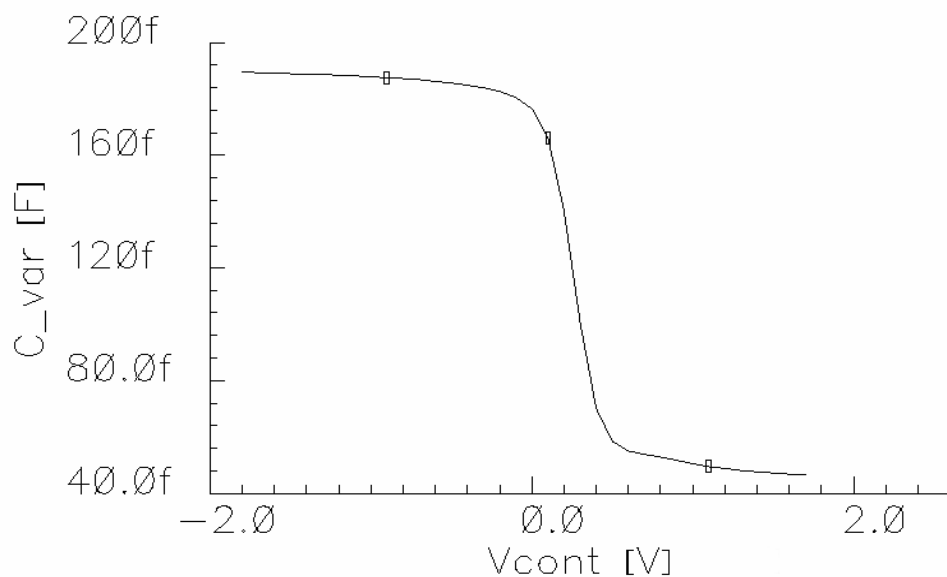


Figure 4.6. Typical varactor characteristic.

Fig. 4.7 illustrates this effect of the supply voltage. Simulations indicate that for nominal supply voltage of 1.8 V, the VCO exhibits a wide tuning range of 2.2 GHz. On the other hand, for $V_{DD}=1.5$ V, the variable portion of the varactor cannot be fully utilized, resulting in a reduced tuning range of 300 MHz.

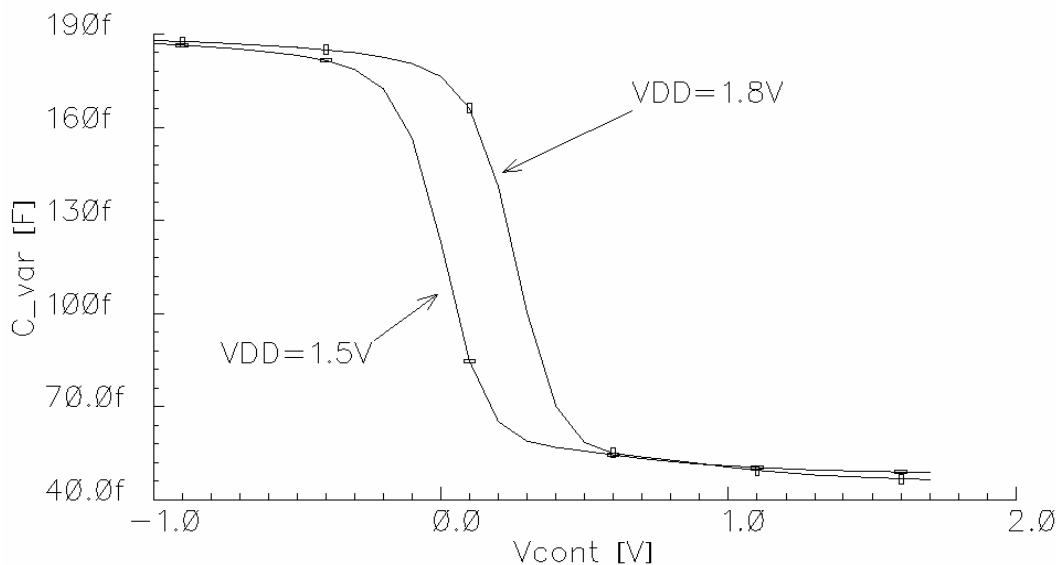


Figure 4.7. Varactor behaviour under two different supply voltages.

This limitation of the tuning range is not necessarily a drawback for the VCO; it can be very useful in SONET systems: Submicron technologies require reduced supply voltages in order to prevent oxide breakdown. On the other hand, supply voltage scaling in deep-submicron technologies inevitably increases K_{VCO} for a given tuning range [22].

In order to satisfy the jitter tolerance and jitter generation requirements in high bit rate SONET systems, the VCO control voltage must be free of unwanted spikes, glitches or other noise disturbances. For a VCO with high K_{VCO} , even a few millivolts of disturbance on the V_{cont} results in significant frequency variations, which then causes unsatisfactory performance of the overall system. It would be preferable to have an

adaptable tuning scheme in the VCO so that one can make use of the high K_{VCO} for the frequency acquisition and achieve fast frequency lock and a lower K_{VCO} for the data recovery loop to satisfy the jitter tolerance requirements.

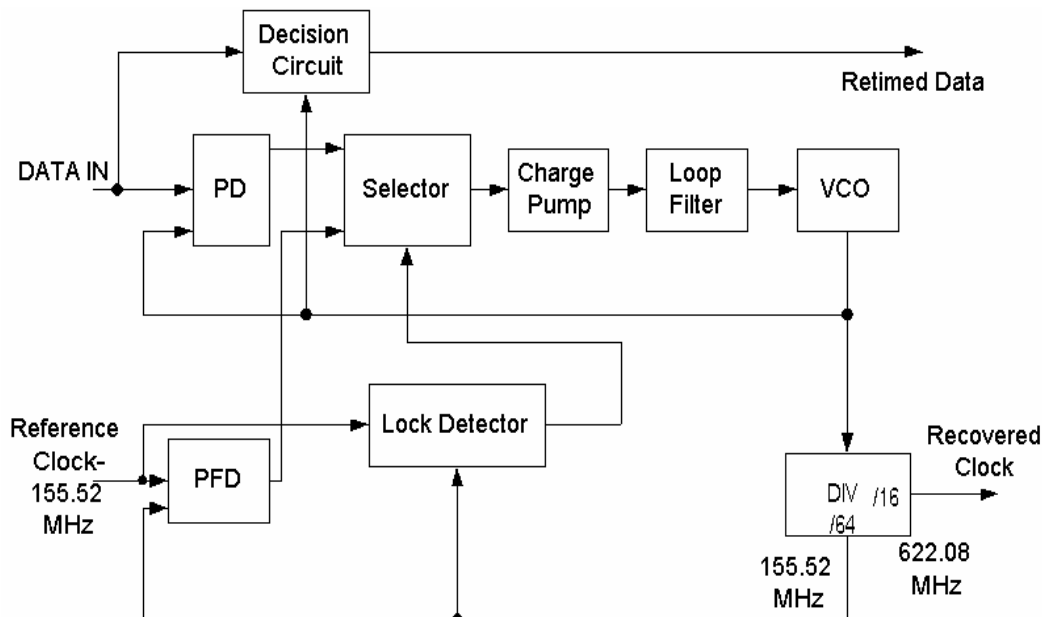


Figure 4.8. Double-loop CDR architecture in [21].

In most of the CDR systems there are various ways to bring the free running VCO frequency near the vicinity of the operating frequency. One method is employing two phase-locked loops. A double-loop CDR architecture is shown in Fig. 4.8, [21]. In this architecture while the PFD, Charge Pump (CP), Loop Filter (LPF), VCO, and the Divider form the frequency acquisition loop (Loop 1); the PD, CP, LPF, and the VCO form the data recovery loop (Loop 2). The Lock Detector decides when to switch from one loop to the other. Briefly, when the CDR unit is first turned on, or has lost lock after sometime, the VCO will be running at its free running frequency; therefore, it needs to be brought towards the data rate. Loop 1 initiates this frequency acquisition process with the help of an external reference. The frequency difference between the external reference and the VCO output is contained in a well-defined boundary,

expressed in parts per million [ppm]. Loop 2 takes over after this and achieves a phase lock, which then makes the CDR unit ready for data recovery.

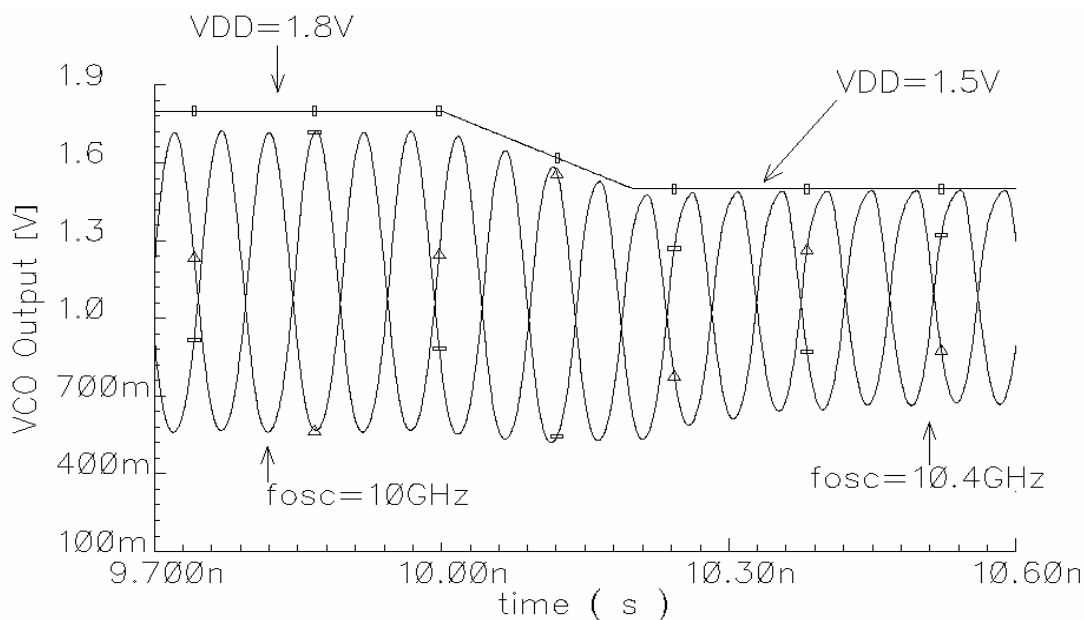


Figure 4.9. Simulating the supply voltage reduction.

The supply switching can prove useful in this arrangement. For a V_{cont} voltage span of [0--1.8 V], it can automatically reduce the tuning range from 2.2 GHz to 300 MHz, corresponding to a K_{VCO} of 1.2 GHz/V and 200 MHz/V, respectively. One can start the VCO with $V_{DD}=1.8$ V and achieve a fast frequency lock after which he can switch V_{DD} down to 1.5 V and proceed to data recovery.

In order to see the effects of the switching scenario, we have simulated the VCO accordingly. The simulation result is shown in Fig. 4.9. The circuit does not cease oscillation during the switching. The amplitude slightly decreases and the frequency goes up by 400 MHz. With a careful design of the output buffers and the supply switching circuit, the VCO can provide sufficiently high output swing and achieve robust operation.

4.4.2 Measurement Results

The VCO was fabricated in CHRT 0.18- μm RF CMOS 2-poly 6-metal process. The active chip area is 280 μm x 250 μm . The test setup is comprised of Cascade Microtech™ Ground-Signal-Ground (GSG) on-wafer measurement probes, high-frequency calibrated cables, and HP 8565E spectrum analyzer featuring a frequency measurement span of 9 kHz-50 GHz.

The maximum oscillation frequency is measured to be 10.5 GHz for both supply voltages of 1.5 V and 1.8 V. Fig. 4.10 and Fig. 4.11 present the frequency spectrum analyzer plot of the VCO output at 10.33 GHz and the chip micrograph, respectively.

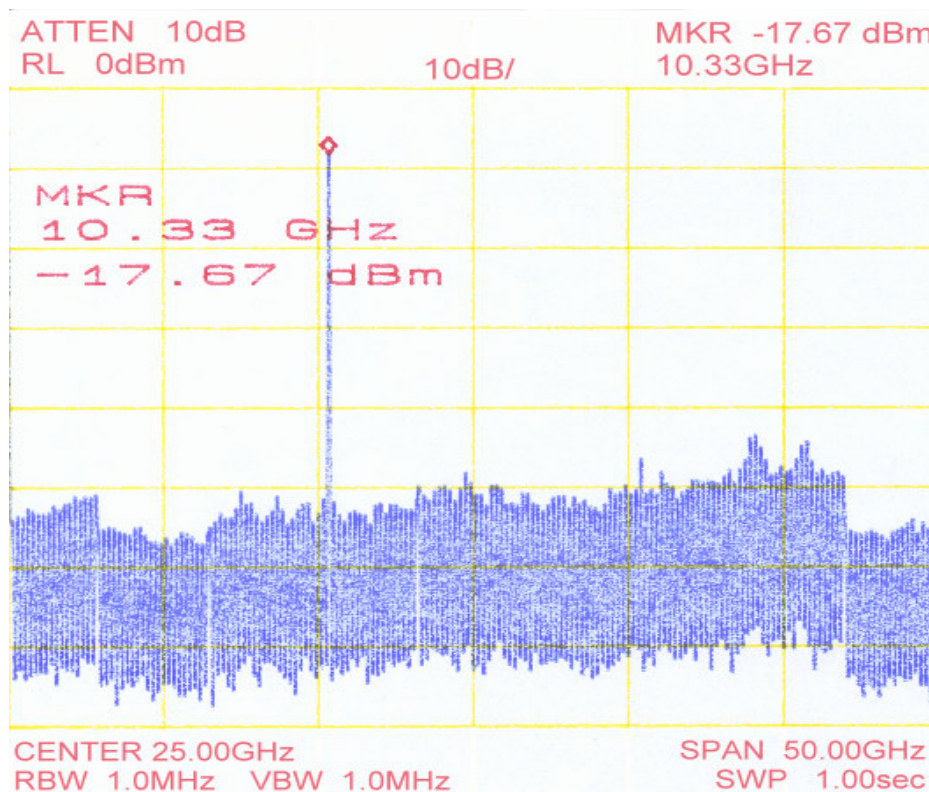


Figure 4.10. Spectrum analyzer plot of the VCO output.

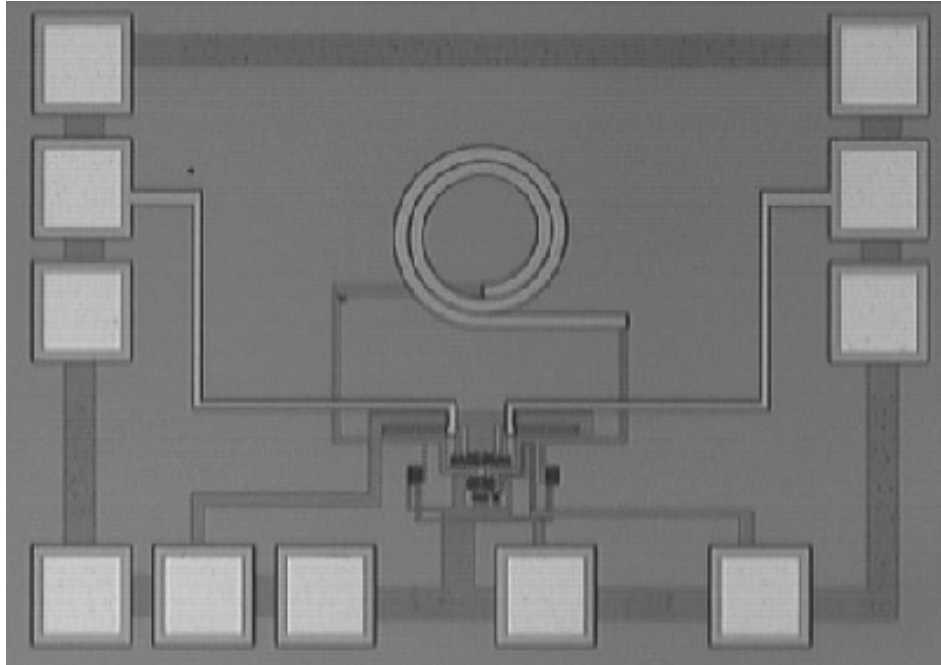


Figure 4.11. Chip micrograph of the 10-GHz VCO.

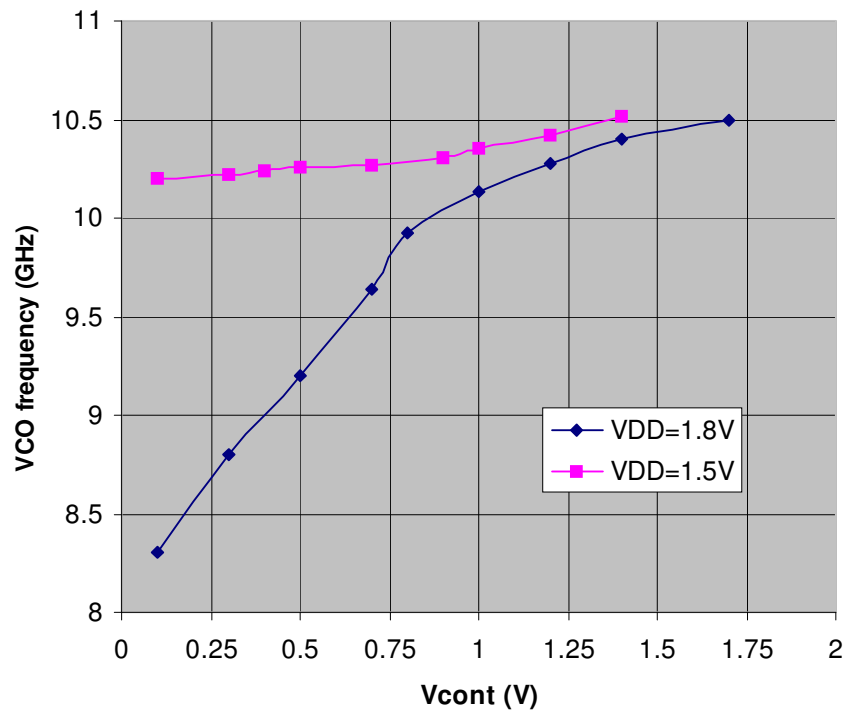


Figure 4.12. VCO tuning range for different supply voltages.

The measured VCO output frequency versus V_{cont} is plotted in Fig. 4.12 so as to illustrate the slope change in the K_{VCO} for different supply voltages. A wide tuning range of 2.2 GHz is obtained for 1.8-V supply, whereas it reduces to 300 MHz for 1.5 V.

The phase noise is measured to be -95 dBc/Hz at 1-MHz offset. The below-3mW power consumption -excluding the buffers- indicates that our design is also suitable for low-voltage and low-power applications. Table 4.2 summarizes the measurement results and compares them with the previously reported VCOs.

Table 4.2. Performance comparison of the fabricated VCO with the existing designs.

	Designed VCO (1.8V)	Designed VCO (1.5V)	[33]	[34]	[35]
Max. frequency (GHz)	10.5	10.5	10.4	10.55	10.7
Phase noise (dBc/Hz)/ frequency offset	-95/1MHz	-93/1MHz	-91/100kHz	-84.4/100kHz	-107/1MHz
Tuning range (GHz)	2.2	0.3	1.1	0.3	1.5
Voltage supply (V)	1.8	1.5	1.8	3.5	1.8
Power consumption w/o buffers (mW)	2.52	1.95	5.8	28	NA
Technology	0.18- μm CMOS	0.18- μm CMOS	0.18- μm CMOS	0.35- μm CMOS	0.18- μm CMOS

Our VCO and the one that is reported in [33] make use of standard spiral inductors, whereas those in [34] and [35] enjoy the advantages of the symmetric differential structures. Nevertheless, the proposed VCO performs efficiently with the given low

power consumption and wider tuning range in the 1.8-V mode. It should also be noted that the phase noise value given in [35] is not the stand-alone VCO contribution; it is rather the overall CDR phase noise. As a result of the filtering effect of the loop, this value is much lower than the stand-alone VCO phase noise.

4.5 Summary

Fundamental concepts about the oscillators are described in this chapter. The pros and cons of major oscillator topologies and the frequency tuning methods are investigated. The LC tuned VCO is the suitable choice for our 10-Gb/s OC-192 CDR design.

The effects of supply voltage variations on the VCO tuning range and methods to optimize the VCO performance exploiting this feature are also investigated for SONET system applications. The design of a 10-GHz VCO for high-frequency data communication applications is presented for this purpose. The circuit is fabricated in a commercial 0.18- μm RF CMOS process. The phase noise is measured to be -95 dBc/Hz at 1-MHz offset with a very low power consumption of 2.5 mW from a 1.8-V supply, excluding the output buffers. The performance of the 10-GHz VCO circuit strengthens our belief that CMOS technology has great potential for optical data communication circuits.

CHAPTER 5

Phase Detectors

A phase detector circuit detects and amplifies the phase difference between the input signal and a reference clock signal and provides this information to the succeeding blocks in the loop. Unlike the sequential phase and frequency detectors employed in the frequency synthesizers and other periodic-input PLL systems, the PDs that are incorporated in CDR systems operate on *random* data format. Due to the nature of the random data that was described previously, the PD design is not a straightforward process and it requires a good analysis of the input data characteristics.

The PDs for random data must be able to perform two critical operations [11]:

- 1) *Edge detection* to determine the data transitions in order to produce a clock signal from a NRZ data for synchronization.
- 2) *Phase difference detection* to align the clock signal to complete the clock and data recovery process.

Recently, a significant effort has been spent on designing high-speed low-power CMOS phase detectors for CDR systems as the performance of CDR is critically dependent on the characteristic of the PD [2], [7], and [19]-[23]. Traditionally, there are two main categories of PDs that are dealing with random data input: Linear PD and binary PD.

5.1 Linear Phase Detectors

A typical example of a linear phase detector is the Hogge phase detector reported in [36]. Fig. 5.1 shows the simplified block diagram of a Hogge PD and its output waveforms.

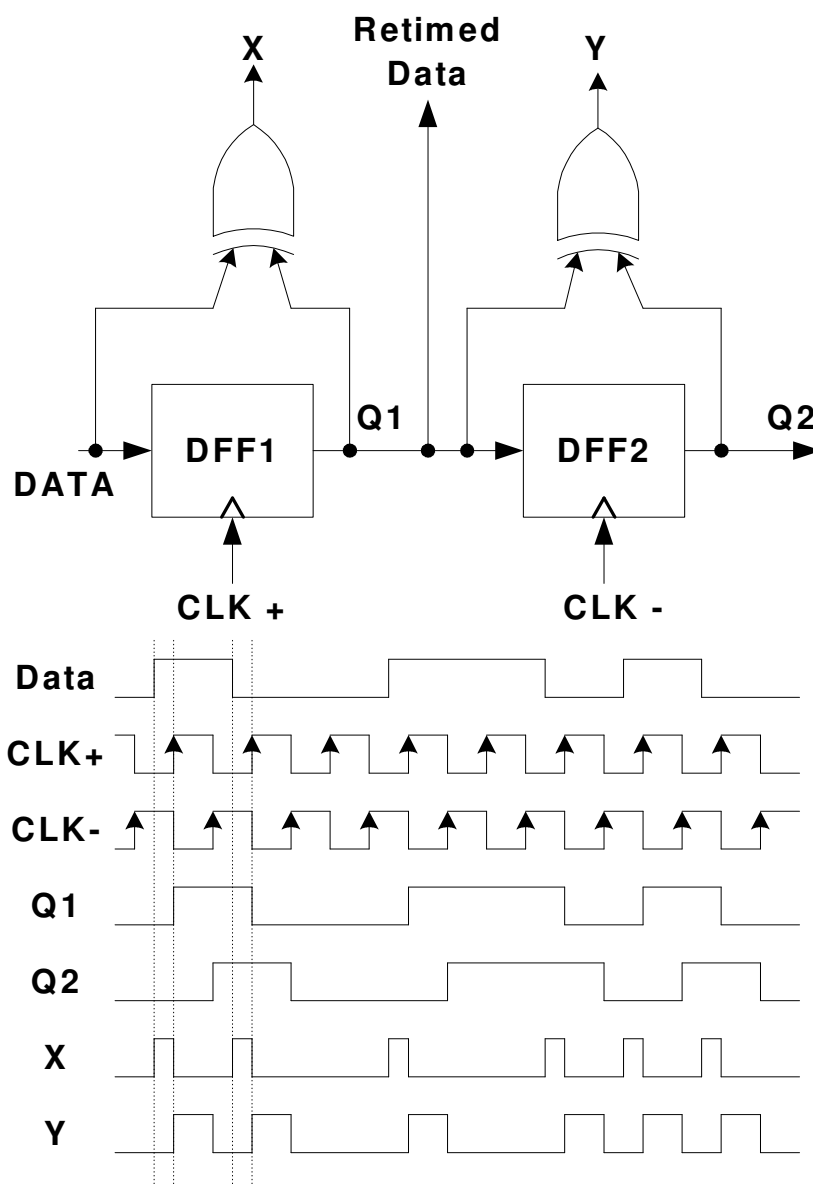


Figure 5.1. Hogge phase detector and its waveforms.

The first D-flip-flop DFF1 samples the incoming data by the VCO output $CLK+$, producing $Q1$, which is a delayed version of the input data. Passing this delayed

replica and the original data signal through an Exclusive-OR gate XOR will result in X , the *raw* phase difference between these two signals. In order to reduce the sensitivity of the circuit to the data transition density and prevent a false lock situation, DFF2 is added to the core phase detection unit. $Q1$ from DFF1 and the complementary clock signal $CLK-$ from the differential VCO are input to the DFF2 to generate $Q2$, half a clock period delayed version of $Q1$. When $Q1$ and $Q2$ are XOR-ed, fixed-width pulses are generated. This width does not change with the data transition density and provides the reference for accurate comparison of the phase difference.

As can be seen in Fig. 5.1, for each data transition there is a pulse X , the width of which is proportional to the input phase difference, suggesting that the circuit can operate as a linear PD satisfying both of the above-mentioned requirements. An additional feature of this configuration is that since the DFF1 output is aligned with the $CLK+$, it can be output as the retimed data, obviating the need for an extra decision block for data retiming.

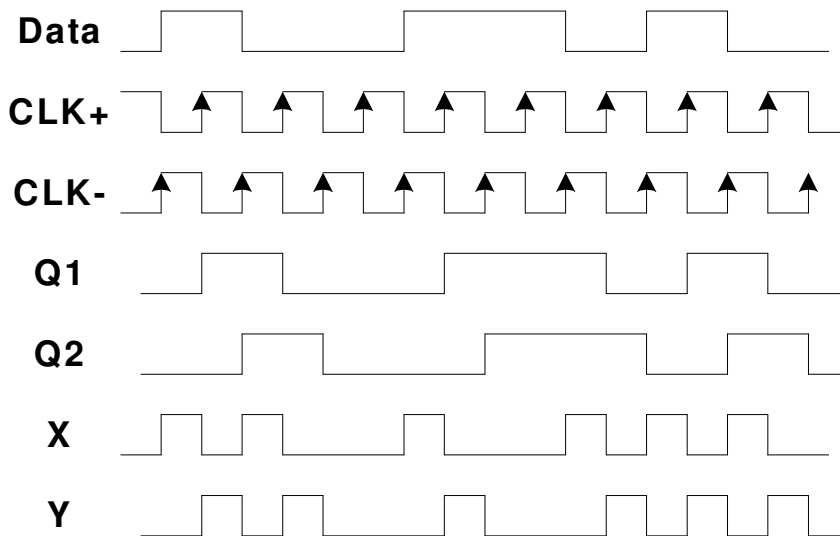


Figure 5.2. PD waveforms in phase-locked condition.

Under locked condition, the rising edge of $CLK+$ signal is sampling the midpoint of each bit for optimal sampling of the data stream, thus X and Y produce equal pulse widths (Fig. 5.2). As a result, the Hogge PD does not generate significant activity on the VCO control line and hence it results in a smaller output jitter [37] in the locked condition.

While exhibiting a linear characteristic, the Hogge PD entails a number of issues that require to be taken care of in the design stage as much as possible. First, the finite delay through DFF1 introduces a phase offset in the locked condition [36], degrading the clock phase margin. Second, as shown in [11], the retiming delay through DFF2 may lead to a half-period skew between X and Y pulses. Iterative simulations have to be carried out to eliminate or minimize these delays.

5.2 Binary Phase Detectors

Contrary to the proportional outputs of the linear PDs, binary PD produces two *digital* outputs: a 'zero' for UP and a 'one' for $DOWN$. They indicate whether the data is early or late with respect to the clock [20]. Due to their rail-to-rail operation, these PDs can also be called *bang-bang* PDs.

A typical example of the binary phase detector is the Alexander configuration [38] that is shown in Fig. 5.3. It is also known as the *early-late phase detector*. The Alexander PD employs four flip-flops to realize a three-point sampling scheme and two XOR gates to compare the samples.

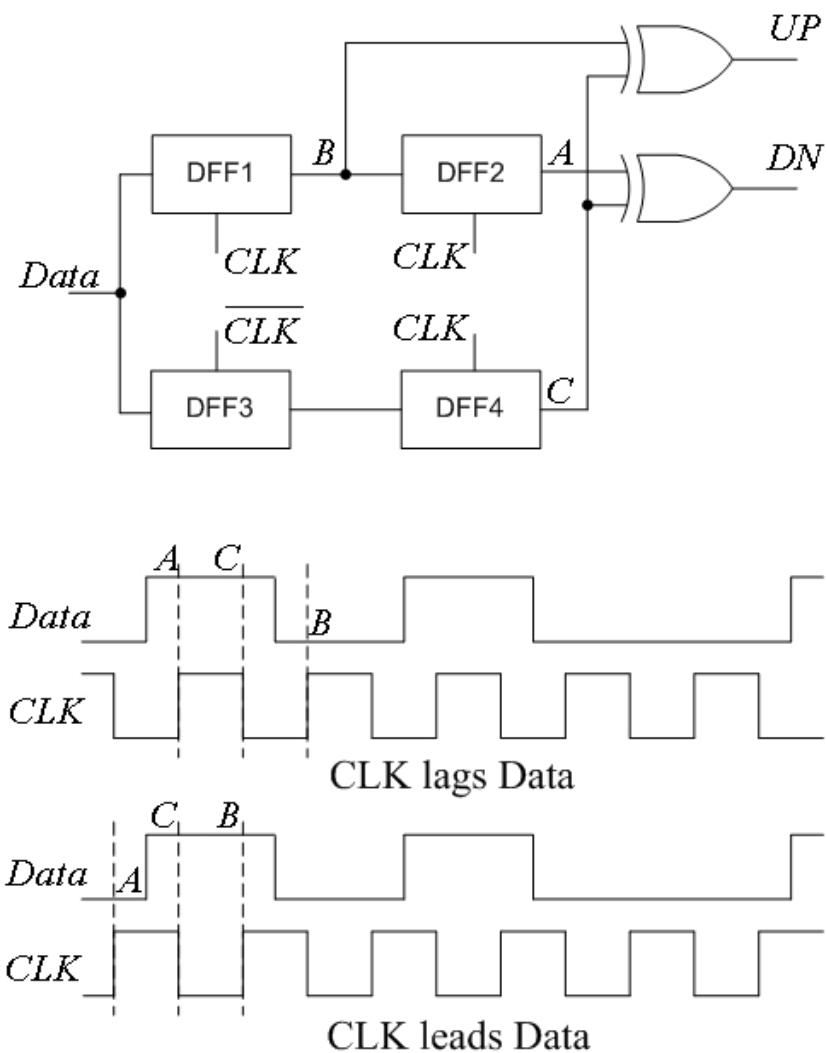


Figure 5.3. Alexander PD and its waveforms for the two cases.

As illustrated in Fig. 5.3, DFF1 and DFF2 sample the data inputs on two consecutive rising edges of *CLK*, producing *B* and *A*, respectively. DFF3 samples *Data* input on the falling edge of *CLK*, and DFF4 delays this sample by half a clock period, generating *C*. If *CLK* leads *Data*, then $A \neq C = B$, generating a low *UP* and a high *DN*. Conversely, if *CLK* lags *Data*, then $A = C \neq B$, forcing a high level at *UP* and a low level at *DN* [11], [38].

Similar to a linear Hogge PD, binary PDs can provide inherent data retiming feature. The retimed data can be directly obtained from DFF1 or DFF2 outputs. The digital nature of the binary PD makes it less demanding on the analog features of the IC technology [20]. On the other hand, being a bang-bang circuit and sensitive to the zero crossings of the signals, the sample C falls in the vicinity of the data zero crossings and causes DFF3-DFF4 pair to enter metastability when the phase difference between the data and the clock approaches zero [39]. The high gain of the PD produced at this state often introduces disturbing ripples in the VCO control line and hence generates high jitter at the VCO output [40].

The binary PDs exhibit nonlinearity and hence its jitter bandwidth varies with the jitter amplitude, making the overall CDR analysis more difficult than that of a linear system [7].

5.3 Half-rate Linear Phase Detectors

If the data rate is higher than the maximum tolerable speed of phase detectors and VCOs, a half-rate CDR architecture can be used [41], [42]. The idea is to run the VCO at a frequency equal to half of the data rate, thereby relaxing the design of the circuits in the signal path. A half-rate linear phase detector was reported in [22] with 10-Gb/s data rate. The simplified diagram of this half-rate linear phase detector is shown in Fig. 5.4.

The half-rate linear PD consists of four latches and two XOR gates. The data is applied to the inputs of two sets of cascaded latches [DL1-DL4] where each cascade forms a flip-flop. The CLK input is running at half the data rate.

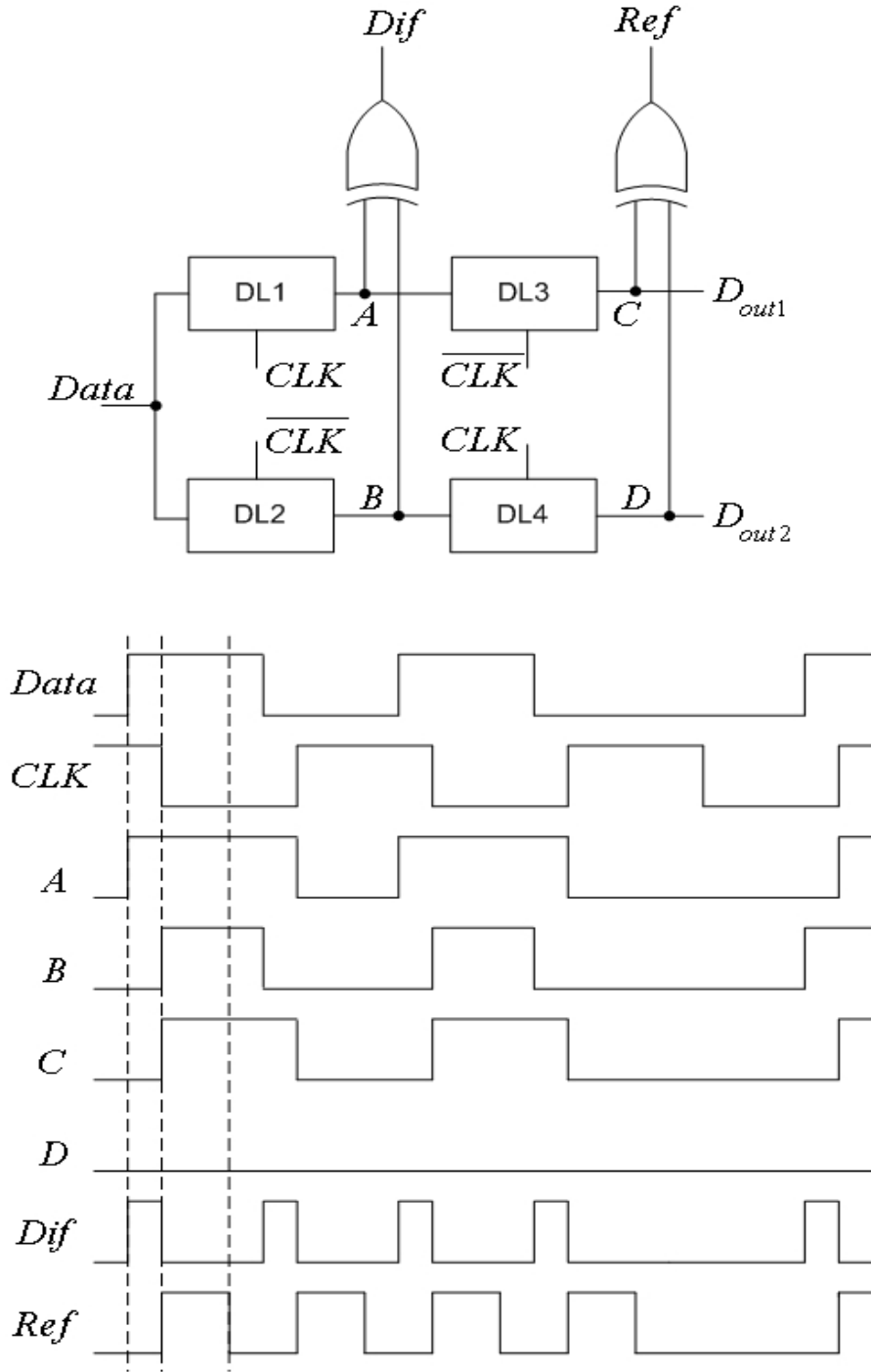


Figure 5.4. Half-rate linear PD with its waveforms [22].

Assuming that *Data* leads *CLK* by ΔT and latches DL1 and DL2 sample *Data* on rising and falling edges of *CLK*, DL1 produces a pulse *A* of width equal to $T_{CLK} / 2 + \Delta T$ and DL2 generates a pulse *B* of width equal to $T_{CLK} / 2 - \Delta T$.

Therefore, $A \oplus B$ produces a pulse of width ΔT for each data, indicating that output $Dif = A \oplus B$ is actually the *proportional* pulse and the circuit can indeed operate as a linear PD. In order to provide the reference pulse to complete the task of phase detection for random data, the other two latches DL3 and DL4 are required to produce pulse C and pulse D . The two waveforms are identical except for a phase difference equal to half the clock period. Thus, $C \oplus D$ produces a constant-width pulse on every data transition, serving as a reference. The two XOR gates provide both the proportional and reference pulses for every data transition. However, the Dif pulses are only half as wide as the Ref pulses. In order to obtain a zero average output from this PD when the data and the clock are locked, the amplitude of Dif outputs is scaled up by a factor of two by doubling the corresponding current source in the XOR gate [22].

The half-rate linear PDs are convenient choices when the semiconductor technology does not support a full-rate CDR because of the speed limitation. A half-rate CDR architecture will also enjoy a higher capture range. However, conventional half-rate PDs suffer from increased design complexity and their performance is dependent on the clock edge precision. The lack of inherent *full-rate* data retiming feature [22] is another issue that may further complicate the overall system design and degrade the jitter performance.

5.4 Half-rate Binary Phase Detector

A binary phase detector employing half-rate technique was reported in [23]. A simplified block diagram of half-rate binary PD and its operating principle are shown in Fig. 5.5.

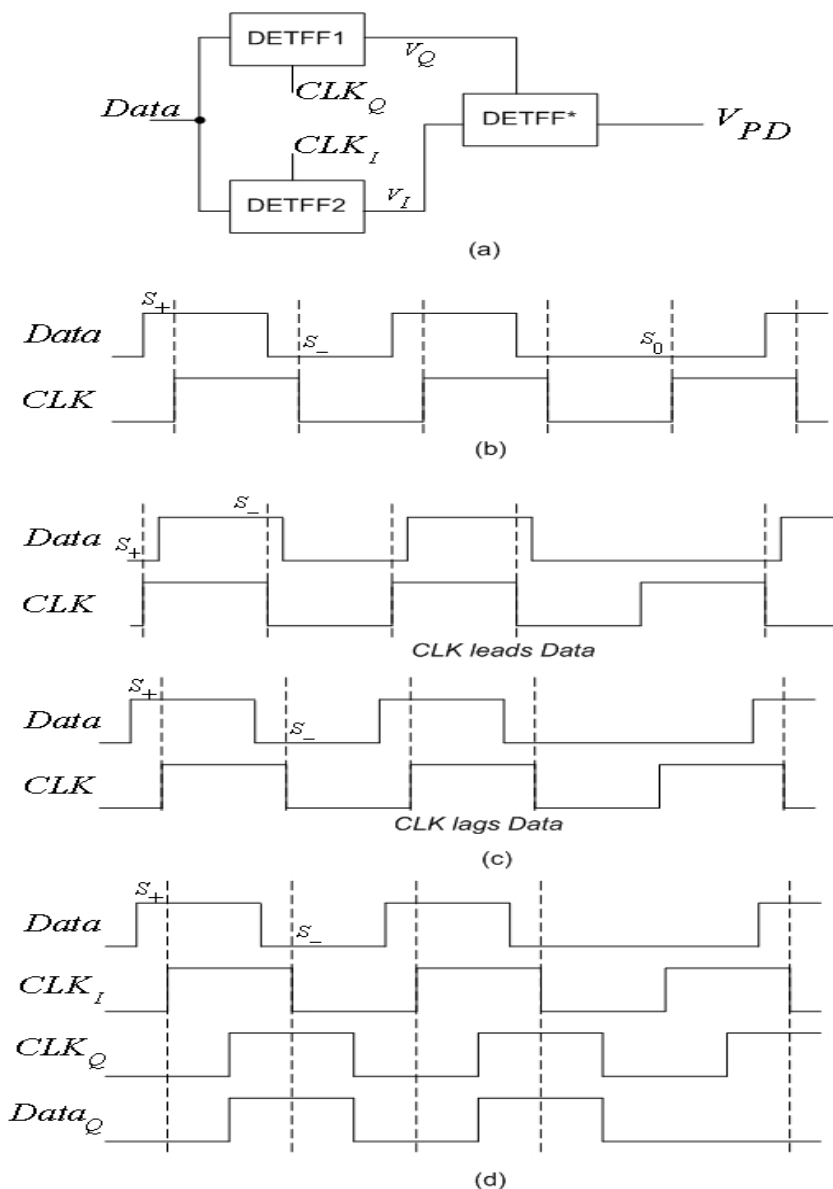


Figure 5.5. (a) A half-rate binary PD, (b) A DETFF sampling the *Data* by *CLK*, (c) S_0 samples discarded for late and early *CLK*, (d) Detecting the absence of data transition [23].

The half-rate binary PD employs three double-edge-triggered flip-flops (DETFFs) that can be formed by two latches operating on opposite clock phases along with a multiplexer [23]. Shown in Fig. 5.5.(a), *Data* input is sampled by *CLK* through a single DETFF. In Fig. 5.5.(b), three types of samples can be identified: those in the

immediate vicinity of positive data edges, S_+ ; those in the immediate vicinity of negative data edges, S_- ; and those near no data edges, S_0 . In Fig. 5.5.(c), S_+ and S_- samples are examined for *early CLK* and *late CLK*, respectively. In order to uniquely determine whether *CLK* is early or late, S_- samples are negated in DETFF*. Illustrated in Fig. 5.5.(d), *Data* input is retimed in DETFF1 by the quadrature phase of *CLK*, CLK_Q , thereby a delayed $Data_Q$ is generated. A positive transition on $Data_Q$ means an S_+ sample has already been taken; and a negative transition on $Data_Q$ means an S_- sample has already been taken. From the Fig. 5.5.(a), it can be observed that V_I output contains S_+ and S_- samples, and V_Q output serves as the retimed *Data*. DETFF* samples V_I by V_Q , negating S_- on the falling edges of V_Q . As a result, the half-rate binary PD output V_{PD} is positive if the clock is late and negative if it is early.

The well known advantages of the half-rate operation left aside, the design of this PD is more complex than a half-rate linear PD and the half-rate binary PD cannot match the full-rate architecture in terms of simplicity. Furthermore, similar to an Alexander PD, it creates significant ripple on the VCO control line and increases the jitter generation at the VCO output.

5.5 Summary

A detailed literature review on the phase detectors for random data is presented in this chapter. Major types of PDs along with their advantages and drawbacks have been described. It is noted that for the SONET OC-192 applications, it is important to have low-jitter and high-speed PDs.

The linear PDs emerge as the better-suited candidates for the phase detection task as a result of their proportional pulses, inherent data retiming, and low switching activity to satisfy the jitter requirements of the overall CDR unit that will be designed and realized in a 0.18- μm CMOS process technology.

Unfortunately, the conventional linear PDs require some innovative design techniques both at system and circuit level if they are supposed to operate reliably at frequencies that are considered marginal for this 0.18- μm CMOS process. Two such methods for enhancing the performance of the linear PDs will be described in the next chapter.

CHAPTER 6

Techniques to Improve the Phase Detector Performance

In this chapter, we are going to describe our proposed techniques to improve the performance of the phase detectors for the OC-192 applications. While the first proposal tackles the issues related to full-rate PDs, the second technique targets the half-rate PD implementations.

6.1 Hogge PD with Improved Flip-Flop

6.1.1 Circuit Design

The operation speed of 10 GHz poses significant constraints on the PD design especially when the CMOS process is not very well characterized for such boundary conditions. Therefore, new circuit techniques are essential to achieve the desired performance. A Hogge PD is opted to demonstrate the effectiveness of the proposed modification.

Theoretical advantages of the linear PDs are marred by the practical constraints that are imposed by the high-frequency parasitics and low-voltage requirements of the new generation submicron CMOS processes. Although its operation principles are well documented, the implementation of the PD is far from reaching the ideal performance when conventional circuits are used and the operation frequency pushes the process to its limits.

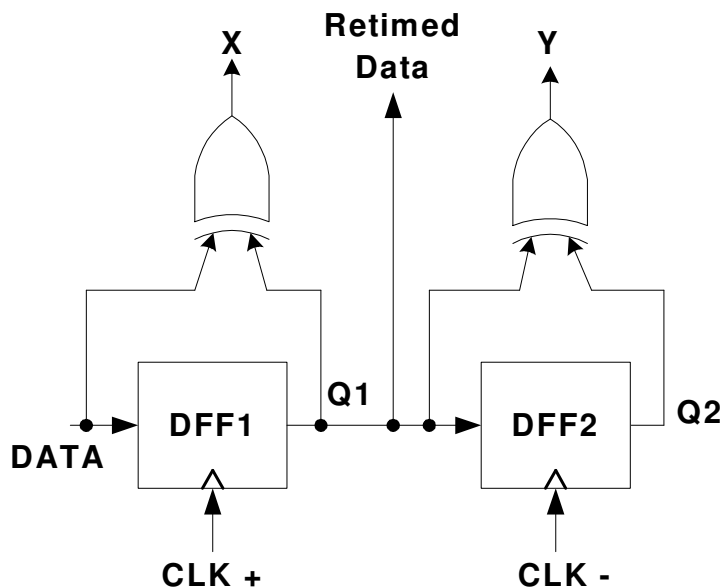


Figure 6.1. Hogge PD block diagram.

Although in this chapter we will go down to the *circuit* level, the block diagram of the Hogge PD has been included in this chapter again for completeness (Fig. 6.1). Data retiming and phase detection mainly depend on the DFF performance in a Hogge PD. The conventional flip-flops shown in Fig. 6.2 suffer from the fixed value of load resistance R_L , whereas an *adaptive* load resistance would be more appreciated in a high-frequency environment. The load resistance is supposed to change according to the sampling and latching instants: The flip-flop should exhibit a small time constant to efficiently sample the state with [M1-M2] and a large load resistance to boost the output of the latching section [M3-M4] so that the next stage can enjoy sufficient amount of voltage swing. The biasing transistor M7 further degrades the output swing since it draws some voltage headroom to provide a well-defined current to the DFF core.

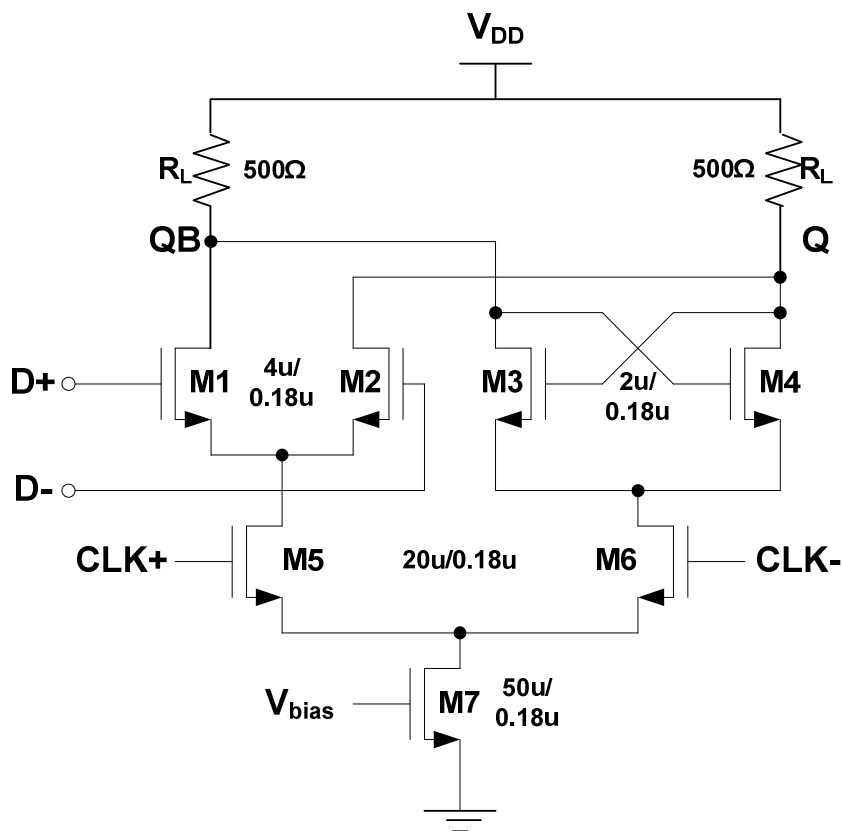


Figure 6.2. Conventional current-steering DFF core.

It is obvious from its schematic that the preferred adaptive resistance scheme cannot be applied to the conventional DFF circuit. A method to control the resistance should be employed.

Therefore, we have modified a T-flip-flop (TFF) reported in [43] to obtain a high-speed dynamic DFF that can be used to implement our PD. The operation of this DFF is based on the principle of providing the right amount of load resistance at the right time. As shown in Fig. 6.3 the modified DFF has a sampling pair (M1-M2), a latching pair (M3-M4), a pair of PMOS active loads (M5-M6), and a clock-switching transistor (M7).

In this configuration, when the CLK is high, CLKB goes low and turns on the PMOS devices, minimizing the impedance of the PMOS loads. Thus, the time constant of the capacitive network that is formed by the device capacitance and the load resistances is small at this state, enabling a fast charge up and the data sampling.

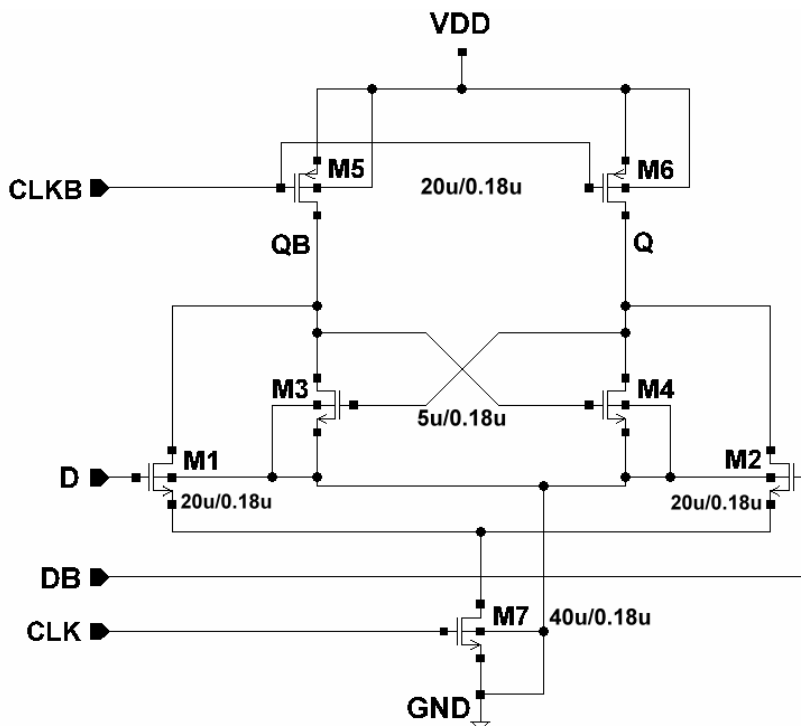


Figure 6.3. Modified DFF for high-speed Hogge PD.

Once the CLK goes low, CLKB goes high and hence the PMOS loads are in cut-off region, exhibiting high impedance to the latching pair. The signal is then transferred to the next DFF with a high voltage swing, facilitating the faster switching of these DFFs [43]. In this topology, there is no need for a biasing transistor; therefore, the low-voltage operation can be achieved easily with a 1.8-V supply.

The XOR gates are designed using the source-coupled logic (SCL) circuit family that is described in [44] (Fig. 6.4). Although their power consumption is somewhat high, these gates achieve higher speeds and produce less switching noise when compared to

the ones that are designed in static CMOS logic. Special attention has been given to the device sizes, as the amount of the parasitic capacitance of the components is inversely proportional to the operating speed of these XOR gates.

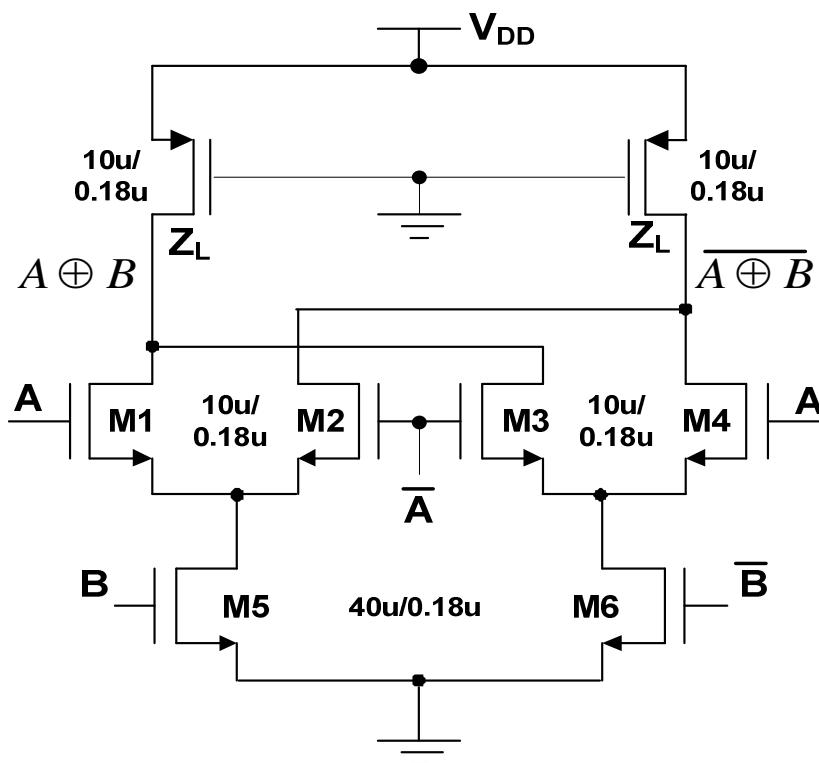


Figure 6.4. Dynamic XOR gate.

6.1.2 Simulation Results and Comparison

The Hogge PD with fast DFFs (PD-F) is designed for 10 GHz and simulated using the CHRT 0.18- μm CMOS process design kit. Another Hogge PD with conventional DFFs (PD-S) is also simulated for comparison. The operation conditions as well as the simulation settings are kept the same as much as possible. The random data pattern is obtained using a piecewise linear voltage source that allows us to define the voltage levels for different time intervals. The clock signal frequency is 10 GHz.

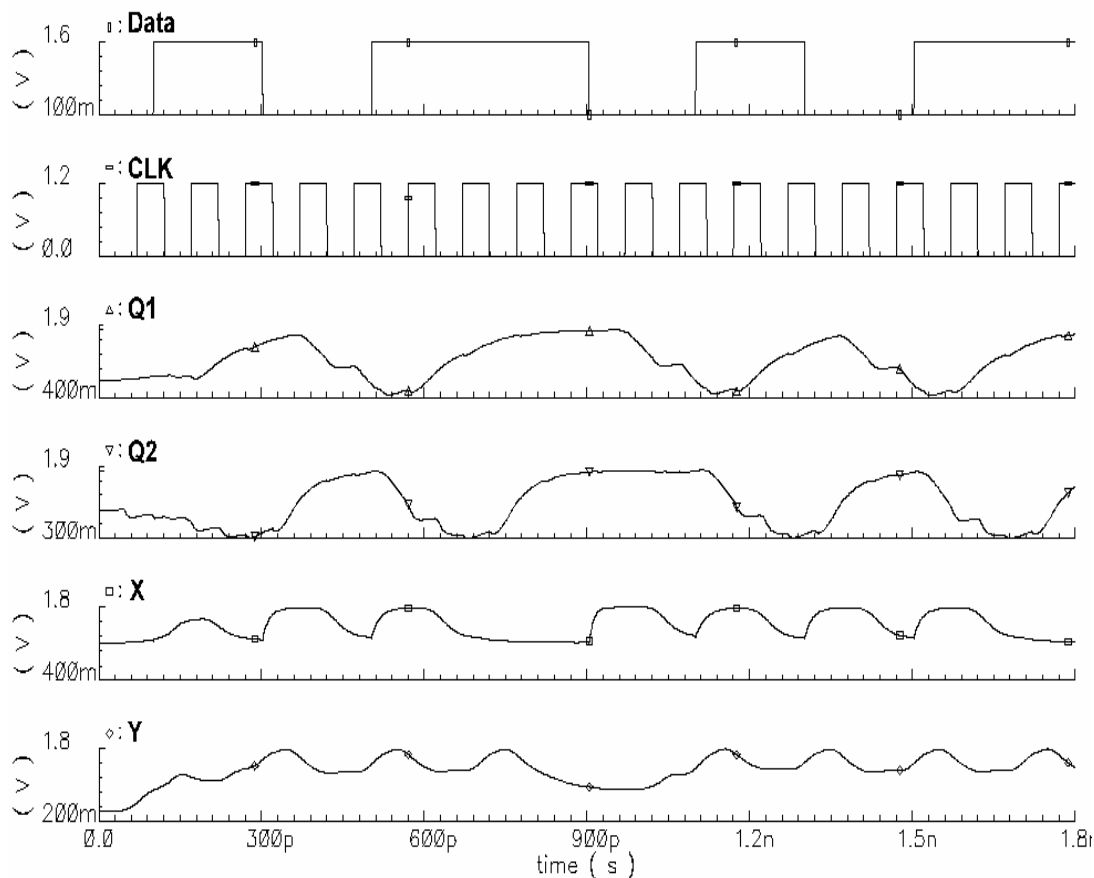


Figure 6.5. The waveforms for the Hogge PD with conventional DFFs.

The performance of the PD-S is depicted in Fig. 6.5. Due to the speed limitations of the conventional DFFs, PD-S suffers from long rise and fall times, resulting in uneven XOR gate outputs at 10 GHz. Furthermore, the output swing of 500-mV_{p-p} with a 1.4-V-dc is too low to facilitate the proper operation of the devices that are connected to these terminals. Incomplete switching in a charge pump that is following this PD-S may fail to generate or sink the required current to achieve lock in the CDR.

Fig. 6.6 illustrates the significant improvement delivered by the fast DFFs to the Hogge PD in the case of the PD-F. As can be seen from the waveforms, Q1 and Q2

outputs are well defined and the XOR gate outputs have a wide swing of $1.5 V_{p-p}$ with a dc average settling at 900 mV.

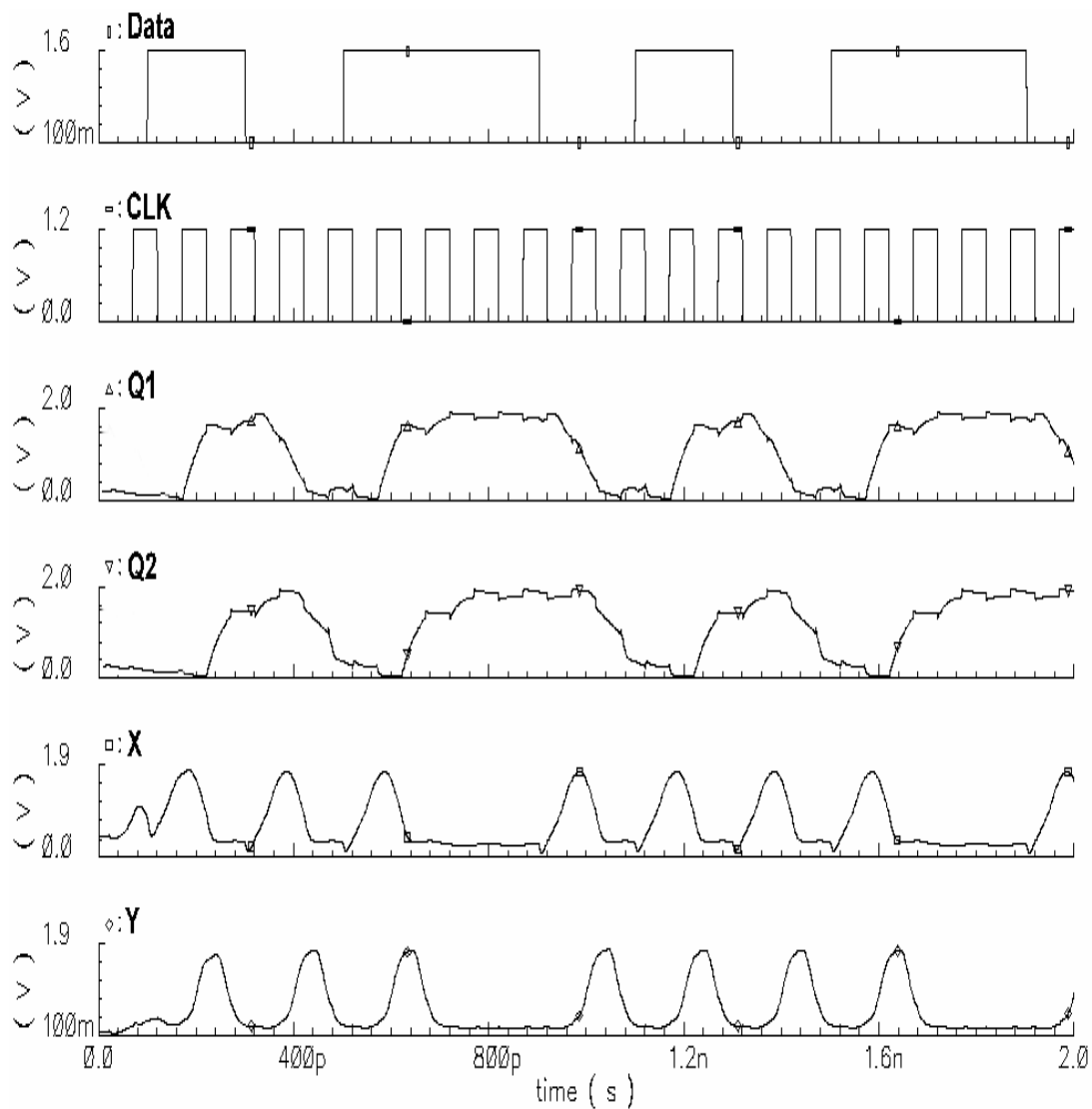


Figure 6.6. The waveforms for the Hogge PD with fast DFFs.

The net phase variations of the two designs with respect to time are compared in Fig. 6.7. The linear operation of the PD-F is clearly visible. The low and uneven phase difference output from PD-S makes it unpractical to be used in 10-GHz applications.

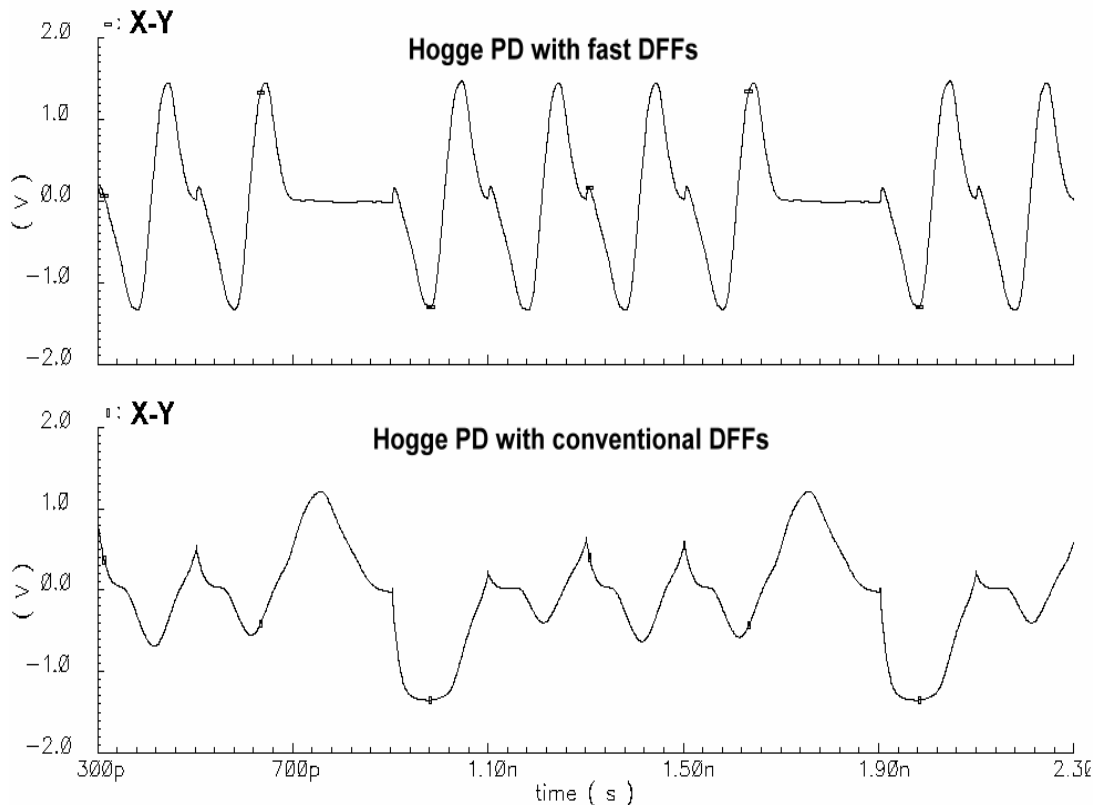


Figure 6.7. Net phase difference vs. time for the two PDs.

The simulated power consumption of the PD-S is 16.8 mW from a 1.8-V supply, whereas the power consumption for the PD-F reaches 28 mW. We have tried to equalize these two values to have a better comparison. Unfortunately, increasing the current in the PD-S has not provided any improvement in terms of the speed; in fact, it has degraded the performance. This is due to the low-voltage environment where the increased current results in high voltage drops at every component on its way to the ground terminal, leading to a low output swing. The higher power consumption of PD-F is due to its clock-switched tail transistor M7. The high peak value of the CLK turns on M7 hard and its high gate-source voltage V_{GS} leads to instantaneously high currents of 7mA. Nevertheless, the advantages offered by the fast DFF justifies its high power consumption because OC-192 systems have yet to go portable. Currently, their

priorities are speed and the jitter performance rather than the power consumption. Additionally, when compared to the recent reports on the PD designs in the literature, our PD-F has a reasonable performance in the overall perspective [19], [20], and [22]. To the best of our knowledge, our circuit is the only full-rate linear PD solution in 0.18- μm CMOS that can run with 10-GHz clock signal.

6.2 Dual-Rate Linear PD

The PD designs reported so far have one thing in common: They cannot operate in a full-rate CDR system if they are designed according to the half-rate architecture. Similarly, the same argument is valid for the full-rate PDs targeting the half-rate CDR applications [19]-[23], [36], and [38]. Therefore, to facilitate the *dual-rate* operation, either the CDR or the PD will have to go through major changes. On the other hand, a PD circuit that can work with both half-rate and full-rate CDR architectures could offer the optical receiver designers some flexibility. Thanks to the double-edge-triggered D-flip-flops (DETFs), we can design a half-rate linear PD that can perform clock recovery in a slightly modified full-rate CDR system as well.

6.2.1 Half-Rate Linear PD Architecture

Various PD designs have been reported so far [7], [20]-[23]. Being full-rate designs, [20] and [21] employ binary phase detection and provide direct extraction of the retimed data at the expense of high power consumption and high-cost SiGe BiCMOS processes. On the other hand, [22] and [23] report half-rate PDs in CMOS process with relaxed speed requirements as the low-power and low-cost alternatives to their SiGe counterparts. Based on the half-rate bang-bang phase detection principle, [7] requires an *early/late logic* circuit to determine the phase relationship between the data and the

clock signals, further complicating the design and increasing the power consumption. The design does not facilitate the data retiming within the PD and hence the additional decision circuit makes the PD prone to the systematic offset.

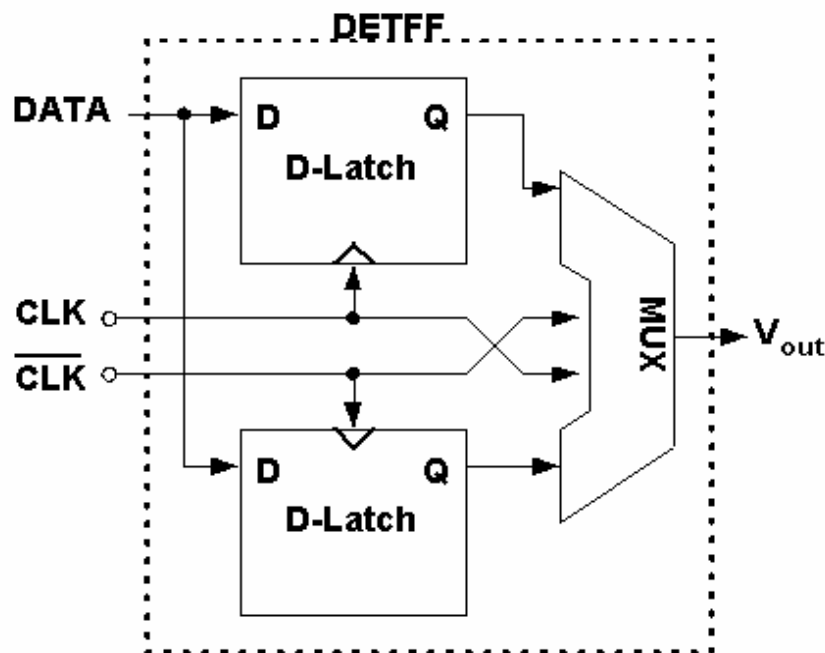


Figure 6.8. Double-edge-triggered D-flip-flop (DETFF).

We have previously seen that regardless of its type, a PD must provide two functions: *Edge detection* and *phase difference detection*. Most of the full-rate PDs incorporate single-edge-triggered flip-flops for these tasks. Unfortunately, a single-edge-triggered DFF cannot detect the data edges when clocked by a signal with frequency equal to half the data rate. If both edges of the half-rate clock are utilized to sample the data using DETFFs and the original data signal is input to an XOR gate with this sampled version, the data transitions can be detected [22]. One possible implementation of the DETFF for this task is shown in Fig. 6.8 [11].

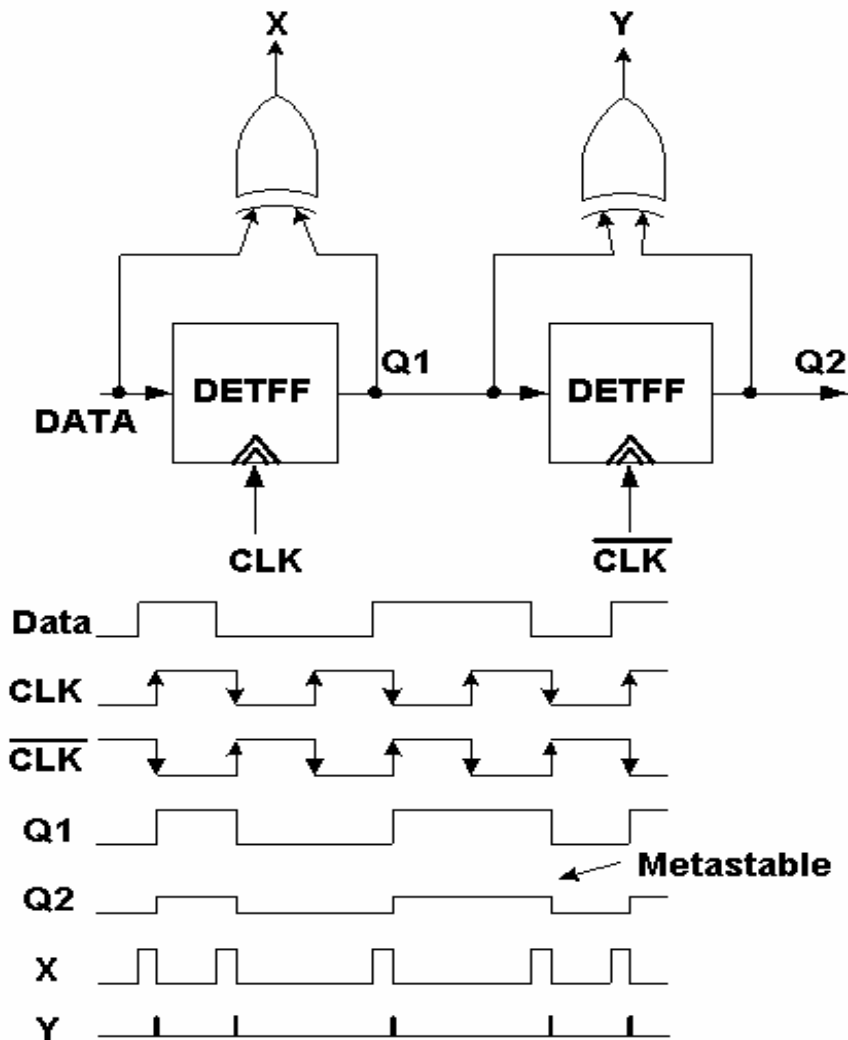


Figure 6.9. Failure of half-rate PD with single-phase clock signals.

Although the core circuit formed by the DETFF and the XOR gate can detect the data edges and generate pulses proportional to the phase difference between data and clock signals, we need to introduce another DETFF-XOR pair to provide a reference output to uniquely extract the phase error information for different data transition rates.

One might wonder whether these pairs will be able to realize half-rate phase detection when clocked by single-phase signals CLK and \overline{CLK} . Illustrated in Fig. 6.9, while the

first DETFF retimes the data with the clock signal, the metastable output of the second DETFF makes it impossible to generate a reference signal out of the second XOR gate.

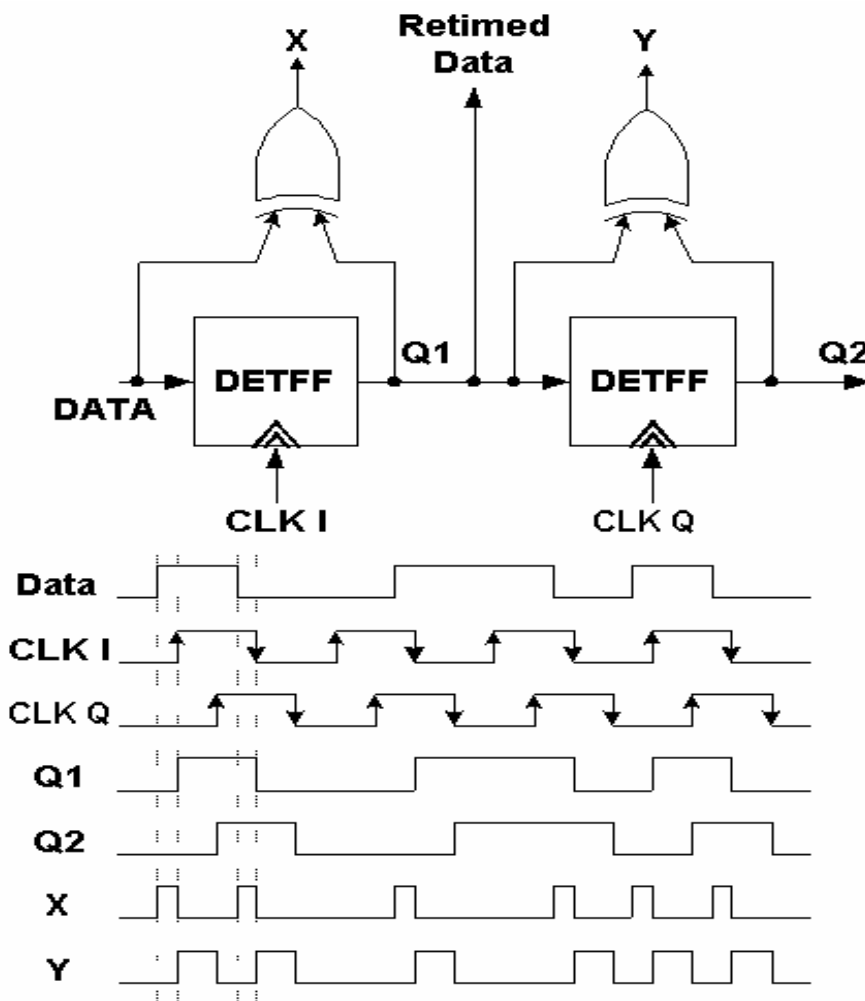


Figure 6.10. Proposed half-rate PD architecture and its timing diagram.

At this point we make an important observation: If we replace the single-phase clock inputs CLK and \overline{CLK} with quadrature phase counterparts $CLKI$ and $CLKQ$, this modification will lead us to the half-rate linear PD implementation that can successfully provide the phase error information required by the charge pump (Fig. 6.10).

The design in Fig. 6.10 obviates the need for external multiplexers or decision circuits to retime the data and hence it eliminates the systematic offset as the first DETFF output QI serves as the full-rate retimed data. Unlike the half-rate linear PD described in [22], this topology does not impose any constraint on the XOR gate dimensions in order to scale up the amplitude of the *phase error* signal with respect to the *reference* signal.

When compared to the half-rate binary PDs in [21] and [23], the proposed *linear* PD can be an attractive alternative for highly sensitive CDR applications where the ripple on the oscillator control voltage plays a significant role in the jitter generation.

6.2.2 Proposed PD in a Full-Rate CDR Configuration

The half-rate PD that is described in the previous section can easily be configured to function as a full-rate PD in a CDR with full-rate clock signal. As shown in Fig. 6.11, this CDR configuration does not require quadrature clocks. A VCO circuit with differential CLK outputs and a *divide-by-2* circuit are sufficient for full-rate operation.

Triggered by the 10-GHz VCO output CLK , the first DETFF performs the data retiming and the phase detection. The second DETFF produces metastable outputs when clocked by a 10-GHz signal and it fails to generate the reference pulses. Therefore, \overline{CLK} is passed through a *divide-by-2* circuit to obtain a 5-GHz clock signal. The waveform diagram in Fig. 6.11 clearly illustrates that QI is the recovered data and the overall PD can successfully perform the phase detection.

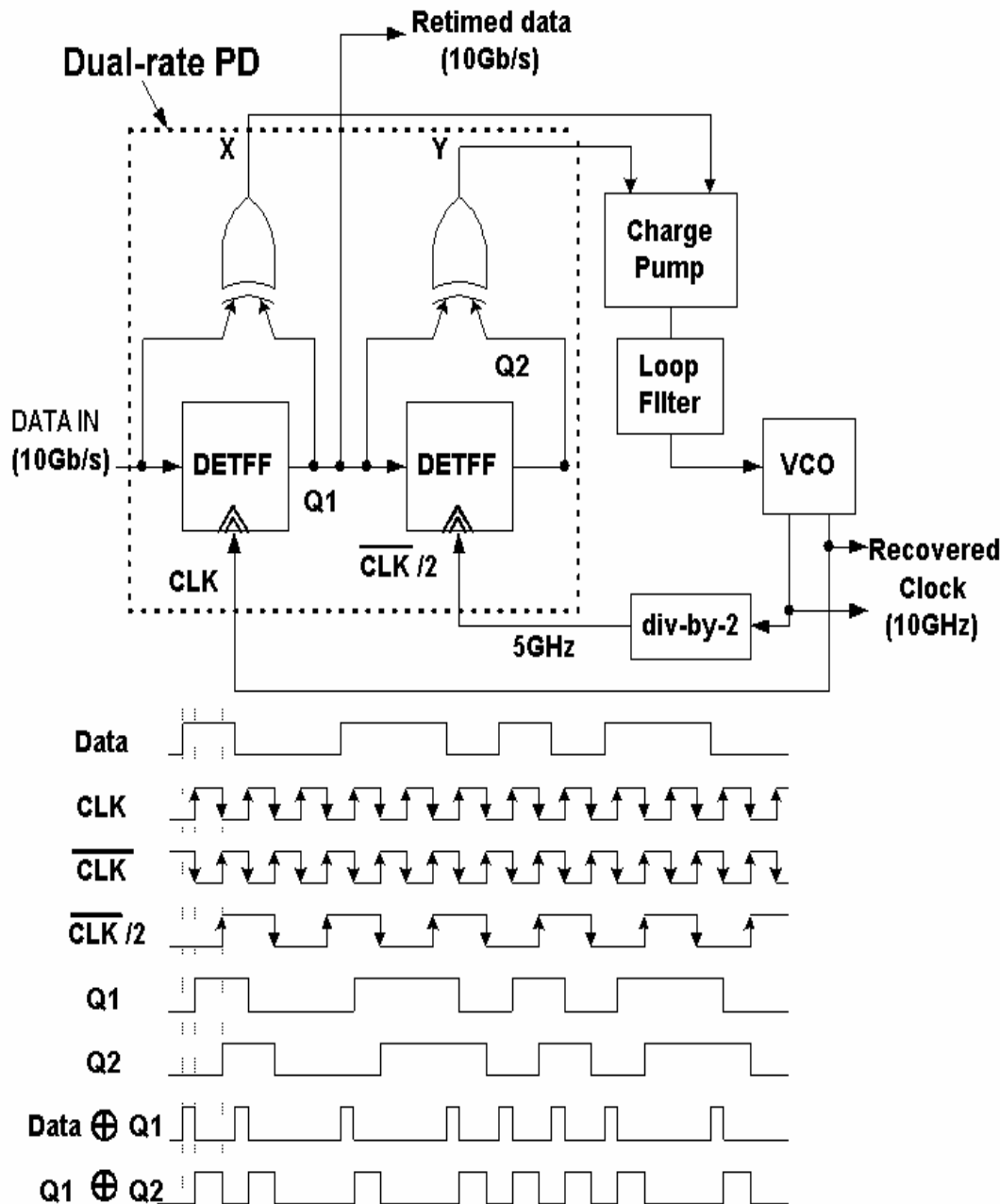


Figure 6.11. The PD and its waveforms in a full-rate CDR configuration.

The addition of a divide-by-2 circuit to the CDR system here should not be seen as a major change for it is worth the versatility offered by this configuration. We should also note that none of the previously reported PDs are capable of dual-rate operation with such slight modifications.

6.2.3 High-Frequency Circuit Design Techniques

Although the proposed PD offers a solution to the problem of ‘half-rate/dual-rate phase detection and data regeneration’ from an *architectural* point of view, a brief discussion on the issues related to its circuit design will be useful.

To eliminate the cross-talk and to improve the jitter performance, differential circuit structures should be employed throughout the design. The half-rate operation principle described in this architecture facilitates a relaxed approach to most of the issues related to the high-frequency design such as parasitic capacitance and technology limitations when compared to the full-rate architectures.

All the building blocks of the PD can be of the SCL family. The DETFF can be realized using either the conventional dynamic D-latch or the modified high-frequency DFFs. The aspect ratio of the latching pair of the D-Latch is set to be smaller than that of the sampling pair to enhance the switching speed.

The loading effect on the MUX block in the first DETFF structure requires careful current-voltage swing adjustment because its output $Q1$ serves as both the input signal for the second DETFF and the retimed data output. The 2:1 MUX that is employed in the design is shown in Fig. 6.12. The circuit employs current steering technique. With the absence of the feedback paths, it can easily achieve operation frequency of 5 GHz when designed in a 0.18- μm CMOS technology. The device dimensions of the XOR gates are carefully tuned to relax the loading effect on the DETFFs without jeopardizing their robust operation.

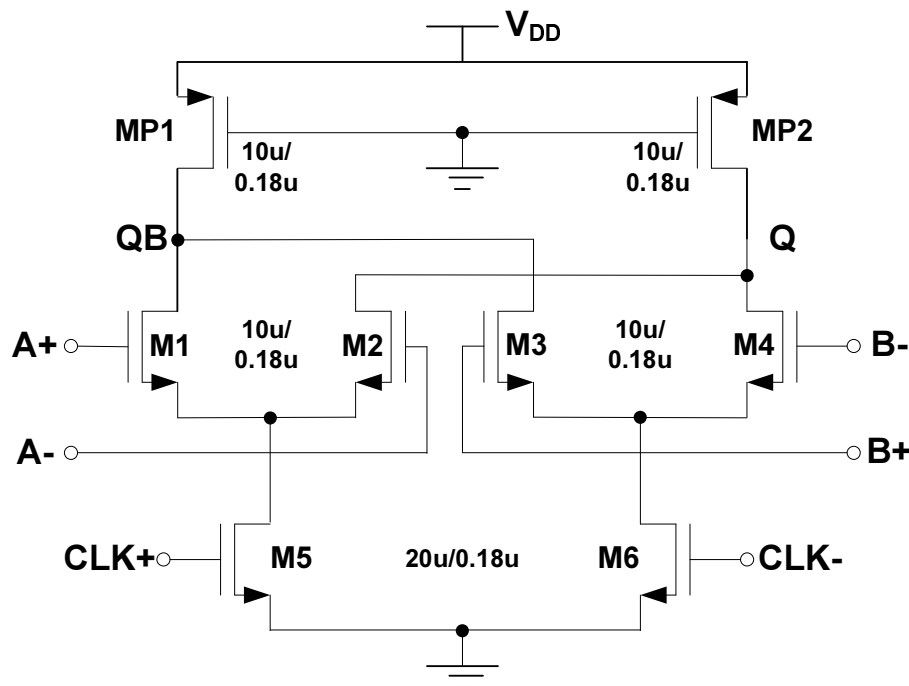


Figure 6.12. 2:1 Multiplexer.

The quadrature clock signals can be generated by RC-CR filtering [45], two stage ring oscillator [46] or a quadrature VCO [47]. These are widely used in half-rate CDR systems [7], [23], [48] and hence their design procedure is well documented in the literature [11]. However, the choice of VCO topology still depends on various trade-offs such as chip area, power budget, and jitter requirements.

6.2.4 Simulation Results for the Dual-Rate PD

In order to demonstrate its high-frequency operation capability, a circuit level implementation of the proposed half-rate linear PD is designed and simulated in 0.18- μm CMOS process with a typical 10-Gb/s NRZ random data input. The layout of the proposed PD is drawn to extract the parasitic effects for the circuit simulation. Fig. 6.15 shows the PD core layout with a size of 130 μm x 160 μm , making this

design a low-cost alternative to other PDs with higher device count and larger silicon space [7].

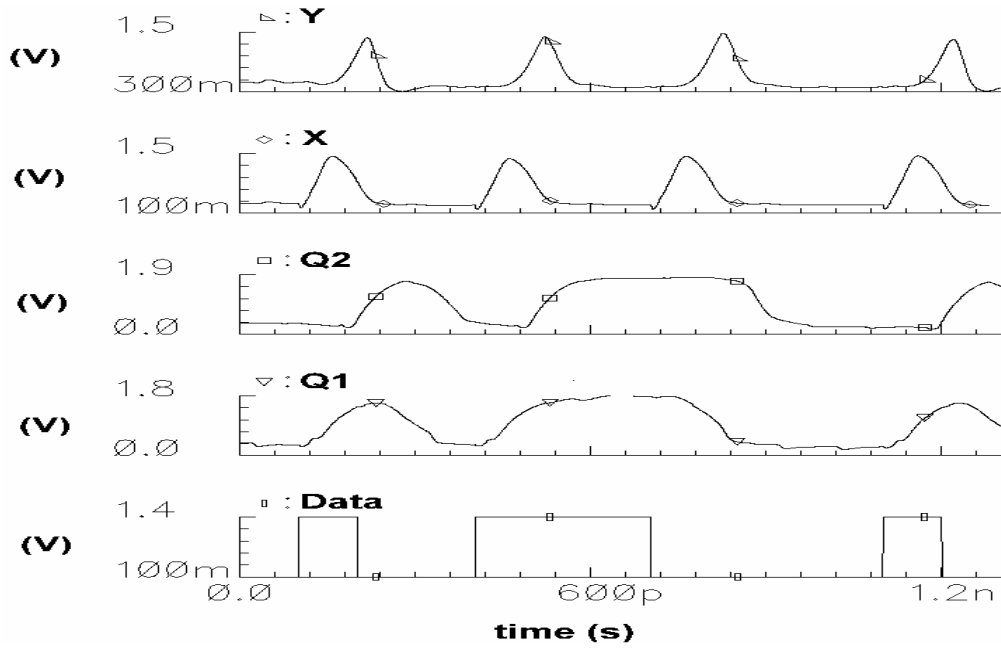


Figure 6.13. PD output for 10-Gb/s random data after pre-layout simulation.

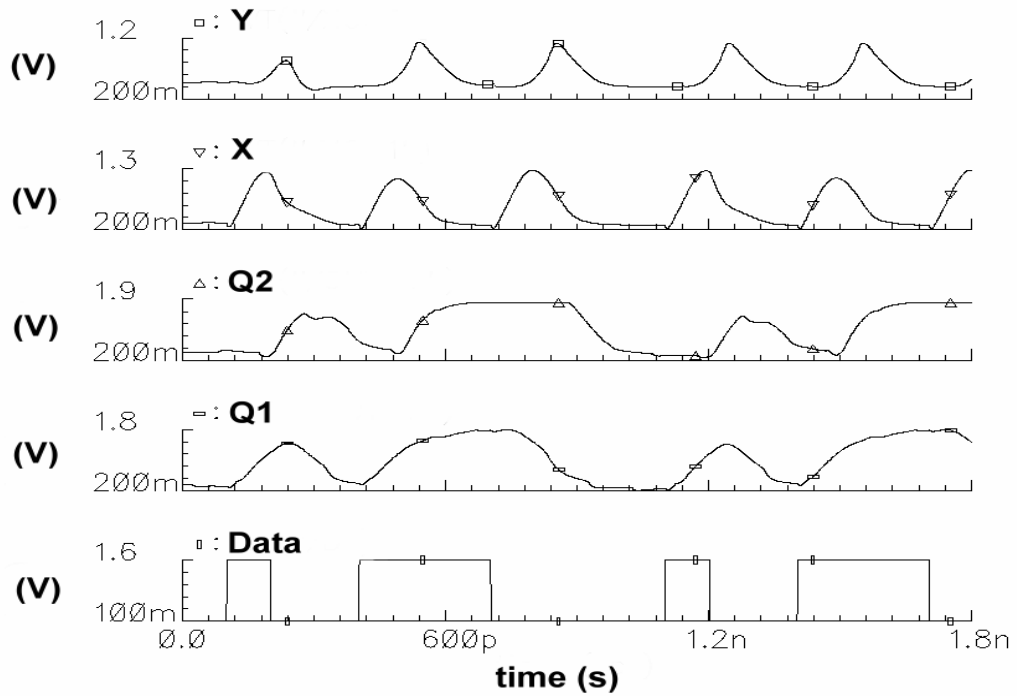


Figure 6.14. PD output for 10-Gb/s random data after post-layout simulation.

The simulations are carried out for both pre-layout and post-layout cases to examine the effects of the parasitics on the circuit. The respective PD outputs are presented in Fig. 6.13 and Fig. 6.14.

The retimed data QI and the proportional phase difference X along with the reference pulse Y can be clearly observed in both graphs. However, the parasitic effects on the rise and fall times of the signals as well as the amplitude of the voltage swings are clearly visible in Fig. 6.14. This is due to the capacitive loading at the first DETFF output. Nonetheless, the PD can successfully detect the phase difference and provide the necessary output to the next building block in the system. The total power consumed by the circuit is 27 mW from a 1.8-V supply.

It is worth mentioning that this work focuses on the architecture of the new PD; therefore, the simulation results presented in this section are process dependent and may not reflect the entire capabilities of the proposed architecture. The comparison of the half-rate linear PD design with the existing PDs is presented in Table 6.1.

Table 6.1. Comparison of existing designs with the proposed PD.

PD Parameters	[22]	[23]	[7]	THIS PD
<i>Type</i>	linear	early/late	early/late	linear
<i>Data retiming</i>	with extra MUX	direct output	with extra decision circuit	direct output
<i>Clock frequency</i>	5 GHz	5 GHz	5 GHz	5 GHz
<i>Power supply</i>	1.8 V	1.8 V	1.8 V	1.8 V
<i>Power dissipation</i>	33 mW	42 mW*	N/A	27 mW
<i>Technology</i>	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS

* This value includes the additional frequency detection circuit as well.

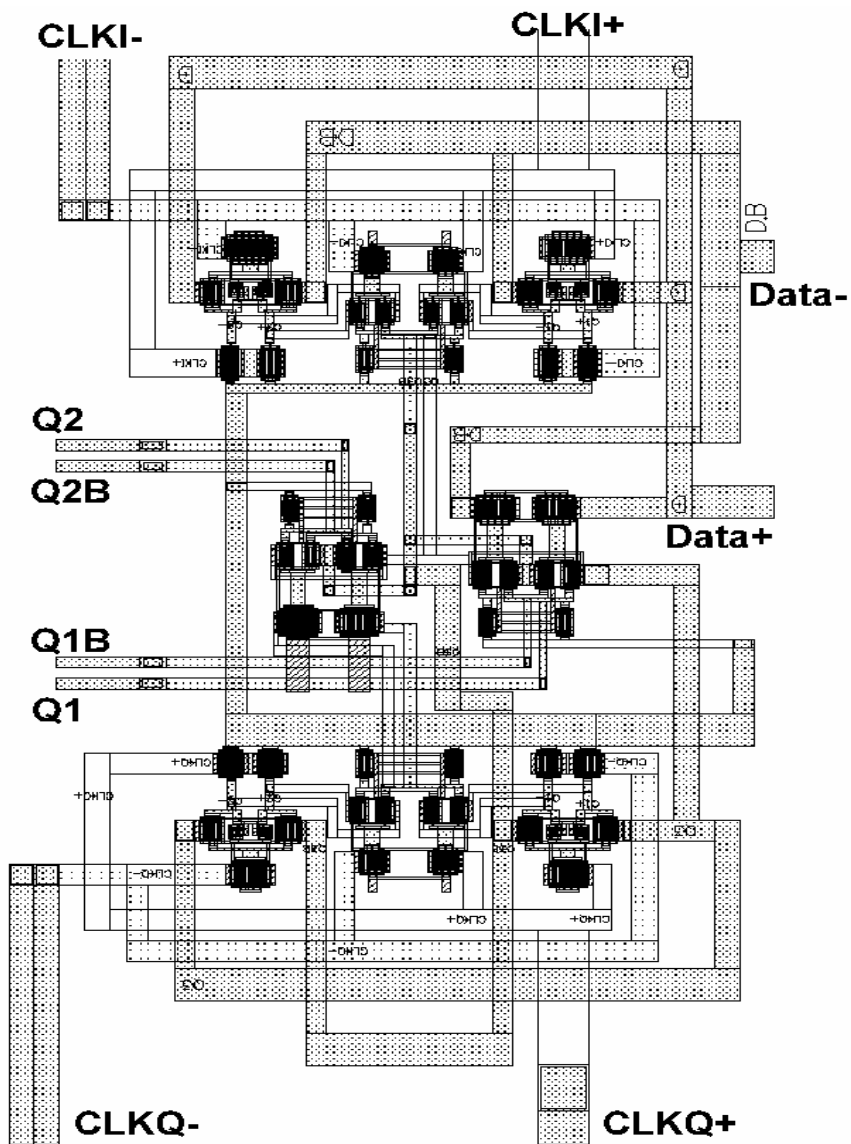


Figure 6.15. Layout of the proposed PD.

6.3 Summary

Despite the aggressive device scaling in CMOS technology, the CDR circuits that are realized in CMOS processes still face significant speed and high-frequency design speed challenges. When it comes to complying with the stringent requirements posed by the optical communication standards and SONET applications, CMOS circuits have

to *work harder* than its GaAs or SiGe counterparts to overcome the limitations that are caused by the high-frequency parasitics. Therefore, an increase in the popularity of the half-rate CMOS CDR architectures is expected.

A half-rate/dual-rate linear PD architecture is described in this chapter. It retimes the data without any additional decision circuit and hence it minimizes the systematic offset. Thanks to the DETFFs, the half-rate linear PD described here can perform clock recovery in a slightly modified *full-rate* CDR system as well. To the best of our knowledge, this is the only PD architecture that facilitates the *dual-rate* operation.

The power consumption is 27 mW from a 1.8-V supply and the layout size of the core circuit is 130 μm x 160 μm . With its small size and low power consumption, this PD can be easily fit into a fully integrated CDR unit. Being a dual-rate design, the proposed architecture can offer an attractive solution for the applications targeting high-bit-rate SONET systems such as OC-192 or OC-768 (40-Gb/s).

CHAPTER 7

A Fully Integrated 10-Gb/s CMOS Clock and Data Recovery Circuit

We have described the major building blocks of a typical clock and data recovery circuit in the previous chapters. Several important improvements and innovative modifications to the conventional circuits have been developed for these blocks. The effects of these modifications to the individual blocks are illustrated subsequently in the relevant chapters throughout the thesis. Now it is time to investigate their collective performance in a CDR formation.

For this purpose, a fully integrated 10-Gb/s CDR circuit is designed and fabricated in CHRT 0.18- μm CMOS process. A full-rate architecture is employed along with a new loop filter topology facilitating full integration of the CDR circuit.

Up to date, no OC-192 CDR has been reported to have fully integrated structure. The loop filters employed in those designs in order to satisfy the stringent SONET requirements suffer from bulky capacitors that prove too large to be implemented on-chip and hence it results in the use of external components for the loop filters. We hope that our design will introduce new insights to the monolithic CDR implementations.

7.1 CDR Architecture

As shown in Fig. 7.1, in a typical CDR the phase detector compares the phase of the data input with the phase of the clock signal generated by the VCO. The data retiming is performed in the PD block as well. The phase comparison generates the phase error information, which is then sent to the charge pump where appropriate amount of current is pumped into or out of the loop. The current is then filtered and converted to a voltage value by a loop filter in order to generate the VCO control voltage to correct the phase error.

Our focus in this project is mainly investigating the feasibility of a full-rate CDR in 0.18- μm CMOS process, where it is claimed the opposite [22], [23]. Although the device scaling and the CDR implementations in recently introduced technologies continue as aggressively as usual [49]-[51], making use of the *rather outdated* versions of the CMOS technology for 10-Gb/s CDR design can provide low-cost solutions and efficient use of the resources at hand. Therefore, we have opted for the CDR architecture shown in Fig. 7.1 to demonstrate the effectiveness of the proposed modifications.

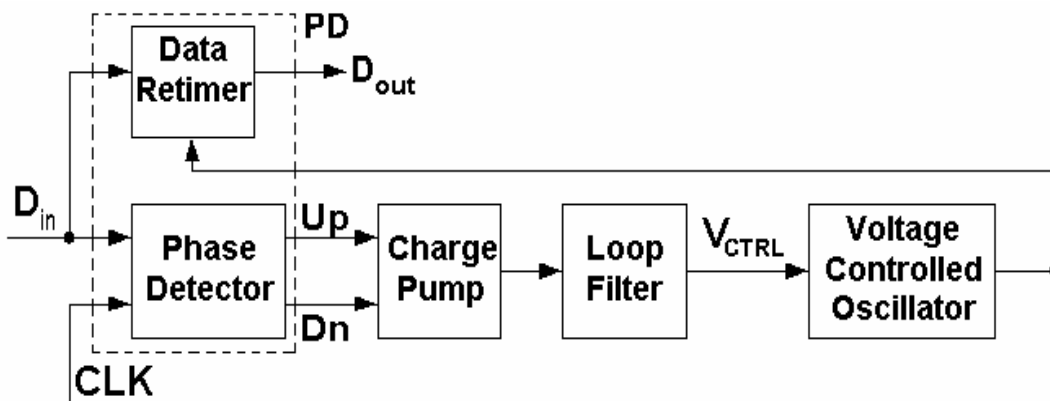


Figure 7.1. Typical CDR architecture.

7.2 Building Blocks

7.2.1 Phase Detector and Charge Pump

The modified Hogge PD described in Chapter 6 is employed as the linear PD of choice here. A simplified schematic of this PD is shown in Fig. 7.2. The circuit is fully differential and hence it minimizes the risk of cross-talk that might degrade the high-frequency performance of the CDR unit.

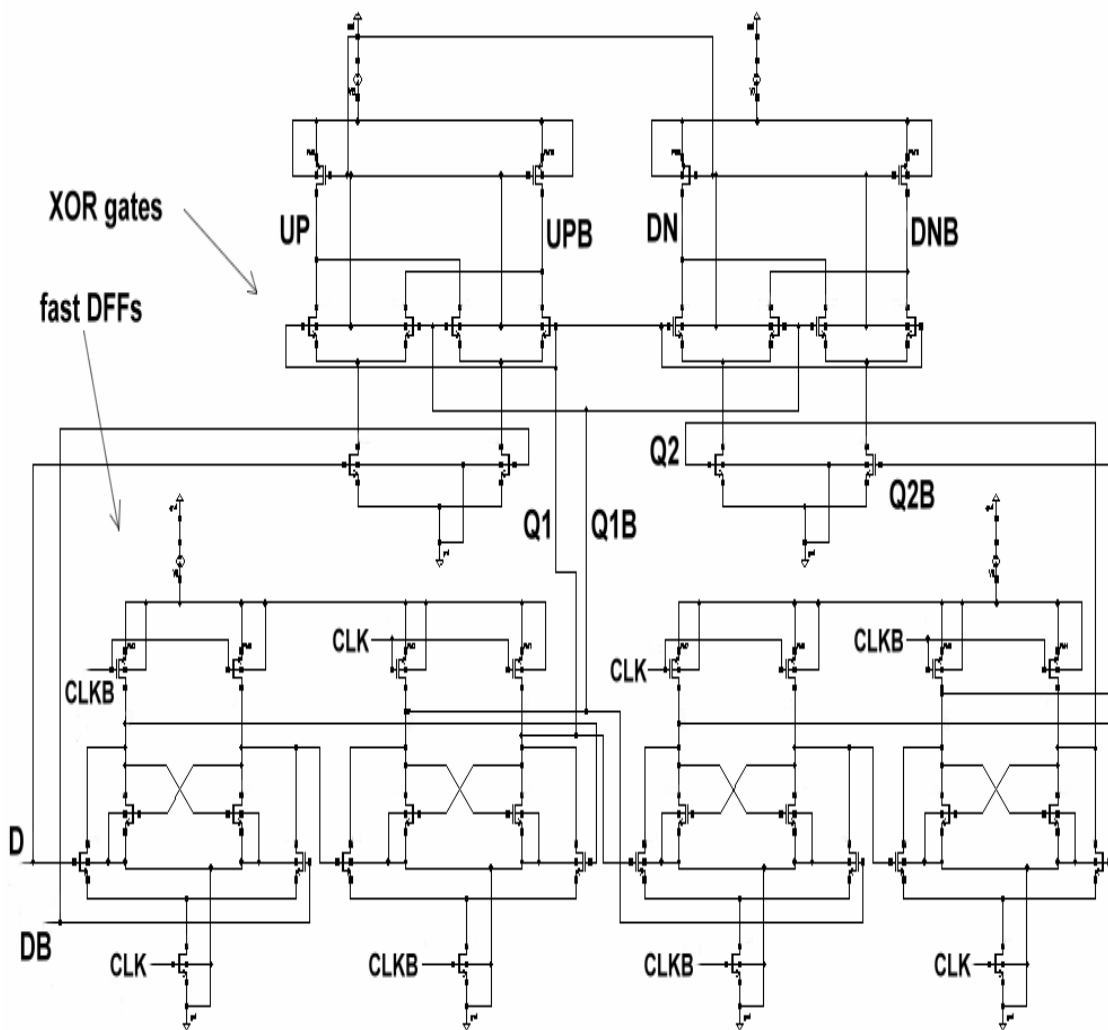


Figure 7.2. Hogge PD with fast DFF.

The retimed data is obtained from the Hogge PD via output buffers (Fig. 7.3).

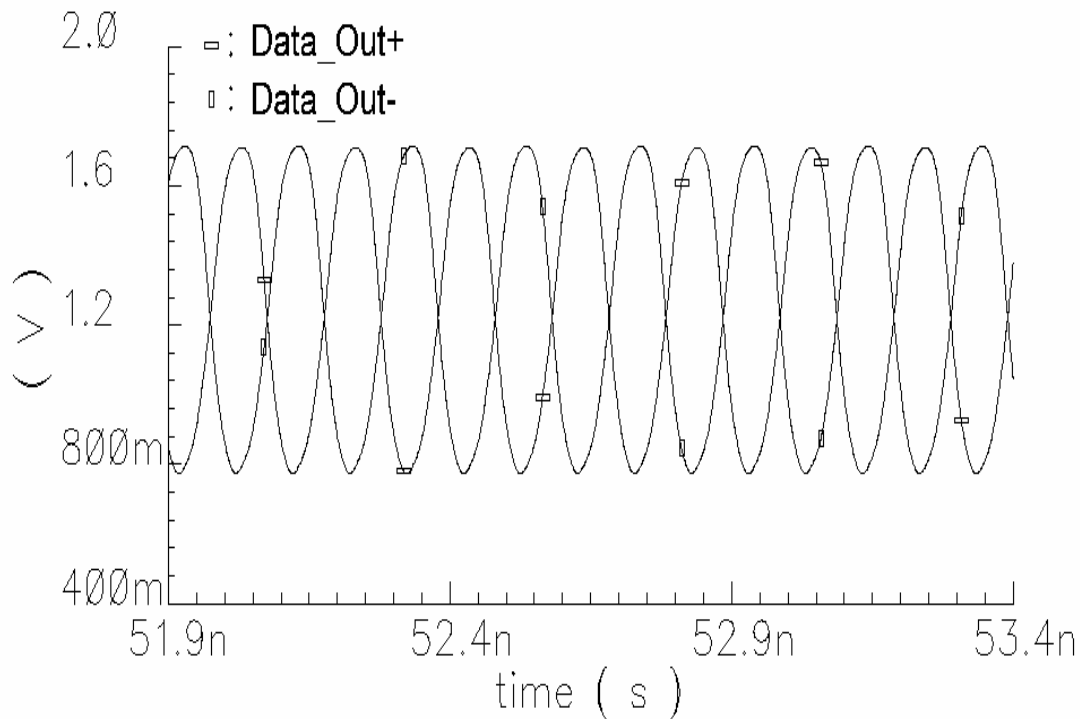


Figure 7.3. The recovered data for a typical 10-Gb/s input.

A differential-input single-ended-output charge pump topology is dictated in the CDR unit by the single-ended nature of the control mechanism of the VCO circuit. As shown in Fig. 7.4, the charge pump incorporates PMOS [M3-M4]/NMOS [M1-M2] pairs for pumping/sinking current to/from the loop so that the VCO receives the proper control signal in order to lock the phase. The current steering technique in this charge pump facilitates the high-speed operation [52]. Furthermore, the high operation frequency dictates the use of minimum-length devices in order to achieve fast switching. The existence of both PMOS and NMOS devices in the circuit requires attention to the sizing of these devices so as to minimize the current mismatch and hence the phase offset. Fortunately, the phase offset can be tolerated in a CDR unit contrary to the case where they may produce significant disturbance in a frequency synthesizer [52].

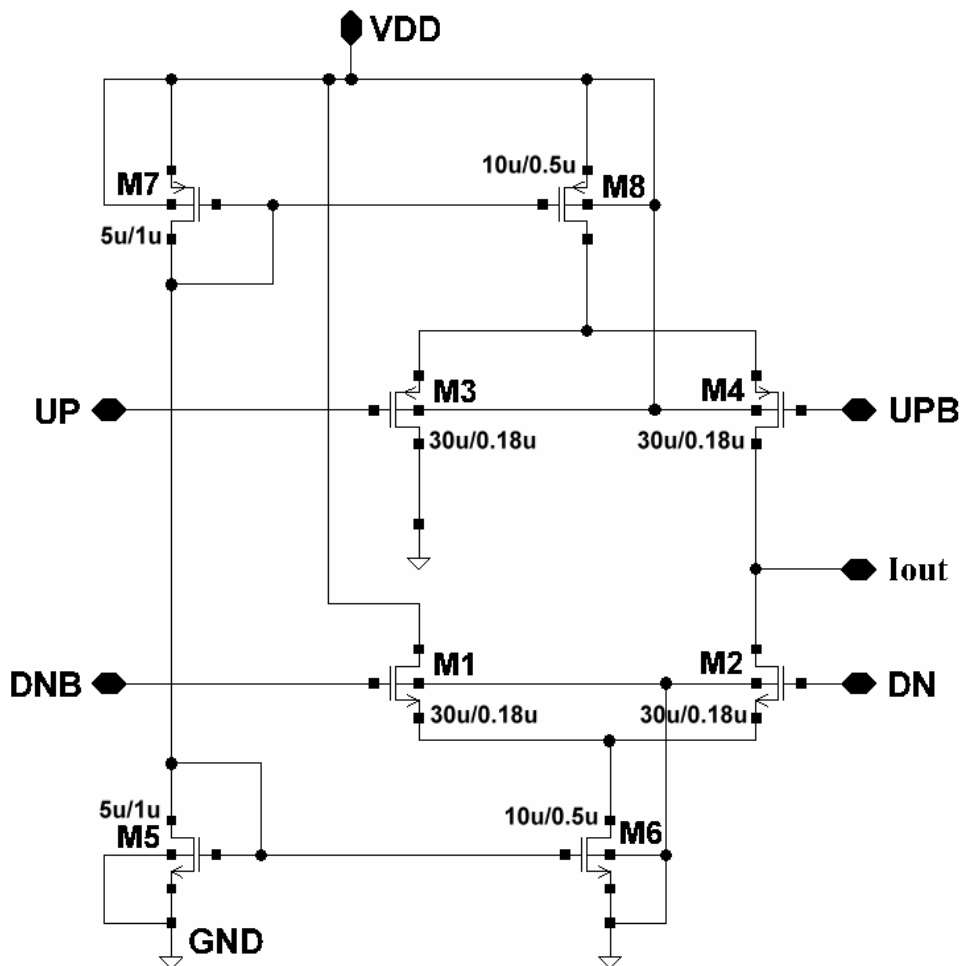


Figure 7.4. Charge pump circuit.

The UP and DN signals are provided by the differential PD described above. When the data is ahead of the clock, the UP and DN signals are logic '1' and logic '0', respectively. This will turn M4 on and the mirrored current can now flow following the path $M8 \rightarrow M4 \rightarrow I_{out}$ to the loop filter. Similarly when the clock is leading the data, M2 will be turned on and the current will be pumped out of the loop via $I_{out} \rightarrow M2 \rightarrow M6$ to the ground terminal. M3 and M1 are included in the schematic to accommodate the differential PD outputs. The simulated power consumption of this circuit does not exceed 2 mW from a 1.8-V supply.

7.2.2 Integrated Loop Filter

Because of their switching nature, the charge pump circuits generate ripples that can disturb the VCO control voltage and hence degrade the jitter performance of the CDR. To reduce these ripples, loop filters are added to the control line. There are two types of loop filters: *active* and *passive*.

An *active filter* is comprised of operational amplifiers (op-amps), capacitors, and resistors. It is used to generate a tuning voltage higher than what a charge pump circuit can provide. This high output voltage is crucial for tuning the VCO in wideband applications such as frequency synthesizers. Because of the active devices in their structure, active filters introduce noise to the loop. Furthermore, the op-amp speed limits its operation range to the frequencies that are much lower than 10 GHz.

The *passive filter*, on the other hand, has the advantages of reduced noise, lower circuit complexity, and -relatively- no speed limitation. Formed by resistors and capacitors, they are used as the charge pump loads to generate the control voltage proportional to the phase error.

The choice of the loop filter depends mainly on the jitter requirements of the CDR. Typical LPF topology that has been used in many PLL and CDR applications is shown in Fig. 7.5. The analysis of the PLL employing this type of filter was presented in Chapter 3.

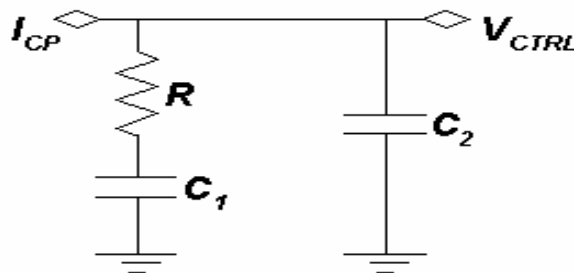


Figure 7.5. Loop filter, type-II 2nd-order.

I_{CP} and V_{CTRL} represent the charge pump output and the VCO control voltage input ports, respectively. Unfortunately, this filter is not suitable for the fully integrated CDR applications because the bandwidth specifications of the systems result in bulky off-chip capacitors in this topology [20]-[23], [27]-[29].

A parallel combination of the resistor-capacitor (RC) components is employed in our design to facilitate the integration of the loop filter into the chip (Fig. 7.6.).

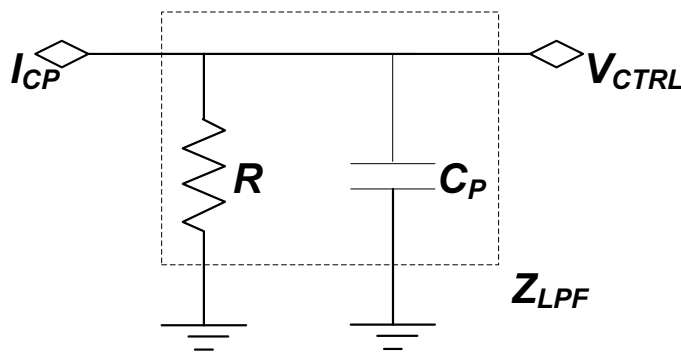


Figure 7.6. Integrated loop filter.

The linear model of the CDR architecture resulting from this modification is presented in Fig. 7.7. We should note that the loop bandwidth, which is on the order of megahertz, is negligibly small compared to the input frequency of 10 GHz and hence the state of the circuit changes by a small amount on each cycle of the input signal, permitting the use of the simple transfer functions for the analysis [17].

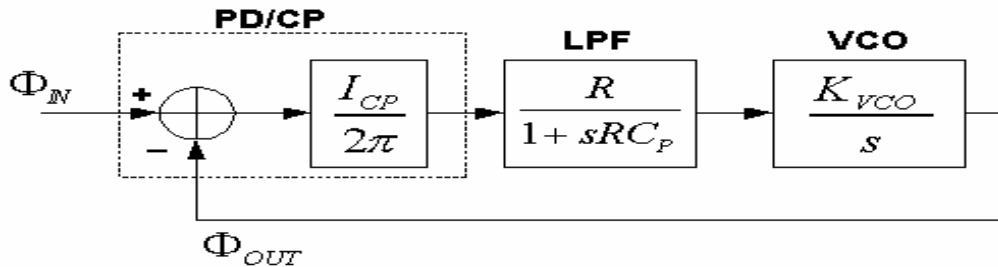


Figure 7.7. Linear model of the CDR.

The open loop transfer function of the input and output phases can be written as:

$$\frac{\Phi_{OUT}}{\Phi_{IN}}(s) |_{OPEN} = \frac{I_{CP}}{2\pi} \cdot \frac{R}{1 + sRC_P} \cdot \frac{K_{VCO}}{s} = G(s) \quad (7.1)$$

where K_{VCO} is the VCO gain in rad/s/V. The closed-loop transfer function can then be derived from:

$$H(s) = \frac{G(s)}{1 + G(s)} \quad (7.2)$$

as

$$H(s) = \frac{I_{CP} \cdot K_{VCO} \cdot R}{2\pi \cdot RC \cdot s^2 + 2\pi \cdot s + I_{CP} \cdot K_{VCO} \cdot R} \quad (7.3)$$

If we rewrite (7.3) so that it looks like the control theory transfer function

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n \cdot s + \omega_n^2} \quad (7.4)$$

We obtain the final form

$$H(s) = \frac{\frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot C_P}}{s^2 + \frac{1}{RC} \cdot s + \frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot C_P}} \quad (7.5)$$

Using (7.4) and (7.5), we define the natural frequency ω_n and the damping factor ζ for this CDR loop as:

$$\omega_n = \sqrt{\frac{I_{CP} \cdot K_{VCO}}{2\pi \cdot C_P}} \quad (7.6)$$

and

$$\zeta = \frac{1}{2R} \sqrt{\frac{2\pi}{I_{CP} \cdot K_{VCO} \cdot C_P}} \quad (7.7)$$

The two poles of the closed-loop system are also calculated from the denominator of (7.4) as

$$s_{1,2} = \left(-\zeta \pm \sqrt{\zeta^2 - 1}\right) \cdot \omega_n \quad (7.8)$$

The foregoing analysis reveals some interesting details:

The open-loop transfer function indicates that there is one pole at the origin, making the loop a Type-I PLL. The closed-loop transfer function, on the other hand, has a 2nd-degree polynomial at its denominator and hence we call this CDR a 2nd-order loop. Unlike the filter structure given in Fig. 7.5, the integrated filter does not employ a series R-C connection. Therefore, the charge pump current passing through the filter does not introduce significant ripples to the VCO control line and hence the addition of an extra capacitor to the filter structure for suppressing the ripples is avoided. Furthermore, this feature of the filter enhances the stability by preserving the Type-I 2nd-Order nature of the PLL. Equation (7.8) indicates that for $\zeta > 1$, the two poles are real and the stability of the loop is well maintained for this condition.

When compared to the conventional Type-I PLL structure without the charge pump [11], this 1st-order filter requires smaller R and C values to achieve the desired ω_n and ζ so that the peaking in the jitter transfer function and the settling time are minimized.

The circuit implementation of the filter shows that both C_P and R are below 20 pF and 500 Ω , respectively. These values are relatively easier to achieve using on-chip components and hence the CDR can be designed as a single chip circuit, obviating the need for external passive components.

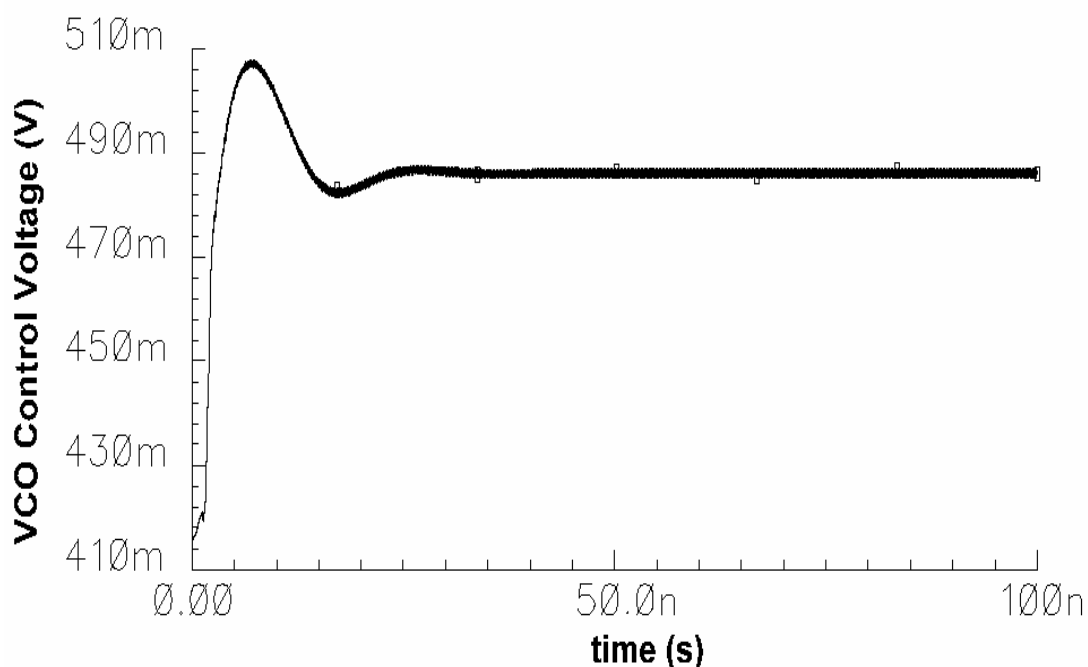


Figure 7.8. Locking characteristics of the loop.

For our design, the charge pump current is set to be 300 μA . The resulting natural frequency and the damping factor are 12.32 MHz and 1.29, respectively. These values are in good agreement with the existing CDR designs [19]-[23]. The post-layout simulation result of the typical locking behaviour of the loop is shown in Fig. 7.8.

7.2.3 10-GHz VCO

The clock signal for this CDR is obtained from the 10-GHz VCO circuit described in Chapter 4 [53]. Making use of the dependency of the VCO tuning range on the supply voltage, the VCO is biased with a 1.6-V supply so as to exhibit a VCO gain of

200 MHz/V for this application. Having a low VCO gain improves the ripple immunity of the control voltage and enhances the CDR phase noise performance.

The post-layout simulated recovered clock is shown in Fig. 7.9. The CLK swing is sufficient to switch the PD devices. The symmetrical swing is obtained by careful analysis of the parasitic capacitances extracted from the layout.

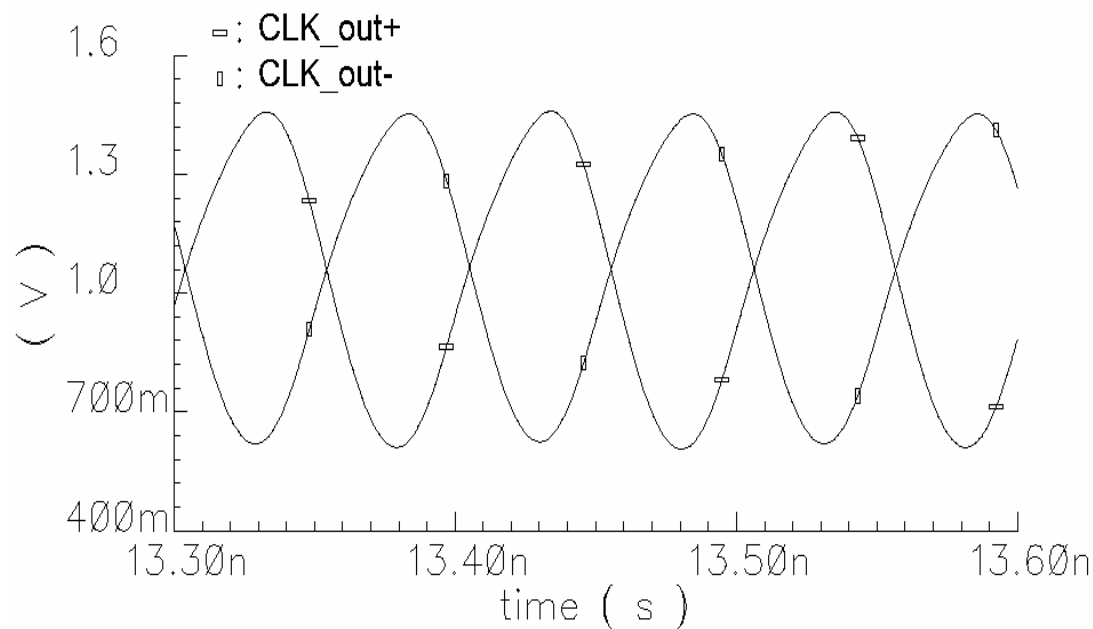


Figure 7.9. The recovered clock output at 10 GHz.

7.3 Jitter Analysis of the Designed CDR

7.3.1 Jitter Transfer Function

The preferred jitter transfer function of a PLL is similar to its input-output transfer characteristics: For small and slow variations of the jitter (i.e., low-frequency jitter) that is accompanying the input signal, the PLL in the CDR should be able to track the variations at the zero crossings of the signal to maintain the phase lock. If the jitter varies rapidly (i.e., high-frequency jitter), the PLL should not get carried away with it

and it should filter out these high-frequency components as much as possible to avoid distraction from the phase-locked state.

Using the transfer function of this CDR given in (7.5) and the substitution $s_0 = j \cdot \omega_{-3dB} = j\omega_0$, we can calculate the -3-dB bandwidth:

$$\left| \frac{\omega_n^2}{s_0^2 + 2 \cdot \zeta \cdot \omega_n \cdot s_0 + \omega_n^2} \right| = \frac{|\omega_n^2|}{|s_0^2 + 2 \cdot \zeta \cdot \omega_n \cdot s_0 + \omega_n^2|} = \frac{\sqrt{2}}{2} \quad (7.9)$$

and hence

$$\frac{\omega_n^4}{(-\omega_0^2 + \omega_n^2)^2 + (2 \cdot \zeta \cdot \omega_n \cdot \omega_0)^2} = \frac{1}{2} \quad (7.10)$$

After expanding the parentheses and some manipulation, we will get the following expression:

$$\omega_0^4 - 2 \cdot \zeta \cdot \omega_n^2 \cdot (1 - 2\zeta^2) \cdot \omega_0^2 - \omega_n^4 = 0 \quad (7.11)$$

This expression can be easily converted to a quadratic equation and solved using the substitution $t = \omega_0^2$, giving the general formula for the -3-dB bandwidth frequency as

$$\omega_{-3dB}^2 = \omega_0^2 = \omega_n^2 \cdot \left[(1 - 2\zeta^2) + \sqrt{2 - 4\zeta^2 + 4\zeta^4} \right] \quad (7.12)$$

ω_n and ζ determine the -3-dB bandwidth. Remember from (7.5) and (7.8) that $\zeta > 1$ should be satisfied in order to enhance the PLL stability. A ζ value that is greater than 1 will ensure that the roots do not deviate from the real axis, a case where the stability of the loop is threatened [11], [17], and [18]. One might suggest that we increase the damping ratio to address this issue. In fact this method is used in most of the Type-II CDRs where $\zeta \cdot \omega_n$ is maximized at the expense of bulky off-chip

capacitors. Unfortunately, rewriting (7.12) as in (7.13) indicates that we cannot increase the ζ indefinitely in our case:

$$\omega_{-3dB}^2 = \omega_n^2 \cdot \left[(1 - 2\zeta^2) + \sqrt{(2\zeta^2 - 1)^2 + 1} \right] \quad (7.13)$$

and for $2\zeta^2 \gg 1$, (7.13) can be simplified as:

$$\omega_{-3dB}^2 = \omega_n^2 \cdot \left[(1 - 2\zeta^2) + (2\zeta^2 - 1) \right] = 0 \quad (7.14)$$

Based on the foregoing analysis, we can conclude that the -3-dB bandwidth of the jitter transfer function is inversely proportional to the filter resistor R and capacitor C_p. Therefore, the loop filter can be designed to have a small bandwidth as long as it does not jeopardize the PLL stability. Contrary to the conventional filter topologies in use, this can be achieved without making the filter capacitor exceptionally large, facilitating the concept of fully integrated CDR systems in CMOS.

As an illustrative example, remember that the natural frequency and the damping ratio are given in the previous section as 12.32 MHz and 1.29, respectively. Then the resulting -3-dB frequency is calculated from (7.12) to be 5.57 MHz. This is further verified by the MATLAB plot of the transfer function shown in Fig. 7.10. Although this value is apparently in conflict with the jitter transfer bandwidth requirement of 120 kHz, the large bandwidth is to satisfy the jitter tolerance requirements, as we will see in subsequent sections. Nevertheless, the stringent jitter transfer bandwidth specifications need not be satisfied if the CDR is followed by a demultiplexer. This is contrary to the case where the CDR is part of a repeater chain that is used to regenerate the data over long distance transportation [7], [22], and [50]. Furthermore, since the closed loop transfer function does not have a zero, there will be no jitter peaking. The peaking-free loop filter characteristic is illustrated in Fig. 7.11.

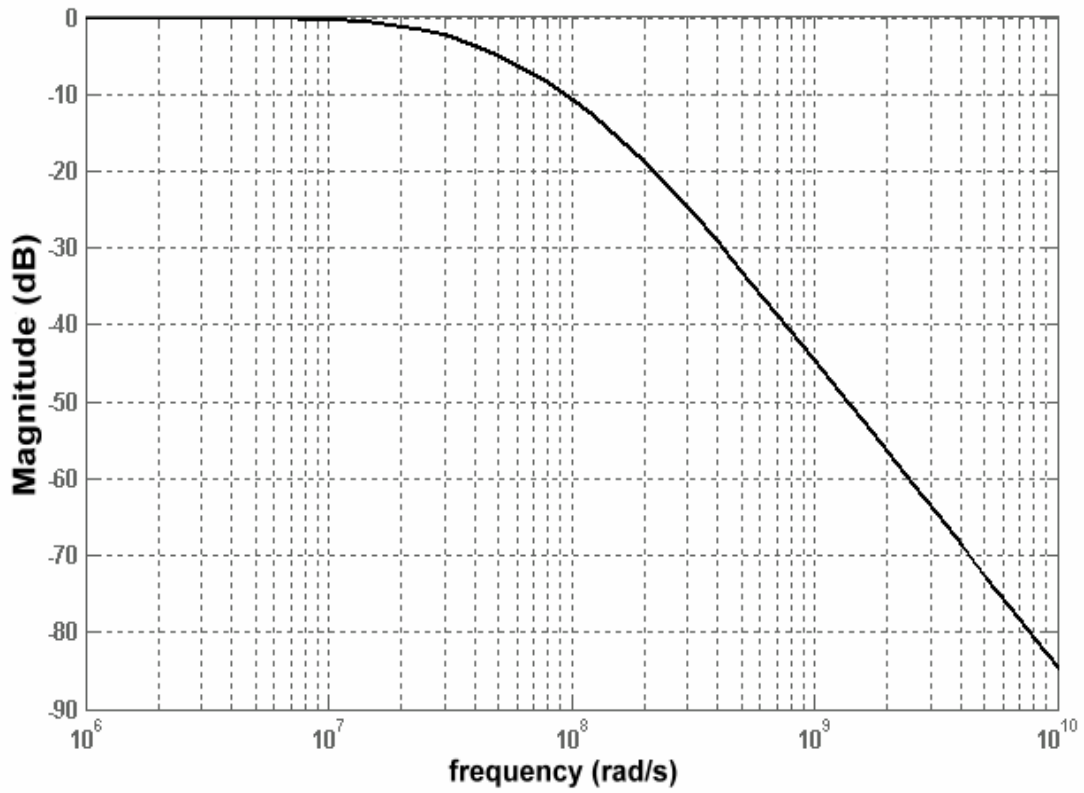


Figure 7.10. Magnitude of the transfer function response.

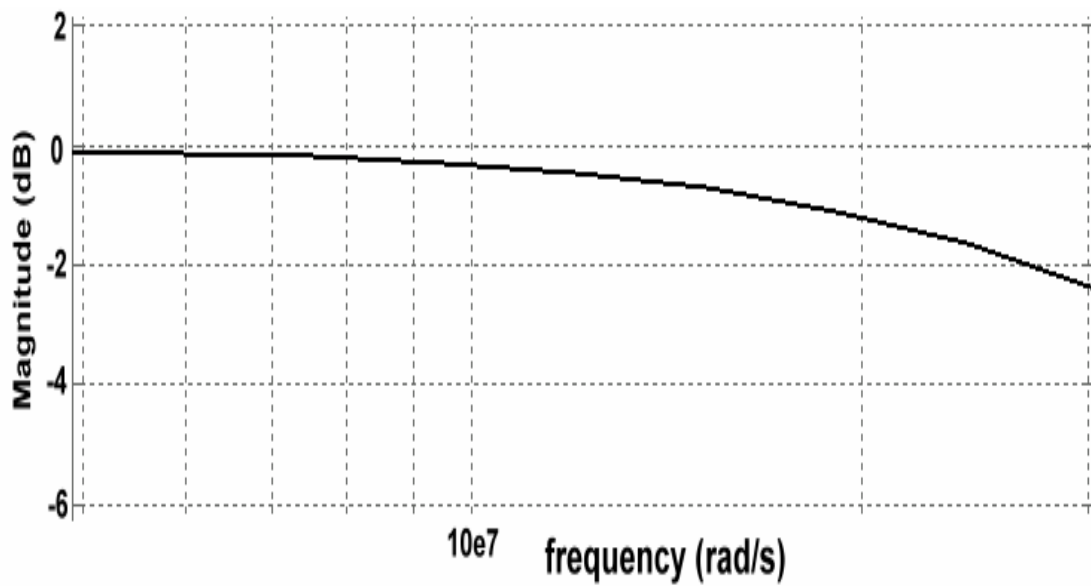


Figure 7.11. Zoom to jitter peaking region of the transfer characteristics.

7.3.2 Jitter Generation

Jitter generation depends on the performance of the building blocks and it is not dependent on the external factors such as outside jitter or noise etc. The noise generators within the system must be minimized so that the device passes the test.

The major sources of jitter generation are identified in [11] as

- 1) VCO phase noise,
- 2) Ripple on the control voltage,
- 3) Coupling of data transitions to the VCO through the clock signal interfaces such as PDs and DFFs,
- 4) Supply and substrate noise coupling.

Of all these four factors, only the first two are controllable at the design stage because the rest of them can only be determined *after* the fabrication of the chip. Efforts to *simulate* the effects of the last two in the design stage are generally not very helpful as the high-frequency behaviour of the devices and the substrate are not fully characterized for such marginal frequencies. However, we should note that enhancing the layout symmetry, employing differential circuit structures, and isolating the noisy digital circuitry from the clock lines may prove useful for reducing the effects of the last two factors.

The VCO phase noise is the main contributor to the jitter generation. Therefore, knowing the free-running VCO jitter can give the designer an idea about the overall CDR jitter generation. The cycle-to-cycle jitter ΔT_{CC} of a VCO is given in [9] as

$$\Delta T_{CC}^2 \approx \frac{4\pi}{\omega_0^3} \cdot S_\phi(\Delta\omega) \cdot \Delta\omega^2 \quad (7.15)$$

where ω_0 is the oscillation frequency and $S_\phi(\Delta\omega)$ is the relative phase noise power at frequency offset $\Delta\omega$.

In general, the overall phase noise of the PLL system tends to be lower than that of a free-running VCO. Thanks to the loop filter, the higher the loop bandwidth, the greater the jitter suppression over a wider frequency range and hence the lower jitter generation [54]. The amount of time t_s that the jitter can freely accumulate before entering saturation is determined in [9] as

$$t_s = \frac{1}{2\pi f_{BW}} \quad (7.16)$$

where $2\pi \cdot f_{BW}$ is the loop bandwidth. Subsequently, the total jitter accumulated over this time interval will be [9]

$$\Delta T_s = \Delta T_{CC} \cdot \sqrt{\frac{f_0}{2} \cdot t_s} \quad (7.17)$$

Substituting (7.15) and (7.16) into (7.17) will result in the relationship between the phase noise and the jitter generation:

$$\begin{aligned} \Delta T_{PLL} &= \frac{2\Delta\omega}{\omega_0} \cdot \sqrt{\frac{\pi}{\omega_0} \cdot S_\phi(\Delta\omega)} \cdot \sqrt{\frac{\omega_0}{4\pi} \cdot \frac{1}{2\pi \cdot f_{BW}}} \\ &= \frac{1}{\sqrt{2\pi \cdot f_{BW}}} \cdot \frac{\Delta\omega}{\omega_0} \cdot \sqrt{S_\phi(\Delta\omega)} \end{aligned} \quad (7.18)$$

Using (7.18), the maximum allowed VCO phase noise at $\Delta\omega = 2\pi \cdot 100\text{krad} / s$ offset to satisfy the $\Delta T_{PLL} = 1\text{ps} - \text{rms}$ jitter generation requirement can be calculated by substituting $f_{BW} = 5.6\text{ MHz}$ and $\omega_0 = 2\pi \cdot 10 \cdot 10^9\text{ rad/s}$:

$$S_\phi(\Delta\omega) = -64.53\text{ dBc} / \text{Hz} \text{ at } 100\text{-kHz offset.}$$

This value can be easily achieved using the LC VCO that we have described before. In fact, the jitter generation from that VCO can be calculated to be approximately 0.3 ps-rms, given the condition that measured stand-alone VCO phase noise is below -90 dBc/Hz at 1-MHz offset. We should also note that if the bandwidth were to be chosen as 120 kHz instead of 5.6 MHz, the phase noise requirement would be as low as -81 dBc/Hz at 100-kHz offset -a value that could only be satisfied *marginally* in a 0.18- μ m CMOS process.

We have seen earlier that the ripple on the control voltage can be minimized by choosing the right type of PD for the right job. As we have done in our VCO design, reducing the VCO gain provides the control line some form of immunity from the disturbances as well. The loop filter can also provide additional suppression. In fact, as far as the loop dynamics and the chip space availability permit, the filter capacitor can be made larger to tackle the ripple.

The cycle-to-cycle jitter generation due to a periodic ripple signal $V_M \cdot \cos(\omega_M \cdot t)$ on the control voltage is expressed in [9] as

$$\Delta T_{CC} = K_{VCO} \cdot \frac{V_M}{f_0^2} \cdot \sqrt{1 - \cos \frac{\omega_M}{f_0}} \quad (7.19)$$

Given the fact that our simulated control voltage exhibits a ripple of 2 mV with frequency not exceeding 10 GHz, the resulting jitter from this ripple at 10 GHz operation frequency is 0.05 ps, producing an overall jitter of 0.4 ps-rms.

7.3.3 Jitter Tolerance

Jitter tolerance mask is presented in Chapter 2 (Fig. 2.7). The CDR designs must exhibit tolerance values that should remain above this mask. The loop filter, once again, plays a significant role to determine the jitter tolerance performance of the CDR. The filter must be able to handle large jitter variations at low frequencies (15UI up to 2.4 kHz). On the other hand, the expected jitter tolerance for high frequencies decreases outside the filter bandwidth (0.15 UI after 4 MHz).

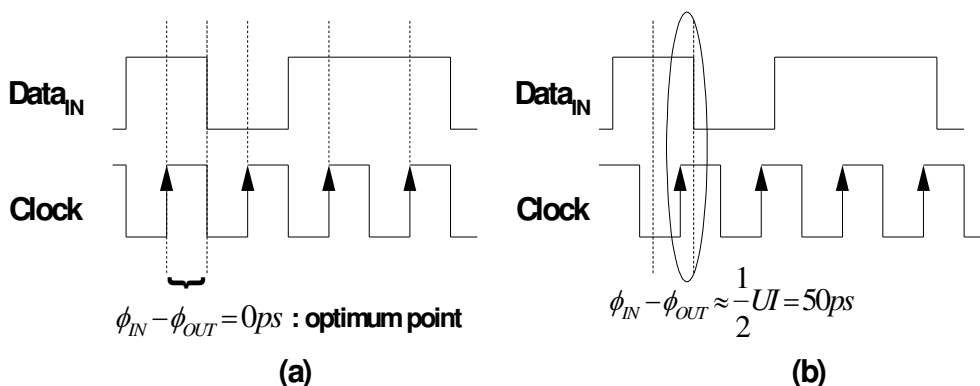


Figure 7.12. The position of the clock and data edges (a) optical sampling point (no jitter) and (b) with jittered data input.

In this section we are going to verify analytically that our design can satisfy the OC-192 jitter tolerance mask imposed by the SONET standards. As shown in Fig. 7.12, when the phase difference between the data input and the clock signal deviates from the optical sampling point towards the data zero crossings, the probability of detection error, i.e., the BER, will increase. The condition to keep BER under control is given in [11] as

$$\phi_{IN} - \phi_{OUT} < \frac{1}{2}UI \quad (7.20)$$

Using (7.20) and the relationship between input and output phases ($H(s) = \frac{\phi_{OUT}}{\phi_{IN}}$),

we get

$$\phi_{IN} < \frac{0.5UI}{1 - H(s)} \quad (7.21)$$

We can specify this value as the minimum amount of input jitter to be tolerated by the CDR in order to keep the BER below the permissible levels. This provides us more conservative jitter tolerance limits when compared to the other expressions such as the one in [19]. Using (7.12) and the transfer function derived for our CDR design in (7.5), we can now define the jitter tolerance as

$$JTOL(s) = \frac{1}{2 \cdot (1 - H(s))} = \frac{1}{2} \cdot \frac{s^2 + 2\zeta \cdot \omega_n \cdot s + \omega_n^2}{s \cdot (s + 2\zeta \cdot \omega_n)} \quad (7.22)$$

In order to see whether this transfer function will satisfy the jitter tolerance mask or not, we can express the magnitude of the JTOL(s) for $s = j\omega$

$$|JTOL(j\omega)|^2 = \frac{1}{4} \cdot \frac{(\omega_n^2 - \omega^2) + 4\zeta^2 \cdot \omega_n^2 \cdot \omega^2}{\omega^4 + 4\zeta^2 \cdot \omega_n^2 \cdot \omega^2} \quad (7.23)$$

and calculate the jitter tolerance at critical points using (7.23). The results are displayed in Table 7.1.

Table 7.1. Calculated jitter tolerance vs. SONET mask requirements.

Critical Frequency	Calculated Jitter Tolerance	Min. Required Jitter Tolerance
2.4 kHz	990 UI	15 UI
24 kHz	99 UI	1.5 UI
400 kHz	5.98 UI	1.5 UI
4 MHz	0.72 UI	0.15 UI

The jitter performance of the loop is simulated using MATLAB and the resulting graph is shown in Fig. 7.13. It can be observed that the jitter tolerance specifications can be easily met by carefully placing the poles and the zeros of the loop filter.

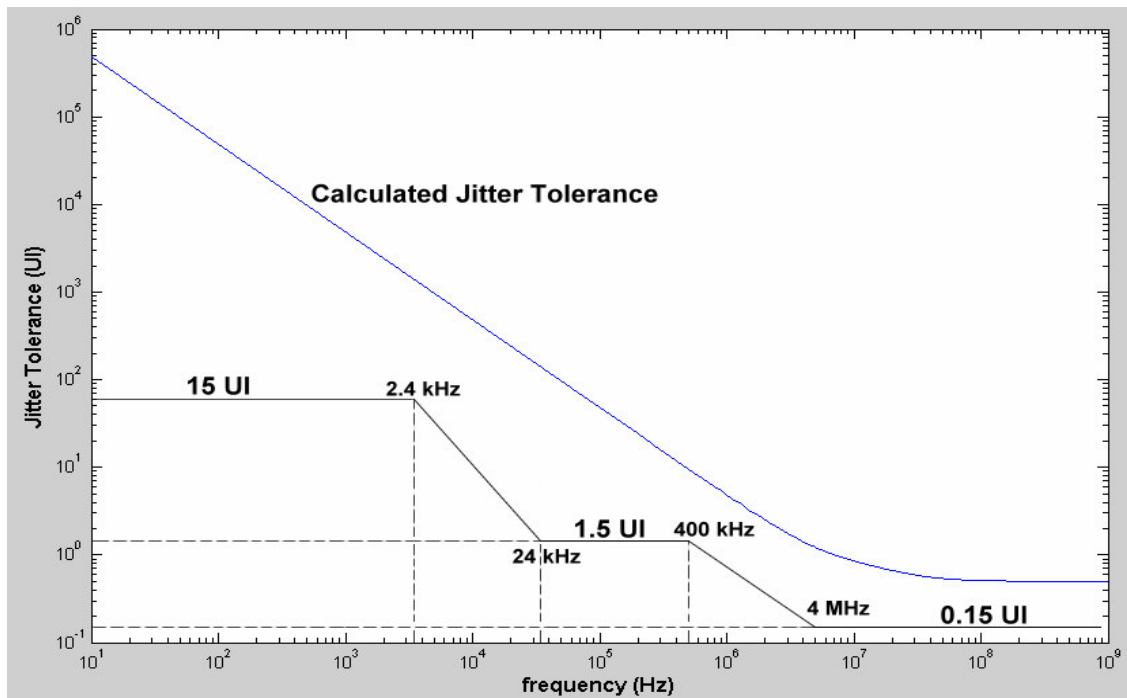


Figure 7.13. Calculated jitter tolerance and SONET mask.

Fig. 7.13 further confirms the high-pass nature of the loop with respect to the input jitter since the tolerable jitter is higher at lower frequencies.

7.4 Measurement Results

The layout of the CDR is drawn using the CHRT 0.18- μm CMOS PDK. The layout size is 560 μm x 780 μm (Fig. 7.14). The measured power consumption of the chip including the output buffers is 48 mW from a 1.8-V supply. This value is much lower than those of the existing designs that are fabricated in CMOS [22] and other more expensive processes [20], [21].

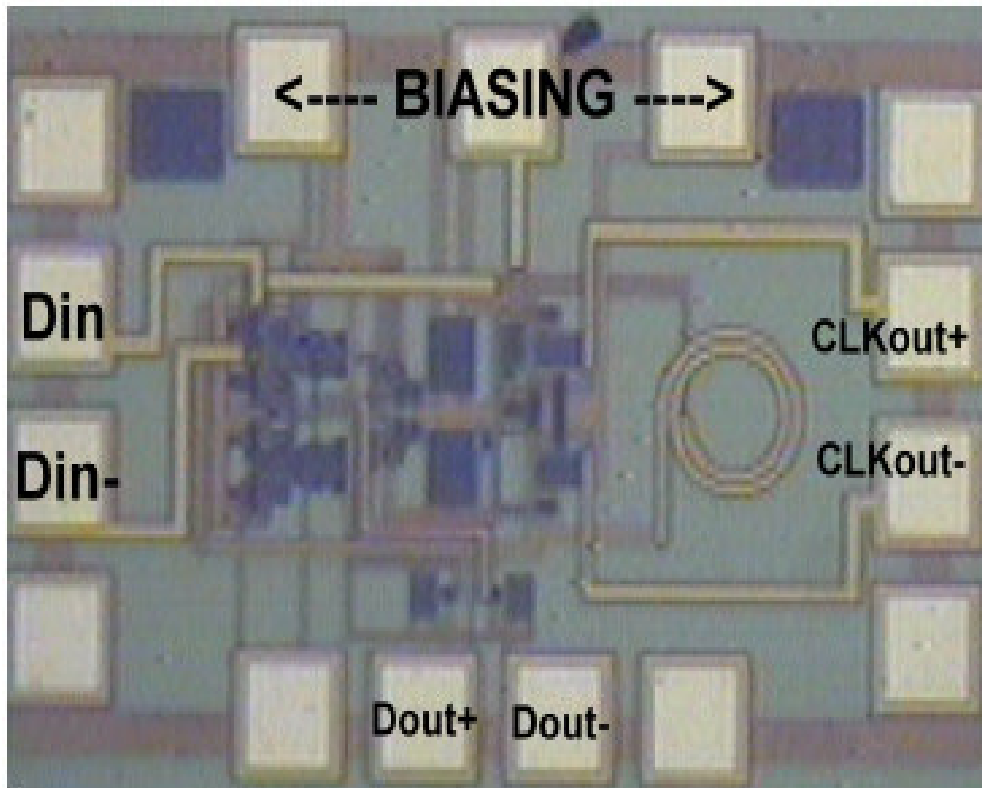


Figure 7.14. Full-rate integrated CDR micrograph.

The on-wafer measurements were carried out using the HP8510C Network Analyzer (Fig. 7.15), Cascade Microtech Coplanar GSG and GSSG probes. The HP Spectrum Analyzer 8565E with the frequency range from 9 kHz to 50 GHz was connected to the RF probe to examine the spectrum of the CDR output.

The prototype that we have managed to test exhibits a somewhat lower operation frequency than the ideal 9.953 GHz. The maximum frequency is measured to be 8.13 GHz. In order to investigate the cause of the frequency deviation, the post-measurement simulations are carried out and it is observed that there are few important factors contributing to the discrepancy:

- 1) The excessive parasitics in the VCO resonator tank structure limit the oscillation frequency and decrease it by 18%. Unlike the standalone design, the VCO circuit here has connections to CLK inputs of the DFFs in addition to the measurement pads. These parasitics increase the loading on the VCO output terminals, reducing both the oscillation frequency and the amplitude. No matter how well the other building blocks perform in a CDR, once the VCO fails to achieve the desired frequency, overall system will not be able to recover the clock and the data from the OC-192 signal.

In order to address this issue in the next fabrication, we can keep the inductor value constant and reduce the varactor size, resulting in a lower tank capacitance. By keeping the inductor constant, we can still maintain the good phase noise value and obtain a higher oscillation frequency. The side effect of this solution will be a narrower tuning range for the VCO, which is nevertheless tolerable for a CDR implementation.

- 2) The shift in the VCO frequency can be compensated using an external control input as well. Assuming that the VCO tuning range covers the 9.953 GHz despite its shifted frequency range due to the parasitics, this control voltage can bring the VCO frequency to signal data rate and hence it can provide an aided acquisition.
- 3) The difference between the simulated and the measured power consumption indicates that at least one of the circuit blocks is not functioning properly. This may be due to the low VCO output swing that results in incomplete switching

of the PD clock inputs. The post-measurement simulations implementing the scenario of reducing the VCO swing by $500 \text{ mV}_{\text{p-p}}$ demonstrate that the PD fails to track the phase difference between the data signal and the clock signal. The discrepancy is translated into an incorrect V_{CTRL} signal through the charge pump and the loop filter. The generated control voltage tunes the VCO to an arbitrary frequency different than 9.953 GHz.

- 4) Although it is possible to operate beyond 5 GHz, the 0.18-um CMOS process that we are using in this work is not optimized for OC-192 applications and the device models are not characterized up to 10 GHz. Therefore, the parasitic extraction using the models provided by the CHRT PDK library is unable to fully reflect the resistive and capacitive parasitics on the interconnects, varactors, and inductors at 10 GHz. We have relied on our intuitive simulation results and foundry-provided measurement results to estimate the parasitics for our CDR layout. Unfortunately, these estimations have fallen short of the actual values.

Several fabrication iterations might be required to do these characterizations and tune the circuits so that they can function properly. However, it is obvious that the amount of effort, time, and necessary expertise to carry out such a large scale modeling and characterization task is beyond the scope of this Ph.D. work.



Figure 7.15. The probing station for measurements.

The phase noise is measured to be -107 dBc/Hz at 1-MHz offset (Fig. 7.16). This value is good enough for a CDR to satisfy the jitter generation requirements. The power consumption is 48 mW from a 1.8-V supply.

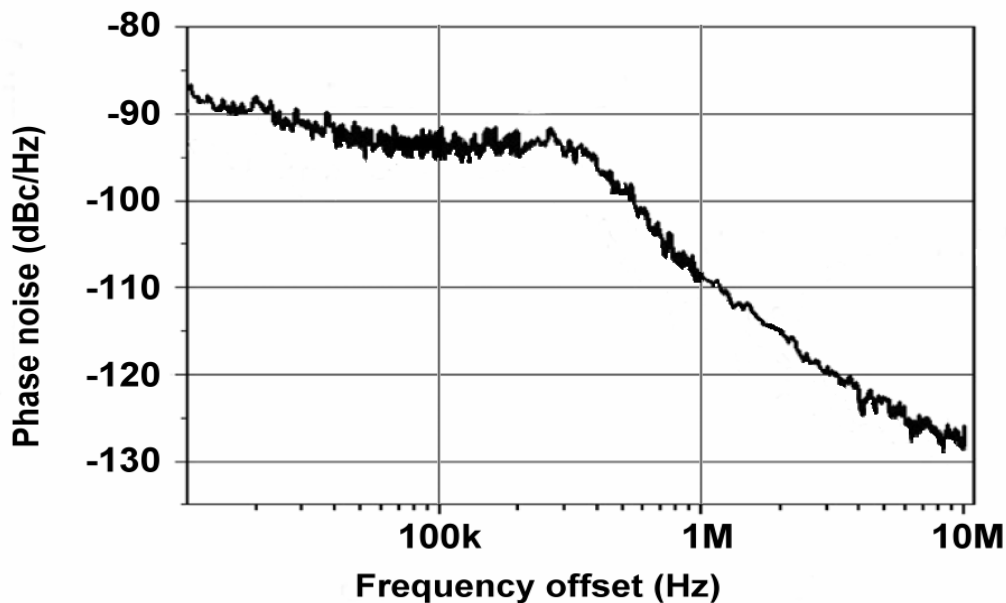


Figure 7.16. Measured phase noise of the full-rate CDR.

Due to the lack of resources, we are not able to perform the jitter tolerance and jitter generation measurements using a dedicated analyzer. Thanks to the analytical calculations and the measured phase noise, we can conclude that the jitter generation will be below the 1 ps-rms mark and the jitter tolerance can satisfy the mask.

Table 7.2. Summary and comparison of the CDR performances.

	This CDR		[19]	[20]	[35]	[51]
	simulated	measured				
Bit Rate	9.953 Gb/s	8 Gb/s	9.953 Gb/s	9.953 Gb/s	9.953 Gb/s	9.953-10.7 Gb/s
VCO Frequency	10 GHz	8.1 GHz	10 GHz	10 GHz	10 GHz	10 GHz
Jitter Transfer Bandwidth	5.52 MHz	5.52 MHz	4 MHz	11 MHz	1.8-10 MHz	8 MHz
Jitter Peaking	<0.1 dB		<0.1 dB	<0.1 dB	<0.1 dB	<0.1 dB
Jitter Generation	0.4 ps-rms	<1 ps-rms	0.78 ps-rms	0.8 ps-rms	0.38 ps-rms	0.44 ps-rms
Jitter Tolerance Mask	Satisfied	-	Satisfied	Satisfied	Satisfied	Satisfied
Capture Range	80 MHz	60 MHz	25 MHz	60 MHz	-	1.8 GHz
Recovered CLK Phase Noise at 1-Mhz offset	-112 dBc/Hz	-107 dBc/Hz	-110 dBc/Hz	-110 dBc/Hz	-107 dBc/Hz	-
Supply Voltage	1.8 V	1.8 V	-5 V	-5 V	1.8 V	1.2-1.8 V
Loop Filter Status	Integrated		External	External	External	External
Power Consumption (w/o buffers)	70 mW*	48 mW*	1.5 W	4.5 W	870 mW	1.65 W**
Technology	0.18- μ m CMOS		SiGe HBT	SiGe HBT	0.18- μ m CMOS	0.09- μ m CMOS
Die Size	560 x 780 μ m ²		3 x 3 mm ²	4.5 x 4.5 mm ²	2.5 x 2.1 mm ²	19 x 19 mm ²

* Including the output buffers.

** Including the transmitter section and the buffers.

Table 7.2 summarizes the performance of the designed CDR and compares it with the reported full-rate designs in the literature. It can be observed from the table that the low supply voltage and power consumption as well as the small silicon area are the

main strengths of the proposed design when compared with power hungry bipolar implementations [19] and [20]. Although the CMOS CDRs in [35] and [51] exhibit satisfactory performance, their silicon area and external loop filter requirements may pose significant challenges to the overall system integration.

7.5 Summary

The design and implementation of the full-rate CDR unit for the OC-192 applications is presented in this chapter. The impact of the modifications and improvements in both circuit topology and system architecture is investigated. A new loop filter topology is also highlighted in this chapter. The small size of the capacitor in this filter makes a fully integrated CDR system feasible in terms of the chip area and hence the cost. The jitter performance of the CDR is analyzed and it is shown that the jitter requirements are satisfied with safe margins for OC-192 applications.

CHAPTER 8

A Fully Integrated Half-Rate

10-Gb/s CDR

In order to investigate the performance of the half-rate phase detector that we have described in Chapter 6, we have designed and implemented a fully integrated half-rate CDR circuit using this PD. Similar to the full-rate version; this CDR design is also based on the same 0.18- μm CMOS process.

8.1 Half-Rate CDR Architecture

Since we have focused on the half-rate PD performance in this round, we have opted for the single loop CDR architecture for the design (Fig. 8.1). The loop incorporates the half-rate PD and the quadrature VCO in addition to the charge pump and the loop filter blocks that have been used in the full-rate CDR.

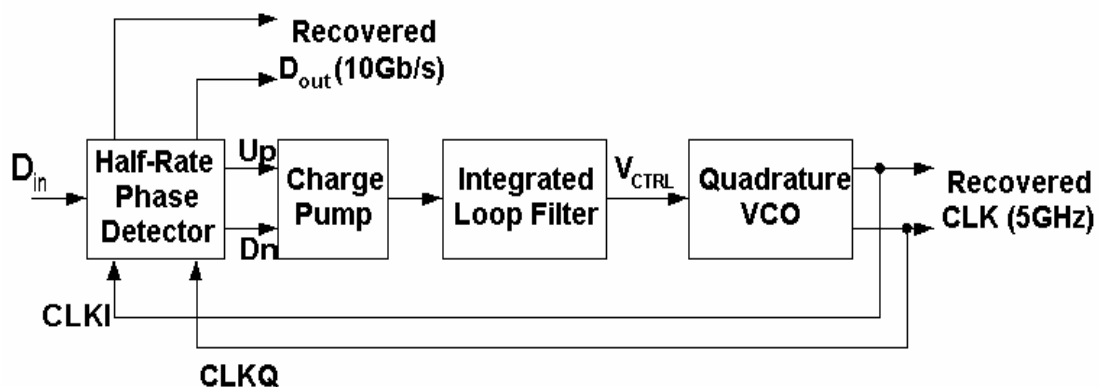


Figure 8.1. Half-rate CDR architecture.

The differential structures are maintained in the circuit designs, as this is an effective way to minimize the crosstalk and the substrate noise. We have described the operating principles of the PD, charge pump, and the loop filter in detail in the previous chapters. Therefore, we will elaborate on the design of the quadrature VCO here. Subsequently, the simulation and measurement results will be presented to complete the discussion on the performance of the half-rate CDR.

8.2 The Quadrature VCO with 5-GHz Operating Frequency

Quadrature clock signals are extensively used in the direct conversion transceivers [55]-[57]. With the recent introduction of the half-rate CMOS CDR designs, they gained popularity in SONET applications as well. Among the various methods to generate the quadratic signals such as the poly-phase network [58], even-stage ring oscillator [23], and quadrature LC-VCO [46], [59]; the quadrature VCOs have been the best choice for their low phase noise, low jitter generation, and high speed [47].

Two identical voltage controlled oscillators are coupled in such a way that the outputs produced by this coupling exhibit 90° phase difference. Following the schematic given in Fig. 8.2, the quadrature output generation can be explained as follows:

We start by expressing the sinusoidal outputs of the two VCO cores in phasor notation as $(OUT1+) = r \cdot e^{j\theta}$ and $(OUT2+) = r \cdot e^{j\beta}$, where θ and β are the arbitrary phases. Since the VCO cores are identical, the amplitudes of the outputs and hence the complex modulus (or magnitudes) of the phasors are equal. The differential counterparts of the corresponding outputs will then be $(OUT1-) = r \cdot e^{j(\theta+\pi)}$ and

$(OUT2-) = r \cdot e^{j(\beta+\pi)}$, respectively. The relationship between these outputs can be approximated as

$$G_{M14} \cdot (OUT1+) = (OUT2-) \Rightarrow G_{M14} \cdot (r \cdot e^{j(\theta)}) = r \cdot e^{j(\beta+\pi)} \quad (8.1)$$

and

$$G_{M4} \cdot (OUT2-) = (OUT1-) \Rightarrow G_{M4} \cdot (r \cdot e^{j(\beta+\pi)}) = r \cdot e^{j(\theta+\pi)} \quad (8.2)$$

G_{M4} and G_{M14} are the transconductance values of M4 and M14, respectively. Dividing (8.1) by (8.2) and applying cross-multiplication, we get

$$G_{M14} \cdot (e^{j(2\theta+\pi)}) = G_{M4} \cdot (e^{j(2\beta+2\pi)}) \quad (8.3)$$

Given that $G_{M4} = G_{M14} = G_M$ for the two oscillator cores with equal bias currents, we can easily show that the two phases exhibit quadrature characteristics:

$$e^{j(2\theta+\pi)} = e^{j(2\beta+2\pi)} = e^{j(2\beta)} \Rightarrow \beta = \theta + \frac{\pi}{2} \quad (8.4)$$

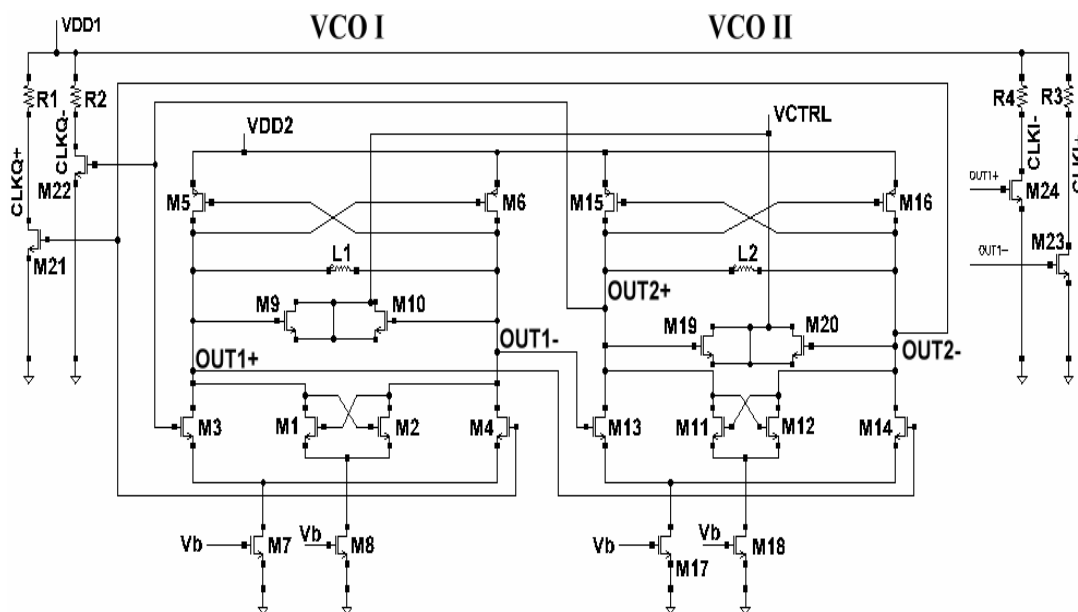


Figure 8.2. Quadrature VCO for 5-GHz clock signal generation.

As shown in Fig. 8.2, two complementary cross-coupled LC VCO cores (M1-M2 and M11-M12) employ anti-phase coupling to generate the quadrature signals in our CDR

design. The output buffers (M21-M22 and M23-M24) are used to isolate the VCO from the PD block and provide a well-defined swing to the DFF circuits used in the PD.

The tuning scheme of this VCO differs from the previously reported QVCOs [11], in such a way that the frequency is varied using the varactors (M9-M10 and M19-M20) instead of changing the coupling ratio of the QVCO through M7-M8 and M17-M18. This is done so as to eliminate the degradation of the resonator quality factor with increasing coupling ratio [60]. The operation frequency of 5 GHz is low enough to allow us to adjust the varactor and the inductor values to optimize the phase noise and increase the tuning range to tackle process variations. Table 8.1 describes the device sizes of the designed QVCO.

Table 8.1. QVCO device parameters.

Device	Size (W/L)
[M1-M4] and [M11-M14]	30 μm /0.18 μm
[M5-M6] and [M15-M16]	30 μm /0.18 μm
[M21-M24]	60 μm /0.18 μm
M7 and M17	50 μm /0.18 μm
M8 and M18	40 μm /0.18 μm
[M9-M10] and [M19-M20]	150 μm /0.45 μm
L1 and L2	1.9 nH
[R1-R4]	150 Ω

The layout size of the QVCO is 600 μm x 280 μm , relaxing the chip space requirements. This layout has been used to generate the parasitic capacitance and resistances for post layout simulations. While the layout is shown in Fig. 8.3, the

simulated output of this VCO along with the phase noise is given in Fig. 8.4 and Fig. 8.5, respectively.

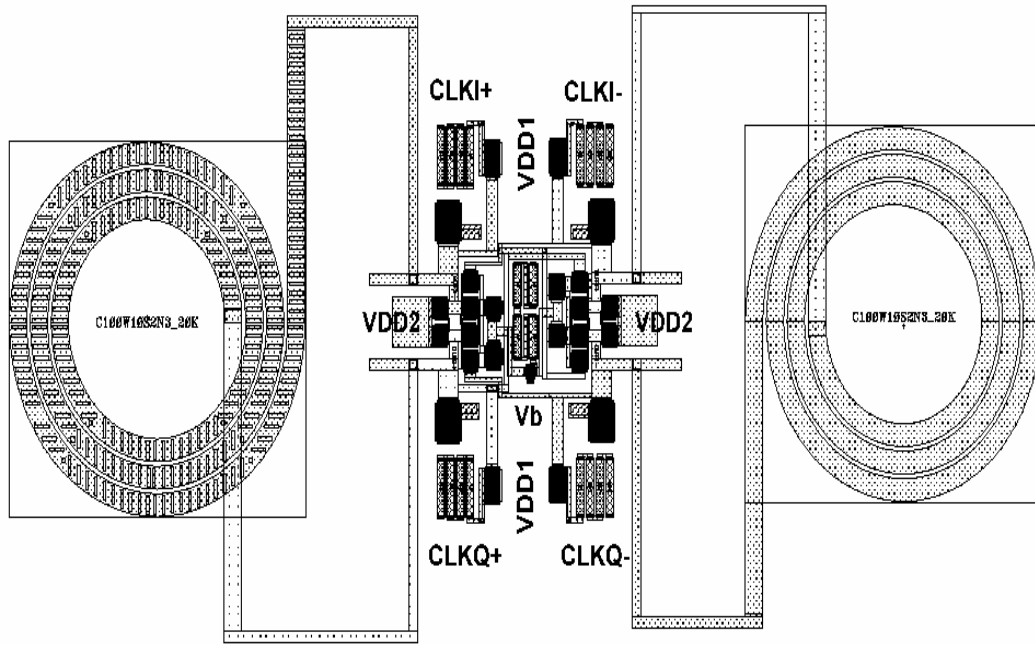


Figure 8.3. QVCO layout.

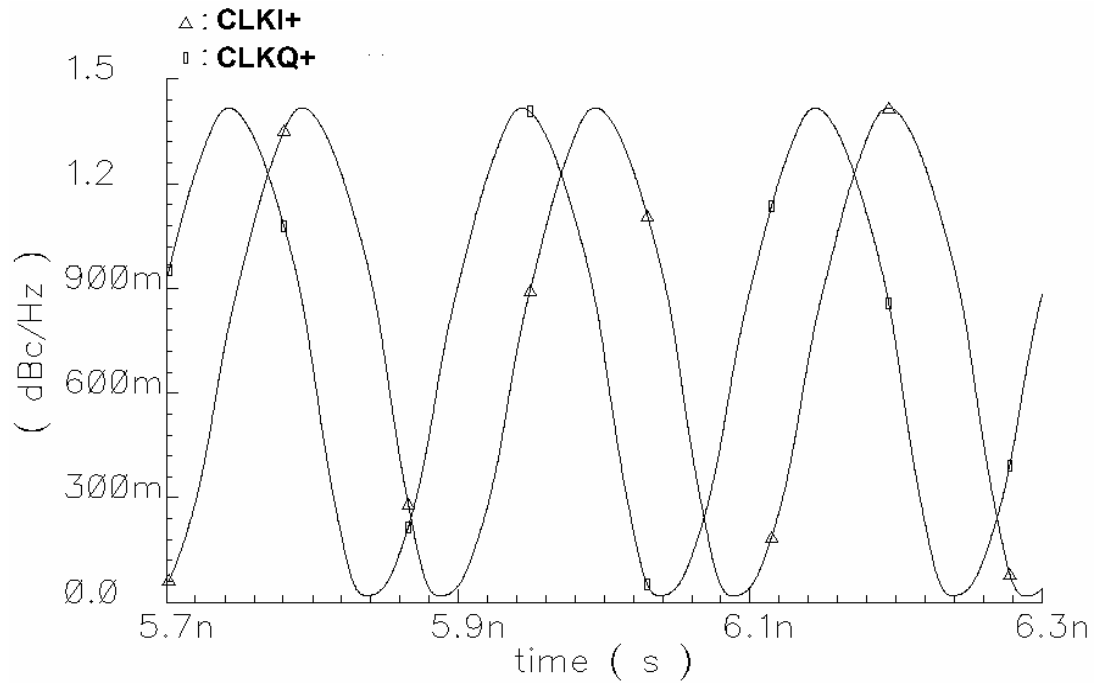


Figure 8.4. QVCO outputs.

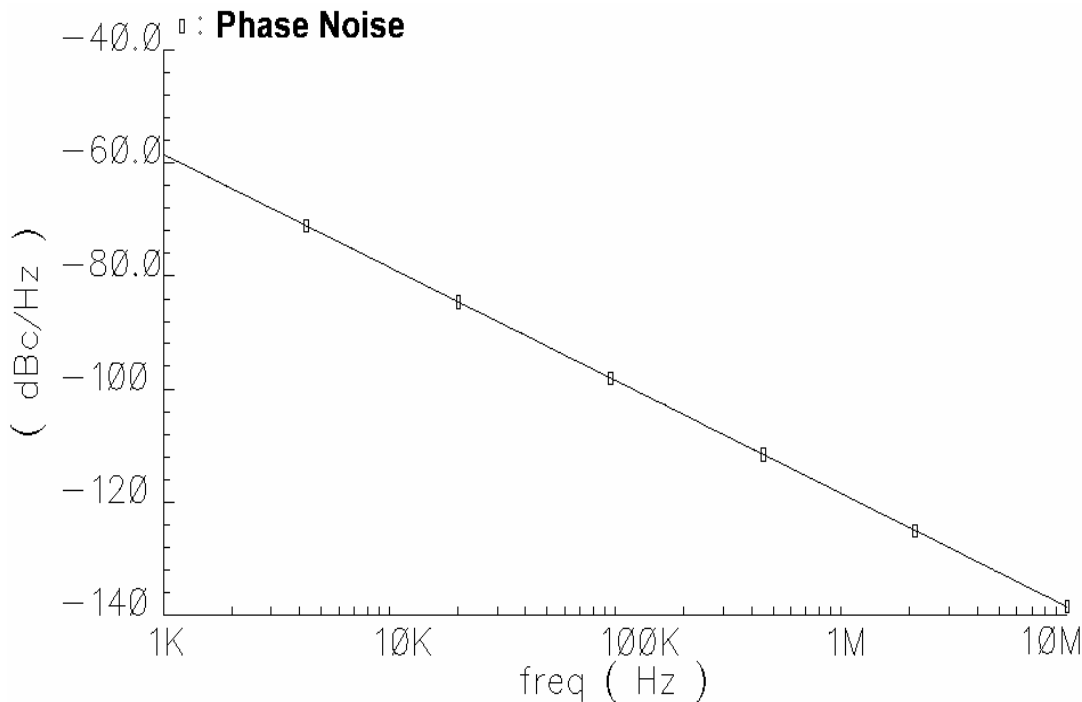


Figure 8.5. QVCO simulated phase noise.

It can be seen that the outputs exhibit the 90° phase difference between the quadrature clock signals. The peak-to-peak output swing is sufficient to switch the DETFFs of the PD. Fig. 8.5 indicates that the simulated phase noise of this VCO is below -115 dBc/Hz at 1-MHz offset. The oscillation frequency range is from 4.65 GHz to 5.5 GHz, wide enough to compensate for the process and temperature variations. The VCO gain K_{VCO} can also be calculated as 400 MHz/V ($= 2\pi \cdot 400$ Mrad/s/V).

The simulated power consumption is 55.5 mW from a 1.8-V supply (15 mW for the core and 40.5 mW for the output buffers). This high figure is somewhat expected since there are two pairs of VCO cores and output buffers; double the number of devices in the 10-GHz VCO that is described in Chapter 4.

8.2.1 QVCO Measurement Results and Comparison

The QVCO is realized in CHRT 0.18- μm CMOS process and the measurement results are obtained to verify the simulated performance (Fig. 8.6). The measured operation frequency of 5.8 GHz and the tuning range of 1 GHz are slightly higher than the simulated ones. K_{VCO} has increased to 550 MHz/V with the tuning range. This is due to the over-cautiously selected parasitic capacitors for the post-layout simulations that produced a lower operation frequency. Nevertheless the frequency span is large enough to cover the half-rate clock frequency of 5 GHz. We predict that the operation frequency will be further lowered to the optimum point by the additional loading from the phase detector after the QVCO is integrated into the CDR system. The phase noise is measured to be -109 dBc/Hz at 1-MHz frequency offset. The chip photograph and the phase noise plot are given in Fig. 8.6 and Fig. 8.7, respectively.

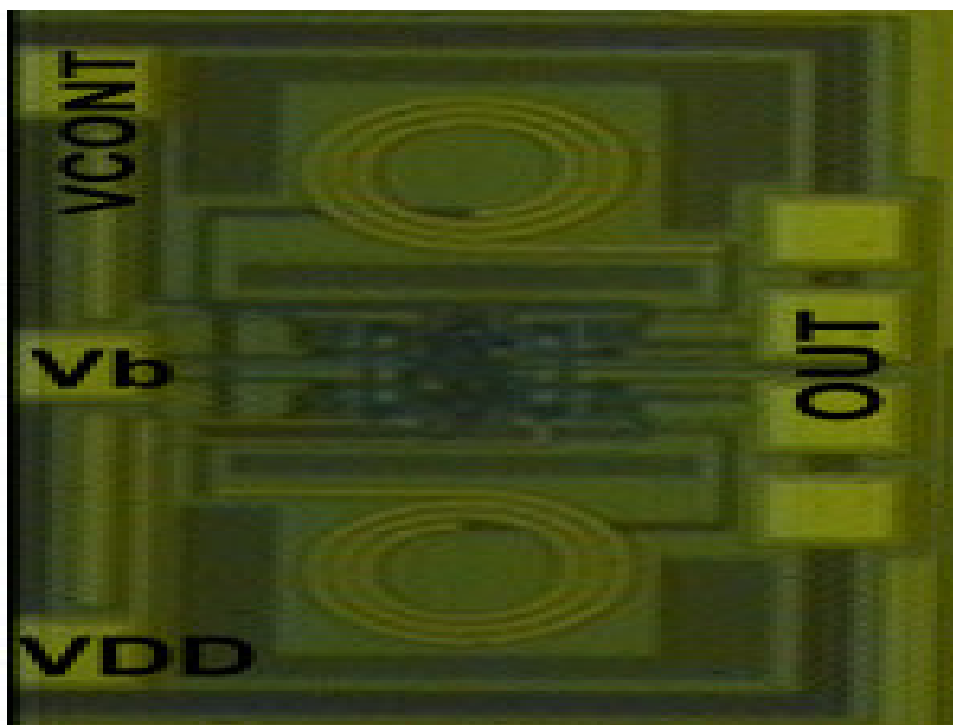


Figure 8.6. QVCO chip photograph.

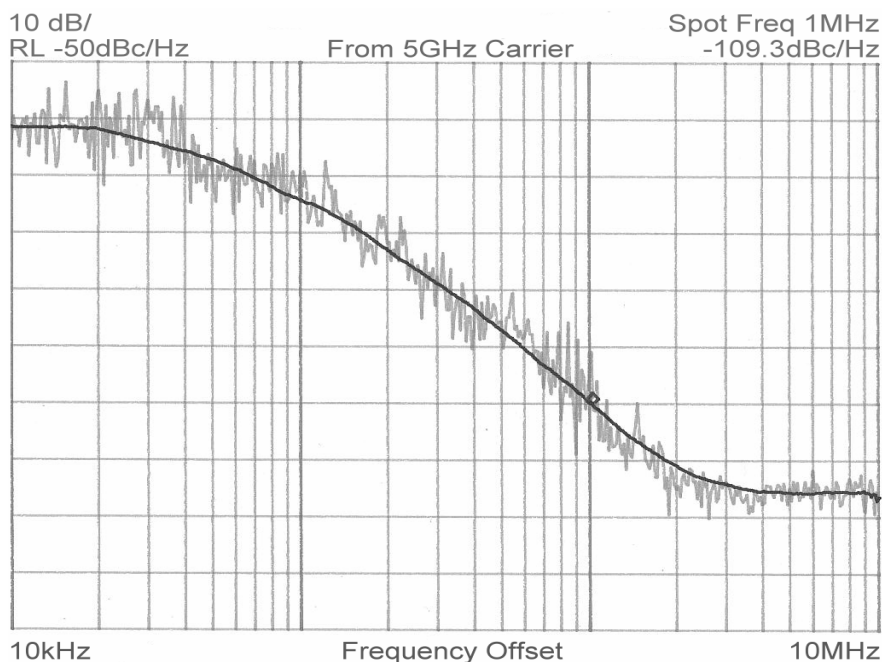


Figure 8.7. QVCO measured phase noise.

The designed QVCO performance is summarized and compared with an existing 5-GHz QVCO in Table 8. 2. The VCO in [7] performs quadrature clock generation using microstrip delay lines in a ring formation. Unanticipated delay and parasitic losses between the delay stages result in lower-than-expected oscillation frequency and a narrow tuning range. With its low power consumption, wide tuning range, and low phase noise, our QVCO proves that LC resonator oscillators exhibit better performance at high frequencies when compared to the ring oscillators.

Table 8.2. Simulated QVCO performance and comparison.

	5-GHz QVCO		[7]
	Post-Layout Simulation	Measurement	
Max. frequency	5.5 GHz	5.8 GHz	4.43 GHz
Phase noise at 1-MHz offset	-115 dBc/Hz	-109 dBc/Hz	-103 dBc/Hz
Tuning range	750 MHz	1 GHz	240 MHz
Voltage supply	1.8 V	1.8 V	1.8 V
Power consumption w/o buffers	15 mW	20 mW	70 mW
Technology	0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS

8.3 Half-Rate CDR Simulation and Measurement Results

We have used the Cadence SpectreRF simulator engine to obtain the simulation results for the other crucial parameters. All of the simulations are based on the post-layout circuits that include the parasitics extracted from the layout using the PDK that is provided by the foundry. The on-wafer measurements were carried out using the full-rate CDR measurement setup described in Chapter 7. Anritsu 68347C Synthesized Signal Generator is used in order to produce the 10-Gb/s input signal.

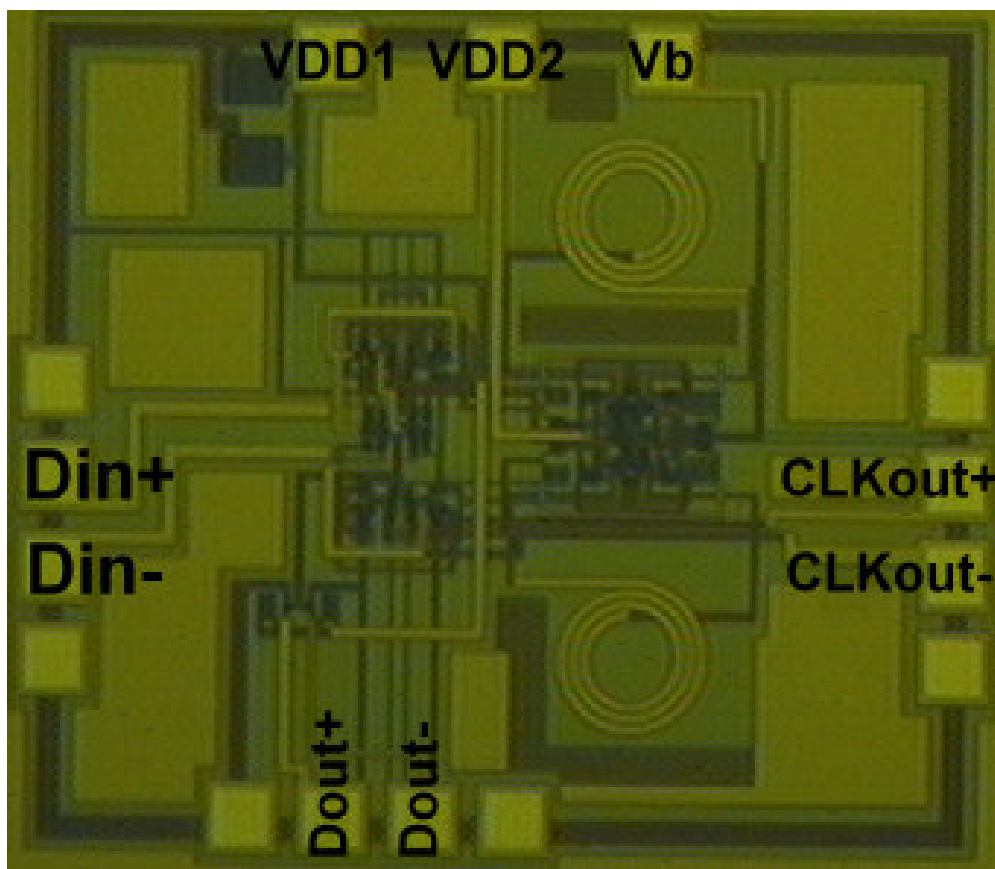


Figure 8.8. Half-rate CDR chip photograph.

The chip photograph is shown in Fig. 8.8. The overall size including the pads is $820\ \mu\text{m} \times 840\ \mu\text{m}$, which is much smaller than the reported CDRs [7], [19]-[23]. This

compact size can facilitate the low-cost implementations on CMOS technology. The core circuit can be easily integrated into a bigger system that will include the transmitter. Fine-tuning of the metal line widths to match the parasitics in the complementary differential paths is done using the information gathered from the layout extraction, resulting in a better symmetry.

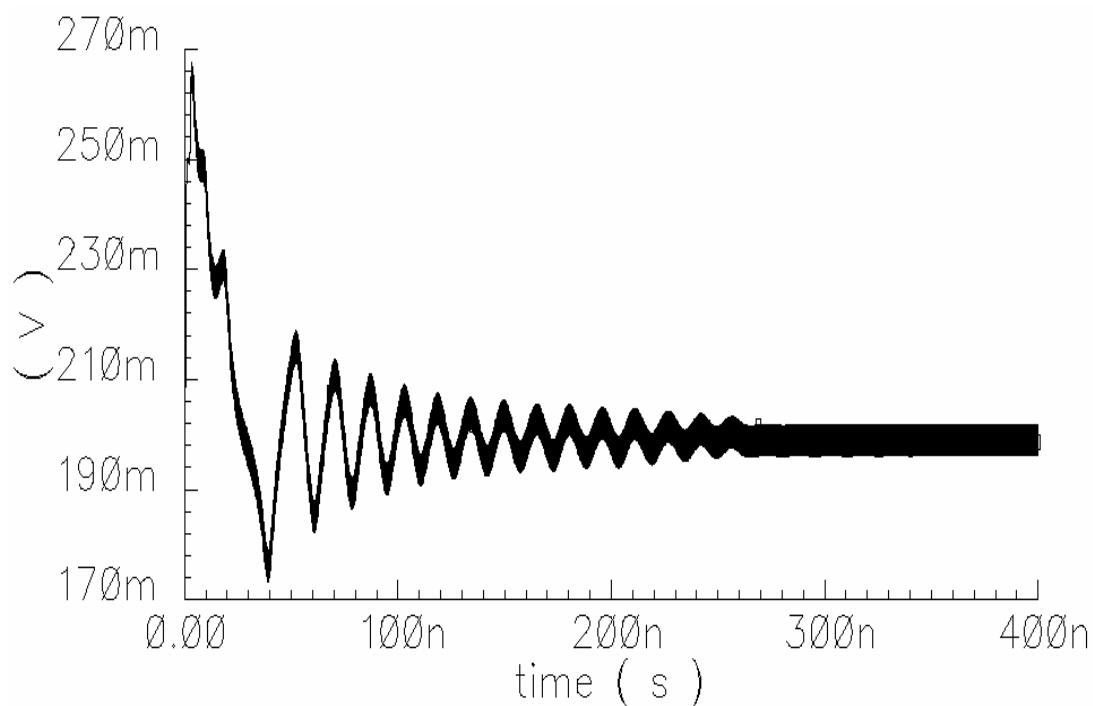


Figure 8.9. Locking characteristics of the loop.

The CDR loop can acquire lock in less than 300 ns (Fig. 8.9). The ripple on the control voltage is higher than that of the full-rate implementation, but it is still within the acceptable limits as will be shown by the jitter generation calculations in the subsequent section.

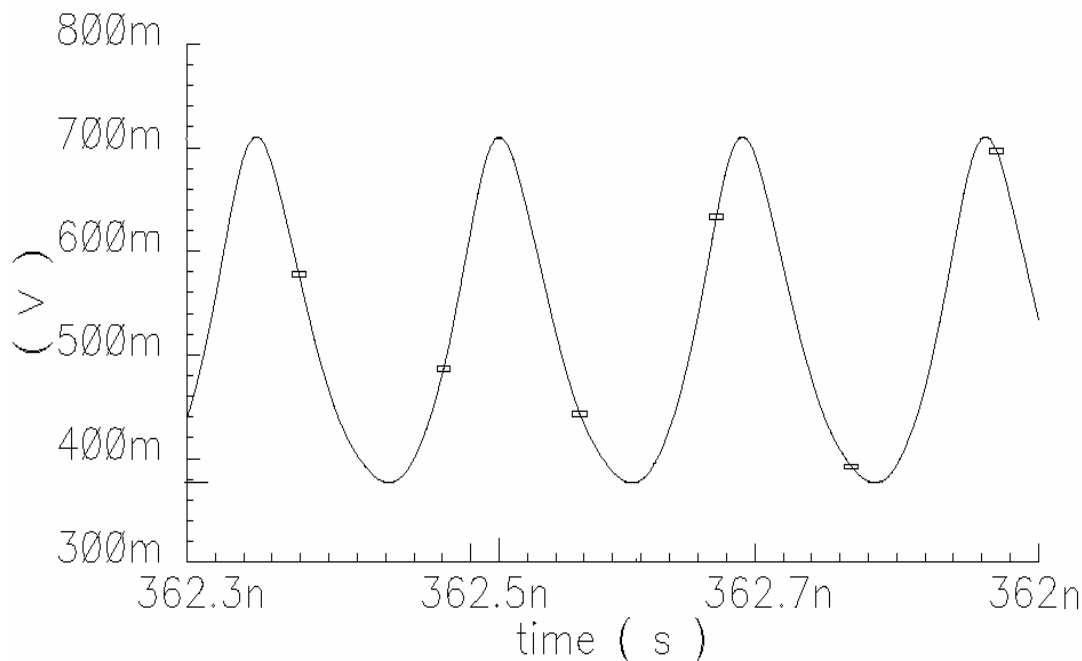


Figure 8.10. The 10-Gb/s recovered data output from the half-rate PD.

The capture range for this CDR is 80 MHz. This value is sufficient for the CDR to lock the clock signal to the data input. In order to illustrate the inherent data-retiming feature of the circuit, the recovered data is obtained through a buffer from the first DETFF output terminal of the half-rate PD. The output swing is around $300\text{ mV}_{\text{p-p}}$ (Fig. 8.10). The swing can be further improved at the expense of the increased power consumption at the output buffers. We should also note that the buffer loading must be carefully monitored at the PD output since this node is susceptible to extra loading from the internal MUX and XOR gate circuits as well.

The overall power consumption for the CDR is simulated as 85 mW from a 1.8-V supply. The measured power consumption, however, is 74 mW due to the single-input testing dictated by the signal generator.

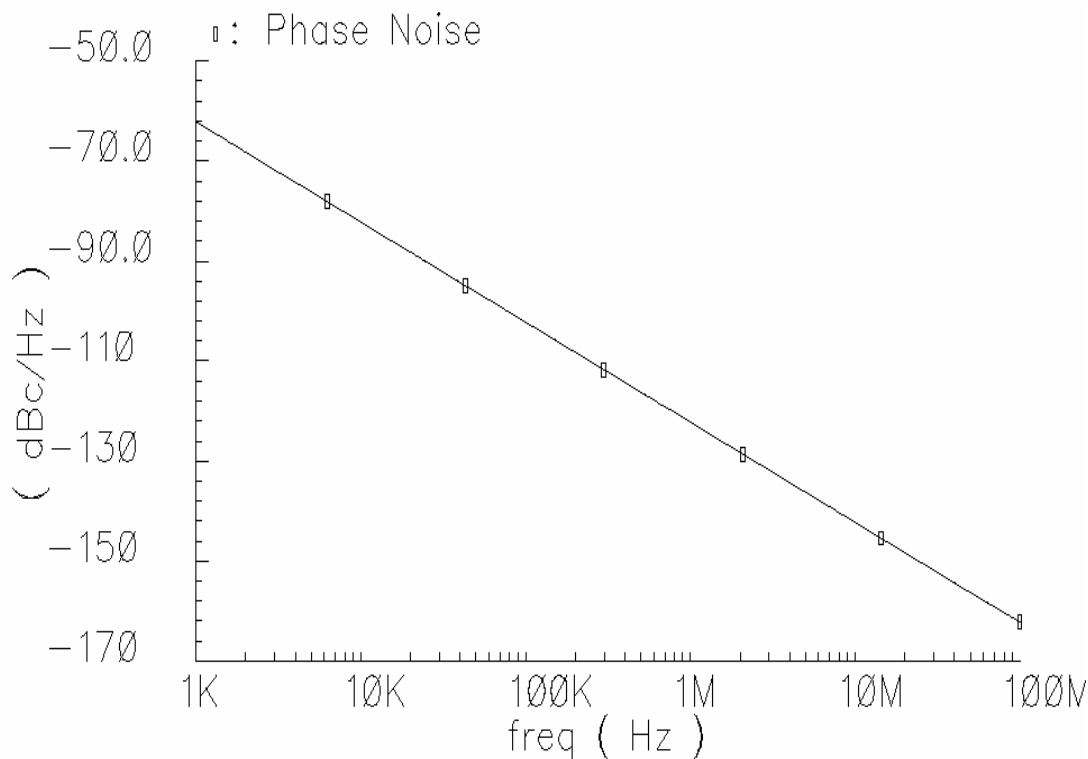


Figure 8.11. Half-rate CDR recovered clock simulated phase noise.

The lack of differential input manifests itself on the phase noise as well. The simulated and the measured phase noise values of the recovered clock are presented in Fig. 8.11 and Fig. 8.12, respectively. The suppression of the noise components within the loop bandwidth further reduces the VCO phase noise.

The simulated phase noise is found to be -121 dBc/Hz at 1-MHz frequency offset, whereas the measured value is -114 dBc/Hz at 1-MHz frequency offset. The jitter calculations indicate that the discrepancy is still tolerable and the requirements are satisfied with the measured value.

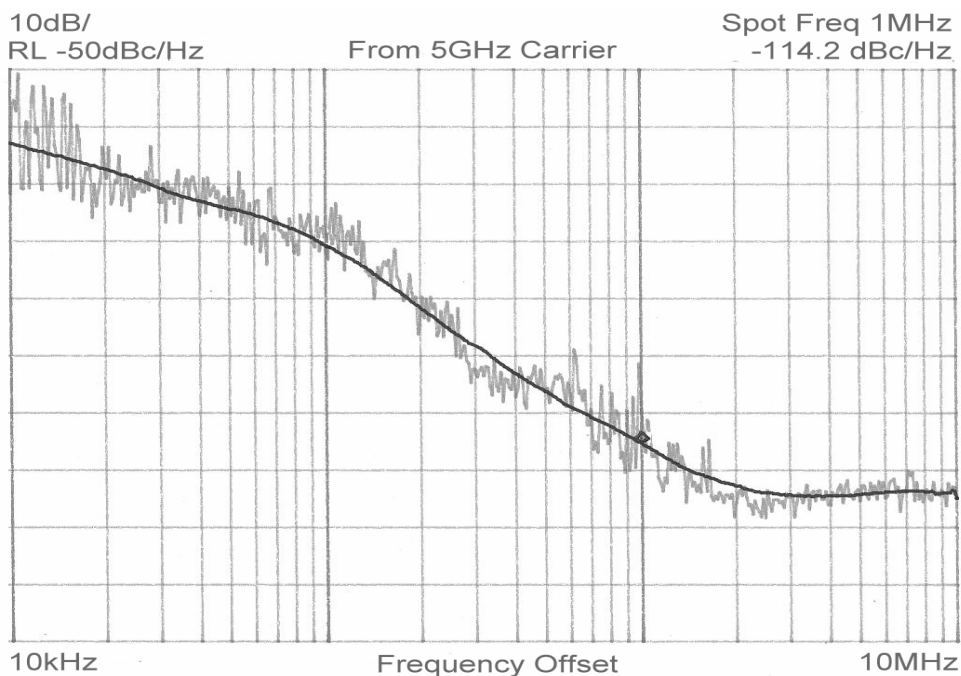


Figure 8.12. Half-rate CDR recovered clock measured phase noise.

The frequency spectrum of the recovered clock is illustrated in Fig. 8.13. The filtering effect of the PLL structure is clearly visible in this figure.

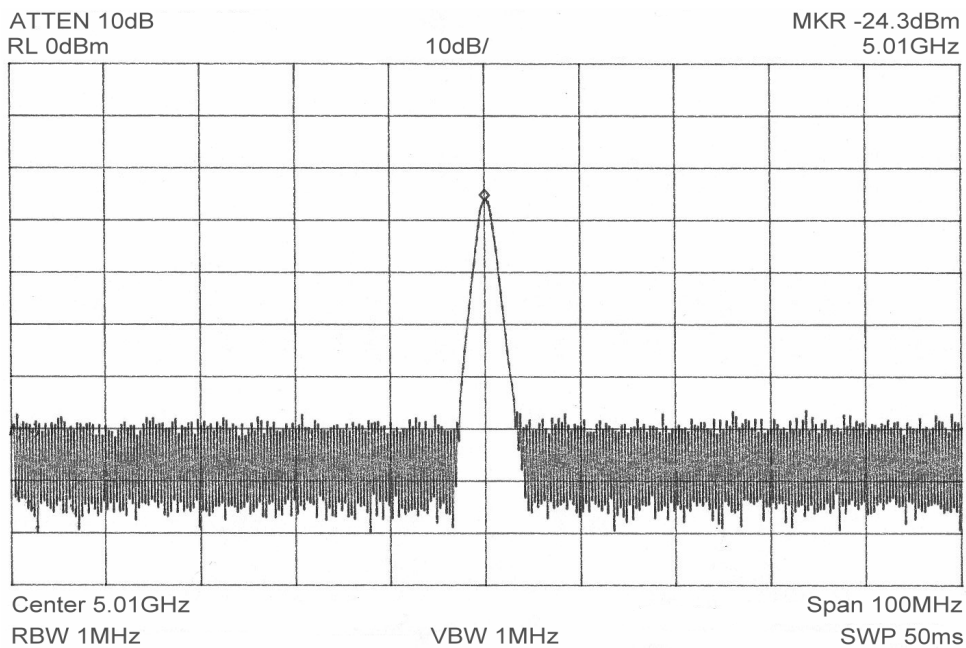


Figure 8.13. Half-rate CDR recovered clock spectrum at 5 GHz.

8.4 Jitter Performance of the Half-Rate CDR

The charge pump current is set as 150 μA . Although the half-rate clock is 5 GHz, the operation is still based on the 10-Gb/s OC-192 standard. Therefore, the natural frequency and the damping ratio are almost identical to those of the full-rate CDR design described in Chapter 7, i.e., $\omega_n = 2\pi \cdot 12.3 \text{ Mrad/s}$ and $\zeta = 1.3$, respectively.

Using these values, the jitter transfer bandwidth is calculated as $\omega_{-3dB} = 2\pi \cdot 5.52 \text{ Mrad/s}$. No jitter peaking is observed. The jitter generation will be calculated from the VCO phase noise using

$$\Delta T_{PLL} = \frac{1}{\sqrt{2\pi \cdot f_{BW}}} \cdot \frac{\Delta\omega}{\omega_0} \cdot \sqrt{S_\phi(\Delta\omega)} \quad (8.5)$$

For the loop bandwidth $f_{BW} = 5.52 \text{ MHz}$, the frequency offset $\Delta\omega = 2\pi \cdot 1 \text{ Mrad/s}$, the operating frequency $\omega_0 = 2\pi \cdot 5 \text{ Grad/s}$, and the CDR phase noise $S_\phi(\Delta\omega) = -114 \text{ dBc/Hz}$ at 1-MHz offset, the jitter generation is given as 0.067 ps-rms.

The K_{VCO} for this design is $2\pi \cdot 550 \text{ Mrad/s/V}$ and the maximum ripple frequency is 5 GHz. Using the equation (7.19), the jitter generation due to the 5-mV ripple on the control voltage is less than 0.4 ps-rms. The overall jitter generation is below 0.5 ps-rms, satisfying the OC-192 requirement. Finally, since the loop parameters are approximately the same as those of the full-rate CDR design, we can conclude that the jitter tolerance requirements will also be satisfied with a safe margin (please refer to Fig. 7.13.).

The performance of the fully integrated half-rate CDR is summarized and compared with the existing half-rate CDR designs in Table 8.3. The proposed half-rate CDR has the lowest jitter generation and second lowest power consumption in the comparison.

Table 8.3. CDR comparison with the existing designs.

	This CDR		[7]	[22]	[23]	[50]
	simulated	measured				
Bit rate [Gb/s]	9.953		9.953	9.953	9.953	9.953-10.7
VCO frequency [GHz]	5		5	5	5	5
Jitter transfer bandwidth [MHz]	5.52		3	15	5.2	8
Jitter peaking [dB]	<0.1		<0.1	1.48	<0.1	<0.1
Jitter generation	0.4 ps-rms	<0.5 ps-rms	8 ps p-p	0.6 ps-rms	0.8 ps-rms	3 ps p-p
Jitter tolerance mask	Satisfied		Satisfied	Failed	Failed	Satisfied
Capture range	80 MHz		21 MHz	6 MHz	1.43 GHz	-
Recovered CLK phase noise [at 1-MHz offset]	-121 dBc/Hz	-114 dBc/Hz	-127 dBc/Hz	-106 dBc/Hz	-107 dBc/Hz	-
Supply voltage [V]	1.8		1.8	2.5	1.8	1.2-1.8
Loop filter status	Integrated		External	External	External	External
Power consumption (w/o buffers) [mW]	85	74	285	72	91	>100
Technology	0.18- μ m CMOS		0.18- μ m CMOS	0.18- μ m CMOS	0.18- μ m CMOS	0.13- μ m CMOS
Die size	820 x 840 μ m ²		1.9 x 1.5 mm ²	1.1 x 0.9 mm ²	1.7 x 1.5 mm ²	19 x 19 mm ² (package)

Furthermore, while the other CDRs employ off-chip components to realize the loop filter, our CDR maintains its monolithic structure by using on-chip capacitors. It can be seen from the table that the designed CDR performance is one of the best when compared to the existing half-rate CDRs.

8.5 Summary

A half-rate CDR circuit incorporating a novel half-rate PD design and a fully integrated loop filter is presented in this chapter. The analytical jitter performance of the circuit is described and the simulation and measurement results are shown for various performance parameters. The jitter requirements are satisfied with safe margins.

While the low-power dissipation and low-cost implementations are becoming norms in CMOS CDRs, the continuous efforts to improve the performance of these circuits can get another boost from the all-integrated-design approach, thanks to the integrated loop filter.

The half-rate architecture will maintain its position as an attractive alternative while the data rates of the SONET applications increase beyond the values where a full-rate state-of-the-art CMOS CDR can operate comfortably.

CHAPTER 9

Conclusion & Recommendations

9.1 Conclusion

In this thesis, the design of fully integrated high-speed low-power CMOS CDR circuits for SONET OC-192 applications has been explored.

We have proposed several modifications and circuit design techniques in this thesis. We should note that these improvements can be applied to any other technology or SONET standard as well.

A 10-GHz VCO was designed and fabricated in CHRT 0.18- μm Analog/RF CMOS 2-poly 6-metal process. The active chip area is 280 μm x 250 μm . The phase noise was measured to be -95 dBc/Hz at 1-MHz offset with power consumption less than 3 mW, excluding the buffers.

The effect of the supply voltage scaling on the tuning voltage of this VCO was also investigated. A wide tuning range of 2.2 GHz was obtained for 1.8-V supply, whereas this range decreased to 300 MHz for 1.5 V. This variable VCO tuning range is useful for improving the jitter performance of the overall CDR by providing resistance against the ripples on the VCO control line.

Two methods were proposed for the PD block; one in circuit level and the other in architectural dimension:

First method involves a modification to the existing DFFs such that very high switching speeds can be achieved using the 0.18- μm CMOS devices. With our proposed DFF, one can easily achieve 10 GHz with reasonable power consumption. The improvement in the DFF speed directly enhances the PD performance, as the DFFs are the main building blocks of a sequential PD. The modified DFF outputs can also provide high voltage swings of 1.5 $V_{\text{p-p}}$ with a 900 mV-dc. The power consumption of this PD is 28 mW from the nominal 1.8-V supply.

Second method describes a novel dual-rate linear PD that can be used in both half-rate and full-rate CDR systems. This PD provides a much-needed flexibility in an environment where the available CMOS technology can hardly operate at its boundaries, failing to satisfy the jitter requirements. Additionally, the design retimes the data without an additional decision circuit and hence it minimizes the systematic offset. With its total power consumption of 30 mW from a 1.8-V supply, this PD has one of the best power efficiency among the existing PDs. To the best of our knowledge, this is the only PD architecture with *dual-rate* operation capability.

We have proposed a modified loop filter topology that facilitates the realization of fully integrated PLL-based CDRs. The parameters related to the loop dynamics and transfer characteristics of the integrated CDR are derived. The filter capacitor can be selected as low as 20 pF in this filter topology.

In order to investigate the collective contributions of the proposed modifications, a fully integrated 10-Gb/s CDR circuit was designed and fabricated in CHRT 0.18- μm CMOS process. Analytical evaluation of the loop parameters indicated that the CDR can successfully meet the jitter requirements of the OC-192 standard. The small chip size of 840 μm x 850 μm , low phase noise of the recovered clock (-112 dBc/Hz at 1-MHz offset), and low-power consumption of 70 mW from a 1.8-V supply further enhance the significance of the design as an attractive solution to the 10-Gb/s applications.

Finally, the half-rate PD circuit was also tested in a fully integrated half-rate CDR design example. The design of a quadrature VCO is also described as part of this implementation. A low power of 85 mW from a 1.8-V supply and a low phase noise of -114 dBc/Hz at 1-MHz offset are among the main achievements obtained in this design. Using the previously calculated loop parameters from the full-rate version, the post layout simulations and the measurement results of the half-rate CDR indicate that the design satisfies the OC-192 jitter requirements.

9.2 Recommendations

Although the research on the feasibility of the CMOS CDR for SONET applications at and beyond 10 Gb/s has traveled a long way for the last 4-5 years, a number of issues still remain unaddressed.

The speed of the CMOS devices continuously doubles every one and a half year, but the supply voltage scaling -an inevitable consequence of the foretold trend- may work to the circuit designers' disadvantage. Alternatives to the conventional stacked circuit

structures should be ready at hand before attempting to design a new CDR in faster CMOS technologies with devices having 0.13- μm or 90-nm channel lengths. The drawbacks of the conventional topologies put aside, we believe that the performance of the existing OC-48 or OC-192 CDRs can be significantly enhanced if the proposed techniques are implemented in a state-of-the-art technology such as 90-nm CMOS instead of a 0.18 μm counterpart. The supply voltage scaling will reduce the power consumption and the compact size will result in lower fabrication cost.

As we have focused on improving the data recovery portion of the OC-192 receiver in this thesis, the integration of this CDR unit with a frequency acquisition loop can be investigated as a future work. The double-loop architecture will also be useful in meeting the jitter transfer bandwidth specification of 120 kHz if the system is intended to be used as a repeater block. The method of supply voltage variation of the VCO can then be optimized for such a complete receiver system. Extra care should be exercised when dealing with digital and analog blocks on the same substrate as the digital circuits introduce significantly high switching noise and this noise can be carried to the analog section via the low-resistive silicon substrate.

The proposed improvements can also be applied to higher bit-rate standards such as OC-768 (40 Gb/s) as long as the technology allows such a migration. The half-rate CDR can be particularly useful at such a high data rate. We should, however, note that the proposed circuit structures do not alter the speed of the devices; they rather make *better* use of the available speed. Therefore, the CMOS technology that will be employed for an OC-768 application should, at least theoretically, be capable of achieving the minimum speed requirements of the application.

The methods to integrate the whole CDR should be further investigated. One cannot rely on the conventional filtering techniques even when using a highly sophisticated 90-nm CMOS technology. Use of external filter capacitors with such technology just does not get along well to fulfill the dream of fully integrated CDR systems in CMOS. The burden should be shared by the two research areas: 1) The device engineering that can improve the quality and the density of the on-chip passive components, and 2) the circuits and systems engineering to introduce new techniques to integrate whatever components are available.

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