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Monolithic Integration of Si-CMOS and III-V-on-Si Through Direct Wafer Bonding Process

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ABSTRACT Integration of silicon-complementary metal oxide-semiconductor (Si-CMOS) and III-V compound semiconductors (with device structures of either InGaAs HEMT, AlGaInP LED, GaN HEMT, or InGaN LED) on a common Si substrate is demonstrated. The Si-CMOS layer is temporarily bonded on a Si handle wafer. Another III-V/Si substrate is then bonded to the Si-CMOS containing handle wafer. Finally, the handle wafer is released to realize the Si-CMOS on III-V/Si substrate. For GaN HEMT or LED on Si substrate, additional wafer bonding step is required to replace the fragile Si (111) substrate after high temperature GaN growth with a new Si (001) wafer to improve the robustness of the GaN/Si wafers. Through this substrate replacement step, the bonded wafer pair can survive the subsequent processing steps. The monolithic integration of Si-CMOS + III-V devices on a common Si platform enables new generation of systems with more functionality, better energy efficiency, and smaller form factor.

INDEX TERMS Integration, wafer bonding, III-V/Si, Si-CMOS.

I. INTRODUCTION

The miniaturization of silicon (Si) complementary metal-oxide-semiconductor (CMOS) devices which is the key booster for device performance in the semiconductor industry is now reaching fundamental and economic bottlenecks [1], [2]. Further shrinking of CMOS devices is believed to result in unreliable, variation-prone and more expensive devices [3], [4]. To address these challenges, a paradigm shift has occurred in the industry from dimensional scaling alone to materials innovation. One such example is the introduction of SiGe, Ge or III-V compound semiconductor materials, as they have unique properties for faster speed and lower power computation applications. III-V compound semiconductors have higher electron mobility than Si, they are also a suitable candidate for the fabrication of high-electron-mobility transistors (HEMTs) [5]–[8]. In addition, most of the III-V compound semiconductors are direct bandgap materials. They can be used as a hybrid light source in a silicon photonics platform in order to enhance the performance and design flexibility of optical interconnects [9]–[12]. Such III-V/Si hybrid devices would compensate for the poor ability of Si to emit light and open up new circuit capabilities and applications beyond communication such as sensing and optical computation.

Unfortunately, III-V bulk substrates present very high acceptance barrier to Si foundries as they impose a higher risk of cross-contamination. In addition, the wafer sizes of III-V materials are usually smaller (6 inches or smaller) and this results in a higher cost per -device/-chip during processing/production. Hence, this work focuses on the monolithic integration of III-V compound semiconductors and Si-CMOS on a common Si substrate. Through this approach, the cross-contamination issue can be addressed and mass production can be realized as we can leverage well-established Si-CMOS technology and business models. Most importantly, the heterogeneous integration of III–V devices with Si-CMOS on Si substrates will enable the realization of integrated circuits that take advantage of the superior

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performance of III–V devices and the high integration density of Si-CMOS, which opens up ample opportunities for new circuit applications and capabilities in the RF, mixed-signal, and optical spaces [13]–[19].

In the conventional hybrid approach, Si and III–V circuits are fabricated and packaged separately, and then assembled on a carrier substrate (e.g., PCB). This approach is confronted by long interconnect distances and high losses, which affect performance, form factor, power consumption, cost, and complexity. For III/V-Si hybrid integration, direct epitaxial growth of III-V compounds on Si substrates allows for III-V and Si CMOS devices to be closely-spaced for integration. Recently, Si-CMOS/InP HBT/Si (001) [20] and Si-CMOS/GaN HEMT/Si (111) [13] hybrid wafers have been demonstrated successfully, but special starting wafers are required. For the Si-CMOS/InP HBT/Si (001), silicon on lattice-engineered substrate (SOLES) which contains a buried Ge template layer for enabling the direct growth of high-quality III–V epitaxial material in windows directly on the Si substrate is required. Conversely, a modified SOI substrate with Si (001) as top layer, and Si (111) as substrate, is used in Si-CMOS/GaN HEMT/Si (111) work. The process flows to realize the Si-CMOS+III-V devices in both cases are: (i) fabrication of SOLES or the modified SOI substrates through fusion bonding, (ii) fabrication of Si-CMOS devices; (iii) formation of III-V windows; (iv) epitaxial growth of III-V materials in the windows; (v) fabrication of III-V devices; (vi) formation of multilayer interconnects. Some of the known drawbacks of this approach are: (i) inability to process the CMOS and III-V materials separately, hence cross-contamination might become an issue, (ii) different starting wafers need to be prepared, and (iii) sub-optimal III-V growth temperatures in the windows to avoid high temperatures typically used for III-V growth (i.e., 600-800°C for III-As/P growth and $1000-1300$°C for III-N growth), which would severely degrade the CMOS transistors.

On the other hand, wafer bonding is another promising approach to integrate III-V materials on Si substrates [21]–[24]. In this work, wafer bonding is utilized in a different process flow to integrate III-V/Si substrates and Si-CMOS wafers on common platforms to realize novel side-by-side hybrid circuits, all within a single chip, while avoiding the exposure of the Si CMOS devices to high III-V growth temperatures. Building on previous work [21], [22], this study demonstrates for the first time the integration of functional Si-CMOS devices on SOI wafers and III-V device layers on Si substrates. All wafers are 200 mm in diameter. The III-V device layers can be either InGaAs HEMT, AlGaInP LED, GaN HEMT or GaN LED. The challenges of integration will be discussed and addressed in this study as well.

II. EXPERIMENT

Several sets of wafers were prepared: (i) Si (001) wafers, (ii) functional Si-CMOS devices on SOI substrates that have undergone front-end-of-line (FEOL) processing only in Si foundries, Fig. 1 (a), (iii) InGaAs HEMT or AlGaInP LED device structures on GaAs/Ge/Si (001) wafers, and (iv) GaN HEMT or LED on Si (111) wafers. The Si-CMOS/SOI substrates used in this study consisted of Si (1 μm) and buried oxide (BOX, 0.4 μm by thermal oxidation) layers. The InGaAs HEMT and AlGaInP LED epitaxial films were grown directly on the GaAs/Ge/Si (001) wafers with 6° off-cut toward the [110] direction. The GaN HEMT and LED epilayers were grown on Si (111) substrates. All III-V epilayers were grown by metalorganic chemical vapor deposition (MOCVD), and all wafers used were 200 mm in diameter. The details of these growths have been published in previous reports [25]–[30].

In our process, a 500 nm oxide layer was deposited onto the Si-CMOS/SOI wafer by plasma-enhanced chemical vapor deposition (PECVD). Additional densification was carried out to eliminate the residual gas molecules and by-products incorporated into the layer during oxide deposition. The densification process was carried out at 600 °C in N_2 environment. After densification, the oxide surface was planarized by chemical mechanical planarization (CMP). The SOI (after PECVD oxide deposition and CMP) and Si handle wafers were subjected to O_2 plasma exposure, followed by rinsing them with deionized water and then spin drying in a spin rinse dryer (SRD). O_2 plasma exposure increase the surface hydrophilicity (water droplet surface contact angle $<5°$) of the dielectric. The rinsing step is necessary to clean the wafers surfaces and to populate the surface with hydroxyl (OH) groups at a sufficiently high density to initiate wafer bonding. The post-bonding annealing of the bonded wafer pair was carried out at 300 °C in an atmospheric pressure N_2 ambient for 3 hours to further increase the bond strength (Fig. 1 (b)). The Si substrate from the SOI wafer was then removed by a combination of mechanical grinding and wet etching in tetramethylammonium hydroxide (TMAH) solution. Prior to wet-etching in the TMAH solution, the back side of the Si handle wafer was protected with a protective film. Since the BOX layer acted as an etch-stop layer, the Si-CMOS layer was temporarily attached to the Si handle wafer as depicted in Fig. 1 (c).

The BOX layer was then removed and replaced with PECVD oxide (with densification and planarization) and PECVD Si_3N_4 (with densification) layers as illustrated in Fig. 1 (d) [21], [22] to address issues with pinholes and outgassing. The III-V/Si wafers (InGaAs HEMT, AlGaInP LED, GaN HEMT or GaN LED wafers) were also subjected to the same PECVD oxide and nitride deposition processes. After that, the Si-CMOS-handle wafer was bonded to one of the III-V/Si substrates, as shown in Fig. 1 (e). Similar grinding and wet-etching processes were carried out to remove the Si handle wafer to realize the Si-CMOS/III-V/Si wafer depicted in Fig. 1 (f). The overall process flow is schematically summarized in Fig. 1.

An infrared (IR) camera was used to verify the bonding quality of the bonded wafer pair after the first and second bonding processes. Since the materials are transparent to IR,

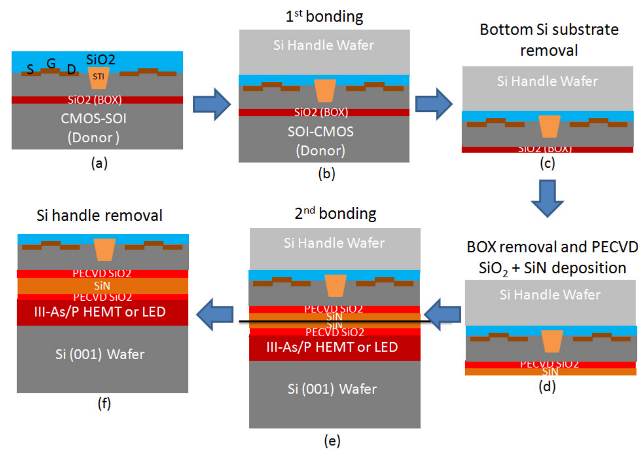

FIGURE 1. Schematic of the process flow to realize the integrated CMOS + III-As/P HEMT or LED on a common Si (001) wafer. (a) Si-CMOS on a SOI wafer. (b) First wafer bonding between the Si-CMOS on SOI and a Si handle wafers. (c) Removal of the Si substrate from the SOI wafer. (d) Removal of the BOX layer and deposition of SiO_2 and SiN layers. (e) Second wafer bonding between the Si-CMOS-containing handle and a III-As/P HEMT or LED wafer. (f) Removal of the Si handle to realize the integrated Si-CMOS on III-As/P HEMT or LED wafer.

interfacial voids can be observed by transmitting IR light through one side of the bonded wafer pair and observing from the other side with an IR camera. Transmission electron microscopy (TEM) with an operating voltage of 200 kV was used to examine the bonding interfaces.

III. RESULTS AND DISCUSSION

A. SI-CMOS + INGAAS HEMT OR ALGAINP LED WAFER

The bonding quality of the first bonded wafer pair between Si-CMOS/SOI wafer and Si handle wafer is inspected by the IR camera as shown in Fig. 2 (a). The bonding is excellent with no observable voids or particles found from the IR image.

The Si from the SOI wafer was then ground down to 50 μm and the remaining Si was etched chemically in TMAH solution (Fig. 1 (c) of the overall process). The wafer was immersed in the TMAH for a longer duration to make sure that the Si was completely removed. Although TMAH is known to have excellent selectivity over thermal oxide, the extended exposure to TMAH results in the presence of pin-holes on the exposed BOX surface. The defects will lead to unsuccessful bonding with multiple voids in the subsequent wafer bonding steps. To address this problem, we discovered that replacing the BOX layer with a PECVD SiO_2 layer was the most effective way as compared with other methods.

The defective BOX layer was completely removed in HF solution (HF : H_2O = 1: 10) and replaced with a PECVD oxide layer. CMP was carried out to smoothen the PECVD oxide layer. A thin PECVD Si_3N_4 film was then deposited and densified on the smoothened PECVD oxide layer. The thin nitride layer can prevent outgassing (such as in the case of direct PECVD oxide to PECVD oxide bonding) which generates voids at the bonding interface. After that, the wafer was bonded to an InGaAs HEMT or AlGaInP LED wafer (after similar oxide, nitride deposition and densification processes were carried out on the latter wafer as described above). The bonding quality is excellent and no observable voids are found from the IR image as shown in Fig. 2(b). Fig. 2(c) shows that the Si-CMOS + AlGaInP LED wafer has excellent bonding yield after the Si handle is removed.

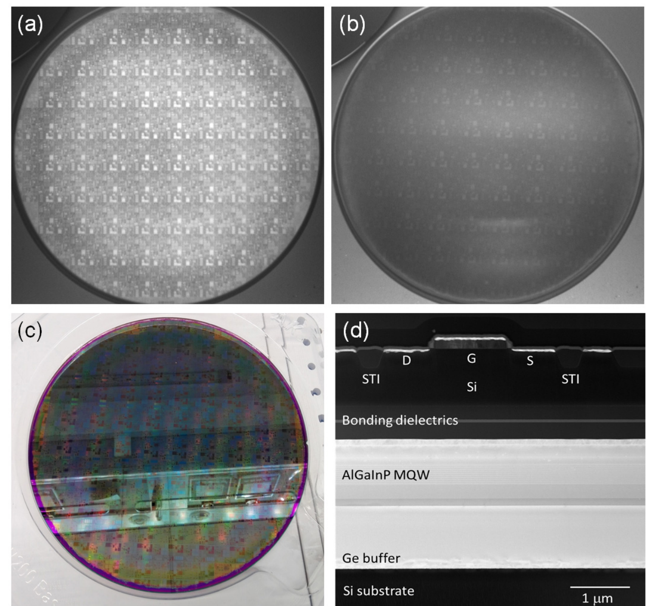

FIGURE 2. Infrared (IR) images of (a) the first bonding between a Si-CMOS/SOI wafer and a Si handle wafer and (b) the second bonding between the bonded Si-CMOS containing handle and an AlGaInP LED wafer. From the IR images, no observable voids are found in the bonded wafer pair. (c) Photograph of the bonded Si-CMOS + AlGaInP LED wafer after the Si handle is removed. (d) Cross-sectional TEM image of the bonded Si-CMOS + AlGaInP LED wafer. All data shown are from 200 mm diameter wafers.

The cross-sectional TEM image in Fig. 2(d) shows the layer stack of Si-CMOS + AlGaInP LED after the removal of the Si handle wafer from the second bonding. No micro voids were observed at the bonding interface between the two PECVD Si_3N_4 layers. This indicates that a uniform and flawless bond was established successfully at the microscale level.

Non-destructive characterization techniques, such as high-resolution x-ray diffraction (HRXRD) and wafer curvature measurements, were used on the wafers before and after the wafer bonding processes to confirm that the properties of the AlGaInP LED wafer were not affected by the wafer bonding processes. From the reciprocal space map (RSM) as shown in Fig. 3, the peak positions and full-widths at half maximum (FWHMs) of the p-AlGaInP, Ge+GaAs, and n-AlGaInP layers are not altered significantly after the wafer bonding processes, thereby confirming that the film integrity was not compromised.

The wafer curvatures of the as-received Si-CMOS wafer (+84μm), as-grown AlGaInP LED wafer (−51μm), and

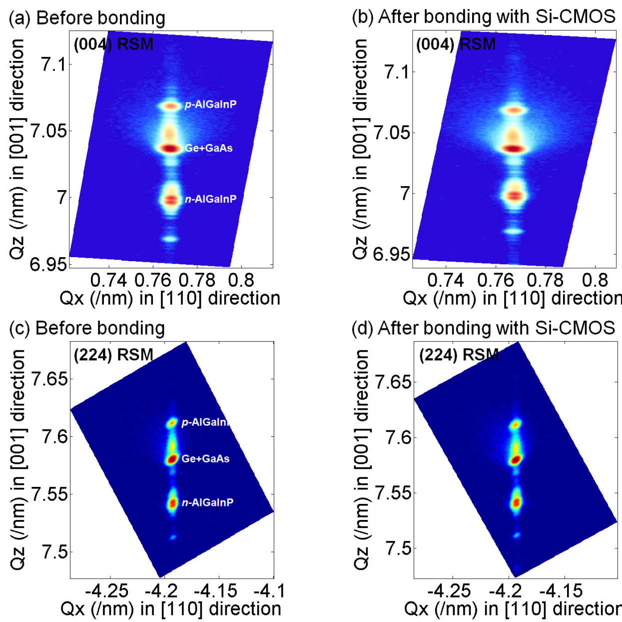

FIGURE 3. **Symmetric (004) reciprocal space map (RSM) of a AlGaInP LED structure (a) before and (b) after wafer bonding measured from high resolution X-ray diffraction (HRXRD). (c), and (d) are the asymmetric (224) RSM of an AlGaInP LED structure before, and after wafer bonding, respectively.**

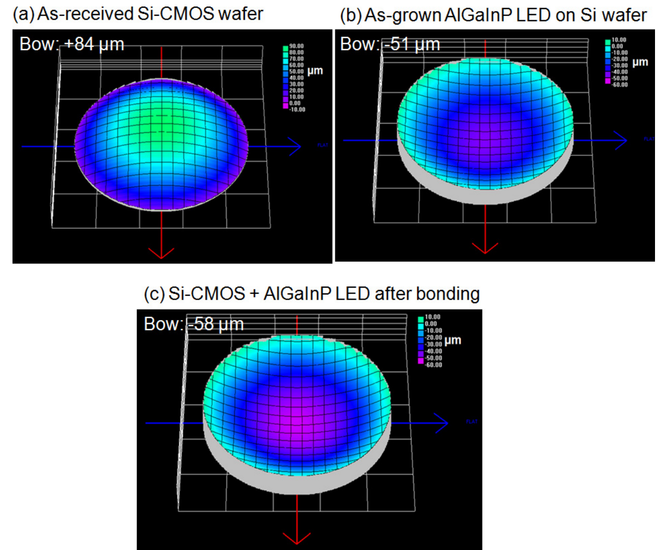

FIGURE 4. **Wafer curvature measurements on the (a) as-received Si-CMOS wafer, (b) as-grown AlGaInP LED wafer and (c) Si-CMOS + AlGaInP LED wafer.**

Si-CMOS+AlGaInP LED wafer (−58μm) after the wafer bonding processes are shown in Fig. 4. The wafer curvature of the Si-CMOS+AlGaInP LED wafer is still within the specification of ± 75 μm which is one of the prerequisites for re-entry of the wafers into CMOS foundries' back-end-of-line (BEOL) processes.

After the successful demonstration of the integration of Si-CMOS + AlInGaP LED, the next step is to fabricate the AlInGaP LED devices and send the integrated wafers back to the Si foundries for BEOL processes to interconnect the Si-CMOS and AlGaInP LED devices together. The preliminary results related to the electrical and optical properties of these integrated devices are discussed. In particular, we investigated the effects of the thermal processing (up to 750 °C) used for our wafer bonding on the Si-CMOS (Si-CMOS on Si wafers processed by both FEOL and BEOL processes, 750 °C for 30 seconds × 2 cycles) and AlInGaP LED wafers (600 °C for 12 hours).

For Si-CMOS, the electrical tests were based on the foundry's proprietary test structures. We studied the changes in key 0.18 μm CMOS device parameters, such as V_t, I_{dsat}, I_{off}, and BV for 1.8 and 3.3 V MOS devices, respectively, and R_{sh} for poly resistors. The additional thermal processing budget led to a < 3% variation from the foundry baseline in all the key parameters, confirming that the wafer bonding process flow that we have developed in this work is compatible with the 0.18 μm CMOS used.

Photoluminescence (PL) spectra at a fixed input laser power of 20 mW of the AlGaInP LED wafer before and after the thermal processing are shown in Fig. 5(a). A minor shift of the peak wavelength from 664.9 nm (before) to 665.6 nm (after) was observed which is within the wavelength non-uniformity (± 2 nm) across the entire 200 mm wafer. *I-V* characteristics and electroluminescence (EL) spectra of the AlGaInP LED wafer before and after the thermal processing are shown in Fig. 5(b) and (c), respectively. After thermal processing, a higher leakage current as well as higher operating current were observed. The ideality factor was degraded slightly from 1.34 (before) to 1.43 (after). The EL intensity of the AlGaInP LED wafer after thermal processing was enhanced. Most importantly, a negligible peak emission wavelength shift from 666.4 nm to 667.2 nm was observed. We believe that the degradation that is observed in the *I-V* curves could be due to several factors, e.g., process variations between the samples during the device fabrication, sensitivity of As/P material systems to high temperature treatments, etc. Hence, from the negligible peak wavelength shift and slight degradation in the *I-V* performance, we can conclude that the thermal processing may causes minor changes to the AlInGaP LED devices' performances.

B. SI-CMOS + GAN HEMT/LED WAFERS

Although similar preparation and bonding steps as described in Section III-A were carried out to demonstrate the integration of Si-CMOS + GaN HEMT/LED wafers, ∼ 50% of the GaN HEMT/LED wafers were fragile and broke during the processes. This is mainly because the robustness of the Si (111) wafers were weakened and they becomes brittle after high temperature GaN growth due to slip line formation at the wafer edge as shown in Fig. 6. The slip lines originate from the edge of the wafer and propagate toward the center of the wafer. Minimizing radial temperature differences across the 200 mm Si wafer during growth through the optimization of heater zone settings is one key way to

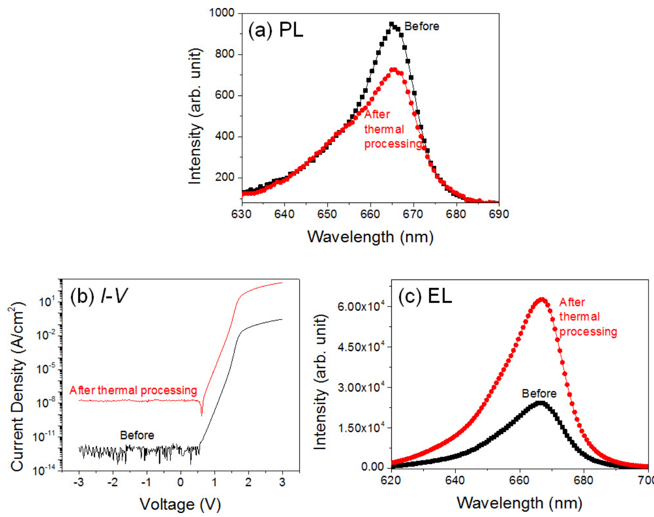

FIGURE 5. (a) Photoluminescence (PL), (b) I-V, and (c) electroluminescence (EL) measurements of the AlGaInP LED samples before and after the thermal processing.

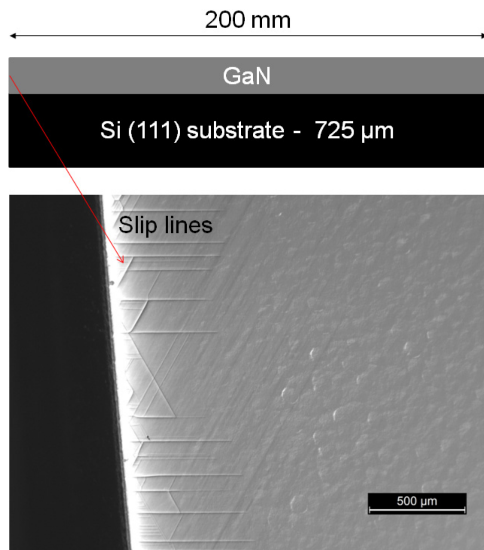

FIGURE 6. Schematic illustration of the structure of GaN/Si substrate and Nomarski microscopic image of edge region of the GaN/Si wafer. The slip lines originate from the edge of the wafer and propagate toward the center of the wafer.

reduce slip line formation and wafer fragility, but it is not possible to fully eliminate vertical temperature differences through the wafer as heating is only performed on the backside of the wafer in our MOCVD reactor. Thus, in almost all cases, wafer fragility remains an issue due to the high growth temperatures involved in III-nitride on Si epitaxy. Additionally, the AlGaN buffers and subsequent GaN layers contribute different levels of stress and build up the stress levels on the Si (111) substrate which ultimately makes the Si substrate even more fragile.

In order to address this issue, the fragile Si (111) substrate can be replaced by a new Si (001) substrate through another wafer bonding step. A PECVD SiO_2 layer was deposited

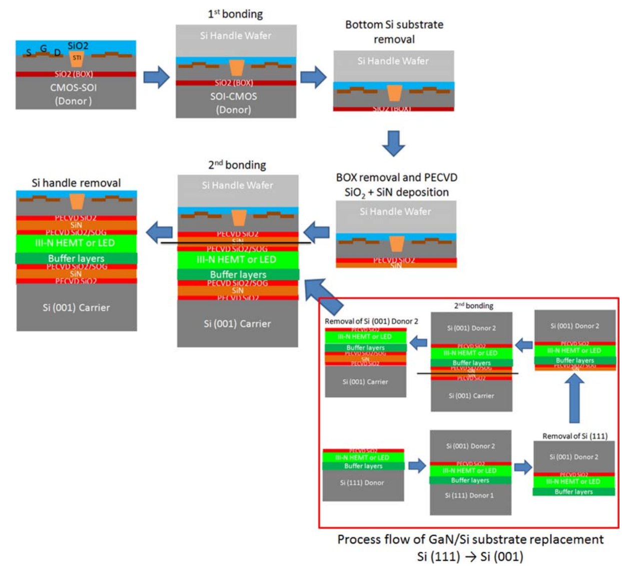

FIGURE 7. Schematic of the updated process flow to realize the integrated Si-CMOS + III-N HEMT or LED on a common Si (001) wafer. The Si (111) substrate of the III-N HEMT or LED wafer is replaced by a fresh Si (001) wafer.

onto the GaN HEMT/LED on the Si (111) wafer. After that, densification and CMP processes were carried out. A Si donor wafer was then attached to the GaN HEMT/LED wafer and then the bonded wafer pair was annealed. The Si (111) substrate was removed through mechanical grinding and wet-chemical etching. In this case, HNA solution (hydrofluoric + nitric + acetic acids) was used to remove the remaining Si (111) substrate. The III-N buffer layers are now exposed. These buffer layers can be removed, depending on application or process requirements. The buffer removal step can further reduce the stress levels and improve the robustness of the final GaN HEMT/LED on Si (001) wafer. Subsequently, another PECVD SiO_2 film was deposited on the GaN HEMT/LED-containing Si donor and Si (001) carrier substrates. Similar densification, CMP and PECVD nitride deposition steps were carried out. The two wafers were then bonded together and annealed. The Si donor wafer was removed to realize the GaN HEMT/LED on a fresh Si (001) carrier substrate. The GaN HEMT/LED on the Si (001) wafer was then bonded to the Si-CMOS-containing handle wafer and the handle wafer was removed to realize the Si-CMOS + GaN HEMT/LED wafer. The overall process flow, specially designed for the Si-CMOS + GaN HEMT/LED–on–Si (001) substrates, is schematically shown in Fig. 7.

Through this substrate replacement method, whereby the Si (111) wafer was replaced by the Si (001) wafer, the wafer breakage rate of the GaN HEMT/LED on the Si (001) substrate is reduced drastically, from 50% (before) to 0% (after) without removal of the buffer layers. Hence, the GaN HEMT/LED wafers can be handled and processed using regular process steps without the need for additional precautions.

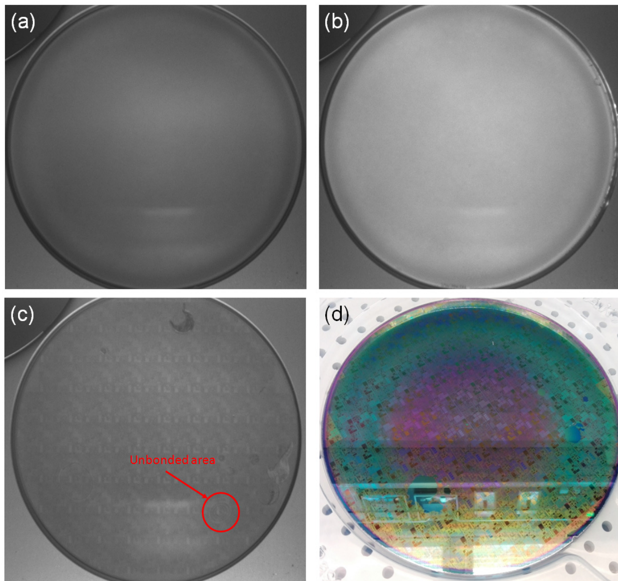

FIGURE 8. Infrared (IR) images show (a) first bonding between a GaN HEMT-on-Si (111) substrate and a Si donor wafer and (b) second bonding between the GaN-HEMT-donor and a fresh Si (001) carrier wafer. From the images, no observable voids are found in the bonded wafer pair. (c) IR image and (d) photograph of a bonded Si-CMOS + GaN HEMT wafer (with substrate replacement process) with 200 mm diameter Si (001) substrate. From the images, the overall bonding quality is degraded with some trapped particles between the bonded pair and further improvement is required.

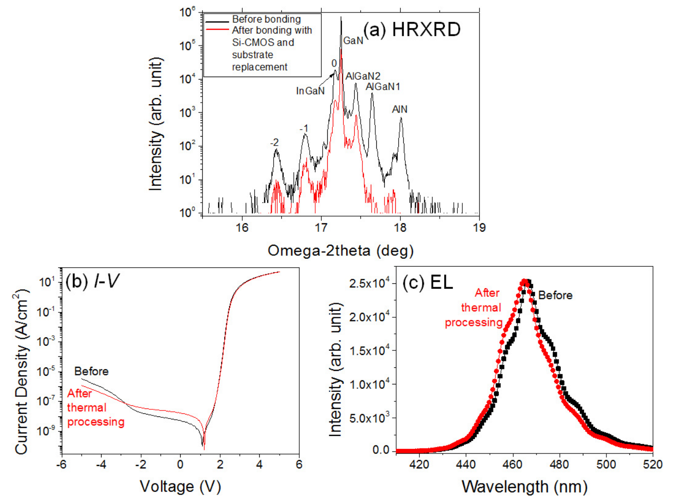

FIGURE 9. (a) Symmetric (002) high resolution x-ray diffraction (HRXRD) of a GaN LED structure before and after wafer bonding processes with Si-CMOS and substrate replacement. (b) I-V, and (c) electroluminescence (EL) measurements of the GaN LED samples before and after the thermal processing.

Fig. 8 (a) and (b) show the IR images of the first bonding and second bonding of the substrate replacement process. The bonding is excellent with no observable voids or particles found from the IR images. Fig. 8 (c) shows the IR image of Si-CMOS-containing handle wafer + GaN HEMT wafer on Si (001) substrate and some unbonded areas are observed after 4 bonding steps due to the presence of undesired particles. The corresponding photo after the Si handle wafer was removed is shown in Fig. 8 (d). The unbonded areas shown in Fig. 8 (c) were peeled off after the Si handle was removed. In the research environment, particles are one of the main challenges. However, particle count can be controlled to a sufficiently low level to build integrated circuit prototypes using optimized cleaning and handling methods. Fortunately, modern wafer bonding equipment minimizes particles due to reduced human handling, controlled clean environments and *in-situ* cleaning.

From the HRXRD analysis shown in Fig. 9 (a), the peak positions of the InGaN MQWs, GaN, AlGaN 2 layers are not altered significantly after the wafer bonding processes (with Si-CMOS and substrate replacement). However, AlGaN 1 and AlN layers are removed unintentionally during the removal of the Si (111) substrate in HNA solution. *I-V* and EL of the GaN LED wafer before and after the thermal processing (600 °C for 12 hours) are shown in Fig. 9 (b) and (c), respectively. Similar *I-V* characteristics and ideality factor of 1.68 are achieved. In addition, similar EL intensity with a negligible shift in peak wavelength from 466.2 nm to 464.6 nm is observed which is within the peak wavelength variation (± 1.4 nm) across the diameter of the 200 mm GaN LED–on–Si wafer. Hence, from these results, we concluded that the thermal treatments do not affect the GaN LED devices' performances in any significantly way.

Through direct wafer bonding processes, integration of Si-CMOS and III-V compound materials on a common Si substrate become possible. III-V devices and Si CMOS devices are integrated for the first time in similar fashion and scale as traditional VLSI/ULSI CMOS devices. This paves the way for new circuits and applications such as ultra-efficient circuits for handheld, mobile or remote applications; self-sensing and self-tuning/self-configuring circuits; RGB (red, green, blue) micro-LED arrays with control circuitry, etc.

IV. CONCLUSION

In summary, monolithic integration of Si-CMOS and III-V compound semiconductors on a common Si substrate has been demonstrated successfully. Defects on the BOX can be overcome by replacing the BOX layer with PECVD SiO_2 and Si_3N_4 layers and void-free bonding can be achieved. The fragility of the GaN HEMT/LED on Si (111) wafers can be addressed by replacing the Si (111) substrate with a fresh Si (001) substrate. Although two additional bonding steps are involved, the yield is improved significantly. Monolithic integration offers the ability to use different materials for different circuit and device components of a system, allowing different circuit functional blocks to be optimized, therefore leads to overall improvement in performance of a system in terms of speed, power consumption, and form factor.

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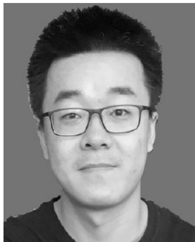

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