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Characterisation and Modeling of Chemical Mechanical Planarization (CMP) for Deep Submicron Integrated Circuit (IC) Fabrication

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A thesis submitted to the Nanyang Technological University
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Doctor of Philosophy

2006

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TABLE OF CONTENTS

Title Page

Acknowledgement.....i

Table of Content.....iii

Abstract.....vi

List of Figures.....vii

List of Tables.....xi

List of Symbols.....xii

Abbreviation.....xiv

CHAPTER 1: INTRODUCTION 1

1.1 Background.....1
1.2 History of CMP.....2
1.3 Overview of CMP.....3
1.3.1 What is CMP?.....3
1.3.2 Why use CMP?.....5
1.3.2.1 Global Planarization..... 5
1.3.2.2 Step Coverage.....7
1.3.2.3 Multilayer Interconnection.....8
1.3.2.4 Inlaid process.....9
1.3.3 Integration of CMP.....10
1.4 Role and Challenges of CMP in Semiconductor Manufacturing..... 10
1.5 Research Objectives.....11
1.6 Thesis Organization.....12
1.7 Summary.....13

CHAPTER 2: FUNDAMENTALS REVIEW AND EMPIRICAL MATERIAL REMOVAL RATE 14

2.1 Introduction.....14
2.1.1 CMP tool.....15
2.1.2 Polyurethane Pad..... 15
2.1.3 Slurry.....17
2.1.4 Carrier.....18
2.1.5 Dresser.....20
2.1.6 Wafer.....20
2.1.7 End point detection (EPD) system.....21
2.1.8 Other influencing factors.....22

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2.2 Material Removal Rate in CMP....23
2.2.1 Material Removal Rate model....23
2.3 Kinematics of CMP Process....29
2.3.1 Kinematics derivation....29
2.3.2 Simulation of the effects of relative velocity components....33
2.4 Material Removal Rate of Polysilicon CMP process....36
2.4.1 Experimental Descriptions....37
2.4.2 Experimental Observations....38
2.5 Summary....46

CHAPTER 3: DIRECT SHALLOW TRENCH ISOLATION CHEMICAL MECHANICAL PLANARIZATION 47

3.1 Introduction....47
3.2 Shallow Trench Isolation (STI)....48
3.2.1 Role of silicon nitride layer....50
3.3 STI CMP....51
3.3.1 Selectivity....52
3.3.2 Nitride loss (Erosion)....52
3.3.3 Dishing....53
3.3.4 Active Dummy....54
3.3.5 Reverse Mask....55
3.3.6 Direct STI CMP....55
3.4 Experimental Descriptions....55
3.4.1 Architecture, functions and settings of the system components....56
3.4.1.1 Carrier (Head)....58
3.4.1.2 Polyurethane Pad....59
3.4.1.3 Slurry Mobile Cart....60
3.4.1.4 Mix in Place Slurry System (MIPSS)....61
3.4.1.5 On Track....62
3.4.2 Ceria based slurry....64
3.4.2.1 Test method for weight content....64
3.4.2.2 Test method for specify gravity....65
3.4.2.3 Test method for viscosity....65
3.4.2.4 Test method for pH....65
3.4.2.5 Test method for particle size (abrasive only)....65
3.4.3 Wafer preparation....66
3.4.3.1 Blanket wafers....66
3.4.3.2 Pattern wafers....66
3.5 Results....72
3.5.1 Blanket removal rate and non-uniformity of SiO2 and CeO2 slurry...75
3.5.1.1 Setup for platen 1 (silica based slurry)....75
3.5.1.2 Setup for platen 2/3 (ceria based slurry)....77
3.5.2 Particles contaminations from SiO2 and CeO2 slurry....82
3.5.3 Non-uniformity within wafer (NUWIW)....84
3.5.3.1 Post STI-CMP: Silicon nitride NUWIW distribution....84
3.5.3.2 Post STI-CMP: Trench oxide NUWIW distribution....86
3.5.4 Non-uniformity within die (NUWID)....88
3.5.4.1 Post STI-CMP: Silicon nitride NUWID distribution....89

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3.5.4.2 Post STI-CMP: Trench oxide NUWID distribution................91
3.5.5 Silicon nitride loss................92
3.5.6 Dishing................95
3.5.7 Roughness................97
3.5.8 Metal contaminations................99
3.5.9 Electrical test results................99
3.6 Summary................101

CHAPTER 4: CMP PROCESS MODELING: CONTACT MECHANICS APPROACH 103

4.1 Introduction................103
4.2 Polyurethane Pad Surface Characterization................104
4.2.1 Statistical Parameters: Moments of a Probability Distribution................106
4.2.2 Measurement Results................107
4.3 Real Contact Area between Wafer and Polyurethane Pad................110
4.3.1 Simulations results................113
4.3.2 Experimental Observations................117
4.3.3 Discussion................119
4.4 Methodology Development................120
4.4.1 Blanket removal thickness (BRT)................120
4.4.2 Process Capability................122
4.4.3 Experimental Description and Results................123
4.4.3.1 Off-line monitoring................125
4.4.3.2 On-line Implementation................128
4.4.4 Discussions................129
4.5 Potential Issue: Subsurface Stress................130
4.6 Summary................134

CHAPTER 5: CONCLUSIONS AND FUTURE WORK 136

5.1 Material Removal Rate................137
5.2 Selectivity................139
5.3 Repeatability................141
5.4 Future Work................143

PUBLICATION & INVENTIONS

APPENDIX A: CS03-039, CMP Polishing Heads Retaining Ring Groove Design for Microscratch Reduction

APPENDIX B: Metrology Tools

BIBLIOGRAPHY

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Characterization and Modeling of Chemical Mechanical Planarization (CMP) for Deep Submicron Integrated Circuit (IC) Fabrication

ABSTRACT

Chemical mechanical planarization (CMP) also known as chemical mechanical polishing has emerged as the fastest growing operation in the semiconductor manufacturing industry. It is expected to show equally explosive growth in the future [1]. CMP is the only known visible technology so far that can achieve the requirements of providing the global planarized thin film surface on wafer substrate. However, the CMP process still faces challenges such as material removal rate, uniformity of post thickness, selectivity, repeatability and defect for its successful implementation in deep submicron IC fabrication. Characterization and modeling are needed to address a variety of concerns in CMP applications. This thesis identifies and directs towards alleviating some of these major issues as highlighted in the following three paragraphs that associated with application of CMP in ultra large scale integrated (ULSI) circuit manufacturing.

Beginning with the material removal rate, a wide range of new materials are expected to be employed in fabricating high-performance IC devices. Thus, this has motivated the need to verify CMP material removal rate models. Studies show the inadequacies of existing removal rate models in describing polysilicon material which is used to fill the deep trenches in bipolar complementary metal-oxide-semiconductor (BiCMOS) fabrication. A more general and versatile empirical material removal rate at the practical regime is proposed for CMP application in IC fabrication. The model is statistically evaluated by the cross-validation method which shows the predictive capability of the model.

Selectivity is a crucial parameter as CMP is employed to remove more than one type of material concurrently and coupled with a wide range of pattern density. Conventional silica based slurry being unable to effectively planarize the oxide after trench filling and stopping on the silicon nitride. Therefore, reverse masking and etching are needed prior to shallow trench isolation (STI) CMP. The characterization work of direct STI CMP with ceria based slurry to eliminate non-value-added processes is reported in this thesis. Performances in terms of non-uniformity post thickness within wafer (NUWIW), non-uniformity post thickness within die (NUWID), nitride loss, dishing, roughness, metal contamination, and electrical properties of both approaches are documented.

The requirement to consistently achieve the specific target mean film thickness for CMP applications is becoming more and more stringent as device geometry continues to shrink. In addition, cost and cycle time are the driving forces to avoid rework. A methodology based on contact mechanics modeling approach is developed to predict the optimal process time. It captures the variation of incoming wafer thickness, material removal rate and random behavior due to the CMP process environment. Experimental works show this approach offers better control of the average thickness for various types of devices with C_p and C_{pk} value above 1. Potential issues involving CMP applications in the near future advanced IC fabrication are highlighted for the first time through this contact mechanics modeling approach.

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LIST OF FIGURES

Fig. 1. 1 The Evolution of the IC 2
Fig. 1. 2 CMP Equipment's main components (EBARA) 4
Fig. 1. 3 DOF vs wavelength 6
Fig. 1. 4 Planarization distance of planarizing techniques [4]. 6
Fig. 1. 5 Cross Section of Aluminum interconnection 8
Fig. 1. 6 Gate and interconnect delay vs feature size [7]. 9
Fig. 1. 7 Planarization Potential Solutions Outline [7]. 10

Fig. 2. 1 Complexity of CMP Process. 14
Fig. 2. 2 Schematic diagram and performance of advance retaining ring of the carrier [23]. 19
Fig. 2. 3 Effect of TTV of wafer on non-uniformity [27]. 20
Fig. 2. 4 Copper removal rate as a function of product of 22
Fig. 2. 5 Layout of coordinate systems and motion for: 30
Fig. 2. 6 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and both rotate in the same direction 33
Fig. 2. 7 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and both rotate in the same direction 34
Fig. 2. 8 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and rotate in the opposite direction 34
Fig. 2. 9 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and rotate in the opposite direction 35
Fig. 2. 10 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and rotate in the same direction with carrier oscillates across the polyurethane pad. 35
Fig. 2. 11 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and rotate in the same direction with carrier oscillates across the polyurethane pad. 36
Fig. 2. 12 Deep trench in BiCMOS process 37
Fig. 2. 13 Hole configurations for carrier. 38
Fig. 2. 14 Effects of hole configurations on non-uniformity of material removal rate across wafer 38
Fig. 2. 15 Material removal rate data of polysilicon with hole configuration A fit across various models 40
Fig. 2. 16 Material removal rate data of polysilicon with hole configuration B fit across various models 41
Fig. 2. 17 Material removal rate data of polysilicon with hole configuration C fit across various models 42

Fig. 3. 1 Two different schemes of STI CMP 47
Fig. 3. 2 Bird's beak encroachment limits the scaling of channel widths. 48

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Fig. 3. 3 Process sequence used to form STI: a) etch trench in silicon substrate; b) grow thermal oxide trench liner to improve trench Si/SiO_2 interface; c) fill trench with HDP-CVD oxide; d) use CMP to planarize and stop at nitride layer; e) strip nitride to leave the STI structure 49
Fig. 3. 4 Post STI CMP after nitride strip. Elevation or step height: Height between isolated and active area. Divot: Erosion depth at the interfaces. (Courtesy: Chartered Semiconductor Manufacturing Ltd) 50
Fig. 3. 5 a) Cross section after block + planarizing resist; b) Cross section after RIE etch, showing local oxide spikes; c) Measured oxide step heights before and after CMP, showing fast removal rate of such spikes; d) Fundamental problem of "CMP-only" process. [37] 51
Fig. 3. 6 Cross section TEMs of the polysilicon gate for two different STI step heights.(a) large step height (b) small step height [63] 53
Fig. 3. 7 Origin of the dishing effect in CMP (a) polishing pad flexes into the trench opening (b) formation of concave surface. (c) trench area remains "dished" after planarization 54
Fig. 3. 8 Layout of equipment setting 56
Fig. 3. 9 Mirra with On Track Integra 57
Fig. 3. 10 Schematic diagram of retaining-ring/pad/wafer/membrane interaction [20] 59
Fig. 3. 11 Slurry Mobile Cart 60
Fig. 3. 12 MIPSS a) Machine layout b) Mix and dispense reservoirs c) Control panel 62
Fig. 3. 13 PVA brush 63
Fig. 3. 14 Layout of active and isolation of a die 67
Fig. 3. 15 Various trench sizes within a die. 68
Fig. 3. 16 Process monitoring location. 68
Fig. 3. 17 SRAM 69
Fig. 3. 18 Pad oxide and nitride deposition 70
Fig. 3. 19 Active and isolation definitions. 71
Fig. 3. 20 STI trench formation 71
Fig. 3. 21 STI depositions. 72
Fig. 3. 22 Solid concentration vs stirring time. 73
Fig. 3. 23 Diameter scan for pre, post thickness and removal rate. 75
Fig. 3. 24 Polar map-49pts scan. 76
Fig. 3. 25 Removal rate vs no of wafer. 77
Fig. 3. 26 Diameter scan for pre, post thickness and removal rate for platen 2/3. 78
Fig. 3. 27 Polar map-49pts scan for platen 2/3. 78
Fig. 3. 28 Removal rate vs no of wafer for platen 2/3. 79
Fig. 3. 29 Step height ratio 80
Fig. 3. 30 Delta and post thickness across a wafer. 81
Fig. 3. 31 Particle contaminations 83
Fig. 3. 32 NUWIW of Silicon nitride for a)Direct STI CMP b)Reverse Mask CMP 85
Fig. 3. 33 Repeatability and margin of NUWIW of silicon nitride. 86
Fig. 3. 34 Incoming wafer structures. 87
Fig. 3. 35 NUWIW of trench oxide for a) Direct STI CMP b) Reverse Mask CMP. 87
Fig. 3. 36 Repeatability and margin of NUWIW of trench oxide 88
Fig. 3. 37 Big pad 89
Fig. 3. 38 NUWID of Silicon nitride for a) Direct STI CMP b) Reverse Mask CMP. 90

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Fig. 3. 39 Repeatability and margin of NUWID of silicon nitride. 90
Fig. 3. 40 NUWID of trench oxide for Direct STI CMP and Reverse Mask CMP ... 91
Fig. 3. 41 Repeatability and margin of NUWIW of silicon nitride 92
Fig. 3. 42 Erosion at isolated structures. a) Direct STI CMP for isolated structure at center b) Direct STI CMP for isolated structure at edge c) Reverse mask STI CMP for isolated structure at center d) reverse mask STI CMP for isolated structure at edge 93
Fig. 3. 43 Si3N4 loss for both direct and reverse mask STI CMP 94
Fig. 3. 44 Si_3N_4 thickness across different active structures dimensions for both direct and reverse mask STI CMP 94
Fig. 3. 45 Dishing at process monitoring structures. a) Direct STI CMP for 120μm oxide trench at center b) Direct STI CMP for 120μm oxide trench at edge c) Reverse mask CMP for 120μm oxide trench at center d) Reverse mask CMP for 120μm oxide trench at edge 95
Fig. 3. 46 Dishing at dense structures. a) Direct STI CMP for 0.4μm oxide trench at center b) Direct STI CMP for 0.4μm oxide trench at edge c) Reverse mask CMP for 0.4μm oxide trench at center d) Reverse mask CMP for 0.4μm oxide trench at edge 96
Fig. 3. 47 Dishing for Wide Trench 97
Fig. 3. 48 Dishing for Narrow Trench 97
Fig. 3. 49 Surface roughness. a) Surface roughness at center using silica based slurry b) Surface roughness at edge using silica based slurry c) Surface roughness at center using ceria based slurry d) Surface roughness at edge using ceria based slurry 98
Fig. 3. 50 TXRF analysis of metal contents for post CMP wafers 99
Fig. 3. 51 STI Elevation after Poly deposition 100
Fig. 3. 52 Electrical STI thickness and its variation for both schemes of processes 100
Fig. 3. 53 Vt vs Id plot for both schemes of processes. 101

Fig. 4. 1 Schematics diagram of CMP process. 104
Fig. 4. 2 Typical trace profile of the polyurethane pad 105
Fig. 4. 3 Perforated Polyurethane Pad Measurement 108
Fig. 4. 4 Mean line distribution 108
Fig. 4. 5 Height asperity distribution 109
Fig. 4. 6 Curvature asperity distribution 109
Fig. 4. 7 Interface between patterned wafer and polyurethane pad. 111
Fig. 4. 8 Separation distance (*d*) and contact area ratio as the function of applied pressure. 114
Fig. 4. 9 Interface pressure as the function of applied pressure 114
Fig. 4. 10 Abrasives on the asperity 115
Fig. 4. 11 *d* as the function of step height over a range of applied pressure 116
Fig. 4. 12 Contact pressure difference as the function of step height 116
Fig. 4. 13 Step height profile in typical process monitoring structures 118
Fig. 4. 14 Step height evolution 118
Fig. 4. 15 Material removal rate at both lands and trenches locations 119
Fig. 4. 16 Evolution of P_{land} and P_{trench}. 121
Fig. 4. 17 Removal rate diagram 121
Fig. 4. 18 Typical ILD and IMD layers in IC device 124
Fig. 4. 19 Blanket material removal rate profile in Ebara-222 CMP tool 124
Fig. 4. 20 Comparison of wafer to wafer variation for Device A. 126

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Fig. 4. 21 Comparison of wafer to wafer variation for Device B 127
Fig. 4. 22 Wafer to wafer variation for four different devices by using *BRT* methodology 128
Fig. 4. 23 Typical C_p and C_{pk} value for two different device without implement the *BRT* methodology 129
Fig. 4. 24 A simple run-to-run controller for CMP process............ 130
Fig. 4. 25 Principal stress distribution and contours of principal shear stress underneath............ 132
Fig. 4. 26 Cracks are found underneath the wafer surface after CMP process........ 133
Fig. 4. 27 Cracks are found on both surface and subsurface 133
Fig. 4. 28 Unrepeatable end point trace on patterned wafer. 135

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LIST OF TABLES

Table 2. 1 Impact of pad properties on CMP performances [15] 16
Table 2. 2 Material removal rate models for CMP applications............................... 29
Table 2. 3 Cross validation for hole configuration A 45
Table 2. 4 Cross validation for hole configuration B.. 45
Table 2. 5 Cross validation for hole configuration C.. 45

Table 3. 1 Input parameters setting for experiments.. 58
Table 3. 2 Properties of IC1010 pad [67]. 59
Table 3. 3 Mixing Ratio test 61
Table 3. 4 Recipe for brush cleaning. 63
Table 3. 5 Recipe for spin station 64
Table 3. 6 Properties of ceria abrasive and additive. 73
Table 3. 7 Mixing ratio test result... 74

Table 4. 1 Recipe for the process 125

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LIST OF SYMBOLS*

A = area

a_s = contact area form by single asperity

a_r = radius of contact area by single asperity

C_p = capability potential

C_{pk} = process capability

D = data set

d = separation distance

d_{mh} = metal height

E = estimation set

E = Young's modulus

E^*= effective Young's modulus

F = force

h = step height on wafer surface

J = total moving distance, mm

K_p= Preston's constant coefficient

k_1= system constant

k_2= imaging constant

k = extinction coefficient

Ku = kurtosis

L = scan length

l = interconnect metal line length

M_n =moments

m = mean line

N = total number of measurements

N_w = rotational speed of wafer, rpm

N_p = rotational speed of pad, rpm

NA= numerical aperture

n = nano unit, 10^{-9}

n_e = electron density

n_i = index of refraction

P = pressure, psi

p = probability density

R = radius from pad center

R_{res}= resolution of photolithography

RR = removal rate

r = radius from wafer center

r_c = radius of local contact sport region

r_{cc} = distance between center of the pad and wafer

S = selectivity

Sk = skewness

T = test set

t = time

t_{thick} = metal thickness

V = average relative velocity

V_p = velocity of platen

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$V_{r,w}$ = radial velocity components of wafer

$V_{\theta,w}$ = angular velocity components of wafer

$V_{r,p}$ = radial velocity components of pad

$V_{\theta,p}$ = angular velocity components of pad

$V_{r,R}$ = radial velocity components of relative velocity of the wafer to pad

$V_{\theta,R}$ = angular velocity components of relative velocity of the wafer to pad

$V_{\theta,average}$ = average relative velocity of angular component

$V_{r,average}$ = average relative velocity of radial component

V_R = magnitude of relative velocity

V_{th} = threshold voltage

X_j = product of P^2V

$\hat{Y}_j$ = prediction of removal rate

y = single measurement

$\bar{y}$ = average value of measurement

Z = profile height

z = height of asperity from mean line

Å = angstrom unit, 10^{-10}

β = radius of curvature

ε_o = permittivity of free space

κ = dielectric constant

κ_c = curvature

η = asperity density

ρ = interconnect metal resistivity

μ = micron unit, 10^{-6}

ν = Poisson's ratio

θ = angle

α = area fraction

α_j, β_j = estimated coefficient

ϕ_z = asperity height distribution

ϕ_β = asperity curvature distribution

σ = standard deviation

σ_r, σ_θ, σ_z = principal stress along z-axis

τ_l = principle shear stress

ω_w = angular velocity of wafer

ω_p = angular velocity of pad

λ = escape depth

λ_{exp} = exposure wavelength

%wt = weight percent

*** Unless otherwise specified, the symbols employed in this thesis are as described.**

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ABBREVIATION

AEP	Advanced edge performance
AFM	Atomic Force Microscopy
APC	Advanced process control
BEOL	Back End On Line
BPSG	Borophosphosilicate glass
BRT	Blanket removal thickness
CMOS	Complementary metal oxide silicon
CMP	Chemical Mechanical Planarization / Polishing
CRS	Chemical resist strip
DF	Down force
DI	Deionized
DOF	Depth of focus
DRAM	Dynamic random access memory
EBIC	Electron beam induced current
FEOL	Front End On Line
HDP	High Density Plasma
HDPCVD	High Density Plasma Chemical Vapour Deposition
HF	Hydrofluoric acid
HPR	High pressure rinse
HRP	High Resolution Profiler
HSS	High selectivity slurry
IC	Integrated circuit
ILD	Inter layer dielectric
IMD	Inter metal dielectric
ISRM	In-situ removal monitor
LOCOS	Local oxidation of silicon
LPCVD	Low Pressure Chemical Vapour Deposition
MEMS	Micro-electromechanical system
MIPSS	Mix in place slurry system
MOSET	Metal oxide silicon field effect transistor
NTRS	National Technology Roadmap for Semiconductors

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NUWID	Non-uniformity within die
NUWIW	Non-uniformity within wafer
PECVD	Plasma Enhanced Chemical Vapour Deposition
PETEOS	Plasma Enhanced Tetra-ethly-ortho- silicate
PME	Process Monitoring
PRS	Plasma resist strip
PSD	Position sensitive detector
PVA	Polyvinyl alcohol
PVD	Physical Vapour Deposition
RC	Resistance and capacitance
RCA	Radio Corporation America
RIE	Reactive Ion Etching
RM	Reverse mask
ROI	Return on investment
SC	Standard clean
SE	Spectroscopic Ellipsometry
SEM	Scanning Electron Microscopy
SHR	Step height ratio
SOG	Silicon On Glass
SRAM	Static random access memory
STI	Shallow Trench Isolation
TEOS	Tetra-ethly-ortho- silicate
TTV	Total thickness variation
TXRF	Total-Reflection X-Ray Fluorescence
ULSI	Ultra large-scale integration
USG	Undoped Silicon Glass

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CHAPTER 1

INTRODUCTION

1.1 Background

The first transistor, a point contact type was invented before the Christmas of 1947. John Bardeen and Walter Brattain from AT&T Bell Laboratories demonstrated a solid-state electrical device made from germanium. The integrated circuit (IC) era arrived in 1958 when Jack Kilby observed that discrete devices like resistors, capacitors diodes and transistors could be made from a piece of semiconductor material, silicon. In 1961, Fairchild Semiconductor made the first commercially available integrated circuits (Robert Noyce's Chip) on ~10mm diameter silicon wafer. It used the basic process techniques such as photolithography and etch of modern IC chips. Since then the IC industry developed rapidly. In 1964, Gordon Moore from Intel Corporation noticed that the number of components on a chip doubled every year, while the price stayed the same. This prediction becomes well known in the semiconductor industry as Moore's law. Since the 1970s, the use of microelectronics has been increasing at an exponential rate. Semiconductor manufacturing is probably one of the most challenging and complicated of the new technologies that have developed in the last half of twentyth century [1]. The complexity of the construction of today's device designs remains one of the miracles of the technological age and the demand for speed has pushed technology since the start, and continues to do so today (Figure 1.1). As devices are scaled to deep submicron dimension and additional levels are added to multilevel-interconnection schemes in ICs, the required degree of planarization process is increased. Chemical and mechanical planarization/polishing (CMP) is currently being used in the fabrication of state-of-art integrated circuits and has been identified as an enabling technology for not only multi-layer interconnection in the back end on line (BEOL) but trench isolation in the front end on line (FEOL) as well. CMP used for deep submicron fabrication differs from conventional polishing and lens fabrication processes. A high degree of planarity and uniformity is required with a very low material removal rate (~2000Å/min) and tighter tolerances (+/- 800Å). In addition, the surface generated should be free from scratches under load and free

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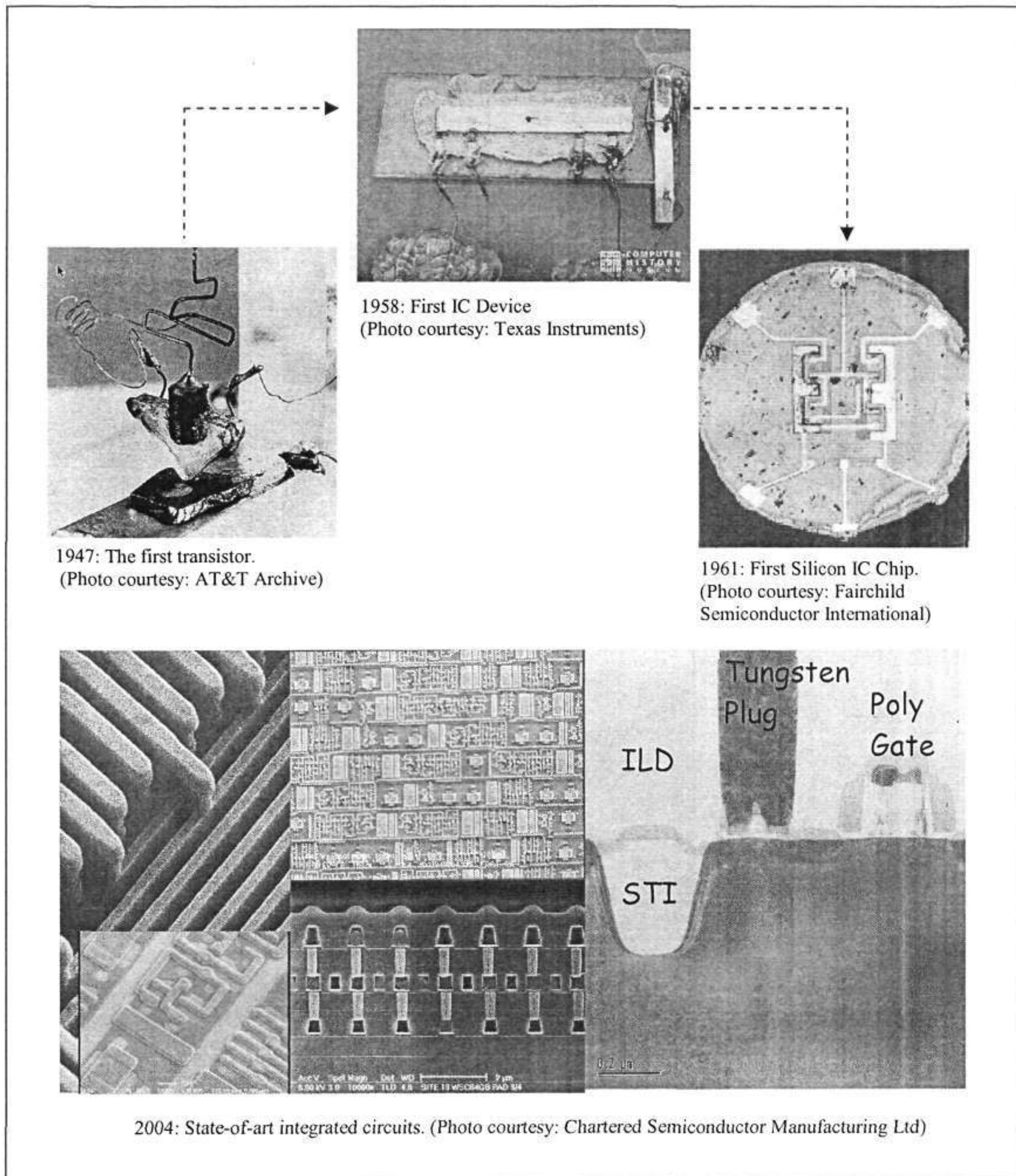
from contamination after delivering thousands of abrasives onto the wafer surface through the slurry.



1947: The first transistor. (Photo courtesy: AT&T Archive)

1958: First IC Device (Photo courtesy: Texas Instruments)

1961: First Silicon IC Chip. (Photo courtesy: Fairchild Semiconductor International)

2004: State-of-art integrated circuits. (Photo courtesy: Chartered Semiconductor Manufacturing Ltd)

Fig. 1. 1 The Evolution of the IC

1.2 History of CMP

" You want to take my wafer and do what?!" was the reaction evoked when taking a very old and dirty technology such as polishing and applying it to leading edge chips [2]. However, polishing has now becomes a critical and important process technology

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for achieving device technologies smaller than 0.35μm. The original IBM development work on CMP was undertaken at East Fishkill, New York, around 1983, in what was referred to as the Base Technology Lab. Research and development was exclusively performed within IBM until 1988. IBM decided to share some CMP data with Intel as Intel microprocessors were selected for IBM's PC product line. At that time the dynamic random access memory (DRAM) market was dominated by Japanese manufacturing companies. IBM was wary of having to rely entirely on foreign suppliers for such a critical component of its computer system. Hence, IBM elected to help strengthen a domestic DRAM supplier- Micron Technology by teaching them about the CMP process. Information about CMP was included in the process for the 4 MB DRAM that IBM sold to Micron Technology. Motorola was introduced to CMP through the Power-PC microprocessor project, a joint venture of IBM, Motorola and Apple Computer. In 1989, IBM also published the first paper on the CMP of oxide films [3]. These events initiated the rapid proliferation of CMP throughout the IC industry.

1.3 Overview of CMP

Unlike other IC fabrication process, CMP is a relatively new semiconductor manufacturing process technology, which is becoming a standard fabrication step at an increasing number of semiconductor companies. The main driver behind CMP is the promise of lower overall cost per function and/or cost per chip. Having the ability to increase functionality per square centimeter allows the manufacturer to sell chips at a higher than average selling price without increasing the cost of silicon. In addition, the manufacturing can achieve a cost benefit from CMP by increasing the packing density of the device, resulting in more chips per wafer with minimal impact on process costs. CMP therefore has become widely accepted as the method that will enable chip manufacturers to build multilayer devices without compromising packing density.

1.3.1 What is CMP?

CMP is a method for planarizing an uneven topography surface. It is a material removal process achieved by chemically modifying the surface properties and

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mechanically removing the surface with high selectivity between height elevations of the surface. As shown in figure 1.2, a wafer is held on a wafer carrier or polishing head by means of vacuum during loading and the wafer is then rotated and pressed against a rotating porous polyurethane polishing pad attached to a rotating platen via carrier and back side pressure.

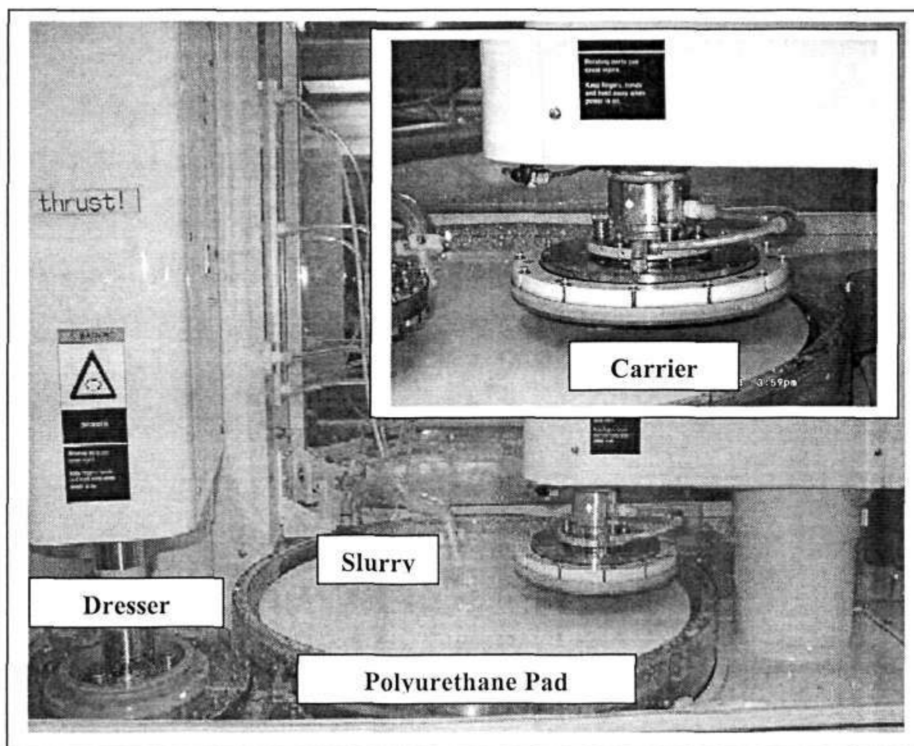

Fig. 1. 2 CMP Equipment's main components (EBARA)

(Photo courtesy: Chartered Semiconductor Manufacturing Ltd)

A retaining ring on the carrier is used to prevent slippage of the wafer from underneath the carrier during the process. The input pressure to the retaining ring is also used to control the removal rate at the edge of the wafer. The carrier may exhibit certain motion in addition to rotation. This is to reduce the variation of relative velocity between the center and edge of the wafer and utilize the whole pad area. Slurry composed of abrasives suspended in a chemical solution is dripped onto the pad during the process. Generally, material removal is achieved by chemical weakening the surface film followed by mechanical interaction with pad and abrasives. Over time, the pad surface becomes glazed which causes a decrease in the removal rate. Therefore, pad conditioning by a dresser is needed to keep the desired roughness on the pad.

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1.3.2 Why use CMP?

CMP is the process of choice for achieving local and global planarization to meet the more stringent lithographic requirements. CMP is the preeminent process for ultraprecision machining of composite materials that have layers with different mechanical properties [4].

1.3.2.1 Global Planarization

Reduced minimum features require higher-resolution photolithography. The resolution is determined by the wavelength and numerical aperture using Rayleigh's formula as shown in equation below.

$$R_{res} = k_1 \frac{\lambda_{\exp}}{NA} \qquad \textbf{1-1}$$

where R_{res} is the minimum dimension or resolution that can be printed, λ_{exp} is the exposure wavelength of the light and NA is the numerical aperture of the projection lens, which indicates the capability of the lens to collect the diffraction light and k_1 is a dimensionless system constant. On the other hand, the range in which the light is in focus and can achieve good resolution is called the depth of focus (DOF) and can be described by

$$DOF = k_2 \frac{\lambda_{\exp}}{(NA)^2} \qquad \textbf{1-2}$$

where k_2 depends on the criteria used to define acceptable imaging and on the type of features being imaged. Unfortunately, the resolution and DOF work oppositely. To print smaller features, one needs a shorter wavelength and/or a larger NA, which result in a reduction of DOF. As device size decreases, sensitivity to focus errors increase dramatically. With the required reduction in the wavelength of the light used for the photolithography to print smaller devices, the corresponding reduction in the available lithographic depth of focus demands improvement in the level of global planarization to maintain critical dimension control of all features over the die (figure

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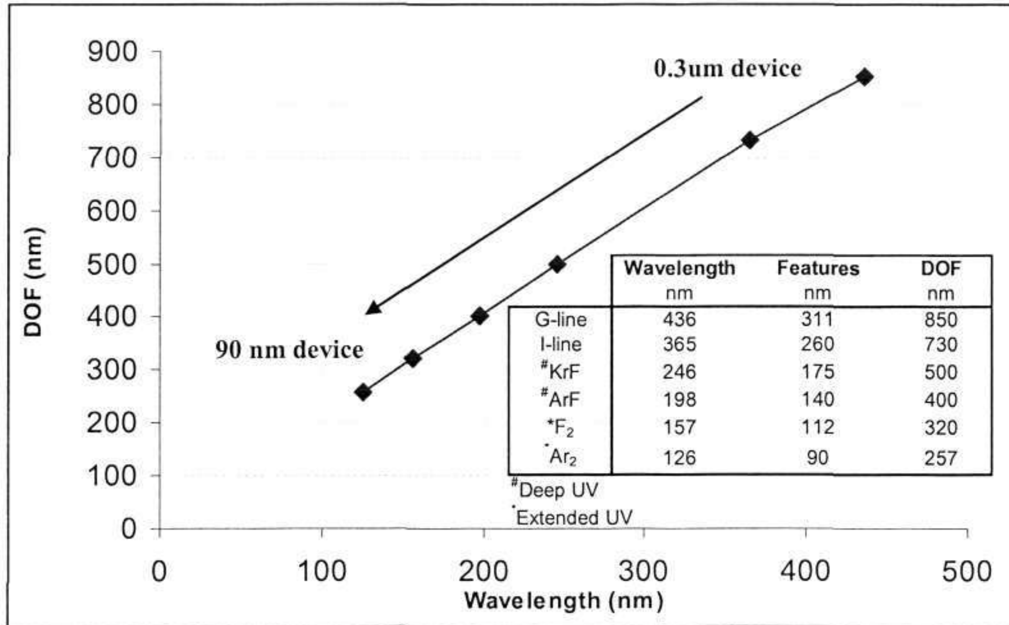
1.3). Meeting DOF requirement means meeting them over the area exposed by the photolithography in one focus adjustment; that is typically a square of ~20 mm on edge. CMP, because of its imposition of planarity external to the wafer itself, is thus far the only viable method of achieving planarity over the required distances.



	Wavelength nm	Features nm	DOF nm
G-line	436	311	850
I-line	365	260	730
#KrF	246	175	500
#ArF	198	140	400
*F_2	157	112	320
*Ar_2	126	90	257

Fig. 1. 3 DOF vs wavelength

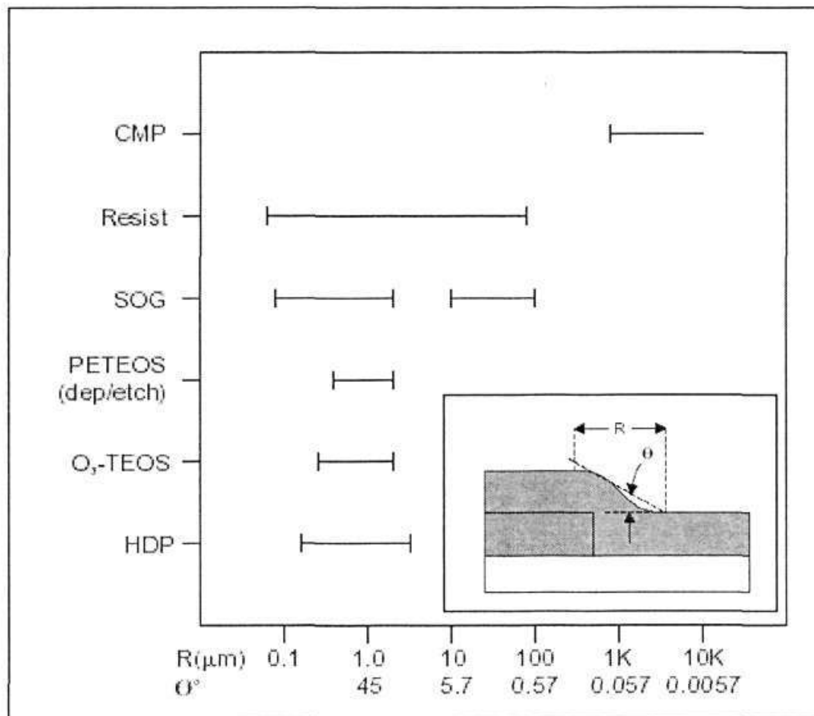


Fig. 1. 4 Planarization distance of planarizing techniques [5].

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In general, planarization techniques such as thermal flow, sacrificial-resist etchback, and spin on glass are inadequate for an interconnect system with more than three layers of metal. All of these techniques ultimately provide only a limited degree of smoothing and local planarization but are not able to provide global planarization [5-7] as shown in figure 1.4. The initial driving force for using CMP was the need for surface amplitudes to remain within the ever-decreasing DOF required by photolithography. Obviously, it is much easier to image fine-line geometries on a nearly flat surface than on a surface with a significant topography.

1.3.2.2 Step Coverage

CMP has additional value beyond the ability to improve the capability of the lithography process. CMP, due to its inherent step reduction, can significantly improve the result of subsequent metal deposition. For instance, step coverage is the capability of a deposition technique, particularly PVD aluminum, to deposit a conformal layer. This becomes more difficult with increased topography, especially as the number of metallization layers increases.

There are other methods that result in local smoothing of the topography to improve step coverage. Oxide thermal flow or reflow is one of them. During reflow the deposited dielectric is heated until it flows, smoothing the topography and filling the gaps. The main limitation of the thermal flow is the thermal budget. Once aluminum has been deposited on the wafer, reflow cannot be used, as the high temperature will melt the aluminum. In addition, even for the pre-metal dielectrics, the high temperatures can cause the dopant atoms in the transistor junctions to diffuse too far, limiting the use of this technique.

Another technique for planarization is a sacrificial layer etch back. This technique involves deposition of a dielectric over the metal lines. Then, a thick sacrificial layer of photoresist, spin-on-glass (SOG) or polyimide is deposited over the dielectric. Film is then smoothed by baking at temperature above 150^{0}C. A dry etch, such as reactive ion etching (RIE), is used to etch the sacrificial layer and the dielectric at the same time. The SOG etchback can also provide good gapfill capability. Both thermal flow and photoresist or SOG etchback are primarily driven by surface tension, and the lateral distance over which planarization takes place does not exceed about 100μm.

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1.3.2.3 Multilayer Interconnection

In general, five layer metallization with an inter metal dielectric (IMD) constant around 3 are designed for 0.25-0.18μm generation devices with aluminum as the interconnect material. As shown in figure 1.5, CMP is an enabling technology to achieve such architecture by providing planar surface at each layer.

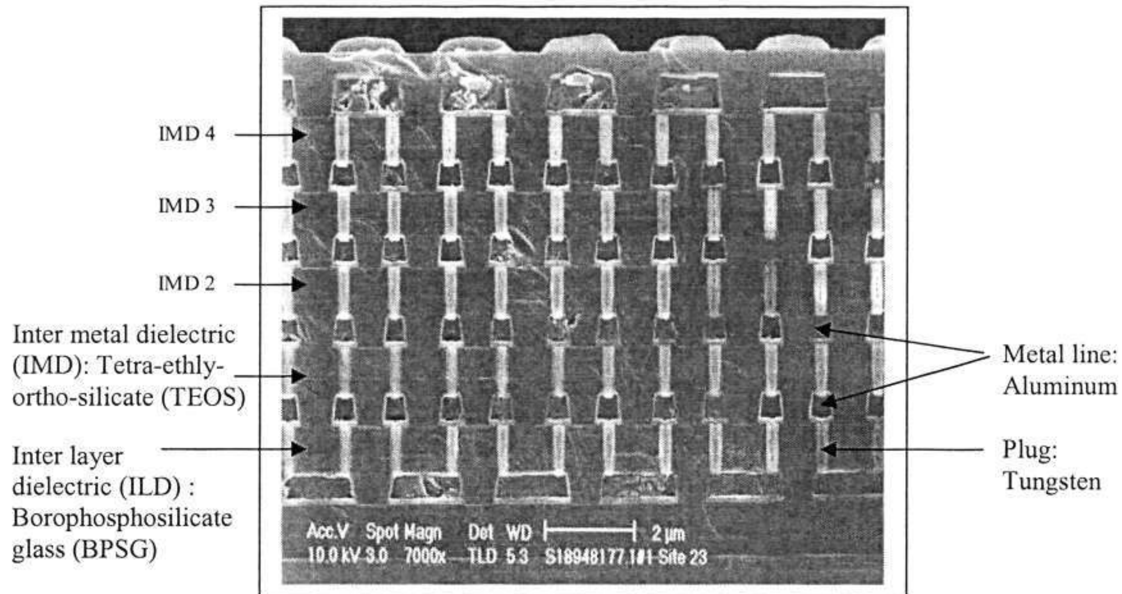

Fig. 1. 5 Cross Section of Aluminum interconnection.

(Photo Courtesy: Chartered Semiconductor Manufacturing Ltd)

The 1994 National Technology Roadmap for Semiconductors (NTRS) identified interconnects materials as the key to addressing the device performance bottleneck. Circuit speed is determined by interconnect resistance and capacitance (RC) delay, which can be express as follow

$$R_{\text{int}} C_{\text{int}}\ delay = \frac{\kappa \varepsilon_o \rho l^2}{t_{thick} d_{mh}} \quad \textbf{1-3}$$

where κ is the insulator dielectric constant, ε_o is the permittivity of free space, ρ is the interconnect metal resistivity, l is the interconnect metal line length, t_{thick} is the metal thickness and d_{mh} is the metal height. Figure 1.6 illustrates the introduction of copper and low dielectric constant (low-κ) materials into interconnect structures, which causes a significant decrease in the delay time. Thus, the semiconductor manufacturing industry has moved from aluminum towards copper as an interconnect material for 0.13μm generation and beyond by employing the dual damascenes

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process since copper practically does not form volatile compounds. Once again, this makes CMP an enabling technology and critical process in semiconductor manufacturing.

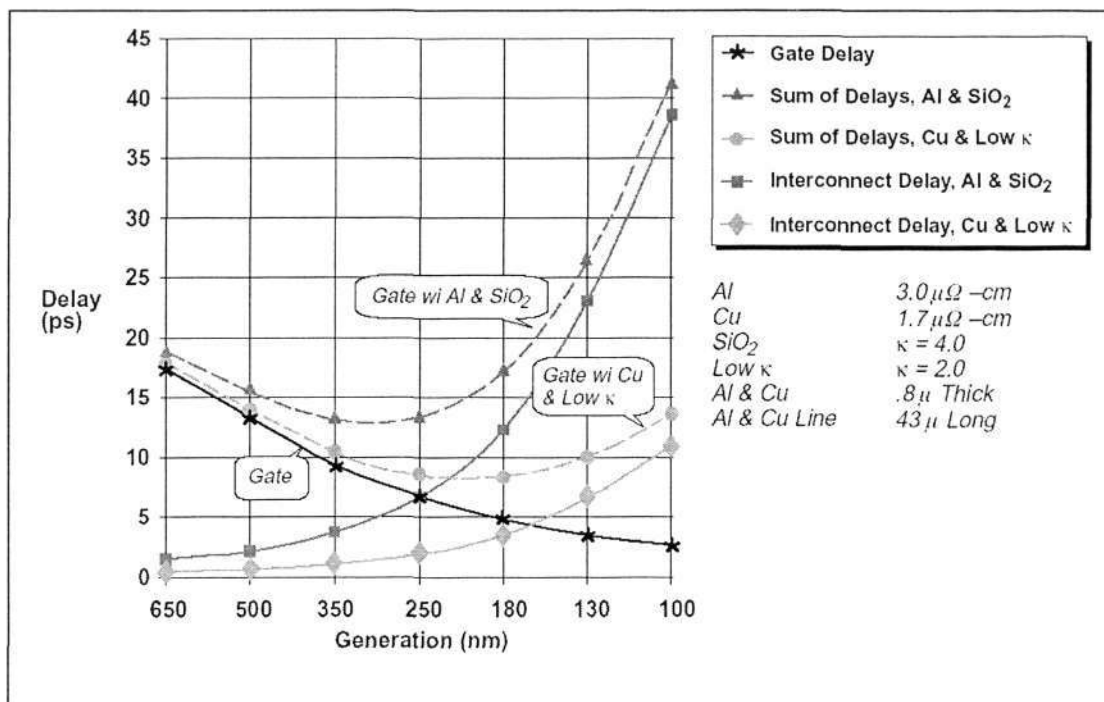

Fig. 1. 6 Gate and interconnect delay vs feature size [8].

1.3.2.4 Inlaid process

In the semiconductor industry, single damascene such as shallow trench isolation (STI) , deep trench isolation and tungsten plug; dual damascene structure such as copper interconnect structure as mentioned in the previous section are classified as inlaid processes. The technique has long been popular as an adornment to sword hilts and beautiful jewelry. The term damascene originates from Damascus, the capital of Syria. Today, this technique is widely used in advanced transistor fabrication. To produce the damascene, the thin film on wafer surface is first outlined with the structures to be inlaid and then etched away to form trenches or holes. After etching, the wafer surface is deposited with another thin film material that is required to fill the trenches. CMP is the only feasible solution so far in semiconductor manufacturing to realize the inlaid process by removing excess material that filled over the wafer surface so that material is embedded inside the trenches only.

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1.3.3 Integration of CMP

CMP is an inherently dirty process that can introduce yield-reducing defects to the wafer. Some early resistance to the adoption of CMP stemmed from contamination concerns. The CMP process therefore must be integrated with a reliable wafer cleaning system (Dry in, dry out concept). The current technology of choice for both oxide and metal CMP uses double sided brush scrubbing, although megasonics immersion has also been used. Such scrubbing must function reliably with bases (e.g. NH_4OH) , and acids (e.g. HF) in order to optimally remove both metals and mobile ions. Tribological metrology and active control may be fully integrated for active force and temperature control [9].

1.4 Role and Challenges of CMP in Semiconductor Manufacturing

The advent of CMP as one of the major process technologies has had a great impact on the semiconductor industry. Today, a typical high-end processor or graphics card undergoes 10 to 15 CMP processing step [10]. Despite its extensive use in semiconductor manufacturing recently, fundamentals are not yet well understood. Fundamental research for CMP in semiconductor manufacturing are expected as indicated in the 1997 NTRS as shown in figure 1.7.

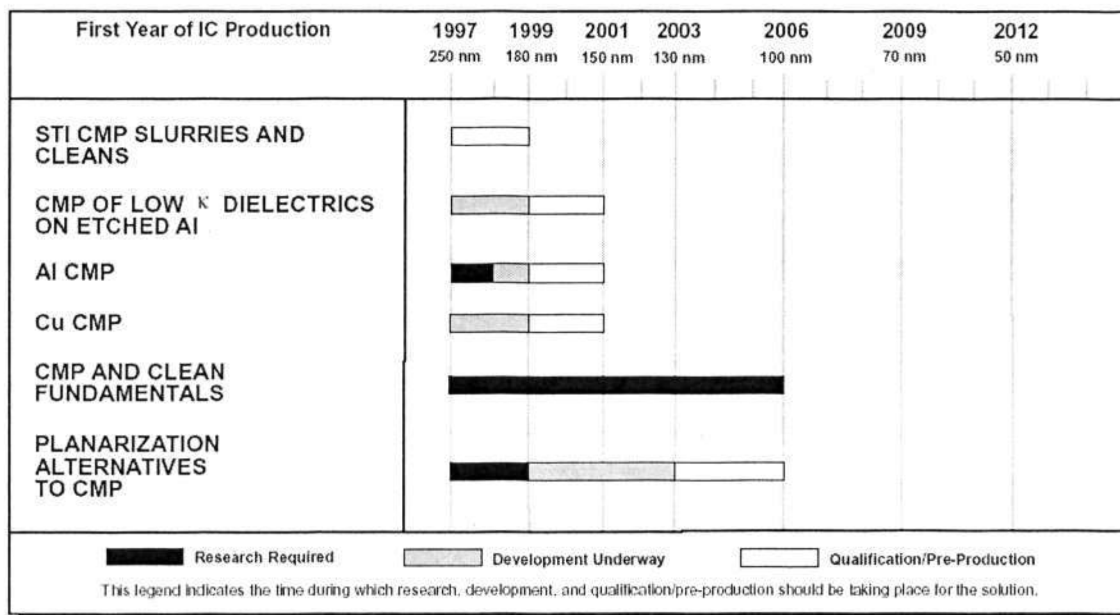

Fig. 1. 7 Planarization Potential Solutions Outline [7].

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CMP replaced others techniques and will remain the leading planarization technology in current and future transistors fabrication [8]. Selectivity and repeatability are two of the greatest challenges for all the processes in deep submicron fabrication to ensure a high production yield. Since CMP is the only feasible solution so far for the inlaid process, selectivity is the primary concern. Unlike, inter layer dielectric (ILD) or IMD CMP process, inlaid CMP process involves the removal of more than one type of material. The greatest challenge is to remove the overburden materials with the minimal loss of the underlying materials until all trenches are defined over wide range of the dimensions of the trenches. The problem is amplified by complex structures with various densities on the wafer surface and this is especially true in formation of STI in the FEOL. The CMP process is complicated by many factors, capability of repeatability in achieving the post target film thickness is another great challenge in CMP process. As wafer throughput and cycle time become increasingly important to the capacity constrained requirements of wafer production, rework of wafers becomes especially burdensome because it will affect the return on investment (ROI) and decrease the throughput.

1.1 Research Objectives

This thesis addresses some of the challenges associated with the CMP process in deep submicron fabrications. This is achieved by investigating the feasibility of direct STI CMP using ceria based slurry in order to remove non-value added process step as in the conventional approach. (Chapter 3 covers the details). Typically a manufacturer can save up to US$100 million a year by moving towards the direct CMP method [11]. Nitride thickness becomes more critical for gapfill in STI process due to high aspect ratio resulting from narrow and deep trenches as feature sizes get smaller and denser. On top of that, nitride and trench oxide thickness will determine the step height between active and isolation areas for transistors. Whereas ILD or IMD CMP, the *wafer-to-wafer* dielectric thickness variation makes subsequent processes more difficult (contact or via etch) and produces less predictable dielectric capacitance. Thus, *wafer-to-wafer* thickness variation is crucial for the CMP step. A general methodology for timing prediction to achieve a better thickness control based on contact mechanics model to address mechanical aspects of CMP is developed. This

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will help to improve process capability (C_p and C_{pk}) and reduce rework. This methodology is also useful as a guide in developing recipes to increasing throughput.

1.2 Thesis Organization

The report is divided into five chapters. The present chapter has given an overview of the CMP process in semiconductor manufacturing. In chapter 2, fundamentals of the CMP process will be first reviewed and followed by experiments to verify the adequacy of the basic blanket material removal rate equation with other models which have been reported in literature.

Conventional STI CMP with silica based slurry even with planarization aid (i.e. reverse mask) is unable to effectively planarize the oxide film after trench filling and stopping on a silicon nitride layer over wide pattern density variations in the die layout. Direct STI CMP with ceria based slurry will be covered in chapter 3. In this chapter, the conventional approach will be discussed. Experiments are conducted and comparative studies are made between the reverse mask and direct STI CMP schemes.

The contact mechanics approach to explore the interface contact between polyurethane pad and wafer is studied and presented in chapter 4. In this chapter, pad surface characterization is first made to investigate the geometrical properties of commercial polyurethane pad followed by statistical treatment to extract the parameters that are needed in the contact mechanics model. Local phenomenon on the wafer surface will be hypothesized, which the proposed methodology will be based on in predicting timing for the CMP process.

The thesis conclusion and future work are presented in Chapter 5. This chapter summarizes the main conclusions of the study while emphasizing the key contributions. Thoughts and recommendations on area for future work are also identified for successful CMP implementation in advanced IC fabrications.

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1.7 Summary

In this chapter, an introduction to CMP process in semiconductor manufacturing and area of this research is outlined. Planarization is the process of smoothing and planing surfaces. CMP is the process of smoothing and planing aided by chemical and mechanical forces. The "P" term also refers to polishing. However, in general, polishing is the process of smoothing the surface not necessarily planar. Hence, CMP for chemical mechanical planarization will be used in this thesis. One of the unique aspects of CMP is that the process was invented, developed, and put into application by the industry itself without any significant interaction with academic institutions. Consequently, the whole process is shrouded in secrecy, with most of the literature available being in the form of patents. A casualty of this approach has been the lack of a fundamental understanding of the CMP process. The lack is further compounded by the large number of input variables (>20) and output variables (>4) that need to be optimized. Time dependent contributions by some of these variables cause further complexities in the process. All of these factors have contributed to the impression that CMP is more of an art than science.

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CHAPTER 2

FUNDAMENTALS REVIEW AND EMPIRICAL MATERIAL REMOVAL RATE

2.1 Introduction

Unlike for semiconductor devices, the physics of many IC processes is still not well understood [12, 13]. This is especially true for CMP process due to it being a relatively new process [14] (less than 25 years) in IC fabrication. Coupled with a massive number of independent variables (as shown in figure 2.1) with all possible interactions between these parameters has made successful physics-based modeling to capture the problems completely in CMP process not feasible. This allows empirical or phenomenological based CMP models to play an important role for simulating process in IC fabrication. Nevertheless, understanding the fundamentals of the process is essential for optimal process design and control and thus has initiated research efforts from both industry and universities.

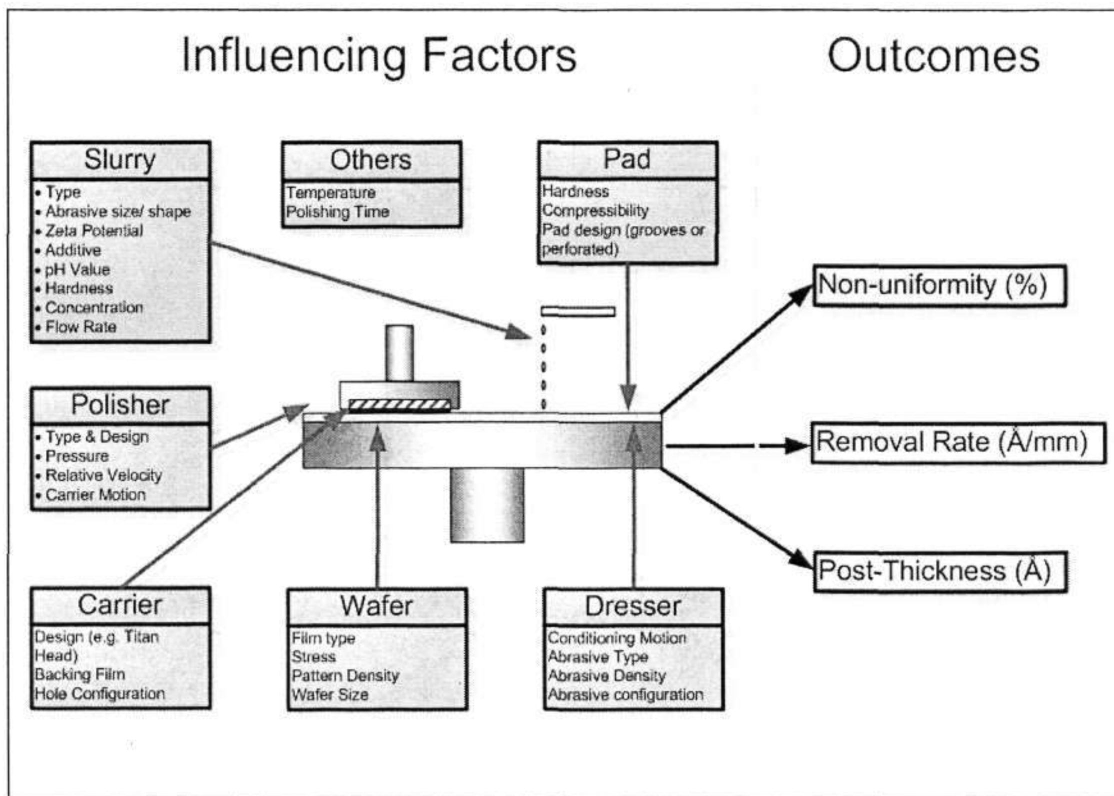

Fig. 2. 1 Complexity of CMP Process.

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2.1.1 CMP tool

There are number of different tools and consumables used in a complete CMP process. The basic tool used for CMP evolved from the machines that had been used to polish bare silicon substrate surfaces. When the idea for CMP was first conceived at IBM, they purchased silicon polishing tools from Strasbaugh and Westech (now SpeedFam-IPEC). The general configuration of the tool was mentioned in chapter 1.3.1. The first tool adapted for CMP had a single wafer carrier. The CMP machine differs from the Si polishing tool in a number of ways. In Si polishing several tens of microns of material are removed, while CMP process removes only about 0.05-1.0μm of material. The uniformity of material removal across a wafer in CMP is also much more stringent than for Si polishing, which is around ± 0.5-0.1nm for CMP. Furthermore, CMP tools require a higher level of automation, throughput, reliability, and critical process-parameter control. Thus, a specific CMP tool was developed for the IC industry. While early CMP tools used a single wafer carrier, more recent designs contain multiple carriers and multiple platens. This increases the throughput of the polisher and allows multi-step CMP processes to be carried out on a single tool. CMP tools that use a platen that moves past the rotating wafer carrier in a linear motion have also been developed and so are called linear CMP tools. These tools offer the potential benefits of higher linear speeds of 400-500 ft/min (122-152 m/min) while around 34 ft/min (10 m/min) in rotary CMP tools. Dual damascene process with copper replacing aluminum and low-κ materials as dielectric material becomes the interconnect integration solution in IC fabrication for 90nm node and beyond. A CMP tool developed by Nikon has become the first successful system to achieve on applied pressure of less than 0.1 psi compared to conventional tool with the condition of 3-7 psi to overcome the lower mechanical strength and adhesiveness in copper and low-κ structures on 300mm wafer while at the same time, achieving the required material removal rate [15].

2.1.2 Polyurethane Pad

Pads used in CMP process for IC manufacturing are made of cast and sliced polyurethane. The polyurethane type is resistant to acid and alkaline solutions [16]. While there is no overall consensus, it is generally agreed that the hardness and

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porosity of the pad are important parameters and play a crucial role in determining the performance of the process. However it is still poorly understood. In many CMP applications two pads are simultaneously used, while a hard pad gives better local planarity, a softer pad gives better uniformity of material removal across the entire wafer. Using a combination of two pads provides a compromise between these extremes. The surface of a pad is either cut with concentric grooves or contains perforations 1-mm wide and 250-μm deep punched into the pad. Grooved pads yield a higher removal rate than perforated pads and this can be attributed to the difference in contact area between two pads, 90.7% for the perforated pad compared to 83.3% for grooved pad [17].These grooves or perforations form channels to help transport the slurry between the pad and wafer. Pores present on the pad surface also aid in slurry transport. A comprehensive summary of the effect of polyurethane pad on CMP performance is summarised in table 2.1 [18]. Height and curvature distribution of asperities at the contact area of the typical commercial polyurethane pad will be characterized and presented in chapter 4.

Table 2. 1 Impact of pad properties on CMP performances [18]

	Scale			
Pad Property	**Wafer**	**Die**	**Feature**	**Conditionability**
Density (porosity)	RR,NU	D	CD,O	Yes
Hardness	MS	D	D,Rg,CD,O	Yes
Tensile Properties	L			Yes
Abrasion Resistance	L			Yes
Stiffness	EE,NU	P		
Top pad compressibility		P	CD	
Base pad compressibility	EE,NU	P		
Pad texture	L,RR,NU,EE			
Pad roughness	RR,NU	P	CD,O	Yes
Hydrophilic	RR			Yes

RR	Removal rate	P	Planarization
NU	Non-uniformity	D	Defectivity
EE	Edge Effects	CD	Conductor Dishing
MS	Macro-scratches	O	Oxide Loss
L	Pad Life	Rg	Roughness

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2.1.3 Slurry

The goal for each CMP process is to find a slurry that produces high removal rates, good planarity and high selectivity (for the process involved two or more type of thin film materials). On top of that, it should also be easily cleaned from the wafer surface and cause no defect to the wafer surface such as scratches. Therefore, slurry plays a crucial role in a successful CMP process. Particulates in slurry mechanically abrade the wafer surface and remove surface material. On the other hand, chemicals in the slurry solution react with surface materials or the particulates and dissolve the material or form other compounds that can be removed by abrasives particles. Slurries consist of small, abrasive particles of specific size which range from 10-1000nm and specific shape suspended in an aqueous solution. The abrasive particles have roughly the same hardness as the film being polished. Acids or bases are added to the solution, depending on the material to be removed. The slurry that impacts the removal rate includes the chemical composition slurry. Also important are the shape and size distribution of the slurry particles.

However, inconsistent and contradictory results conclusions are reported in the literature. Removal rates are proportional to applied pressure and relative velocity but independent of abrasive size [19] whereas another group of people reported that variations in removal rate occurred with an increase in abrasive size in the slurry [20]. The sizes of the abrasive in the slurry play a critical role in mechanical effects. With abrasives smaller than 0.3microns, changes in removal rate are indistinguishable [21]. The effect of abrasive size on removal rate was modeled by two different mechanisms [22]. For smaller abrasives, the dominant mode of material removal is the contact area mechanism. Whereas for larger abrasives, indentation plays the dominant role. On the other hand, small particles may not be adequate for sufficient mechanical removal rate, while large particles may cause excessive scratching. Abrasives hardness also affects the potential for scratching.

Slurries are marketed by a number of suppliers, such as Cabot Corp., Rodel Inc., Fujimi Inc., Olin Microelectronic Materials, Praxair Surface Technologies, and EKC Technology Inc. An automatic slurry feeding system is commonly used to ensure uniform wetting of the polyurethane pad and the proper delivery of the slurry. Slurries

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tend to dry rapidly on a wafer once it leaves the wet environment of the polishing table. Once the slurry dries, it is very difficult and hard to remove all its particles from the wafer surface. Hence, wafers are quickly placed into the cleaning unit and this is why polishing tools are always integrated with cleaning systems.

Slurries for oxide or STI CMP conventionally consist of colloidal silica or fumed silica suspended in an alkaline solution. The solids content of oxide CMP slurries is 10-15 wt% and the pH is between 10-11. By controlling pH within this range, agglomeration is minimized. Generally, the removal rate of oxide increases with increasing pH, with increasing slurry particles concentration and with increasing particle size. However, STI CMP performance with these kinds of slurries is not good in terms of selectivity, which induces defects such as erosion and dishing. The selectivity of oxide-to-nitride for SS-12 and Klebesol 1501-50 slurry ranges from 3 to 1 to 4 to 1 [23]. Novel particles, such as ceria, have entered mainstream CMP in the formulation of slurry. Instead of relying on sophisticated end-point detection systems, high selectivity slurry offers better solution for process performance. Ceria based slurry with ceria as an abrasive medium can achieve high selectivity and are an attractive option for STI CMP [24, 25]. However, the information that can be obtained from commercial slurries or gleaned from the patent literature is inadequate for developing an understanding of impact of this ceria based slurry on STI CMP performance. The lack of this understanding is a significant barrier to the development and optimization to ensure better process control. Therefore, characterization and investigation of ceria based slurry is needed and is the first step for further improvement in STI CMP performance. Characterization of direct STI CMP with ceria based slurry is reported in this thesis in chapter 3.

2.1.4 Carrier

The basic function of carrier is to hold the wafer in place while it is processed. Instead of directly holding the wafer on the chuck, a backing film is sandwiched between the wafer and steel chuck. This film provides elasticity between the two. Without a flexible backing film any defect or particles on the chuck or on the back of the wafer will cause a small spot in the film being polished. In addition, the possibility of wafer breakage is increased. In conventional wafer carriers the retaining ring does not make

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contact with the pad. As a result, there is no pressure applied to the pad by this ring. Thus, the pad pressure at the edge of the wafer is not well controlled and the polishing rate of the film is decreased at the wafer edge. Hence an edge exclusion ring of 5-7mm must be enforced for wafers with such carriers. Carriers used in some CMP tools such as Applied Materials' Mirra® (known as Titan Head) are designed with a retaining ring that can apply variable pressure to the pad as shown in figure 2.2 [26]. An independently-controlled pressure is applied onto the retaining ring to absorb pad deformation around the wafer edge during the process. This allows the pad profile at the wafers edge to be controlled. A smaller edge-exclusion of around 2-3mm zone on the wafer can therefore be used. Retaining ring design on carrier is critical to ensure edge exclusion on the wafer and uniformity of removal rate near to the edge of the wafer as well.

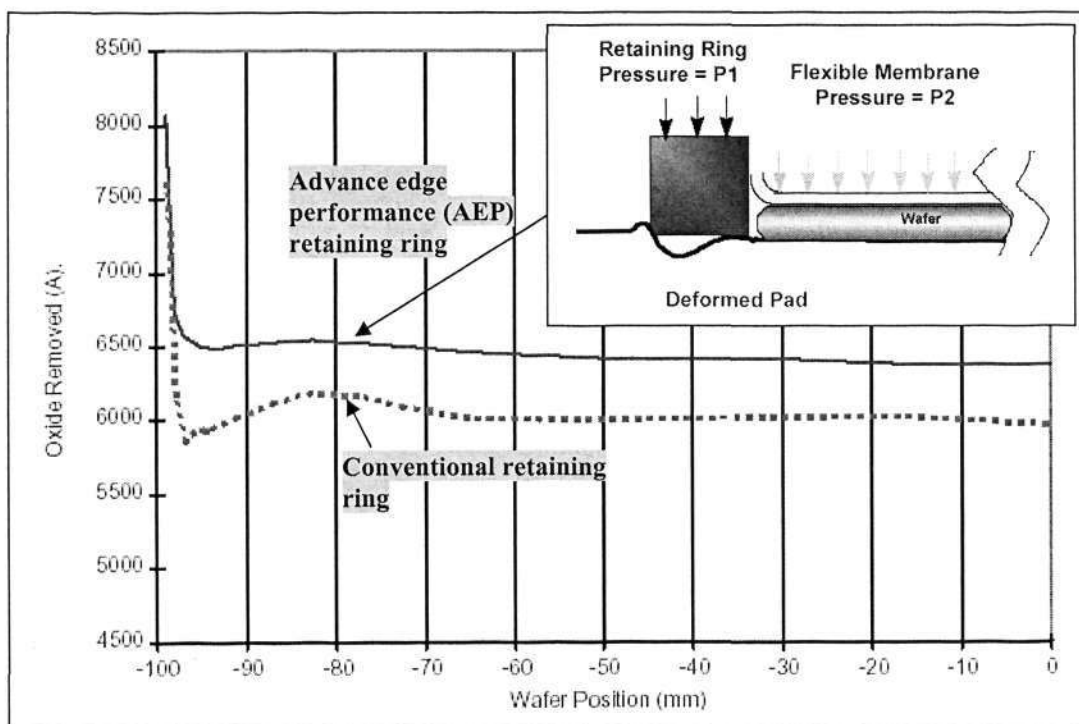

Fig. 2. 2 Schematic diagram and performance of advance retaining ring of the carrier [26].

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2.1.5 Dresser

One of the earliest patents about pad conditioning tool is utilized to trace micro grooves on the pad surfaces [6]. Unless a pad is continuously conditioned, removal rates decrease rapidly with pad usage. This occurs due to the surface of the pad rapidly glazing during the planarization process. The pores of the pad become closed, reducing slurry delivery to the wafer surface and causing an unstable and lower removal rate [27, 28]. A consistent removal rate is necessary for a production-worthy CMP process. This can be achieved by pad conditioning, which opens the pores of the pad by forming microscratches on the pad surface. Typically, a diamond disk sweeps the polyurethane pad surface to obtain a stable process and maintain a consistent acceptable removal rate. While several alternate conditioning methods have shown promise in research environments, diamond disk pad conditioning is the dominant technique used in most production fabs. [29].

2.1.6 Wafer

Thickness variation and shape of bare silicon wafer (substrate) are closely correlated to non-uniformity within wafer and material removal rate [30]. Material removal rate non-uniformity increases linearly with pre-process wafer total thickness variation (TTV) as shown in figure 2.3.

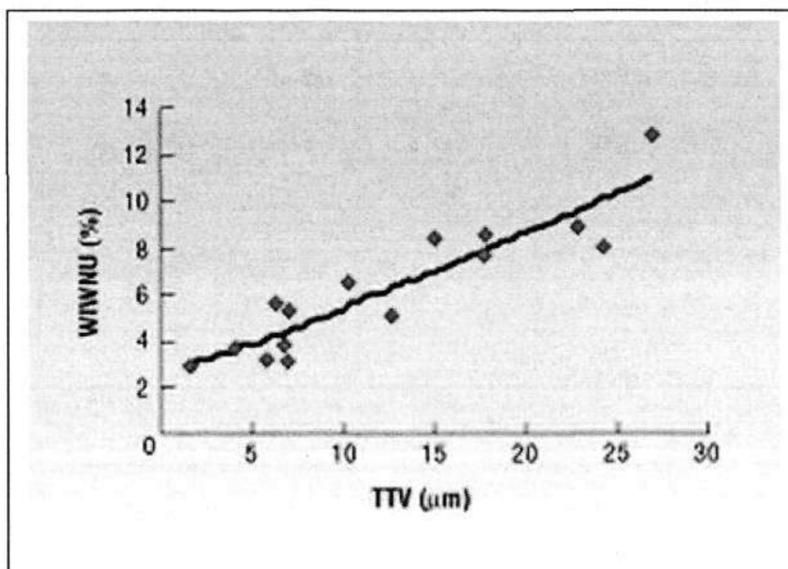

Fig. 2. 3 Effect of TTV of wafer on non-uniformity [30].

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As indicated in 200mm polished Czochralski (CZ) wafer specification, TTV of bare silicon wafer should be equal or less than 15μm according to the American Society For Testing and Materials (ASTM) standard [31, 32]. Adding a dielectric film to the wafer substrate will affect the TTV value and the wafer shape is not static due to thermal expansion coefficients between a thin film and the underlying film or wafer substrate. The stress induced by film deposition can deform a wafer into a concave or a convex shape.

Removal rate and uniformity are strongly dependent on the type of film deposited. For instance, a study was undertaken to compare the results of the CMP non-uniformity for polishing two different types of oxide films, namely, borophosphosilicate glass (BPSG) and tetra-ethly-ortho-silicate (TEOS). Results suggest that better uniformity is achieved by using TEOS film. It was also observed that thermal oxide deposition yielded a decrease in polish rate as compared to oxide deposited by CVD. Stress is introduced to the wafer when a thin film is deposited. The strength and type of this stress depend on the deposited materials as well as thickness and method of deposition. The induced stress therefore affects the distribution of the polishing pressure during CMP. In short, the mechanical properties of the film results from it deposition method or its doping level, which could affect the material removal rate. In addition to the characteristics of the film, the characteristics and quality of the substrate must be considered. A poor silicon substrate with high thickness variation, bow and warp, even with a very uniform film surface may still result in high non-uniformity during CMP removal.

2.1.7 End point detection (EPD) system

Knowing when to stop the process is critical in determining the final thickness of the thin film in the case such as ILD CMP or ensuring excess material is completely removed to reveal underlying materials across the wafer in the case of inlaid CMP process. Thus, other than estimation made by operator using a look-up table, numerous approaches such as optical, electrical and acoustic sensing means to obtain optimal process time have been proposed and patented as *in situ* EPD systems for CMP tools with limited success [33]. This is due to the nature of CMP process environment and presence of various patterns on the wafer surface adds a great deal of

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complexity to the signals and material removal rate in CMP process is more inclined to be erratic as the result of complex interaction between input parameters; it is very difficult to integrate a robust and reliable real time measurement of film thickness in a CMP tool. Typically, ex-situ measurement of thin film thickness is required to characterize the process in IC fabrication. Consistency to achieve the specific target mean film thickness within a tight tolerance (± 80nm) requirement in the process flow for IC fabrication is a great challenge to ensure yield and quality. In chapter 4, a methodology to predict optimal time for the process will be presented.

2.1.8 Other influencing factors

Unlike dielectric material, metal thin films such as copper are temperature sensitive. The wafer surface can be subjected to high temperature as a result of friction with the polyurethane pad. It is observed that the material removal rate of copper decreases with an increase of slurry flow rate while other process conditions remain constant as shown in figure 2.4 [34]. The reduction in copper removal is believed to be due to the cooling effect at higher slurry flow rate.

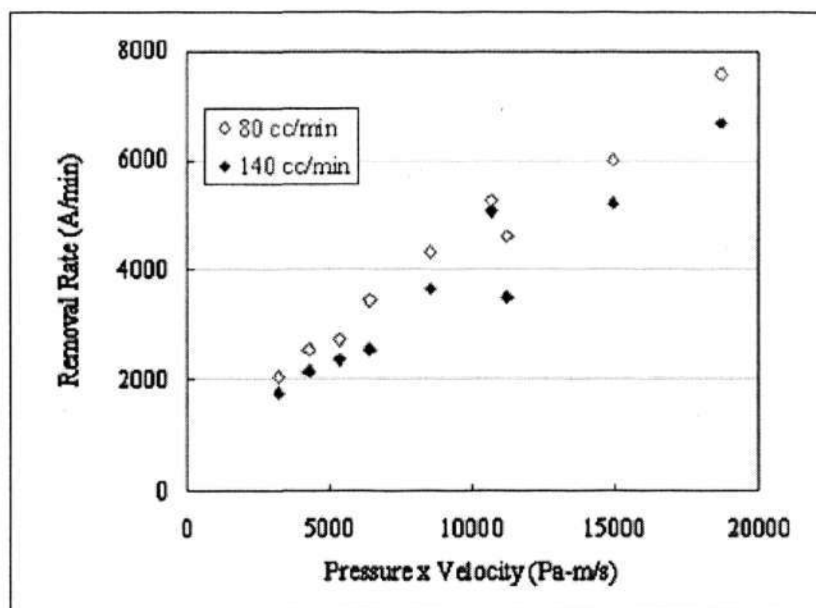

Fig. 2. 4 Copper removal rate as a function of product of pressure and velocity at two flow rates [34]

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2.2 Material Removal Rate in CMP

One of the most important and basic performances measured in CMP process is the material removal rate which is usually expressed in terms of Å/min in IC fabrication. Blanket wafers are used to characterize the material removal rate and non-uniformity across the wafer for a specific configuration of the inputs as shown in figure 2.1(wafer scale). It serves as a fundamental understanding for patterned wafer (die scale, feature scale, particle scale). Variation of the material removal rate across the wafer scale results in material thickness variation known as *non-uniformity-within-wafer* (NUWIW). Whereas variation of material removal rate across the die scale causing the post thickness variation is termed as *non-uniformity-within-die* (NUWID). Planarization performance usually measured by feature scale (step height reduction) as indicated in figure 1.4 whereas particle scale is used to measured surface roughness. Blanket material removal rate model provides an important starting point for elucidating the other aspects of CMP process. Reliable models will facilitate development of process recipes.

2.2.1 Material Removal Rate model

Preston presented the first phenomenological model at 1927 based on results of glass polishing and it still retains a significant influence on CMP experimental and modeling work [35]. To date, the model still remains the standard reference for most detailed models that are used to describe the wafer scale, die scale, feature scale and surface finish in the CMP process of IC fabrication. According to Preston, the material removal rate at any position across the glass surface can be described as:

$$\frac{\Delta H}{\Delta t} = K_p \left(\frac{L}{A}\right)\left(\frac{\Delta s}{\Delta t}\right) \tag{2-1}$$

where $\frac{\Delta H}{\Delta t}$ is the change in thickness or height (H) over time (t), L is the applied load or total load and A is the surface area on which wear occurs, $\frac{\Delta s}{\Delta t}$ is the relative velocity between glass surface and lap, K_p is the Preston coefficient, which is process

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dependent with units of cm^2/dyn [36]. Commonly it is rewritten or simplified as $RR=K_pPV$ with P is the applied pressure which using apparent wafer surface area and V is the average relative velocity for CMP material removal rate. Despite the fact that the model is glass polishing and not physically based, it provides the foundation for the dielectric planarization in semiconductor industry and this empirical model serves as a convenient storehouse for experimental data. In literature, some works have also showed that Preston's equation is also valid for certain metal thin films such as copper. [37-39].

Around 1983, the original CMP development work was undertaken by IBM in East Fishkill, New York [2]. In 1989, IBM also published the first paper which publicly discussed the CMP of oxide films [3]. Since then a number of publications and articles have made use of the fundamental aspects of glass polishing to describe the mechanism of CMP process in IC fabrication. Besides Preston, another well known reference for CMP process is by Cook [36] in 1990, which provides chemical explanation of the process. Cook described the polishing mechanics by a Hertzian indenter model as abrasive penetration into the wafer surface under uniform applied load which can be given by:

$$\frac{\Delta H}{\Delta t}=(2E)^{-1}P\left(\frac{\Delta s}{\Delta t}\right) \tag{2-2}$$

This is equivalent to the Preston equation (2-1), but with the Preston constant expressed as the inverse of twice Young's modulus, E. He also introduced the term of "chemical tooth" which implying that hydroxyl groups played a key role in the surface removal process. Cook explained that surface removal during glass polishing is determined by the relative rates of five processes: i) the rate of molecular water diffusion into the glass surface; ii) subsequent glass dissolution under the load imposed by the polishing particle; iii) the adsorption rate of dissolution products onto the surface of the polishing grain; iv) the rate of silica redeposition back onto the glass surface and v) the aqueous corrosion rate between particle impacts. He concluded that the major factors influencing these processes are the load and velocity of the polishing particles, the elastic properties of both glass surface and particles, the chemical

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durability of the glass, the surface charge of the glass, and the surface charge and ion-exchange capacity of the particle [34].

In 1994, Runnels et al. presented a tribology analysis to demonstrate that hydroplaning is possible in CMP process and concluded that fluid layer between pad and wafer are profound [40]. An analogy to Preston's equation is proposed:

$$R = \hat{k}\,\sigma\tau \qquad \textbf{2-3}$$

where $\hat{k}$ is a constant (similar to K_p), σ and τ are the magnitudes of the normal and shear stresses respectively on the wafer surface. Their study is based on fluid mechanics to the stresses in a solid-liquid-solid system. Assumptions they made in simplification of flow modeling is that the wafer and pad are rigid and smooth. No experimental data is used to verify the model in their study.

In 1996, Liu et al. used statistical methods and elastic theory to describe the wear mechanism on a silicon wafer surface [41]. They derived the following removal rate equation:

$$R.R = C'\left(\frac{HV_w}{HV_w + HV_p}\right)\left(\frac{E_s + E_w}{E_s E_w}\right)PV \qquad \textbf{2-4}$$

where C' contains the chemical effect which is perceived as being independent from mechanical factors and is constant assuming fixed slurry chemistry, Vickers' hardness numbers HV_w and HV_p for wafer and pad respectively, E_w and E_s are the Young's modulus of wafer and abrasive in the slurry. They considered the process of rolling as an analogy (three body interaction) to the CMP removal mechanism in which wafer are being pressed down against the pad, the slurry particle are moving in the gap between the wafer and the pad in a shearing action.

In 1997, Tseng et al. re-examined the pressure and speed dependence for CMP process by modifying the Preston equation which is expressed as follow : [42]

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$$R.R = MP^{\frac{5}{6}}V^{\frac{1}{2}} \qquad \textbf{2-5}$$

They attempted to incorporate elastic contact between particle and wafer as proposed by Cook [36] into solid-liquid-solid system (hydroplaning mode) as suggested by Runnels [40] to take into consideration the material breaking mechanism from principles of solid mechanics. M represents the contribution of chemical erosion and is a function of pressure and velocity. In the same year, Wang et al. [43] described a model for the stress distribution across a wafer during CMP by considering carrier film and pad compressibility on removal rate non-uniformity. They concluded that the non-uniformity across the wafer surface is not due to the normal contact stress and uniformity can be improved by decreasing the polyurethane pad and carrier film compressibility.

Maury et al. introduced a fitting constant R_0 as shown in equation 2-6 into Preston's equation to account for non-zero material removal rate intercept at the practical regime (where the reasonable material removal rate is fall) so called large PV or the product of pressure and velocity [44].

$$\frac{dz}{dt} = k_p PV + R_o \qquad \textbf{2-6}$$

Whereas at a small PV value, the Preston's equation is applied. This model demonstrated better fit to experimental data in oxide CMP as compared to the model proposed by Tseng et al. (equation 2-5) [45].

In 1998, Shi et al.[46, 47] argued that that the fundamental mechanism of the pressure dependence for CMP with a soft pad is completely different from that with a hard pad in glass polishing. The applied pressure causes a change in the indentation depth of abrasive into the wafer in hard pad whereas abrasive embedded into the asperities in the case of soft pad. They proposed a nonlinear pressure dependence model that having a physical limit of zero material removal rate as applied pressure is equal to zero as described by equation 2-7:

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$$RR = K_{sz}P^{\frac{2}{3}}V \quad \textbf{2-7}$$

Similar to K_p in Preston's equation, K_{sz} is the coefficient which is a function of other CMP variables. This model considered a solid-solid system with identical asperities across the area of contact based on Hertz elastic contact theory.

Zhang et al. believed plastic deformation most likely happened between the abrasive and wafer surface in CMP process and the corresponding material removal rate is described as [48] :

$$RR = C_c\sqrt{PV} \quad \textbf{2-8}$$

where C_c is a constant which represents the effects of chemical reaction. In this model, the effect of the adhesion forces is incorporated into Runnels et al. (2-3) model. Experimental data is based on copper wafers.

In 1999, Wrschka et al. proposed a power function material removal rate model as follows [49] :

$$R.R = KP^aV^b \quad \textbf{2-9}$$

with a and b are two fitting parameters and proportionality constant K. They demonstrated inadequacies of Preston's equation in describing the aluminum removal rate in the CMP process.

A material removal rate based on the abrasion model as a function of abrasive weight concentration was proposed by Luo et al. in 2001 as follows [50] :

$$MRR_{thickness} = C_3\left(1-\phi\left(3-C_2P^{\frac{1}{3}}\right)\right)\sqrt{PV} \quad \textbf{2-10}$$

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where C_3 and C_2 are the two values which attempt to reflect the effects and interactions of slurry abrasives, slurry chemicals, pad hardness, pad topography, abrasive size and other consumable parameters, and ϕ a probability function of the abrasive size distribution. These two values are independent of down pressure P and the relative velocity V as suggested by the authors. The model relies on an estimation of the number of active abrasives and force acting on the abrasive particles during the process. This model is based on solid-solid contact mode with assumptions of plastic contact over wafer-abrasive and pad abrasive interfaces, the normal distribution of abrasive size and periodic roughness of the pad surface.

Hocheng et.al, found that the material removal rate is less linearly correlated to the pressure and relative velocity [51]. Based on the bear-and-shear process model, a similar relationship as proposed by Zhang at el. (equation 2-8) is derived where the material removal rate increases with the increasing pressure and velocity to the power of half.

Table 2.2 summaries the publications tracking the development of material removal rate models. In general, it is very difficult to draw any definitive conclusions due to the different CMP tools, applied pressure, relative velocity, film type, consumables and other experimental conditions conducted by various group of people. In practice, the material removal rate model is modeled as a function of controllable parameters such as pressure and relative velocity and used as a guide to reach the optimal process conditions such as magnitude of applied pressure and rotational speed for both platen and carrier to achieve certain removal rate requirement in a particular process based on performances on blanket wafers.

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Table 2. 2 Material removal rate models for CMP applications.

Year	Model	linear	Non-linear	Constant Coefficient	Contact Mode*	Deformation Mode*	Materials: Glass	Thin film-oxide	Thin film-oxide and nitride	Thin film-Aluminium and oxide	Thin-film Copper	Unit	Process Conditions
1927	$RR = K_p PV$	v		v	-	-	v					μm	~ 5cm/s; ~1psi (0.07kg/cm^2)
1983	*For the first time CMP used in IC fabrication*							v				Å	-
1989	*First paper published on CMP in IC fabrication*								v			Å	-
1990	$RR = (2E)^{-1} PV$	v		v	SS	E	v					μm	~ 5cm/s; ~1psi (0.07kg/cm^2)
1994	$RR = k \sigma \tau$		v	v	SIS	E						Å	-
1996	$RR = C'(HV_w/(HV_w + HV_p)(E_s + E_w/E_s E_w)PV$	v		v	SS	E		v				Å	-
1997	$RR = MP^{5/6} V^{1/2}$		v	v	SIS			v				Å	10-70rpm; 4-11psi
	$RR = K_p PV + R_c$	v		v	-	-		v				Å	
1998	$RR = K_{sz} P^{2/3} V$		v	v	SS			v				Å	4-20psi
	$RR = kP^{1/2} V^{1/2}$			v	SS	P					v	Å	1-9psi
1999	$RR = KP^{\alpha} V^{\beta}$			v	-	-				v		Å	43-80 cm/s; 3-6psi
2001	$RR = C_3 (1-\phi(3-C_2 P^{(1/3)}))P^{1/2} V$		v		SS	P					v	Å	

**SS= solid-solid, SIS= Solid-liquid-solid contact, E=Elastic, P=Plastic*

2.3 Kinematics of CMP Process

The importance of the relative motion between pad and wafer has been highlighted in almost every model in the CMP literature as shown in the previous section. Unlike the pressure term, the computation of relative velocity between each point on the wafer and underlying pad is accomplished through a straightforward application of kinematics. The determination of the local and average relative velocities allows the evaluation of the local removal rate and basic understanding for detailed modeling. Thus, kinematics plays an important role in CMP process. Unlike the other two parameters (pressure and coefficient) in Preston's equation, relative velocity is the one that is known with certainty.

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2.3.1 Kinematics derivation

Both linear and rotary polishers are commonly employed in the CMP process. To analyze the kinematics, the coordinate systems for both types of polishers need to be determined and these are shown in figure 2.5.

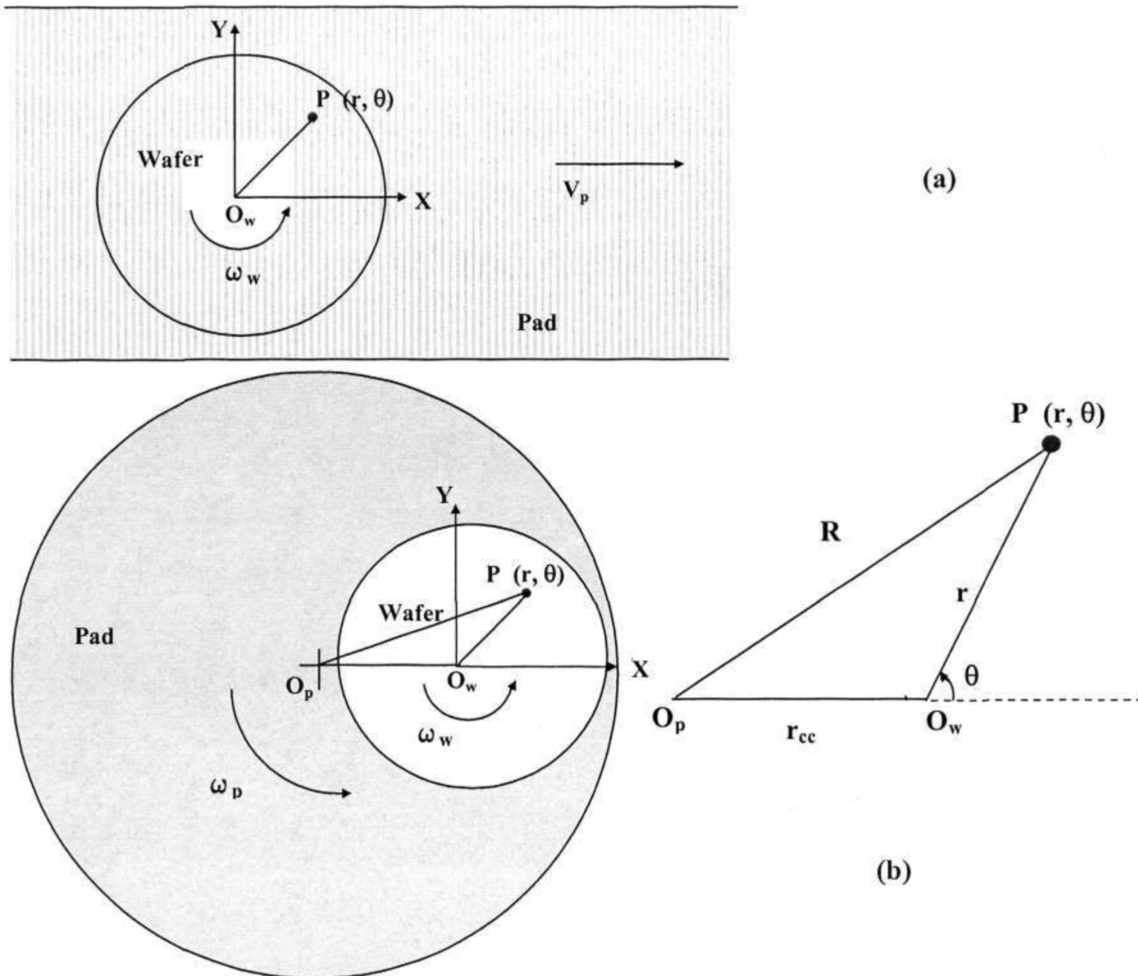

Fig. 2. 5 Layout of coordinate systems and motion for:
(a) linear CMP tool (b) rotary CMP tool with fixed carrier rotation.

In the linear CMP tool, the pad slide along the x-direction with a constant velocity v_p while wafer rotates at an angular velocity, ω_w, about its center O_w. Thus, the velocity components for the wafer, $V_{r,w}$ and $V_{\theta,w}$ and the pad, $V_{r,p}$ and $V_{\theta,p}$, in r, θ coordinates can be expressed as follow:

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Wafer: $$V_{r,w} = 0; \quad V_{\theta,w} = \omega_w r \tag{2-11}$$

Pad: $$V_{r,p} = V_p \cos\theta; \quad V_{\theta,p} = -V_p \sin\theta \tag{2-12}$$

Therefore, the components of the relative velocity of the wafer to the pad are given as:

$$V_{r,R} = V_{r,w} - V_{r,p} = -V_p \cos\theta \tag{2-13}$$

$$V_{\theta,R} = V_{\theta,w} - V_{\theta,p} = \omega_w r + V_p \sin\theta \tag{2-14}$$

and the magnitude of the relative velocity of the wafer to the pad can be written as:

$$V_R(r,\theta) = [V_{r,R}^2 + V_{\theta,R}^2]^{\frac{1}{2}} = [(-V_p \cos\theta)^2 + (\omega_w r + V_p \sin\theta)^2]^{\frac{1}{2}}$$

$$= [V_p^2 + 2\omega_w r V_p \sin\theta + \omega_w^2 r^2]^{\frac{1}{2}} \tag{2-15}$$

Hence, in steady state, the average of the relative velocity components of points located at a radius r can be expressed as:

$$V_{r,average} = \frac{1}{2\pi}\int_0^{2\pi} V_{r,R} d\theta = 0 \tag{2-16}$$

$$V_{\theta,average} = \frac{1}{2\pi}\int_0^{2\pi} V_{\theta,R} d\theta = \omega_w r \tag{2-17}$$

Equation (2-17) shows that the average of angular velocity increase with an increase in radius. From another point of view, sliding distances for any point on a wafer will increase with radius, which results in non-uniform removal rate across the wafer. In order to reduce non-uniform polishing, velocity of platen, V_p, should be much greater than velocity of carrier:

$$V_p >> r_w \omega_w \tag{2-18}$$

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If the above condition is satisfied then polishing is nearly isotropic as described by equation (2-16) since it is the dominant component as compared to that described by equation (2-17). This also explained why in a linear polisher a high platen velocity is applied as compared to rotary polisher.

As for the rotary CMP tool with carrier without sweeping as shown in figure 2.5 (b), the centers of rotation of the wafer and platen are O_w and O_p with the angular velocity of ω_w and ω_p respectively. A fixed distance between center of wafer and platen is indicated as r_{cc}. The velocity components of the wafer at a point "P" are the same as in equation 2-11. Whereas the velocity components for the pad in the rotary polisher can be expressed as:

Pad: $$V_{r,p} = \omega_p r_{cc} sin\theta\ ;\ V_{\theta,p} = \omega_p (r + r_{cc} cos\ \theta) \qquad \textbf{2-19}$$

Hence, the components of relative velocity can be written as follow:

$$V_{r,R} = V_{r,w} - V_{r,p} = -\omega_p r_{cc} sin\theta \qquad \textbf{2-20}$$

$$V_{\theta,R} = V_{\theta,w} - V_{\theta,p} = \omega_w r - \omega_p (r + r_{cc} cos\ \theta) \qquad \textbf{2-21}$$

So, the magnitude of the relative velocity is:

$$\begin{aligned} V_R(r,\theta) &= [V_{r,R}^2 + V_{\theta,R}^2]^{\frac{1}{2}} \\ &= [(-\omega_p r_{cc} \sin\theta)^2 + (\omega_w r - \omega_p (r_{cc} \cos\theta))^2]^{\frac{1}{2}} \\ &= \{[(\omega_w - \omega_p) r \sin\theta]^2 + [(\omega_w - \omega_p) r \cos\theta - \omega_p r_{cc}]^2\}^{\frac{1}{2}} \end{aligned} \qquad \textbf{2-22}$$

Similarly, the average of the relative velocity components of points located at particular radius r are described by equation 2-16 and 2-17. When the angular velocity of wafer, ω_w, and platen, ω_p, are equal then equation 2-22 can be simplified as:

$$V_R (r, \theta) = \omega_p r_{cc} \qquad \textbf{2-23}$$

Thus, equation 2-23 suggests that the relative velocity of any point on the wafer will remain identical and constant throughout the polishing process. This results in

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isotropic polishing. Whereas the direction of any points of the wafer will vary at a frequency $\omega_w/2\pi$.

2.3.2 Simulation of the effects of relative velocity components

Typically, angular rotational speed used in IC fabrication is between 50rpm to 120rpm for rotary CMP tool. Thus, in this section 80 rpm and 100 rpm are used to illustrate the impact of different configurations in rotation speed in rotary CMP tool for both local and average value. The results are shown in figure 2.6 to figure 2.11. Each line on the left hand side of each figure shows the local relative velocity magnitude of a particular point on the wafer surface in completing one revolution (0-360^0). All together 21 points are simulated from the center of the wafer (r = 0mm) to the edge of the wafer (r = 100mm). Whereas the line on the right hand side of each figure show the average relative velocity magnitude across the wafer from center to edge.

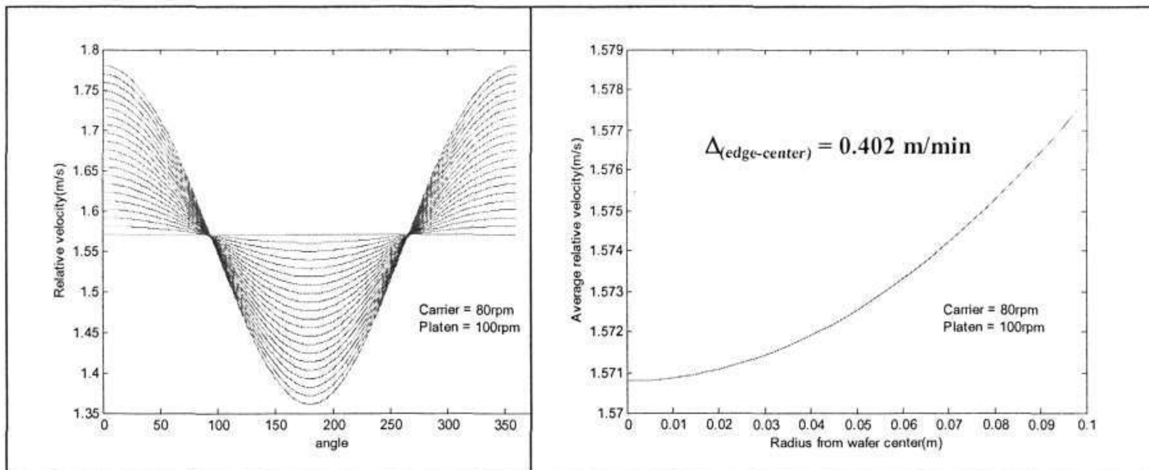

Fig. 2. 6 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and both rotate in the same direction

Figure 2.6 illustrates the velocity profile when the platen rotational speed is higher than the carrier and rotate in the same direction without oscillation motion of the carrier across the platen. In contrast, figure 2.7 demonstrates a case where the carrier has a higher angular rotation speed as compared to platen. A similar profile is obtained but the magnitude of relative velocity is reduced and the difference between center and edge of the wafer is increased for the latter case.

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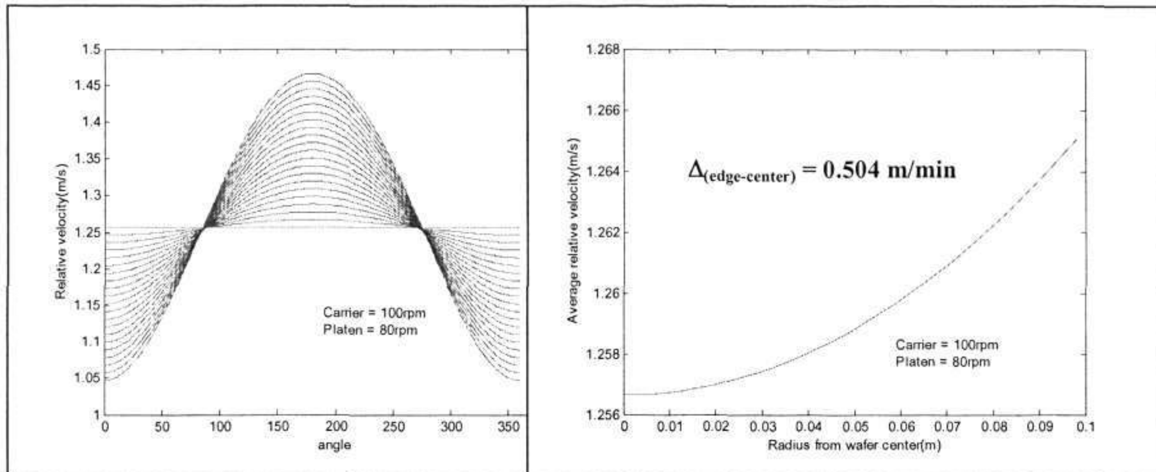

Fig. 2. 7 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and both rotate in the same direction

The effect of rotating in the opposite direction is shown in figure 2.8 and figure 2.9. Despite it might have a higher material removal rate as the relative velocity magnitude increases with the same set of angular rotation speed, the difference between center and edge of wafer increases by two orders of magnitude.

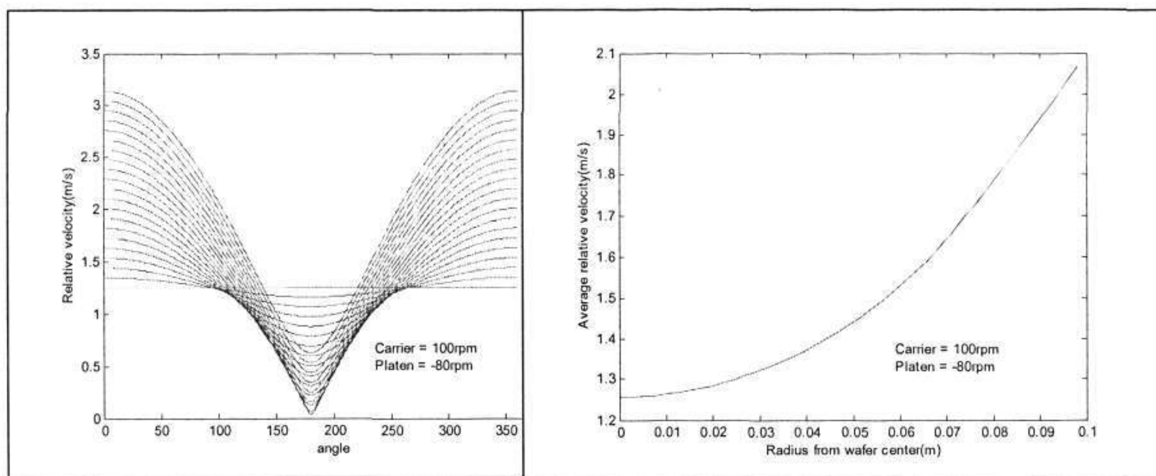

Fig. 2. 8 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and rotate in the opposite direction

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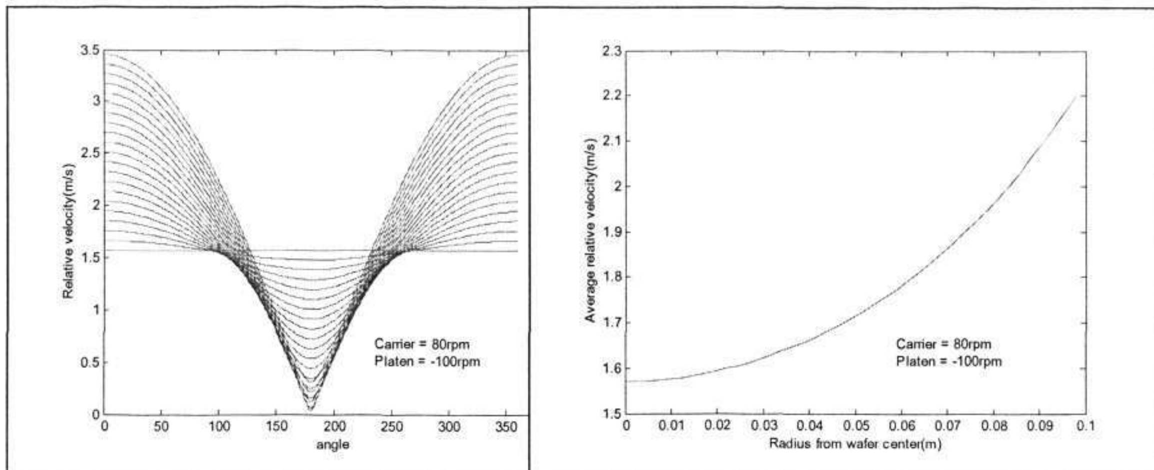

Fig. 2. 9 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and rotate in the opposite direction

Figure 2.10 and figure 2.11 show that as the carrier exhibits oscillations across the platen, similar relative velocity profile is obtained (left hand side of the figure) and instead of a horizontal line or same magnitude for the point at center of the wafer, it varies with time. There are slight increases in the differences between center and edge of the wafer. However, oscillations of the carrier can optimize the usage of the polyurethane pad surface.

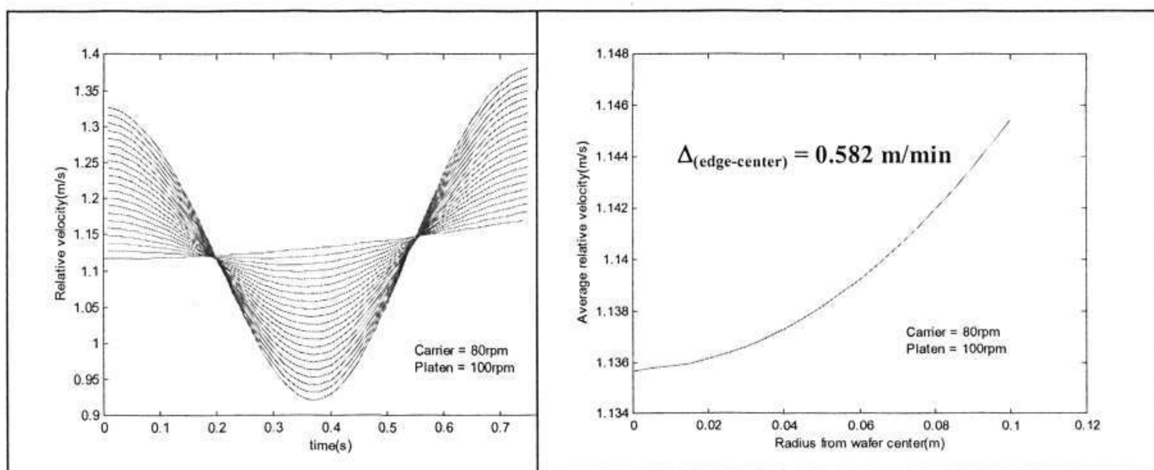

Fig. 2. 10 Velocity profile and average velocity difference across the wafer surface with angular speed of platen higher than carrier and rotate in the same direction with carrier oscillates across the polyurethane pad.

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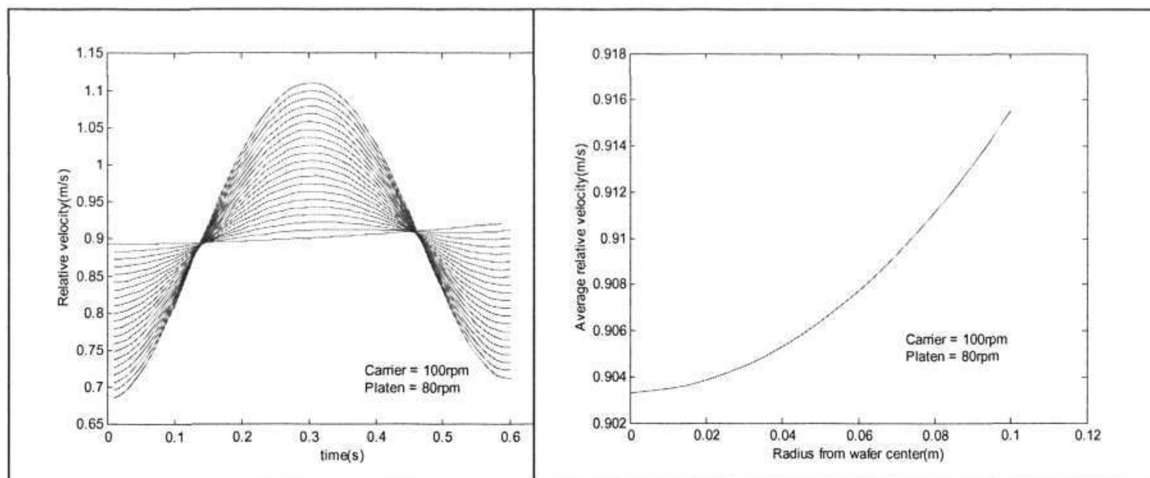

Fig. 2. 11 Velocity profile and average velocity difference across the wafer surface with angular speed of platen lower than carrier and rotate in the same direction with carrier oscillates across the polyurethane pad.

2.4 Material Removal Rate of Polysilicon CMP process.

Since 1983 when CMP was introduced into the IC fabrication, considerable focus has been on the material removal rate of oxide, tungsten, aluminum and copper film as illustrated in section 2.2. Relatively little information about polysilicon CMP exists in the literature. This is mainly due to CMOS still remaining the backbone for the digital logic. However, silicon technology will evolve in directions driven by system needs that are not met by CMOS alone. Designers often use bipolar transistors for many analog and rf circuits in which high performance and/or low power dissipation are required [52, 53]. It is believed that bipolar complementary metal-oxide-semiconductor (BiCMOS) will emerge as an important technology platform for mixed signal systems [54]. Polysilicon material is used to fill the deep trenches before the STI is filled by oxide to reduce collector-to-substrate capacitance in the BiCMOS process flow[55]. CMP is employed to remove the overburden polysilicon materials to define the deep trenches as shown in figure 2.12.

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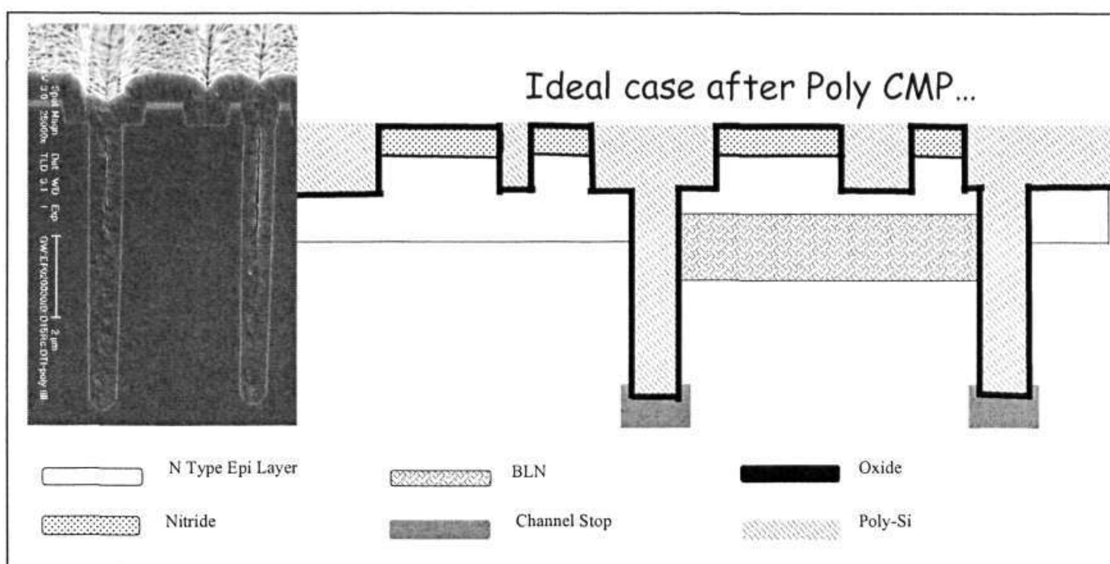

Fig. 2. 12 Deep trench in BiCMOS process.

Reliable patterned wafers modeling for CMP process entails a good understanding of material removal rates in blanket wafers. Although the material removal rate models as reviewed in section 2.2 are becoming increasing predictive, validation is still critical especially when applied to a new process before results obtained from simulations will be considered. In this section, investigation is carried out to verify the removal rate models in the literature for polysilicon materials. As a bare minimal, a model must be able to predict the trends correctly to be useful.

2.4.1 Experimental Descriptions

The experiments were conducted on an EBARA CMP EPO-213 with perforated polyurethane pad and commercial colloidal silica based slurry with different process conditions (variations in pressure and angular speed for both platen and carrier). In the experiment, 200mm blanket wafers with 12000Å thermally grown polysilicon with 1500Å of TEOS film underneath on silicon wafer were used. Three different hole configurations on the carrier were used i.e. 0-4-4-8-0-0-0, 0-4-4-8-4-8-8 and 0-4-4-8-4-8-8 with edge tape as illustrated in figure 2.12 to investigate the impact on the non-uniformity removal rate across the wafer surface. Each wafer was polished for 90 seconds. Opti-probe Therma Wave was used for 49 points (polar map) and 121 points (diameter scan) pre and post thickness measurement.

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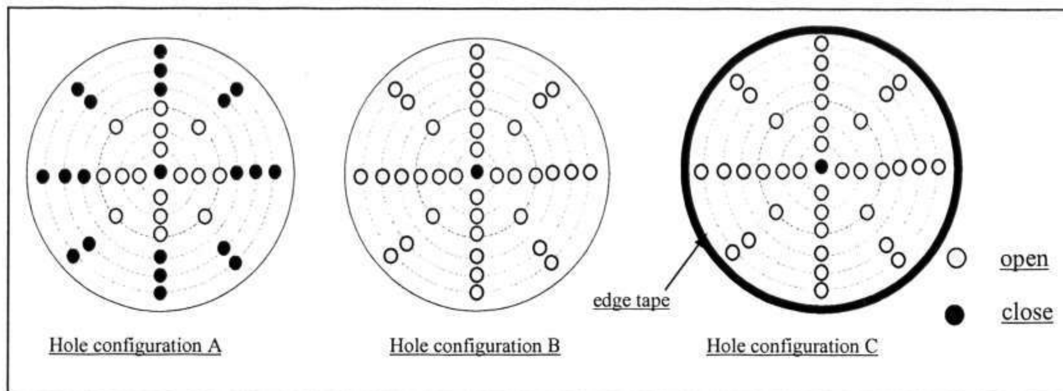

Fig. 2. 13 Hole configurations for carrier.

2.4.2 Experimental Observations

The experimental data were grouped into three different sets according to the hole configurations (figure 2.13) used in the experiment so that the material removal rate is only affected by pressure and angular speed of both platen and carrier. Relatively more wafers (20 wafers) were processed using hole configuration C as compared to hole configuration A (8 wafers). This is due to lower non-uniformity of material removal rate across wafer demonstrated by hole configuration C as shown in figure 2-14 (typical removal rate profiles for three different hole configurations).

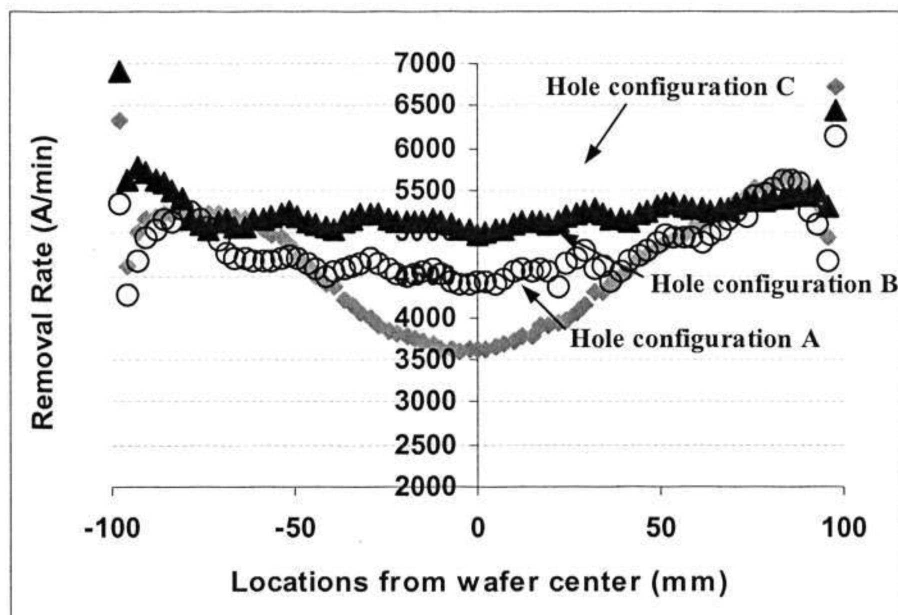

Fig. 2. 14 Effects of hole configurations on non-uniformity of material removal rate across wafer

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In the following three figures (2.15-2.17) various linear regression models in the literature (refer to section 2-2) are evaluated by examining whether the respective model can capture the observed experimental data of polysilicon removal rate in the practical removal rate regime. Coefficient of determination, R^2, is used to interpret the proportion of material removal rate dependent which can be explained by the proposed linear regression models. On the top left corner of each figure, Preston-like model (represented by the dotted line) and Preston model with a constant term (represented by the solid line) are plotted. Different from the material removal rate data as demonstrated in the oxide CMP [45], results obtained from the experiments reveal that the material removal rate model as described by Preston (2-1) does not reflect the observed polysilicon removal rate reasonably well for all three different hole configuration setting in the experiments. Modification of Preston's equation by adding a constant term as suggested by Maury [44] to account for the large PV region does improve the fit relatively but still is not as good as the respective model demonstrated in oxide CMP where more than 95 percent of the variation in material removal rate can be explained. Consistent results are obtained for each material removal rate model across three different hole configurations in the experiment with Tseng et al. [42] model fit relatively well with R^2 value above 0.9, followed by the Zhang et al. [48] model with R^2 value above 0.7 and both models introduced by Shi et al. and Luo et al. [50] failed to represent the observed data. A better linear regression fit to polysilicon materials removal rate disregards three different hole configurations settings in the experiments are observed by the square term of the pressure and velocity product (P^2V) with a constant term [56] as shown at the right bottom of each figure with a typical value of above 95 percent of variation of material removal rate can be described. This study shows that despite some of the models obtaining a better agreement with experimental observations in oxide CMP (such as the physical model as proposed by Shi.et al.) they failed to capture the behavior in polysilicon materials. This is attributed to high interactions due to a large amount of variables in CMP process and the problem addressed piecemeal in physical modeling. The major challenge is to develop models that can quickly, inexpensively and accurately simulate actual semiconductor process and device phenomena [12].As the application of CMP process gains wider appeal across different materials in IC fabrication, a more general and versatile model able to capture the behavior of the process is needed to serve as vehicles for simulating the process.

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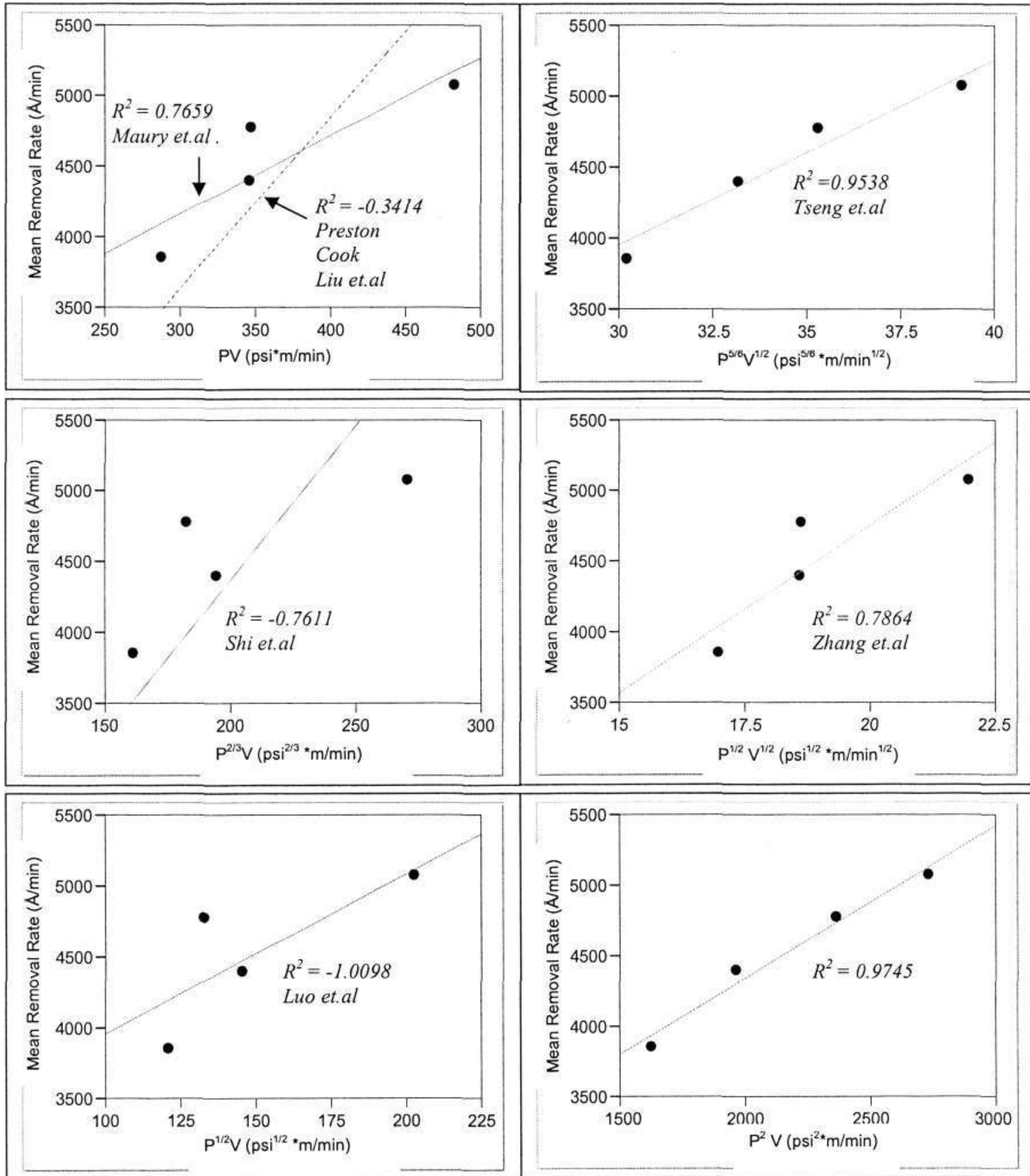

Fig. 2. 15 Material removal rate data of polysilicon with hole configuration A fit across various models

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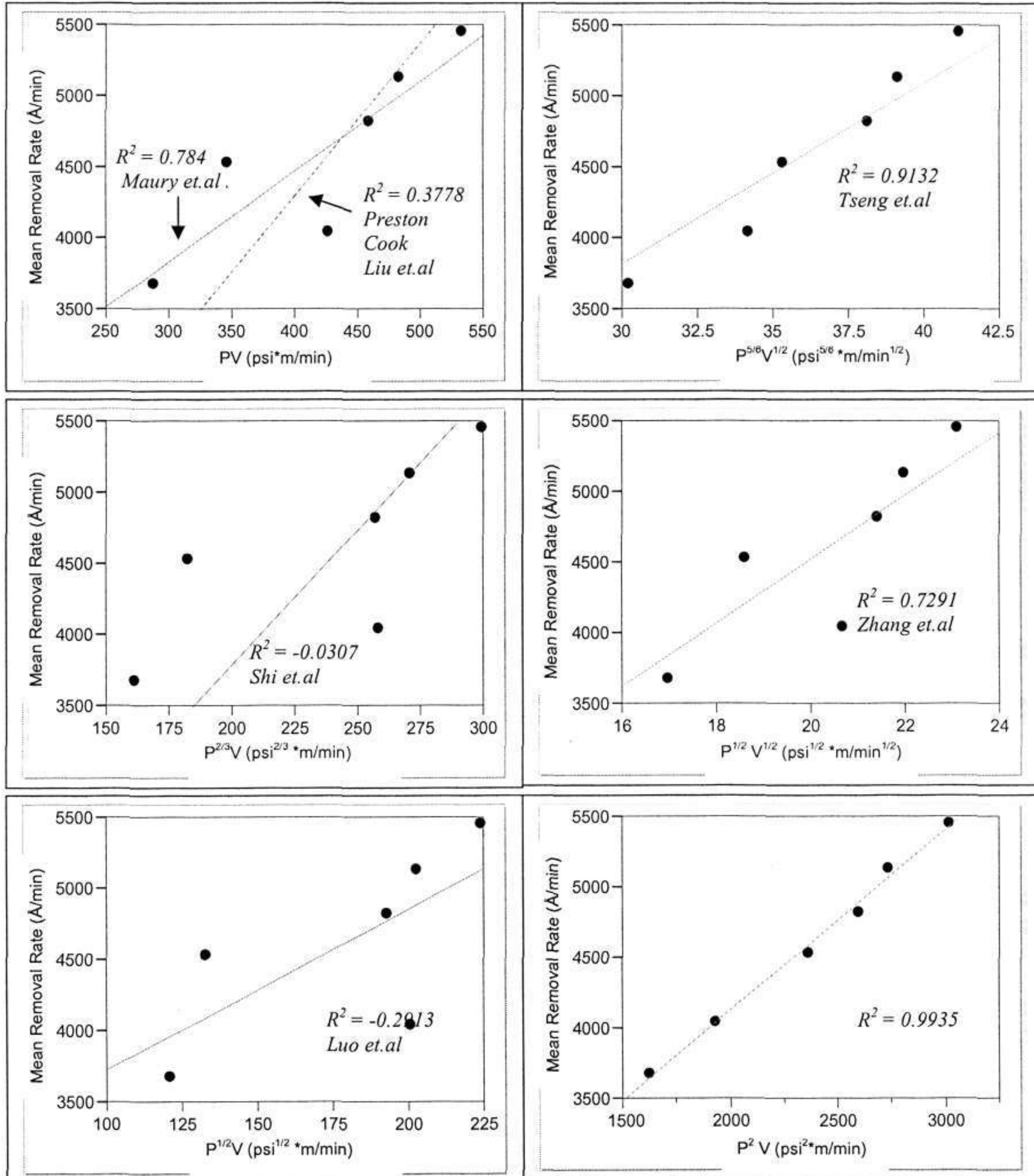

Fig. 2. 16 Material removal rate data of polysilicon with hole configuration B fit across various models

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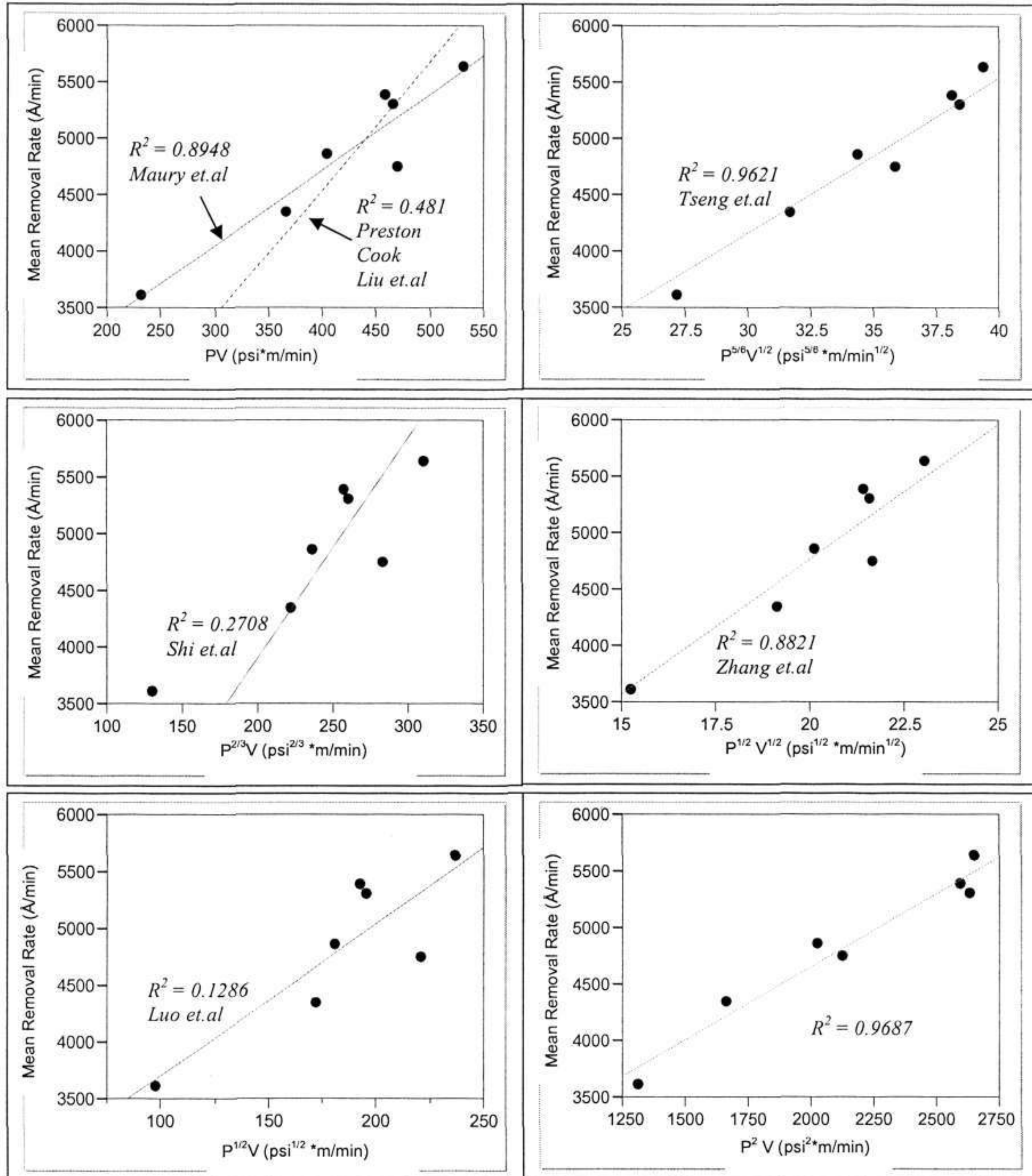

Fig. 2. 17 Material removal rate data of polysilicon with hole configuration C fit across various models

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The prediction of the removal rate for polysilicon based on the following equation

$$RR_{poly} = KP^2V + K_c \tag{2-24}$$

is statistically evaluated via cross validation. All the data are categorised within the respective group (according to the hole configurations). Cross validation assesses the predictive ability of a statistical model. The ideal is that models should be judged by their ability to predict unseen (untrained) data, rather than the degree to which a function fits the data. The statistical model in this context is a linear correlation of polysilicon removal rate with the product of P^2V. Let RR_{poly} denote the quantity to be predicted, in other words, RR_{poly} is the dependent variable. Prediction conditional on the P^2V would be made. Standing notation in this section is: D = data set, E=estimate set (subset of D used for estimation) and T=test set (subset of D used for testing). So the $D_{\text{hole configuration}} = [(PV^2_i, RR_i)|\ i = 1 \text{ to } z_n]$ consists of all the data obtained from experiments and grouped into three different hole configurations respectively. An efficient way and a variation of cross-correlation to evaluate a prediction formula is "take one out" [57]. The data set is divided into k subsets. One subsets is selected as the test set, $T_j = [(PV^2_j, RR_j)]$ and the remaining k-1 elements form the estimation set, E_j = all the data except the jth ($E_j = D \backslash T_j$). In practice test sets with 3 to 20 elements are often used [58]. The prediction model is therefore as shown in the following equation

$$\hat{Y}_j = \alpha_j X_j + \beta_j \tag{2-25}$$

and α_j and β_j estimated from E by the formula (2-26) - (2-29)

$$\alpha_j = \frac{\sum_{i \neq j}[(X_i - \overline{X}_i)(Y_i - \overline{Y}_i)]}{\sum_{i \neq j}[(X_i - \overline{X}_i)^2} \tag{2-26}$$

$$\beta_j = \overline{Y}_i - \alpha_j \overline{X}_j \tag{2-27}$$

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$$\overline{X}_j = \frac{\sum_{i \neq j} X_i}{n} \qquad \text{2-28}$$

$$\overline{Y}_j = \frac{\sum_{i \neq j} Y_i}{n} \qquad \text{2-29}$$

where $\hat{Y}_j$ is the prediction of removal rate and X_j the product of P^2V.

The prediction model based on products of P^2V is validated based on this method. The results are tabulated in table 2.3 to 2.5. According to the proposed model (2-24), the maximum deviation of 907Å/min from actual removal rate was observed for hole configurations A with 8 test set data and as the experimental data increases the difference between predicted and actual removal rate is reduced below 500Å/min as shown by the results for hole configuration B and C. This model suggests the trend of removal rate for polysilicon follows the product of P^2V instead of PV as shown in the removal rate of oxide. Therefore, a more general and versatile empirical model of material removal rate at the practical regime is proposed as follows

$$RR = K_p P^{\alpha_c} V + K_c \qquad \text{2-30}$$

where α_c is the material dependent coefficient which reflects sensitivity of the material being processed. In general, α_c =1 for oxide material as demonstrated by Maury [44] and α_c= 2 as shown in this section for polysilicon material.

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Table 2. 3 Cross validation for hole configuration A

Hole Configuration	J	X_j	α_j	β_j	$\hat{Y}_j$	Actual Removal Rate (Å/min)	$\lvert\Delta\rvert$
A	1	1963	1.1459	2043	4211	4402	191
A	2	1630	0.8827	2687	3069	3865	795
A	3	2367	1.0665	2203	4892	4591	300
A	4	2367	1.0665	2203	4892	5005	113
A	5	2367	1.0765	2190	4915	4937	22
A	6	2367	1.1056	2152	4984	4739	244
A	7	2732	1.1912	1972	5987	5079	907
A	8	2367	1.119	2135	5016	4647	368

Table 2. 4 Cross validation for hole configuration B

Hole Configuration	J	X_j	α_j	β_j	$\hat{Y}_j$	Actual Removal Rate (Å/min)	$\lvert\Delta\rvert$
B	1	2597	1.2722	1564	4867	4852	15
B	2	1935	1.2824	1535	4017	4052	36
B	3	3021	1.2363	1642	5376	5457	80
B	4	2597	1.2607	1583	4857	4933	77
B	5	2597	1.2946	1529	4891	4693	197
B	6	2732	1.2433	1621	5018	5140	122
B	7	1630	1.3232	1430	3587	3683	95
B	8	2397	1.2629	1605	4594	4404	191
B	9	2397	1.2802	1518	4548	4812	263
B	10	2397	1.263	1604	4594	4406	188

Table 2. 5 Cross validation for hole configuration C

Hole Configuration	J	X_j	α_j	β_j	$\hat{Y}_j$	Actual Removal Rate (Å/min)	$\lvert\Delta\rvert$
C	1	2597	1.2832	2092	5424	5402	21
C	2	2597	1.3021	2059	5440	5181	259
C	3	2131	1.2745	2117	4832	4725	107
C	4	2637	1.2976	2066	5487	5313	174
C	5	2131	1.2816	2095	4826	4827	1
C	6	2597	1.2946	2072	5434	5270	164
C	7	2597	1.2947	2072	5434	5268	166
C	8	2597	1.3082	2049	5446	5110	336
C	9	2655	1.2585	2138	5480	5715	234
C	10	2656	1.2673	2121	5487	5632	146
C	11	1319	1.1984	2302	3882	3621	261
C	12	2656	1.2732	2111	5492	5577	85
C	13	1663	1.3185	2000	4193	4368	175
C	14	1663	1.3137	2013	4198	4350	152
C	15	2597	1.2601	2132	5404	5674	270
C	16	2597	1.2623	2129	5407	5648	242
C	17	2130	1.2762	2112	4831	4749	82
C	18	2130	1.2762	2112	4831	4749	82
C	19	2597	1.2811	2096	5423	5428	6
C	20	2596	1.2721	2112	5415	5534	118

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2.5 Summary

Even though the CMP process is intuitively simple, achieving a more detailed understanding has been limited due to the large number of input variables. Therefore, a review of these basic input factors is presented in the first section of this chapter. Material removal rate is one of the major concerns in CMP process and therefore modeling material removal rate is essential to support the needs for process optimization, manufacturing control and understanding of physical behavior of the process. Thus, formulation of alternative material removal rate models continues to be an active area of research. To date, various material removal rate models have been proposed and most of the models are modeled as a function of pressure and relative velocity and some of these models are highlighted and summarised in the second section of this chapter. Unlike the pressure term, relative velocity component is one that is known with certainty and it is an essential quantity in every model; therefore kinematics of the CMP process is presented in the following section to illustrate the impact of relative velocity on material removal rate for completeness. In section 2.4, fundamentals study of material removal rate at practical regime is explored based on blanket wafers with polysilicon thin film material and various models as reviewed in section 2.2 are evaluated with the experimental data. Study reveals inadequacies of existing models in describing the polysilicon removal rate and an empirical model for polysilicon material is reported and evaluated through cross validation methodology. A more general and versatile material removal rate model at practical regime is then proposed for CMP applications IC fabrication.

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CHAPTER 3

DIRECT SHALLOW TRENCH ISOLATION CHEMICAL MECHANICAL PLANARIZATION

3.1 Introduction

Conventional silica based slurry used in shallow trench isolation (STI) chemical mechanical planarization (CMP) is unable to effectively planarize the oxide after trench filling and stopping on nitride layer over wide range of pattern density variations and die layout due to poor selectivity of oxide to nitride as reviewed in chapter 2. This leads to high nitride loss especially for isolated and narrow active structures as additional process time is needed to ensure the nitride film is exposed completely at large or dense active structures. Thus, reverse masking and etching, the addition of dummy active structures, or silicon nitride cap layer are the most commonly employed planarization-aids introduced prior to CMP to reduce dishing and erosion as shown in figure 3.1.

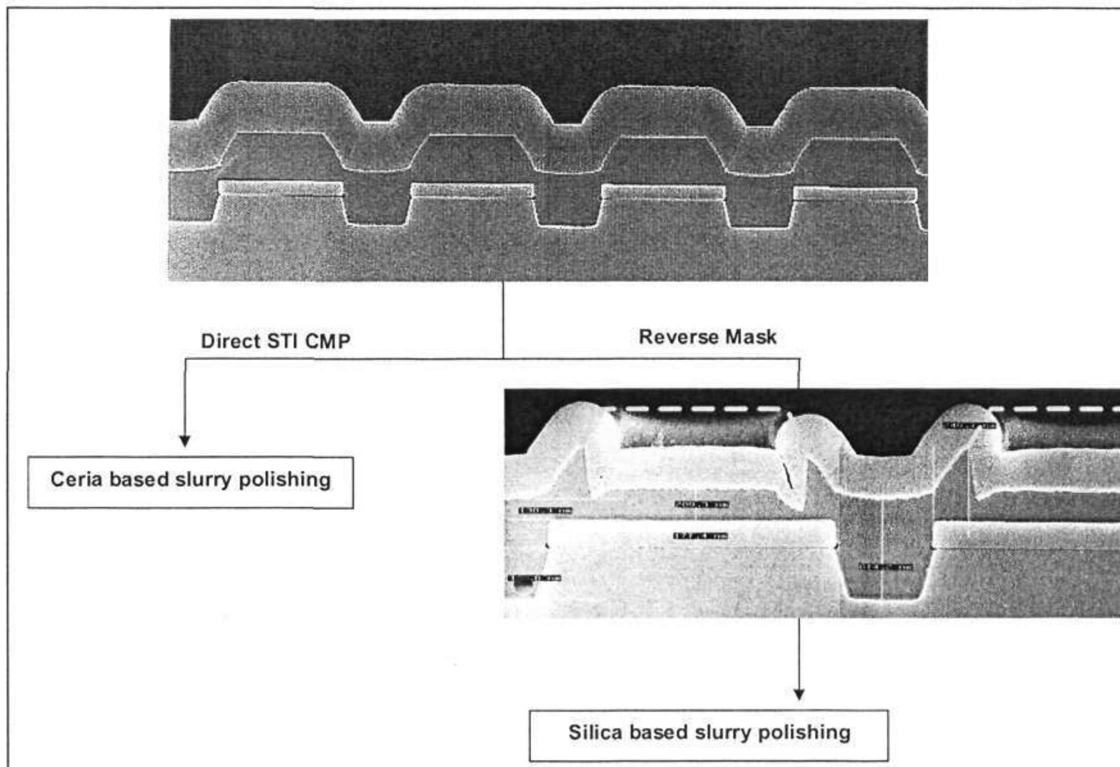

Fig. 3. 1 Two different schemes of STI CMP

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However, these planarization-aids are complex and costly to implement. Typically, a Fab can save up to USD100 million a year by moving towards a direct CMP method [11]. As every manufacturing step is driven by the desire to achieve the lowest cost and the removal of non-value-added operations, direct approach (i.e. without planarization-aids) therefore becomes one of the attractive options for STI CMP.

3.2 Shallow Trench Isolation (STI)

Transistors in ICs have conventionally been isolated by growing thick SiO_2 thermally in the regions between them. This so called local oxidation of silicon (LOCOS) masks off the active areas with a laver of silicon nitride. During the LOCOS isolation process, a thick oxide is grown in the field region of MOSFETs while the active region is protected by a masking layer of silicon nitride. However, oxidant diffuses under the edges of the nitride where unwanted oxide grows. The growth under nitride decrease as oxidant moves inward under the nitride edge. As a result, a gradually tapering oxide wedge merging into the pad oxide forms under the nitride [6]. The oxide grown under the nitride can lift the nitride edges. The shape of the field oxide as it penetrates under the nitride has been given the name "bird's beak". The bird's beak is a lateral extension of the field oxide into the active area of the device [59, 60]. Figure 3.2 shows an example of the bird's beak. The length of the bird's beak depends on the thickness of the pad oxide and nitride layers, and on the oxidation temperature and pressure.To accommodate the bird's beak it is necessary to make the active region larger. This uses extra chip real estate and is inefficient for ULSI circuits.

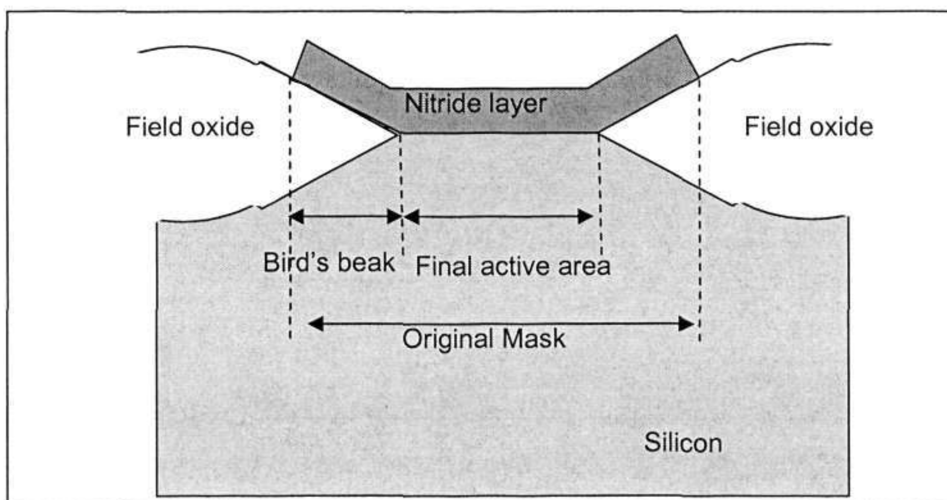

Fig. 3. 2 Bird's beak encroachment limits the scaling of channel widths.

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STI replaces LOCOS because STI has no bird's beak and provides a planar surface for further processing and enables an active area with higher device density. Improved latch up, and junction capacitance are added advantages of STI [61].

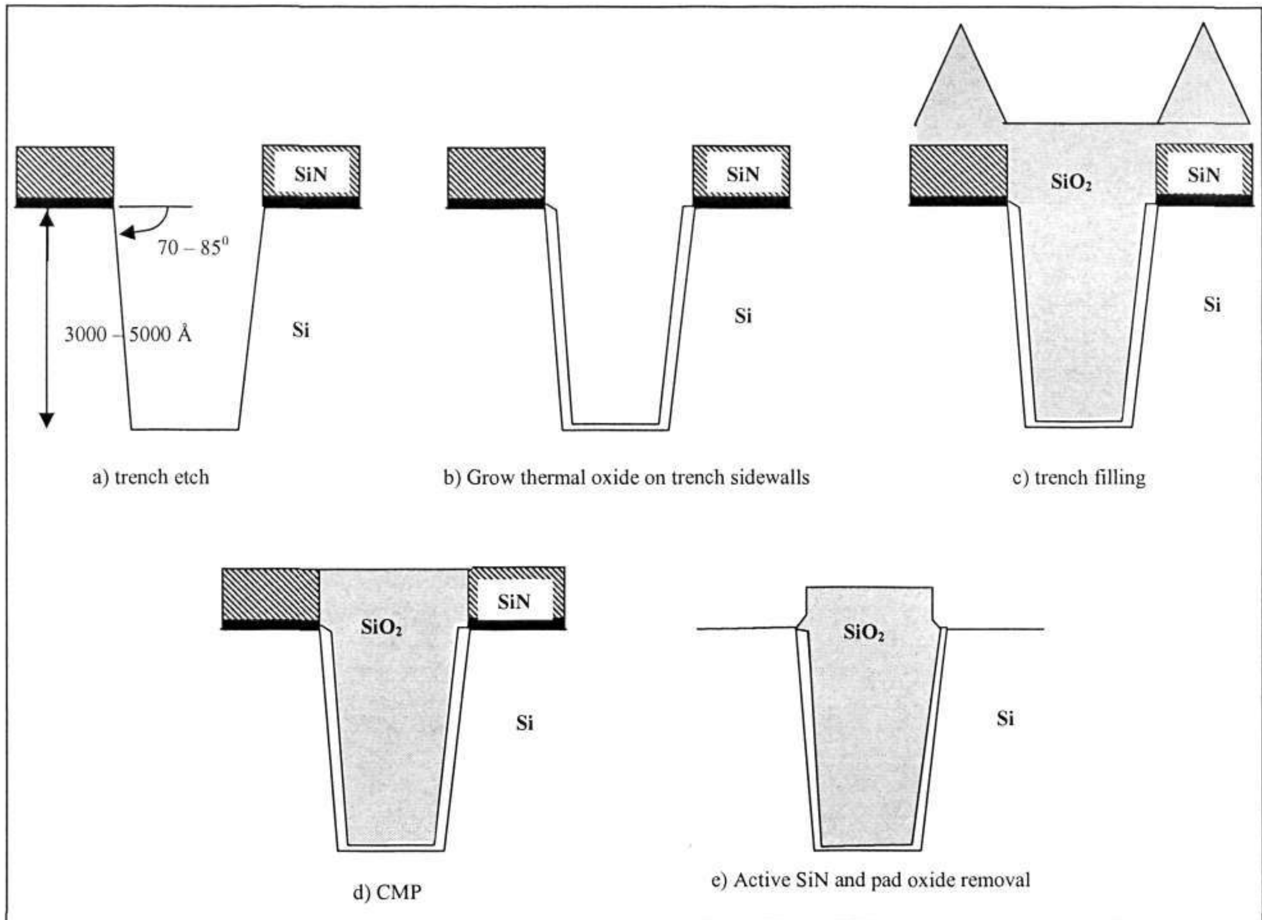

Fig. 3. 3 Process sequence used to form STI: a) etch trench in silicon substrate; b) grow thermal oxide trench liner to improve trench Si/SiO_2 interface; c) fill trench with HDP-CVD oxide; d) use CMP to planarize and stop at nitride layer; e) strip nitride to leave the STI structure

The sequence of steps (figure 3.3) for forming STI structures begins with the growth of a pad oxide, followed by a low pressure chemical vapor deposition (LPCVD) nitride layer. Resist is then applied and a mask is used to pattern the STI trench openings. The nitride and pad oxide are etched first. Then the trench is anisotropically etched to a depth of 3000Å~5000Å. The trench etching process should yield smooth trench sidewalls with angles of 70-85°, rounded bottom-corners to minimize stress, and a residue free silicon surface after etch. After the trenches are etched the resist is stripped and a thin thermal oxide is grown on the trench walls. Next, a high density plasma (HDP) CVD dielectric film (SiO_2) is used to fill the trench. This layer also

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covers the areas of the wafer where nitride remains. A CMP step is used to polish back the dielectric layer until the nitride is reached where the nitride acts as a CMP-stop layer. The dielectric material is densified at about 900°C by rapid thermal anneal (RTA) process. Then the nitride is stripped, leaving the STI structure in place.

3.2.1 Role of silicon nitride layer

The silicon nitride layer is primarily a CMP stop layer over the active silicon areas. CMP has an across wafer variation as well as an inherent pattern dependence. The material removal rate over isolated narrow geometries is much higher than over wide or dense array structures. The silicon nitride layer, therefore, has to be thick enough to leave a reasonable amount of nitride even in areas that suffer additional removal process time. The minimum nitride thickness must also consider coverage of the trench corner by the fill oxide after nitride strip. When the CMP removal rate of the trench-fill oxide is comparable to that of the nitride, the post-CMP surface of the nitride is approximately level with the surface of the trench-fill oxide. Since some of the trench is etched off during the post-CMP cleanups, the nitride thickness will determine the step-height between the active area silicon and the surface of the trench-fill oxide, which should be large enough to avoid the parasitic corner transistor effect.

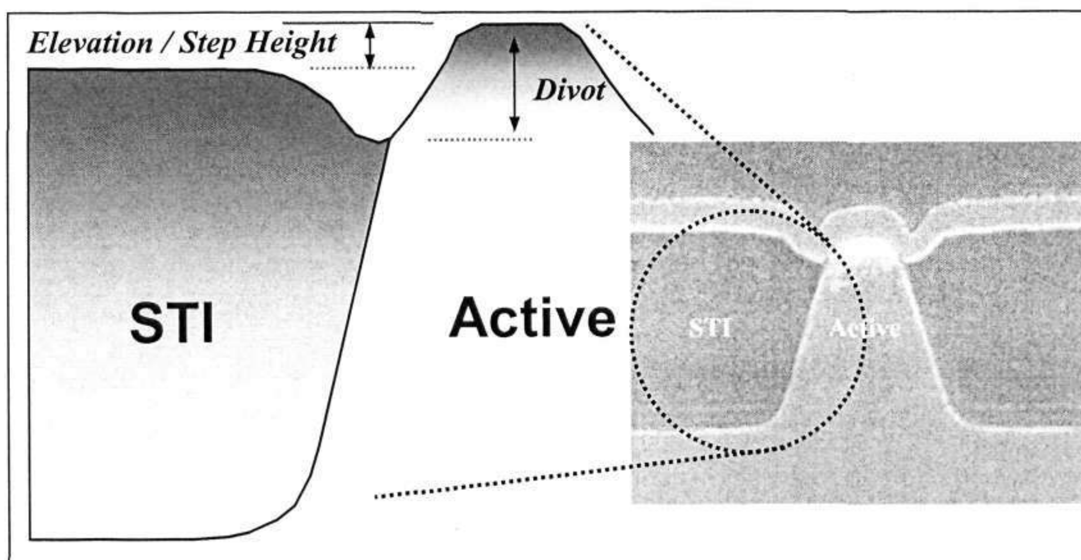

Fig. 3. 4 Post STI CMP after nitride strip. Elevation or step height: Height between isolated and active area. Divot: Erosion depth at the interfaces. (Courtesy: Chartered Semiconductor Manufacturing Ltd)

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3.3 STI CMP

In 1989 IBM published the first paper which discussed the STI CMP [3]. Before STI CMP, resist planarization and reactive ion etching (RIE) etch back process [62] was employed to isolate transistors. After CVD oxide deposition, a block resist is patterned over a large isolation area to bring up the surface to about same level as the active area. The block resist is then hardened, followed by planarizing resist spin and cure. Non-idealities of the planarizing resist due to the resist viscous flow, shrinkage after cure and pattern density effect (figure 3.5a).

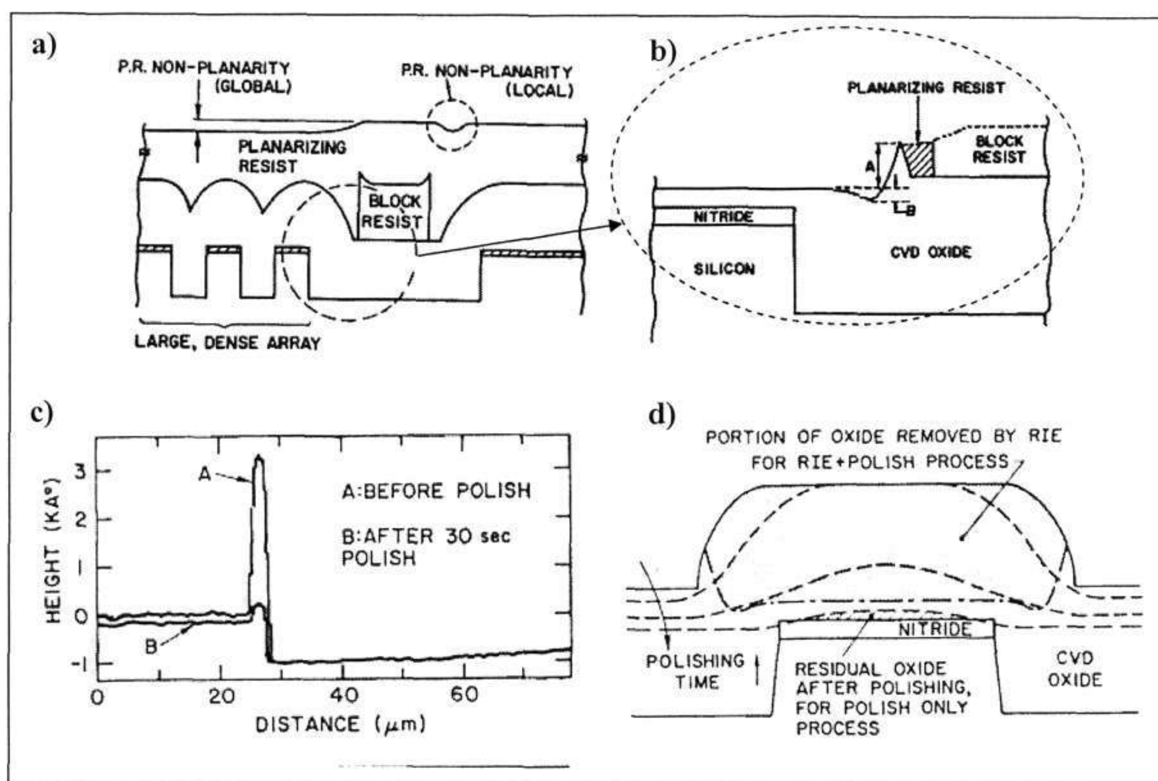

Fig. 3. 5 a) Cross section after block + planarizing resist; b) Cross section after RIE etch, showing local oxide spikes; c) Measured oxide step heights before and after CMP, showing fast removal rate of such spikes; d) Fundamental problem of "CMP-only" process. [3]

Resist spinning is followed by RIE planarization was done to reduce such non-planarities. However, there is a spike present after the RIE (figure 3.5b). Therefore CMP is used to remove the spikes. The CMP process can rapidly remove such small elevated features without significantly thinning the oxide on the flat areas (figure 3.5c). It should be pointed out that the CMP process alone is not viable for planarization because residual oxide will be left on the middle of large active areas or

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arrays after polishing (Figure 3.5d). Combination of RIE and CMP is therefore introduced as a new planarization technique. This technique is successfully applied to 16Mb DRAM technology for the first time.

The challenge in integrating CMP for STI is to expose silicon nitride completely across all active regions, with minimal nitride loss and oxide dishing (maximum recess to the nominal thickness of the oxide in a trench). Device patterns strongly influence the CMP process. Generally, the process margin for CMP is small due to pattern dependencies, low oxide-to-nitride removal selectively, and nitride erosion. Common techniques to increase the process margin include the use of block masks, pattern resists etch-back, and dummy active areas. Although these methods increase the process margin, they also increase the cost and process complexity.

3.3.1 Selectivity

Unlike inter layer dielectric (ILD) CMP, STI CMP involves removing two materials, thus it introduces one very crucial factor that is selectivity (*S*), which is expressed as:

$$S = \frac{Oxide \quad Removal \quad Rate}{Nitride \quad Removal \quad Rate} \tag{3-1}$$

Removal selectivity is the ratio of the removal rates of different materials. Generally high selectivity is desired in the STI CMP process. Selectivity can significantly affect the CMP induced issues such as nitride loss and dishing and slurry is the primary factor. The main technological obstacle to a one step CMP process for STI planarization comes from the fact that the oxide overburden are not selective to silicon nitride. Conventional oxide polishing slurries have very little selectivity towards silicon nitride, around 5:1 at most [63].

3.3.2 Nitride loss (Erosion)

Nitride loss is mainly caused by the pattern density of the IC layout which will degrade the selectivity. Nitride loss occurs during the additional process time because

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the additional removing action causes some nitride to be removed. Thinning of the nitride layer is a serious problem because it causes the underlying active area to be damaged, gap fill capability as more nitride thickness is required prior to CMP thus increases the aspect ratio and variation of step height of STI which will affect the electrical performance of the transistor [64]. Variation of height of STI causes corresponding variations in polysilicon thickness in narrow width MOSFETs. Studies show that higher poly-depletion observed for higher step heights of STI is primarily due to the change in the thickness at the STI edge as shown in the figure 3.6.

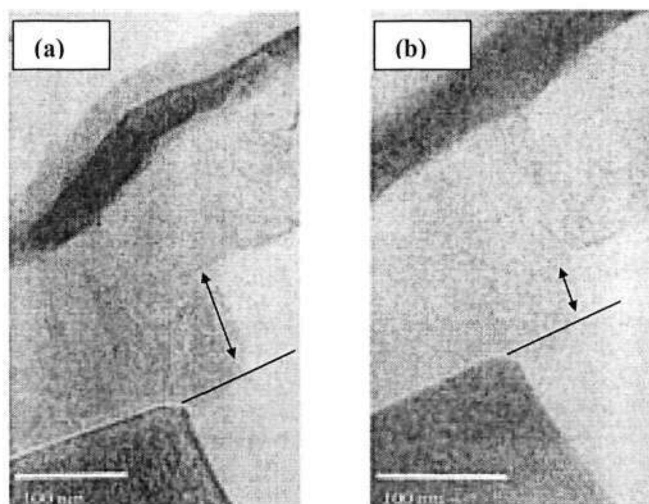

Fig. 3. 6 Cross section TEMs of the polysilicon gate for two different STI step heights. (a) large step height (b) small step height [64]

CMP uniformity is very crucial in advanced CMOS process to ensure uniform step height of STI which in turn reduces threshold voltage (V_{th}) variation.

3.3.3 Dishing

Dishing is a CMP process problem that involves the thinning of regions that remain exposed when a film is being removed down to a CMP-stop layer (in the case of STI, nitride is the stop layer). In general, dishing happens at larger open areas or large trenches in the STI process. Due to the pad not being infinite rigid, deformation will occur in large trenches such as those shown in figure 3.7. The thinning of these exposed areas (dishing) are known to be highly dependent on feature size, with the dishing effect becoming larger as the width of the oxide field is increased. If a pad exhibit perfect rigidity, CMP of the exposed oxide regions would produce a perfectly

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planar surface. This is due to the exposed recessed regions not being subjected to any polishing pressure. Since actual pads exhibit some flexibility, above-zero polishing pressures are produced in recessed areas, especially in the middle of wide exposed regions.

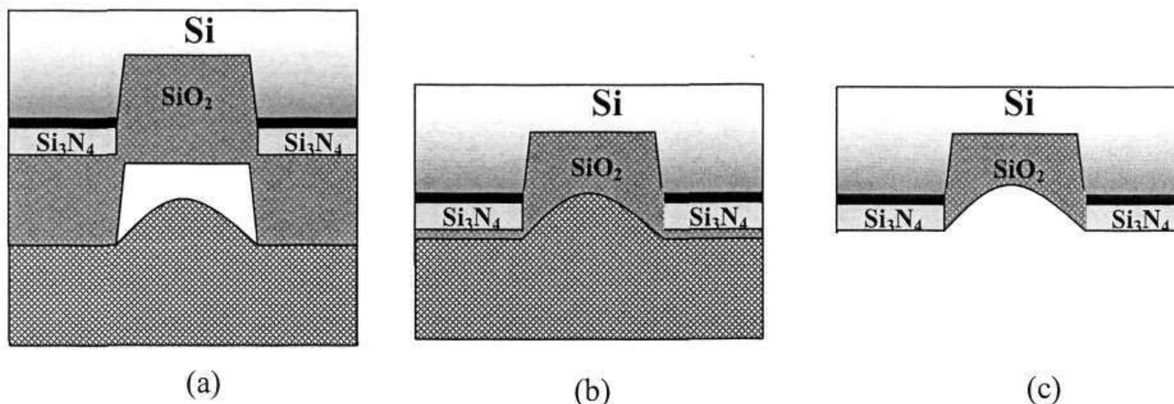

Fig. 3. 7 Origin of the dishing effect in CMP (a) polishing pad flexes into the trench opening (b) formation of concave surface. (c) trench area remains "dished" after planarization

Thus, oxide is removed from these regions, and a "dished" region exists after planarization. This is undesirable because it degrades the quality of the isolation and may damage the edges of the active area. Dishing must be minimized to maintain planarity for subsequent wafer processing. It is a serious impediment to the development of the Damascene process.

3.3.4 Active Dummy

Dummy structures are used to increase the pattern density in large open areas. Dummy structures are one of the first solutions to the pattern dependence problem [65, 66]. They reduce pattern density variation without forcing changes to device placement rules. The technique, however, poses electrical, design, and space constraints, with the main issue being that several times as many structures must be added within a die over original designs. This complicates the design and mask making process, and significantly raises the likelihood of defects.

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3.3.5 Reverse Mask

Dishing and nitride loss can be reduced by using an additional photolithography and RIE etch back prior to CMP. The reverse mask process prints the mask used to pattern the oxide trenches a second time, this time with a reverse tone resist. The resulting resist pattern protects the oxide trenches, while exposing the nitride-covered active regions (depend on the design rule). A partial oxide etch reduces the oxide amounts at the large active areas. Reverse masking is enormously expensive. It adds an additional lithography-etch-strip loop, with all the associated process costs, defect risks and cycle time. Since the feature size involved are close to the minimum design rule, the lithography step requires critical layer steppers. These tools, among the most expensive in the fab, are usually process bottlenecks to begin with. Greg Amico of Lam Research estimated the cost of the reverse mask loop at US$19-US$30 per wafer [67].

3.3.6 Direct STI CMP

As every manufacturing step is driven by the desire to achieve the lowest cost and the removal of non-value-added operations, direct polishing therefore becomes one of the attractive options for STI CMP. As the name implies, direct STI CMP is to remove and planarize the wafer immediately after film deposition without any planarization aid such as reverse mask as mentioned in a previous section (refer to figure 3.1).

3.4 Experimental Descriptions

In this section, equipments, slurry and metrology tools used in this work will be described. Two different types of slurry were used in the experiments to planarize the pattern wafers. First, conventional silica based slurry is used to remove the bulk of the oxide film then this is followed by ceria based slurry at platen 2 and 3 to clear all the oxide and stop at the nitride film. A 4-head and 3-platen CMP tool: Mirra® CMP system was used with 8''(200mm) wafers throughout direct STI CMP evaluation. The high selectivity slurry (HSS) was obtained from Hitachi Chemical and consists of two parts, ceria abrasive and polycarboxylate as planarity selective additive. The abrasive, additive and deionized (DI) water were mixed by a mix-in-placed slurry system

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(MIPSS) with abrasive and additive supply from slurry mobile cart. The slurry is then dispensed into small batches before being delivered to the respective platens. A schematic of the process setting diagram is shown in figure 3.8.

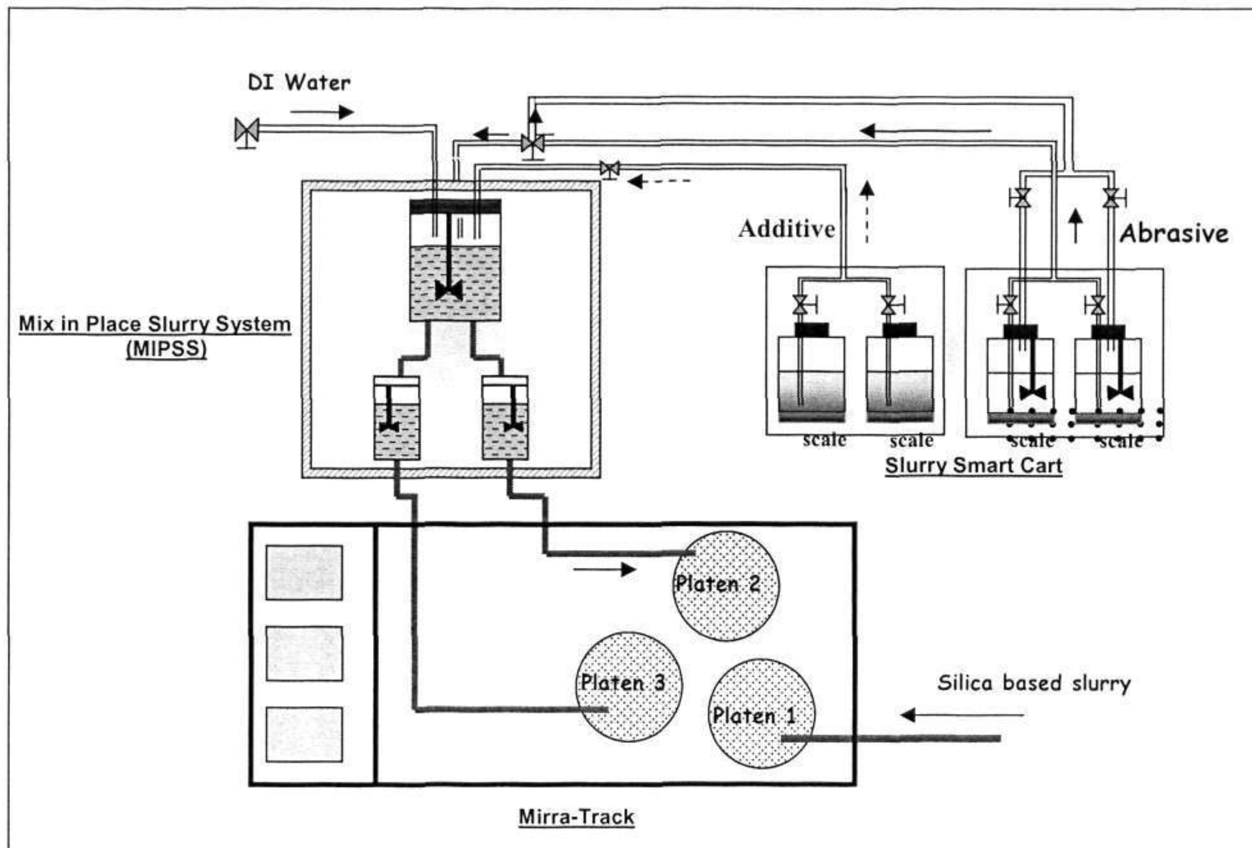

Fig. 3. 8 Layout of equipment setting

3.4.1 Architecture, functions and settings of the system components.

The system has three platens to which the polyurethane pads are attached as shown in figure 3.9. In this design, the wafers are handled by a robot to transfer them to a load/unload station while the three platens operate continuously. Each of the three independently-controlled polishing stations has a 20-inch (508mm) rotating platen and its own pad-conditioning arm. The heads are mounted on linear sweep slides that allow use of the entire pad surface. The "load cup" cleans the head and carrier film before a wafer is loaded and performs a first-pass clean of process wafers with high pressure DI water or chemical spray. Three wafers can be processed simultaneously, either in a batch mode or in-line mode. In the batch mode, all three wafers are loaded

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at the same time, processed using an identical recipe and unloaded together. In the in-line mode, only part of the process is accomplished on each platen. The wafer is loaded onto the carrier in the load cup and moved from platen to platen by the carousel. There are a total of four carriers attached to the carousel. The advantage of the in-line mode is its higher throughout and capability of programming the process in two or more steps. In this work, in line mode is applied with two steps recipe.

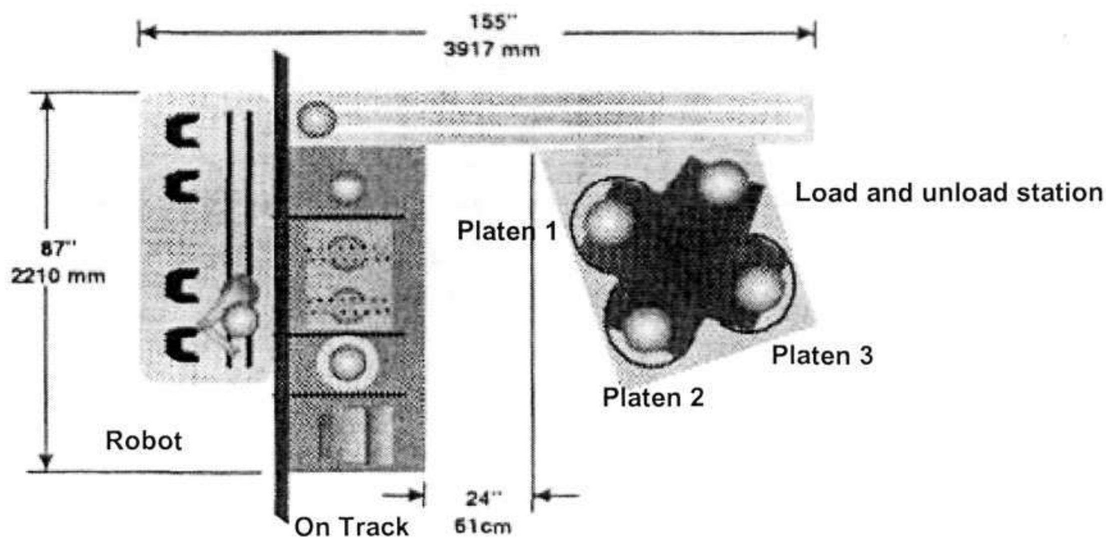

Fig. 3. 9 Mirra with On Track Integra

The system is also equipped with *in situ* removal monitor (ISRM) system. The Mirra's proprietary ISRM system detects changes in film thickness during process and is designed to provide an accurate, real-time process control on patterned or blanket wafers. However, in this work, the ISRM is disabled due to the inability to produce repeatable signals with ceria-based slurry and the fixed time is applied. Immediately after the process, the wafers are then transferred to the On Track cleaning unit to complete the dry-in and dry-out operation. The input parameters used in the experiment are shown in table 3.1.

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Table 3. 1 Input parameters setting for experiments

<table>
<tr><td rowspan="10">PLATEN 1</td><td rowspan="10">Head rotates across to platen.

Conditioning done in situ, end by polish.
1st polish step is a ramp.
2nd step is full polish condition.
No head sweep on ramp polish.
Head sweeps during main polish.
No endpoint during polishing. Use time controlled polishing.
Post polish, the head stops rotating and lifts off. 12s HPR during dechucking; then moves clockwise to 2nd platen.
New pad ex-situ break-in: 4.5lbf DF, 109rpm/50 rpm/s(Platen), 111rpm/50rpm/s (Dresser),10 min</td><td>STEP</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
<tr><td>Platen Speed /Acceleration</td><td>109/40</td><td>109/15</td><td>93/15</td><td>93/15</td></tr>
<tr><td>Head Speed /Acceleration</td><td>146/40</td><td>146/15</td><td>87/15</td><td>87/15</td></tr>
<tr><td>Inner Tube</td><td>1.0</td><td>4.0</td><td>Vented</td><td>6.0</td></tr>
<tr><td>Retaining Ring</td><td>2.0</td><td>6.0</td><td>2.0</td><td>7.0</td></tr>
<tr><td>Sweep rate</td><td>0</td><td>10/min</td><td>0</td><td>0</td></tr>
<tr><td>MEM</td><td>Vac</td><td>4.0</td><td>Vented</td><td>6.0</td></tr>
<tr><td>Slurry FR</td><td>200</td><td>200</td><td>0</td><td>0</td></tr>
<tr><td>HPR</td><td>0</td><td>0</td><td>HPR</td><td>HPR</td></tr>
<tr><td>Time</td><td>4</td><td>Varies (30-50Sec)</td><td>6</td><td>8</td></tr>
<tr><td></td><td></td><td colspan="5">Dresser:
Speed: 79 rpm
Down Force: 4.5lbf
Sweep: Customized Sinusoidal Sweep,1.75 in to 9.30in sweep, 10 zones, 10 sweeps/min</td></tr>
<tr><td rowspan="10">PLATEN 2/3</td><td rowspan="10">Head rotates across to platen.

Conditioning done in situ, end by polish.
1st polish step is a ramp.
2nd step is full polish condition.
No head sweep on ramp polish.
Head sweeps during main polish.
No endpoint during polishing. Use time controlled polishing.
Post polish, the head stops rotating and lifts off; 12s HPR during dechucking; then moves clockwise to 3rd platen.
New pad ex-situ break-in: 4.5lbf DF, 109rpm/50 rpm/s(Platen), 111rpm/50rpm/s (Dresser),10 min</td><td>STEP</td><td>1</td><td>2</td><td>3</td><td>4</td></tr>
<tr><td>Platen Speed /Acceleration</td><td>77/40</td><td>77/15</td><td>93/15</td><td>93/15</td></tr>
<tr><td>Head Speed /Acceleration</td><td>73/40</td><td>73/15</td><td>87/15</td><td>87/15</td></tr>
<tr><td>Inner Tube</td><td>1.0</td><td>4.0</td><td>Vented</td><td>6.0</td></tr>
<tr><td>Retaining Ring</td><td>2.0</td><td>4.6</td><td>2.0</td><td>7.0</td></tr>
<tr><td>Sweep rate</td><td>0</td><td>10/min</td><td>0</td><td>0</td></tr>
<tr><td>MEM</td><td>Vac</td><td>4.0</td><td>Vented</td><td>6.0</td></tr>
<tr><td>Slurry FR</td><td>200</td><td>200</td><td>0</td><td>0</td></tr>
<tr><td>HPR</td><td>0</td><td>0</td><td>HPR</td><td>HPR</td></tr>
<tr><td>Time</td><td>4</td><td>Varies (50-70Sec)</td><td>6</td><td>8</td></tr>
<tr><td></td><td></td><td colspan="5">Dresser:
Speed: 79 rpm
Down Force: 4.5lbf
Sweep: Customized Sinusoidal Sweep,1.75 in to 9.30in sweep, 10 zones, 10 sweeps/min</td></tr>
</table>

3.4.1.1 Carrier (Head)

The challenge in carrier design is to assure the required CMP process performance: low non-uniformity, high removal rate, low defects, good head to head matching, and low pressure with high speed capability. A conventional carrier coupled with polyurethane-based polyurethane pad have a limitation in achieving a low non-uniformity due to the pad deformation at the edge of the wafer during the process, as manifested by a slow or fast edge polishing rate. In this work, an advanced polishing head namely Titan Head™ design is used together with advanced edge performance (AEP) retaining ring to improved CMP performance. The retaining ring design has a

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significant impact on NUWIW due to the ring-pad-wafer-membrane interaction as shown in the figure 3.10.

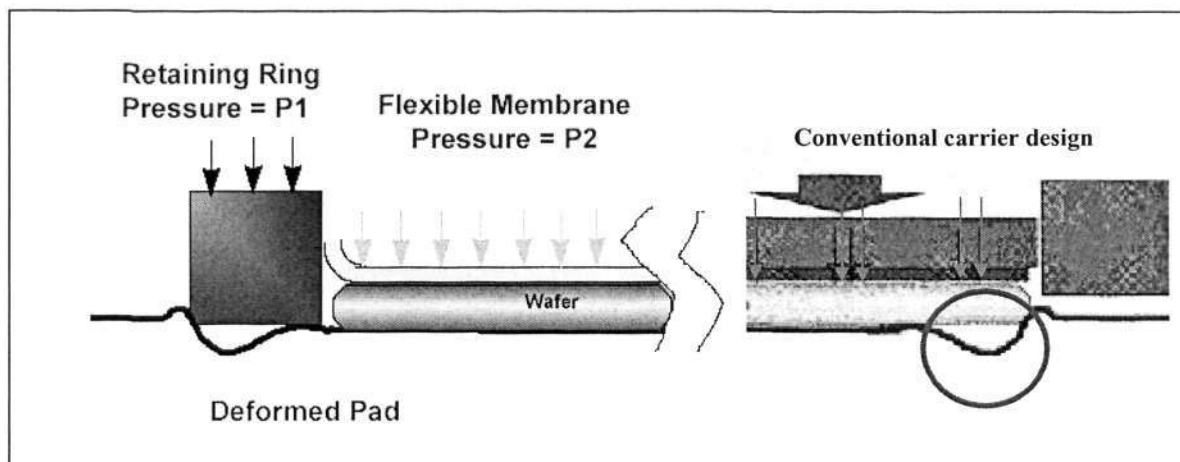

Fig. 3. 10 Schematic diagram of retaining-ring/pad/wafer/membrane interaction [23]

In a Titan Head design (figure 3.10), an independently-controlled pressure (P_1) is applied onto the retaining ring to absorb pad deformation around the wafer edge during polishing. Meanwhile, a uniform pressure (P_2) is applied by a flexible membrane over the wafer backside to achieve a desirable polishing rate.

3.4.1.2 Polyurethane Pad

In this study, Rodel® IC1010 pad are used. The Rodel® IC1010 is made of a rigid, microporous polyurethane material. Additionally, the pad has a tighter specific gravity range and unique propriety grooving pattern. The IC1010 comes in a prestacked configuration. The top pad is stacked on to a Suba IV substrate, resulting in the stacked specifications listed [68] in table 3.2.

Table 3. 2 Properties of IC1010 pad [68].

Top Pad	Specific Gravity	78-84
	Thickness	2mm (80mil)
	Hardness-Shore D	52-62
	Compressibility	0.5-4.0
Stacked Pad	Durometer	35-65 Shore D
	Compressibility	0-6%
	Deflection	0-0.15mm (0-6 mil)

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3.4.1.3 Slurry Mobile Cart

This Slurry Mobile Cart (figure 3.11) is used to re-circulate and monitor slurry delivery to the MIPSS (figure 3.12). The system provides a mobile platform to deliver slurry. In this study, the Slurry Mobile Cart will re-circulate raw slurry from two 10-litre containers on a switching basis, while accurately monitoring slurry levels in each container by using a patented Load Cell Technology. The slurry is re-circulated in a loop out to the MIPSS and back into the Mobile Cart in a continuous fashion to assure it remains in suspension. In addition, the slurry is stirred via variable speed stir motors. The system provides continuous mixing of the slurry to prevent any settling of the slurry components. The incoming ceria concentration to MIPSS is measured during the start-up. The solids concentration specification is 5.0 +/- 0.2%. A sample is collected from the slurry mobile cart before the MIPSS. The sample is then baked dry and the remaining solids content and size distribution of ceria are measured. The measurement is facilitated by Hitachi Chemical Ltd.

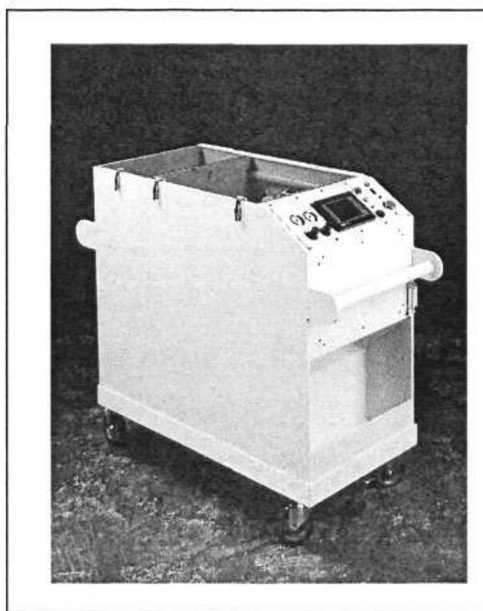

Fig. 3. 11 Slurry Mobile Cart

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3.4.1.4 Mix in Place Slurry System (MIPSS)

Abrasive and additive are delivered from slurry mobile cart to the MIPSS. The MIPSS will mix the three different mixing ratios as indicated in the table 3.3.

Table 3. 3 Mixing Ratio test

Test	Item	Specification
Mixing Accuracy	1:0 (Ceria: DI)	+/- 2%
	1:2 (Ceria: DI)	+/- 2%
	1:19 (Ceria: DI)	+/- 2%

For each mixing ratio, a total of three samples will be collected. Sample A will be incoming ceria slurry from the slurry mobile cart as mentioned in the previous section. The incoming ceria slurry solids concentration should be verified each time to confirm it is within the specification of 5% +/-0.2%. Samples B and C will be collected from the slurry arms on platen 2 and 3 respectively.

The purpose of MIPSS is to automatically blend slurry and up to four components, then deliver the blended slurry directly to the Mirra's three separate platens. This system contains two mix reservoirs. Mix reservoir 1 located on the left hand top section of the system, is used to blend slurry to be delivered to dispense reservoir 1 and dispense reservoir 2. In the experiments, mix reservoir 2 is not used. Dispense reservoir 1 receives the blend slurry from mix reservoir 1 and delivers the blended slurry to platen 2 within the Mirra tool. MIPSS is shown in the figure 3.12. First, the request volume of the abrasive components of the slurry will be drawn into the Mix reservoir. When the proper volume has been attained, the system will draw in the requested volume of DI water. After completion, the requested amount of another components of the slurry, additive, will be drawn in. The ratio of 1:8:11 is used in this experiment. First component refers to abrasive then followed by DI water and lastly additive. While the blending sequence is occurring, the stir motor within the reservoir is ensuring the various components are appropriately mixed.

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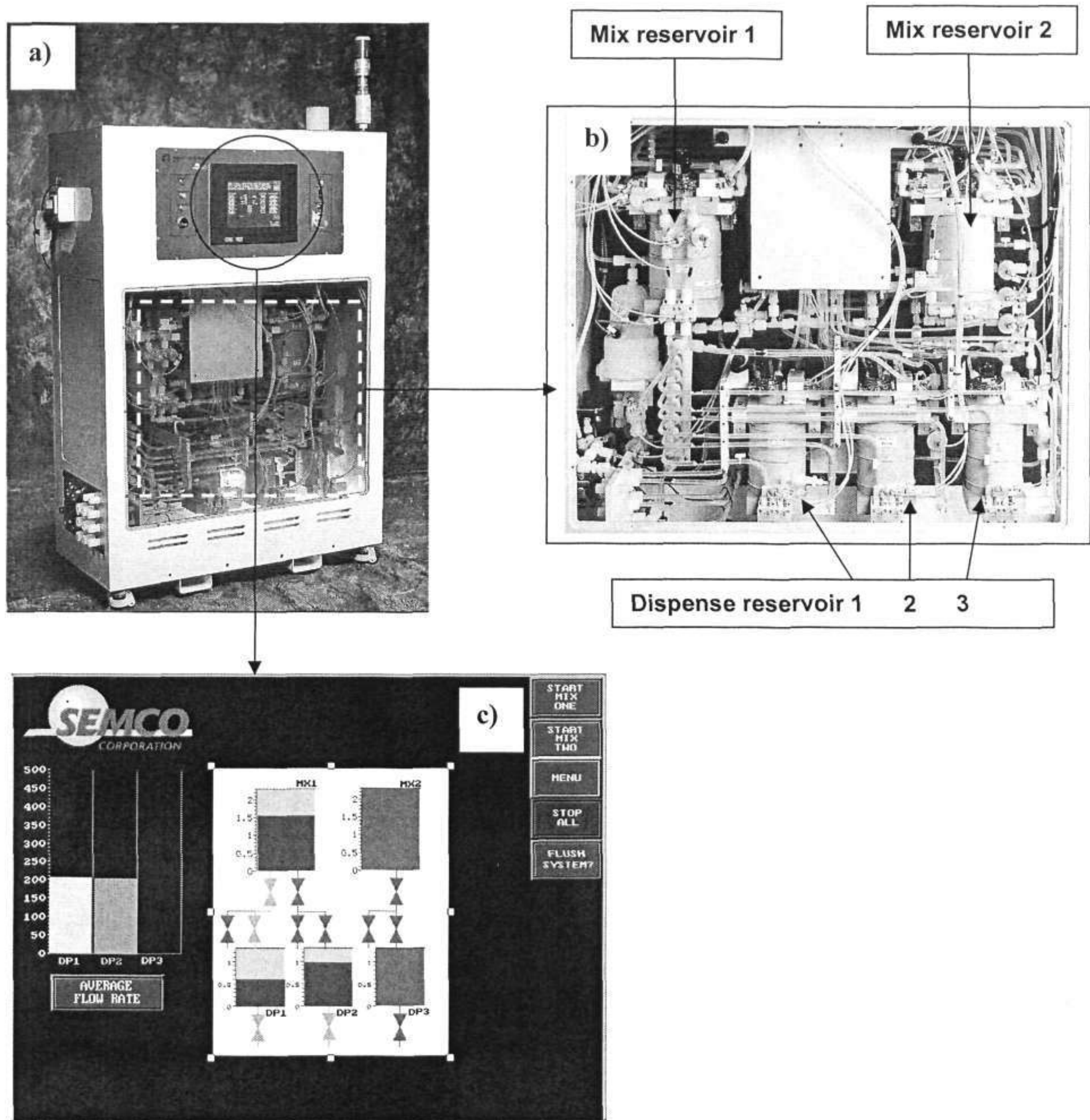

Fig. 3. 12 MIPSS a) Machine layout b) Mix and dispense reservoirs c) Control panel

3.4.1.5 On Track

Post-CMP wafer clean is an inseparable part of the CMP process. A successful CMP process integration is not only able to planarize the surface but also able to clean the surface of the wafers thus reduce the defects. Cylindrical polyvinyl alcohol (PVA) brushers are used in the On Track system (figure 3.13). PVA material has an open structure consisting of interconnecting cells that allow the brush to be constantly

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flushed with DI water during wafer cleaning. These softer brushers clean more efficiently when they are compressed against the wafer [69, 70].

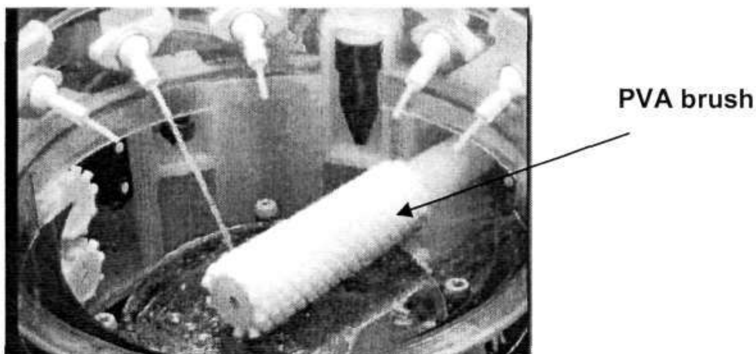

Fig. 3. 13 PVA brush

As the brush height is lowered and pressure on the wafer increases, the number of particles remaining reaches a minimum when the brushes are compressed 2mm [71]. PVA brushes are compatible with cleaning chemistries in the 2 to 12 pH range, and NH_4OH is commonly used with this brush material. The recipe used in this experiment to perform the cleaning process is summarised in table 3. 4.

Table 3. 4 Recipe for brush cleaning.

	Parameter	1	2
BB1	Brush speed (rpm) :	120	
	NH4OH Flow rate (ml/min):	2.6	
	Water flowrate (ml/min):	1000	
	Roller speed (rpm):	50	
	Time (s):	40	
	Edge clean flow	on	
	Exhaust (mls)	12	
	Brush height (mm)	3	
BB2		1	2
	Brush speed (rpm) :	120	120
	NH4OH Flow rate (ml/min) :	2.6	0
	Water flowrate (ml/min):	1000	1000
	Roller speed (rpm):	50	50
	Time (s):	10	40
	Edge clean flow	on	on
	Exhaust (m/s)	12	
	Brush height (mm)	3	3

The wafers are transported to brushes station 1 from load station by belts. NH_4OH is used to alter the zeta potential of the wafer, brushes and particles. The concentration of NH_4OH is around 29% weight percentage. The wafers are then transported to another a second brush and only DI water is used for a duration of 40s as spray. Following brush cleaning, the wafers are transferred to the spin rinse and dry station

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where DI water sprays onto the front and back wafers prior to application of heat during the drying cycle. An edge-handling unloader transfers the dry wafers to the output station. The recipe used for spin station is summarized in the table 3.5.

Table 3. 5 Recipe for spin station

SPIN STATION	DIW jet Heat lamp comes on during the spin dry high rotation cycles.		1	2	3	4	5
		UWF	on	on	on	0	0
		LWF	on	on	on	0	0
		Temp	off	off	on	on	on
		Speed (rpm)	100	300	400	1000	1800
		Time (s)	1	9	2	2	15
		Exhaust (m/s)	4.5				
		Hepa filter set to min value of 4m/s					

3.4.2 Ceria based slurry

In this section test method for ceria-based slurry is reported. Properties of two main components of the slurry namely ceria abrasives and polycarboxylate additives are investigated in terms of weight content, specific gravity, viscosity, pH and particle size (for abrasive only). All these test were facilitated by Hitachi Chemical Co., Ltd. Results of these properties are presented in section 3.5.

3.4.2.1 Test method for weight content

An aluminum cup with inside radius and depth of about 85mm, 55mm respectively and a weight of 5g is used. First of all, an aluminum cup with 1mg accuracy is measured and term as W1. 10ml of the sample (abrasive and additive) is placed into the cup and weight measurement is taken and term as W2. Afterwhich, the sample is kept in an oven at 150 ± 3°C for 1.0 ± 0.1hour (abrasive) and 1.5 ± 0.1hour (additive) respectively. The sample is then taken out and the weight of the aluminum cup is measured. This procedure is repeated twice and the weight of the content of the abrasive or additive is calculated as follows:

$$weight\ content\ (\%) = \frac{(W3-W1)}{(W2-W1)} \times 100 \qquad \textbf{3-2}$$

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3.4.2.2 Test method for specify gravity

Specific gravity meter with the measurement range of 1.000-1.060, 0.002 minimum graduation and 160mm length is used. First, the water temperature is checked inside the water bath at 25.0 ± 0.3°C. About 100ml of the sample (abrasive and additive) is placed into a polyethylene container, sealed tightly and placed into the water bath for about 30 min. After that, the polyethylene container is taken out and the 100ml of the sample is then added into the graduated cylinder and the specific gravity is immediately taken.

3.4.2.3 Test method for viscosity

Ubbelohde's viscometer with the measurement range of 0.6-3.0 cSt. is used. The water temperature inside the water bath is checked 25.0 ± 0.3°C and then 100ml of the sample (abrasive and additive) is sealed tightly in a polyethylene container and placed in the water bath for about 30min. Afterwhich, the Ubbelohde's viscometer is used immediately and the dynamic viscosity is measured. The viscosity of abrasive and additive sample is then calculated as follows:

$$viscosity\ (mPa.s) = Dynamic\ viscosity\ (St)\ x\ Specific\ gravity\ (g.cm^3) \qquad \textbf{3-3}$$

3.4.2.4 Test method for pH

HM14P (Toa Dempa Kogyo) pH meter model is used. Before measurement, pH meter is calibrated with standard buffer, solution made by Wako Junyaku Kogyo. Then the electrode of pH meter is placed into the sample (abrasive and additive) and measurement reading is taken after 3 min.

3.4.2.5 Test method for particle size (abrasive only)

MasterSizer (Malvern) that employs the laser diffraction method is used to measure the particle size distribution. Average particle size (μm) which consists of 50% in

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volume of slurry and 80% in volume cumulatively (cumulative particle size) is measured.

3.4.3 Wafer preparation

Two distinct types of wafers are used in the study. First, around 4 pods or 100 blanket wafers are used to study the removal rate, uniformity and contaminations of the process. Another 50 blanket wafers were used to monitor the stability of the equipment before polishing any pattern wafers. 100 pattern wafers are mainly used to characteristic the CMP performance on the dishing, erosion and non-uniformity within wafer (NUWIW) and non-uniformity within die (NUWID) as well on various pattern densities.

3.4.3.1 Blanket wafers

A Czochralski (CZ), 200mm, B, P-type <100> test bare silicon wafers with thickness of 725μm from Sumitomo Mitsubishi Silicon Corporations (SUMCO) is used. Undoped silicon glass (USG) of around 16,000Å is then deposited on top of it. Thickness measurement is taken by ASET-5x in 49 points polar map and 121 points diameter line scan. Next, pre-CMP contaminations of wafers check are measured by Surfscan (SP1).

3.4.3.2 Pattern wafers

The pattern wafers used in this experiment consists of the 90nm STI test structure only or so-called Layer 10 mask to characterize direct STI CMP. For comparison purpose, Layer 11 mask as a reverse mask is also used for conventional process flow. This test chip was designed with the basic intention of allowing rapid characterization, empirical modeling and comparison of pattern dependencies as a function of process, consumable, or equipment options.

The overall field size of this STI test mask on wafer is 29,998μm x 23,938μm. This mask consists of very small trench sizes for 90nm technology and various line-in-

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space for planarization characterization. Line-in-space structure consists of single line as an active area in wide space as a trench area to test line survivability during CMP. The layout of the L10 mask is shown in figure 3.14.

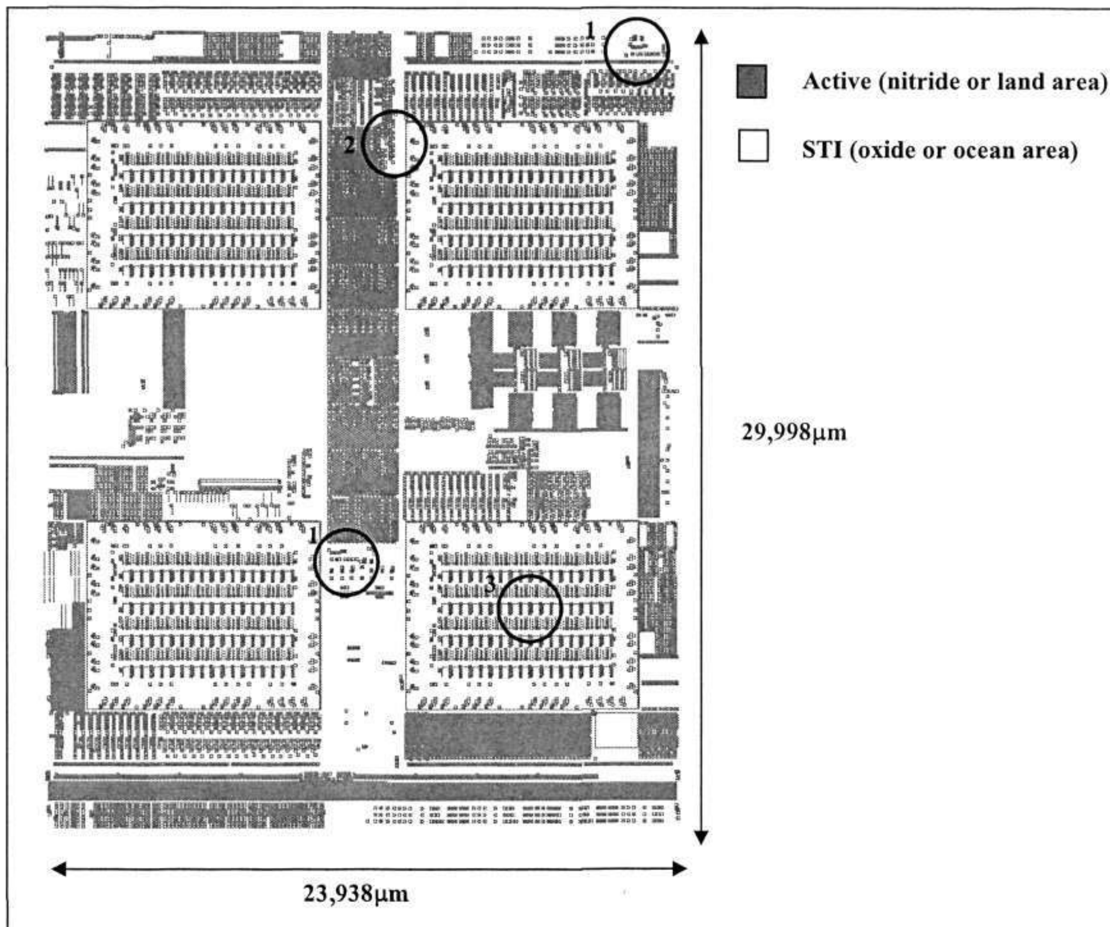

Fig. 3. 14 Layout of active and isolation of a die

Region 1 indicated in the figure 3.14 has various trench sizes, which are designed to monitor dishing. Whereas area 2 is the location for process monitoring and area 3 is part of the region of SRAM transistor. Details of these areas are magnified and shown in figure 3.15-3.17.

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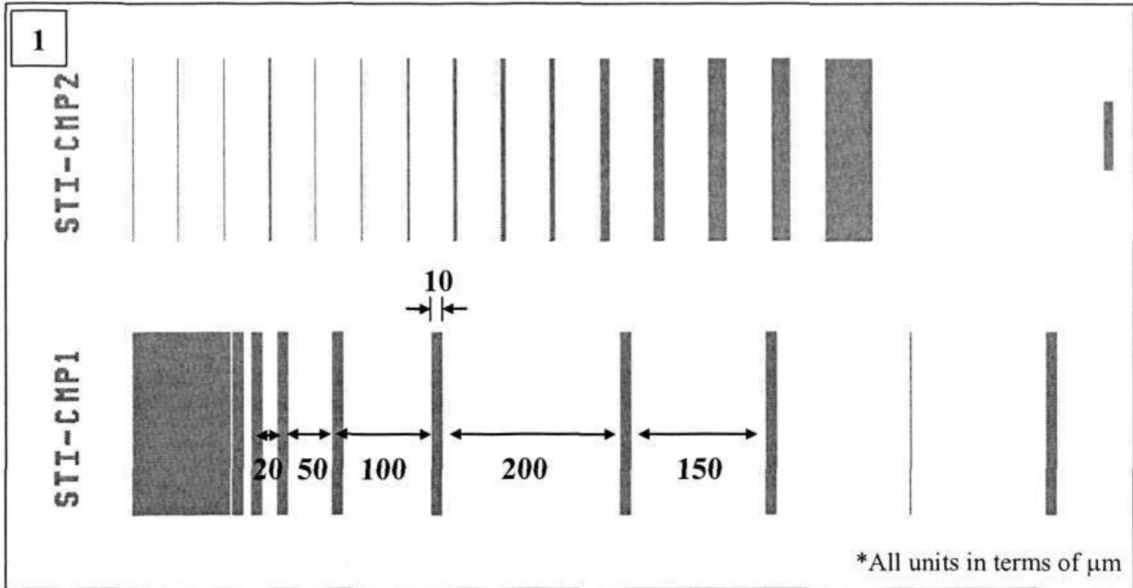

Fig. 3. 15 Various trench sizes within a die.

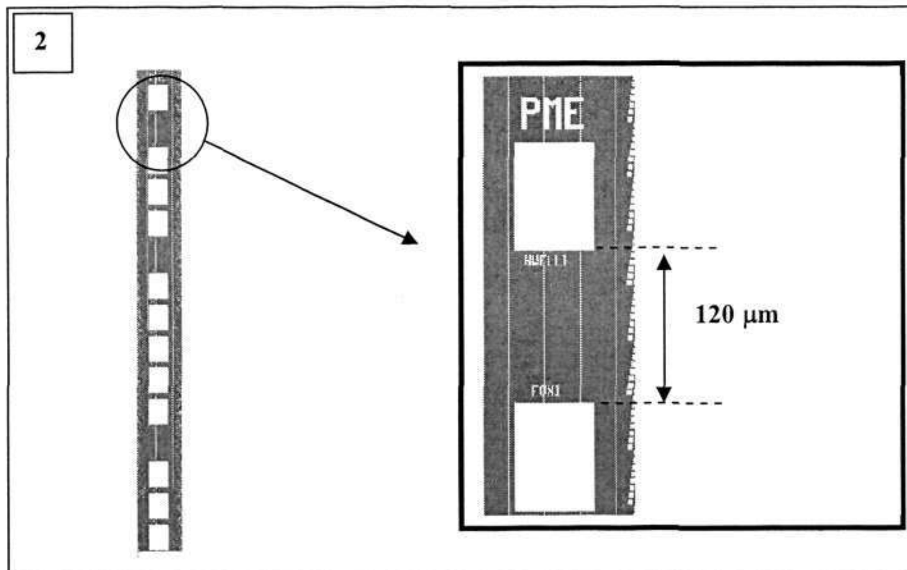

Fig. 3. 16 Process monitoring location.

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3

0.88

1.44

0.23

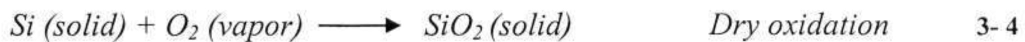
0.14

0.3

* All units in terms of µm

Fig. 3. 17 SRAM

Similarly, a CZ, 200mm, B, P-type <100> prime bare silicon wafers with thickness of 725µm from Sumitomo Mitsubishi Silicon Corporations (SUMCO) is first cleaned with Radio Corporation of America (RCA) clean and hydrofluoric acid (HF). The first step in the RCA clean is called Standard Clean-1 (SC1). Its function is to remove organic film contamination, metals and particles. Followed by the second step, Standard Clean (SC2). Its function is to remove inorganic ions, alkali ions, and heavy metals. After cleaning, around 100Å oxide layer is thermally grown on the surface at 800^{0}C in the amorphous state termed fused silica.



$$Si\ (solid) + O_2\ (vapor) \longrightarrow SiO_2\ (solid) \qquad \textit{Dry oxidation} \qquad 3\text{-}4$$

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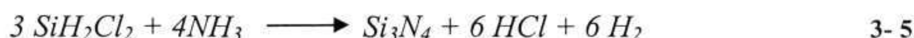
The function of this layer is called a pad or buffer oxide, which is to cushion the transition of stresses between the silicon substrate and the subsequent deposited nitride. Then, a thickness of 1600Å of nitride is deposited with dichlorosilane (SiH_2Cl_2) and ammonia (NH_3) by low-pressure chemical vapor deposition (LPCVD) at 760^{0}C and the chemical reaction can be expressed as:



$$3\,SiH_2Cl_2 + 4NH_3 \longrightarrow Si_3N_4 + 6\,HCl + 6\,H_2 \qquad 3\text{-}5$$

LPCVD is a high temperature deposition method and used to deposit a nitride layer (refer to figure 3.18) because LPCVD produces a better film quality and less hydrogen integration than plasma enhanced chemical vapor deposition (PECVD) method. In addition, LPCVD is not prone to plasma-induced device damage, which is unavoidable with the PECVD process.

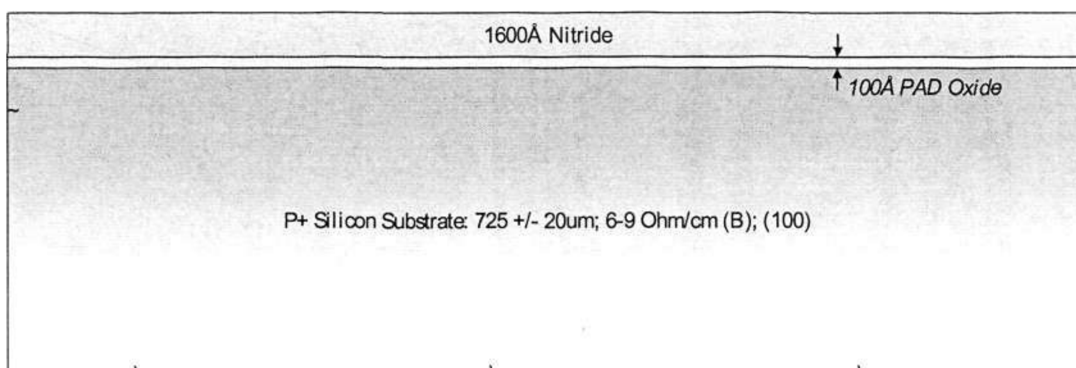
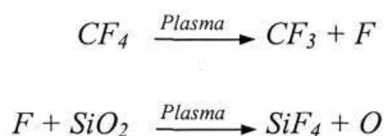


Fig. 3. 18 Pad oxide and nitride deposition

First layer mask i.e. L10 mask is used to define the active and isolation regions using 193nm resist and ASML 1100 scanner. A resist pattern is used to protect all of the areas where active devices will be formed. The nitride layer at the isolation area is then etched away and the pad oxide as well. Plasma with CF_4 gases is employed to achieve an anisotropic etch. The chemical reactions of plasma etching of silicon nitride and silicon oxide are:



$$CF_4 \xrightarrow{Plasma} CF_3 + F$$

$$F + SiO_2 \xrightarrow{Plasma} SiF_4 + O$$

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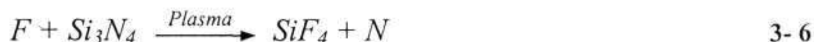

$$F + Si_3N_4 \xrightarrow{Plasma} SiF_4 + N \quad 3\text{-}6$$

Argon is used in the etching process to increase the ion bombardment. This helps to increase the etch rate and achieve the anisotropic etch profile by breaking the strong Si-O and Si-N bonds. This is followed by a plasma resist strip (PRS) and chemical resist strip (CRS) and the expected profile is shown in figure 3.19.

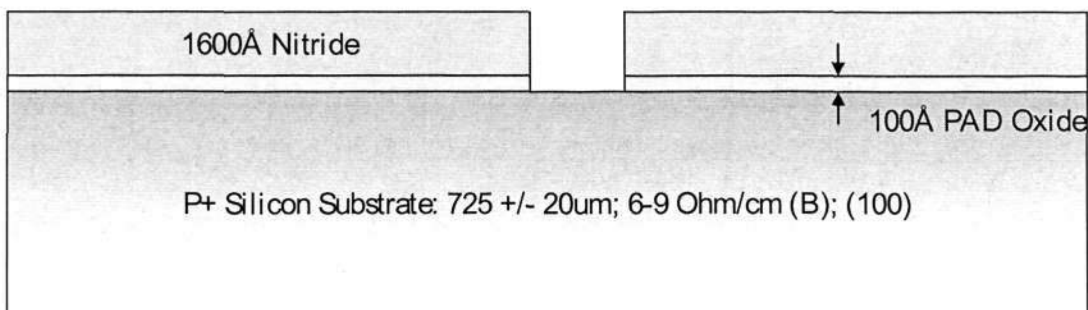

Fig. 3. 19 Active and isolation definitions.

A trench size of 4000Å Si depth is etched away to form a STI trench as illustrated in figure 3.20. HBr is used as main etchant and O_2 as the side wall passivation agent. In plasma, HBr dissociates and releases free bromine radicals, which can react with silicon to form volatile silicon tetrabromide ($SiBr_4$). The main chemical reaction of the single crystal silicon plasma etching process is:

$$HBr \xrightarrow{Plasma} H + Br$$

$$Br + Si \xrightarrow{Plasma} SiBr_4 \quad 3\text{-}7$$

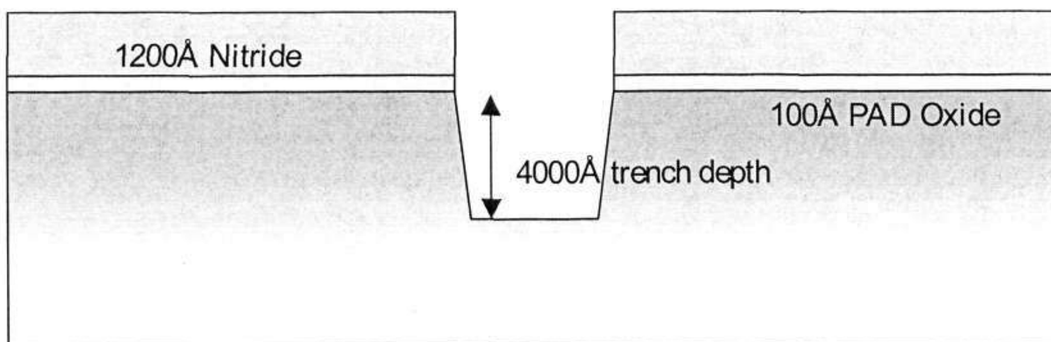

Fig. 3. 20 STI trench formation

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Around 150Å of silicon dioxide is used as barrier layer to prevent contamination of silicon substrate before trench fill in the STI process as indicated in figure 3.21. The trench is filled by High Density Plasma (HDP) CVD process. Since the HDPCVD process always brings small amounts of impurities, a dense, thermally grown silicon oxide barrier layer is necessary to block possible contamination. Afterwhich, HDP TEOS is used to deposit the oxide thickness of 6200Å in an AMAT Ultima X machine. HDP densification is performed at 1000^0C prior to the CMP step.

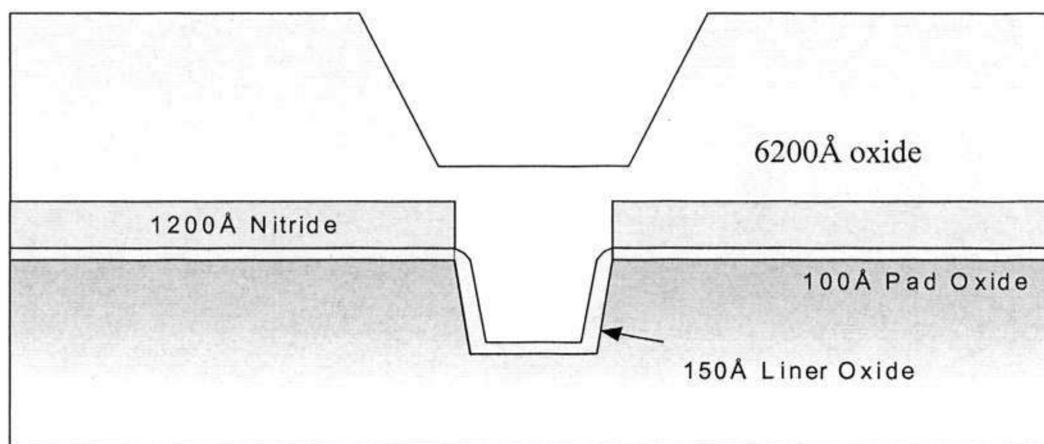

Fig. 3. 21 STI depositions.

3.5 Results

Two different schemes of the STI CMP process namely reverse mask scheme and direct polish scheme were investigated. Performances of the ceria-based slurry were characterized and reported in detail on many aspects, from NUWIW to the electrical performance of the transistors. Properties and solid concentration controlled of ceria based slurry is presented first, followed by results of blanket wafer polishing and particle contamination and finally NUWIW, NUWID, erosion, dishing, roughness, metal contamination and electrical performances of transistors for patterned wafers with 90nm device test chip masks are reported. Table 3.6 below summaries the test results for the abrasives and additives from Hitachi Chemical Co., Ltd. [72, 73].

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Table 3. 6 Properties of ceria abrasive and additive.

	Parameter	Test Condition	Unit	Properties
Ceria abrasive	Weight content	150^{0}C / 1hr	%	5 ± 0.2
	Specific gravity	25°C	-	1.04 ± 0.07
	Viscosity	25°C	mPa.s	0.94 ± 0.08
	pH	25°C	-	8.0-8.7
	Particle size	-	μm	0.22 ± 0.05
Additive	Weight content	150^{0}C / 1.5hr	%	3.2 ± 0.1
	Specify gravity	25°C	-	1.01 ± 0.01
	Viscosity	25°C	mPa.s	1.51 ± 0.08
	pH	25°C	-	6.4-6.8

Unlike ready-to-use slurries, the ceria based slurry used in this experiment consists of three components namely abrasive, additive and DI water. Before the abrasive is ready to be supplied to MIPSS, the abrasive concentration needs to be examined. Thus, the optimal time for blending to achieve 5 +/- 0.2% solid concentration of abrasive (ceria) is first determined.

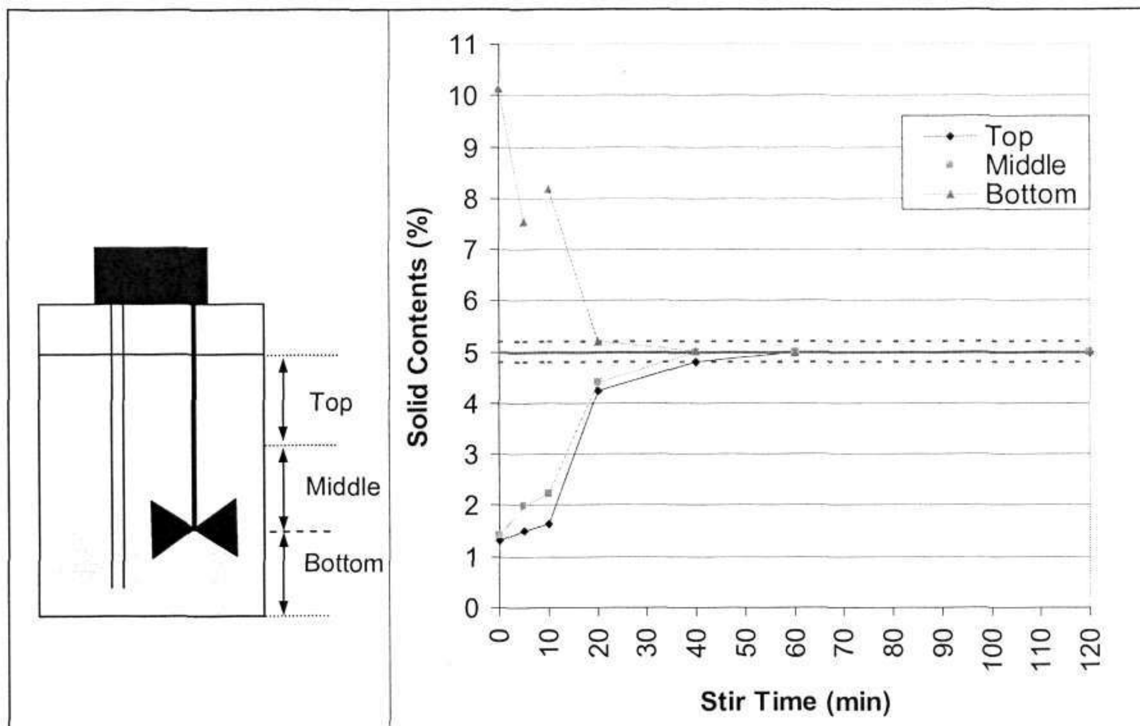

Fig. 3. 22 Solid concentration vs stirring time.

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From figure 3.22, the ceria abrasive concentration is evenly distributed in the range of 4.8% to 5.2% at around 40 min stirring time at 1500rpm. It is expected that the bottom concentration will be high at initial state and low at the top volume due to settling of the abrasive. Blending is not as simple as it seems at first glance. Factors such as flow rate, diameter of the pipe, blades design etc. should also be considered however, these are beyond the scope of this report.

After 40 minutes of blending, the abrasive is then drawn by the MIPSS to mix with DI water in the specific mixing ratio and the results are summarised in table 3.7.

Table 3. 7 Mixing ratio test result

Label	Description	Solid Contents (%wt)
Incoming, top	From abrasive bottle	4.871
Incoming, Middle	From abrasive bottle	5.045
Incoming, Bottom	From abrasive bottle	5.050
Ratio: 1:0 (P2)	Abrasive from platen 2	4.997
Ratio: 1:0 (P3)	Abrasive from platen 3	4.970
Ratio: 1:2 (P2)	Abrasive: DI water = 1:2 from platen 2	1.680
Ratio: 1:2 (P3)	Abrasive: DI water = 1:2 from platen 3	1.685
Ratio: 1:19 (P2)	Abrasive: DI water = 1:19 from platen 2	0.267
Ratio: 1:19 (P3)	Abrasive: DI water = 1:19 from platen 2	0.270

Before any mixing ratio test was performed, the concentration of the solid content from the source (abrasive bottle) is first investigated. The average concentration value of top, middle and bottom is within the specifications i.e. 5 ± 0.2 %. The effective transportation of this solid concentration needs to be ensured and this was verified by collecting a slurry sample at the slurry arm on platens 2 and 3. Results show that 4.997% and 4.970% of the abrasive concentration is obtained from each of the respective platens is within the specification of 5 ± 0.2 % with the mixing ratio of 1:0 (purely abrasive). Abrasive and DI water was then mixed with the ratio of 1:2. The concentration target value for this mixing ratio was 1.667% ± 0.2 % (5% divide by 3). The result indicates that abrasive for both platen 2 and 3 was within this range in this mixing ratio. Similarly a mixing ratio of 1:19 was evaluated. Ideal abrasive concentration for this mixing ratio will be 0.25 ± 0.2 % (5% divide by 20). This is the abrasive concentration, which was used in this work. The mixing ratio test is used to investigate the solid concentration and a tight specification is employed to minimize the factor of abrasive concentration on the polishing performance.

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3.5.1 Blanket removal rate and non-uniformity of SiO_2 and CeO_2 slurry

Blanket wafer polishing is the first step in understanding the polishing characteristics of patterned wafers. As mentioned in the previous chapter, 16kÅ of USG on silicon was used. In blanket wafers, two parameters are the major factors to be considered. First, removal rate in terms of Å/min, which should not be very high as this may result in difficulty to control and not too slow as it will increase the cycle time. Secondly, non-uniformity should be as low as possible to achieve better planarity performance. Before any experiment can be conducted, the blanket removal rate and non-uniformity of removal rate both need to be determined and should fall within a specified range of $\pm 3\sigma$.

3.5.1.1 Setup for platen 1 (silica based slurry)

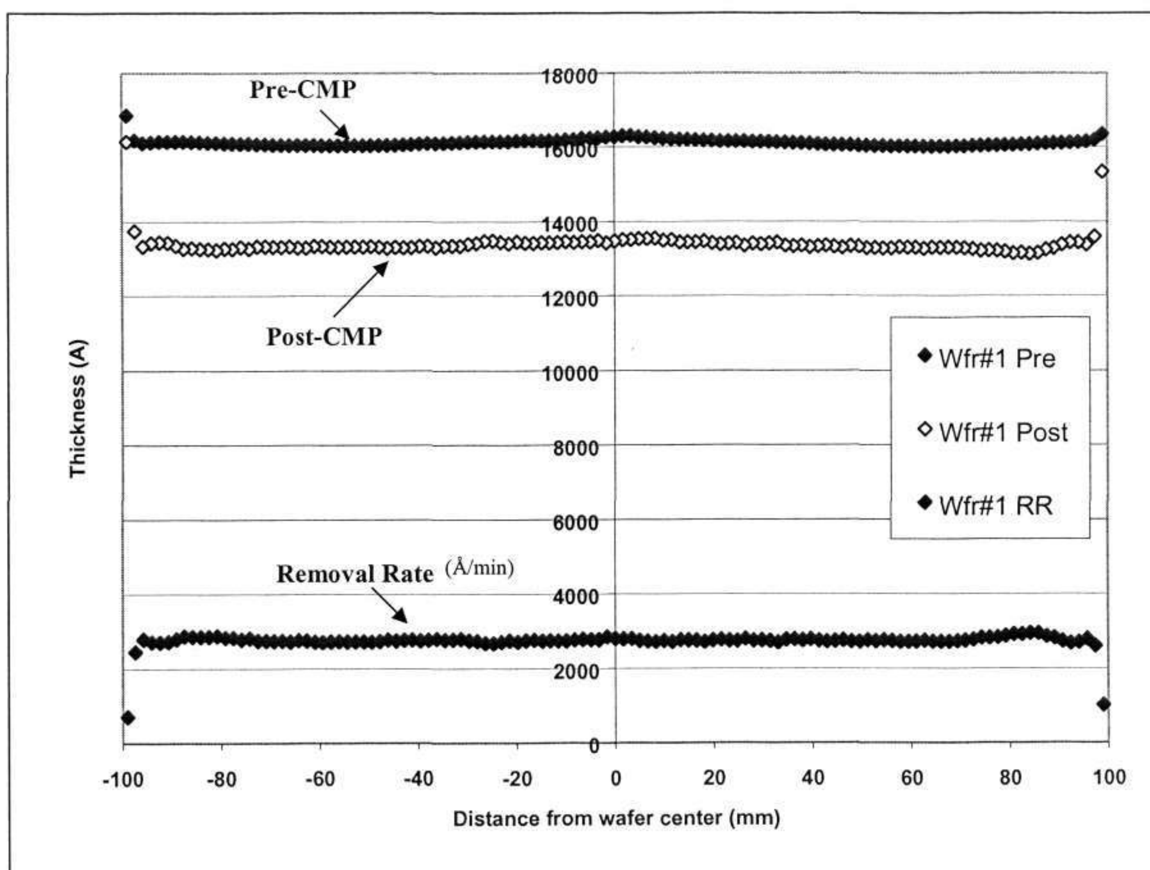

Fig. 3. 23 Diameter scan for pre, post thickness and removal rate.

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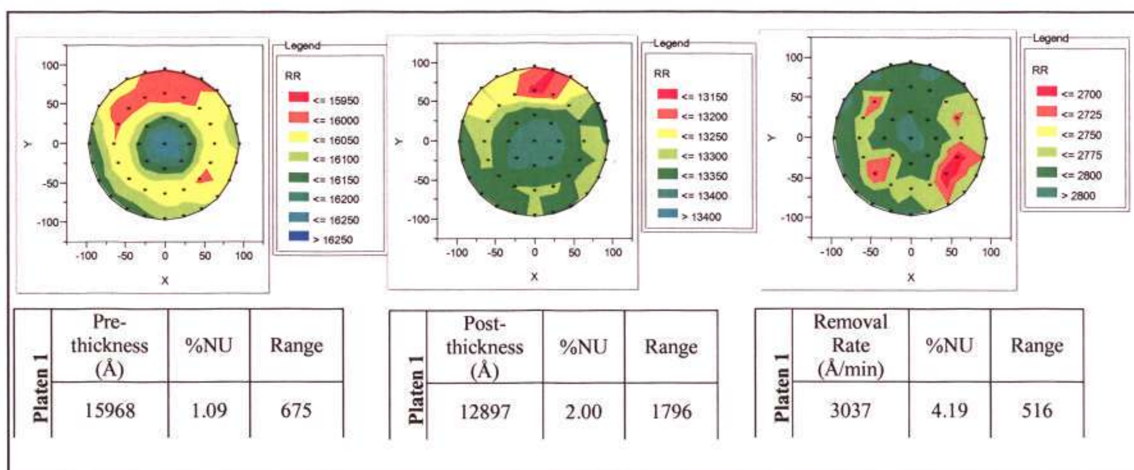
The measurement pattern will affect the results [74]. Therefore diameter scan (figure.3.23) and polar map scan (figure.3.24) were taken in order to obtain more information. Fewer points are taken for the diameter scan at the edge to represent thickness or removal rate at largest perimeter and is therefore less accurate as compared to the polar map scan. However, if the carrier design is not able to eliminate the edge effects then the polar map might capture misleading results. On the other hand, less data points are obtained for the polar map at the center as compared to the diameter scan and thus the polar map is less effective in representing the center portion of the wafer from a statistic point of view. Hence, two different pattern measurements are necessary to reveal the thickness and removal rate. After one minute of polishing on platen 1, a 121 points diameter scans result shows that with silica based slurry and the optimized recipe (refer to figure 3.23) the removal rate was around 2976Å/min with a non-uniformity of less than 3.96%. The polar map results are shown in the figure 3.24. Removal rate was around 3037Å/min with non-uniformity of 4.19%. Both measurements indicate that removal rate was around 3000Å/min and non-uniformity is less than 5 %.



	Pre-thickness (Å)	%NU	Range
Platen 1	15968	1.09	675

	Post-thickness (Å)	%NU	Range
Platen 1	12897	2.00	1796

	Removal Rate (Å/min)	%NU	Range
Platen 1	3037	4.19	516

Fig. 3. 24 Polar map-49pts scan.

After achieving the optimal removal rate and non-uniformity by tuning the process parameters, the next step was to perform a marathon run to investigate the stability of the process. Marathon run result shows that the mean removal rate was 2750Å/min and non-uniformity was kept below 5% (figure 3.25).

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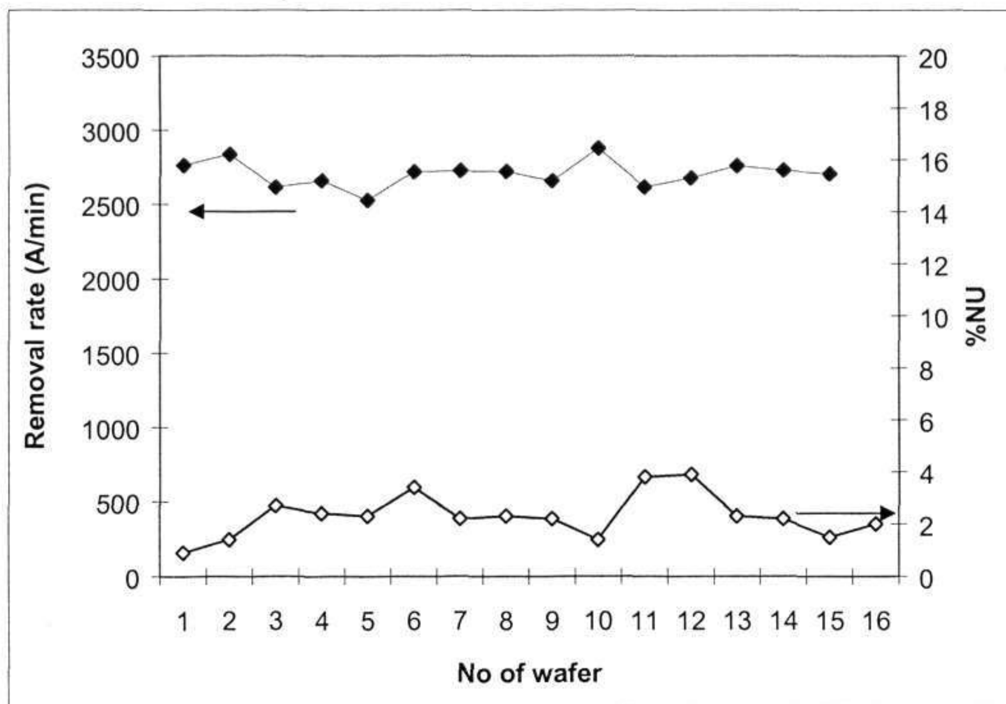

Fig. 3. 25 Removal rate vs no of wafer.

3.5.1.2 Setup for platen 2/3 (ceria based slurry)

The removal rate of ceria based slurry in platen 2 and 3 are shown in figure 3.26 and figure 3.27. Low removal rate and high non-uniformity are obtained. Removal rate for both platens were around 550Å and non-uniformity as high as 50% was observed. This is believed to be mainly due to the effect of polycarboxylate additive in the slurry. Additives that wraparound the abrasive will also prevent direct contact between the abrasives and the film surface and thus reduce the removal rate. Since there is an intrinsic surface charge on the oxide surface at any pH value, it is believed that the root cause of the non-uniform removal rate is due to the non-uniform distribution of the anion polymer additives on the oxide surface. Polar map (figure 3.27) indicates that the edge removal rate was faster than at the center. Similarly, this trend is also reflected in the diameter scan. Similar to platen 1, a marathon run was performed, the results are shown in figure 3.28. The mean removal rate for platen 2 and 3 were 543Å and 527Å respectively with an average non-uniformity of 27% and 22% each.

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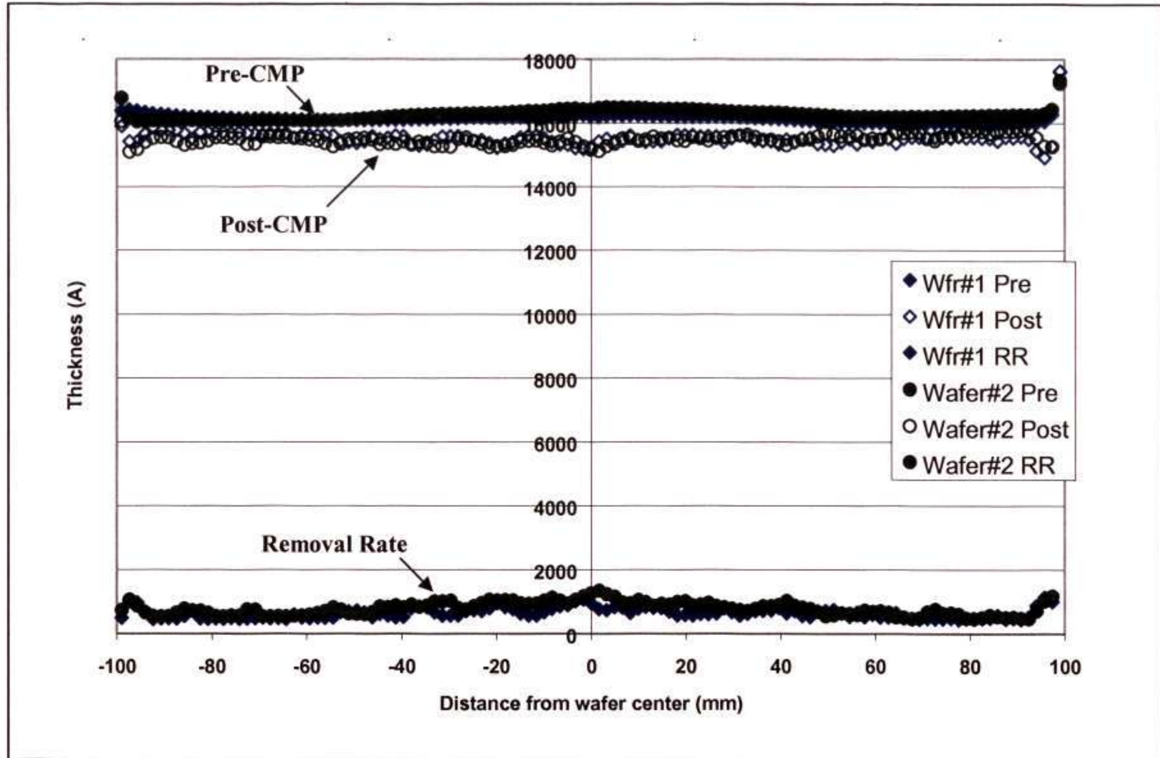
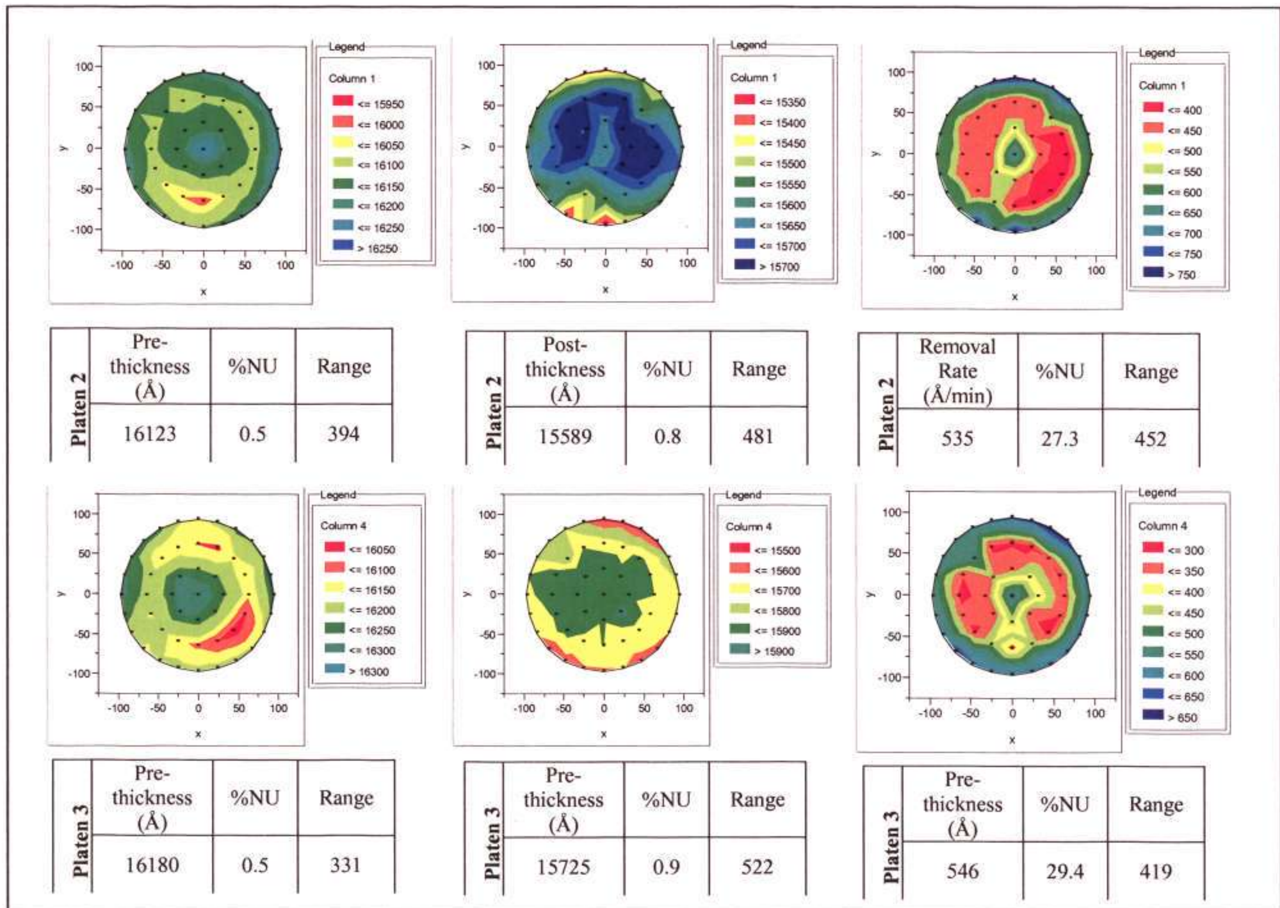


Fig. 3. 26 Diameter scan for pre, post thickness and removal rate for platen 2/3.



	Pre-thickness (Å)	%NU	Range
Platen 2	16123	0.5	394

	Post-thickness (Å)	%NU	Range
Platen 2	15589	0.8	481

	Removal Rate (Å/min)	%NU	Range
Platen 2	535	27.3	452

	Pre-thickness (Å)	%NU	Range
Platen 3	16180	0.5	331

	Pre-thickness (Å)	%NU	Range
Platen 3	15725	0.9	522

	Pre-thickness (Å)	%NU	Range
Platen 3	546	29.4	419

Fig. 3. 27 Polar map-49pts scan for platen 2/3.

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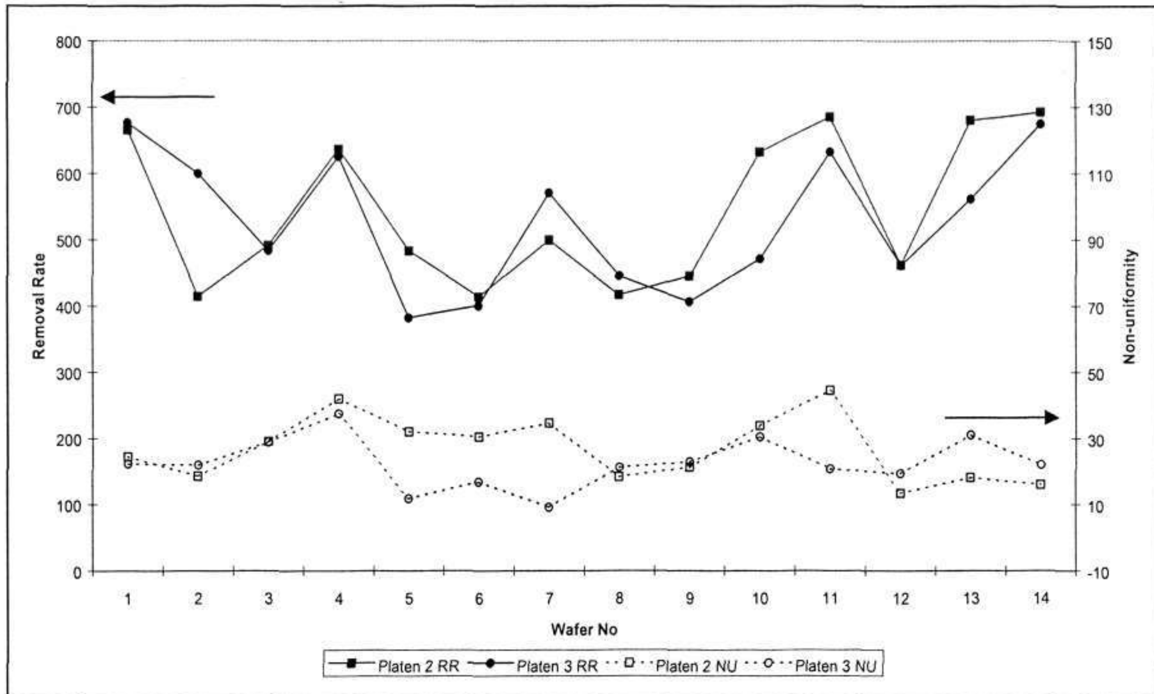

Fig. 3. 28 Removal rate vs no of wafer for platen 2/3.

3.5.1.3 Discussion

Planarity is a local, microscopic term, which is defined as:

$$Planarity = (1 - SHR) \times 100\% \qquad \textbf{3-8}$$

where SHR is step height ratio and defined as :

$$SHR = \frac{Final\ step\ height}{Initial\ step\ height} \qquad \textbf{3-9}$$

This concept of the relationship between the thickness polished and the remaining step height can be understood from figure 3.29.

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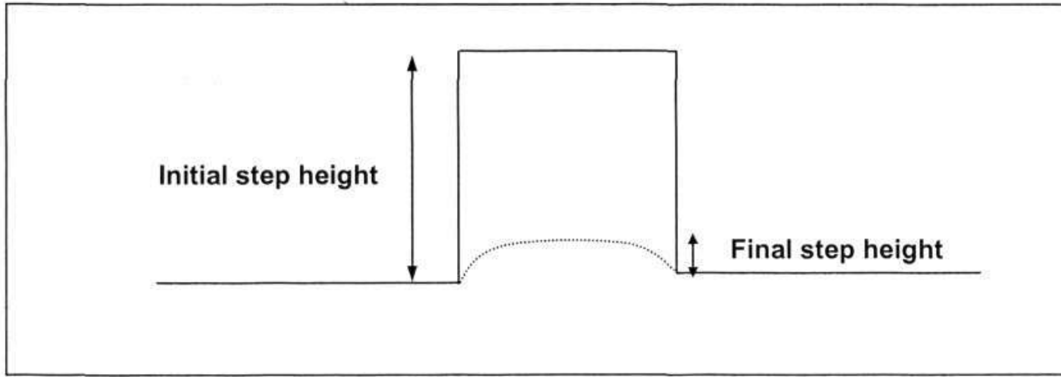

Fig. 3. 29 Step height ratio

Planarity can vary from one pattern feature to another. On the other hand, non-uniformity is a global, macroscopic term, which is described as:

$$Non-uniformity = \frac{\sigma}{\bar{y}} \times 100\% \qquad \text{3- 10}$$

where

$$\bar{y} = \frac{\sum y}{N} \qquad \text{3- 11}$$

$$\sigma = \sqrt{\frac{\sum (y-\bar{y})^2}{N}} \qquad \text{3- 12}$$

where y is a single measured value of thickness and N is the total number of the measurements performed across a wafer [75]. Non-uniformity indicates the thickness variation across a wafer. Due to there being no direct mathematical relationship between planarity and non-uniformity, it is possible that the planarity is 100% (meaning SHR=0) for some features, while the final thickness non-uniformity can be very high.

Three different thickness specifications namely, pre- and post-thickness and thickness delta are used. Normally, non-uniformity of delta thickness is used to indicate the CMP tool performance and daily qualifications. Figure 3.30 shows a blanket wafer pre- and post-thickness and as well as the delta thickness. PECVD is able to produce a

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perfectly flat oxide surface on top of un-patterned substrate (silicon) with incoming thickness of 16,000Å.

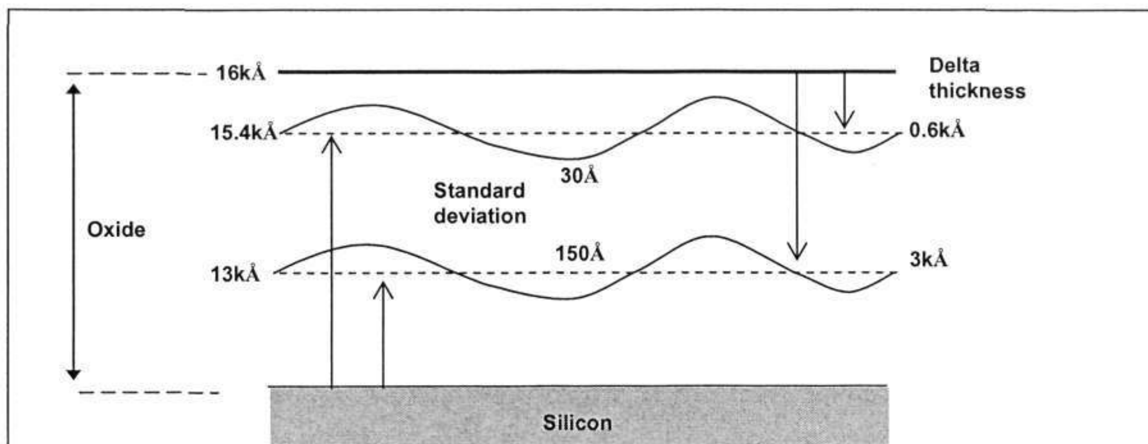

Fig. 3. 30 Delta and post thickness across a wafer.

In general, post thickness standard deviation increases with more thickness is removed. If 15,400Å remains after CMP, 600Å is removed and standard deviation of 30Å of post thickness, then post thickness non-uniformity is 30Å/15,400Å = 0.19%. However delta thickness non-uniformity is 30Å/600Å = 5%. This 5% non-uniformity indicates the CMP tool capability. If more thickness is removed, for instance, 3000Å and thus 13,000Å remains after CMP, then the standard deviation on the final thickness will be 5% x 3000Å = 150Å rather than 30Å. This causes the final thickness non-uniformity to change from 0.19% to 1.15% (150Å/13,000Å). Similarly, if this tool with 5% non-uniformity capability is used to polish 6000Å and therefore 10,000Å thickness remains then the final thickness non-uniformity will be 3%.

CMP tool capability is strongly dependent on the consumables especially the slurry. This is reflected in the results presented in the previous sections. Non-uniformity for platen 1 using silica based slurry is around 4%. The amount of thickness removed was around 3000Å and non-uniformity post thickness was 2%. However this capability value is not shown in platen 2 and 3. If, based on 4% delta non-uniformity value, the non-uniformity of post thickness value for removal amount of 600Å should be around 0.15% (4% x 600/15,400). But, results of non-uniformity post-thickness for platen 2 and 3 were in the range of 0.8-0.9% are far from the value of 0.15%. The delta non-uniformity (tool capability) for platen 2 and 3 which using ceria based slurry is around

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30% as indicated in the figure 3.27. Even though the amount of thickness removal was small for platen 2 and 3 but non-uniformity is worse than platen 1 which removed five times the amount than platen 2 and 3. Results suggest that the CMP tool capability is strongly dependent on the type of slurry is used. Polycarboxylate is an anion polymer additive, which is used to increase the selectivity for STI polishing in the ceria based slurry. A certain amount of these additives will cover the silicon dioxide surface on the blanket wafer thus resulting in high non-uniformity.

3.5.2 Particles contaminations from SiO_2 and CeO_2 slurry

A complete CMP process sequence will end with an effective cleaning process, leaving the planarized surface contamination and defect free for the next step in the IC fabrication. The more obvious and understandable issue concerns the very high level of residual particles left by CMP. These particles essentially originate from the used slurries (SiO_2 and CeO_2) but also from the polished surface materials and to a lesser extent from the polishing equipment environment. These particles can physically adsorb at the surface or even in the worse case partially embed in the film due to the mechanical pressure exerted by the pad. The requirement of the particle size is scaled down with the minimum features size of the technology [76].

In this work, the same cleaning recipe (refer to table 3.4) was used to clean the wafers after polishing by either silica or ceria based slurry. Scrubber based cleaning technology, which provides a synergetic force of mechanical scrubbing and chemical action by ammonia hydroxide (NH_4OH) and DI water were employed. Cylindrical polyvinyl alcohol (figure 3.13) brushes in this study use a soft, flexible foam material that is brought into direct contact with the wafer surface. PVA material has an open structure consisting of interconnecting cells that allow the brush to be constantly flushed with DI water during wafer cleaning. PVA brushes are compatible with cleaning chemistries in the 2 to 12 pH range. NH_4OH is used to increase the pH value, which permits the brushes to remain clean, even with exposure to tens of thousands of slurry-laden wafers.

Figure 3.31 shows the particle count result examined by Surfscan SP1. Less particle count was observed for wafers polished by silica based slurry on platen 1 as compared

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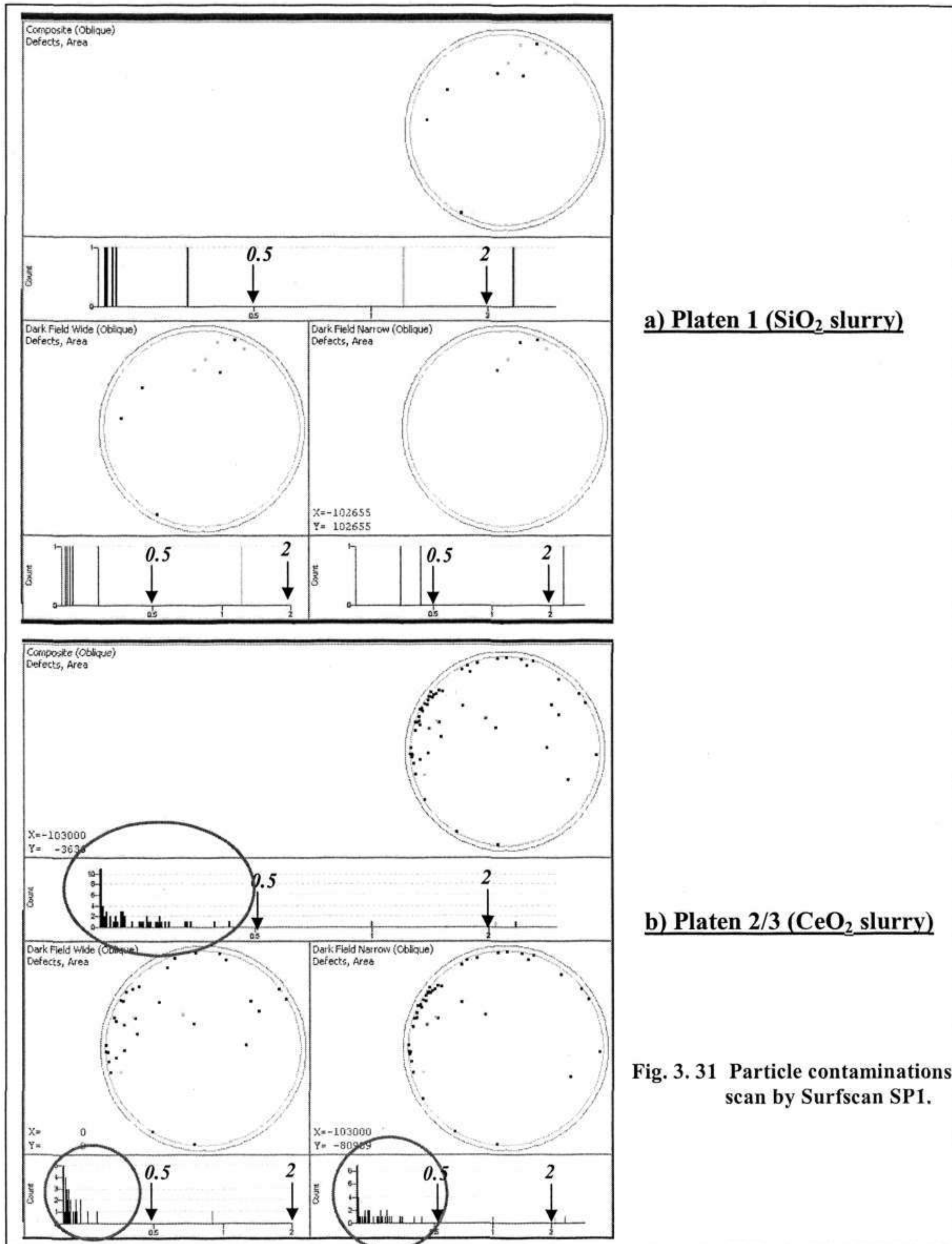
to wafers processed by ceria based slurry on platen 2 and 3. Most of the particles size were around 0.2-0.3μm. As shown in figure 3.31(b), the particles were mainly residue at the edge of the wafer especially for the wafers polished on platen 2 and 3. Nevertheless, the total amount of particles count for these three platen were less than 100 which is the general guide to evaluate the cleaning recipe based on blanket wafers.



a) Platen 1 (SiO_2 slurry)

b) Platen 2/3 (CeO_2 slurry)

Fig. 3. 31 Particle contaminations scan by Surfscan SP1.

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The characteristics of particle removal are strongly dependent on the film type and the state of the surface. The cleaning action consists of the mechanical dislodgment of particles from the wafer surface by the brush. After that, the particles stay suspended in the liquid layer above the surface of the wafer and go over the edge of the wafer to the drain as the liquid is continuously delivered to the wafer surface. However this scenario assumes that once the particle is dislodged, it never reattaches to any surface and quickly moves away within the liquid layer. Two possible events might occur, firstly, reattachment of the particles to the wafer surface and secondly attachment of the particles into the porous brushes structure so called brush loading. At first glance, all these are the particles that could not be removed by the cleaning recipe but effects such as roughness and scratches might be misdetected as particle counts. Thus, one kind of defect detection tool may not be able to tell the whole story.

3.5.3 Non-uniformity within wafer (NUWIW)

The major challenge for STI CMP is whether it is able to clear all the oxide film on top of nitride with minimal erosion and dishing. Two different schemes of the process were performed in the experiment namely direct STI CMP and STI CMP with the reverse mask as shown in the figure 3.1. RIE was used in the reverse mask schemes to etch away 4200Å of oxide for the active structures that are greater than $0.88\mu m$ prior to the CMP process. In this section the performance of these two-types of slurry are reported in terms of NUWIW for nitride film of the active structures (island) as well as trench oxide (ocean). Full map measurement was taken for both nitride and trench oxide film at PME locations (refer to figure 3.16).

3.5.3.1 Post STI-CMP: Silicon nitride NUWIW distribution

Uniformity thickness of nitride is crucial, which will determine the step height of the isolation, which in turn affects the transistor performance. As device features continue to shrink, aspect ratio is a challenge for the etch and deposition process. One can help to increase the process margin by reducing the nitride thickness (aspect ratio reduced). However, this solution relies on how well is the CMP process in controlling the uniformity of post thickness of nitride and the erosion.

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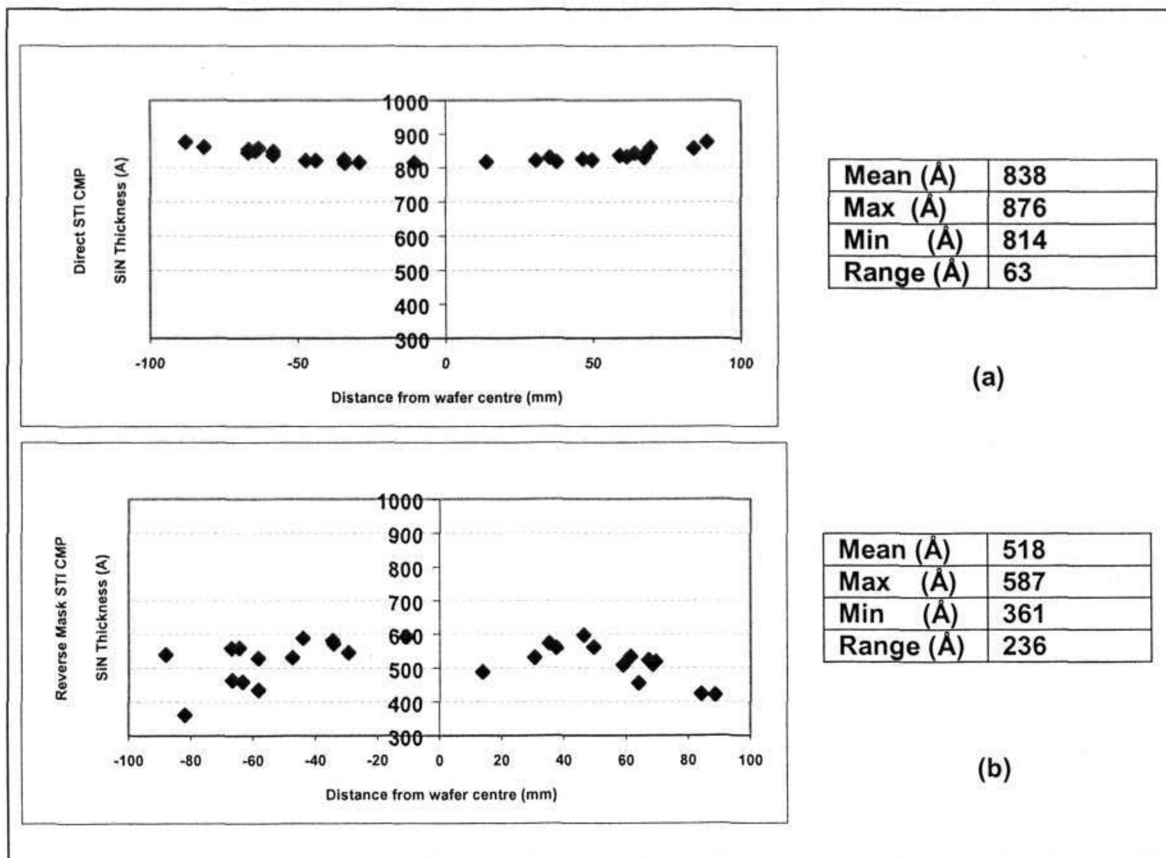

Fig. 3. 32 NUWIW of Silicon nitride for a) Direct STI CMP b) Reverse Mask CMP

Incoming nitride thickness of 850Å was deposited by LPCVD as a CMP stop layer was used by both schemes to study the impact of two different types of slurry. Figure 3.32 shows that minimum nitride loss and superior uniformity of nitride thickness (range) was demonstrated by direct STI CMP. Reverse mask process results in around a 300Å nitride loss and a range that is greater than 100Å. This results shows that ceria based slurry is able to achieve lower non-uniformity as compared to silica based slurry.

Repeatability and margin study of non-uniformity of silicon nitride thickness by direct STI CMP with ceria based slurry was performed. The study shows that ceria based slurry is able to maintain a nitride range across the wafer below 100Å (refer to figure 3.33). Beside that, even with over polishing condition the NUWIW of nitride is not affected.

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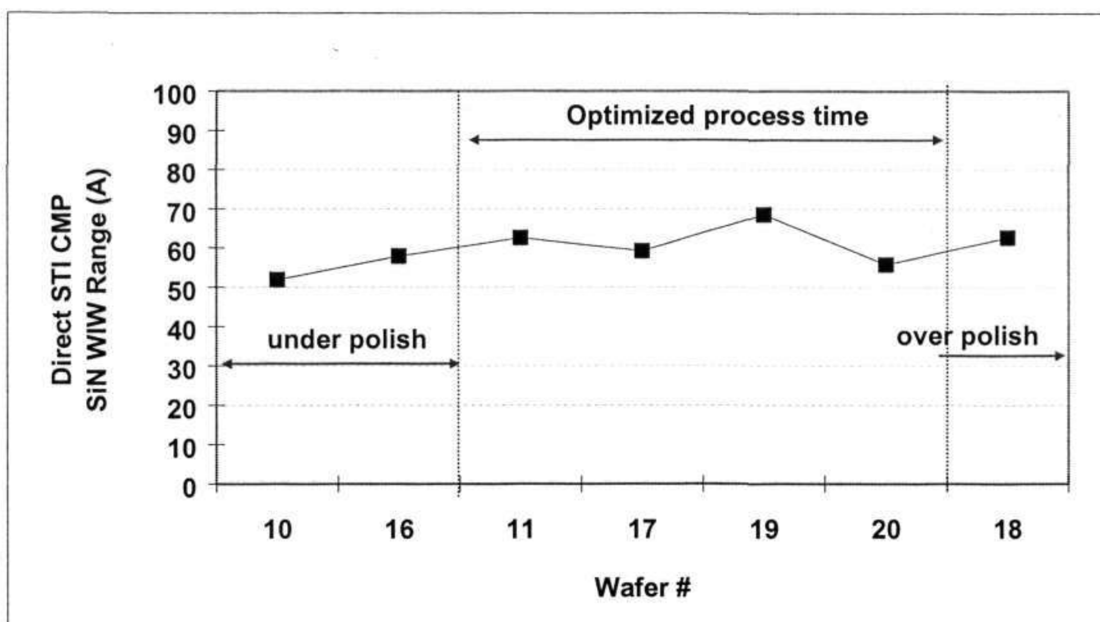

Fig. 3. 33 Repeatability and margin of NUWIW of silicon nitride.

3.5.3.2 Post STI-CMP: Trench oxide NUWIW distribution

The primary function of trench oxide is effectively isolating the active device. Uniformity of trench oxide thickness across various trench sizes and location is desired to fabricate reliable transistors. It has been reported that narrow width effect, which is caused by the STI oxide step height [64]. This emphasizes the need for uniformity of trench oxide across the wafer.

HDPCVD was used to deposit 6200Å undoped silicon dioxide with 1250Å overburden as shown in figure 3.34. This is the pattern wafer structure for direct STI CMP schemes. However, etch back was needed for reverse mask schemes to reduce the amount of oxide at the active area which is larger than 0.88μm as shown in the figure 3.1. Direct STI CMP achieved a better trench oxide non-uniformity as compared to reverse mask schemes as illustrated in figure 3.35 which shows the variation of the oxide thickness plotted against the location within the wafer. The polishing rate near the edges of the wafer is consistently faster than at the center. The range of the same oxide trench dimension (120μm) across the wafer was below 500Å by direct STI CMP schemes whereas around 600Å trench oxide range was polished by reverse mask schemes. Figure 3.36 shows the oxide trench thickness range for the repeatability and as well as under and over polish. The variation of the range even

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with the same polishing time has erratic symptoms. Nevertheless, the range of trench oxide is below 500Å by direct STI CMP schemes and the variation of the range is around 200Å between under and over polishing time.

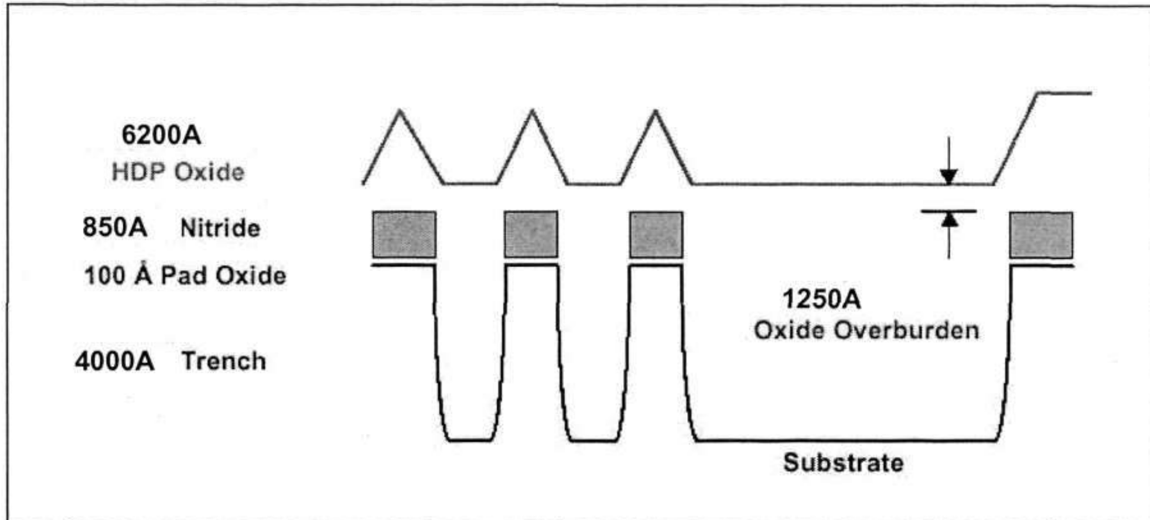
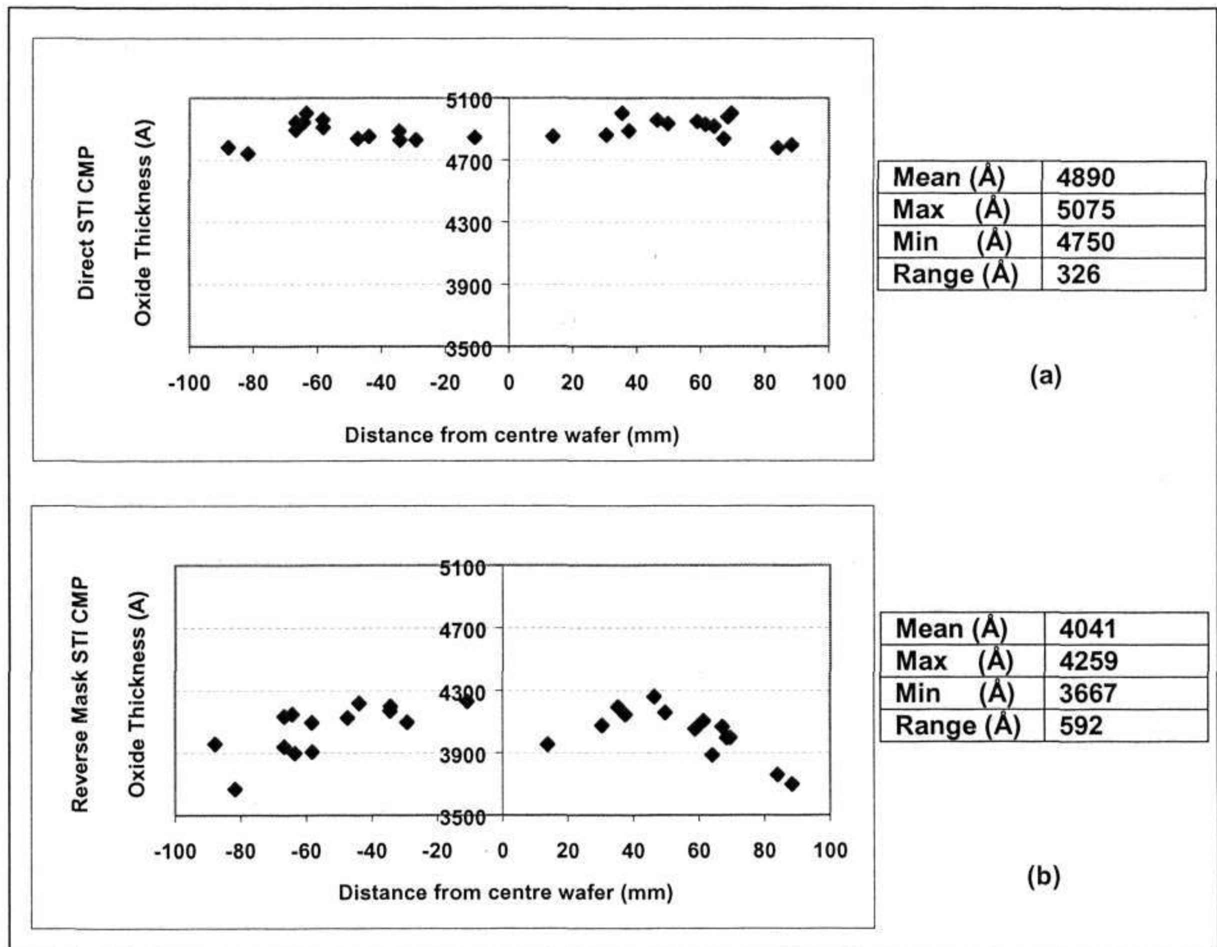


Fig. 3. 34 Incoming wafer structures.



(a)	
Mean (Å)	4890
Max (Å)	5075
Min (Å)	4750
Range (Å)	326

(b)	
Mean (Å)	4041
Max (Å)	4259
Min (Å)	3667
Range (Å)	592

Fig. 3. 35 NUWIW of trench oxide for a) Direct STI CMP b) Reverse Mask CMP.

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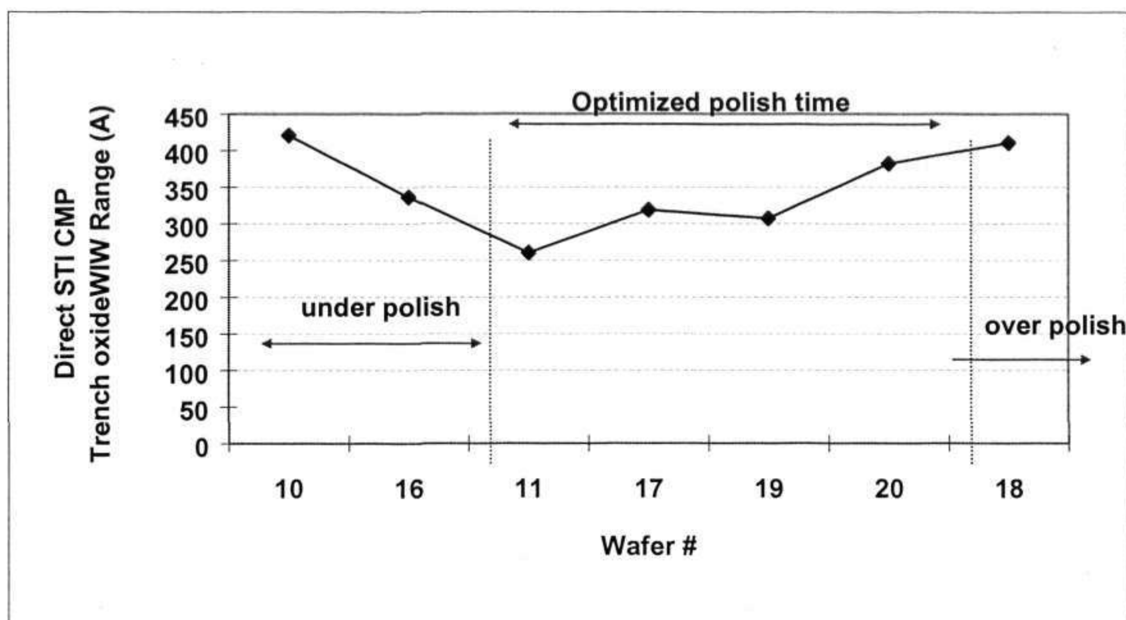

Fig. 3. 36 Repeatability and margin of NUWIW of trench oxide

3.5.4 Non-uniformity within die (NUWID)

The die level measurement captures the layout pattern dependency. In order to incorporate the wafer level variation as reported in the previous section, two die locations namely center and edge were taken since the highest range is between center and edge of the wafer. The importance of pattern density in CMP can be explained by way of an intuitive argument. The higher the pattern density, the larger the contact area with the pad, and the lower the pressure on the raised features, thus lowering the removal rate at that particular area. In other words, the removal rates at any particular point will vary inversely with the pattern density at that particular location. In short, the high regions polish slower than low density regions. For instance, normally oxide residual will be observed at the location that has a large active area the so called "big pad" (figure 3.37) while other active locations were free of oxide. The wider the pattern density range, the greater the post CMP thickness variation. Hence, a narrow pattern density ranges in the circuit layout is desired. However, it is normally very difficult or not feasible to restrict the circuit functional layout just for one particular process, therefore the only way is to improve the CMP performance to cater for a wide range of pattern density.

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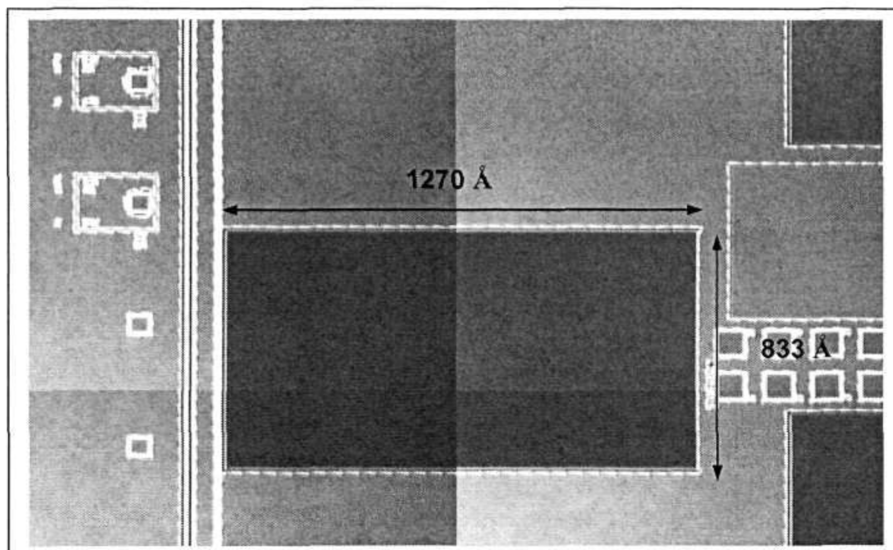

Fig. 3. 37 Big pad.

3.5.4.1 Post STI-CMP: Silicon nitride NUWID distribution

Figure 3.38 shows the die-level variation for direct and reverse mask process with optimized polishing time. Direct STI CMP with ceria based slurry demonstrated great nitride uniformity, which was below 100Å across the wide range of active dimensions. The mean nitride thickness value for reverse mask process was around 600Å with the range that is greater than 100Å. More nitride loss for the reverse mask process is due to low selectivity and thus is more sensitive to pattern density resulting in a higher range across the die. Less variation of the nitride thickness range within die for both center and edge was observed in the direct STI CMP with ceria based slurry schemes as compared to the reverse mask STI CMP with silica based slurry. Results also indicate that less nitride was lost by direct STI CMP schemes. Figure 3.39 shows the time evolution of the die level variation for direct STI CMP process. NUWID is less sensitive to the polish time and less than 100Å range of the nitride thickness across a wide number of active structure dimensions is achievable by direct STI CMP with ceria based slurry. This indicates that this kind of slurry is able to automatically stop at the nitride layer or less nitride loss even when process time increases to ensure all the oxide film is removed at the large active structures. This also implies a wider process margin in terms of polishing time. Less than 50Å variation between center and edge die was observed.

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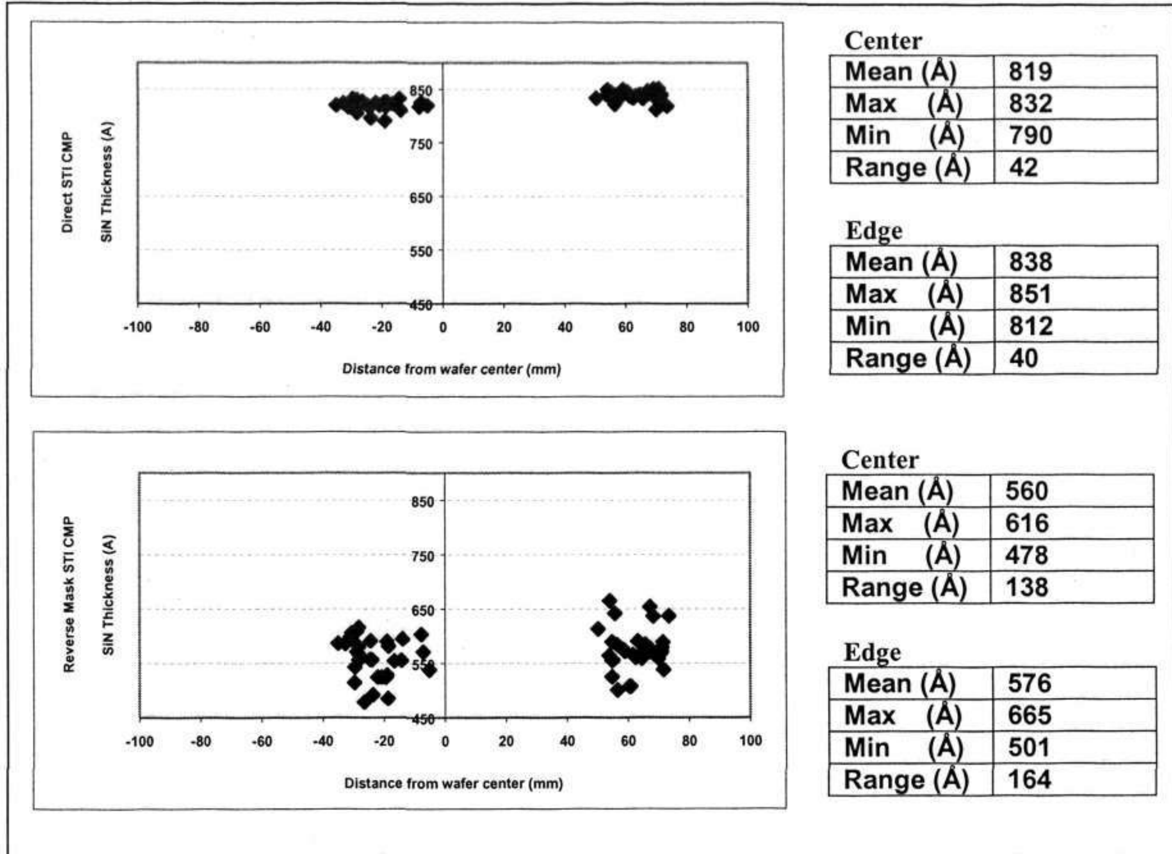

Center

Mean (Å)	819
Max (Å)	832
Min (Å)	790
Range (Å)	42

Edge

Mean (Å)	838
Max (Å)	851
Min (Å)	812
Range (Å)	40

Center

Mean (Å)	560
Max (Å)	616
Min (Å)	478
Range (Å)	138

Edge

Mean (Å)	576
Max (Å)	665
Min (Å)	501
Range (Å)	164

Fig. 3. 38 NUWID of Silicon nitride for a) Direct STI CMP b) Reverse Mask CMP.

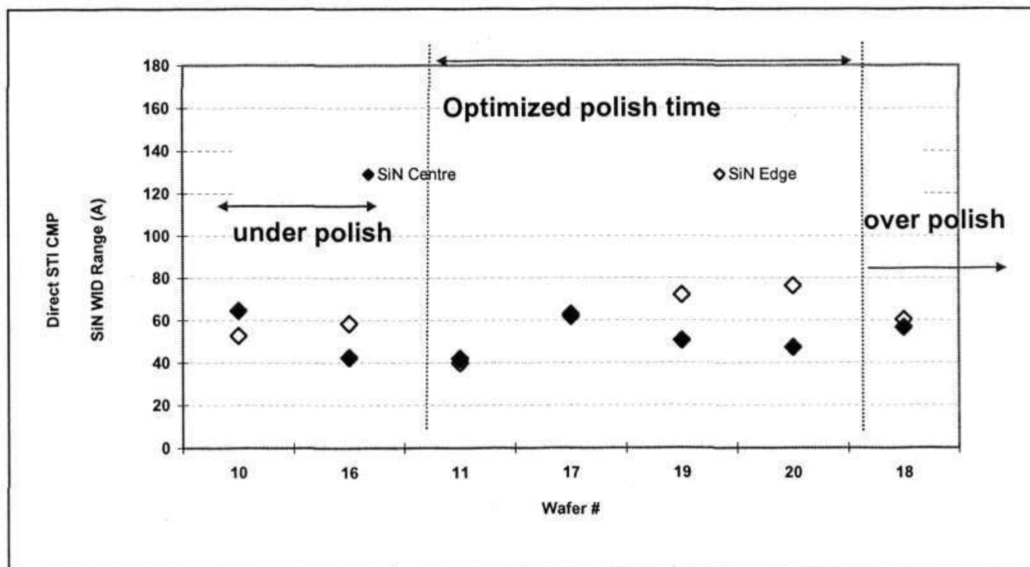

Fig. 3. 39 Repeatability and margin of NUWID of silicon nitride.

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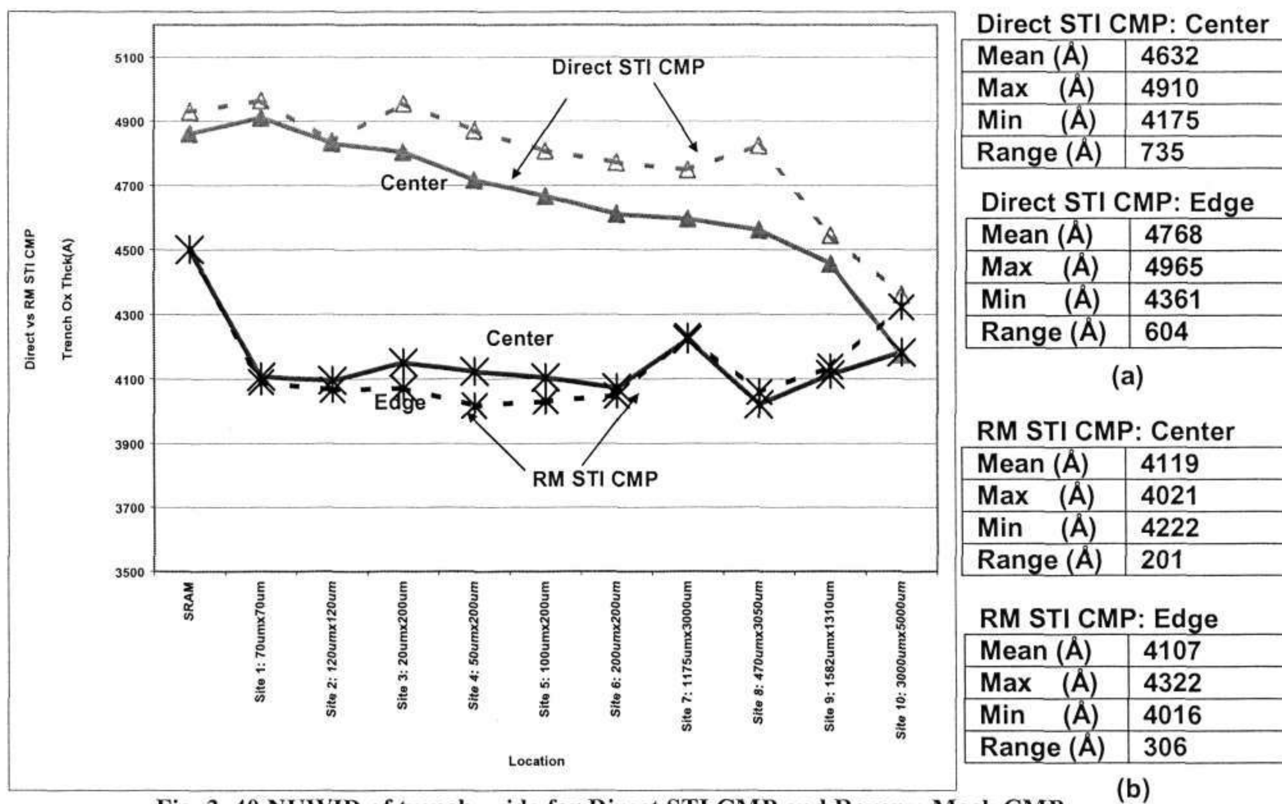
3.5.4.2 Post STI-CMP: Trench oxide NUWID distribution

Figure 3.40 shows the thickness of the trench oxide plotted as a function of trench size for both schemes of the process. Unlike NUWID for nitride thickness, trench oxide thickness within a die exhibits a large range value (around 700Å) between small and large trenches in the direct scheme as compared to the reverse mask process. As shown in the figure 3.40, the thickness of oxide decreases as trench size increases for direct STI CMP whereas it seems to reach the saturation point in the trench size from site 1 to site 10 for the reverse mask process. Oxide thickness in the direct STI CMP with ceria based slurry process is relatively to be sensitive to the dimension of the trench. As for direct STI CMP process, more oxide was removed at the center as compared to the edge die and higher oxide range value at the center die. In contrast, trench oxide at the edge die removed more than the one at the center and hence a higher value of range is at the edge die. However, the mean thickness for direct STI CMP is around 4700Å as compared to around 4100Å for reverse mask process, less oxide thickness loss occurs in the direct STI CMP relative to the reverse mask process for most of the trenches size except for the largest trench since the ideal thickness for the trench oxide thickness is 4950Å.



Direct STI CMP: Center

Mean (Å)	4632
Max (Å)	4910
Min (Å)	4175
Range (Å)	735

Direct STI CMP: Edge

Mean (Å)	4768
Max (Å)	4965
Min (Å)	4361
Range (Å)	604

RM STI CMP: Center

Mean (Å)	4119
Max (Å)	4021
Min (Å)	4222
Range (Å)	201

RM STI CMP: Edge

Mean (Å)	4107
Max (Å)	4322
Min (Å)	4016
Range (Å)	306

Fig. 3. 40 NUWID of trench oxide for Direct STI CMP and Reverse Mask CMP

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Figure 3.41 shows die level variation range for three categories of process time. Less range variation between the center and edge and within the die itself was observed in the under optimized process timing (meaning there are oxide film residuals at the large active structure). Significant variation of the range between both dies was noticed in the optimized and over polishing time. The trend is the center die having a highest range oxide thickness value as compared to the die at the edge.

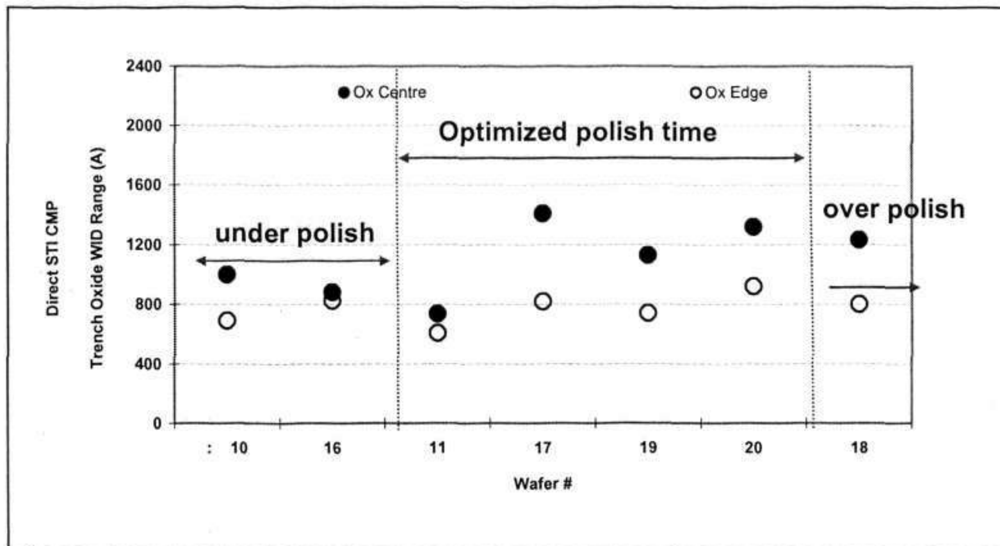

Fig. 3. 41 Repeatability and margin of NUWIW of silicon nitride

3.5.5 Silicon nitride loss

In the STI CMP process, nitride loss or erosion at a particular point is defined as the amount of nitride removed (nitride thickness before CMP process minus nitride thickness after CMP process). The goal of STI CMP is to remove all the oxide film over the dense active area and as well as the low density or isolated active area while keeping the same nitride thickness which serves as a polishing stop layer across the wafer. The nitride thickness determines the step height between the active surface and the trench oxide surface. A greater nitride thickness is required to protect the isolated structures if selectivity of the CMP process is low. This ultimately adds a burden to the etching and depositing process due to the high aspect ratio especially for advanced devices as trench dimensions get narrower. Silicon nitride loss is compared between silica based slurry (which using planarization aid by reverse mask to etch back large amount of oxide film at large active area) and ceria based slurry (direct CMP) in this

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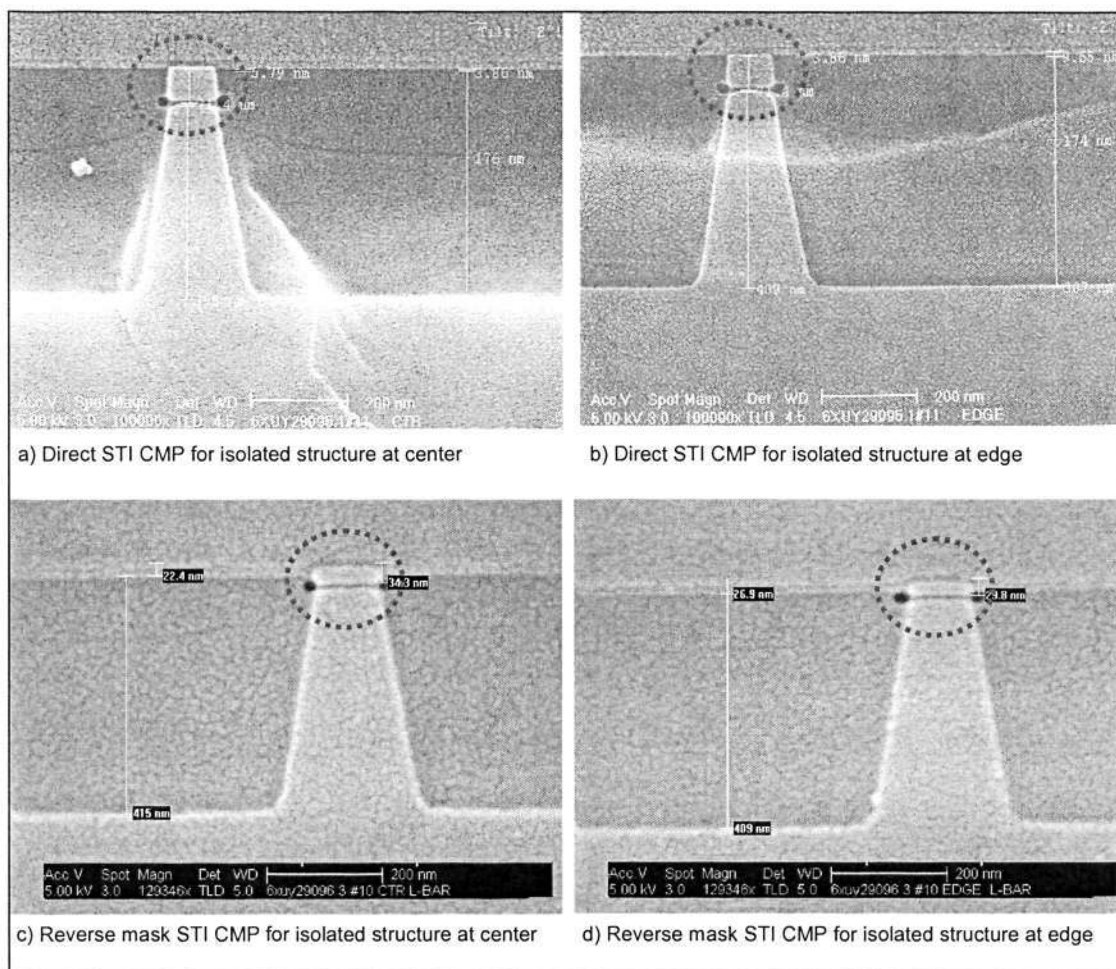
section. Figure 3.42 shows the cross section of SEM pictures for both STI CMP schemes for an isolated active structure in a patterned test wafer with 90nm device test chips. It can be clearly seen that serious erosion was observed for silica based slurry with reverse mask process as compared to ceria based slurry. Around 140Å (850Å –714Å) nitride was lost at both center and edge location for this isolated structures by direct STI CMP process. Whereas 507Å (850Å-343Å) nitride was lost at center and even serious erosion at edge with 552Å (850Å-298Å) by silica based slurry with reverse mask process. This result also indicate that more uniform post nitride thickness is achieved by direct STI CMP as compared to reverse mask and less variation of erosion was observed between center and edge for ceria based slurry process over silica based slurry. Observations agreed with the results in section 3.5.3 which indicate NUWIW is low for direct STI CMP process.



a) Direct STI CMP for isolated structure at center

b) Direct STI CMP for isolated structure at edge

c) Reverse mask STI CMP for isolated structure at center

d) Reverse mask STI CMP for isolated structure at edge

Fig. 3. 42 Erosion at isolated structures. a) Direct STI CMP for isolated structure at center b) Direct STI CMP for isolated structure at edge c) Reverse mask STI CMP for isolated structure at center d) reverse mask STI CMP for isolated structure at edge

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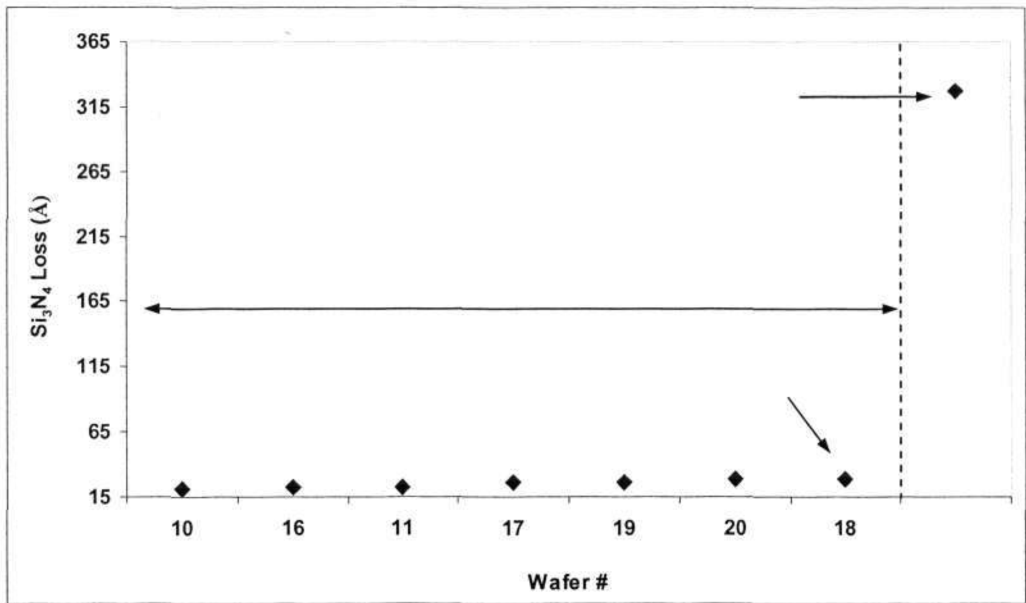

Fig. 3. 43 Si_3N_4 loss for both direct and reverse mask STI CMP

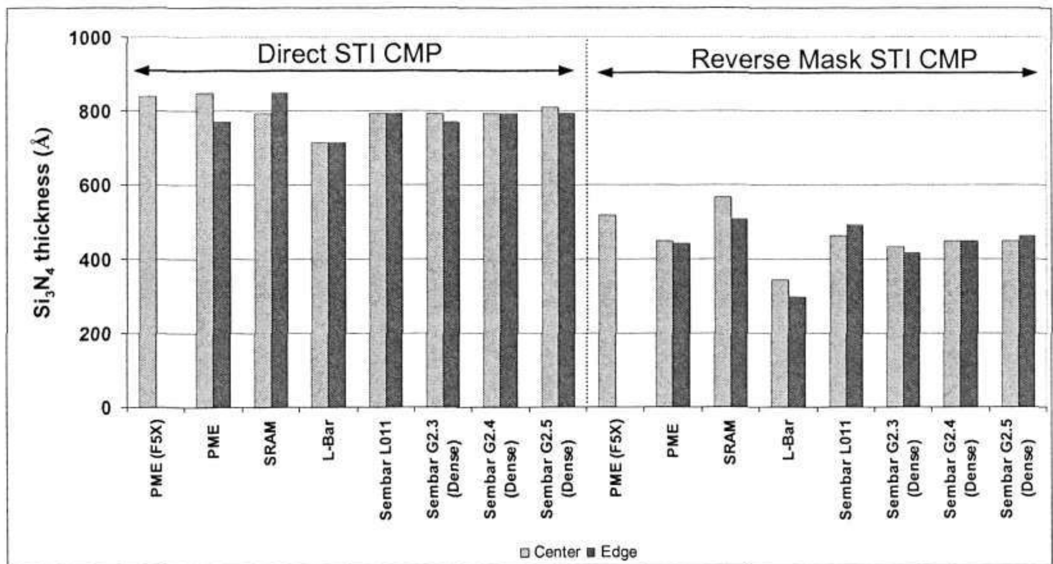

Fig. 3. 44 Si_3N_4 thickness across different active structures dimensions for both direct and reverse mask STI CMP

Figure 3.43 shows the comparison between both schemes of the process in terms of nitride loss. It is clear that direct STI CMP with ceria based slurry achieved relative low nitride loss even in the over polishing condition as compared to silica based slurry with reverse mask aid and optimized time. Nitride thickness across different active structures dimensions are shown in figure 3.44. With reference to ideal nitride thickness 850Å, direct STI CMP with ceria based slurry is able to minimize the erosion as compared to silica based slurry with reverse mask aid polishing schemes. A

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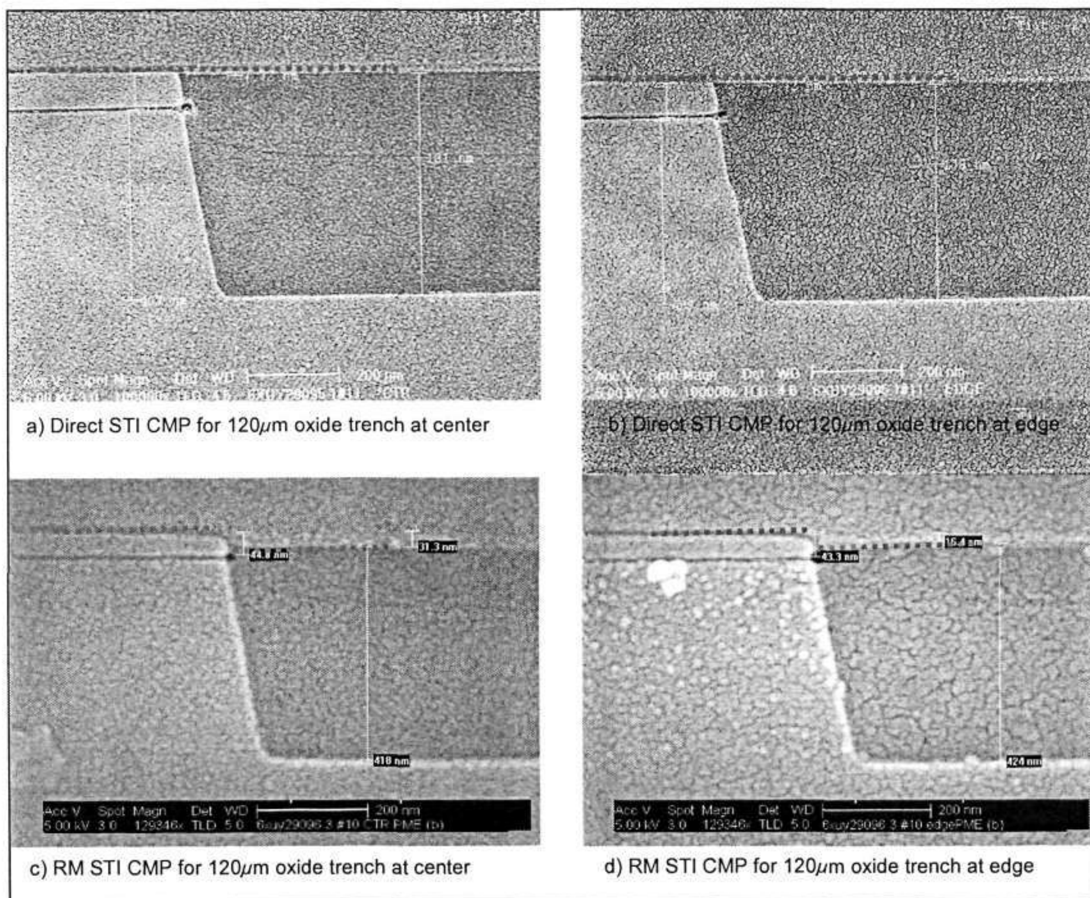
general trend which can be observed for both processes is that more nitride loss occurs at the isolated structures (L-bar) as compared to dense areas.

3.5.6 Dishing

Basically, dishing for STI CMP process is defined as the percentage of the maximum recess to the nominal depth of the filling material in trench. Dishing of the isolation oxide regions may affect implant depth and degrade planarity. Overpolish is needed to ensure all the oxide film is removed in dense or large active areas to prevent masking during the nitride striping step. However, this will cause excessive thinning especially at large exposed areas due to polishing pad elasticity.



a) Direct STI CMP for 120μm oxide trench at center
b) Direct STI CMP for 120μm oxide trench at edge
c) RM STI CMP for 120μm oxide trench at center
d) RM STI CMP for 120μm oxide trench at edge

Fig. 3. 45 Dishing at process monitoring structures. a) Direct STI CMP for 120μm oxide trench at center b) Direct STI CMP for 120μm oxide trench at edge c) Reverse mask CMP for 120μm oxide trench at center d) Reverse mask CMP for 120μm oxide trench at edge

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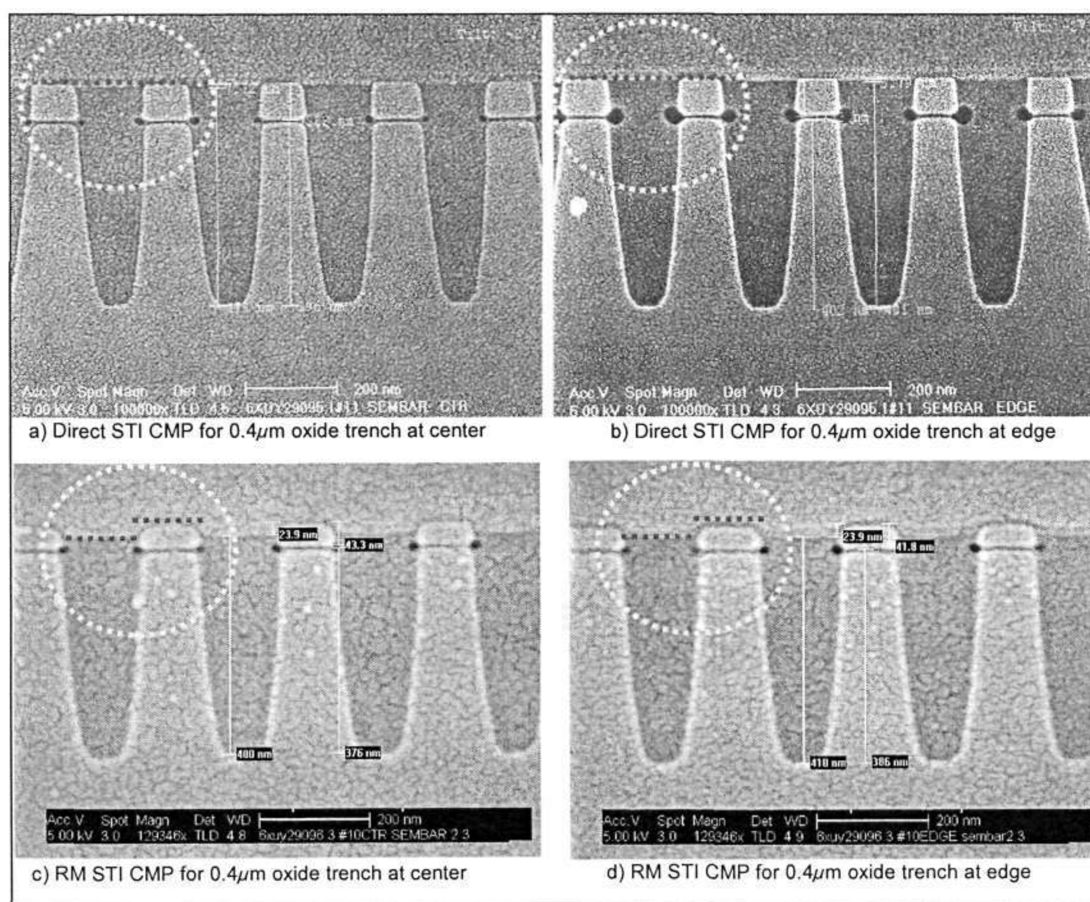
Figure 3.45 shows the cross section SEM pictures for the 120μm oxide trench after direct STI CMP and reverse mask schemes. Less dishing was observed for direct STI CMP as compared to reverse mask process as shown in the SEM pictures. Around 227Å and177Å dishing at the center and edge of the wafer for direct STI CMP with ceria based slurry whereas dishing for reverse mask process was as high as 677Å (center) and 568Å (edge). Dishing for narrow trench is shown in figure 3.46. Drastic improvement was observed in the SEM pictures for direct STI CMP over reverse mask polishing process in the trench of 0.4μm.



a) Direct STI CMP for 0.4μm oxide trench at center
b) Direct STI CMP for 0.4μm oxide trench at edge
c) RM STI CMP for 0.4μm oxide trench at center
d) RM STI CMP for 0.4μm oxide trench at edge

Fig. 3. 46 Dishing at dense structures. a) Direct STI CMP for 0.4μm oxide trench at center b) Direct STI CMP for 0.4μm oxide trench at edge c) Reverse mask CMP for 0.4μm oxide trench at center d) Reverse mask CMP for 0.4μm oxide trench at edge

The amount of dishing across the center and edge for both schemes of the process is summarised in figure 3.47 and 3.48 for respective trench sizes. The result shows that dishing is below 300Å for 120μm trench size even with over polishing time of up to 30s as compared to silica based slurry, which can vary up to around 700Å. Silica based slurry with reverse mask process is very sensitive to polishing time in wider

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trench i.e. 120μm as shown in figure 3.47. Around 200Å additional dishing was observed with only 10s over polishing time. This implies tighter process control is needed for the reverse mask process to prevent overpolishing, thus reducing dishing. As for narrow trench i.e. 0.4μm trench (figure 3.48), a drastic improvement was demonstrated by direct STI CMP schemes with less than 30Å dishing.

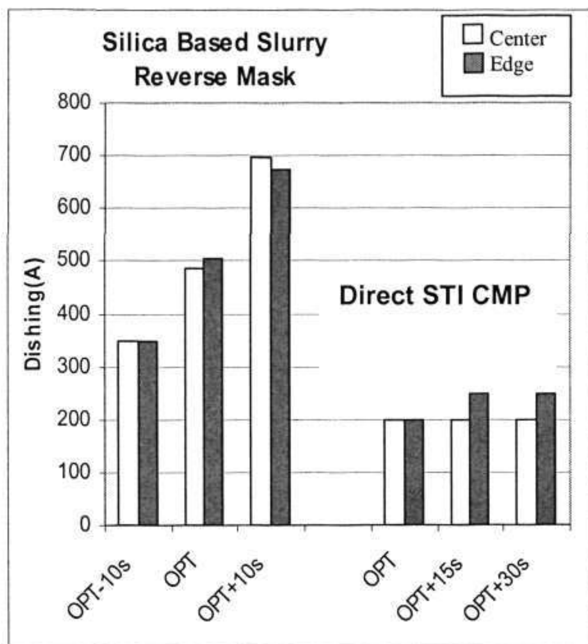

Fig. 3. 47 Dishing for Wide Trench

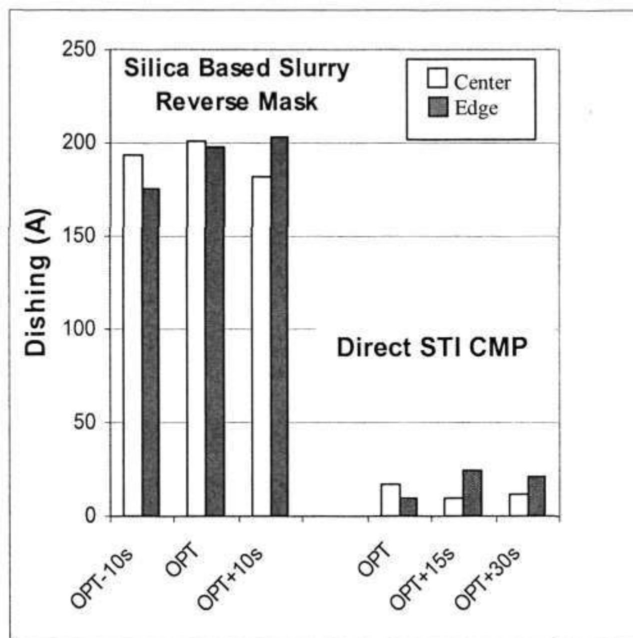

Fig. 3. 48 Dishing for Narrow Trench

3.5.7 Roughness

The rapid miniaturization of semiconductor devices has placed more exacting requirements on the CMP process. Excessive surface roughness not only can alter the device performance but also compromises the uniformity of layers deposited on top of the devices. Smaller devices require a high degree of finishing for subsequent processes for better performance. Other than improve the cleaning recipe to achieve better surface roughness, this section shows that the type of slurry can further enhance finishing.

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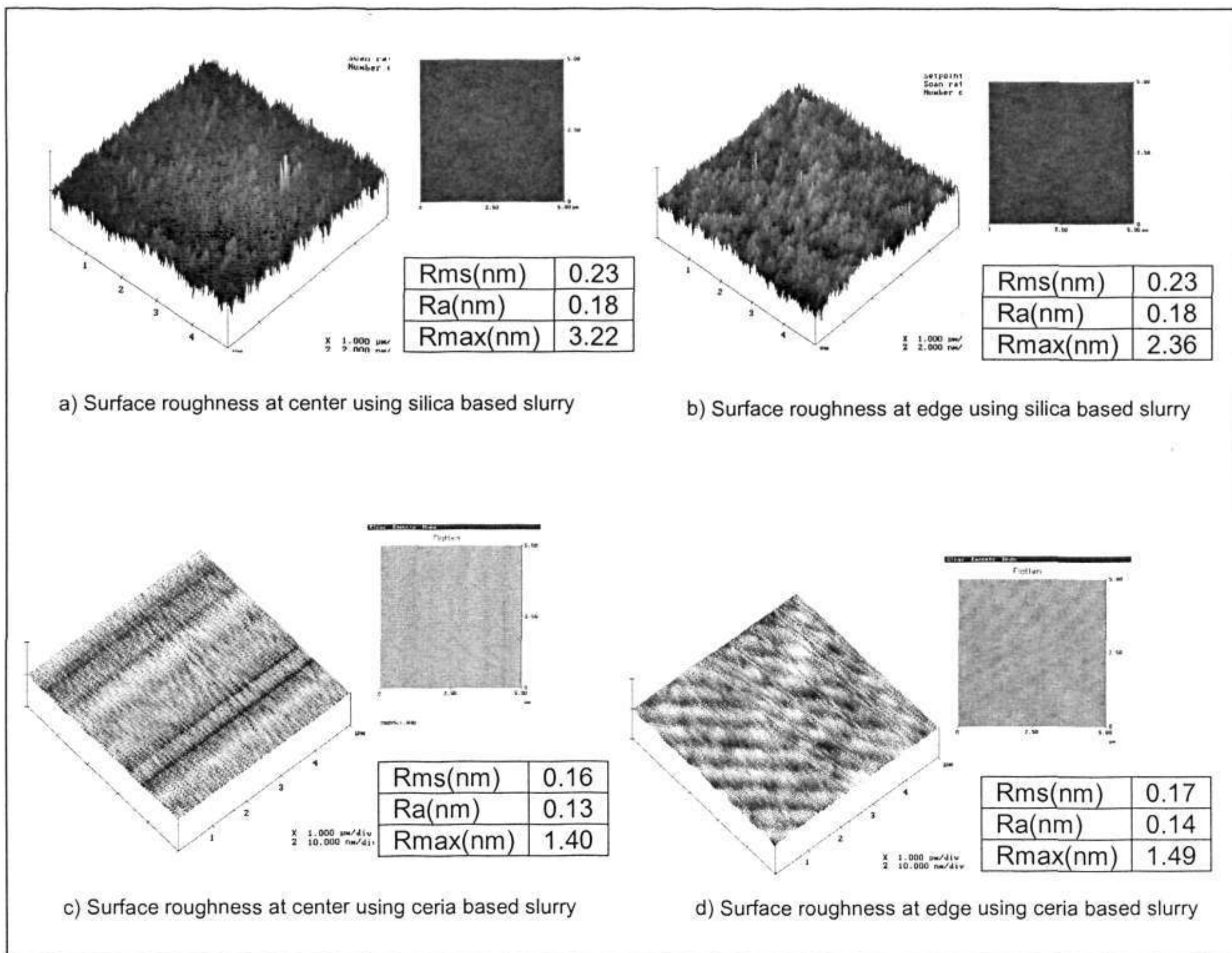

Fig. 3. 49 Surface roughness. a) Surface roughness at center using silica based slurry b) Surface roughness at edge using silica based slurry c) Surface roughness at center using ceria based slurry d) Surface roughness at edge using ceria based slurry

In figure 3.49, surface roughness of the oxide film polished by two different schemes, silica and ceria based slurry was obtained by using AFM. Since the cleaning recipe for both schemes of the process (reverse mask by silica based and direct CMP by ceria based) was the same, it can therefore be concluded that surface roughness can be further reduced by using ceria based slurry. AFM results show that the arithmetic mean roughness value (R_a) processed by silica based slurry is around 0.18nm whereas ceria based slurry can polish down to around 0.13nm. No significant variations of surface roughness were shown between center and edge of the wafer within the same process. This roughness measurement results also indicate that these was no false signal by the Surfscan SP1 (refer to appendix for metrology tool descriptions), since the roughness values were far below the threshold ($0.2\mu m$) of the particles

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measurement tool therefore no surface roughness effects which could be falsely picked up as particles.

3.5.8 Metal contaminations

The source of metal contamination could be the chemical solution from the slurry and the reactive ion etching (RIE) process. Metal contamination are prohibited especially in the FEOL process such as STI. TXRF is used in this work to investigate the improvement by direct scheme over the reverse mask scheme in terms of metal contamination since direct STI CMP replaced the need for the RIE process in the conventional process of reverse mask scheme. At the same time to study any negative effects brought by the ceria based slurry in terms of surface contamination.

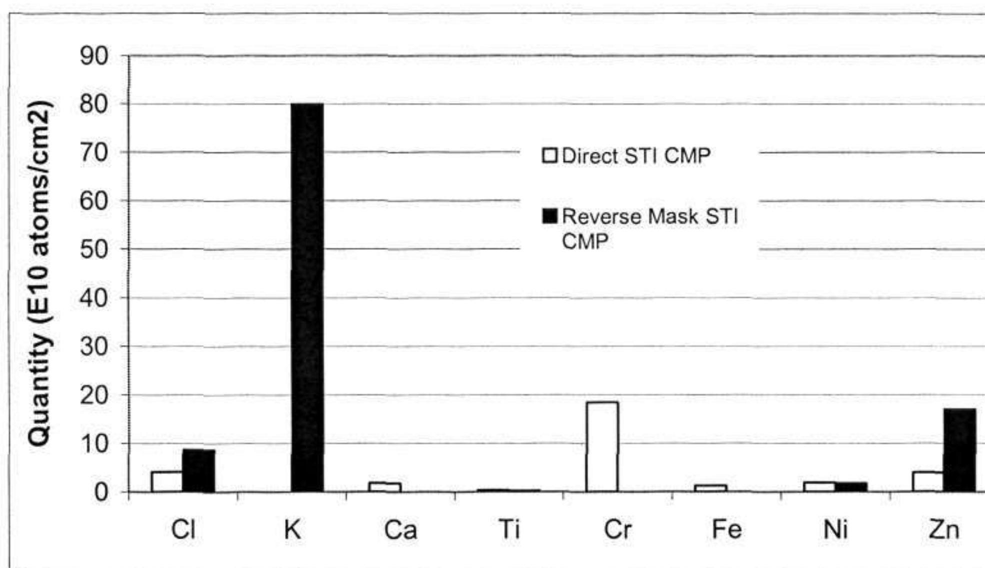

Fig. 3. 50 TXRF analysis of metal contents for post CMP wafers

Analysis from TXRF as shown in figure 3.50 indicates that less metal contamination was observed for direct STI CMP schemes as compared to the reverse mask process. Metal level is less than 20×10^{10} atoms/cm^2 after post-cleaning by using ammonia for direct STI CMP process. Skipping the RIE process for the reverse mask process also reduces the chance for additional metal contamination.

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3.5.9 Electrical test results

The excellent planarization performance with direct STI CMP process is reflected in the significant reduction in STI elevation variation from wide trench to narrow trench. With direct polish schemes, the STI elevation variation is less than 100Å between wide and narrow trench, while it (STI) elevates with 300Å at narrow trench and 100Å recesses at wide trench for reverse mask schemes process (figure 3.51).

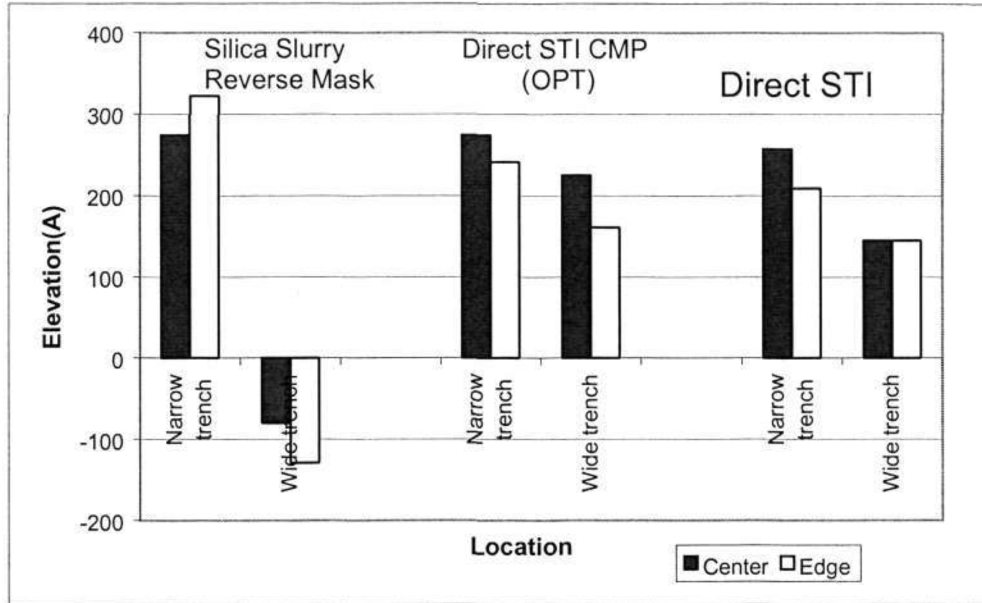

Fig. 3. 51 STI Elevation after Poly deposition

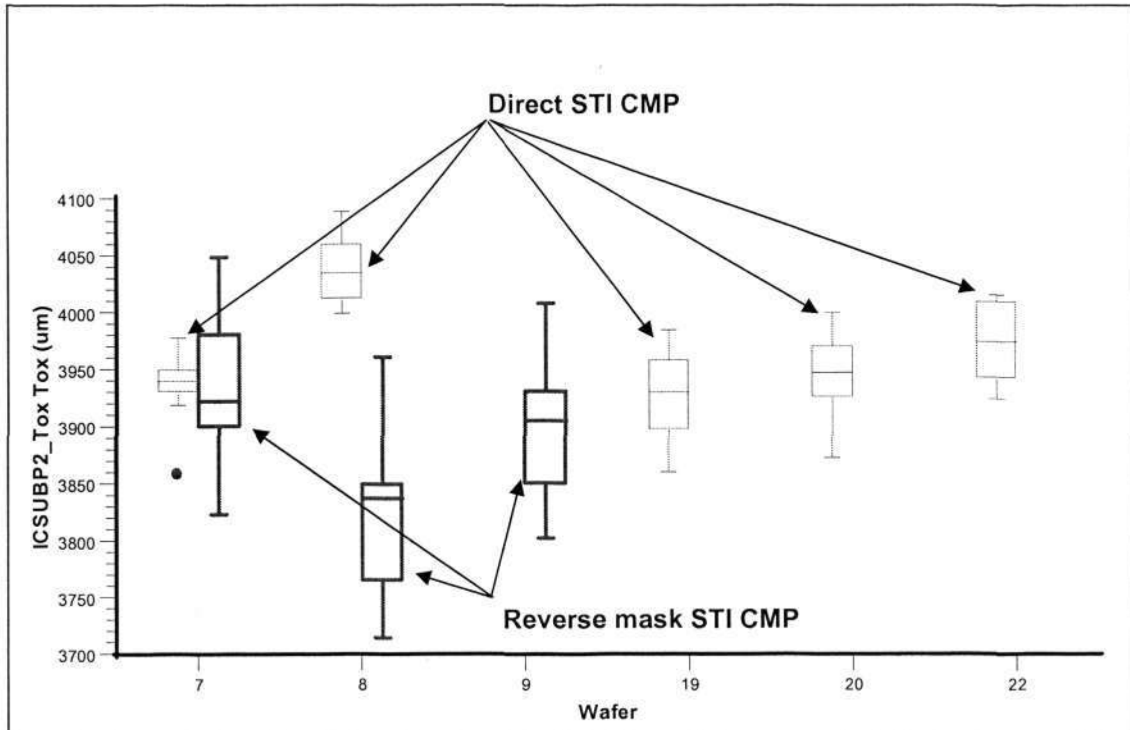

Fig. 3. 52 Electrical STI thickness and its variation for both schemes of processes

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STI thickness uniformity for both schemes of process was also verified by electrical thickness test as shown in figure 3.52. Figure 3.53 illustrates the electrical test result. Higher Vt_{lin} (threshold voltage) and Id_{sat} (drive current) and lower I_{off} (leakage current) is achieved by direct STI CMP with ceria based slurry when compared relatively to reverse mask STI CMP with silica based slurry process.

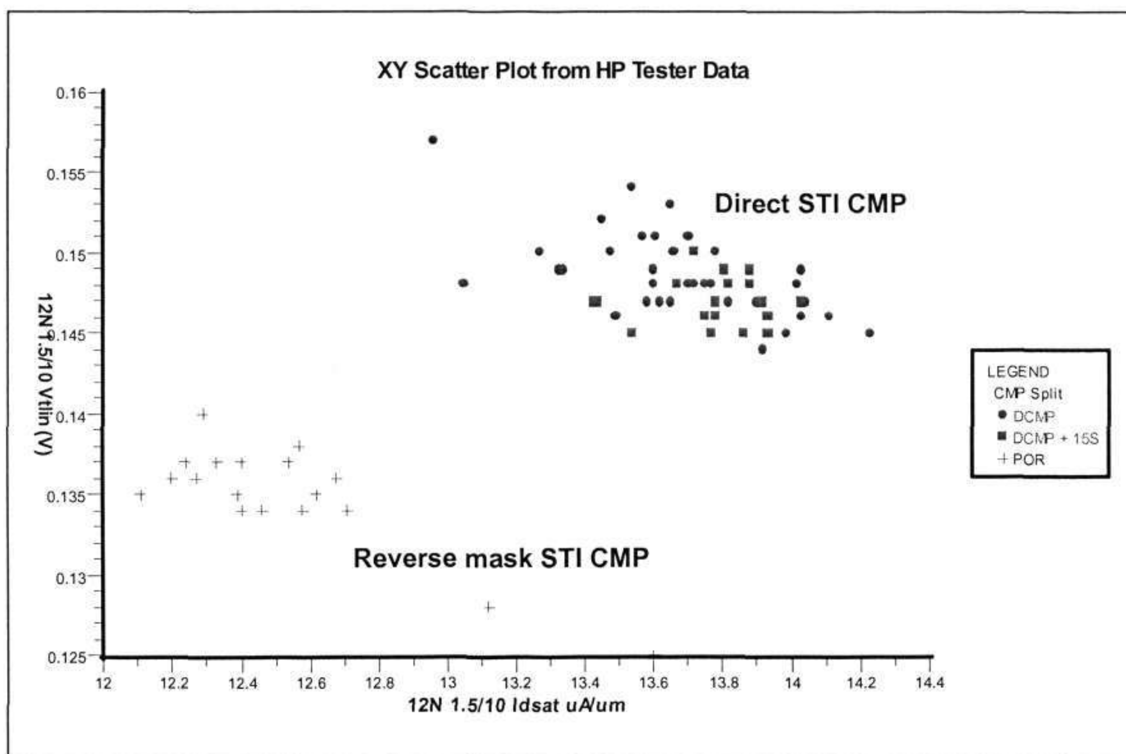

Fig. 3. 53 Vt vs Id plot for both schemes of processes.

3.6 Summary

This chapter reported the properties of ceria based slurry used in this work and followed by the investigation of both schemes of the processes namely reverse mask STI CMP with silica based slurry and direct STI CMP with ceria based slurry. Results in terms of removal rate, uniformity of removal rate across wafer and particles contamination on blanket wafers; NUWIW, NUWID, erosion, dishing, roughness, metal contaminations and electrical results on pattern wafers were presented.

The main advantages of ceria based slurry over silica-based slurry are high selectivity and high planarization capability. These make the polishing process able to achieve

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minimum nitride loss during the overpolish phase, as it is needed to ensure nitride film is clear on the active area for a wide range of pattern density while at the same time retaining good planarity over the wafer. Additive (polycarboxylate polymer) in the ceria based slurry plays a dominate role in achieving high selectivity and planarization as it is used to protect the nitride layer while at the same time wrapping the ceria abrasive at the lower point of the oxide film topography to prevent the film from being further removed. In addition, dishing is also reduced which helps to achieve a highly planarized trench surface. Due to these characteristics direct STI CMP is feasible (i.e. elimination of the reverse mask and RIE processes) using ceria based slurry even with wide range of pattern densities. The comparisons are made between silica based slurry by using reverse mask as planarization aid and direct CMP using ceria based slurry in terms of blanket removal rates and non-uniformity and NUWIW, NUWID, erosion, dishing, roughness, metal contamination and electrical for patterned wafers. Lower removal rates and high non-uniformity levels are shown by ceria based slurry in comparison with silica based slurry on blanket wafers. However, ceria based slurry demonstrates better performance over silica based slurry on pattern wafers. Lower NUWIW and NUWID for nitride thickness, less erosion and dishing for each dimension of active and trench structures, better surface finishing of the trench oxide, lower metal contamination and improved electrical performance of transistor is achieved by direct STI CMP with ceria based slurry as compared to silica based slurry with reverse mask schemes.

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CHAPTER 4

CMP PROCESS MODELING: CONTACT MECHANICS APPROACH

4.1 Introduction

As highlighted in chapter 1, selectivity and repeatability are two of the greatest challenges for the CMP process in deep submicron IC fabrication. Characterization works show that ceria based slurry can provide high selectivity between silicon dioxide and silicon nitride and thus direct STI CMP is an attractive option to replace the conventional approach in the STI CMP process (as presented in chapter 3). The issue of repeatability will be addressed in this chapter. The requirement to consistently achieve the specific target mean film thickness within a tight tolerance (± 80nm) in the IC fabrication process flow is a great challenge in order to ensure a high yield and quality. In general, except process time, all other process parameters value such as applied pressure, velocity for both carrier and platen, slurry flow rate and pad conditioning duration are kept at the constant condition in a typical process recipe so as to reduce the source of variations. These conditions are reached through experiments on blanket wafers (as demonstrated in chapter 2). However, sources of variation such as incoming wafer thickness and its variation are subject to consumable degradation and can cause a significant variation in the target mean film thickness of a patterned wafer after CMP process if the process time is not varied accordingly. This will lead to rework if the target mean film thickness of the patterned wafer is under- or over-removed and this will in turn affect the return on investment and decrease wafer production throughput. Other than the engineering decision made by operator, numerous approaches have been proposed and these include optical, electrical and acoustic as means of end point detection to obtain optimal process time however, with limited success [33]. This is due to the nature of the CMP process environment and the presence of various patterns on the wafer surface which add to the complexity of the signals. Thus, it is very difficult to integrate a robust and reliable real time measurement of film thickness into a CMP tool. Typically, ex-situ measurement of thin film thickness is required to characterize the process in IC fabrication. Thus, a methodology that offers an alternative means to predict an optimal process time with

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the aim of improving process capability is developed. Firstly, a contact mechanics approach is employed to explore the fundamental understanding of the interface between wafer surface and polyurethane pad in the CMP process. Through this approach, the knowledge is extended by developing the methodology and a potential issues for the CMP process in near future IC fabrication is highlighted in the later section of this chapter.

4.2 Polyurethane Pad Surface Characterization

Figure 4.1 illustrates the fundamentals physical problem of CMP process. With the advancement in carrier design as mentioned in chapter 2, uniform applied pressure distribution is assumed at the back side of the wafer. The corresponding force balance equation can be described as follow:

$$Load_{applied} = Load_{pad} = Load_{trench} + Load_{land} \qquad \textbf{4-1}$$

$$P_{applied} A_{apparent\,wafer} = P_{pad} A_{pad} = P_{trench} A_{trench} + P_{land} A_{land} \qquad \textbf{4-2}$$

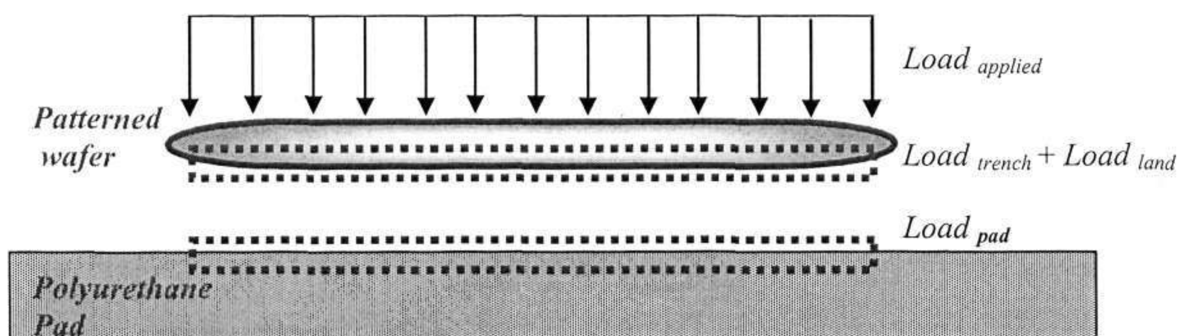

Fig. 4. 1 Schematics diagram of CMP process.

In general, $Load_{applied}$ or $P_{applied}$ is commonly employed to direct correlate the material removal rate on a blanket wafer in finding the optimal process conditions or material removal rate modeling as described in section 2.2 and 2.4. However, investigations on interface conditions $Load_{pad}$ ($P_{pad}A_{pad}$) and $Load_{trench}$ + $Load_{land}$ ($P_{trench}A_{trench}$ +$P_{land}A_{land}$) are particularly important to understand the material removal rate on patterned wafers and thus provide a better process control. Since to obtain the value of

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the P term at the interface is not straight forward and $Load_{applied}$ is a constant magnitude for a particular recipe that used in the CMP process, thus the strategy is to examine the A term at the interface, which is the real contact area between the wafer surface and polyurethane pad.

The first step in understanding the real contact area on the polyurethane pad, $A_{pad,}$ is to characterize the pad surface. In this section, surface parameters that are used in this work are introduced for completeness. Since the surface texture of a commercial CMP pad is invariant with respect to translation, a homogeneous surface is considered. Homogeneous surface can be further classified into deterministic surface and random surface. Some of the CMP modeling work [47, 77] considered the texture of CMP pad to be a deterministic surface, which has strong periodicities. However, it must be kept in mind that a deterministic surface is an ideal case and it might over simplify the problem. A typical profile of polyurethane pad and Z(x), in which profile heights are measured from a reference line is shown in figure 4.2. The mean line is defined as the line such that it divides the area between the trace profile and the mean line is equal to that below the mean line:

$$m = \frac{1}{L_x L_y} \sum_{y=0}^{L_y} \sum_{x=0}^{L_x} Z_{xy} \qquad \textbf{4-3}$$

where L_x and L_y is smapling lengths in x and y direction respectively.

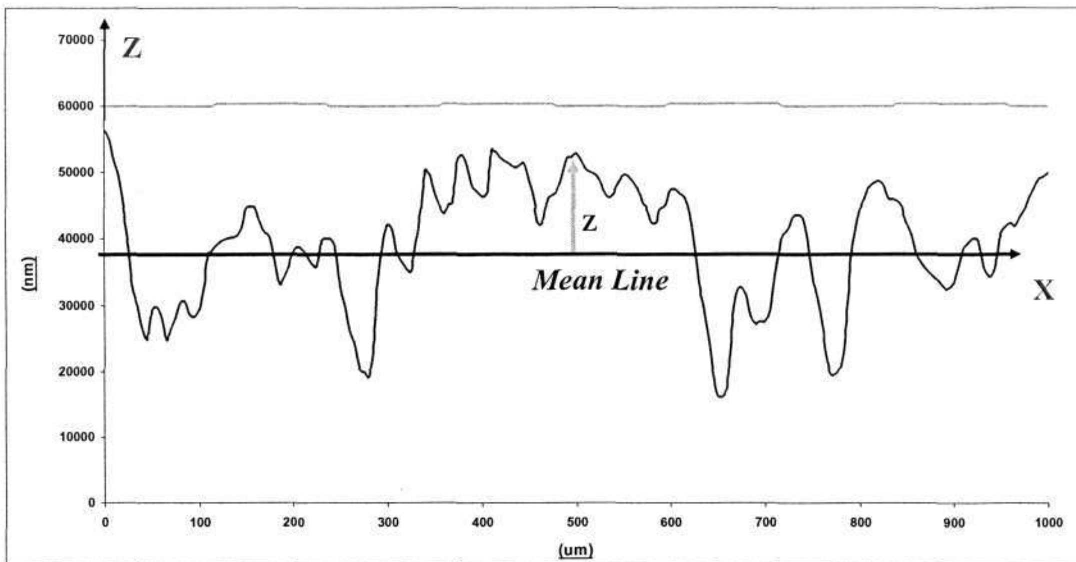

Fig. 4. 2 Typical trace profile of the polyurethane pad.

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When a wafer surface is pressed into contact with a pad, high spots or 'asperity' of the pad will deform and bring more asperities into contact. An asperity ($z_x = Z_x - m$) is defined as a peak in profilometer trace where three adjacent sample heights, z_{x-1}, z_x, z_{x+1}, the middle one z_x is greater than both the outer two. The asperity is assumed to be spherical in shape and thus curvature of asperity can be defined as:

$$\kappa_c = \frac{(z_{x+1} - 2z_x + z_{x-1})}{j^2} \quad \text{4-4}$$

and thus radius of curvature is:

$$\beta = \frac{1}{\kappa_c} \quad \text{4-5}$$

where j is the discrete interval length between two heights measurement.

4.2.1 Statistical Parameters: Moments of a Probability Distribution

The shape of probability distribution of height and curvature of the asperity from the pad measurement provides useful information on the contact behavior at the interface between wafer and polyurethane pad. This shape property can be expressed in terms of moments of the general function as follow:

$$M_n = \int_{-\infty}^{\infty} x^n p(x) dx \quad \text{4-6}$$

where M_n is defined as the nth moment of the distribution and in this particular case that the distribution is a probability density, $p(x)$. As for pad characterization study, $p(x)$ is replaced by $p(z)$ for asperity height and $p(\kappa)$ for asperity curvature. For completeness, zeroth moment is always 1 due to the density distribution being normalized and the mean of the distribution is defined by the integral that happens to be the first moment. The second moment helps to describe the way that the

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probability density is distributed about its mean. For discrete distribution such as asperity height from measurement it can be expressed as follow:

$$M_2 = \int_{-\infty}^{\infty} (z)^2 p(z)dz = \frac{1}{L_x L_y} \sum_{y=0}^{L_y} \sum_{x=0}^{L_x} z_{xy}^2 = \sigma^2 \qquad 4\text{-}7$$

where σ is the standard deviation. The third moment M_3 is the skewness (Sk), a statistical parameter in defining variables with an asymmetric spread and represent the degree of symmetry of the density function. It is usual to normalize the third moment as describe as:

$$Sk = \frac{1}{\sigma^3} \int_{-\infty}^{\infty} (z)^3 p(z)dz = \frac{1}{L_x L_y \sigma^3} \sum_{y=0}^{L_y} \sum_{x=0}^{L_x} z_{xy}^3 \qquad 4\text{-}8$$

Whereas, the kurtosis (Ku) is the fourth moment M_4 and represents the peakedness of the distribution and the normalized fourth moment:

$$Ku = \frac{1}{\sigma^4} \int_{-\infty}^{\infty} (z)^4 p(z)dz = \frac{1}{L_x L_y \sigma^4} \sum_{y=0}^{L_y} \sum_{x=0}^{L_x} z_{xy}^4 \qquad 4\text{-}9$$

4.2.2 Measurement Results

Talyscan 150, a profilometer instrument is used to characterize the commonly used commercial perforated polyurethane pad as shown in figure 4.3. 1mm by 1mm scan area with the spacing of 5μm in length (x and y direction) and total number of 201 points in each traced are made. First, a datum is established by finding the straight line called the mean line in order to extract other parameter information from the data. A typical distribution of mean line is shown in figure 4.4. The first moment of the mean line distribution has a value of 38.29μm and since the standard deviations is relatively small, thus based on this value the asperities within the scan area are identified next.

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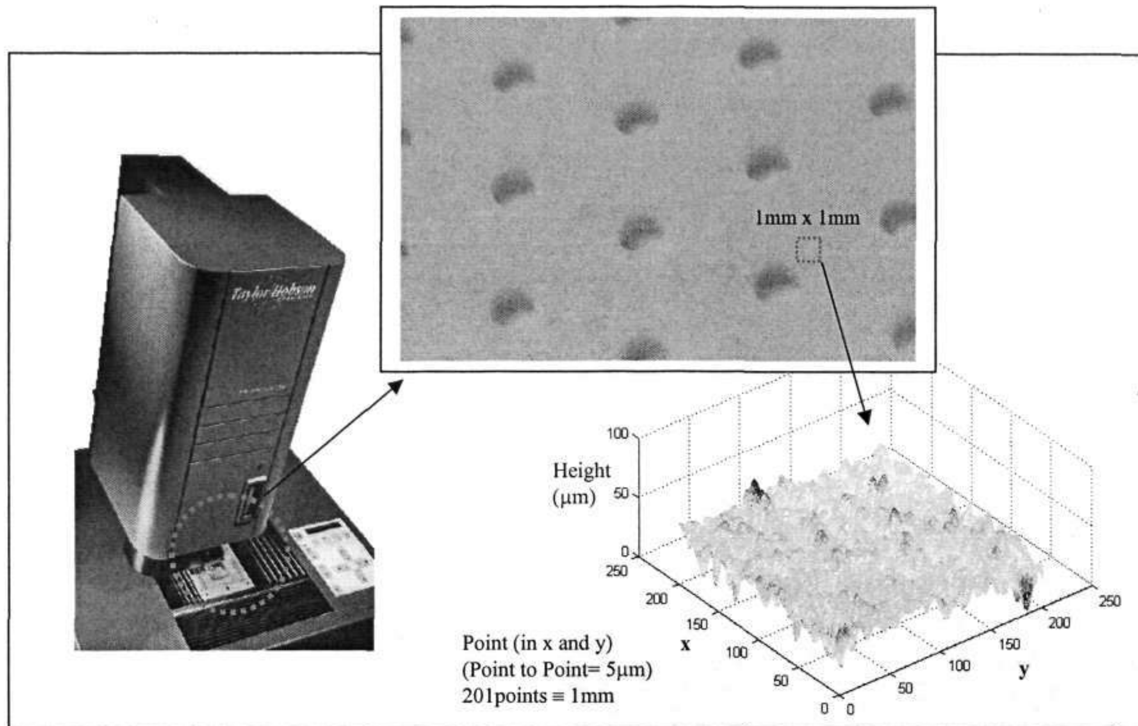

Fig. 4. 3 Perforated Polyurethane Pad Measurement of heights

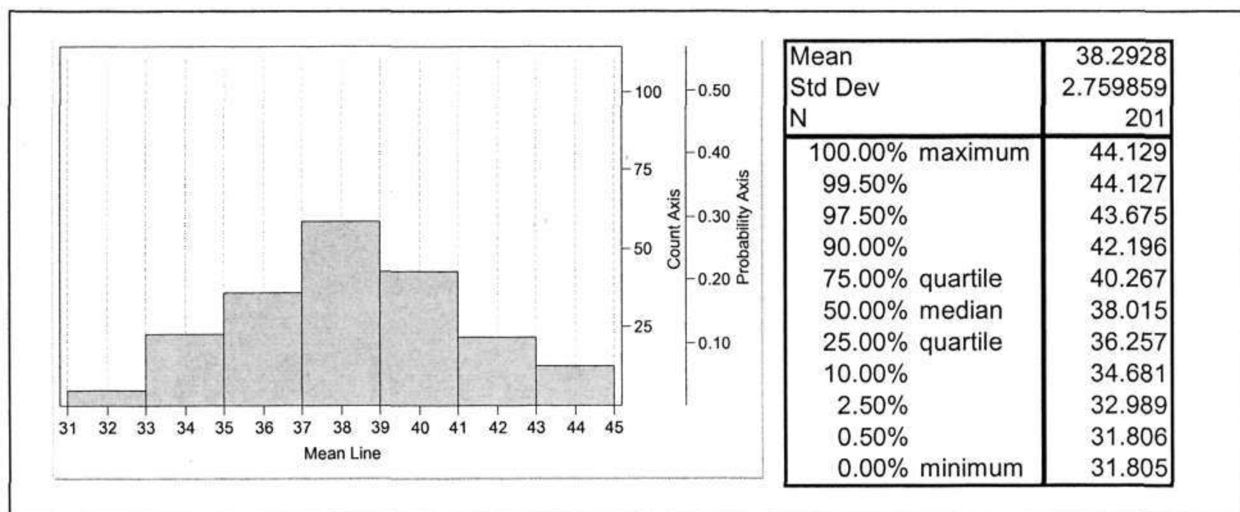

Fig. 4. 4 Distribution of mean line

Figure 4.5 shows the typical asperity height distribution, which exhibit a distribution close to that of a Gaussian probability function. It has the mean value of 3.9μm and standard deviation of 7.61 μm. For ideal Gaussian distribution, the skewness value is zero and kurtosis value is 3. Whereas, negative skewness and a lower kurtosis value is

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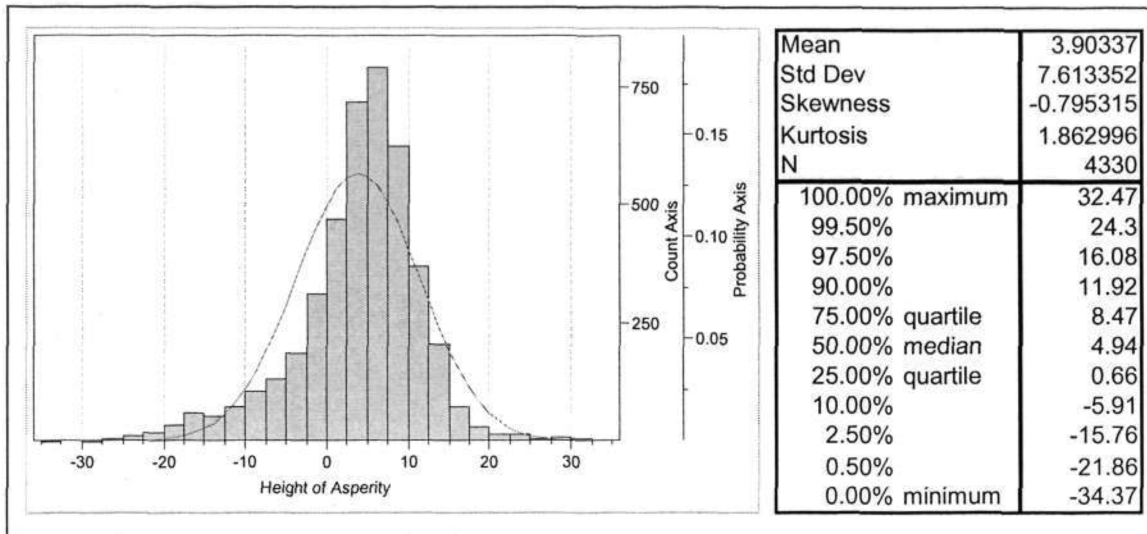
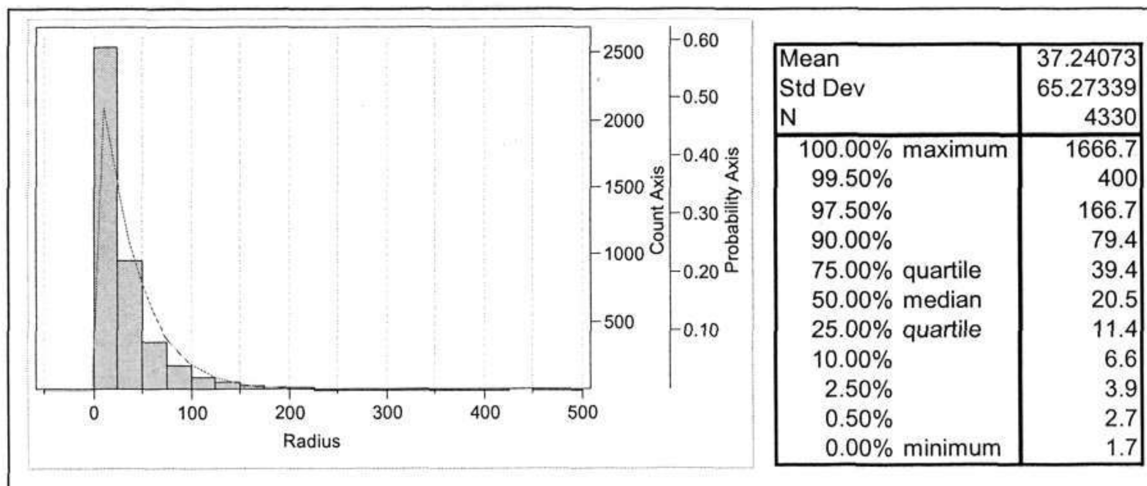
obtained from the measurements. This implies that more local asperity heights are above the mean line. Another piece of information can be obtained from this data is the density of the asperity which having a typical value of 4330 per mm^2.



Mean	3.90337
Std Dev	7.613352
Skewness	-0.795315
Kurtosis	1.862996
N	4330
100.00% maximum	32.47
99.50%	24.3
97.50%	16.08
90.00%	11.92
75.00% quartile	8.47
50.00% median	4.94
25.00% quartile	0.66
10.00%	-5.91
2.50%	-15.76
0.50%	-21.86
0.00% minimum	-34.37

Fig. 4. 5 Height asperity distribution

The respective curvature for the asperities is then calculated and can follow an exponential like distribution as shown in figure 4.6.



Mean	37.24073
Std Dev	65.27339
N	4330
100.00% maximum	1666.7
99.50%	400
97.50%	166.7
90.00%	79.4
75.00% quartile	39.4
50.00% median	20.5
25.00% quartile	11.4
10.00%	6.6
2.50%	3.9
0.50%	2.7
0.00% minimum	1.7

Fig. 4. 6 Curvature asperity distribution

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4.3 Real Contact Area between Wafer and Polyurethane Pad.

The physical illustration in scale at the interface between patterned wafer surface and polyurethane pad is shown in figure 4.7. The applied pressure, $P_{applied}$, is supported by asperities and the fluid film which fills the gap between asperities and pores or channels (eg: perforated or groove) on the polyurethane pad. Real contact area between wafer and polyurethane pad is a fundamental issue to provide a better understanding for the interface. Although real contact area is considered in most of the modeling works [47, 77, 78], assumptions of constant radius curvature and/or constant asperity height are always employed in their studies. Furthermore, no detailed study about the effect of the separation distance on the real contact area as the function of step height on the patterned wafer has been published. Real contact area is the main factor that will affect the number of participating abrasives, the amount of load that is applied to each abrasive influences the indentation depth of the abrasive into the wafer surface in the material removal process as indicated from the roughness on the wafer surface as shown on the top left hand side in figure 4.7. Thus, a detailed investigation on the separation distance of the real contact area at the interface based on pad characterization results is presented in this section. From a local point of view, instead of a specific contact mode condition, each local location on the wafer surface will experience a different type of contact mode (such as solid-solid contact, hydroplaning or mixed) at any instant. This is a matter of degree of each mode at the specific process conditions. However it is almost impossible to predict which contact mode that particular interest local locations on the wafer surface is experienced at the specific instant due to the complex mechanics and dynamics interaction of each mode. In a typical CMP process for IC fabrication, 3 to 5 psi (~20-35kPa) applied pressure is commonly used, which is as good as putting a weight of 66 to 110 kg on the backside of the 200mm wafer and relatively slow angular velocity (<200 rpm or less than 2m/s of linear relative, refer to section 2.3.2; whereas ~1000rpm range for bearing operation) is used for both platen and carrier, thus solid-solid contact mode is focused. In this study, the applied load is mainly carried by asperities that are assumed to have spherical summits; however an assumption of constant height and curvature of asperities is not adopted. Since *in situ* conditioning is commonly used and polyurethane pad have high compliance properties, theoretical estimation of the real contact area based on linear elastic contact is further assumed.

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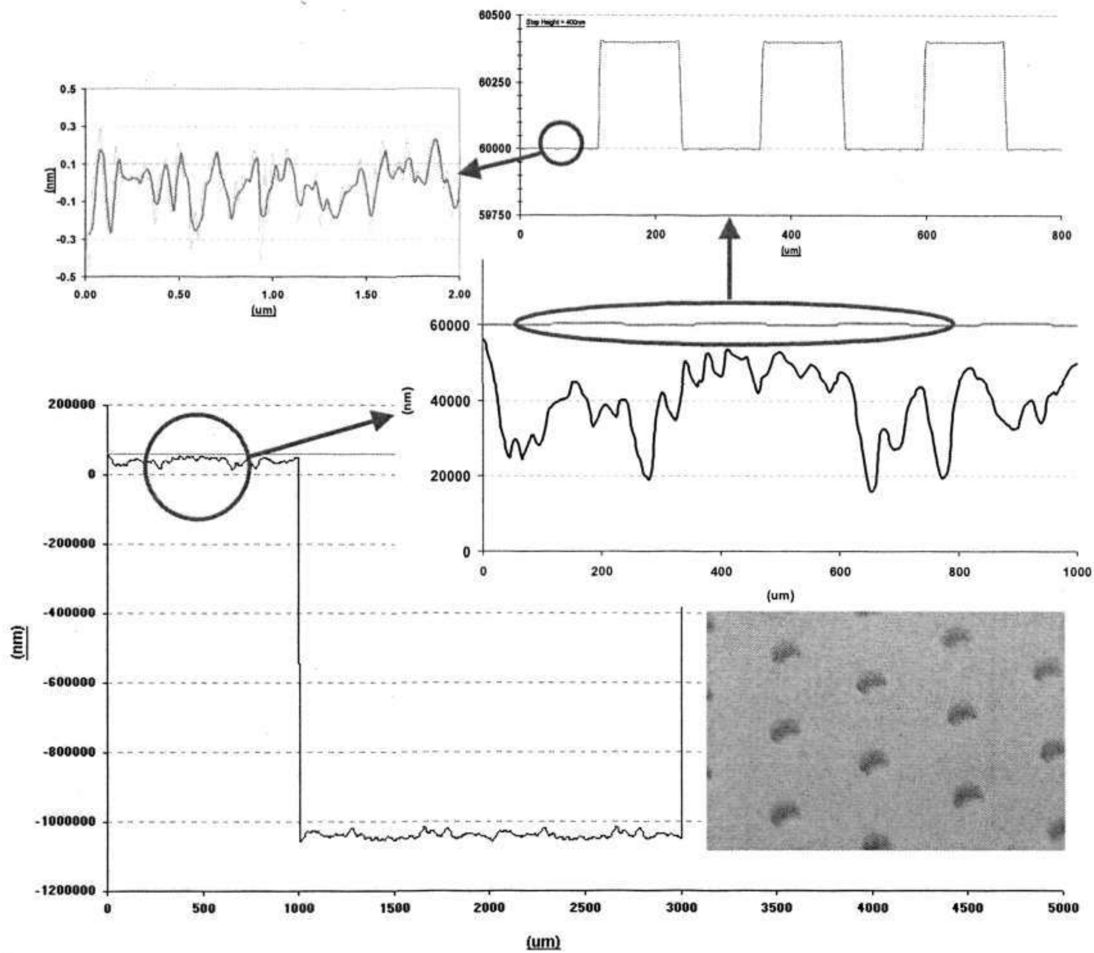

Fig. 4. 7 Interface between patterned wafer and polyurethane pad.

Under these conditions, the contact area formed by a single asperity can be evaluated through the following geometrical equation:

$$a_s = \pi\beta(z-d) \qquad \textbf{4- 10}$$

where d is the separation distance (measure from mean line, refer to figure 4.2) between wafer surface and polyurethane pad. The total contact area form by asperities between wafer and polyurethane pad is obtained from integration:

$$A_{pad} = \eta A \int_{d}^{\infty}\int_{0}^{\infty} a_s \phi_\beta \phi_z \, d\beta \, dz \qquad \textbf{4- 11}$$

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where η is the density of the asperity and take note that A is projected nominal wafer size area on the polyurethane pad by excluding pores on the pad surface. (As reviewed in chapter 2, e.g:17% of the area is occupied by the groove). From the measurement results as shown in the previous section, the asperity height can be approximate to a Gaussian distribution, whereas radius curvature of the asperity having an exponential distribution as describe as:

$$\phi_z = \frac{1}{\sqrt{2\pi S_z}} e^{-\frac{z^2}{2S_z^2}} \tag{4- 12}$$

$$\phi_\beta = \frac{1}{\beta} e^{-\frac{z}{\beta}} \tag{4- 13}$$

where S_z =7.6μm and β =37μm (refer to figure 4,5 and 4.6). The deformation of all the asperities is assumed within an elastic region and thus Hertz's theory [79] is employed to relate the separation distance and the applied load for single asperity in contact with a rigid plane:

$$P = \frac{4}{3} E^* \beta (z-d)^{\frac{3}{2}} \tag{4- 14}$$

where $E^* = \frac{E}{1-\nu^2}$ is an effective Young's modulus of asperity with E is Young's modulus of asperity and ν is Poisson's ratio . The total load at the interface is:

$$Load_{pad} = \eta A \int_d^\infty \int_0^\infty F \phi_\beta \phi_z \, d\beta \, dz \tag{4- 15}$$

Since the $Load_{pad}$ is equal to $Load_{\text{applied}}$ and $A_{apparentwafer}$ is the nominal area of the wafer as described in force balance equation 4-1, separation distance, d can be theoretical estimated for a given applied pressure used in a CMP process. As for

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patterned wafers, equation 4-15 needs to be modified to take into account for the step height on the wafer surface.

$$Load_{applied} = \eta A\left[\alpha\int_{d}^{\infty}\int_{0}^{\infty} P_{trench}\phi_{\beta}\phi_{z}d\beta dz + (1-\alpha)\int_{d}^{\infty}\int_{0}^{\infty} P_{land}\phi_{\beta}\phi_{z}d\beta dz\right] \quad 4\text{-}1$$

where α is area fraction of trenches on the patterned wafer surface and F_{land} is same as described by 4.14, whereas

$$P_{trench} = \frac{4}{3}E^{*}\beta(z-d-h)^{\frac{3}{2}} \quad 4\text{-}2$$

where h is the step height difference between land and trench.

4.1.1 Simulation results of contact area and contact pressure

Equation 4-15 and 4-11 are solved numerically through the trapezoid rule for the separation distance, d, and the contact area, A_{pad}, since the applied load for the process is known in advance. This is done iteratively by assuming an initial d and using equation 4-15 to calculate the corresponding applied load and d is updated until the actual applied load is obtained. A total of 3000 integration points with an increment of 0.01μm for asperity height is employed. Equation 4-2 is then used to calculate the average contact pressure. Effective Young's modulus of asperity is assumed to be 100MPa [80]. Figure 4.8 is an example to show the d and the contact area ratio ($A_{pad}/A_{apparentwafer}$) as a function of the applied pressure. The corresponding contact pressure is plotted in figure 4.9. Around four orders of magnitude higher for the pressure at the interface as compared to the typical pressure applied at the rear side of the wafer in the CMP process. However, this contact pressure at the interface does not vary dramatically over a wide range of applied pressures. This suggests that an increase in material removal rate as the applied pressure in CMP process is increased is due to an increase in the contact area rather than the interface pressure. The physical scale illustration of the sizes of abrasive (0.2μm- 1μm) in the commercial slurry for CMP process are much smaller than the asperities is shown in figure 4.10.

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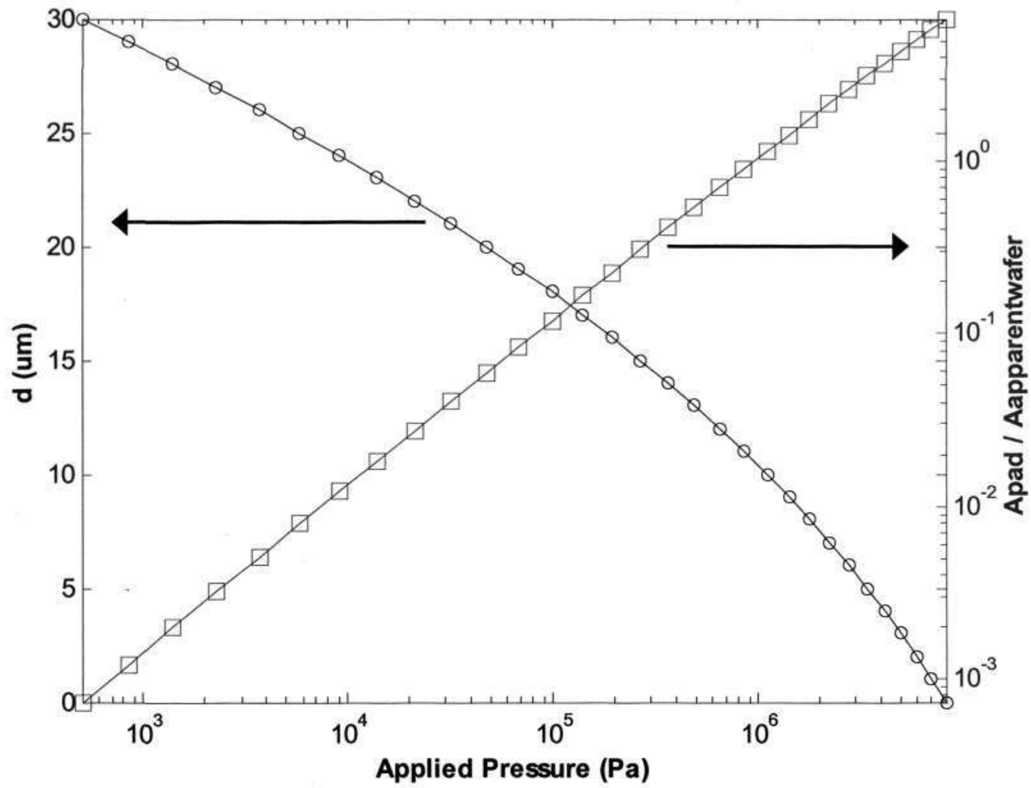

Fig. 4. 8 Separation distance (*d*) and contact area ratio as the function of applied pressure.

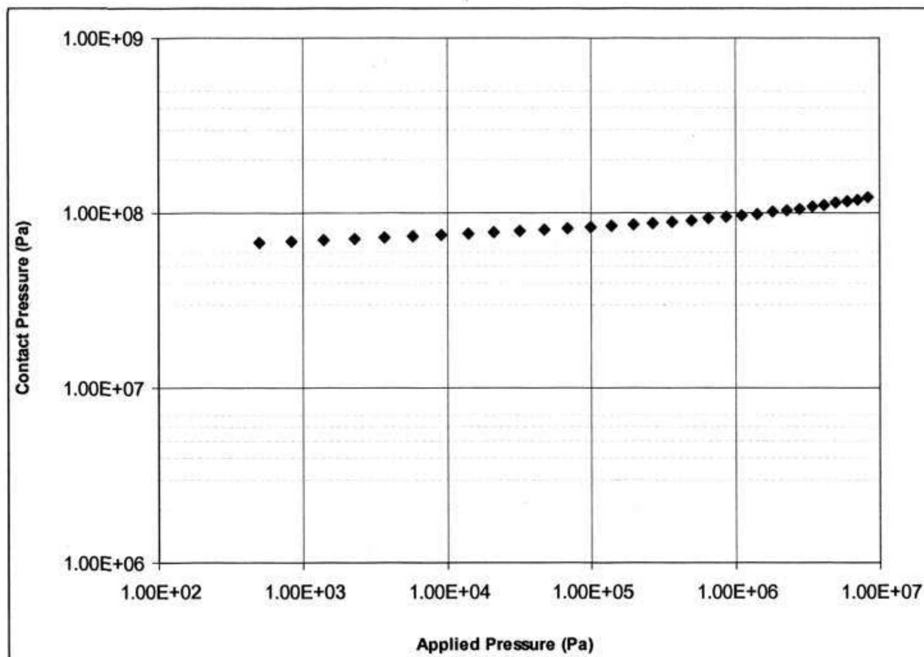

Fig. 4. 9 Interface pressure as the function of applied pressure

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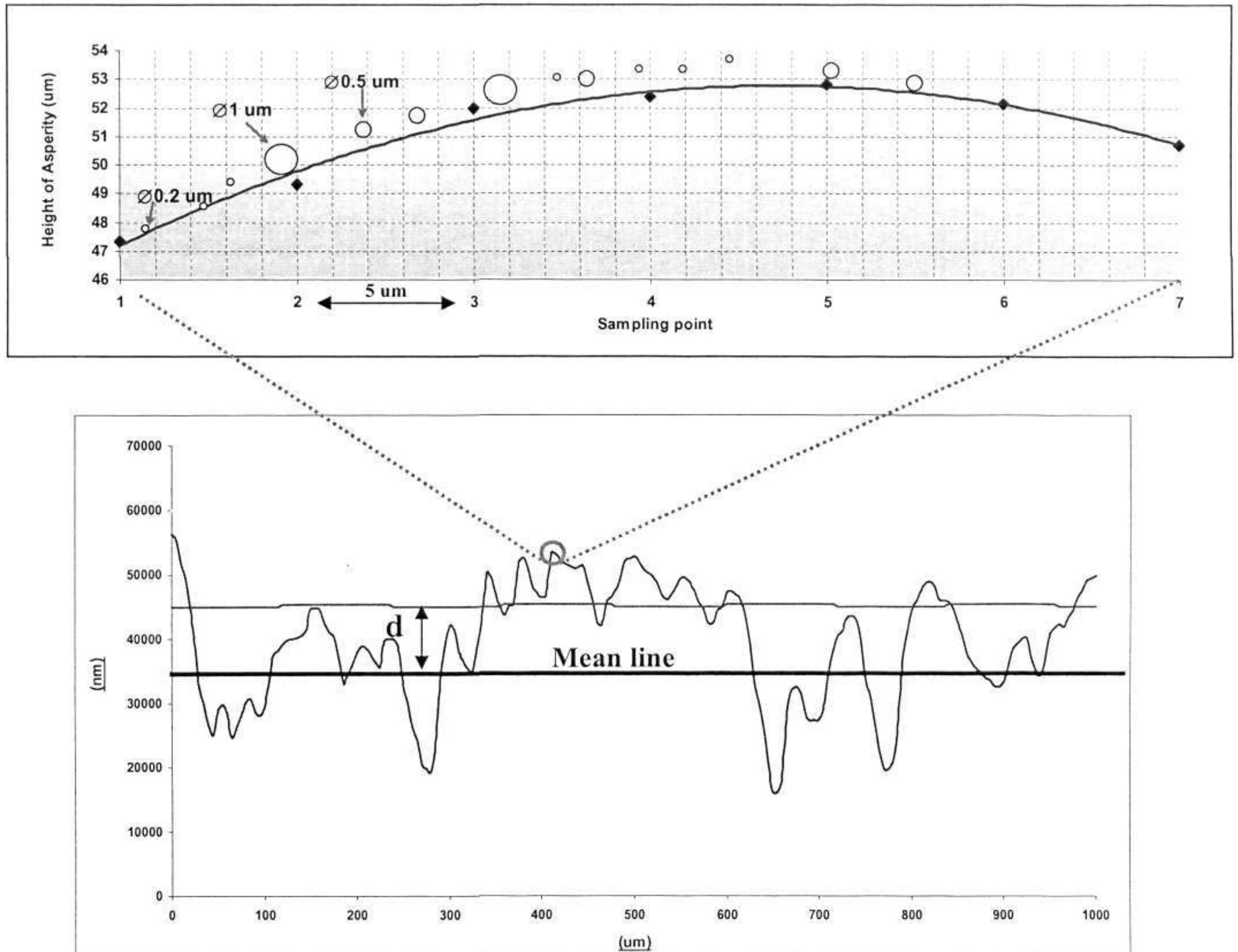

Fig. 4. 3 Abrasives on the asperity

When the wafer is pressed against the polyurethane pad, the contact area formed by the asperities will determine the number of participating abrasives. Thus, an increase in CMP material removal rate as the applied pressure increases [4] is the result of a significant increase in the contact area that will capture and embed more abrasives with a higher and almost stable average contact pressure. Since abrasive is a second order influence factor, it is ignored in this work. As for patterned wafers, equation 4-16 is solved numerically by assuming two dimensional periodic structure on the wafer surface with the α value of 50% and a typical initial step height value is taken care by equation 4-17.

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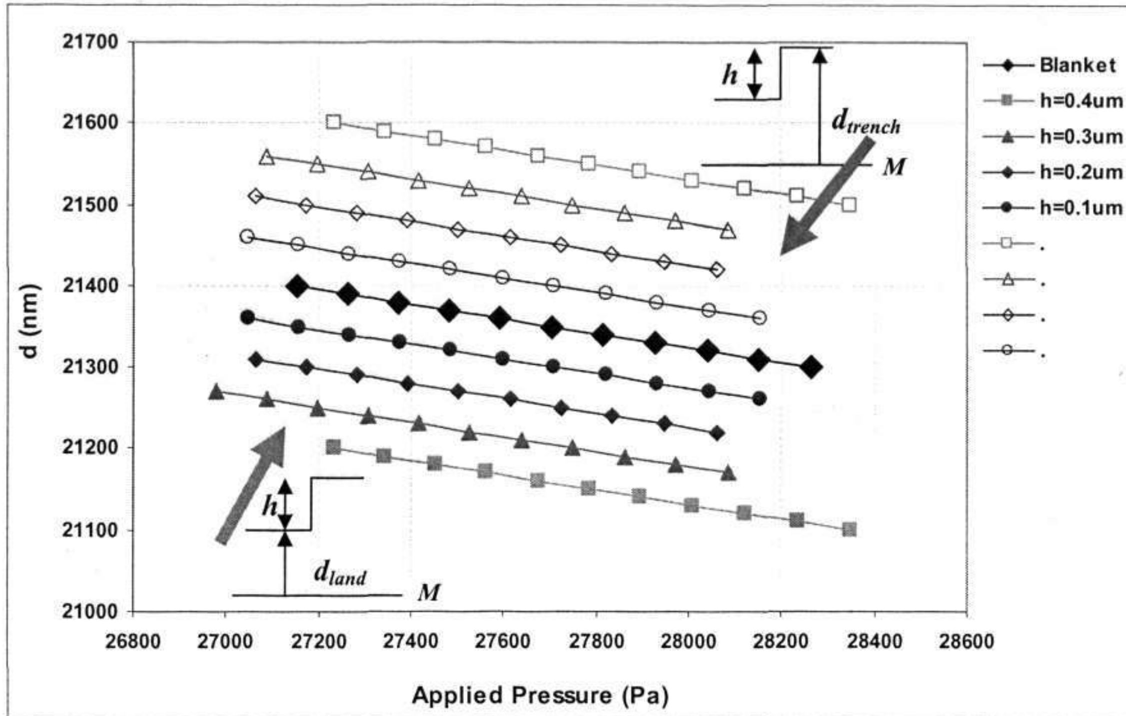

Fig. 4. 11 *d* as the function of step height over a range of applied pressure.

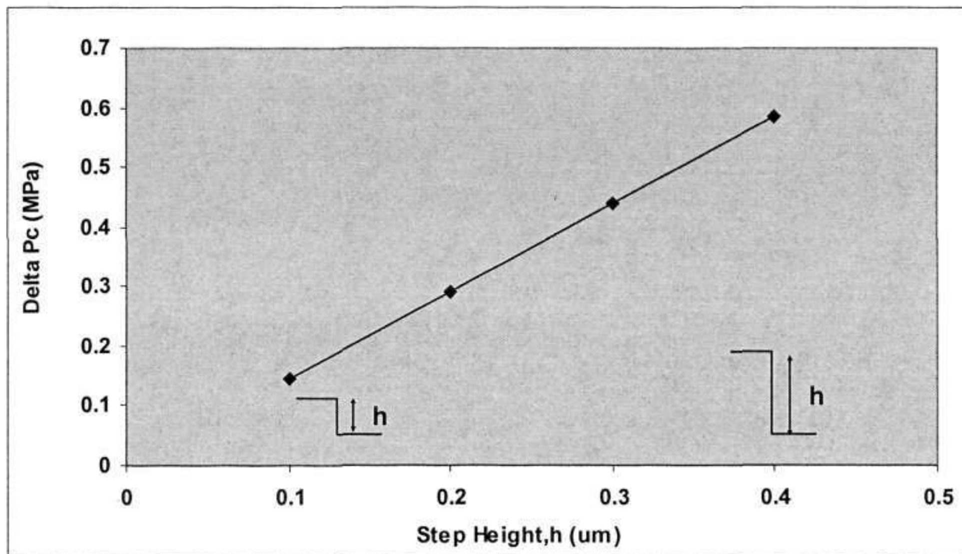

Fig. 4. 12 Contact pressure difference as the function of step height.

Figure 4.11 shows the evolution of *d* for the land and trench on the patterned wafer as step height is reduced over a typical applied pressure condition with the initial step height of 4000Å. If perfect planarization can be achieved, both land and trench will eventually have the same magnitude of *d* as for a blanket wafer under the same process condition. Due to the difference in *d* for the two locations, the land will have a

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larger contact area as compared to the trench and therefore a pressure difference will exist for these two locations on the patterned wafer. The evolution of average contact pressure difference is shown in figure 4.12.

4.3.2 Experimental Observations

Experiments have been conducted to characterize the material removal rate on both lands and trenches on the patterned wafer by using the in-house (Chartered) 0.13μm test mask. Around 4000Å silicon dioxide (SiO_2) thin film is deposited on 200mm patterned wafer by HDPCVD. The typical initial step height profile of a process monitoring structure along the scribe line on the patterned wafer is then measured by KLA-Tencor's high resolution profiler as shown in figure 4.13. Spectroscopic ellipsometry (ASET-F5x) is used to measure pre and post thickness of the thin film on both land and trench locations. A total of 20 die measurements are made. The wafer is then processed using one of the platen from Mirra CMP tool with IC1000 perforated polyurethane pad and commercial silica based slurry. The typical process condition is shown in table 3.1. Step height and material removal rate of the respective structures are monitored at four different time intervals. Figure 4.14 shows the typical step height evolution. As suggested by the results, a linear reduction of the step height can be assumed. The corresponding time interval material removal rate for the lands and trenches is shown in figure 4.15. Results indicate that for typical process monitoring structures in IC fabrication, assumption of zero material removal for trenches or so-called down area is not applicable since trenches exhibits nearly 40% material removal rate of lands as shown in an initial time interval. Locations of land having a material removal rate of around 5500Å/min up to the first 20 seconds, and then followed by a sharp decrease in material removal rate down to 1000Å/min for the last time interval. Whereas the changes in the material removal rate at trenches are not that drastic; a material removal rate of around 1000-3000Å/min occurs throughout the four time intervals. However, the difference in material removal rate for both lands and trenches is getting smaller as step height is reduced. This is in agreement with the simulations results as shown in figure 4.12 since the material removal rate for SiO_2 CMP is proportional to the pressure term as suggested by Preston equation [35].

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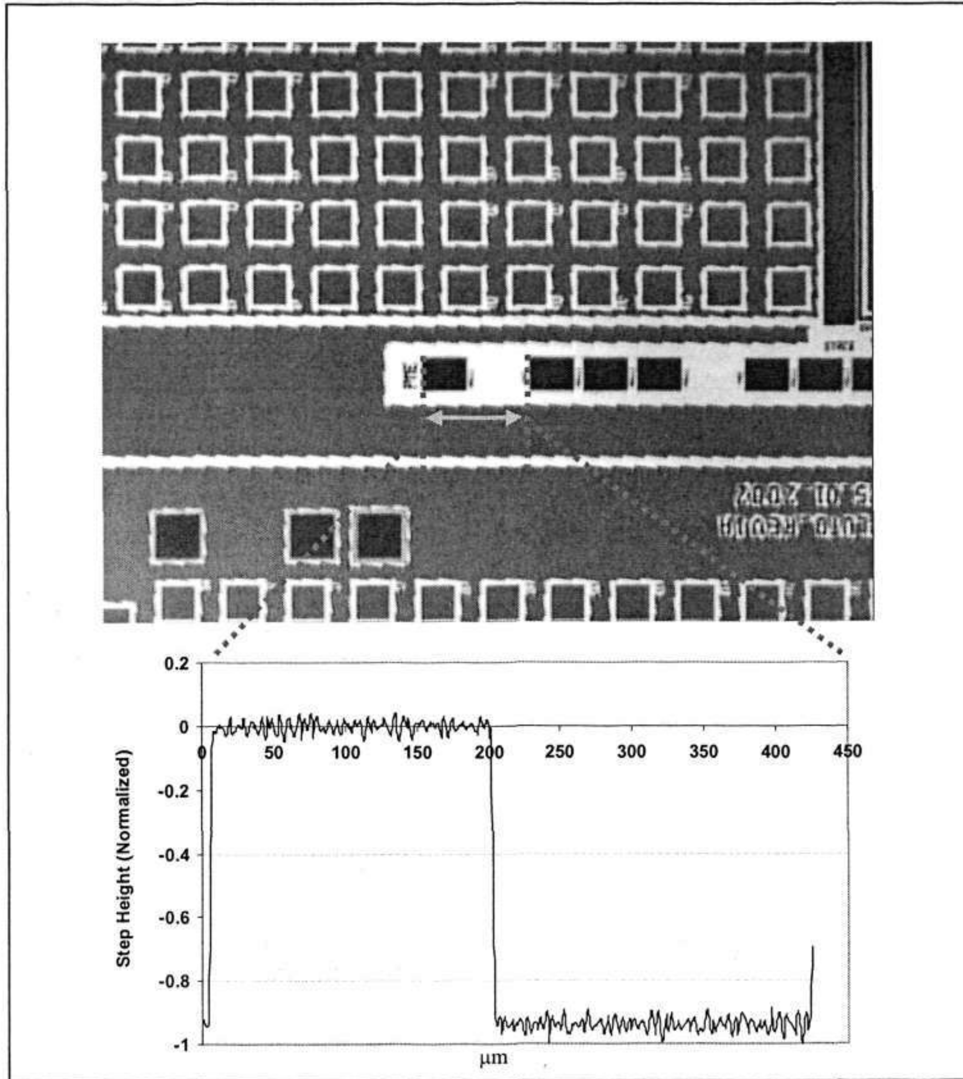

Fig. 4. 13 Step height profile in typical process monitoring structures

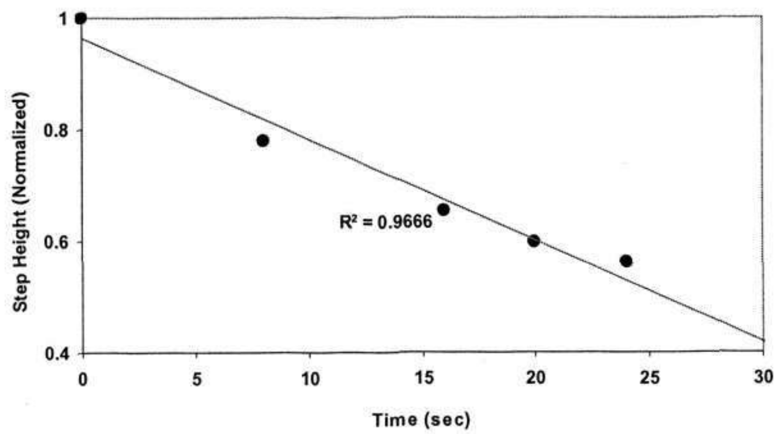

Fig. 4. 14 Step height evolution

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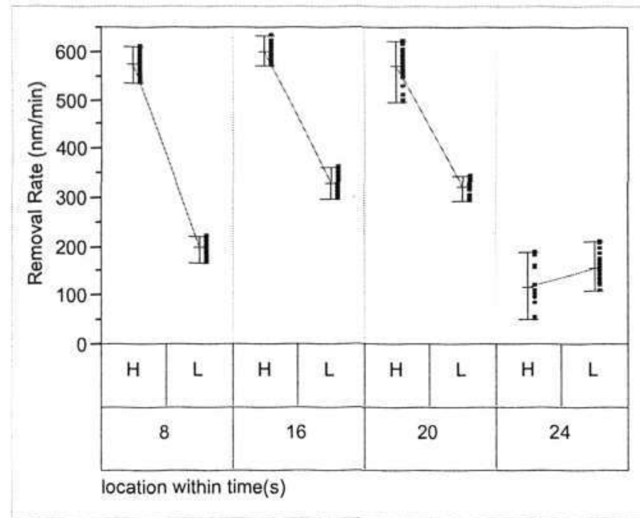

Fig. 4. 15 Material removal rate at both lands and trenches locations

4.3.3 Discussion

The entire wafer surface is assumed to be in contact with the polyurethane pad via asperities. Unlike the CMP process, others IC fabrication processes such as photolithography, a high precision wafer vacuum chuck is needed [81]. It must hold a wafer flat to extremely tight tolerances of 100 to 200nm all the way across the wafer substrate [81].Whereas the total thickness variation (TTV) specification for the 200mm CZ wafer should be ≤15μm for 200mm wafer as according to the ASTM method [82]. Whereas, in common CMP equipment design, instead of vacuum the wafer substrate, a wafer is pushed against the polyurethane pad. In this situation, the wafer substrate is free to deform. Due to imperfections in the wafer substrate, in reality a different value of d exists across the entire wafer surface even for blanket wafers. Due to the difference in d, the contact area will be location dependent and thus the material removal rate will vary. This explains the improvement of non-uniformity on wafer level (NUWIW) performance in the CMP process as a function of total thickness variation of substrate (refer to figure 2.3) is reduced [30]. An increase in the non-uniformity removal rate as a result of the pad not being properly mounted on the platen [83] could explain the difference in d across the wafer surface.

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4.4 Methodology Development

As mentioned before consistency in achieving a specific target mean film thickness within a tight tolerance is critical and a major challenge for deep submicron IC fabrication. The failure of end point detection system in providing a stable and repeatable signal affects the repeatability of the process in achieving target mean film thickness and hence the reliability of the circuit performance. In general, for large volume manufacturing, timing is the only input parameters that can be manipulated while others remain unchanged in a specific recipe to reduce source of variations. Several works [84-86] have proposed models to predict the post thickness of the structures within die which attribute to the effect of pattern density in particularly. These works provide some insight for the IC design point-of-view. However, from the IC fabrication standpoint the process should be pattern density independent and repeatable to obtain the average post target thickness across the wafer with realistic and minimal input information. In previous sections, contact mechanics approach has been employed to explore the fundamental understanding at the interface between polyurethane pad and wafer by incorporating the results from the pad surface characterization work. This knowledge is extended, in this section by developing a methodology that aims to improve the CMP process capability.

4.4.1 Blanket removal thickness (BRT)

For the ideal case the wafer is perfectly flat. Due to the step height (h), lands and trenches having a separation distance of d_{land} and d_{trench} respectively across the wafer as shown in figure 4.12. This results in a relatively large contact area formed by the asperities at the lands as compared to trenches on the wafer for a given applied pressure. Thus, there is a pressure difference at these two locations with lands on the wafer sharing a larger portion of the applied load as shown in figure 4.16 from the simulation result. As step height is decreased, d_{land} increases and d_{trench} decreases proportionally as illustrated in figure 4.12. In the case of perfect planarization, d_{land} and d_{trench} will have the same magnitude of separation distance and this value is exactly equal to d on the blanket wafer under the same process conditions. This implies that the pressure difference for these two locations is reducing as step height is reduced as indicated in figure 4.13. The material removal rate in CMP process is

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proportional to the pressure term ($RR \propto P^n$) as supported by the majority of experiments reported in the literature [21, 42, 51, 87] and particularly the linear relationship as suggested by Preston equation for oxide CMP [35].

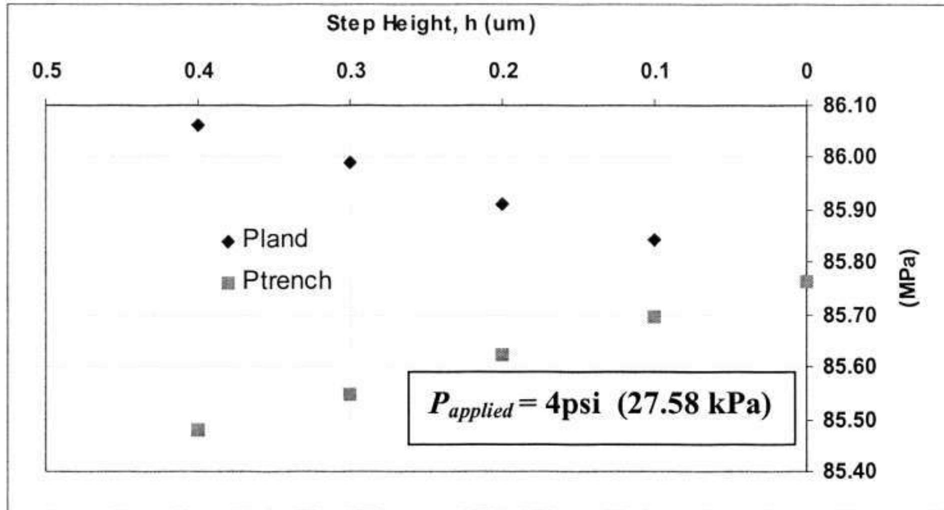

Fig. 4. 16 Evolution of P_{land} and P_{trench}.

Therefore, based on this physical premise, a material removal rate diagram for oxide CMP is presented in figure 4.17. Initially the material removal rate is higher at the location of the lands. This is attributed to the d_{land} being relatively lower which results in a larger contact pressure. As step height decreases, the corresponding material removal rate decreases proportionally. This continues until t_c, where ideal planariztion is achieved. A constant material removal rate is exhibited from that time onwards.

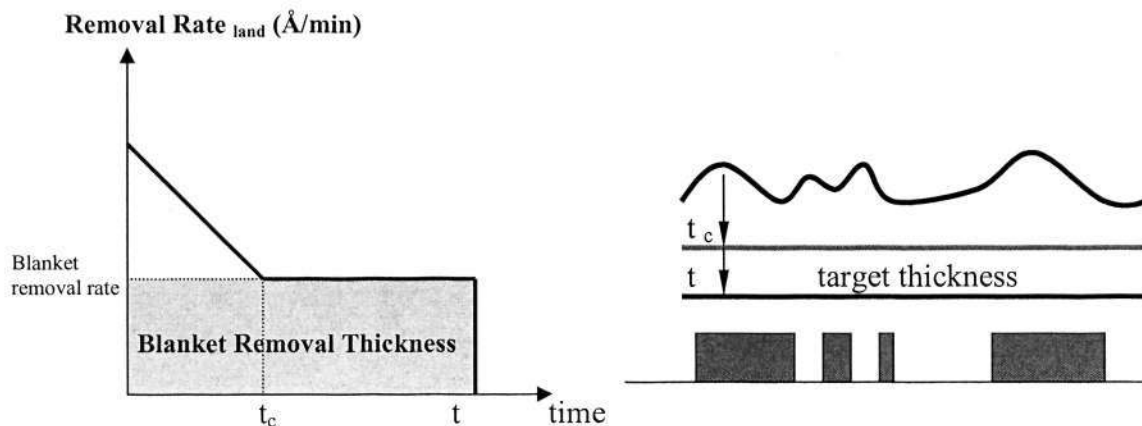

Fig. 4. 17 Removal rate diagram

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In the ideal case of a zero step height being obtained, pressure on the patterned wafer is exactly same as on a blanket wafer. The process continues until *t*, where the final target mean film thickness is obtained.

The area under the constant material removal rate as highlighted in grey in figure 4.17 is known as the blanket removal thickness. If perfect planazation is achieved, this area simply is the thickness that removed under the blanket removal rate condition within the period of *t*. This blanket removal thickness can be described as follows:

$$BRT = (Blanket\ \ Removal\ Rate\ x\ t) + (Removal\ Target - Actual\ Removal) \qquad \textbf{4-18}$$

where *t* is the actual process time, *Removal Target* is the targeted amount of thickness that need to removed and *Actual Removal* is the actual thickness removed within the period of *t* (i.e. the total area under the curve). Since the process is stochastic in nature, the timing for each wafer should be updated accordingly as:

$$t_{w+1} = \frac{BRT_w + (Pre\ thickness - Pre\ target)}{Blanket\ Removal\ Rate} \qquad \textbf{4-19}$$

where t_{w+1} is the timing for the next wafer, BRT_w is the blanket removal thickness of the current wafer, *Pre Thickness* is the actual incoming thickness of the next wafer and *Pre target* is the targeted incoming thickness from the upstream of the process. On top of disturbances of incoming thickness variation and material removal rate, this methodology takes care of the undetermined elements such as slurry and pad quality by *BRT*.

4.4.2 Process Capability

Process capability is the repeatability and consistency of a manufacturing process relative to the requirements in terms of specification limit. Rework is needed if the target mean film thickness of patterned wafer is not within the specifications. If the thickness is too thick (i.e. above upper specification), the wafer would be re-routed back through the CMP operation to receive additional process time. This procedure definitely results in increase of cycle time. On the other extreme which is more critical is where the wafer is too thin (i.e. below the lower specification). There is a

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possibility that the wafer might need to be scrapped in the case of underlying metal layer being exposed. However, if there is no exposure of metal, the wafer might be re-routed back to the deposition process and again followed by the CMP process. This rework procedure adds many hours of cycle time by receiving multiple redundant operations. Therefore, repeatability is important in IC fabrication to ensure higher throughput, lower cycle time and cost of manufacturing. Capability analysis determines the repeatability of a process by numerical assessment [88]:

$$C_p = \frac{USL - LSL}{6s} \tag{4-20}$$

where *USL* is upper specification limit of film thickness, *LSL* is lower specification limit of film thickness and s is the sample standard deviation. This index compares process spread to specifications, however it doesn't take into account for the lack of centering of process. It measures how capable the process could be. Whereas

$$C_{pk} = Min(C_{pl}, C_{pu}) \tag{4-21}$$

where

$$C_{pu} = \frac{USL - Mean}{3s} \tag{4-22}$$

and

$$C_{pl} = \frac{Mean - LSL}{3s} \tag{4-23}$$

measure how capable the process is by comparing process spread to specifications and accounts for lack of centering process.

4.4.3 Experimental Description and Results

In order to verify the concept of *BRT*, inter layer dielectric (ILD) or inter metal dielectric (IMD) CMP process are put into test. Typical ILD and IMD on the IC are

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shown in figure 4.18. The experiments are conducted on different layers for each different device. This implies that the methodology undergo various pattern density evaluation since each device layer has a unique pattern density produced by the layout of metal lines. First, 8000Å of HDPCVD oxide is deposited followed by 10000Å PETEOS oxide film. A total of 18000Å incoming oxide thickness is used for IMD layers and target post thickness after CMP process is 10000Å ± 800Å as illustrated in figure 4.18.

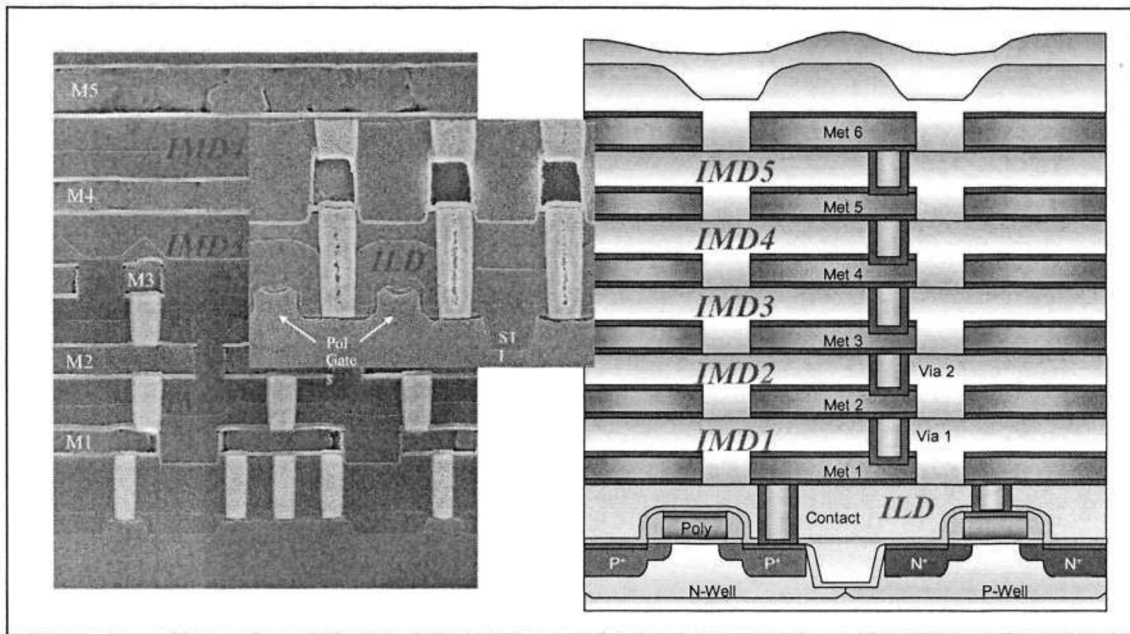

Fig. 4. 18 Typical ILD and IMD layers in IC device.

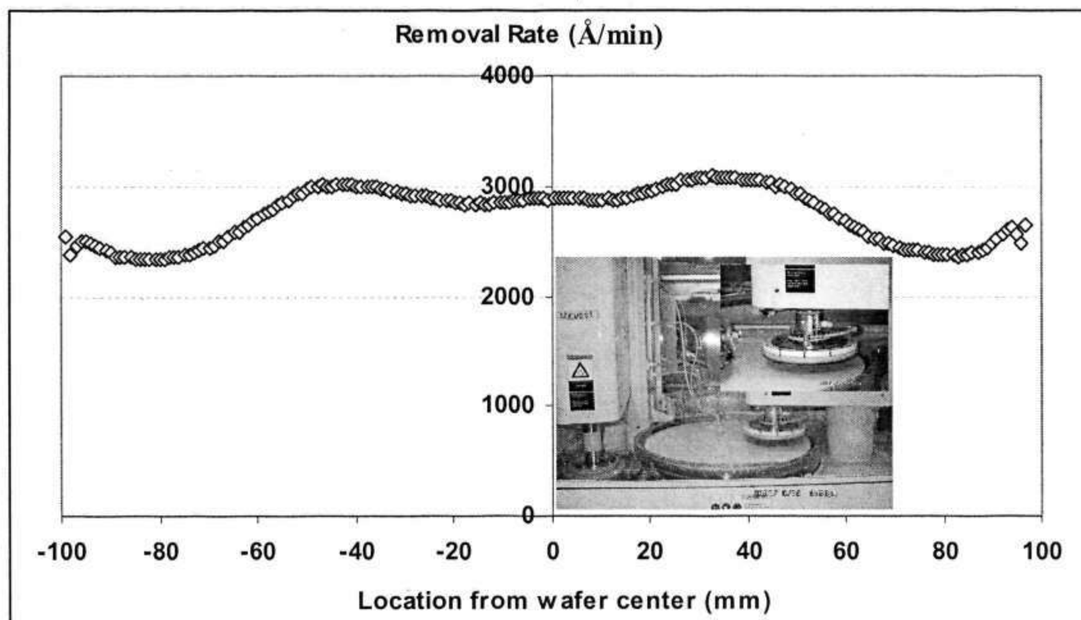

Fig. 4. 19 Blanket material removal rate profile in Ebara-222 CMP tool

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Commercial CMP tool Ebara 222, Rodel's IC1000 perforated pad and silica based slurry from Cabot are used in the experiments. The typical blanket material removal profile is shown in figure 4.19 and the process conditions are listed in table 4.1 for completeness.

Table 4. 1 Recipe for the process

Parameter	Step	Dress
Process time[Sec]	**Variable**	17
T.T. Rotation[rpm]	70	50
T.R. Rotation[rpm]	90	NA
T.R. Pressure[Pa*100]	414	NA
T.R. Oscillation[mm]	0	NA
Backside Pressure[Pa*100]	50	NA
Guide Ring Pressure(Pa*100)	250	NA
Slurry Select	Line A / B	D.I. + Atm
Slurry Rate LineA[cm3/min]	150	NA
Slurry Rate LineB[cm3/min]	150	NA
Diaphragm Pressure[Pa*100]	NA	NA

4.4.3.1 Off-line monitoring

Figures 4.20 and 4.21 show the actual and predicted thickness of IMD layers for two different IC products namely device A and device B. The actual post thickness is the result by the process time that is obtained from the decision made by the CMP operators based on the look-up table. Whereas the predicted thickness is the expected thickness that can be obtained by using the process time given by the *BRT* methodology. Around 50 wafers in each of the three different IMD layers for device A is monitored. C_{pk} less than 1 is observed for each layer in device A by using the timing given by the operators. However, the results show that *BRT* methodology provides better time estimation as shown by an improvement in C_p and C_{pk} value as indicated in the figure 4.20. Overall, an increase in a range of 24-35% and 17-22% in C_p and C_{pk} respectively for the three different layers in device A. The experiment is extended to another device to verify the effectiveness of this approach. Device B with four IMD layers and total of 170 wafers are monitored. Similarly, the wafer to wafer variations is reduced in each layer for device B as illustrated in the figure 4.21. The value of C_p is increased in a range of 32-37% for the four different IMD layers. A drastic improvement in C_{pk} is observed with an increase of up to 91% for IMD4 and

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52% for IMD3 in device B. Although the actual thickness for both IMD3 and IMD4 are relatively low spread as indicated by the value of C_p, operators tend to be more conservative in estimating the process time that result in the process being off-centered with the thickness relatively thicker as indicated by the value of C_{pk}. This explains the significant increase in these both layers. As shown in this off-line monitoring experiment, *BRT* methodology demonstrates capability in providing an optimum process time.

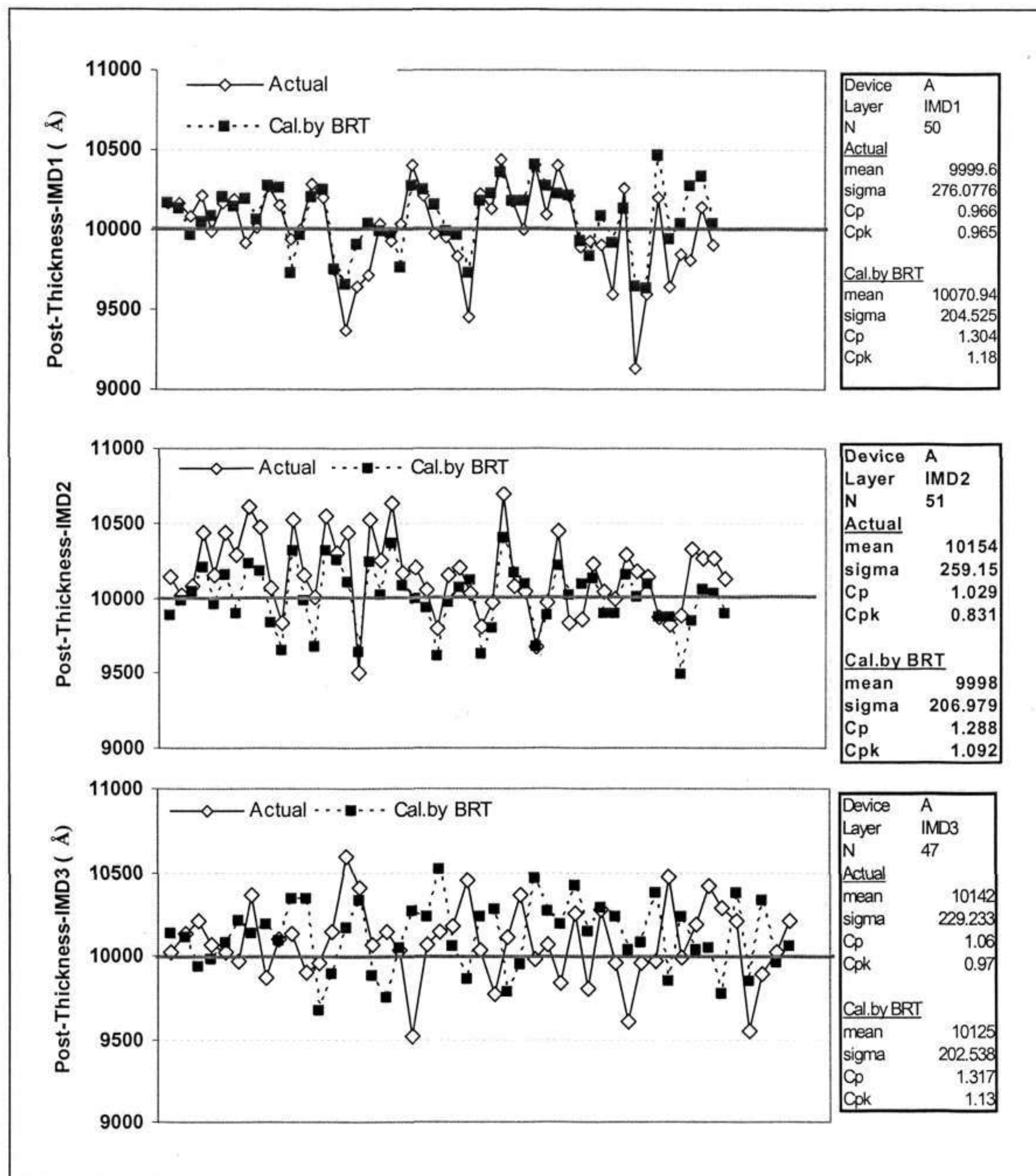

Fig. 4. 20 Comparison of wafer to wafer variation for Device A.

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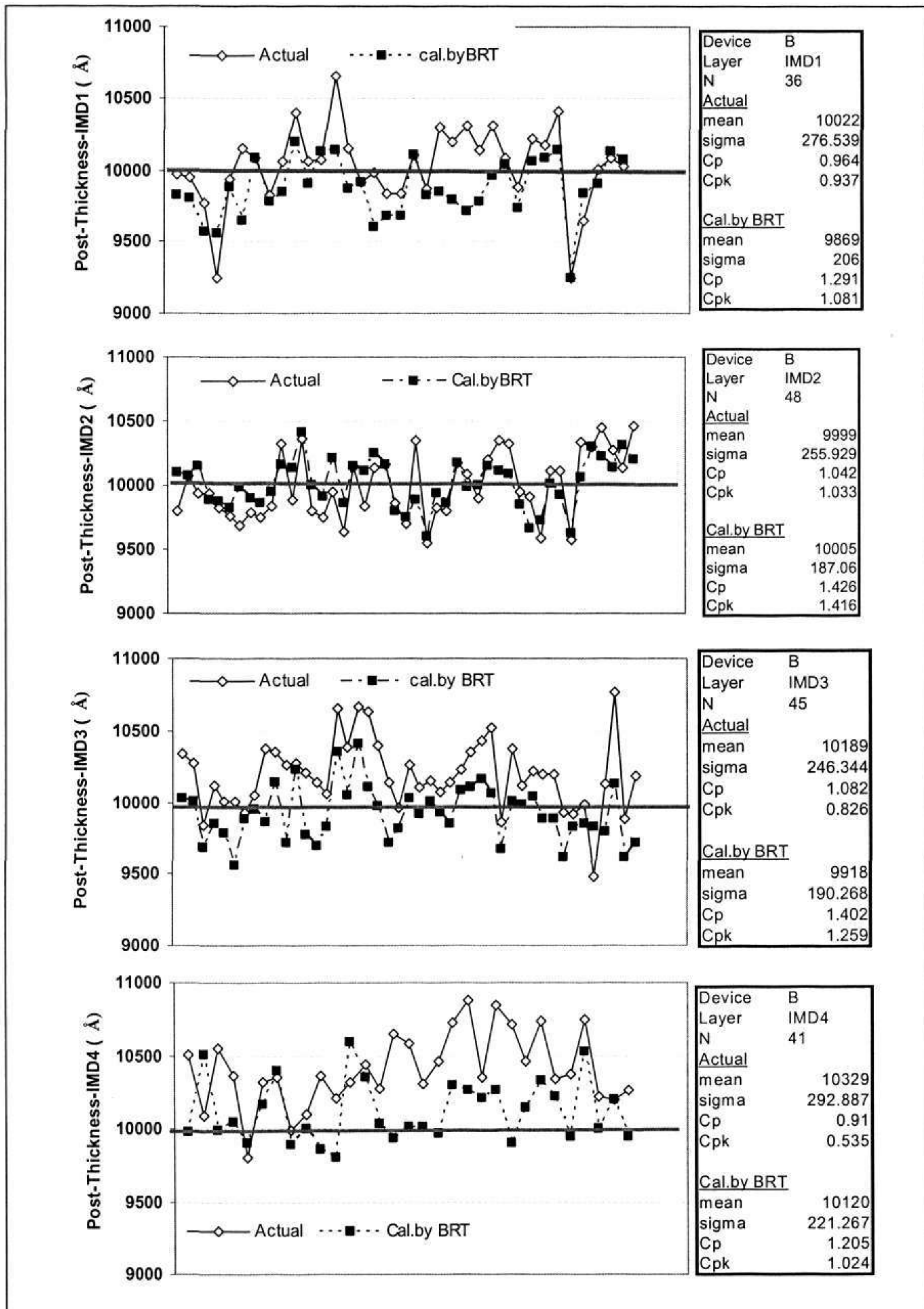

Fig. 4. 21 Comparison of wafer to wafer variation for Device B

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4.4.3.2 On-line Implementation

Through the improvement of process capability by employing *BRT* methodology as illustrated in off-line monitoring, experiments of implement the predicted process time on various devices at different layers are conducted. The results of a total of 71 wafers from four unique IC devices at different IMD layers are applied with the predicted timing offered by *BRT* methodology are shown in figure 4.22. Data shows that the wafer-to-wafer thickness variation is reduced as indicated by the C_p value of 1.27. The process is centered around the process target of 10000Å and this has resulted in C_{pk} value of 1.2.

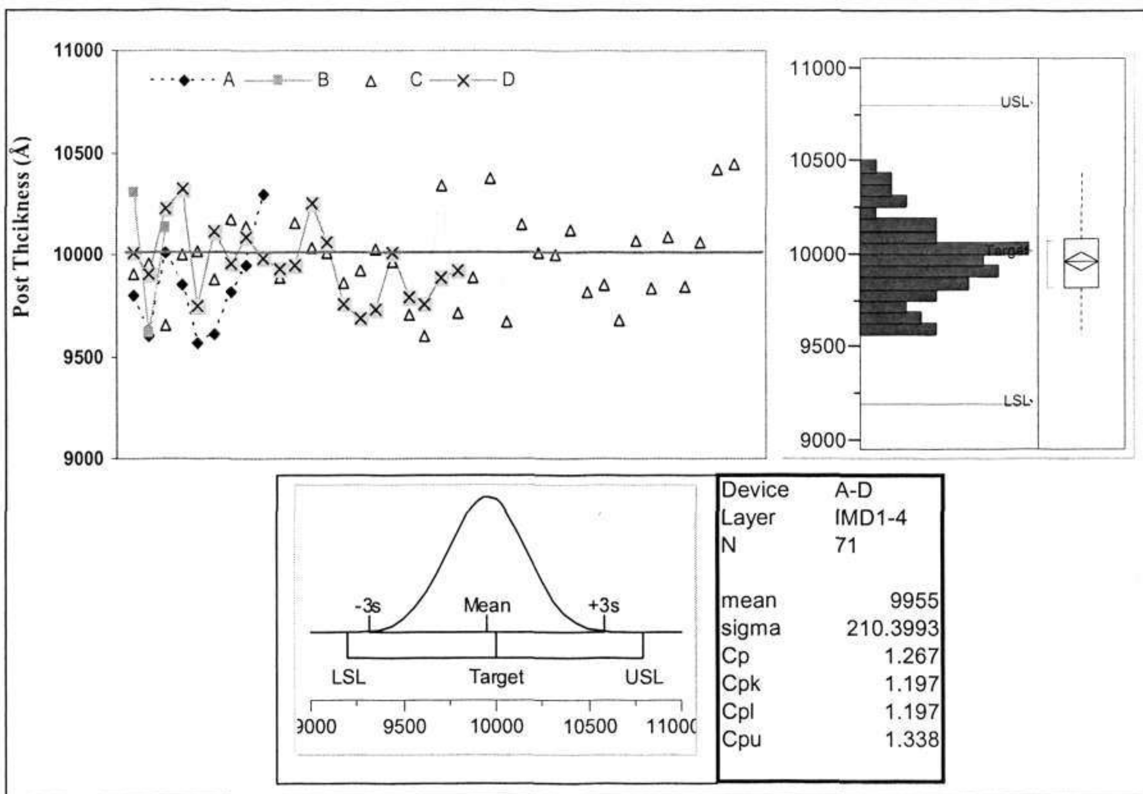

Fig. 4. 22 Wafer to wafer variation for four different devices by using *BRT* methodology

Prior to implementation of the methodology, tool operators used a time adjustment table to compensate for variations in incoming film thickness due to variation at the upstream deposition process. The corresponding process capability in each layer is shown in figure 4.20 and 4.21 and the overall performance for these two devices is shown in figure 4.23. In general, a typical value of C_{pk} is less than 1 and this

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performance metric is improved and tighter distribution is obtained by employed the *BRT* methodology as shown in figure 4.23. This suggests that the concept of *BRT* can provide a relatively optimum process time for any type of devices at different IMD layers.

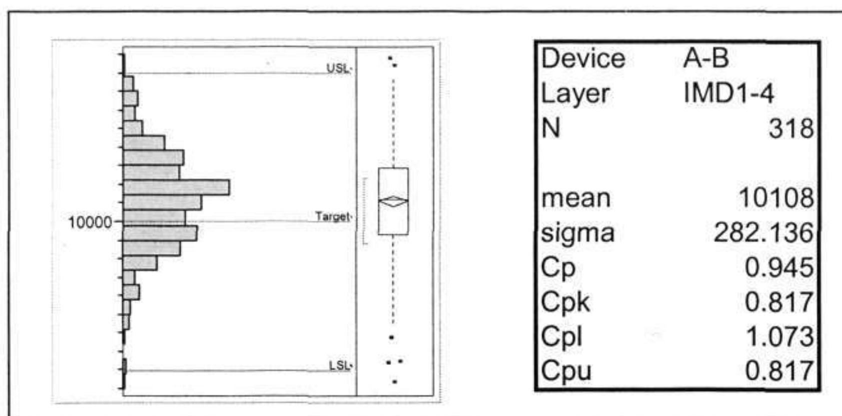

Fig. 4. 23 Typical C_p and C_{pk} value for two different device without implement the *BRT* methodology

The resulting reductions in process margin for IMD layers in manufacturing operation can create the opportunity to implement new design rules which could lead to better performance for devices. For instance, linewidth of metal line (refer to figure 4.18) variations reduction due to possible in re-optimization in lithography steps as the result of tighter distribution of post thickness provided in CMP process.

4.4.4 Discussions

Recently, there have been a number of works on modeling the CMP process as reviewed in chapter 2. The CMP process is complicated by many factors and incorporating all these factors into one single model is almost impossible. Therefore, this work has addressed only some aspects of a larger problem. Nevertheless, these efforts provide some insight to certain areas such as consumable development or IC layout design. Relatively few control-relevant models have been developed for CMP process. One of the major issues of the CMP process in IC fabrication is to ensure that the average film thickness is within a tight tolerance specification for any type of pattern density on the devices. A model is expected to capture the behavior of the process and on the other hand too much insignificant information should be avoided due to the computation-intensive nature of the process which is unrealistic in the

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production environment. As such, this *BRT* methodology based on the contact mechanics model has been developed and offered alternative means for predicting the optimum process time. The experimental data show that the thickness of IMD layers after the CMP process have a tighter distribution and the corresponding mean value is closer to its target after implementation of the *BRT* methodology. In addition, this methodology can be extended by incorporating into a run-to-run controller design to further enhance the CMP process performance. There are many different ways that a run-to-run controller can be formulated in order to perform the necessary control task. A simple run-to-run controller design for the CMP process is shown in figure 4.24 for illustration.

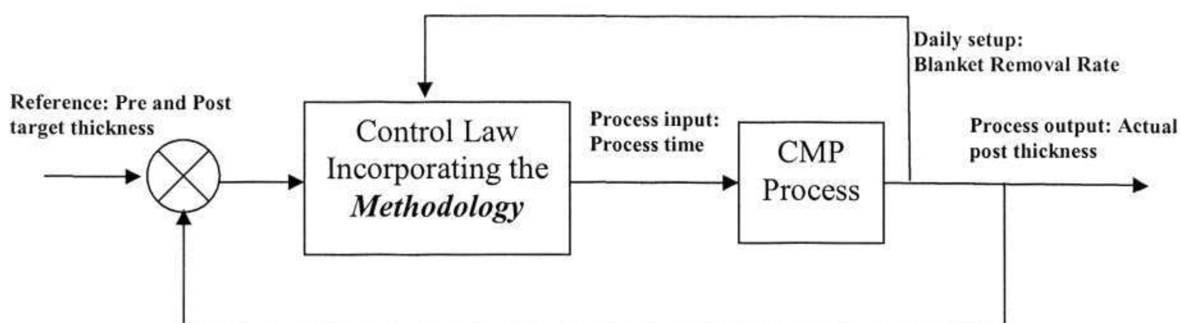

Fig. 4. 24 A simple run-to-run controller for CMP process

The reader is refered to other references [89-92] for the details about the control law and controller design. This run-to-to controller can be integrated under the Advanced Process Control (APC) framework as a component for a fab-wide control which is identified as the approach for future IC fabrication [93, 94] and especially for 300mm wafer fabrication. The control of processes as isolated steps in a manufacturing flow is not adequate for 300mm processing. Rather cooperative control of all operations will ensure manufacturing of optimal products at lower prices [94].

4.5 Potential Issue: Subsurface Stress.

While the CMP process is the enabling technology for multilayer and in-laid architecture in IC fabrication, it also introduced many defects. The most common and prominent defect is scratches [95], which occurred in the region of contact spots

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during CMP process. So far the attention is focused on the quality on the wafer surface, sub-surface stress of the wafer is generated by a large number of different asperity heights (with most the height is above the mean line as shown in figure 4.5) and curvature from polyurethane pad should not be overlooked. Since spherical asperity is assumed, point contact will be discussed in the study. The pressure distribution on this local circular contact spot region of radius r formed by a single asperity can be found in the general form of:

$$P = P_o(1 - \frac{r^2}{a_r^{\ 2}})^n \qquad \textbf{4-24}$$

where P_o is the maximum pressure. The reader should refer to Johnson [96], for details about this pressure distribution. For convenience, n =0.5 is considered, which is given by Hertz theory for elastic contacts [79]. As described in section 4.3, Hertz analysis is used to determine the depth of a penetration for a given applied pressure and the corresponding contact area can be found .Thus, the radius of contact spot region can be expressed as:

$$a_r = \{R(z-d)\}^{\frac{1}{2}} \qquad \textbf{4-25}$$

The stress along the z-axis can be calculated by considering a ring of concentrated force at radius a_r:

$$\frac{\sigma_r}{P_o} = \frac{\sigma_\theta}{P_o} = -(1+\nu)\left\{1 - \left(\frac{z}{a_r}\right)\tan^{-1}\left(\frac{a_r}{z}\right)\right\} + \frac{1}{2}\left(1 + \frac{z^2}{a_r^{\ 2}}\right)^{-1} \qquad \textbf{4-26}$$

$$\frac{\sigma_z}{P_o} = -\left(1 + \frac{z^2}{a_r^{\ 2}}\right)^{-1} \qquad \textbf{4-27}$$

where ν is the Poisson's ratio, σ_r, σ_θ, and σ_z are principal stress along z-axis. The principal shear stress is

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$$\tau_1 = \frac{1}{2}\left|\sigma_r - \sigma_\theta\right| \qquad \textbf{4-28}$$

For the case of ν=0.3, the distribution of stresses below the wafer surface and the contours of principal shear stress are shown in figure 4.25. The contour plot illustrated a specific case. A separation distance of 21μm between wafer and pad is resulted from the corresponding applied pressure of around 32kPa (4.6 psi) as shown in the figure 4.8. The subsurface stress experienced by the locations of the wafer that interact with the heights of the asperities of 23.3μm is shown in this contour plot. The maximum value of $0.31P_o$ occurs at a depth of $0.48a_r$.

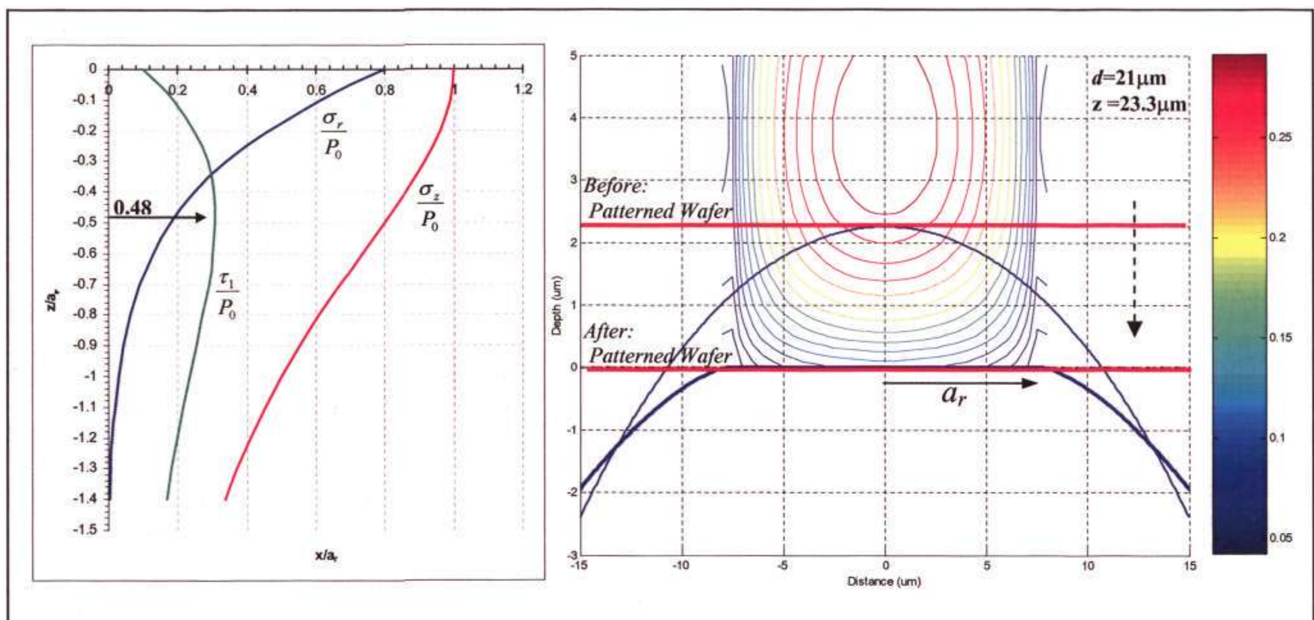

Fig. 4. 25 Principal stress distribution and contours of principal shear stress underneath the wafer surface.

The evidence of seriousness of this subsurface stress are shown in figure 4.26 and figure 4.27. The 4μm AlCu metal line is deposited with 40kÅ HDPCVD oxide followed by 80kÅ PETEOS oxide as the IMD layer. CMP is used to planarize the surface with the post target thickness of 40kÅ. Cracks are found underneath the wafer surface after the CMP process as shown in figure 4.26. Similar defects are also found in another product wafer (refer to figure 4.27) with incoming AlCu metal line of 4μm deposited with 40kÅ HDPCVD oxide followed by 30kÅ PETEOS oxide. Post thickness of 6.5kÅ is obtained after CMP process step. This subsurface cracking is not a critical defect for the IMD layers in terms of functional yield as long as no bridging between the metal lines occurs. However, this theoretical study and

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experimental observation reveals the potential issue in near future IC fabrication for CMP process step.

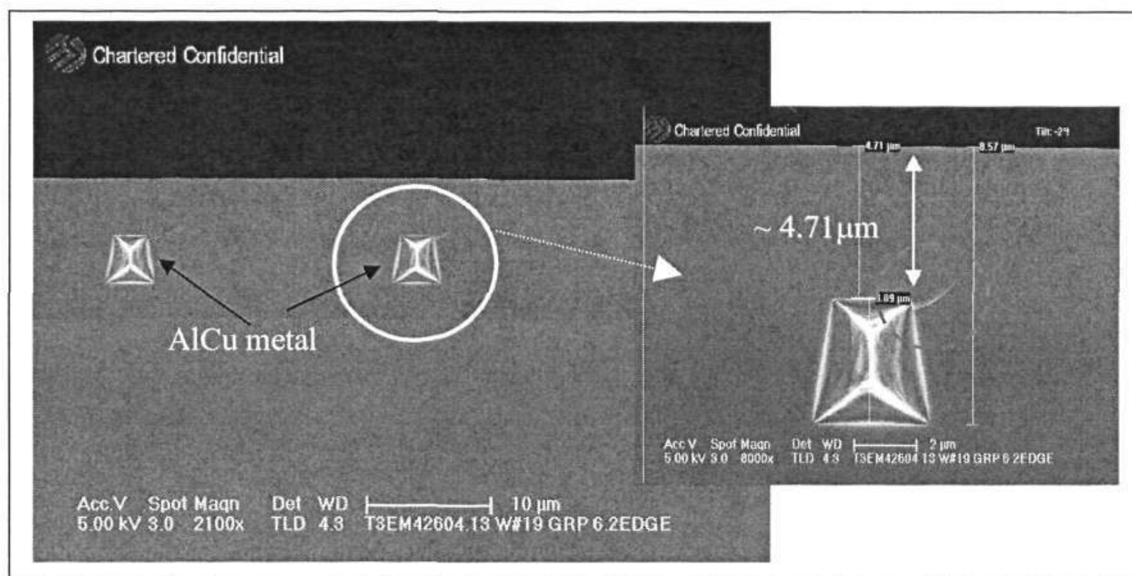

Fig. 4. 26 Cracks are found underneath the wafer surface after CMP process

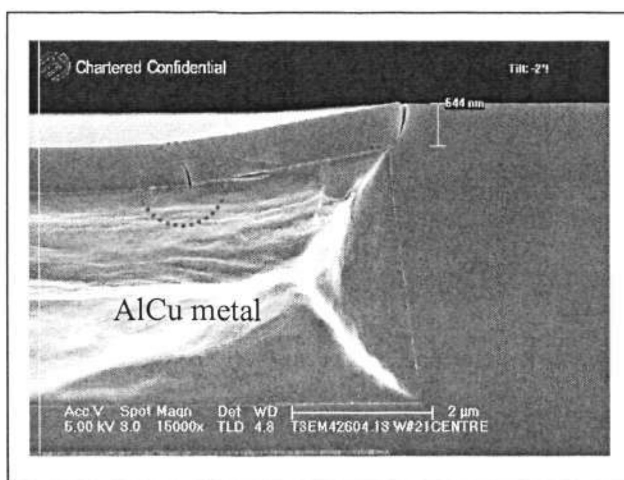

Fig. 4. 27 Cracks are found on both surface and subsurface of the wafer after CMP process

For the front end on line (FEOL), the straining of a silicon crystal (wafer substrate) is a well-known technique to increase charge carrier's mobility and thus enhancing device performance for 65nm or lower technology node [9]. Regardless of the approach whether it is global or local to strain the wafer substrate, the undesired subsurface stress that induced by the CMP especially in ILD CMP process (more closer to the substrate; refer to figure 4.18) might alter the underneath engineering strain layer. As for backend on line (BEOL), the introduction of new low-k dielectric

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materials into copper dual-damascene interconnect structures are a wild card in the CMP deck. Materials that have a low dielectric constant are always accompanied with low mechanical strength. Thus, occurrences of the dielectric collapsing is likely to happen in the conventional CMP process. Although a new architecture of CMP tool is introduced with the capability of achieving a reasonable material removal rate at lower applied pressure [15], subsurface stress is the intrinsic physical phenomenon. The subsurface stress is a great challenge in the success of CMP implantations for advanced IC fabrication.

4.6 Summary

As technology scales, the requirement on better process control for CMP process in IC manufacturing requiring an understanding of the surface interaction. The basic principle of surface interaction between a wafer and a polyurethane pad involves the determination of the real area of contact. Therefore, modeling the CMP process based on the contact mechanics approach is employed to explore the fundamentals. Studies show that applied pressure used in CMP process is to control the real contact area rather than interface pressure. The difference in the separation distance, d, due to the step height on the patterned wafer which leads to a difference in contact pressure at the location of land and trench under a given applied pressure. The knowledge of contact pressure evolution is then extended to an oxide removal rate diagram. Based on this diagram, *BRT* methodology is developed to provide an optimum process time prediction for oxide CMP process. The motivation behind this methodology development is because one of the main concerns in the control of CMP process for IC manufacturing is its capability in producing consistent thin film thickness to provide a more conformal product to downstream operations. However, the inconsistency of the end point detection system in generating a distinguishable curve for determining an appropriate endpoint based on distinct responses (as shown in figure 4.28) yields a wide range of post thickness variations after CMP process. Adjustment table and engineering decision made by tool operators approach are prone to errors. Thus, an alternative approach is needed to address the issue of "How long is needed to *polish* in order to obtain the required thickness?" Promising results are demonstrated by the *BRT* methodology as shown in the experimental data with total sample of around 400 product wafers. Through the contact mechanics modeling

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approach, the issue of subsurface stress is highlighted as a great challenge in CMP process control in near future advanced IC fabrication for both FEOL and BEOL.

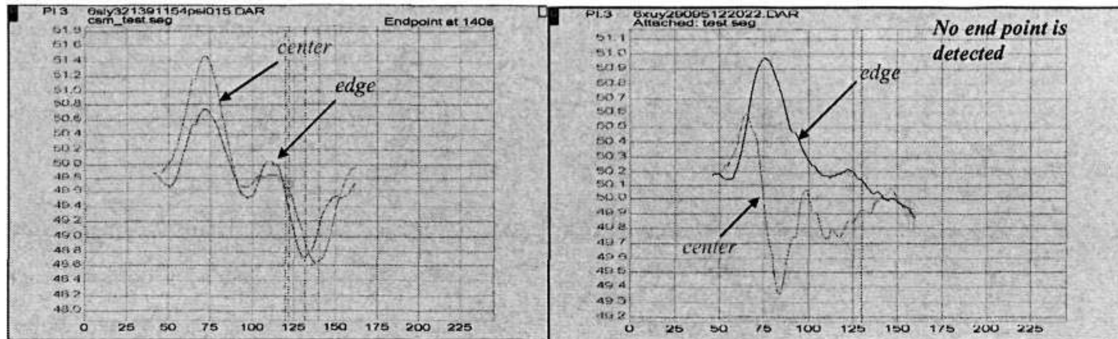

Fig. 4. 28 Unrepeatable end point trace on patterned wafer.

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CHAPTER 5

CONCLUSIONS AND FUTURE WORK

This work has examined a wide range of issues that must be addressed in the CMP process for deep submicron IC fabrication in ULSI, where an integrated circuit (IC) contains over 10 million semiconductor devices per die (or chip). As for 2004, typical chips are of size 1 cm^2 [97]. For example, GeForce FX Go5700, a mobile graphics solution with a very capable processor contains 80million transistors from 0.13 μm technology. As the device shrank beyond submicron (<0.35μm), STI replaced LOCOS as the method of isolation for transistors such that continuation of device miniaturization is possible in order to realize the higher packing density of the IC product as mentioned. These devices are connected together by means of microscopic wires to form circuits. Nearly all MSI (medium-scale integration), LSI (large-scale integration) and earlier generations of VLSI (very large scale integration) used only one level of Al wiring [98]. Today, and near future advanced IC fabrication, multilevel wiring is the way. Multilevel metallization provides greater flexibility in circuit design and even more importantly, a substantial reduction in die size [98]. Both reduction of the device feature length (and related dimensions) and increase in the levels of metallization are driven by speed and size requirements. Hundreds of process steps are needed to fabricate such complex deep submicron IC devices on the silicon wafer substrate. Except the CMP process, these processes have emerged from the numerous manufacturing processes which have evolved since the introduction of transistors in IC such as lithography, etching, implantation and deposition. Only until the 1980s, CMP technology was introduced into the mainstream for the deep submicron IC fabrication. CMP brought about the evolution of the IC to the next level by being the enabling technology for inlaid processes such as STI and multilevel metallization. As the application of CMP is gaining wider for advanced IC fabrication, it is expected to play a key role in semiconductor industry. However, CMP remains one of the least understood areas in IC processing. Due to the many complexities of CMP, controlling the process in a production environment is challenging. This chapter summarizes the main conclusions of the major issues involved with implementation of CMP process in deep submicron IC fabrication which include

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material removal rate, selectivity and repeatability. Future work is also identified for successful integration of the CMP process in near future advanced IC fabrication. The contributions of this thesis to the three important aspects for CMP process in deep submicron IC fabrications are summarized as follows:

i) ***Material Removal Rate***: Inadequacies of existing models in describing the polysilicon removal rate have been revealed. This implies that the empirical model remains the most practical approach to search for the ideal conditions to fulfill the requirement of the material removal rate for a specific process. A versatile empirical material removal rate model is proposed for various material film types.

ii) ***Selectivity***: Implemented the direct STI CMP with ceria based slurry approach on 90nm device fabrication and the characterization results concluded that the feasibility of removing planarization aid: reverse mask + RIE prior to STI CMP process.

iii) ***Repeatability***: A methodology based on the contact mechanics modeling approach to predict the optimum process time for IMD CMP process has been developed, implemented and verified by production line wafer experiments.

Together, this work helps to alleviate some of the challenges associated with the CMP process in deep submicron IC fabrications.

5.1 Material Removal Rate

CMP is a material removal process. The process that is employed to remove undesired topography or to remove excess material to reveal the underlying material in defining the damascene structures. Thus, material removal rate is the primary concern in IC manufacturing. Since the metric affects the throughput, intuitively it should be as high as possible. On the other hand, precise control of the removal thickness is compulsory. Typical average material removal rate for CMP process in IC fabrication is in the range of 2000-5000Å/min which is characterized by the blanket wafer. Due to the imperfection of the process, the variation of the material removal rate across wafer

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and die known as NUWIW and NUWID are inherent. In chapter 2, the impact of various input parameters on CMP performances are systematically reviewed. After the selected tool and consumables are packed together in one process, process control parameters such as rotational speed of both carrier and platen, applied pressure, slurry flow rate and conditional (dressing) conditions are to be determined next to fulfill the specific requirement of the average material removal rate and uniformity. These conditions are obtained through the blanket wafer experiments. Furthermore, controlling of the CMP process for product wafers entails a good understanding of the material removal rate in blanket wafers. Normally, optimum material removal rate and uniformity depend on the combinations of applied pressure and rotational speed. Based on the kinematics simulations for rotary CMP tool, ideally both carrier and platen should have the same magnitude of rotational speed so that the linear relative velocity between center and edge of the wafer is identical for better uniformity performance. The simulation results explained the commonly observed phenomenon in practice where the rotary CMP tool has a better uniformity performance as both carrier and platen are rotated in the same direction. The kinematics model also suggests that with the same set of rotational speed, better uniformity is expected when the higher rotational speed is applied on the carrier component. However, the tradeoff of lower material removal rate is predicted since a smaller magnitude of the linear relative velocity is produced with this configuration. This kinematics simulation describing the nature relative motion of time and position dependence may be also used to understand the fluid flow under the wafer, defects such as scratches, stress and heat generation on the wafer. Other than running the experiments, models might offer an alternative approach to provide input parameters conditions in meeting the requirements of a specific process. Although material removal rate models are becoming increasing predictive as demonstrated in the literature, validation is still critical especially as it is applied to new processes before results obtained from simulations will be considered. This work has evaluated the polysilicon CMP removal rate due to polysilicon becoming the material for filling the deep trenches in BiCMOS IC fabrication and this silicon technology is believed will emerge as an important technology platform for mixed signal system [54]. In addition, lack of information about polysilicon material removal rate as compared to material such as oxide, tungsten and copper. Experimental data has revealed that the inadequacies of the existing models in describing the behavior of polysilicon removal rates on blanket

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wafer as indicated by coefficients of determination, R^2, and suggest that removal rate behavior is sensitive to film types. Based on the results, the removal rate profile across the wafer can be improved by modifying the hole configurations for carrier (figure 2.13). However, no significant difference in material removal rate is observed. This suggests that backside pressure has the greatest impact on uniformity but little effect on the material removal rate. As a bare minimal, a model must be able to predict the trends correctly to be useful for simulating the process in the production environment. Thus, a more general empirical material removal rate is proposed to capture the essence of the observed phenomena for the various film types removal rate in CMP process. While most of the experimental data in the CMP literature support the oxide material removal rate as being proportional to the product of applied pressure and linear relative velocity, the polysilicon material removal rate correlates well with the product of applied pressure by the power of two and linear relative velocity. This model is assessed through cross validation method and the result shows the great predictive ability of the model. This implies that empirical modeling is absolutely essential to offer a means of predicting CMP material removal rate especially for new materials due to the complex interactions of the massive input parameters in the CMP process which make the physical basis not well understood. The model summarizes some representative existing works and serves as a guide for the practical prediction of material removal rate for various film types in IC fabrication. The main conclusion is any attempt to predict the material removal rate without conducting the experiments is likely to fail or the deviation is far beyond the acceptance region for the precise fabrication in IC manufacturing.

5.2 Selectivity

CMP is an enabling technology for the inlaid process in deep submicron IC fabrication such as STI and copper damascenes interconnects. STI replaced LOCOS as an isolation alternative due to STI being scalable for devices smaller than 0.35μm. The ratio of the materials removal rate (removal selectivity) is the prime concern in fabricating single damascenes structures on the wafer substrate since there are two different type of materials i.e. nitride and oxide are involved in the removal process. Unlike other inlaid processes in IC fabrication, planarization aids such as reverse mask and RIE are needed prior to STI CMP due to the low selectivity and poor

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planarization of conventional silica based slurry to reduce nitride loss and dishing. In addition, inability to effectively planarize the oxide after a trench is filled and stopping on nitride layer over wide range of pattern density variations and die layout will lead to a high range of variation in the oxide and nitride thickness. Thus, the issue of selectivity in implementing the STI CMP for deep submicron devices fabrications is addressed in chapter 3. Two different process schemes for STI CMP are studied namely reverse mask prior to CMP with silica based slurry and direct STI CMP with ceria based slurry. This work demonstrated the feasibility of implementing the direct STI CMP process since every manufacturing step is driven by the desire to achieve the lowest cost and the removal of non-value-added operations. This conclusion is supported by the characterization results that covered a wide range of the performance metrics. Nitride thickness becomes more critical for gapfill in STI process due to the high aspect ratio result from narrow and deep trench as features sizes become smaller and denser. In addition, as gate geometry continues to shrink non-uniformity should be low enough to meet the DOF for the deep submicron gate patterning process. Experimental data shows that around a 73% reduction in NUWIW with the range of nitride thickness around 60Å by ceria based slurry as compared to silica based slurry which results in a typical value that more than 100Å. In general, it is not practical to restrict the circuit functional layout design in order to narrow down the pattern density in the circuit just to cater for the performance of NUWID in the CMP process. As for NUWID, the direct STI CMP process shows around a 70% improvement for nitride thickness variation over a wide range of STI structure dimensions. Both center and edge die show less than 50Å difference in nitride thickness range. Whereas, the mean nitride thickness value for the reverse mask process is around 600Å with the range that is greater than 100Å. The emphasize for the need of uniformity of trench oxide is reported due to the narrow width effects which are caused by the STI oxide step height. The direct STI CMP process achieved a relatively better trench oxide uniformity across the wafer as compared to silica based slurry. Unlike NUWID for nitride, trench oxide thickness is relatively sensitive to the dimension in direct STI CMP with ceria based slurry. However, less oxide thickness loss between small and large trenches as compared to the reverse mask with silica based slurry process. The performance for both nitride and oxide thickness within wafer and die is confirmed with additional runs and similar results are reported. Dishing in the isolation trench may affect implant depth and degrade the transistor performance. Ceria based slurry

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offers significant improvements in dishing over conventional silica slurry. Results from HRP characterization shows that dishing reduces to below 300Å even with additional process time as compared to the conventional silica based slurry which varies up to 700Å. Furthermore, more than a 80% reduction in dishing at the trench size of 0.4μm or less is observed through the cross SEM pictures. The excellent planarization performance with ceria based slurry is reflected in the significant reduction in STI elevation variation which is less than 100Å from wide trench to narrow trench. Surface roughness is also important because it indicates defects associated with scratching, and it also affects the morphology, and thus reliability of subsequently deposited layers. AFM results indicate that a relatively smooth surface is obtained by using ceria based slurry. In addition to the performance of as mentioned, the mobile ions are one of crucial parameters that influence the electrical properties especially in the FEOL process like STI. The main source of the mobile ions is related to the inherent properties of the slurry. Therefore TXRF is used for direct STI CMP with ceria based slurry evaluation and result shows that with the conventional post clean method after CMP process, it is able to keep metallic contamination level to less than 20×10^{10} atoms/cm^2. This selectivity characterization work is performed on the 90nm manufacturing standard test chip design. The great performance of the direct STI CMP with ceria based slurry process is verified by the electrical results. Higher threshold voltage and drive current and lower leakage is obtained. The main advantages of ceria based slurry over silica-based slurry are high selectivity and high planarization capability. These enable the removal process to achieve minimum nitride loss during the additional processing time, as it is needed to ensure the oxide film is clear on the active area for a wide range of pattern densities while at the same time retaining good planarity over the wafer.

5.3 Repeatability

Whether CMP is applied for inlaid or multilayer fabrication, maintain consistency of the thin film thickness for each product wafers is not only the demand of the downstream process but also to ensure high yield and cost effectiveness of the overall operation in making the IC. This prevents needless cycle time from accruing for rework and wafer to be scrapped due to thickness is out of specifications. Like it or not, the problem of integrating the robust real time thickness measurement associated

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with the nature of the CMP process make it unfeasible. In order to properly control the thin film thickness produced by the CMP process, a fundamental understanding of the process is essential. As empirical modeling is effective in providing the process conditions for the desired material removal rate as reported in chapter 2, a better control of a CMP process under specific process conditions demands a basic understanding of the interface between the wafer and polyurethane pad Therefore, in chapter 4, a contact mechanics modeling approach is employed to explore locally relevant information regarding a chosen process conditions and *BRT* methodology is developed based on this premise to address the repeatability issue and enabling better thickness control for CMP process. The methodology has been experimentally verified and promising results are demonstrated. Large number of factors and variables interactions to be treated in order to cover every consideration in one model to predict the exact material removal rate on the patterned wafer, which is impractical and beyond the scope of this thesis. Thus, in this work the treatment is limited to solid-solid contact between wafer and pad to capture the essence of the process behavior. The fundamental problem under elastic contact condition is investigated through the contact mechanics modeling approach. The separation distance and real contact area at the interface over a wide range of the applied pressure is theoretical estimated by incorporating the commercial polyurethane pad surface characterization results into Hertz's theory. In a typical applied pressure condition for the CMP process, around 20μm range separation distance exists between wafer and polyurethane pad and the corresponding real contact area ratio is less than 1%. The model suggested that interface pressure has almost 4 times the order of magnitude higher than the typical applied pressure of 3 to 5 psi (~20-35kPa). However, simulation results show that the applied pressure in CMP process is to control the real contact area rather than interface pressure since an increase in applied pressure result in a significant increase of contact area as compared to the latter. Due to the step height on the patterned wafer, the difference in the interface pressure at trench and land exists which is caused by the contact area at these two locations from the two distinct separation distances. The respective separation values depend on the area fraction of both trench and land on the patterned wafer. For a perfect planarization case, simulation results show that eventually both trench and land having an identical separation distance as in blanket wafer under the same magnitude of the applied pressure which is as expected. Based on this premise, a hypothesis of material

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removal rate evolution on the patterned wafer is suggested for ILD or IMD CMP process and *BRT* methodology is then developed to provide the optimum process time prediction to reduce wafer to wafer thickness variation for the IMD process. Maintaining a consistent thickness of IMD layers is a relatively challenging task as compared to fabricating the damascene structures. As demonstrated by high selectivity slurry by ceria based slurry for STI CMP process, the nitride thickness remained within a tight range even with additional process time. However, wafer to wafer thickness variation for ILD or IMD is significantly affected by the process time. The parameter of *BRT* is designed to capture all the complicated coupling effects of the process variables which can be determined after the post thickness of the patterned wafer measurement is taken. Finally, the optimum time calculated for the next wafer is based on the information of *BRT*, incoming thickness and blanket material removal rate. Both offline and online results from a total of 250 product wafer experiment demonstrated that better process control is achieved and *wafer-to-wafer* thickness variation is reduced as reflected in both C_p and C_{pk} values of around 1.2. In addition, this experiment is performed on various devices and layers showing that *BRT* methodology is not restricted by the pattern density due to different IC layout. This methodology provides several benefits. First, no additional characterization mask or instrument need to be employed to extract the required parameters. Secondly, it provides a high degree of ease of use and flexibility in a production environment. Thirdly, it can be integrated into a run-to-run control design to enhance the process performances. Four, instead of a particular fixed time being employed, this methodology can work in conjunction with the end-point detection system in providing the variable additional process time after the end point signal is received.

5.4 Future Work

Beyond the three important issues as mentioned, near future advanced IC fabrication trend: strained silicon in fabricating the transistors at FEOL and low-k interconnects architecture at BEOL placed another challenging matter that need to be addressed for successful implementation of CMP process. Subsurface stress induced by the nature of CMP process as qualitative described in the last section of the chapter 4 is a potential issue for both emerging technology in advanced IC fabrications.

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PUBLICATIONS & INVENTIONS

List of Publications

1. **Wang, S.K**. and Butler, D.L. *A Methodology To Reduce Wafer to Wafer Thickness Variation In CMP*. in *World Tribology Congress III*. September 2005. Washington,D.C.

2. **Wang, S.K**., Liu, D.S., Chen, F., and Butler, D.L. *The Evaluation and Modeling of the Chemical Mechanical Planarization (CMP) Removal Rate for Polysilicon*. in *Thin Films & Nanotech 2004*. July 2004. Singapore.

3. **Wang, S.K.**, Lim, C.G., Chen, F., and Butler, D.L. *Couple effect of largest ceria abrasive size and pressure on direct STI CMP*. in *Symposium on Microelectronics 2004*. June 2004. Singapore.

4. **Wang, S.K**., Chen, F., Lim, C.G., and Butler, D.L. *Effect of Polymer in Ceria based Slurry on CMP Removal Rate*. in *AVS Fifth International Conference on Microelectronics and Interfaces*. March 2004. San Francisco.

5. Chen, F., **Wang, S.K**., Lim, C.G., Chen, H.H.D., Lau, A., Lee, R., Goh, E., and Butler, D.L. *Direct STI CMP with Ceria Based Slurry for 90nm Technology*. in *19th International VLSI Multilevel Interconnection Conference (VMIC) 2002*. November 2002. Singapore.

List of Inventions

1. Chen, F., Lim, C.G., and **Wang, S.K**., *A novel method to reduce microscratches on wafer in the polisher*. September 2002, accepted as company (Chartered Semiconductor Manufacturing Ltd) trade secret.

2. Chen, F., Lim, C.G., Leong, L.S., and **Wang, S.K**., *CMP Polishing Heads Retaining Ring Groove Design for Mircoscratch Reduction*. September 2003, DRAFT Patent application Reference CS03-039.

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APPENDIX A:

CS03-039,

CMP Polishing Heads Retaining Ring Groove Design for Microscratch Reduction

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1 **CMP Polishing Heads Retaining Ring Groove Design for Microscratch Reduction**

2

3 **Background of Invention**

4 **1) Field of the Invention**

5 Embodiments of this invention relate to Chemical Mechanical

6 Polishing (CMPing) methods and machines, and particularly to retaining ring designs for

7 CMP heads and more particularly to particularly to retaining ring designs with curved

8 grooves for reducing Microscatches on semiconductor structures.

9

10 **2) Description of the Related Art**

11 In semiconductor fabrications, the chemical-mechanical polish (CMP)

12 technique is widely used for the global planarization of semiconductor wafers that are used

13 for the fabrication of VLSI (very large-scale integration) and ULSI (ultra large-scale

14 integration) integrated circuits.

15 FIGS. 1A and 1B are schematic diagrams showing a conventional CMP

16 machine. The CMP machine comprises a polishing table 10 on which a polishing pad 12 is

17 layered, a polishing head 14 for holding a semiconductor wafer 16 in position, and a nozzle

18 18 for applying a mass of slurry to the semiconductor wafer 16 during the CMP process.

19

20 FIG. 1C shows a respective view of the structure inside of the polishing

21 head 14. As shown, the polishing head 14 includes an air-pressure means 20 which applies

22 air pressure to a wafer loader 22 used to hold the wafer 16. In addition, a retainer ring 24 is

23 mounted around the loader 22 and the wafer 16, which can retain the wafer 16 in fixed

24 position during the CMP process. Moreover, a cushion pad (not shown) is placed between

25 the wafer 16 and the loader 22.

26 A problem of current chemical-mechanical polish (CMP) machines and

27 process is the micro-scratches formed on the substrate during the CMP process.

28

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1 The importance of overcoming the various deficiencies noted above is
2 evidenced by the extensive technological development directed to the subject, as
3 documented by the relevant patent and technical literature. The closest and apparently
4 more relevant technical developments in the patent literature can be gleaned by considering
5 US 6,386,962(Gotkis et al.) shows a wafer carrier with retainer ring for a chemical-
6 mechanical polish (CMP) apparatus.
7 US 6,527,624 B1(Tollers et al.) shows a retaining ring having a trough
8 and one or more channels to channel the slurry to the pad. See e.g., figures 2-6.
9 US 6,110,025(Williams et al.) teaches a retainer ring with passages. See
10 fig 13.
11 US 6,293,850 B1(Lin et al.) shows retaining ring with slurry passages
12 at the bottom of the retainer ring.
13 US 6,224,472 B1(Lai et al.) teaches a retaining ring with channels.
14
15 However, the retaining rings can be further improved.

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1

2 **Summary of the Invention**

3 It is an object of example embodiments of the present invention to
4 provide a retaining ring for use in a chemical-mechanical polish (CMP) machine.
5
6 It is an object of example embodiments of the present invention to
7 provide CMP method and a retaining ring having channels with rounded edges or curved
8 surfaces for use in a chemical-mechanical polish (CMP) machine.
9
10 To accomplish the above objectives, an embodiment of the present
11 invention provides a retaining ring which is characterized :
12
13
14 [A complete summary of the invention will be written when this draft is
15 returned.]
16
17
18 The above advantages and features are of representative embodiments
19 only, and are not exhaustive and/or exclusive. They are presented only to assist in
20 understanding the invention. It should be understood that they are not representative of all
21 the inventions defined by the claims, to be considered limitations on the invention as
22 defined by the claims, or limitations on equivalents to the claims. For instance, some of
23 these advantages may be mutually contradictory, in that they cannot be simultaneously
24 present in a single embodiment. Similarly, some advantages are applicable to one aspect of
25 the invention, and inapplicable to others. Furthermore, certain aspects of the claimed
26 invention have not been discussed herein. However, no inference should be drawn
27 regarding those discussed herein relative to those not discussed herein other than for
28 purposes of space and reducing repetition. Thus, this summary of features and advantages

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1 should not be considered dispositive in determining equivalence. Additional features and
2 advantages of the invention will become apparent in the following description, from the
3 drawings, and from the claims.

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1

2 **Brief Description of the Drawings**

3 The features and advantages of a retaining ring and methods thereof
4 according to example embodiments the present invention will be more clearly understood
5 from the following description taken in conjunction with the accompanying drawings in
6 which like reference numerals designate similar or corresponding elements, regions and
7 portions and in which:

8 Figure 1A is a schematic top view of a chemical-mechanical polish
9 (CMP) machine for performing a CMP process on a semiconductor wafer according to the
10 prior art.

11 Figure 1B is a schematic section view of the chemical-mechanical
12 polish (CMP) machine of figure 1A according to the prior art.

13 Figure 1C is a cross sectional view showing an inside structure of the
14 polishing head used on the CMP machine of figures 1A and 1B according to the prior art.

15 Figure 2A is perspective view of a retaining ring having rectangular
16 grooves 204.

17 Figure 2B is a close up perspective view a groove in the a retaining ring
18 having rectangular grooves 204 as shown in figure 2A.

19 Figure 2C is a cross sectional view of a groove that has slurry particles
20 that cause the problems as discovered by the inventors.

21 Figure 3A is perspective view of a retaining ring that has non-
22 rectangular grooves 304 according to an aspect of the invention.

23 Figure 3B is a close up perspective view of an embodiment where the
24 groove has a semicircle profile according to an aspect of the invention.

25 Figure 3C is a cross sectional view of a groove that has a semicircle
26 profile according to an aspect of the invention.

27 Figure 3D is a cross sectional view of a groove that has rounded or
28 curved or non-angular bottom corners according to an aspect of the invention.

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1 Figure 3C is a cross sectional view of a groove that has a semicircle
2 profile according to an aspect of the invention.
3 Figure 4A is perspective view of a retaining ring that has non-
4 rectangular grooves 404 and curved top corners according to an aspect of the invention.
5 Figure 4B is a close up perspective view of an embodiment where the
6 groove has curved top corners according to an aspect of the invention.
7 Figure 3C is a cross sectional view of a groove that has a semicircle
8 profile and curved top corners according to an aspect of the invention.
9 Figure 4D is cross sectional view of a retaining ring that has a
10 rectangular groove 404D and curved top corners according to an aspect of the invention.
11
12

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1 **Detailed Description of the Preferred Embodiments**

2

Please add comments to make the invention broader. Such as different curved groove shapes.

Please write down Low and High ranges (for example ___ to ___) for all parameters that you wish to claim. Without a range, we can not claim a parameter.

3

Dear Inventor,

The "Detailed Description of preferred embodiments" section below must have information to met the following two legal requirements: (1) enablement and (2) best mode.

- For (1) enablement - This section should be written so that if your colleagues read this patent, they would be able (e.g., enable) to practice this invention. Therefore, please add any information/description necessary to enable someone to perform the invention . **Please add any information even if there are no questions.**
- For (2) best mode – We must disclose the best way to perform the invention - Therefore Please add any parameters that are important.
    - For critical parameters, please give 3 ranges : 1) preferred, 2) more preferred and 3) optimum parameters and please explain why they are preferred.
- Please contact me if you have any questions: bill_stoffel@yahoo.com

4 ***A. Slurry in groove can cause micro scratches***

5 Referring now to the drawings and more particularly to Figures 2A,
6 2B, and 2C there is shown a retaining ring 200 over which the aspects of the present
7 invention are an improvement. It is to be understood in this regard that no portion of
8 Figures 2A, 2B and 2C is admitted to be prior art as to the present invention. Rather, this
9 these diagrams are an effort to provide an improved understanding of some of the
10 problems that are overcome by the invention.

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1 Figure 2A is perspective view of a retaining ring 200 having rectangular
2 shaped grooves 204. The ring has a lower surface 201 (polishing surface or pad side
3 surface) that in operation faces the polish pad.
4 Figure 2B is a close up perspective view a groove 204 that has non-
5 curved corners or edges in the a retaining ring 200.
6 Figure 2C is a cross sectional view of a groove 204 that has slurry
7 particles 208 that cause the problems as discovered by the inventors.
8 Microscratches are a defect caused by the CMP process. Many efforts
9 have been made by the CMP pundits to reduce the level of microscratches. Big particles
10 and/or dry slurry are causes of the microscrathes. Big particle size can be control by
11 filtration in the supplier's factory and the dried slurry is had material normally found the
12 in-house slurry delivery related components. The forming of dried slurry can occur when
13 the water vaporizes from the slurry droplet spilled on the surface of some polishing
14 machine components.
15 The inventors have found that the retaining ring in the chemical-
16 mechanical polish (CMP) machine is a source of dried slurry. As shown in figure 2C, the
17 corner of the groove of the wafer polishing head's retaining ring was found to accumulate
18 a few chunks of dried slurry. A purpose of these grooves is to allow the slurry flow in to
19 the wafer polishing head for efficient planarization process. Unfortunately, the design of
20 the current retaining ring grooves can cause slurry particles to accumulate and increase
21 micro scratches.
22

23 ***B. Example embodiments of the grooves of the invention***

24 Example embodiments of the grooves of the invention have at least a
25 portion of the groove surface that is curved. Examples of curvilinear portion of groove are:
26 semicircle shaped grooves, groves with rounded bottom corners, grooves with rounded top
27 corners, grooves with curved sidewalls and combinations thereof. The example

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1 embodiment of the grooves reduce the buildup of dried slurry in grooves and thus reduce
2 microscratches.

Expanded scope of the invention

Dear Inventor – based on the problem you described of slurry particles getting caught in "angled" groove surfaces, I include many examples of different grooves that have at least one rounded surface (in addition to the 2 examples (figs 3C and 4C) in the invention disclosure. See figure 3D, 3E, 3F, 4C, and 4D,

Please add any other examples of groove shapes that are appropriate. Please let me know if any of the grooves shown in the figs will not work.

If you have any questions, please contact me at bill_stoffel@yahoo.com

3
4
5 As shown in figure 3A, a chemical-mechanical polish (CMP) retaining
6 ring comprises: an inner peripheral surface 303; an outer peripheral surface 301; a lower
7 surface 301. The lower surface 301 is adapted to contact and depress an upper surface of a
8 polishing pad during chemical mechanical polishing of a lower surface of a substrate
9 contained within the inner peripheral surface of the retaining ring during chemical
10 mechanical polishing.
11 The retaining ring 300 has grooves 304 on the lower surface 301. The
12 grooves 304 preferably extend from a position at or adjacent the inner peripheral surface of
13 the retaining ring, to a position at or adjacent the outer peripheral surface of the retaining
14 ring. **At least a portion of the groove 304 has a rounded contour.**
15 The term "rounded" can mean: curved, or with curved parts: having
16 curved, not straight or angular, surfaces or edges.
17
18 The grooves do not have to have the same cross sectional area along the
19 length of the groove. The grooves can have a depth between ___ and ____

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1
2 Figure 3B shows a closer view of a preferred embodiment of the
3 invention where the groove 304C has a semicircle profile.
4
5 Figure 3C shows a cross sectional view of a groove 304C that has a
6 semicircle profile 301 with a radius 311. The grooves 304C have a semicircle profile
7 preferably with a radius between ___ and___ . The semicircle profile of the groove helps
8 prevent the slurry particles from accumulating in the groove.
9 **Q. please add any comments about fig 3C. ___**
10
11 In the aspect shown in figure 3D, the groove 304D has curved sidewalls
12 316 and a rounded bottom corner 312 and a flat bottom 314. The grooves can have at
13 least one rounded corner. The grooves have rounded edges 312 adjacent to the bottom
14 314 of the grooves. The rounded edges or surfaces 312 can prevent slurry form
15 accumulating in the groove.
16 In an aspect, the retaining ring has grooves with rounded top edges
17 adjacent to the lower surface 301 of the retaining ring.
18
19 Referring to figure 3E, the groove 304E has a rounded top corner 320
20 near the lower surface of the ring. The groove has a sloped sidewall 322. The groove has a
21 rounded bottom corner 311 and a flat 316 bottom. The bottom can be flat or curved.
22 In an aspect shown in figure 3F, the CMP retaining ring has a groove
23 has with about vertical sidewalls 330 and an about horizontal flat bottom 316 and at least
24 one rounded corner 311 between the vertical sidewalls 330 and the horizontal bottom
25 316. The grooves can have a width between ___ and ____
26
27 Figure 4A shows another embodiment where the groove 404 has top
28 edge with a curved shape.

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1 Figure 4B shows a perspective view of the groove 404 with the rounded
2 top corner 420. In the aspect shown in figure 4B and 4C the groove has a semicircle profile
3 and top rounded corners.
4 Figure 4C shows a preferred embodiment of the invention of a groove
5 404C with rounded top corners 420 and a semicircle profile 410. In an option, the rounder
6 top corners can be formed from a arc of a circle having a radius 411.
7 **Q.- Inventor - please add any comments**
8 In an aspect shown in figure 4D, the groove 404D has a rounded top
9 corners 420 and vertical sidewalls, about right angled bottom corners and a bottom 430.
10
11 The retaining ring can have other channels on the lower surface. Also,
12 the lower surface of the retaining ring can further comprise a plurality of protrusions and
13 recesses or a mixture of both. In addition, the retaining ring can have other passages thru
14 the ring such as a passage connecting the grooves to the top side of the ring. See e.g., US
15 6,527,624 B1.
16 It will be understood that CMP retaining rings embodiments of the
17 invention may be advantageously used with any type of CMP polishing system, pad
18 material and/or polishing slurry, such as where the lower (or pad-side) surface of the
19 retaining ring contacts the polishing pad during polishing. Examples of suitable CMP
20 slurries include, but are not limited to, Cabot "SS25", Cabot "SS12",
21 ________________________________ etc.
22 It should be noted that the retaining ring and wafer carriers of the
23 present invention may be used with any suitable CMP systems such as linear CMP
24 apparatus or rotary CMP apparatus.

25 ***C. Example and supporting data***

26 **Inventor – if available please include any data showing how the**
27 **rounded grooves of the invention actually reduced microscraches.**

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1 **Inventor** – is there a certain slurry particle size, slurry type or chemical-
2 mechanical polish (CMP) process that is extra sensitive to Slurry accumulation problem in
3 the grooves?
4 Please describe the process/problem including parameters. Eg.
5 thickness of retaining ring, width of groove, size wafer, CMP step e.g., metal CMP, etc.....
6 If possible give data showing that the invention's grooves improved the problem.
7
8
9 Please add any additional benefits.
10
11
12 In the above description numerous specific details are set forth in order
13 to provide a more thorough understanding of the present invention. It will be obvious,
14 however, to one skilled in the art that the present invention may be practiced without these
15 details. In other instances, well known process have not been described in detail in order
16 to not unnecessarily obscure the present invention.
17 Given the variety of embodiments of the present invention just
18 described, the above description and illustrations show not be taken as limiting the scope
19 of the present invention defined by the claims.
20 While the invention has been particularly shown and described with
21 reference to the preferred embodiments thereof, it will be understood by those skilled in
22 the art that various changes in form and details may be made without departing from the
23 spirit and scope of the invention. It is intended to cover various modifications and similar
24 arrangements and procedures, and the scope of the appended claims therefore should be
25 accorded the broadest interpretation so as to encompass all such modifications and similar
26 arrangements and procedures.
27

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Note: The element numbers and figure number in the claims will be removed for the final patent application. The element numbers are only to make it easier to understand the claims for the draft.

.

What is claimed is:

1 1. A CMP retaining ring, comprising:
2 an inner peripheral surface;
3 an outer peripheral surface;
4 a lower surface adapted to contact and depress an upper surface of a polishing pad
5 during chemical mechanical polishing of a lower surface of a substrate; said substrate is
6 contained within said inner peripheral surface of said retaining ring during chemical
7 mechanical polishing; and
8 at least a groove on said lower surface of said retaining ring and extending from a
9 position at or adjacent said inner peripheral surface of said retaining ring, to a position
10 at or adjacent said outer peripheral surface of said retaining ring;
11 at least a portion of said groove has a rounded contour.
12
13 2. The CMP retaining ring of claim 1 wherein said groove 304A has a semicircle
14 profile.
15 3. The CMP retaining ring of claim 1 wherein said groove has a semicircle profile
16 and said groove has a rounded profile adjacent to the lower surface of the retaining ring.
17 4. figure 3C - The CMP retaining ring of claim 1 wherein said groove has a
18 semicircle profile with a radius between ___ and___ .
19 5. The CMP retaining ring of claim 1 wherein said groove has at least one rounded
20 corner.

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21 6. The CMP retaining ring of claim 1 wherein said grooves have at least one rounded
22 bottom corner.
23 7. figures 3D and 3E - The CMP retaining ring of claim 1 wherein said groove has
24 rounded edges adjacent to the bottom of said grooves.
25 8. The CMP retaining ring of claim 1 wherein said groove has rounded top edges
26 320 420 adjacent to the lower surface 301 of said retaining ring.
27
28 9. The CMP retaining ring of claim 1 wherein the cross sectional area of said groove
29 changes along the length of said groove.
30 10. The CMP retaining ring of claim 1 wherein said groove has a width between ___
31 and ____ ; said groove has a depth between ___ and ____
32 11. The CMP retaining ring of claim 1 wherein grooves have vertical sidewalls or
33 sloped sidewalls.
34 12. figure 3F - The CMP retaining ring of claim 1 wherein said groove has vertical
35 sidewalls and an about horizontal bottom and at least one rounded corner between said
36 vertical sidewalls and said horizontal bottom.
37 13. fig 3F - The CMP retaining ring of claim 1 wherein said groove has straight
38 sidewalls and top and bottom corners; at least one of said corners is rounded or
39 curvilinear.
40 14. The CMP retaining ring of claim 1 wherein said retaining ring can further comprise
41 other channels; the lower surface of the retaining ring can further comprise a plurality of
42 protrusions and recesses or a mixture of both.
43
44 15. (process) A process for chemical-mechanical polish (CMP) a wafer comprising:
45 said wafer is disposed within a polishing head with the deposition layer
46 facing down a polishing table; said wafer is retained within the polishing head by a
47 retainer ring, and at least a portion of said groove has a rounded contour.

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48 supplying a slurry a slurry supplier to be evenly distributed over the
49 deposition layer through the retainer ring;
50 rotating said polishing table and spinning said polishing head to
51 chemically polish said wafer.
52 16. The process of claim 15 which further includes: forming a deposition layer on the
53 surface of said wafer and chemical mechanically polishing said deposition layer.
54 17. The process of claim 15 wherein said groove 304A has a semicircle profile.
55 18. The process of claim 15 wherein said groove 304A has a semicircle profile and
56 said groove has a rounded profile adjacent to the lower surface of the retaining ring.
57 19. The process of claim 15 wherein said groove has at least one rounded corner.
58 20. The process of claim 15 wherein said grooves has at least one rounded bottom
59 corner.
60 21. The process of claim 15 wherein said groove has rounded edges adjacent to the
61 bottom of said grooves.
62 22. The process of claim 15 wherein said groove has rounded top edges 320 420
63 adjacent to the lower surface 301 of said retaining ring.
64 23. The process of claim 15 wherein said groove has a width between ___ and ____
65 said groove has a depth between ___ and ____
66
67
68

24. Q.- Inventor - is there anything else to claim. ?

25. Note - more claims will be written when the draft is returned.

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CMP Polishing Head Retaining Ring Groove Design for Microscratch Reduction

Abstract

A chemical-mechanical polish (CMP) machine and fabrication process using the same. The CMP machine has a CMP retaining ring, comprising: an inner peripheral surface; an outer peripheral surface; a lower surface adapted to contact and depress an upper surface of a polishing pad during chemical mechanical polishing of a lower surface of a substrate. The substrate is contained within said inner peripheral surface of said retaining ring during chemical mechanical polishing. At least a groove on said lower surface of said retaining ring . At least a portion of said groove has a rounded contour. In an aspect, the groove has a semicircle profile. In another aspect, the groove has a semicircle profile and a curved profile at adjacent to the lower surface of the retaining ring. The retaining ring with a curved portion reduces the accumulation of dried slurry and thus reduces micro-scratches.

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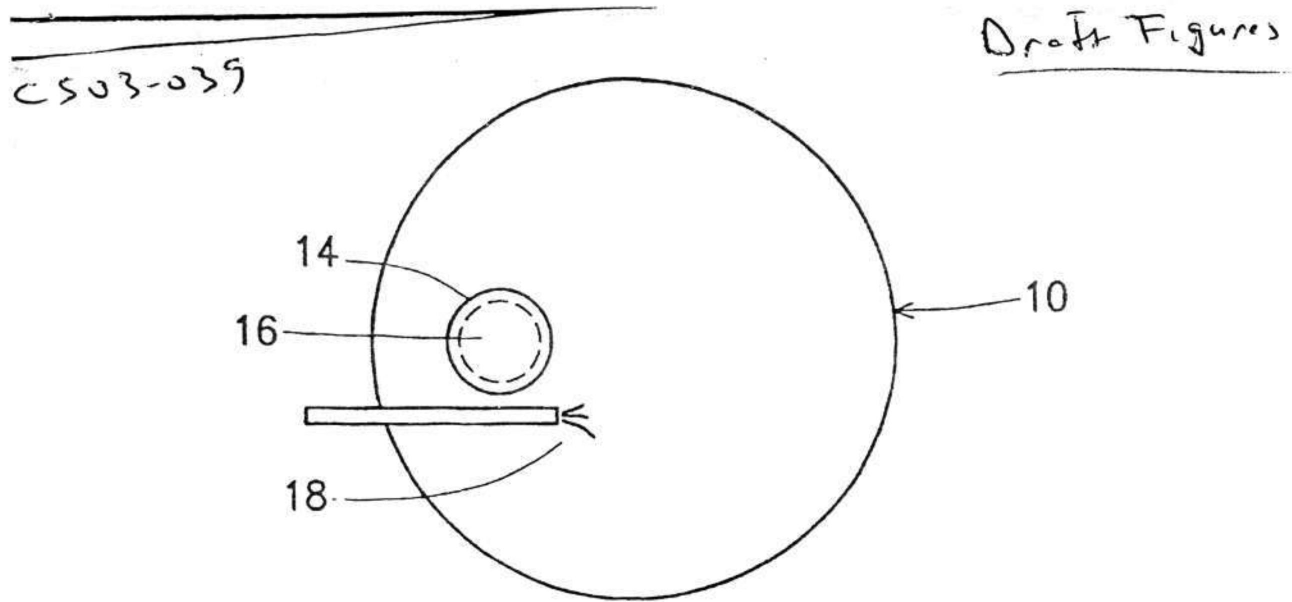

FIG. 1A (PRIOR ART)

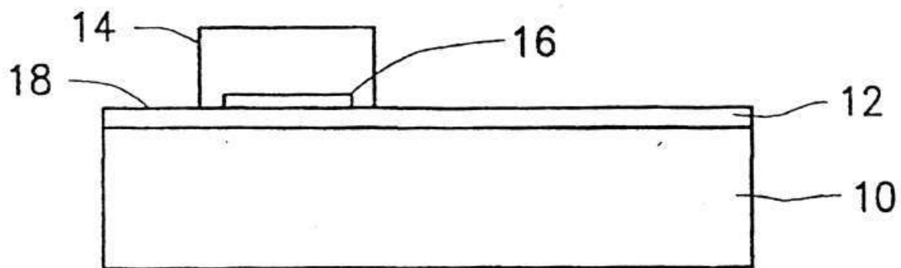

FIG. 1B (PRIOR ART)

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-S03-039

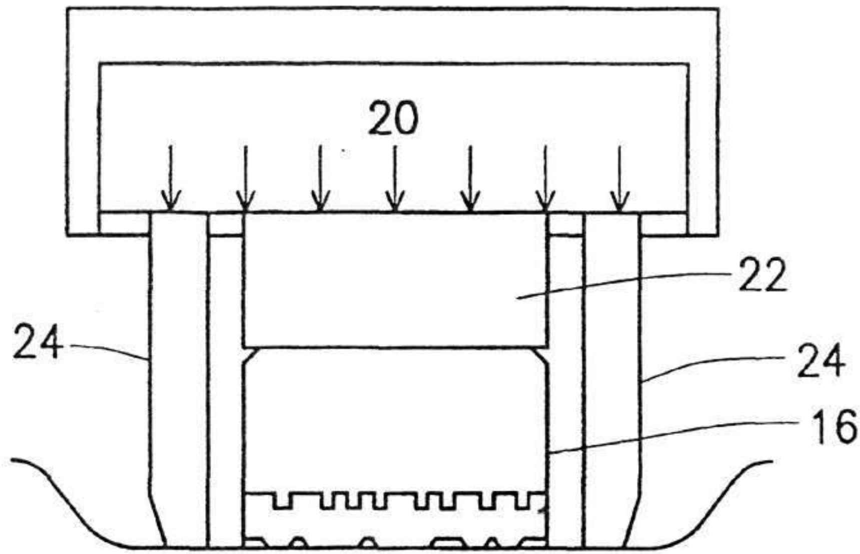

FIG. 1C (PRIOR ART)

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Chartered
semiconductor manufacturing

Original Design

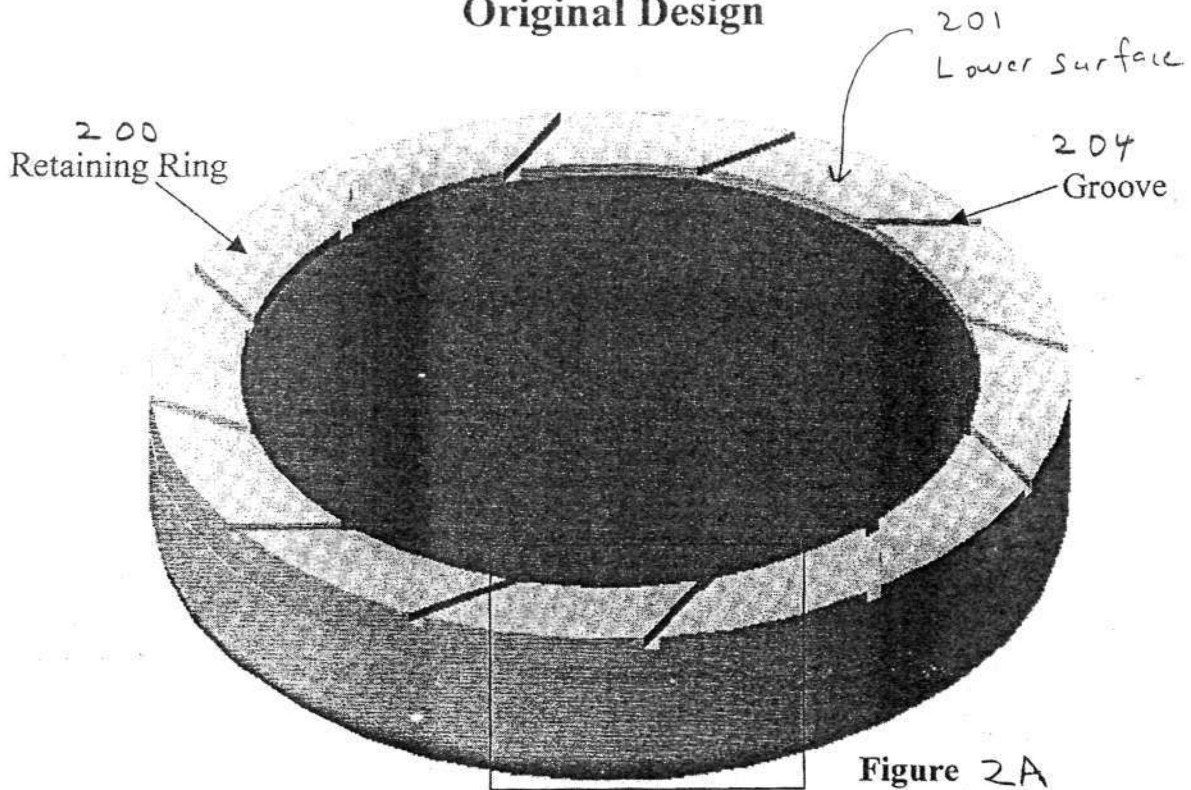

Figure 2A

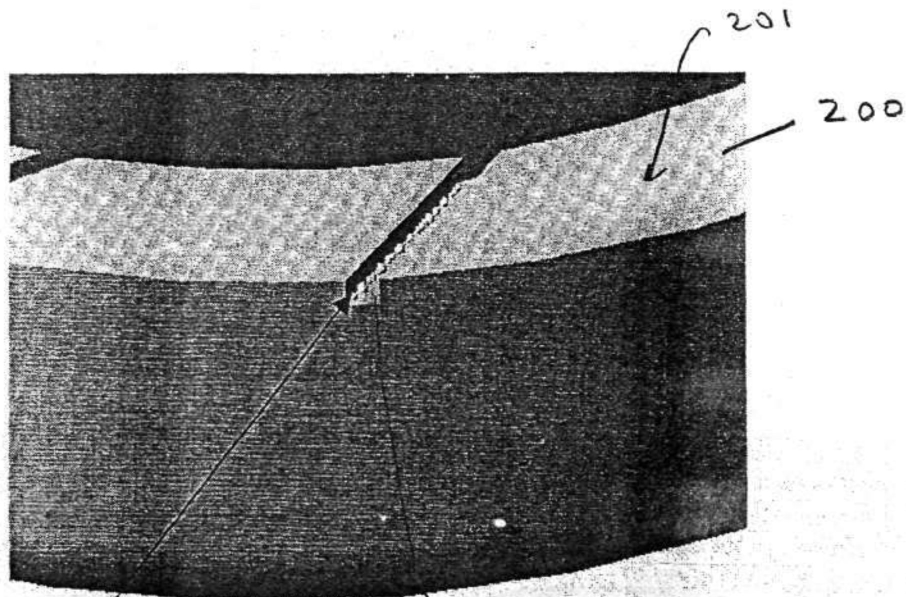

Figure 2B

Dried slurry stuck around the corner of the groove.

208

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Design 1

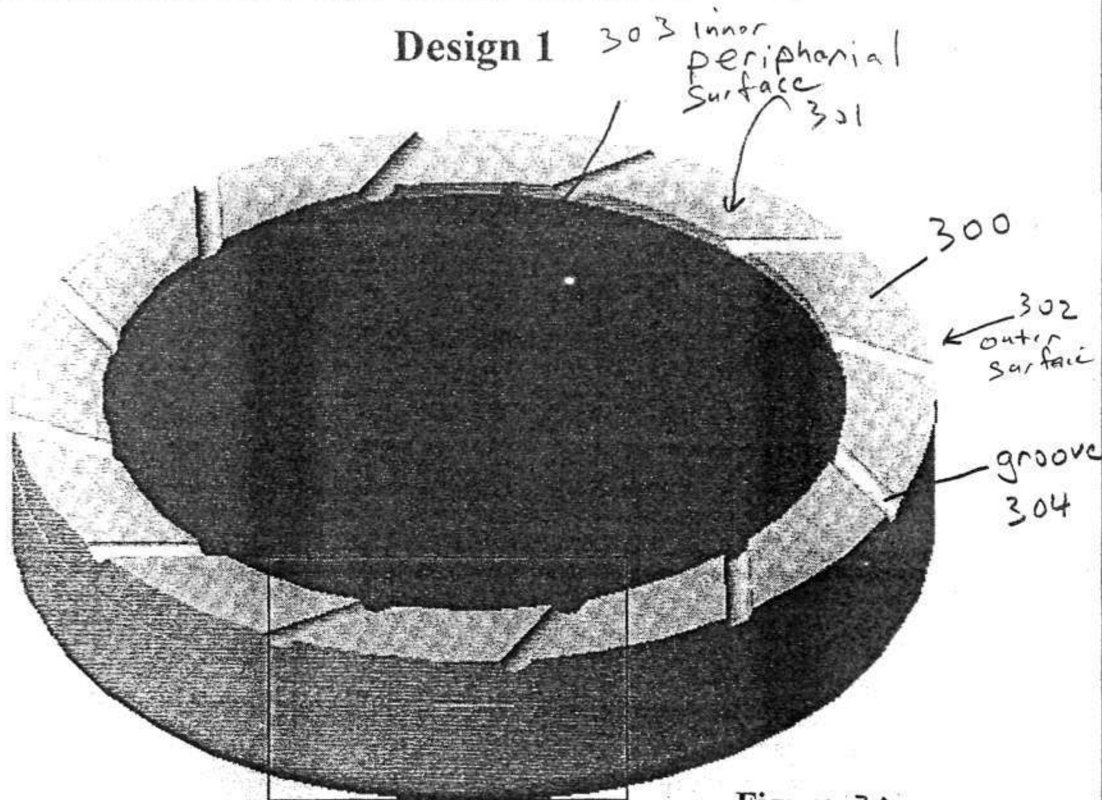

Figure 3A

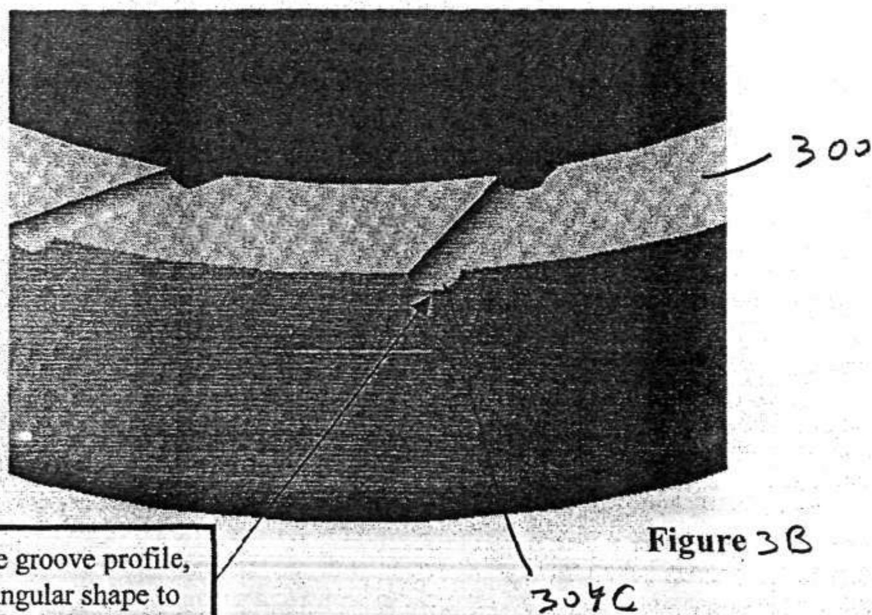

Figure 3B

Modification on the groove profile, changed from rectangular shape to semicircle profile.-310

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CS03-039 Draft Figs

0/0

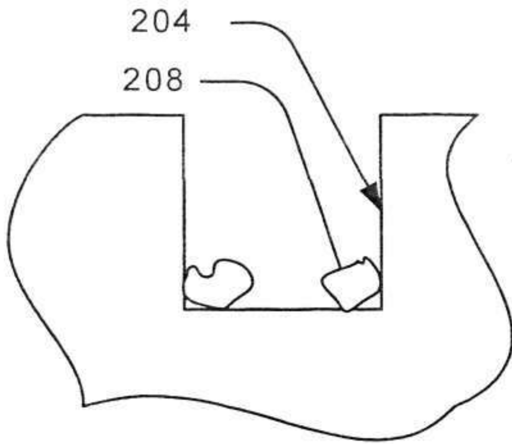

FIGURE 2C

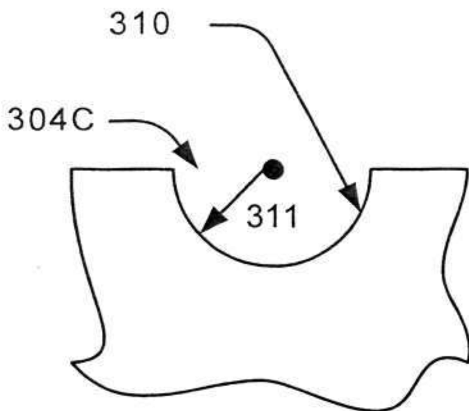

FIGURE 3C

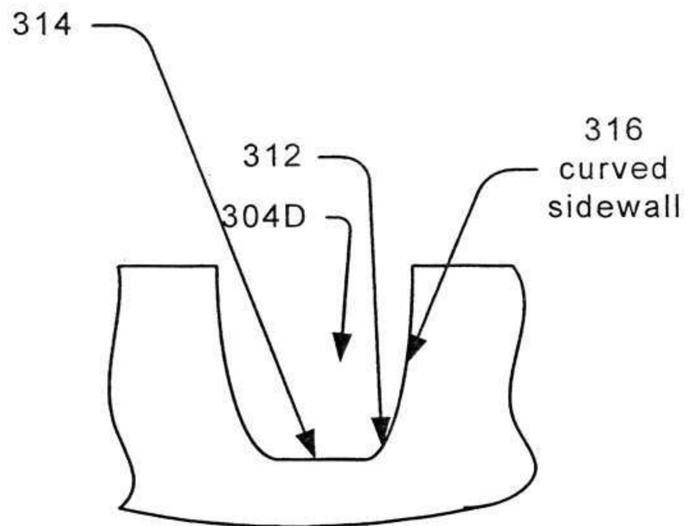

FIGURE 3D

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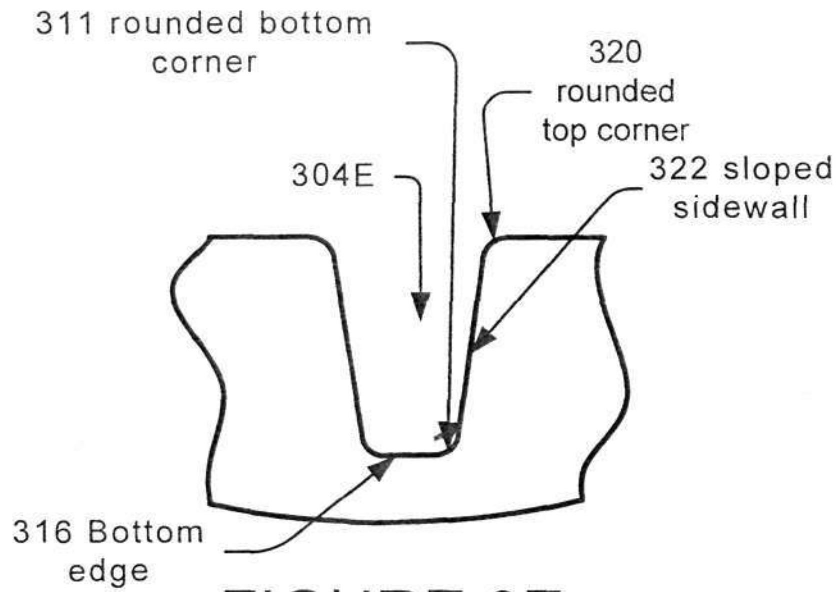

FIGURE 3E

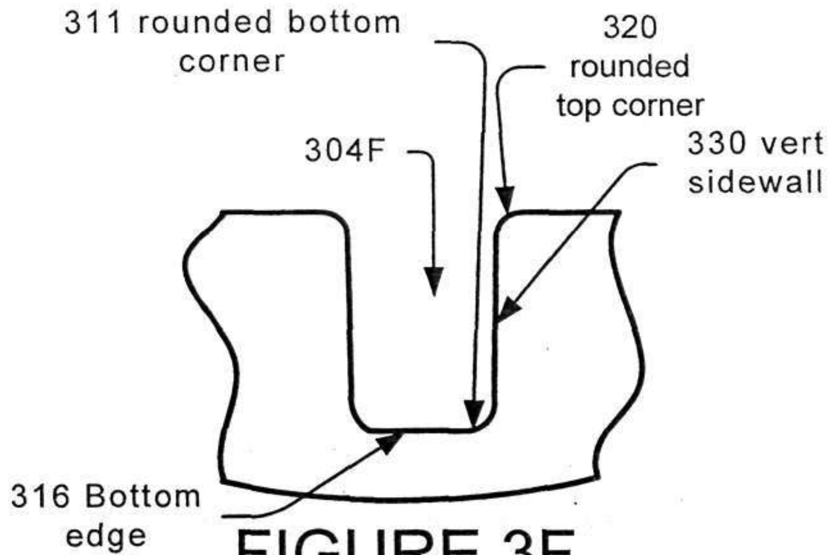

FIGURE 3F
vertical sidewall and bottom

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Chartered
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Design 2

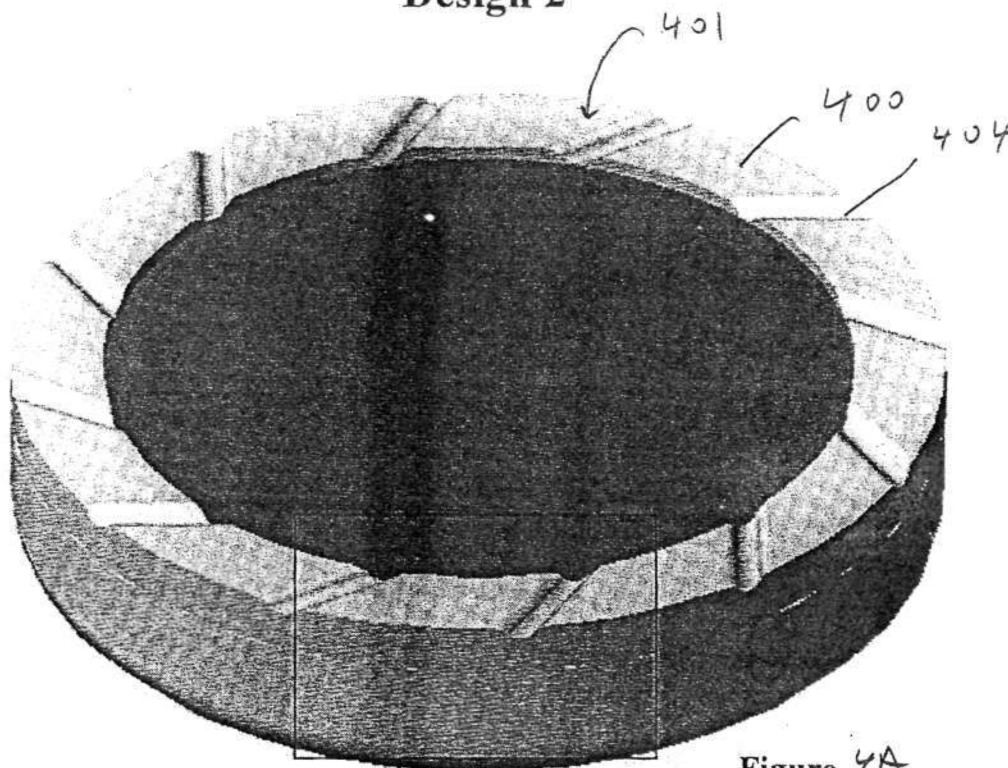

Figure 4A

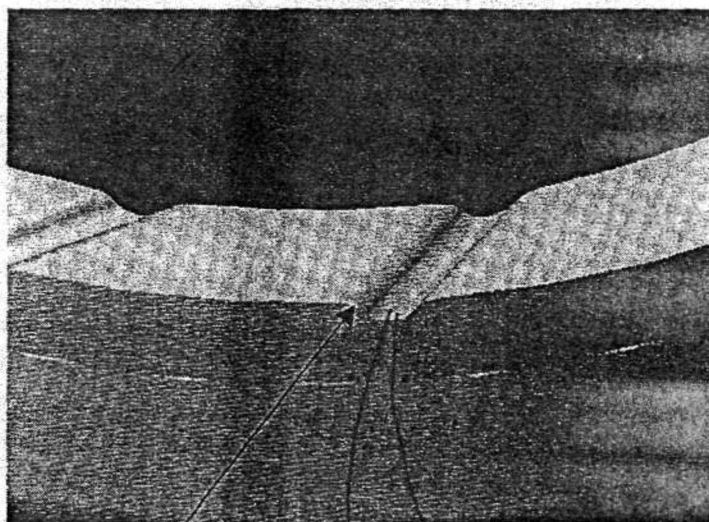

Figure 4B

Further modification based on design 1, the sharp edge was changed to curvature profile.

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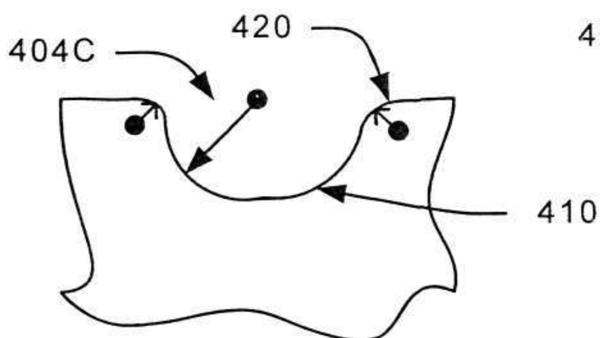

FIGURE 4C

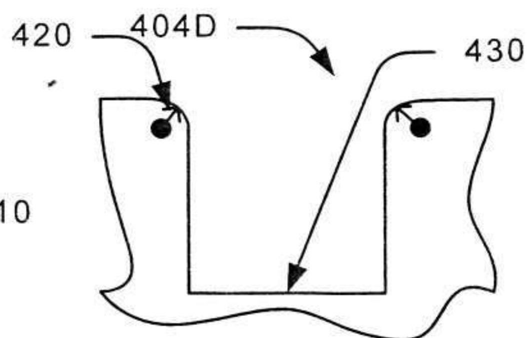

FIGURE 4D

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APPENDIX B:

Metrology Tools

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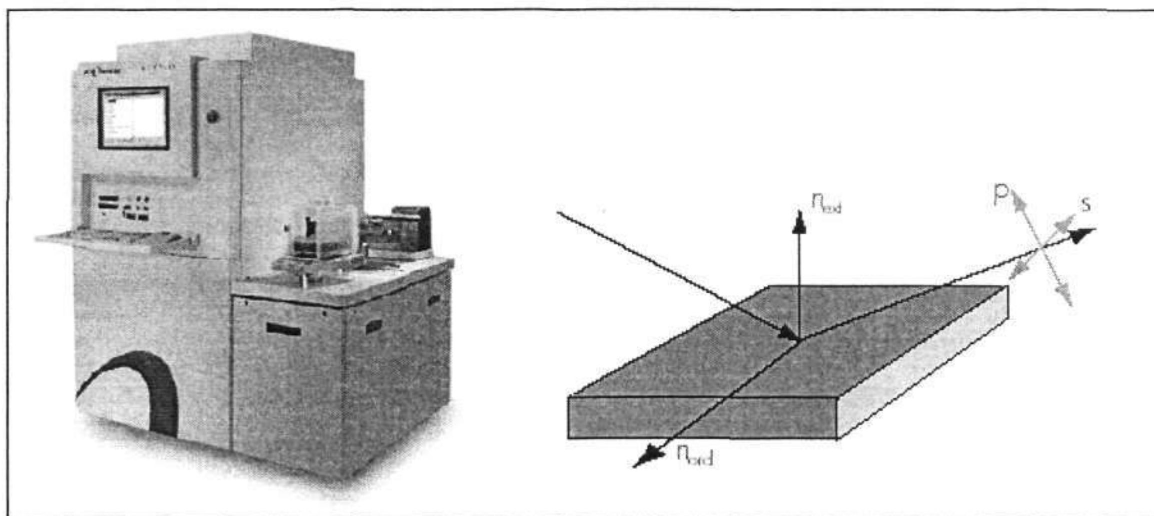
A.1 ASET 5X

The accurate measurement of thin film thickness is critical to investigate, analysis, monitor and control the process during wafer fabrication. One of the optical techniques for measuring the thin film is ellipsometry. Archer was the first to use this method, and details analysis of the method is found in his original paper [99]. The ellipsometry technique makes use of the change of state of the polarization of light when it is reflected from a surface. The state of polarization is radiation, and by the phase difference between two components. The polarization change depends on the optical constants of the silicon, the angle of incidence of the light, the optical constants of the film (i.e., the index of refraction and the extinction coefficient), and film thickness. If index of refraction and extinction coefficient of the substrate are known and if the film is non-absorptive at the wavelength being used (i.e., extinction coefficient =0), the state of polarization of the reflected beam depends only on index of refraction and the thickness of the transparent film.



A. 1 ASET 5X [100].

All the pre- and post-CMP film thickness is measured by ASET-F5x from KLA-Tencor's thin film thickness measurement tool (figure A.1) for direct STI CMP characterization study (refer to section 3.5.1, 3.5.3-3.54). ASET-5x integrates advanced optical metrology-spectroscopic ellipsometry (SE) technique to handle the full range of thin film measurement challenges created by new interconnect technologies, increasing device density and advanced gate structures. SE is a non-

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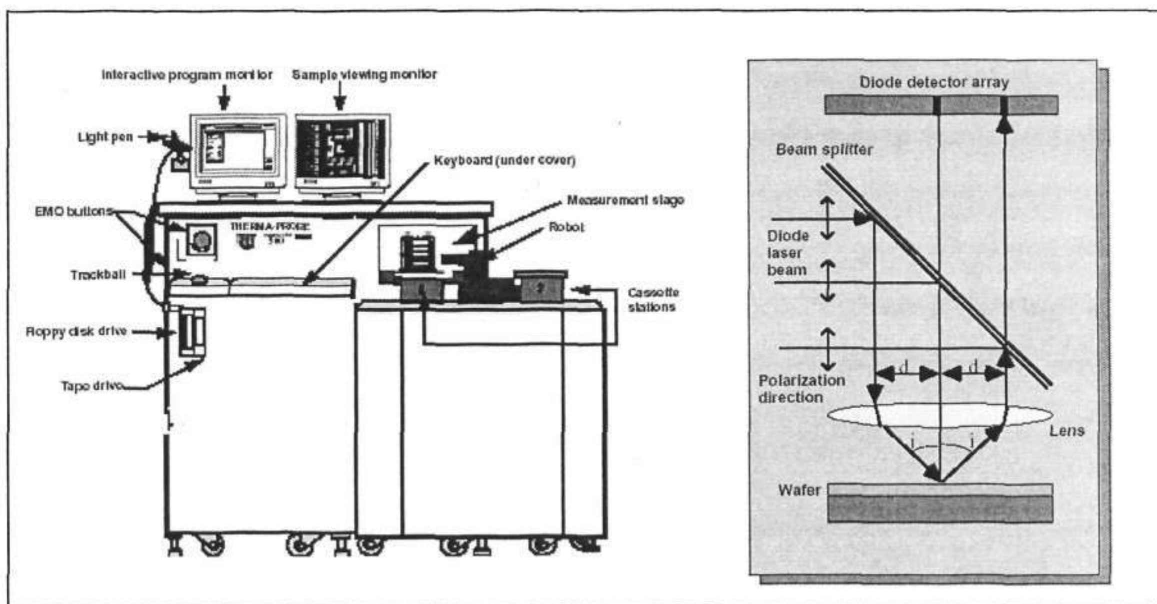
destructive, optical technique for characterizing the optical and material properties of thin films and structures.

A.2 OPTI-PROBE

Various films (such as CVD oxides, nitrides and oxynitrides, polysilicon and amorphous silicon, copper, and other metal films) is deposited in IC fabrication. Optical properties that are functions of deposition conditions and can vary across a single wafer and between different lots of wafers. To precisely measure the thickness of these films, an accurate knowledge of these optical properties is necessary and requires the ability to perform simultaneous measurements of thickness, refractive index, and in some cases extinction coefficient. Unlike ASET 5X, Opti-Probe (figure A.2) measures film and film stacks by integrating three film thicknes measurement techniques: reflectivity as a function of angle (Beam Profile Reflectometry), reflectivity as a function of wavelength (Spectrometry), and changes in polarization state (Ellipsometry) [101]. The polysilicon (section 2.4) and IMD layers thickness(section 4.4.3) is measured by Opti-probe from Therma-Wave Inc.



A. 2 Opti-Probe [101].

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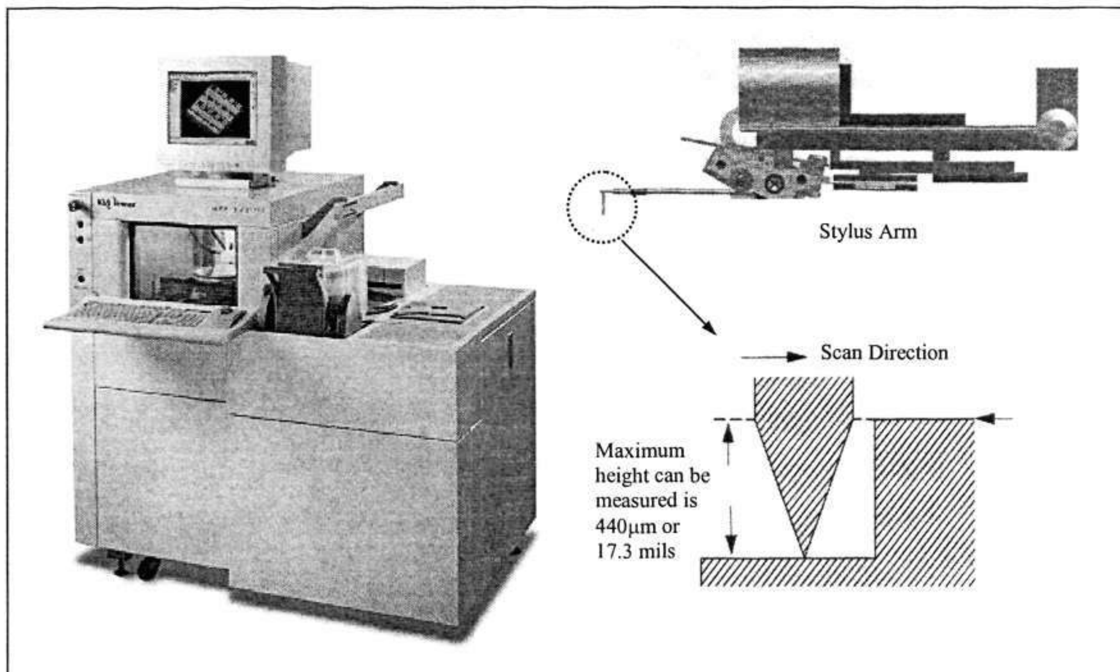
A.3 High Resolution Profiler (HRP)

Step height and dishing of the trench after CMP are evaluated by profilers (section 3.5.6 and 4.3.2). KLA-Tencor's high resolution profiler (HRP) is designed to monitor CMP processes in the fab (figure A.3). The HRP is a highly sensitive surface profiler capable of obtaining images as small as 0.5μm x 0.5μm to as large as 205 mm in radius. The HRP uses dual-stage, stylus-based scanning to achieve AFM-scale resolution in a production environment. The HRP features the ability to measure even submicron features with a vertical resolution 0.1Å and a lateral resolution of 1 nm [102], which makes it particularly useful for surfaces treated with new submicron processes such as CMP. Basically, in this technique, a stylus scans across a pattern features in contact with wafer, while Z motion signal reflects the surface topography scanned. This technique can cover a large scan length, thus it is suitable to evaluate the large trench width. However, depending on the down force and the scan rate, the resolution can vary.



A. 3 HRP [102]

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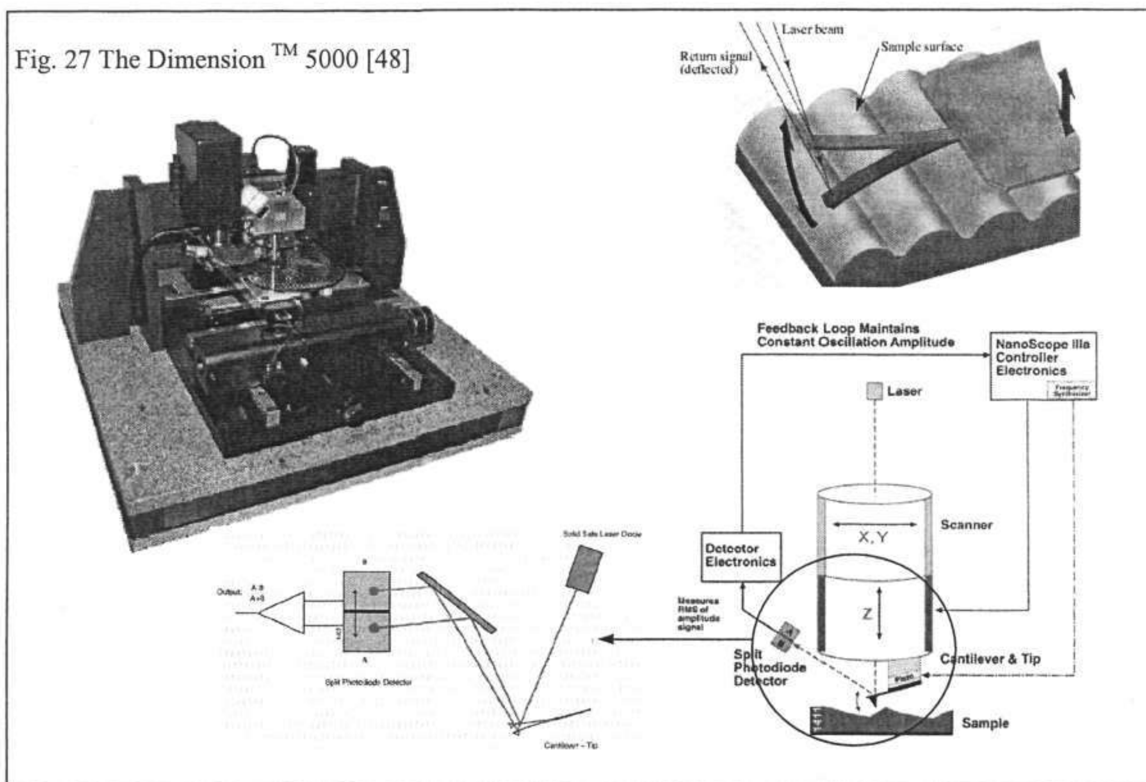
A.4 Atomic Force Microscopy (AFM)

Surface topography before and after CMP (section 3.5.7) is examined by AFM. The main advantages of AFM over profilometry are high spatial resolution, enabling it to function as an imaging tool, and the ultra low force exerted at the surface. AFM can be run in three different modes: contact, non-contact, and tapping mode. Tapping mode is used throughout the study of roughness. Unlike the other two modes, tapping mode can achieved high resolution without introducing destructive friction force.



A. 4 The Dimension 5000 [103]

As shown in the figure A.4 the cantilever oscillates near its resonant frequency as it scanned over the sample surface. The probe is brought closer to the sample surface until it begins to intermittently contact or tap on the surface [103]. This change in oscillation enables the signal to reflect the surface topography accurately with no friction or damage incurred. A laser signal interferometer is used as a position sensor to detect the oscillation change. Laser light from solid state diode is reflected off the back of the cantilever and collected by a position sensitive detector (PSD) consisting of two closely spaced photodiodes whose output signal is collected by differential amplifier. Angular displacement of cantilever results in one photodiode collecting

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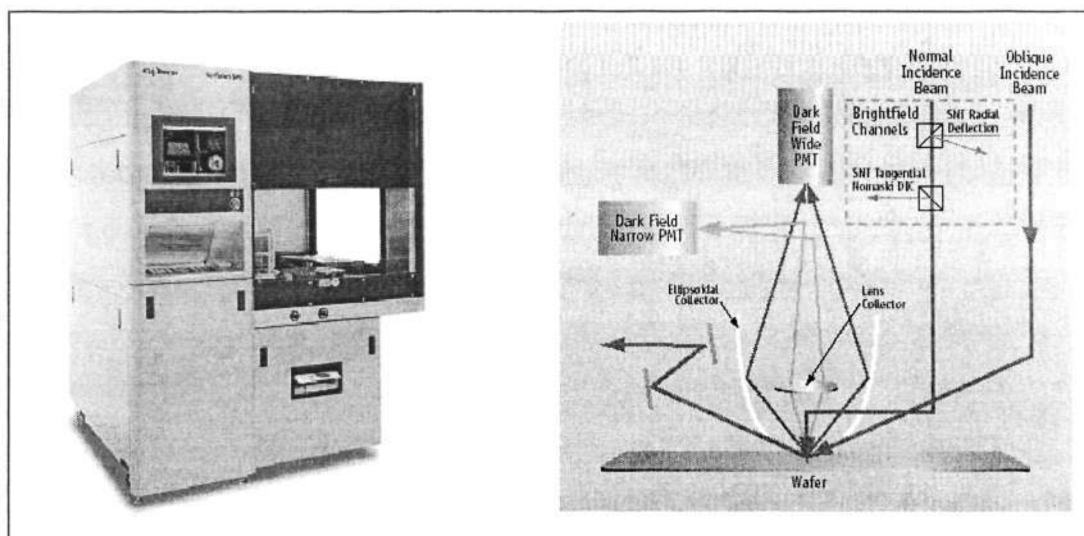
more light than other photodiode, producing an output signal, which is proportional to the deflection of the cantilever.

A.5 Surfscan SP1

In order to minimize wafer surface contamination and particulates, especially for the CMP process since the process is contributing particles to the wafer surface, thus techniques to detect their presence must be available. The concentration level of particles needs to be quantifiably measured after the process. Relatively clean wafers are initially scanned to obtain pre-particles count before CMP. These wafers are then passed through the polisher and the resulting counts determined. In this work, oxide layers on blanket wafers were polished using ceria based and silica based slurry on Mirra polisher platen1 and platen 2/3 respectively (section 3.5.2), and then wafers were cleaned by using scrubbers with ammonia in the On-track cleaning unit. The polished wafers were then inspected on a Surfscan SP1 (figure A.5).



A. 5 Surfscan SP1 [104]

The system is used to detect submicron particles on the *unpatterned* wafers surface and to investigate the effectiveness of the same cleaning process applied to two slurries with different chemistry and abrasive. In brief, such inspection tools rely on the optical scattering of light beams by particles. The beams are scanned across wafer surface and an integrating light collector is used to collect any scattered light. On a

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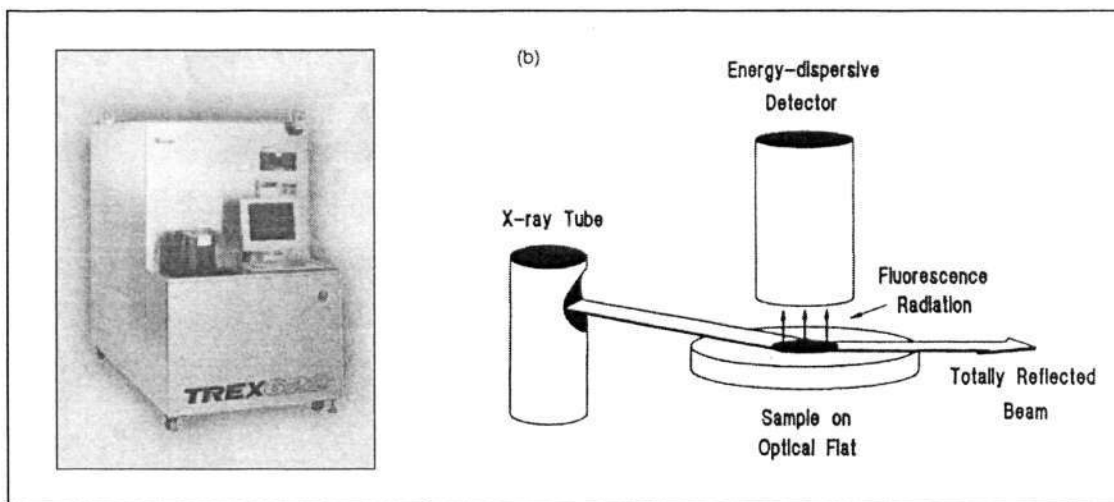
clean and smooth surface, normally-incident laser light will be reflected straight back, and thus will escape between the light collectors without being detected.

A.6 Total-Reflection X-Ray Fluorescence (TXRF)

Metal contaminations are strictly prohibited in the front-end on line process as it will degrade or damage the transistors. TREX 620 series tool (figure A.5) from Technos International is employed to evaluate metal contaminations on the surface of the wafers after CMP (section 3.5.8). In TXRF, x-ray is generated using high energy electrons hitting either tungsten (W) or molybdenum (Mo) targets. In this work, W is used as the target. The x-rays from different targets different spectra of wavelengths. Filters such as nickel (Ni) or zirconium (Zr), with different thickness, can be used to control the needed x-ray wavelength and intensities. The x-ray is then applied to the materials to be analyzed. The x-ray photons knock out the inner shell electrons in the atoms of an element. This causes the outer shell electrons to fall into the vacancy in the inner shells, emitting photons. Due to different elements having different electron shell configurations and energies, the photons emitted from various elements will have their own characteristics. From these emission spectra, the elements can be both qualitatively and quantitatively determined.



A. 6 TREX 620 [105]

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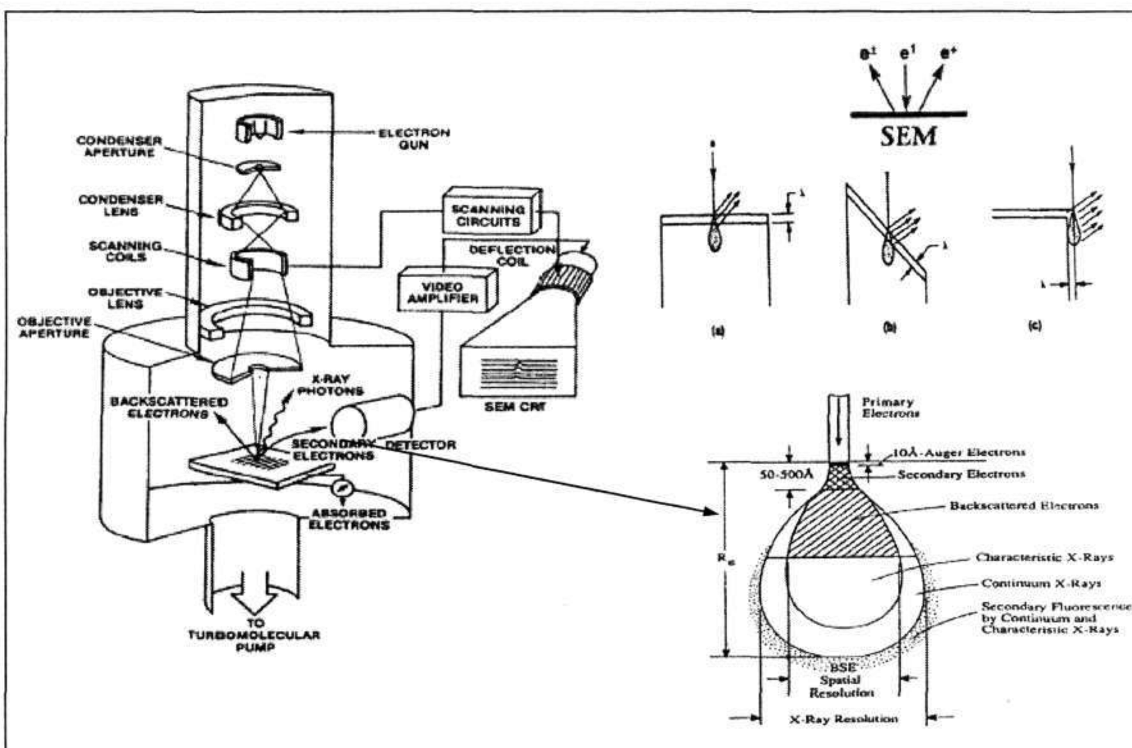
A.7 Scanning Electron Microscopy (SEM)

The accurate way to measure the film thickness is to prepare a cross section of the film on the silicon substrate and take scanning electron microscope (SEM) picture of the stack (section 3.5.5-3.5.6). For SEM, an electron beam impinges at a high energy (5 to 30 keV) on the sample, resulting in: secondary electrons, backscattered electrons, X-ray, Auger electrons, light and Electron Beam Induced Current (EBIC) and the schematics is shown in figure A.6. Secondary electrons (SE) will show better resolution than backscatter electrons or X-ray because of the smaller escape depth of SE. X-ray can escape from the specimen within a much bigger escape depth, thus it can be used to provide materials information.



A. 7 SEM [106]

Secondary electrons can only escape from the specimen within the escape depth λ. Hence tilting the sample will give stronger SE signal. This explained the sample edge gives particularly strong SE signal, thus SE can provide topographical contrast.

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