

Novel RF Process Monitoring Test Structure for Silicon Devices

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Abstract—This paper demonstrates a novel RFCMOS process monitoring test structure. Outstanding agreement in dc and radio frequency (RF) characteristics has been observed between conventional test structure and the new process monitoring test structure for MOSFET with good correlations in measured capacitances also noted for metal-insulator-metal capacitor and MOS varactor. Possible process monitoring test structure is also suggested as a reference benchmarking indicator for interconnects.

Index Terms—MIM capacitor, MOS varactor and interconnect, process monitoring, RFCMOS, scribe line.

I. INTRODUCTION

SEMICONDUCTOR foundries of today grant fabless integrated circuit design companies not only easy access to advanced silicon processing technologies but also provide reliable production capacity of high-yield wafer manufacturing. With the ever-growing interests of exploiting the mature and cost-effective silicon technology for radio frequency (RF) integrated circuit (IC) designs, limitations of the mixed-signal/RFCMOS processes must be carefully characterized and well understood by yield, device modeling, as well as circuit design engineers [1], [2]. Very often, because of circuit design sensitivities to process variations, a designer's product may still encounter setbacks even though production wafers are within the specification limits of the technology. Such sensitivities are detrimental and can manifest as yield loss, early life reliability failures or even shifts in circuit operating frequency, affecting the overall business performance of these circuit design companies.

Most foundries do not normally provide extensive information on electrical specifications, performance boundaries and process variations of the RF devices offered in the process design kits. Hence, the development of new RF process monitoring test structures to characterize these process variations and correlating them to the circuit performances become extremely important. Close partnerships between circuit design companies and foundries benefit both parties, making one-pass design success and high-yield RFCMOS process possible. Process monitoring test structures will help identify critical RF device performance indicators that are sensitive to the circuits, subsequently establishing them as important RF electrical specifications for

that particular process. Reliable test structures and knowledge of critical parameters to monitor, allow RF performance distribution across the process to be accurately incorporated into device corner models. With these models, circuit designers can take preventive measures prior to circuit fabrication if the process variations are found to have adverse effects during circuit simulations.

II. TEST STRUCTURES, RESULTS AND DISCUSSIONS

In this paper, novel layout designs for RF process monitoring test structures are proposed. Silicon devices are characterized to investigate and verify the functionality for this new design. Conventional device test structures are usually layout in the east-west configuration, allowing calibrated RF probes to touch down on the two sets of ground-signal-ground (GSG) pads. Such layout schemes are very popular and widely adopted for RF device characterization as well as device model development.

To monitor a process, scribe line test structures residing between adjacent dies on the wafer have to be designed such that the overall width of the whole test structure typically do not exceed more than 80–100 μm wide. This imposes limitations in designing scribe line RF test structures because it is believed that calibration of the test instrument and cables up to the probe tips for test pads in the nonconventional layout style, involves technical expertise and experience to obtain reliable measured S-parameters. In this paper, new test structure layout approach together with Cascade Microtech's Infinity probes [3] that allow devices to be tested with smaller pad geometries, demonstrate reliable and repeatable on-wafer RF scribe line device measurements on MOSFET, metal-insulator-metal (MIM) capacitor, and MOS varactor.

A. MOSFET

RF nMOSFET with channel width (W) and length (L) ratio of $W/L = 24/0.18 \mu\text{m}$ (6 Fingers) layout using both the conventional and scribe line designs are fabricated in the current 0.18 μm RFCMOS processing technology. Fig. 1 shows the die photos of the conventional RF test structures, with the device under test, its corresponding open and short de-embedding calibration structures. In Fig. 1(a), the gate (Port 1) of the NMOS is on the west side, the drain (Port 2) is on the east side. The source and bulk of the transistor are connected together and tied to the RF ground pads. Fig. 2, on the other hand, consolidates die photos of the RF process monitoring test structures with new

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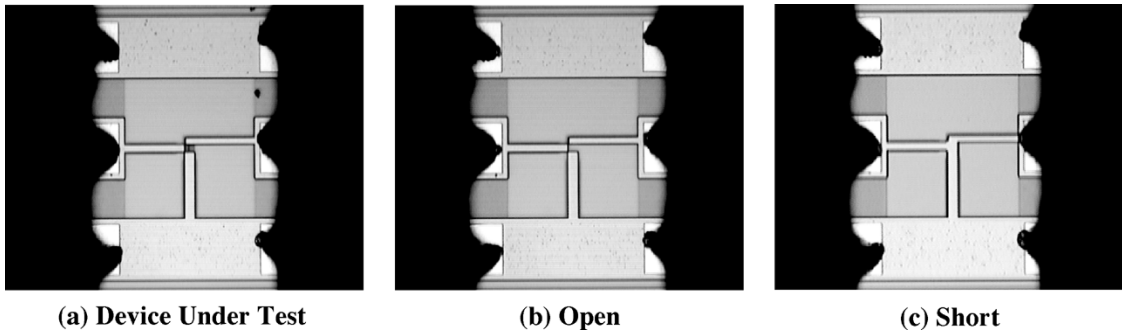


Fig. 1. (a) Die photos showing the conventional GSG RFCMOS test structures (CON) with cascade microtech infinity probes for (a) a 6-finger RF NMOS, (b) its open and (c) short de-embedding structures.

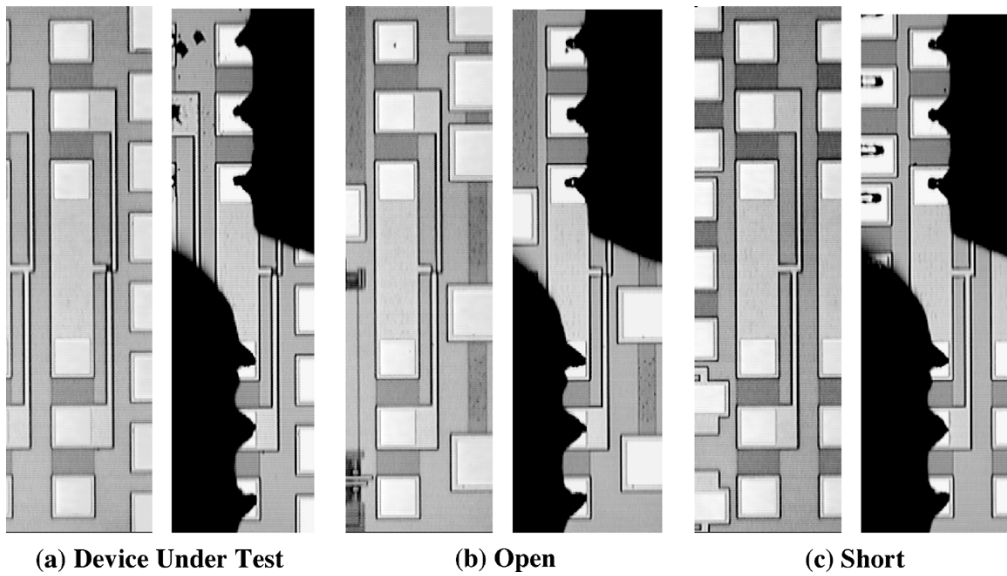


Fig. 2. Die photos showing the proposed Scribe Line Process Monitoring test structure (SLM) with and without infinity probes for (a) a 6-finger RF NMOS (a), its open (b) and (c) short de-embedding structures.

scribe line layout scheme having GSG pads in the north-south configuration.

Characterization experiments to compare the performances of this device in the two designs help verify if the new scribe line design function unfaithfully. First part of the experiment evaluates the dc characteristics of the transistors using kelvin force/sense measurements available in Agilent 4156C semiconductor parameter analyzer. High-frequency on-wafer S-parameter measurements are subsequently carried out using Agilent 8510C Vector Network Analyzer [4] and Cascade Microtech Infinity probes. The wafer and RF probes are shielded within the Microchamber of the S300 Semi-automated Probe Station during the test and measurements. Two-port S-parameters of the transistors are extracted over the frequency range from 50 MHz to 20.05 GHz. Two-step de-embedding technique, both open and short, are performed to accurately remove the parasitics of the test frame [5]. To facilitate the de-embedding process, both open pad and short calibration structures are fabricated next to the devices.

Comparing the dc characteristics of the two test structure designs in Fig. 3(a) and (b), there are no significant differences in drain current, transconductance and the output resistance at various terminal biases. Moving on to the RF performance com-

parison, for gate bias sweep from 0.5 to 1.8 V in steps of 0.1 V and at constant drain bias of 1.8 V, Fig. 3(c)–(f) consolidates the 2-Port characteristics of the NMOS transistor. Both test structure designs produce similar input and output match characteristics. Fig. 3(e) and (f) shows no significant differences in gain-frequency response between the two designs with only small deviations of about 3.5% and -2% in S21 magnitude and phase, respectively, for most of the gate biases. The extracted unity-gain cutoff frequency, F_T , for both designs are also in good agreement with a deviation of no more than $\pm 1.5\%$. Studies on PMOSFETs and transistors of other sizes, together with impacts of de-embedding technique on the correlations of the two test structure designs have been investigated and reported in [6].

B. Metal-Insulator-Metal (MIM) Capacitor

2-pF MIM capacitors fabricated between metal 5 and 6 of the $0.18\ \mu\text{m}$ technology have been included for further investigations to ensure that the proposed scribe line test structure design is reliable and extendable to other devices. Fig. 4(a) shows the conventional test structure layout for the MIM capacitor. On-wafer Two-Port S-parameter measurements up to 10 GHz

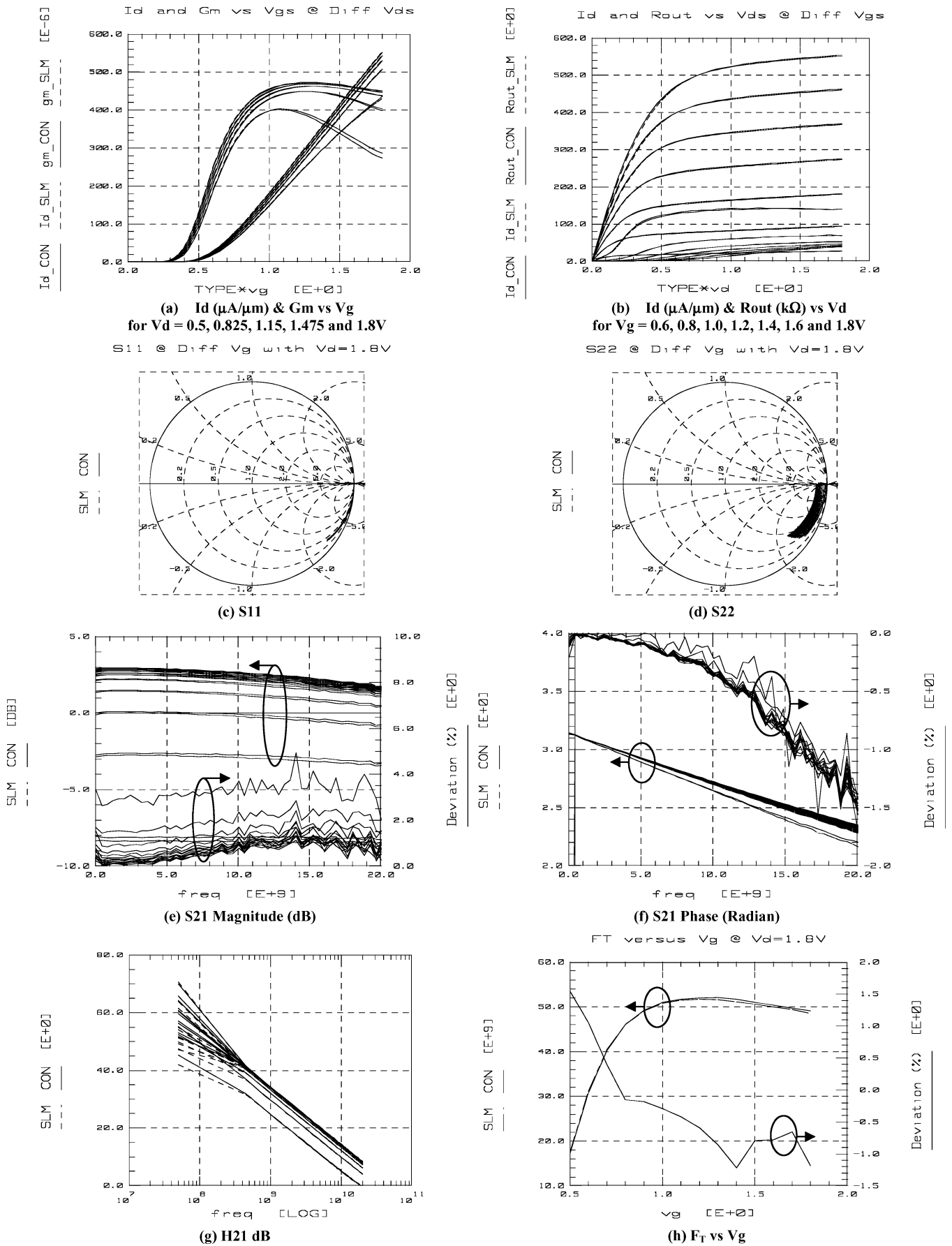


Fig. 3. Conventional (CON) versus Scribe Line (SLM) design for a 6-finger NMOS transistor ($W/L = 24/0.18 \mu\text{m}$). (a)–(b) IV; (c)–(f) S-parameters; (g) H21; and (h) F_T (h) for $V_g = 0.5 - 1.8 \text{ V}$ in steps of 0.1 V @ $V_d = 1.8 \text{ V}$.

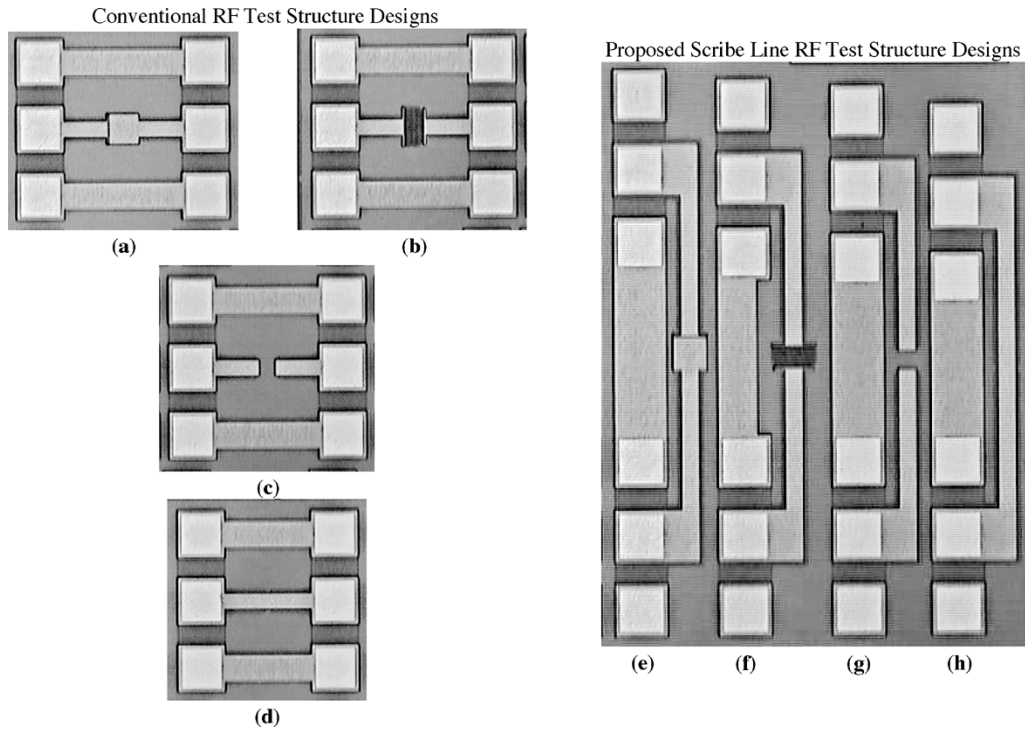


Fig. 4. Die photos showing the conventional (CON) versus proposed scribe line (SLM) design for 2 pF MIM capacitor and MOS varactor with open and thru' de-embedding structures. (a) MIM capacitor; (b) MOS varactor; (c) open; (d) thru'; (e) MIM capacitor; (f) MOS varactor; (g) open; (h) thru'.

are performed on the MIM capacitor in similar experimental setup as described for the MOSFET in Section II-A. A two-step de-embedding technique using open and thru' calibration structures shown in Fig. 4(c) and (d) is used to remove the pad capacitive and test leads resistive and inductive parasitics respectively. RF characterization is repeated for the MIM capacitor in scribe line layout design, its open and thru' de-embedding test structures as shown in Fig. 4(e), (g), and (h), correspondingly.

The measured results for the MIM capacitors are compared in Fig. 5. Up to 10 GHz, the two test structure designs yield good agreement in measured capacitance with deviation of not more than -2% . Both layout schemes produce similar trends in quality factor frequency response as shown in Fig. 5(d), exhibiting good correlations between the proposed scribe line and conventional RF layout schemes. Such excellent association between conventional and scribe line approach is achievable due to the reliable two-step, open-thru' de-embedding methodology.

C. MOS Varactor

Identical MOS varactors, readily available in $0.18\text{-}\mu\text{m}$ RFCMOS technology device library, with tuning capacitance range from 0.6 to 2.6 pF are layout in both the conventional and proposed scribe line test structure designs. MOS varactors used in this experiment are actually nMOSFET in Nwell, operating in the accumulation mode i.e. Polysilicon gate is the capacitor top plate and bottom plate refers to Nwell. Shown in Fig. 4(b), (c), and (d) are die photos of the MOS varactor under test and its open and thru' calibration structures, respectively for the conventional test structure designs. Scribe line designs for this

MOS varactor, on the other hand, are revealed in Fig. 4(f), (g), and (h). S-parameter measurements are performed with the vector network analyzer and the semiconductor parameter analyzer supplies dc biases to the gate and Nwell of the MOS varactor in similar experimental setup used for MOSFET's. A linear potential sweep from -1.8 to 1.8 V in steps of 0.1 V is applied to the gate of the MOS varactor and Nwell, on the other hand, is tied at 0 V.

Fig. 6(a)–6(d) consolidate the measured Two-Port S-parameters of the MOS Varactor showing good agreement between the conventional and scribe line test structure designs at various bias conditions. Fig. 6(e) compares the measured capacitance versus frequency and good agreement is noted between the two test structure designs. When capacitances at 5 GHz are extracted from Fig. 6(e), capacitance versus gate voltage plot is obtained as depicted in Fig. 6(f). Excellent correlations are observed between the conventional and scribe line designs with capacitance deviations of not more than $\pm 1\%$ for positive gate biases, a region which is generally of greater interests to circuit designers. Both layout schemes also reveal similar trends in quality factor versus frequency characteristics and quality factor versus gate bias behavior at 5 GHz.

D. Interconnects

Inductors are important components in RFCMOS designs and they are used primarily in matching networks and LC tank circuitries. Nonetheless, process monitoring of spiral inductors for RF applications is difficult since these inductors generally have huge dimensions and cannot be accommodated in the scribe lines. When inductors are used as important circuit components, routing of devices in circuit design also introduces additional

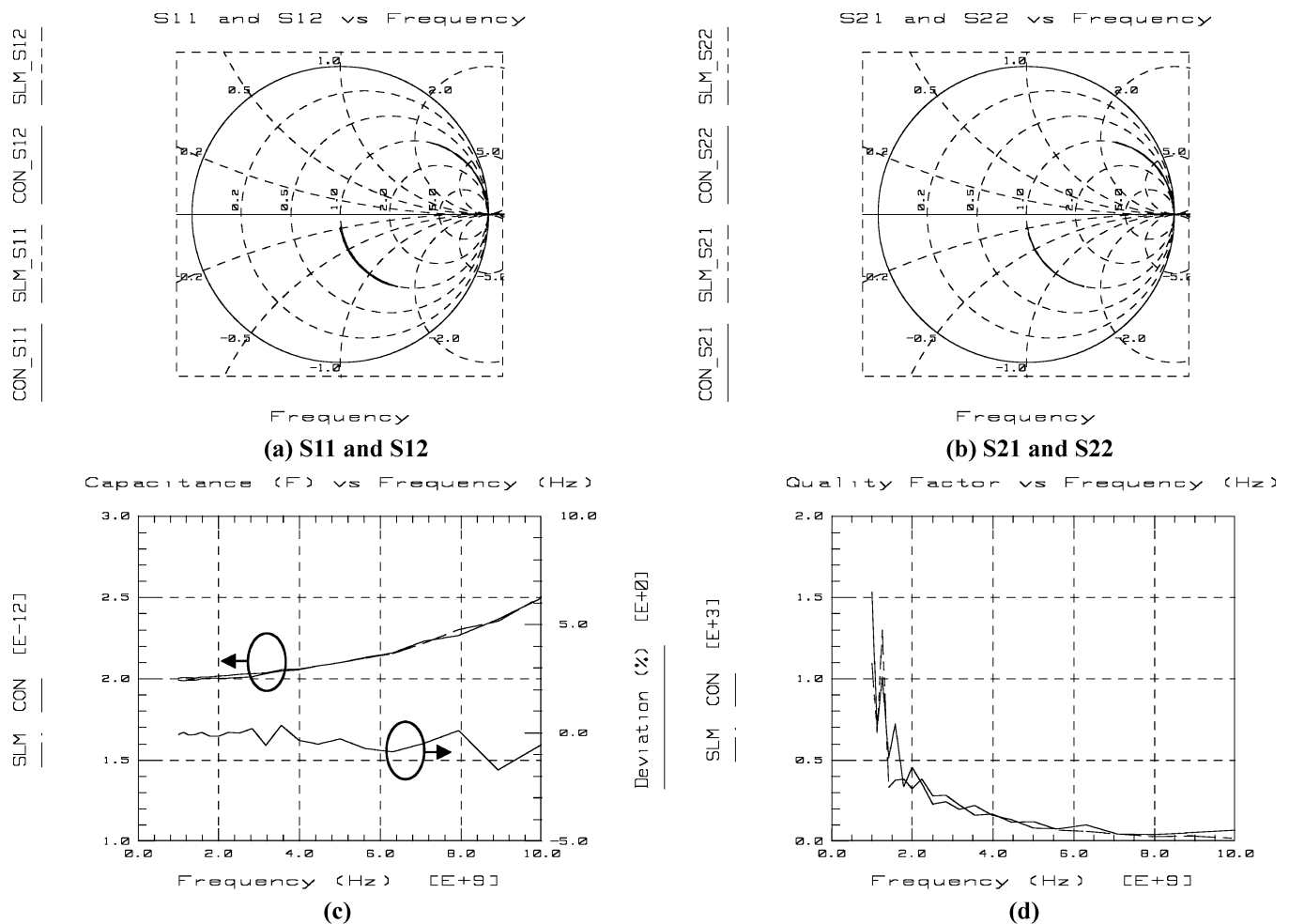


Fig. 5. Conventional (CON) versus Scribe Line (SLM) design for 2 pF MIM capacitor, (a) and (b) S-parameters, (c) capacitance, and (d) quality factor versus frequency.

metallization into the circuits. Self-inductances of these interconnects at gigahertz frequencies are nonnegligible. Parasitic resistance associated with these metal lines will increase with frequency due to skin effects and their substrate losses also become dominant at the high RF regime.

Hence, it is important to perform RF characteristics process monitoring of metallization to ensure that detrimental effects of these interconnects on circuit performance are kept in checks, providing also insights as to how spiral inductors behave in the production environment. A possible scribe line design for interconnects is proposed in this work. Die photos of conventional and scribe line designs for interconnects with corresponding open calibrations structures are consolidated in Fig. 7. Due to the north-south placement of GSG probes in the scribe line design, metal 6 interconnect line with identical length and width of 500 and 10 μm , respectively, has to be layout with two 90° bends as compared to the conventional layout style shown in Fig. 7(c).

On-wafer RF characterization are performed on these interconnect test structures. Fig. 8(a) and (b) compares S-parameters of the interconnect lines from the conventional and scribe line layout schemes. Fig. 8(c) and (d) reveals that up to 10 GHz, there is about 10% difference in the extracted parasitic inductance and resistance of the interconnect line. At low fre-

quencies, extracted resistances from the two test structures correlates well since the interconnects have identical length and width. Up to 4 GHz, the scribe line design has a +5% deviation in resistance when compared against interconnect in the conventional layout scheme. Although measured RF characteristics between the conventional and scribe line designs do not agree completely, primarily due to the two 90° bends, the proposed scribe line design can still be adopted to monitor the RF characteristics of metallization.

Good correlations between conventional and the proposed scribe line layout schemes for devices like transistors, capacitors, and varactors must be achieved since the device models used in circuits are developed with measurement data from test structures in the conventional layout style. It is however uncertain to know the dimensions of the RF interconnects used in different parts of the circuits and the smallest useful spiral inductors are still too large to fit into scribe lines between dies. Therefore, until a better scribe line design for interconnect is developed, interconnects' parasitic inductance and resistance derived from the proposed scribe line test structure can still serve as a benchmarking reference indicator for a particular process, allowing process engineers to react accordingly if inductances and resistances associated with interconnects increase abnormally.

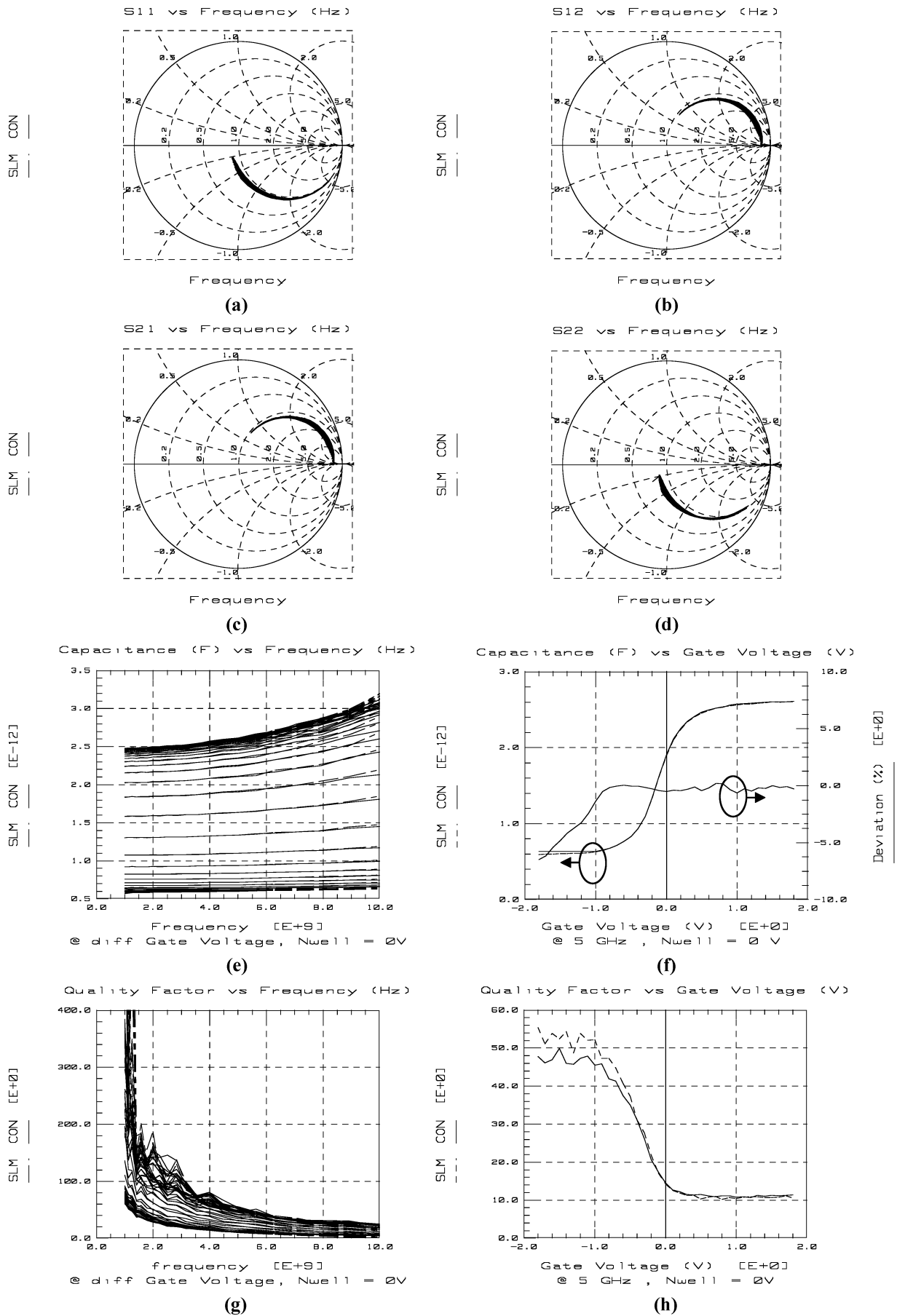


Fig. 6. (a)-(d) Conventional (CON) versus scribe line (SLM) design for 2 pF MOS Varactor, (a)-(d) S-parameters, (e) capacitance versus frequency @ diff gate bias, (f) capacitance versus gate bias @ 5 GHz, (g) quality factor versus frequency @ diff gate bias, and (h) quality factor versus gate bias @ 5 GHz.

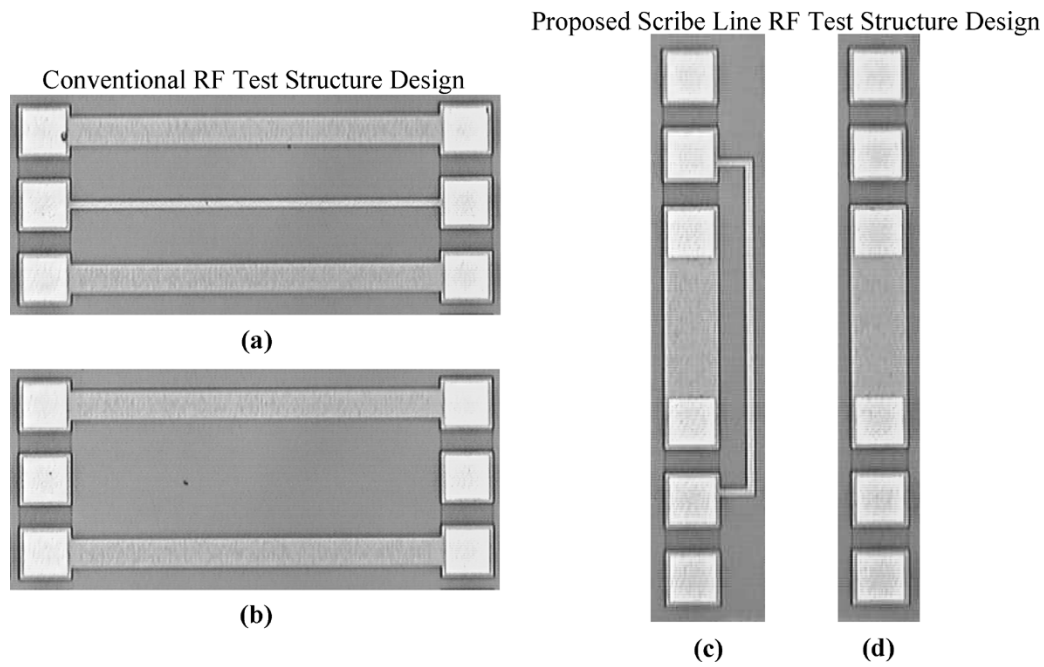


Fig. 7. Die photos showing the conventional (CON) versus proposed scribe line (SLM) design for metal 6 interconnect structure (Length = 500 μm , Width = 10 μm) with open de-embedding structures. (a) Interconnect; (b) open; (c) interconnect; (d) open.

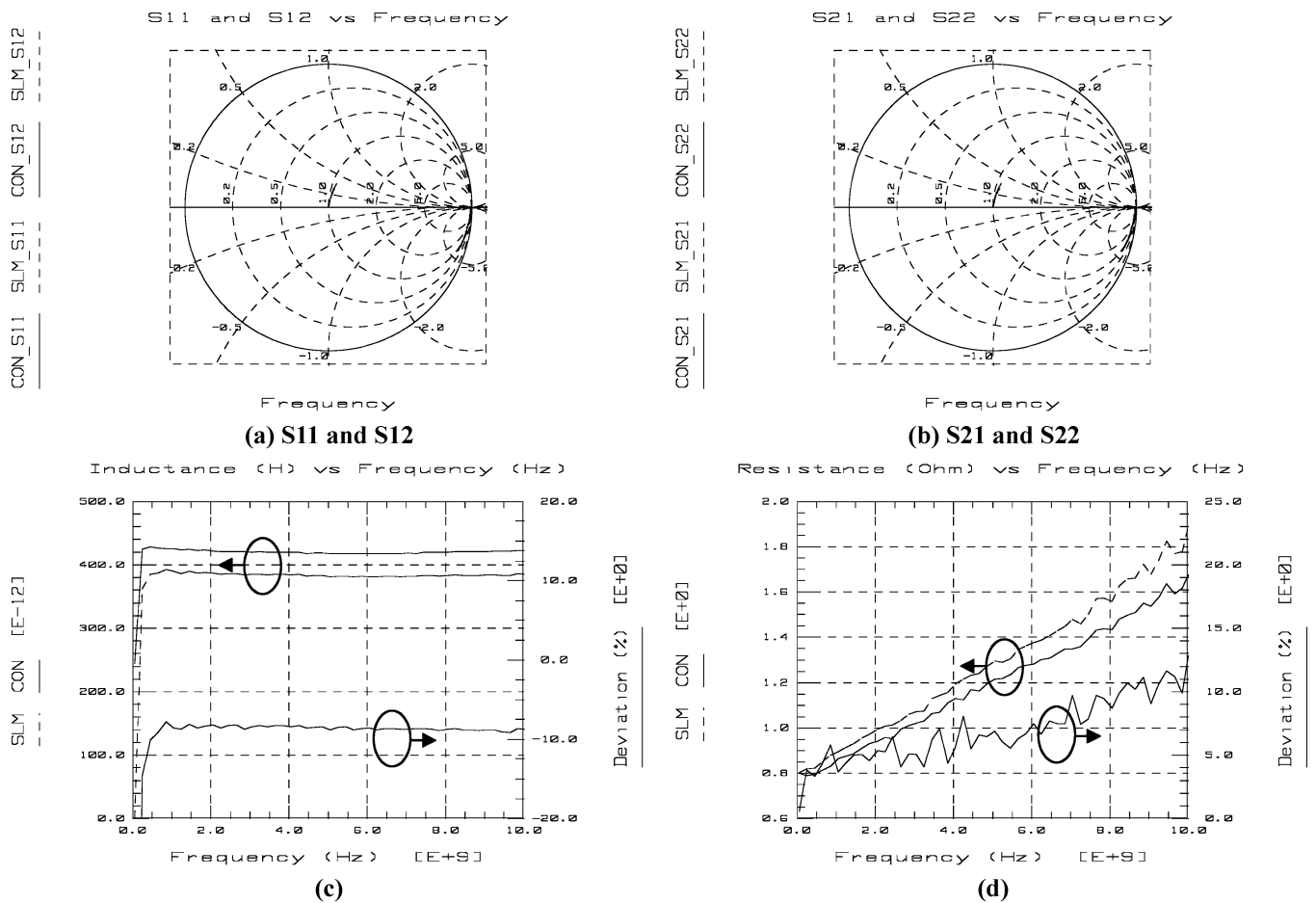


Fig. 8. Conventional (CON) versus scribe line (SLM) design for metal 6 interconnect (Length = 500 μm , Width = 10 μm), (a) and (b) S-parameters, (c) parasitic inductance, and (d) resistance versus frequency.

III. CONCLUSION

This paper highlighted and emphasized the need for reliable RF process monitoring test structures to understand circuit sensitivities to process variations, allowing both semiconductor foundries and circuit design companies to achieve better process and circuit yield. A novel design for RF process monitoring test structure has been proposed in this paper. The functionality and reliability aspects of this new test structure design have been tested extensively. Excellent agreement in measured RF characteristics has been observed for MOS transistors, capacitors and varactors. A possible scribe line design is also proposed to serve as a reference benchmarking indicator for interconnects.

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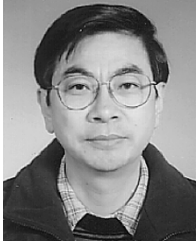


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