DESIGN OF HIGH PERFORMANCE LOW-DROPOUT REGULATORS FOR ON-CHIP APPLICATIONS

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TABLE OF CONTENTS

ABSTRACT

The growing portable and battery powered devices have driven the power management circuits to consume as low power as possible so as to prolong the operation life of the devices. Low-dropout (LDO) regulators are important building blocks in power management unit which provides majority or all power sources in a system chip. This work focuses on the circuit design techniques for high-performance regulators for on-chip applications.

This thesis presents (i) a new frequency compensation technique for multistage amplifier, (ii) two types of composite power transistor, (iii) a new ultra-low quiescent current regulator architecture and (iv) a new low-impedance loading network circuit design technique for LDO regulator applications. For frequency compensation, the design objectives are to address power-bandwidth-efficiency as well as area-efficiency at a large capacitive load. Turning to the LDO regulator designs, the focuses are to address low quiescent current consumption, low voltage operation, good stability and current efficiency at light loads.

A cross feedforward cascode compensation technique is proposed for a three-stage amplifier design. Implemented in 65 nm CMOS technology, the amplifier only consumes a quiescent current of 17 μA at a 1.2 V supply and occupies an active area of 0.0088 mm^2. In addition, when driving a 500 pF capacitive load, it achieves a unity-gain bandwidth of 2 MHz with a phase margin of 52°. The proposed amplifier is stabilized by a small compensation capacitor of only 1.15 pF. In view of

application as an error amplifier in LDO regulator design, it is particularly useful for driving a power transistor with significant large input capacitance.

In another contribution, two types of composite power transistor based regulator are proposed. Due to employment of shunt feedback resistor to reduce impedance in the composite power transistor, the stability criterion is relaxed whereas on-chip compensation capacitor can be reduced to only few pF level. For the first output-capacitorless LDO (OCL-LDO) regulator with push-pull composite power transistor, it can operate at a minimum supply of 0.75 V and supply a maximum load current of 50 mA while consuming only 12.15 μW. It is fabricated in 65 nm CMOS technology and occupies an active area of 0.0096 mm^2. The measured output change is 103 mV when load current is switched from 0 to 50 mA in 100 ns at a 100 pF capacitive load. For the second output-capacitor LDO (OC-LDO) regulator with dynamic-biased composite power transistor, it is capable to provide a maximum current of 450 mA from a 1.2 V supply and dissipates only 4.7 μA of quiescent current at zero load current. It is realized and simulated in 0.18 μm CMOS technology. With an output capacitor of 4.7 μF, the simulated output change is 64.62 mV when the load current is changed from 0 to 450 mA in 10 ns. It has shown that both LDO regulators greatly enhance the transient responses with respect to conventional counterparts.

Further contribution deals with a new architecture employing adaptive power transistors circuit technique for ultra-low quiescent current OCL-LDO regulator. Depending on the load current, the OCL-LDO regulator transforms itself to a two or three stage configuration automatically. Implemented in 65 nm CMOS process technology, the proposed regulator consumes a quiescent current of 0.9 μA at zero

load current. It occupies an active area of 0.017 mm^2 and is able to supply a maximum current of 100 mA from a 1.2 V supply. Despite having low quiescent current performance, the transient response is not compromised significantly. The measured output change is 68.8 mV when the load current is switched from 0 to 100 mA in 300 ns with a capacitive load of 100 pF. It is able to recover from transient response within 6 μs.

Finally, the introduction of a low-impedance loading network circuit is dedicated to enhance the stability or to improve light-load efficiency. To demonstrate the proposed circuit technique, it is applied to the design of an OCL-LDO regulator. The simulation results have confirmed the circuit operation in 0.18 μm CMOS technology. The simulated quiescent current is 14 μA at a 1.2 V supply, no minimum loading current is required. Therefore, the current efficiency at light load is enhanced. The proposed design technique can be applied to LDO regulator with any structure.

All the proposed works in this thesis consume very small quiescent currents whilst having a good balanced performance metrics when compared with the representative prior-art works. It has validated that they are useful for on-chip applications.

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1

INTRODUCTION

1.1 MOTIVATIONS

Power management integrated circuits (ICs) are normally employed to power up the functional blocks in battery-powered portable devices. Typical power management system consists of several subsystems including linear regulators, switching regulators, and control logics [1]. The control logics turn the subsystems on and off to optimize the power consumption of the whole system [2].

Switching regulator is one of the popular voltage regulators which are able to provide a wide range of output voltages [3-6]. One feature of the switching regulator is that the output voltage can be either lower or higher than the input voltage. This makes it popular to serve as an interface between two different voltages. Another feature, which is the most important one, of a switching regulator is its high power efficiency. The power efficiency of a switching regulator can attain higher than 80% when compared to a 5V to 3V linear regulator which can achieve only a maximum efficiency of 60%. However, as the voltage scales down, the switching regulators suffer a lower efficiency due to a larger loss in the post-rectifying filter [7]. Moreover, the switching regulators are not suitable for noise sensitive analog and RF blocks. The switching regulators also require more costly filtering components and larger board space. On the other hand, linear regulators are popular due to better

transient responses, less noise, simpler and cheaper. As a result, linear regulators are usually placed after switching regulators to improve their efficiency. LDO regulators fall into the category of linear voltage regulators with improved power efficiency by reducing the voltage differences between the input and output terminal.

LDO regulator is one of the most important power sources. The demand has been driven by the portable electronics market, industrial and automotive applications. The main objective is to provide a regulated voltage source to supply the noise sensitive functional blocks. Figure 1.1 shows that the output voltage of a battery discharges almost linearly with time. As a result, optimal circuit performance with reduced power supply which is time dependent cannot be obtained. Therefore, power management circuit is required to enhance the circuit performance. Furthermore, battery operated applications impose saving power as much as possible.

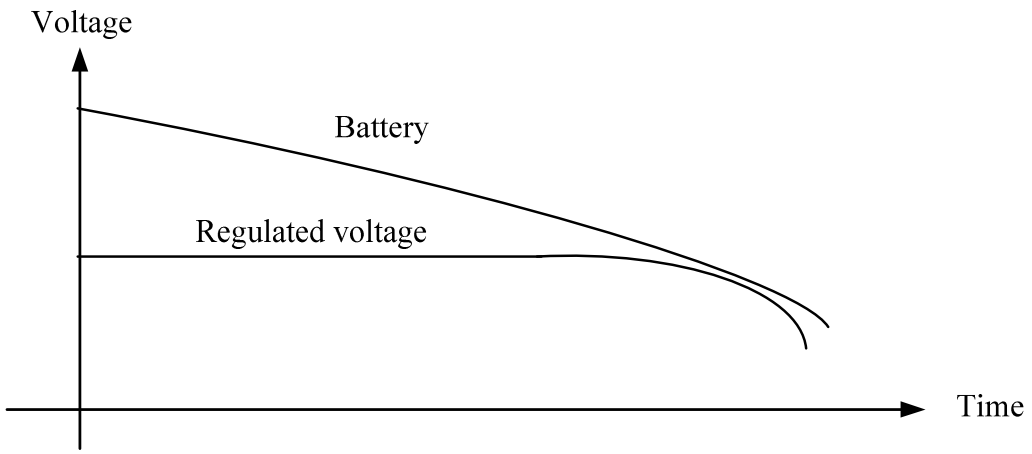


Figure 1.1: Regulated and unregulated voltage against time

As can be seen in Fig. 1.1, LDO regulator can provide a regulated voltage supply which is time independent. Therefore, optimal circuit performance can be achieved.

For battery-powered devices, such as cellular phones, camera recorders and laptops, low power consumption is the key to extend the battery life [8]. Thus, low voltage and ultra-low quiescent current are desired to improve the battery life. LDO voltage regulators have inherent advantages over the conventional linear voltage regulators, making them more suitable for on-chip power management system applications [9].

Figure 1.2 shows a typical structure of a switching regulator driving a few LDO regulators in a power management system [10]. The voltage from battery (V_{BAT}) is converted into four different voltage supplies (V_{o1}, V_{o2}, V_{o3} and V_{o4}) by a switching regulator. Some of the output voltages can be applied directly to the System-on-Chip (SoC) IC while some need to be post-regulated by external or on-chip LDO regulators. The voltage regulators require some capacitors to ensure the closed-loop stability and to achieve good line response as well as load transient response. Normally, an external LDO regulator requires an output capacitor, C_o, which cannot be integrated on-chip to maintain stability. On the other hand, the on-chip LDO regulator can be fully integrated by eliminating the large output capacitor. This makes it attractive for on-chip applications.

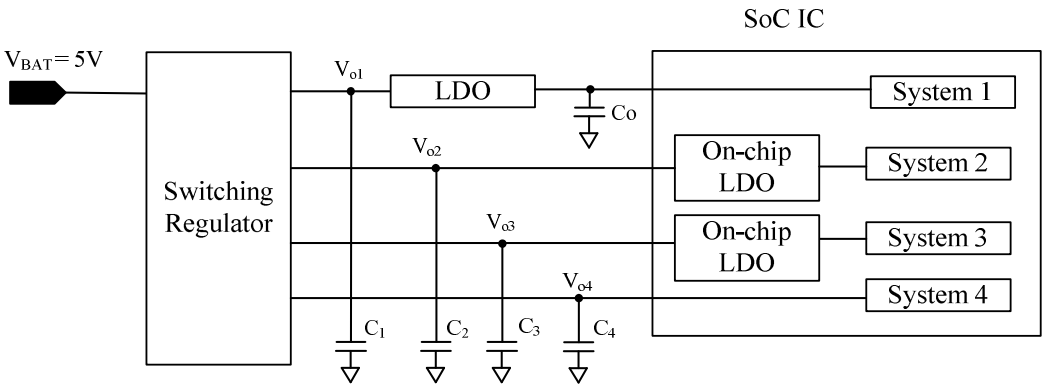


Figure 1.2: A typical SoC IC with power management unit

The emerging low voltage IC systems have been driven heavily by the rapid development of the semiconductor advanced technology. Moreover, the increasing demand for portable and battery operated products has forced the circuits to operate under lower voltage conditions. However, the power consumption of the IC system is not necessary to be lower under low voltage environment. The advanced technology provides the opportunities to integrate more functional blocks into one chip. In fact, the power consumption of the IC system is going to be larger than ever. When the LDO voltage regulator is used to provide a regulated voltage supply to the system, the low voltage in conjunction with high load current requirement makes the design of the LDO regulator a challenging task. Most often, the quiescent power of a LDO regulator increases when the output load current increases. As observed in the survey shown in Fig. 1.3, the quiescent current consumption is roughly proportional to the output load current. This indicates the design tradeoff between output load current and quiescent power. As a result, LDO regulator with low quiescent power and large output current is highly desirable.

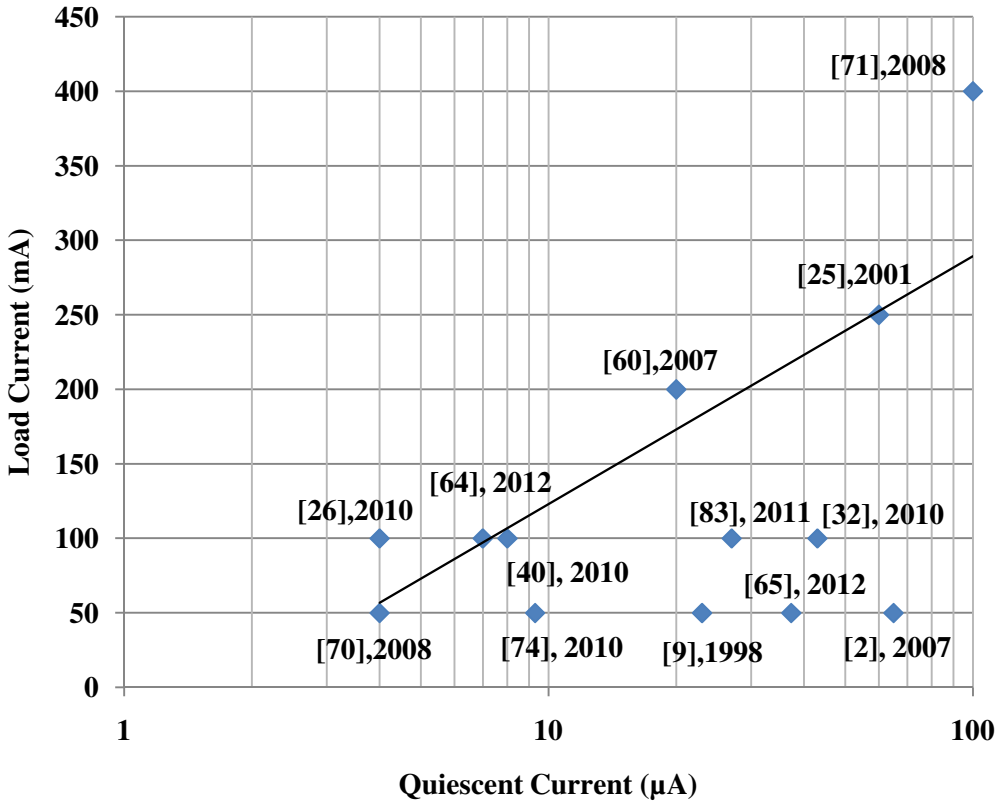


Figure 1.3: Load current verses quiescent current of reported works

In addition, the higher level of integration in portable devices also pushes LDO regulators to deliver larger load current. For example, the load current demanded by an on-board circuitry can vary from below 0.1mA up to a few hundreds mA [11] in cellular phones. It is common to see that there will be more than one LDO regulator are required to supply different sub-systems [12]. Figure 1.4 shows a block diagram of a power management sub-system IC for code division multiple access (CDMA) handset which includes 11 LDO circuits, control logic, bandgap reference voltage detectors, battery charger and 32-kHz oscillator [12]. Since the IC needs to supply different voltages to different components in the sub-system, many LDO regulators with different output voltages and currents are required.

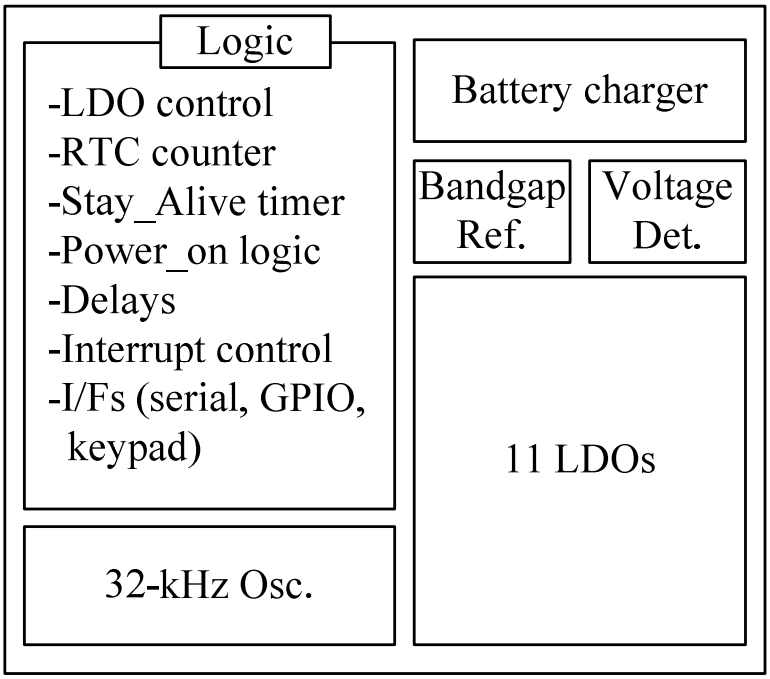


Figure 1.4: IC block diagram of a CDMA handset [12]

As shown in Table 1.1, the output voltage ranges from 1.5 V to 3.0 V while the output current ranges from 50 mA to 180 mA depending on the requirements. Therefore, each LDO regulator has to be optimized to suit the specifications. However, in the power management sub-systems IC, those components that require the same supply voltage level can be powered by a very low-quiescent and high-drive LDO regulator such that the number of LDO regulators can be reduced. This benefits the reduction of area-dominant power devices as well as the simplification of power management IC control algorithm. However, it is desirable to have a fast transient response property because some of the blocks may need a fast-transient supply in a shared power source environment.

TABLE 1.1: EXEMPLARY REQUIRED LDO REGULATORS [12]

	LDO	V_{OUT} (V)	I_{OUT} (mA)
1	Baseband Digital	2.9	150
2	Baseband Analog	2.5	50
3	Coin Cell, SRAM	3.0	50
4	Audio	2.9	180
5	Vibrator	2.9	150
6	Baseband core	2.6	50
7	RF RX1	2.9	100
8	RF TX	2.9	150
9	RF TX2	2.9	50
10	RF Option	2.9	50
11	Other option	1.5	150

The intrinsic design issues of a low power, low voltage and fast transient response LDO regulator include the stability, the maximum output load current and the regulation performance metric. It is not easy to achieve stability in low quiescent environment. This is because the parasitic poles are potentially located at low frequencies. To push the poles to higher frequencies, the quiescent current has to be increased. In order to provide a higher output load current, the size of the power transistor has to be larger. As a result, the parasitic poles will be located at even lower frequencies. Besides, the maximum output load current is restricted by the low voltage environment. This gives the fundamental motivation of the research project to design the low-quiescent current and high-efficient LDO regulators.

Finally, low voltage circuit tents to limit the regulating performance of a voltage regulator due to the headroom problem. The conventional circuit design techniques, such as cascode gain structure, source follower and so forth, become restrained [13-

17]. Therefore, this gives another key motivation of the research project to design the low-voltage LDO regulators.

1.2 OBJECTIVES

The objectives of this thesis are (i) to investigate and develop an advanced frequency compensation technique to enhance the small-signal as well as large-signal performance of the multistage amplifier which is dedicated to drive a large capacitive load, (ii) to investigate effective circuit techniques as well as architectures which can be used to design low-power and high-performance output-capacitor LDO (OC-LDO) regulators as well as output-capacitorless LDO (OCL-LDO) regulators in nanometer CMOS technologies dedicated to the battery-operated and on-chip applications, (iii) to conduct the analysis of a series of the proposed LDO regulator circuits and (iv) to test the silicon prototypes implemented in 65 nm CMOS technology. The ultimate goals are to achieve key performance metric on the basis of application specific LDO regulators. These include low power consumption, low voltage operation, low circuit complexity, fast transient response and high output load current in nanometer CMOS technologies.

1.3 CONTRIBUTIONS

The main contributions of this research work in this report are summarized as follows:

(i) Investigate a new area-efficient and power-bandwidth-efficient frequency compensation technique for the design of a three-stage amplifier which is able to drive a large capacitive load arising from the effective input capacitance of power device used in OC-LDO regulator. The proposed frequency compensation technique permits the amplifier to achieve the highest load capacitance to compensation capacitance ratio, and to offer excellent small-signal and large-signal performance metric.

(ii) Investigate a new push-pull composite power transistor for OCL-LDO regulator design. The proposed LDO regulator can operate in a sub-1V environment and achieve fast transient responses.

(iii) Investigate a new dynamic-biased composite power transistor which permits the realization of a low-quiescent high-drive OC-LDO regulator with fast transient responses. The proposed LDO regulator achieves a good load current to quiescent current ratio whist having good transient responses.

(iv) Investigate a new architecture with adaptive power transistors circuit technique and its application to the design of an ultra-low-quiescent OCL-LDO regulator. The proposed LDO regulator is able to achieve ultra-low-quiescent current consumption whilst maintaining good stability in multistage LDO circuit architecture. This overcomes the stability issue of the conventional design in multistage LDO topologies at low biasing current.

(v) Investigate a new low-impedance loading network circuit technique for the design of low-quiescent OCL-LDO regulator. The result suggests that the proposed circuit technique eliminates the minimum loading requirement encountered in conventional OCL-LDO regulators. It can also be applied to other OC-LDO regulators as well.

1.4 ORGANIZATION OF THE REPORT

This report is organized in seven chapters as follows.

Chapter 2 reviews the representative frequency compensation techniques that are commonly used in LDO regulator design. The structures of conventional and OCL-LDO regulators are also discussed. Fundamental issues of stability and transient response are investigated and discussed such that limitations and tradeoffs can be understood.

Chapter 3 presents an area-efficient and power-bandwidth-efficient frequency compensation technique for a three-stage amplifier that drives a large capacitive load. The proposed multistage amplifier with the advanced frequency compensation technique can be used as an error amplifier which drives a large power transistor in high-drive LDO regulator.

Chapter 4 introduces two LDO regulators with composite power transistor. It starts with a brief review of Class-A composite power transistor followed by a proposed push-pull composite power transistor with slew-rate enhancement. Besides, a new composite power transistor with dynamic biasing technique is also presented in this chapter. To demonstrate the usefulness of the proposed composite power transistor circuit structures, they have been employed in the respective OCL-LDO and OC-LDO regulator design. Simulation and measurement results show excellent transient response of both composite power transistor based LDO regulators when compared with that of the counterparts.

Chapter 5 presents an ultra-low quiescent current OCL-LDO regulator circuit architecture using adaptive power transistors. The proposed architecture is developed to reduce the quiescent power and to improve the stability at low load current condition. The circuit operation and the advantages of the proposed design are detailed in the chapter.

Chapter 6 presents a new ac low-impedance loading network circuit technique to enhance the circuit stability and current efficiency of OCL-LDO regulator at low load current condition.

Chapter 7 gives the concluding remarks as well as recommendations for future works.

CHAPTER 2

REVIEW OF FREQUENCY COMPENSATION TECHNIQUES AND LDO REGULATORS

2.1 INTRODUCTION

In this chapter, the frequency compensation techniques and LDO regulators are reviewed. Basically, LDO regulators can be viewed as an amplifier with negative feedback structure [18]. Of most importance, the frequency compensation techniques for the design of LDO regulators are firstly studied in details. Subsequently, different types of LDO regulator are then described.

2.2 REVIEW OF FREQUENCY COMPENSATION TECHNIQUES

LDO regulators use the negative feedback loop to ensure the output voltage is constant at different loading conditions. In all feedback system, stability has to be considered and frequency compensation techniques are employed to ensure the stability of the system. LDO regulator can be viewed as a multistage amplifier in negative feedback configuration [18]. The choice of the frequency compensation technique will greatly affect the performance of the LDO regulators in terms of speed (transient responses), silicon area (size of compensation capacitor) and power

consumption (quiescent current). Therefore, an effective frequency compensation technique, especially for large capacitive load, needs to be explored for LDO regulator applications.

This chapter reviews different existing frequency compensation techniques. In general, frequency compensation is achieved by pole splitting, pole-zero cancellation, feedforward technique and so forth. This review focuses on frequency compensation techniques commonly employed in LDO regulators design. In this section, there are two common assumptions made for all topologies.

1. All the gain stages are much larger than one ($g_{mi}R_{oi}$ >>1 and $g_{mL}R_{oL}$ >>1).
2. The compensation capacitors and the loading capacitor are much larger than the lumped output parasitic capacitor (C_L and C_{mi} >> C_{pi}).

2.2.1 SINGLE MILLER COMPENSATION (SMC)

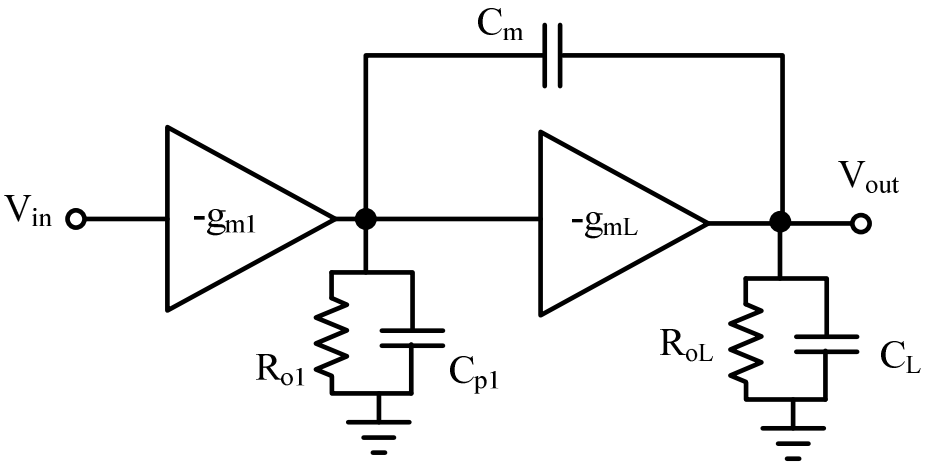


Figure 2.1: Topology of Single Miller Compensation amplifier

Figure 2.1 shows the topology of the two-stage Single Miller Compensation (SMC) amplifier. The SMC is one of the most commonly used frequency compensation technique in amplifier design due to its simple structure. The transfer function of the SMC is given by

$$A_{V(SMC)} = \frac{g_{m1} g_{mL} R_{o1} R_{oL} \left(1 - s\frac{C_m}{g_{mL}}\right)}{\left(1 + sC_m g_{mL} R_{o1} R_{oL}\right)\left(1 + s\frac{C_L}{g_{mL}}\right)} \tag{2.1}$$

From Eq. (2.1), there are two left-hand-plane (LHP) poles and one right-hand-plane (RHP) zero. The dominant pole, non-dominant pole and RHP zero are given by

$$p_{-3dB} = \frac{1}{C_m g_{mL} R_{o1} R_{oL}} \tag{2.2}$$

$$p_2 = \frac{g_{mL}}{C_L} \tag{2.3}$$

$$z_1 = -\frac{g_{mL}}{C_m} \tag{2.4}$$

To ensure stability, p_2 and z_1 have to be located beyond the unity-gain frequency (UGF). This can be achieved by increasing C_m and pushing p_{-3dB} to a lower frequency. However, the GBW=g_{m1}/C_m and z_1 is reduced at the same time. Alternatively, the stability can be achieved by increasing g_{mL} which will move both p_2 and z_1 to a higher frequency at a price of higher power consumption. By setting p_2 to be double of GBW, the dimension of C_m can be obtained as

$$C_m = 2\frac{g_{m1}}{g_{mL}} C_L \tag{2.5}$$

The dimension is obtained based on the assumption that z_1 is located at a higher frequency than p_2. As a result, the ratio g_{m1}/g_{mL} has to be small in order to fulfill the condition ($C_m<C_L$). If z_1 is placed before p_2, the gain margin will be degraded and the amplifier maybe unstable. It can be seen that the compensation capacitor is directly proportional to the size of C_L which implies that SMC is not suitable for large capacitive load applications.

2.2.2 CASCODE COMPENSATION

Figure 2.2 shows the structure of cascode compensated amplifier [19]. In fact, the cascode compensation can be viewed as Single Miller compensation with current buffer to block feedforward path.

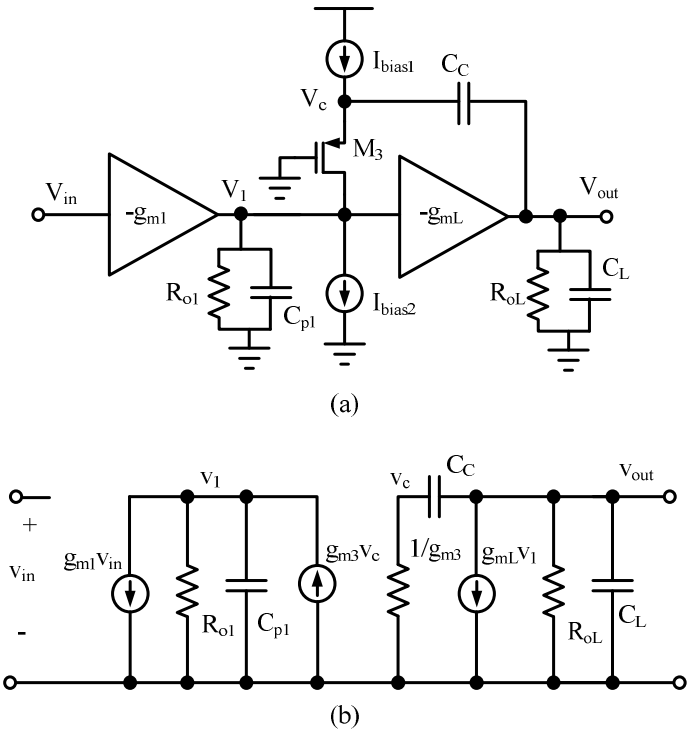


Figure 2.2: (a) Topology and (b) Small-signal model of Cascode Compensation amplifier

The transfer function is shown as follow:

$$A_{V(Cascode)} = \frac{g_{m1} g_{mL} R_{o1} R_{oL}}{1 + s\left(R_{o1} C_{p1} + R_{oL} C_L + R_{oL} C_C + g_{mL} R_{oL} R_{o1} C_C\right) + s^2 R_{o1} R_{oL} C_{p1} \left(C_C + C_L\right)} \quad (2.6)$$

Other than the assumptions stated previously, it is also assumed as follows:

1. g_{m3} is much larger than g_{m1} and g_{mL}.
2. Input impedance of the current buffer is equal to the reciprocal of its transconductance ($1/g_{m3}$).

If these conditions are not met, there will be a parasitic zero and a high frequency pole that appear in the transfer function. From the transfer function, it is interesting to notice that the RHP zero is being eliminated in this SMC amplifier due to the feedforward path whereas the poles are real and widely spaced. They are given as

$$p_{-3dB} \approx \frac{1}{C_C R_{o1} g_{mL} R_{oL}} \quad (2.7)$$

$$p_2 \approx \frac{g_{mL} C_C}{\left(C_C + C_L\right) C_{p1}} \quad (2.8)$$

From Eq. (2.8), the non-dominant pole p_2 is approximately located at C_C/C_{p1} times higher than that of the SMC technique. On the other hand, the GBW=g_{m1}/C_C is same as the SMC, resulting in a better phase margin. The extra phase margin of cascode compensation can be used to trade for smaller power and/or area. Therefore, the cascode compensation offers better power-efficient and area-efficient performance metric when compared to SMC technique. However, if there is any mismatch between the current sources (I_{bias1} and I_{bias2}), the effectiveness of the cascode

compensation will be degraded. Besides, the requirement of $g_{m3} >> g_{m1}$ and g_{mL} (to avoid parasitic zero and pole), also increases the power consumption.

2.2.3 NESTED MILLER COMPENSATION (NMC)

Both SMC (Fig. 2.1) and cascode compensation (Fig. 2.2) is a two-stage amplifier which might not be able to provide enough voltage gain and voltage swings in low-voltage design. Instead, three-stage amplifier is commonly used to boost the gain by increasing the number of stages. Figure 2.3 shows the topology of the Nested Miller Compensation (NMC) amplifier [20]. NMC is a well-established pole splitting technique for multistage amplifier compensation. In a three-stage NMC amplifier, it consists of three gain stages and two compensation capacitors. These two compensation capacitors are employed to split the poles of the amplifier to ensure the stability. In fact, the second and the third gain stage can be viewed as a two-stage SMC amplifier that is compensated by C_{m2} and form a one pole system. g_{m1} and the equivalent amplifier (formed by g_{m2} and g_{mL}) form another two-stage SMC amplifier which is compensated by C_{m1}.

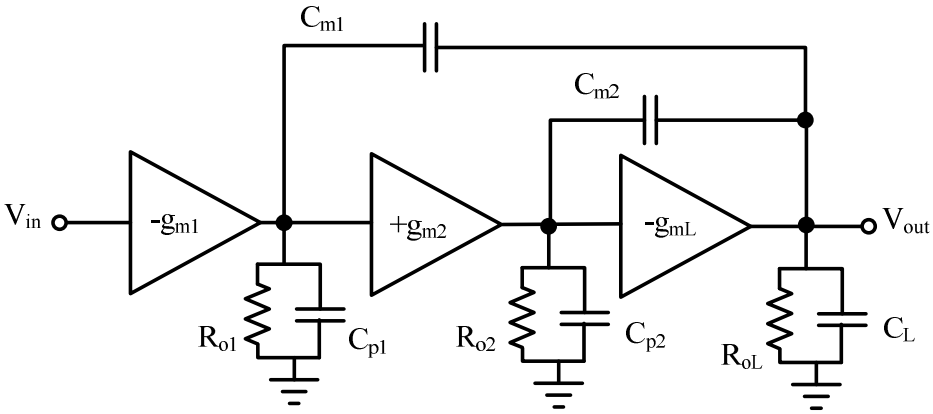


Figure 2.3: Topology of Nested Miller Compensation amplifier

The transfer function of NMC amplifier is given by

$$A_{V(NMC)} = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\left(1 - s\frac{C_{m2}}{g_{mL}} + s^2\frac{C_{m1}C_{m2}}{g_{m2}g_{mL}}\right)}{\left(1 + sC_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\right)\left(1 + s\frac{C_{m2}\left(g_{mL} - g_{m2}\right)}{g_{m2}g_{mL}} + s^2\frac{C_L C_{m2}}{g_{m2}g_{mL}}\right)} \tag{2.9}$$

The open-loop gain and GBW of the amplifier is shown as

$$A_{dc} = g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL} \tag{2.10}$$

$$GBW = \frac{g_{m1}}{C_{m1}} \tag{2.11}$$

The transfer function has one RHP zero and one LHP zero. The zeros are located at

$$z_{1,2} = -\frac{g_{m2}}{2C_{m1}} \mp \sqrt{\left(\frac{g_{m2}}{2C_{m1}}\right)^2 + \frac{g_{m2}g_{mL}}{C_{m1}C_{m2}}} \tag{2.12}$$

The denominator in (2.9) can be further simplified, if g_{mL} is much larger than g_{m2}. In this case the NMC amplifier should have a third-order Butterworth frequency response with unity feedback configuration [18]. Therefore, the dimension condition for C_{m1} and C_{m2} are obtained as follows:

$$C_{m1} = 4\frac{g_{m1}}{g_{mL}}C_L \tag{2.13}$$

$$C_{m2} = 2\frac{g_{m2}}{g_{mL}}C_L \tag{2.14}$$

With (2.13) and (2.14), the non-dominant complex poles are located at

$$p_{2,3} = -\frac{g_{mL}}{2C_L} \pm j\frac{g_{mL}}{2C_L} \tag{2.15}$$

and the damping factor of the complex pole is $1/\sqrt{2}$. The stated dimension conditions in (2.13) and (2.14) imply that the values of the compensation capacitors are linearly depending on C_L. In other words, this scheme requires a larger compensation capacitor for a larger C_L. Equations (2.13) and (2.14) also show that C_{m1} and C_{m2} can be made smaller when a larger g_{mL} is used. However, in a low-power design, increasing g_{mL} is not desirable. The condition $g_{mL} >> g_{m1}$ and g_{m2} is very important and critical to the stability of NMC amplifier. This is to ensure the output small-signal current is much larger than the feedforward current such that the zeros give negligible effect to the stability. If g_{mL} is smaller that g_{m1} or g_{m2}, a RHP zero or peaking effect due to small damping factor of the complex pole appears. This makes the amplifier unstable. The nesting topology of the compensation capacitor reduces the bandwidth substantially. Although the NMC is not a power and area-efficient technique, it is relatively simple to be implemented and the stability of the amplifier can be ensured.

2.2.4 DAMPING-FACTOR-CONTROL FREQUENCY COMPENSATION (DFCFC)

Figure 2.4 shows the topology of the Damping-Factor-Control Frequency Compensation (DFCFC) amplifier [21]. As can be seen in Fig. 2.4, DFCFC removes the internal compensation capacitor C_{m2} in NMC amplifier and replaces it with a DFC block which consists of g_{m4} and C_{m2} to control the damping factor of the non-dominant poles to make the amplifier stable.

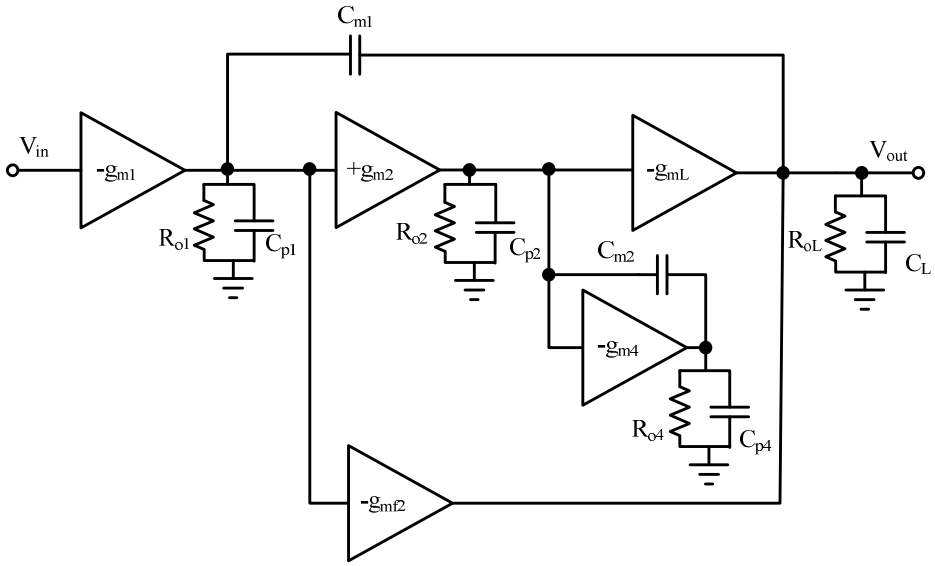


Figure 2.4: Topology of Damping-Factor-Control Compensation amplifier

The transfer function is given as follows:

$$A_{V(DFCFC)} = \frac{A_{dc}\left(1+s\frac{C_{p2}g_{mf2}-C_{m1}g_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}-s^2\frac{C_{p2}C_{m1}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_Lg_{m4}}{g_{m2}g_{mL}+g_{mf2}g_{m4}}+s^2\frac{C_{p2}C_L}{g_{m2}g_{mL}+g_{mf2}g_{m4}}\right)} \quad (2.16)$$

Other than the assumptions stated previously, it is also assumed as follows:

1. $g_{m4}R_{o4}$ is much larger than 1.
2. C_{p4} is very small and can be ignored.
3. For simplicity, both compensation capacitors (C_{m1} and C_{m2}) are set to be equal to each other.

The open-loop gain, dominant pole and GBW are given by

$$A_{dc} = g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL} \tag{2.17}$$

$$p_{-3dB} = \frac{1}{C_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}} \tag{2.18}$$

$$GBW = \frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right) \tag{2.19}$$

whereas the stability conditions can be established as follows:

$$g_{mf2} = g_{mL} \tag{2.20}$$

$$g_{m4} = \beta\left(\frac{C_{p2}}{C_L}\right)g_{mL} \tag{2.21}$$

$$C_{m1} = \frac{4}{\beta}\left(\frac{g_{m1}}{g_{mL}}\right)C_L \tag{2.22}$$

$$C_{m1} \geq C_{m2} > C_{p2} \tag{2.23}$$

$$\text{where } \beta = 1 + \sqrt{1 + 2\left(\frac{C_L}{C_{p2}}\right)\frac{g_{m2}}{g_{mL}}} \tag{2.24}$$

From the transfer function (2.16), the structure results in a pair of complex non-dominant poles and the damping factor can be controlled by g_{m4}. This topology helps to increase the bandwidth of the amplifier, especially when driving a large

capacitive load. The size of compensation capacitor is reduced as it is proportional to the square root of C_L. As a result, the transient responses are enhanced. However, the operating point of the DFC block is outside the feedback loop and is very sensitive to process variation. As a result, additional control circuitry is required to make sure the correct operation point [22].

2.2.5 ACTIVE-FEEDBACK FREQUENCY COMPENSATION (AFFC)

Figure 2.5 shows the topology of Active-Feedback Frequency Compensation (AFFC) amplifier [23]. A high speed block (HSB) is added to improve the bandwidth by directing the high frequency signal to bypass the slow response high gain block (HGB). AFFC makes use of an active capacitive feedback network in contrast to the passive capacitive feedback network. In fact, AFFC can be viewed as an extended version of cascode compensation if the HGB is treated as a single high gain stage which is compensated by C_{m2}. An active positive gain stage (current buffer) is added in series with the dominant compensation capacitor. In addition, the HSB removes the RHP zero by blocking the feedforward signal current.

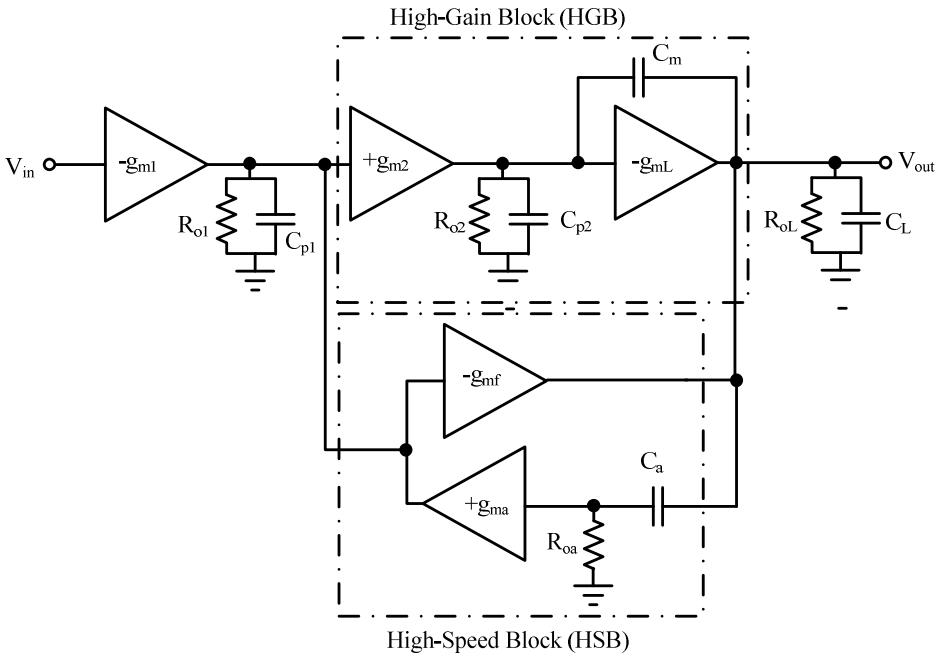


Figure 2.5: Topology of Active-Feedback-Frequency Compensation amplifier

The transfer function of AFFC amplifier can be expressed as

$$A_{V(AFFC)} = \frac{g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\left(1+s\frac{C_a}{g_{ma}}\right)}{\left(1+sC_a g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}\right)\left(1+s\frac{C_{p1}C_L}{C_a(g_{mf}-g_{m2})}+s^2\frac{C_{p1}C_L}{g_{ma}(g_{mf}-g_{m2})}\right)} \quad (2.25)$$

Other than the assumptions stated previously, it is also assumed as follows:

1. Input impedance of the current buffer is equal to the reciprocal of its transconductance ($1/g_{ma}$).
2. For simplicity, both compensation capacitors are set to be equal to each other.
3. $g_{ma}R_{o1}$ is much larger than 1.

The open-loop gain, dominant pole and GBW of the amplifier are given as follows:

$$A_{dc} = g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL} \quad (2.26)$$

$$p_{-3dB} = \frac{1}{C_a g_{m2} g_{mL} R_{o1} R_{o2} R_{oL}} \tag{2.27}$$

$$GBW = \frac{g_{m1}}{C_a} \tag{2.28}$$

The dimension condition for g_{ma} and C_a are shown as follows:

$$g_{ma} = 4 g_{m1} \tag{2.29}$$

$$C_a = \frac{4}{N} \frac{g_{m1}}{g_{mL}} C_L \tag{2.30}$$

$$\text{where } N = \sqrt{8\left(\frac{C_L}{C_1}\right)\left[\frac{g_{m1}\left(g_{mf} - g_{m2}\right)}{{g_{m3}}^2}\right]} \tag{2.31}$$

Similar to DFCFC, (2.30) and (2.31) show that the compensation capacitor is inversely proportional to square root of C_L. Hence, AFFC is effective for large capacitive load. The bandwidth improvement of the AFFC amplifier increases when driving a large capacitive load. However, similar to cascode compensation, the implementation of the current buffer is highly affected by the mismatch of the current sources.

2.2.6 SUMMARY OF FREQUENCY COMPENSATION TECHNIQUES

All the frequency compensation techniques discussed in this section are summarized in Table 2.1. The stability conditions have to be met in order to stabilize the amplifier. It can be seen that the cascode based compensation and DFCFC are effective for large capacitive load (larger GBW or smaller compensation capacitors) which is suitable for LDO regulator applications. However, in general, these types of compensation techniques are more complex than the Miller based compensations.

TABLE 2.1: SUMMARY TABLE OF FREQUENCY COMPENSATION TECHNIQUES

Topology	dc gain	Stability Conditions	GBW	Driving Large C_L	Complexity
SMC	$g_{m1}g_{mL}R_{o1}R_{oL}$	$C_m = 2\frac{g_{m1}}{g_{mL}}C_L$	$0.5\left(\frac{g_{mL}}{C_L}\right)$	moderate	simple
Cascode	$g_{m1}g_{mL}R_{o1}R_{oL}$	$g_{m3} \gg g_{m1}$ and g_{mL} $C_C = \sqrt{2\frac{g_{m1}}{g_{mL}}C_{p1}C_L}$	$0.5\left(\frac{g_{mL}}{C_L}\right)$	excellent	moderate
NMC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}$	$g_{mL} \gg g_{m1}$ and g_{m2} $C_{m1} = 4\frac{g_{m1}}{g_{mL}}C_L$ $C_{m2} = 2\frac{g_{m2}}{g_{mL}}C_L$	$0.25\left(\frac{g_{mL}}{C_L}\right)$	poor	moderate
DFCFC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}$	$g_{mf2} = g_{mL}$ $C_{m1} = \frac{4}{\beta}\frac{g_{m1}}{g_{mL}}C_L$ $C_{m1} \geq C_{m2} > C_{p2}$ $g_{m4} = \beta\frac{C_{p2}}{C_L}g_{mL}$ $\beta = 1+\sqrt{1+2\left(\frac{C_L}{C_{p2}}\right)\frac{g_{m2}}{g_{mL}}}$	$\frac{\beta}{4}\left(\frac{g_{mL}}{C_L}\right)$	excellent	complex
AFFC	$g_{m1}g_{m2}g_{mL}R_{o1}R_{o2}R_{oL}$	$g_{mf} = g_{m2}$ $C_a = \frac{4}{N}\frac{g_{m1}}{g_{mL}}C_L$ $C_a \geq C_m > C_{p2}$ $g_{ma} = 4g_{m1}$ $N = \sqrt{8\left(\frac{C_L}{C_1}\right)\left[\frac{g_{m1}\left(g_{mf}-g_{m2}\right)}{{g_{m3}}^2}\right]}$	$\frac{N}{4}\left(\frac{g_{mL}}{C_L}\right)$	excellent	complex

2.3 REVIEW OF LDO REGULATORS

This section begins with the introduction of the conventional LDO regulators. Some of the intrinsic problems such as stability and transient responses issues are discussed. Design techniques that tackle the problems have been reviewed. The advantages and limitations of each technique are detailed.

2.3.1 CONVENTIONAL LDO REGULATORS

The structure of the conventional LDO regulator, as shown in Fig. 2.6, is composed of an error amplifier, a voltage buffer, a power transistor, a resistive feedback network, and a voltage reference [24].

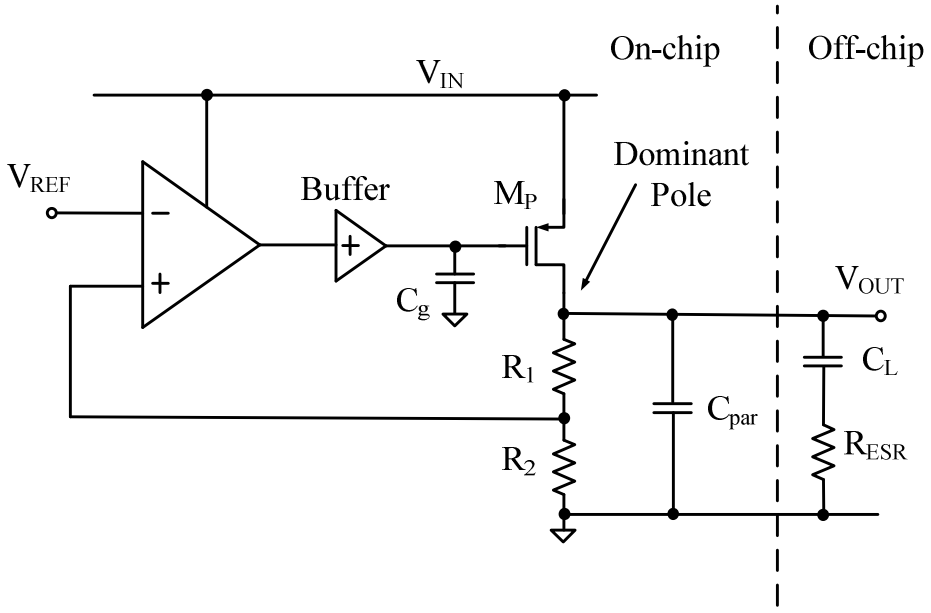


Figure 2.6: Conventional LDO regulator

The input of the error amplifier is driven by a stable dc reference generated by the voltage reference. The error amplifier, power transistor and feedback network form a regulation loop. The output voltage is sensed and compared with a stable voltage

reference. A control signal is then generated at the output of error amplifier and buffered to drive the power transistor and regulate output. The dropout voltage defines the minimum supply voltage in order to regulate the required output voltage.

Referring to Fig. 2.6, the structure is intrinsically unstable as there are three poles at the output of the error amplifier, the voltage buffer, and the LDO regulator, respectively. In order to keep the system stable, a large off-chip capacitor is used to create a very low frequency pole at the output of LDO regulator. In addition, the zero created by the off-chip capacitor and its equivalent series resistance (ESR) is used to cancel the pole at the output of the error amplifier [9], [25]. The voltage buffer is employed to isolate the large output resistance of the error amplifier from the input capacitance of the power transistor. The voltage buffer is often realized by a source follower, taking advantage of its circuit simplicity. Except with high supply, high output swing is difficult to achieve in low voltage LDO regulator design.

2.3.1.1 STABILITY CONSIDERATIONS

The stability of a conventional LDO regulator can be illustrated in Fig. 2.7. The dominant pole, p_{-3dB}, is located at the output of the LDO regulator. The zero, z_1, is used to cancel the pole, p_2, located at the output of the error amplifier. The stability is achieved by locating the non-dominant pole p_3, located at the output of voltage buffer, well beyond the unity-gain frequency (UGF). However, when the loop gain of the LDO regulator is too high, UGF will become higher than p_3, resulting in unstable condition.

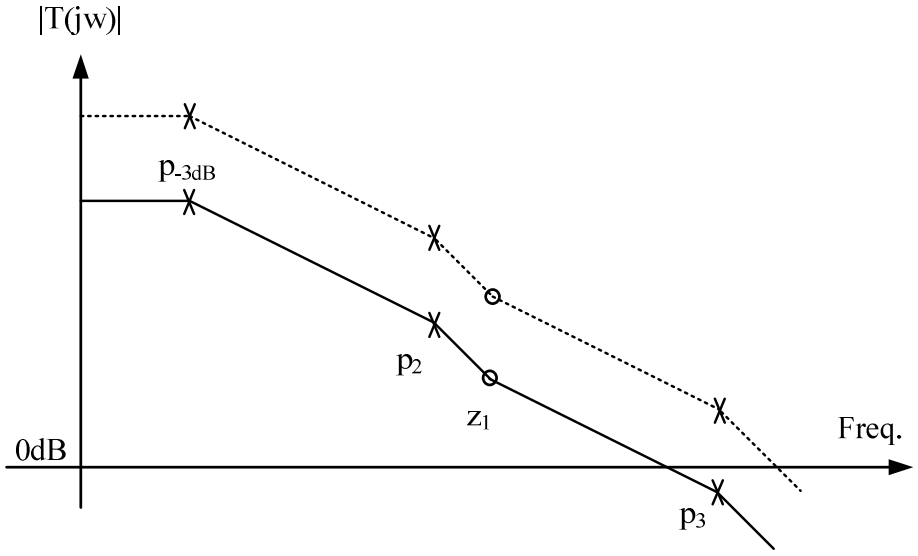


Figure 2.7: Loop gain of conventional LDO regulator

In order to deliver high load current and achieve low dropout voltage in LDO regulator design, a large size of PMOS power transistor is required. As a result, the larger capacitance of the PMOS power transistor shifts p_3 to a lower frequency. To push the pole to a higher frequency, the quiescent current has to be increased, leading to higher power consumption. Therefore, a low quiescent current in conjunction with high output current LDO regulator is highly desirable.

2.3.1.2 TRANSIENT RESPONSE CONSIDERATIONS

The transient response time [9] can be estimated as

$$t_r = \frac{1}{BW_{cl}} + C_g \frac{\Delta V}{I_{sr}} \tag{2.32}$$

where BW_{cl} is the closed-loop bandwidth of the system, C_g is the associated gate capacitance of power transistor, ΔV is the voltage change associated with the C_g and I_{sr} is the slew rate limited current. For fast transient response, a large closed-loop bandwidth and slew rate are needed. However, the stability issue limits the extension of the closed-loop bandwidth whereas the slew rate increases the power consumption of the voltage buffer. Both factors cause the tradeoff in low-power design.

2.3.2 LDO REGULATORS WITH DYNAMIC BIASING

To overcome the problems, some designs based on dynamic biasing scheme are reported. In [9], a buffer stage with dynamic biasing is introduced. As shown in Fig. 2.8, the biasing current of the buffer stage is made proportional to the output load current such that the slew rate is independent of the biasing current of the voltage buffer. In [26], a dynamic biasing circuit technique is applied to the design of error amplifier in the LDO regulator. As shown in Fig. 2.8, the biasing current of the error amplifier is made proportional to the output load current. As a consequence, the current efficiency at light load is improved while the bandwidth of the error amplifier is enhanced at high load current. Moreover, a good transient response can be obtained without jeopardizing the current efficiency. It is obvious that dynamic biasing is a good design technique to achieve low quiescent power while

maintaining the good performance of the circuits. This approach improves the current efficiency at low load current significantly.

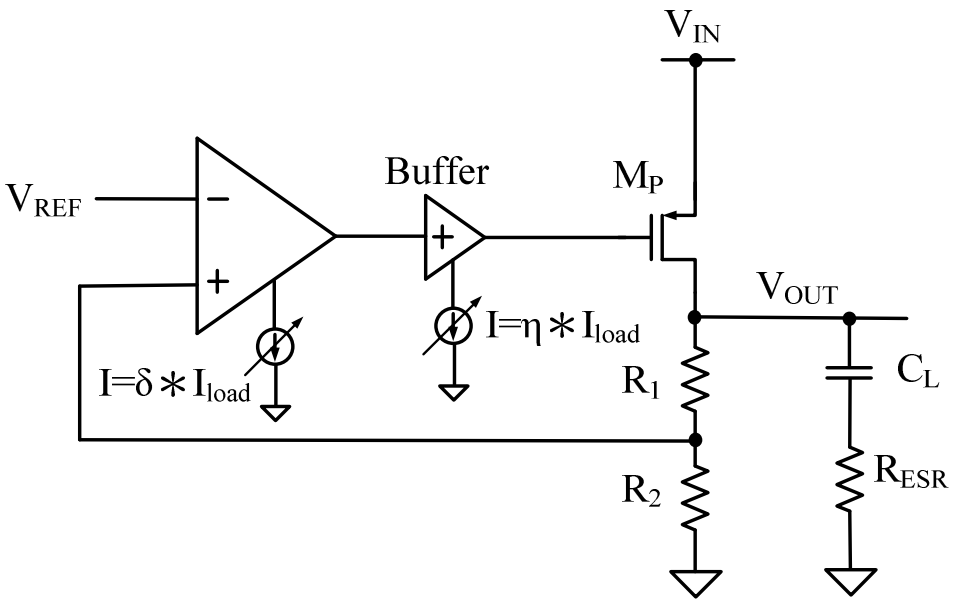


Figure 2.8: LDO regulator with dynamic biasing technique

2.3.3 LDO REGULATORS WITH CURRENT BOOSTING

It is also observed that large current is only needed during the transient events but not in the steady state. Therefore, a voltage buffer with a current-boosting circuit [27] is introduced. The basic concept of voltage buffer with current boosting is depicted in Fig. 2.9. As can be seen in Fig. 2.9, the biasing current of the voltage buffer is momentarily increased against the load changes such that it provides large momentarily current to charge and discharge the gate of the power transistor. The key advantage is that the transient response of the LDO regulator will be greatly improved without dissipating a large quiescent power. This involves the design of a fast detection circuit to detect the rapid changes of output load current. It may increase the circuit complexity. Of most economical implementation, the capacitive-

coupling technique formed by a pair of RC components is employed to realize the bias-boosting circuitry. This technique permits the quiescent current to remain low at steady state but at the expense of silicon area.

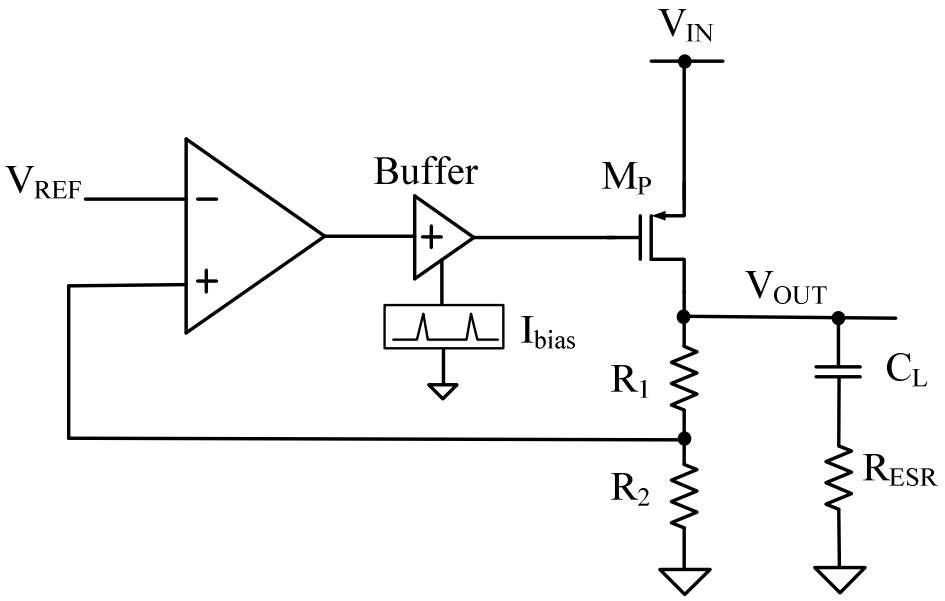


Figure 2.9: LDO regulator with current boosting

Alternatively, an internal zero [28] can be generated to track the second pole more closely instead of an external zero which is defined by the external capacitor and its ESR. Turning to other implementation [29], a wideband g_m-enhanced MOS composite transistor is reported to realize a power transistor of a linear voltage regulator. The regulator is able to deliver a high current of 735 mA with very fast response. However, the quiescent current is relatively large due to the Class-A operation, reducing the current efficiency at light loads. Therefore, a low quiescent power and fast transient LDO regulator whilst maintaining the high output current driving capability gives one of the research motivations in this project.

2.3.4 OUTPUT-CAPACITORLESS LDO (OCL-LDO) REGULATORS

OC-LDO regulators usually rely on a large off-chip capacitor to form part of the frequency compensation in the design. The large off-chip capacitor may not be favorable for the embedded voltage regulators for on-chip applications. This increases the popularity on the research of OCL-LDO regulators. An exemplary structure of an OCL-LDO regulator is shown in Fig. 2.10.

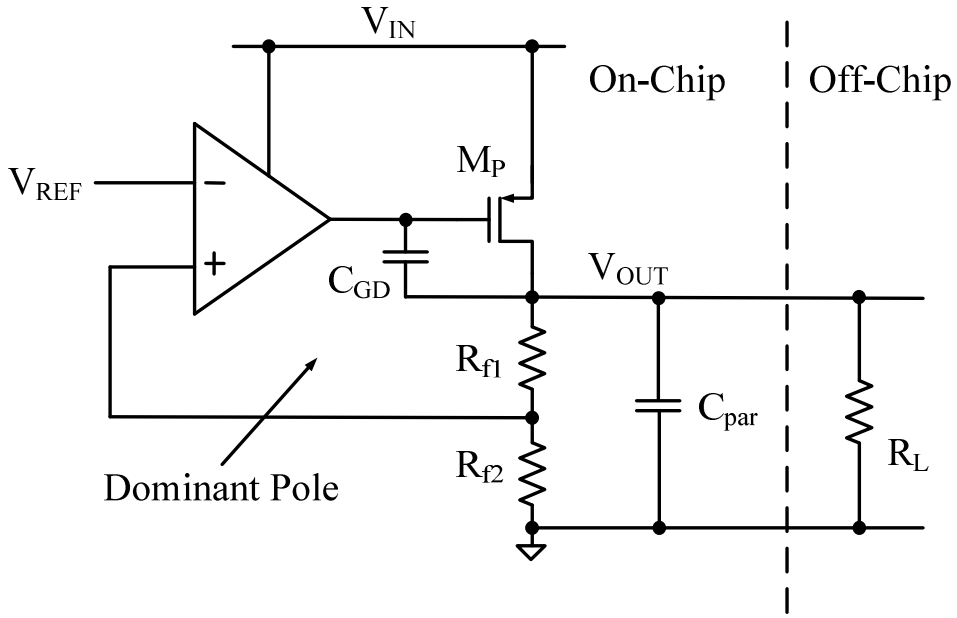


Figure 2.10: Output-capacitorless LDO regulator

The OCL-LDO structure is similar to that of OC-LDO regulator without the large output capacitor. Therefore, OCL-LDO regulator cannot rely on the output capacitor for stability purpose.

2.3.4.1 STABILITY CONSIDERATIONS

The OCL-LDO regulator has at least two poles at the output of error amplifier and output of LDO regulator, respectively. The stability of an uncompensated OCL-LDO regulator can be illustrated in Fig. 2.11. p_1 is located at the output of error amplifier while p_2 is a load-dependent pole which is located at the output of LDO regulator. As shown in Fig. 2.11, the OCL-LDO regulator is intrinsic unstable because there are two poles appear within UGF.

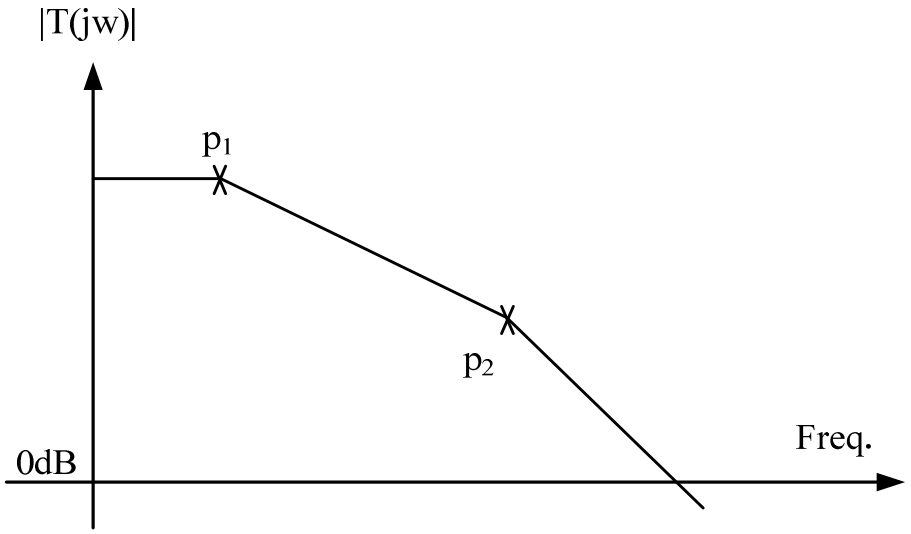


Figure 2.11: Loop gain of conventional LDO regulator

In order to reduce the dropout voltage of the LDO regulator at heavy load condition, the size of the power transistor has to be very large. The gate-drain capacitance, C_{GD}, of the pass transistor becomes large and it also serves as a Miller capacitor which increases the effective input capacitance of the pass transistor. The pole location of p_1 is given by

$$p_1 = \frac{1}{R_1 \cdot \left(C_1 + C_{GD} g_{mp} R_{OUT}\right)} \tag{2.33}$$

where g_{mp} is the transconductance of M_P and $R_{OUT}=(R_{f1}+R_{f2})//r_{ds}//R_L$ is the output resistance of the LDO regulator. R_1 and C_1 are the resistance and capacitance at the output of error amplifier, respectively. $g_{mp}R_{OUT}$ is a function of output load current. Therefore, p_1 is a load-dependent pole but it is less than p_2. The location of p_2 is given by

$$P_2 = \frac{1}{R_{OUT} \cdot C_{par}} \tag{2.34}$$

where R_{OUT} is the output resistance of LDO regulator. R_{OUT} is inversely proportional to the output load current. Therefore, p_2 moves to higher frequencies when the load current increases. It is common to observe that the stability of OCL-LDO regulator is enhanced when the load current increases. However, R_{OUT} increases significantly at low load current condition and p_2 is shifted to low frequency. This leads to a condition that p_1 and p_2 are close to each other causing potential instability. Typically, the worst case stability for the OCL-LDO regulator occurs at no load condition. This gives rise to the need of advanced frequency compensation techniques which is employed to ensure the stability of the OCL-LDO regulators.

2.3.4.2 TRANSIENT RESPONSE CONSIDERATIONS

The large output capacitor in OC-LDO regulator can serve as a charge buffer and supply transient current during rapid load changes. Unfortunately, in OCL-LDO regulator, the on-chip parasitic capacitance is very small when compared to the large off-chip capacitor. The change in output voltage is approximately given by

$$\Delta V_{OUT} = \frac{\Delta I_{OUT} \cdot t_r}{C_{par}} \tag{2.35}$$

where t_r is the transient response time and ΔI_{OUT} is the change of output load current. It can be seen that the change in output voltage is inversely proportional to output parasitic capacitance. In this aspect, the OCL-LDO regulators do not have the advantage of large output capacitance to help supply the transient current. This turns out that the transient enhancement technique is very critical in OCL-LDO regulator design. To overcome the stated problem, there are several reported circuit techniques [2], [18], [30-39] recently.

2.3.5 OUTPUT-CAPACITORLESS LDO WITH DAMPING-FACTOR-CONTROL

Figure 2.12 shows an OCL-LDO regulator using Damping-Factor-Control (DFC) frequency compensation [18].

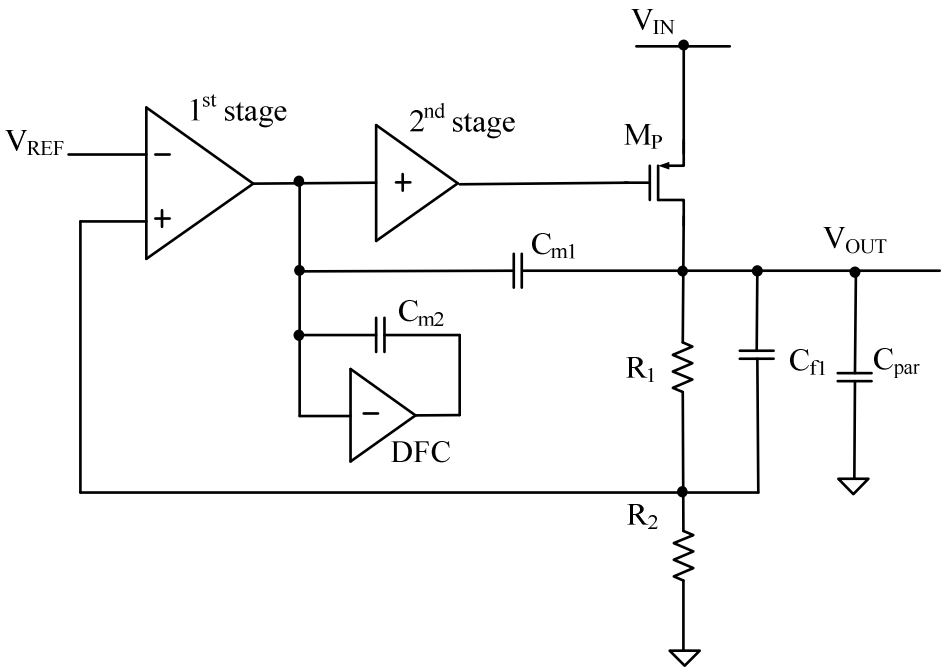


Figure 2.12: LDO regulator with damping-factor-control

The DFC frequency compensation technique is a pole splitting compensation technique especially designed for multistage amplifier with a large capacitive load. The DFC block comprises of a negative gain stage with a compensation capacitor C_{m2} and it is connected at the output of the first stage. The DFC block is used to create an internal dominant pole at the output of the first stage. Besides, another compensation capacitor C_{m1} is required to achieve pole splitting effect. A zero, generated by the capacitor C_{f1}, is utilized to cancel the effect of non-dominant pole in the LDO regulator so as to improve the stability. To push the parasitic pole contributed by the resistive-feedback network, the resistor R_2 has to be much smaller than R_1. This implies that the required reference voltage should be much smaller than LDO regulator output voltage. However, the generated zero is relatively fixed and it does not move with the load-dependent poles. This greatly reduces the effect of the pole-zero cancellation. Furthermore, the OCL-LDO regulators with DFC are unstable for light load condition due to peaking effect appears near the UGF.

Similarly, the proposed topologies [18], [31], [34], [35] demand a minimum load current, $I_{LOAD(min)}$, for stable operation. Although the peaking effect due to the complex poles near the UGF in the open-loop response can be reduced via minimum load current design, the current efficiency is compromised, especially at low load current condition.

2.3.6 OUTPUT-CAPACITORLESS LDO WITH DIFFERENTIATOR

Figure 2.13 shows a LDO regulator which includes an auxiliary fast loop (differentiator) [2].

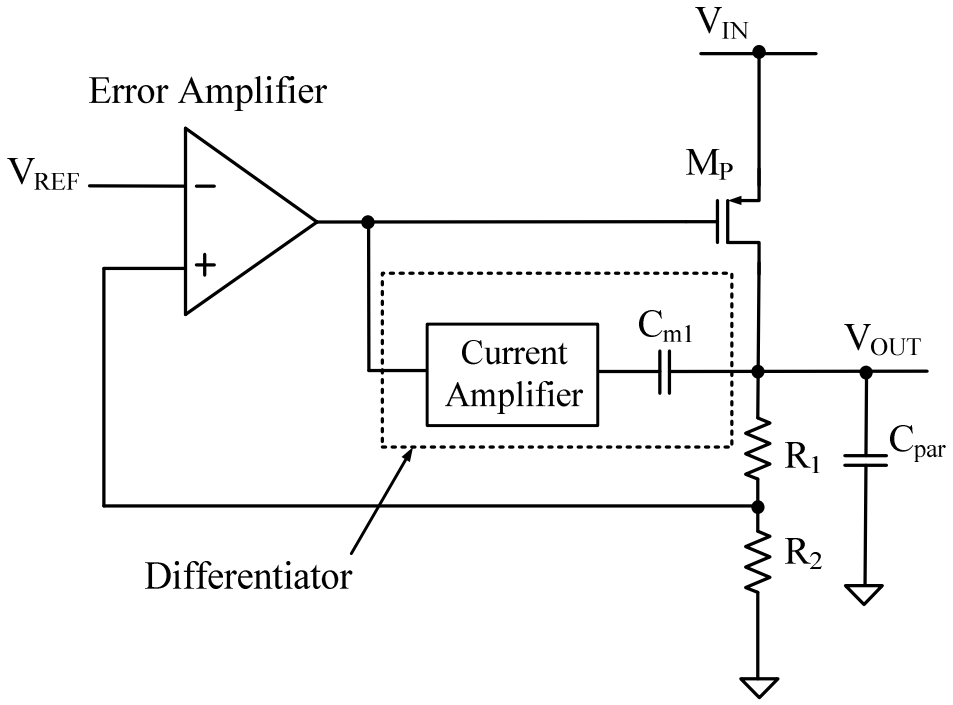


Figure 2.13: LDO regulator with differentiator

The differentiator forms the core of the LDO regulator providing both a fast transient path as well as internal ac compensation. C_{m1} senses the changes in the output voltage in the form of current that is then injected into the parasitic gate capacitance of power transistor. Similar to the Miller compensation scheme, the compensation circuitry splits the poles to achieve stable operation. It also improves the speed at the same time. When a current step ΔI is applied at the output of LDO regulator, the ΔV output change is generated. The current flowing through C_{m1} is

extracted from the parasitic gate capacitance of power transistor until a point where the output voltage returns back to its steady state. This design does not require any minimum loading current to ensure stability. Since its maximum output current is only 50mA, it may not suitable for some applications which require higher output current. In order to maintain stability at higher output current, the quiescent current has to be increased substantially. Another drawback of this design is that it does not have high loop gain. This is mainly because it has only two gain stages and hence the accuracy of the LDO regulator is compromised. Finally, for low voltage application, the smaller head room causes the size of the power transistor to be increased greatly. Therefore, the power consumption has to be increased as well.

2.3.7 OUTPUT-CAPACITORLESS LDO REGULATOR WITH FLIPPED VOLTAGE FOLLOWER

Figure 2.14 shows a LDO regulator structure which is based on a flipped voltage follower (FVF) [40]. LDO regulator based on FVF topologies is reported in [32]. The output voltage of the LDO regulator is set by the gate voltage of transistor M_2. When there is step current at the output of LDO regulator, transistor M_2 senses the voltage changes and serves as a common gate amplifier. It amplifies the signal and transfers it to the gate of power transistor so that the output voltage is regulated. The LDO regulator in [32] draws a 95 µA of quiescent current in order to obtain an acceptable transient response. To reduce the quiescent power, a FVF LDO regulator with voltage spike detection capability is introduced [33]. The voltage spike detection circuit provides extra momentary current to charge or discharge the gate of the power transistor. As a result, the required quiescent power is reduced. Both LDO

regulators in [32] and [33] does not require any compensation capacitor to be stabilized. Although the LDO regulators based on FVF topologies in [32], [33] are stable without an off-chip capacitor, the FVF based LDO regulators impose a power transistor with very large aspect ratio in order to avoid the large swing associated at the gate that may drive the tail current source transistor to triode region in low voltage design. Besides, these simple LDO regulators do not have high loop gain due to the simple gain circuit structure, leading to the significant tradeoff for precision, line regulation, load regulation and power supply rejection (PSR).

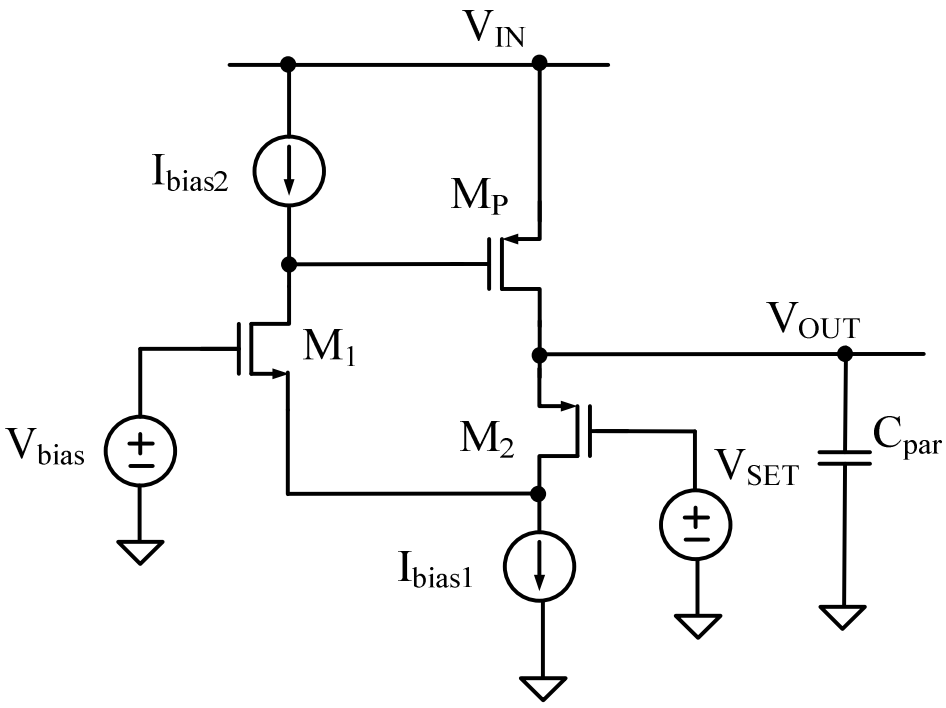


Figure 2.14: LDO regulator with flipped voltage follower

To solve this problem, an extra gain stage [41] is introduced. With the additional gain stage, the loop gain of the LDO regulator is improved, enhancing both the line and load regulation. However, the stability in light load current is sacrificed due to increased circuit complexity. A minimum load current is required for the LDO

regulator to maintain stability. This shows the tradeoff between the stability and accuracy.

Therefore, it is needed to design a low-quiescent low-voltage OCL-LDO regulator which can operate from no load to full load current range without affecting the stability whilst offering good load/line regulation performances.

2.4 LAYOUT CONSIDERATIONS

A proper layout is essential for high-performance analog circuits. Device properties such as matching, noise and high frequency characteristic are heavily depending on good layout technique. The layout considerations for LDO regulator are mainly on the matching of the transistors and the power transistor layout with minimum parasitic.

2.4.1 TRANSISTOR MATCHING

Matching is a critical issue in analog circuit layout. Many circuit building blocks, such as current mirrors, input differential pairs and current mirror active loads involve matching. In order to reduce the mismatch offset arising from the fabrication process, interdigitized technique and common-centroid technique are employed for critical component pair (differential pair and current mirrors). Fig. 2.15 gives an exemplary symmetrical layout technique. Device A and device B are laid out interleaved at the top, and are reversely order in the bottom. This gives the independence of process in one gradient direction. The dummy transistors are introduced at both sides to reduce lateral etching effect.

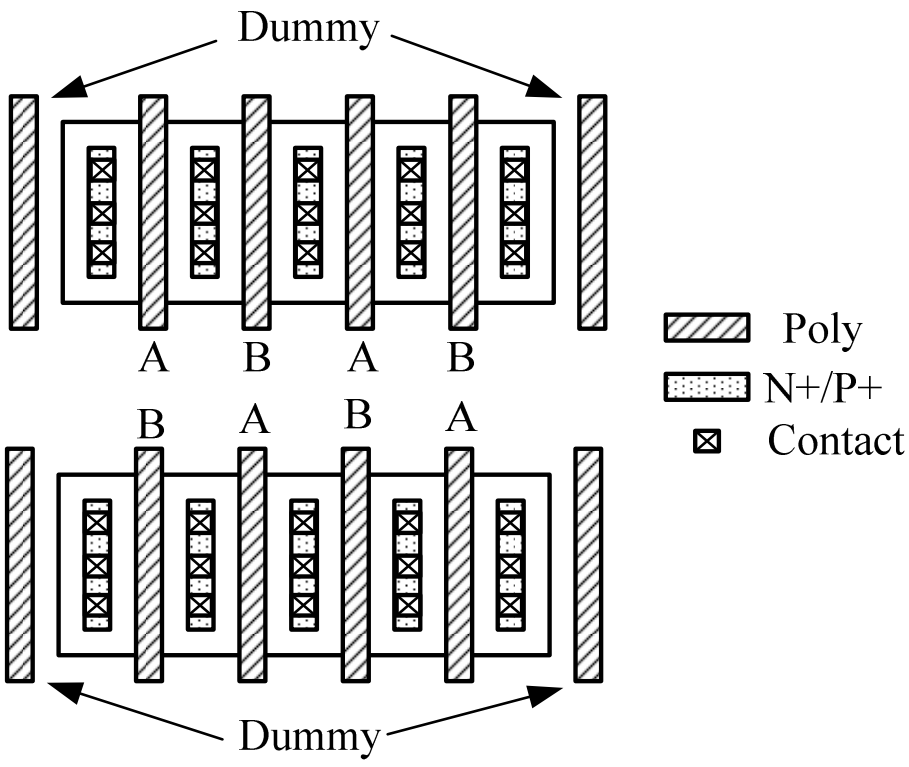


Figure 2.15: Common-centroid layout example

Besides, the interdigitized technique is also adopted for matching of passive devices like feedback resistors. The precise ratio of the feedback resistors is critical for system accuracy and dc offset.

2.4.2 POWER TRANSISTOR

The layout of the power transistor is importance for a good performance regulator. To regulate large amounts of current and reduce the on-resistance (R_{on}), the device size (W/L ratio) has to be much larger than the normal low-power transistor and the minimum channel length is used. To minimize the distributed gate resistance, the layout of the power transistor is made by breaking the power transistor into a number of multi-fingers structures and arranging the multi-fingers to form a transistor array. In a transistor array, the fingers are connected to interleaved source and drain metallization which is then connected to higher level of metal by contacts and vias up to the top metal level. Fig. 2.16 shows the typical multi-fingers connection of the transistor array. This layout technique not only reduces the gate resistance but also reduces the junction capacitances [42, 43].

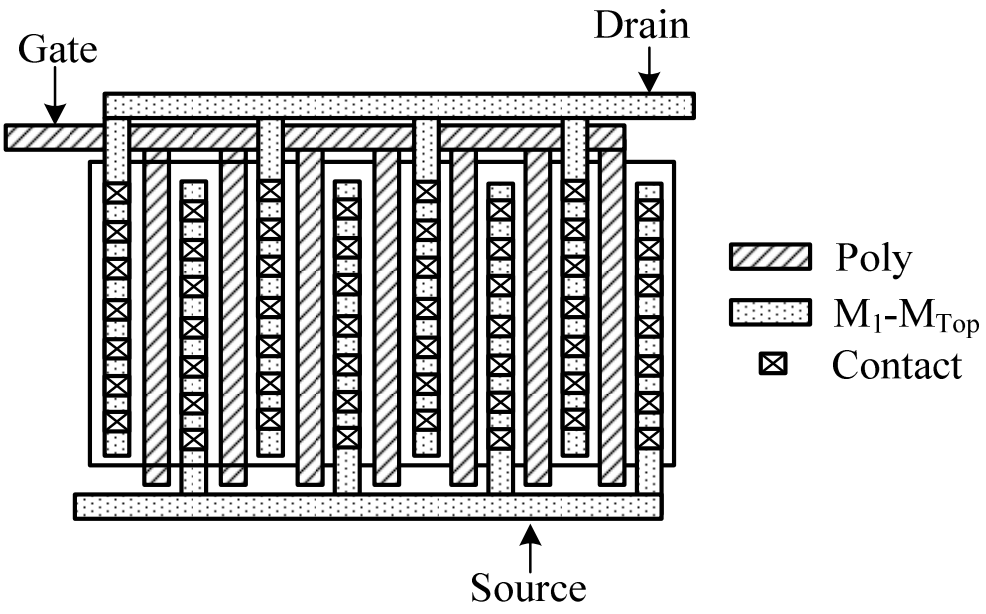


Figure 2.16: A typical multi-finger layout structure

In general, it is believed that R_{on} can be reduced by increasing the number of transistors in parallel configuration. However, the R_{on} does not continue to reduce. In fact, at some point, R_{on} will be saturated as it is dominated by the interconnect resistance. To further reduce the R_{on}, some layout design techniques have been reported. Fig. 2.17 shows a modified version of the multi-finger layout technique [44]. In this layout, wider metal layers are used to minimize the R_{on}. Nevertheless, there is a tradeoff between the width of the metal layer as well as the number of contacts for drain/source.

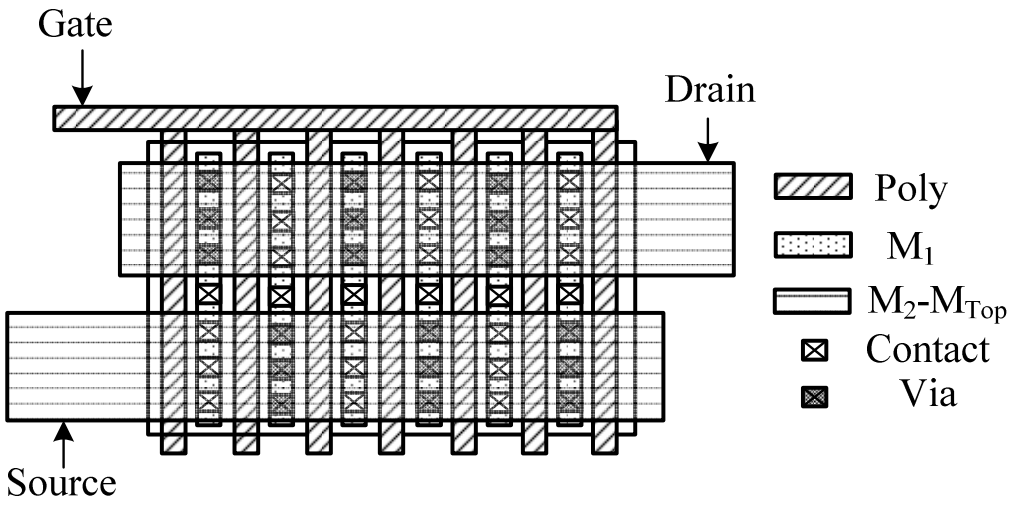


Figure 2.17: A modified version of multi-finger layout structure

Other than the modified version of the multi-finger transistor layout technique, waffle transistor layout technique is also one of the possible choices. Waffle transistor layout is depicted in Fig. 2.18. It achieves lower R_{on} by using a mesh of horizontal and vertical poly gate stripes to divide the source and drain implant into an array of squares. By connecting these drain and source contact alternately, one can arrange four drains around each source and four sources around each drain [45]. The drains/sources are connected together by a diagonal stripes formed by metal

layers. In general, the waffle layout offers a better packing density than the multi-finger layout [44]. However, due to the CMOS design rule (e.g. minimum metal width and spacing) of the metal layer, the drain/source diffusion area should be larger to accommodate the metal layer. Moreover, in more recent CMOS process, the R_{on} of the transistor is often dominated by the metallization that causes the improvement of R_{on} less significant.

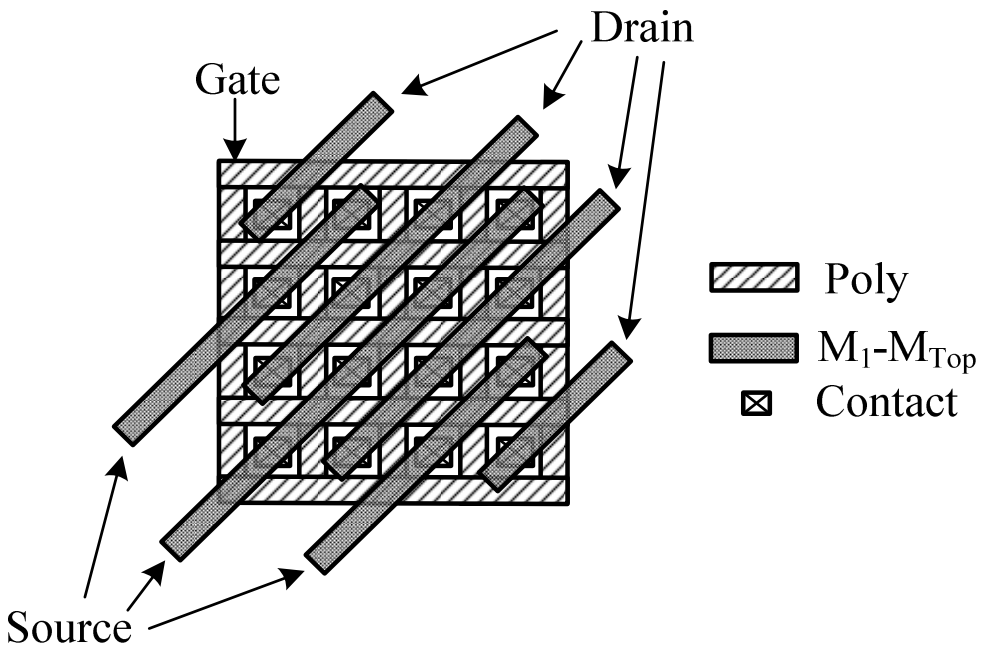


Figure 2.18: A waffle layout structure

In layout design for power transistor, it is also necessary to consider the total width of the metal wire to collect the large amount of load current. It is because the parasitic resistances of the metal layer will cause additional voltage drop across metal wire or bus of the regulator. Furthermore, the metals that carry too much current will form a high current concentration zones which may lead to metal eletromigration and formation of "Hot Spots" during operation of the device. The result is the change in conductor dimensions and eventually failure. In practice, the

higher levels of metal should be used for power routing as they have a lower sheet resistance.

2.5 SUMMARY

In this chapter, several representative frequency compensation techniques for multistage amplifier are discussed. These involve pole splitting and feedforward technique. The SMC and NMC scheme require the compensation capacitors which are directly proportional to the load capacitance. On the other hand, the cascode based (active feedback) compensation schemes require smaller compensation capacitors. As a result, the effectiveness of the compensation scheme is improved. Therefore, cascode based compensation schemes are suitable for OCL-LDO regulators.

Both OC-LDO and OCL-LDO regulators are reviewed. Some of the intrinsic problems, especially, stability and transient response have been discussed as well. In order to solve these problems, various circuit design techniques such as dynamic biasing, current boosting and flipped voltage follower are presented.

Finally, the layout considerations for LDO regulator are discussed. For better matching, interdigitized technique in conjunction with common-centroid layout techniques can be applied to critical devices (differential pair/ current mirror). Besides, the layout techniques for power transistor (multi-finger, modified multi-finger and waffle layout structure) are also described.

CHAPTER 3

PROPOSED FREQUENCY COMPENSATION TECHNIQUES FOR LARGE CAPACITIVE LOAD

3.1 INTRODUCTION

LDO voltage regulator can be treated as a multistage amplifier with power transistor as the last stage driving a large capacitive load where the capacitive load is the power line or the output capacitor. Therefore, an effective frequency compensation technique can be adopted and applied in the LDO voltage regulator implementation to improve the performance and to ensure the stability. For example, the damping-factor-control frequency compensation (DFCFC) and active-feedback frequency compensation (AFFC) for large capacitive load are applied in LDO voltage regulator in [18] and [30], respectively, with slightly modifications. Both LDO voltage regulators achieve fast transient response by using smaller compensation capacitor while consuming low quiescent power. Therefore, it is desired to investigate the frequency compensation technique for large capacitive load in a multistage amplifier topology.

Moreover, a high-gain high-bandwidth amplifier driving a large capacitive load can serve as an error amplifier in LDO regulator [46] which has either an on-chip or an off-chip power transistor as shown in Fig. 3.1.This power transistor is usually large and it serves as the load of the error amplifier. The lumped parasitic capacitor, C_{par},

associated with such a transistor becomes large. Besides, the effective input capacitance of power transistor will be pronounced when adding up the Miller effect caused by the large gate-to-drain parasitic capacitance (C_{GD}) in a power transistor amplification stage. As a result, the lumped parasitic capacitor C_{par} can be represented by $C_{par} \approx C_a + g_{mp}R_{OUT}C_{GD}$, where $R_{OUT}=(R_1+R_2)//r_{ds}//R_L$ is the output resistance of LDO regulator and C_a is capacitance at the output of error amplifier. Therefore, an effective frequency compensation for large capacitive load is desired to overcome the stated problem.

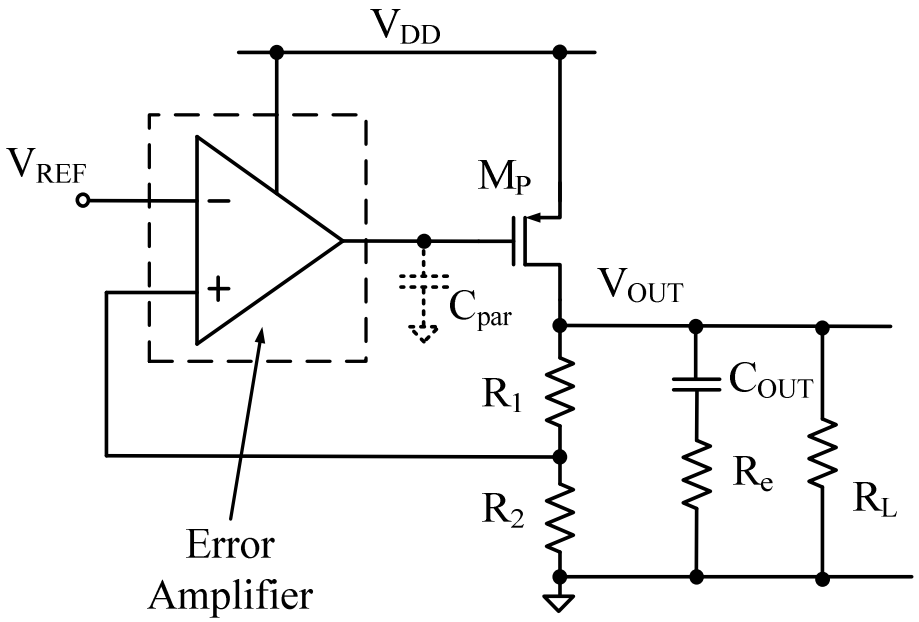


Figure 3.1: Structure of LDO regulator

In this chapter, an area-efficient cross feedforward cascode compensation (CFCC) technique [47] is presented for a multistage amplifier. With the proposed technique, the amplifier can drive a large capacitive load of 500 pF at low power consumption. Moreover, the non-dominant complex poles associated with the amplifier can be located at high frequencies, resulting in bandwidth extension. In addition, the

presence of two left-hand-plane (LHP) zeros in the proposed scheme improves the phase margin and relaxes the stability criteria. The amplifier can be stabilized with a small on-chip compensation capacitor when driving a large capacitive load. Therefore, the overall silicon area of the amplifier is greatly reduced. Furthermore, the proposed technique offers significant technical merits in terms of area, small-signal and large-signal performance metrics.

3.2 PROPOSED CROSS FEEDFORWARD CASCODE COMPENSATION TECHNIQUE

3.2.1 STRUCTURE

The topology of the proposed three-stage amplifier with CFCC technique is shown in Fig. 3.2.

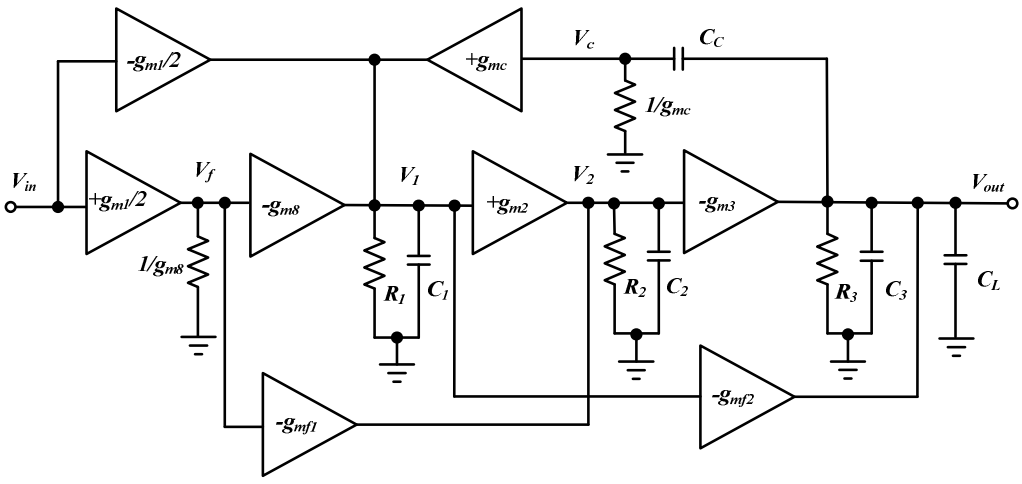


Figure 3.2: Topology of proposed three-stage CFCC amplifier

$R_{1\text{-}3}$ and $C_{1\text{-}3}$ denote the output resistance and the lumped parasitic node capacitance at the outputs of each stage, respectively. To stabilize the amplifier, a small cascode

compensation C_C is employed. C_L is the load capacitance which represents the C_{par} in Fig. 3.1. The transconductance stages g_{m1}, g_{m2} and g_{m3} compose the conventional three-stage amplifier. Due to the differential signal, g_{m1} is separated into two paths ($+g_{m1}/2$ and $-g_{m1}/2$). g_{mf1} and g_{mf2} are two feedforward stages. The function of the feedforward stage, g_{mf1}, from V_f to the output of the second stage is different from that of the feedforward stage in [48]. In [48], the feedforward stage is used to improve the transient response without affecting the frequency response by only introducing a high frequency RHP zero to the amplifier. However, in this proposed topology, a LHP zero is introduced by the feedforward stage to improve and enhance the overall stability of the multistage amplifier. The proposed CFCC structure has only one compensation capacitor when compared to the well-known conventional NMC topology. As a result, both the bandwidth and the transient performance of the proposed CFCC amplifier are greatly improved and enhanced. The feedback network is realized by a cascode compensation scheme which includes a compensation capacitor, C_C, and a transconductance stage, g_{mc}. The cascode compensation removes the RHP zero in a normal Miller compensation scheme by blocking the high frequency feedforward small-signal current. Compared to DACFC in [49], the proposed CFCC scheme only consists of one feedback network for compensation, resulting in a simpler structure. The distinction between the CFCC topology and the AFFC topology [23] is that the inner Miller capacitor is removed in the proposed scheme. Thus, the overall physical dimension of the new amplifier can be reduced. In the proposed scheme, the compensation capacitor, C_C, combines with the finite input resistance of the transconductance stage, g_{mc}, form a LHP zero. Together with the LHP zero introduced by the feedforward stage, g_{mf1}, the presence of both LHP zeros in the CFCC topology can be used to compensate for the negative

phase shift that occurs because of non-dominant poles. In the CFCC structure, the transconductance and feedforward stages, g_{m2} and g_{mf1} as well as g_{m3} and g_{mf2}, form a push-pull stage at the second and output stages, respectively. This enhances the transient performance of the proposed CFCC amplifier while keeping the power consumption low at steady state.

3.2.2 TRANSFER FUNCTION

The small-signal model of the proposed CFCC amplifier in Fig. 3.2 is shown in Fig. 3.3. The small-signal transfer function should be investigated in order to analyze the stability of the CFCC amplifier.

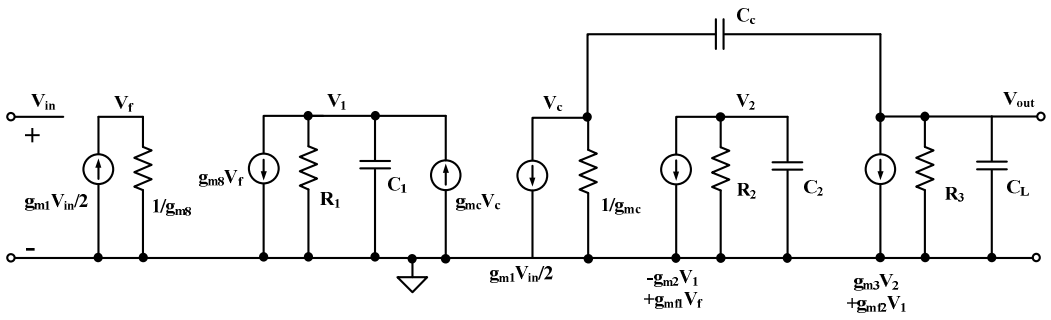


Figure 3.3: Small-signal model of the proposed three-stage CFCC amplifier

The transfer function is derived using the following assumptions: (i) The input resistance of the feedback transconductance stage, g_{mc}, is equal to the reciprocal of its transconductance. (ii) The gain of all the stages is much greater than 1. (iii) The capacitance C_1, C_2, C_3 and C_C are much smaller than C_L. Given these assumptions, the transfer function is obtained as follows:

$$A_{V(CFCC)} = \frac{A_{dc}\left(1+s\frac{C_C}{2g_{mc}}\right)\left(1+s\frac{g_{mf1}C_1}{g_{m1}g_{m2}}\right)\left(1-s\frac{g_{m1}C_2}{g_{mf1}g_{m3}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_LC_1}{g_{m3}g_{m2}R_2C_C}+s^2\frac{C_LC_1}{g_{m3}g_{m2}R_2g_{mc}}\right)(1+sR_2C_2)} \quad (3.1)$$

The low frequency gain A_{dc} and the dominant pole p_{-3dB} are given respectively by

$$A_{dc} = g_{m1}g_{m2}g_{m3}R_1R_2R_3 \quad (3.2)$$

$$p_{-3dB} = -\frac{1}{C_C g_{m2}g_{m3}R_1R_2R_3} \quad (3.3)$$

Hence, the GBW is obtained as

$$GBW = A_{dc} \times p_{-3dB} = \frac{g_{m1}}{C_C} \quad (3.4)$$

From the transfer function, the non-dominant complex poles and their corresponding Q-value can then be determined by

$$|p_{2,3}| = \sqrt{\frac{g_{m3}A_{v2}g_{mc}}{C_LC_1}} \quad (3.5)$$

$$Q = \sqrt{\frac{C_C{}^2A_{v2}g_{m3}}{C_LC_1g_{mc}}} \quad (3.6)$$

where $A_{v2} = g_{m2}R_2$ is the second stage gain. Equations (3.5) and (3.6) indicate that both the location and Q-value of the non-dominant complex poles depend on the parameters A_{v2}, g_{m3}, g_{mc} and C_L that control the stability of the CFCC amplifier. The fourth pole shown in (3.7) is a parasitic related pole which can be easily located at high frequencies.

$$p_4 = -\frac{1}{R_2C_2} \quad (3.7)$$

There are also two LHP zeros and one RHP zero in the CFCC amplifier. The zeros can be derived as follows:

$$z_1 = -\frac{2g_{mc}}{C_C} \tag{3.8}$$

$$z_2 = -\frac{g_{m1}g_{m2}}{g_{mf1}C_1} \tag{3.9}$$

$$z_3 = +\frac{g_{mf1}g_{m3}}{g_{m1}C_2} \tag{3.10}$$

The RHP zero occurs at very high frequency which is much higher than that of the fourth pole. As such, its effects can be ignored. Finally, the two LHP zeros can be used to compensate for the non-dominant complex poles. This leads to an extension of the bandwidth in the CFCC amplifier.

3.2.3 STABILITY CONSIDERATIONS

The pole-zero diagram of the CFCC amplifier is illustrated in Fig. 3.4.

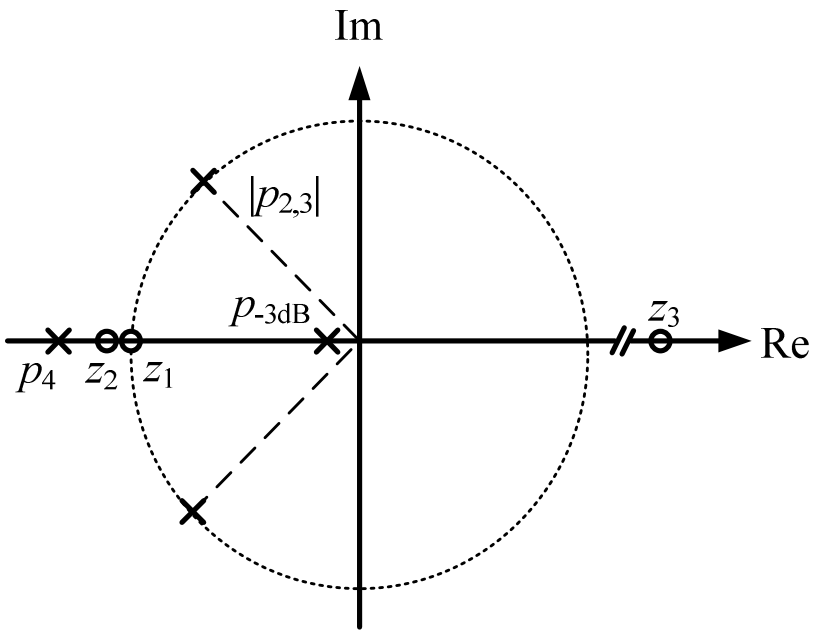


Figure 3.4: Pole-zero diagram of CFCC amplifier

The phase shift of the non-dominant complex poles depends on both location and Q-

value. In order to avoid the frequency "peak", a Q-value of $1/\sqrt{2}$ is suggested [49]. AFFC and DLPC amplifiers limit the GBW to at least $2\sqrt{2}$ times less than that of the non-dominant complex poles by adopting the third-order Butterworth response. Similar to the DACFC [49], in the proposed scheme, the negative phase shift of the $|p_{2,3}|$ is compensated by the positive phase shift generated by z_1 and z_2 on the basis of conditions: $z_1 = |p_{2,3}| = 2$ x GBW and $z_2 = 3$ x GBW. Therefore, the GBW of the proposed amplifier can be set at a larger while maintaining stability.

The dimension condition for g_{mc}, C_C and g_{mf1} can be determined based on the criteria outlined above. Since z_1 is 2 x GBW, the dimension condition of g_{mc} can be found as

$$g_{mc} = g_{m1} \tag{3.11}$$

Further, when $z_1 = |p_{2,3}| = 2$ x GBW, the dimension condition of C_C is obtained as

$$C_C = 2\sqrt{\frac{g_{m1}C_1C_L}{g_{m3}A_{v2}}} \tag{3.12}$$

As shown in (3.12), the size of the cascode compensation capacitor is proportional to the square root of the product of the parasitic and load capacitance. The size is also reduced by the square root of second-stage gain. The physical size is greatly reduced as a result. With $z_2 = 3$ x GBW, the dimension condition of g_{mf1} is calculated as

$$g_{mf1} = \frac{g_{m2}C_C}{3C_1} \tag{3.14}$$

Based on the discussion above, a pole-zero distribution can be realized. The phase margin (PM) is expressed by

$$PM = 180° - \tan^{-1}\left(\frac{GBW}{p_{-3dB}}\right) - \tan^{-1}\left(\frac{\left(\frac{GBW}{|p_{2,3}|}\right)}{Q\times\left(1-\left(\frac{GBW}{|p_{2,3}|}\right)^2\right)}\right)$$

$$+\tan^{-1}\left(\frac{GBW}{z_1}\right)+\tan^{-1}\left(\frac{GBW}{z_2}\right)-\tan^{-1}\left(\frac{GBW}{p_4}\right) \qquad (3.15)$$

$$\approx 90° - \tan^{-1}\left(\frac{GBW}{p_4}\right)$$

As can be seen in (3.15), the phase margin of the CFCC amplifier depends on the location of p_4. Equation (3.7) shows that p_4 is inversely proportional to R_2 and C_2. Hence, C_2 has to be kept as small as possible in order to have a good phase margin. Since C_1 and C_2 are in the order of 100s of fF and 10s of fF, respectively. In this design, p_4 can be located at high frequency even with the presence of the Miller effect due to the third stage gain.

3.2.4 SLEW RATE AND SETTLING TIME

In this section, the settling time (T_S) and slew rate (SR) are discussed. The slew rate due to influence of the second stage can be ignored because C_L and C_C is much larger than the internal lumped parasitic capacitance C_2. Furthermore, a push-pull stage is formed by the feedforward stage g_{mf2} and the output stage g_{m3}, hence, slew rate is not limited in both directions. As a result, the slew rate of the proposed amplifier is limited by the cascode capacitor C_C which is driven by the first stage. The slew rate is given as

$$SR = \frac{I_1}{C_C} \tag{3.16}$$

where I_1 is the maximum amount of current that available to drive cascode capacitor C_C. From (3.16), the slew rate is proportional I_1 and inversely proportional to C_C. Hence, the slew rate can be improved by reducing the size of C_C or increasing I_1. In this proposed design, from (3.12), the required compensation capacitor C_C is greatly reduced by a factor of square root of second gain stage. As a result, for a given amount of I_1, the internal slew rate of the proposed amplifier is enhanced.

The location of the doublet frequency and pole-zero spacing will highly affect the settling behavior of the amplifier [50]. Fortunately, with the proposed scheme, all the zeros and non-dominant poles are not located within the UGF. Hence, the pole-zero doublets are not appears in the passband. As a result, the settling time degradation that arises due to the high frequency doublets will not be as strong as the low frequency doublets [50] and the settling behavior is not greatly affected by the proposed pole zero cancellation in CFCC scheme.

3.3 CIRCUIT IMPLEMENTATIONS OF AMPLIFIER

The schematic of the proposed multistage amplifier with CFCC scheme in transistor level is depicted in Fig. 3.5.

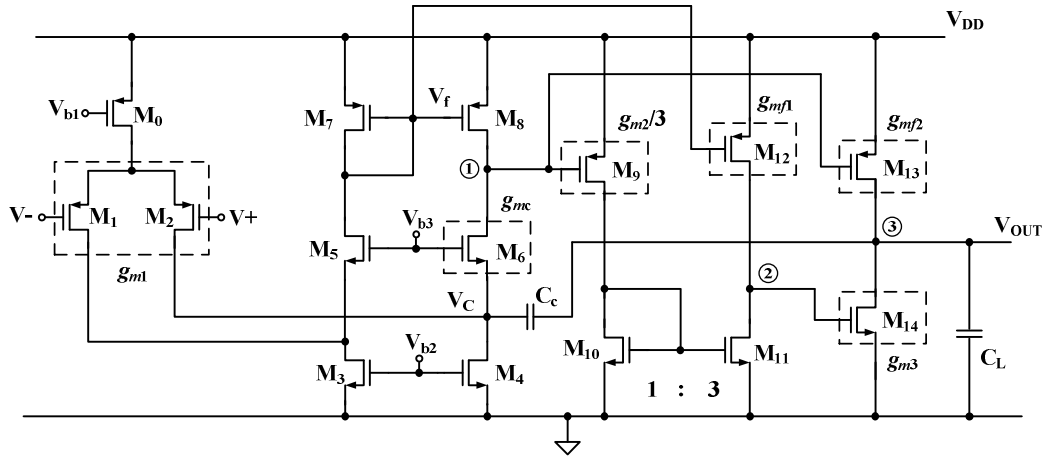


Figure 3.5: Schematic of the proposed three-stage CFCC amplifier

The first gain stage is realized by a folded cascode operational transconductance amplifier. It is implemented by transistors M_1-M_8. The first-stage transconductance g_{m1} is determined by the PMOS differential pair that comprises transistors M_1/M_2. The second-stage of the amplifier is formed by transistor M_9 as well as a pair of current mirror transistors M_{10} and M_{11}. The current ratio of this current mirror is designed to be 1: 3. The transistor M_{12} serves as an active load and the feedforward stage g_{mf1}. With this feedforward stage, it forms a push-pull second stage with transistors M_9-M_{11}. The output stage is realized by the third gain stage g_{m3} and a feedforward stage g_{mf2}. Similarly, a push-pull output stage is formed. In order to have a smaller lumped parasitic capacitance C_2 at node 2 such that p_4 can be located at higher frequencies, the third gain stage is implemented by a common-source nMOS transistor M_{14}. The feedforward stage, g_{mf2}, is realized by transistor M_{13}

which is driven by the output of first stage. The compensation capacitor C_C and cascode transistor M_6 form the cascode compensation network that responsible for the stability of the amplifier. Transistor M_6 can be viewed as a common-gate amplifier or current buffer with transconductance of g_{mc}. C_L is the load capacitor which realized off-chip. Transistor M_7 and M_{12} can be viewed as a pair of current mirror since they share the same gate-source voltage. As a result, the biasing current condition of the second stage can be properly controlled by simply scaling the device ratios between transistors M_7 and M_{12}. Similarly, the biasing for the output stage is control by the aspect ratio of M_9 and M_{13}. In this proposed scheme, the amplifier can be stabilized by a small on-chip metal-oxide-metal (MOM) capacitor C_C of 1.15 pF when driving a 500 pF capacitive load. The circuit parameters and the transistor sizes of the CFCC amplifier are summarized in Table 3.1 and Table 3.2, respectively.

TABLE 3.1: PARAMETERS OF THE CFCC AMPLIFIER

g_{m1} = 13.5 µA/V	g_{m2} = 150 µA/V	g_{m3} = 145 µA/V
g_{mc} = 13.5 µA/V	g_{mf1} = 120 µA/V	g_{mf2} = 204 µA/V
C_C = 1.15 pF	C_L = 500 pF	

TABLE 3.2: TRANSISTORS SIZE.

TRANSISTOR	W/L
M_0	30/1
M_1, M_2	20/1
M_3, M_4	50/0.5
M_5, M_6	6/ 0.06
M_7, M_8	5/1
M_9	24/0.3
M_{10}	3/1
M_{11}	9/1
M_{12}	50/1
M_{13}	80/0.2
M_{14}	4/0.2

3.4 EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed amplifier with CFCC scheme is designed and fabricated in UMC 65-nm CMOS process. Fig. 3.6 shows both the microphotograph and layout of the amplifier. The CFCC amplifier occupies an active area of about 0.0088 mm^2.

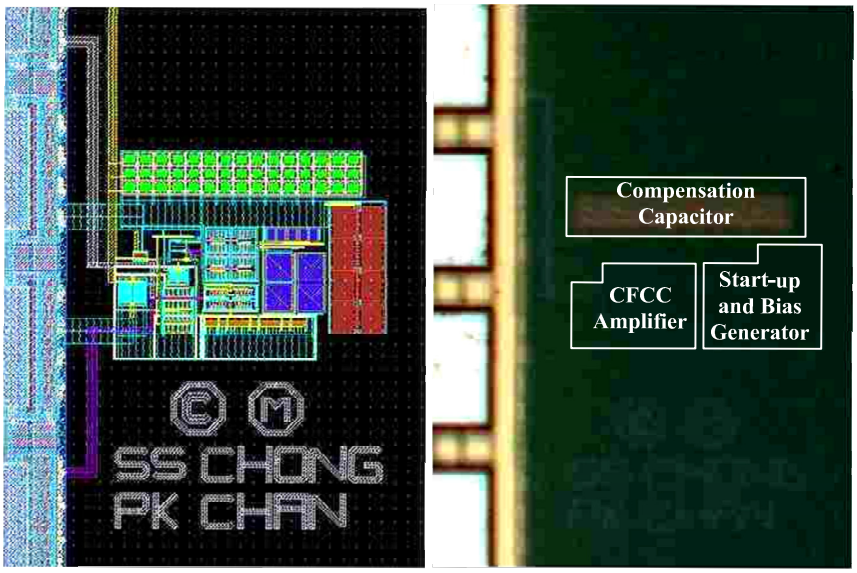


Figure 3.6: Layout and micrograph of CFCC amplifier

The measured frequency response of the CFCC amplifier with C_L = 500 pF is shown in Fig. 3.7. To demonstrate the robustness of the proposed scheme against the variations of the capacitive load, measured results with C_L = 330 pF and 680 pF are also shown. An input common mode voltage of 400 mV is used when measuring the frequency and phase responses of the CFCC amplifier.

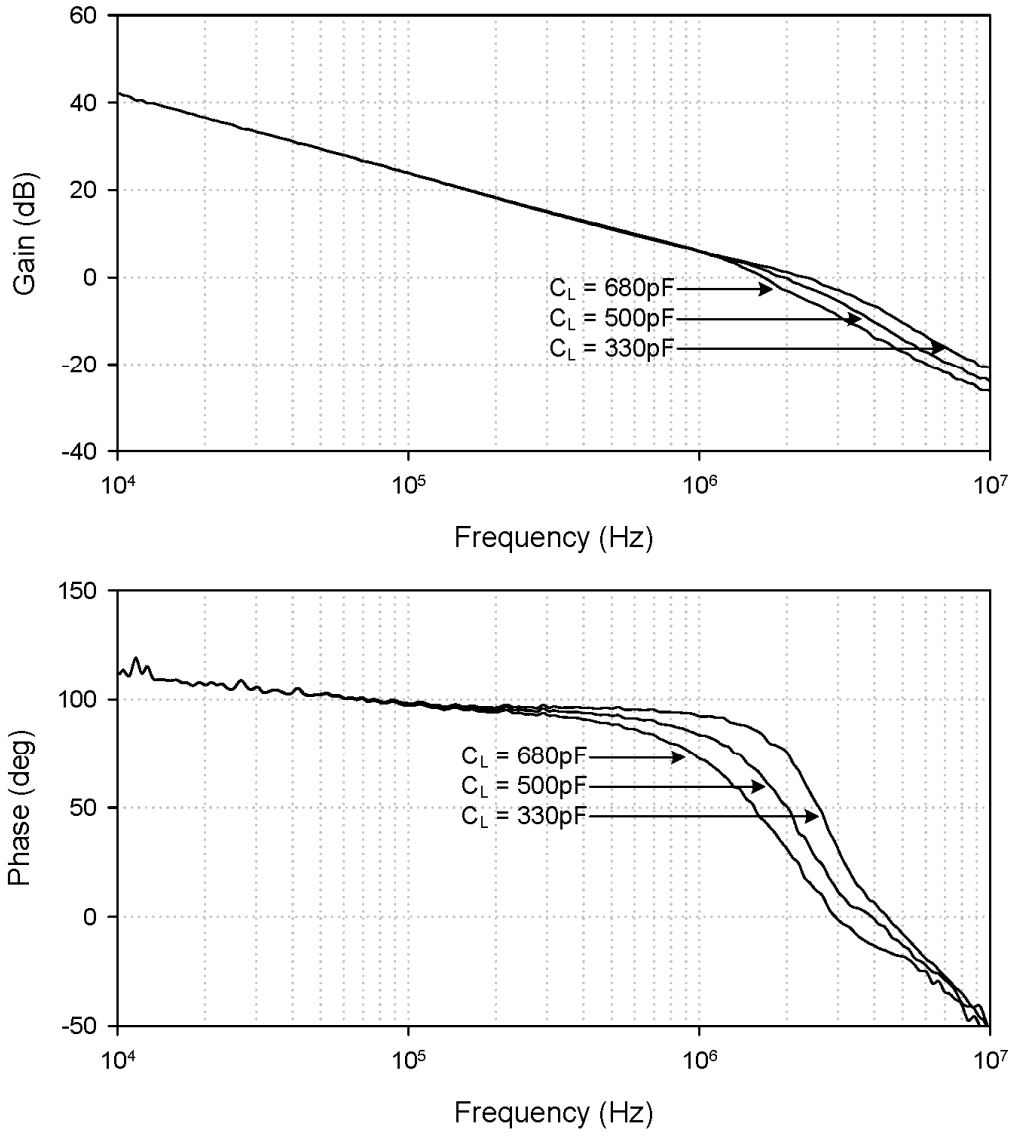


Figure 3.7: Measured open-loop gain frequency response of CFCC amplifier at C_L = 330 pF, 500 pF and 680 pF

As can be seen in Fig. 3.7, the proposed amplifier obtains a unity-gain bandwidth of 2.35 MHz, 2 MHz and 1.66 MHz with a phase margin of 60°, 52° and 45° for C_L = 330 pF, 500 pF and 680 pF, respectively. Based on the measured results in Fig. 3.7, the CFCC amplifier is experimentally verified to be stable when C_L varies from 330 pF to 680 pF. To study the effect of process and temperature variations on unity-gain frequency, gain margin and phase margin, the CFCC amplifier is simulated using the corner transistor model. The simulated results with C_L = 500 pF at different corners and temperatures are summarized in Table 3.3. From the simulated results, it can be observed that the deviation of the phase margin at different corner from the typical corner is only about 4 degree at temperature of 27°C. The similar amount of deviation is observed from the simulations conducted at corner temperatures of -40°C and 125°C. Therefore, it can be concluded that the proposed amplifier remains stable with a minimum gain margin of 7.38 dB and phase margin of 37.87 degree, across the extreme process and temperatures corners.

TABLE 3.3: CORNERS MODEL SIMULATIONS OF THE PROPOSED CFCC AMPLIFIER

-40 degree

CORNER	TT	FF	SS	SNFP	FNSP
UGF (MHz)	2.26	2.50	2.05	2.3	2.22
PM (Degree)	41.95	43.22	37.87	41.03	41.49
GM (dB)	7.73	7.38	7.85	7.45	7.85

27 degree

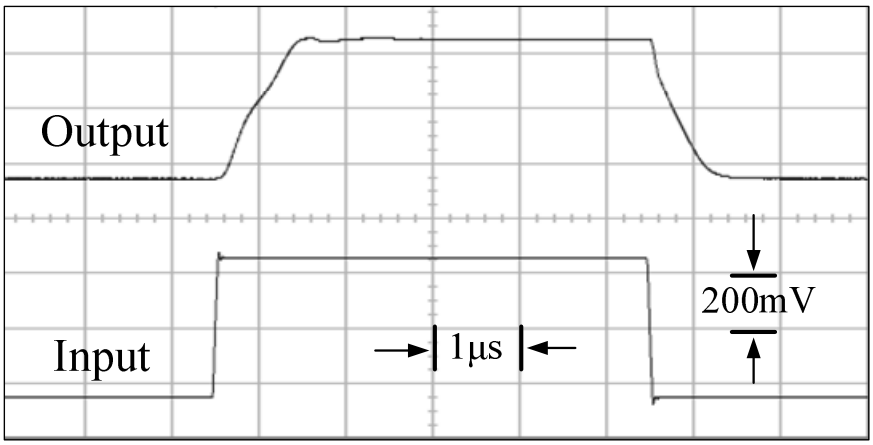
CORNER	TT	FF	SS	SNFP	FNSP
UGF (MHz)	2.15	2.34	2.04	2.23	2.17
PM (Degree)	52.77	53.94	48.82	51.56	52.34
GM (dB)	7.70	7.56	7.82	7.58	7.80

125 degree

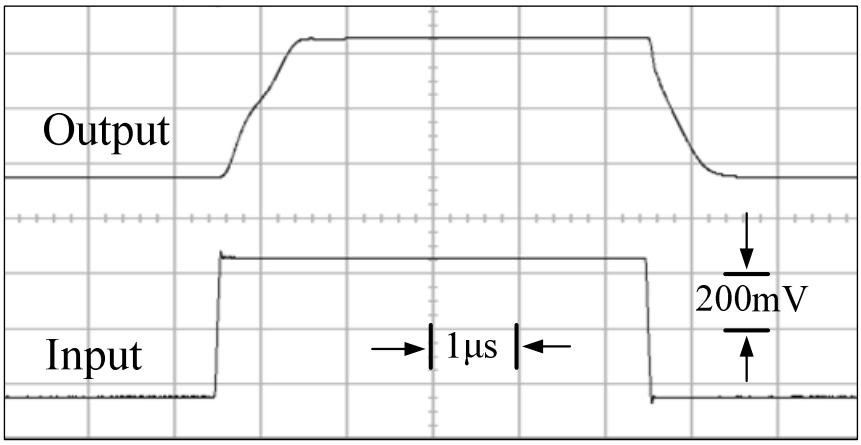
CORNER	TT	FF	SS	SNFP	FNSP
UGF (MHz)	2.06	2.36	1.97	2.10	2.08
PM (Degree)	63.81	64.54	60.65	62.73	63.46
GM (dB)	7.64	7.61	7.57	7.51	7.63

TT = typical; FF = fast NMOS/fast PMOS; SS = slow NMOS/slow PMOS; SNFP = slow NMOS/fast PMOS; FNSP = fast NMOS/slow PMOS

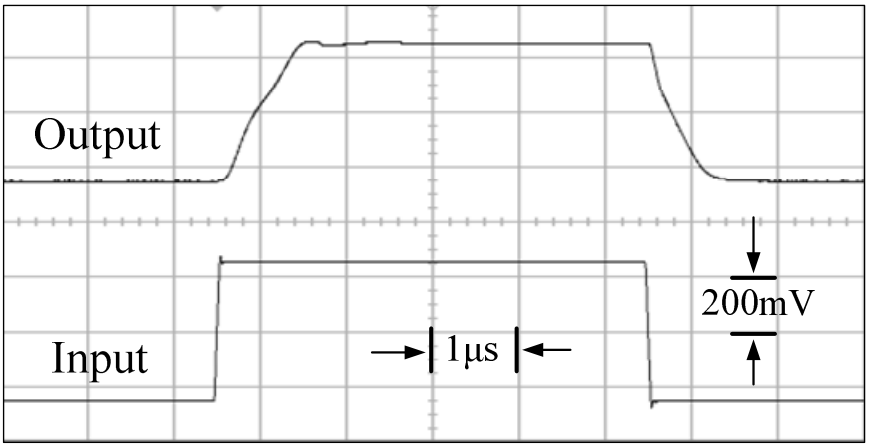
The measured transient responses of the proposed amplifier with C_L = 330 pF, 500 pF and 680 pF are depicted in Fig. 3.8. As can be observed from Fig. 3.8, the transient responses are not greatly affected by the capacitive loads. This is due to the push-pull output stage. The slew rate is not limited by the load capacitor C_L. Therefore, it shows that the slew rate is mainly limited by the on-chip compensation capacitor C_C. In addition, when C_L = 500 pF, the measured 1% settling time and average slew rate of the CFCC amplifier is 1.225 µs, 0.65 V/µs, respectively.



(a)



(b)



(c)

Figure 3.8: Measured transient response of CFCC amplifier (a) C_L = 500pF, (b) C_L = 330pF, (c) C_L = 680pF

In order to validate the performance of the proposed CFCC amplifier against its NMC counterpart, the NMC amplifier is implemented and simulated using the same technology. Table 3.4 shows the measured results of the CFCC amplifier and simulated results of the NMC amplifier. As can be seen, the amplifier with CFCC scheme outperforms the benchmark NMC topology. With the similar total current consumption and capacitive load, the UGF, slew rate and settling time are enhanced

by 60.6, 72 and 51.7 times, respectively. Furthermore, the total size of the required compensation capacitor is reduced by nearly 169 times.

TABLE 3.4: RESULTS SUMMARY OF NMC AND CFCC AMPLIFIERS

	NMC†	CFCC
Technology	65 nm	
C_L (pF)	500	
DC Gain (dB)	>100	
I_{dd} (mA)	0.017	
UGF (MHz)	0.033	2
PM (degree)	52.9	52
SR +/- (V/μs)	0.01/0.008	0.59/0.71
1% T_S +/- (μs)	73.53/53.14	1.49/0.96
C_T (pF)	C_{m1} = 150, C_{m2} = 44	1.15

† Simulated results

Table 3.5 shows the performance comparison of the proposed CFCC scheme and previous topologies. Two figures-of-merit, FOM_S and FOM_L, are adopted to evaluate the large-signal and small-signal performance metrics of the multistage amplifier. Both FOM_S and FOM_L are shown as

$$FOM_S = \frac{GBW \cdot C_L}{power} \tag{3.17}$$

$$FOM_L = \frac{SR \cdot C_L}{power} \tag{3.18}$$

Since the supply voltages are different for most of the reported works, it becomes appropriate to use biasing current related FOMs as follows:

$$IFOM_S = \frac{GBW \cdot C_L}{I_{dd}} \tag{3.19}$$

$$IFOM_L = \frac{SR \cdot C_L}{I_{dd}} \tag{3.20}$$

From Table 3.5, it can be seen that the proposed amplifier with CFCC scheme achieves outstanding FOM and IFOM enhancements over previously reported works. This indicates that the proposed CFCC topology has better power to bandwidth and slew rate efficiency. The proposed CFCC amplifier also achieves the largest load capacitance to total compensation capacitance ratio (C_L/C_T). This confirms that the proposed scheme is an area-efficient frequency compensation scheme.

TABLE 3.5: PERFORMANCE COMPARISON OF REPORTED PRIOR-ART RESULTS

TECHNIQUES	TECHNOLOGY	C_L pF	C_T pF	$\frac{C_L}{C_T}$	I_{dd} mA	$Power$ mW	GBW MHz	SR $V/\mu s$	FOM_S $\frac{MHz \cdot pF}{mW}$	FOM_L $\frac{V/\mu s \cdot pF}{mW}$	$IFOM_S$ $\frac{MHz \cdot pF}{mA}$	$IFOM_L$ $\frac{V/\mu s \cdot pF}{mA}$
Huijsing'85 [51]	3GHz f_t BJT	100	-	-	9.5	76	60	20	79	26	632	211
Eschauzier'92 [52]	3GHz f_t BJT	100	-	-	9.5	76	100	35	132	46	1053	368
You'97 [53]	2µm	20	-	-	0.34	0.68	0.61	2.5	18	74	36	148
Leung'00 [21]	0.8µm	100	21	4.6	0.21	0.42	2.6	1.32	619	314	1238	629
Ramos'04 [54]	0.35µm	130	18	7.2	0.19	0.275	2.7	1.0	1276	473	1915	709
Lee'03 [23]	0.8µm	120	10	12	0.20	0.40	4.5	1.49	1350	447	2700	894
Lee'03 [55]	0.6µm	120	7.3	16.4	0.22	0.33	7.0	3.3	2545	1200	3818	1800
Peng'04 [56]	0.35µm	500	13	38.5	0.162	0.324	1.9	1.0	2932	1543	5864	3086
Fan'05 [46]	0.5µm	120	4	30	0.205	0.41	9.0	3.4	2634	995	5268	1990
Peng'05 [57]	0.35µm	150	2.02	74.3	0.03	0.045	2.85	1.035	9500	3450	14250	5175
Grasso'07 [58]	0.5µm	500	11.35	44.1	0.035	0.105	1.1	1.29	5238	6143	15714	18429
Peng'11 [59]	0.35µm	150	1.6	93.8	0.02	0.03	4.4	1.8	22000	9000	33000	13500
Guo'11 [49]	0.35µm	500	2.2	227.3	0.13	0.26	4	2.2	7692	4231	15385	8462
This work	65nm	**500**	**1.15**	**434.8**	**0.017**	**0.0204**	**2**	**0.65**	**49020**	**15931**	**58823**	**19118**

DC Gain > 100dB for all works

3.5 SUMMARY

This chapter presents a new cross feedforward cascode compensation (CFCC) technique for a multistage amplifier dedicated to drive a large capacitive load contributed by the power device. By applying the proposed CFCC scheme, the non-dominant complex poles can be shifted to higher frequencies. With the cross feedforward and cascode compensation mechanism, two LHP zeros are generated. As a result, under large capacitive load, the phase margin and the stability criteria is improved and relaxed. In addition, the transient response is improved by the use of a smaller cascode compensation capacitor and the push-pull output configuration. Implemented and verified experimentally, the proposed amplifier with CFCC scheme obtains better large-signal as well as small-signal performance metrics than previously reported designed. Furthermore, it also achieves the largest C_L/C_T ratio than all other works, indicating the area effectiveness of the proposed frequency compensation scheme. Amplifier implemented with the CFCC topology can be served as an error amplifier for LDO regulator with on-chip or off-chip power transistor which has a large effective input parasitic capacitance.

CHAPTER 4

FAMILIES OF LDO REGULATORS WITH COMPOSITE POWER TRANSISTORS

4.1 INTRODUCTION

In this chapter, two LDO regulators, which are based on new composite power transistor comprising a shunt feedback embedded gain stage and a power device, are presented. The proposed composite power transistor can be applied to both ultra-low voltage OCL-LDO regulator and OC-LDO regulator. Furthermore, the composite power transistors are modified to (i) push-pull and (ii) dynamic-biased in order to improve the performance metric.

4.2 CLASS-A COMPOSITE POWER TRANSISTOR

Under ultra-low-voltage operating environment, in order to have enough loop gain, LDO regulators with multistage structure are often adopted. Furthermore, to maximize the voltage swing, output stage with only two transistors (shown in Fig. 4.1(a)) are allowed to serve as a power transistor driver. By adopting this topology, the LDO regulator is potentially unstable because of the multiple high impedance nodes in the control loop. To solve this problem, a complex frequency compensation technique is required. In order to avoid the need of complex frequency compensation, a Class-A composite power transistor is proposed in [29], [60]. The

schematic of the Class-A composite power transistor, which has an open-loop structure, is depicted in Fig. 4.1(b).

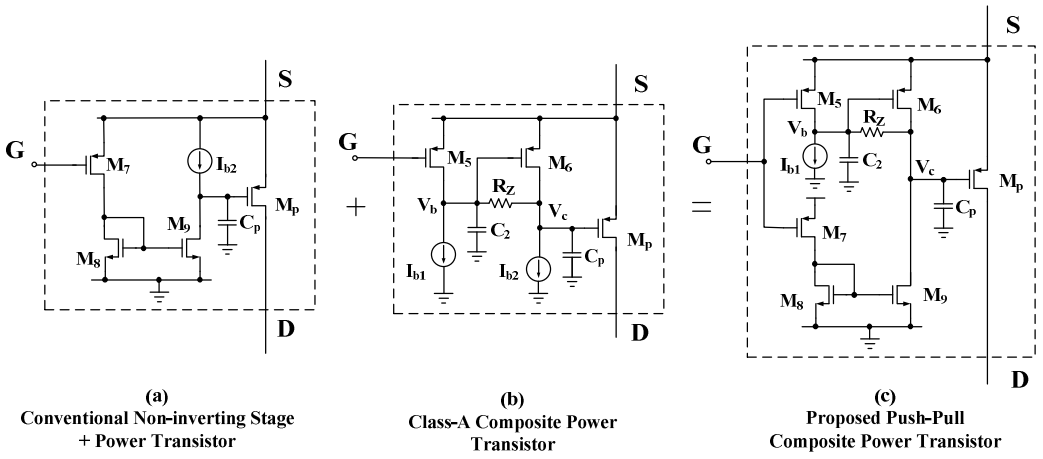


Figure 4.1: (a) Conventional non-inverting stage + power transistor, (b) Class-A composite power transistor, (c) Proposed push-pull composite power transistor.

The small-signal model of the Class-A composite power transistor is depicted in Fig. 4.2, with R_L and C_L representing the effective resistive and capacitive load, respectively. This loading effect will be included in the analysis when the composite transistor forms the circuit in the subsequent LDO circuit topology.

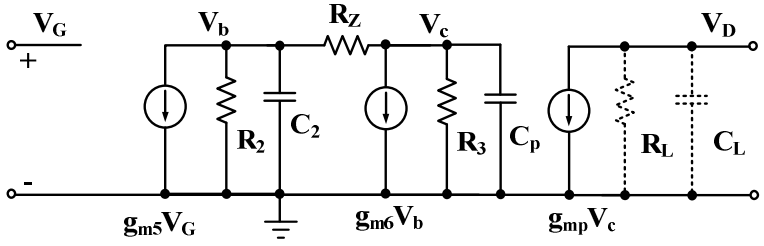


Figure 4.2: Small-signal model of the Class-A composite power transistor.

By applying the nodal analysis to the small-signal model that excludes the loading effect, the frequency-dependent transconductance $G_{mp(class\text{-}A)}$ of the composite power transistor which is defined as the ratio of output current $g_{mp}V_c$ to input voltage V_G can be approximated as

$$G_{mp(Class-A)} = \frac{g_{m5}R_z}{\left(1+\frac{C_p\left(R_2+R_Z\right)}{g_{m6}R_2}s\right)\left(1+\frac{C_2R_ZR_2}{R_2+R_Z}s\right)} \times g_{mp} \quad (4.1)$$

where g_{mi} is the transconductance for the respective devices, C_i and R_i are the respective lumped parasitic capacitance and resistance at the output of each stage. As can be seen from (4.1), the transconductance consists of two poles. In general, the parasitic capacitor C_2 is small. Therefore, the second pole can be ignored. Due to the shunt feedback resistor R_Z, the output impedance of the Class-A driver approximately equals to $(R_2+R_Z)/R_2g_{m6}$. If $R_2 >> R_Z$, the output impedance $\approx 1/g_{m6}$. This low impedance will be helpful in the context of stability of the LDO regulator. In advanced nanometer CMOS technology, the value of R_Z could be close to R_2 such that the output impedance is approximately $2/g_{m6}$. In short, the Class-A driver can be viewed as a buffer stage with gain of $g_{m5}R_Z$. Therefore, it offers the advantage of higher stability over other designs. Furthermore, the transconductance and bandwidth of the composite power transistor can be adjusted independently. However, the main drawback of this Class-A composite power transistor is that the sinking capability at node V_c is limited by the bias current I_{b2}. To turn on the LDO regulator fast, the charges at node V_c has to be discharged quickly. However, the parasitic capacitor C_p is relatively large in ultra-low voltage LDO regulator. This is due to large power transistor dedicated to low supply operation. Thus, for a limited bias current I_{b2}, the turn-on speed of the power transistor M_P is greatly affected. This turns out that the OCL-LDO regulator will exhibit a large undershoot. This may not be acceptable, especially in the ultra-low voltage environment.

In order to solve the sinking capability problem in the Class-A composite power transistor, a modified push-pull composite power transistor is shown in Fig. 4.1(c).

The proposed circuit technique is to combine the conventional non-inverting stage and Class-A driver together. As a result, the sourcing and sinking capability is not limited by the biasing current.

4.3 PROPOSED PUSH-PULL COMPOSITE POWER TRANSISTOR

The operation of the push-pull composite power transistor in Fig. 4.1(c) is explained in the following. The static bias current source I_{b2} is replaced by a signal-dependent current source formed by transistors M_7-M_9. Consequently, the bias current of transistor M_6 and M_9 depends on the voltage level at the gate of the composite power transistor. With the signal-dependent current source, the sinking capability at node V_c is no longer limited by the static current source I_{b2}. The proposed low-voltage push-pull structure will provide extra transient current which is much larger than the static bias current at node V_c during transient event.

Similar to the Class-A counterpart, the frequency-dependent transconductance $G_{mp(push\text{-}pull)}$ is derived and given as

$$G_{mp(push-pull)} = \frac{\left(g_{m5}R_z + \frac{g_{m7}}{g_{m6}}\right)\left(1+\frac{g_{m7}C_2}{g_{m5}g_{m6}}s\right)}{\left(1+\frac{C_p\left(R_2+R_Z\right)}{g_{m6}R_2}s\right)\left(1+\frac{C_2R_ZR_2}{R_2+R_Z}s\right)} \times g_{mp} \qquad (4.2)$$

From (4.2), it can be seen that the transconductance of the push-pull composite power transistor is larger than that of the Class-A counterpart due to the signal-dependent current source. Besides, the signal-dependent current source also introduces a left-hand-plane zero. However, it is a function of parasitic capacitance

and can be located at high frequency easily. Furthermore, the parasitic pole is also located at high frequency. Similar to the Class-A version, the transconductance and bandwidth are independent of each other. Table 4.1 summaries the calculated poles and zero location in the push-pull composite power transistor. All the parameters used in the calculation are extracted from the simulation setup from the proposed LDO regulator in the following Section 4.3.1.

TABLE 4.1: POLES AND ZERO LOCATION OF CLASS-A COMPOSITE POWER TRANSISTOR

Parameters	Frequency locations
$z_1=g_{m6}g_{m5}/g_{m7}C_2$	~265MHz
$p_1=g_{m6}R_2/C_p(R_2+R_Z)$	~1.5 MHz
$p_2=(R_2+R_Z)/R_2R_ZC_2$	~67.22MHz

4.3.1 PROPOSED OCL-LDO REGULATOR WITH PUSH-PULL COMPOSITE POWER TRANSISTOR

The schematic of the proposed LDO regulator with push-pull composite power transistor is depicted in Fig. 4.3. The error amplifier is composed by five transistors M_1-M_4 and M_{b1} with $M_1=M_2$ and $M_3=M_4$. The transistors M_1 and M_2 form a differential pair whereas the transistors M_3 and M_4 form a current mirror. The transistor M_{b1} serves as the current source of error amplifier. The push-pull composite power transistor is formed by a low-voltage embedded gain stage (M_5-M_9) and a power transistor (M_P). C_m is the Miller compensation capacitor whereas C_p is the lumped parasitic capacitance at the gate of M_P. The feedback resistive divider network is realized by resistors R_{F1} and R_{F2}. The on-chip capacitance and

load current are represented by C_L and R_L, respectively.

The push-pull stage can be viewed as a buffer stage in the LDO regulator in [9], [61]. With the proposed push-pull composite power transistor, the high impedance node at the output of the error amplifier and the parasitic capacitance node at the gate of the conventional power transistor are decoupled. It benefits the LDO regulator to have a high stability performance as revealed by the analysis.

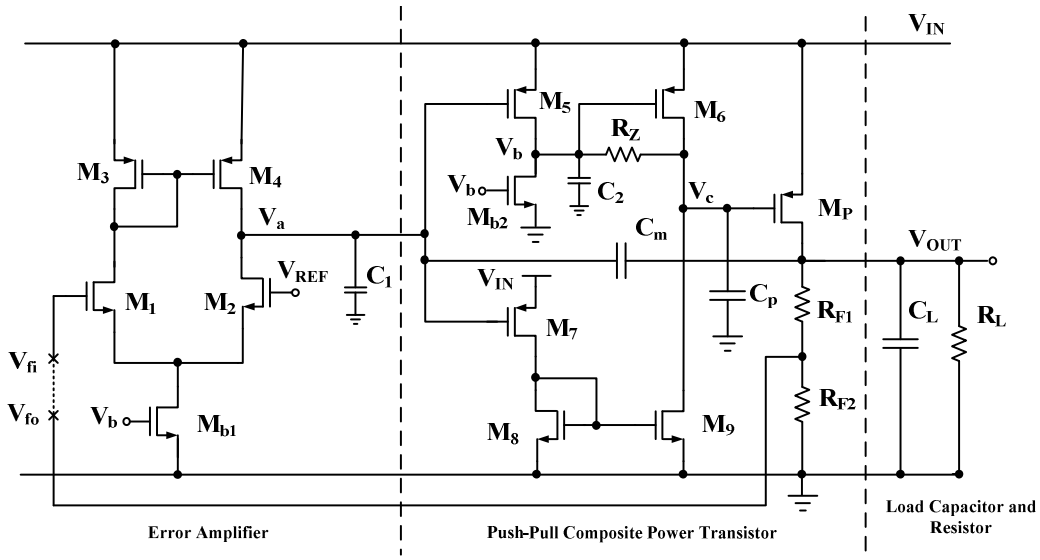


Figure 4.3: Schematic of the proposed OCL-LDO regulator with push-pull composite power transistor

The proposed LDO regulator can be considered as a quasi-two stage amplifier driving a capacitive load of C_L. With the proposed push-pull composite power transistor, the high impedance node at the output of the error amplifier and the parasitic capacitance node at the gate of the conventional power transistor are decoupled. It benefits the LDO regulator to have a high stability performance as revealed by the analysis.

4.3.1.1 STABILITY ANALYSIS

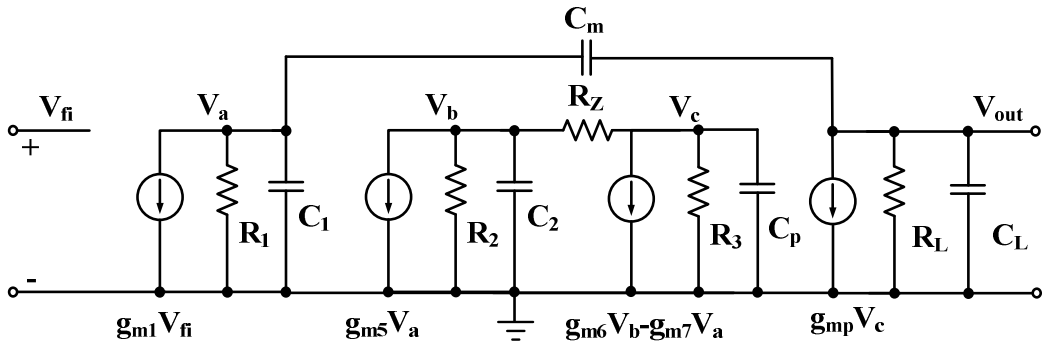


Figure 4.4: Small-signal model of the proposed LDO regulator with push-pull composite power transistor

The simplified small-signal model of the proposed LDO regulator is shown in Fig. 4.4. The stability is investigated using the loop-gain transfer function of the regulation loop. The transfer function is obtained as follows:

$$A_v = \frac{-g_{m1}g_{mp}A_E R_1 R_L\left[1+\left(\frac{g_{m7}R_Z C_2}{g_{m6}A_E}-\frac{C_m}{g_{mp}A_E}\right)s\right]}{\left(1+C_m g_{mp}A_E R_1 R_L s\right)\left(1+\frac{\frac{g_{m7}g_{mp}R_Z C_2}{g_{m6}}+C_L}{g_{mp}A_E}s+\frac{C_p C_L\left(R_2+R_Z\right)}{g_{mp}g_{m6}A_E R_2}s^2\right)} \quad (4.3)$$

where $A_E = g_{m5}R_Z + \frac{g_{m7}}{g_{m6}}$ is the gain of the push pull stage. The derivation is based on the following assumptions: (i) $g_{m1}R_1 >> 1$, $g_{m5}R_2 >> 1$, $g_{m6}R_3 >> 1$, (ii) $C_L >> C_m >> C_1$. From the transfer function, it can be observed that there are one dominant pole, a pair of complex poles and one zero. The dc gain and dominant pole p_{-3dB} are obtained as

$$A_{DC} = g_{m1}g_{mp}A_E R_1 R_L \quad (4.4)$$

$$p_{-3dB} = \frac{1}{C_m g_{mp} A_E R_1 R_L} \tag{4.5}$$

Since the load current varies greatly, the stability of the LDO regulator will be discussed at different loading conditions. There are two cases to be considered.

Case 1→ low to moderate load current

Under this case, the transistor M_P is working in subthreshold region. The transconductance g_{mp} is small. Therefore, $C_m/g_{mp}A_E >> g_{m7}R_ZC_2/g_{m6}A_E$, $C_L >> g_{m7}g_{mp}R_ZC_2/g_{m6}$ and the transfer function can be simplified as

$$A_v = \frac{-g_{m1}g_{mp}A_E R_1 R_L \left(1 - \frac{C_m}{g_{mp}A_E}s\right)}{\left(1 + C_m g_{mp} A_E R_1 R_L s\right)\left(1 + \frac{C_L}{g_{mp}A_E}s + \frac{C_p C_L (R_2 + R_Z)}{g_{mp}g_{m6}A_E R_2}s^2\right)} \tag{4.6}$$

Both the dc gain and dominant pole remain the same. Stability of this condition is determined by the location of the RHP zero and the non-dominant complex poles. Of particular interest, the location of the RHP zero is shifted to higher frequencies by a factor of A_E. The location of the non-dominant complex poles can be approximately modeled as

$$\left|p_{2,3}\right| = \sqrt{\frac{g_{mp}g_{m6}A_E R_2}{C_p C_L (R_2 + R_Z)}} \tag{4.7}$$

As indicated in (4.7), the non-dominant complex poles are a function of g_{mp} which is proportional to the square root of I_{LOAD}. This implies that the non-dominant complex poles are shifted to higher frequencies when I_{LOAD} increases. Therefore, the worst case stability happens at no load condition. The stability condition can be achieved by adjusting the compensation capacitor C_m and locating the non-dominant complex poles beyond the unity gain frequency (UGF) which is about 1 MHz in this design.

Case 2→ moderate to high load current

Under this case, the transistor M_P is working in saturation region. The transconductance g_{mp} is large. Therefore, $g_{m7}R_ZC_2/g_{m6}A_E >> C_m/g_{mp}A_E$, $g_{m7}g_{mp}R_ZC_2/g_{m6} >> C_L$ and the transfer function can be simplified to

$$A_v = \frac{-g_{m1}g_{mp}A_E R_1 R_L\left(1+\frac{g_{m7}R_ZC_2}{g_{m6}A_E}s\right)}{\left(1+C_m g_{mp}A_E R_1 R_L s\right)\left(1+\frac{g_{m7}R_ZC_2}{g_{m6}A_E}s+\frac{C_pC_L\left(R_2+R_Z\right)}{g_{mp}g_{m6}A_E R_2}s^2\right)} \quad (4.8)$$

The RHP zero is replaced by a high frequency LHP zero. It can be noticed that the location of the non-dominant complex poles still can be modeled by (4.7). Due to the large g_{mp}, the non-dominant poles are shifted to even higher frequencies. Therefore, the stability is ensured. Table 4.2 summaries the calculated poles and zero location.

TABLE 4.2: POLES AND ZERO LOCATION OF THE PROPOSED LDO REGULATOR

	Low to moderate load	Moderate to high load
zero	80MHz (RHP)	265MHz (LHP)
p_{-3dB}	4.5 kHz-1.7 kHz	1.7 kHz-1.3 kHz
$\|p_{2,3}\|$	2.7MHz-22.37MHz	22.37MHz-123MHz

By adopting the third-order Butterworth response, the dimension condition of the Miller compensation capacitor C_m can be found by

$$C_m = \frac{2\sqrt{2}g_{m1}}{\left|p_{2,3}\right|} = 2g_{m1}\sqrt{\frac{2C_pC_L\left(R_2+R_Z\right)}{g_{m6}g_{mp}A_E R_2}} \quad (4.9)$$

To ensure the stability, the C_m needs to be found at maximum C_L and minimum g_{mp} conditions. From (4.9), the dimension condition of the C_m is proportional to the square root of the product of C_p and C_L. This implies that the required compensation

capacitor size is smaller when compared to that of the conventional Miller compensation scheme which is directly proportional to the size of C_L. As a result, the silicon area can be reduced. Furthermore, the size of C_m can be further reduced by increasing g_{m6}, g_{m5} or g_{mp}.

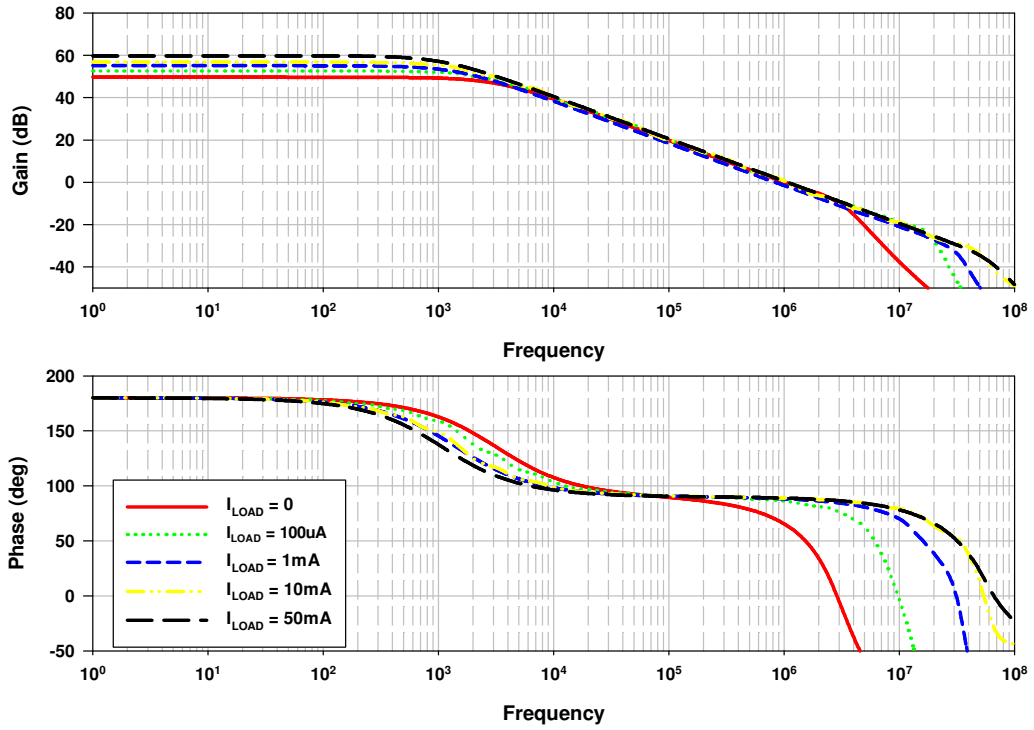


Figure 4.5: Simulated open-loop gain at different I_{LOAD} at C_L = 100 pF

Fig. 4.5 shows the simulated loop gain response of the proposed LDO regulator at different I_{LOAD} conditions. The regulator achieves a minimum phase margin of 60 degree at no load condition. As load current raises, the phase margin increases to approach 90 degree, suggesting that it is an effective one pole system. It is because the non-dominant complex poles are shifted to higher frequencies. The loop gain response simulation is conducted at C_L = 100 pF and C_m = 2 pF.

4.3.1.2 LARGE SIGNAL DYNAMIC BEHAVIORS

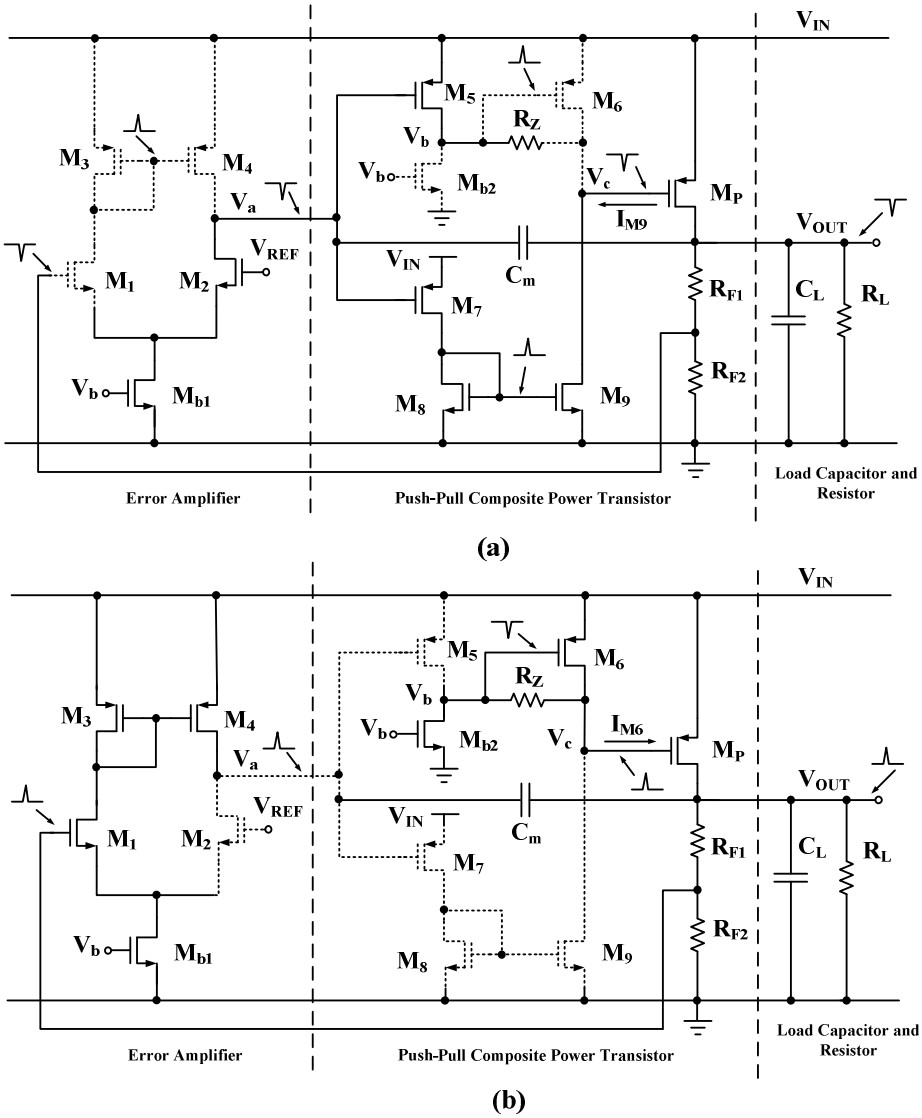


Figure 4.6: .Operation principle of the proposed LDO regulator (a) undershoot and (b) overshoot.

As shown in Fig. 4.6(a), when the I_{LOAD} suddenly increases, V_{OUT} drops rapidly and this drop is sensed and amplified by the error amplifier. This undershoot will force the transistor M_6 and M_9 to be in off and on, respectively. As a result, the gate of M_P is discharged by I_{M9}. The power transistor is then turned on to supply the required I_{LOAD}. Similarly, as illustrated in Fig. 4.6(b), when I_{LOAD} suddenly decreases, V_{OUT}

rises rapidly. This will create an overshoot that appears at the gate of both transistors M_5 and M_7. This turns out that the transistors M_6 and M_9 are on and off, respectively. The transistor M_6 injects current I_{M6} to charge the gate of M_P, causing the power transistor to turn off to decrease the I_{LOAD}.

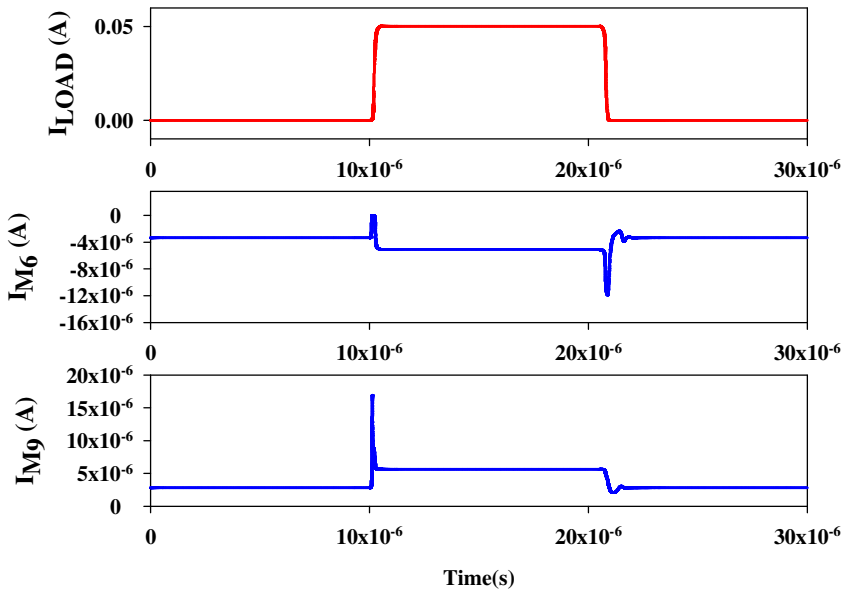


Figure 4.7: .Simulated transient currents of transistor M_6 and M_9.

Fig. 4.7 shows the simulated exemplary transient currents of transistor M_6 and M_9. As can be observed, when the I_{LOAD} is switched between 0 and 50 mA with edge time of 100 ns, V_{IN} = 0.75 V and V_{OUT} = 0.5 V, the transistors M_9 and M_6 are able to sink and source a peak current of 17 µA and 12 µA, respectively. The slew-rate of the composite power transistor is enhanced through the push-pull action. This leads to the improvement of the transient response of the LDO regulator without requiring a large static bias current.

4.3.1.3 EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed LDO regulator has been implemented and fabricated in a UMC 65-nm CMOS technology. In order to compare the performance with the counterparts, both regulators based on Class-A composite power transistor [29] and Q-reduction compensation technique [31] are also fabricated on the same die. The die micrograph is shown in Fig. 4.8. The active area of the proposed LDO regulator is only 0.0096 mm^2, excluding I/O pads.

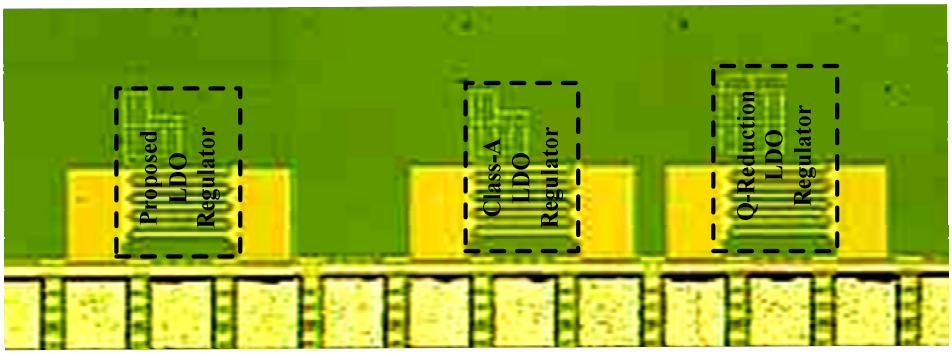


Figure 4.8: Micrograph of the proposed, Class-A and Q-reduction LDO regulators

The LDO regulators are able to deliver a maximum I_{LOAD} of 50 mA with an output voltage of 0.5 V for a supply range from 0.75-1.2 V. The measured quiescent current is 16.2 µA which includes 10 µA consumed by resistive divider. The on-chip compensation capacitor C_m is 2 pF and an off-chip capacitor of 100 pF is used to emulate the on-chip capacitance C_L. The measured results of the proposed LDO regulator are summarized in Table 4.3.

TABLE 4.3: PERFORMANCE SUMMARY OF THE PROPOSED LDO REGULATOR

V_{IN} (V)	0.75-1.2
V_{OUT} (V)	0.5
I_Q (µA)	16.2
I_{LOAD} (mA)	0-50
Load Reg. (mV/mA)	0.56
Line Reg. (mV/V)	6.67
$-\Delta V_{OUT}$ (mV)	103
$+\Delta V_{OUT}$ (mV)	100
PSR	-46@1kHz
Unity-Gain Frequency	1MHz

Fig. 4.9(a)-(c) show the measured load transient responses comprising the proposed LDO, Class-A LDO and Q-reduction LDO. In waveforms (a)-(c), the I_{LOAD} is switched between 0 and 50 mA in 100 ns with V_{IN} = 0.75 V. It can be seen that, the proposed LDO regulator with push-pull composite power transistor displays an undershoot and overshoot of 103 mV and 100 mV, respectively. The LDO regulator with Class-A composite power transistor has a large undershoot due to the limited sinking capability at the gate of power transistor. For the Q-reduction LDO regulator, both undershoot and overshoot are relatively large because the internal slew rate is greatly affected by the compensation capacitors. Waveforms (d), (e) and (f) display the results from different measurement set-up conditions for the proposed LDO. As expected, the LDO remains stable. Of particular interest, there is no impact to the undershoot and overshoot performance at zero C_L condition. Besides, the undershoot and the overshoot are smaller when edge time becomes 1 µs.

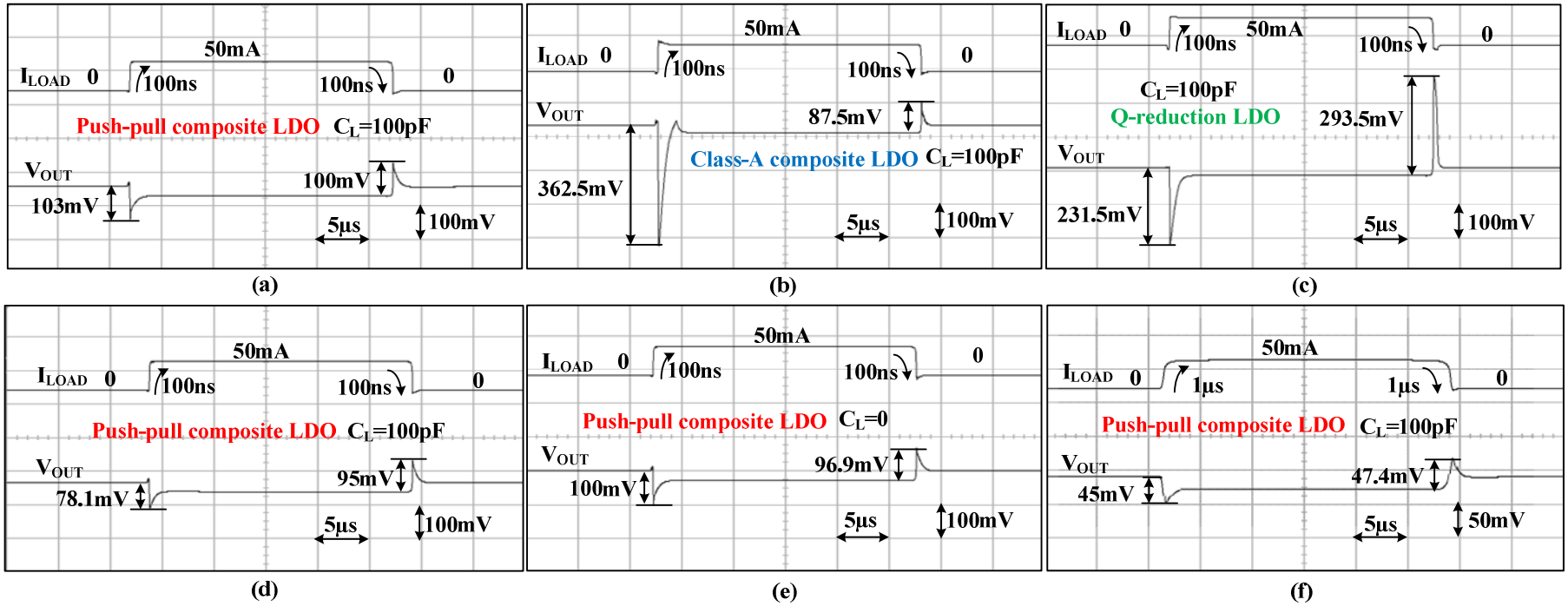


Figure 4.9: Measured load transient responses of the three LDO regulators with (a)-(c) V_{IN} = 0.75 V, V_{OUT} = 0.5 V and C_L = 100 pF, (d) V_{IN} = 1.2 V, V_{OUT} = 0.5 V and C_L = 100 pF, (e) V_{IN} = 0.75 V, V_{OUT} = 0.5 V and C_L = 0 and (f) V_{IN} = 0.75 V, V_{OUT} = 0.5 V, C_L = 100 pF and edge time = 1 µs

Fig. 4.10(a) shows the measured load regulation of the proposed LDO regulator. The voltage drop at high load condition is due to the parasitic resistance of the single bonding wire which is around ~400 mΩ from the MediaTek QFN40 packaging. Therefore, the IR drops can be as large as 25 mV when I_{LOAD} = 50 mA. To demonstrate the IR drop of the bonding wire, simulations with and without a 500 mΩ parasitic resistor are performed and depicted in Fig. 4.10(b).

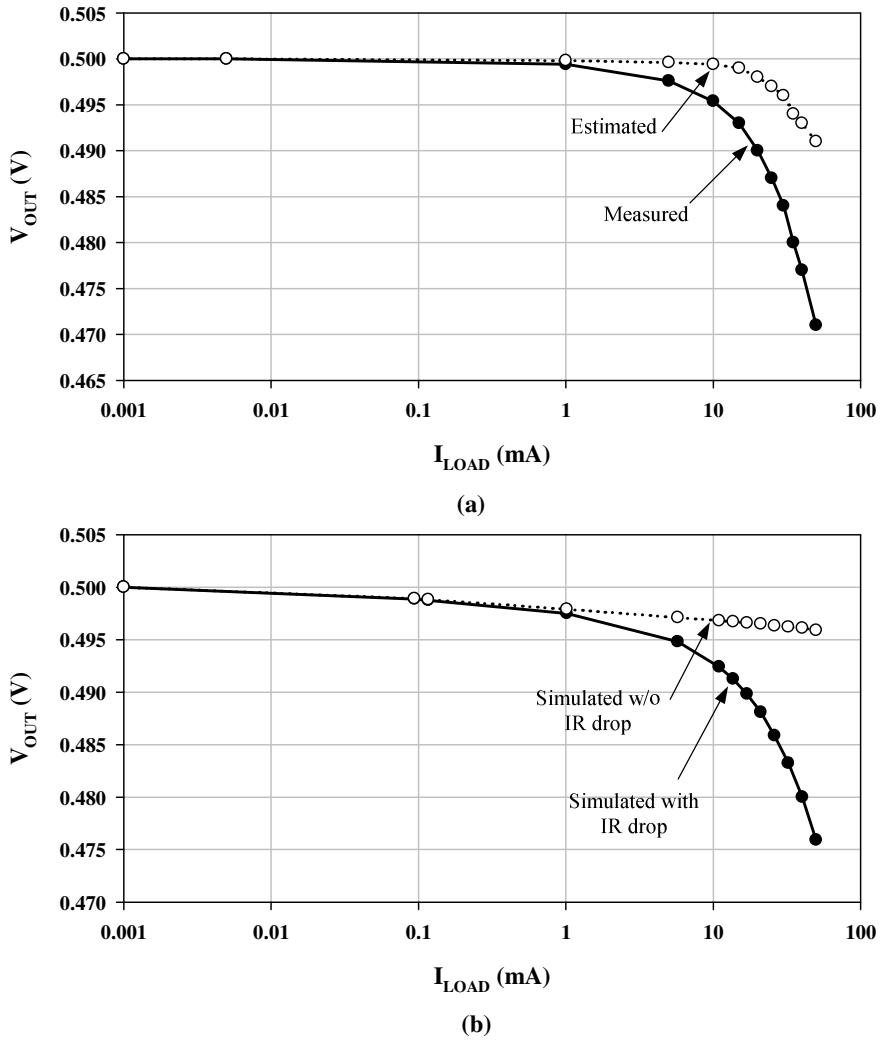


Figure 4.10: (a) Measured load regulation (b) Simulated load regulation at V_{IN} = 0.75 and V_{OUT} = 0.5V

It can be seen that the measured and simulated results are close to each other. The estimated load regulation which excludes the IR drop is added for comparison. The load regulation due to IR drop at high load current condition can be improved by using the multiple bonding wires or Kelvin connection. Due to the limited IO pads in the test chip, only single IO pad is used the LDO regulator output.

Fig. 4.11 shows the measured dropout voltage as a function of load current at V_{IN} = 0.75 V. The dropout voltage is less than 250 mV when I_{LOAD} = 50 mA. Fig. 4.11 also suggests that the dropout voltage can be designed to be a smaller value when the required maximum I_{LOAD} is smaller.

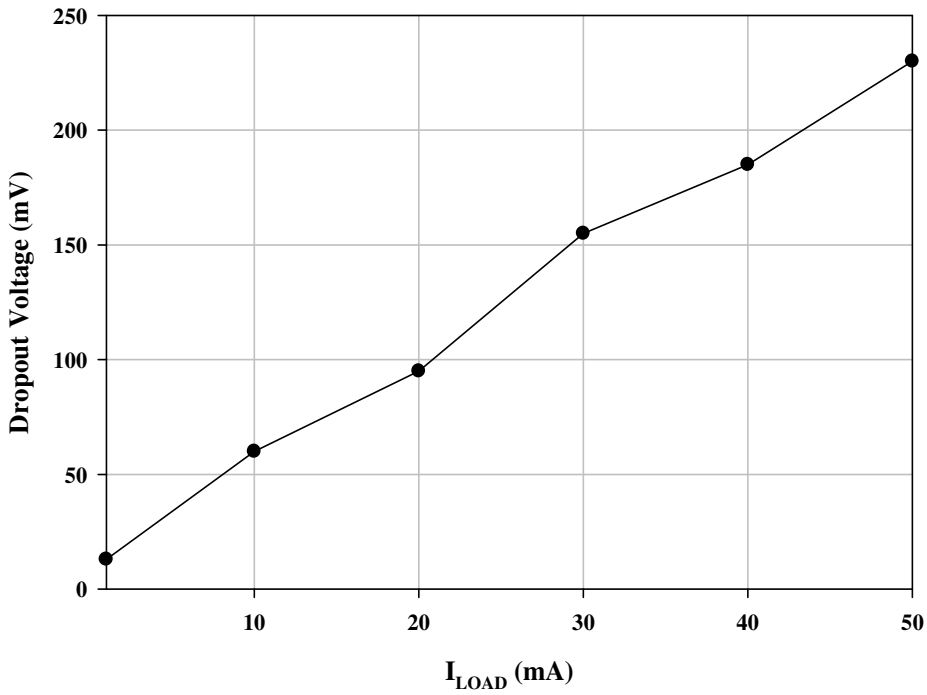


Figure 4.11: Measured dropout voltage as a function of I_{LOAD} at V_{IN} = 0.75 V

Finally, the measured PSR at load current of 50 mA, V_{IN} = 0.75 V, V_{OUT} = 0.5 V and C_L = 100 pF is shown in Fig. 4.12. The PSR is measured by using a network analyzer (HP 4395A) and a high impedance active probe (HP 41800A). The proposed OCL-LDO regulator has achieved a PSR of -46 dB at 1 kHz.

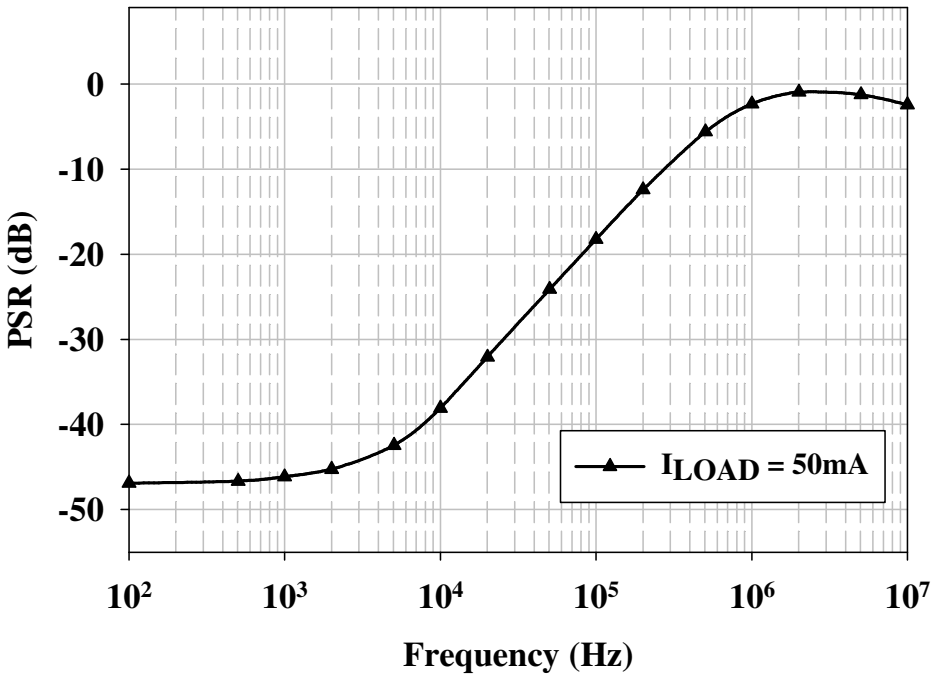


Figure 4.12: Measured PSR of proposed OCL-LDO at V_{IN} = 0.75 and I_{LOAD} = 50 mA

As can be shown in Fig. 4.13, with an external voltage reference, the measured temperature coefficient of the proposed LDO regulator is 63 ppm/°C at I_{LOAD} = 50 mA.

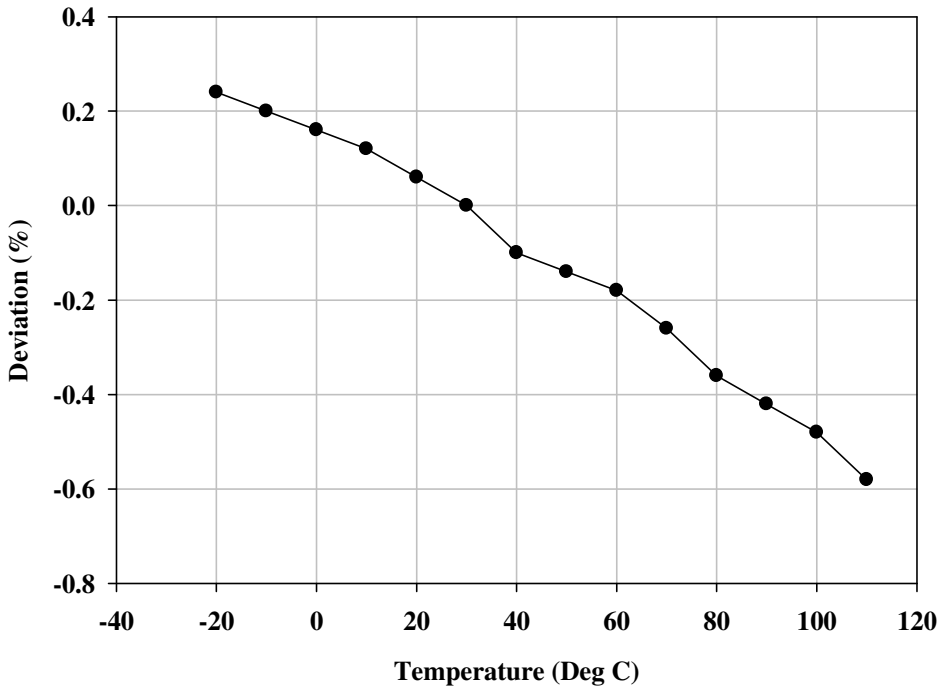


Figure 4.13: Measured temperature dependence at I_{LOAD} = 50 mA

The performance of the proposed LDO regulator is compared to the reported OCL-LDO regulators in Table 4.4. The figure-of-merit (FOM) in [41] is adopted for comparison. The proposed design achieves the smallest FOM than all the works except [41]. However, the tradeoff is that it requires a minimum I_{LOAD} of 3 mA to maintain stable operation. In view of silicon area, it is comparable with that of recently reported work [41] having similar specification as well as technology. Therefore, area-efficiency of the proposed work is demonstrated.

TABLE 4.4: PERFORMANCE COMPARISON WITH REPORTED PRIOR-ART OCL-LDO REGULATORS

Parameters	[62]	[63]	[41]	[64]	[65]	[66]	[31]*	[29]*	**This work**
Technology (µm)	0.18	0.35	0.09	0.18	0.35	0.13	0.065	0.065	**0.065**
Chip Area (mm^2)	0.07	0.096	0.019	0.09	0.064	0.018	0.011	0.0096	**0.0096**
$I_{LOAD(max)}$ (mA)	50	50	100	50	100	50	50	50	**50**
$I_{LOAD(min)}$ (mA)	0	0	3	0.05	0.05	0.05	0	0	**0**
V_{IN} (V)	0.65-0.95	0.9-2	0.75-1.2	1.2-1.8	2.5-4	1.2-1.4	0.75-1.2	0.75-1.2	**0.75-1.2**
V_{OUT} (V)	0.5	0.5	0.5	1	2.35	1	0.5	0.5	**0.5**
$C_{on\text{-}chip}$ (pF)	N.A.	0	7	0	7.5	21	5	2	**2**
C_L (pF)	0	0	0-50	0-100	0-100	0-20	0-100	0-100	**0-100**
I_Q (µA)	12.72	0.103	8	1.2	7	37.32	18.6	17.5	**16.2**
$-\Delta V_{OUT}$ (mV)	300	~300	73	~400	236	54	231.5	362.5	**103**
$+\Delta V_{OUT}$ (mV)	N.A.	~320	114	~350	227	40	293.5	87.5	**100**
ΔI_{LOAD} (mA)	50	50	97	49.95	99.95	49.95	50	50	**50**
Settling Time (µs)	10	400	5	3	0.15	0.4	1.85	1.2	**1.2**
Unity-gain Freq. (MHz)	N.A.	N.A.	1	N.A.	N.A.	3.84	1	1	**1**
Edge time (ns)	N.A.	N.A.	100	N.A.	500	200	100	100	**100**
FOM (µV) [41]	N.A.	N.A.	9.4	N.A.	82.6	80.7	109.2	126.9	**33.4**

* Implemented in 65 nm for comparison

4.4 PROPOSED DYNAMIC-BIASED COMPOSITE POWER TRANSISTOR

Fig. 4.14 depicts the composite power transistor with pseudo push-pull [67] circuit structure which is also an open-loop structure. This is favorable to stability as well as bandwidth extension.

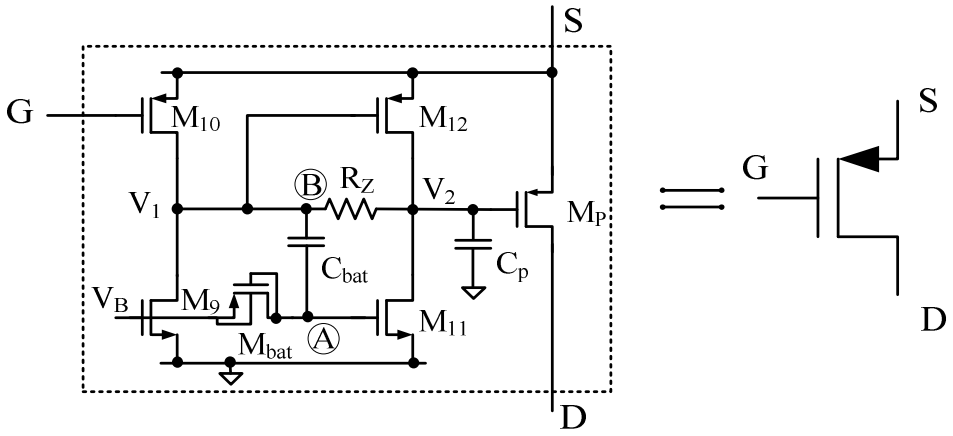


Figure 4.14: Composite power transistor with pseudo push-pull structure

As shown in Fig. 4.14, the composite power transistor can be viewed as a three terminal transistor with the body tied to the source terminal. Different from the push-pull technique realization proposed in the section 4.3, the embedded gain stage in the composite power transistor is modified from a Class-A to push-pull output stage by applying the biasing technique in [68]. The output stage of the embedded gain stage is now synthesized in a form of an economic CMOS push-pull structure. The slew rate at the gate of transistor M_p is enhanced due to the current boosting effect by the push-pull structure. The transistor M_{bat} functions as a very large resistor, called "pseudoresistor" [69]. In order to realize a very large resistor, M_{bat} is biased in the cut-off region where the resistance is very high. C_{bat} acts like a floating

battery and it serves as a voltage divider with the parasitic capacitance at node A. Depending on the parasitic capacitance at node A, a suitable value of C_{bat} can be chosen. As a design guideline, C_{bat} is recommended to be 5~10 times larger than parasitic at node A. During transient condition, the voltage at node B, V_{GS} of transistor M_{12}, is subjected a large change and C_{bat} cannot be charged or discharged through transistor M_{bat} immediately. The voltage changes at node B are transferred to node A so as to provide the push-pull operation to the output stage of embedded gain stage. The maximum voltage swing at node V_2 of the composite power transistor is approximated by $I_{b1}R_Z$. The value of R_Z can be obtained based on the DC voltage gain and voltage swing consideration.

Similar to the previous section, the stability is investigated by the small-signal model. The derived transfer function is

$$G_{mp(Class-AB)} = \frac{g_{m10}R_Z}{\left(1+\frac{C_p}{g_{m12}}s\right)\left(1+R_Z C_1 s\right)} \times g_{mp} \tag{4.10}$$

From (4.10), it can be seen that the gain of the embedded gain stage is approximately $g_{m10}R_z$ and the bandwidth is given by g_{m12}/C_p. As a result, the bandwidth can be increased by increasing g_{m12} when the dynamic-biasing technique is introduced. The same applies for the gain parameter g_{m10}.

In order to achieve ultra-low quiescent current and improve the current efficiency at light loads, the dynamic-biasing technique [26] is applied to the embedded gain stage, in which the biasing current is made proportional to the load current. Since the power transistor operates across all three operating regions (sub-threshold, saturation and triode), it is hard to obtain an accurate current sensing. However, it still provides

the standard back-end dynamic current sensing function if an extra unit transistor is placed close to the power device. The scheme can be extended to the frontend dynamic current sensing function via sensing the current through M_{10}. This is due to the finite gain of the embedded gain stage that yields the moderate signal swing at the gate of M_{10}. It gives a more accurate sensing value because the transistor M_{10} operates only in saturation region. In addition, the scaling for a lower dynamic biasing current is relatively easier because the dynamic current in M_{10} is smaller than that of the power device.

The schematic of the composite power transistor with the dynamic-biasing scheme is shown in Fig. 4.15. As can be observed, both the back-end and front-end dynamic-biasing networks are adopted in this design.

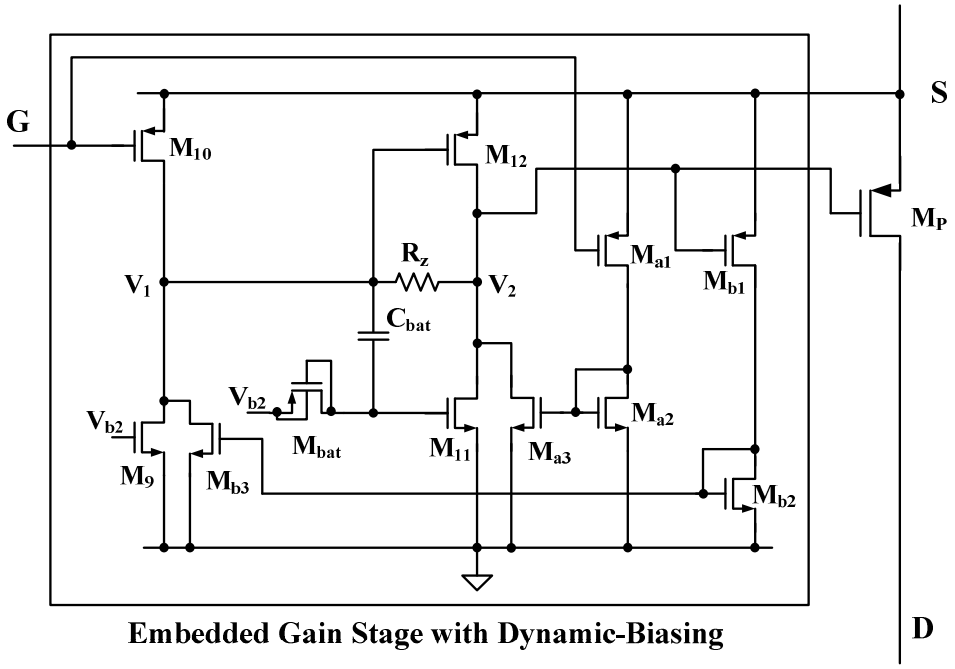


Figure 4.15: Dynamic-biased composite power transistor

The front-end dynamic-biasing network is formed by transistors M_{a1}-M_{a3}. Transistors M_{a1} and M_{10} are driven by the same input signal of the composite power

transistor and biased by the same V_{GS}. The drain current of M_{a1} and M_{10} is designed to have a current ratio of 1 : K. The current is then copied to increase the biasing current of M_{12}, which is located at the output stage of the embedded gain stage. Hence, the driving capability and slew rate of the embedded gain stage can be increased. Consequently, the increase of the transconductance of M_{12} pushes the pole at the output of the embedded gain stage to a higher frequency. Turning to the back-end dynamic-biasing network, it is formed by transistors M_{b1}-M_{b3}. The biasing current of M_{10} is made proportional to the load current. Similar to the front-end network, the transistor M_{b1} and M_p is in a current ratio of 1 : N. Since the accuracy of the current ratio between M_{b1} and M_p is not critical in the design, the extra biasing current from M_{b3} increases the transconductance of M_{10}. The overall gain of the embedded gain stage is thereby enhanced. It should be noted that the dynamic current copied from M_{a1} cannot be used for M_{10}. It is mainly because this forms a positive feedback loop from M_{10} to M_{b3}, jeopardizing the operation of the circuit. Therefore, the biasing current of M_{10} is achieved by second part of the dynamic-biasing network.

4.4.1 PROPOSED LDO REGULATOR WITH DYNAMIC-BIASED COMPOSITE POWER TRANSISTOR

The schematic of the proposed LDO regulator is depicted in Fig. 4.16. The error amplifier is realized by a single folded cascode stage with transistors M_0-M_8. Besides the normal biasing current for the weak inversion design of the amplifier, a dynamic-biasing network which is formed by the transistors M_{a1}-M_{a2} and M_{a4}-M_{a8} is added to improve the bandwidth of the circuit under high load currents. The

conventional power transistor is replaced by the dynamic-biased composite power transistor. It also constitutes the second gain stage in the LDO regulator. The embedded gain stage has the same function as that of the buffer stage [9] in the conventional LDO regulator whilst providing gain to enhance the current driving capability of the regulation transistor. The feedback network is realized by two diode-connected PMOS transistors, M_{R1} and M_{R2}, with same aspect ratio. By using this approach, the silicon area of the feedback network is smaller as compared to the conventional approach using passive resistors. Since M_{R1} and M_{R2} are identical in design, the reference voltage, V_{ref}, is half of the LDO regulator output voltage. Finally, the proposed LDO regulator consists of an external load that sources I_{LOAD} and an external capacitor C_L with its series resistance R_e.

The proposed LDO regulator can be treated as a quasi two-stage amplifier driving a large capacitive load and can be stabilized by means of both Miller and cascode compensation techniques. Such a two-stage structure avoids complicated frequency compensation schemes that may jeopardize the low quiescent power objective in exchange of the stability for multi-stage (>2) LDO regulator design. Cascode compensation offers high power-bandwidth efficiency and displays the robustness with respect to other frequency compensation techniques when driving a very large capacitive load. Moreover, cascode compensation scheme allows the amplifier to achieve a wider UGF, better PSR as well as improve the stability by removing the right-hand-plane zero. However, cascode compensation suffers from the peaking effect which decreases the gain and phase margin for stability. Hence, only a small Miller capacitor is introduced to avoid the peaking effect arising from the cascode compensation. Nevertheless, there is a trade-off between the stability and PSR.

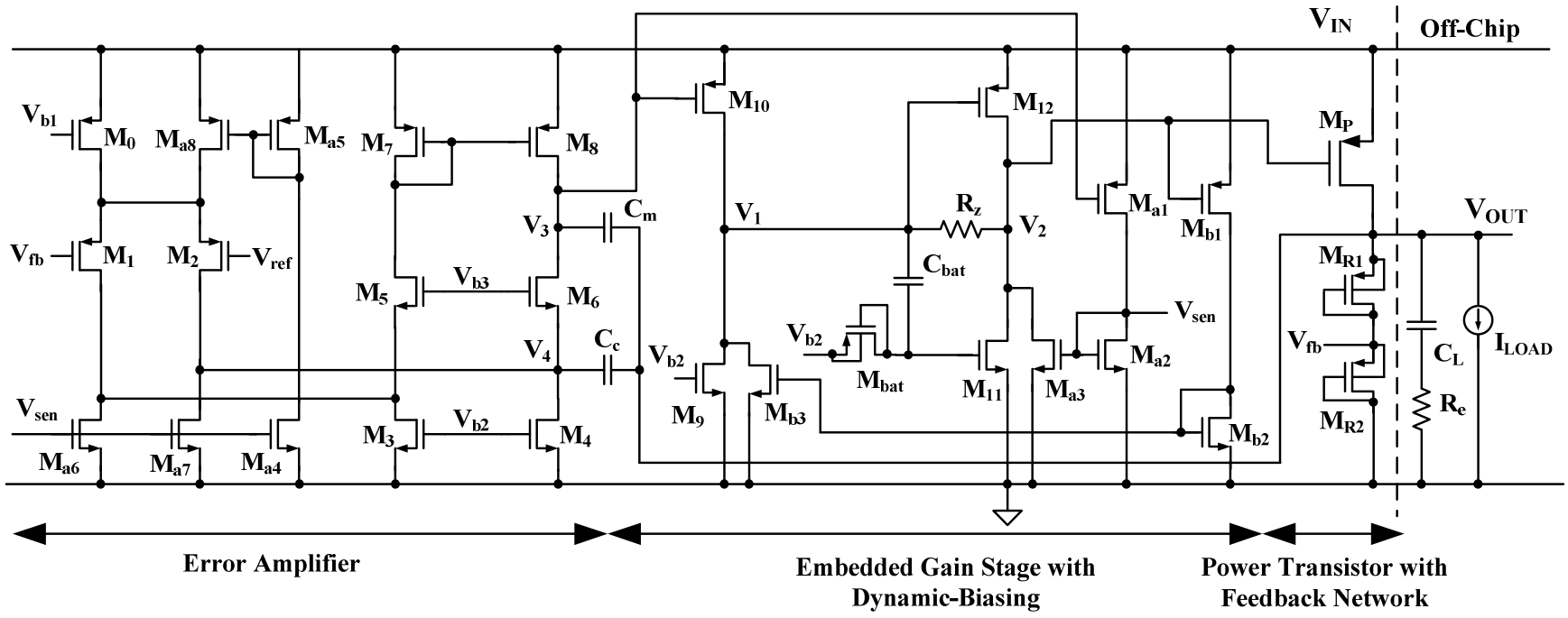


Figure 4.16: Schematic of the proposed LDO regulator with dynamic-biased composite power transistor

4.4.1.1 STABILITY ANALYSIS

Fig. 4.17 shows the simplified small-signal model of the proposed LDO regulator. The stability analysis is based on the loop-gain transfer function of the regulation loop. Note that g_{mi} is the transconductance of the respective device and R_{oi} is the output resistance of the respective stage. G_{mp} is the frequency-dependent transconductance of the composite power transistor.

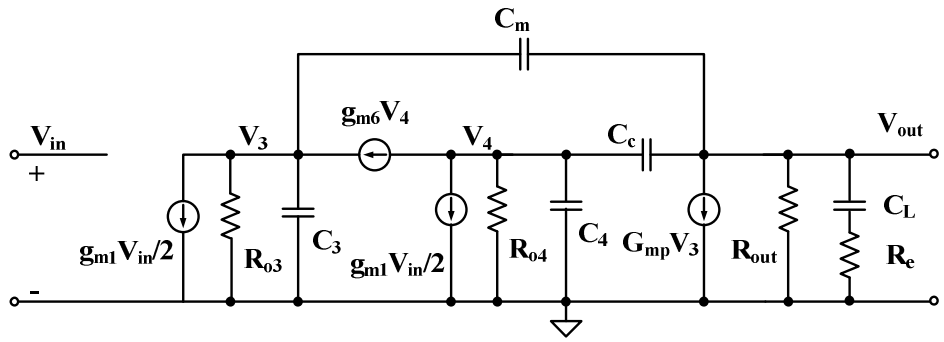


Figure 4.17: Small-signal model of the proposed LDO regulator

The transfer function of the proposed LDO regulator can be approximated as

$$T(s) \approx -\frac{A_{dc}}{\left(1+\frac{C_2}{g_{m12}}s\right)} \times \frac{\left(1+C_L R_e s\right)\left(1+\frac{C_c}{g_{m6}}s\right)}{\left(1+as+bs^2+cs^3\right)} \tag{4.11}$$

$$a = C_L R_{out} + R_{out} R_{o3} G_{mp0} (C_m + C_c) \tag{4.12}$$

$$b = C_L (C_m + C_3) R_{out} R_{o3} \tag{4.13}$$

$$c = \frac{C_L (C_m + C_3) C_c R_{out} R_{o3}}{g_{m6}} \tag{4.14}$$

where $A_{dc} = g_{m1}G_{mp0}R_{o3}R_{out}$ is the DC loop gain. In the LDO regulator design, the transconductance and the output resistance of composite power transistor form the gain of the output stage. This gain is inversely proportional to the square root of the load current ($1/\sqrt{I_{LOAD}}$). Since the output load current varies greatly, the stability of the proposed LDO regulator will be discussed for different loading conditions.

When $I_{LOAD} = 0$, the power transistor M_p is working in sub-threshold region, the transconductance as well as the output resistance is at its minimum and maximum, respectively. Therefore, $C_L R_{out} >> R_{out}R_{o3}G_{mp0}(C_m+C_c)$ and the transfer function can be simplified and given by

$$T(s)\Big|_{I_{LOAD}=0} \approx$$
$$-\frac{A_{dc}}{\left(1+\frac{C_2}{g_{m12}}s\right)}\times\frac{\left(1+C_L R_e s\right)\left(1+\frac{C_c}{g_{m6}}s\right)}{\left(1+C_L R_{out}s+C_L(C_m+C_3)R_{out}R_{o3}s^2+\frac{C_L(C_m+C_3)C_c R_{out}R_{o3}}{g_{m6}}s^3\right)} \quad (4.15)$$

From (4.15), there are 4 LHP poles and 2 LHP zeros in this system. If the dominant pole, second pole, third pole and composite power transistor pole are separated widely, the pole-zero analysis result can be estimated as follows:

$$p_{-3dB} = -\frac{1}{C_L R_{out}} \quad (4.16)$$

$$p_{com} = -\frac{g_{m12}}{C_2} \quad (4.17)$$

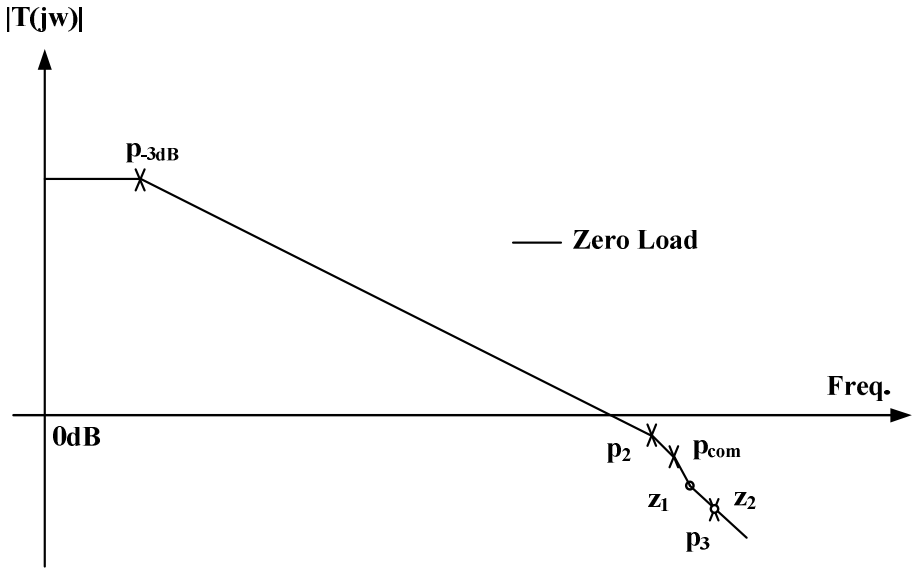
$$p_2 = -\frac{1}{(C_m+C_3)R_{o3}} \quad (4.18)$$

$$p_3 = -\frac{g_{m6}}{C_c} \tag{4.19}$$

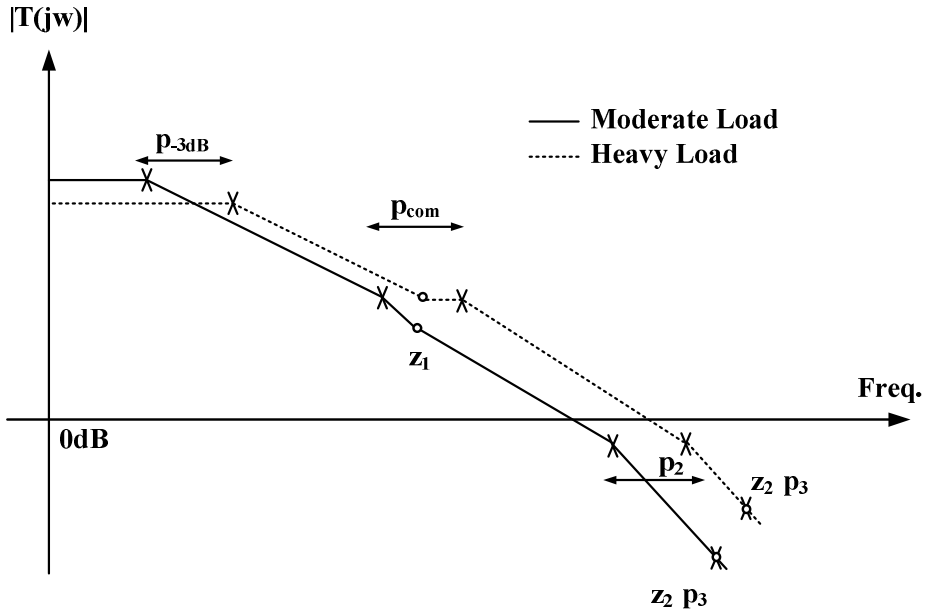
$$z_1 = -\frac{1}{C_L R_e} \tag{4.20}$$

$$z_2 = -\frac{g_{m6}}{C_c} \tag{4.21}$$

Fig. 4.18(a) shows the relative position of poles and zeros with reference to the UGF at very low quiescent biasing condition. Except the dominant pole at the output of the regulator, all the poles and zeros are located higher than the UGF. Thus, a good phase margin is achieved when $I_{LOAD} = 0$. It is interesting to observe that p_3 cancels z_2.



(a)



(b)

Figure 4.18: Loop gain of the proposed LDO structure. (a) zero load. (b) moderate and heavy load

When there is a certain increase of load current, the power transistor M_p is moving from sub-threshold region to saturation region. The transconductance, g_{mp}, and the output resistance R_{out} increase and decrease respectively when the load current increases. The dominant pole in (4.16) is shifted to higher frequencies as the output resistance of the LDO regulator decreases. However, the LDO regulator is still stable, as long as the p_2 is located outside the UGF. When the load current continues increasing, the transconductance of composite power transistor G_{mp} also increases significantly. At the juncture, the composite power transistor starts to provide gain function, and the pole splitting takes places. The new dominant pole will be contributed by the Miller and Miller Cascode effect. Therefore, $C_L R_{out}$ <<

$R_{out}R_{o3}G_{mp0}(C_m+C_c)$ and the transfer function can be simplified and given by

$$T(s)\Big|_{I_{LOAD}\neq 0} \approx -\frac{A_{dc}}{\left(1+\frac{C_2}{g_{m12}}s\right)}\times \frac{\left(1+C_L R_e s\right)\left(1+\frac{C_c}{g_{m6}}s\right)}{\left(1+G_{mp0}R_{o3}R_{out}\left(C_m+C_c\right)s+C_L(C_m+C_3)R_{out}R_{o3}s^2+\frac{C_L(C_m+C_3)C_cR_{out}R_{o3}}{g_{m6}}s^3\right)} \tag{4.22}$$

The transfer function indicates that there are 4 LHP poles and 2 LHP zeros in this system under this condition. The location of the poles and zeros can be estimated as:

$$p_{-3dB} = -\frac{1}{G_{mp0}R_{out}R_{o3}\left(C_m+C_c\right)} \tag{4.23}$$

$$p_{com} = -\frac{g_{m12}}{C_2} \tag{4.24}$$

$$p_2 = -\frac{G_{mp0}}{C_L}\times\frac{C_m+C_c}{C_m+C_3} \tag{4.25}$$

$$p_3 = -\frac{g_{m6}}{C_c} \tag{4.26}$$

$$z_1 = -\frac{1}{C_L R_e} \tag{4.27}$$

$$z_2 = -\frac{g_{m6}}{C_c} \tag{4.28}$$

The dominant pole is no longer located at the output of LDO regulator, but at the output of error amplifier. The stability of the LDO regulator is now depending upon the separation between the new dominant pole and other poles and zeros. As shown in Fig. 4.18(b), the dominant pole (p_{-3dB}) and non-dominant poles (p_{com} and p_2) are

made proportional to the load currents. They shift to higher frequencies together as the load current increases. In addition, the ESR zero, z_1, is now used to cancel the pole p_{com}. Therefore, the LDO regulator can be maintained stable, as long as the pole-zero separation is less than half of a decade, indicating that the G_{mp} term is approximately frequency-independent. Finally, since p_3 cancels z_2 and p_2 is easily made larger than UGF through the cascode factor, the system is approximated as a single pole system. When the load current keeps increasing, the power transistor moves from saturation region to triode region. The output resistance R_{out} is dominated by either r_{op} or R_L whilst the DC loop gain drops.

The dynamic-biasing technique is applied to the error amplifier as well as the embedded gain stage of composite power transistor. Besides the quiescent-aware implementation, another objective is to enhance the bandwidth when the load current increases. Since the additional biasing current pushes both the dominant and non-dominant poles to higher frequencies together, the stability of the proposed LDO regulator is not affected when the dynamic-biasing technique is applied. In a final remark, the PSR of the system is effectively improved due to the wider loop-gain bandwidth.

4.4.1.2 SIMULATED RESULTS AND DISCUSSIONS

To verify the effectiveness of the dynamic-biased embedded gain stage for the proposed composite power transistor shown in Fig. 4.15, it is implemented and simulated using GLOBALFOUNDRIES 0.18-µm CMOS process and BSIM3 models.

The simulated frequency responses of the proposed embedded gain stage under different biasing conditions are depicted in Fig. 4.19. The UGF is obtained as 0.6 MHz, 7 MHz, 18 MHz and 50 MHz for biasing currents of 2 µA, 5.5 µA, 15.5 µA and 50 µA, respectively. The simulation results have validated that the gain and pole frequency are proportional to the transconductance parameters, g_{m10} and g_{m12}, through the dynamic increase of the biasing currents.

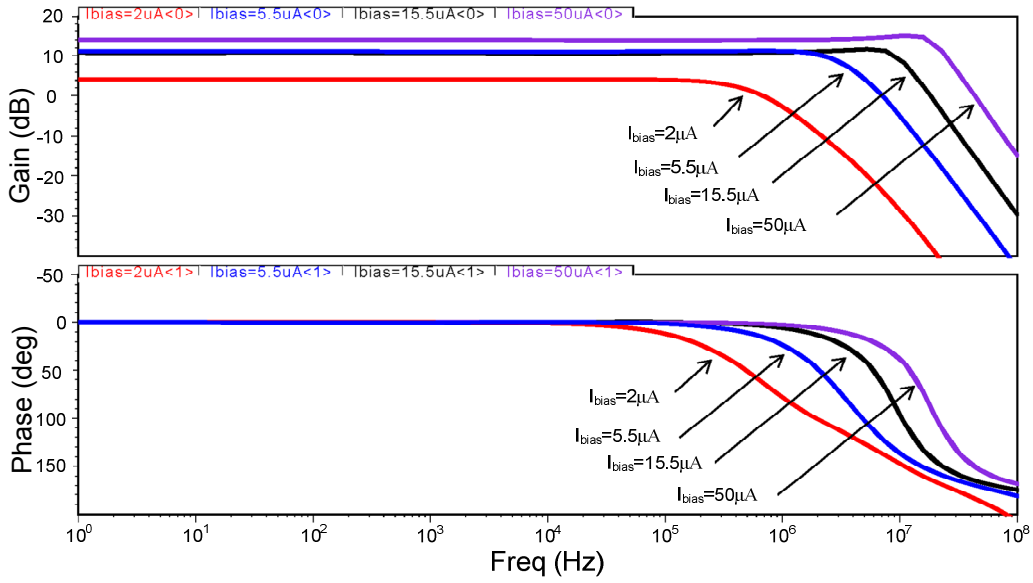


Figure 4.19: Open-loop frequency response of the proposed embedded gain stage at different biasing conditions

The proposed LDO regulator is designed to deliver 0 to 450 mA output current which is sufficient for most of the applications with an output voltage of 1 V from 1.2 to 1.8 V supply. The dropout voltage is 200 mV at the maximum load current. The aspect ratio of power transistor is 13500 µm/ 0.18 µm. It is based on the parallel of 1500 unit transistors having the aspect ratio of 9 µm /0.18 µm. The total on-chip capacitance is only 1.15 pF which occupies a very small area. The quiescent current is 4.7 µA under no-load condition while the quiescent current of 84.91 µA is

consumed at full load condition. Line regulation at output is 156 µV/V at full load condition. Load regulation is 7.73 µV/mA at V_{IN} = 1.2 V. It can be seen that the dynamic parameters show good performance results. The current efficiency can reach more than 99% at both the light load and full load, suggesting that the influence of dynamic biasing technique to the current efficiency is of no concern. The simulated loop-gain frequency responses of the proposed LDO regulator at the load currents of 0, 1 mA, 10 mA, 100 mA and 450 mA for C_L = 4.7 µF and Re = 0.1 Ω are shown in Fig. 4.20. It demonstrates that the proposed LDO regulator is stable and the improvement of the UGF when the dynamic-biasing technique is adopted.

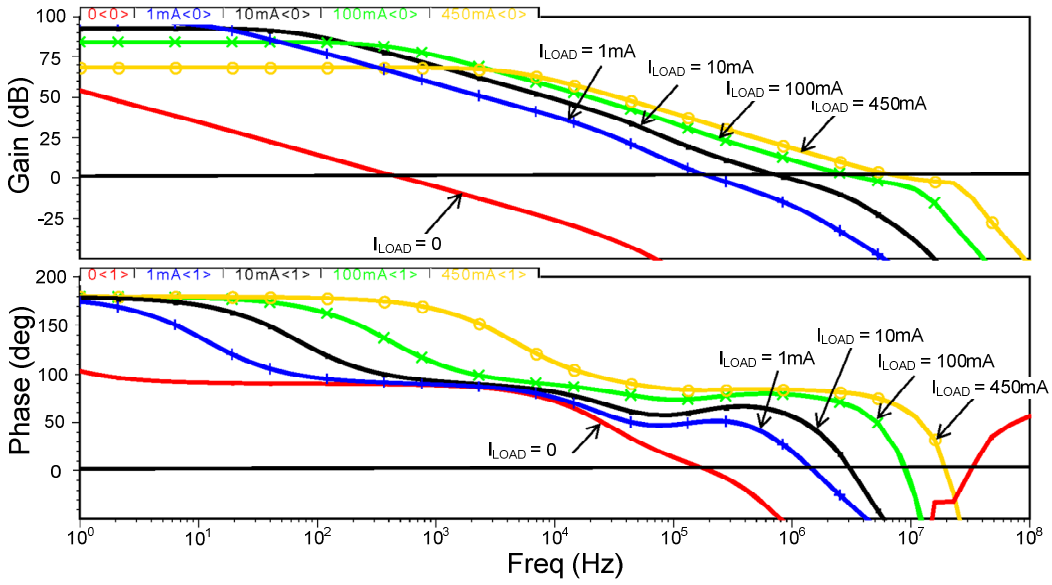


Figure 4.20: Open-loop frequency response of the proposed LDO regulator at 0, 1mA, 10mA, 100mA and 450mA

Fig. 4.21 shows the simulated phase margin of the loop gain transfer function under different process corners at the extreme temperatures for the whole range of the load current. The minimum phase margin is always larger than 45 degree under typical condition. However, the worst case happens when the process is ss (slow NMOS

and slow PMOS) at -40 °C where the minimum phase margin is 35 degree at $I_{LOAD} \approx$ 200 µA.

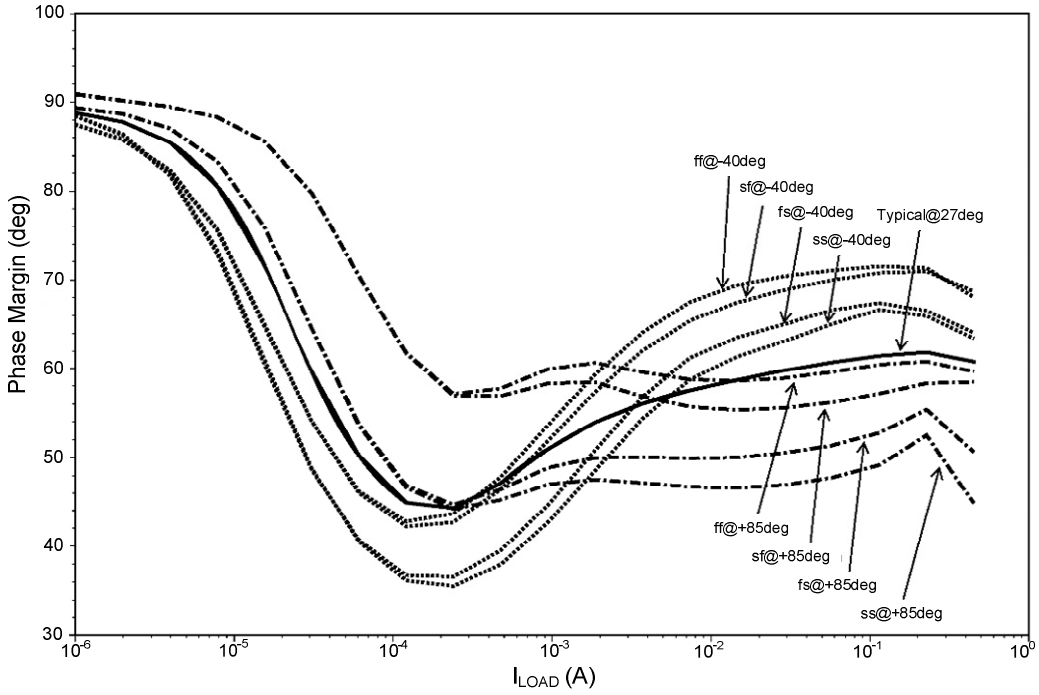
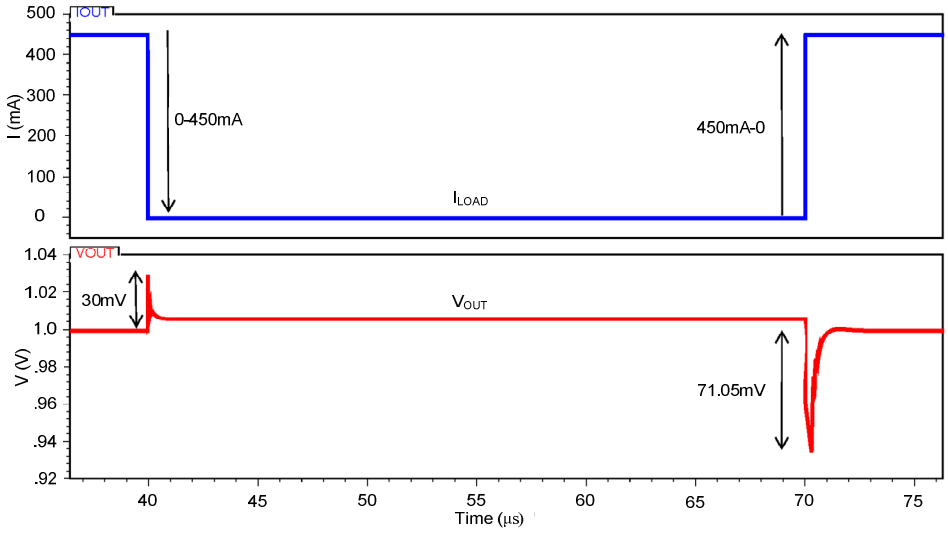
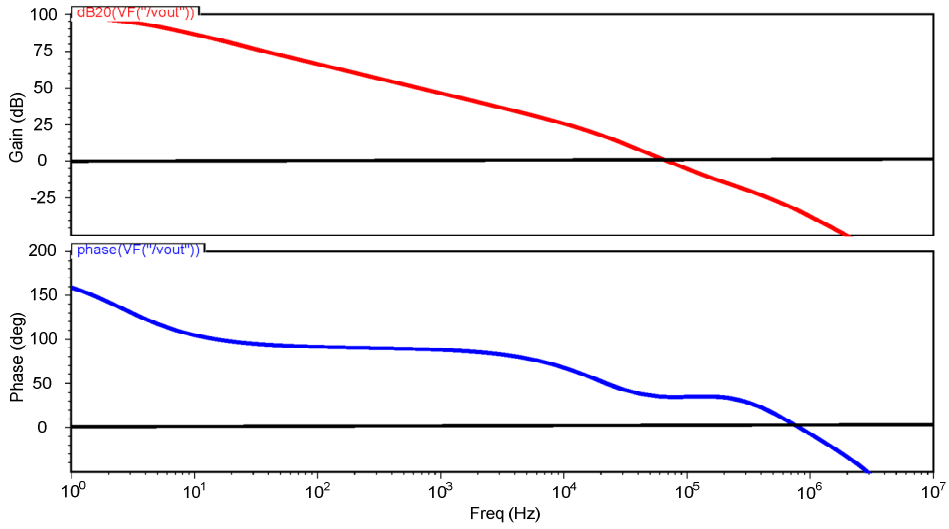


Figure 4.21: Phase margin of the proposed LDO regulator as a function of load current under extreme temperatures and process corners

To investigate the stability under such condition, the transient and ac responses are simulated and shown in Fig. 4.22. It can be seen that there is no ringing in the transient response. For ac response, besides phase margin, the gain margin is another important parameter to access the stability of a system. The simulation results show that the proposed LDO regulator has 34 dB gain margin which ensures the stability. Both the transient and ac responses indicate that the system is still stable under worst case condition



(a)



(b)

Figure 4.22: Simulated worst case result under ss condition at -40°C when I_{LOAD} = 200 µA (a) Transient response, (b) Frequency response

In order to confirm that the proposed LDO regulator is stable against the variation in both the output capacitor and ESR, simulations are conducted. Table 4.5 summaries the variation of UGF and phase margin with respect to the output capacitor and ESR. Furthermore, the UGF and phase margin at full load condition are simulated

while the output capacitor and ESR are varied between ±20%. The worse case occurs when the output capacitor is at the minimum value and the ESR is at the maximum value. The reduction of 1 degree in the phase margin is of no concern to the stability.

TABLE 4.5: VARIATION OF UGF AND PHASE MARGIN WITH DEVIATION OF THE OUTPUT CAPACITOR (4.7µF) AND ESR (0.1 Ω)

C_L	$0.8C_L$			C_L			$1.2C_L$		
R_e	$0.8R_e$	R_e	$1.2R_e$	$0.8R_e$	R_e	$1.2R_e$	$0.8R_e$	R_e	$1.2R_e$
UGF(MHz)	7.7	8.8	9.7	7.7	8.8	9.7	7.7	8.8	9.7
Phase Margin(deg)	62	60.3	59.6	62.5	60.6	59.8	62.8	60.9	60

Fig. 4.23 shows the transient responses of the proposed LDO regulator when the load current changes from 0 to 450 mA and vice versa in 10 ns. Under typical condition, the proposed LDO regulator has displayed an undershoot and an overshoot of 64.6 mV and 31.2 mV, respectively.

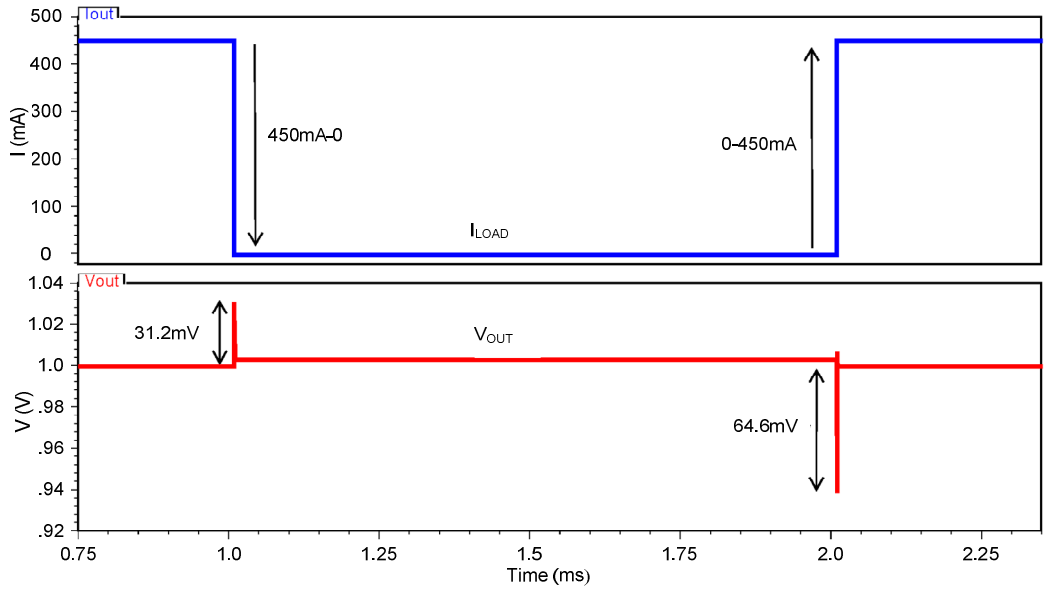


Figure 4.23: Transient response of the proposed LDO regulator with C_L = 4.7µF and R_e = 0.1Ω

It can be shown that the 1% settling time is less than 350 ns. This demonstrates that the proposed embedded gain stage with shunt feedback improves the transient response time of LDO regulator.

To validate the robustness of the proposed LDO regulator, the corner simulations in conjunction with worst case temperatures have been performed. The simulation results are summarized in Table 4.6. This implies that the LDO regulator is stable and able to sustain the operation under extreme process and temperature variations.

TABLE 4.6: SIMULATION RESULTS FOR THE PROPOSED LDO REGULATOR UNDER EXTREME PROCESS AND TEMPERATURE CORNERS

Temperature(°C)	27	-40				85			
Process Corner*	Typ	ss	sf	fs	ff	ss	sf	fs	ff
I_Q(µA)	4.7	2.3	4.1	2.3	4.2	5.2	7.9	5.2	8.0
Overshoot(mV)	31.2	29.9	23.2	28.3	21.4	35.4	32.1	34.8	31.1
Undershoot(mV)	64.6	71.2	64.8	70.3	63.5	65.9	57.9	65.1	57.1
1/PSR (dB@1MHz)	24.9	26.6	26.9	27.4	27.8	21.3	25.4	21.4	26.0
Load Reg. (µV/mA)	7.7	13.1	6.3	13.1	6.0	9.3	6.8	9.2	6.6
Line Reg. (mV/V)	156	168.5	142.8	152.7	136.3	197.7	186.7	258	226

*Typ = Typical; ss = slow NMOS/slow PMOS; sf = slow NMOS/fast PMOS; fs = fast NMOS/slow PMOS; ff = fast NMOS/fast PMOS.

In order to compare the ac and transient performance of the proposed LDO regulator with the conventional LDO regulator, a conventional LDO regulator is designed using the source-follower based buffer structure as the replacement of the embedded gain stage. For a fair comparison, the quiescent current of the buffer is made equal to the maximum biasing current in the embedded gain stage at a given load current. The power transistor size remains the same for both design cases. In the view of the large output swing of the source follower that will drive the output transistors of the error amplifier into triode region at a maximum load current of 450 mA, the load

current is set at 100 mA for both regulators. This ensures that the operation headroom is adequate for the conventional LDO regulator.

The simulated ac loop gain responses are depicted in Fig. 4.24. The simulation results show that the proposed LDO regulator achieves a wider UGF as well as higher loop gain. The simulated phase margin for the proposed LDO regulator and the conventional one at I_{LOAD} = 100 mA is 60 degree and 55 degree respectively.

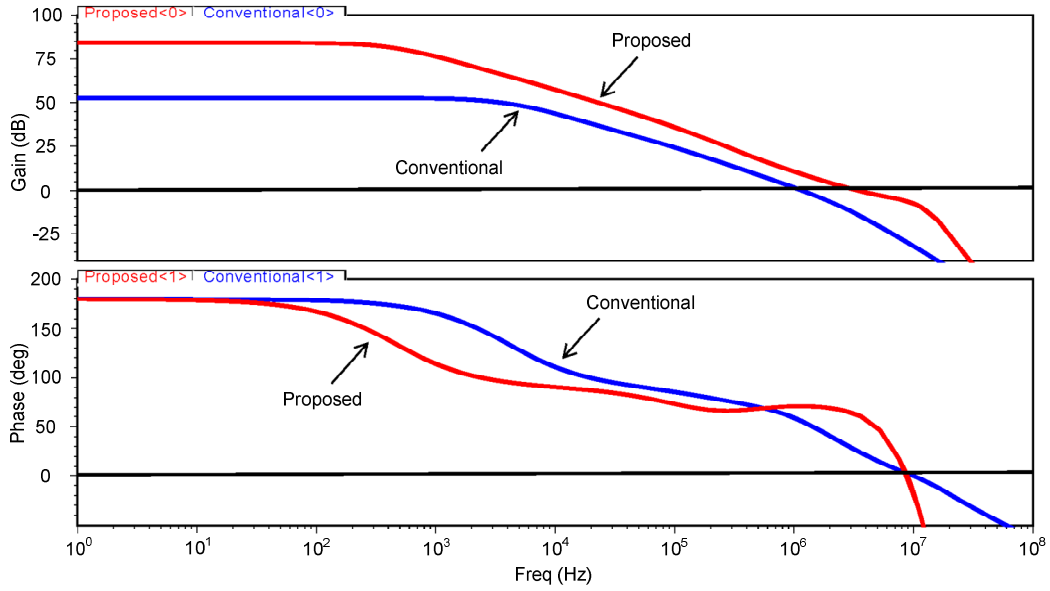


Figure 4.24: Open-loop frequency response of the proposed and conventional LDO regulator

Fig. 4.25 shows the load transient responses of both LDO regulators. The proposed LDO regulator and the conventional one show a load regulation of 2 mV and 4.96 mV respectively for a 100 mA load step. Therefore, the transient response and accuracy of the proposed LDO regulator are improved. This verifies the technical merit of the shunt feedback within the broadband embedded gain stage.

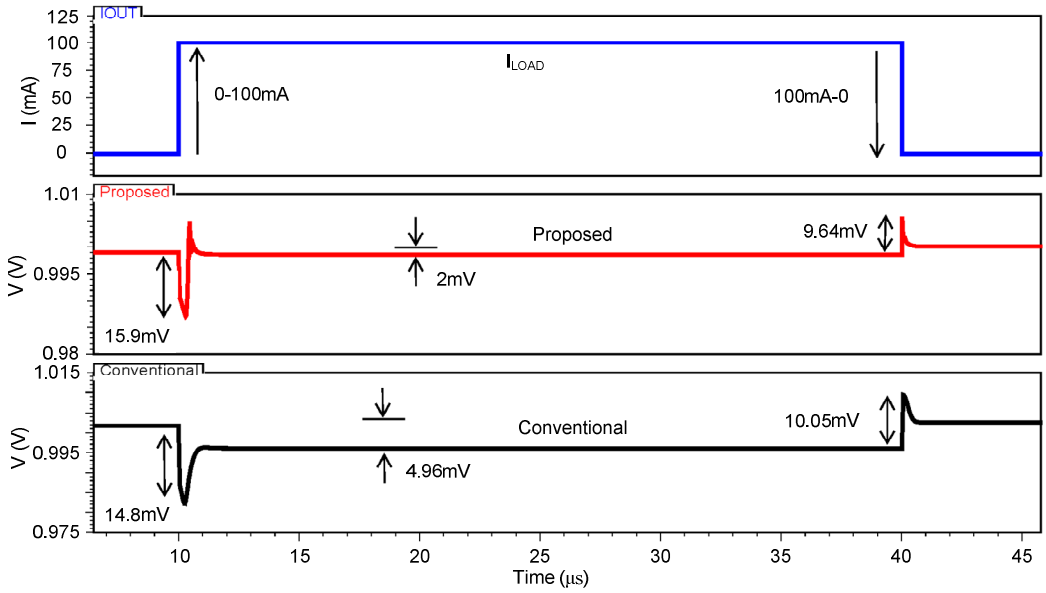


Figure 4.25: Transient response of the proposed and conventional LDO regulator

Table 4.5 shows the performance comparison of the proposed work with respect to the prior-art works. In order to provide a fair comparison, a figure-of-merit (FOM) in [70] is adopted to compare the transient response of different LDO regulators. Since the parameter ΔV_{OUT} in the FOM is greatly affected by the edge time of loading current. For example, ΔV_{OUT} is 64.6 mV and 19.9 mV for edge time of 10ns and 1µs respectively in this design. Therefore, the edge time introduced in [41] is needed in the FOM dedicated to evaluate the OC-LDO regulators. Based on two definitions in [70] and [41], a new FOM_1 for comparison of different OC-LDO regulators is proposed as follows:

$$FOM_1 = K \times \left(\frac{C_L \Delta V_{out} I_{Q,\min}}{I_{LOAD,\max}^{\ 2}} \right) \tag{4.29}$$

where K is the edge time ratio and defined by K = Δt used in the measurement/the smallest Δt among the comparison design.

Since the edge time used in [71] is the smallest value, it becomes the reference for the other designs and has a K factor normalized to 1. The smaller the FOM_1, the better the transient response the LDO regulator achieves. From Table 4.5, the proposed LDO regulator achieves the smallest FOM_1 when compared to other reported LDO regulators, suggesting that the proposed LDO regulator has a better transient response than that of the prior-art works.

In order to quantify the quiescent current efficiency for yielding the maximum output current driving capability in LDO regulator design, another new figure-of-merit [67] is defined as

$$FOM_2 = \frac{I_{LOAD,\max}}{I_{Q,\min}} \tag{4.30}$$

The larger the FOM_2, the better the efficiency for the dynamic ratio between the maximum output current and the minimum quiescent current that the LDO regulator achieves. It implies that the LDO regulator is able to provide a higher loading current for a low quiescent current. From Table 4.7, it can be seen that the proposed LDO regulator has the highest FOM_2 among all the prior-art works.

TABLE 4.7: PERFORMANCE COMPARISON OF REPORTED PRIOR-ART RESULTS

Parameter	[9]	[26]	[61]	[71]	[72]	[73]	[27]	[74]	[75]	This work*
Year	1998	2001	2007	2008	2008	2009	2010	2010	2010	2010
CMOS Process (µm)	2.0	0.6	0.35	0.35	0.35	0.18	0.35	0.18	0.09	0.18
$I_{LOAD(max)}$ (mA)	50	250	200	50	400	50	100	150	50	450
V_{DO} (mV)	200	200	200	150	300	40	200	541	100	200
V_{OUT} (V)	1	3.4	1.8	0.9	3.3	1.5	1.8	1.5	0.9	1
Total Cap On-chip (pF)	N.A.	N.A.	10	N.A.	N.A.	N.A.	N.A.	10	N.A.	1.15
C_L (µF)	4.7	1	1	1	1	0.033	1	1	1	4.7
I_Q (µA)	23–230	60-170	20–340	4.04–164	100	69.1	4	8.5-35	9.3	4.7–84.91
Edge time Δt (µs)	N.A.	N.A.	0.1	0.01	5	0.1	0.05	N.A.	0.01	0.01
ΔV_{OUT} (mV)	19	320†	54	6.6	6.5	250	55	196	8	64.62
1/PSR (dB)	N.A.	N.A.	45 @20kHz	50 @1MHz	33 @100kHz	46 @1kHz	32 @1MHz	64.3 @1kHz	54 @100kHz	57 @20kHz 45 @100kHz 24.9@1MHz
Load Reg. (µV/mA)	380	10	170	61.4	0.153	760	100	101	8.2	7.73
Line Reg. (mV/V)	1.05	1.5	2	1.061	0.4	2.3	17	2.77	14	0.156
Current Efficiency@ I_{max} (%)	99.54	99.915††	99.83	99.672	99.975	99.862	99.996	99.977	99.981	99.981
Current Efficiency@ 1 mA (%)	N.A.	N.A.	N.A.	N.A.	90	93.537	99.602	N.A.	99.079	99.264
FOM_1	N.A.	N.A.	0.27	0.0106	2.05	2.28	0.11	N.A.	0.0298	0.007
FOM_2	2,174	4,167	10,000	12,500	4,000	723.6	25,000	17,647	5376.3	95,744
Edge time ratio, K	N.A.	N.A.	10	1	500	10	5	N.A.	1	1

*Simulated results.

† Transient response from 0 to 50 mA †† I_{load} = 200mA.

4.5 SUMMARY

In this chapter, two new composite power transistors are presented. Firstly, a push-pull composite power transistor is applied to an area-efficient OCL-LDO regulator in 65-nm CMOS technology. The low-voltage circuit architecture permits the regulator to operate at sub-1V supply. The proposed push-pull structure improves the load transient response. Both undershoot and overshoot are improved greatly when compared with the counterparts. Finally, with the proposed composite power transistor, the non-dominant poles are located at higher frequencies. Thus, the compensation capacitor can be made small. In view of silicon area, the smaller compensation capacitor leads to a small-area LDO regulator.

Secondary, an ultra-low quiescent, high-drive and fast-transient LDO regulator, which makes use of a dynamic-biased composite power transistor, is presented. Due to the multi-gain stages reduced to the pseudo two-stage LDO regulator using the composite power transistor, this permits the ease of frequency compensation which leads to low quiescent current for stability. Compared to the prior-art works, the proposed high- drive LDO regulator can be stabilized using ultra-low quiescent current at no load whilst delivering very high load currents at full load for a small dropout voltage. The transient response and other dynamic performance parameters are also significantly improved. The simulation results have validated the effectiveness of the LDO regulator. The robustness and reliability of the proposed architecture is confirmed by the simulations using worst case process corners at extreme temperature points, worst case load current and variations of output capacitor and ESR.

CHAPTER 5

AN ULTRA-LOW QUIESCENT CURRENT OUTPUT-CAPACITORLESS LDO REGULATOR

5.1 INTRODUCTION

This chapter presents an ultra-low quiescent current OCL-LDO regulator using an adaptive power transistors architecture and technique in 65 nm CMOS process [76]. The proposed architecture and technique allows the regulator to transform itself from a 2-stage structure to a 3-stage structure OCL-LDO regulator when a larger load current is drawn from the output. In addition, it also offers an ultra-low quiescent current solution for OCL-LDO regulator at no load condition whilst achieving stability across the whole load current range.

5.2 PROPOSED ARCHITECTURE

5.2.1 STRUCTURE

The architecture of the proposed regulator is depicted in Fig. 5.1. It is formed by a dynamic-biased error amplifier as first gain stage, a non-inverting second gain stage, a smaller sub-power transistor M_{P1}, a main power transistor M_{P2} that can be adaptively turned on/off (depending on the output load current condition), an

overshoot reduction circuitry, a feedback network and a frequency compensation network.

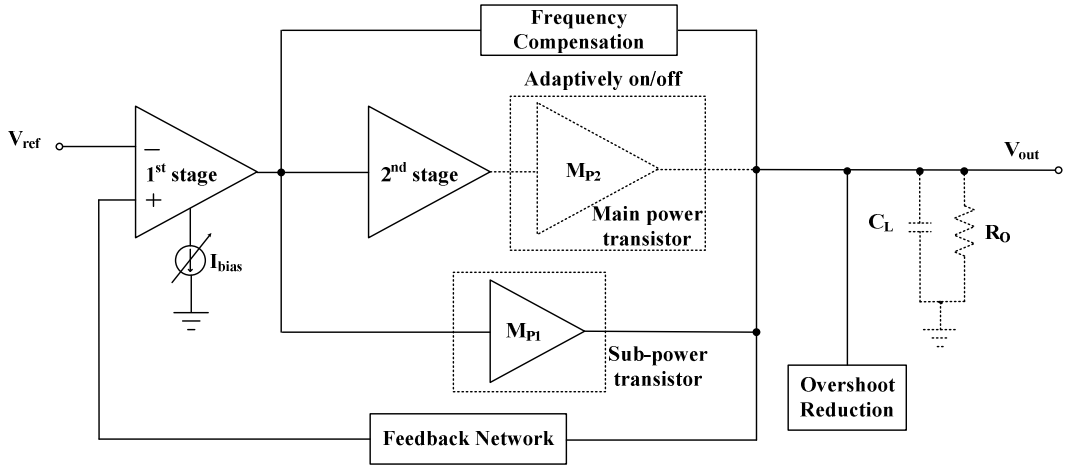


Figure 5.1: Structure of proposed OCL-LDO regulator

At low load condition, the second gain stage is driven into triode region. As a result, the main power transistor is fully turned off. Due to the fact that both second gain stage and main power transistor are off when the load current is lower than the defined threshold current I_{ON}, the proposed regulator is effectively a 2-stage structure. Besides, in order to achieve ultra-low power and current consumption and improve the efficiency at low loads, the biasing current (I_{bias}) of the error amplifier is added with the dynamic biasing technique in [71]. In this design, dynamic biasing is achieved by increasing the I_{bias} proportional to the current flows in the sub-power transistor M_{P1}. It should be noted that I_{bias} stops increasing after the second gain stage and main power transistor M_{P2} are activated.

On the other hand, the proposed regulator transforms itself into a 3-stage structure at the point where the load current increases above I_{ON}. Due to the reduced effective output impedance and higher transconductance arising from the load current, the

pole associated at the output of regulator is moved to higher frequencies. As such, the proposed regulator remains stable with the transformation into 3-stage structure. Moreover, the requirement of the minimum loading current problem in most of the OCL-LDO regulators with multistage structure is eliminated. This leads to the proposed structure that can achieve ultra-low quiescent and stability simultaneously.

5.2.2 STABILITY ANALYSIS

The stability of the whole system relies on cascode compensation technique. Similar to the LDO regulator proposed in section 4.4, the main reason to adopt cascode compensation is its higher current-bandwidth efficiency when compared to the Miller compensation technique [19]. Turning to other merits, both stability and PSR are improved when cascode compensation is adopted [19],[77, 78].

The stability of the proposed OCL-LDO regulator is studied through its small-signal transfer function. Due to the architectural transformation, the stability of the proposed OCL-LDO regulator is discussed on the basis of 2-stage and 3-stage structure as shown in Fig. 5.2. As usual, g_{mi} denotes the transconductance of the respective device. The lumped output resistance and output parasitic capacitance of each node are denoted by R_i and C_i, respectively. In this OCL-LDO regulator design, the feedback factor β is ½. The small-signal transfer function is derived using the following assumptions:

(i) The input impedance of the transconductance stage, g_{mc}, is equal to the reciprocal of its transconductance.

(ii) The gain of first stage and second stage are much larger than 1

(iii) The parasitic capacitors C_1, C_2, C_3 and C_C are much smaller than C_L.

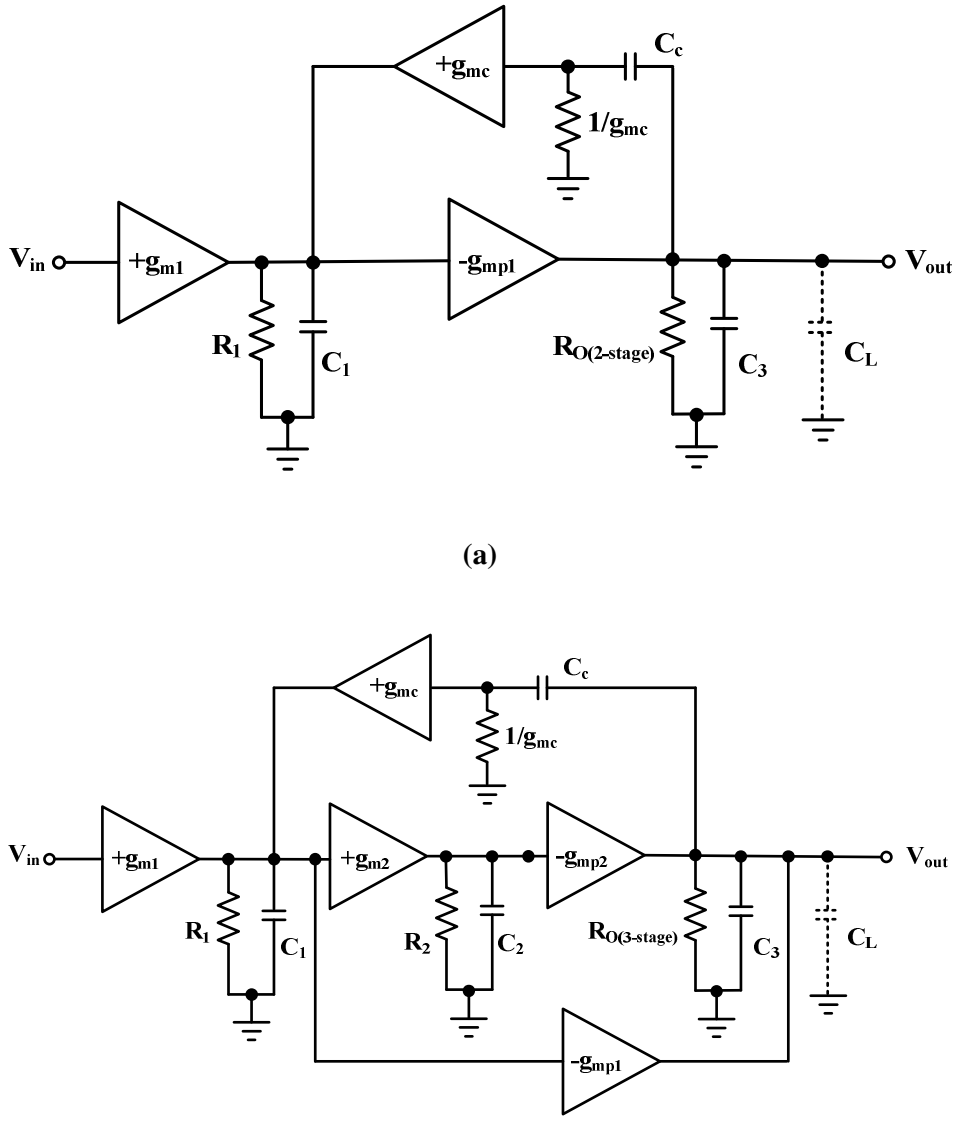


Figure 5.2: Small-signal model of the proposed OCL-LDO regulator. (a) 2-stage and (b) 3-stage structure

5.2.2.1 CASE I ($I_{LOAD} < I_{ON}$ → 2-STAGE STRUCTURE)

When $I_{LOAD} < I_{ON}$, the output transistor of second gain stage is designed to operate in triode region whereas the main power transistor is totally off. They will not affect the stability. Therefore, they are ignored in the analysis. The small-signal model of

the proposed OCL-LDO regulator becomes the 2-stage structure as shown in Fig. 5.2(a). The effective output impedance of the 2-stage structure is defined by $R_{O(2\text{-}stage)} = r_{oMp1}//R_{FB}//R_{LOAD}$, where R_{LOAD}, R_{FB} and r_{oMp1} are load resistance, feedback network resistance and output impedance of sub-power transistor, respectively. In general, when the load current is small, $R_{O(2\text{-}stage)}$ is large. The transfer function derived from Fig. 5.2(a) is shown as follows:

$$A_{V(I_{LOAD}<I_{ON})} = \frac{-\beta \times A_{dc}\left(1+s\frac{C_C}{g_{mc}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{C_L C_1}{C_C g_{mp1}}+s^2\frac{C_L C_1}{g_{mc} g_{mp1}}\right)} \tag{5.1}$$

where A_{dc} is the DC gain and p_{-3dB} is dominant pole. Both of them are given as

$$A_{dc} = g_{m1} g_{mp1} R_1 R_{O(2-stage)} \tag{5.2}$$

$$p_{-3dB} = -\frac{1}{C_C g_{mp1} R_1 R_{O(2-stage)}} \tag{5.3}$$

Hence, the GBW can be obtained as

$$GBW = \frac{g_{m1}}{C_C} \tag{5.4}$$

In (5.1), the zero and non-dominant poles can be obtained by

$$p_2 = -\frac{C_C g_{mp1}}{C_1 C_L} \tag{5.5}$$

$$p_3 = -\frac{g_{mc}}{C_C} \tag{5.6}$$

$$z_1 = -\frac{g_{mc}}{C_C} \tag{5.7}$$

The relative position of zero and poles are shown in Fig. 5.3. It can be seen that z_1 and p_3 cancel to each other. The dominant pole located at the output of error amplifier is the only pole that falls within the unity-gain bandwidth. This turns out that the location of p_2 is the only factor to determine the loop stability. As can be observed from (5.5), p_2 is shifted to higher frequencies by cascode factor of C_C/C_1. The non-dominant pole p_2 is directly proportional to g_{mp1}, which is also proportional to the square-root of I_{LOAD}. When the load current increases, the non-dominant pole p_2 is moved to higher frequencies. As a result, the phase margin is improved. Therefore, the worst case stability happens at no load condition.

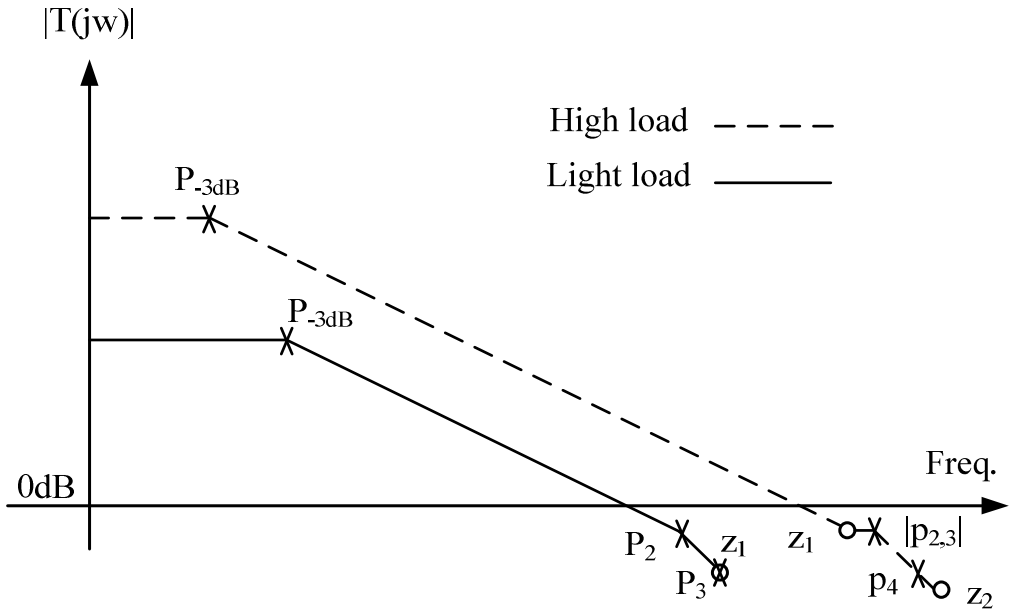


Figure 5.3: Loop gain (magnitude plot not in scale) of the proposed LDO regulator

5.2.2.2 CASE II ($I_{LOAD} > I_{ON}$ → 3-STAGE STRUCTURE)

When $I_{LOAD} > I_{ON}$, both the second gain stage and the main power transistor are turned on. Fig. 5.2(b) shows the small-signal model of the proposed OCL-LDO regulator in the 3-stage structure. The second gain stage and main power transistor need to be included in the stability analysis since they are activated. The overall structure can be treated as a 3-stage amplifier with cascode compensation. The effective output impedance for 3-stage structure is defined by $R_{O(3\text{-stage})} = r_{oMp1}//r_{oMp2}//R_{FB}//R_{LOAD}$, where R_{LOAD}, R_{FB}, r_{oMp1} and r_{oMp2} are the load resistance, feedback network resistance, output impedance of sub-power transistor and main power transistor, respectively. The effective output impedance is greatly affected by load current ($\propto 1/I_{LOAD}$) and dominated by the load resistance, R_{LOAD}. Hence, $R_{O(3\text{-stage})}$ is small. The derived transfer function of the 3-stage structure is given by

$$A_{V(I_{LOAD}>I_{ON})} = \frac{-\beta \times A_{dc}\left(1+s\frac{C_C}{g_{mc}}\right)\left(1+s\frac{C_2 g_{mp1}}{g_{m2}g_{mp2}}\right)}{\left(1+\frac{s}{p_{-3dB}}\right)\left(1+s\frac{g_{mp1}C_2}{g_{m2}g_{mp2}}+s^2\frac{C_1C_2}{g_{m2}g_{mp2}g_{mc}R_{O(3-stage)}}\right)\left(1+sC_LR_{O(3-stage)}\right)} \quad (5.8)$$

The DC gain A_{dc} and dominant pole p_{-3dB} are obtained as follows:

$$A_{dc} = g_{m1}g_{m2}g_{mp2}R_1R_2R_{O(3-stage)} \quad (5.9)$$

$$p_{-3dB} = -\frac{1}{C_C g_{m2}g_{mp2}R_1R_2R_{O(3-stage)}} \quad (5.10)$$

It is obvious that the GBW remains unchanged. However, the GBW is extended when compared to the 2-stage configuration (Fig. 5.4). It is because g_{m1} is increased

by the dynamic biasing scheme. From the derived transfer function in (5.8), the non-dominant complex poles and its corresponding Q factor are determined as

$$\left|p_{2,3}\right| = \sqrt{\frac{g_{m2}g_{mp2}g_{mc}R_{O(3-stage)}}{C_1C_2}} \tag{5.11}$$

$$Q = \sqrt{\frac{g_{m2}g_{mp2}C_1}{g_{mp1}^{\ 2}g_{mc}C_2R_{O(3-stage)}}} \tag{5.12}$$

It can be seen from (5.11) and (5.12) that both $|p_{2,3}|$ and Q factor are dependent on parameters g_{m2}, g_{mc} and $R_{O(3\text{-stage})}$ which control the stability of the proposed regulator. $|p_{2,3}|$ can be placed at high frequencies easily as they are parasitic (C_1 and C_2) related poles . It can be observed from (5.12) that the Q factor is proportional to the square-root of $g_{mp2}/R_{O(3\text{-stage})}$. The largest Q factor happens at maximum I_{LOAD} where the g_{mp2} and $R_{O(3\text{-stage})}$ is the maximum and minimum, respectively. To prevent "peaking effect" due to high Q factor, a smaller g_{m2} or a larger g_{mc} and g_{mp1} can be used. In general, a larger g_{mc} is chosen because it moves the non-dominant complex pole $|p_{2,3}|$ to a higher frequencies as well.

The location of fourth pole is obtained as

$$p_4 = -\frac{1}{C_LR_{O(3-stage)}} \tag{5.13}$$

As shown in (5.13), the p_4 depends on the output impedance and output capacitance. The effective output impedance is inversely proportional to the output load current that will shift the p_4 to higher frequencies when the load current increases. On the other hand, from the transfer function (5.8), there are two zeros in the system. They can be given as follows:

$$z_1 = -\frac{g_{mc}}{C_C} \tag{5.14}$$

$$z_2 = -\frac{g_{m2}g_{mp2}}{C_2 g_{mp1}} \tag{5.15}$$

Fig. 5.3 illustrates the relative poles and zeros position when $I_{LOAD} > I_{ON}$. The zero z_1 is located slightly higher than the GBW to improve the phase margin. This can be achieved by designing transconductance g_{mc} to be slightly larger than transconductance g_{m1}. The zero z_2 appears at the frequency which is even much higher than that of the p_4. As such, the effect due to z_2 can be neglected. The poles and zeros locations with C_L = 100 pF in the 2-stage and 3-stage structure are summarized in Table 5.1.

TABLE 5.1: POLES AND ZEROS LOCATION WITH C_L = 100 PF

Configuration	Parameter	Range
2-stage	p_{-3dB}	0.3kHz ~ 2kHz
	p_2	250kHz ~ 14MHz
	p_3 & z_1	320kHz ~ 5.6MHz
3-stage	p_{-3dB}	100Hz ~ 300Hz
	$p_{2,3}$	40MHz ~ 57MHz
	p_4	1.6MHz ~159MHz
	z_1	5.6MHz ~ 10MHz
	z_2	6.5MHz ~ 663MHz

The simulated open-loop gain response of the regulator at different load current conditions with C_L = 100 pF are depicted in Fig. 5.4. The regulator is having a minimum phase margin of 53° with a DC open-loop gain of 40 dB at no load current condition. The open-loop gain increases to around 100 dB as the load current increases. When I_{LOAD} > 1mA, due to the dynamically increase in the bias currents,

the regulator obtains a gain bandwidth product GBW of about 9 MHz with a phase margin of 80°.

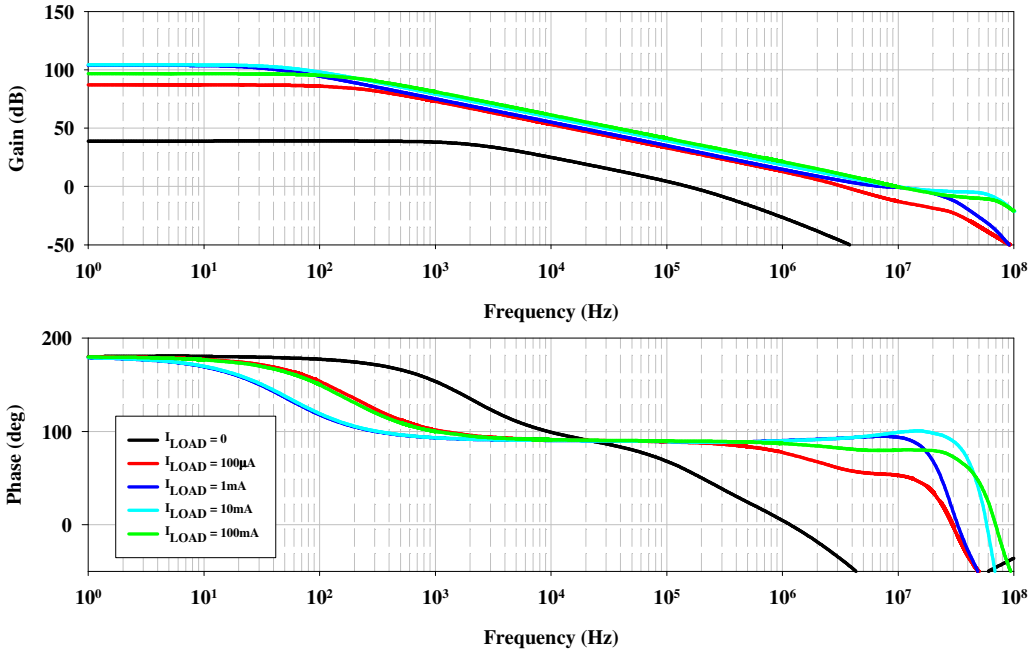


Figure 5.4: Simulated open-loop gain at different load currents with C_L = 100 pF

The simulated phase margin as a function of output load currents are illustrated in Fig. 5.5. Similar to previous reported works [41], [2], as expected, the regulator has a minimum phase margin when C_L is at its maximum while I_{LOAD} is at its minimum. From Fig. 5.5, it can be seen that the phase margin is above 50° for all cases. Therefore, it can be concluded that the regulator remains stable over the full range of load current given that C_L is less than 100 pF.

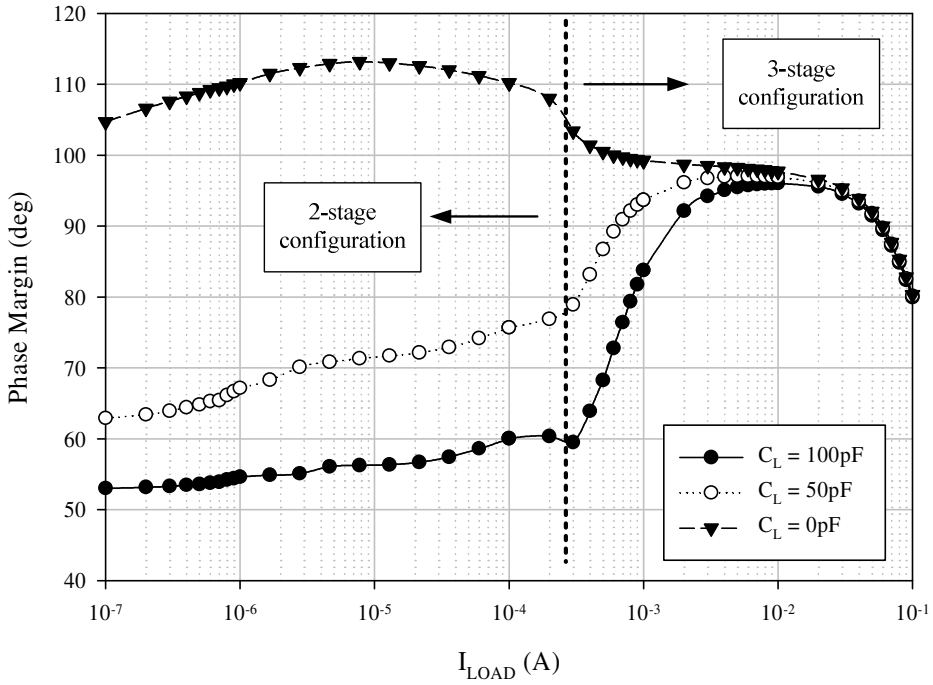


Figure 5.5: Phase margin as a function of load currents

5.3 CIRCUIT IMPLEMENTATION OF PROPOSED LDO REGULATOR

5.3.1 SCHEMATIC

The simplified schematic of the OCL-LDO regulator with adaptive power transistors is shown in Fig. 5.6. The error amplifier (first gain stage) is realized by a folded-cascode stage with transistor M_0-M_8. The transistors, M_{a1}-M_{a7}, form the dynamic biasing network to enhance the bandwidth of the proposed regulator under moderate loading conditions. The non-inverting second gain stage is formed by the transistors M_9-M_{12}. The transistors M_{P2} and M_{P1} are main power and sub-power transistor, respectively. The aspect ratio of M_{P2} and M_{P1} is 1800 μm/60 nm and 120 μm/60 nm, respectively. Similar to section 4.4.1, the feedback network is realized by a string of

diode-connected PMOS transistors M_{15}-M_{18} biased in the subthreshold region to minimize the silicon area as well as the quiescent power [79]. The required silicon area by the passive resistors will be much larger if the feedback network is realized, especially in ultra-low power design. Finally, the load of the regulator is modeled by a parasitic load capacitor C_L and a resistor R_{LOAD} in parallel. The quiescent current distribution at no load condition is indicated in Fig. 5.6. When I_{LOAD} = 0, the dynamic current sources are negligible because they are insignificant when compared to the static current source. The designed total quiescent current is approximately 500 nA for the core circuit.

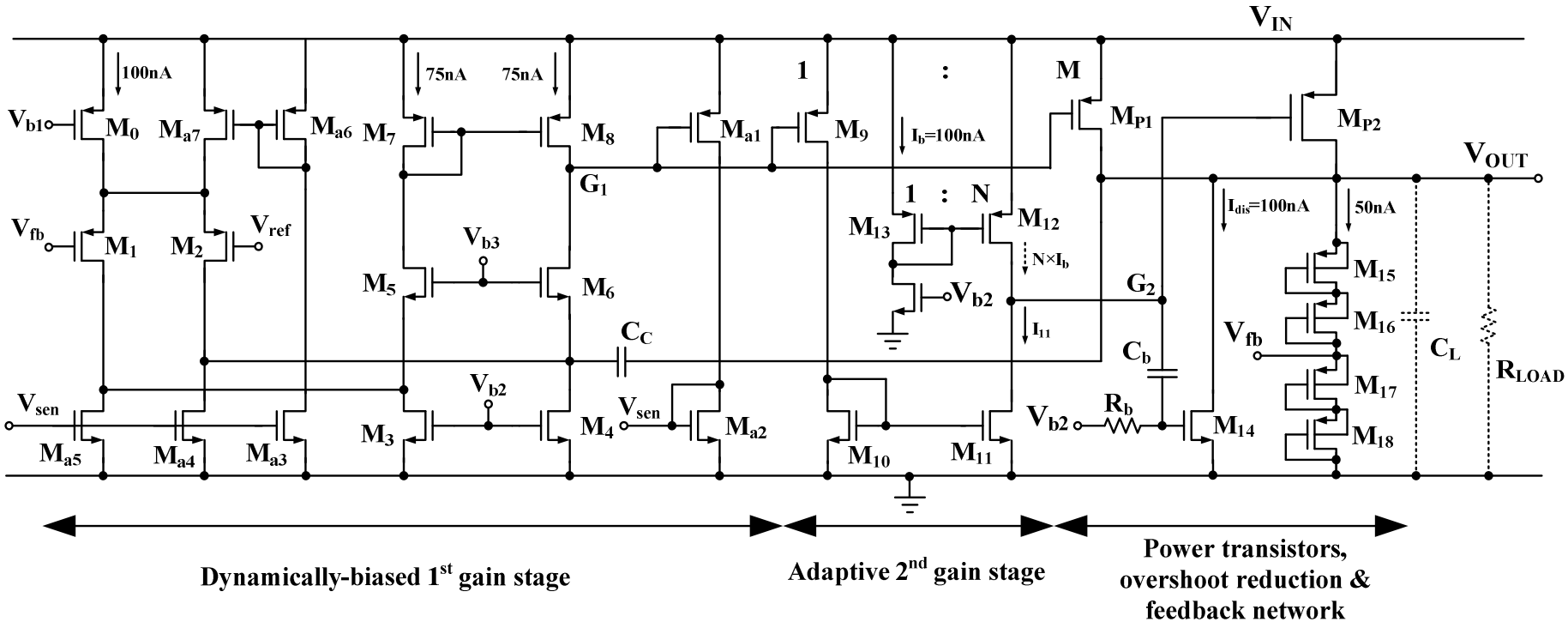


Figure 5.6: Schematic of the proposed LDO regulator

Fig. 5.7 shows the bias current generator and start-up circuit for the proposed design. A supply-independent current generator realized by the resistor R_{b1} and the transistors M_{b3}-M_{b6} is designed to provide biasing currents to the core circuit. A start-up circuit with capacitive-coupling [80] is adopted as it basically dissipates no static power. However, the drawback is that the start-up capacitors occupy extra silicon area. As shown in Fig. 5.7, the bias current generator dissipates only 300 nA.

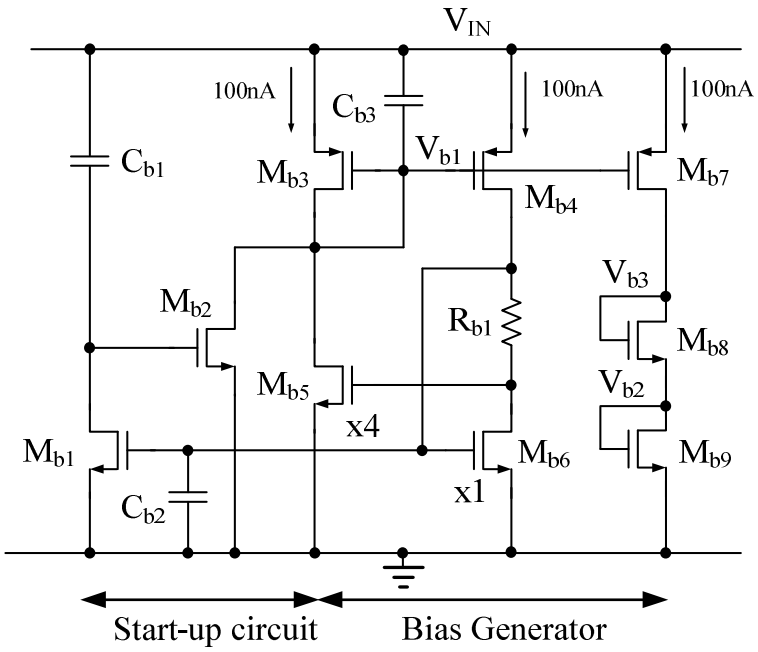


Figure 5.7: Schematic of bias generator and start-up circuit

When the system operates in the 2-stage mode, all the load current is supplied by the sub-power transistor M_{P1}. The transistor M_{a1} in the dynamic biasing network is used to copy a portion of the load current from the transistor M_{P1} [71], since they share the same gate-source voltage. A gate-source voltage (V_{sen}) which changes according to the load current is developed. As a result, the biasing current of the first gain stage will be increased proportionally. It should be noted that the biasing current of the first gain stage stops increasing when the system transforms into the 3-stage mode. It

is because the excess load current is now supplied by the main power transistor M_{P2}. Therefore, the amount of current flowing through the sub-power transistor M_{P1} is approximately fixed.

Both the second gain stage transistor M_9 and sub-power transistor M_{P1} are driven by the output of the dynamic-biased first gain stage at voltage node G_1. Hence, they can be treated as a pair of current mirrors that having a current ratio of 1: M. When the load current is low, the current $I_{11} = I_{LOAD}/M$. The transistor M_{12} is designed to source a current of $N \times I_b$. When $I_{11} < N \times I_b$, the transistor M_{12} is forced to work in the triode region. As such, the node potential at G_2 will be pulled up close to V_{IN} potential and the main power transistor M_{P2} is turned off. Despite of the parasitic capacitances arising from the gate of M_{P2}, the pole associated at node G_2 is located at high frequency. This ensures stable operation.

When the load current increases gradually at the transition bias point where $I_{11} = I_{LOAD}/M = N \times I_b$, the transistor M_{12} moves from the triode region to the saturation region. At this moment, the proposed OCL-LDO regulator transforms itself into the 3-stage structure. The second gain stage is activated and the main power transistor starts to conduct and supply the additional required load current. Due to extra gain stage, the amount of loop gain increases considerably. It should be noted that the switching between two modes is not a “hard-switch” but a “soft-switch” in continuous-time operation. The main power transistor M_{p2} is not turned on instantly at load current of 200 µA. The reason is that the operation of transistor M_{12} cannot switch from triode to saturation region immediately. The main power transistor M_{P2} starts to conduct some current before 200 µA and the transition between two modes is achieved automatically and continuously.

The threshold current ($I_{ON} = M \times N \times I_b$) can be defined by the design parameters M, N

and I_b. The value of N, I_b and M and are 125, 100 nA and 67, respectively. The calculated I_{ON} based on the design parameters is about 837.5 μA. However, the simulated value of I_{ON} is around 200 μA. After investigation, the difference is due to the combined effect of channel length modulation and reverse short-channel effect (RSCE) [81, 82]. In this proposed design, the channel length of the transistor M_9 and M_{P1} is 500 nm and 60 nm (60 nm is allowed by the foundry and stated in the design rule), respectively. The extracted threshold voltage of transistor M_9 is 78 mV smaller than the sub-power transistor M_{P1}. Therefore, for a given gate-source voltage, the normalized current driving capability of sub-power transistor M_{P1} is smaller than that of the transistor M_9. Despite of that, the early activation of the main power transistor M_{P2} would not affect the operation and stability of the proposed scheme. To confirm the stability of the regulator, corner and temperature simulations have been conducted.

5.3.2 OVERSHOOT AND UNDERSHOOT REDUCTION

In general, when compared to the LDO regulator with a large off-chip output capacitor, the OCL-LDO regulator will be having a larger undershoot/overshoot. In this proposed design, the undershoot is minimized by applying the dynamic biasing scheme [83]. It has demonstrated that dynamic biasing technique obtains a smaller undershoot when compared to LDO regulator with fixed biasing current. It is mainly because the bandwidth of the LDO regulator is broader and the total current that can be used to discharge the gate capacitance of the power transistors is larger. In fact, the overshoot is reduced by the dynamic biasing technique too. However, when I_{LOAD} is switched from full load to no load, the subthreshold PMOS diode-connected

feedback network is the only path to discharge the extra charges at the output. As a result, the overshoot appears at the output needs longer time to recover during transient event. In order to suppress the overshoot, an overshoot reduction network, which consists of a transistor M_{14}, a resistor R_b and a capacitor C_b, is proposed. C_b is a 3 pF MOS capacitor that is realized by a high-voltage native device to prevent leakage current and save silicon area whereas R_b is a very large pseudo-resistor realized by a PMOS transistor working in the cut-off region. This proposed overshoot reduction network is similar to the RC coupling circuits used in [27]. Instead of the typical design that the overshoot reduction network senses the load voltage spikes from the output of regulator, the proposed scheme senses the voltage spikes from the gate of power transistor. It is because the voltage swing at the gate of power transistor is large when the load current is switched from full load to no load. The concept is similar to the pseudo class-AB amplifier design in [68]. As shown in Fig. 5.6, the steady state current I_{dis} is around 100 nA. When the I_{LOAD} is changed from full load to no load, the capacitor C_b couples the transient signal to the gate of M_{14}. The discharging current I_{dis} is increased momentarily. As a result, the magnitude of the overshoot is suppressed and the transient response is enhanced. The simulated transient responses of the proposed LDO regulator with and without overshoot reduction network are illustrated in Fig. 5.8. The overshoot is reduced significantly from 93 mV to a very small value. Since g_{mp2} is much larger than g_{m14}, the overall small-signal frequency response is unaffected by the proposed overshoot reduction network.

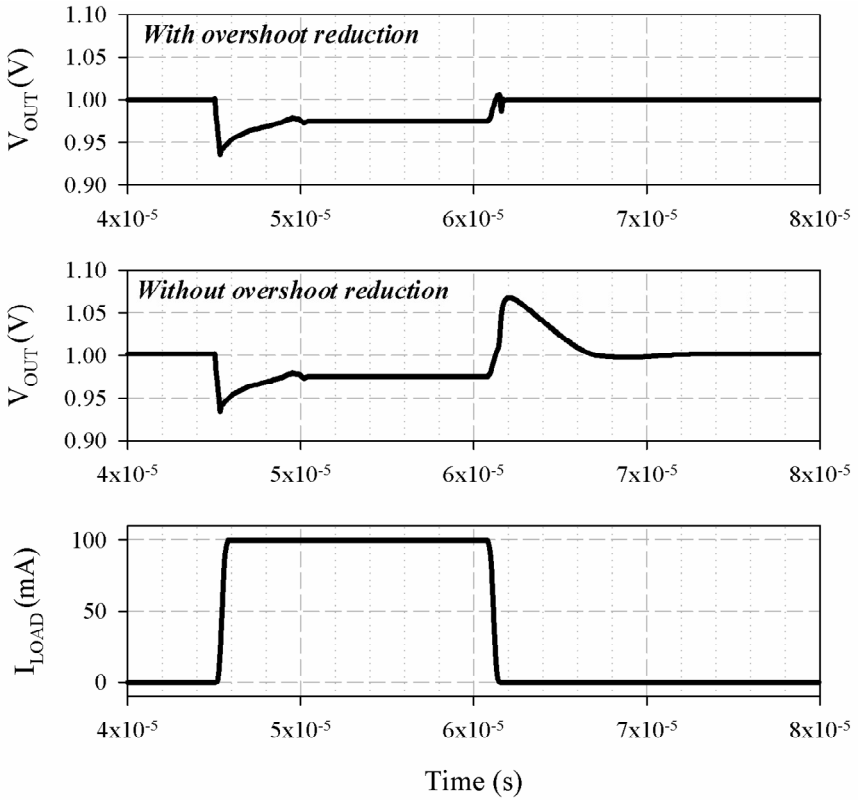


Figure 5.8: Simulated load transient responses

5.4 EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed OCL-LDO regulator is implemented and fabricated in UMC 65-nm low-leakage CMOS technology. Fig. 5.9 shows the microphotograph and layout of the proposed regulator which occupies an active area of about 0.017 mm^2 (including the start-up circuit and bias generator).

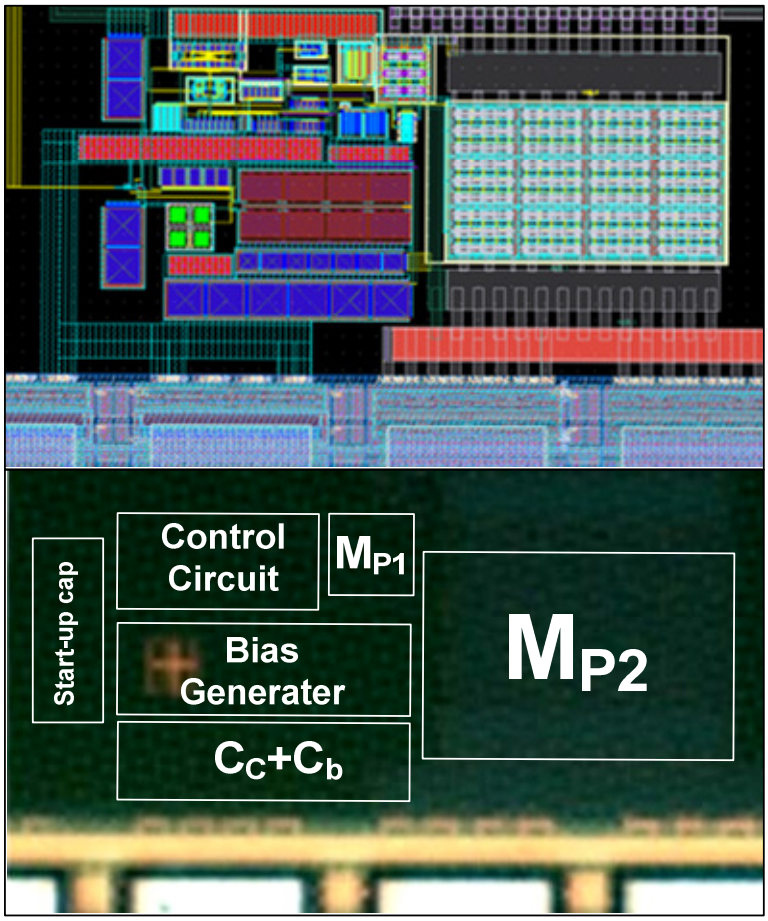
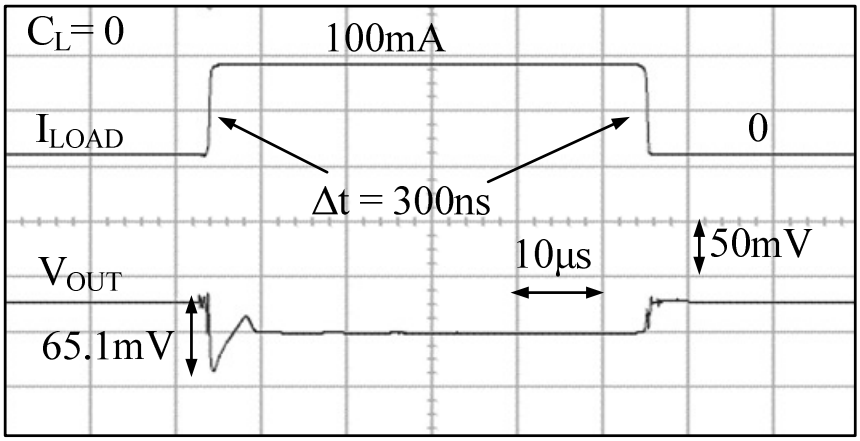


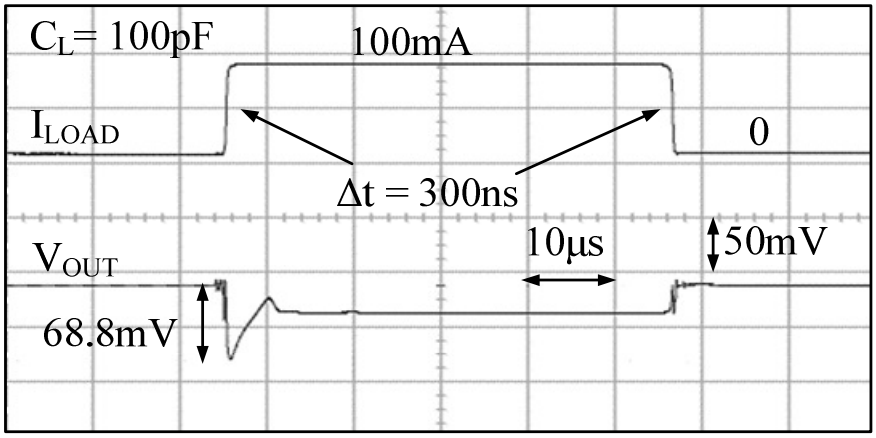
Figure 5.9: Layout and chip microphotograph

It is able to provide an output voltage of 1 V and supply I_{LOAD} from 0 to 100 mA at a supply voltage of 1.2 V. The measured quiescent current of the proposed regulator including the biasing circuit is only 900 nA. This is slightly larger than the designed value of 800 nA at I_{LOAD} = 0. At maximum load current condition, the measured dropout voltage is less than 200 mV. It is compensated by a small cascode capacitor C_C of 1.5 pF throughout the whole load current range. An off-chip ceramic capacitor of 100 pF is added to model the load capacitor and an external voltage reference of 500 mV is used for measurement purpose. Both (5.5) and (5.13) suggest that, with a smaller C_L, the non-dominant pole is moved to higher frequencies. Therefore, it can be concluded that the system remains stable as long as the C_L is less than 100 pF.

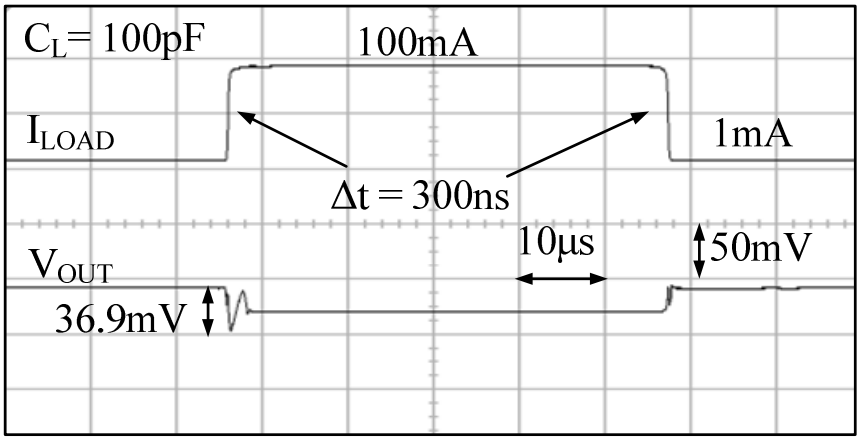
Fig. 5.10(a)-(d) show the measured load transient responses under different loading conditions. The measured results confirm the stability of the proposed LDO regulator. When conducting the load transient measurement, the V_{IN} and V_{OUT} are set to 1.2 V and 1 V, respectively.



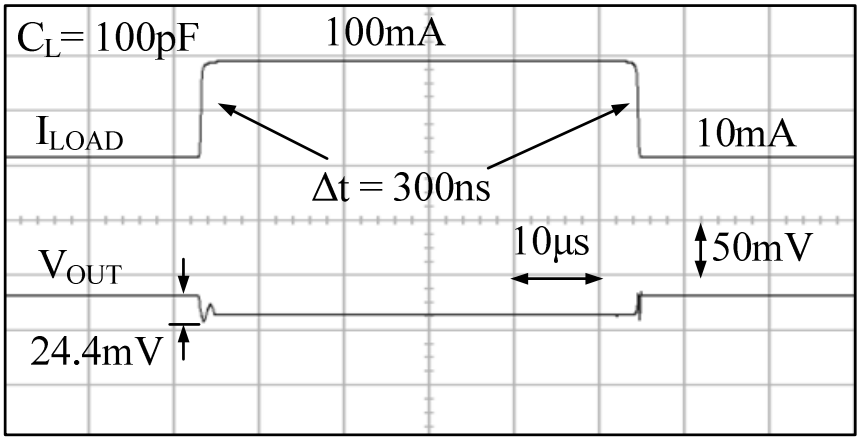
(a)



(b)



(c)



(d)

Figure 5.10: Measured load transient response with V_{IN} = 1.2 V and V_{OUT} = 1 V (a) C_L = 0, I_{LOAD} = 0 ↔100 mA (b) C_L = 100 pF, I_{LOAD} = 0 ↔100 mA, (c) C_L = 100 pF, I_{LOAD} = 1 mA ↔100 mA (d) C_L = 100 pF, I_{LOAD} = 10 mA ↔100 mA

In Fig. 5.10 (a) and (b), the output load current is changed between 0 and 100 mA with a slew rate of 100 mA/300 ns for C_L = 0 and 100 pF, respectively. There is no obvious overshoot when output load current is changed from 100 mA to 0. It is because of the employment of overshoot reduction network and the higher GBW contributed by the dynamic biasing scheme. On the other hand, the LDO regulator displays an undershoot of 65.1 mV and 68.8 mV for C_L = 0 and 100 pF, respectively. The undershoot is due to the relatively low quiescent current of 900 nA

at zero load current condition. Nevertheless, it is able to recover to its final value in 6 µs and the maximum magnitude of the output voltage variation is less than 7% (68.8 mV/1 V). Fig. 5.10 (c) and (d) show the measured load transient responses when the load current is changed from 1 mA and 10 mA to 100 mA, respectively. Similarly, an edge of 300 ns is used. It can be shown that the magnitude of the measured undershoot is reduced to 36.9 mV and 24.4 mV, respectively. It is due to the fact that the main power transistor has been turned on and the first gain stage has larger biasing current. These measured load transient responses have validated that the proposed regulator remains stable for whole range of load current as long as C_L is less than 100 pF.

The measured load regulation of the proposed work is depicted in Fig. 5.11. Similar to the IR drops described in section 4.3.1.2, the voltage drops at moderate and high load condition could be due to the parasitic resistance arising from the bonding wire which is around 250 mΩ (parallel of 2 bonding pads, each is around 500 mΩ) from the MediaTek QFN40 packaging. When I_{LOAD} = 100 mA, the IR drops across the parasitic bonding wire can be as large as 25 mV. In order to estimate the actual load regulation, the IR drop due to the parasitic bonding resistance is excluded and plotted in Fig. 5.11 for comparison purpose. The IR drops at high load current can be minimized by using multiple bonding or Kelvin connection method.

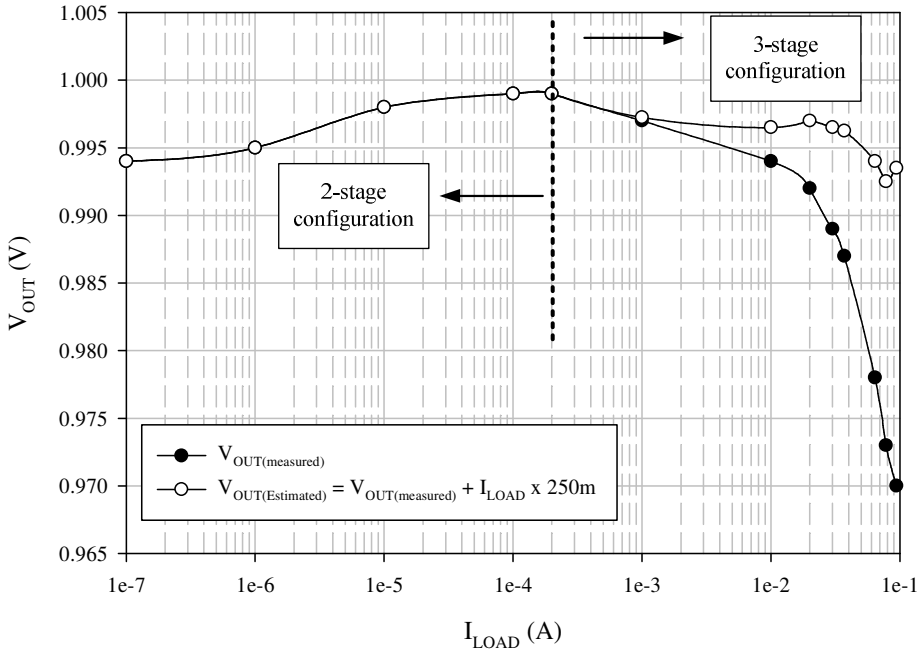


Figure 5.11: Measured and estimated load regulation with C_L = 100 pF

Fig. 5.12 shows the measured line transient response. The supply voltage V_{IN} switches between 1 V and 1.2 V in 10 µs. The output voltage is settle to about 0.8 V at I_{LOAD} = 0.

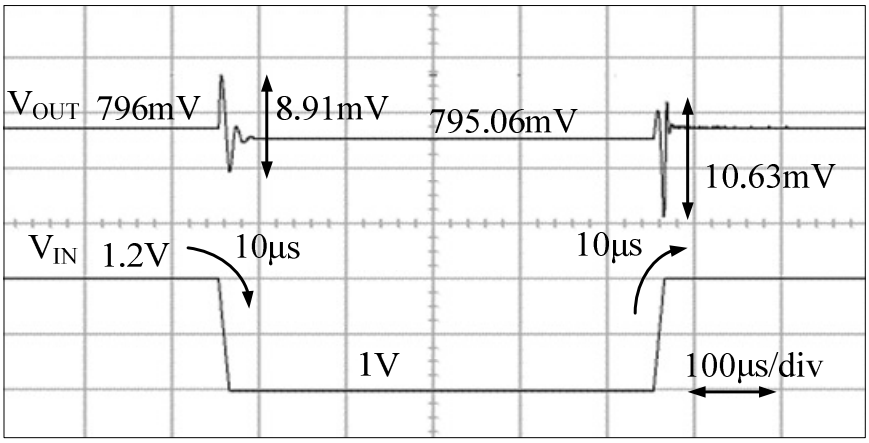


Figure 5.12: Measured line transient response at I_{LOAD} = 0 and V_{OUT} = 0.8 V

The measured result shows that the maximum voltage spike is about 10.63 mV when V_{IN} is switched from 1 V to 1.2 V. It is interesting to observe an overshoot of 8.91

mV at V_{OUT} when V_{IN} is switched from 1.2 V to 1 V. From simulation result, the overshoot is actually caused by the residue charges at the gate of M_{14} when V_{IN} is switched from 1 V to 1.2 V.

The measured dropout voltage as a function of load current is depicted in Fig. 5.13. When I_{LOAD} = 100mA, it can be seen that the measured dropout voltage is less than 200 mV.

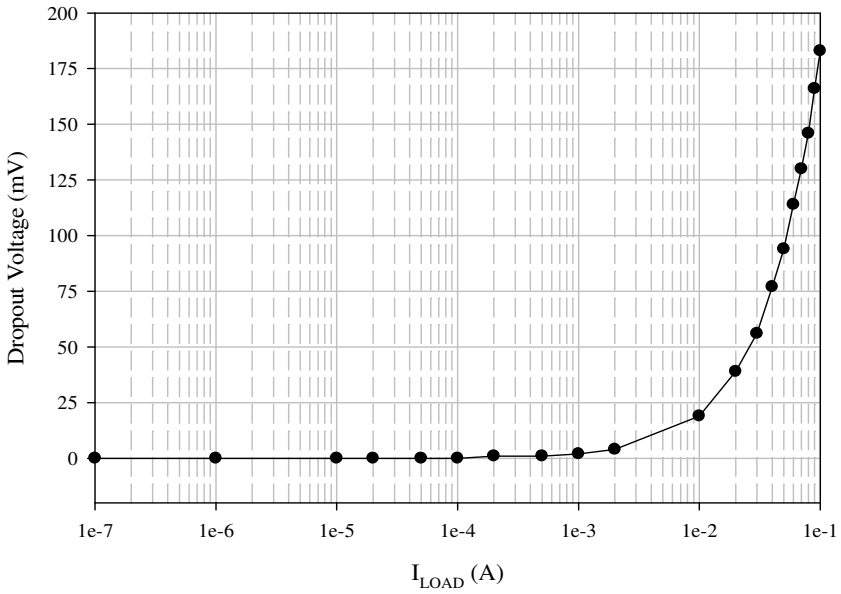


Figure 5.13: Dropout voltage as a function of load currents

Fig. 5.14 depicts the measured PSR result of the proposed regulator at load current of 100 mA, V_{IN} = 1.2 V, V_{OUT} = 1 V and C_L = 100 pF. The PSR is measured by using a high impedance active probe (HP 41800A) and a network analyzer (HP 4395A). From the measured result, the proposed regulator achieves a PSR of -58 dB at 10 kHz. Furthermore, in order to measure the ripple-response, a sinusoidal waveform with V_{P-P} of 200 mV and frequency of 50 kHz is applied to the V_{IN} of the LDO regulator. Fig. 5.15 depicts the measured result of the ripple response.

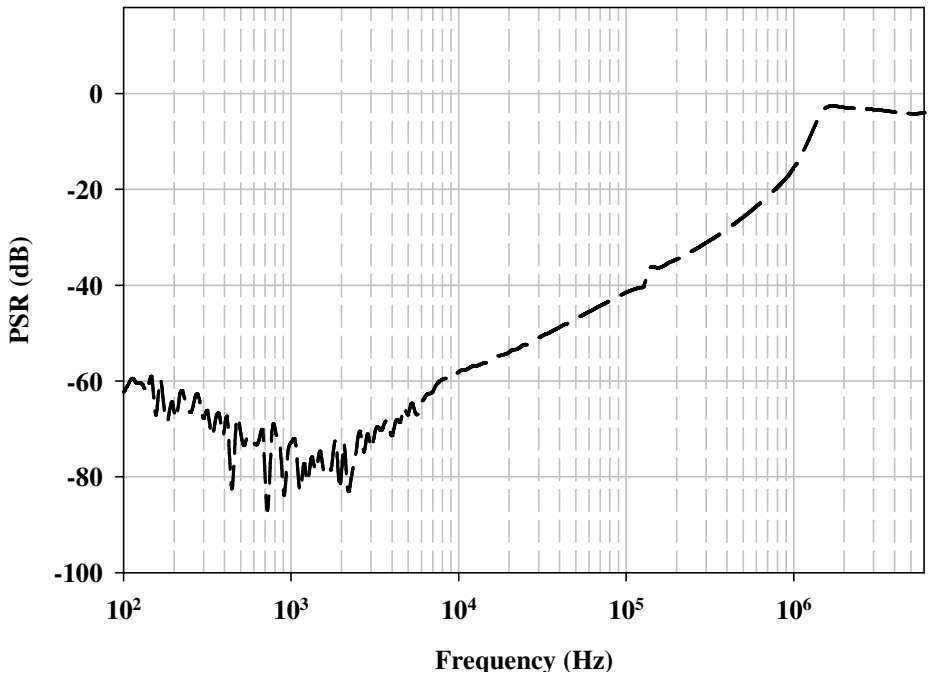


Figure 5.14: Measured PSR at V_{IN} = 1.2 V, V_{OUT} = 1 V and I_{LOAD} = 100 mA

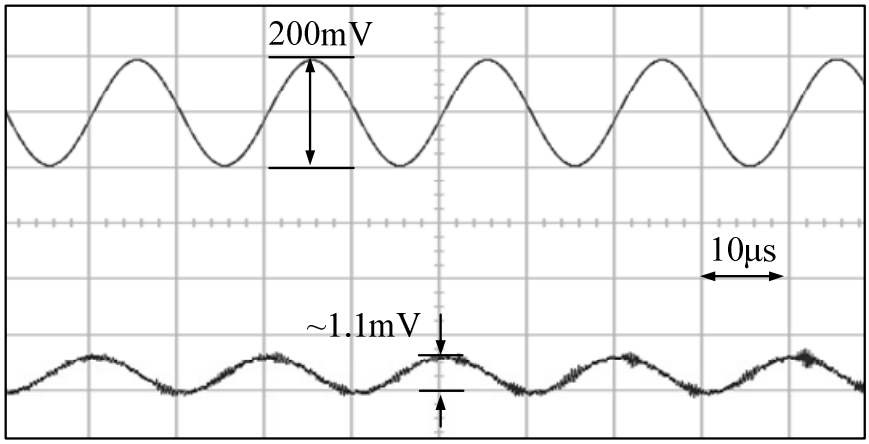


Figure 5.15: Measured ripple-response at V_{IN} = 1.2 V, V_{OUT} = 1 V and I_{LOAD} = 100 mA

The measured quiescent current as a function of I_{LOAD} is shown in Fig. 5.16. As can be seen, the quiescent current keeps increasing when the load current is low and only the sub-power transistor is turned on. The quiescent current stops increasing when I_{LOAD} is about 200 µA. It is where the main power transistor starts conducting

and the second stage starts working in saturation. Due to the channel length modulation effect, the quiescent current increases slightly after I_{LOAD} > 200 µA. The measured quiescent current at full load condition is 82.4 µA. Therefore, the proposed regulator achieves a current efficiency larger than 99.9%.

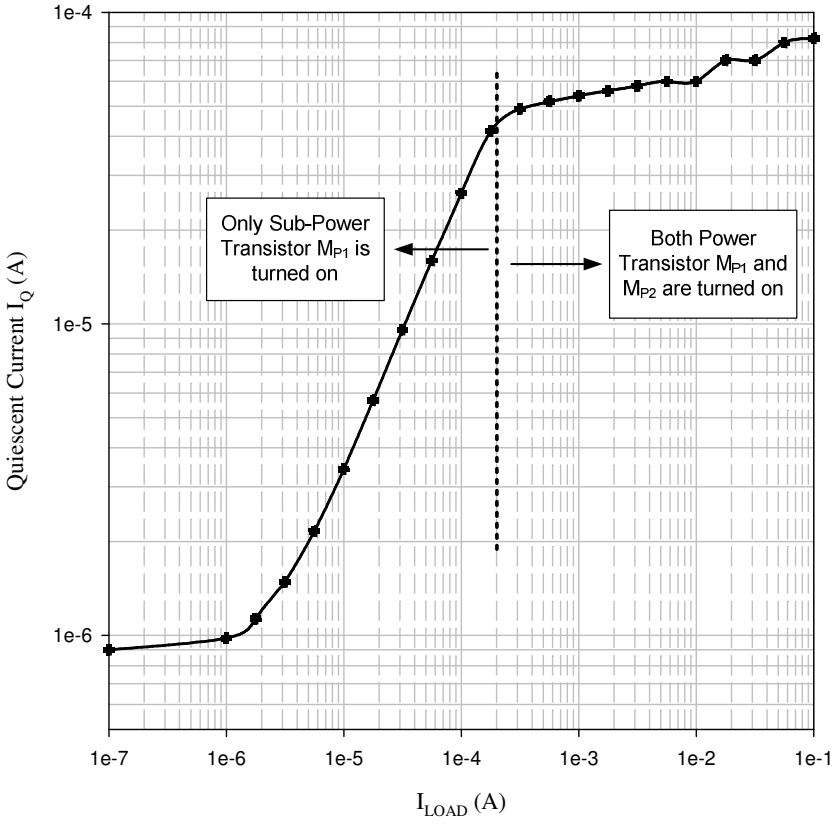


Figure 5.16: Measured quiescent current as a function of I_{LOAD}

The measured temperature dependence is depicted in Fig. 5.17. It can be shown that the measured temperature coefficient of the proposed core LDO regulator is 58 ppm/°C at I_{LOAD} = 100 mA with an external reference of 500 mV.

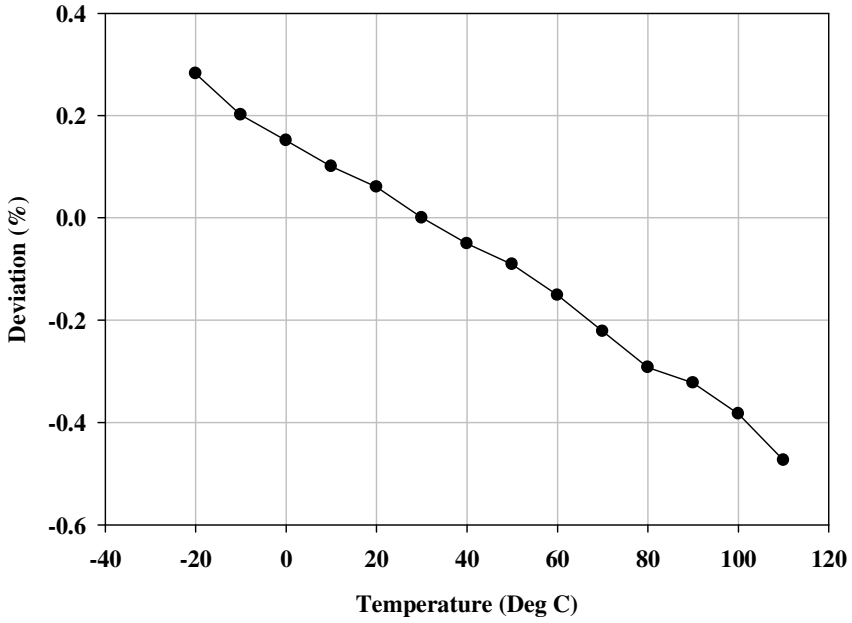


Figure 5.17: Measured temperature dependence at I_{LOAD} = 100 mA

Table 5.2 summaries the measured performance of the proposed regulator.

TABLE 5.2: PERFORMANCE SUMMARY OF THE PROPOSED REGULATOR

V_{IN} (V)	1.2
V_{OUT} (V)	1
I_Q (µA)	0.9-82.4
ΔV_{OUT} (mV)	68.8
I_{LOAD} (mA)	0-100
Line Reg. (mV/V)	4.7
Load Reg. (mV/mA)	0.3
PSR (dB)	-58 @ 10kHz

In addition, the measured performance of the proposed regulator is compared to the reported works in Table 5.3. The FOM for OCL-LDO regulator in [41] is adopted. The smaller the FOM value is, the better is the transient performance metric. As can be seen, the proposed work achieves the smallest OCL-LDO FOM value among all

the reported works. With the adaptive power transistors circuit structure, the overshoot reduction circuitry and the dynamic biasing scheme, the transient performance of the proposed work at ultra-low quiescent current is comparable to the counterparts biased at much higher quiescent values. This suggests that the proposed design has a better transient performance metric. Finally, other performance parameters such as, line and load regulation and PSR have achieved with reasonable good values.

TABLE 5.3: PERFORMANCE COMPARISON WITH REPORTED PRIOR-ART OCL-LDO REGULATORS

Parameters	[70]	[2]	[63]	[30]	[33]	[41]	[84]	**This work**
Year	2005	2007	2008	2010	2010	2010	2011	**2012**
Technology (µm)	0.09	0.35	0.35	0.35	0.35	0.09	0.35	**0.065**
Chip Area (mm^2)	0.098	0.120	0.096	0.145	0.155	0.019	0.2	**0.017**
$I_{LOAD(max)}$ (mA)	100	50	50	100	100	100	100	**100**
$I_{LOAD(min)}$ (mA)	0	0	0	0	1	3	0	**0**
V_{DO} (mV)	300	200	400	200	200	250	142	**200**
V_{OUT} (V)	0.9	2.8	0.5	1.6	1.2	0.5	1.5	**1**
$C_{on\text{-}chip}$ (pF)	N/A	21	-	7	6	7	8	**4.5**
C_L (pF)	600	0-100	0	0-100	0-1000	0-50	0-100	**0-100**
I_Q (µA)	6000	65	0.103	20	43	8	27	**0.9-82.4**
ΔV_{OUT} (mV)	90	90	320	97	70	114	25	**68.8**
ΔI_{LOAD} (mA)	100	50	50	100	99	97	100	**100**
Line Reg. (mV/V)	N/A	23	21.76	0.0574	N/A	3.78	1.046	**4.7**
Load Reg. (mV/mA)	1.8	0.56	0.324	0.109	0.4	0.1	0.0752	**0.3**
PSR (dB)	N/A	-57 (1kHz)	N/A	-40 (10kHz)	N/A	-44 (1kHz)	-39.5 (10kHz)	**-58 (10kHz)**
Settling Time (µs)	N/A	15	400	<9	3	5	N/A	**6**
Edge time (ns)	0.1	1000	N/A	100	1000	100	1000	**300**
Edge time ratio K	1	10000	N/A	1000	10000	1000	10000	**3000**
FOM (V)	0.0054	1.17	N/A	0.0194	0.304	0.0094	0.0675	**0.0019**

5.5 SUMMARY

An adaptive power transistors architecture and technique which enables ultra-low quiescent current and power OCL-LDO regulator is introduced. The regulator is able to maintain stable operation from 0 to 100 mA without the need of minimum loading current requirement. In addition, it dissipates only 0.9 μA at I_{LOAD} = 0 and greatly improved the efficiency at light load. From moderate to full loading condition, the performance is improved by additional power transistor and second gain stage. The proposed concept has been implemented and fabricated in 65 nm CMOS process for demonstration. Compared to the prior-art works, the proposed LDO regulator obtains a better quiescent power and dynamic transient response performance metrics. In addition, it also provides comparable PSR, line regulation and load regulation. Finally, the proposed scheme achieves the best transient FOM value among the OCL-LDO regulators. Therefore, the proposed work is useful for on-chip applications in nanometer CMOS technologies.

CHAPTER 6

AN OUTPUT-CAPACITORLESS LDO REGULATOR WITH LOW-IMPEDANCE LOADING NETWORK

6.1 INTRODUCTION

In this chapter, a new low-impedance loading network is presented [85]. To demonstrate the effectiveness of quiescent current reduction, the proposed circuit technique is applied to an OCL-LDO regulator. In additional to that, the employment of adaptive biasing circuit, the stability and dynamic transient performance metrics of the regulator are improved.

6.2 PROPOSED OCL-LDO REGULATOR STRUCTURE

The simplified schematic of the proposed OCL-LDO regulator is depicted in Fig. 6.1. The first gain stage is formed by a current mirror based operational transconductance amplifier (OTA) with bottom output cascode structure that comprises transistors M_0-M_{10}. Other than the normal biasing current for OTA to operate in weak-inversion region, to improve the bandwidth and speed of the circuit under higher load currents, an adaptive biasing network formed by the transistors M_{b0}-M_{b4}, is included. The power transistor M_P, the proposed low-power low-impedance loading network

consisting of the transistors M_{a0}-M_{a2} and the resistive feedback network consisting of R_{f1} and R_{f2} form the second gain stage.

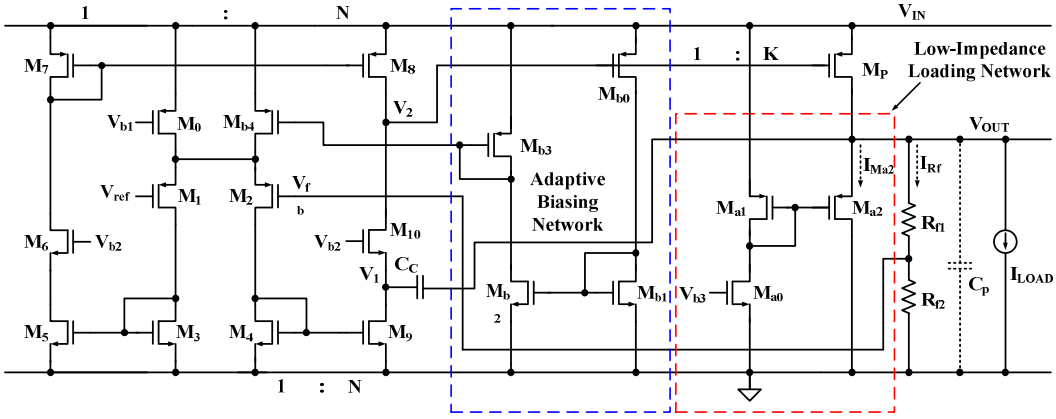


Figure 6.1: Schematic of proposed LDO regulator

The design objective of the low-impedance loading network is to provide a low ac output impedance such that the stability and the phase margin of the OCL-LDO regulator at zero load current as well as low quiescent biasing current can be achieved easily. It should be noted that despite the loading network reduces the second stage gain, the overall two-stage gain are still adequate for the LDO regulator due to the high gain contributed by the micro-power OTA. The overall simulated open-loop gain is around 50 dB ~ 80 dB. The frequency compensation is achieved by the cascode compensation. C_C is the required on-chip compensation capacitance in design. Finally, I_{LOAD} and C_p models the load current and the parasitic load capacitance of the power line.

The output impedance of the proposed low-impedance loading network can be estimated by $1/g_{ma2}$, where g_{ma2} is the transconductance of transistor M_{a2}. The output impedance R_{out} of the LDO regulator at light load currents can be estimated as

$$R_{out} = (R_{f1} + R_{f2}) // \frac{1}{sC_p} // r_{op} // \frac{1}{g_{ma2}} // R_L \approx \frac{1}{g_{ma2}} \quad (6.1)$$

where r_{op} and R_L is the output resistance of the power transistor and load dependent resistance, respectively. Since the power transistor operates in sub-threshold region at light load currents, the value of r_{op} is large. Thus, it is difficult to stabilize the OCL-LDO regulator at zero and light load current without adding the low-impedance network. As the transistor M_{a2} is biased in saturation region, the transconductance g_{ma2} is proportional to the biasing current and aspect ratio. This turns out that only a certain amount of dc biasing current I_{Ma2} is required to yield a low ac output impedance for a large aspect ratio. This is favorable for low power design.

For instance, in this design, I_{Ma2} is 10 µA and W/L = 150 µm /1 µm to yield a g_{ma2} of 200 µA/V. The effective ac output impedance is about 5 kΩ (1/200 µA/V). Therefore, the pole at the output of the proposed LDO regulator is located at higher frequency than that of conventional LDO regulators without the loading network. As a result, the phase margin is improved. Reducing the resistance values for R_{f1} and R_{f2} is another method to achieve low ac output impedance without using the loading network. For example, 200 µA is required to realize a 5 kΩ resistance for an output voltage of 1 V. The required current is about 20 times more than the proposed method. Hence, there will be a significant increase in the dc quiescent power for the OCL-LDO regulator. As a remark, the ac low-impedance loading network is suitable for low power design without depending on low feedback resistance values.

Fig. 6.2 shows the open-loop small-signal diagram of the proposed OCL-LDO regulator. It is noted that the transconductance of respective device is defined as g_{mi}.

R_{oi} and C_i denote the respective output resistance and lumped output parasitic capacitance of each node. C_{gd} is the parasitic gate-drain capacitance of the power transistor.

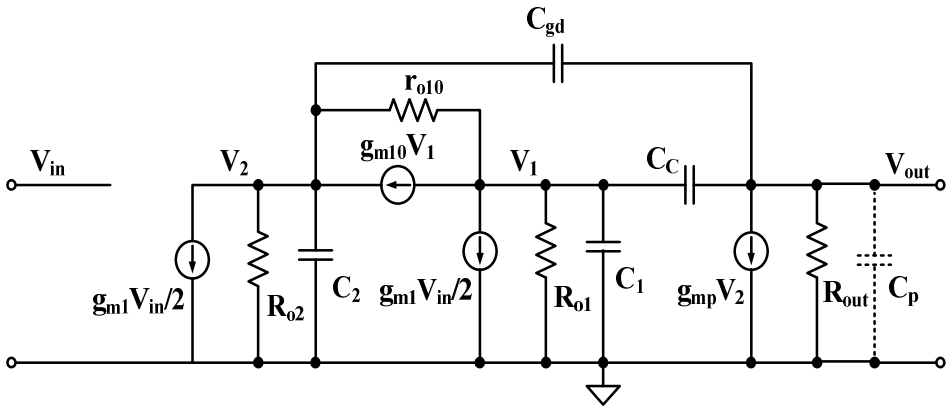


Figure 6.2: Small-signal diagram of the proposed LDO

The derived transfer function is obtained as follows:

$$T(s) = A_{dc} \times \frac{1 + \frac{C_c}{2g_{m10}}s - \frac{C_c(C_2 + C_{gd})}{2g_{m10}g_{mp}}s^2}{(1 + \frac{s}{p_{-3dB}})\left(1 + \left[\frac{C_cC_{gd}}{g_{m10}(C_{gd} + C_c)} + \frac{C_cC_2 + C_2C_p + C_{gd}C_p}{g_{mp}(C_{gd} + C_c)}\right]s + \frac{C_cC_p(C_2 + C_{gd})}{g_{m10}g_{mp}(C_c + C_{gd})}s^2\right)} \quad (6.2)$$

The transfer function is derived based on the following assumptions:

1. $g_{m1}R_{o2} >> 1$ and $g_{mp}R_{out} >> 1$
2. Input impedance of cascode stage $R_{o1}=1/g_{m10}$.
3. Parasitic capacitor C_1 is small and can be ignored in the analysis.

The low frequency DC gain is given as

$$A_{dc} = -g_{m1}g_{mp}R_{o2}R_{out} \times N \times \frac{R_{f2}}{R_{f1} + R_{f2}} \quad (6.3)$$

where N is the aspect ratio between transistor pairs M_4 – M_9 and M_7 – M_8.

The dominant pole is located at

$$p_{-3dB} = -\frac{1}{g_{mp} R_{o2} R_{out} (C_{gd} + C_c)} \tag{6.4}$$

The stability of LDO regulator will be discussed at different loading conditions as the output load current varies greatly. There are two cases to be considered.

6.2.1 CASE 1: I_{LOAD} < 1 MA

When I_{LOAD} is less than 1 mA, the transfer function is to be analyzed as full in (6.2). The zeros are neglected since they are located at much higher frequencies. Due to the small g_{mp} which makes the quadratic equation b^2-4ac < 0 in the denominator, there is a pair of complex poles. The corresponding Q factor and pole frequency of the complex poles are

$$Q = \sqrt{\frac{g_{m10} g_{mp} (C_c + C_{gd})}{C_c C_p (C_2 + C_{gd})}} \times \left[\frac{C_c C_{gd}}{g_{m10} (C_{gd} + C_c)} + \frac{C_c C_2 + C_2 C_p + C_{gd} C_p}{g_{mp} (C_{gd} + C_c)} \right] \tag{6.5}$$

$$\omega_o = \sqrt{\frac{g_{m10} g_{mp} (C_c + C_{gd})}{C_c C_p (C_2 + C_{gd})}} \tag{6.6}$$

From (6.5) and (6.6), it can be shown that by increasing the g_{mp}, the complex poles of the system can be moved to higher frequencies and the Q factor of the system is reduced. At light load currents, the power transistor M_p is operating in sub-threshold region. The transconductance g_{mp} which is defined by qI_D/nkT is weak. Through the reuse of majority of power transistor biasing current for the current I_{Ma2} in the loading network, g_{mp} can be economically increased in a low power way whilst locating the

output pole at high frequency without the need to use low feedback resistances that significantly increase the dc power.

6.2.2 CASE 2: I_{LOAD} > 1 MA

Under this condition, the transfer function of (6.2) can be simplified to

$$T(s) \approx \frac{A_{dc}\left(1+\frac{C_c}{2g_{m10}}s-\frac{C_c(C_2+C_{gd})}{2g_{m10}g_{mp}}s^2\right)}{(1+\frac{s}{p_{-3dB}})\left(1+\frac{C_cC_{gd}}{g_{m10}(C_{gd}+C_c)}s+\frac{C_cC_p(C_2+C_{gd})}{g_{m10}g_{mp}(C_c+C_{gd})}s^2\right)} \tag{6.7}$$

The position of the dominant pole remains unchanged. When g_{mp} is large, the quadratic function at the denominator of (6.7) gives two real poles when b^2-4ac > 0 holds. The frequency compensation is dominated by Miller effect, due to the unavoidable C_{gd} and which also introduces a right-hand-plane zero (6.11). The first and second non-dominant poles and a pair of zeros are obtained as follows:

$$p_1 = -\frac{g_{m10}(C_c+C_{gd})}{C_cC_{gd}} \tag{6.8}$$

$$p_2 = -\frac{g_{mp}C_{gd}}{C_{out}(C_{gd}+C_2)} \tag{6.9}$$

$$z_{LHP} = -\frac{2g_{m10}}{C_c} \tag{6.10}$$

$$z_{RHP} = +\frac{g_{mp}}{C_{gd}+C_2} \tag{6.11}$$

The first non-dominant pole, p_1, is close enough to approximately cancel the left-hand-plane zero, z_{LHP}. Due to large g_{mp}, the right-hand-plane zero, z_{RHP} and the second non-dominant pole, p_2 are located at high frequencies. Stability is guaranteed

as the system is effectively a one pole system. The simulation result shows that the proposed OCL-LDO regulator is stable under this condition with a phase margin of about 90º.

6.3 SIMULATED RESULTS AND DISCUSSIONS

The proposed OCL-LDO regulator with low-impedance loading network has been designed and simulated with GLOBALFOUNDRIES 0.18-µm CMOS process. The LDO regulator is able to deliver a maxium load current of 100 mA with an output voltage of 1 V for a supply range from 1.2 V to 1.8 V. At maximum load current, the dropout voltage is 200 mV at 1.2 V supply. The size of the compensation capacitor C_C is 10 pF and the parasitic capacitance C_P at power line is assumed to be 100 pF. The designed quiescent current is 14 µA. The simulated line regulation at $I_{LOAD} = 0$ and $I_{LOAD} = 100$ mA are 274 µV/V and 220 µV/V respectively. Load regulation is 19.54 µV/mA at $V_{IN} = 1.2$ V.

The open-loop gain frequency responses of the proposed LDO regulator at load current of 0, 1 mA and 100 mA are depicted in Fig. 6.3. There is no obvious peaking effect even at zero load current condition. It can be confirmed that the proposed LDO regulator is stable for the load current value ranging from 0 to 100 mA. The minimum phase margin is 67º at zero load current condition. From Fig. 6.3, it can be observed the improvement of UGF when the adaptive biasing scheme is employed.

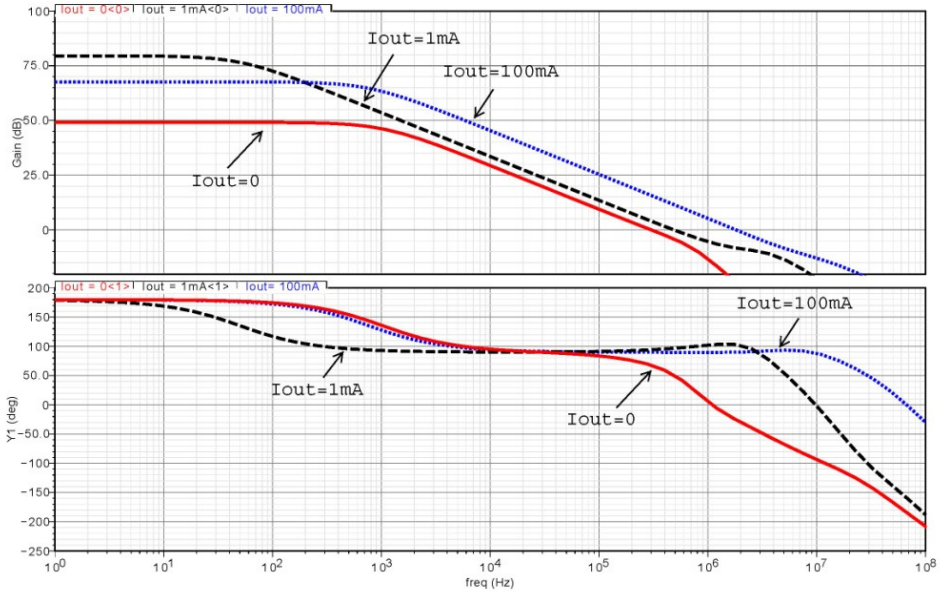


Figure 6.3: Open-loop ac response at different output load condition

The load transient response of the proposed LDO regulator when the load current is switched from 0 to 100 mA and vice versa with an edge time of 1 µs is simulated and illustrated in Fig. 6.4. It can be seen that the proposed LDO regulator has an overshoot and undershoot of 198 mV and 339 mV respectively. The simulation result also indicates that 1% settling time is about 3.96 µs and 1.15 µs respectively.

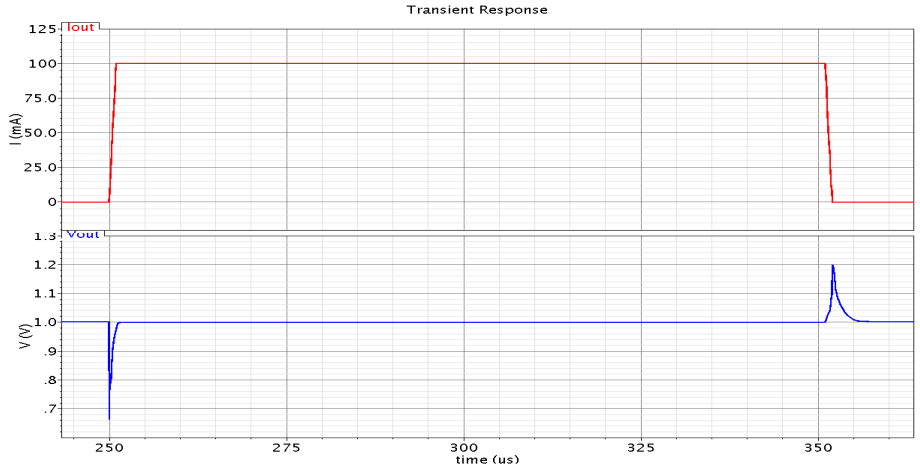


Figure 6.4: Load transient response from 0 to 100mA and vice versa

Table 6.1 shows the performance comparison of the proposed work with respect to the recent prior-art works. It indicates that the optimal tradeoff performance can be obtained in the proposed work.

TABLE 6.1: COMPARISON OF REPORTED PRIOR-ART RESULTS

Parameter	[31]	[2]	[64]	[32]	[34]	[30]	This work
Year	2007	2007	2007	2008	2009	2010	2010
Technology (µm)	0.35	0.35	0.18	0.35	0.35	0.35	0.18
$I_{LOAD(max)}$ (mA)	100	50	50	50	100	100	100
$I_{LOAD(min)}$ (µA)	100	0	50	0	50	0	0
V_{DO} (mV)	200	200	200	200	200	200	200
V_{OUT} (V)	1	2.8	1	1	1	1.6	1
C_C (pF)	6	21	-	-	3	7	10
C_L (pF)	100	0-100	0-100	>20	100	100	0-100
I_Q (µA)	100	65	1.2	95	27-270	20	14-53.5
ΔV_{OUT} (mV)	<50	<90	~400	~180	N.A.	<97	<339
Line Reg. (mV/V)	0.344	<42	4.75	18	0.027	0.0574	0.274
Load Reg. (µV/mA)	338	<840	148	280	1.2	109	19.54
PSR (dB)	N.A.	-57@ 1kHz	N.A.	N.A.	-49.8@ 10kHz	-40@ 10kHz	-46.9@ 10kHz
Settling Time (µs)	~30	~15	3	~0.3	~0.6	<9	<3.96
$I_{STABILITY(min)}$ (µA) = $I_{LOAD(min)} + I_Q$	200	65	51.2	95	77	20	14

6.4 SUMMARY

A low-impedance loading network design technique has been presented in this chapter. It permits the use of low quiescent current to improve the phase margin in the open-loop response of the LDO regulator. The simulation results have confirmed that the required stability current is minimized when compared to that of reported prior-art works. Therefore, the proposed design technique offers a quiescent power-aware design, suggesting that it is attractive for battery-powered on-chip applications.

CHAPTER 7

CONCLUSIONS AND FUTURE WORKS

7.1 CONCLUSIONS

This thesis has presented a study of the frequency compensation, power consumption reduction and transient enhancement techniques dedicated to the design of LDO regulators. All the proposed works are realized in CMOS 0.18 µm or 65 nm technologies and analyzed in details, with the main goals of achieving low quiescent power consumption, low voltage operation, area efficiency and balanced performance parameters. The results are compared with the representative state-of-art works. It turns out that the strategic performance metrics meet the design objectives.

The frequency compensation techniques are first reviewed. It is one of the most importance aspects because the power-bandwidth and the area efficiency of the LDO regulators are influenced by the effectiveness of frequency compensation method. A new frequency compensation technique for use in the error amplifier is proposed. The results have shown that the proposed frequency compensation technique for a three-stage amplifier design achieves very small area as well as high power-bandwidth efficiency with a large capacitive load. This multistage amplifier can be served as an error amplifier dedicated to drive a big on-chip or off-chip power transistor. The proposed frequency compensation technique is effective only

for large capacitive load. For small capacitive load applications, other frequency compensation techniques should be considered.

On top of the above contribution, the fundamental understanding on the limitations of LDO regulators is addressed because it is crucial to the study. Three new circuit techniques dedicated to the design of low-quiescent OC-LDO regulator as well as OCL-LDO regulators are then proposed. They are given in the following remarks.

Firstly, two LDO regulators based on the push-pull and dynamic-biased composite power transistor are proposed. They can be applied to both the OCL-LDO regulator and the OC-LDO regulator. The bootstrap of transconductance parameter for the power device significantly enhances the LDO regulator's performance metrics, particularly on the transient response. Besides, the stability of the LDO regulators is made easy owing to the shunt feedback embedded in the composite power transistors. This avoids the use of complicated frequency compensation schemes to stabilize the LDO regulators. The composite power transistor also enables low voltage design which is usually not possible for conventional source follower buffer.

Secondly, another OCL-LDO regulator is proposed using the adaptive power transistor circuit architecture. This permits the choice of lower quiescent power consumption in context of sustaining stability under a multistage LDO regulator structure. This architecture is particularly suitable for applications that require ultra-low quiescent current under standby operation mode. Of particular importance, the architecture can provide high current efficiency as well as large transient FOM value in conjunction with other balanced performance metrics.

Thirdly, the employment of active low impedance loading network has been demonstrated through an OCL-LDO regulator design. Not only does it enhance the stability at low load current condition, it offers the technical merit that no minimum current is required. As such, when the quiescent current is made low, the current efficiency at low load current is improved significantly. The circuit technique can also be extended to other OC-LDO regulator designs whenever low output impendence is required.

Overall, these low power LDO regulators and the frequency compensation technique will be useful for portable and battery operated electronic systems.

7.2 FUTURE WORKS

A series of circuit design techniques validated from the transistor-level design allows low-power and fast-transient operations of the LDO regulators to be achieved. Although the techniques are successfully demonstrated to enhance the performances for the LDO regulators, there are still some possible future research directions that could be further investigated.

The multistage amplifier employing the CFCC technique can operate as an error amplifier in the OC-LDO regulator. Since the dominant pole is located at the output of the regulator, it can be made stable by generating an internal zero or the ESR zero. For the application in the form of OCL-LDO regulator, it has to be compensated internally for meeting stability issue. Therefore, further frequency compensation technique can be investigated. They play the important role for CFCC error amplifier based OCL-LDO regulator design.

Besides analog aspect, digital implementation for LDO regulator can be useful due to the continual push from advanced CMOS nanometer technologies. This stems from the fact that digital implementation is less sensitive to environment disturbances and more robust to the process and temperature variations, especially for fully digital systems in nanometer technologies.

In view of OC-LDO regulators that exhibit small overshoot and understood with fast switching load, the drawback of OCL-LDO regulator can be seen. In general, the OCL-LDO regulator will experience a larger overshoot and overshoot characteristic.

Therefore, the circuit technique that permits significant reduction of overshoot and undershoot for OCL-LDO regulator is also worth investigated.

The OCL-LDO regulators usually suffer relatively poor high frequencies PSR when compared to that of the OC-LDO regulators counterpart. This is mainly because the OCL-LDO regulators do not have the large output capacitor to shunt the output ripple to ground at high frequencies. As a result, OCL-LDO regulator that has high PSR at high frequencies would be very attractive for many integrated system applications. In view of the reported PSR circuit techniques, they can be observed in the following. (i) They dissipate significant high power consumption for broadband PSR rejection or (ii) they support low load currents (few mA) range with broadband PSR. Therefore, it is highly desirable to investigate very low-power broadband PSR improvement circuit technique whist supporting high load current range (100mA).

The stability of the OCL-LDO regulator is highly affected by the capacitive load at the output. In most of the OCL-LDO regulator designs, the regulators can remain stable with only a specific or a small capacitive load range (0 – 100 pF). The design techniques for applications require higher capacitive load (1 nF to 10 nF) is seldom reported. Therefore, more studies of the circuit techniques, that permit the OCL-LDO regulator to be made stable for a wide range of capacitive load, can be carried out.

AUTHOR'S PUBLICATIONS

JOURNAL PAPERS

1. **S. S. Chong**, H. Kwantono and P. K. Chan, "A 4.7μA quiescent current, 450 mA CMOS low-dropout regulator with fast transient response," *IEICE Transactions on Electronics*, vol. E94-C, no. 8, pp. 1271-1281, Aug. 2011.
2. **S. S. Chong** and P. K. Chan, "Cross feedforward cascode compensation for low-power three-stage amplifier with large capacitive load," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2227-2234, Sept. 2012.
3. **S. S. Chong** and P. K. Chan, "A 0.9-μA quiescent current output-capacitorless LDO regulator with adaptive power transistors in 65-nm CMOS," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 60, no. 4, pp. 1072-1081, April 2013.
4. **S. S. Chong** and P. K. Chan, "A sub-1V transient-enhanced output-capacitorless LDO regulator with push-pull composite power transistor," to appear in *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, 2014.

CONFERENCE PAPERS

1. **S. S. Chong** and P. K. Chan, "A Quiescent Power-Aware Low-Voltage Output Capacitorless Low Dropout Regulator for SoC Applications," *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, Brazil, pp. 37-40, May 2011.
2. **S. S. Chong** and P. K. Chan, "A Flipped Voltage Follower Based Low-Dropout Regulator with Composite Power Transistor", *IEEE International Symposium on Integrated Circuits (ISIC)*, Singapore, pp. 472-475, Dec 2011.

REFERENCES

[1] G. A. Rincon-Mora, "Current efficient, low voltage, low dropout regulators," PhD dissertation, Eletrical Engineering, Georgia Institute of Technology, 1996.

[2] R. J. Milliken, J. Silva-Martinez, and E. Sanchez-Sinencio, "Full On-Chip CMOS Low-Dropout Voltage Regulator," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 54, pp. 1879-1890, Sept. 2007.

[3] M.-H. Huang and K.-H. Chen, "Single-Inductor Multi-Output (SIMO) DC-DC Converters With High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices," *IEEE J. Solid-State Circuits,* vol. 44, pp. 1099-1111, Apr. 2009.

[4] D. Kwon and G. A. Rincon-Mora, "Single-Inductor-Multiple-Output Switching DC-DC Converters," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 56, pp. 614-618, Aug. 2009.

[5] D. Ma, W.-H. Ki, C.-Y. Tsui, and P. K. T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode," *IEEE J. Solid-State Circuits,* vol. 38, pp. 89-100, Jan. 2003.

[6] F. Su, W.-H. Ki, and C.-Y. Tsui, "Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications," *IEEE J. Solid-State Circuits,* vol. 43, pp. 815-822, Apr. 2008.

[7] R. Perez, "A comparative assessment between linear and switching power supplies in portable electronic devices," in *IEEE International Symposium on Electromagnetic Compatibility*, 2000, pp. 839-843 vol.2.

[8] J. Wong, "A low-noise low drop-out regulator for portable equipment," in *Power Conversion and Intelligent Motion*, May. 1990, pp. 38-43.

[9] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits,* vol. 33, pp. 36-44, Jan. 1998.

[10] K. N. Leung, M. Ho, J. Guo, and P. Y. Or, "Development of energy-efficient fast-transient CMOS low-dropout regulators for SoC applications," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May. 2011, pp. 305-308.

[11] J. Xiao, "An ultra-low-quiescent-current dual-mode digitally-controlled buck converter IC for cellular phone applications," PhD dissertation, Eletrical Engineering and Computer Science, University of Califirnia, Berkeley, 2003.

[12] T. Wakimoto, "LDO Design Methodology and an Intelligent Power Management Sub-System IC for CDMA Handsets," *IEICE Trans. Electron.,* vol. E93.C, pp. 1518-1524, Oct. 2010.

[13] A. Matsuzawa, "Low voltage mixed analog/digital circuit design for portable equipment," in *Symposium on VLSI Circuits, Dig. of Tech. Papers*, May. 1993, pp. 49-54.

[14] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*: New York Oxford University Press, 2nd Edition, 2002.

[15] P. R. Gray and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*: New York: John Willy & Sons, Inc, 1993.
[16] B. Razavi, *Design of Analog CMOS Integrated Circuits*: McGraw-Hill, 2000.
[17] R. J. Baker, *CMOS Circuit Design, Layout, and Simulation*: John Wiley & son, 2005.
[18] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits,* vol. 38, pp. 1691-1702, Oct. 2003.
[19] B. K. Ahuja, "An improved frequency compensation technique for CMOS operational amplifiers," *IEEE J. Solid-State Circuits,* vol. 18, pp. 629-633, Dec. 1983.
[20] J. H. Huijsing, "Multi-stage Amplifier with capacitive nesting for frequency compensation," U.S. Patent 4,559,502, Dec. 17, 1985.
[21] K. N. Leung, P. K. T. Mok, W.-H. Ki, and J. K. O. Sin, "Three-stage large capacitive load amplifier with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits,* vol. 35, pp. 221-230, Feb. 2000.
[22] K. N. Leung and P. K. T. Mok, "Analysis of multistage amplifier-frequency compensation," *IEEE Trans. Circuits Syst. I,* vol. 48, pp. 1041-1056, Sept. 2001.
[23] H. Lee and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits,* vol. 38, pp. 511-520, Mar. 2003.
[24] G. A. Rincon-Mora, *Analog IC Design with Low-Dropout Regulator (LDOs)*: McGraw-Hill, 2009.
[25] G. A. Rincon-Mora and P. E. Allen, "Optimized frequency-shaping circuit topologies for LDOs," *IEEE Trans. Circuits Syst. II, Analog and Digit. Signal Process.,* vol. 45, pp. 703-708, Jan. 1998.
[26] Y.-S. Shyu and J.-C. Wu, "A 60μA Quiescent Current, 250mA CMOS Low-Dropout Regulator," *IEICE Trans. Electron.,* vol. E84-C, pp. 693-703, May. 2001.
[27] K. N. Leung and Y. S. Ng, "A CMOS Low-Dropout Regulator With a Momentarily Current-Boosting Voltage Buffer," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 57, pp. 2312-2319, Nov. 2010.
[28] C. K. Chava and J. Silva-Martinez, "A frequency compensation scheme for LDO voltage regulators," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 51, pp. 1041-1050, Jun. 2004.
[29] Y. Tian and P. K. Chan, "Design of high-performance analog circuits using wideband g_m-enhanced MOS composite transistors," *IEICE Trans. Electron.,* vol. E93-C, pp. 1199-1208, Jul. 2010.
[30] E. N. Y. Ho and P. K. T. Mok, "A Capacitor-Less CMOS Active Feedback Low-Dropout Regulator With Slew-Rate Enhancement for Portable On-Chip Application," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 57, pp. 80-84, Feb. 2010.
[31] S. K. Lau, P. K. T. Mok, and K. N. Leung, "A Low-Dropout Regulator for SoC With Q-Reduction," *IEEE J. Solid-State Circuits,* vol. 42, pp. 658-664, Mar. 2007.

[32] T. Y. Man, K. N. Leung, C. Y. Leung, P. K. T. Mok, and M. Chan, "Development of Single-Transistor-Control LDO Based on Flipped Voltage Follower for SoC," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 55, pp. 1392-1401, Jun. 2008.

[33] P. Y. Or and K. N. Leung, "An Output-Capacitorless Low-Dropout Regulator With Direct Voltage-Spike Detection," *IEEE J. Solid-State Circuits,* vol. 45, pp. 458-466, Feb. 2010.

[34] C. Zhan and W.-H. Ki, "A high-precision low-voltage low dropout regulator for SoC with adaptive biasing," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May. 2009, pp. 2521-2524.

[35] Y.-H. Lam, W.-H. Ki, and C.-Y. Tsui, "Adaptively-biased capacitor-less CMOS low dropout regulator with direct current feedback," in *Asia and South Pacific Conference on Design Automation*, Jan. 2006, pp. 104-105.

[36] C.-M. Chen and C.-C. Hung, "A capacitor-free CMOS low-dropout voltage regulator," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May, 2009, pp. 2525-2528.

[37] Y.-H. Lee and K.-H. Chen, "A 65nm sub-1V multi-stage low-dropout (LDO) regulator design for SoC systems," in *IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2010, pp. 584-587.

[38] H.-C. Yang, H.-H. Huang, C.-L. Chen, M.-H. Huang, and K.-H. Chen, "Current feedback compensation (CFC) technique for adaptively adjusting the phase margin in capacitor-free LDO regulators," in *IEEE Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2008, pp. 5-8.

[39] V. Gupta and G. A. Rincon-Mora, "A 5mA 0.6µm CMOS Miller-Compensated LDO Regulator with -27dB Worst-Case Power-Supply Rejection Using 60pF of On-Chip Capacitance," in *IEEE Int. Solid-State Circuits Conf. Dig. of Tech. Papers*, Feb. 2007, pp. 520-521.

[40] R. G. Carvajal, J. Ramirez-Angulo, A. J. Lopez-Martin, A. Torralba, J. A. G. Galan, A. Carlosena*, et al.*, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 52, pp. 1276-1291, Jul. 2005.

[41] J. Guo and K. N. Leung, "A 6-µW Chip-Area-Efficient Output-Capacitorless LDO in 90-nm CMOS Technology," *IEEE J. Solid-State Circuits,* vol. 45, pp. 1896-1905, Sept. 2010.

[42] A. Yoo, "Design, Implementation, Modeling and Optimization of Next Generation Low-Voltage Power MOSFETs," PhD dissertation, Materials Science and Engineering, University of Toronto, 2010.

[43] A. Yoo, M. Chang, O. Trecases, and W. T. Ng, "High performance low-voltage power MOSFETs with hybrid waffle layut structure in 0.25µm standard CMOS process," in *Int. Symp. Power Semiconductor Devices and IC's*, May. 2008, pp. 95-98.

[44] A. Hastings, *The Art of Analog Layout*: Pearson/Prentice Hall, 2006.

[45] L. Baker, R. Currences, S. Law, M. Le, C. Lee, S. T. Lin*, et al.*, "A waffle layout technique strengthens the ESD hardness of the NMOS output transistor," in *EOS.ESD Symp. Proc. EOS-11*, 1989, pp. 175-181.

[46] X. Fan, C. Mishra, and E. Sanchez-Sinencio, "Single Miller capacitor frequency compensation technique for low-power multistage amplifiers," *IEEE J. Solid-State Circuits,* vol. 40, pp. 584-592, Mer. 2005.

[47] S. S. Chong and P. K. Chan, "Cross Feedforward Cascode Compensation for Low-Power Three-Stage Amplifier With Large Capacitive Load," *IEEE J. Solid-State Circuits,* vol. 47, pp. 2227-2234, Sept. 2012.
[48] H. Lee and P. K. T. Mok, "Advances in active-feedback frequency compensation with power optimization and transient improvement," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 51, pp. 1690-1696, Sept. 2004.
[49] S. Guo and H. Lee, "Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers," *IEEE J. Solid-State Circuits,* vol. 46, pp. 452-464, Feb. 2011.
[50] B. Y. T. Kamath, R. G. Meyer, and P. R. Gray, "Relationship between frequency response and settling time of operational amplifiers," *IEEE J. Solid-State Circuits,* vol. 9, pp. 347-352, Dec. 1974.
[51] J. H. Huijsing and D. Linebarger, "Low-voltage operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circuits,* vol. 20, pp. 1144-1150, Dec. 1985.
[52] R. G. H. Eschauzier, L. P. T. Kerklaan, and J. H. Huijsing, "A 100-MHz 100-dB operational amplifier with multipath nested Miller compensation structure," *IEEE J. Solid-State Circuits,* vol. 27, pp. 1709-1717, Dec. 1992.
[53] F. You, S. H. K. Embabi, and E. Sanchez-Sinencio, "Multistage amplifier topologies with nested G_m-C compensation," *IEEE J. Solid-State Circuits,* vol. 32, pp. 2000-2011, Dec. 1997.
[54] R. Joao and M. S. J. Steyaert, "Positive feedback frequency compensation for low-voltage low-power three-stage amplifier," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 51, pp. 1967-1974, Oct. 2004.
[55] H. Lee, K. N. Leung, and P. K. T. Mok, "A dual-path bandwidth extension amplifier topology with dual-loop parallel compensation," *IEEE J. Solid-State Circuits,* vol. 38, pp. 1739-1744, Oct. 2003.
[56] X. Peng and W. Sansen, "AC boosting compensation scheme for low-power multistage amplifiers," *IEEE J. Solid-State Circuits,* vol. 39, pp. 2074-2079, Nov. 2004.
[57] X. Peng and W. Sansen, "Transconductance with capacitances feedback compensation for multistage amplifiers," *IEEE J. Solid-State Circuits,* vol. 40, pp. 1514-1520, Jul. 2005.
[58] A. D. Grasso, G. Palumbo, and S. Pennisi, "Advances in Reversed Nested Miller Compensation," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 54, pp. 1459-1470, Jul. 2007.
[59] X. Peng, W. Sansen, L. Hou, J. Wang, and W. Wu, "Impedance Adapting Compensation for Low-Power Multistage Amplifiers," *IEEE J. Solid-State Circuits,* vol. 46, pp. 445-451, Feb. 2011.
[60] H. K. Kwa, "Amplifier circuit and system incorporating same," U. S. Patent 7,265,632 B2, Sep. 4, 2007.
[61] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator With Buffer Impedance Attenuation," *IEEE J. Solid-State Circuits,* vol. 42, pp. 1732-1742, Aug. 2007.
[62] W. J. Huang and S. I. Liu, "Sub-1V capacitor-free low-dropout regulator," *Electronics Letters,* vol. 42, pp. 1395-1396, Feb. 2006.

[63] Y.-S. Hwang, M.-S. Lin, B.-H. Hwang, and J.-J. Chan, "A 0.35µm CMOS sub-1V low-quiescent-current low-dropout regulator," in *IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 153-156.

[64] T. Y. Man, P. K. T. Mok, and M. Chan, "A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient-Response Improvement," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 54, pp. 755-759, Sept. 2007.

[65] X. Ming, Q. Li, Z.-k. Zhou, and B. Zhang, "An Ultrafast Adaptively Biased Capacitorless LDO With Dynamic Charging Control," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 59, pp. 40-44, Jan. 2012.

[66] E. N. Y. Ho and P. K. T. Mok, "Wide-Loading-Range Fully Integrated LDR With a Power-Supply Ripple Injection Filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 59, pp. 356-360, Jun. 2012.

[67] S. S. Chong, H. Kwantono, and P. K. Chan, "A 4.7µA Quiescent Current, 450mA CMOS Low-Dropout Regulator with Fast Transient Response," *IEICE Trans. Electron.,* vol. E94.C, pp. 1271-1281, Aug. 2011.

[68] J. Ramirez-Angulo, R. G. Carvajal, J. A. Galan, and A. Lopez-Martin, "A free but efficient low-voltage class-AB two-stage operational amplifier," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 53, pp. 568-571, Jul. 2006.

[69] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits,* vol. 38, pp. 958-965, Jun. 2003.

[70] P. Hazucha, T. Karnik, B. A. Bloechel, C. Parsons, D. Finan, and S. Borkar, "Area-efficient linear regulator with ultra-fast load regulation," *IEEE J. Solid-State Circuits,* vol. 40, pp. 933-940, Apr. 2005.

[71] Y.-H. Lam and W.-H. Ki, "A 0.9V 0.35 µm Adaptively Biased CMOS LDO Regulator with Fast Transient Response," in *IEEE Int. Solid-State Circuits Conf. Dig. of Tech. Papers*, Feb. 2008, pp. 442-626.

[72] Y.-H. Lin, K.-L. Zheng, and K.-H. Chen, "Smooth Pole Tracking Technique by Power MOSFET Array in Low-Dropout Regulators," *IEEE Trans. Power Electronics,* vol. 23, pp. 2421-2427, Sept. 2008.

[73] H.-I. Pan and V.-L. Chen, "A 0.18µm Stability-Enhanced CMOS LDO with Robust Compensation Scheme," *IEICE Trans. Electron.,* vol. E92.C, pp. 1080-1086, Aug. 2009.

[74] S. Heng and C.-K. Pham, "A Low-Power High-PSRR Low-Dropout Regulator with Bulk-Gate Controlled Circuit," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 57, pp. 245-249, Apr. 2010.

[75] M. Ho, K. N. Leung, and K.-L. Mak, "A Low-Power Fast-Transient 90-nm Low-Dropout Regulator With Multiple Small-Gain Stages," *IEEE J. Solid-State Circuits,* vol. 45, pp. 2466-2475, Nov. 2010.

[76] S. S. Chong and P. K. Chan, "A 0.9-µA Quiescent Current Output-Capacitorless LDO Regulator With Adaptive Power Transistors in 65-nm CMOS," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. PP, pp. 1-1, 2012.

[77] R. J. Reay and G. T. A. Kovacs, "An unconditionally stable two-stage CMOS amplifier," *IEEE J. Solid-State Circuits,* vol. 30, pp. 591-594, May. 1995.

[78] D. B. Ribner and M. A. Copeland, "Design techniques for cascoded CMOS op amps with improved PSRR and common-mode input range," *IEEE J. Solid-State Circuits,* vol. 19, pp. 919-925, Dec. 1984.

[79] C.-J. Cheng, C.-J. Wu, and S.-Y. Lee, "Programmable pacing channel with a fully on-chip LDO regulator for cardiac pacemaker," in *IEEE Asian Solid-State Circuits Conf.*, Nov. 2008, pp. 285-288.

[80] S. Mandal, S. Arfin, and R. Sarpeshkar, "Fast startup CMOS current references," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May. 2006, pp. 2845-2848.

[81] C. Y. Lu and J. M. Sung, "Reverse short-channel effects on threshold voltage in submicrometer salicide devices," *IEEE Electron Device Letters,* vol. 10, pp. 446-448, Oct. 1989.

[82] C. Subramanian, J. Hayden, W. Taylor, M. Orlowski, and T. McNelly, "Reverse short channel effect and channel length dependence of boron penetration in PMOSFETs," in *Int. Electron Devices Meeting*, Dec. 1995, pp. 423-426.

[83] C. Zhan and W.-H. Ki, "Output-Capacitor-Free Adaptively Biased Low-Dropout Regulator for System-on-Chips," *IEEE Trans. Circuits Syst. I, Reg. Papers,* vol. 57, pp. 1017-1028, May. 2010.

[84] C.-M. Chen and C.-C. Hung, "A fast self-reacting capacitor-less low-dropout regulator," in *Proc. Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sept. 2011, pp. 375-378.

[85] S. S. Chong and P. K. Chan, "A quiescent power-aware low-voltage output capacitorless low dropout regulator for SoC applications," in *IEEE Int. Symp. Circuits Syst. (ISCAS)*, May. 2011, pp. 37-40.