A 12-GHz High Output Power Amplifier using 0.18μm SiGe BiCMOS for low power applications

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***Abstract*—This paper presents a fixed gain high output power amplifier with performance determined by using on-wafer measurement. The amplifier is fully differential based on inductive load and resistive degeneration which is designed using a 0.18 μm SiGe BiCMOS process. The amplifier achieves power gain of 7.2 dB, 3-dB bandwidth of 2.06 GHz, operating frequency of 12 GHz, power consumption of 12 mW using 1.8 V supply voltage and the input referred 1-dB gain compression point of -1.6 dBm. The designed amplifier occupies a die area of 380 μm x 340 μm.**

I. Introduction

The demand for high data rate transmission over wireless media is one of the driving forces for research work. This is made possible with shrinking of process technology node.

The amplifiers used in the RF transmitter [1] requires high linearity to provide large output power and for amplifiers used in the RF receiver chain [2]-[6] requires low noise contribution to the overall system. When the amplifier is operated at high frequency around 12 GHz the performance variation due to process tolerance has to be considered during design stage. The previous amplifiers designed at 12 GHz frequency band were implemented using different process technologies like GaN [1], CMOS SOI/SOS [2], Silicon RF MESFET [3], HEMT [4], GaAs [5] and InAlAs/InGaAs mHEMT [6]. All these process technologies are expensive and are not cost effective as compared to the proposed amplifier's technology. These amplifiers [2]-[6] have low noise performance but consumes high DC power unlike the proposed amplifier which has high output power and low noise performance with a low DC power consumption.

II. Amplifier Circuit Design

A. Design Topology

The amplifier is a single stage fully differential amplifier that is based on common emitter configuration with inductive load. The amplifier input and output are matched to 50 Ω impedance to achieve return loss better than -10 dB for the interested frequency range. The resistive degeneration improves the amplifier linearity and enables high P1dB.

B. Amplifier core design

The main design requirement of the proposed amplifier as shown in Fig. 1 is to achieve high linearity at low power consumption. The amplifier biasing is designed using current mirrors and voltage dividers. The current source for the amplifier biasing is obtained from the bandgap reference that provides PVT (Process-Voltage-Temperature) invariant current. The cross- coupled base-emitter connected transistors Q_2/Q'_2 cancels the Miller capacitance effect of the main amplifying transistors Q_1/Q'_1 and improves the amplifier bandwidth. The biasing of the Q_1/Q'_1 transistors is determined by the base voltage V_B/V'_B set by R_1/R'_1 and R_2/R'_2 biasing resistors and the emitter voltage V_E/V'_E dropped across degeneration resistors R_E/R'_E. The base current through the amplifying transistors Q_1/Q'_1 is determined by choosing proper size of NMOS MN_2/MN'_2 transistors which are derived by current mirroring from the bandgap reference current.

The PMOS transistor switch MP_1/MP'_1 is introduced in the design to enable the power down functionality. The gate terminal of MP_1/MP'_1 is drawn out as an input pin Pwr_Dwn. When the pin Pwr_Dwn is set to voltage 0 V, the PMOS is ON and the amplifier functions in the normal mode and when the pin Pwr_Dwn is set to voltage 1.8 V, the PMOS is OFF and the amplifier is turned OFF consuming small current in the range of nA (nanoAmpere). This functionality enables this amplifier to be used in low power application with Power Save mode which can be de-activated when amplifier function is to be suspended.

C. Matching circuit design

The impedances looking into the amplifier differential inputs and the amplifier differential outputs are observed on the smith chart tool from Agilent ADS. The conjugate matching circuit is determined for the input side with DC decoupling capacitors C_{in}/C'_{in} and the input return loss is enhanced by using the input inductors L_{in}/L'_{in}. The load

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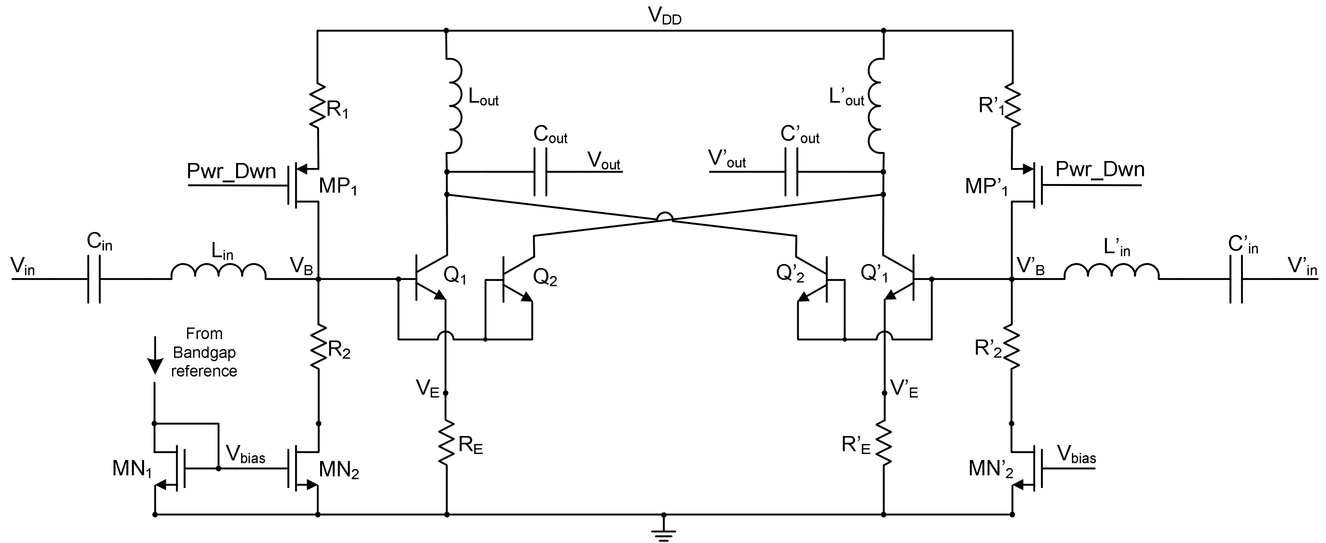

Fig. 1. Proposed amplifier circuit schematic

inductors L_{out}/L'_{out} and output capacitors C_{out}/C'_{out} values are determined for better gain and output impedance with conjugate matching. To optimize the die area, the load inductors L_{out}/L'_{out} is chosen as the differential inductor with center tap connected to the VDD supply.

III. EXPERIMENTAL RESULTS

The proposed amplifier is fabricated in a 0.18 µm SiGe BiCMOS technology from Tower-Jazz Semiconductor. The microphotograph of the fabricated design is shown in Fig. 2. The core area of the design is 0.38 mm x 0.34 mm and the overall area including the I/O pads is 0.68 mm x 0.6 mm. The GSSG probes are included at the input and output for on-wafer measurement of the fully differential amplifier. The amplifier was measured using the Agilent E8364B Vector Network Analyzer (VNA) on the probe station.

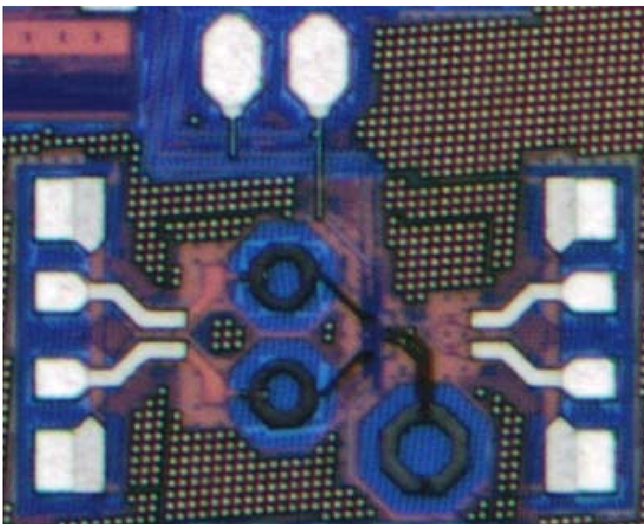
Fig. 2. Microphotograph

A. Gain compression plot

Simulation plot of output power against the variation of the input power is shown in Fig. 3. The 1-dB gain compression point referred to the input side is -1.6 dBm and the output compression point is about +4.0 dBm. This high

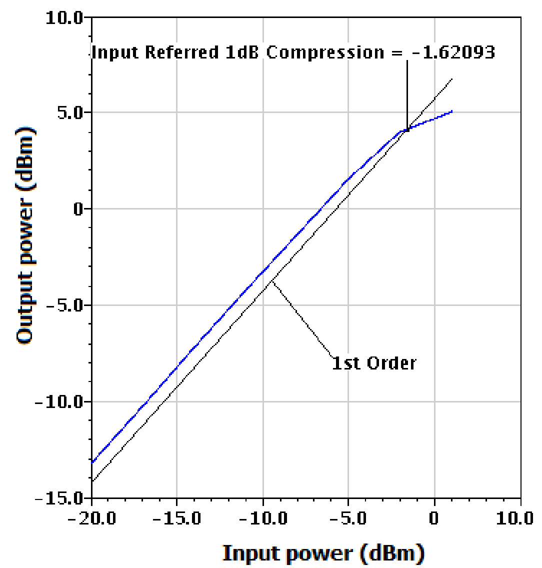

Fig. 3. Simulated gain compression point

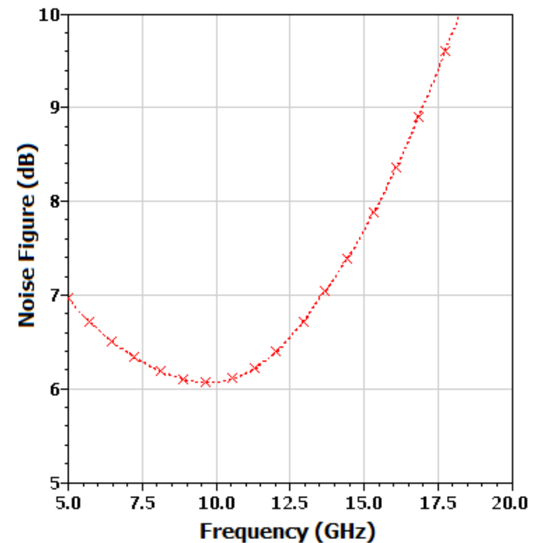

Fig. 4. Simulated Noise Figure

amplifier linearity enables this amplifier to provide large output signal power consuming low DC power and improves the amplifier power conversion efficiency. This performance is a desirable quality of the proposed amplifier to be included in the transmitter chain.

B. Noise Figure plot

Simulated Noise Figure as shown in Fig. 4 for the proposed amplifier is within 6.1 dB to 7.5 dB for the interested frequency range. The smaller noise figure ensures that this amplifier can be included in the receiver chain with minimum noise contribution to the overall system.

C. S-parameter plots

S-parameter measurement is compared with the simulation plots and the results suggests that the measured peak gain is closer to simulation while the bandwidth is narrower in measurement as shown in Fig. 5 (a). The input and output matching shown in Fig. 5 (b) and Fig. 5 (c) is improved in measurement results for the interested frequency range as compared to simulation results.

D. Stability Factors

The stability factors shown in Fig. 6 confirms that the factor Kf > 1.0 and B1f > 0. The amplifier stability factors that are determined from the measurement S-parameters indicates that the amplifier is unconditionally stable over the operating frequency range.

E. Power Down functionality

The proposed amplifier has a provision to conserve the DC power when it is not operational using the Power Down functionality. If the voltage at the circuit nodes *Pwr_Dwn* shown in the circuit schematic of Fig. 1 is set to 1.8 V, the PMOS MP_1/MP'_1 is OFF which prevents both the base bias current and the base to emitter voltage dropped across R_2/R'_2 resistors of the amplifier transistors Q_1/Q'_1. The S-parameter measurement plot with the power down functionality shown in Fig. 7 suggests that the amplifier gain (S21) is smaller along the RF path and is identical to the reverse isolation (S12). The

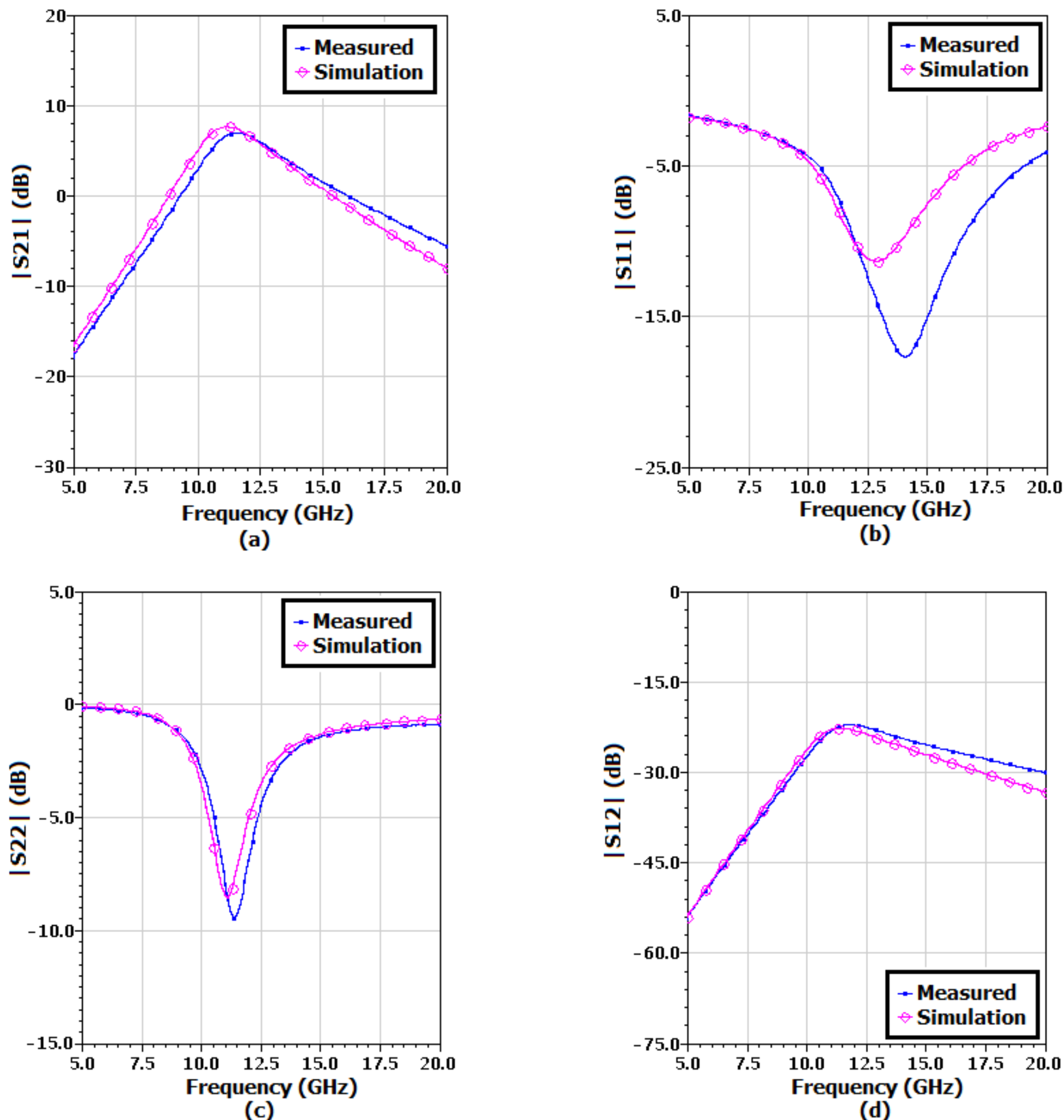

Fig. 5. Measured and simulated S-Parameters plot

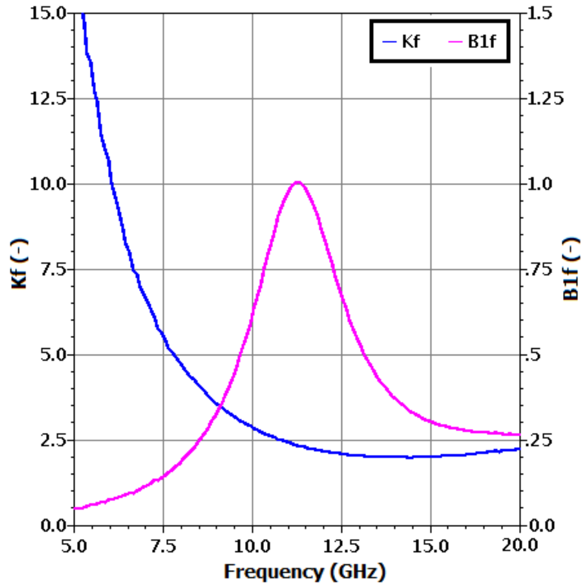

Fig. 6. Measured amplifier stability factors

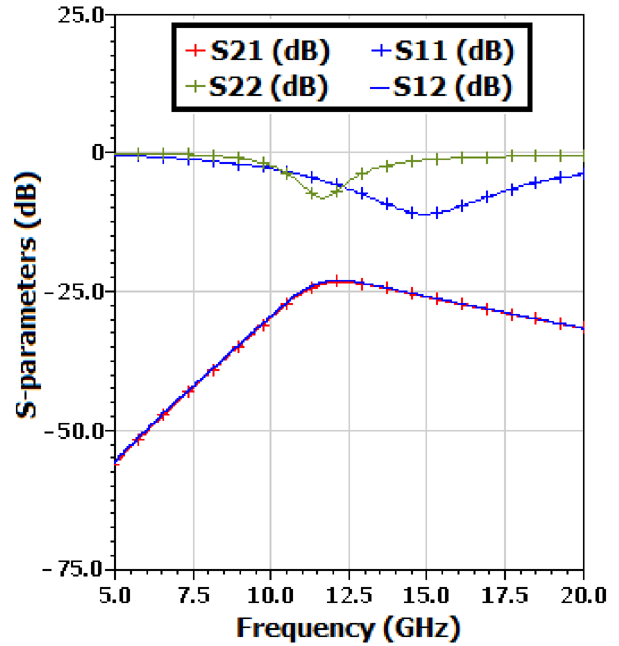

Fig. 7. Measured S-parameter plot with amplifier power down

input and output matching is not affected with the power down functionality and enables easier interface to the other blocks in the transceiver system. The power consumption measured during the power down functionality is about 34 µW as compared to 12 mW DC power consumption during normal amplifier operation and hence saves DC power using a digital input pin connected to nodes *Pwr_Dwn*. If 0 V is provided at the circuit nodes *Pwr_Dwn* then the amplifier functions with normal operation providing good performance.

The amplifier performance is summarized in Table I.

TABLE I
PERFORMANCE SUMMARY OF PROPOSED AMPLIFIER

Parameters	Measured results
Technology	0.18 µm SiGe BiCMOS
Peak Gain	7.2 dB
3-dB bandwidth	10.37 GHz to 12.43 GHz
Supply Voltage	1.8 V
Power consumption	12 mW
Output P1dB (Sim.)	+4.0 dBm
Input P1dB (Sim.)	-1.6 dBm
Noise Figure (Sim.)	6.1 dB to 7.5 dB
Core Area	0.38 x 0.34 mm^2
Die area with I/O pads	0.68 x 0.6 mm^2

IV. CONCLUSION

This paper presents a fixed gain high output power amplifier with performance determined by using on-wafer measurement. The amplifier is fully differential based on inductive load and resistive degeneration which is designed using a 0.18 µm SiGe BiCMOS process. The amplifier achieves power gain of 7.2 dB, 3-dB bandwidth of 2.06 GHz, operating frequency of 12 GHz, power consumption of 12 mW using 1.8 V supply voltage and the input referred 1-dB gain compression point higher than -1.6 dBm. The designed amplifier occupies a core area of 380 µm x 340 µm.

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